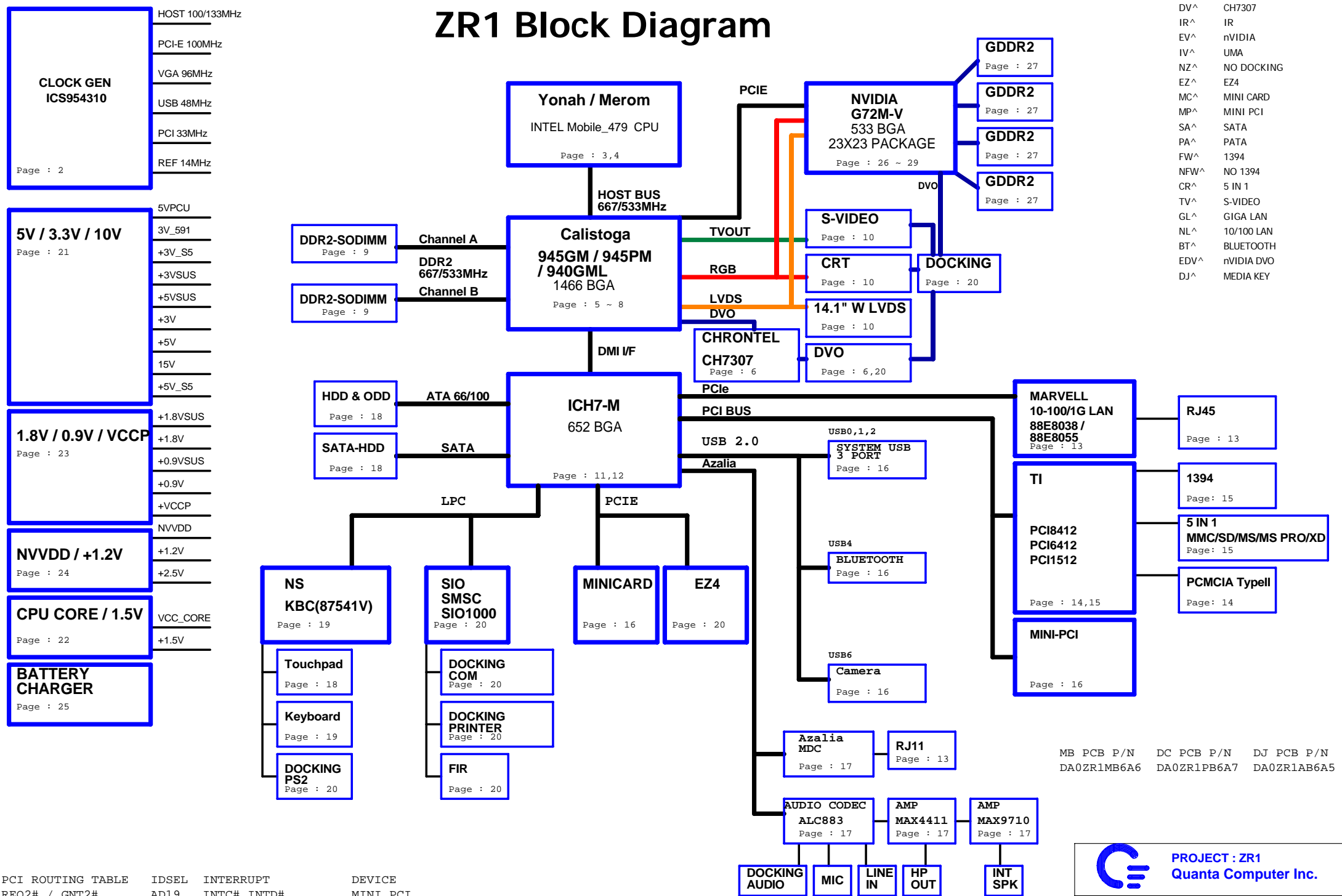



ZR1 Block Diagram



- DV^ CH7307
- IR^ IR
- EV^ nVIDIA
- IV^ UMA
- NZ^ NO DOCKING
- EZ^ EZ4
- MC^ MINI CARD
- MP^ MINI PCI
- SA^ SATA
- PA^ PATA
- FW^ 1394
- NFW^ NO 1394
- CR^ 5 IN 1
- TV^ S-VIDEO
- GL^ GIGA LAN
- NL^ 10/100 LAN
- BT^ BLUETOOTH
- EDV^ nVIDIA DVO
- DJ^ MEDIA KEY

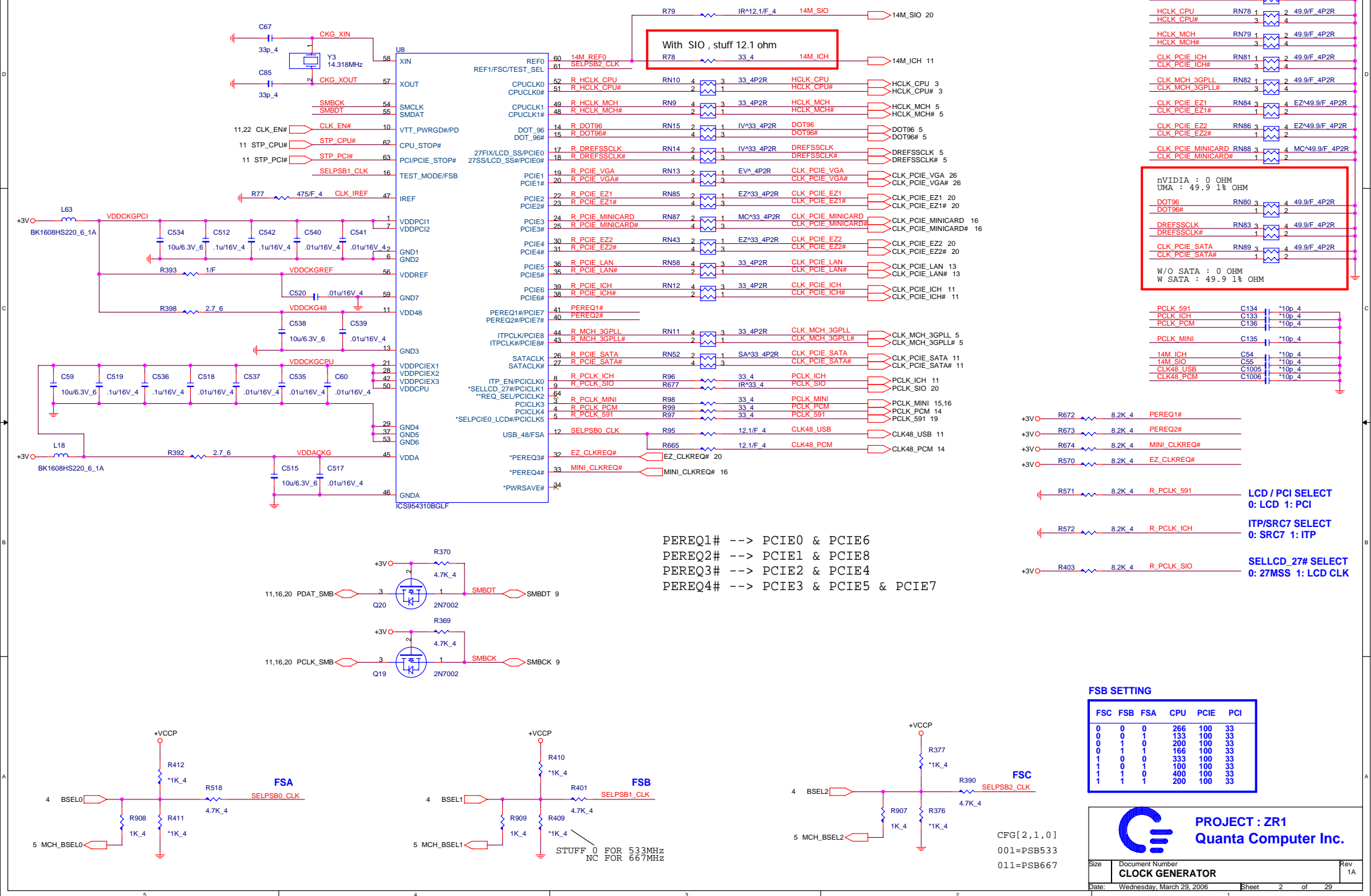
PCI ROUTING TABLE	IDSEL	INTERRUPT	DEVICE
REQ2# / GNT2#	AD19	INTC#,INTD#	MINI PCI
REQ0# / GNT0#	AD25	INTE#,INTF#,INTG#	TI XX12

MB PCB P/N DA0ZR1MB6A6 DC PCB P/N DA0ZR1PB6A7 DJ PCB P/N DA0ZR1AB6A5


PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A
Date: Wednesday, March 29, 2006	Sheet	1 of 29

CLOCK GENERATOR



FSB SETTING

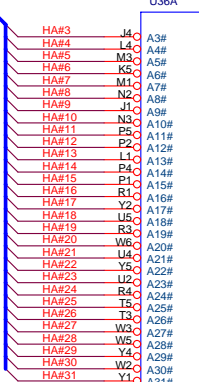
	FSC	FSB	FSA	CPU	PCIE	PCI
0	0	0	0	266	100	33
0	0	0	1	133	100	33
0	1	0	0	200	100	33
0	1	1	0	166	100	33
1	0	0	0	333	100	33
1	0	1	0	100	100	33
1	1	0	0	400	100	33
1	1	1	1	200	100	33



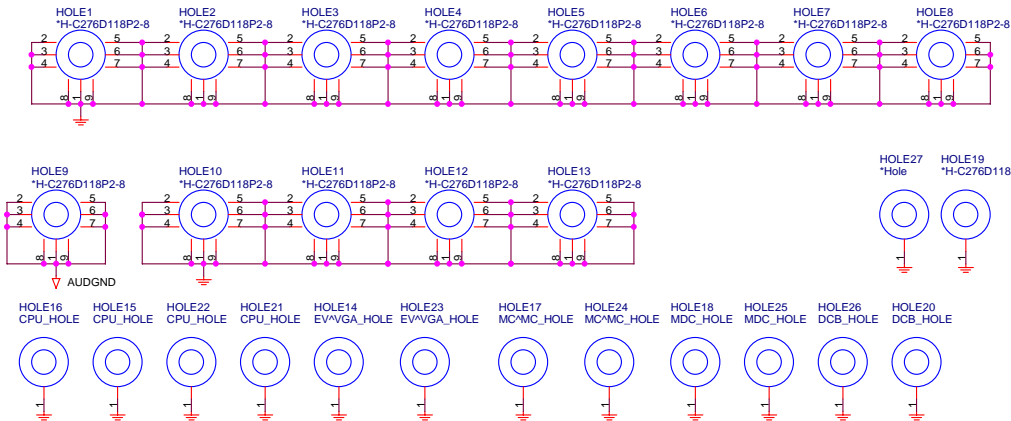
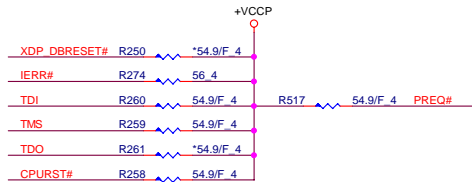
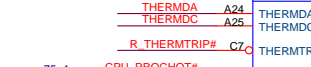
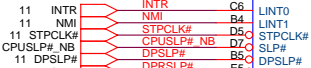
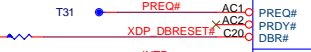
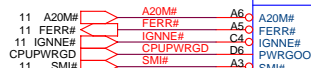
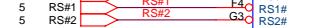
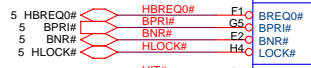
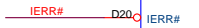
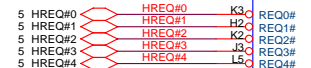
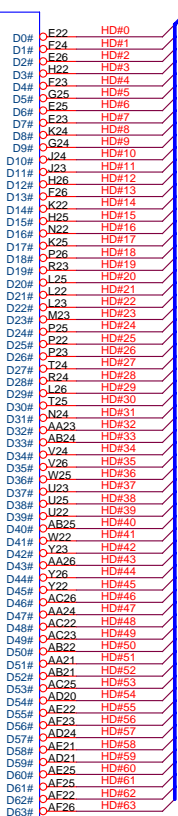
PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number CLOCK GENERATOR	Rev 1A
Date:	Wednesday, March 29, 2006	Sheet 2 of 29

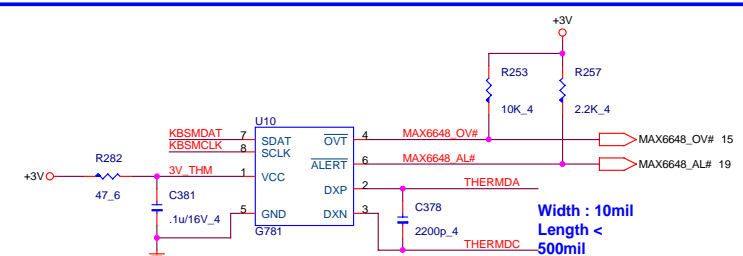
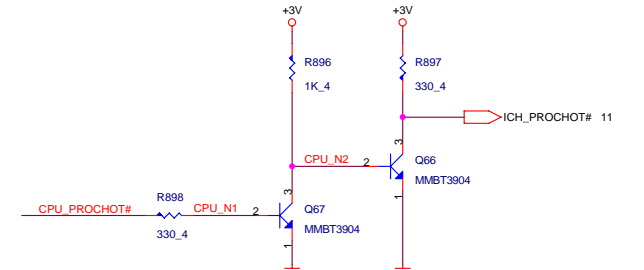
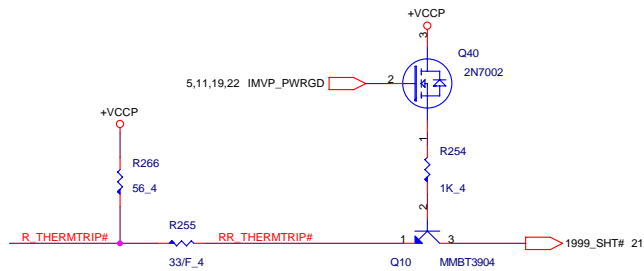
5 HA#[31..3] HA#[31..3]



1 OF 3



125 degree protection



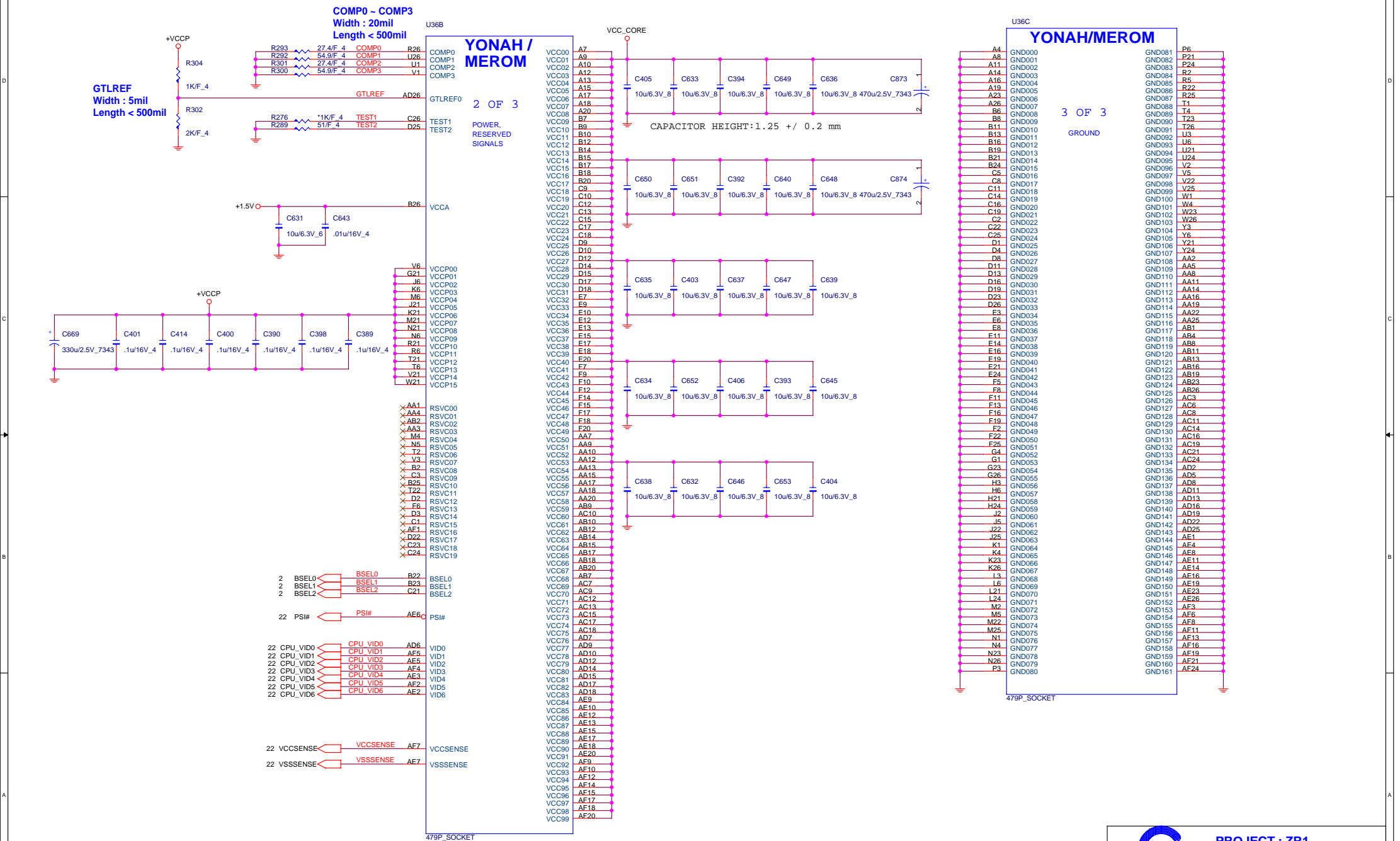
MAXIM 6657 : AL006657020
GMT G781 : AL000781101



PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number CPU (HOST)	Rev 1A
Date:	Wednesday, March 29, 2006	Sheet 3 of 29

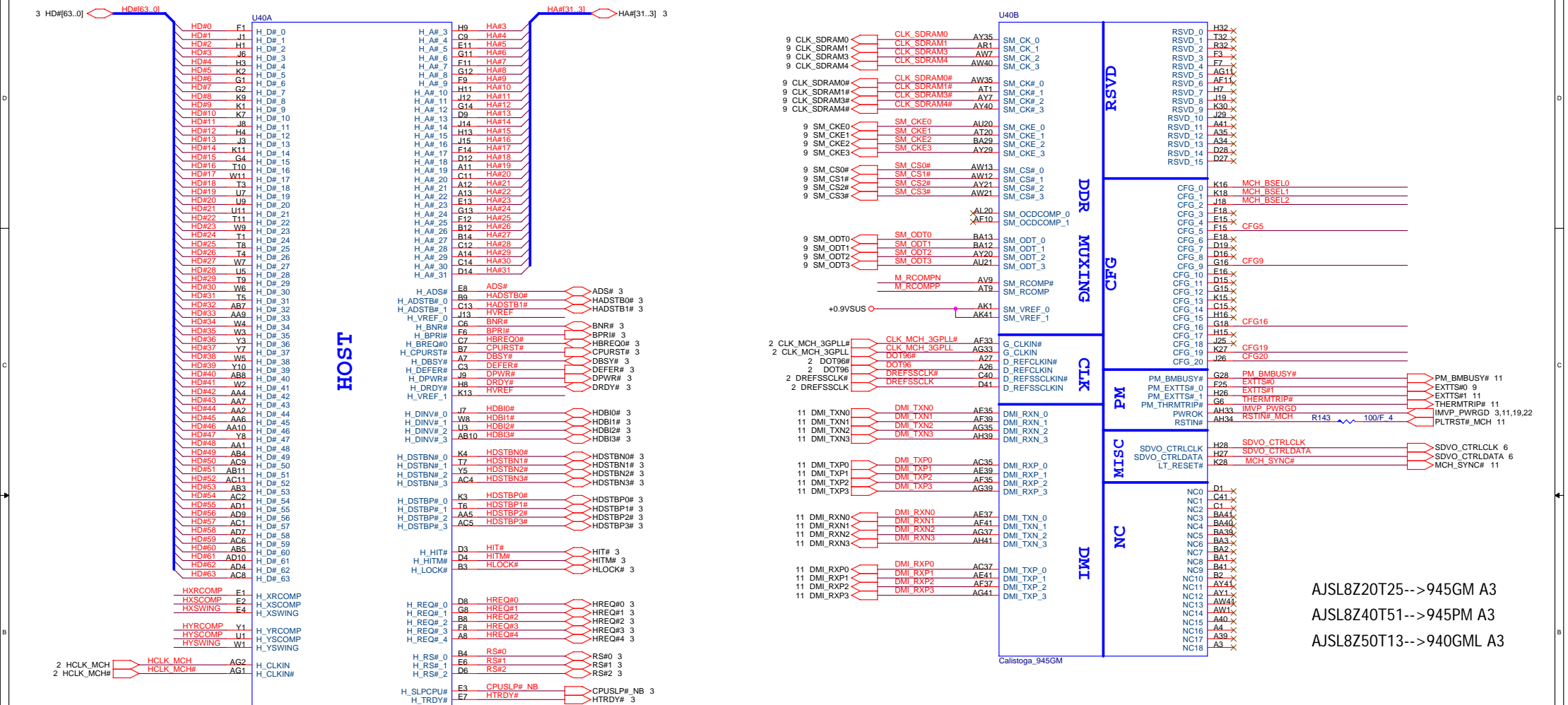
CPU



PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number CPU (POWER)	Rev 1A
Date:	Wednesday, March 29, 2006	Sheet 4 of 29

NB_945GM/PM/940GML



AJSL8Z40T51-->945PM A3

- 1.MCH_CFG_5 : Low = DMI X2, High=DMIX4
- 2.MCH_CFG_6 : Low = Moby Dick, High = Calistoga (Default)
- 3.MCH_CFG_7 : Low = RSVD, High = Mobile CPU
- 4.MCH_CFG_9 PCI Exp Graphics Lane: Low =Reverse lane ,High=Normal
- 5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
- 6.MCH_CFG_11: PSB 4x Enable : Low=Rsvd, High=Calistoga.
- 7.MCH_CFG_16 FSB Dymnic ODT: Low = Dynamic ODT Disabled,
High= Dynamic ODT Enabled.
- 8.MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
- 9.MCH_CFG_19 DMI LANE Reversal:Low=Normal,High=LANES Reversed.
- 10.MCH_CFG_20 PCIE Backward interoperability mode: Low=
only SDVO or PCIE x1 is operational (defaults) ,
High=SDVO and PCIE x1 are operation
simultaneously via the PEG port.

GMCH Strap pin

CFG5 R520 *2.2K 4

C5C9 B522 *2.2K 4

CFG16 R528 ... *2.2K 4

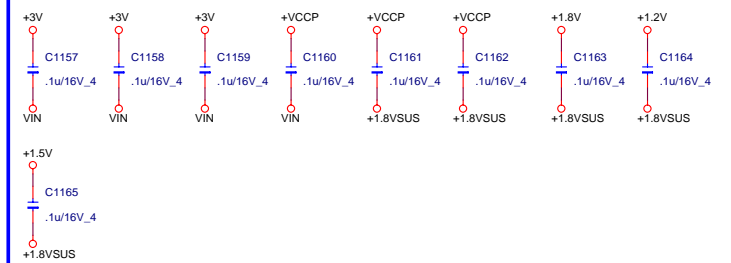
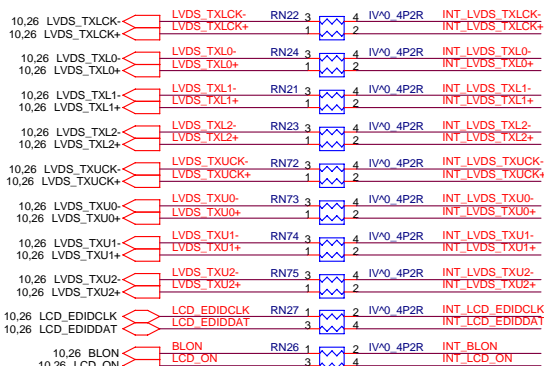
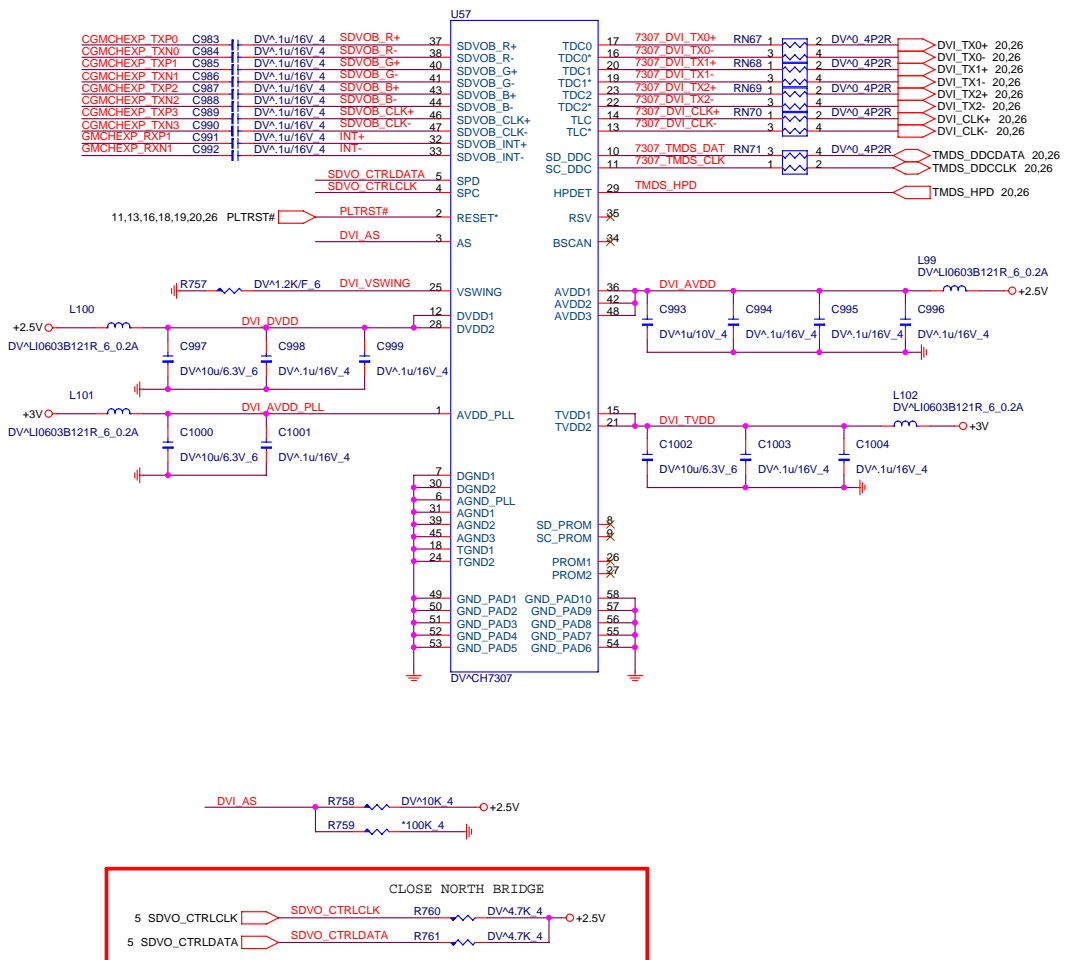
CFG19 R530 *1K 4



PROJECT : ZR1
Quanta Computer Inc.

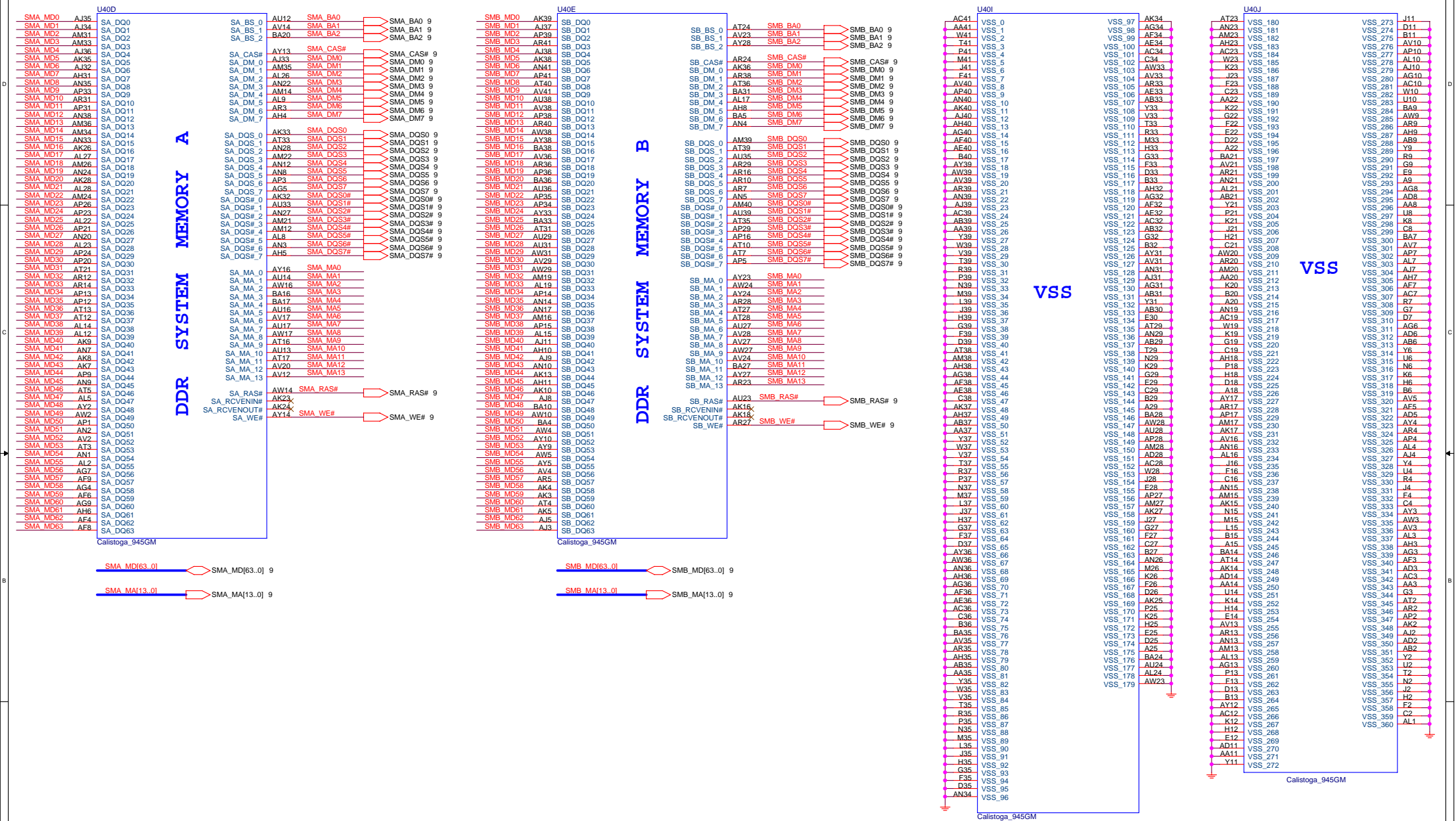
Size	Document Number GMCH (HOST / DMI)	Rev 1A
Date:	Wednesday, March 29, 2006	Sheet 5 of 29

DVO_CH7307



Size	Document Number GMCH (VGA)	Rev 1A
Date:	Wednesday, March 29, 2006	Sheet 6 of 29

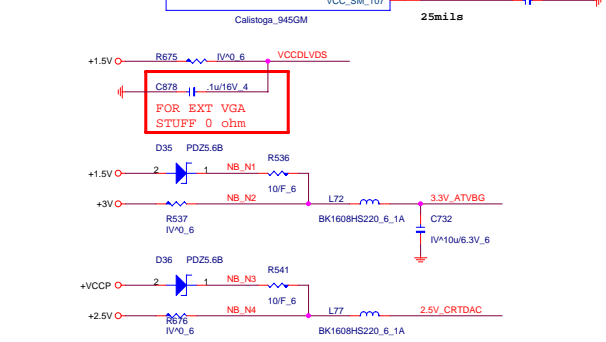
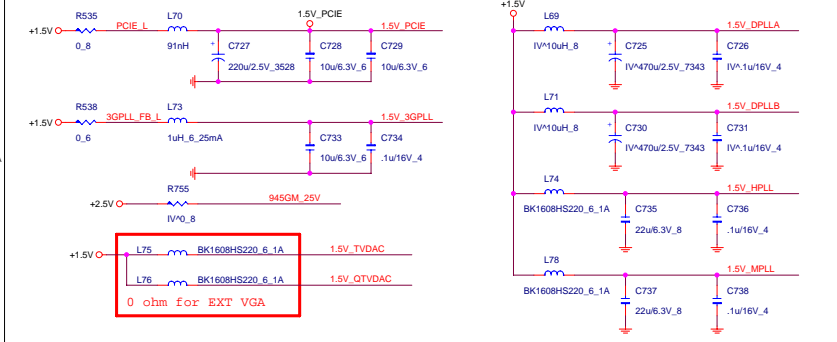
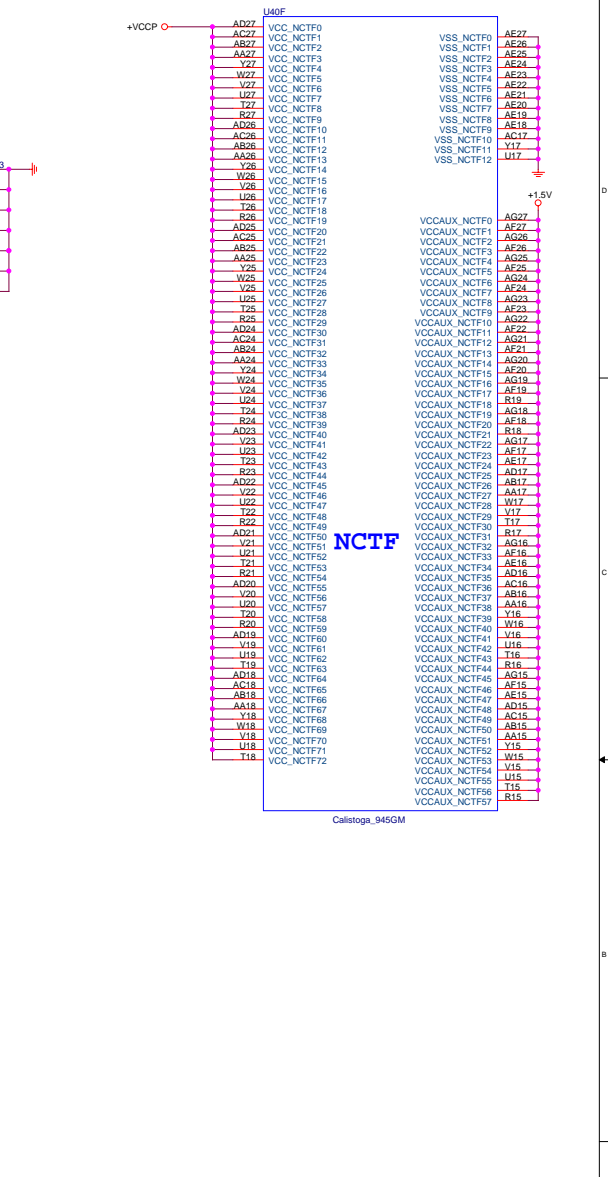
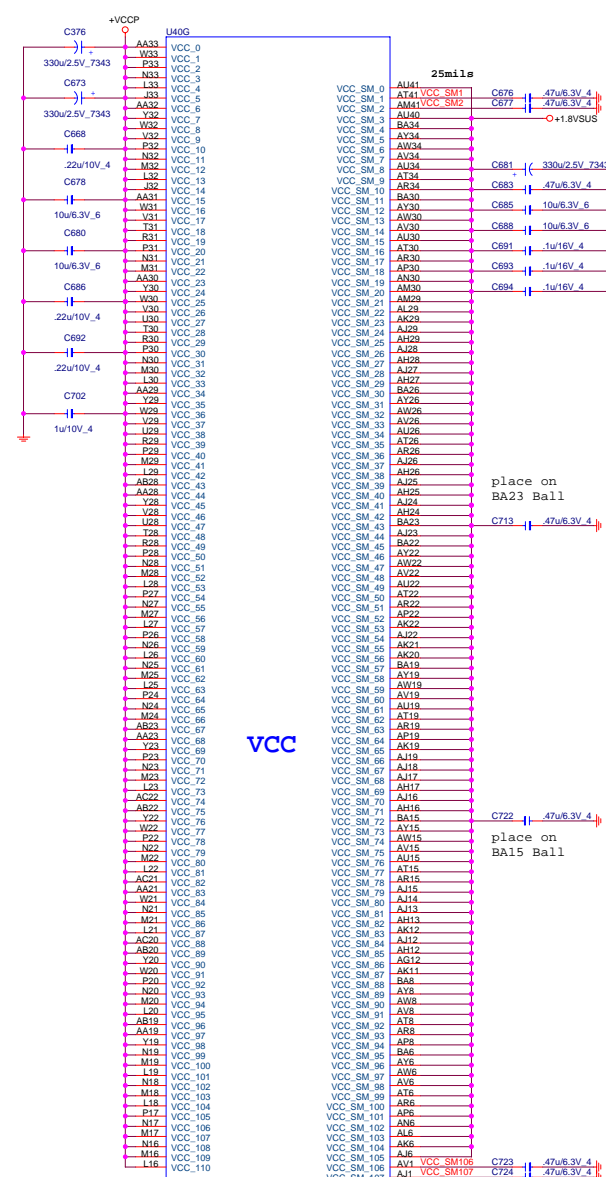
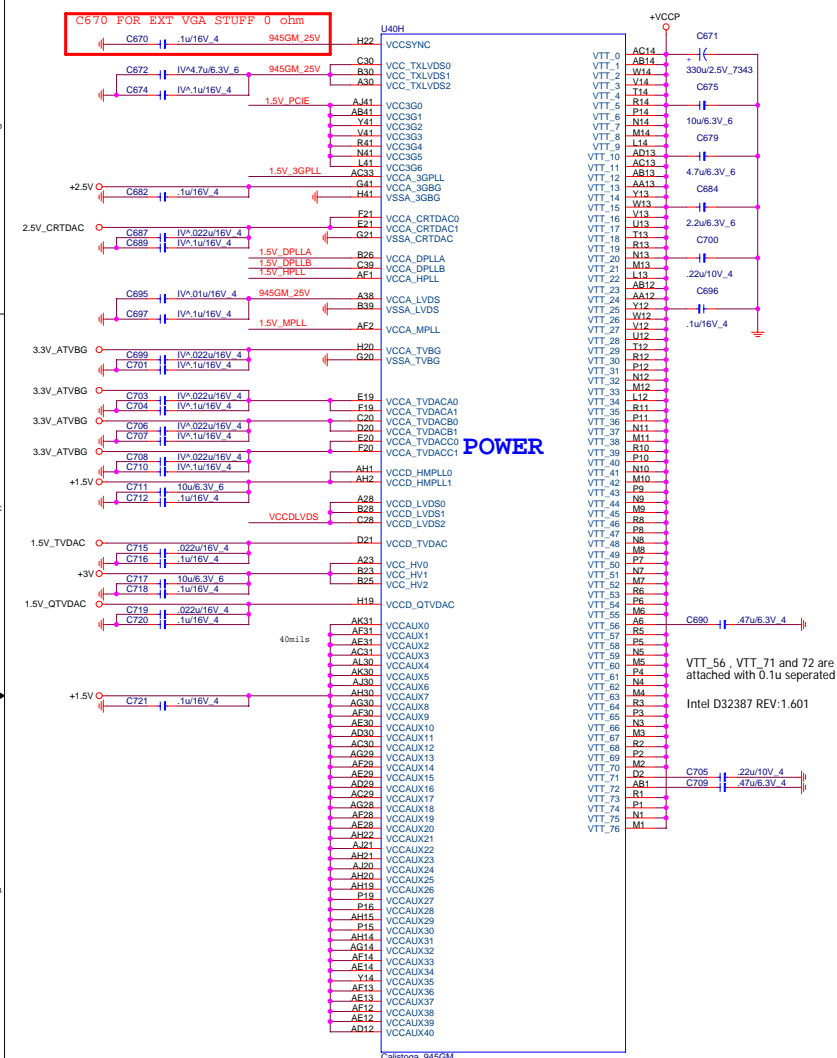
NB 945GM/PM/940GML



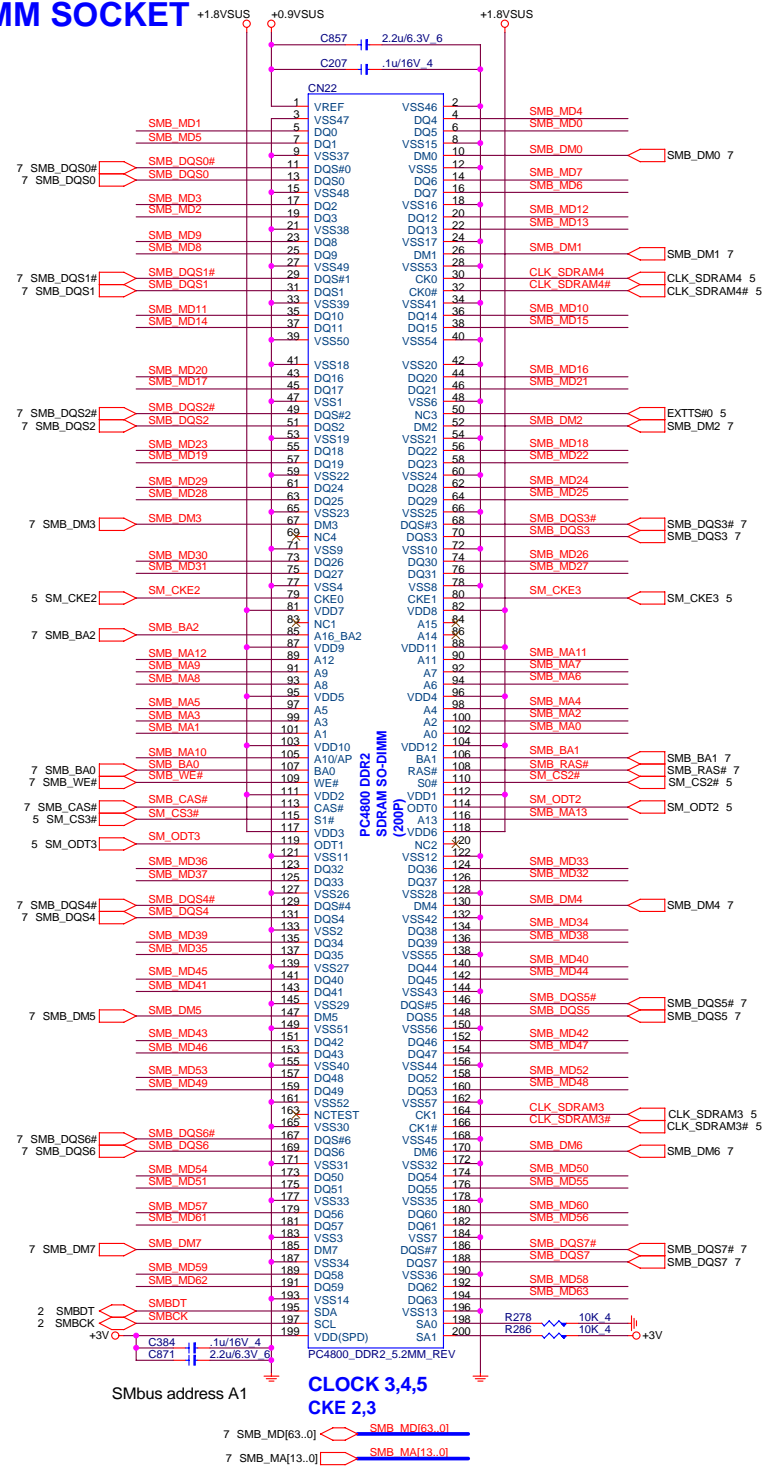
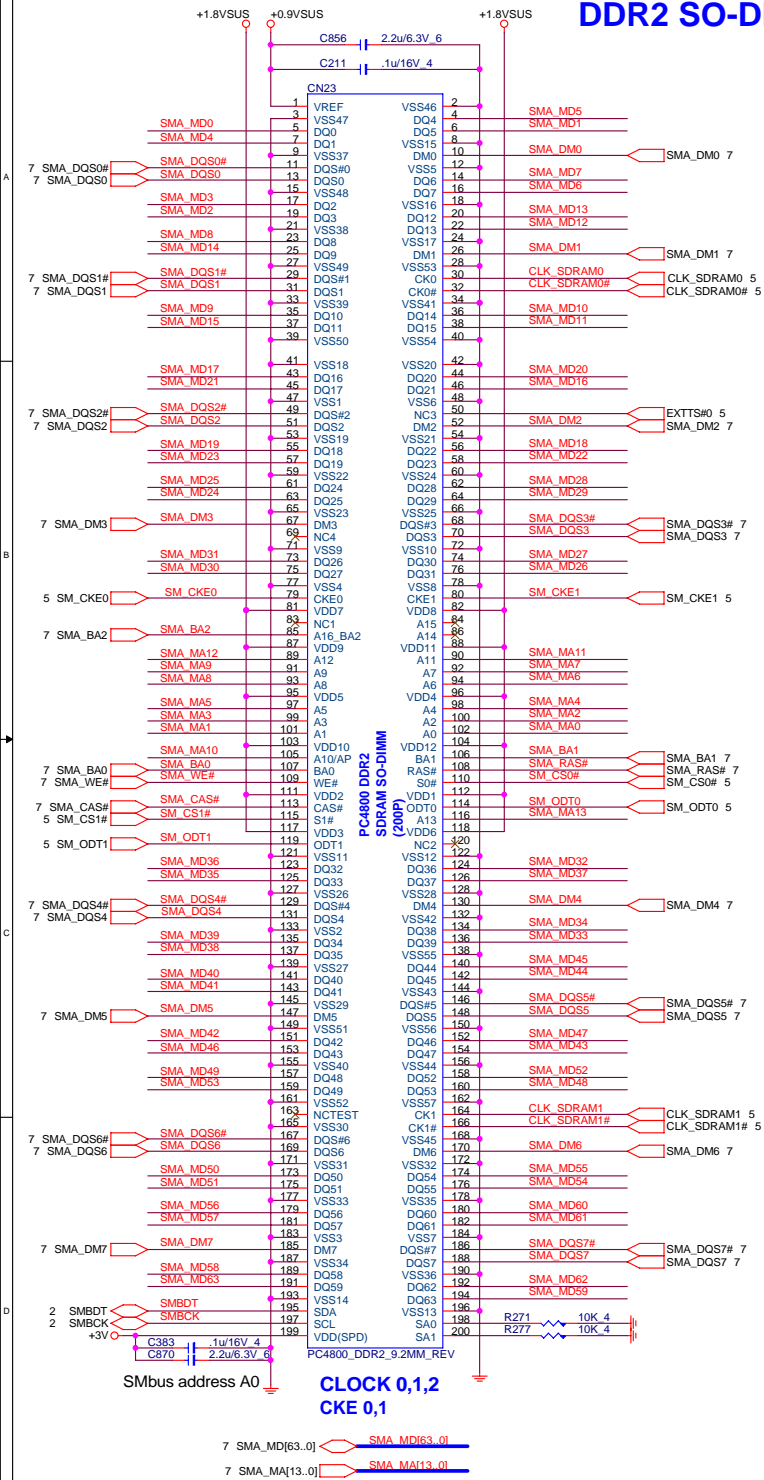
PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number GMCH (MEMORY)	Rev 1A
Date:	Wednesday, March 29, 2006	Sheet 7 of 29

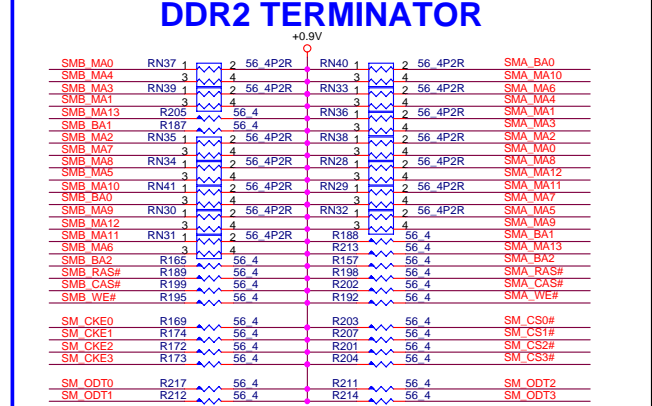
NB 945GM/PM/940GML

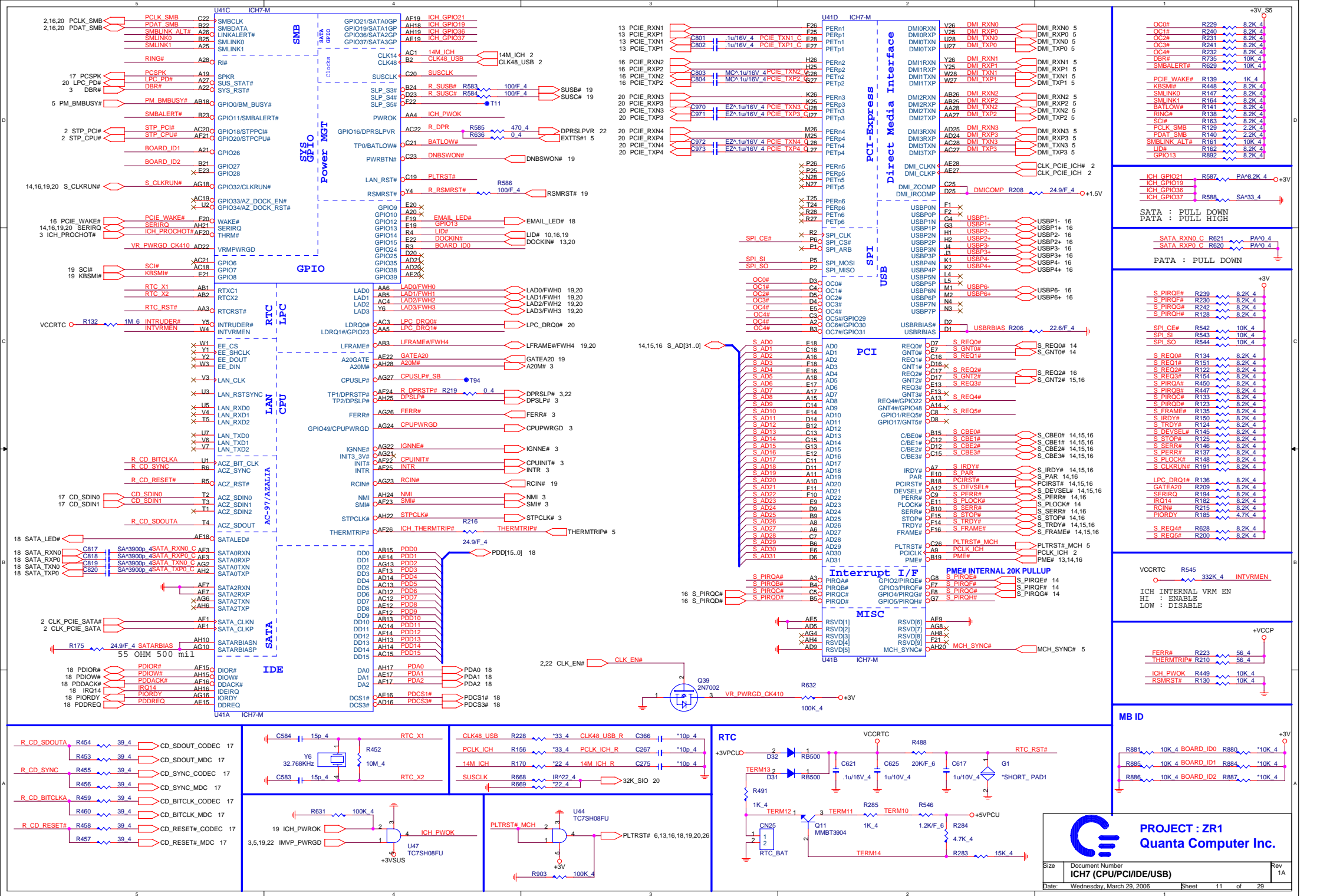


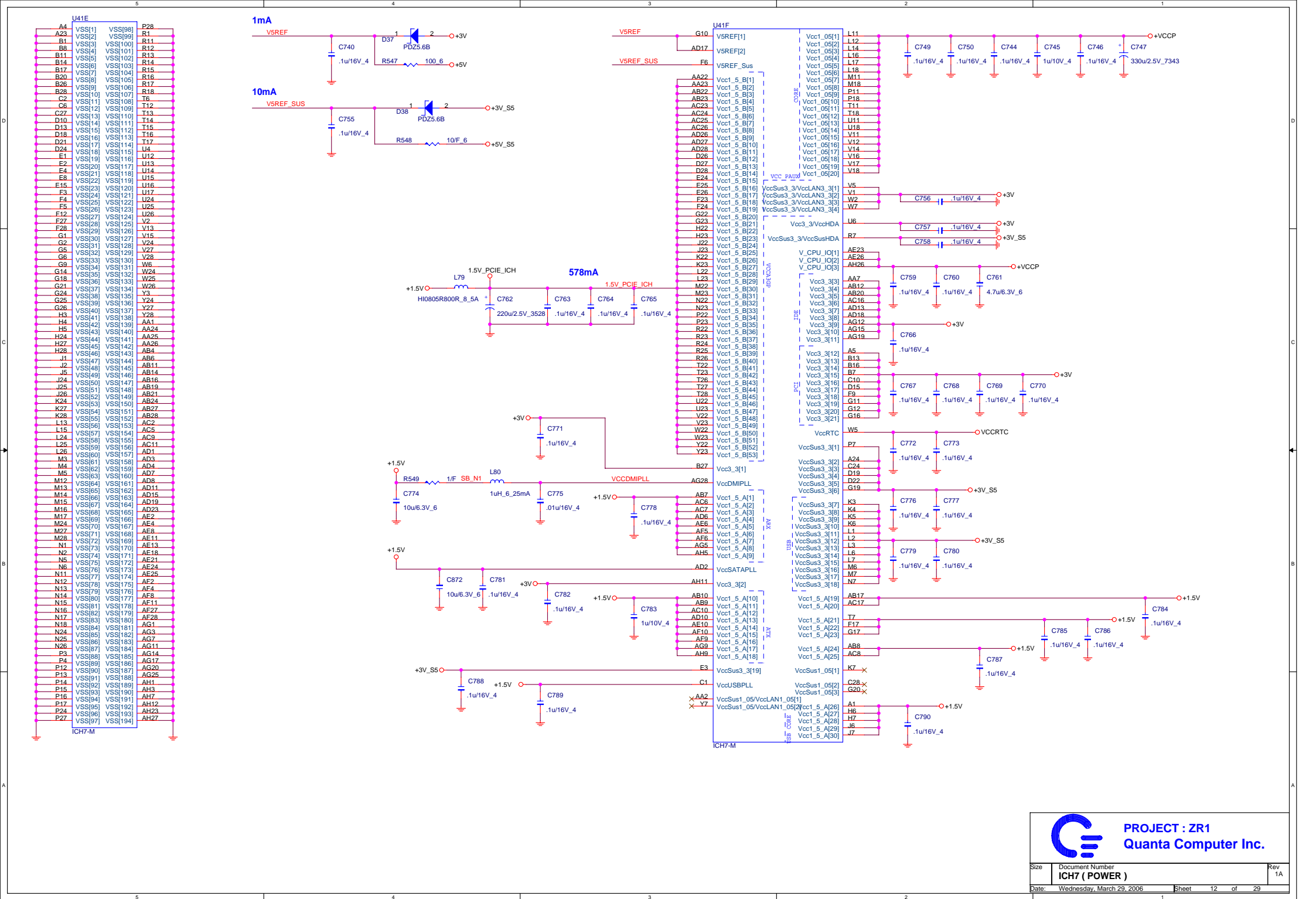
DDR2 SO-DIMM SOCKET



DDR2 TERMINATOR

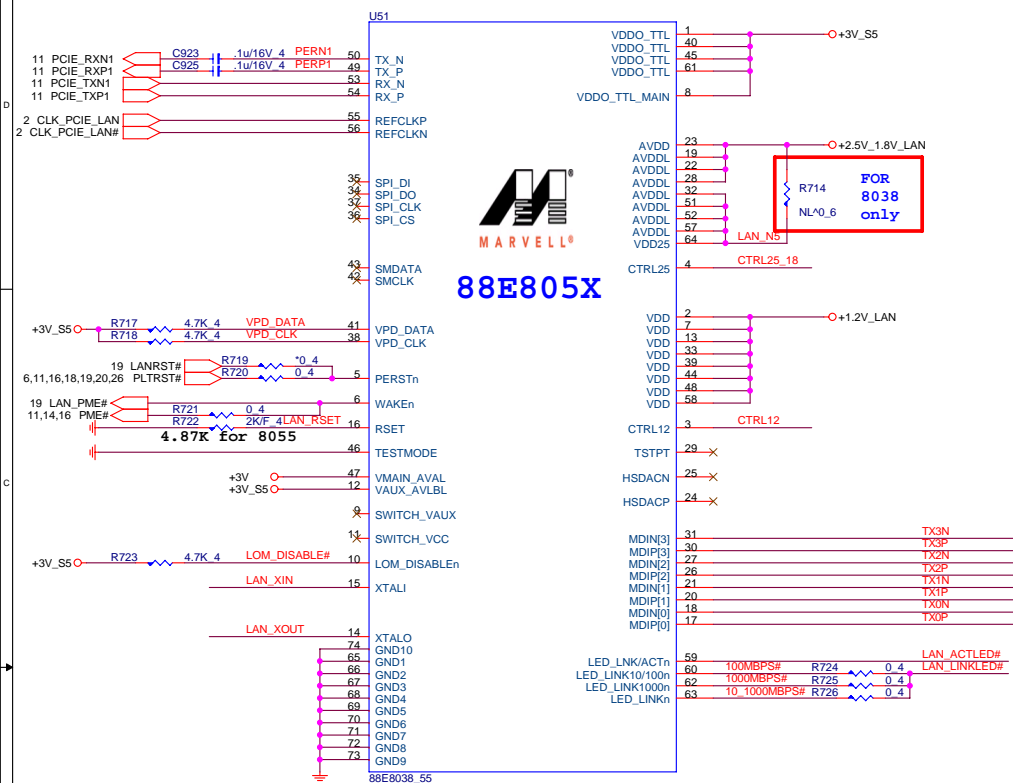




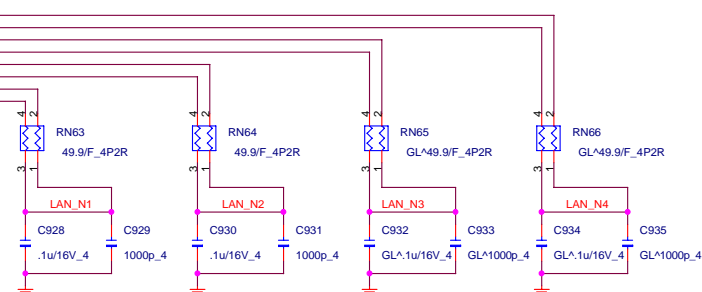
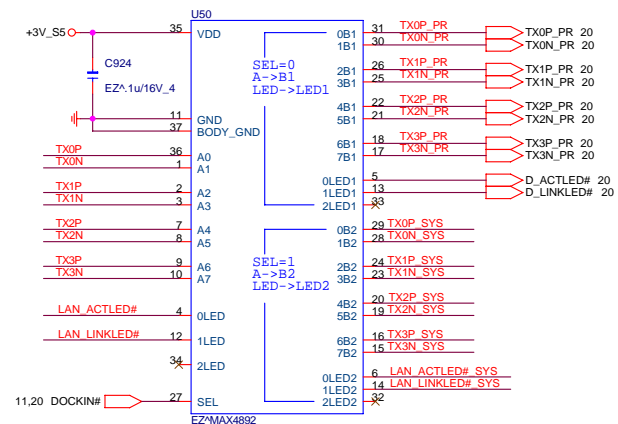
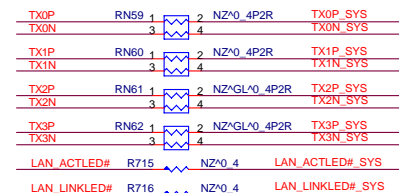
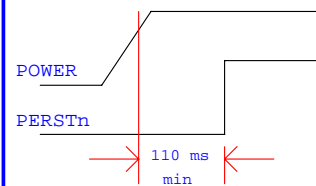


AJ080380000

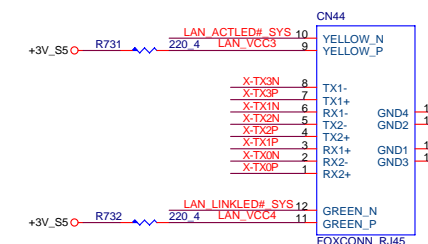
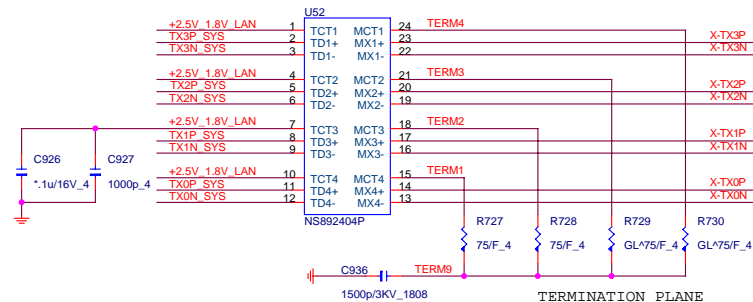
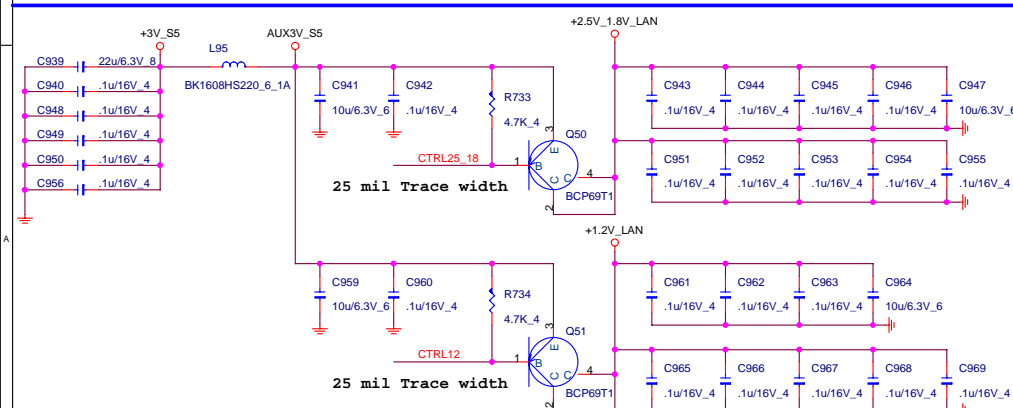
AJ080550011 A2



RESET TIMING



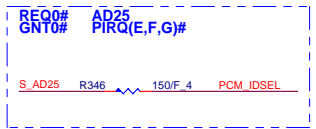
	BOTHHAND	FCE
10/100	DB0KN7LAN24	DBED2LLAN05
GiGa	DBKN1NLAN03	DB0ZH1LAN06



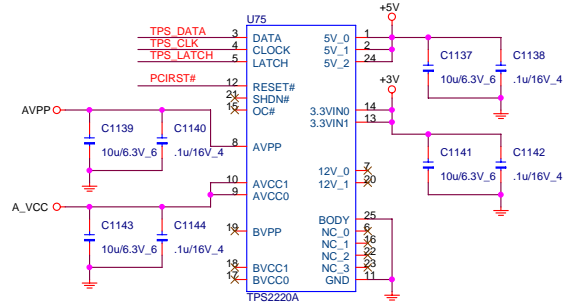
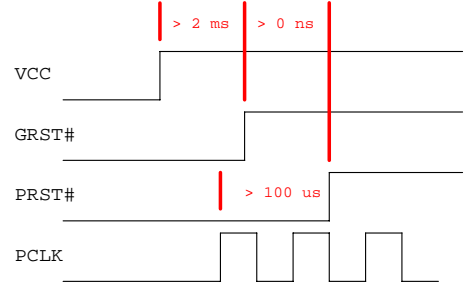
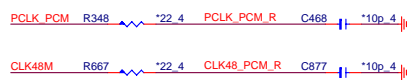
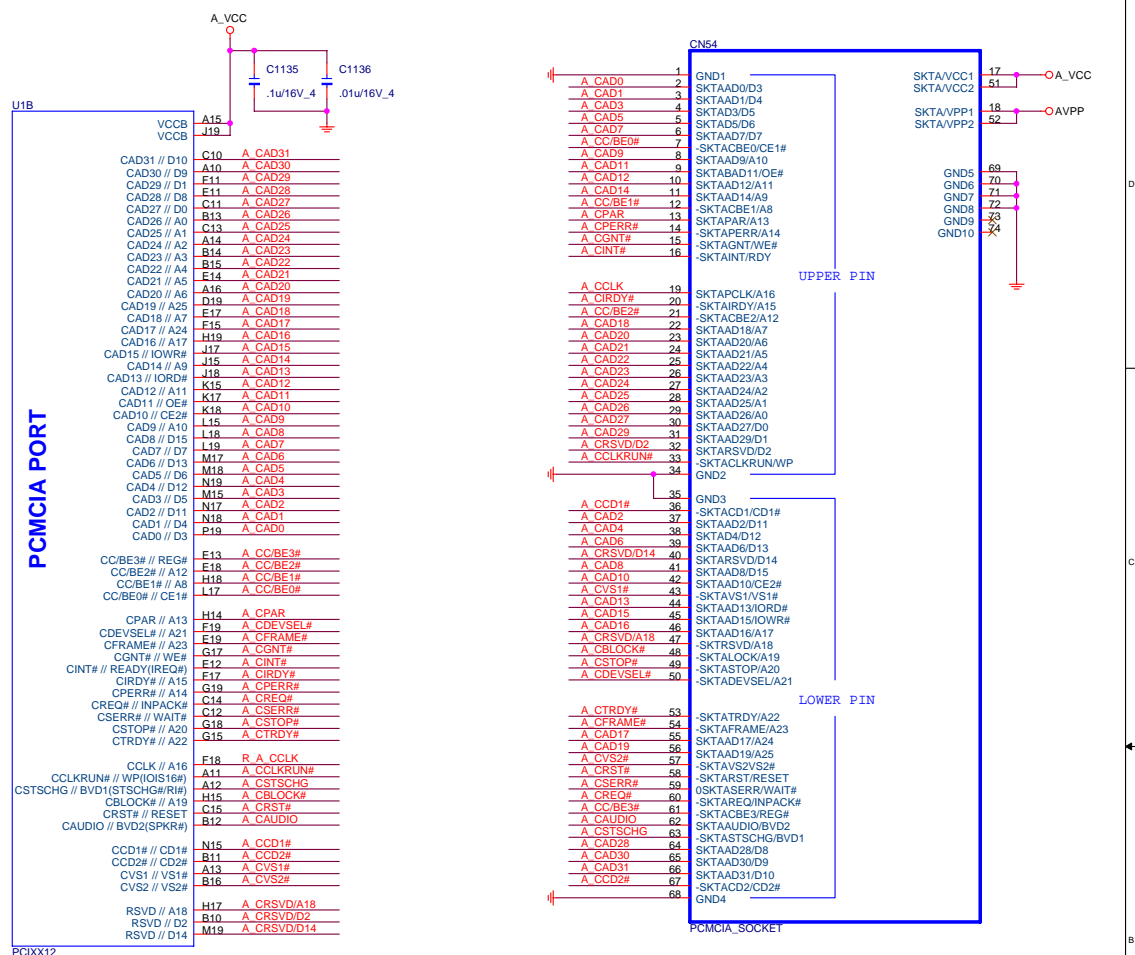
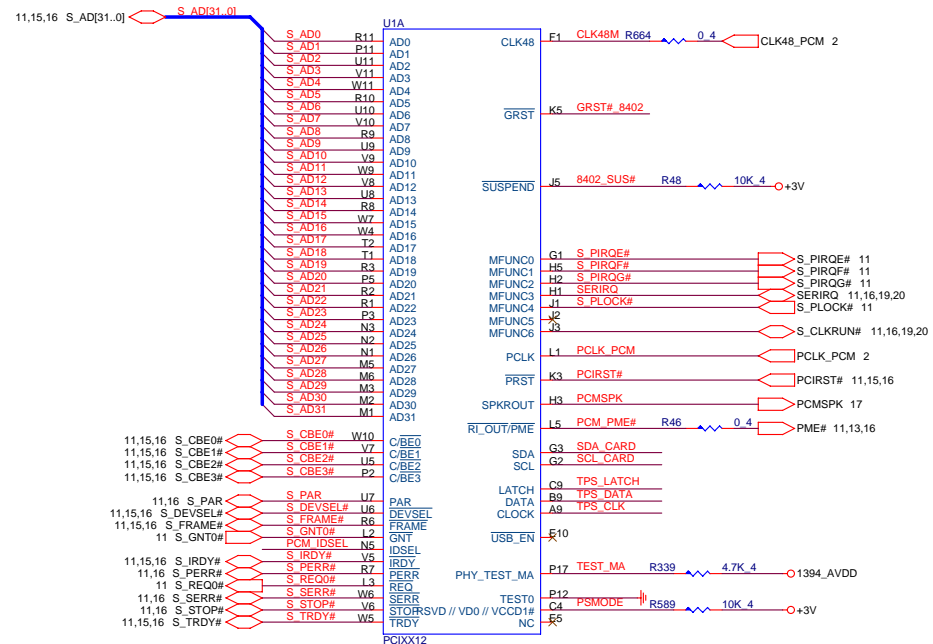
PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number LAN (MARVELL 8038/8055)	Rev 1A
Date:	Wednesday, March 29, 2006	Sheet 13 of 29

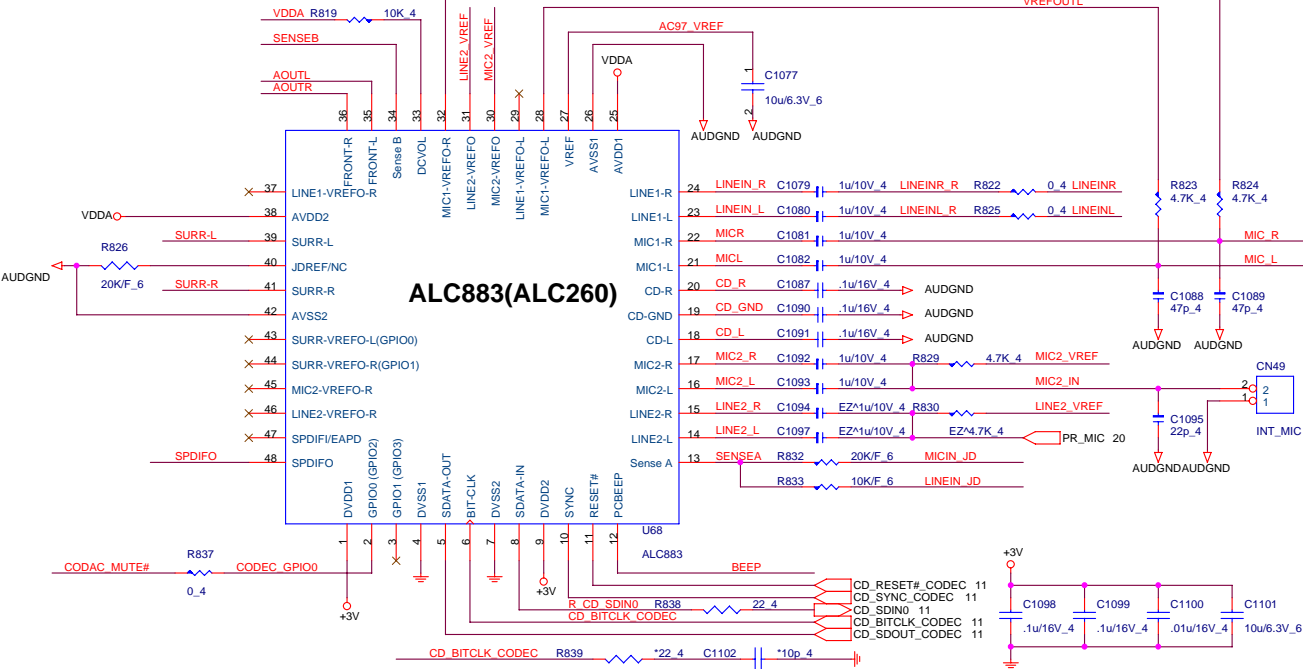
PCIXX12_PCMCIA



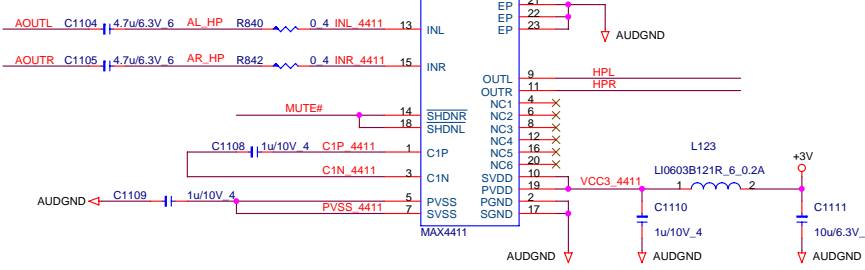
PCI8412 : AJ084120T08 PCMCIA / 1394 / 5 IN 1
PCI6412 : AL064120T04 PCMCIA / 5 IN 1
PCI1512 : AJ015120T02 PCMCIA



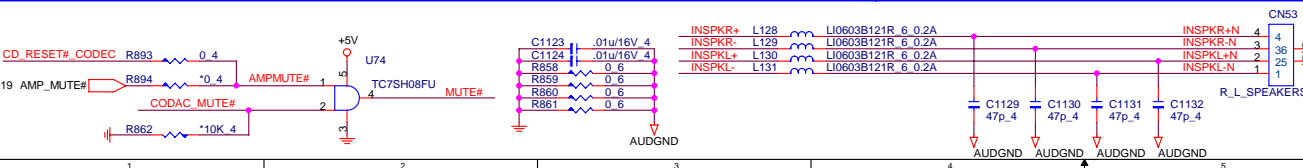
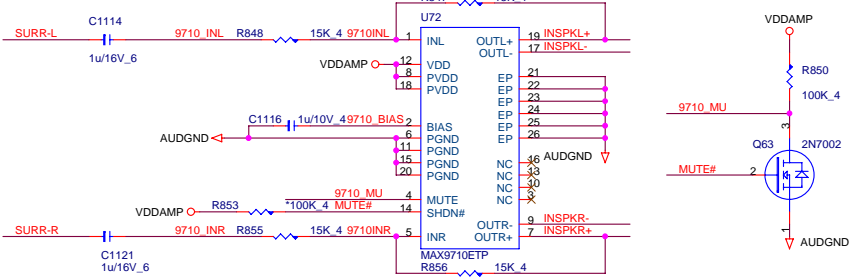
Audio Codec_ALC883



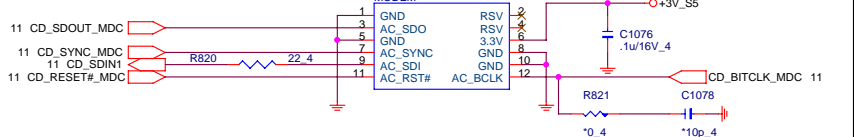
LINE OUT Amplifier



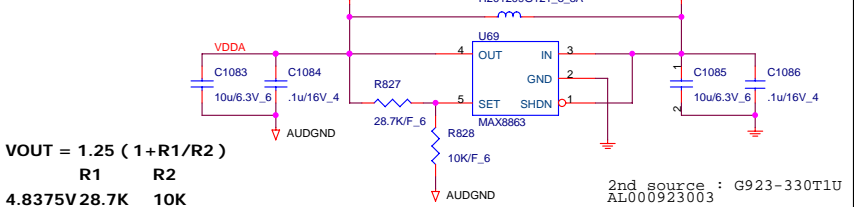
SPEAKER Amplifier



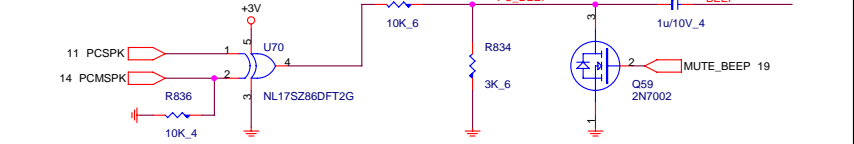
MDC



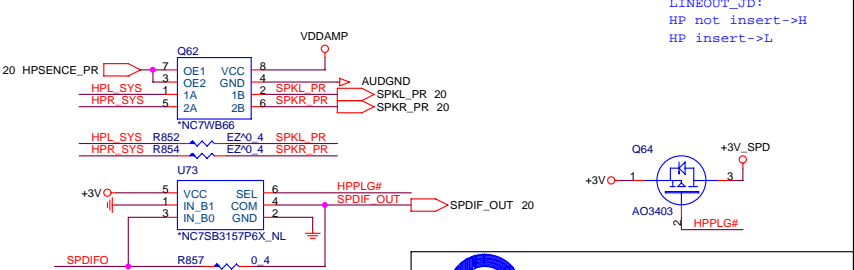
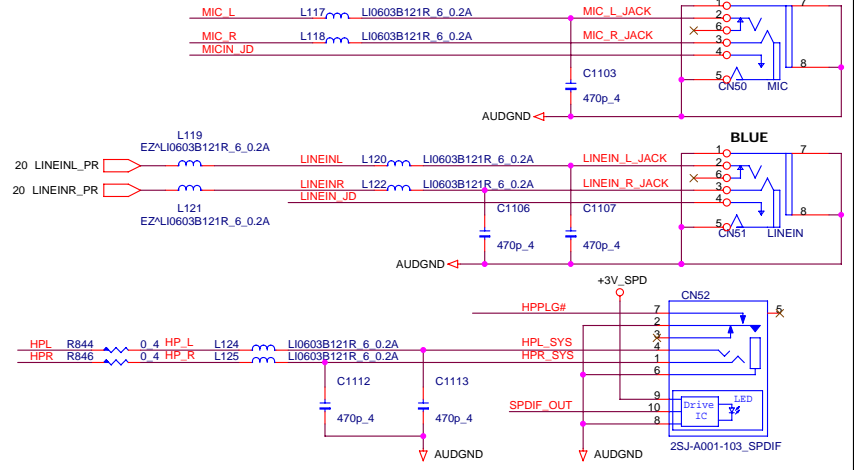
Audio Codec Power



BEEP



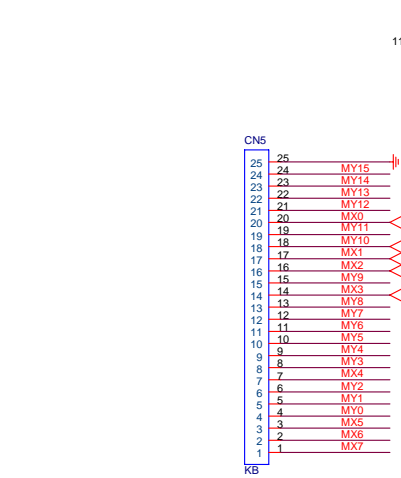
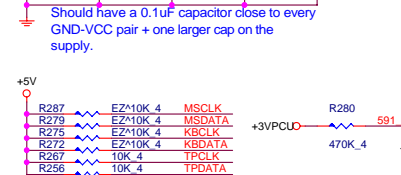
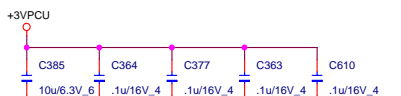
Audio Jack



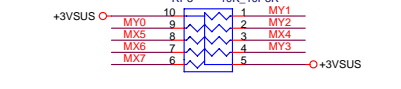
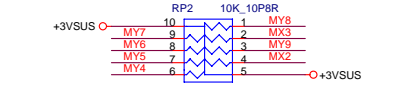
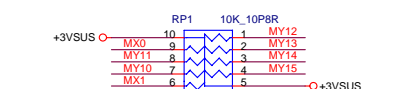
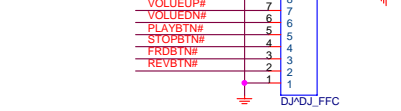
PROJECT : ZR1
Quanta Computer Inc.

K/B CONTROLLER

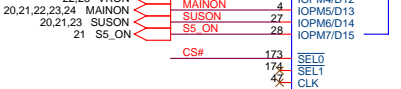
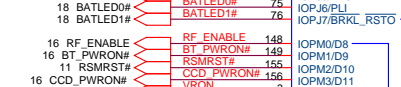
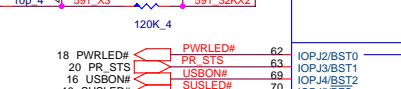
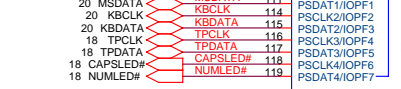
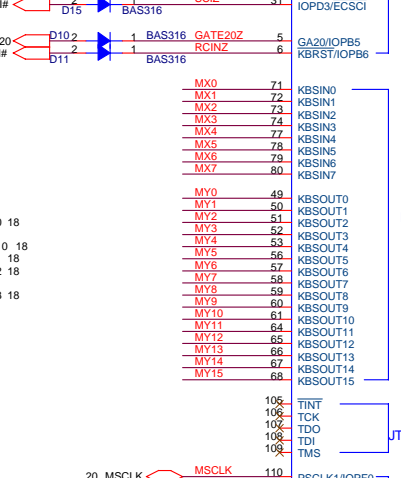
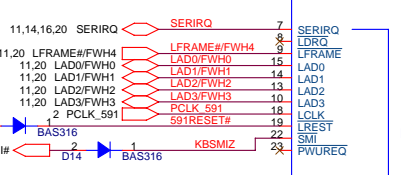
PCLK 591 R270 *22 4 PCLK 591 R C380 *10p 4



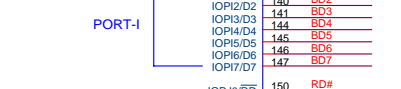
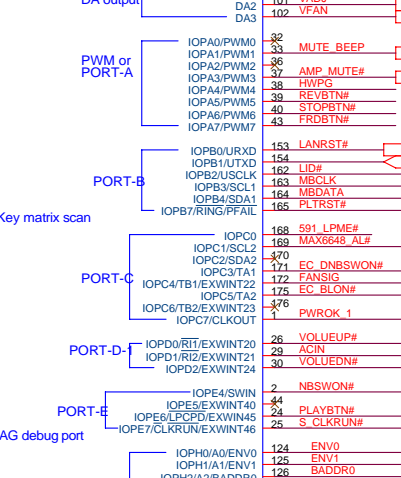
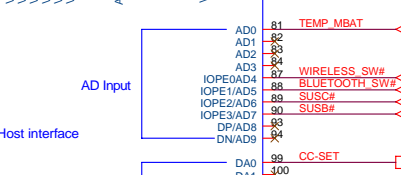
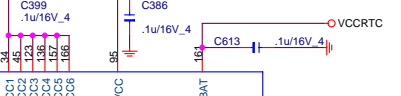
AUDIO DJ



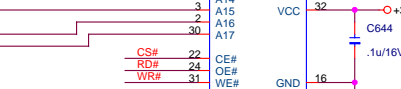
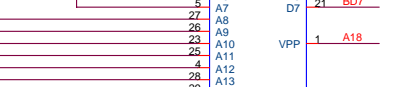
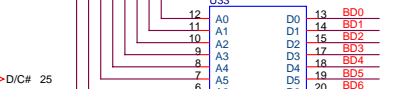
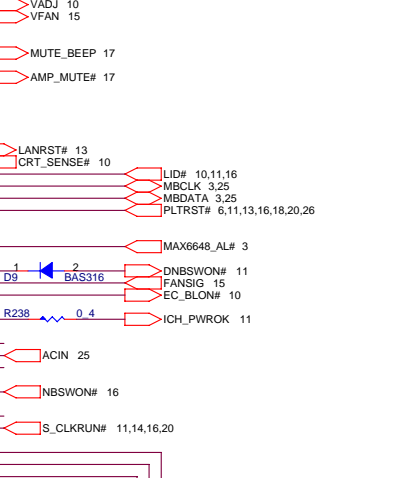
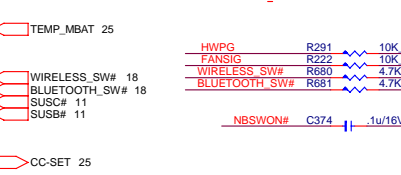
+3V +3VPCU C379 .1u/16V_4 C399 .1u/16V_4 C386 .1u/16V_4 C613 .1u/16V_4 VCCRTC



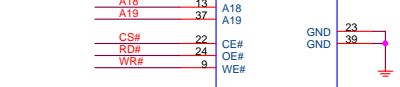
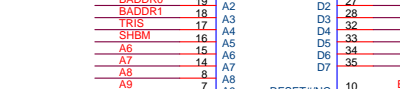
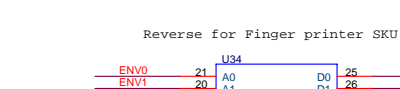
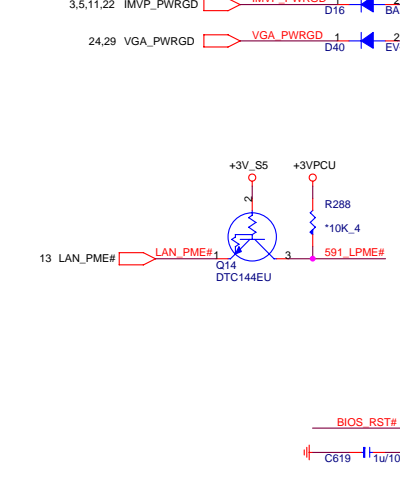
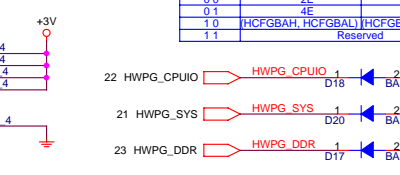
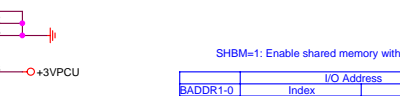
+3V +3VPCU C379 .1u/16V_4 C399 .1u/16V_4 C386 .1u/16V_4 C613 .1u/16V_4 VCCRTC



+3VPCU MBCLK R480 4.7K 4 MBDATA R481 4.7K 4 NBSWON# R245 10K 4

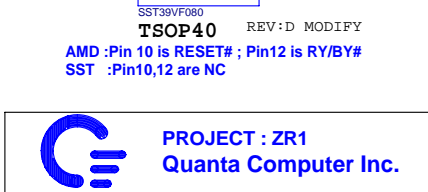
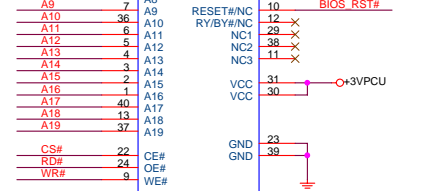
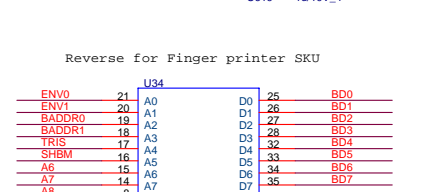
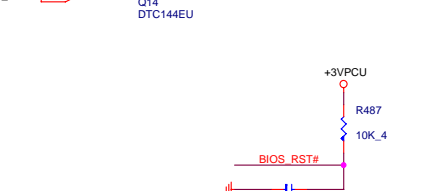
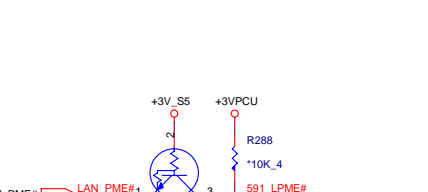
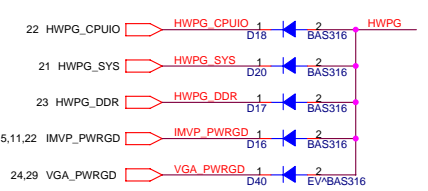



+3VPCU ENV1 R251 10K 4 SHBM R243 10K 4



SHBM=1: Enable shared memory with host BIOS

I/O Address	Index	Data
BADDR1-0	0.0	2E 2F
	0.1	4E 4F
	1.0	HCFGBAH, HCFGGBAL, HCFGGBAL+1
	1.1	Reserved

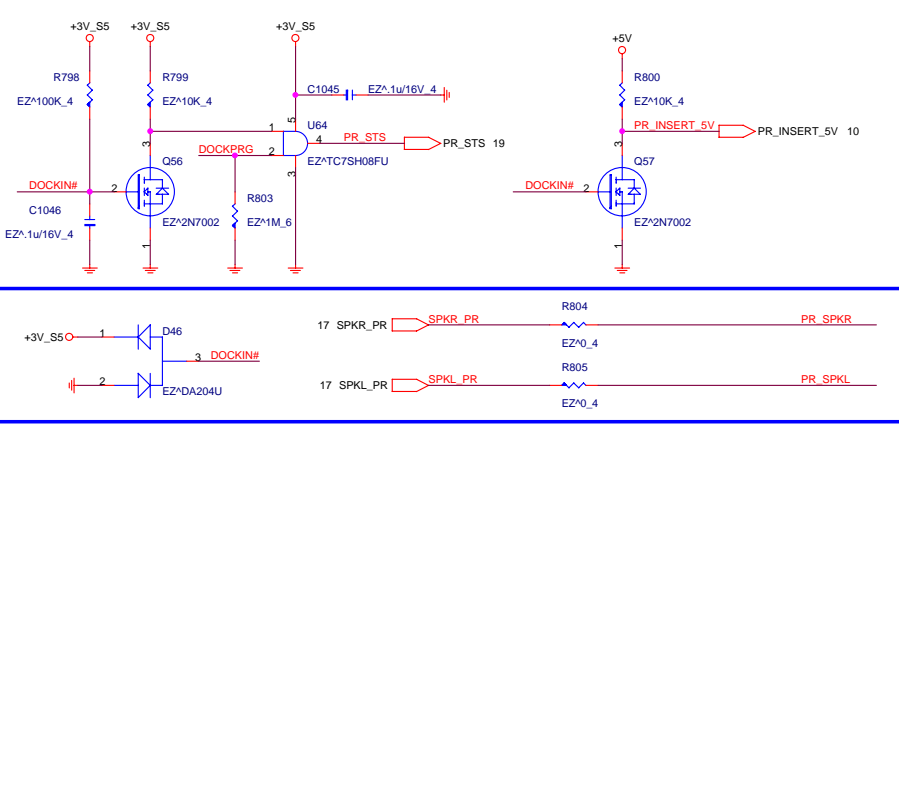
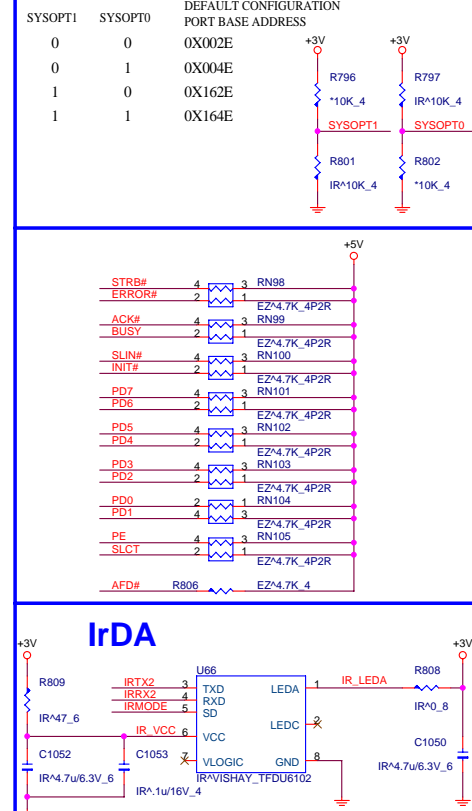
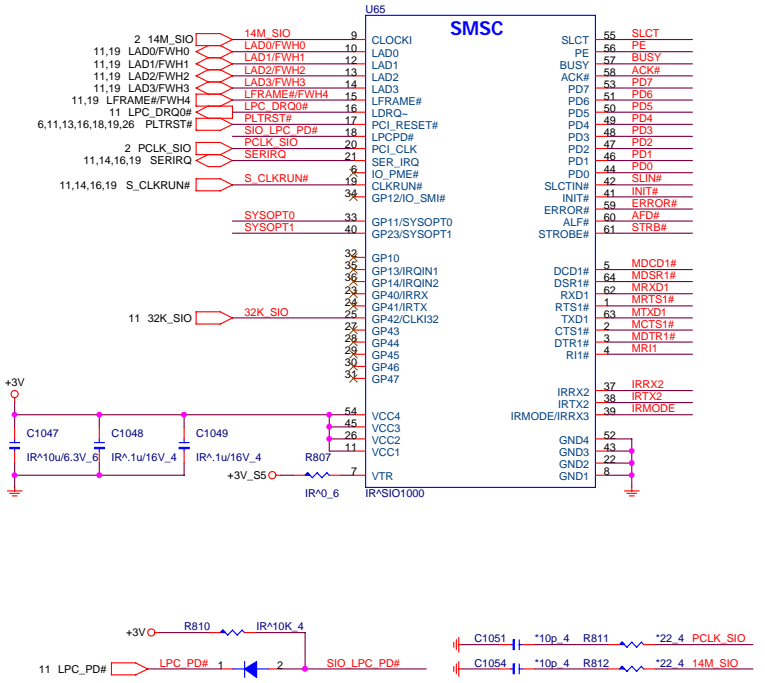




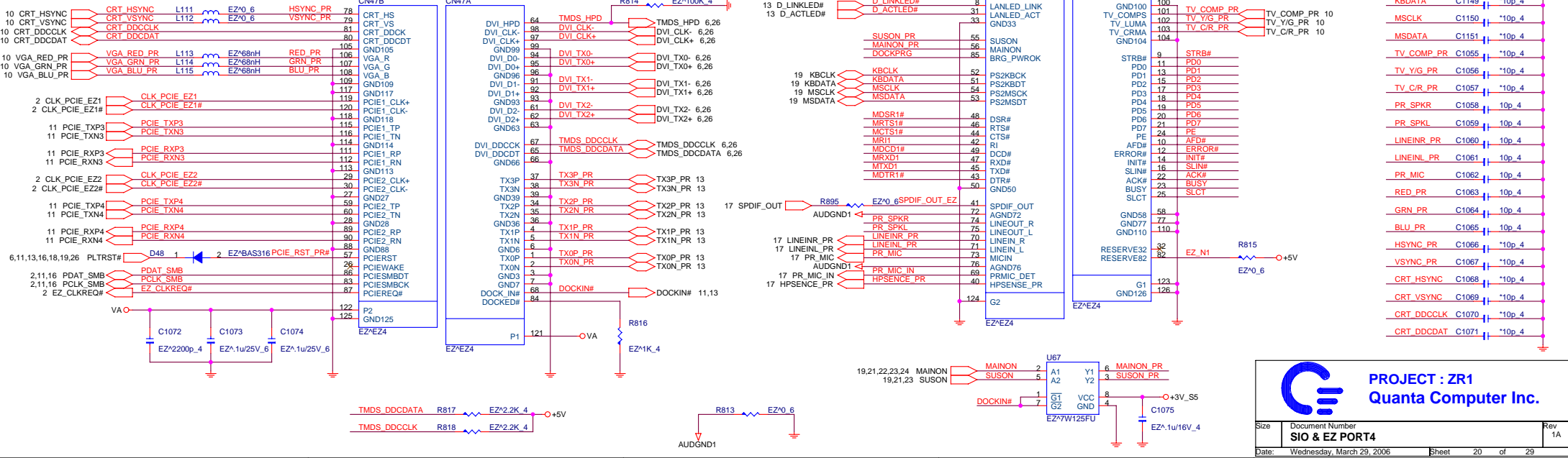
PROJECT : ZR1
Quanta Computer Inc.

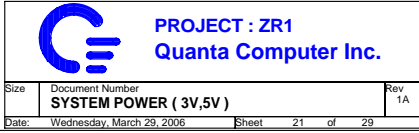
Size	Document Number	Rev
	EC PC87541V	1A
Date:	Wednesday, March 29, 2006	Sheet 19 of 29

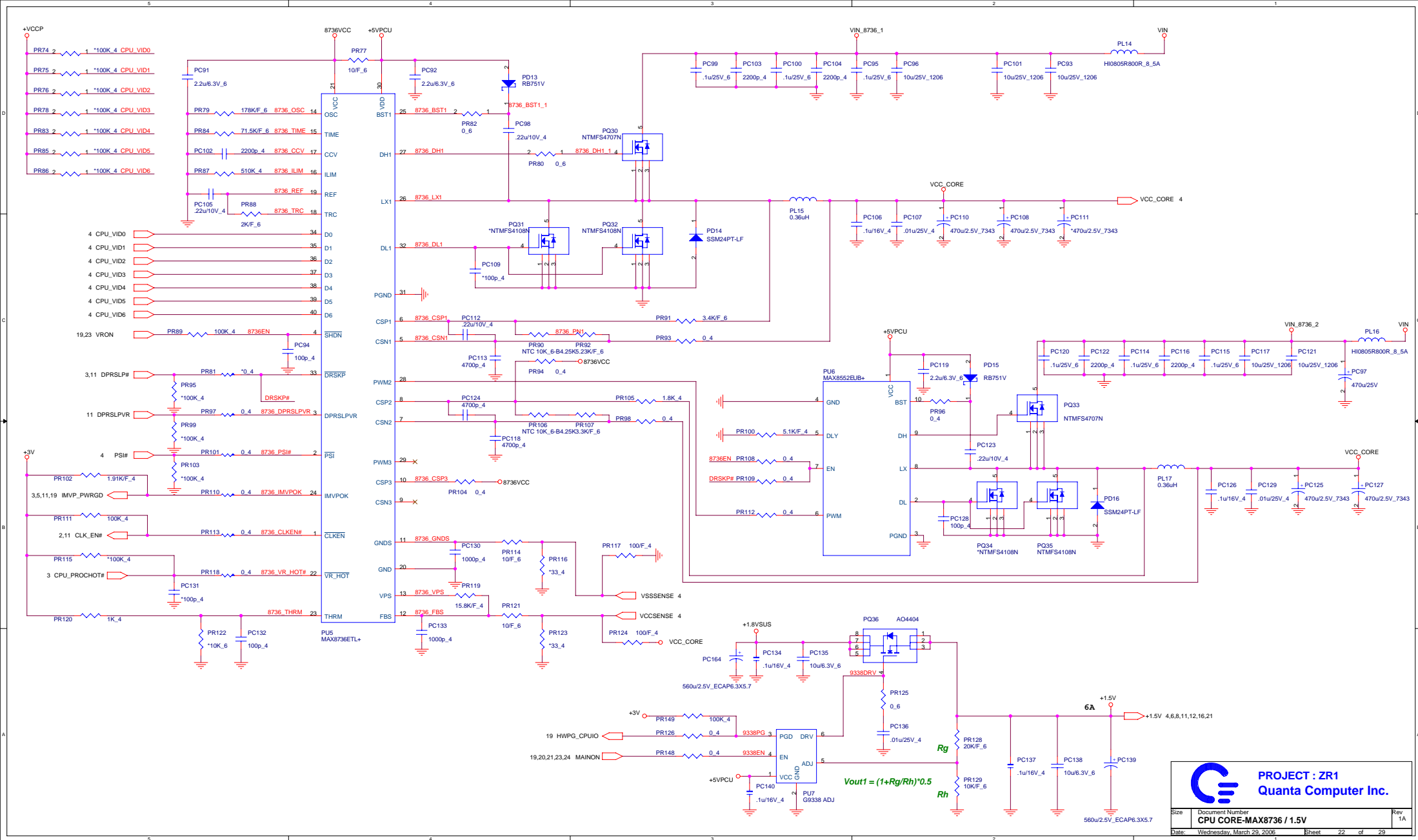
SMSC SIO1000



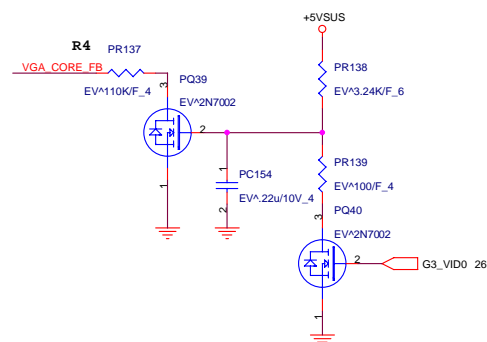
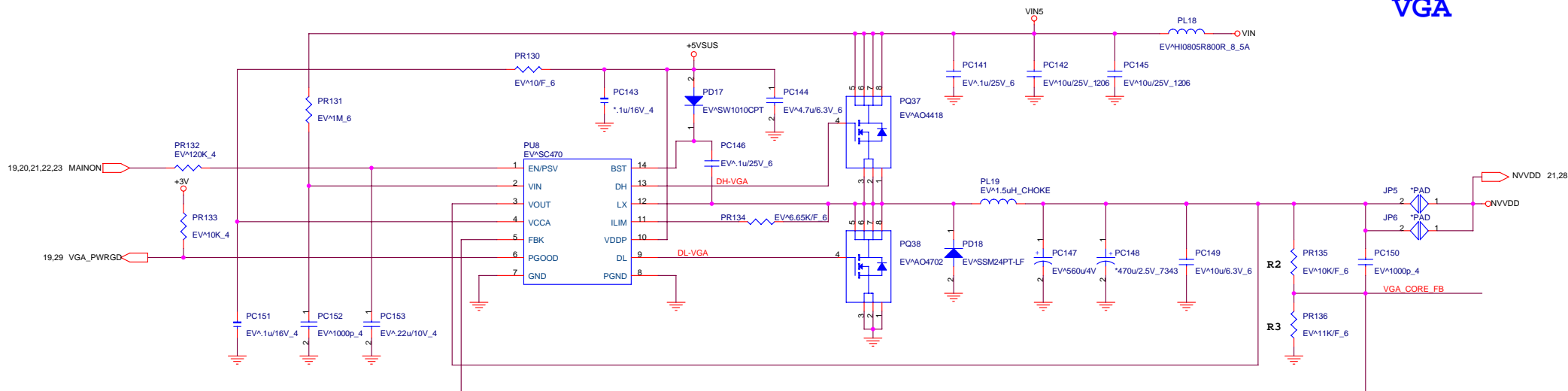
EZ4







VGA



$$HI \rightarrow VOUT = (1 + R2/R3) * 0.5$$

$$LO \rightarrow VOUT = (1 + R2/(R3 // R4)) * 0.5$$

M52P(G)

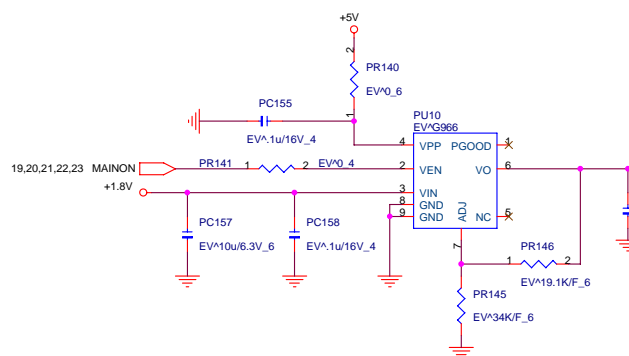
PR1 : 10K
PR4 : 11K
PR2 : 110K

M54P

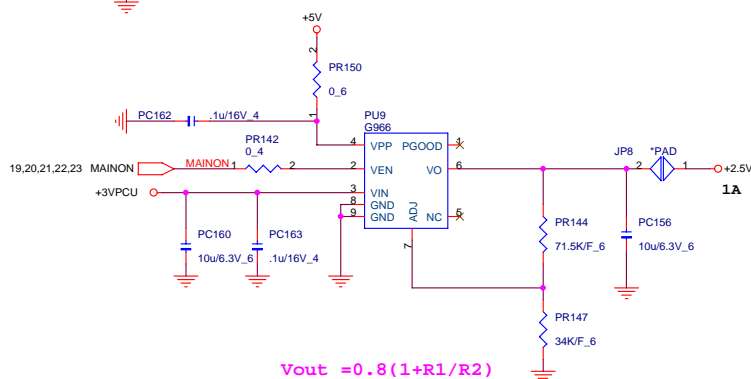
PR1 : 12K
PR4 : 12K
PR2 : 60.4K

Power Play Mode

VGA_PWR_SW	VGA_CORE
HI	0.95V--M52P(G) 1.0V--M54P
Default LO	1.0V--M52P(G) 1.1V--M54P



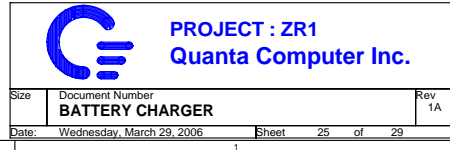
$$Vout = 0.8(1 + R1/R2) = 0.8(1 + 20K/20K) = 1.2V$$



$$Vout = 0.8(1 + R1/R2) = 0.8(1 + 20K/20K) = 2.5V$$



PROJECT : ZR1
Quanta Computer Inc.



NVIDIA
G72M
G3-64
(23X 23)

