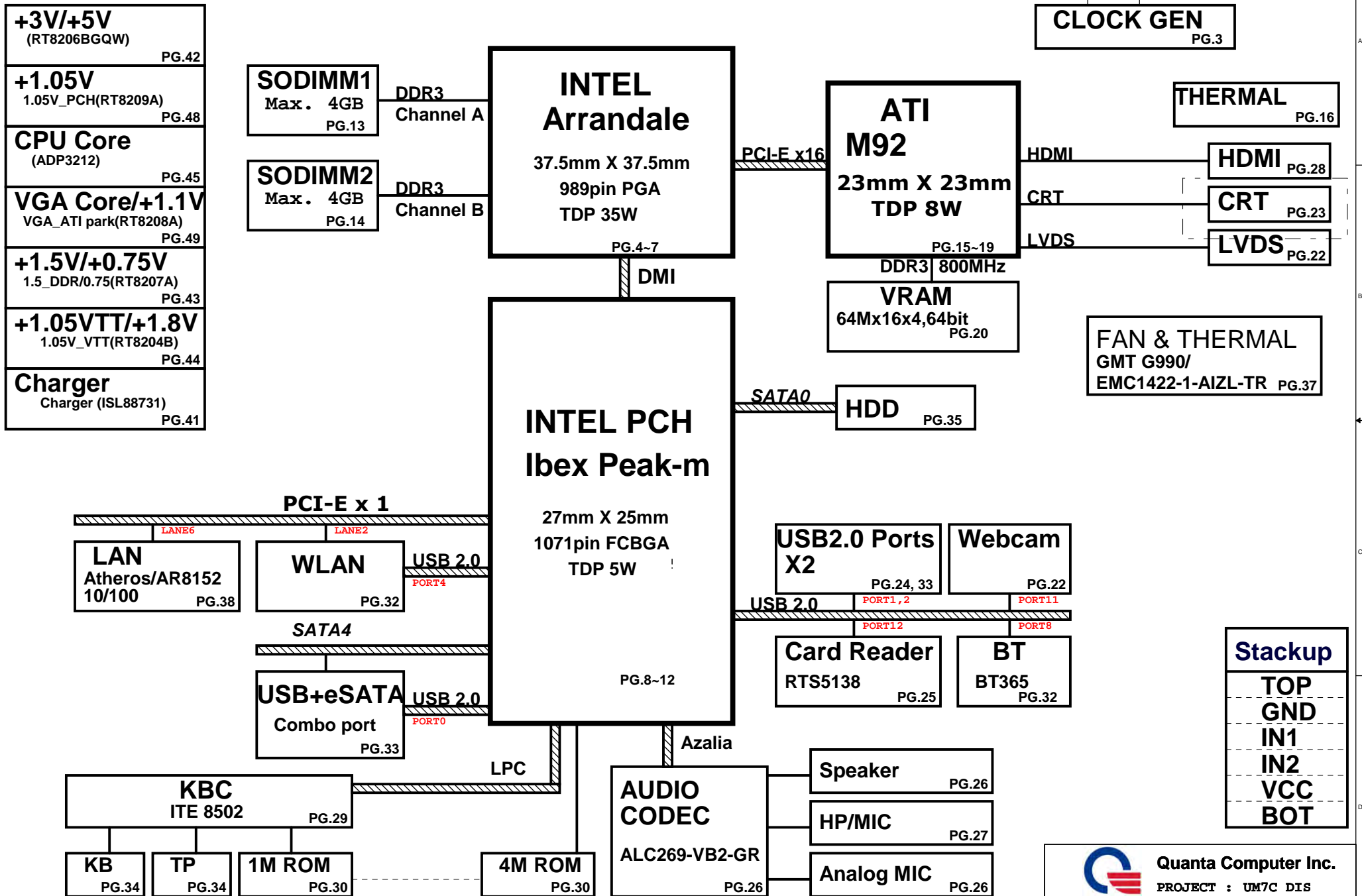


# UM7C DISCRETE SYSTEM DIAGRAM



[illegible]

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	23,42,43,44,45,46,49,50	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	09,12,30,31	RTC		S0~S5
					S0~S5
+5V_ALW	+5V	37,43,44,47,48	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	30,31,37,42,43,45,47,48	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	12,25,34,37,43,44,45,46,47,49,50	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	03,08,09,10,11,12,23,35,37,39,41,46,47,50	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	04,06,14,15,44,47	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	14,15,44	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	08,12,23,24,27,28,29,35,36,37,38,47	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,4,8,9,10,11,12,14,15,23,24,26,27,28,29,30,31,33,34,36,37,38,39,41,47	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	6,12,45	SDVO POWER	RUN_ON	
+1.05V_VTT	+1.1V	4,6,11,12,45,46	CPU POWER	RUN_ON	
+1.5V_RUN	+1.5V	12,33,47	PCH/Min Card	RUN_ON	
+1.05V_PCH	+1.05V	3,8,9,10,12,49	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	6,46	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	23	LCD Power	LCDVCC_TST_EN & ENVDD	

[illegible]

**PROJECT : UM7C DIS**

Size

Document Number

### BLOCK DIAGRAM

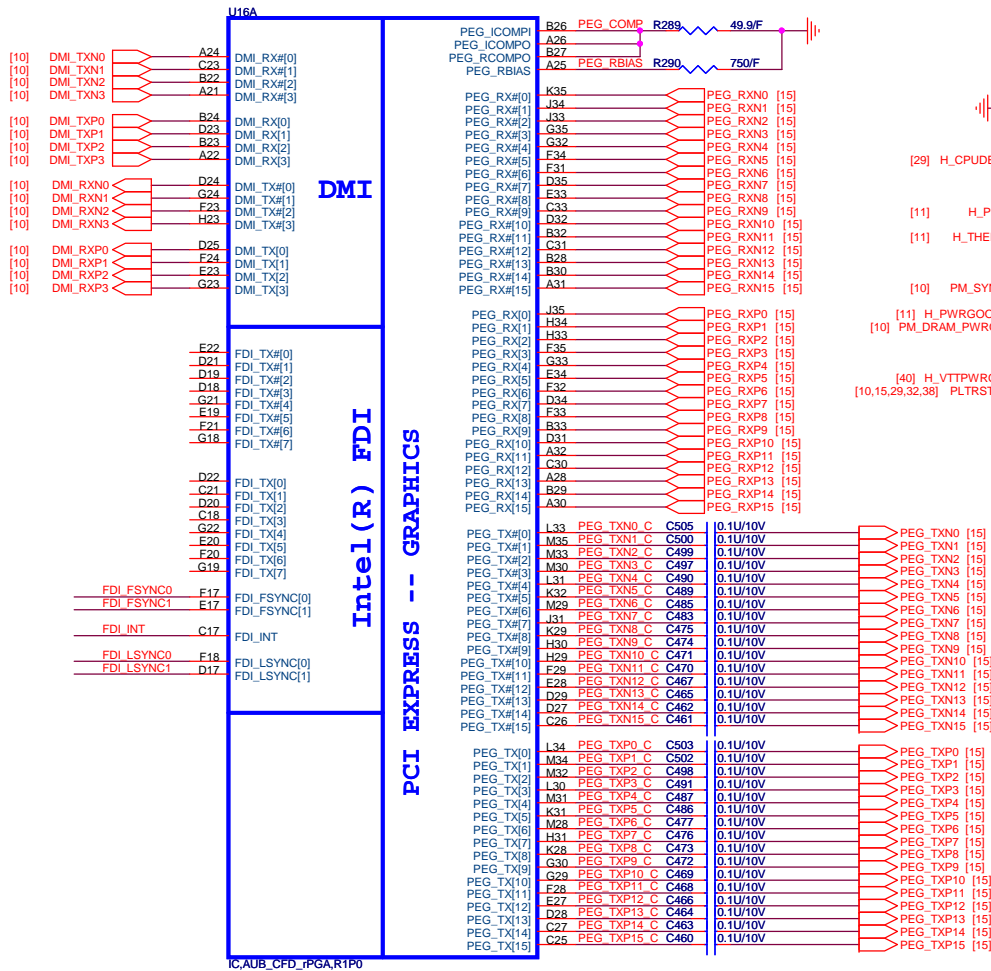
Rev

2A

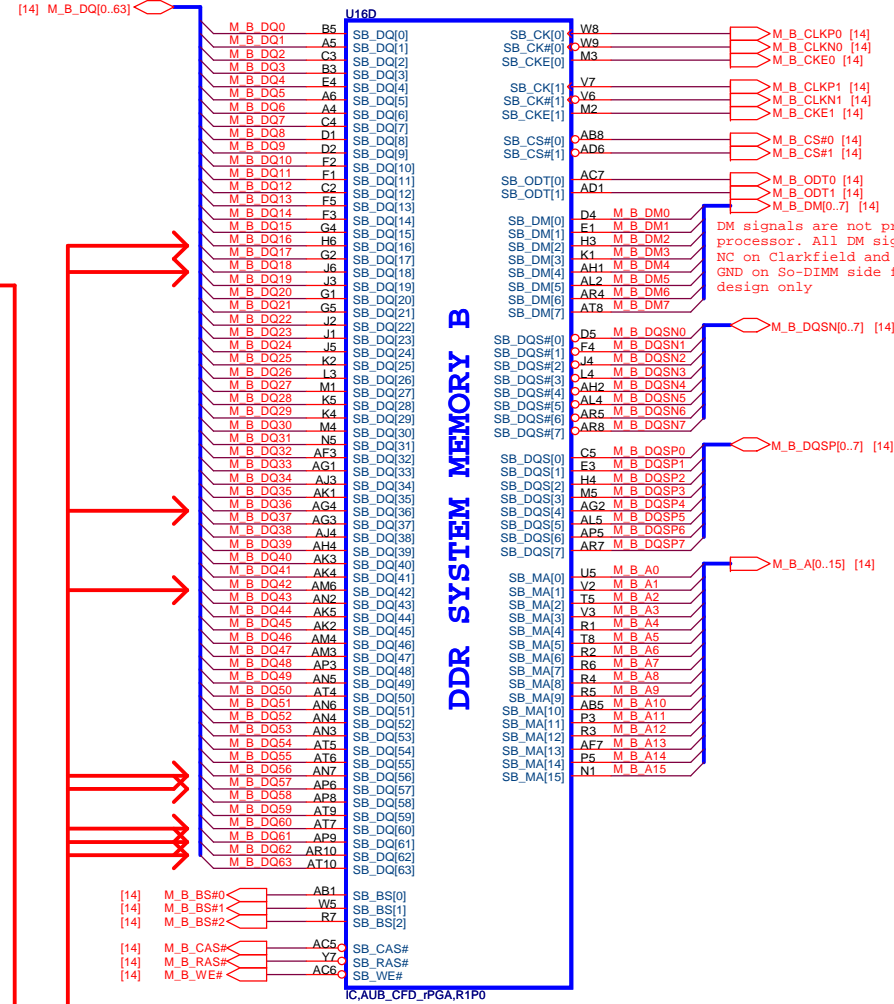
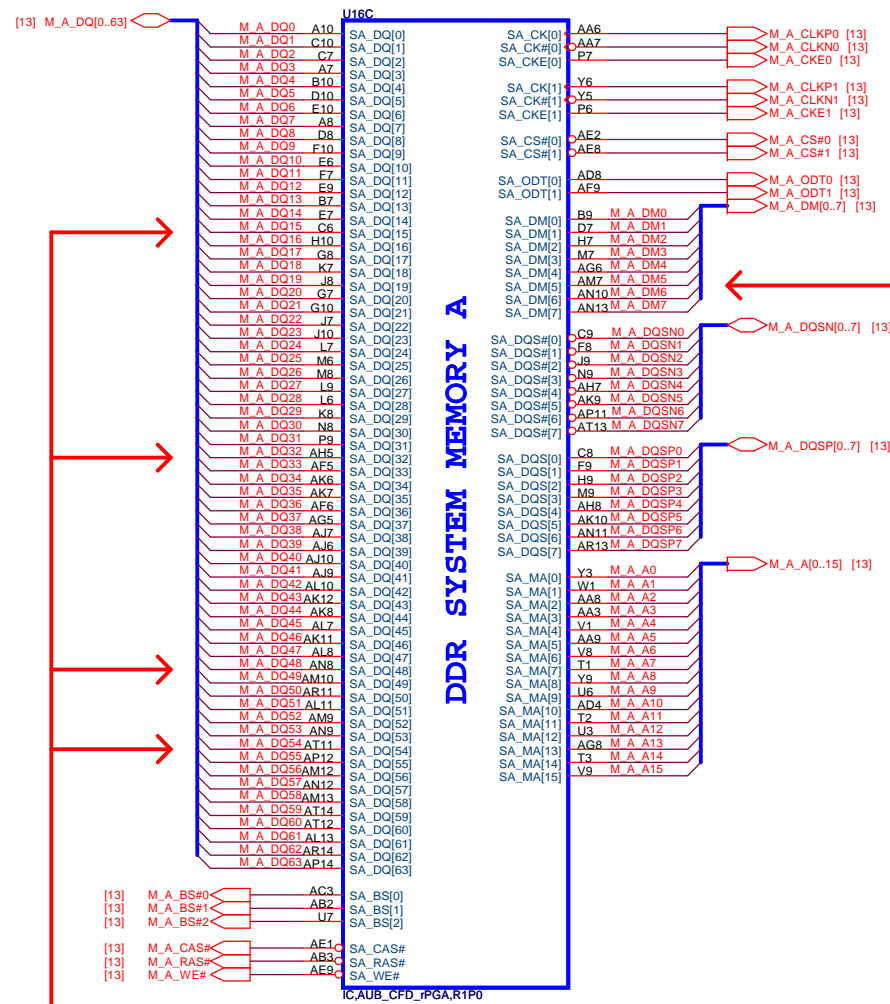
Date: Monday, May 24, 2010

Sheet 2 of 52

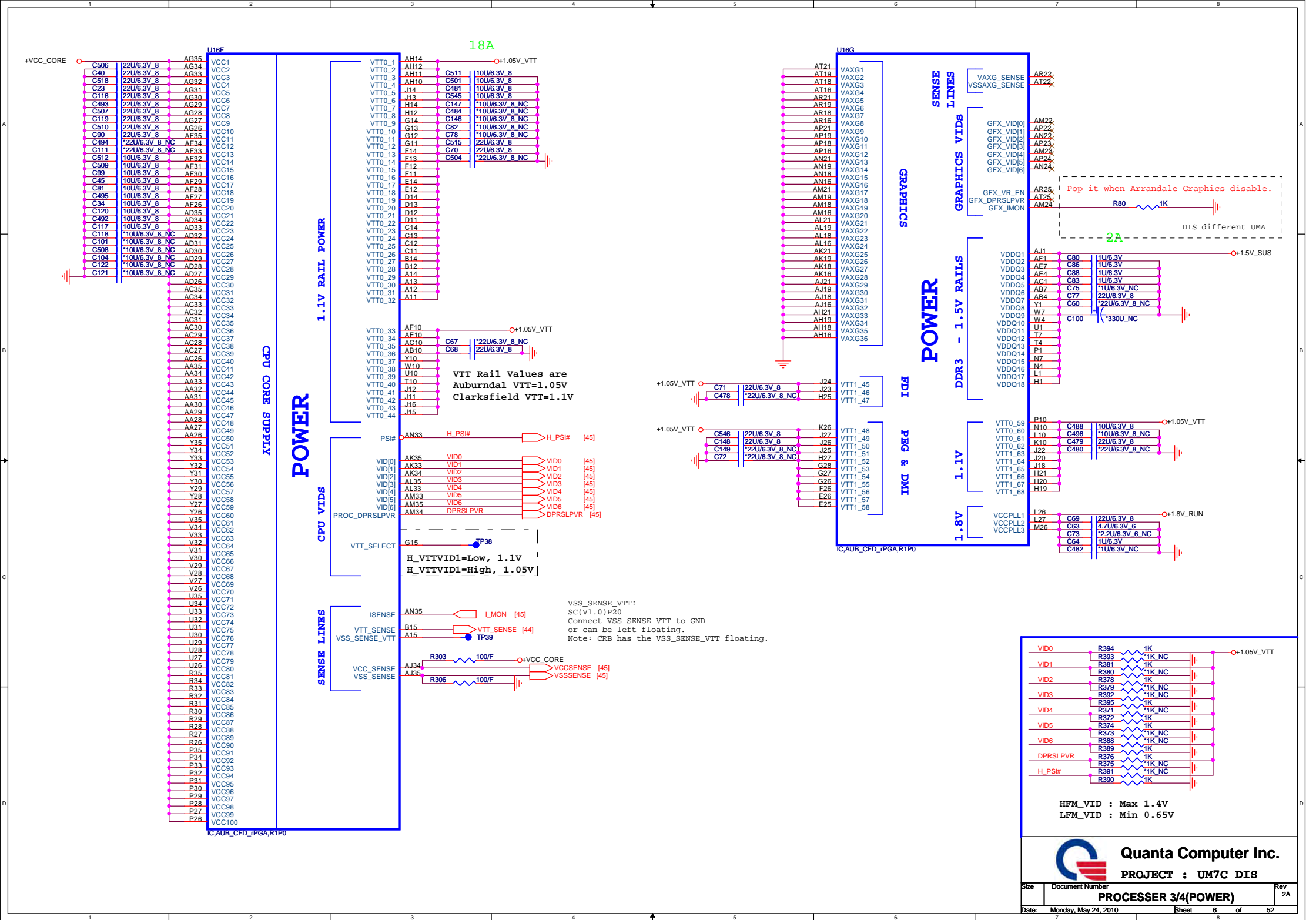




# AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



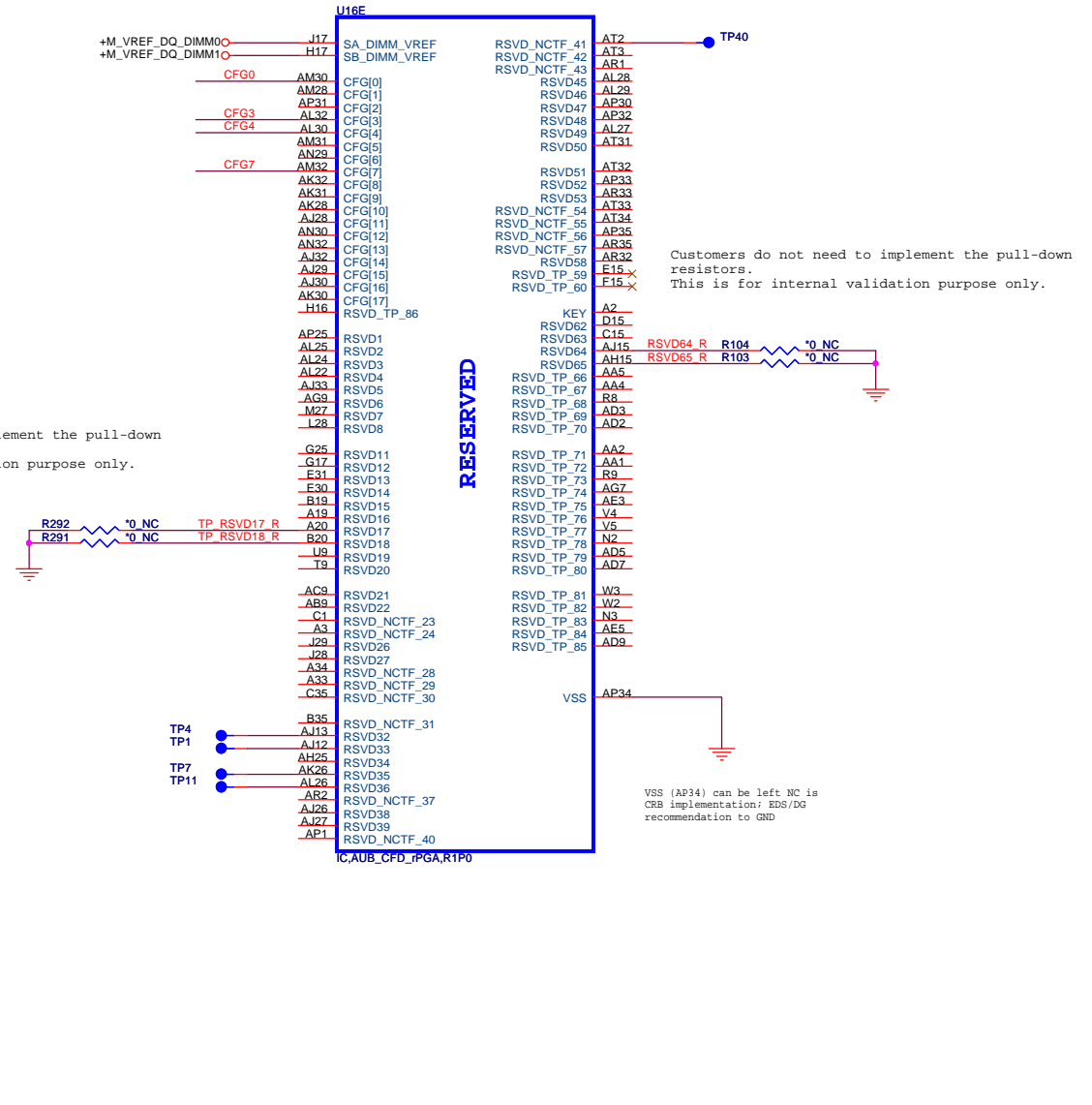
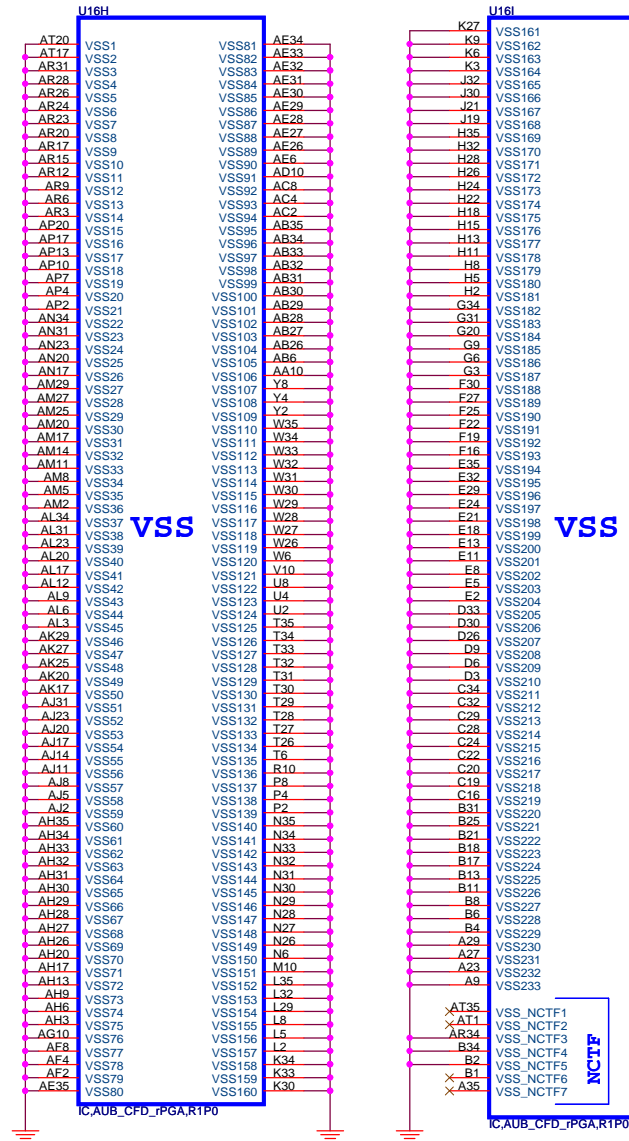
**Quanta Computer Inc.**  
**PROJECT : UM7C DIS**





# Arrandale PROCESSOR (GND)

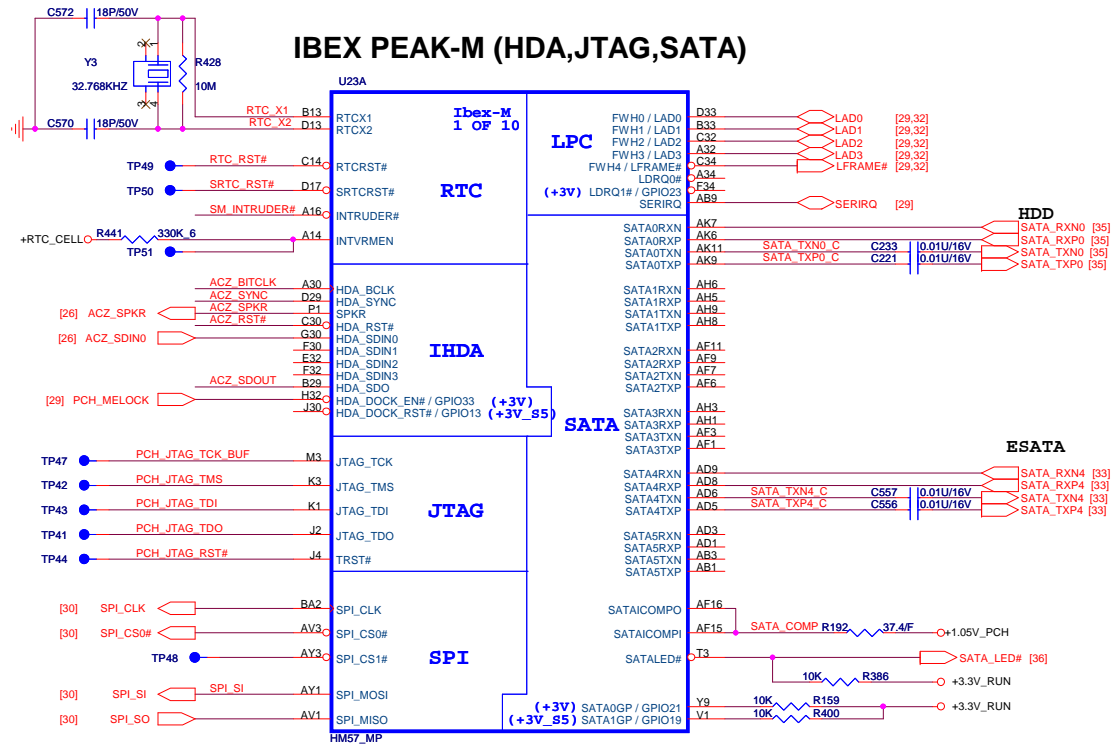
# Arrandale PROCESSOR( RESERVED, CFG)



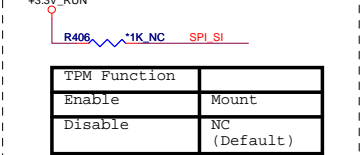
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

INVRMEN - Integrated SUS 1.1V VRM Enable  
High - Enable Internal VRs

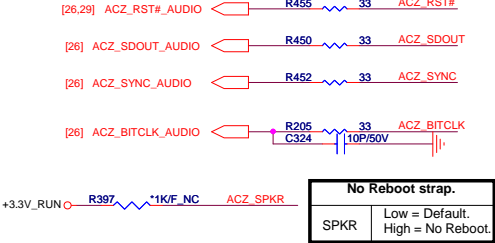
## IBEX PEAK-M (HDA,JTAG,SATA)



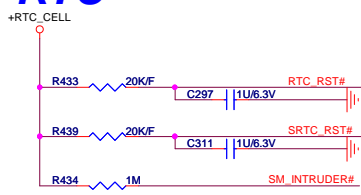
### iTPM ENABLE/DISABLE



### For AUDIO

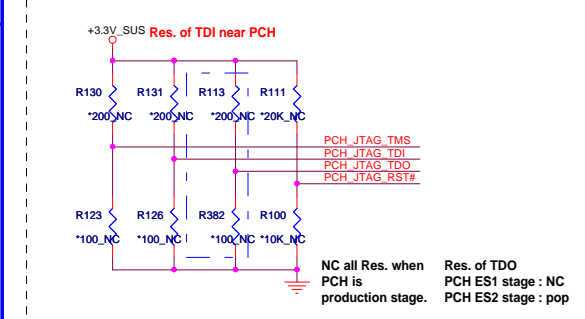


### RTC 1mA



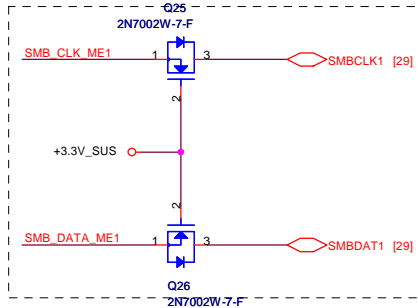
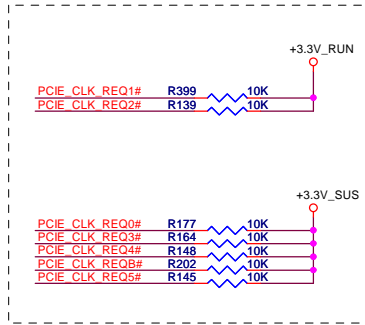
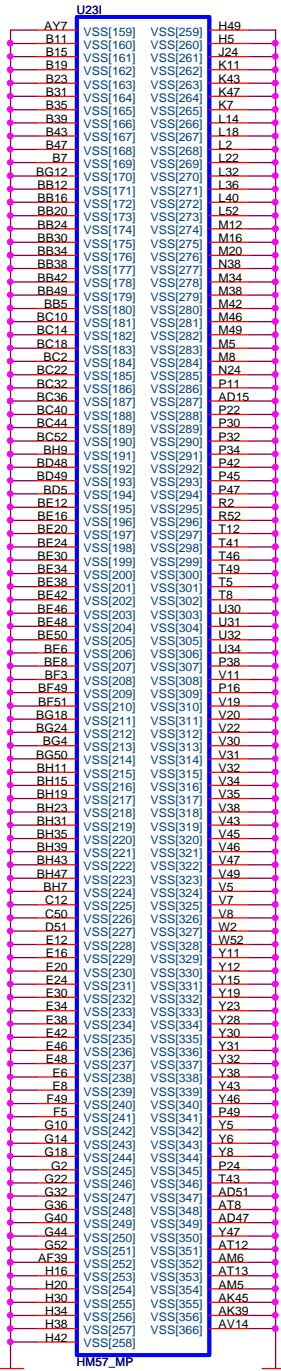
R384 51 PCH\_JTAG\_TCK\_BUF

Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

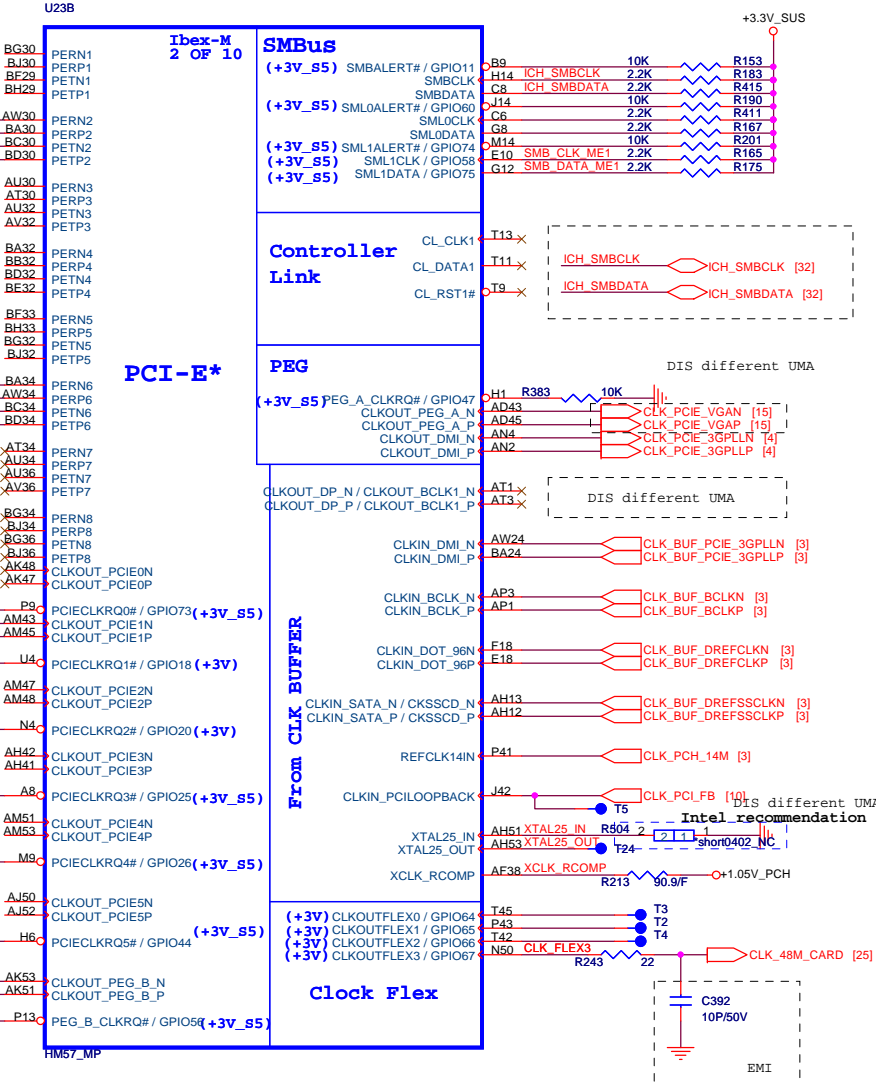




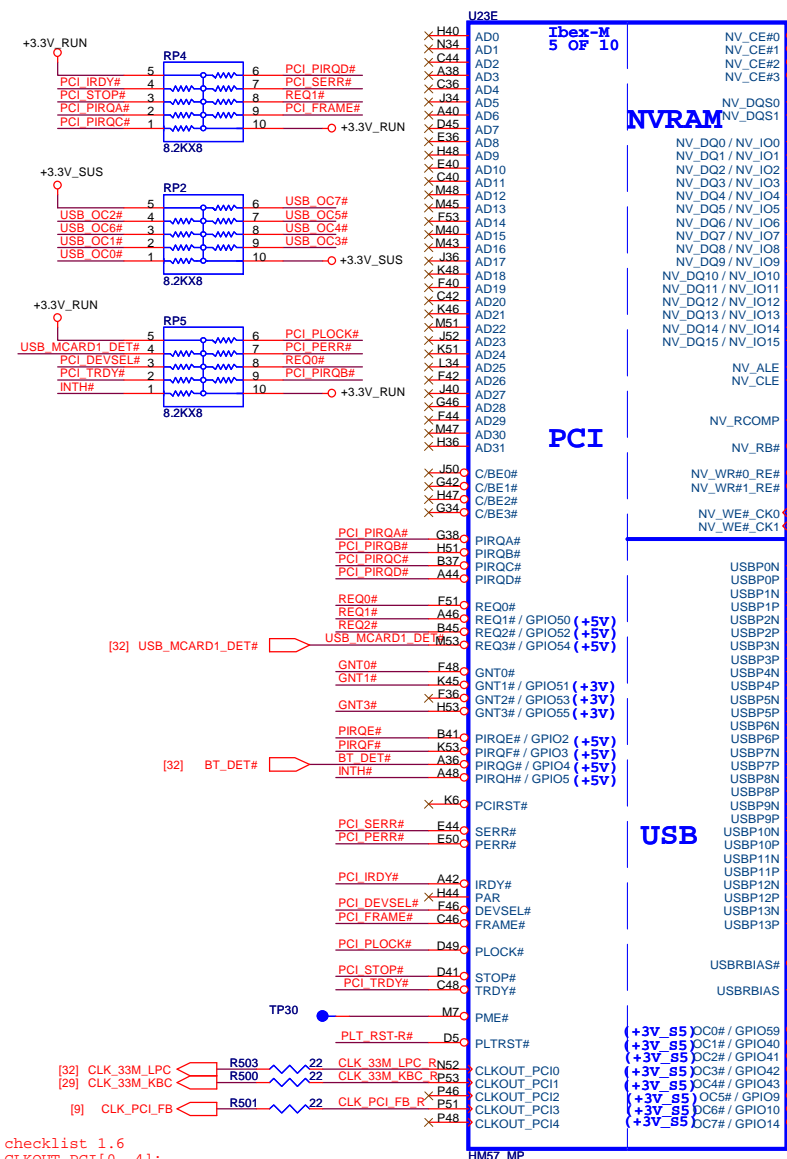
# IBEX PEAK-M (GND)



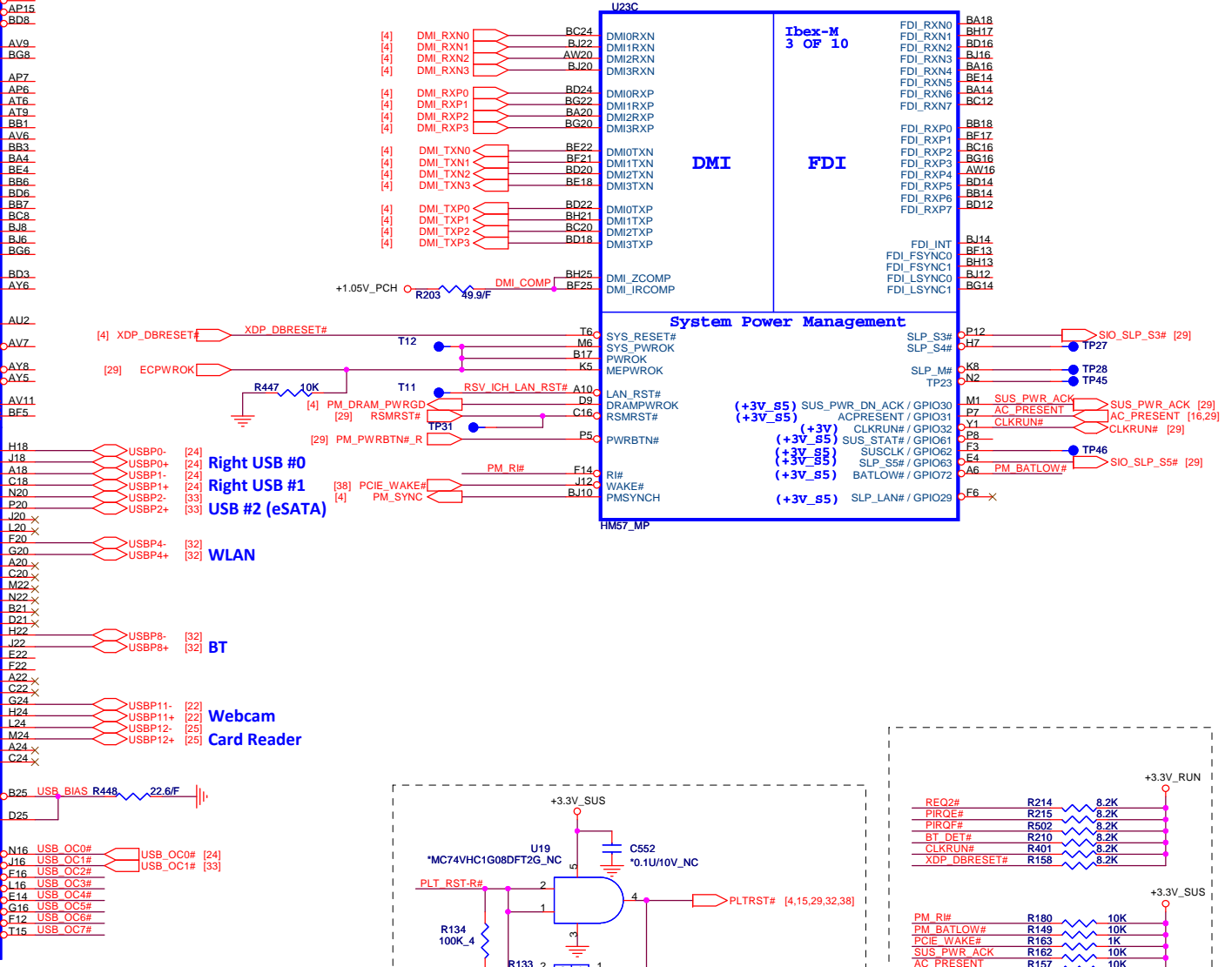
# IBEX PEAK-M (PCI-E,SMBUS,CLK)



# IBEX PEAK-M (PCI,USB,NVRAM)

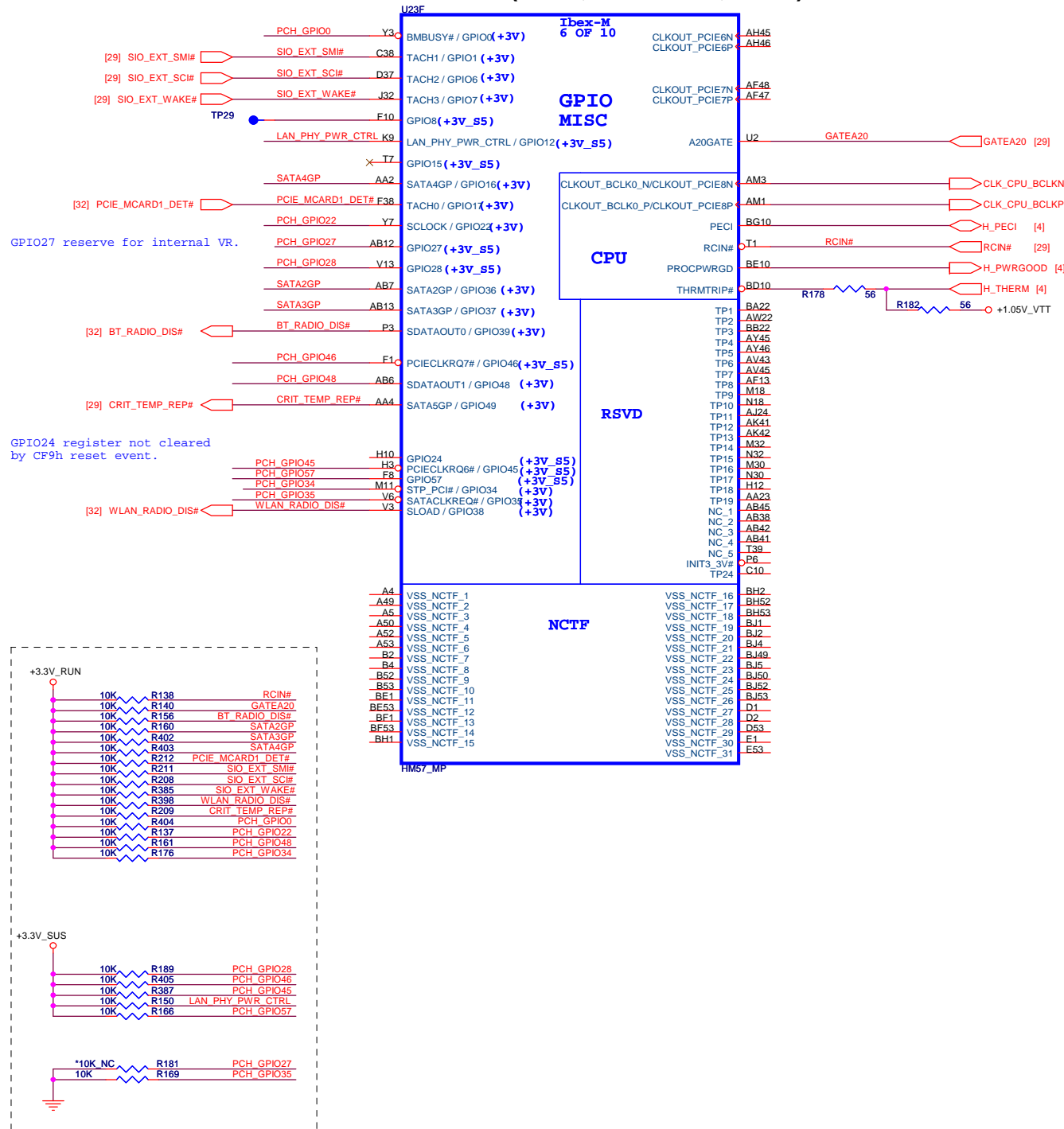


# IBEX PEAK-M (DMI,FDI,GPIO)

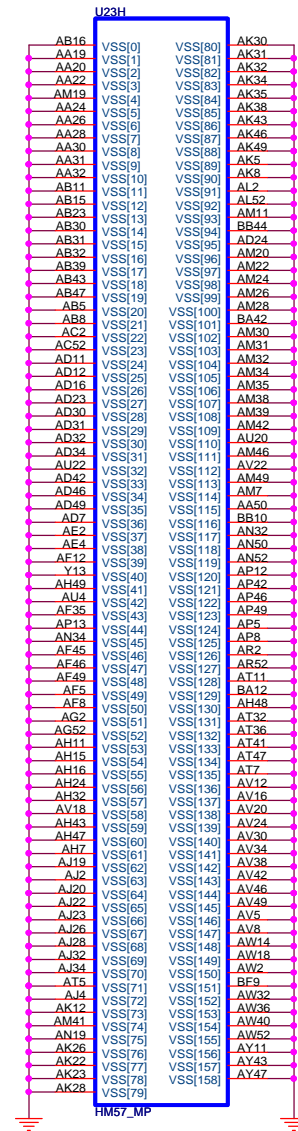


**Quanta Computer Inc.**  
**PROJECT : UM7C DIS**

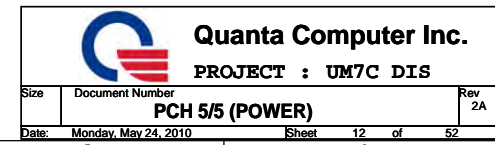
## IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)



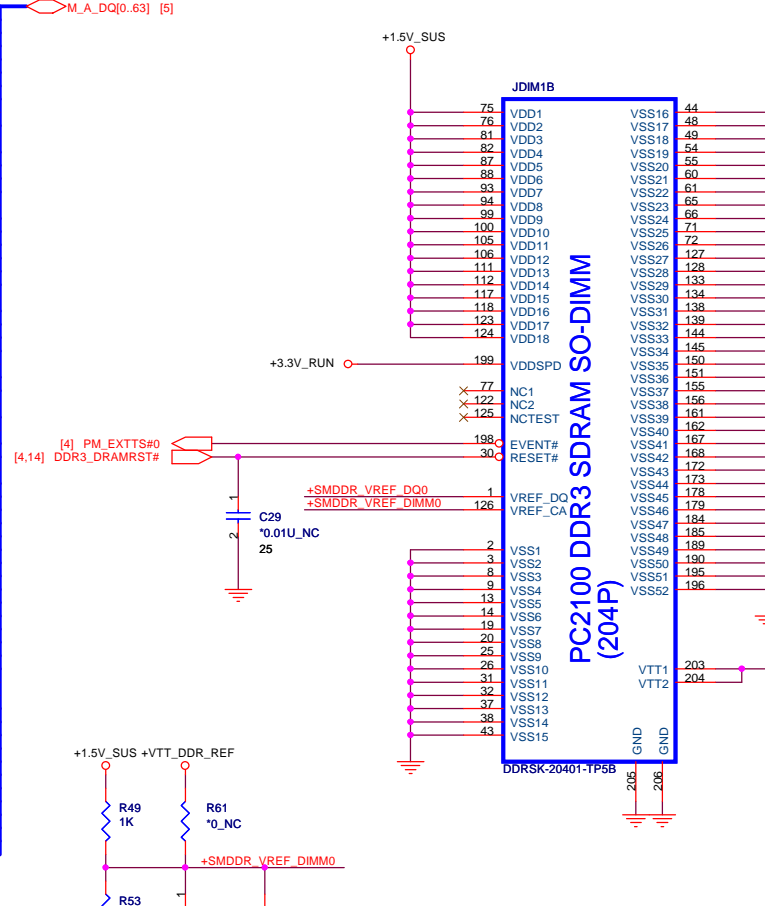
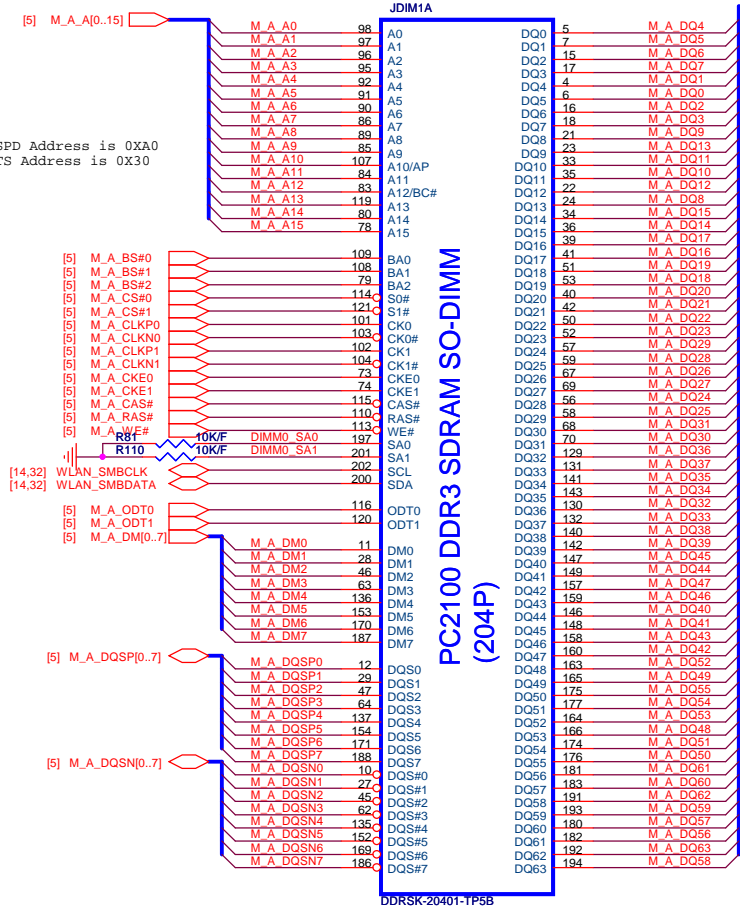
### IBEX PEAK-M (GND)



L32 DIS-SHORT

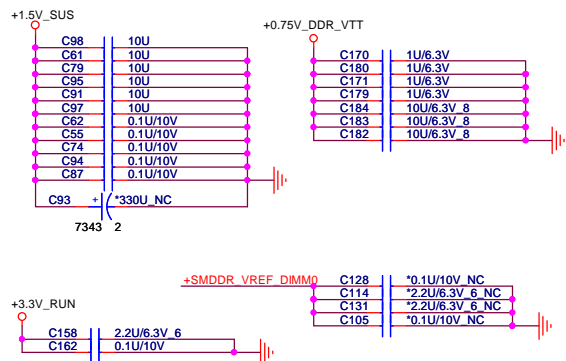


SO-DIMMA SPD Address is 0XA0  
SO-DIMMA TS Address is 0X30

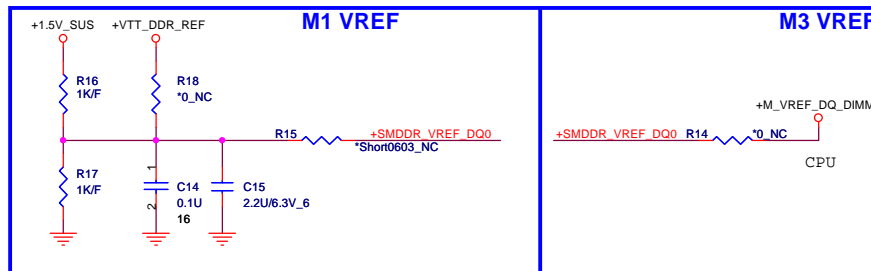


## Place these Caps near So-Dimm0.

Some Projects replace 10UF 0805 by 4.7UF 0603  
It can cost down 30%



H5.2



Quanta Computer Inc.

PROJECT : UM7C DIS

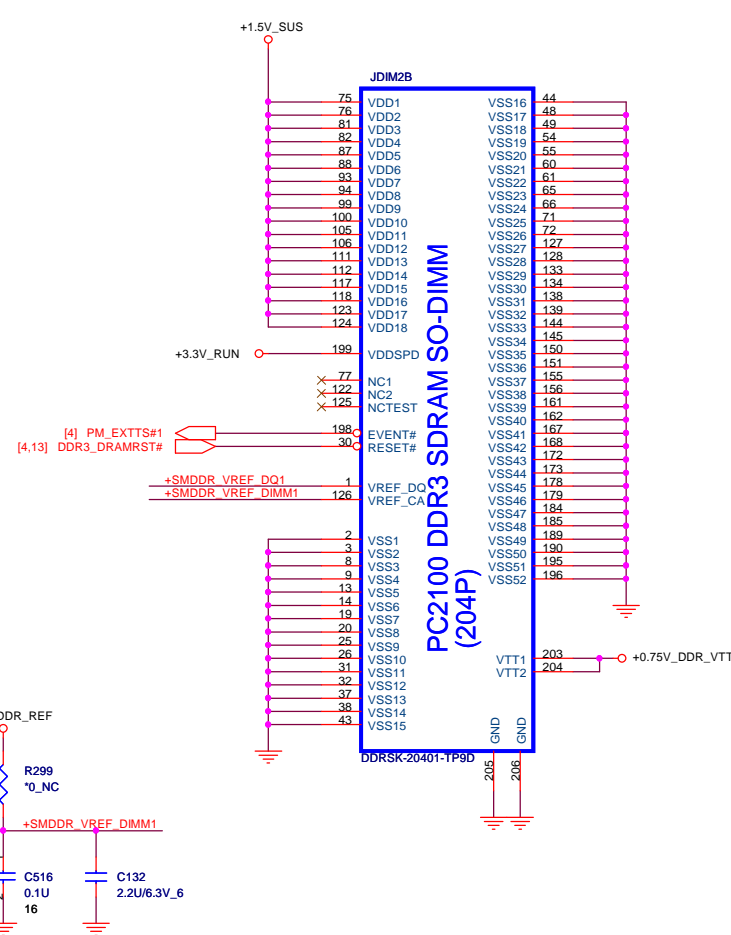
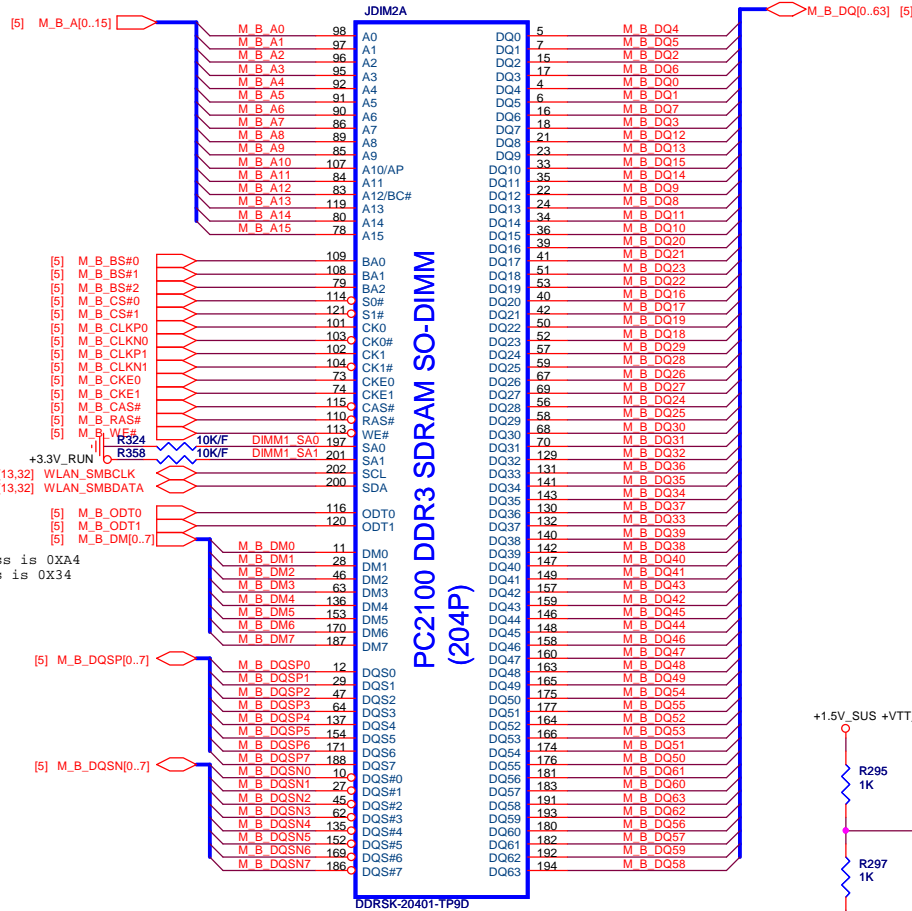
Size Document Number

DDR3 DIMM-0

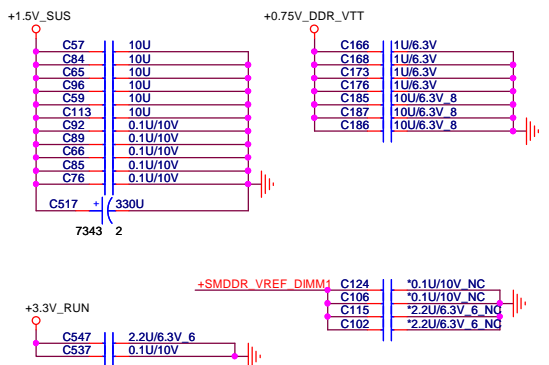
Rev 2A

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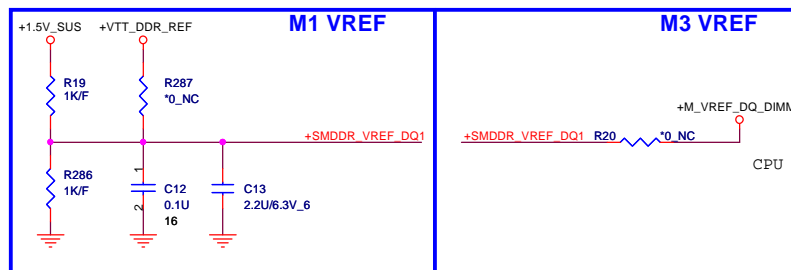




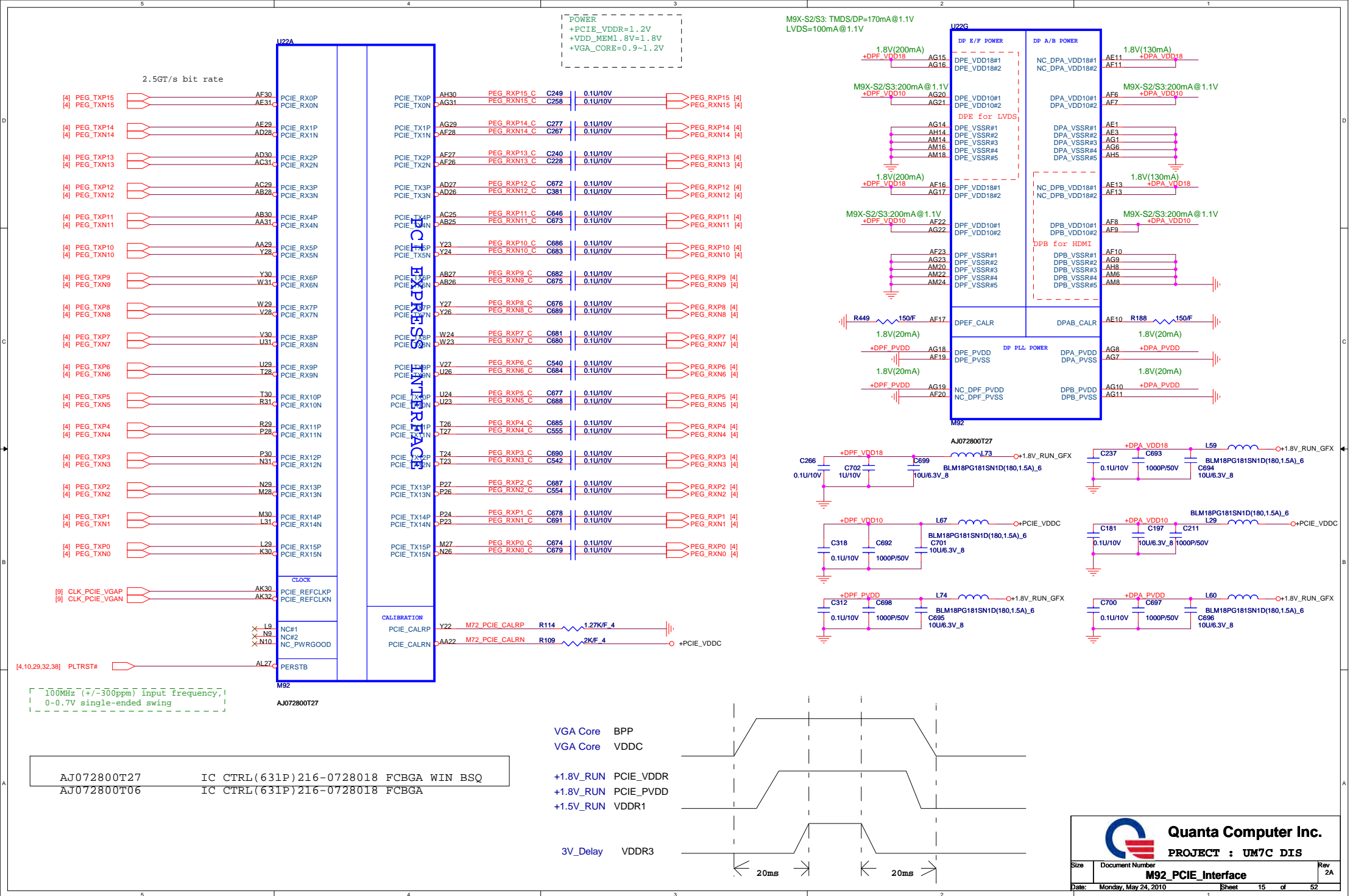
**Place these Caps near So-Dimm1.**  
Some Projects replace 10UF 0805 by 4.7UF 0603  
It can cost down 30%



H9.2







Memory Straps	MEM_ID2	MEM_ID1	MEM_ID0	Quanta PN (QuantaBuy)	Vendor PN	Support GPU
800MHz 512MB(64M*16) Samsung	0	0	1	AKD5LGGT502	K4W1G1646E-HC12	For M92
800MHz 512MB(64M*16) Hynix	0	1	0	AKD5LZGTW00	H5TQ1G63BFR-12C	For M92

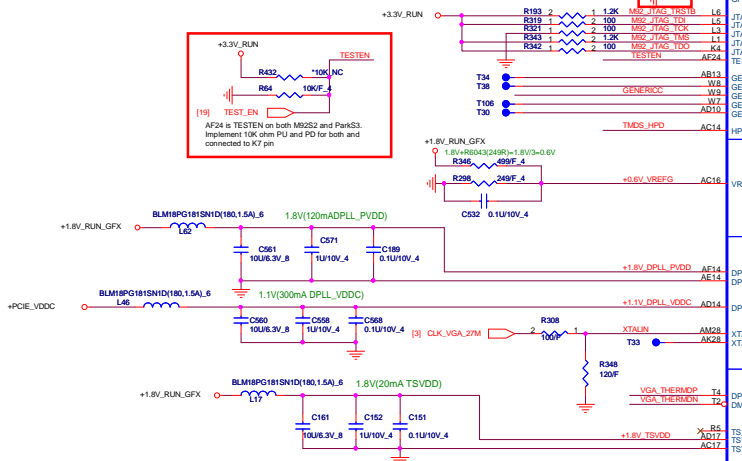
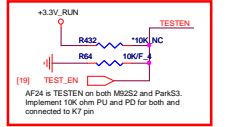
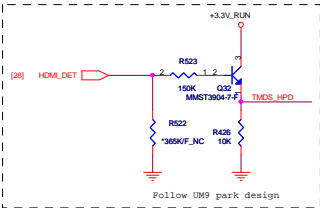
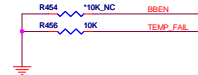
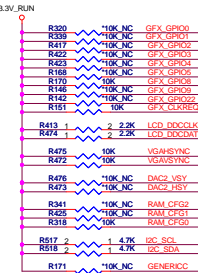
Memory Aperture size

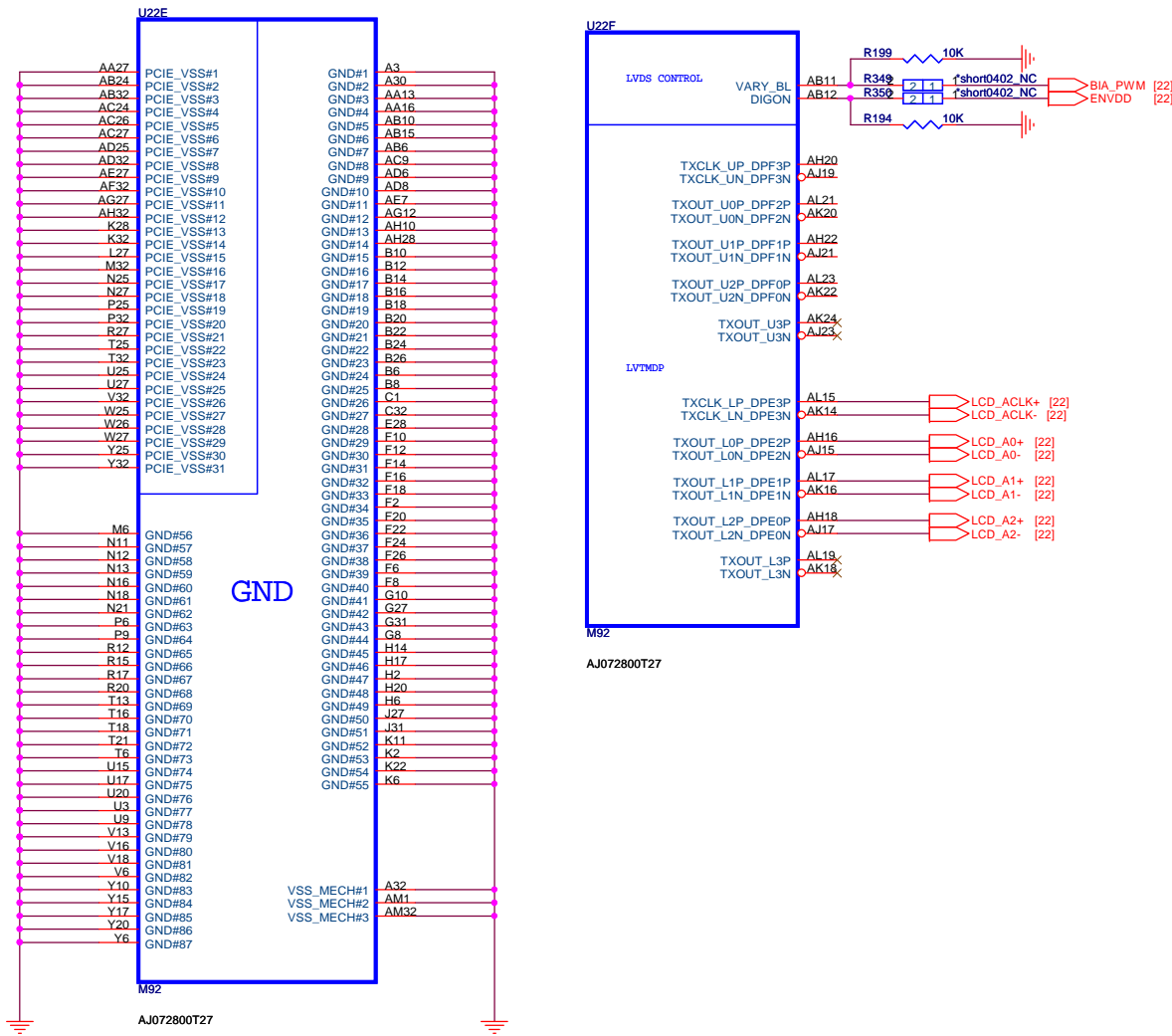
GPIO9		GPIO13	GPIO12	GPIO11
BIOSROM		ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

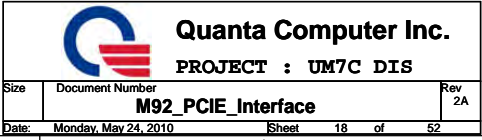
It is a shared pin strap with CONFIG[2:0] if BIOS\_ROM\_EN is set to 0.

	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.05V
M	1	0	0.95V
L	1	1	0.9V

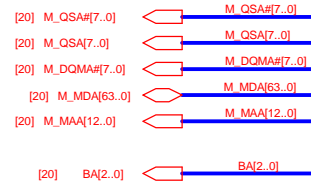
	BBEN	BBP
L	0	V-CORE
H	1	+1.8V



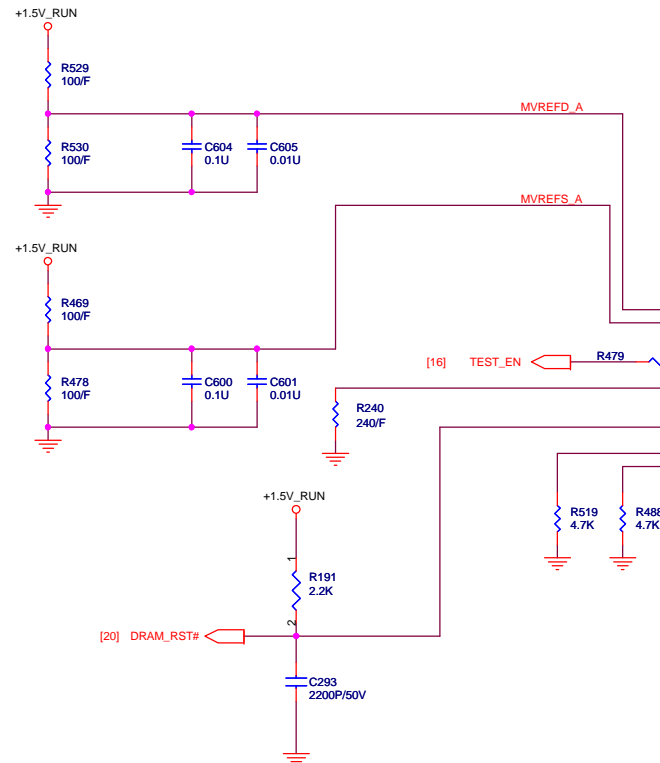


PCIE\_VDDR--PCI-E I/O power. 1.8 V  $\pm$  5%

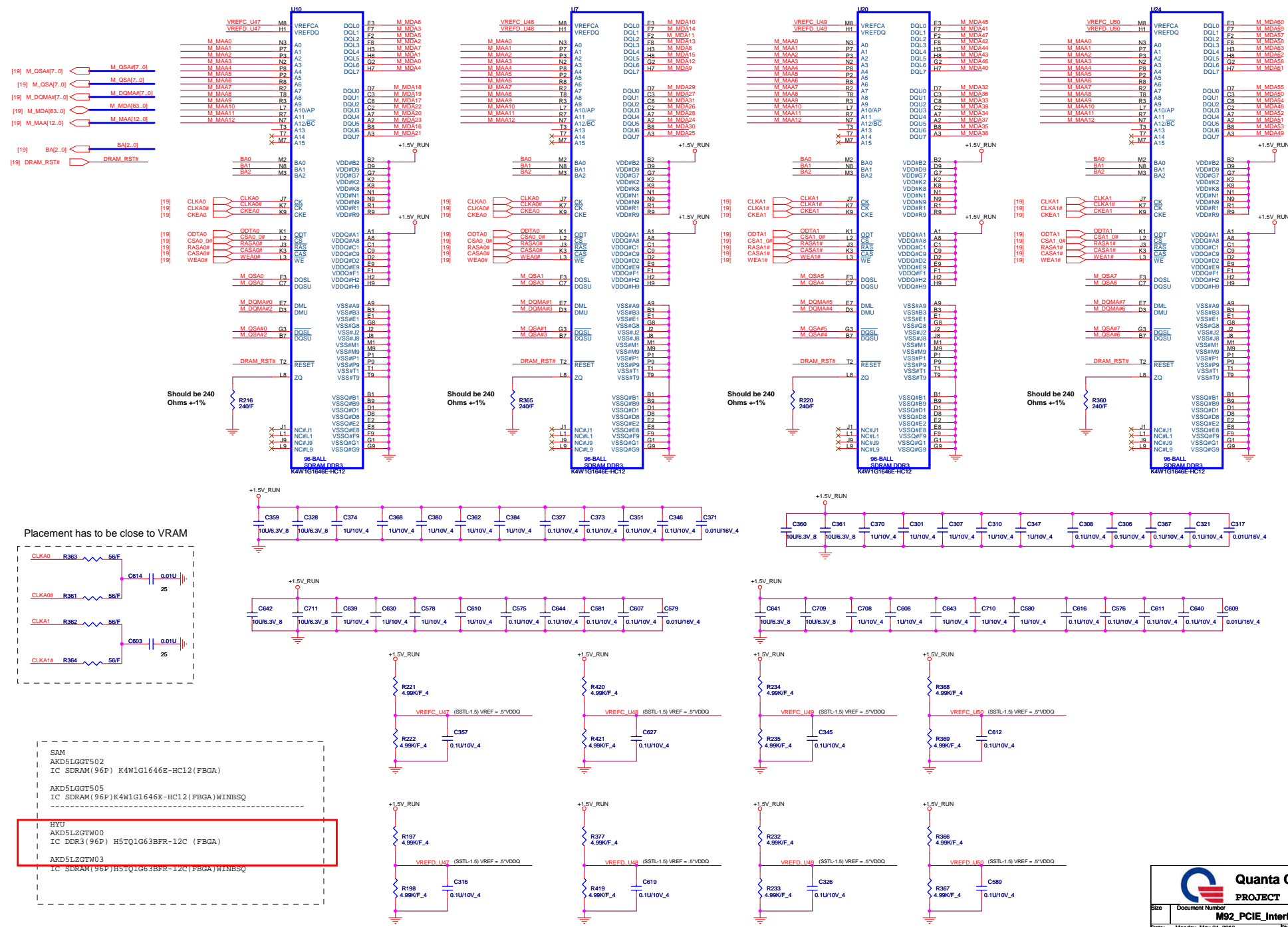
# MEMORY INTERFACE



DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.5V	100R	40.2R
MVREF TO GND	100R	100R

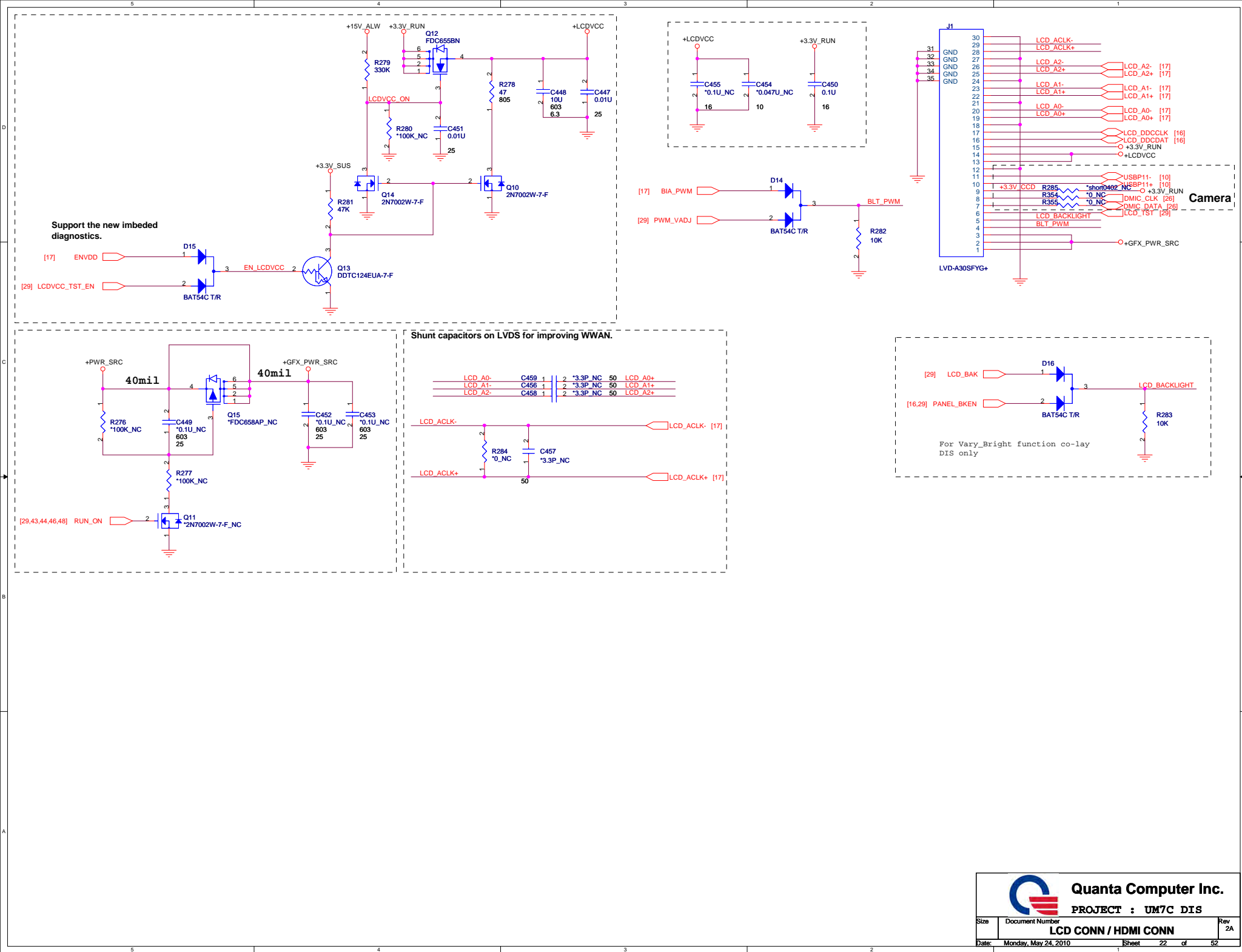


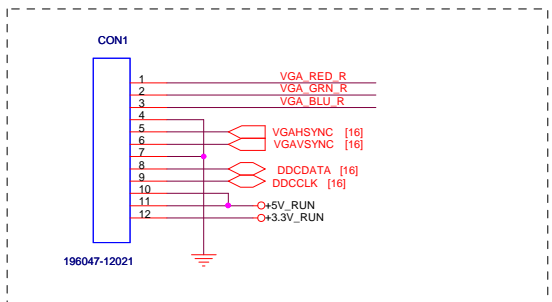
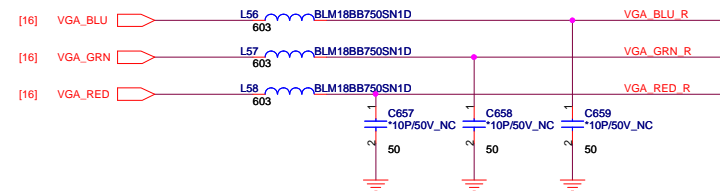
## M92-LP (DDR3 512M)

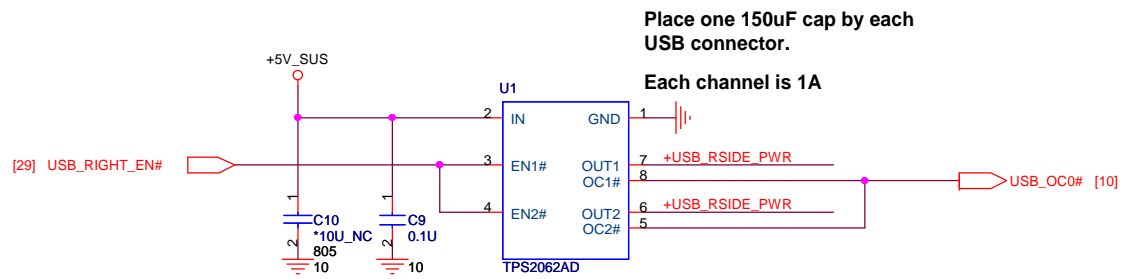
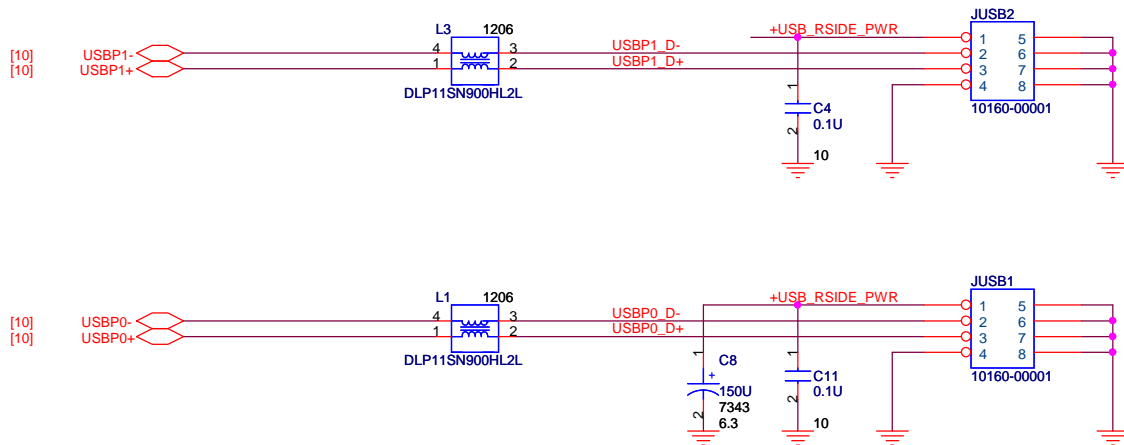






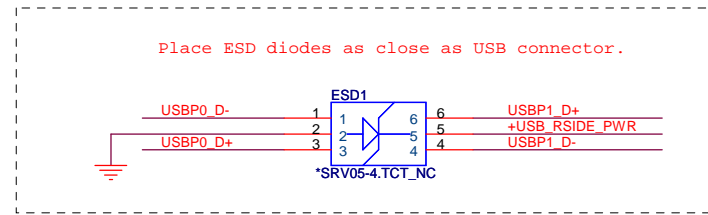


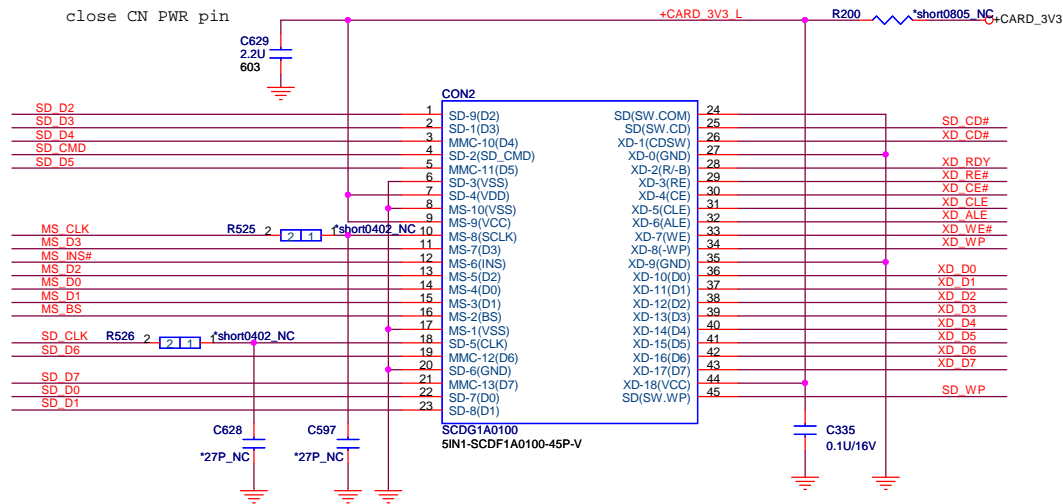




Place one 150uF cap by each USB connector.  
Each channel is 1A

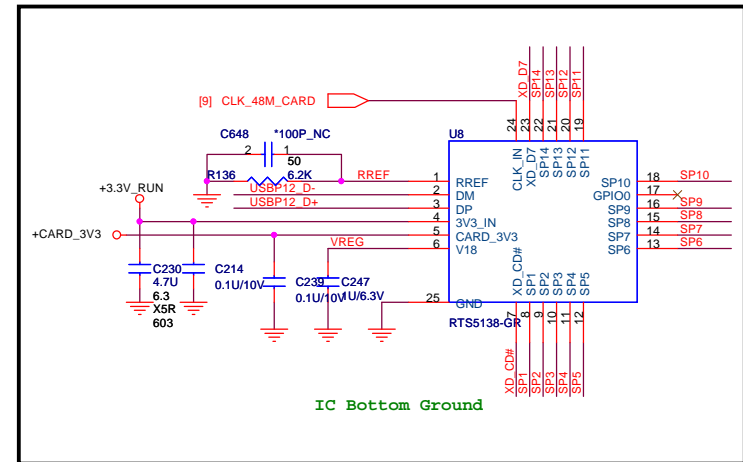
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



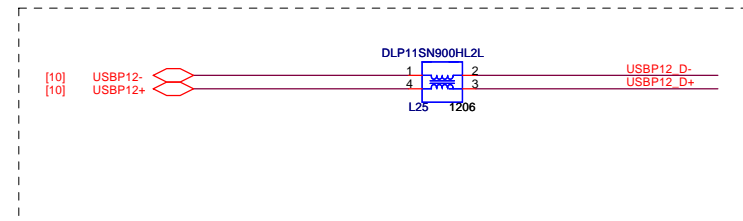


SP1	XD RDY	SD_WP	MS CLK
SP2	XD RE#	SD D1	MS INS#
SP3	XD CE#	SD D0	MS D7
SP4	XD CLE	SD D7	MS D3
SP5	XD ALE	SD CD#	
SP6	XD WE#	SD D6	MS D6
SP7	XD WP	SD CLK	MS D2
SP8	XD D0	SD D5	MS D0
SP9	XD D1	SD D5	MS D0
SP10	XD D2	SD CMD	
SP11	XD D3	SD D4	MS D4
SP12	XD D4	SD D3	MS D1
SP13	XD D5	SD D2	MS D5
SP14	XD D6	MS BS	

Share Pin



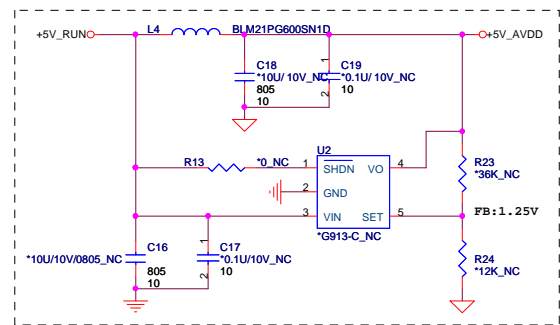
RTS5138-QFN24



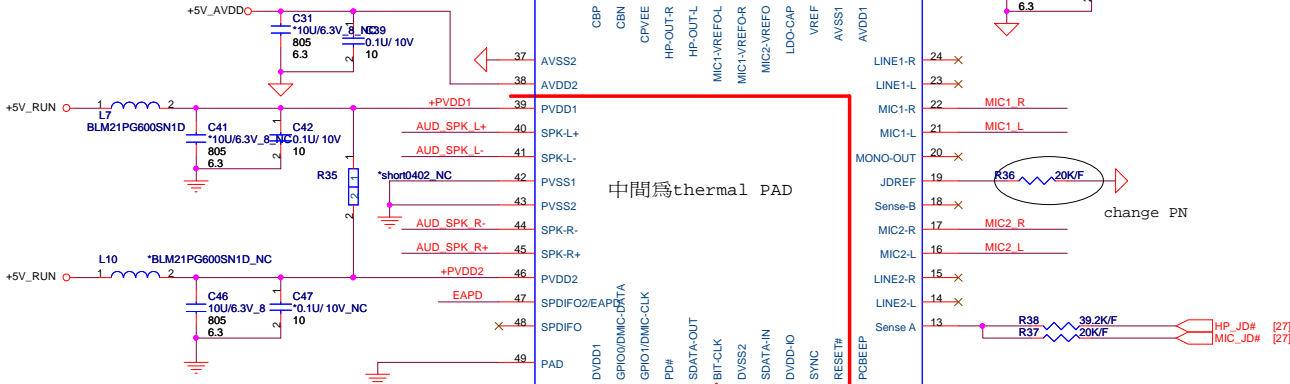
Quanta Computer Inc.

PROJECT : UM7C DIS

Size	Document Number	Rev
	Card Reader(RTS5138)	2A
Date	Monday, May 24, 2010	Sheet 25 of 52



AVDD1, AVDD2 TYP=48mA

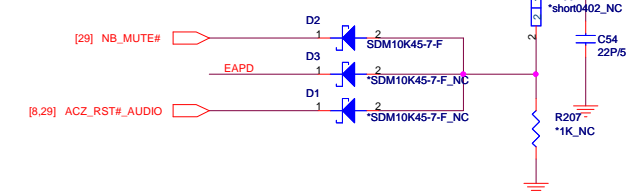


中間為thermal PAD

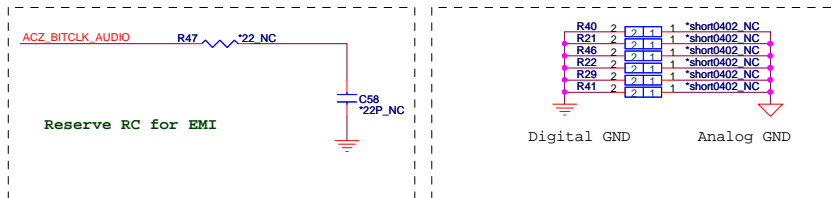
Analog Plane

Digital Plane

DVDD & DVDD-IO TYP=50mA



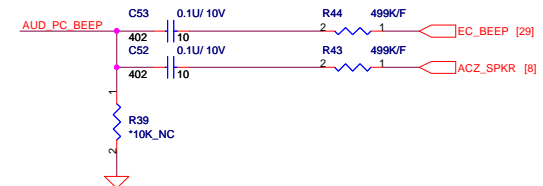
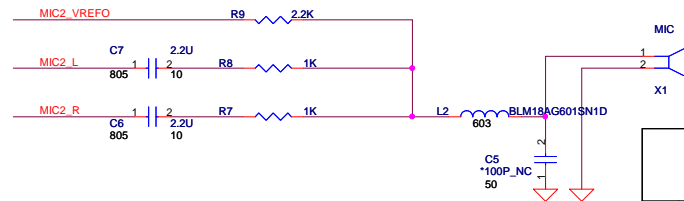
PD#=0V : Power down Class D SPK amplifier  
PD#=3.3V : Power up Class D SPK amplifier  
Internal pulled high.



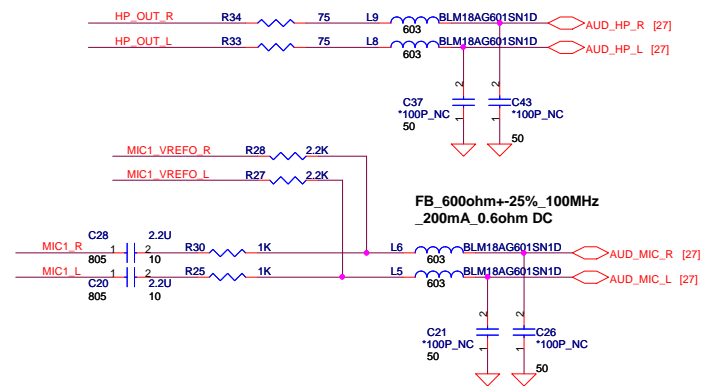
Reserve RC for EMI

Digital GND

Analog GND



5V / 4 Ohm / 1.5W

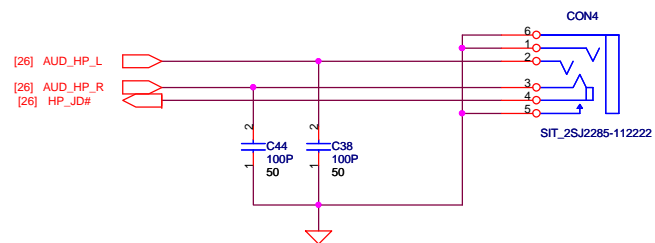


FB\_600ohm+-25%\_100MHz  
\_200mA\_0.6ohm DC



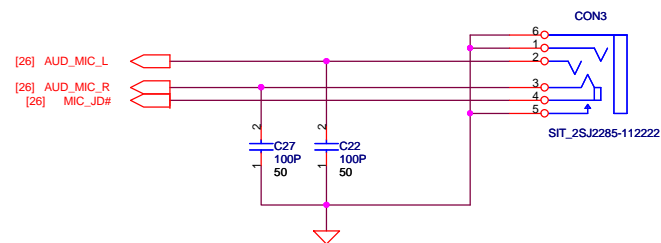
## HP JACKN

SUYIN NORMAL OPEN



## MIC JACK

SUYIN NORMAL OPEN



Quanta Computer Inc.

PROJECT : UM7C DIS

Size Document Number

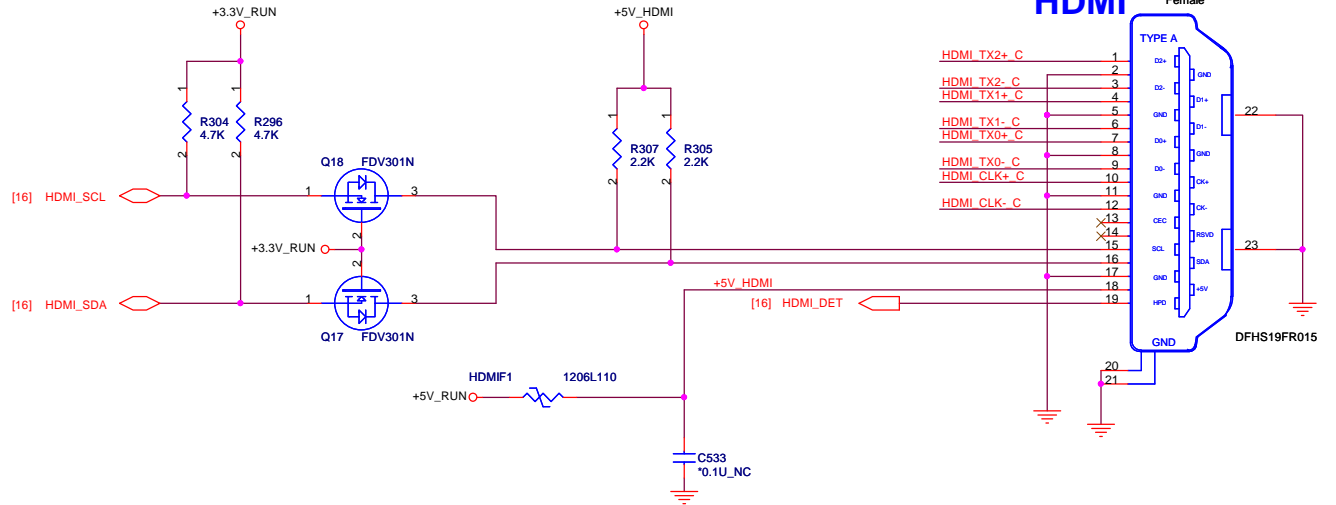
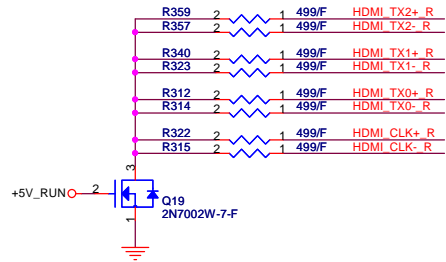
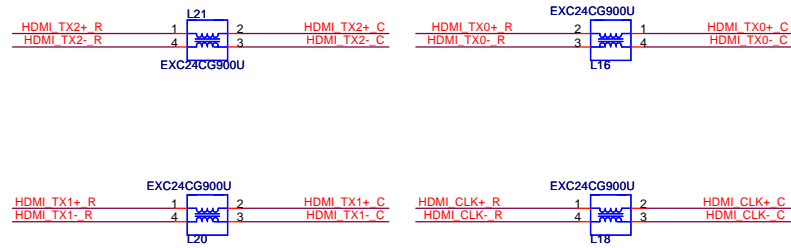
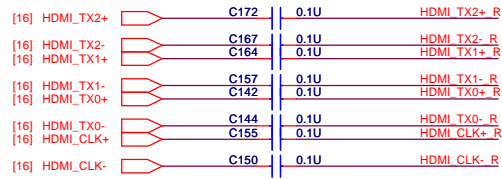
AUDIO CONN

Rev

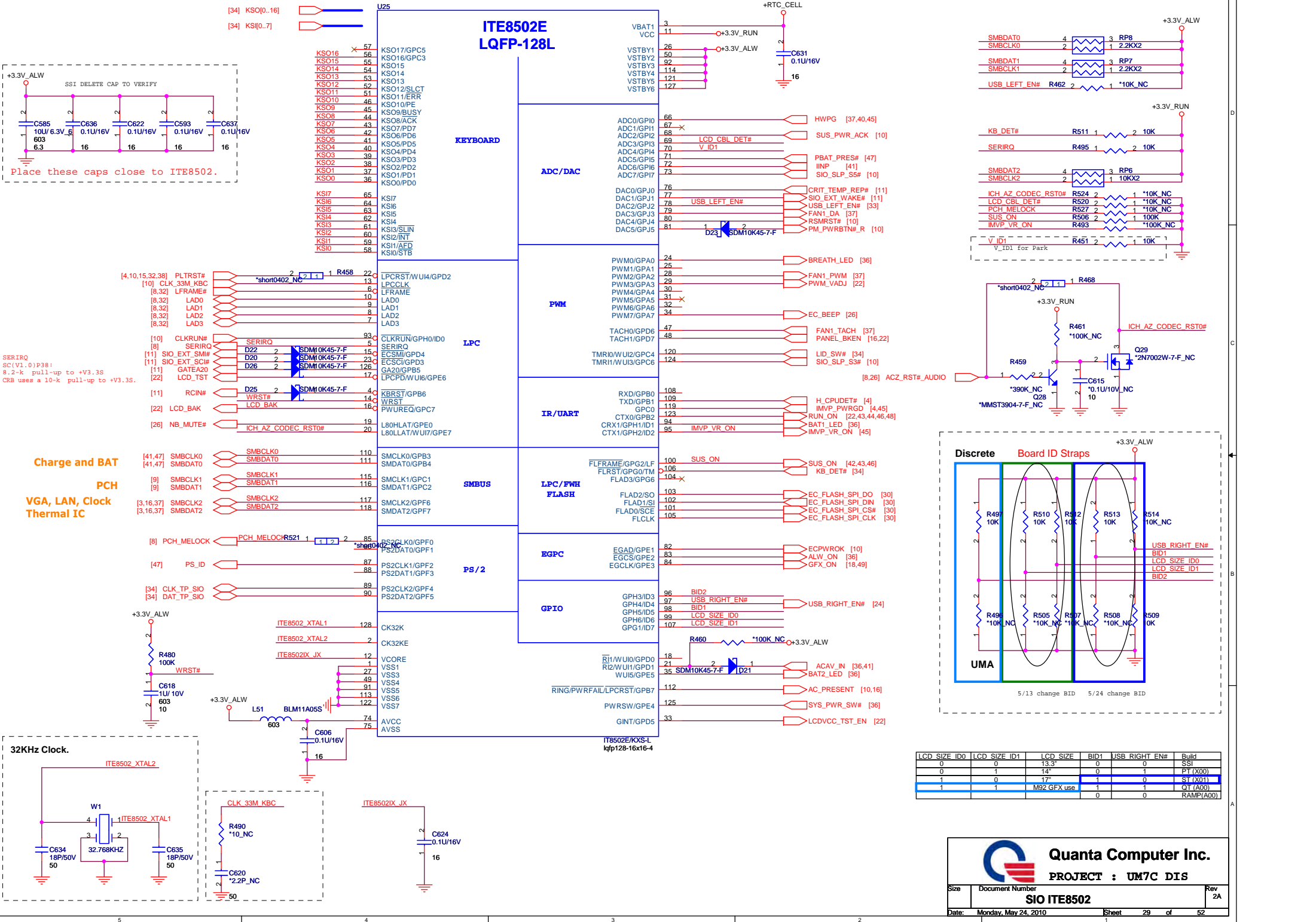
2A

Date: Monday, May 24, 2010

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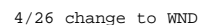


**Quanta Computer Inc.**  
**PROJECT : UM7C DIS**

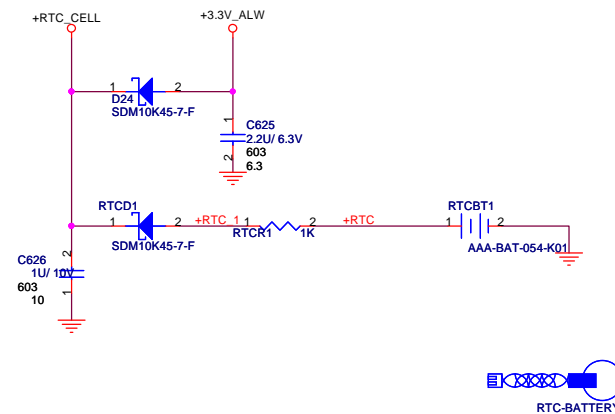


LCD SIZE ID0	LCD SIZE ID1	LCD SIZE	BID1	USB RIGHT EN#	Build
0	0	13.3"	0	0	SSI
0	1	14"	0	1	PT (X00)
1	0	17"	1	0	ST (X01)
1	1	M92 GFX use	1	1	QT (A00)
			0	0	RAMP(A00)

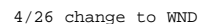
```
[29] EC_FLASH_SPI_CS#
[29] EC_FLASH_SPI_CLK
[29] EC_FLASH_SPI_DIN
[29] EC_FLASH_SPI_DO
```



## +3.3V\_ALW




32Mbit (4M Byte)



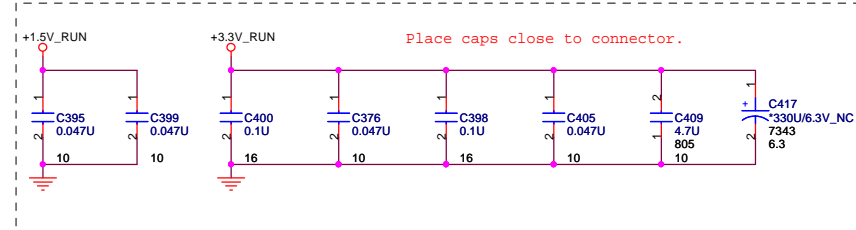
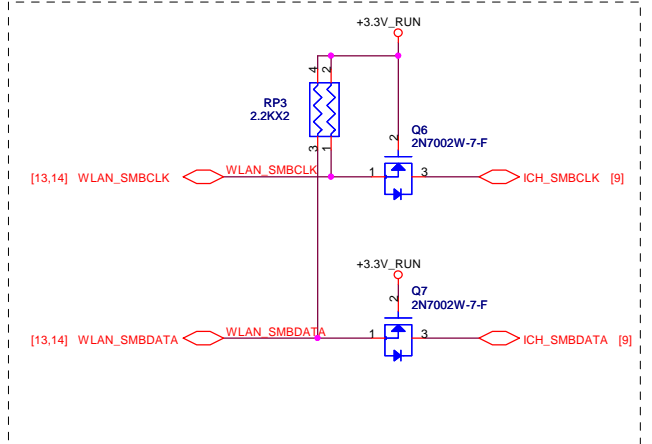
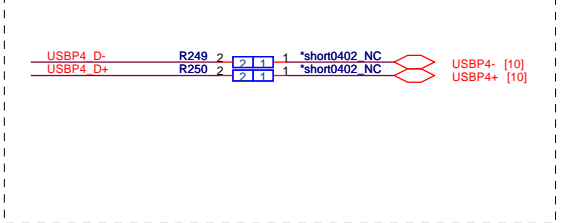
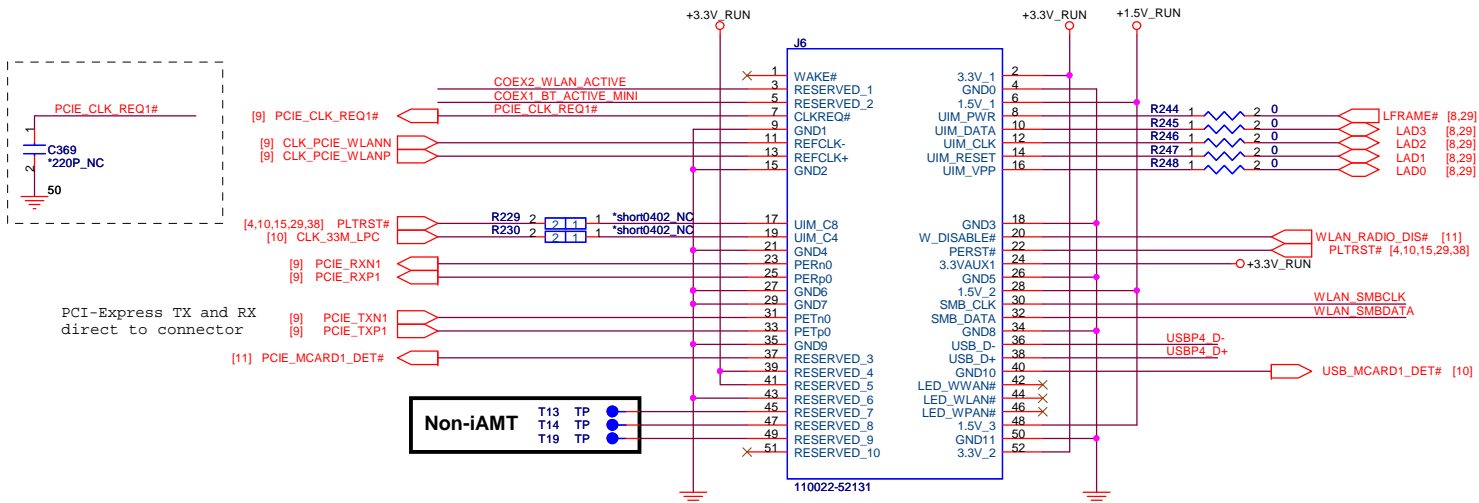
## FLASH/RTC

Rev	2
-----	---

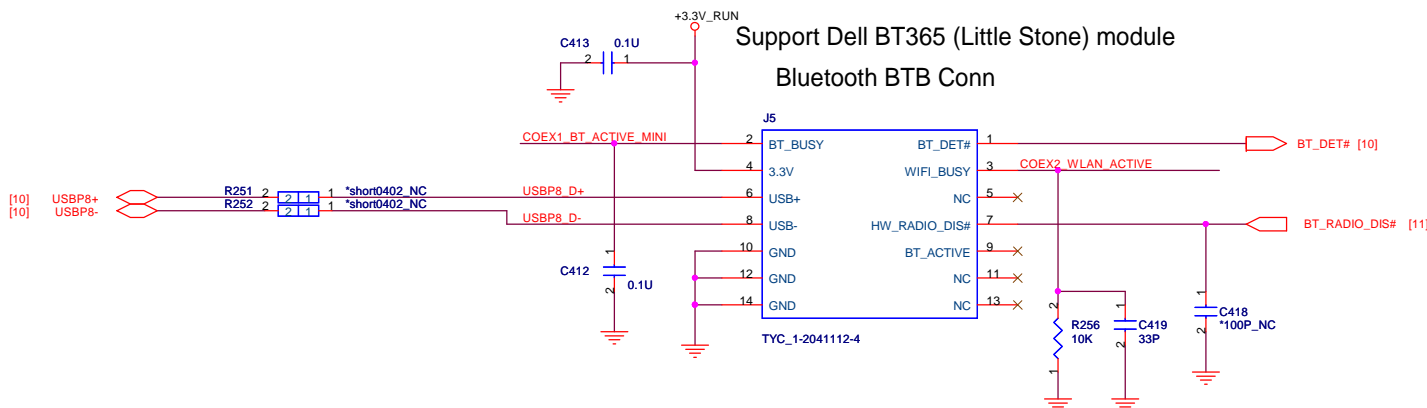


		<b>Quanta Computer Inc.</b>	
		<b>PROJECT : UM7C DIS</b>	
Size	Document Number	Rev	
<b>MINI-Card WWAN</b>		<b>2A</b>	
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# MiniCard WLAN connector



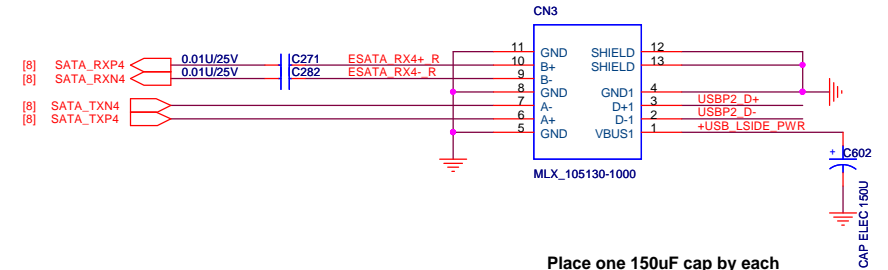
## Support Dell BT365 (Little Stone) module Bluetooth BTB Conn



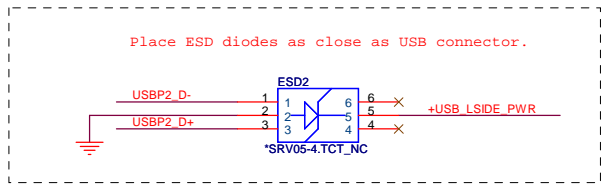
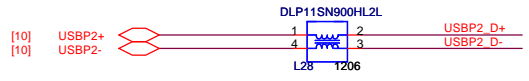
**Quanta Computer Inc.**  
PROJECT : UM7C DIS



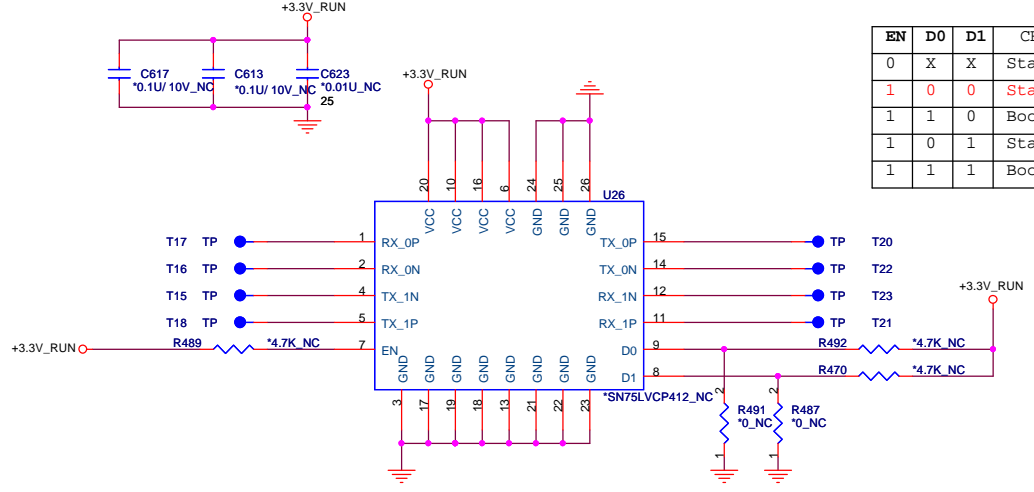
USB and eSATA Conn.



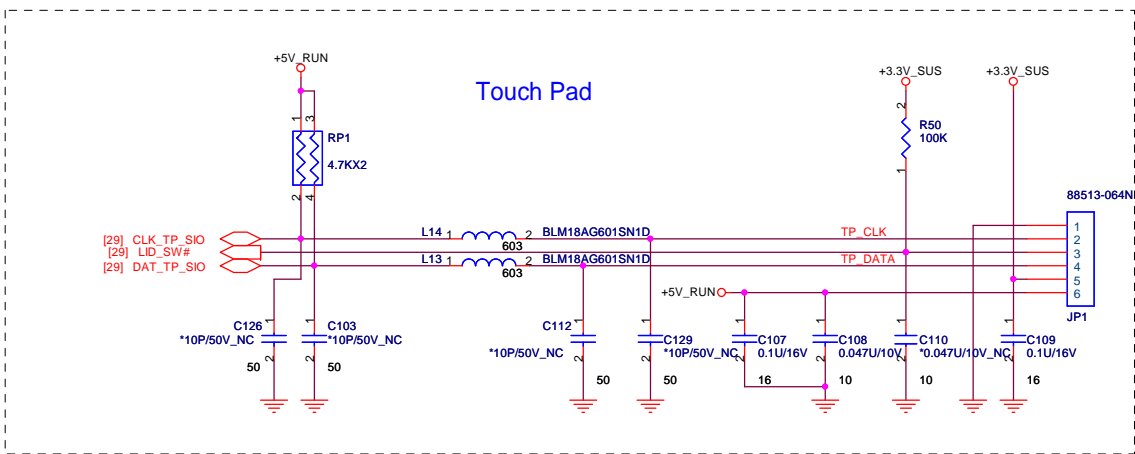
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



E-SATA Re-driver

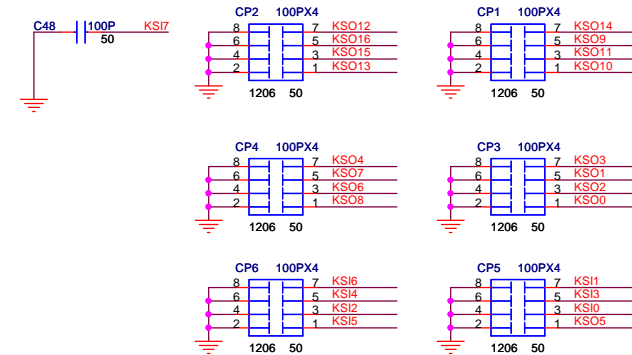
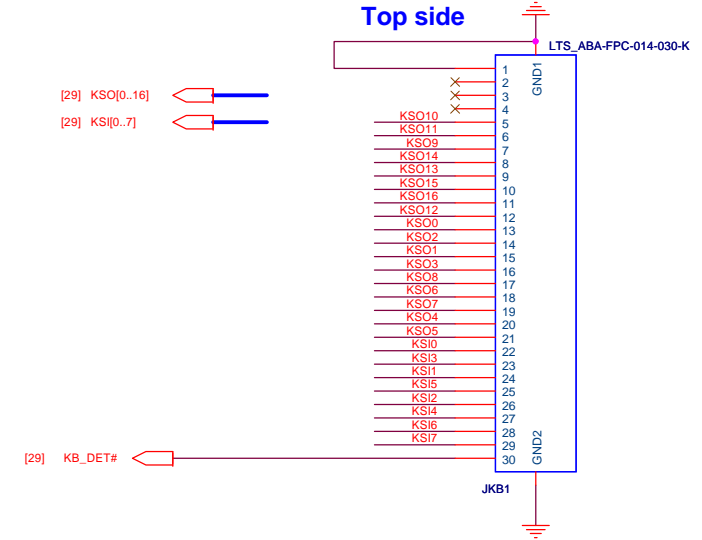


EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost



## KEYBOARD CONNECTOR

Top side



100P CAPS CLOSE TO JKB1

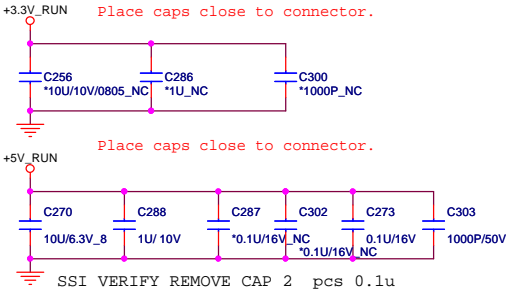
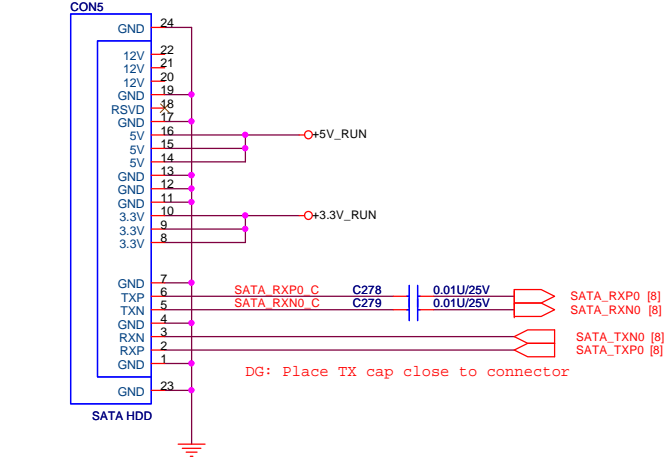


**Quanta Computer Inc.**

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	<b>TOUCH PAD, KB</b>	2A
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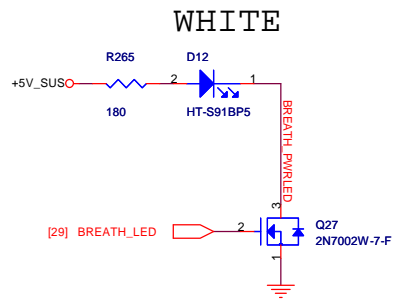
SATA Connector.



# Power

WHITE

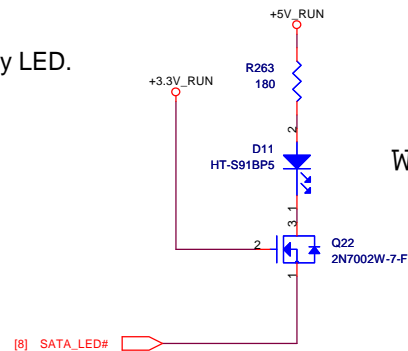
The diagram illustrates the power supply for the WHITE LED. A +5V\_SUS input is connected to a resistor R265 (180 ohms) and the anode of a diode D12 (HT-S91BP5). The cathode of D12 is connected to a red line labeled 'BREATH POWERED'. This line then connects to the gate of a MOSFET Q27 (2N7002W-7-F). The source of Q27 is connected to ground, and its drain is connected to the [29] BREATH\_LED.



HDD activity LED.

WHITE

[8] SATA\_LED#



### Battery

The diagram illustrates a battery status indicator circuit. It features a +5V\_ALW power supply connected to a voltage divider consisting of resistors R260 (240Ω) and R267 (220Ω). The output of this divider is connected to the anodes of two LEDs, D13 (HT-261UD5/BP5), which are labeled AMBER (3:4) and White (2:1). The cathodes of these LEDs are connected to the bases of two NPN transistors, Q8 and Q9 (2N7002W-7-F). The emitters of both transistors are connected to ground. The collectors of Q8 and Q9 are connected to the AMBER and WHITE LEDs, respectively, through resistors R264 and R261 (both 10K\_NC). The AMBER LED is connected to pin [29] BAT2\_LED, and the WHITE LED is connected to pin BAT1\_LED [29].

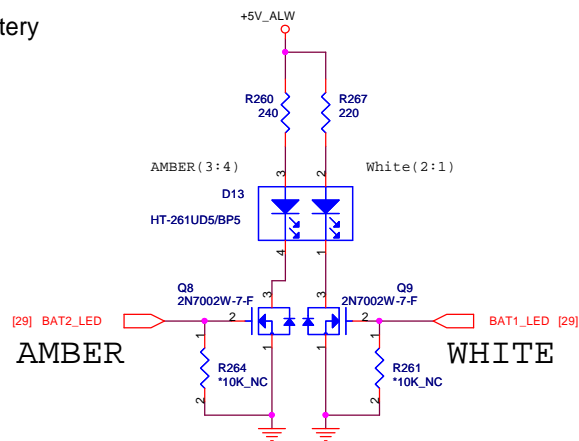
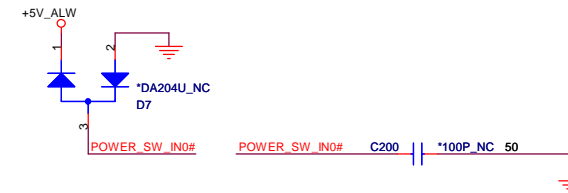
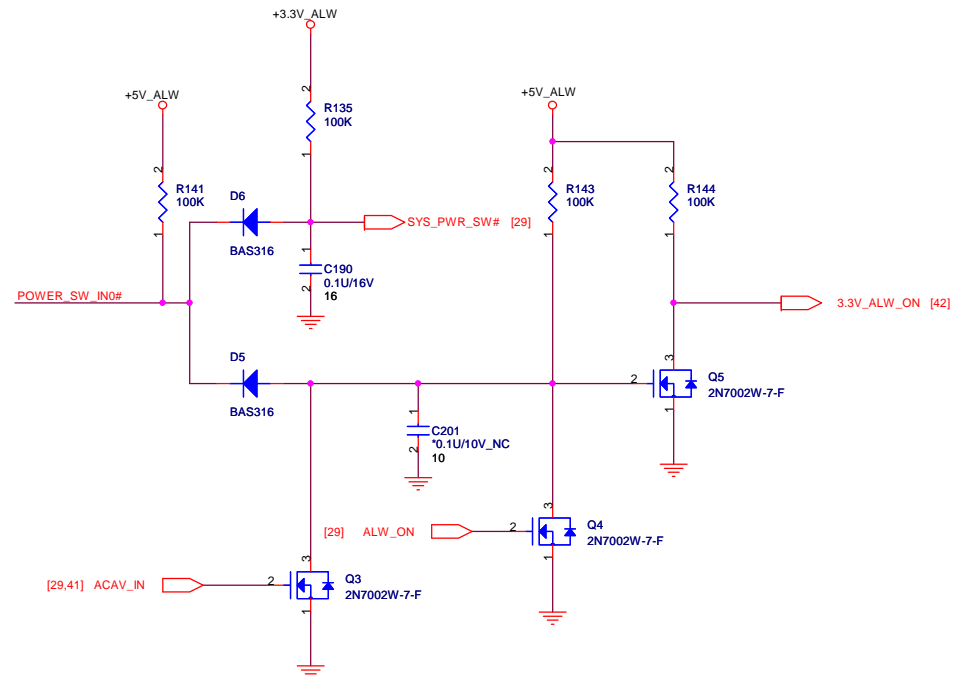
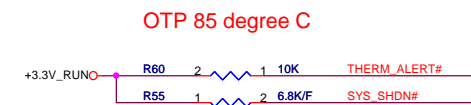
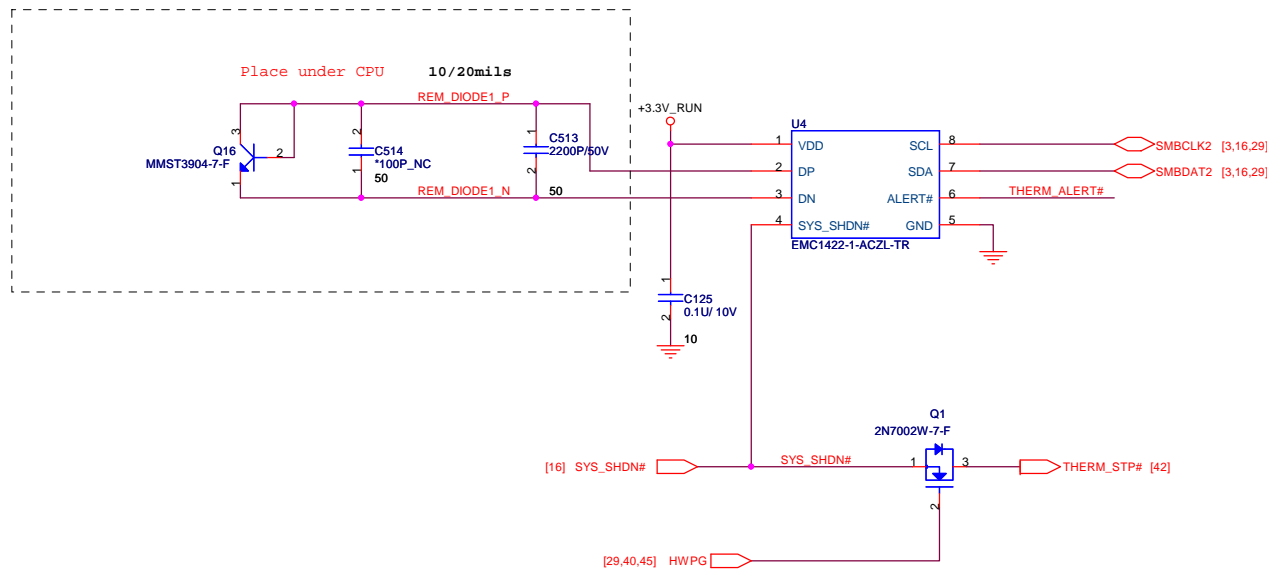
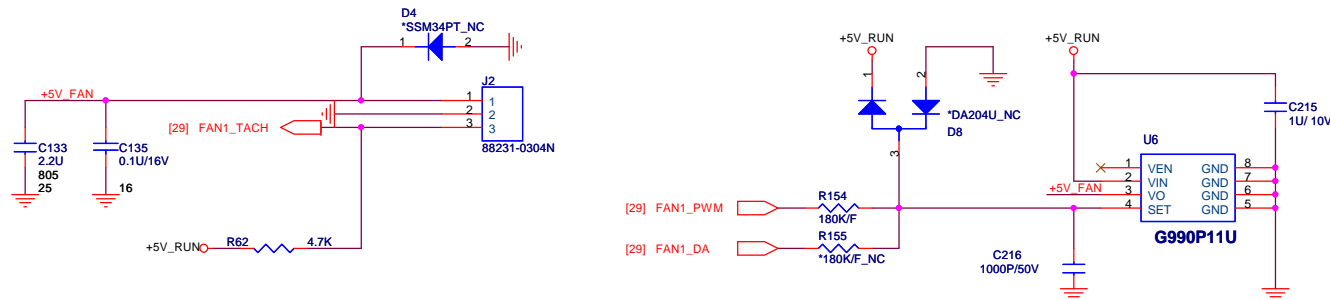


Diagram illustrating the wiring for the 196047-04021 connector:

- Pin 1: +5V SUS
- Pin 2: BREATH PWIRLED
- Pin 3: POWER\_SW IN0#
- Pin 4: Ground



## FAN CONTROL



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Size

Document Number

Rev

**BTB CONN**

2A

Date:

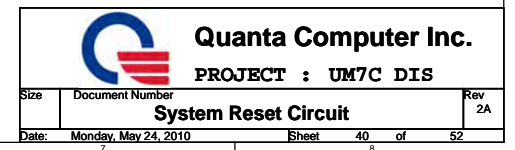
Monday, May 24, 2010

Sheet

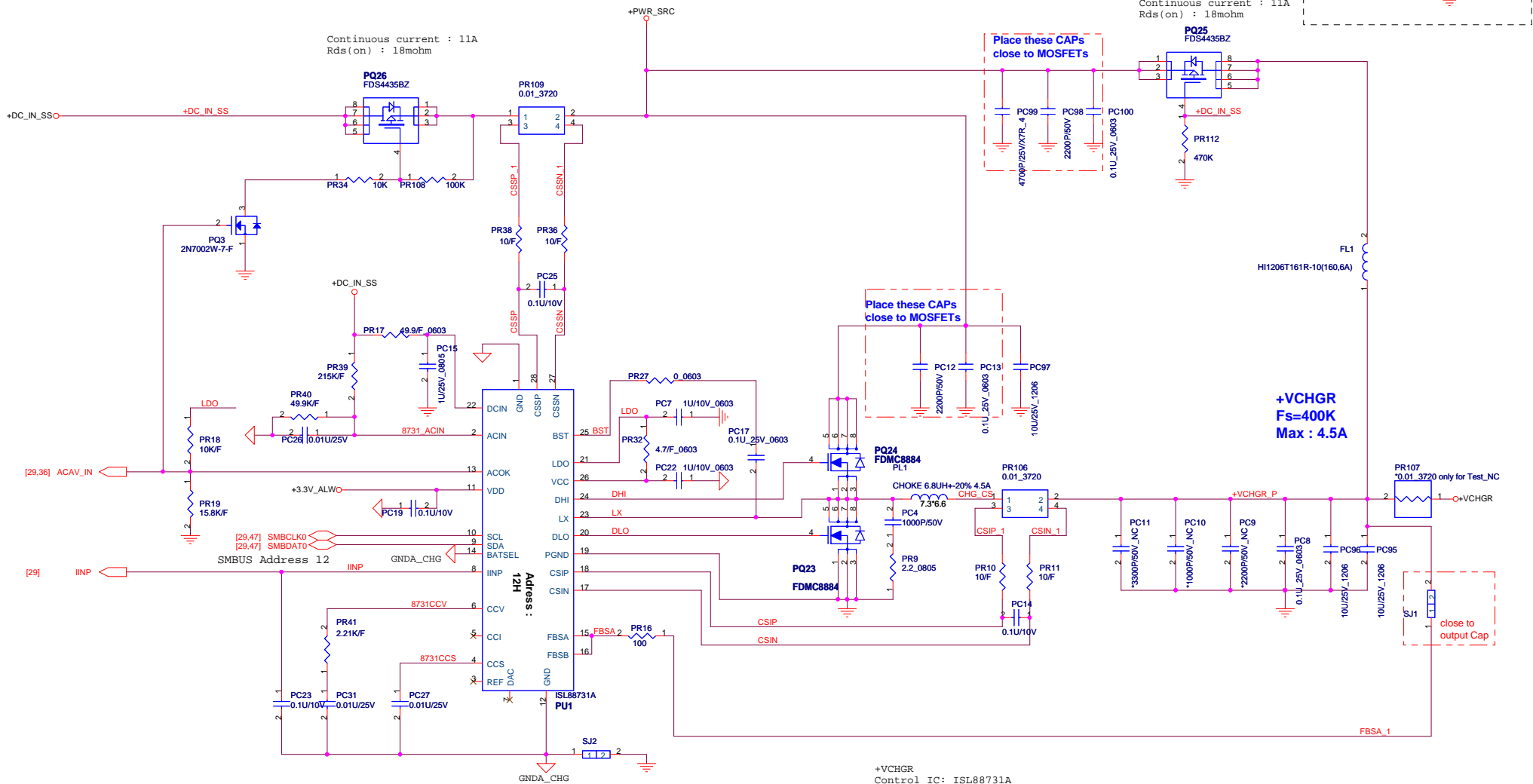
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**+5V\_SUS**  
**Fs=200K**  
**TDC : 4.915A**  
**OCP : 6.881A**

**+3.3V\_ALW**  
**Fs=250K**  
**TDC : 4.477A**  
**OCP : 6.268A**

**+5V\_ALW**  
**Control IC: RT8206B**  
**H/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W**  
**L/S MOSFET: FDS6690AS\_NL(Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W**  
**Inductor: 3.8UH, 30%8A(TPRH10D45F-3R8Y-F02)(TTA), DCR=21mohm**  
**Output Cap: 1\*330U, 6.3V(20%ESR17, 6.3\*5.8)**

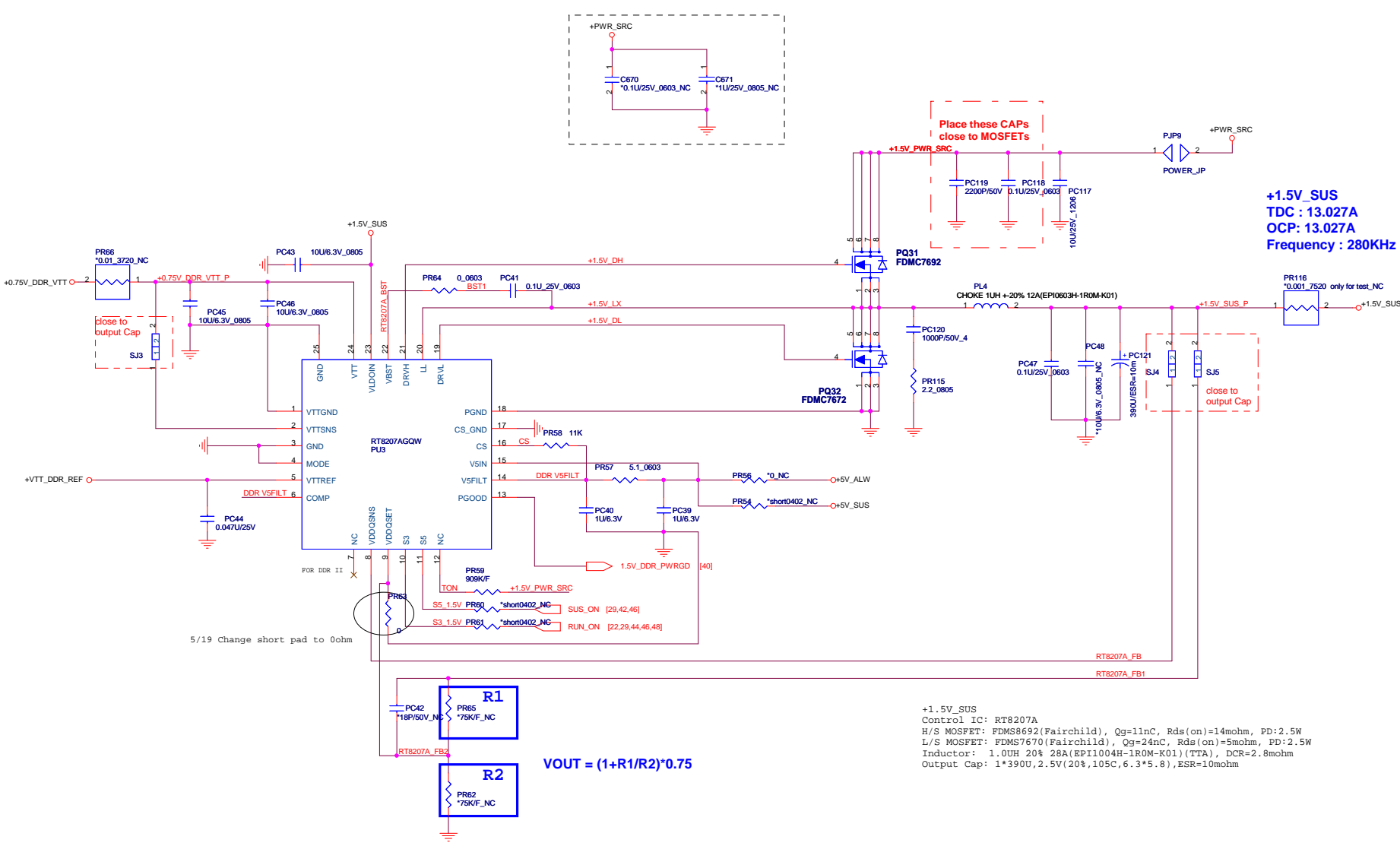
**+3.3V\_ALW**  
**Control IC: RT8206B**  
**H/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W**  
**L/S MOSFET: FDS6690AS\_NL(Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W**  
**Inductor: 3.8UH, 30%8A(TPRH10D45F-3R8Y-F02)(TTA), DCR=21mohm**  
**Output Cap: 1\*330U, 6.3V(20%ESR17, 6.3\*5.8)**

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz



**QUANTA**  
COMPUTER

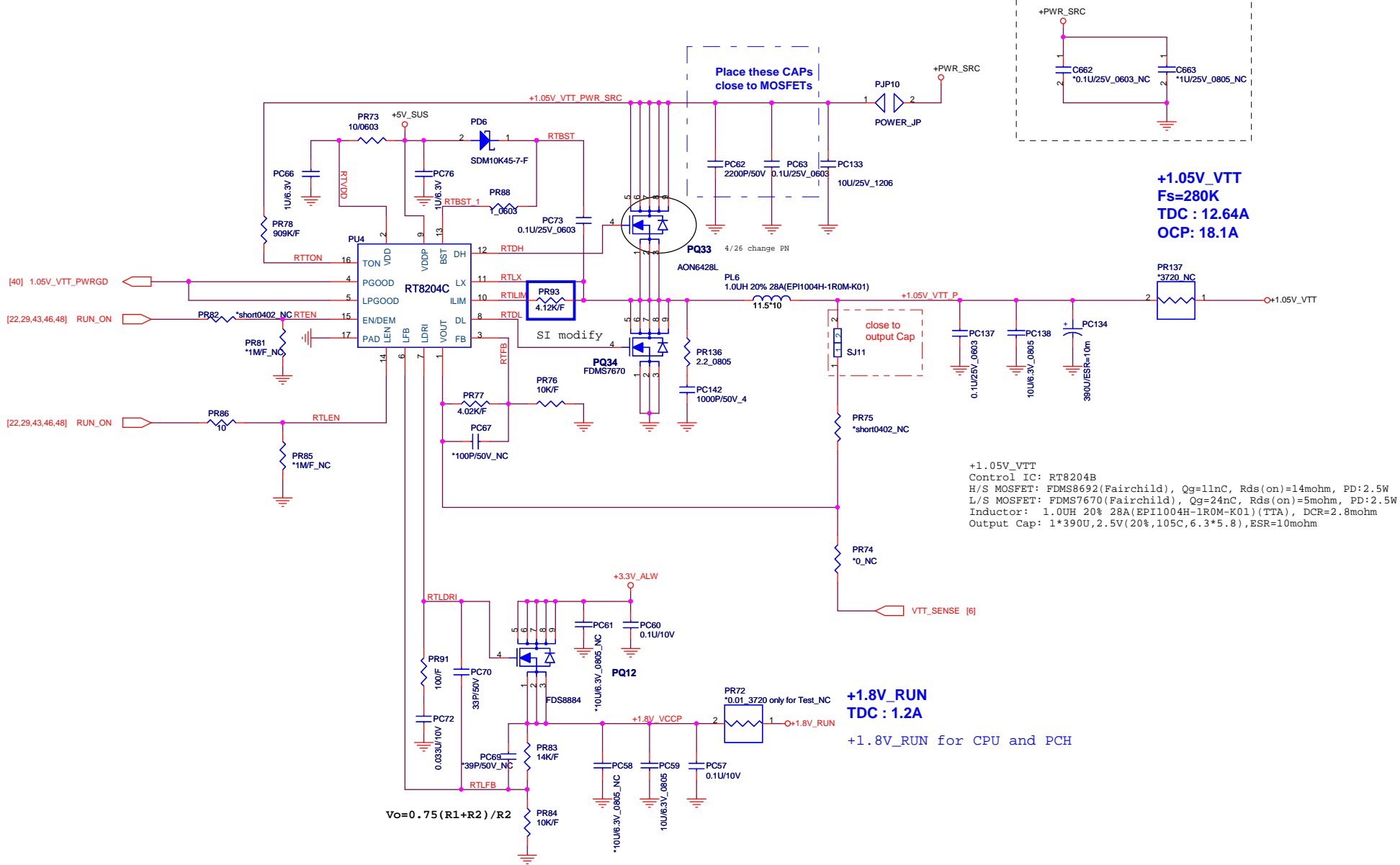
Title		
3.3V_ALW / 5V_ALW(RT8206B)		
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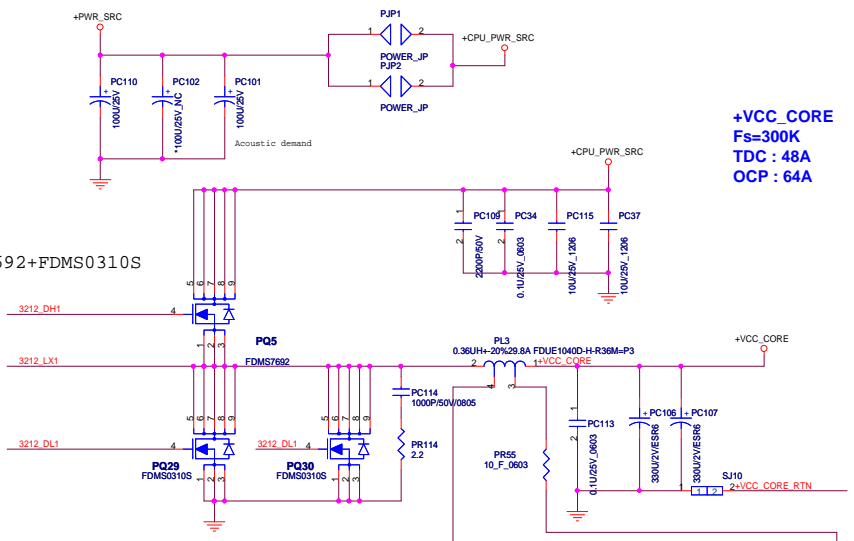
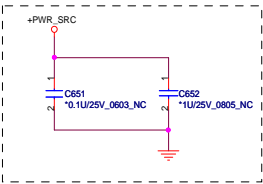
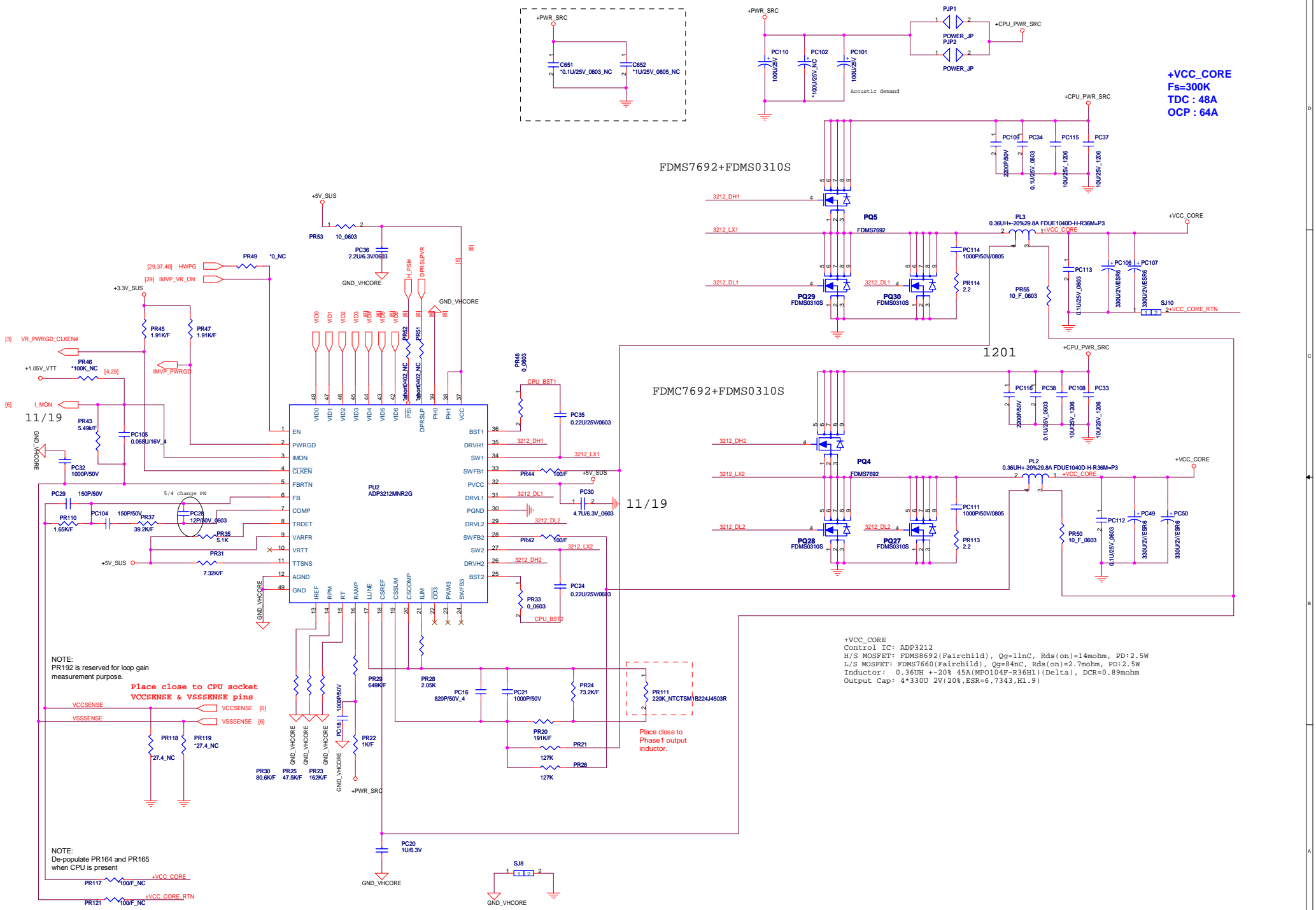
VDDQ and VTT discharge control	
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection				
VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE	
GND	1.5V	VDDQSNS/2	DDR3	
V5IN	1.8V	VDDQSNS/2	DDR2	
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V	

Outputs Management by S3, S5 control					
State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)



Title		
+1.05V_VTT(RT8204B)		
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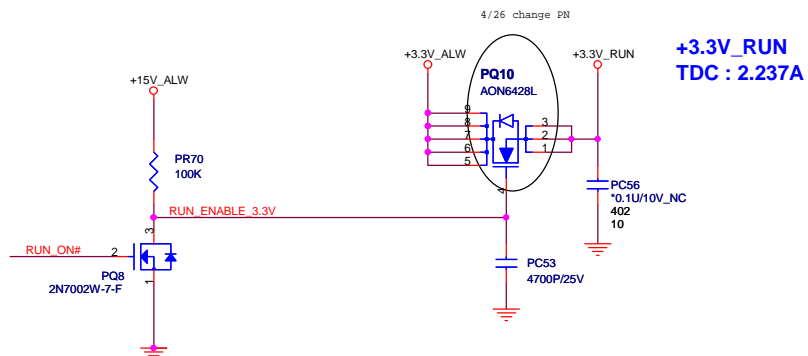
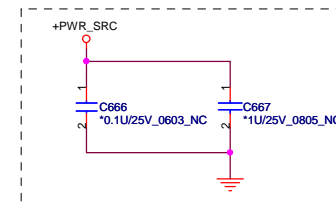
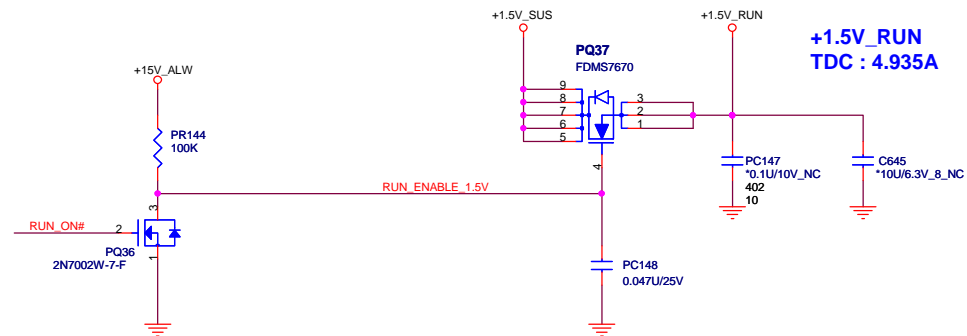
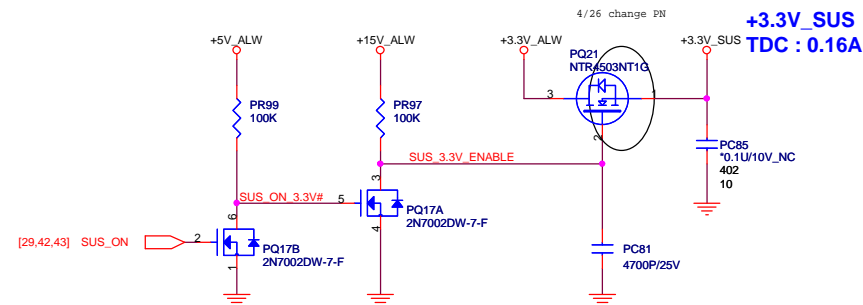
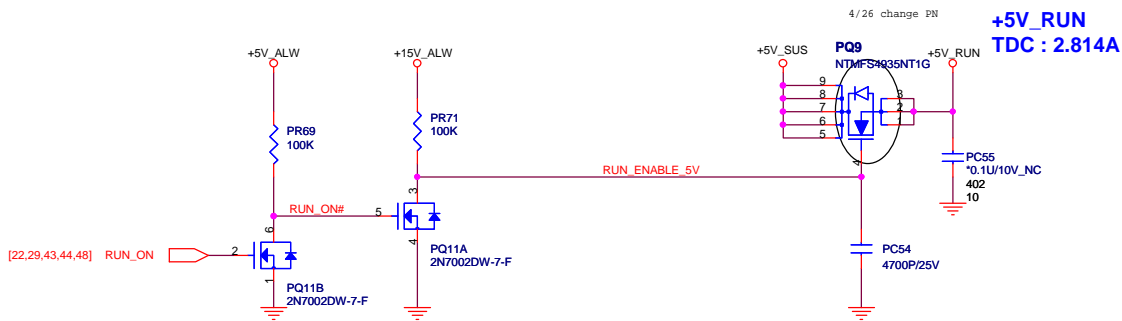
+VCC\_CORE  
Fs=300K  
TDC : 48A  
OCP : 64A

FDMS7692+FDMS0310S

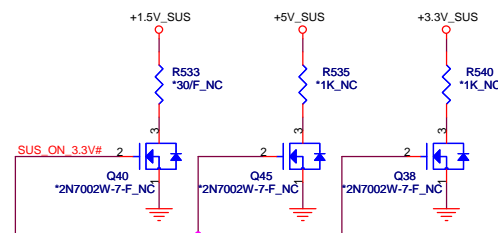
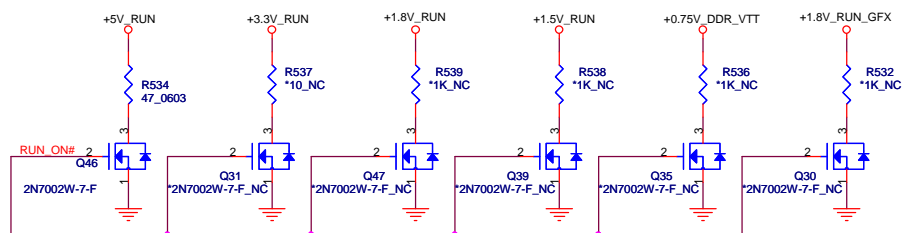
FDMC7692+FDMS0310S

+VCC\_CORE  
Control IC: ADP3212  
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W  
L/S MOSFET: FDMS7660(Fairchild), Qg=84nC, Rds(on)=2.7mohm, PD:2.5W  
Inductor: 0.360H +-20% 45A(MPOL04F-R3611)(Delta), DCR=0.89mohm  
Output Cap: 4\*330U 2V(20%,ESR=6,7343,H1.9)

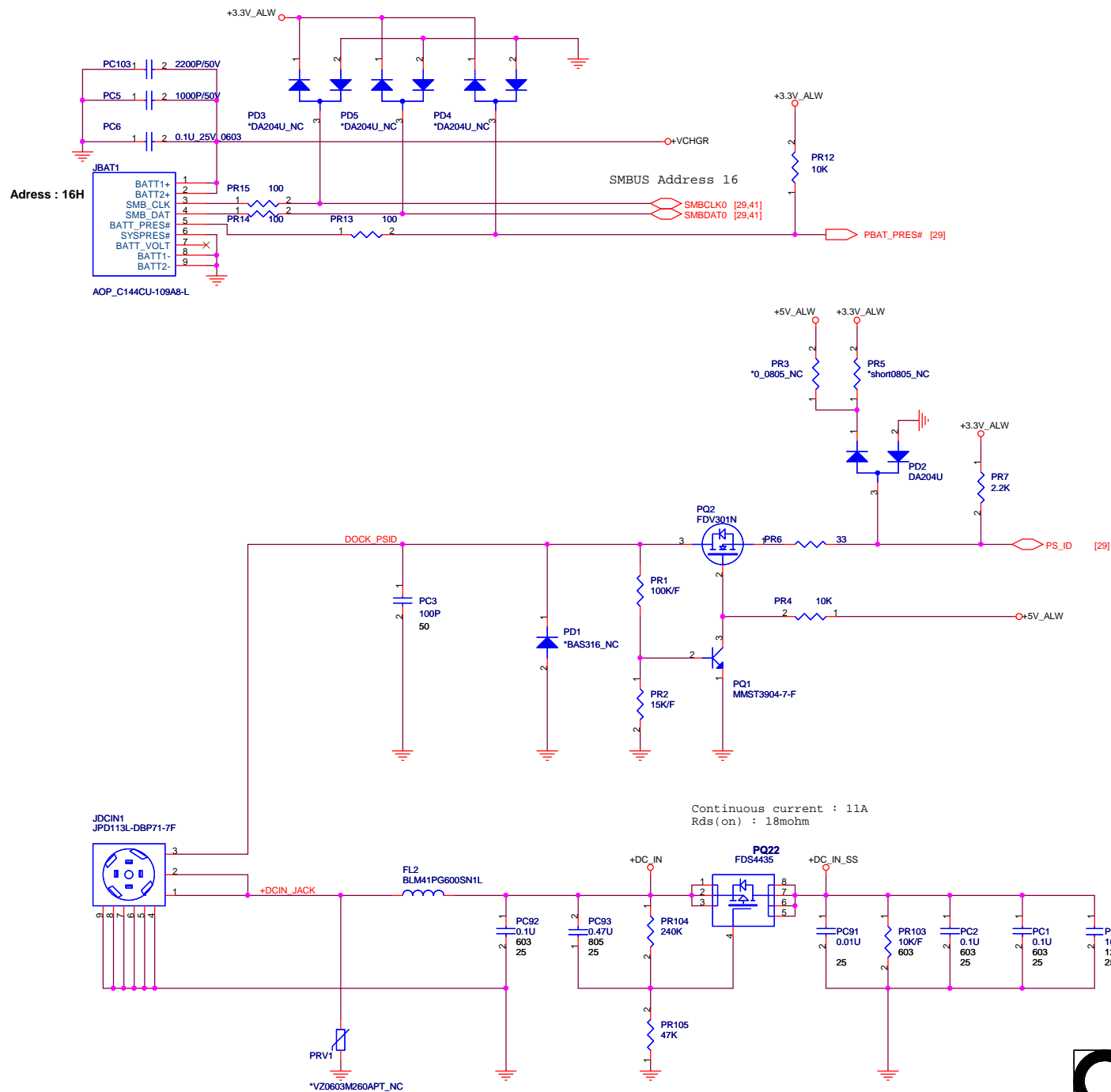
Title		
CPU core (ADP3212MNR2G)		
Size	Document Number	Rev 2A
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### Reserve discharge path



Title			RUN / SUS POWER SW
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Title  
DCIN, BATT CONNECTOR

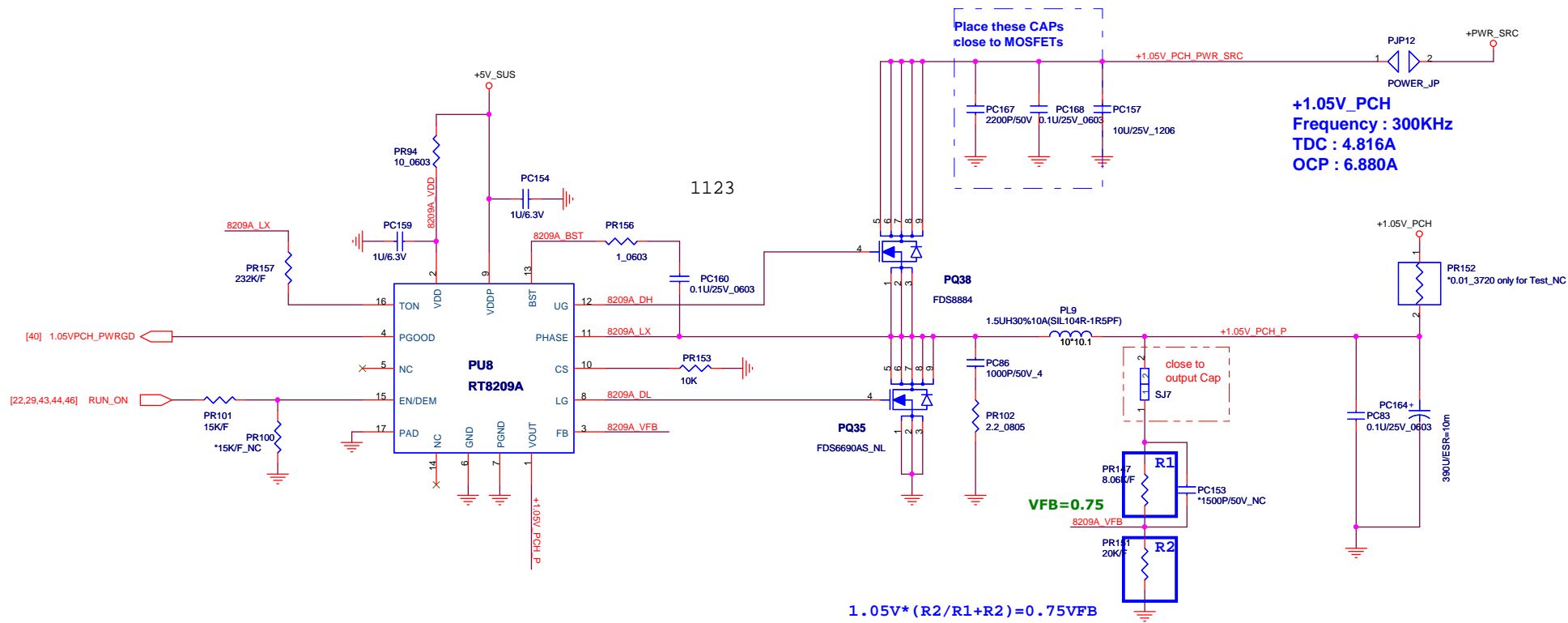
Size  
Document Number  
UM7 Dis

Rev  
2A

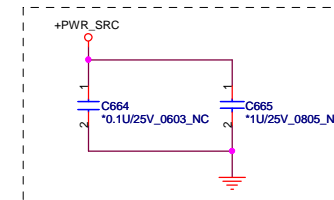
Date: Monday, May 24, 2010

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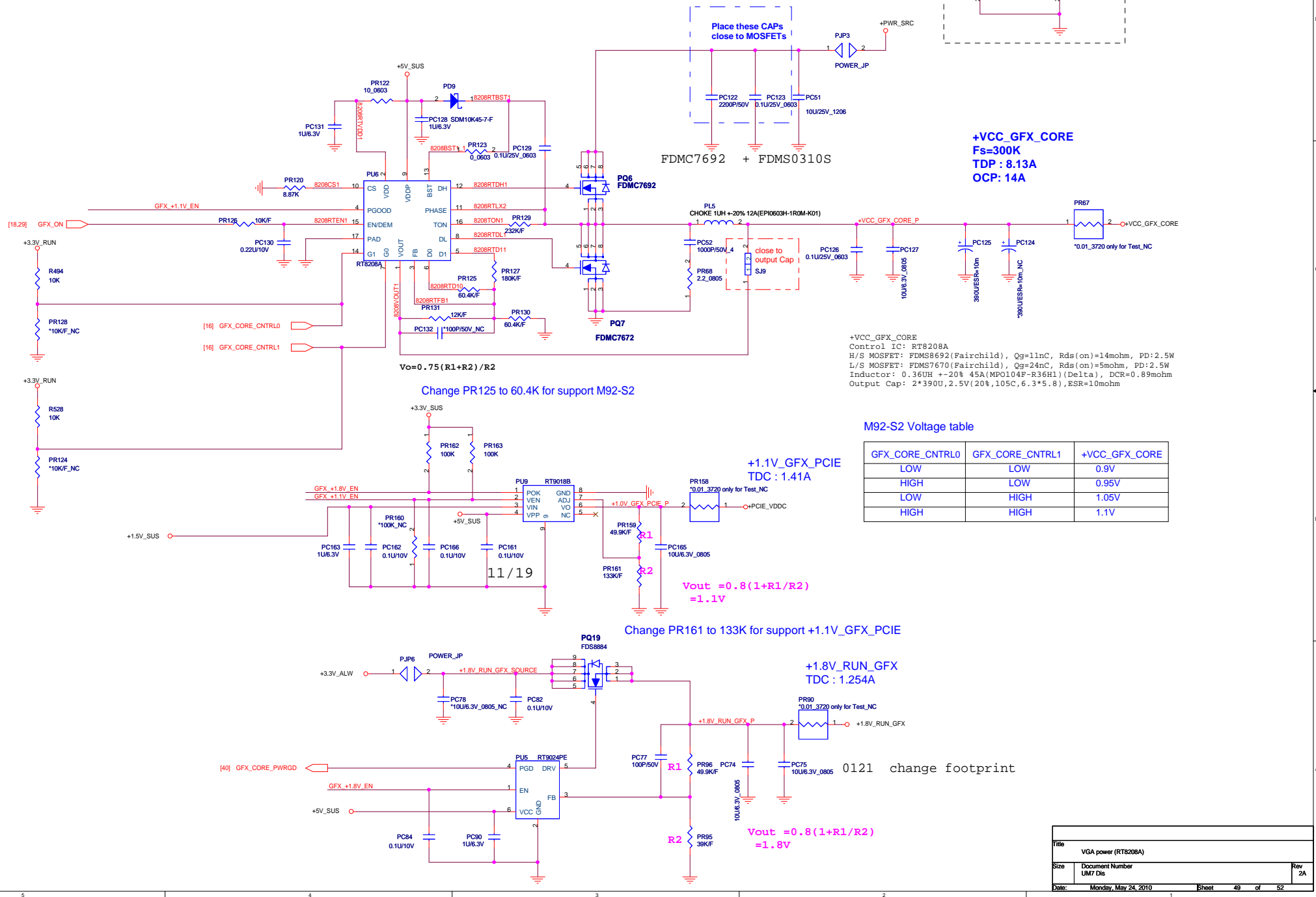


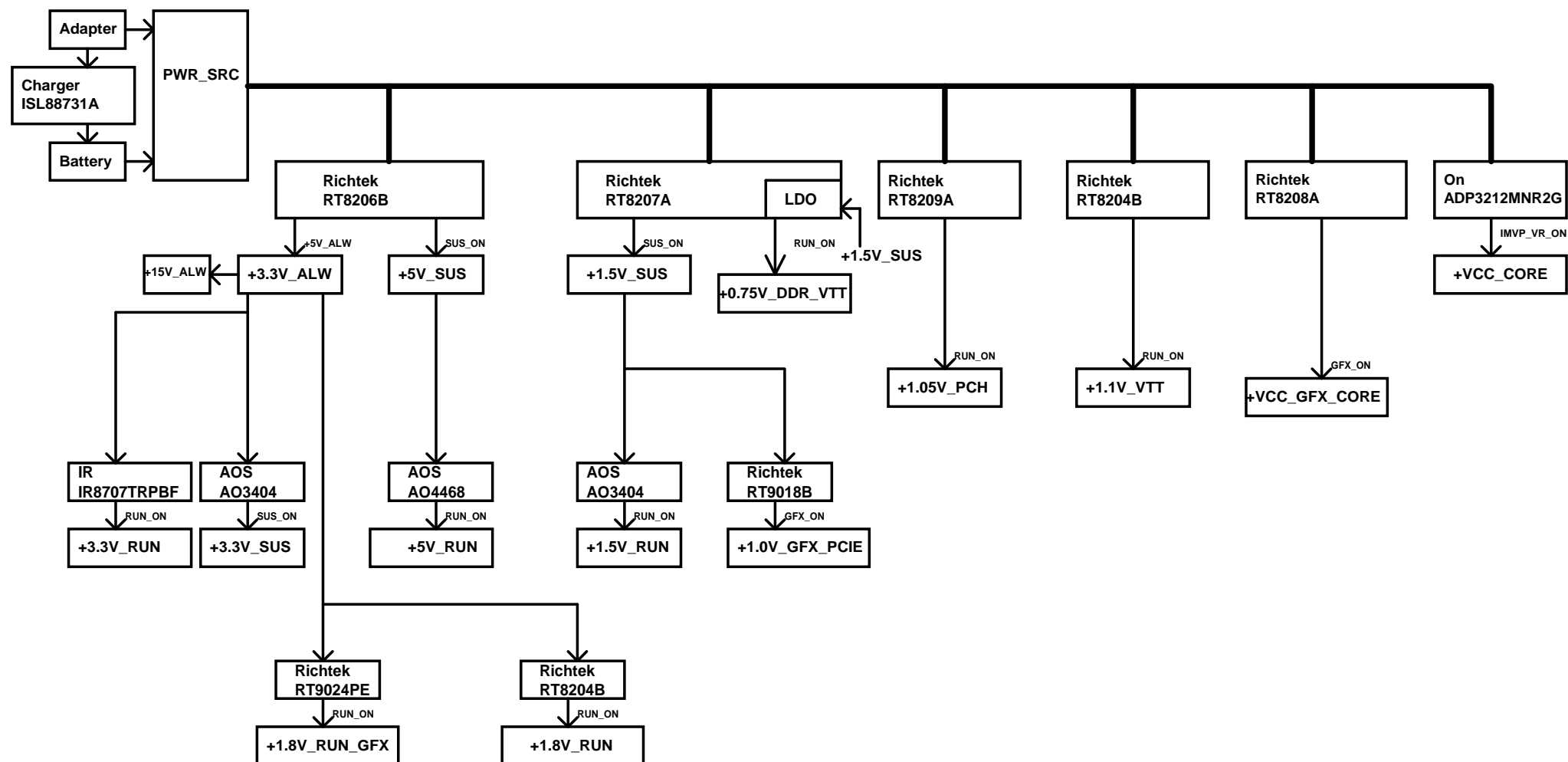


+1.05V\_PCH  
Control IC: RT8209A  
H/S MOSFET: AO4496(AOS), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W  
L/S MOSFET: AO4468(AOS), Qg=12nC, Rds(on)=22mohm, PD:3.1W  
Inductor: 1.5UH+-20% 9A (10D40F-1R5M)(TTA), DCR=10.5mohm  
Output Cap: 1\*390U, 2.5V(20%,105C,6.3\*5.8), ESR=10mohm



Title		
+1.05V_PCH(RT8209A)		
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	Schematic Block Diagram1	2A
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## Power Design Block Diagram 2009/08/24

