

JITR1/R2_DDR3

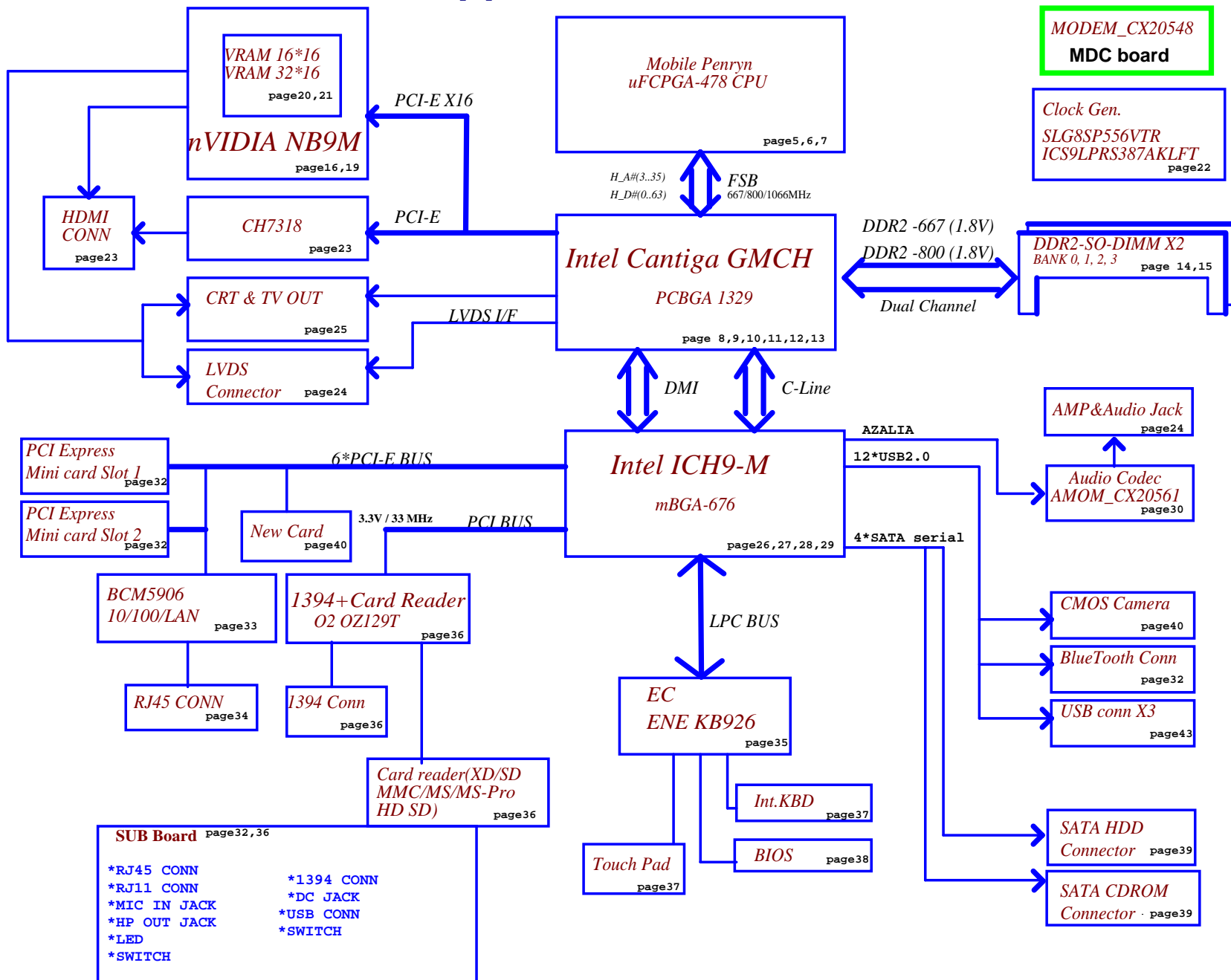
Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM/PM+ICH9-M core logic

Friday, April 18, 2008

REV:1.0

Security Classification	Compal Secret Data			Title		
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Cover Sheet		
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DDR2 Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9VS +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	V	X	X	X	X	X	V	V	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBCLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMICKL_NB HDMIDAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCCLK VGA_DDCDATA	VGA	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	VGA	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT	VGA	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	VGA	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS#_SB FRD#SPI_SO_SB SPI_CLK_SB FWR#SPI_SI_SB	ICH9	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPI_SO SPI_CLK FWR#SPI_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

DDR3 Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

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MB Notes List

JITR1_LA-4141P

VGA and DDR2 Voltage Rails (NB9M-GS)

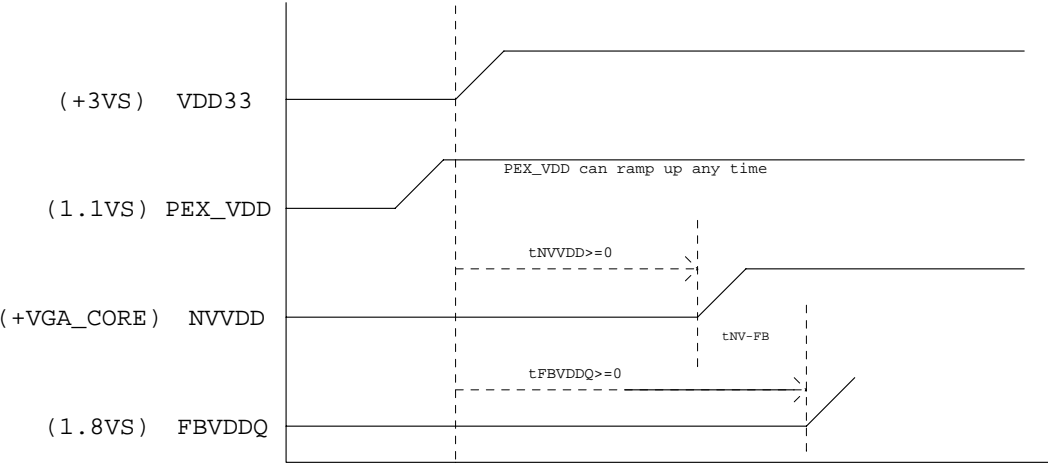
State \ power plane			+1.8V	+3VS +VGA_CORE
	S0	O	O	O
	S1	O	O	O
	S3	O	O	X
	S5 S4/AC	O	O	X
	S5 S4/ Battery only	O	X	X
	S5 S4/AC & Battery don't exist	X	X	X

www.bufanxiu.com EDP at Tj = 97C*

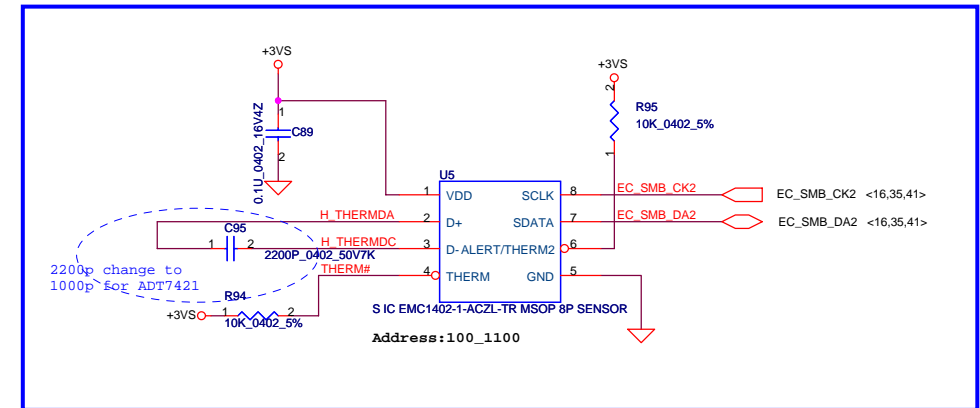
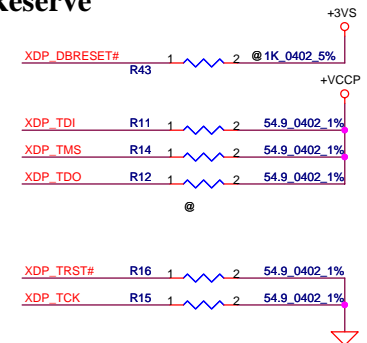
Power Supply Rail		NB9M-GS		NB9M-GE	
(V)		GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	11.22A	10.87A	9.2A	8.88A
FB_DLLAVDD	1.1	25mA			
FB_PLLAVDD	1.1	10mA			
IFPC_IOVDD	1.1	385mA			
IFPD_IOVDD	1.1	385mA			
IFPE_IOVDD	1.1	385mA			
IFPF_IOVDD	1.1	385mA			
PEX_IOVDD/Q	1.1	1550mA			
PEX_PLLVDD	1.1	165mA			
PLLVD	1.1	55mA			
SP_PLLVDD	1.1	25mA			
VID_PLLVDD	1.1	50mA			
TOTAL	1.1	3.425A			
FBVDD/Q	1.8	2.24A	1.65A	2.17A	1.63A
IFPA_IOVDD	1.8	50mA			
IFPB_IOVDD	1.8	50mA			
IFPAB_PLLVDD	1.8	100mA			
IFPCD_PLLVDD	1.8	160mA			
IFPEF_PLLVDD	1.8	160mA			
TOTAL	1.8	2.76A	2.17A	2.69A	2.15A
DACA_VDD	3.3	110mA			
DACB_VDD	3.3	125mA			
DACC_VDD	3.3	110mA			
MIOA_VDDQ	3.3	10mA			
MIOB_VDDQ	3.3	10mA			
VDD33	3.3	80mA			
TOTAL	3.3	0.445A			

POWER SQUENCE

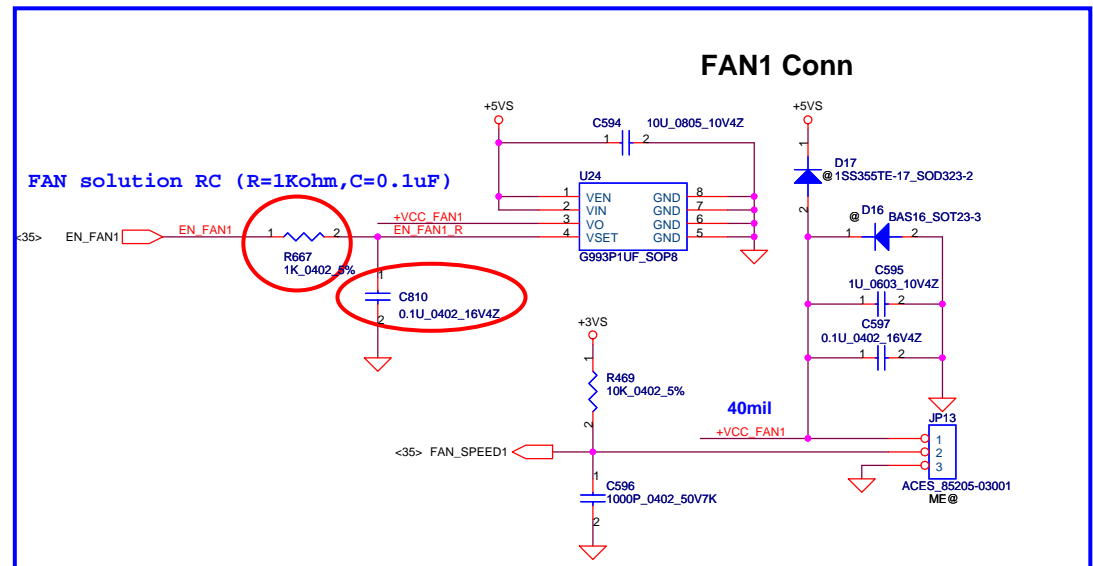
The ramp time for any rail must be more than 40us



XDP Reserve



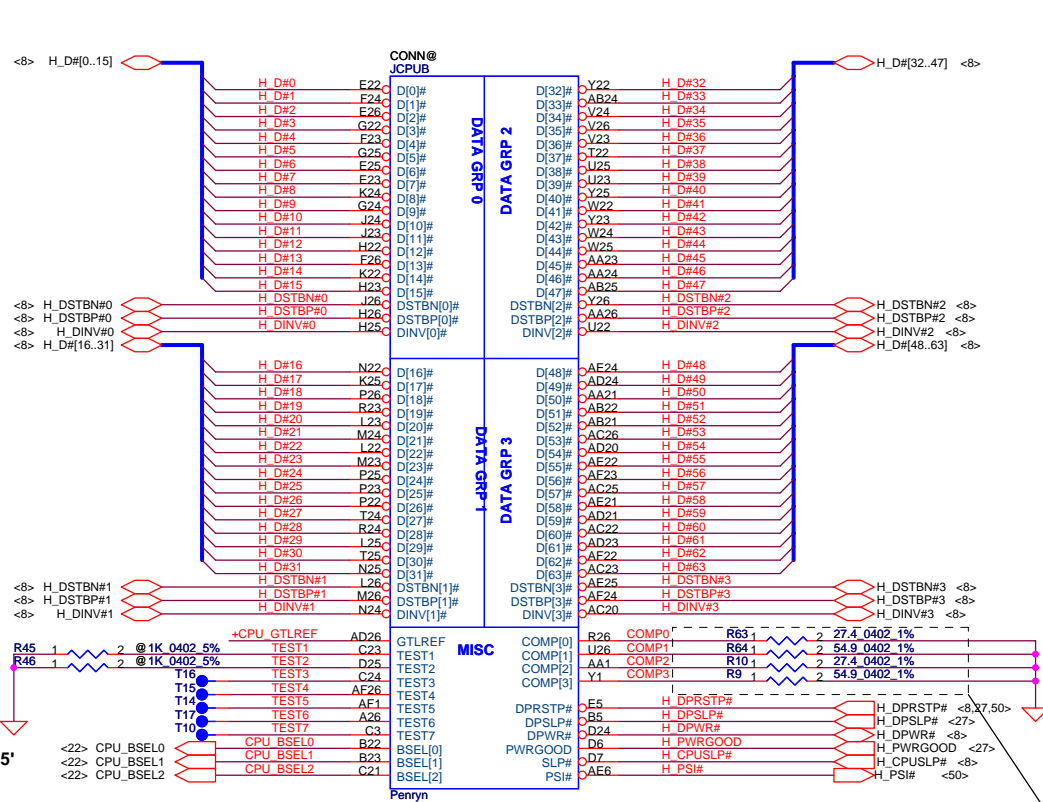
FAN1 Conn



H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

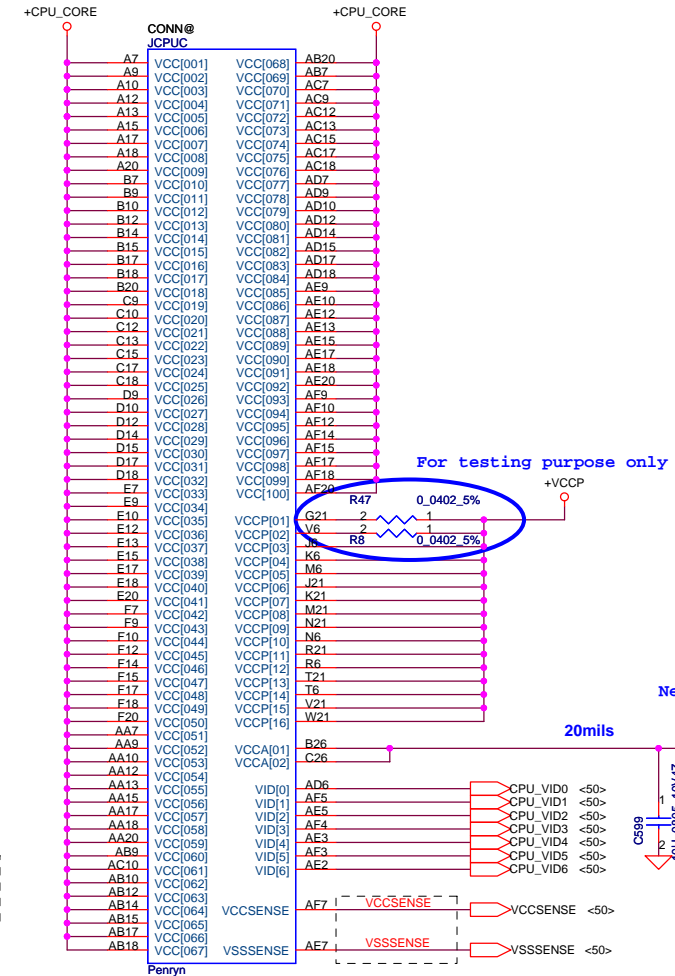
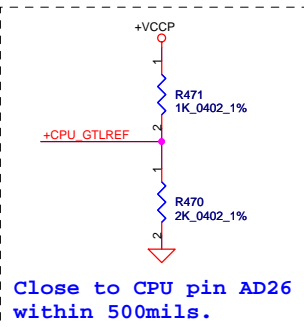
RSVD pins on the CPU
should be left as NO
CONNECT

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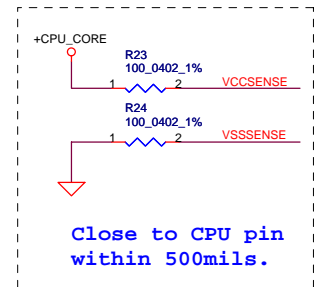
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

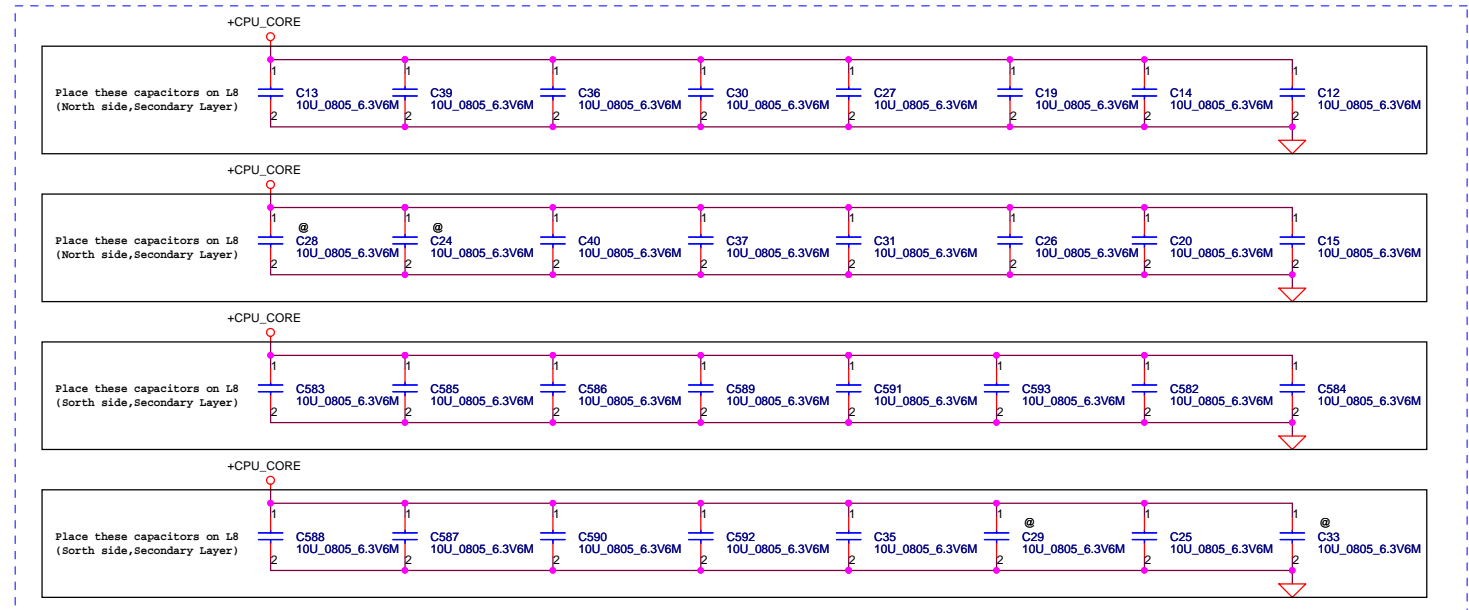
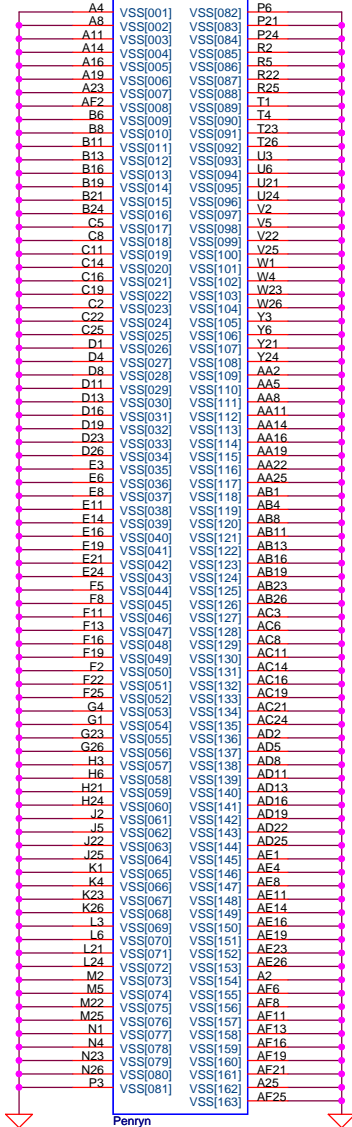


Length match within 25 mils.
The trace width/space/other is
16/7/25.

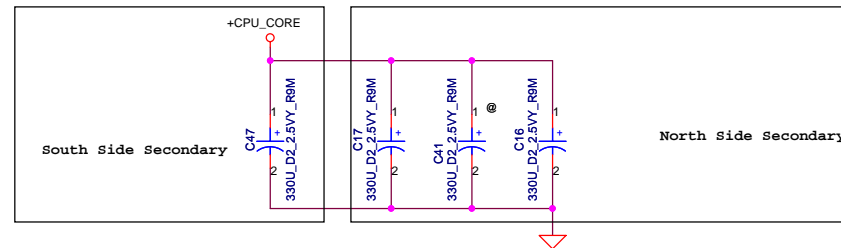
Layout Note:
Route VCCSENSE and VSSSENSE traces at
27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.



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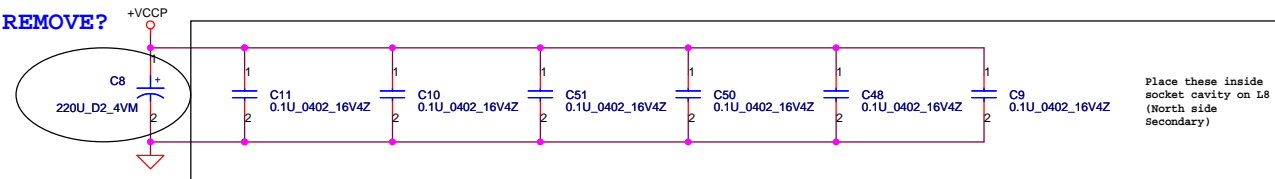
CONN@
JCPU

Mid Frequency Decoupling

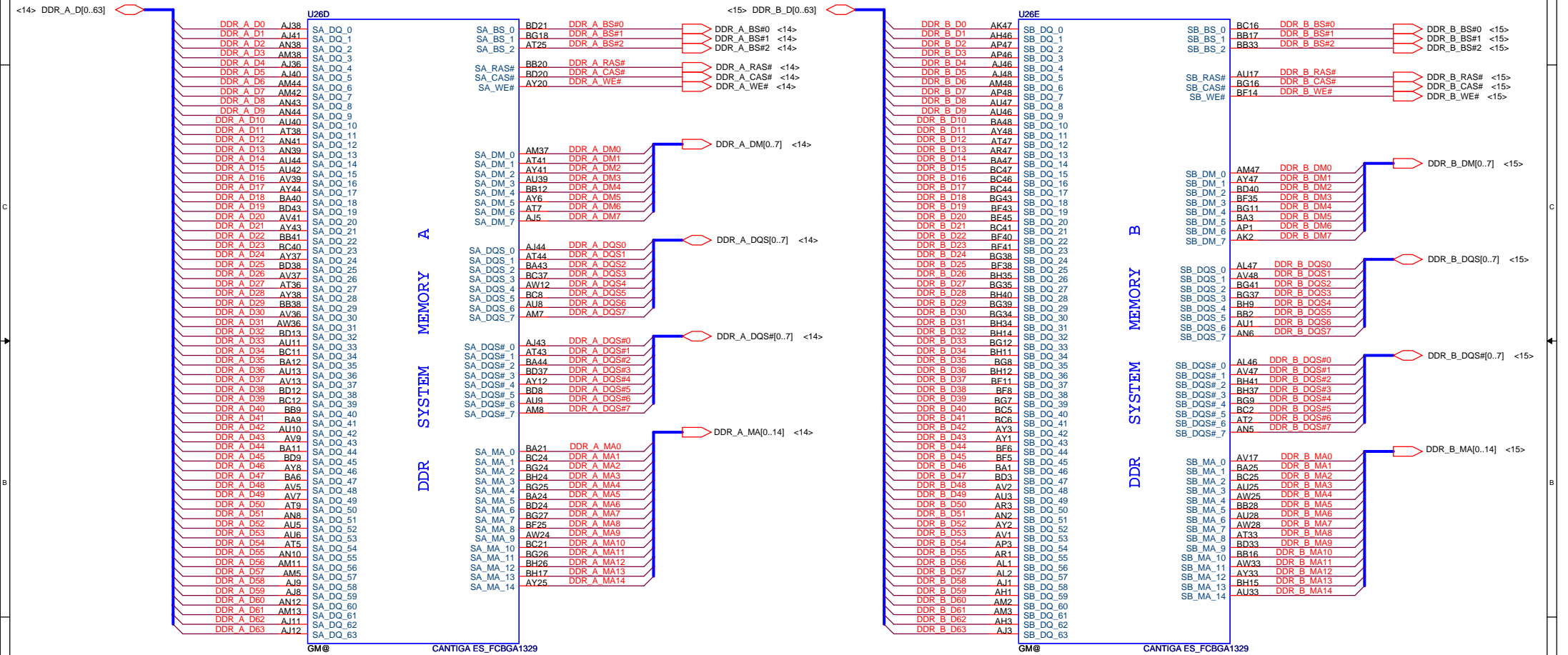


ESR <= 1.5m ohm
Capacitor > 1980uF

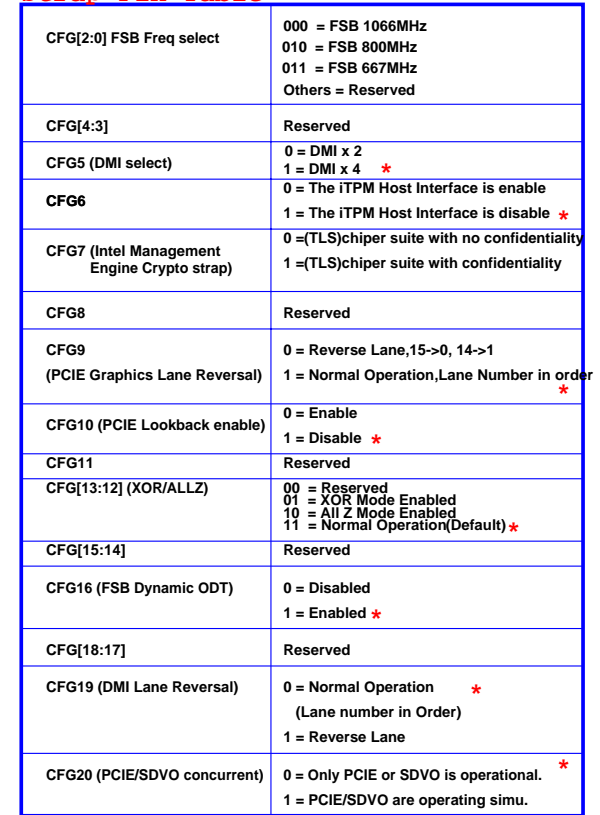
REMOVE?



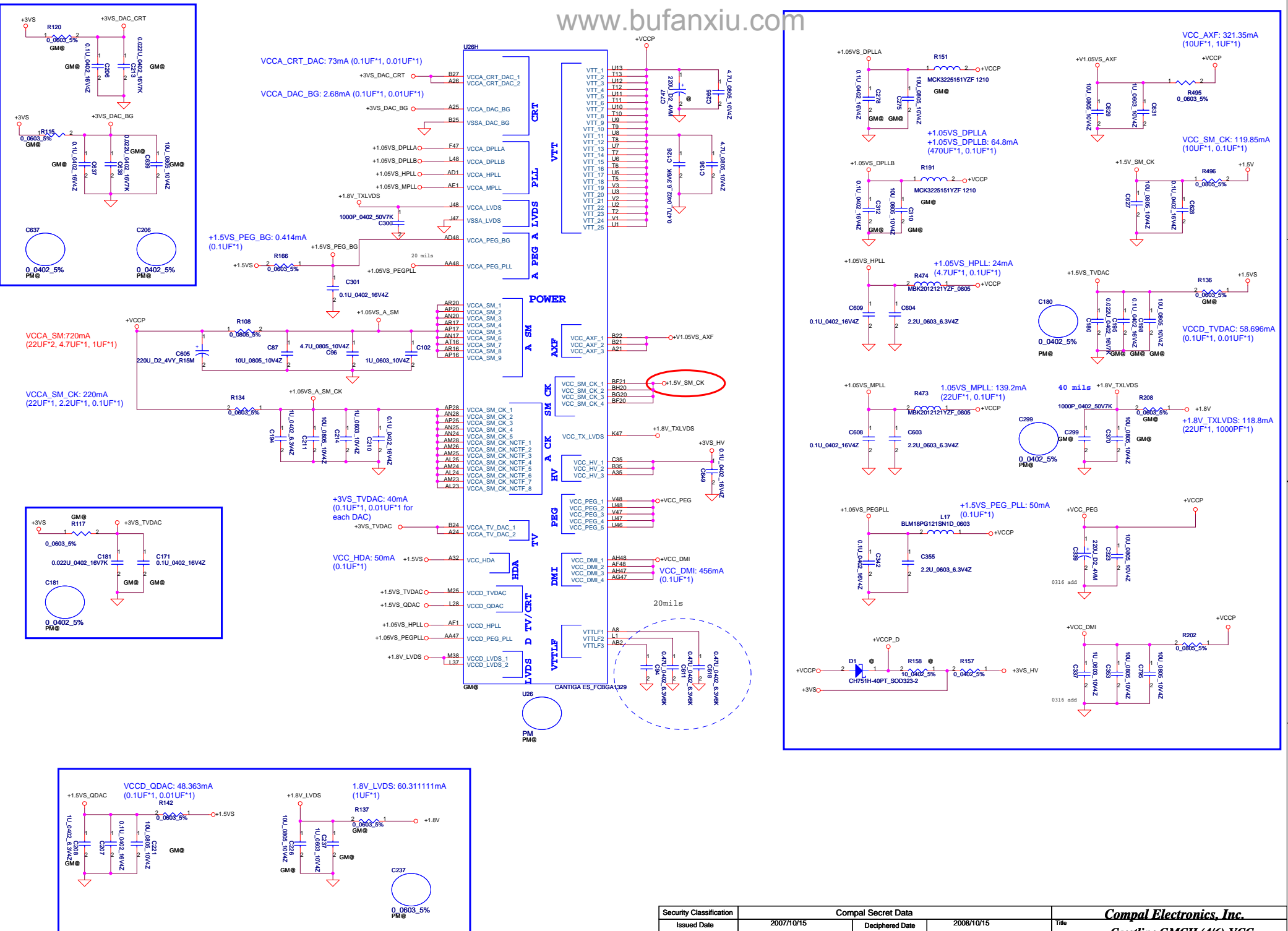
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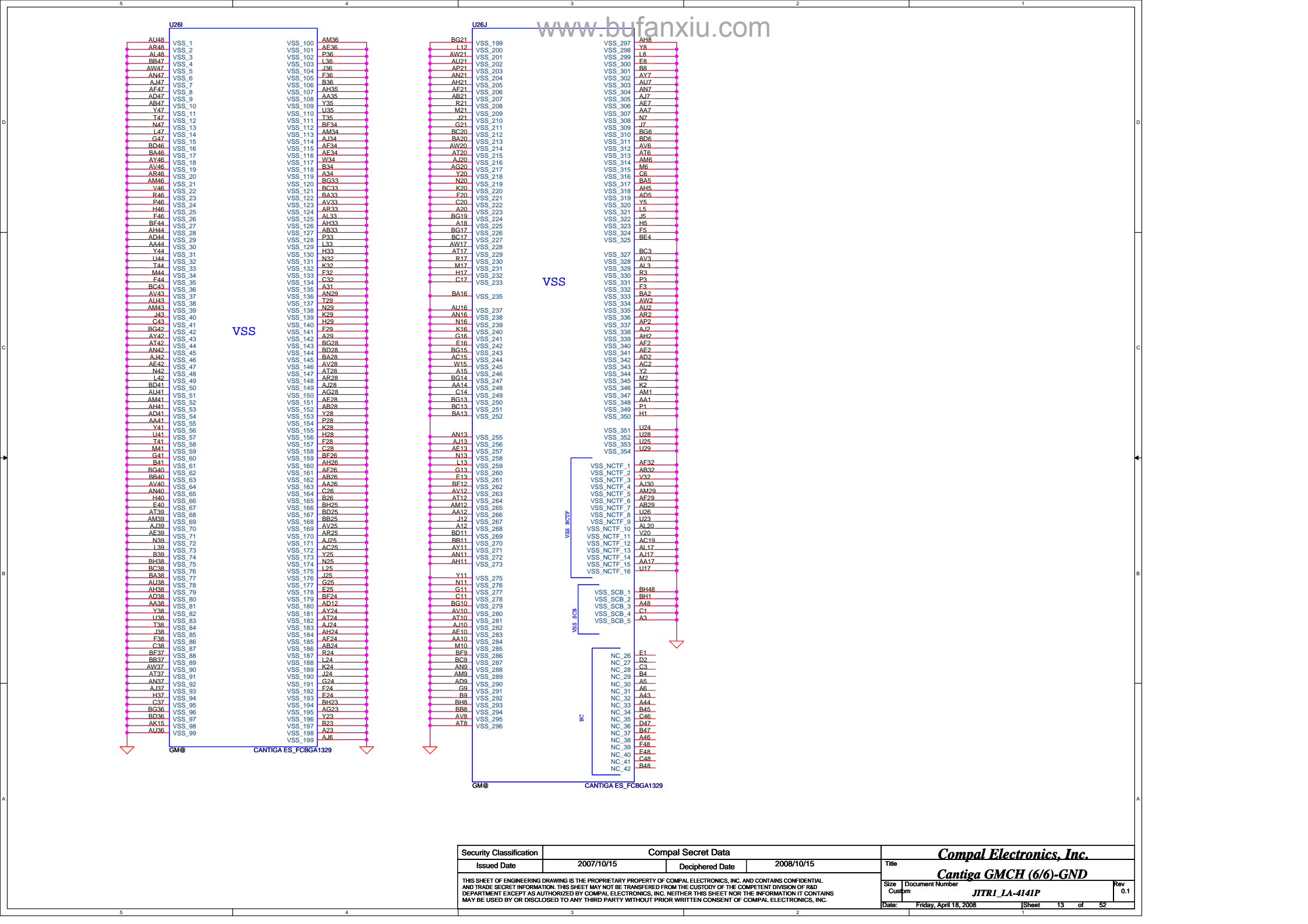


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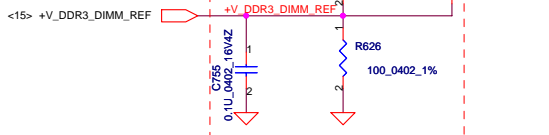
Security Classification		Compal Secret Data		Compal Electronics, Inc. Cantiga GMCH (3/6)-VGA/LVDS/TV	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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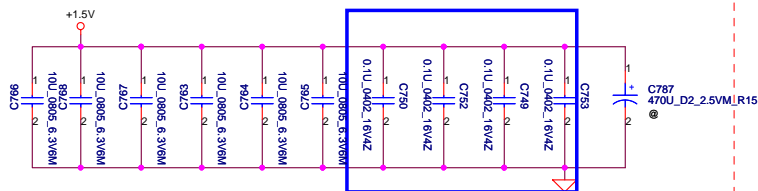
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<9> DDR_A_DQS#[0..7]
<9> DDR_A_D[0..63]
<9> DDR_A_DM[0..7]
<9> DDR_A_DQS[0..7]
<9> DDR_A_MA[0..14]

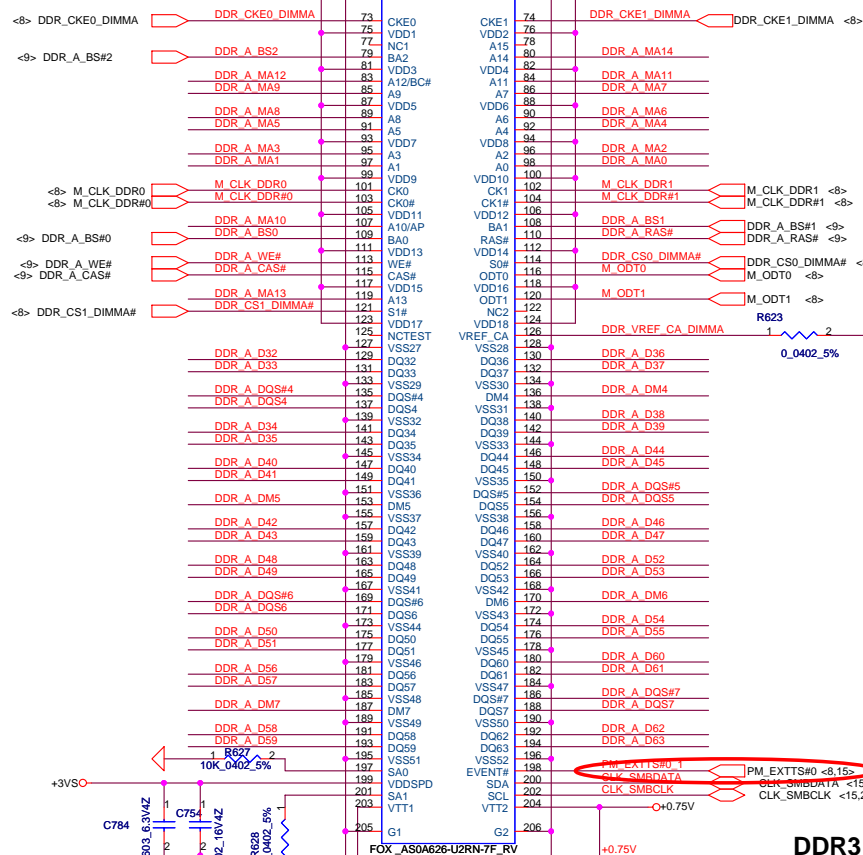
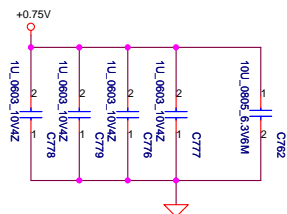


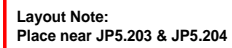
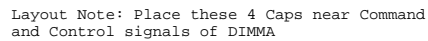
Layout Note:
Place near JP4

Layout Note: Place these 4 Caps near Command
and Control signals of DIMM



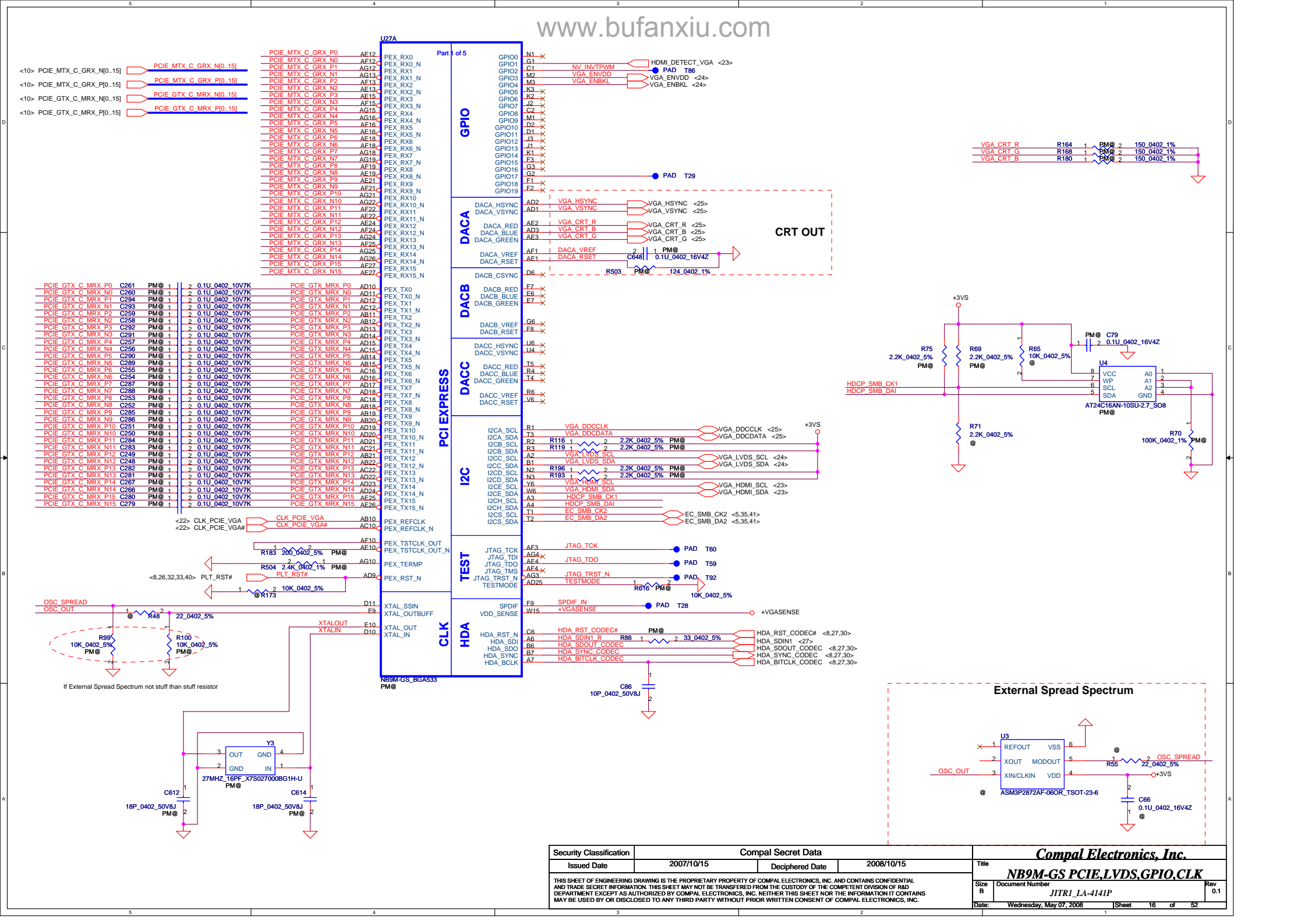
Layout Note:
Place near JP4.203 & JP4.204

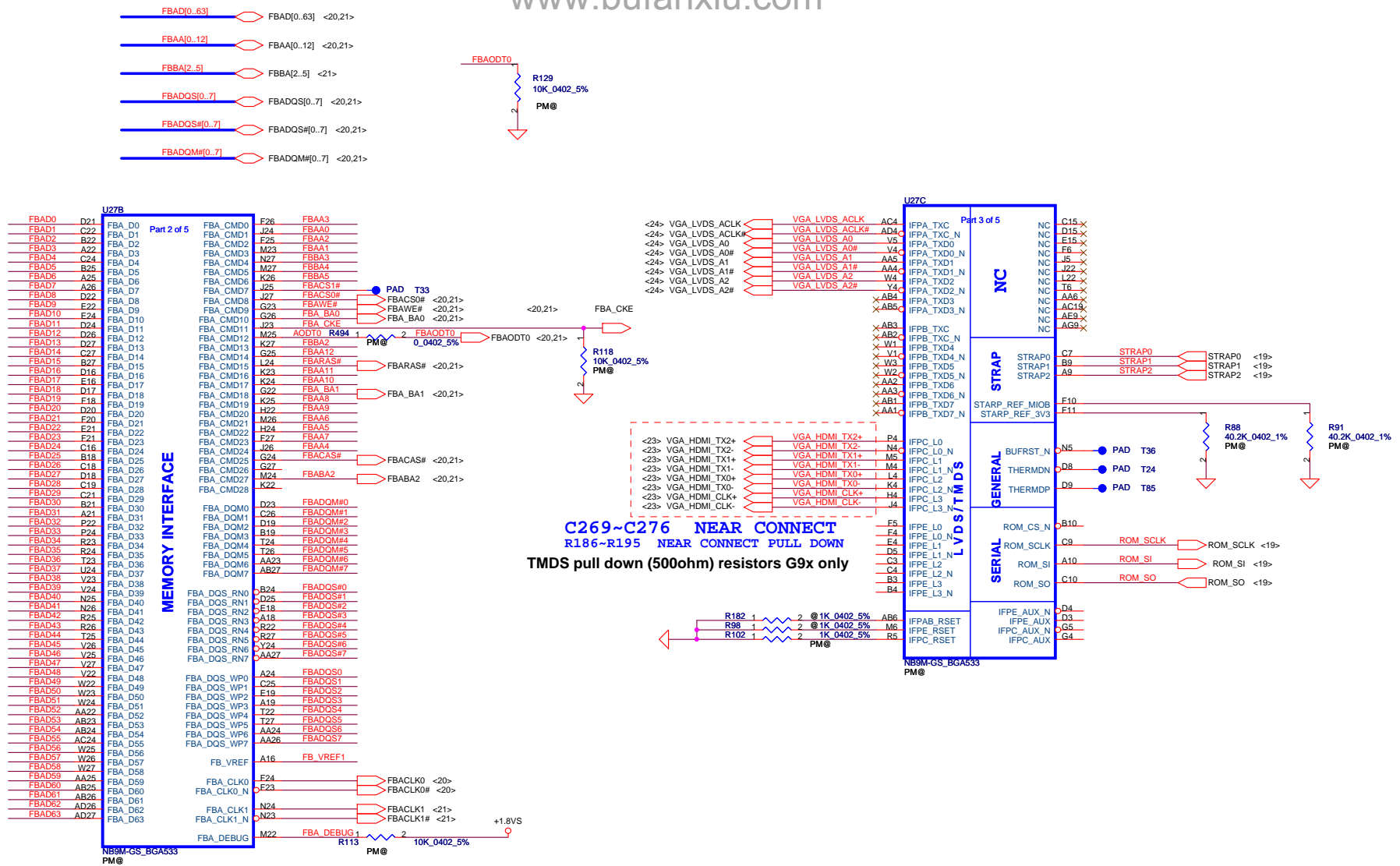




DDR3 SO-DIMM B REVERSE

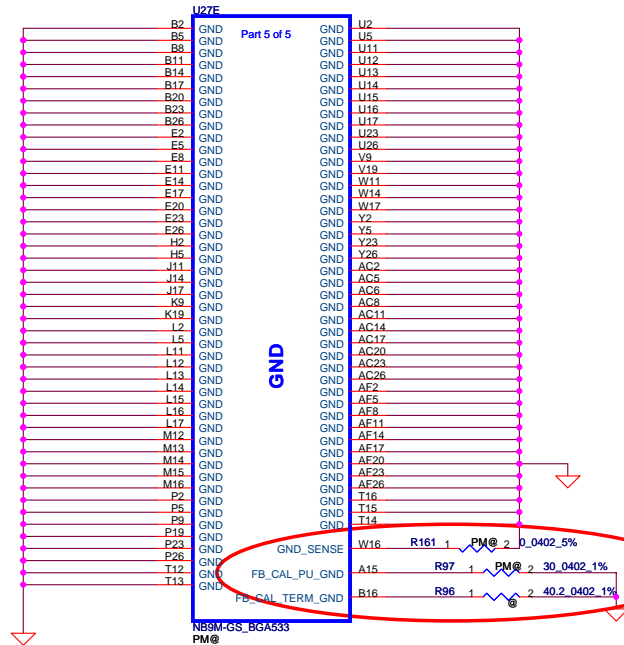
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Issued Date	2007/09/29	Deciphered Date	2007/09/29	Title DDRIII-SODIMM SLOT2		
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				Montevina UMA DDR3		
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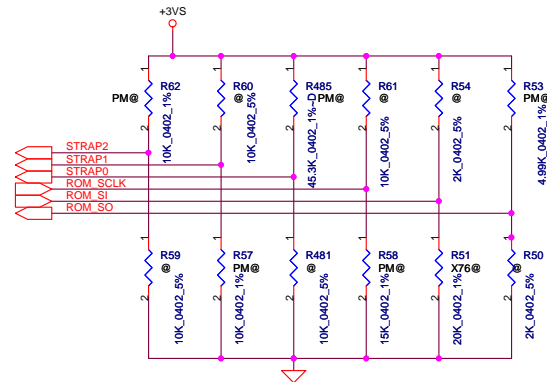


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A total of 8 signals are required for GB1 strapping this includes
2 reference signals
6 physical strapping pins
4 logical strapping bits
A total of 24 logical strapping bits are available



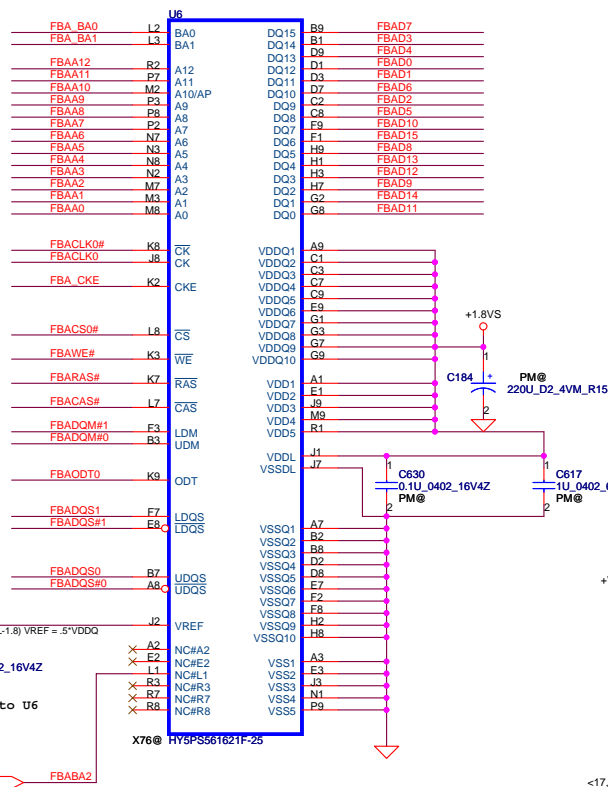
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<17> STRAP1
<17> STRAP0
<17> ROM_SCLK
<17> ROM_SI
<17> ROM_SO



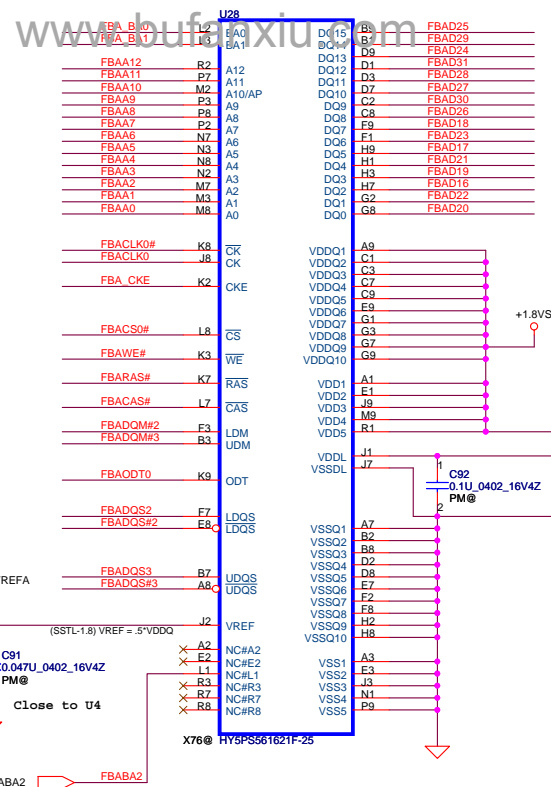
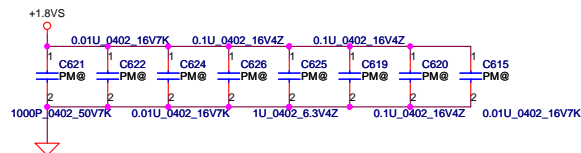
GB1 Family GPU Strap Options

GPU	FB Memory	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
NB9M-GS (0x06E9)	Samsung	16Mx16(1)	PU 5K	PD 15K	PD 10K	PD 10K	PU 45K
		32Mx16(5)	PU 5K	PD 15K	PD 10K	PD 10K	PU 45K
	Hynix	16Mx16(3)	PU 5K	PD 15K	PD 10K	PD 10K	PU 45K
		32Mx16(7)	PU 5K	PD 15K	PD 10K	PD 10K	PU 45K
	Qimonda	16Mx16(2)	PU 5K	PD 15K	PD 10K	PD 10K	PU 45K
		32Mx16(6)	PU 5K	PD 15K	PD 10K	PD 10K	PU 45K

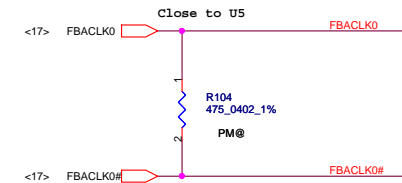
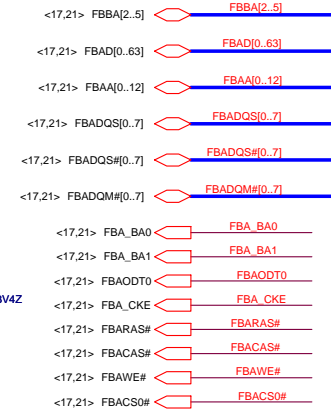
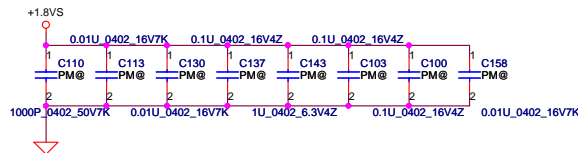
Component	Manufacturer	Compal PN	Compal X76 PN
DDR2 VRAM (32M*16)	Hynix	SA000012G30	X7611338L04
	Qimonda	SA00001YF10	X7611338L05
	Samsung	SA00001KH10	X7611338L06



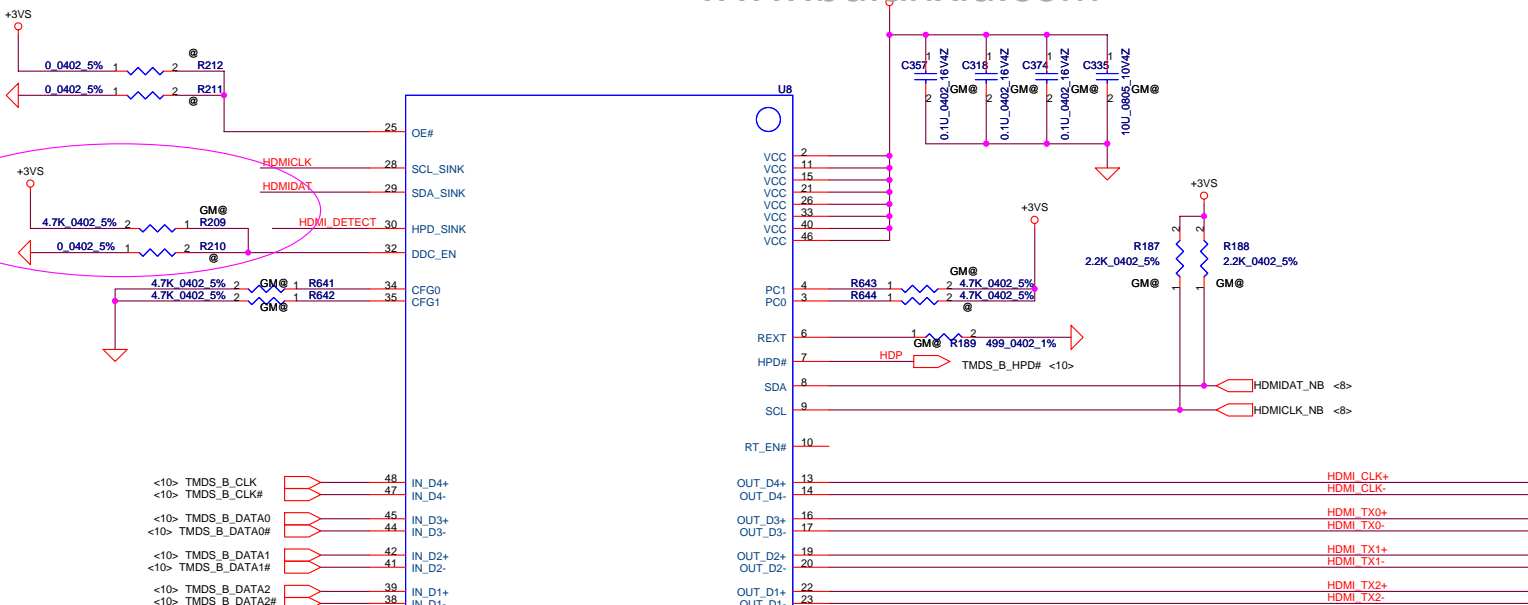
DDR2 BGA MEMORY



DDR2 BGA MEMORY



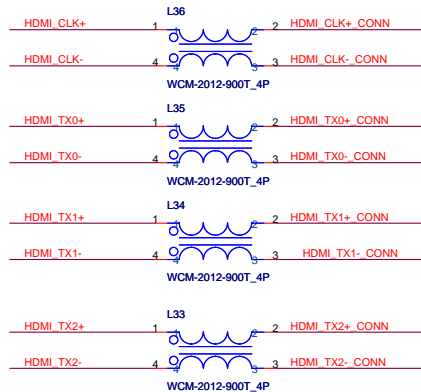
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> VRAM DDRA	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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Date: Friday, May 02, 2008				Sheet 20 of 52	JITR1_LA-4141P



TMDS pull down (500ohm) resistors G9x only

Signal	Pin	Level	Frequency	Period	Duty Cycle	Setup	Hold
HDMI CLK+ CONN	R155	PM@	2	499	0402	1%	
HDMI CLK- CONN	R156	PM@	2	499	0402	1%	
HDMI TX0+ CONN	R150	PM@	2	499	0402	1%	
HDMI TX0- CONN	R153	PM@	2	499	0402	1%	
HDMI TX1+ CONN	R145	PM@	2	499	0402	1%	
HDMI TX1- CONN	R149	PM@	2	499	0402	1%	
HDMI TX2+ CONN	R141	PM@	2	499	0402	1%	
HDMI TX2- CONN	R144	PM@	2	499	0402	1%	

NEAR CONNECT

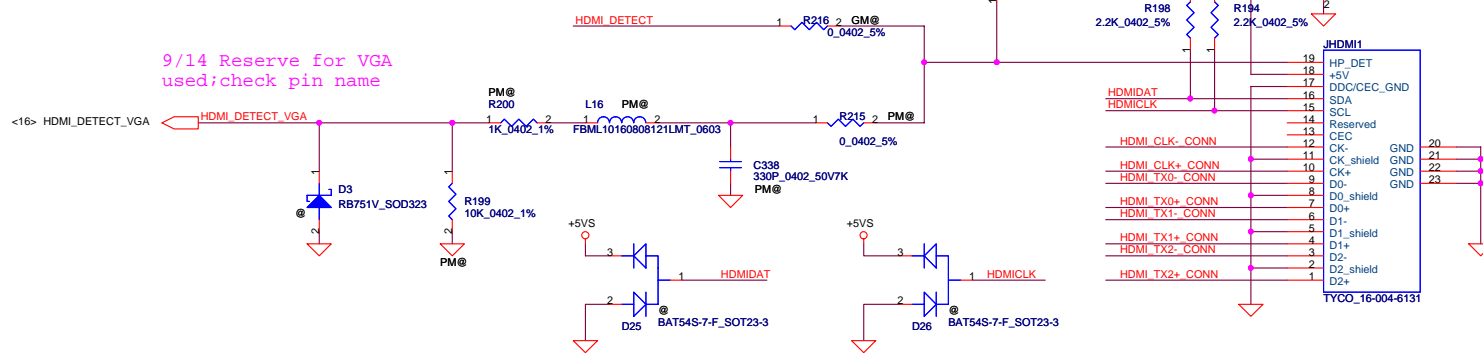


HDMI CLK+	0	0402	5%	1		2	@	R645	HDMI CLK+ CONN
HDMI CLK-	0	0402	5%	1		2	@	R646	HDMI CLK- CONN
HDMI TX0+	0	0402	5%	1		2	@	R647	HDMI TX0+ CONN
HDMI TX0-	0	0402	5%	1		2	@	R648	HDMI TX0- CONN
HDMI TX1+	0	0402	5%	1		2	@	R649	HDMI TX1+ CONN
HDMI TX1-	0	0402	5%	1		2	@	R650	HDMI TX1- CONN
HDMI TX2+	0	0402	5%	1		2	@	R651	HDMI TX2+ CONN
HDMI TX2-	0	0402	5%	1		2	@	R652	HDMI TX2- CONN

P/N:SA00002D700 (8101T)
P/N:SA00001U900

9/14 Modify for
UMA used

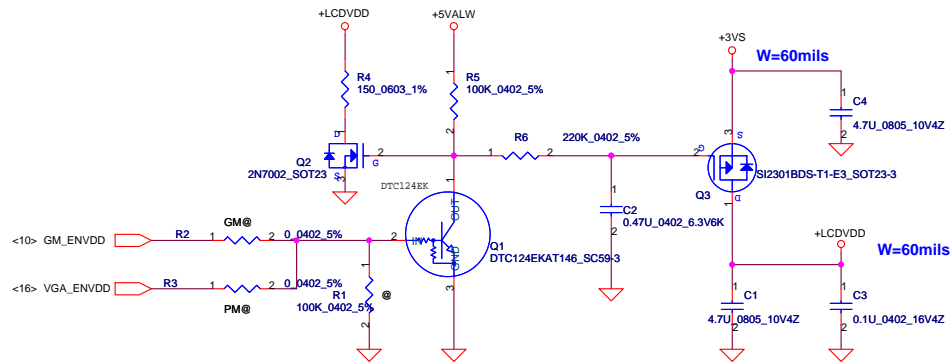
9/14 Reserve for VGA
used;check pin name



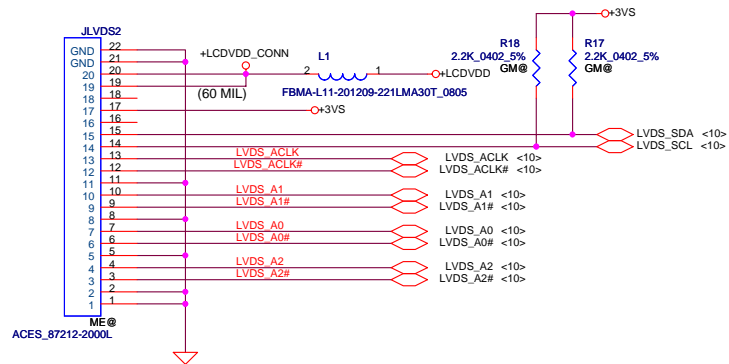
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Title			
Level shifter-CH7318			
Size	Document Number		Rev
	JITR1_LA-4141P		1.0
Date:	Expiry: Mar 02, 2008	Sheet	23 of 50

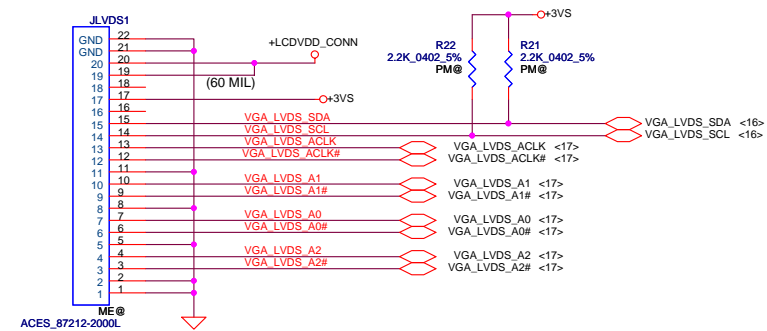
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.



LCD/PANEL BD. Conn.



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Compal Electronics, Inc.

LVDS & DVI Connector

Size

Document Number

Date:

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Sheet

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of

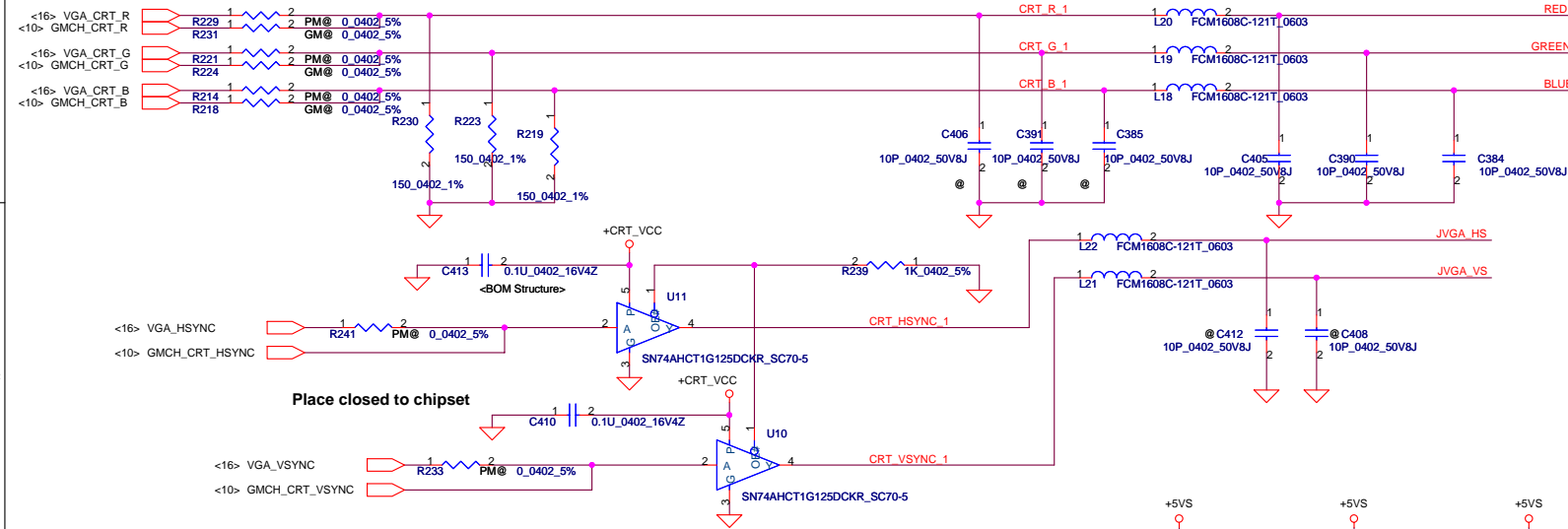
52

Rev

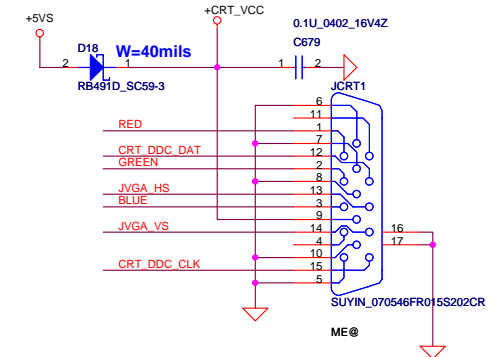
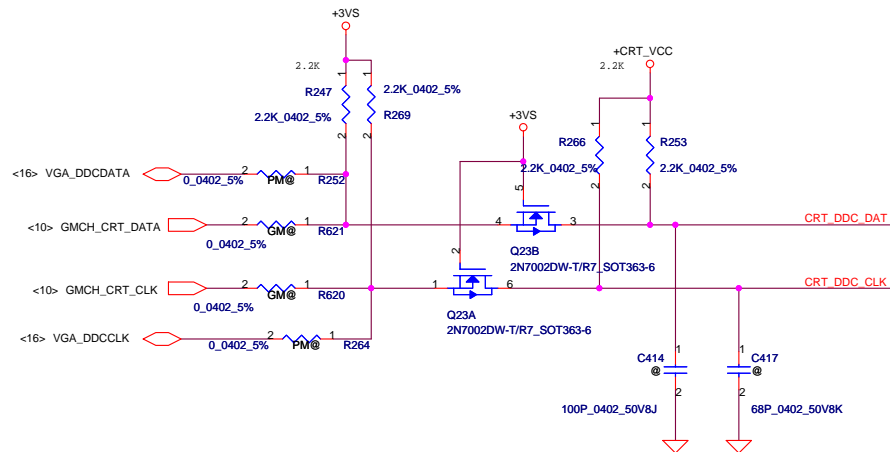
0.1

CRT Connector

Place closed to chipset



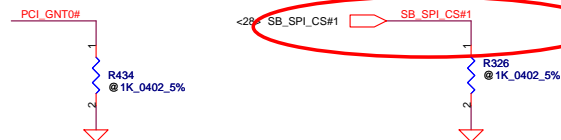
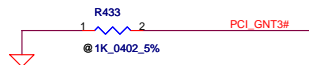
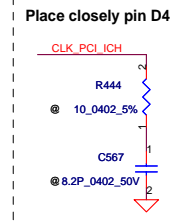
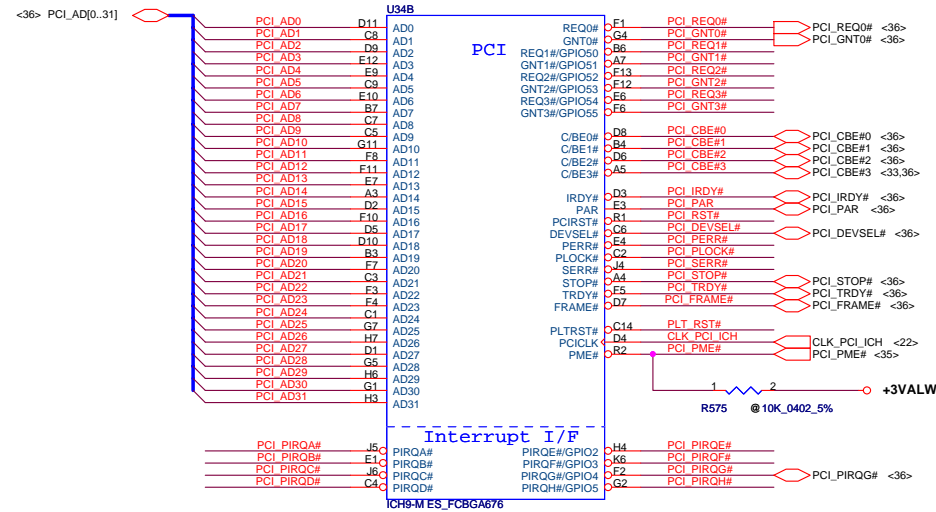
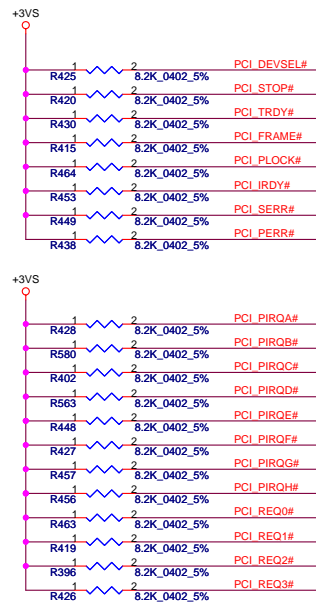
Place closed to chipset



PIN ASSIGMENT

D-SUB	FUNCTION
9	+CRT_VCC
1	RED
6	GND
2	GREEN
7, 5	GND
3	BLUE
8	GND
14	VSYNC
10	GND
13	HSYNC
11	SENSE
12	SM_DAT
15	SM_CLK
4	PIN4

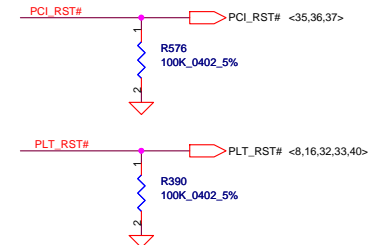
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Size	Document Number	JITR1_LA-4141P		Rev
Custom				0.1
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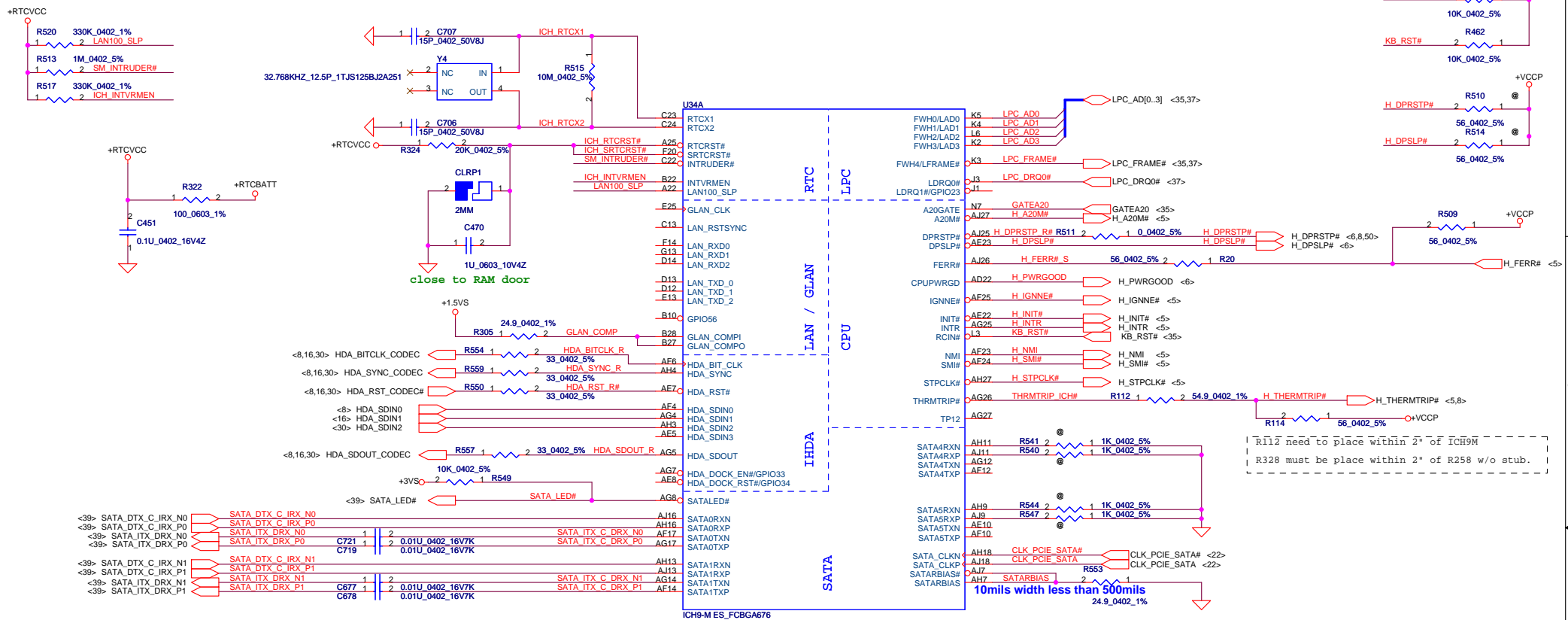


Pull high?

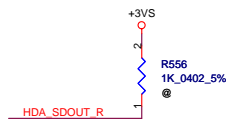
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

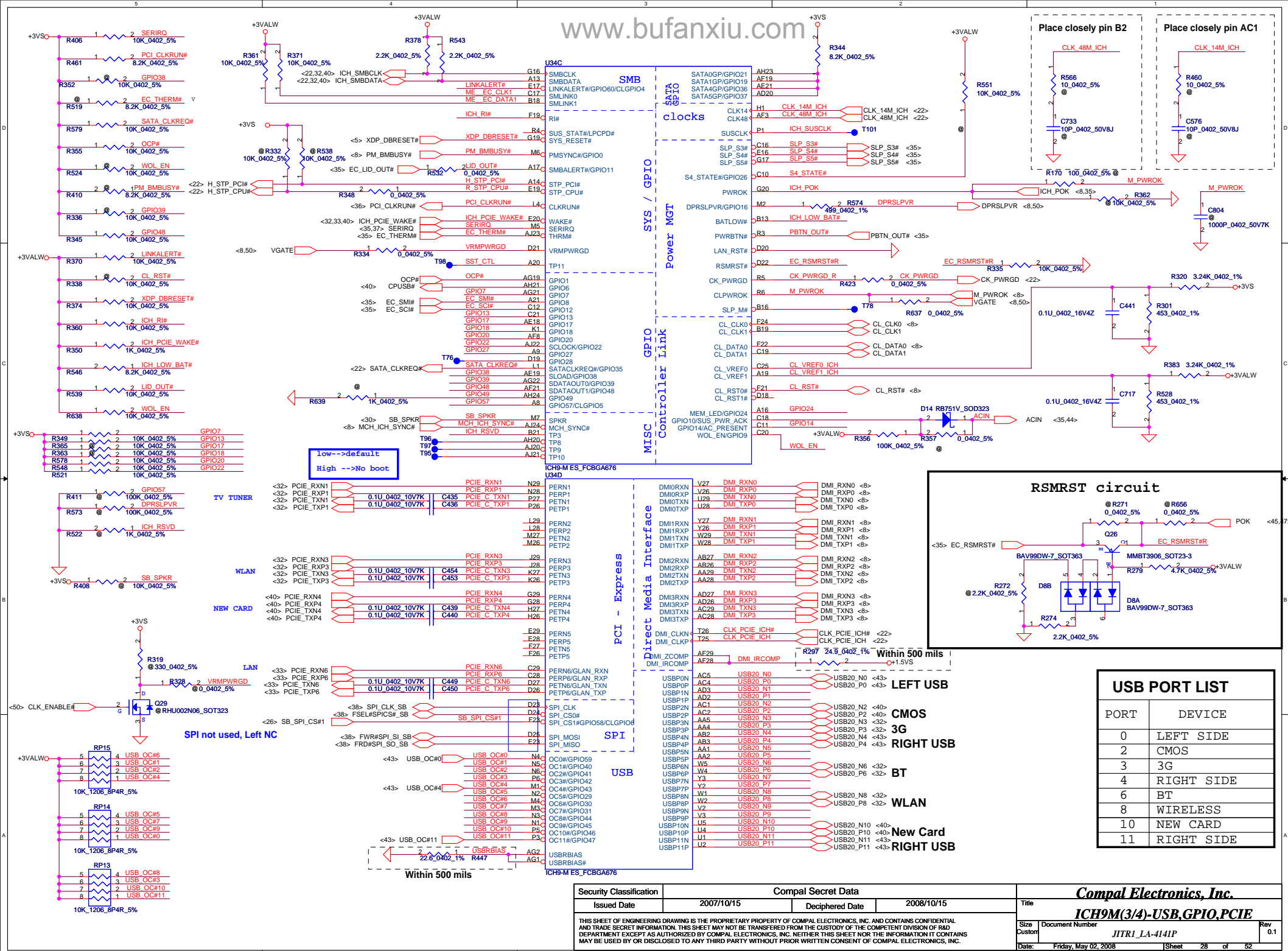


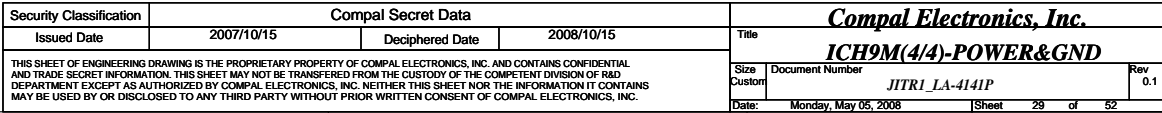


Need check



XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1





AUDIO CODEC

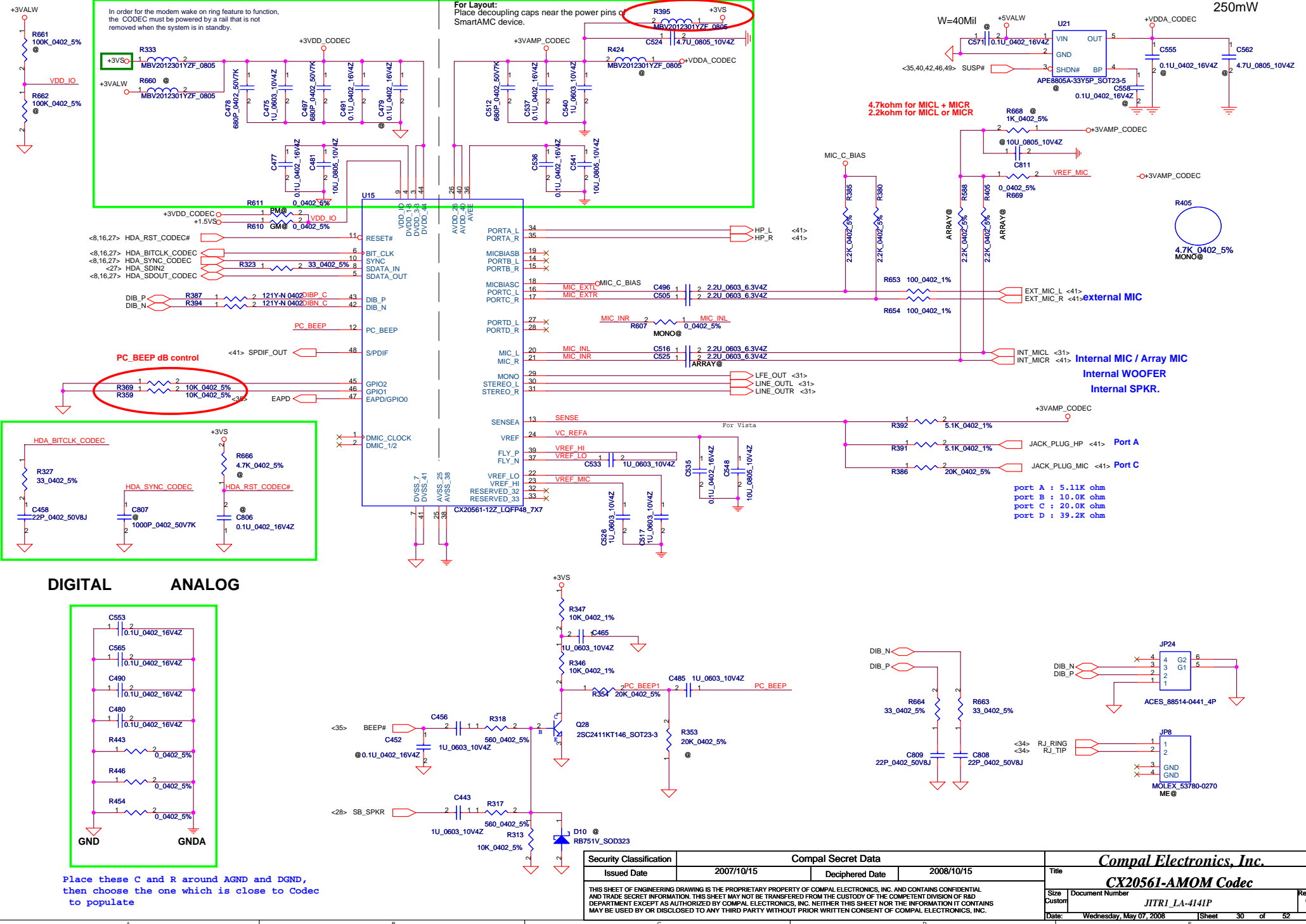
0308_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680pF

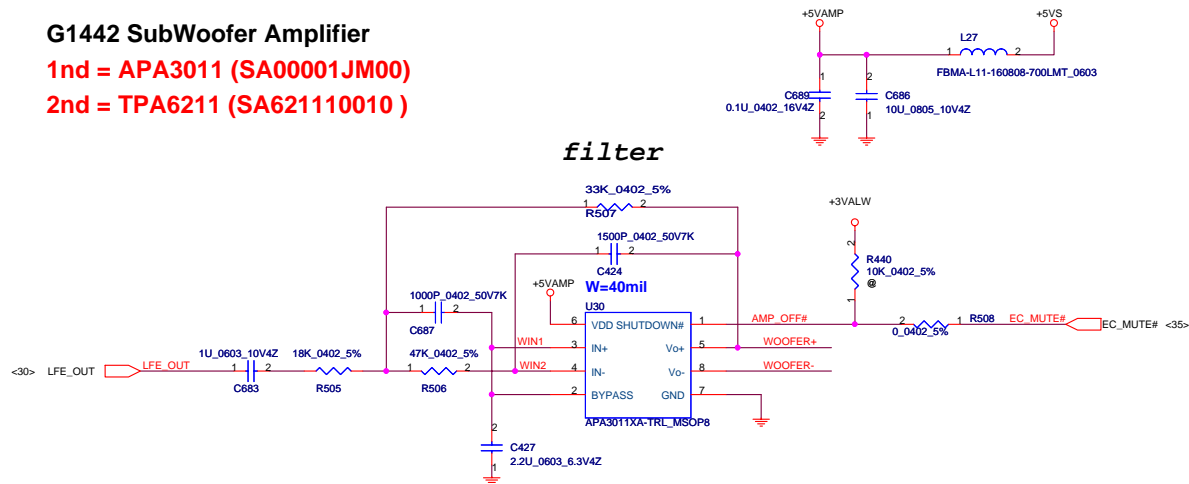
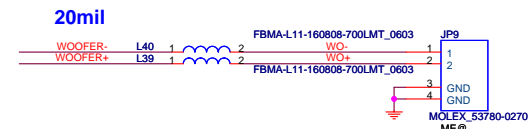
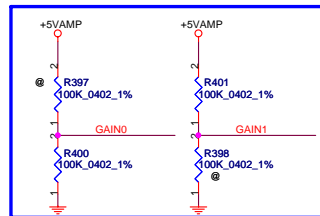
CHANGE TO 0ohm (2008/05/05)

CODEC POWER

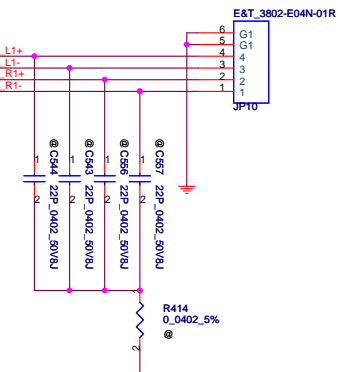
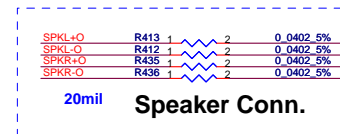
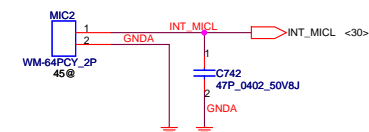
(3.33V)

250mW



G1442 SubWoofer Amplifier**1nd = APA3011 (SA00001JM00)****2nd = TPA6211 (SA621110010)****SubWoofer Conn.****Speaker Amplifier****1nd = APA2031 (SA00001RZ00)****2nd = G1431F2U (SA000012Y00)**

GAIN0	GAIN1	Gain
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

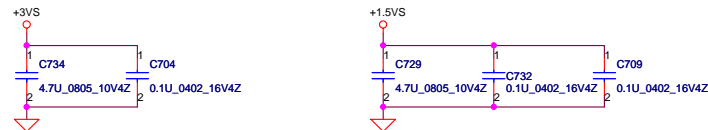
**INT MIC**

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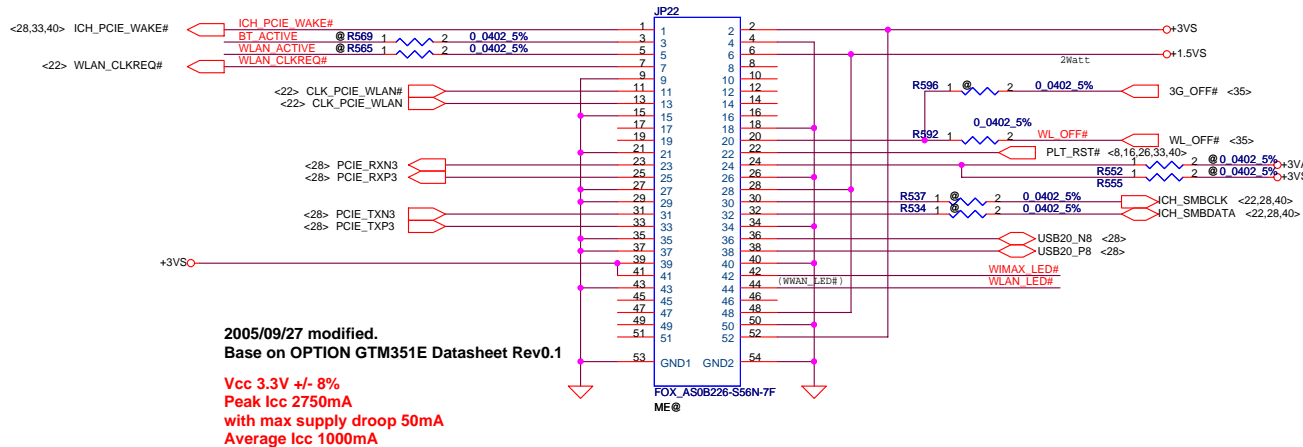
Mini-Express Card for 3G Or TV Tuner

Mini-Express Card for WLAN

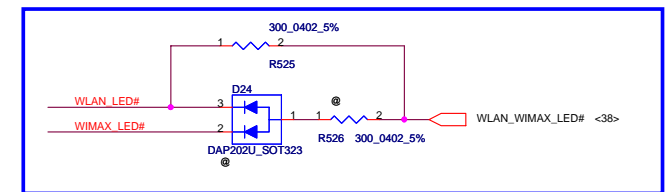
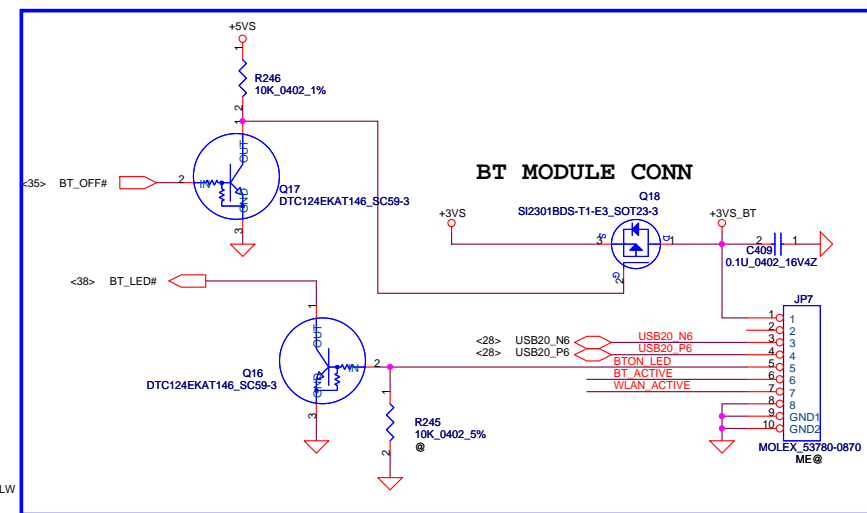
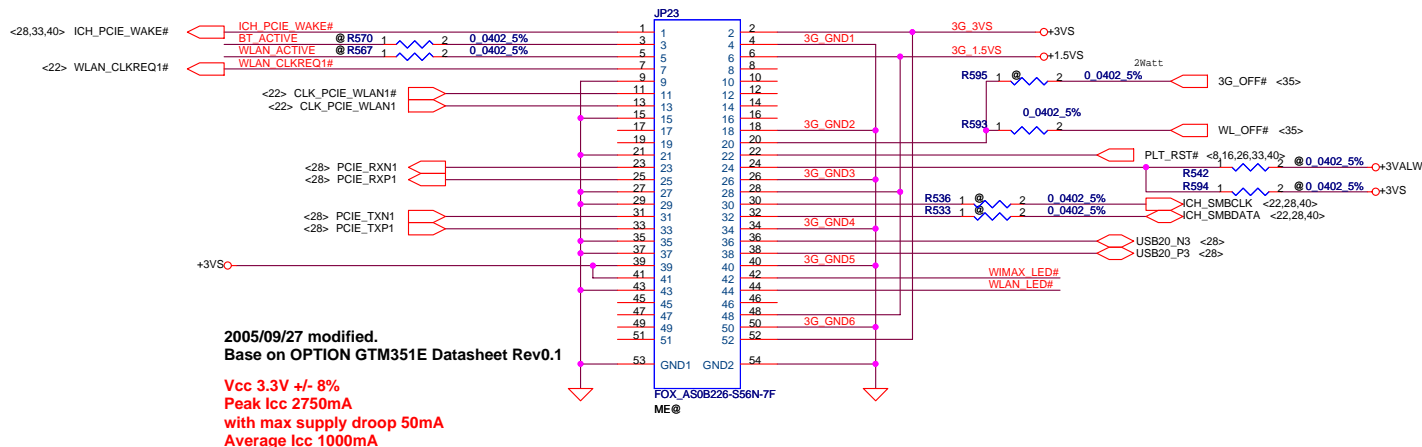
www.bufanxiu.com



Mini-Express Card(Slot 1-WLAN WIMAX)



Mini-Express Card(Slot 2-WLAN WIMAX)



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Size		Document Number		Rev	
Date		Monday, May 05, 2008		Sheet 32 of 52	

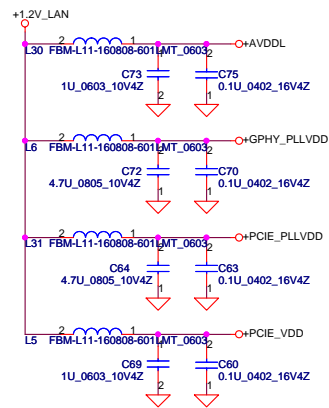
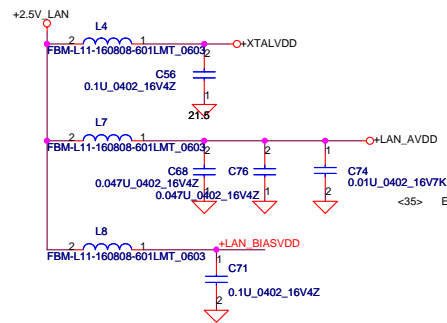
Compal Electronics, Inc.

Mini-Card/3G/FeliCa/BT

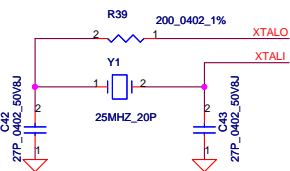
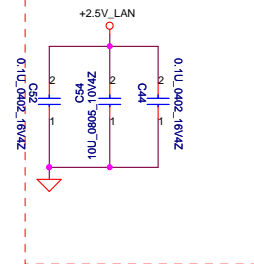
JITR1_LA-4141P

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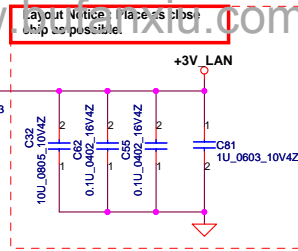
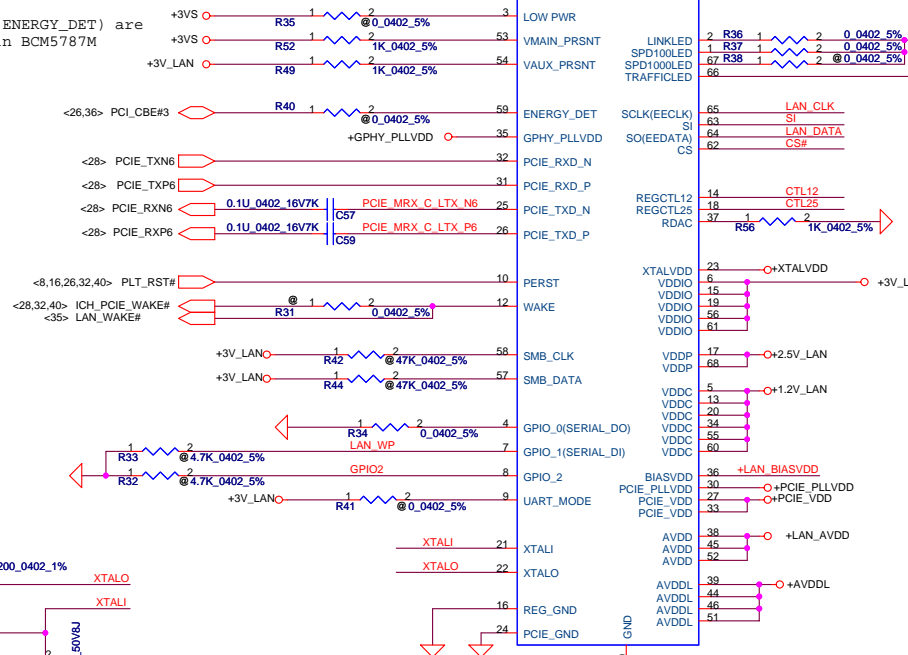
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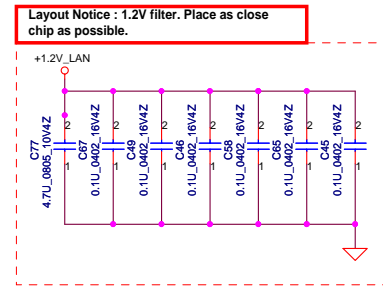
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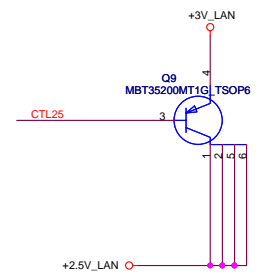
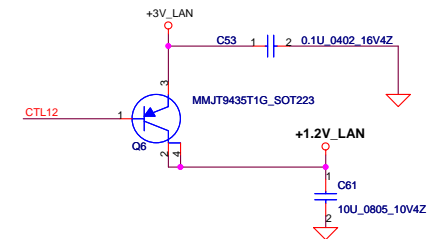
(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M



Layout Notice: Please close this window as close as possible.

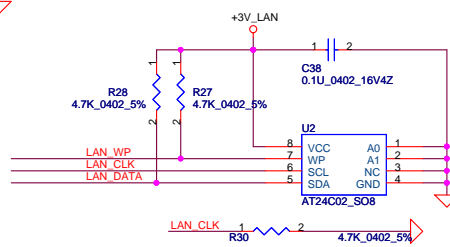


Layout Notice : 1.2V filter. Place as close chip as possible.



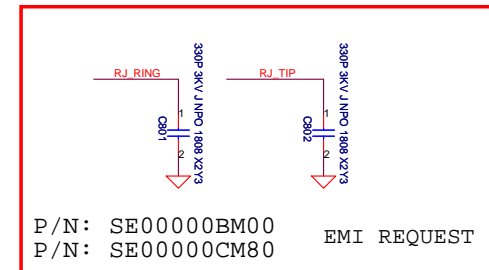
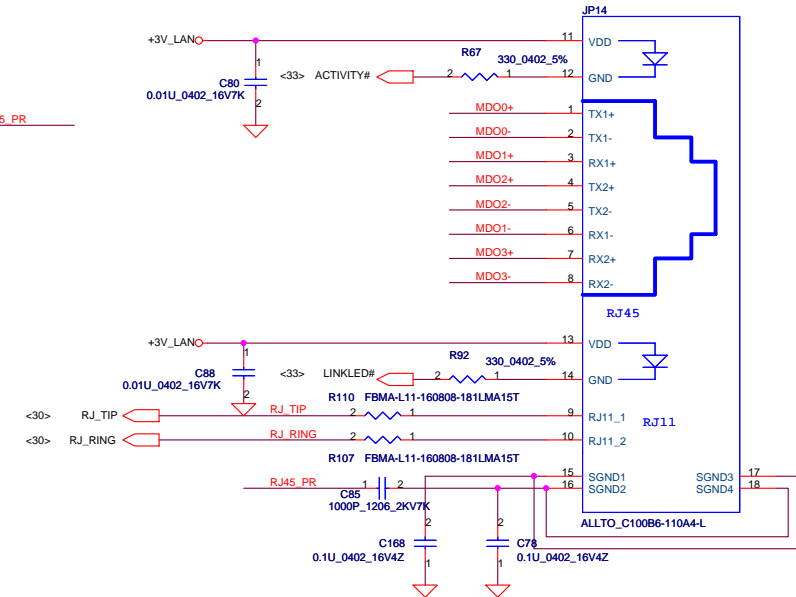
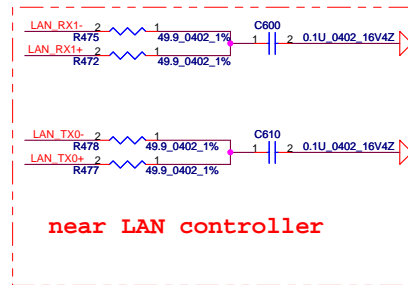
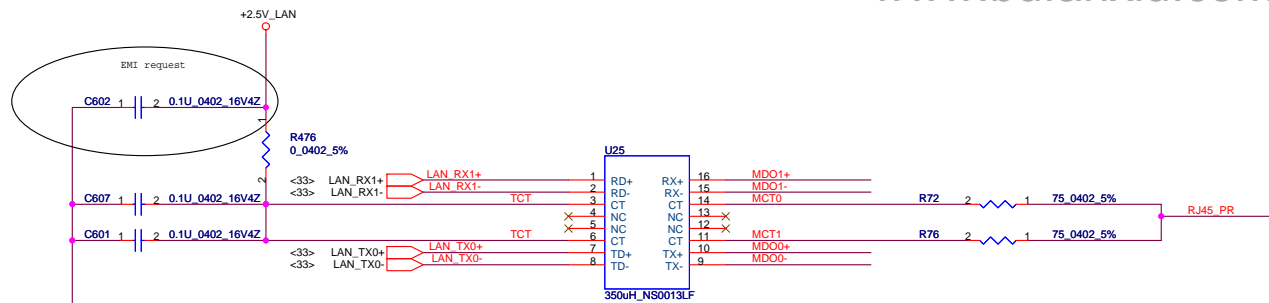
Notice : 4.7u 6.3V capactor Thickness 1.25mm

Layout Notice : Filter place as close chip as possible.

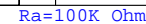


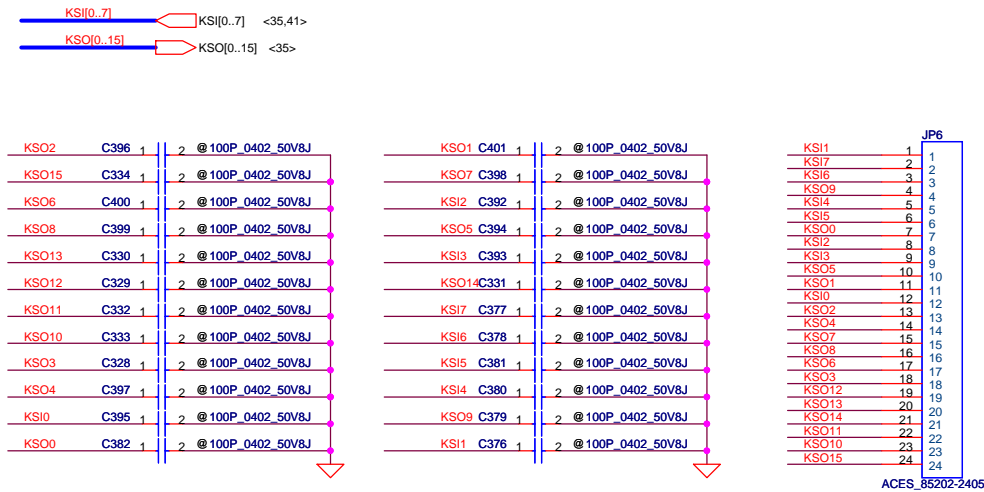
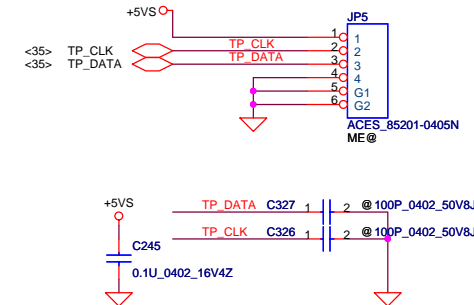
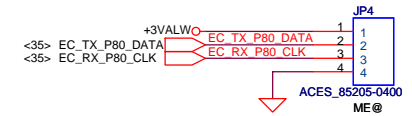
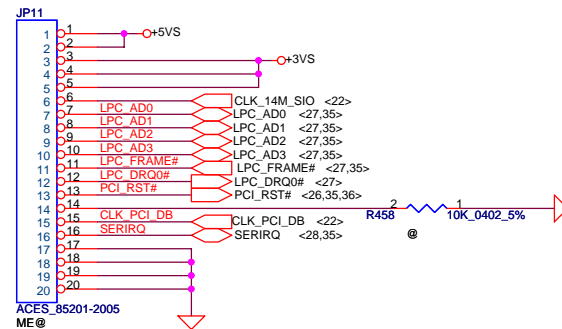
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RJ11+RJ45 CONN

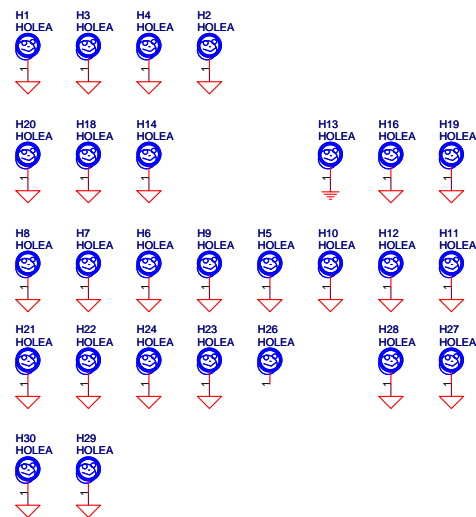
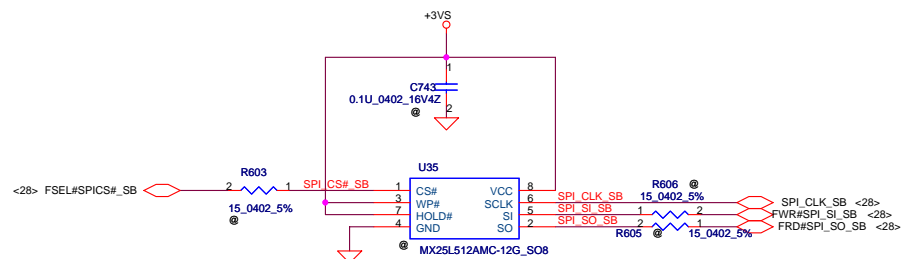


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				Custom	JITRI_LA-4141P
				Date:	Friday, May 02, 2008
				Rev	0.1
				Sheet	34 of 52

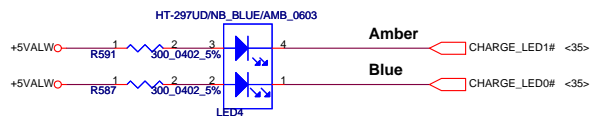


INT_KBD Conn.**To TP/B Conn.****EC DEBUG PORT****FOR LPC SIO DEBUG PORT**

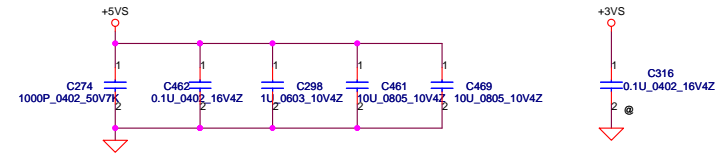
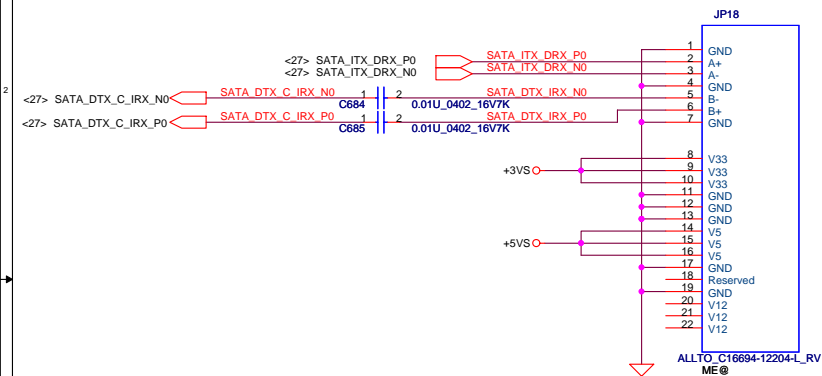
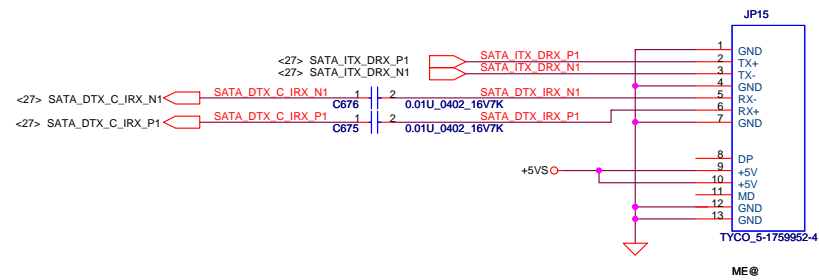
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				JITR1_LA-4141P	
				Date:	Friday, May 02, 2008
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				Rev	0.1



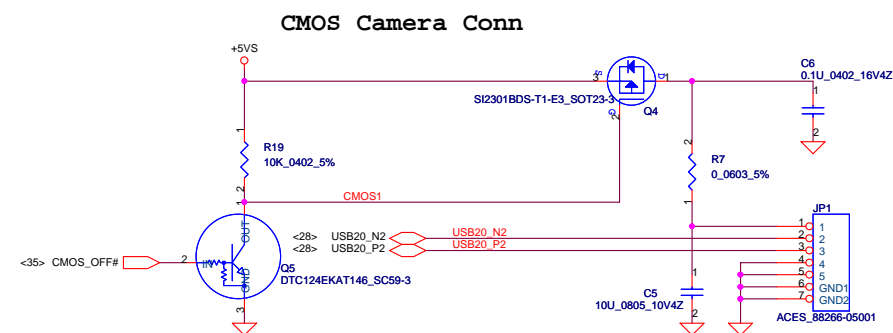
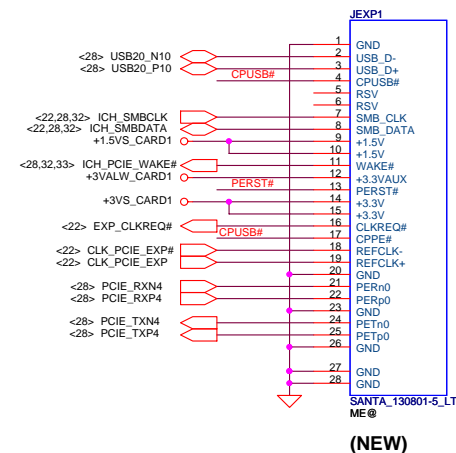
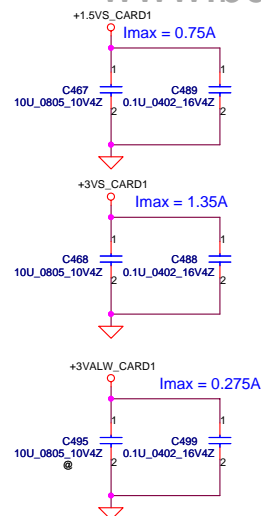
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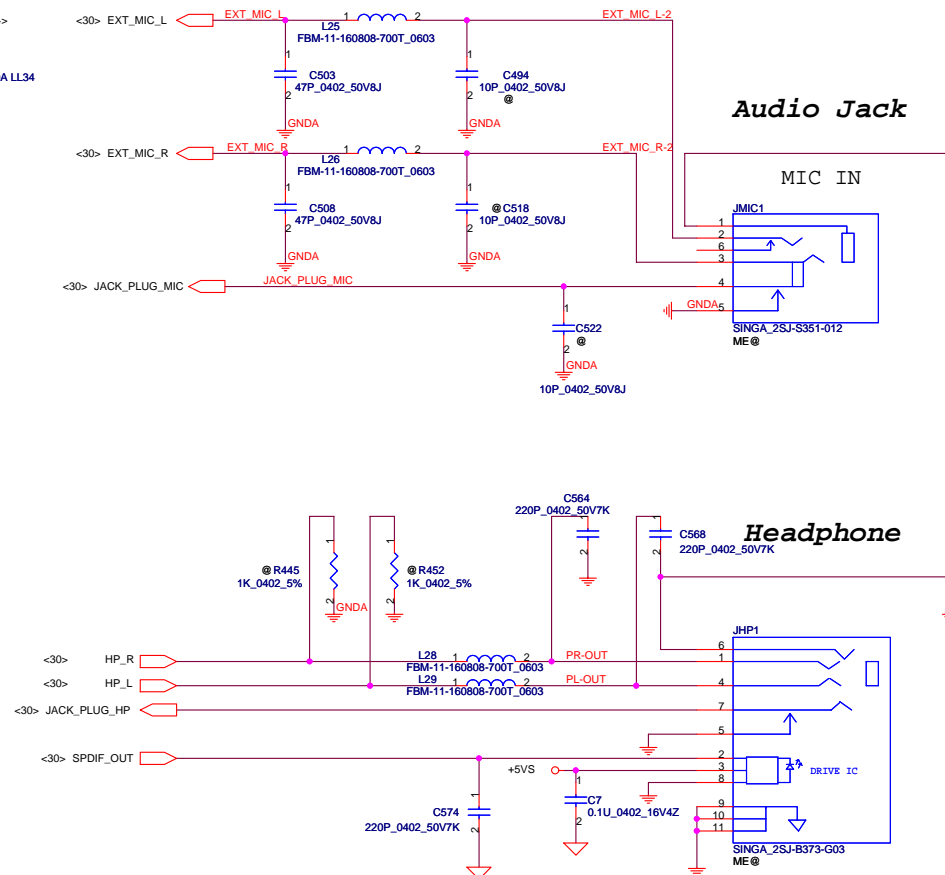
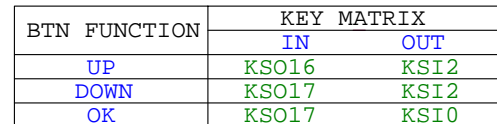
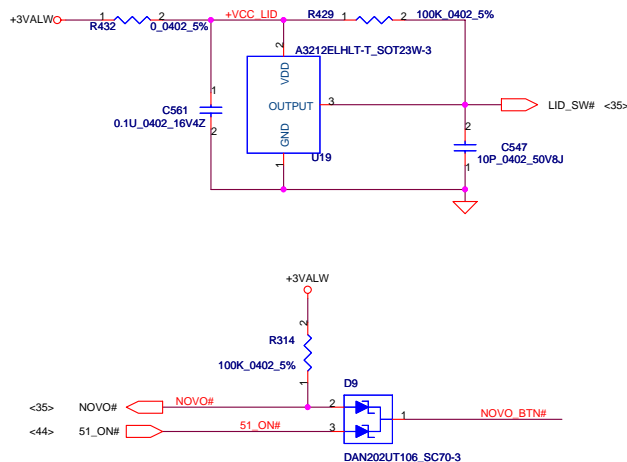
Security Classification		Compal Secret Data		Compal Electronics, Inc. LED/EC SPI ROM		
Issued Date	2007/10/15	Deciphered Date	2008/10/15			
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				Date:	Monday, May 05, 2008	Sheet 38 of 52

**SATA HDD Conn.****SATA ODD Conn.**

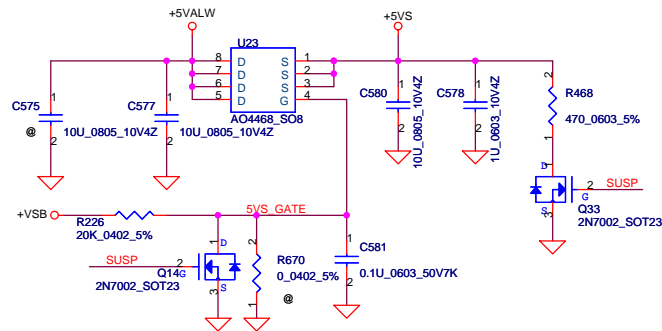
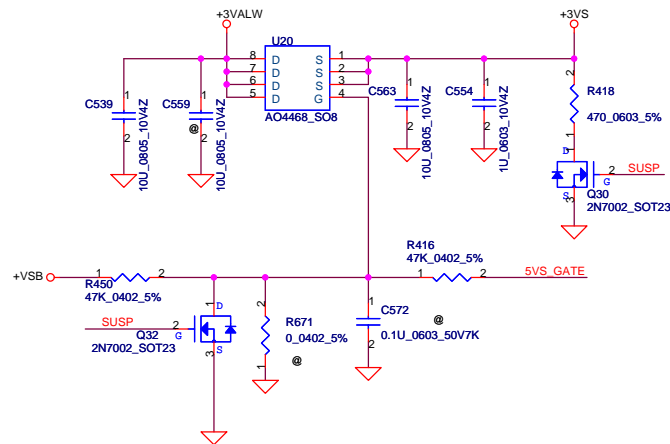
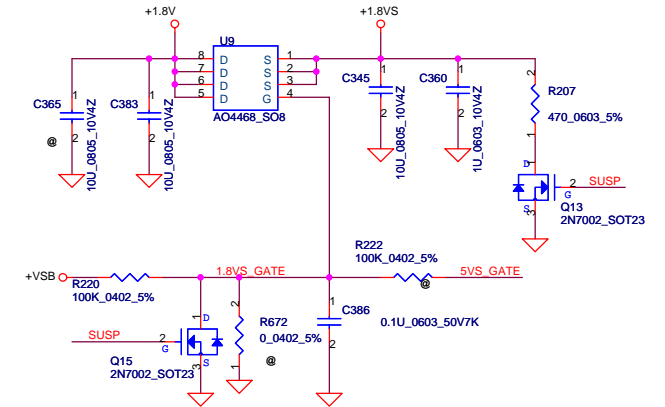
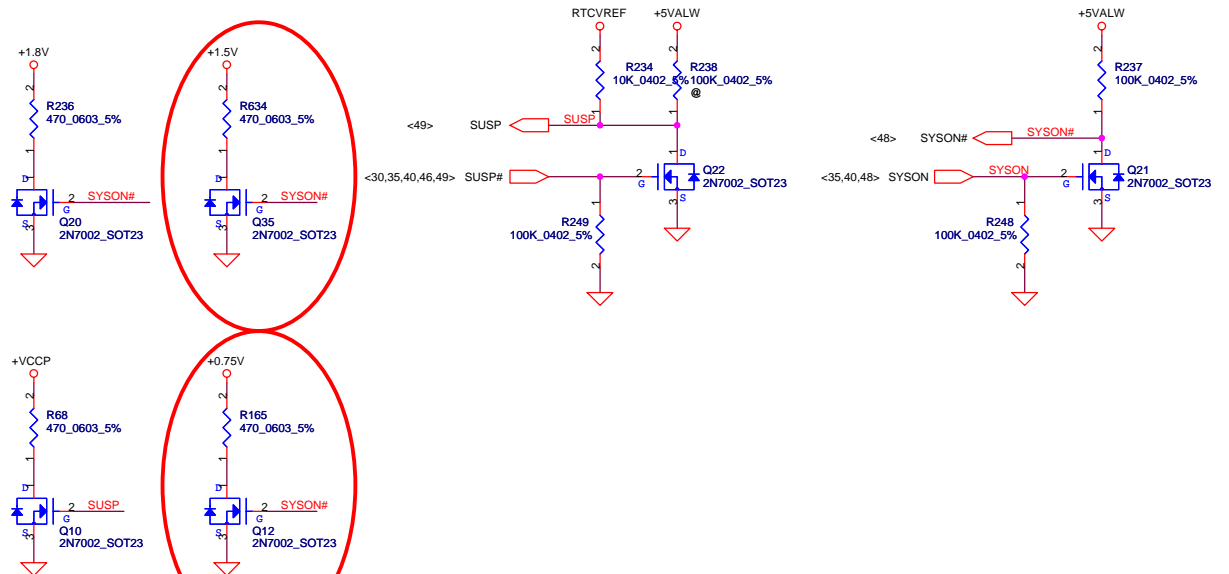
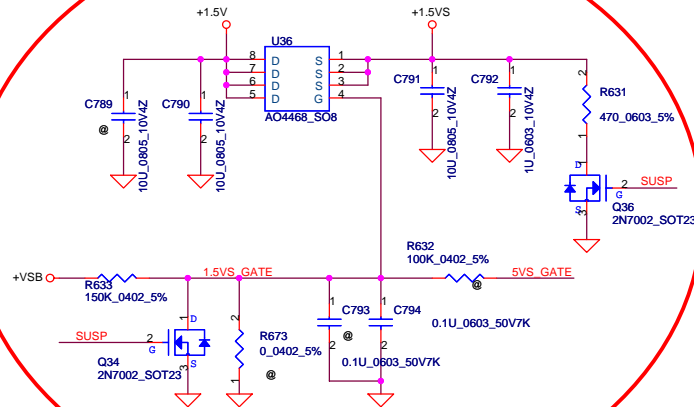
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
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				JITR1_LA-4141P		Rev 0.1
				Date: Friday, May 02, 2008	Sheet 40 of 52	

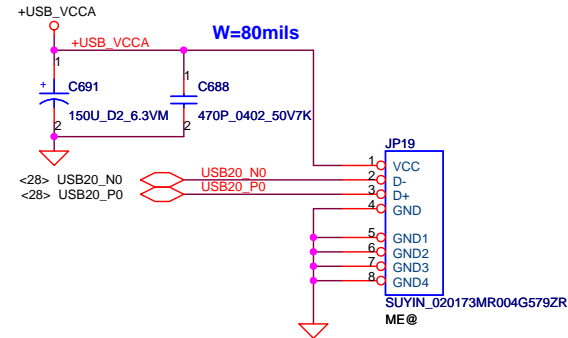
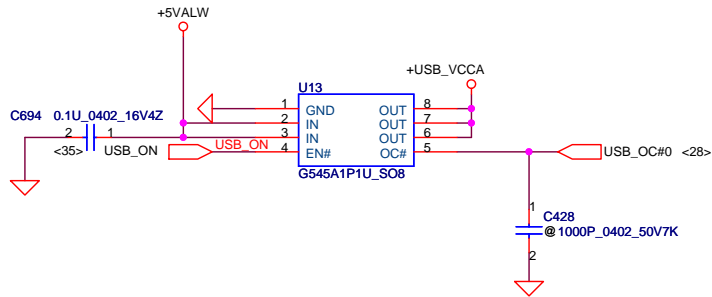


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Issued Date		2007/10/15		Deciphered Date		2008/10/15		Title	
								Audio Jack & SW connector	
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						JITR1_LA-4141P		0	
				Date		Wednesday, May 07, 2008		Sheet 41 of 52	

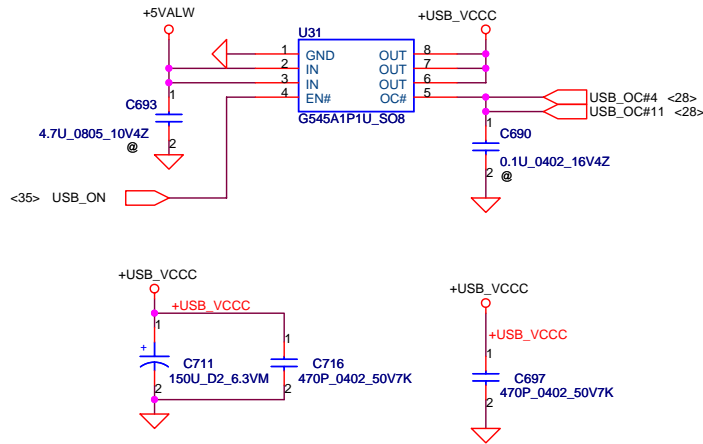
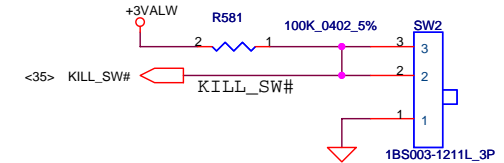
+5VALW TO +5VS**+3VALW TO +3VS****+1.8V to +1.8VS****+1.5V to +1.5VS**

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	Document Number	Rev		1.0	
Date	Monday, May 05, 2008	Sheet	42 of 52	LA-3691P	

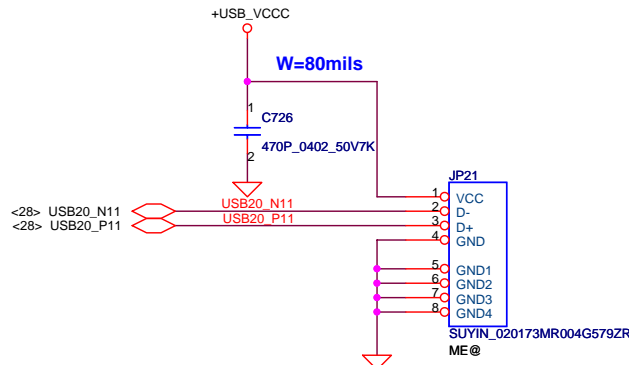
LIFT USB CONN. 1



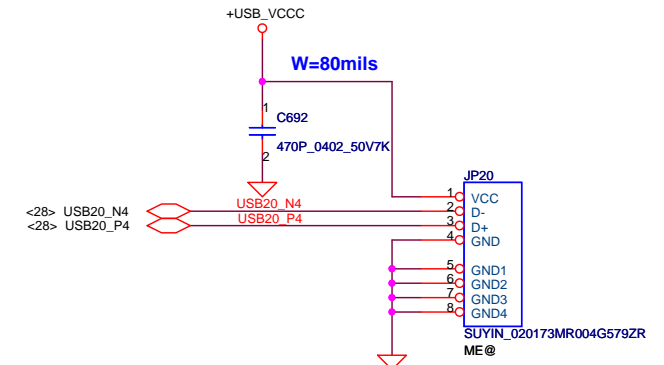
Kill Switch



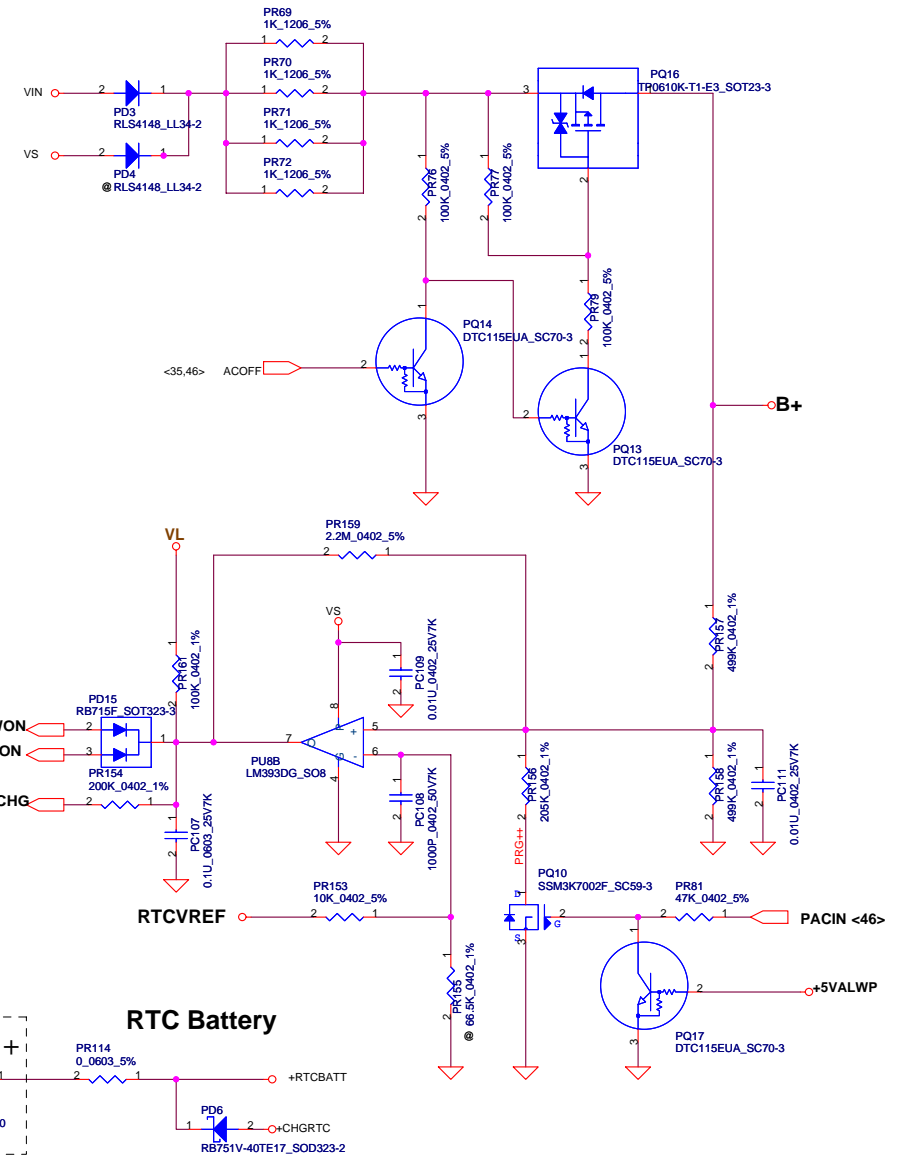
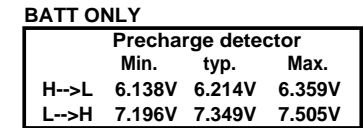
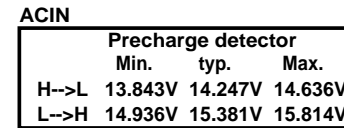
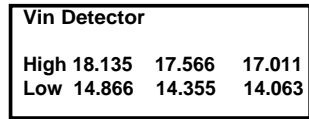
RIGHT USB CONN. 3



RIGHT USB CONN. 2



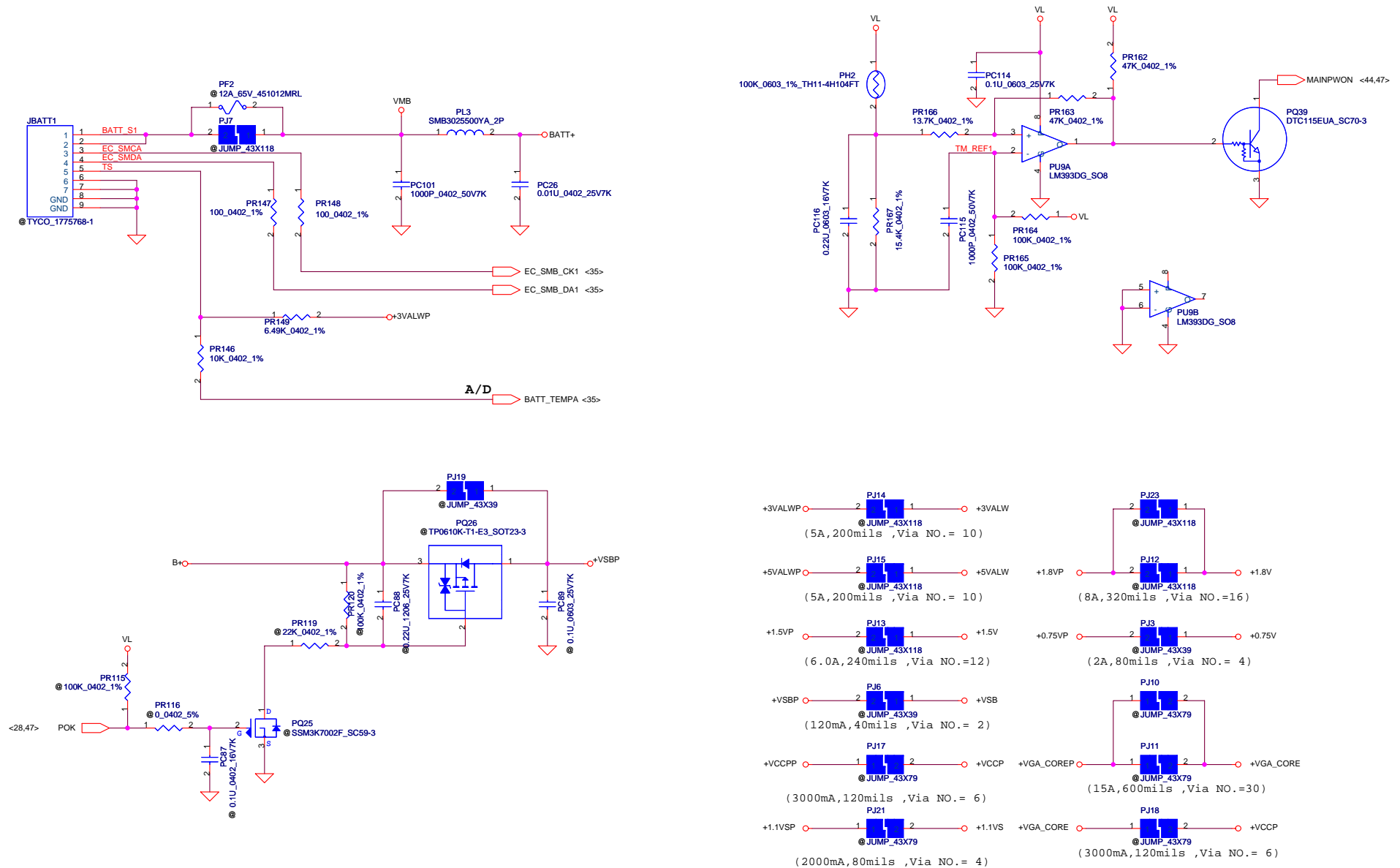
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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SP093MX0000

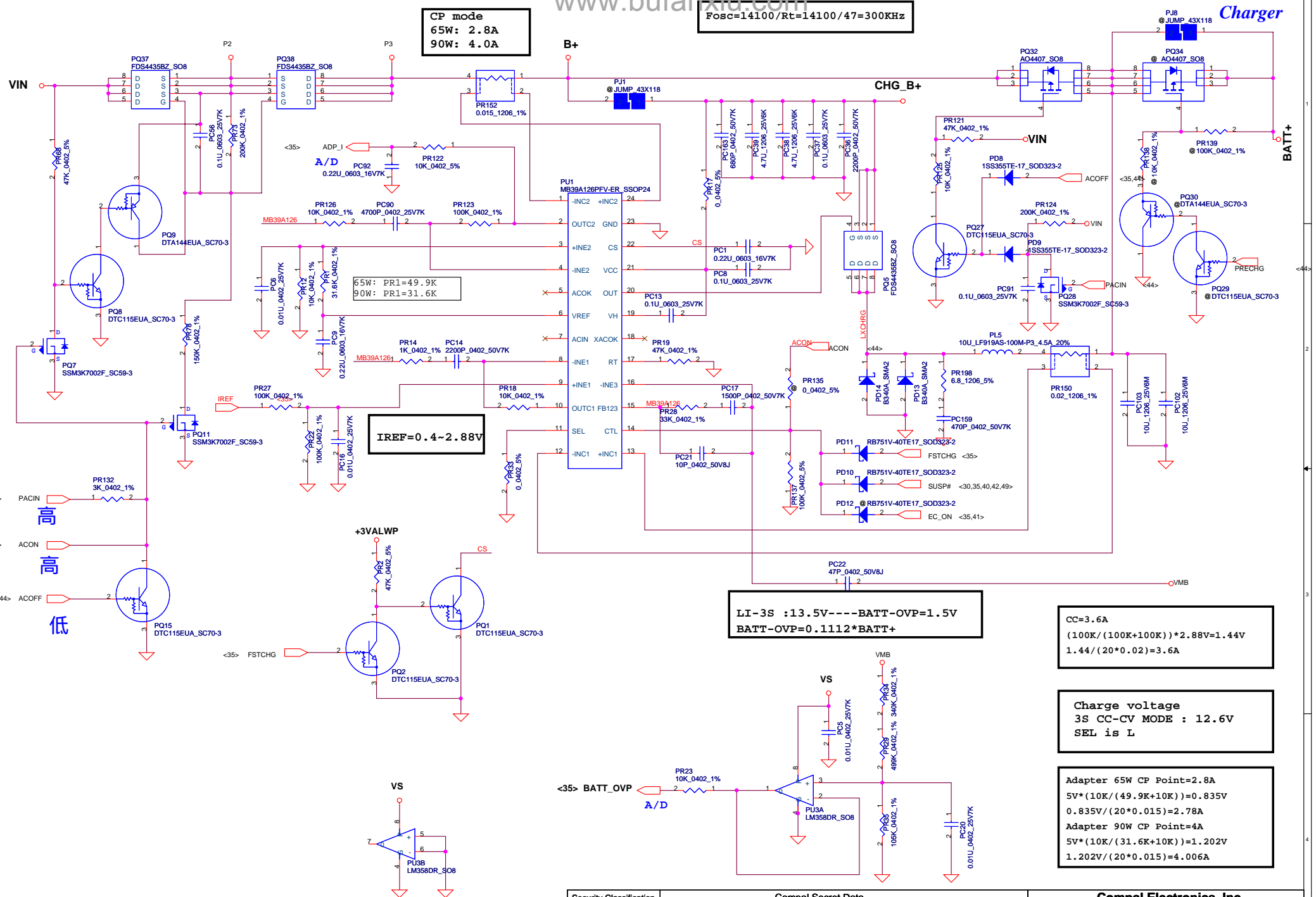
PH1 under CPU botten side :

CPU thermal protection at 92 degree C
Recovery at 56 degree C

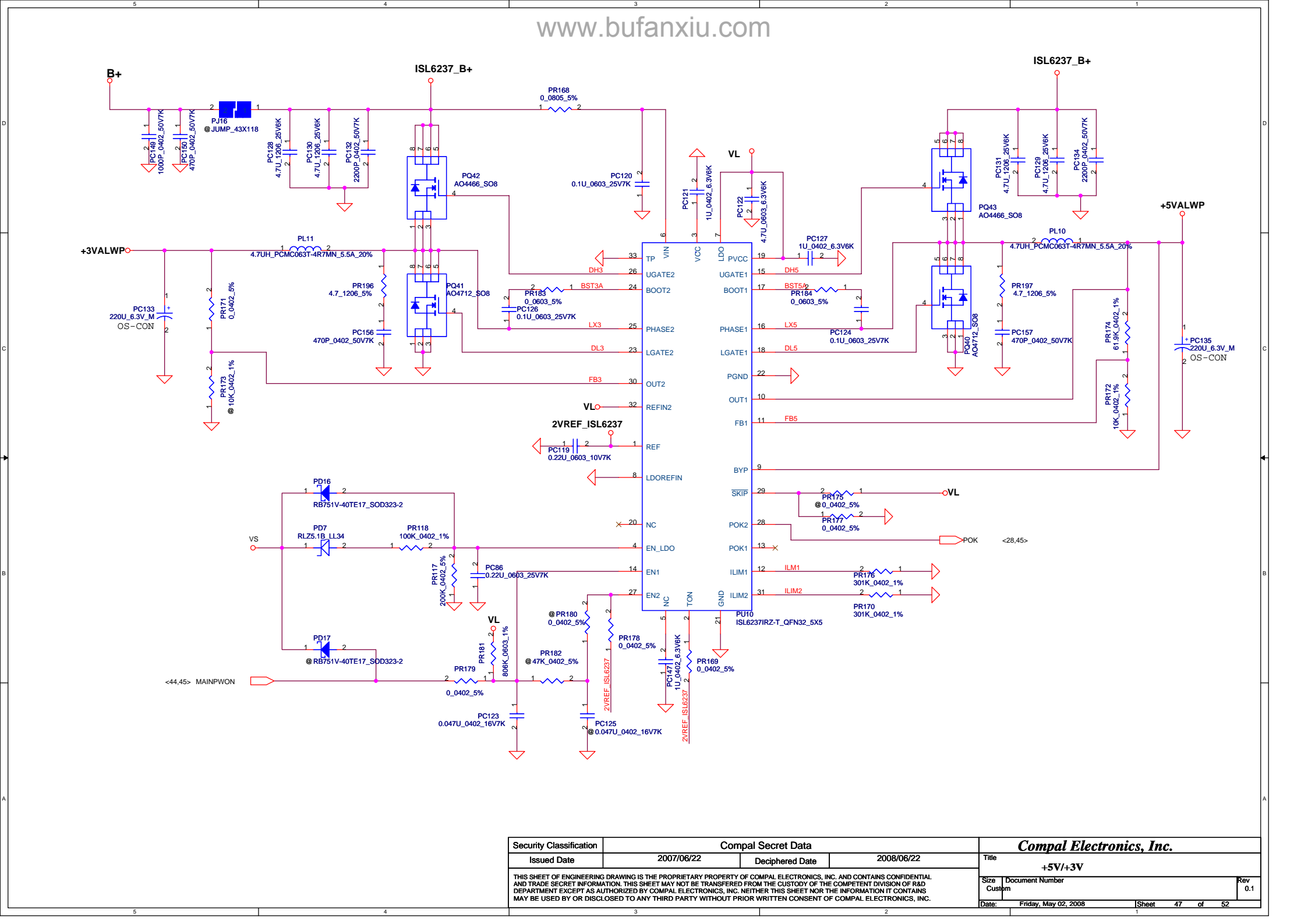


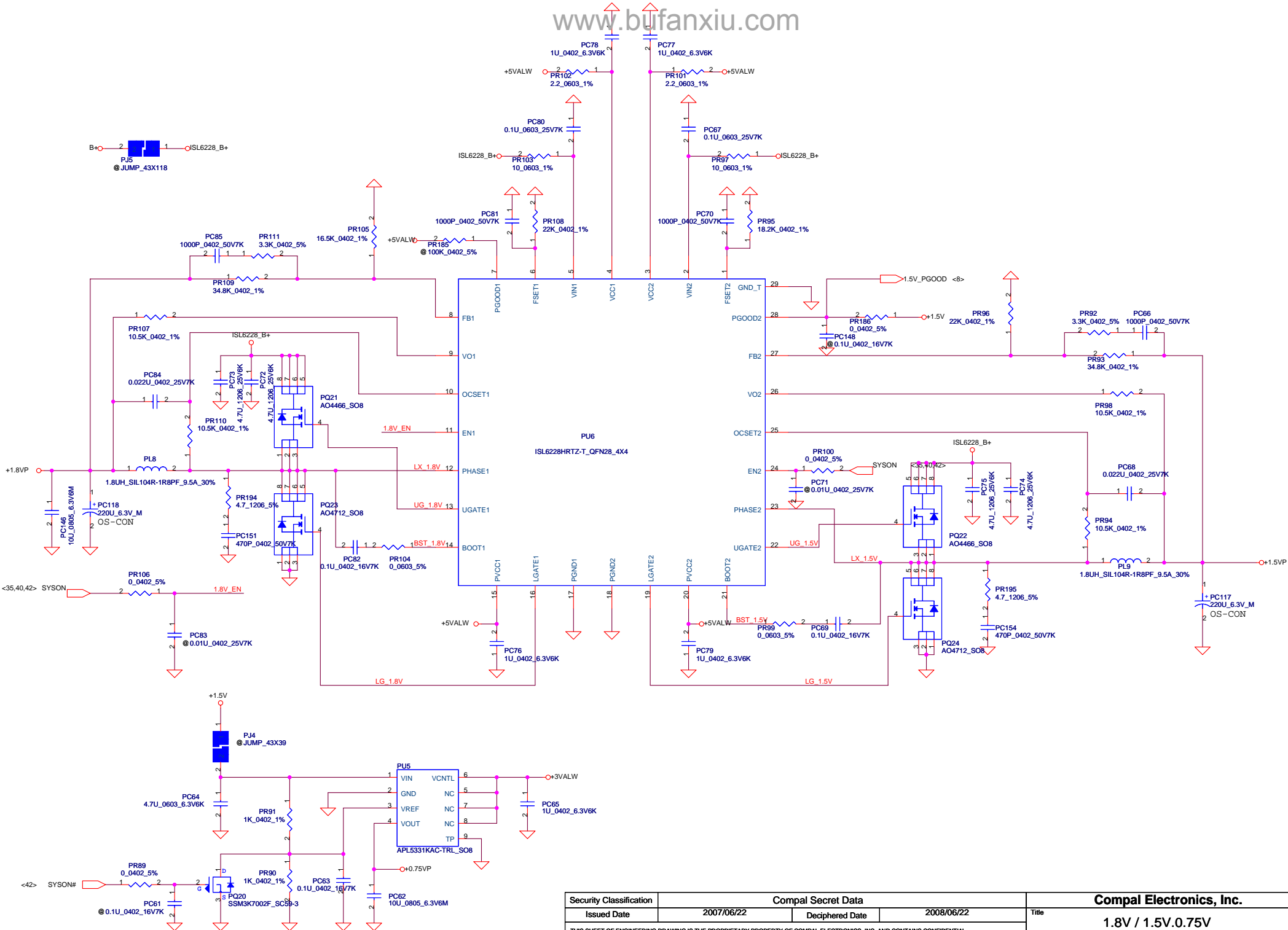
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2007/6/22				Title			
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				2008/6/22				Size			
								Document Number			
								Rev			
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Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title CHARGER		
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[illegible]



NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
10/12		P48	Add PR185, PR186	Reserve for debug use.
10/12		P49	Delete PC110	Because HW reserve enough CAP.
10/17		P49	Add PU11, PC136, PC141, PC142, PC139, PC110, PR187, PR188, PR189	Because need separate +VCCP and +VGA_CORE
10/17		P49	Change PR58 from 2.7k_0402_1% to 2.8k_0402_1% PR59 from 3.24k_0402_1% to 3k_0402_1%.	HW request change VGA_CORE from 1.1V to 1.16V
11/02		P49	Add PU12, PR190, PR191, PR192, PC137, PC138, PC140, PC143, PC144, PQ44	HW request add VCCIO(1.1V) for VGA use.
11/12		P47	Add PD16, PD17	To solve 3/5VALW reboot after remove AC.
11/21		P49	Add PC145	To reduce VGA_CORE ripple.
11/21		P49	Change PR51 from 44.4k to 37.4k.	To change VGA_CORE frequency to 350KHz
12/03		P48	Add PC146	To reduce 1.8VP ripple.
12/03		P47	Add PC147	To reserve for 3/5V IC 2nd source.
12/17		P48	Change PR105 from 16.9k_0402_1% to 16.5k_0402_1%, PR96 from 16.9k_0402_1% to 22k_0402_1%, PR93 from 25.5k_0402_1% to 34.8k_0402_1%.	Adjust 1.5V to 1.549V, 1.8V to 1.8V to 1.865V
12/17		P48	Add PC148.	Reserve for HW adjust power sequence.
12/27		P47, P48, P49, P50	Add PC149, PC150, PC152, PC153, PC155, PC151, PC154, PC156, PC157, PC158, PR194, PR195, PR196, PR197	For EMI request, to decrease power broadband.
12/31		P49	Change PR58 from 2.8k_0402_1% to 3k_0402_1% PR188 from 1.27k_0402_1% to 1.4k_0402_1%.	For intel request, ES2 NB need adjust VCCP to 1.1V.
02/29		P46	Add PR198, PC159.	Reserve charger sunbber.
02/29		P46	Change PR192 from 1.87k_0402_1% to 1.91k_0402_1%.	HW request adjust 1.1V to 1.12V.
02/29		P49	Change PR64 from 0_0402_5% to 100k_0402_1%, PC44 to 0.47u.	HW adjust power sequence.
03/11		P44, 46, 49	Add PC160, PC161, PC162, PC163, PC164, PC165.	EMI requesst to solve power broadband.
03/12		P49	Add PR199, PC166.	Reserve charger sunbber.
03/11		P44, 46, 49	Add PC160, PC161, PC162, PC163, PC164, PC165.	EMI requesst to solve power broadband.
03/12		P49	Add PR199, PC166.	Reserve charger sunbber.
04/29		P50	Add PC167, PC168, PC169	For EMI request, to decrease power broadband.

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				Power PIR		
				Size	Document Number	Rev.
					LA-4141P	0.1
				Date:	Tuesday, April 29, 2008	

NO		DATE	PAGE	MODIFICATION LIST	PURPOSE
11/12	P24			Change LVDS1 & LVDS2 connect type	
11/12	P23			Change HDMI channel	
11/12	P30			Change MDC connect JP8 , Add JP24	
11/14	P16			Remove R492, R490, R489 & R491 (I2C pull- up resistor) ,Remove R66 (HDCP)	
11/14	P16			Unstaff R486, R487, R483, R195, R192, R172, R106, R171, C116 & C183 (unused DACB & DACC)	
11/14	P17			Remove R499 (FB commend14)	
11/14	P17			Unstaff R87, R90 & C90 (FB_VREF)	
11/14	P31			MIC P/N CHANGE FROM CY000000S00 TO CYWM64P0110	
11/15	P18			Add pull down 10kohm (single LVDS signal)	
11/15	P36			Update U32 for card reader power SW (SA000024X00)	
11/22	P32			Add D24 , R526 (add WIMAX_LED# of JP22 JP23 42PIN)	
11/22	P32			delete C737,C735,708,705,C682,C681,680 (for 3G issue)	
12/05	P23			ADD R636 IN TMDS_B_HPD#	
12/11	P8			DELETE R502,R498,RR160 (DELETE DDR2 FUNCTION)	
12/11	P11			R186 CHANGE FROM 0603 TO 0805	
12/11	P28			ADD R638 CONNECT "WOL_EN" TO 3VALW	
12/17	P28			GPIO49 add 1k Ohm pulled-down resistor	
12/17	P7			REMOVE C41	
12/21	P5			U5 CHANGE FROM ADI TO SMSC (SA00001Z700)	
12/21	P10			UMA HDMI TMDS CHANGE FROM C306 TO R640 (OOHM)	
12/21	P16			ADD External Spread Spectrum (ADD U3,R55,C66,R48;DEL R99,R100)	
12/26	P30			ADD R653,R654 TO EXTERNAL MIC	
12/27	P43			CHANGE KILL SW POWER FOR +3VS TO +3VALW	
12/31	P16			UPDATE VGA_HDMI_SCL,VGA_HDMI_SDA FROM I2CD TO I2CE	
2/13	P8			CHANGE R147 FROM 511ohm TO 499ohm 1%	
2/13	P23			CHANGE THE D4 LOCATION	
2/13	P23			ADD D25,D26	
2/13	P25			ADD D27,D28,D29	
2/14	P38			CHANGE LED	
2/14	P29			CHANGE R558,R582 FROM 10ohm TO 100ohm	
2/14	P29			CHANGE C728,C738 FROM 0.1uF TO 0.1uF	
2/14	P32			JP22,JP23 PIN37,PIN43 CONNECT TO GROUND	
2/14	P23			DELETE LEVEL SHIFT CIRCUIT	
2/14	P23			ADD R659	
3/3	P10			REMOVE R240,R235 (GHCH_CRT_HSYNC,GHCH_CRT_VSYNC)	
3/3	P11			REMOVE R186 (+VCCP_PEG)	
3/3	P11			+1.5VS_TVDAC PULL DOWN	
3/3	P28			TO USE THE RSMRST CIRCUIT	
3/3	P28			ADD C804,C805,C806,C807 (ESD REQUESTION)	
3/17	P16			CHANGE R69,R71 FROM 10Kohm TO 2.2Kohm	
4/18	P36			change L41,L42 from L to 0ohm	
5/2	P5			ADD R667,C810 FOR FAN solution RC (R=1Kohm,C=10nF)	
5/2	P30			ADD R668,C811,R669 FOR MIC solution RC (R=1Kohm,C=10uF) , INT_MIC CONNECT TO U15 PIN23	
5/2	P42			ADD R670,R671,R672 FOR AO4468 VGS ISSUE solution	

Title

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