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ZAWBA/ZAWBB DIS M/B Schematics Document

AMD Beema SOC with DDR3L

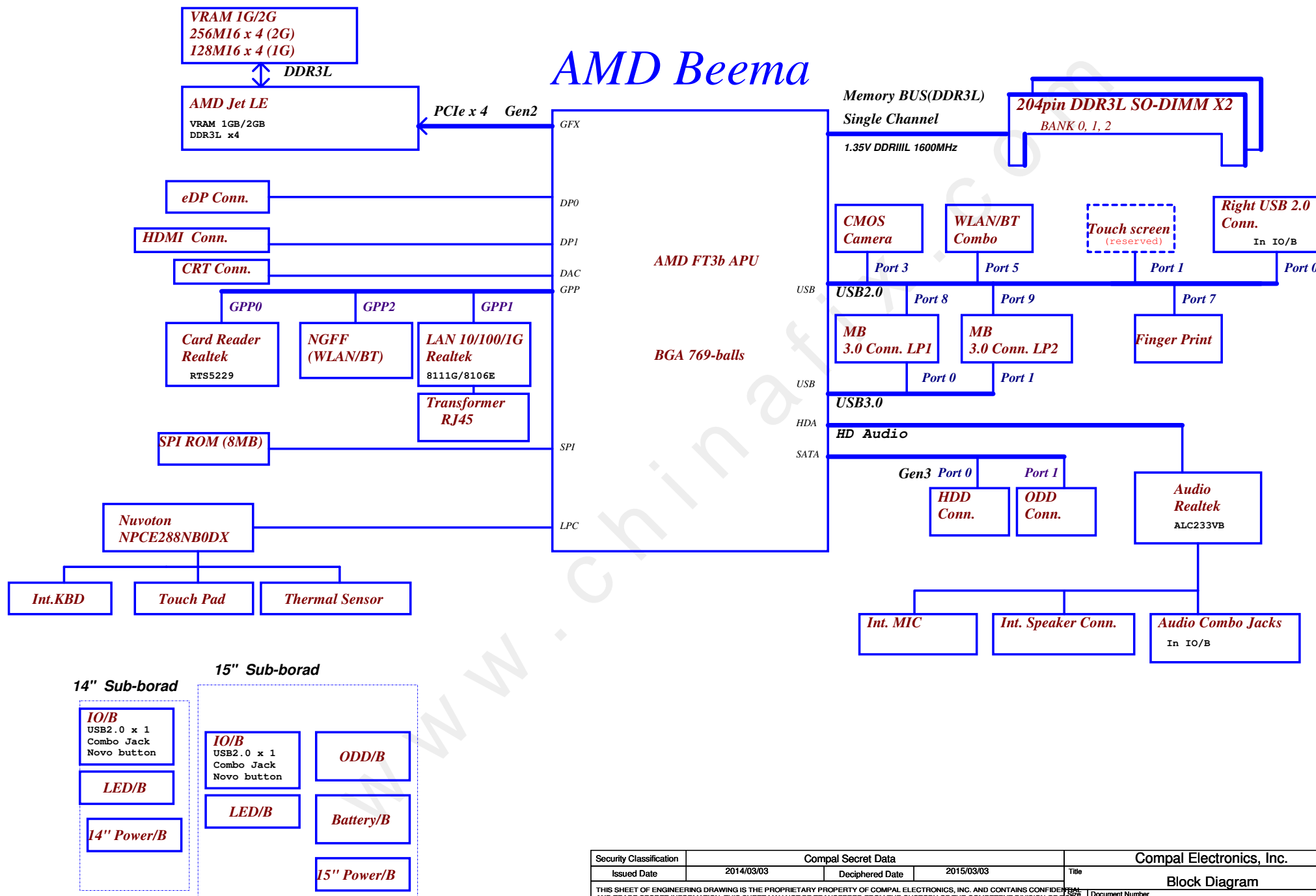
AMD Jet LE

2014-03-03

LA-B291P

REV : 1.0

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2014/03/03		2015/03/03		Cover Page	
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Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title	Block Diagram
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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+0.95VALW	0.95V always on power rail	ON	OFF	OFF
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.35V	1.35V power rail for APU and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+3VGS	3.3V switched power rail for VGA	ON	OFF	OFF
+1.8VGS	1.8V switched power rail for VGA	ON	OFF	OFF
+1.35VGS	1.35V switched power rail for VGA	ON	OFF	OFF
+0.95VGS	0.95V switched power rail for VGA	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	ON	ON
+0.675VS	0.675V switched power rail for DDR terminator	ON	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	MP
1	PVT
2	DVT
3	EVT
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
R1562	100K +/- 5%			
Board ID	R1564	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

USB OC MAPPING

OC#	USB Port
0	USB20 port0
1	USB20 port1,2,8,9
2	
3	

BOM Structure Table

BOM Structure	BTO Item
45@	for HDMI Logo
14@	for 14" component
15@	for 15" component
B5@	15W 2.4GHz BGA APU
B4@	15W 1.8GHz BGA APU
B3@	15W 1.5GHz BGA APU
B2@	10W 1.5GHz BGA APU
B1@	10W 1.35GHz BGA APU
UMA@	UMA part
PX@	Common VGA circuit
JET@	Jet LE GPU
TOPAZ@	Topaz XT GPU
CMOS@	CMOS Camera part
HDMI@	HDMI part
8106ELDO@	Realtek RTL8106E with LDO mode
8106ESW@	Realtek RTL8106E with SWR mode
8111GLDO@	Realtek RTL8111G with LDO mode
8111GSW@	Realtek RTL8111G with SWR mode
TS@	Touch Screen
ZODD@	Zero Power ODD part
NOZODD@	Non-Zero Power ODD part
CHG@	USB Charger function
NOCHG@	Non-USB Charger function
FHD@	Full HD Panel
DR@	VRAM Dual Rank
SR@	VRAM Single Rank
USB2@	USB 2.0
USB3@	USB 3.0
233VB@	Realtek ALC233-VB Audio IC
ME@	ME part
EMIP@	EMI pop component
EMIU@	EMI Un pop component
ESDP@	ESD pop component
ESDU@	ESD Un pop component
GIGAEMIP@	EMI Un pop for LAN GIGA function
@	Unpop

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	FCH	APU	RTD2132
SMB_EC_CK1 SMB_EC_DA1	288N +3VALW	X	V +3VALW	X	X	X	X	X	X	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V +3VS	V +3VS	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	288N +3VS	V +3VS	X	X	X	X	V +3VS	X	V +3VS	X

APU PCIE PORT LIST

Port	Device
0	Card Reader
1	LAN
2	WLAN
3	

USB Port Table

USB 2.0	USB 3.0	Port	3 External USB Port
		0	Touch Screen
		1	RIGHT USB
		2	
		3	Camera
		4	
		5	WLAN/BT Combo
		6	
		7	Finger Print
		8	LEFT USB3.0
		9	LEFT USB3.0
	XHCI	0	
		1	

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	Thermal Sensor	1001 101X b	9AH
			SB-TSI (APU)	1001 100X b	98H
			VGA Internal Thermal	1000 001X b	82H

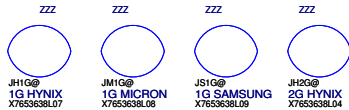
APU SM Bus address

Device	Address	HEX
DDR DIMM1	1010 000Xb	A0H
DDR DIMM2	1010 001Xb	A2H

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Jet LE VRAM STRAP

		X76@			X76@			
		Vendor UV5, UV6, UV7, UV8	ID	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV21	R_pd RV24
1GBytes	ZZZ09 JH1G@	Hynix 2048Mbits SA00006H400 128Mx16 H5TC2G63FFR-11C	0	0	0	0	NC	4.75K
1GBytes	ZZZ10 JM1G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	1	0	0	1	8.45K	2K
1GBytes	ZZZ11 JS1G@	Samsung 2048Mbits SA000068U40 128Mx16 K4W2G1646Q-BC1A	2	0	1	0	4.53K	2K
2GBytes	ZZZ12 JH2G@	Hynix 4096Mbits SA00006E800 256Mx16 H5TC4G63AFR-11C	3	0	1	1	6.98K	4.99K
2GBytes	ZZZ13 JS2G@	Samsung 4096Mbits SA000076P00 256Mx16 K4W4G1646D-BC1A	4	1	0	0	4.53K	4.99K
2GBytes	ZZZ14 JM2G@	Micron 4096Mbits SA000077K00 256Mx16 MT41J256M16HA-093G:E	5	1	0	1	3.24K	5.62K
2GBytes	ZZZ08 JM2G2@	Micron 4096Mbits SA000065D00 256Mx16 MT41K256M16HA-107G:E	6	1	1	0	3.4K	10K
1GBytes	ZZZ16 JM1G2@	Micron 2048Mbits SA00005XB00 128Mx16 MT41K128M16JT-107G:K	7	1	1	1	4.75K	NC



R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Power-Up/Down Sequence

"Jet" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
- It is recommended that the 3.3-V rail ramp up first.
- It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2ms from the start of VDDC ramping up.
- The power rails that are shared with other components on the system should be gated for the dGPU so that when dGPU is powered down (for example AMD PowerXpress™ idle state), all the power rails are removed from the dGPU.
- The gate circuits must meet the slew rate requirement (such as $\leq 50\text{mV/us}$).
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

VDDR3(+3VGS)

PCIE_VDDC(+0.95VGS)

VDDR1(+1.35VGS)

VDDC/VDDCI(+VGA_CORE)

VDD_CT(+1.8VGS)

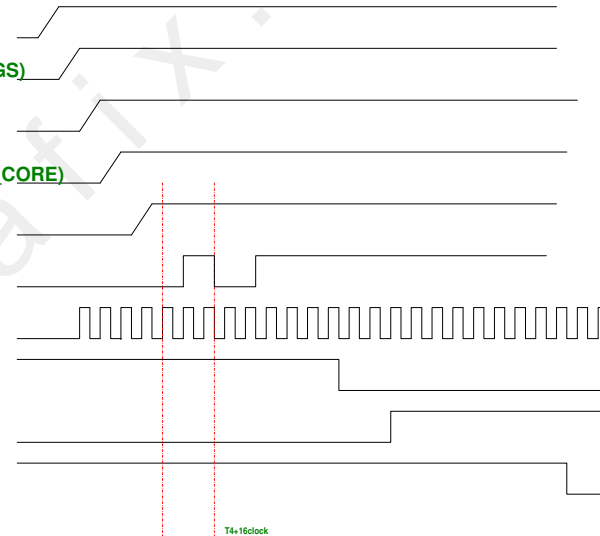
PERSTb

REFCLK

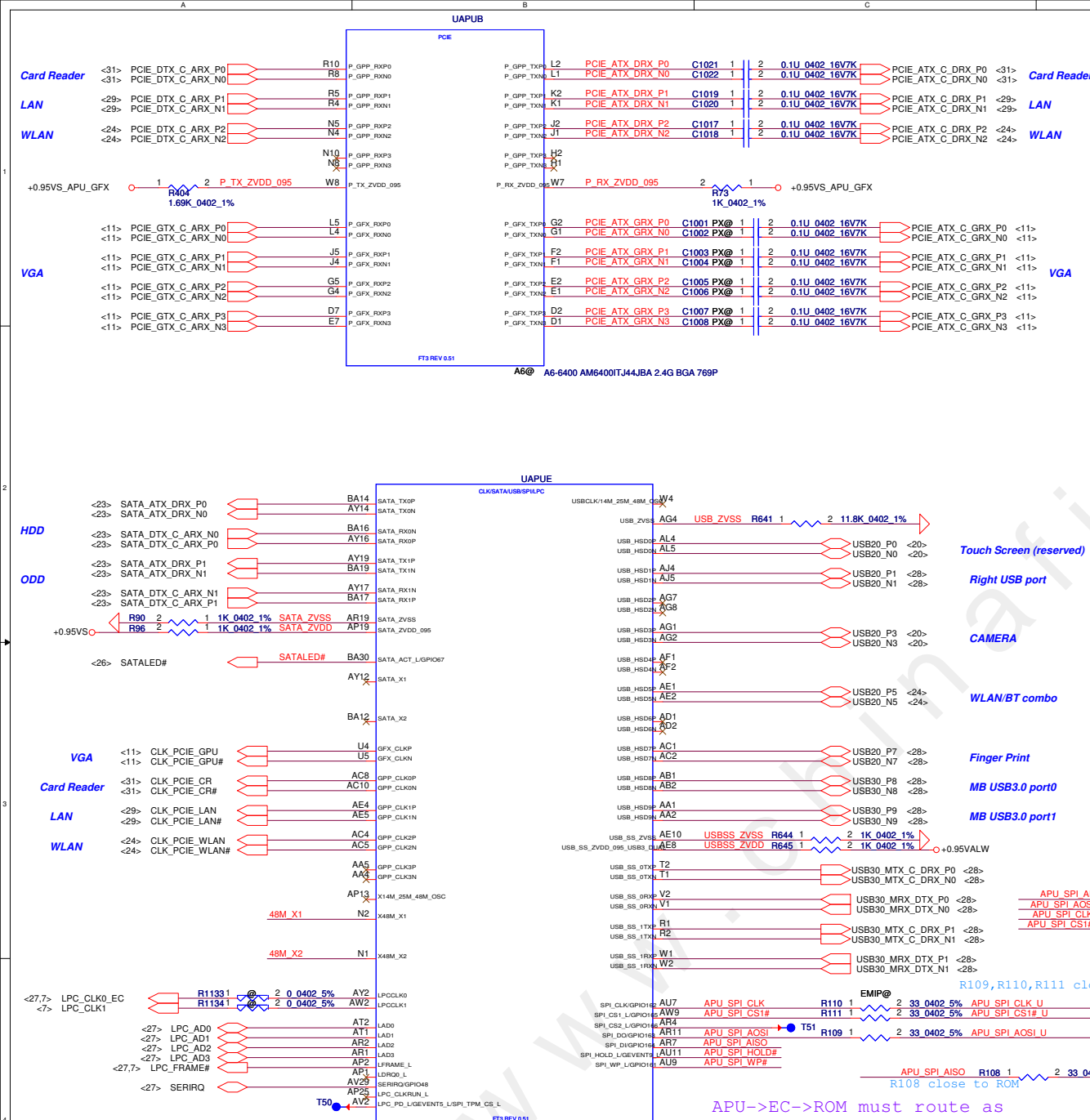
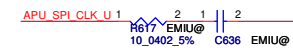
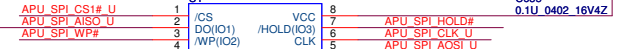
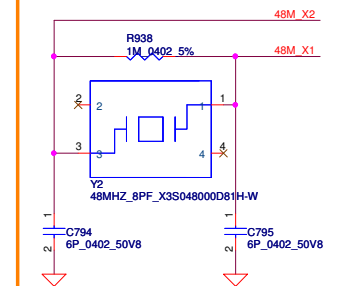
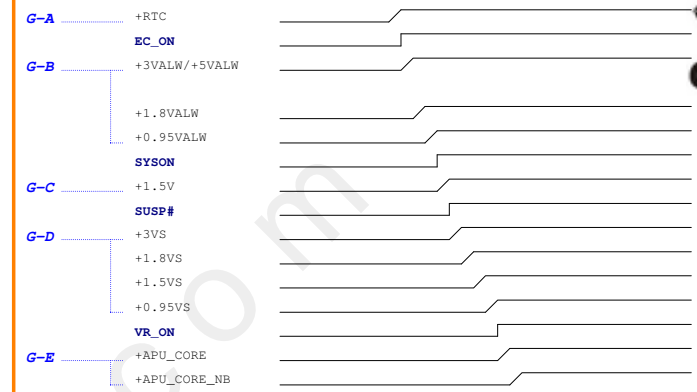
Straps Reset

Straps Valid

Global ASIC Reset

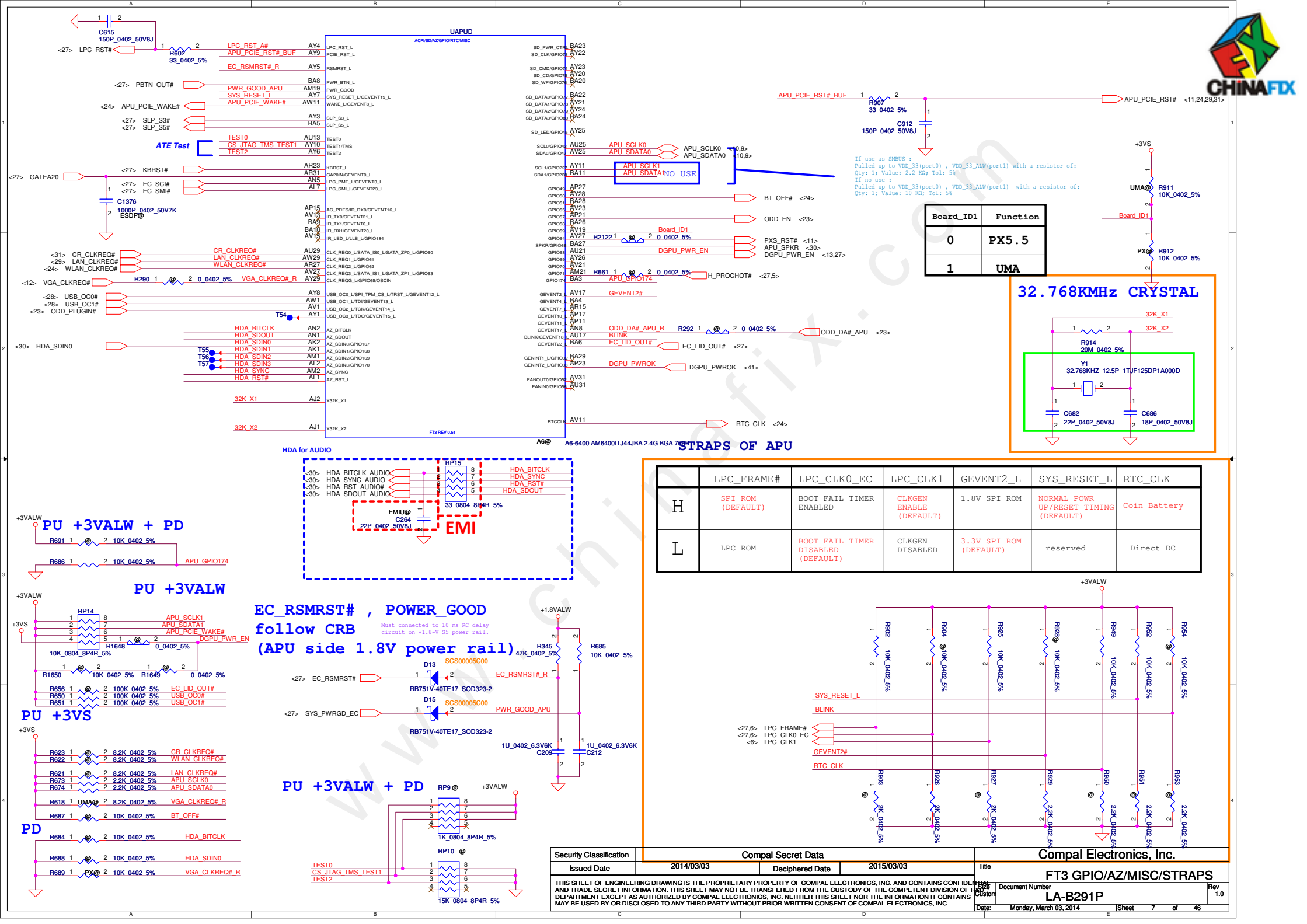






APU->EC->ROM must route as
2.4GB/s Chain for Share ROM quality
(RP12 was request to added for the recoverable
solution as original method)

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								FT3 PCIE/SATA/CLK/USB/SPI			
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Board ID and Function

Board_ID1	Function
0	PX5.5
1	UMA

LPC Frame# and Signals

LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	SYS_RESET_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWR UP/RESET TIMING (DEFAULT)
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	reserved

Security Classification

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FT3 GPIO/AZ/MISC/STRAPS

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Board ID and Function

Board_ID1	Function
0	PX5.5
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LPC Frame# and Signals

LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	SYS_RESET_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWR UP/RESET TIMING (DEFAULT)
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	reserved

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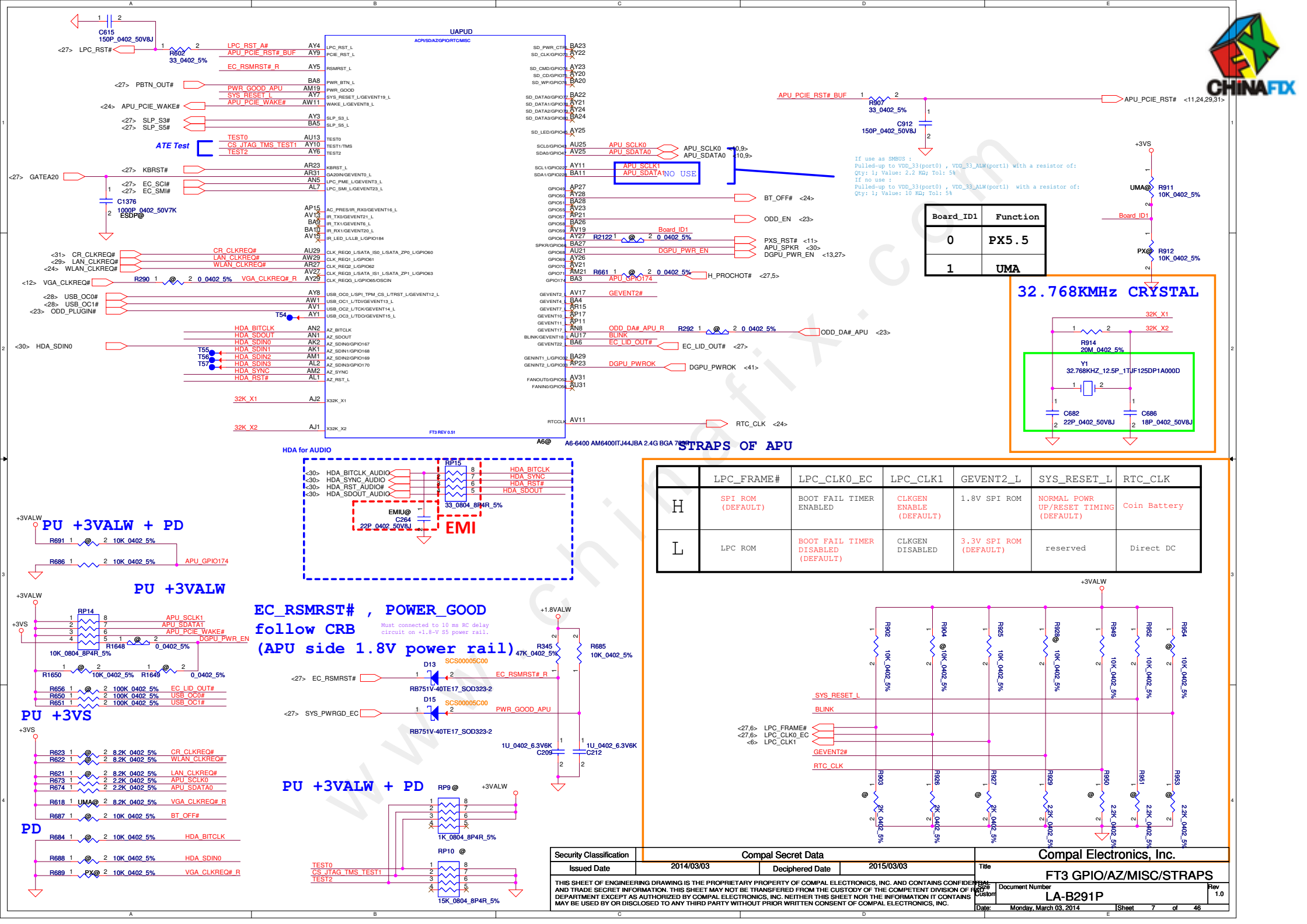
FT3 GPIO/AZ/MISC/STRAPS

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Board ID1 and Function Table:

Board_ID1	Function
0	PX5.5
1	UMA

STRAPS of APU Table:

	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	SYS_RESET_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWR UP/RESET TIMING (DEFAULT)	Coin Battery
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	reserved	Direct DC

Security Classification Table:

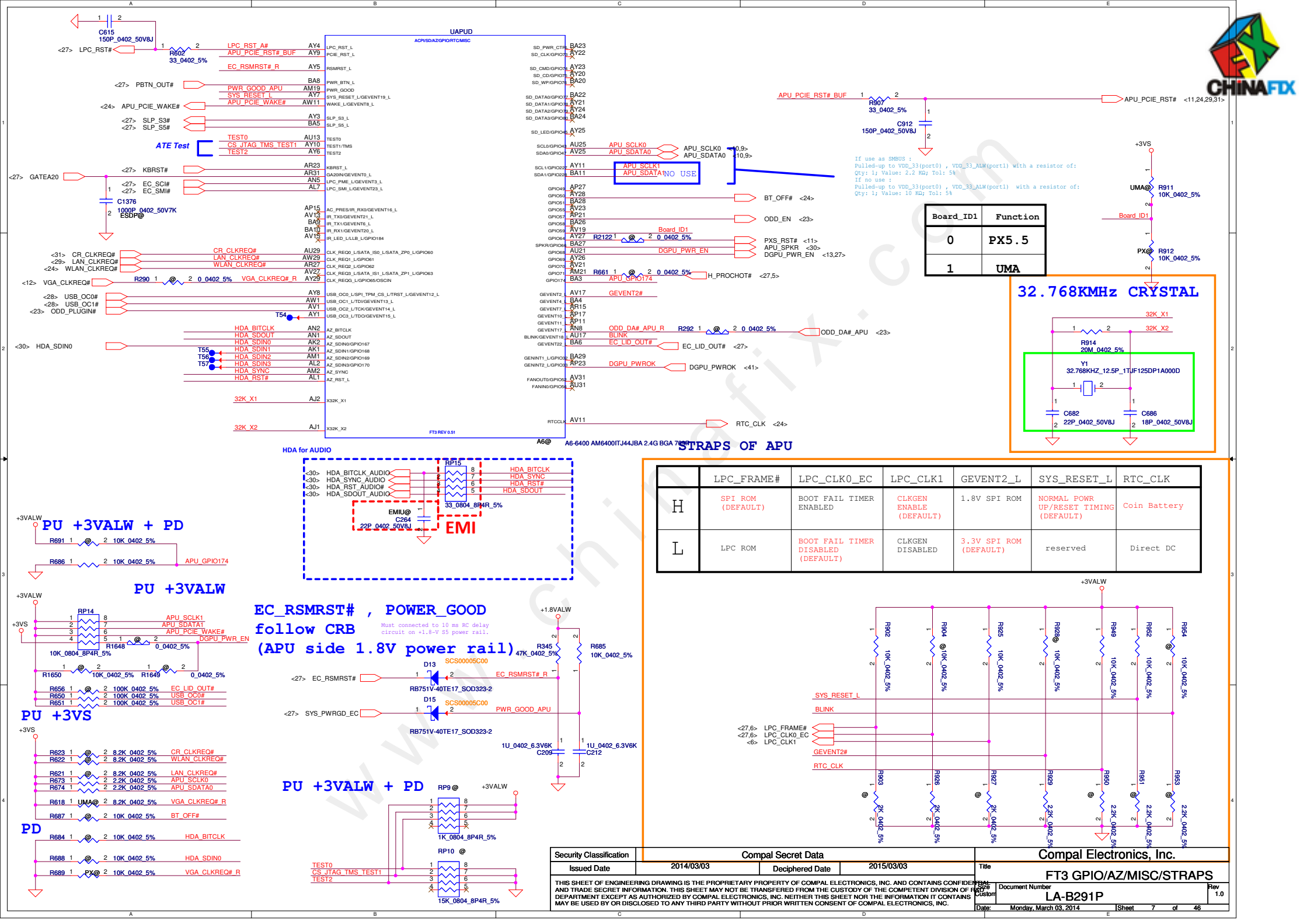
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Board ID1 and Function Table:

Board_ID1	Function
0	PX5.5
1	UMA

STRAPS of APU Table:

	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	SYS_RESET_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWR UP/RESET TIMING (DEFAULT)	Coin Battery
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	reserved	Direct DC

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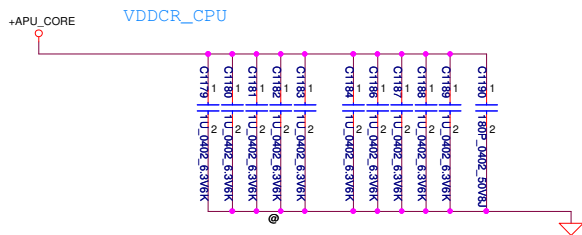
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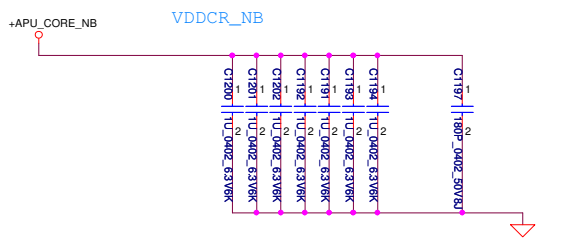
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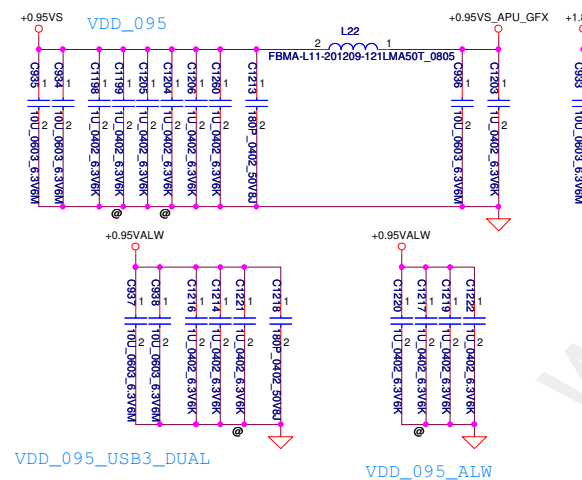
CORE POWER OF APU



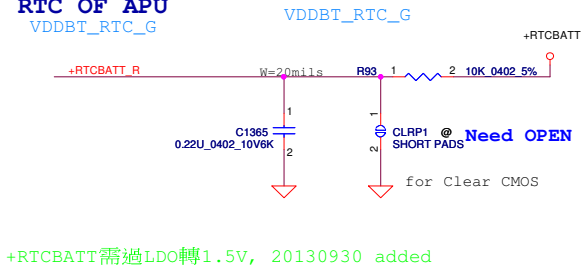
INTEGRATED GPU POWER OF APU



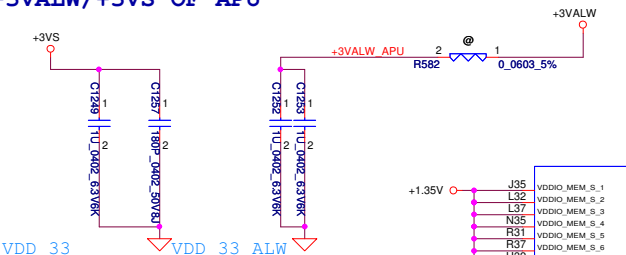
+0.95VALW/+0.95VS OF APU



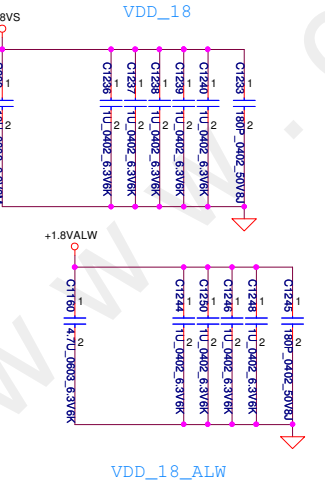
RTC OF APU
VDDBT_RTC_G



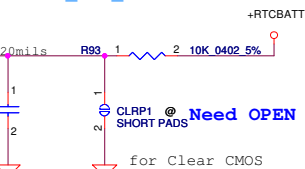
+3VALW/+3VS OF APU



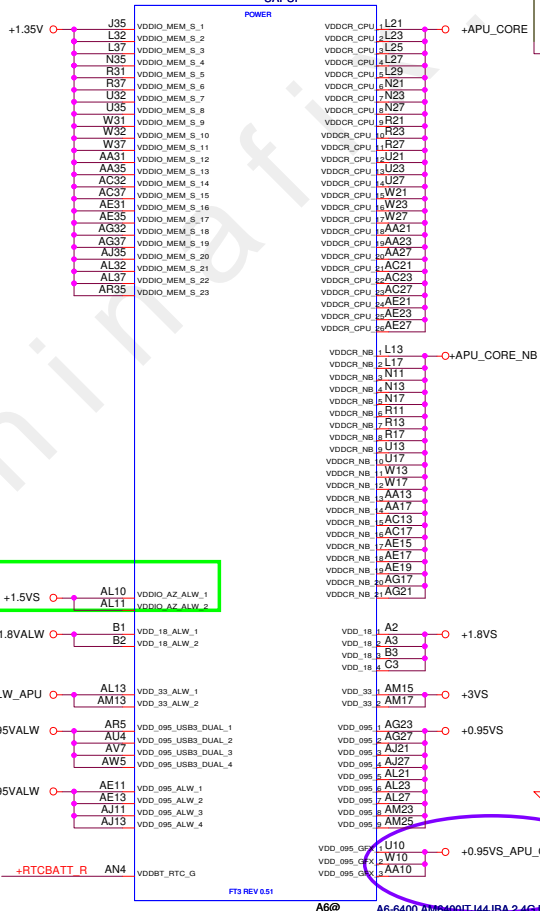
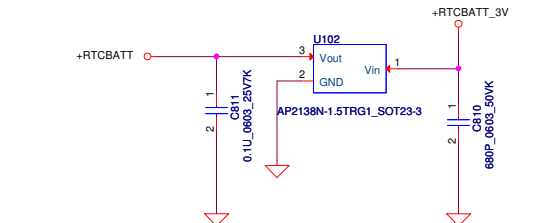
+1.8VALW/+1.8VS OF APU



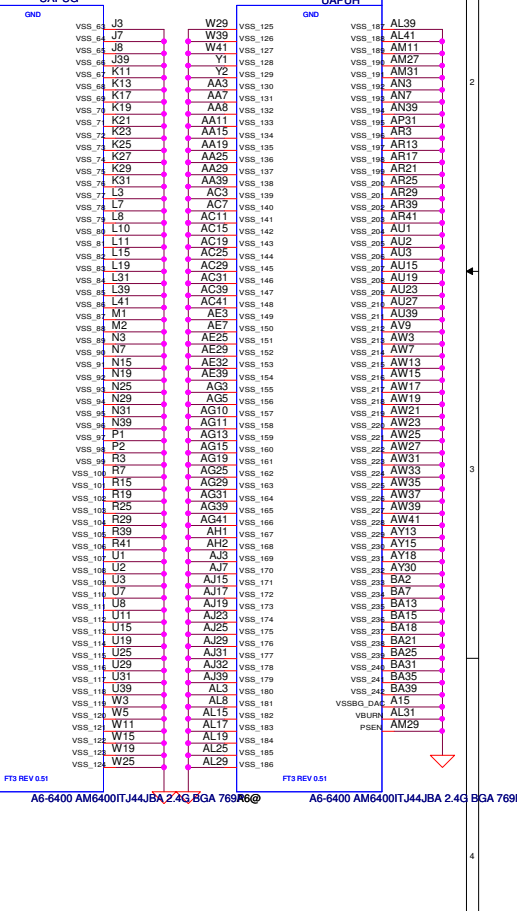
VDDBT_RTC_G



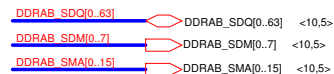
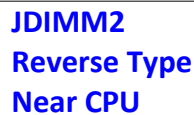
Need use +3.3V transfer to +1.5V LDO to APU side for Beema



LIAPLIC



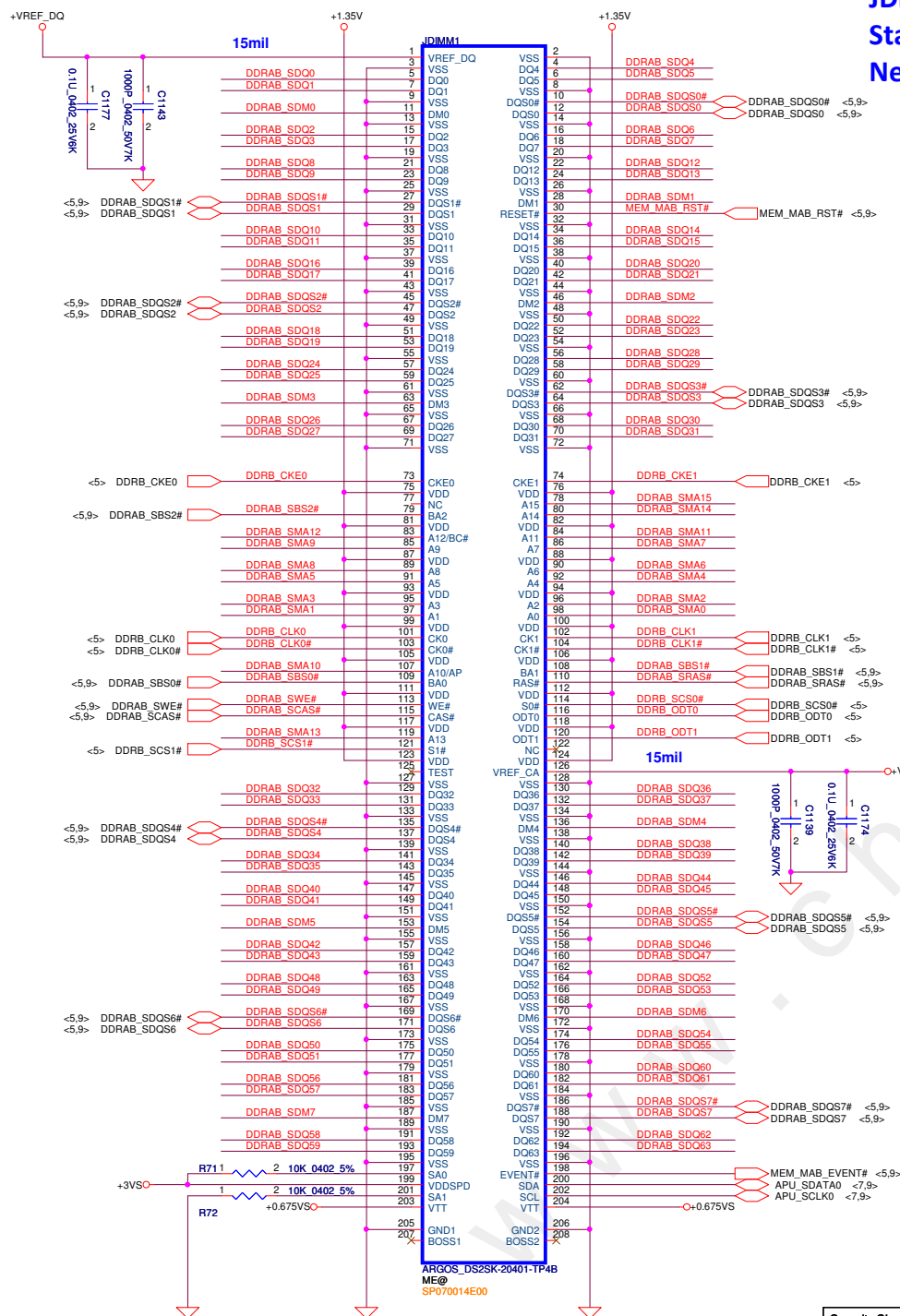
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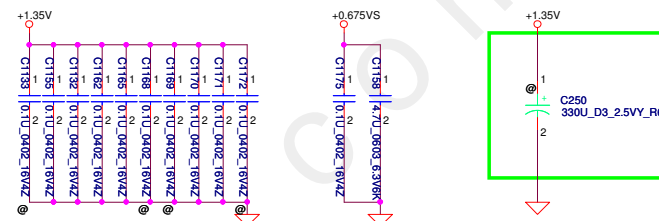
DIMM_A H:4mm
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JDIMM1
Standard Type
Near User



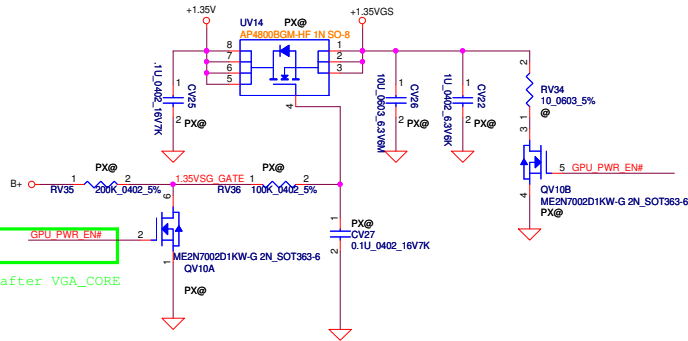
+1.35V/+0.675VS OF DIMM2



DIMM_B H:4mm
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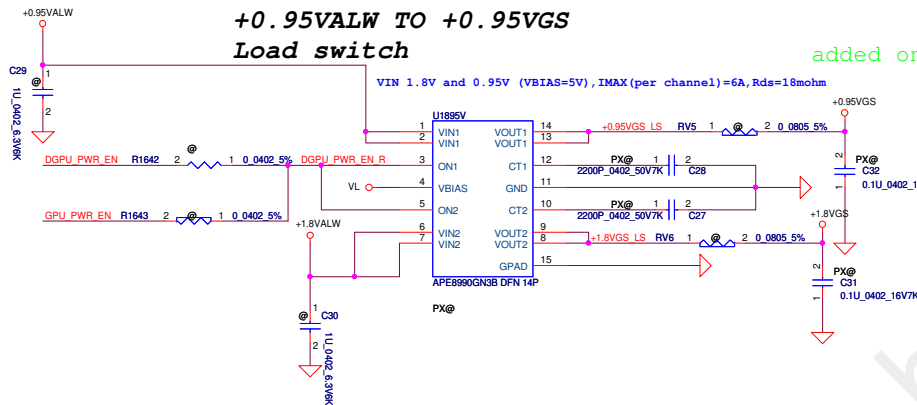
+1.35VS to +1.35VGS



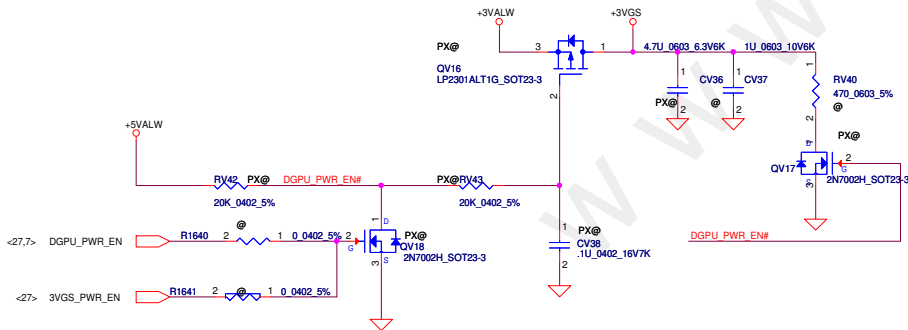
+1.35VGS arises after VGA_CORE

+1.8VALW TO +1.8VGS
+0.95VALW TO +0.95VGS
Load switch

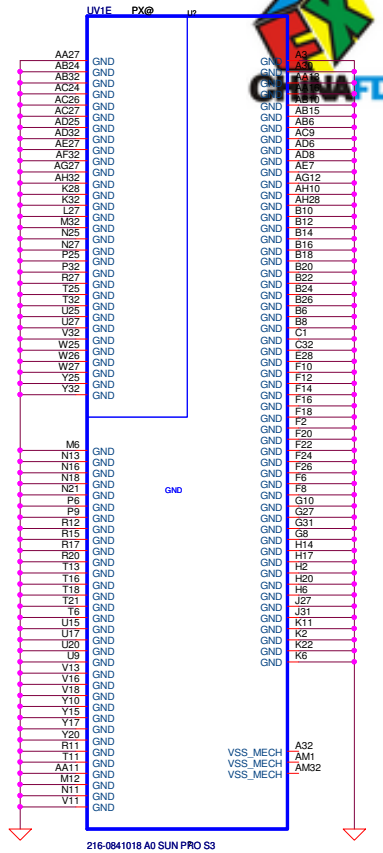
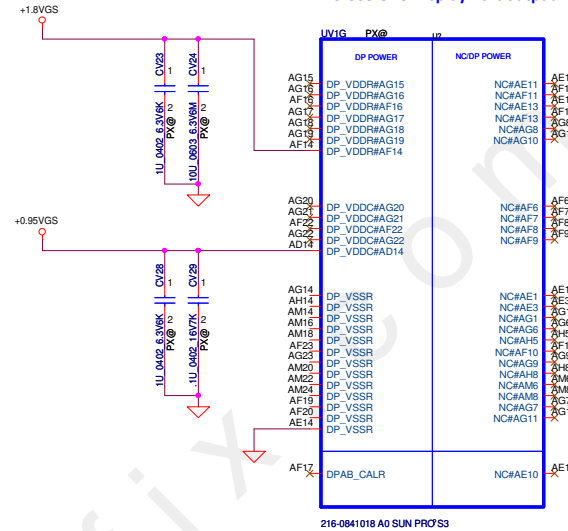
added on 9/28



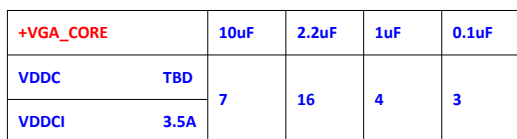
+3VS to +3VS_VGA



No Use GPU Display Port output

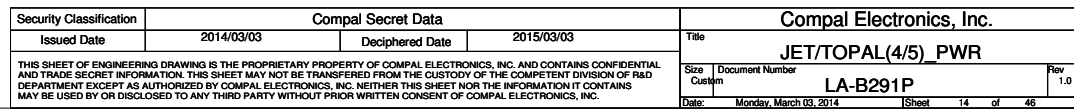







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				Date	Monday, March 03, 2014
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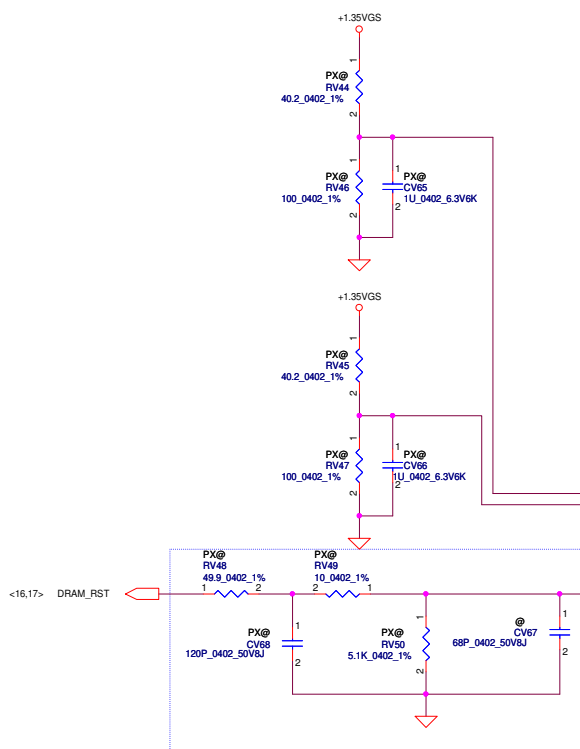


+1.35VGS		10uF	1uF	0.1uF	0.01uF
VDDR1	1.5A	5(3@)	5	5	0

+3VGS		10uF	1uF	0.1uF
VDDR3	25mA	0	1	0

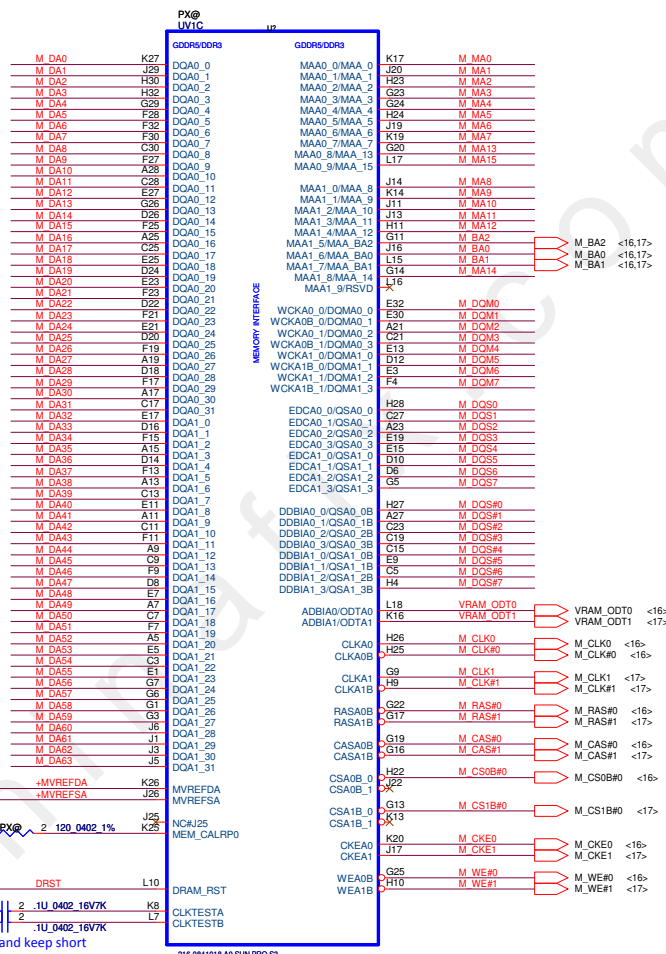


<16,17> M_DA[63..0]  M_DA[63..0]
 <16,17> M_MA[15..0]  M_MA[15..0]
 <16,17> M_DQM[7..0]  M_DQM[7..0]
 <16,17> M_DQS[7..0]  M_DQS[7..0]
 <16,17> M_DQS# [7..0]  M_DQS# [7..0]



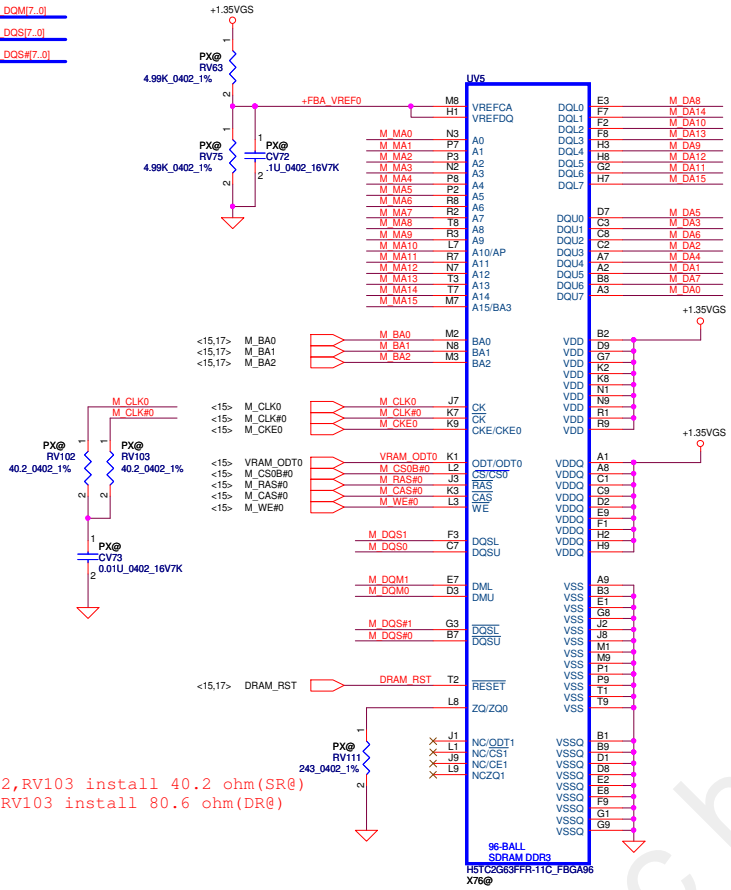
Place close to GPU (within 25mm)
 and place component close to each other

Route 50ohms single-ended/100ohm diff and keep short
 debug only, for clock observation, if not need, DNI.

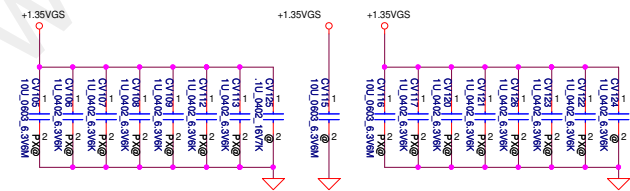
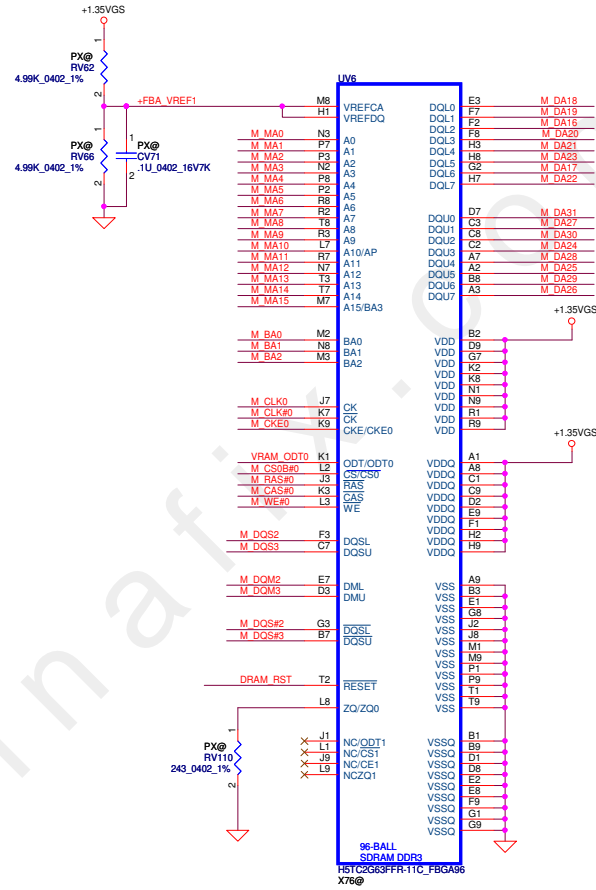


DDR3L Memory Channel Rank 0:A0

- <15,17> M_DA[63..0] M_DA[63..0]
- <15,17> M_MA[15..0] M_MA[15..0]
- <15,17> M_DOM[7..0] M_DOM[7..0]
- <15,17> M_DQS[7..0] M_DQS[7..0]
- <15,17> M_DQS# [7..0] M_DQS# [7..0]

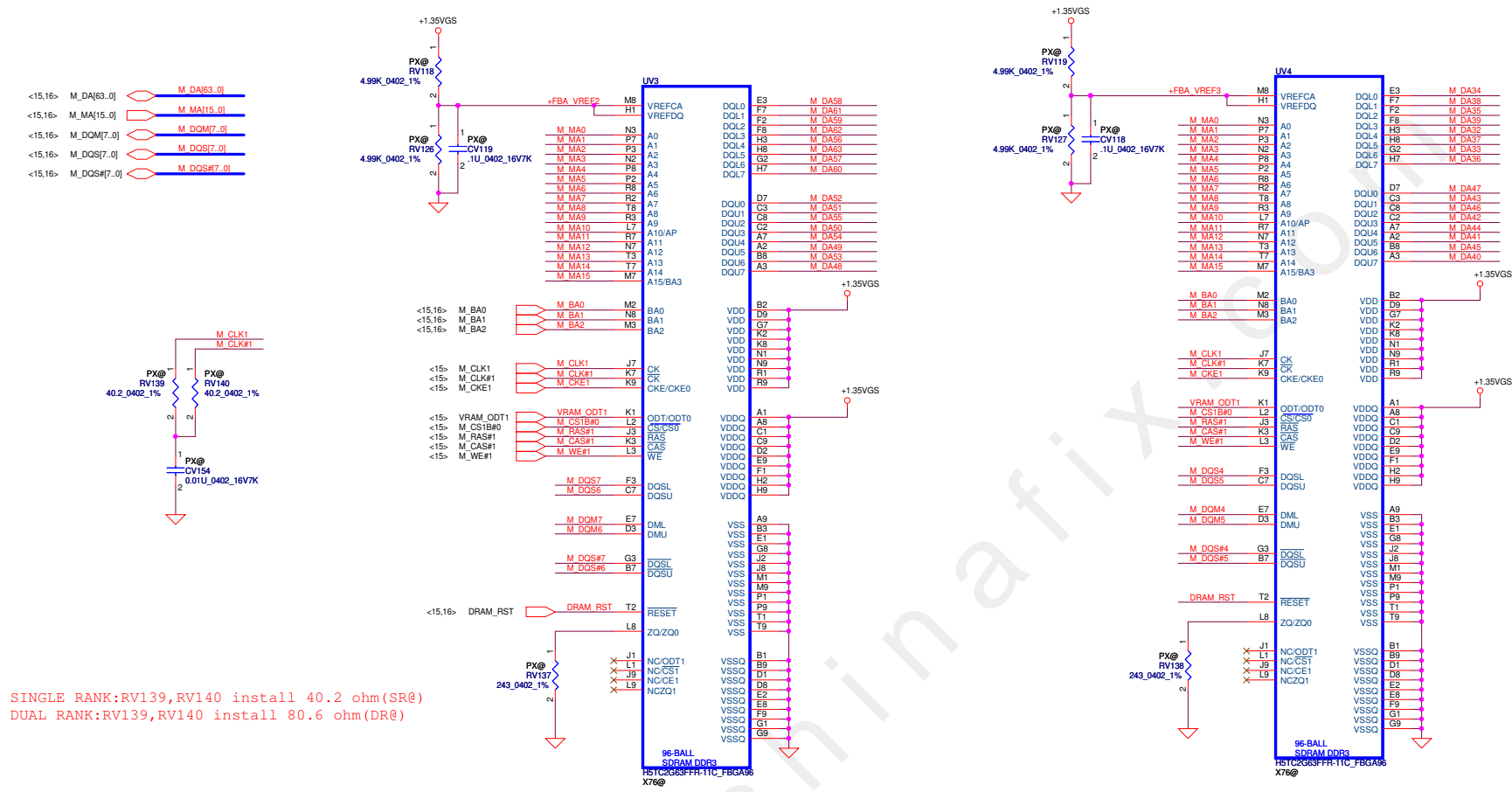


SINGLE RANK:RV102,RV103 install 40.2 ohm(SR@)
DUAL RANK:RV102,RV103 install 80.6 ohm(DR@)



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DDR3L Memory Channel Rank 0:A1



SINGLE RANK:RV139,RV140 install 40.2 ohm(SR@)
DUAL RANK:RV139,RV140 install 80.6 ohm(DR@)

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www.chinafix.com

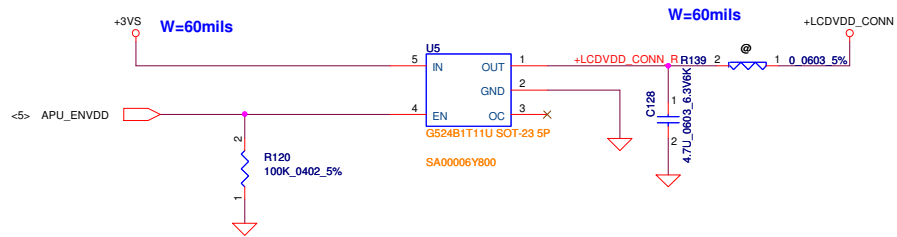
Title			
Reserved			
Size A	Document Number LA-B291P		Rev 1.0
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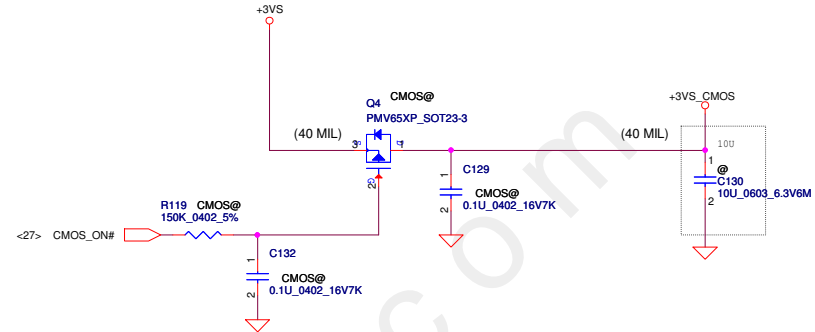
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			A
Title			
Reserved			
Size	Document Number	Rev	
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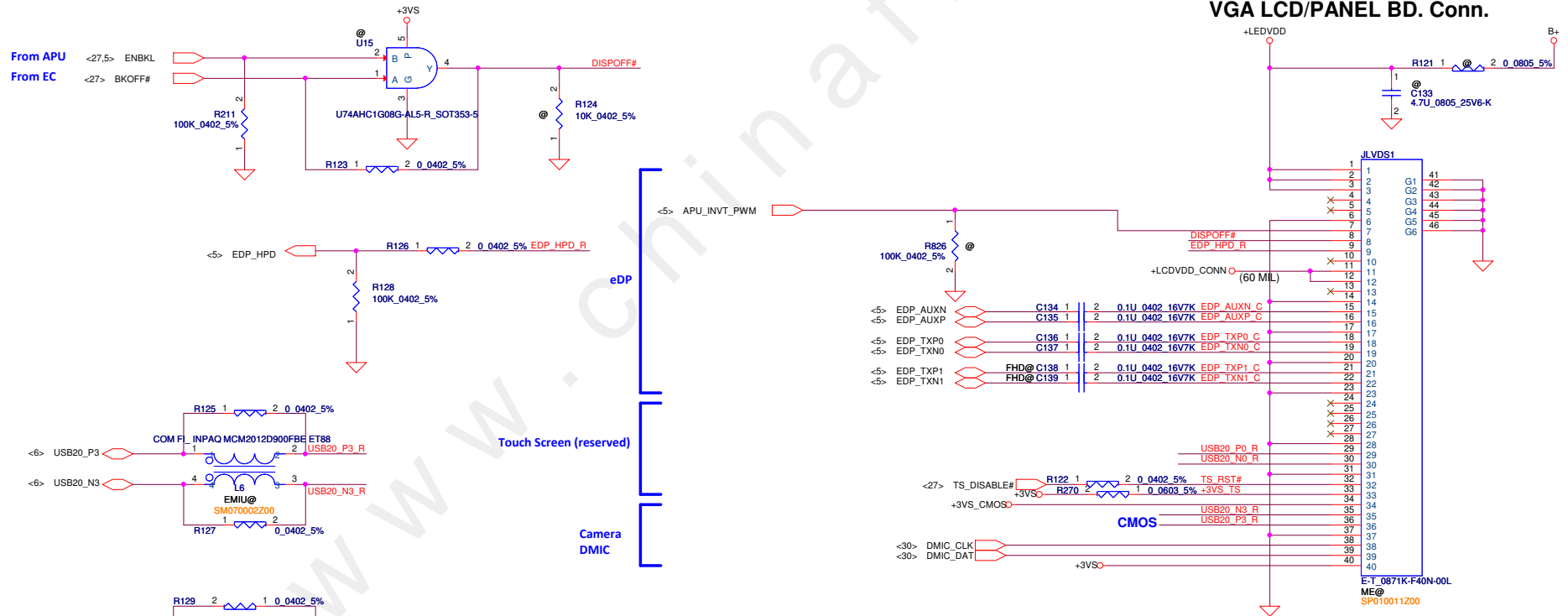
LCD POWER CIRCUIT



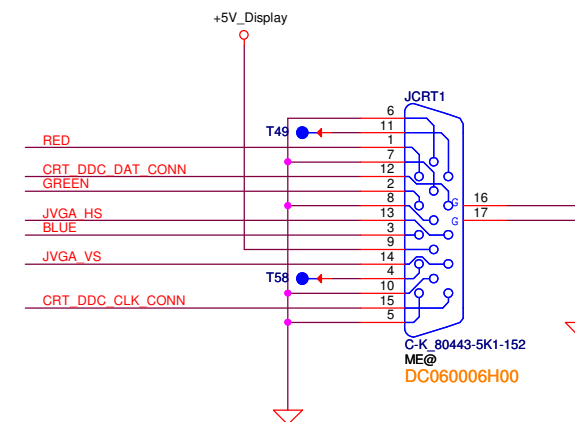
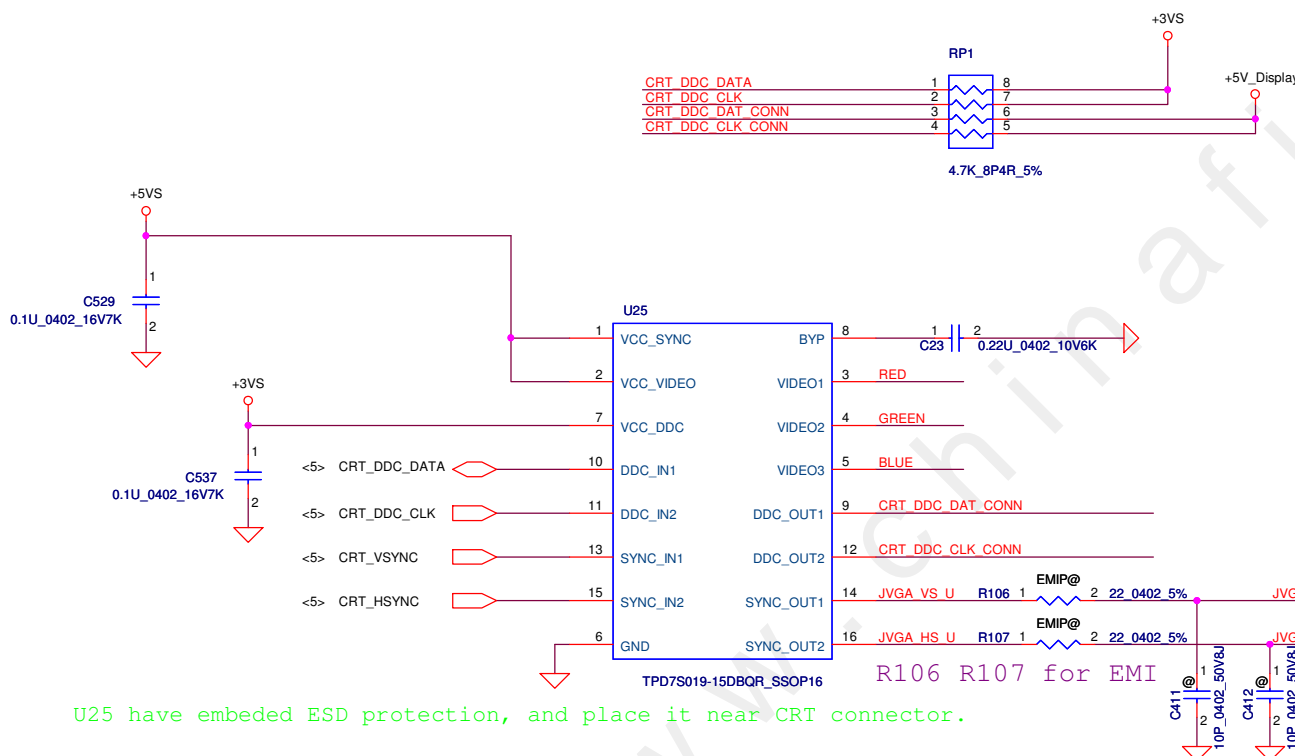
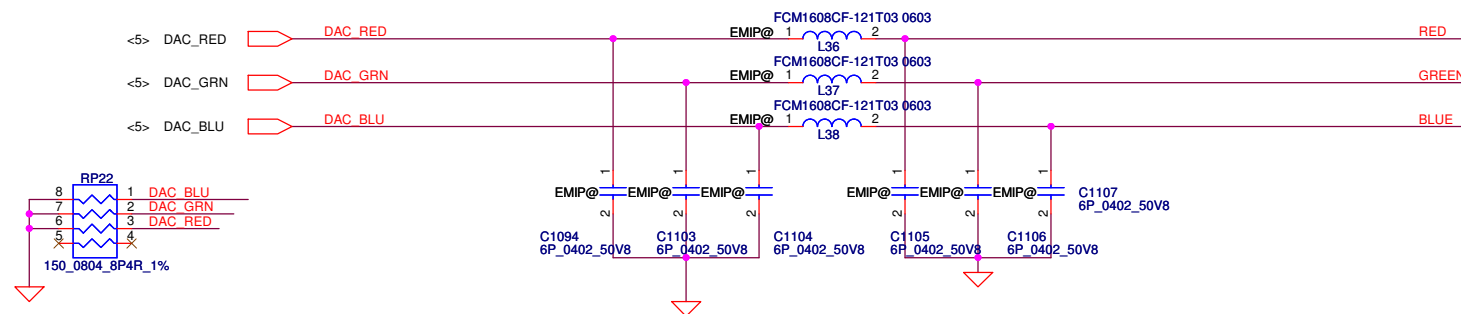
CMOS Camera



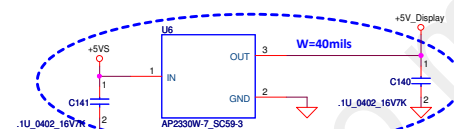
VGA LCD/PANEL BD. Conn.



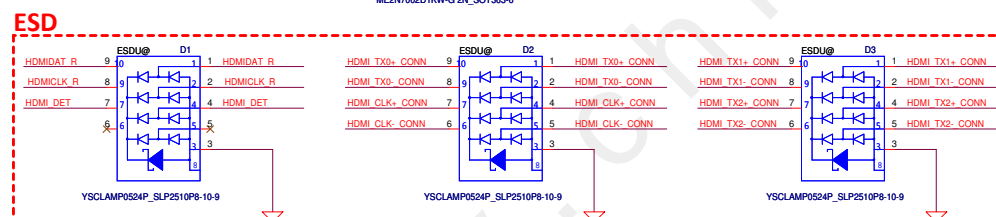
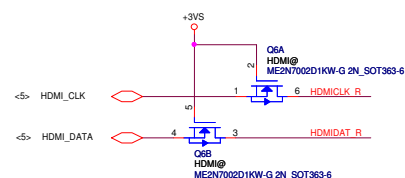
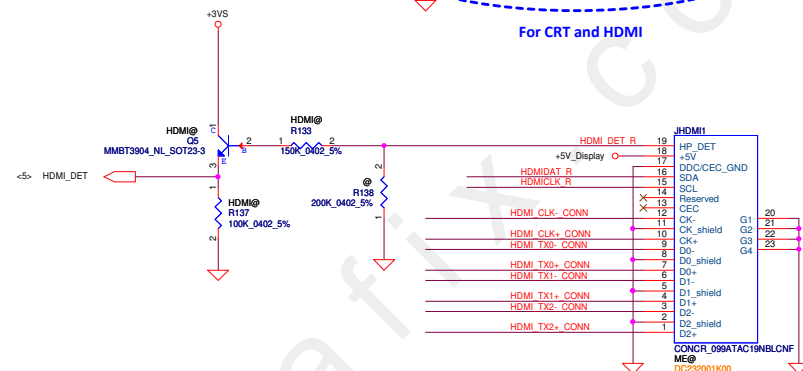
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Issued Date	2014/03/03	Deciphered Date	2015/03/03	Document Number
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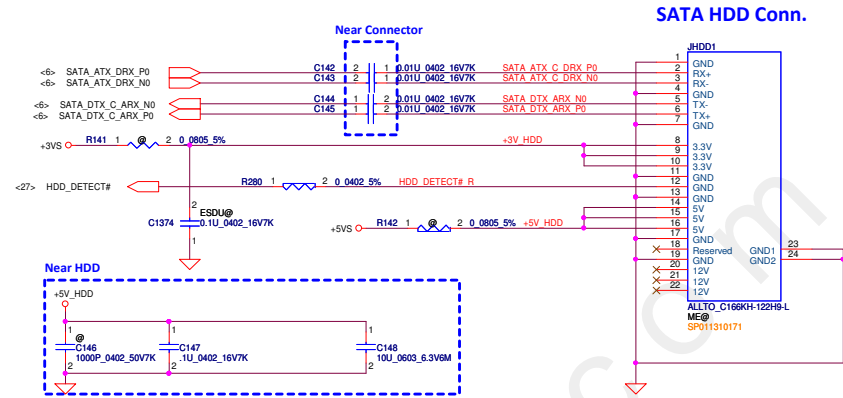
For CRT and HDMI



ESD protection needs to be placed near connector side

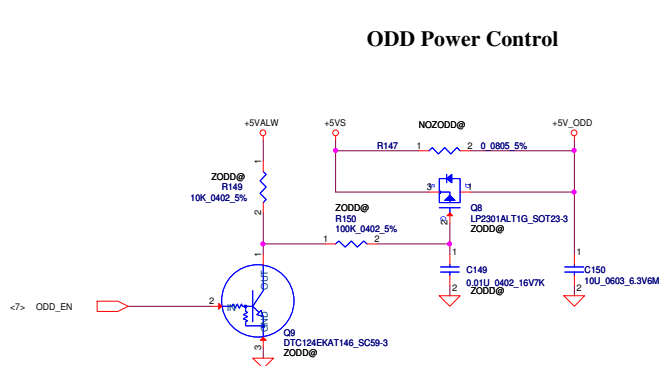
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title	HDMI CONN	
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HDD

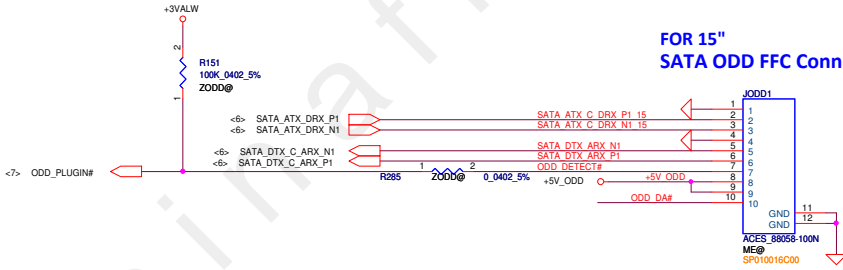


ODD

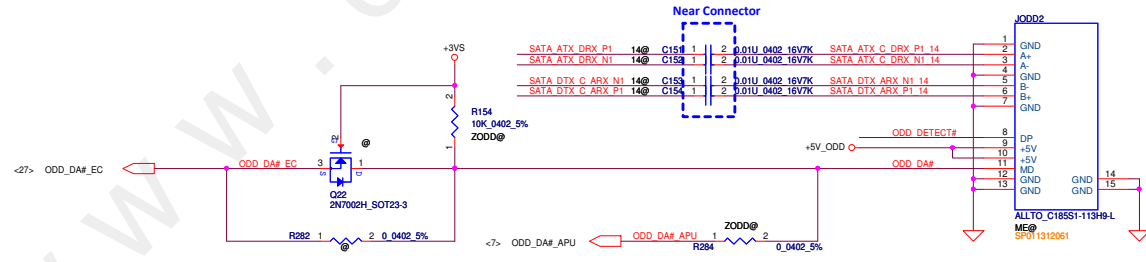
ODD Power Control



FOR 15" SATA ODD FFC Conn.



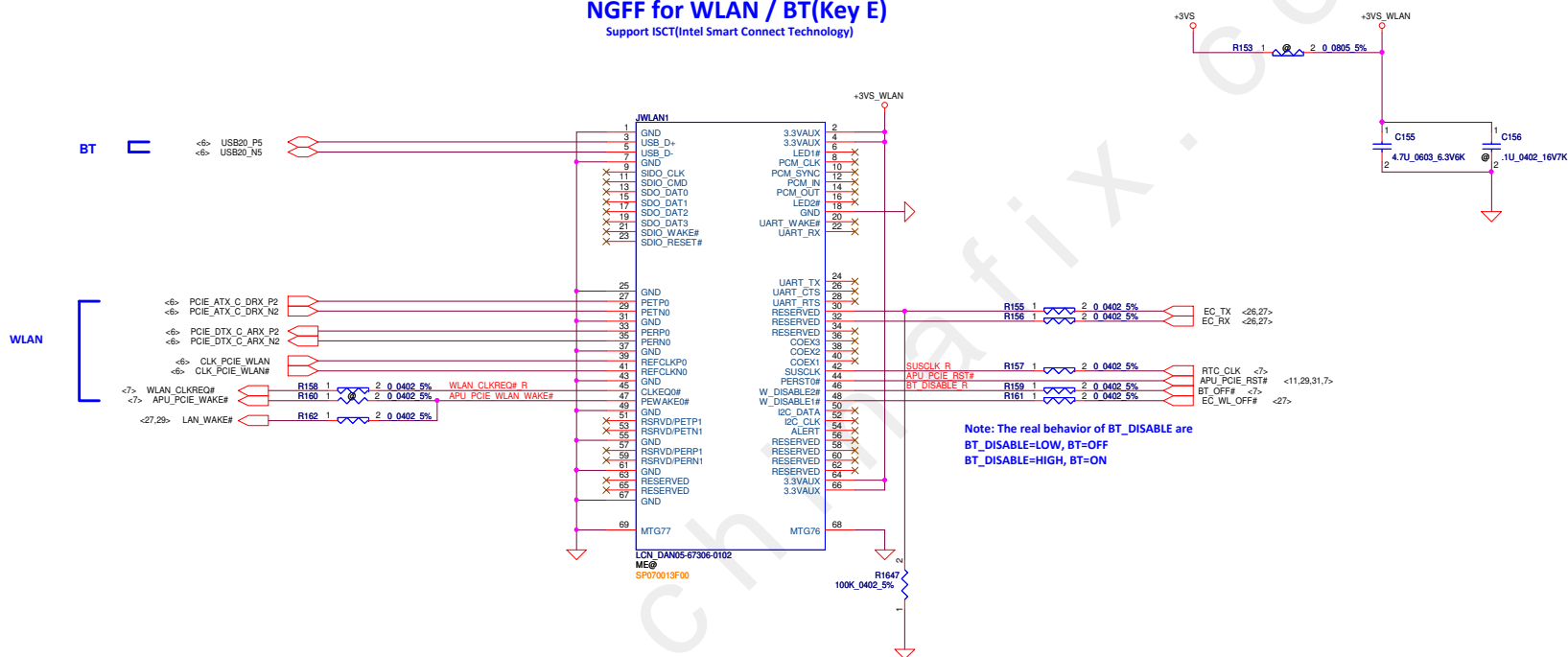
FOR 14" SATA ODD Conn.



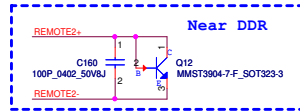
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Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title		
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NGFF for WLAN / BT(Key E)

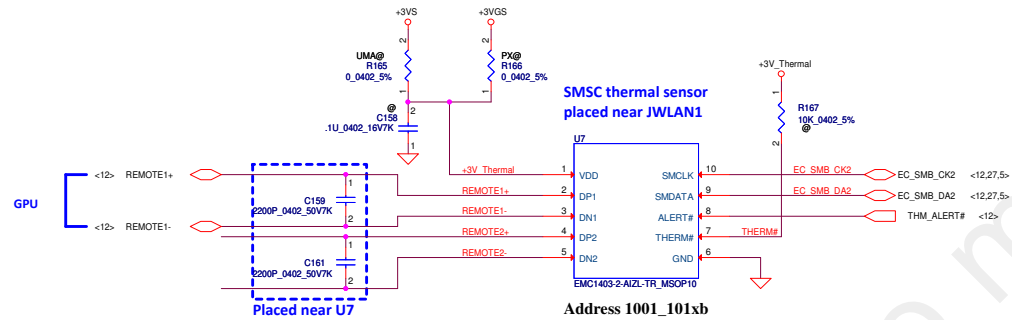
Support ISCT(Intel Smart Connect Technology)



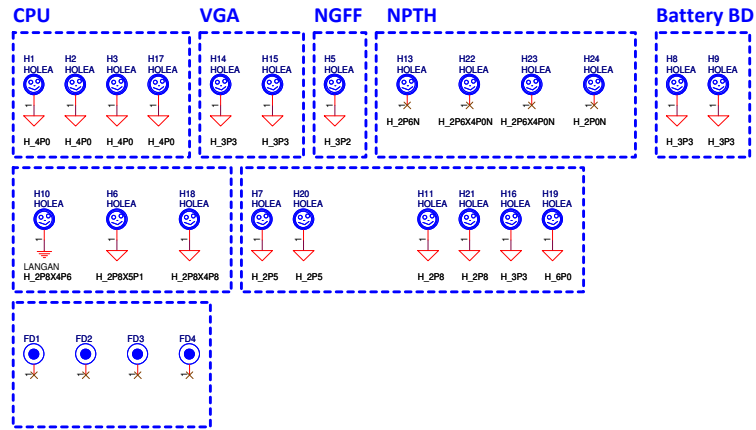
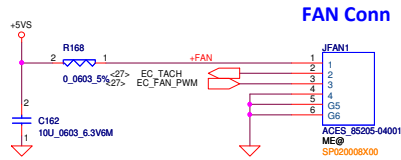
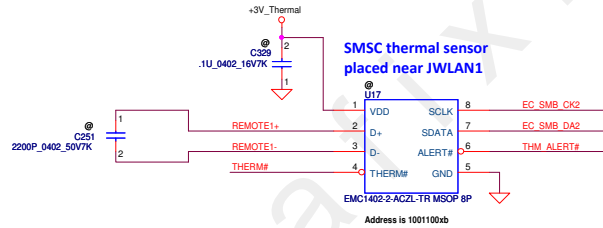
3 Channel



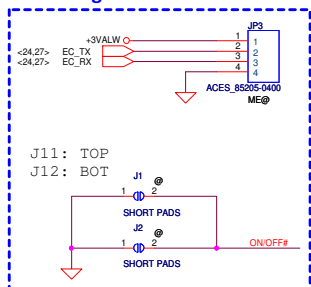
REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



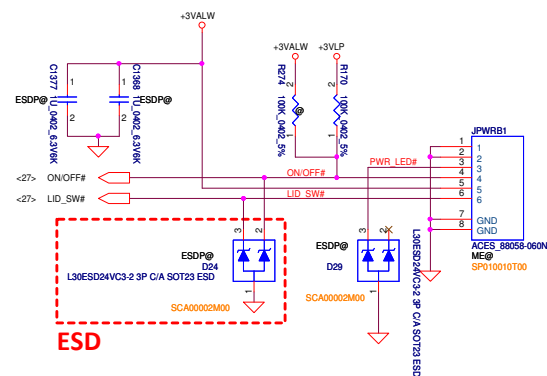
2 Channel



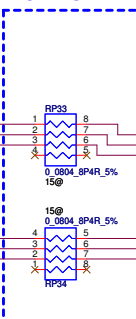
For Debug



ESD



For B15



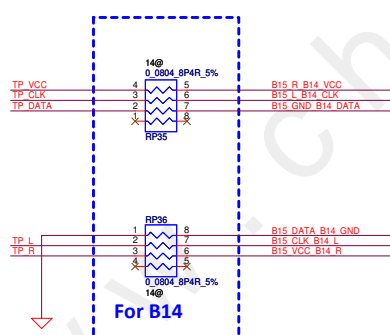
For B15/E14 TP module(100*50)

1	1	VCC	1	VCC
2	2	CLK	2	CLK
3	3	DAT	3	DAT
4	4	GND	4	L
5	5	L	5	R
6	6	R	6	GND

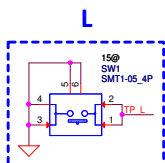
For B14 TP module(84*42)

6	1	VCC	1	VCC
5	2	CLK	2	CLK
4	3	DAT	3	DAT
3	4	GND	4	L
2	5	L	5	R
1	6	R	6	GND

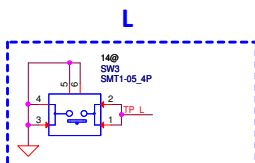
For B14



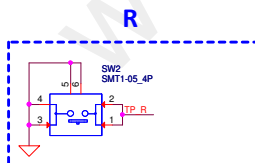
L



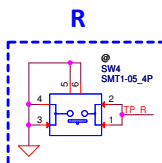
L



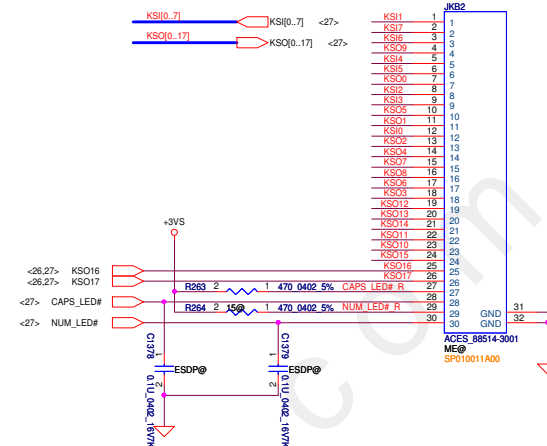
R



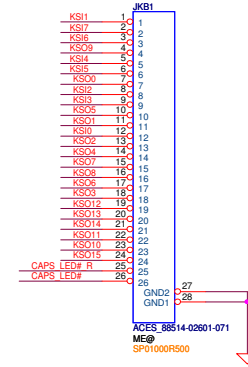
R



KB For B15



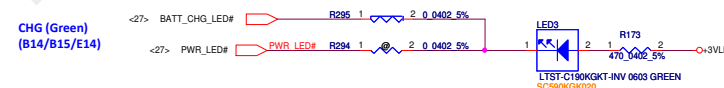
KB For B14/E14



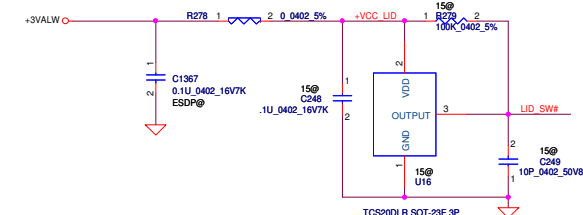
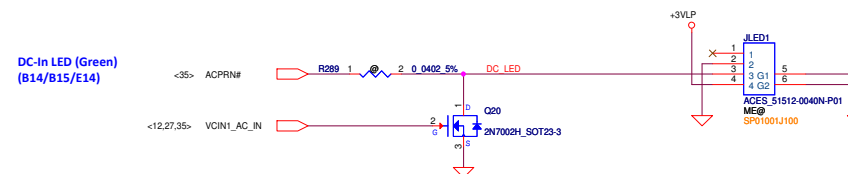
Battery (Amber)
(B14/B15/E14)



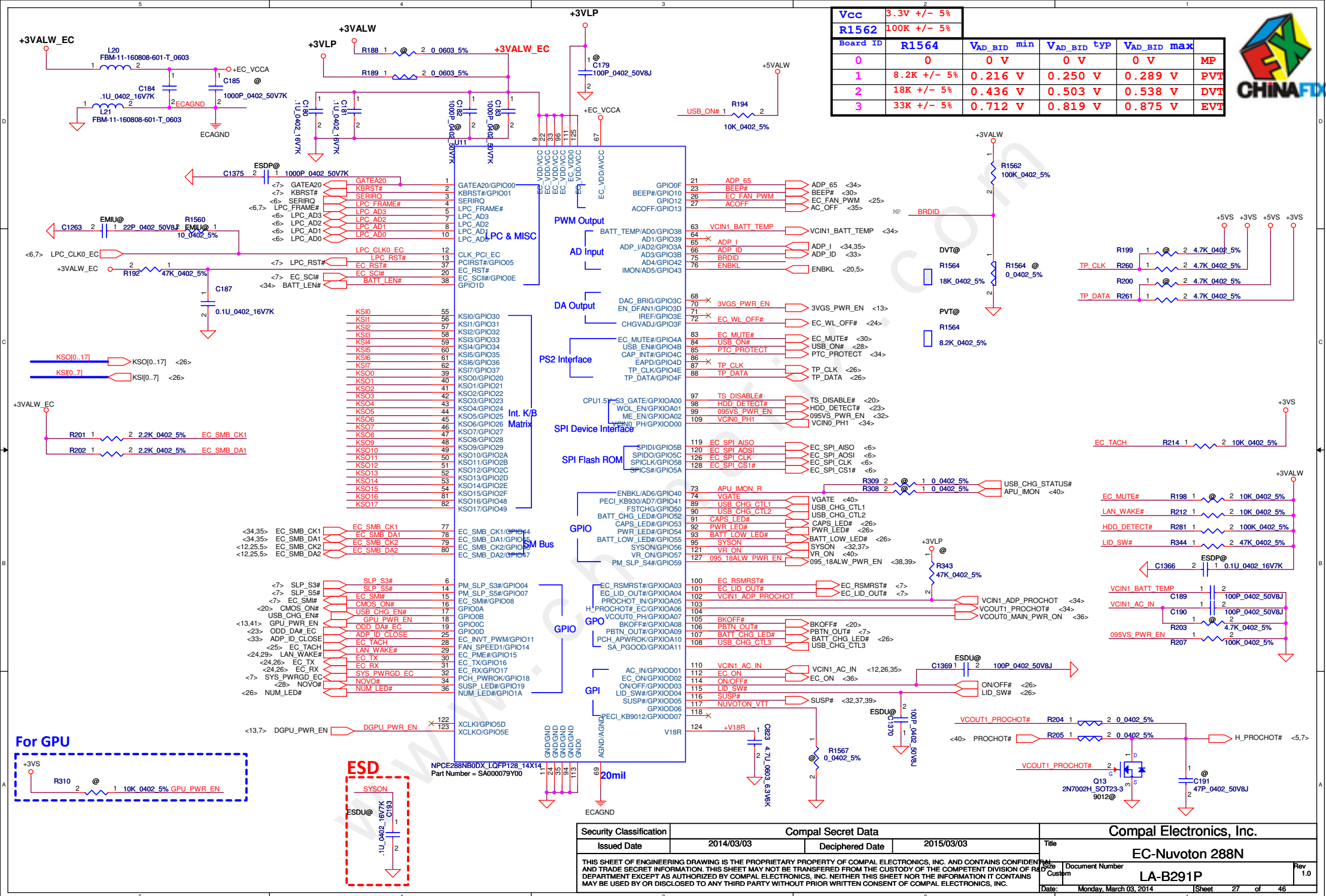
CHG (Green)
(B14/B15/E14)

HDD (Green)
(B14/B15/E14)

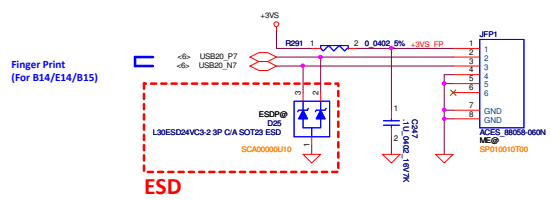
DC-In LED (Green)
(B14/B15/E14)



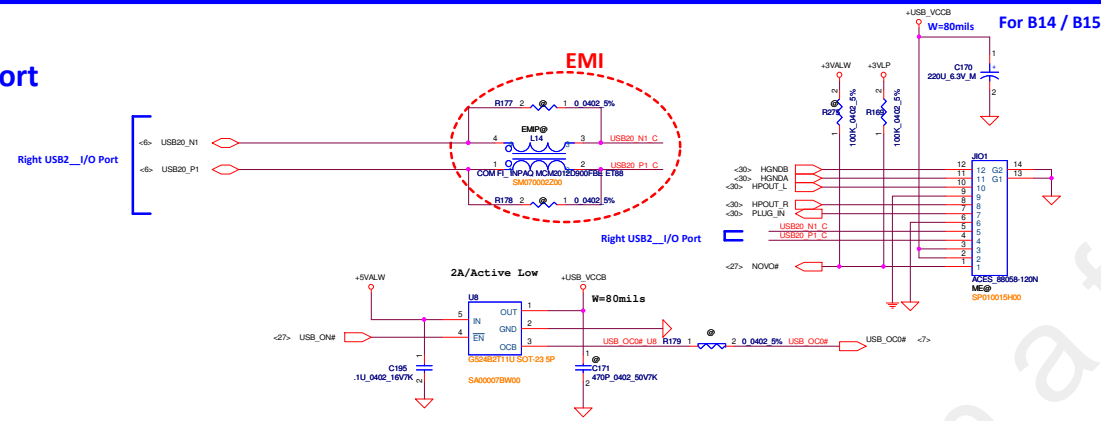
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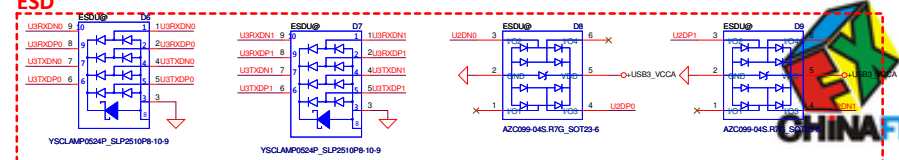
Finger Print



USB2.0_Port

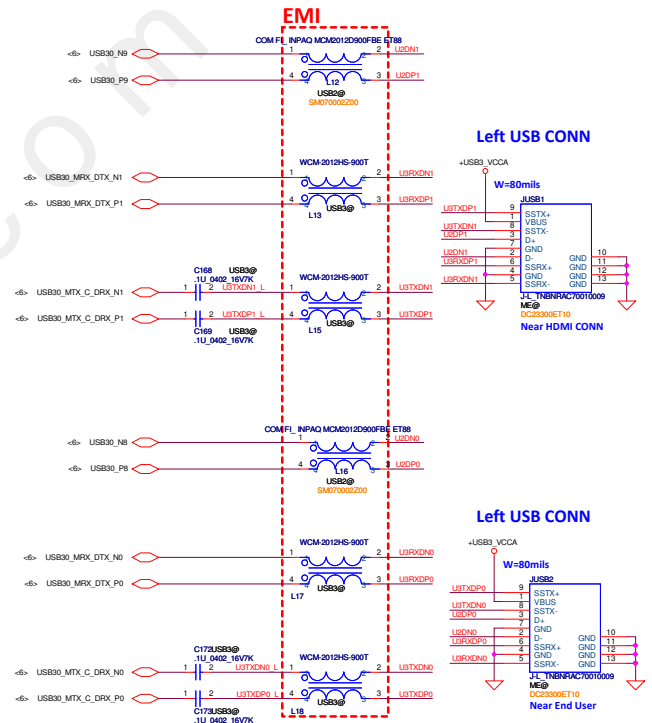


ESD

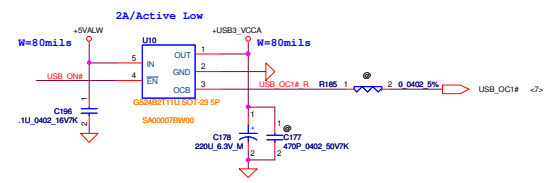


USB3.0_Port

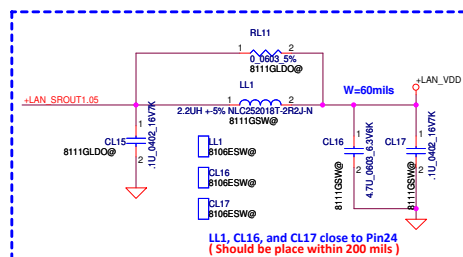
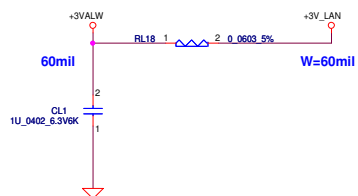
ESD protection needs to be placed near connector side



Place TX AC coupling Cap (C843~C850), Close to connector

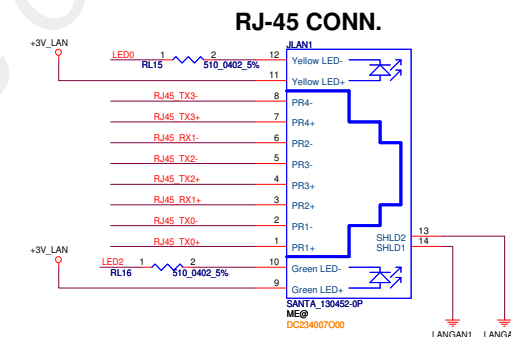
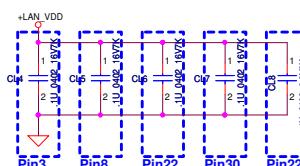
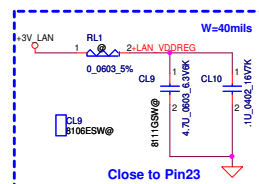
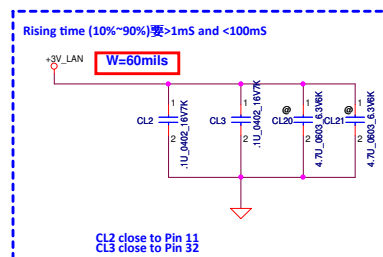


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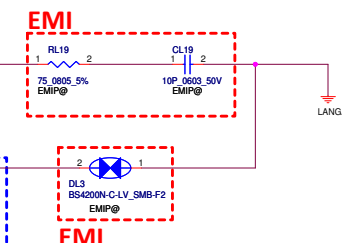
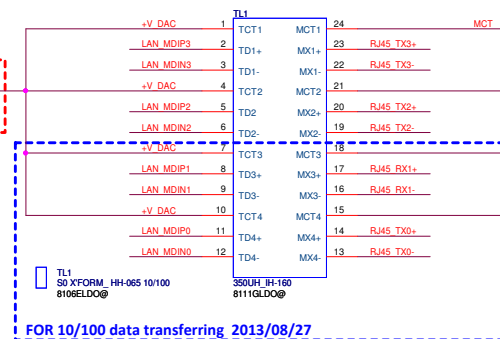
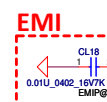
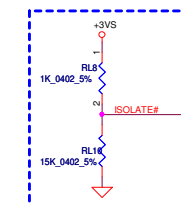
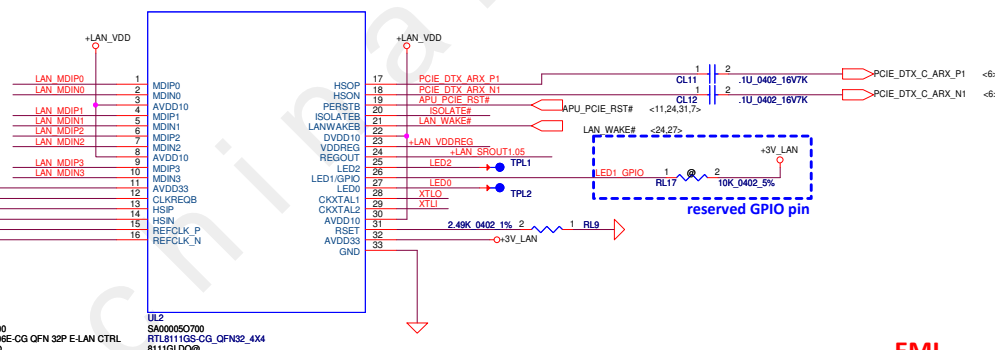
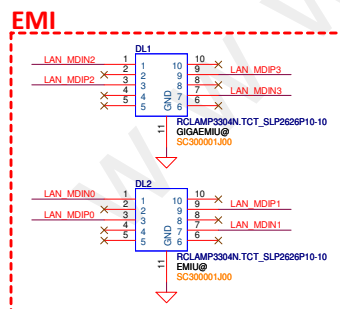
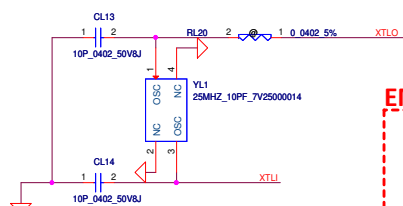


		1.0 V source	LL1	CL16, CL17	CL9, CL10	RL11	CL12
SA00005V700	RTL8111G	LDO	X	X	X	O	C
	RTL8111G	External	X	X	X	X	C
	RTL8111GS/ RTL8111GUS/ RTL8106EUS	SWR	O	O	O	X	X
SA000065V00	RTL8106E	LDO	X	X	X	X	X

Please refer to the table above when using different 1.0V supply source.
For RTL8111GS, RTL8111GUS, RTL8106E and RTL8106EUS, External 1.0V Supply Is Not Permitted

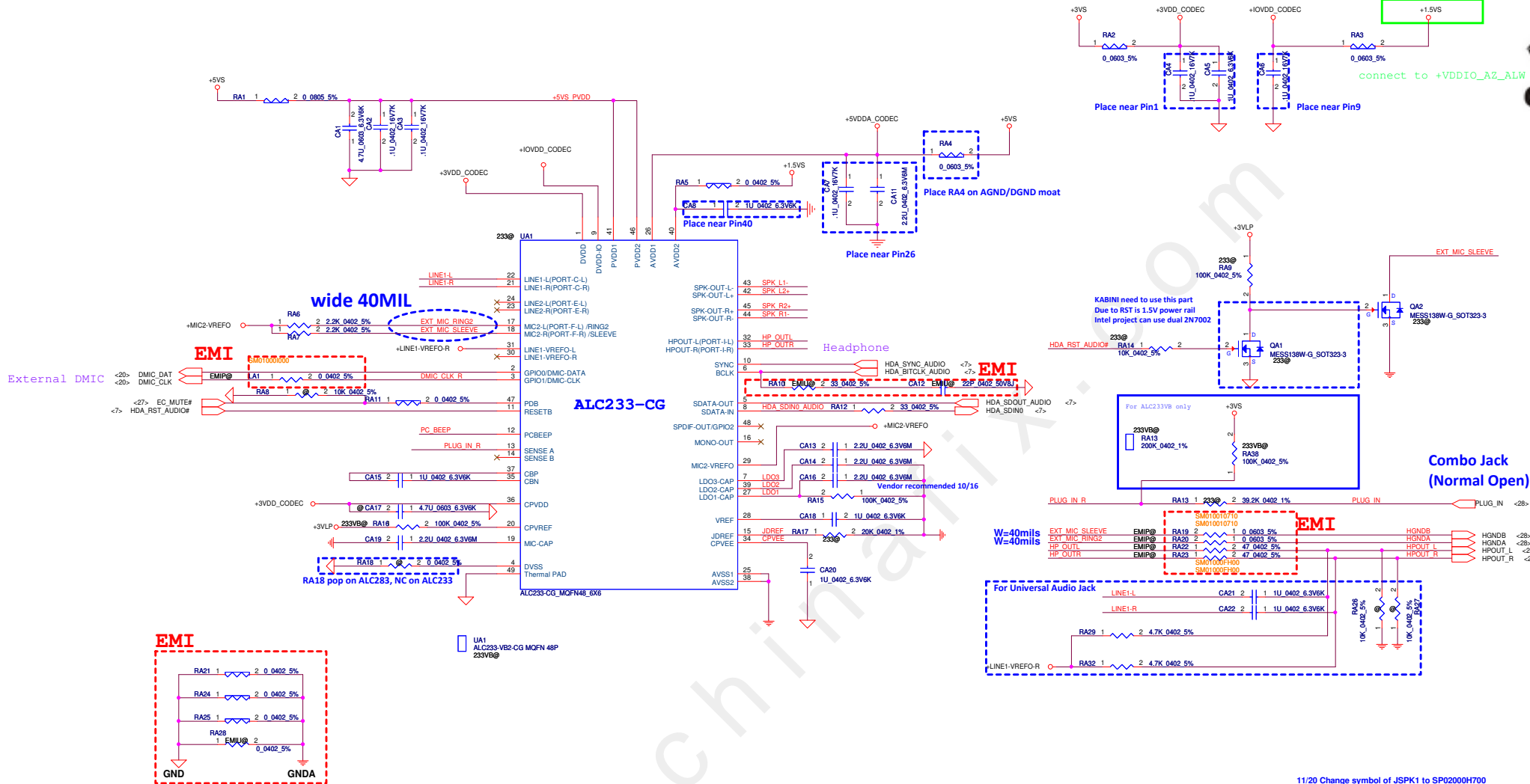


The diagram illustrates a power distribution system with two main feeders, RL4 and RL5, and two additional feeders, EMU@RL6 and EMU@RL7. Each feeder consists of two parallel conductors. The conductors for RL4 and RL5 are labeled with '1' and '2' at the input end, and '0 0 0402 5%' at the output end. The conductors for EMU@RL6 and EMU@RL7 are also labeled with '1' and '2' at the input end, and '0 0 0402 5%' at the output end. All feeders are connected to a common ground labeled 'LANGAN'.

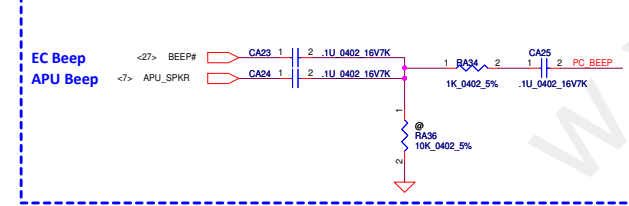


FOR 10/100 data transferring 2013/08/27

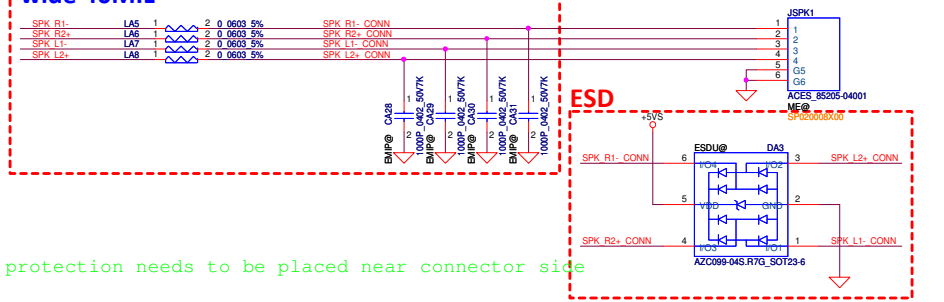
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title	LAN RTL8111G/RTL8106E
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PC BEEP

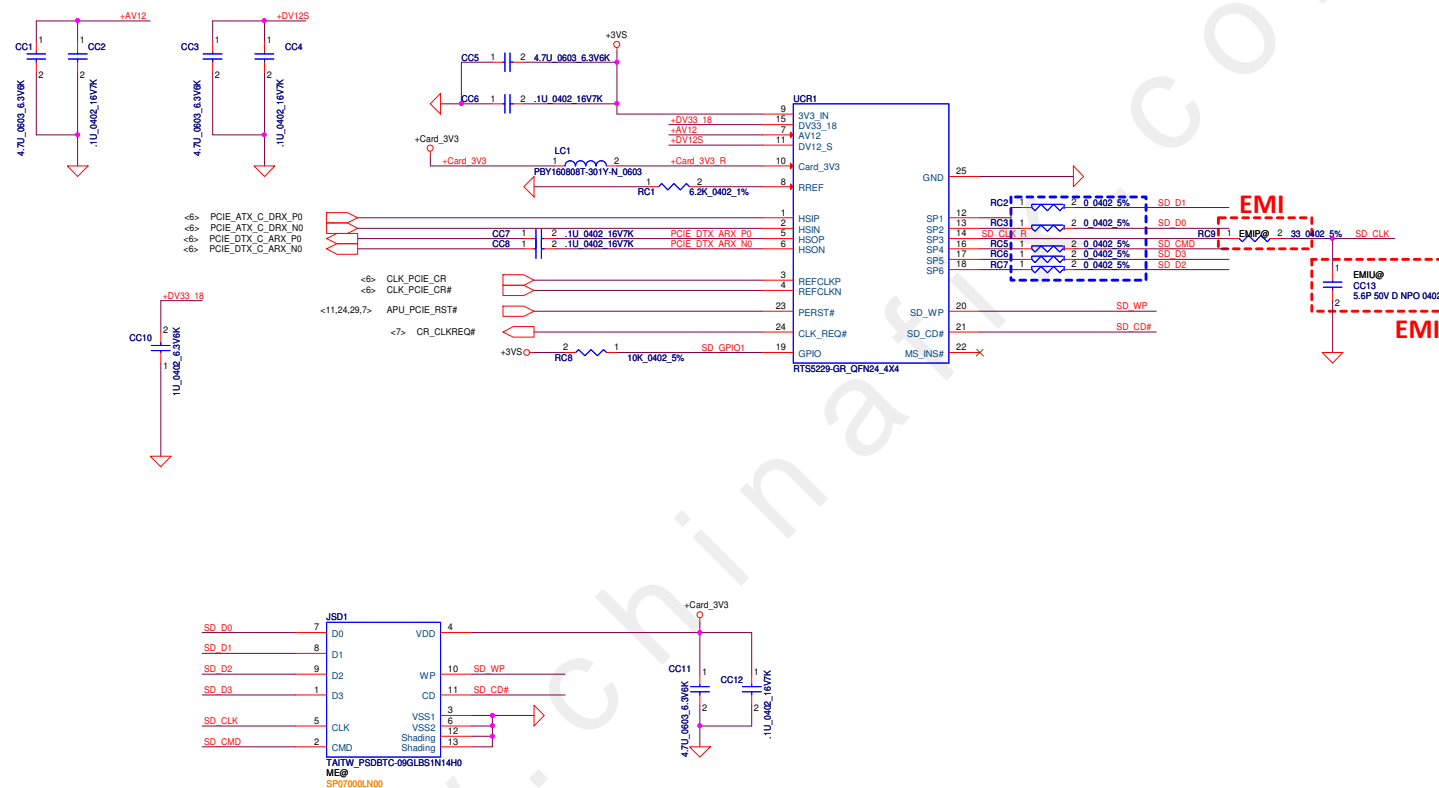


EMI wide 40MIL

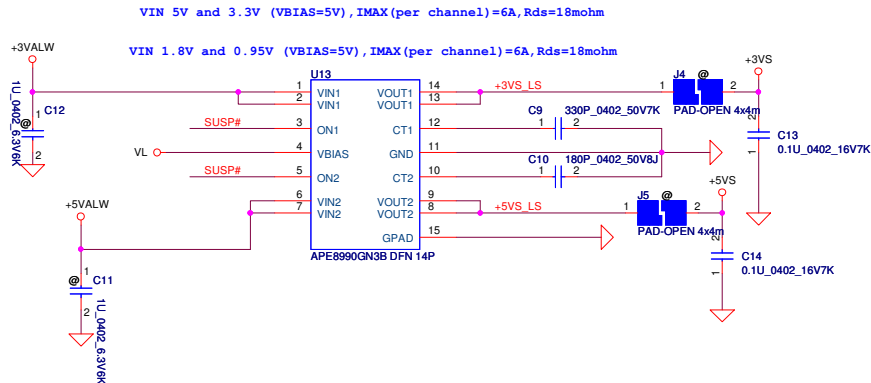


ESD protection needs to be placed near connector side

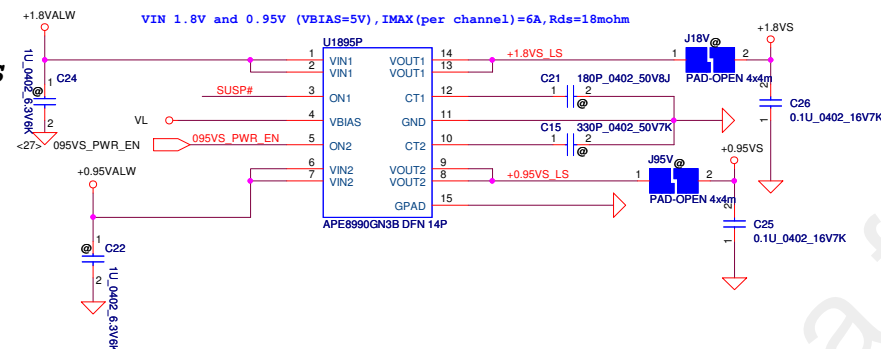
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2014/03/03		2015/03/03		HD Audio Codec ALC233	
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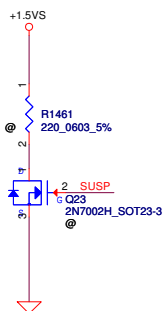
+5VALW TO +5VS
+3VALW TO +3VS
Load switch



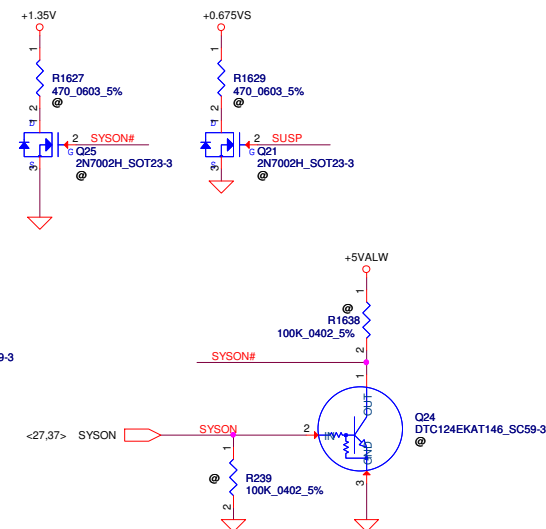
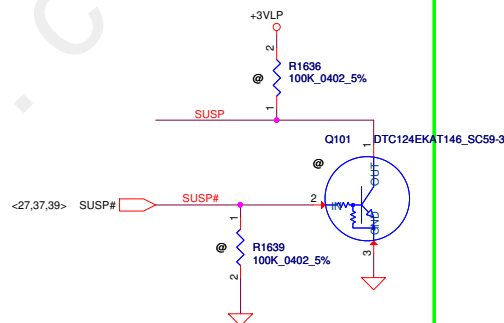
+1.8VALW TO +1.8VS
+0.95VALW TO +0.95VS
Load switch



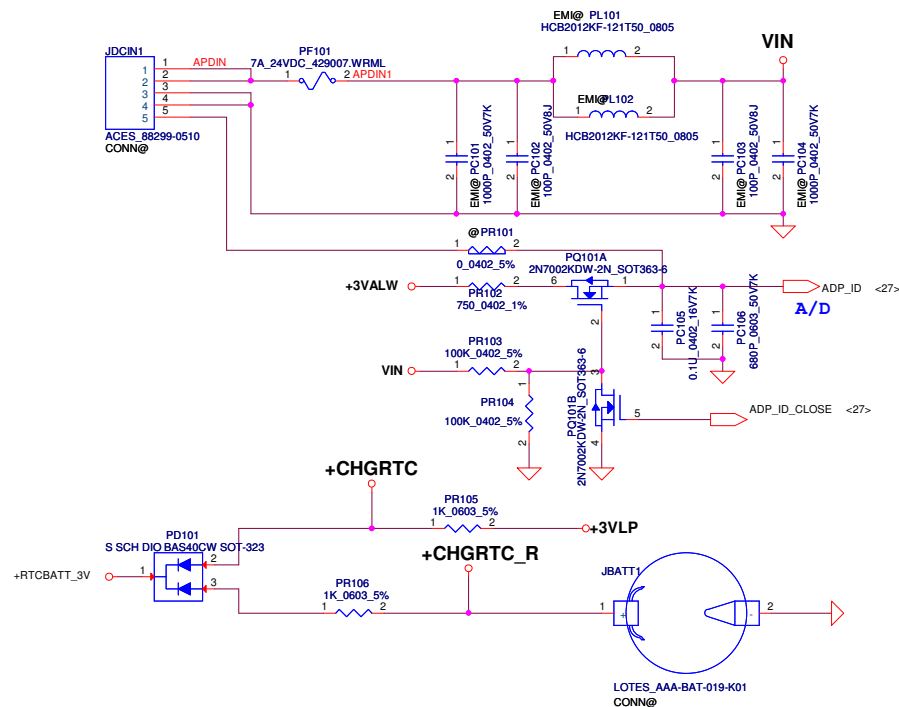
+1.5VS discharge circuit only for Beema
only 1.5VS from PWR



only for Beema



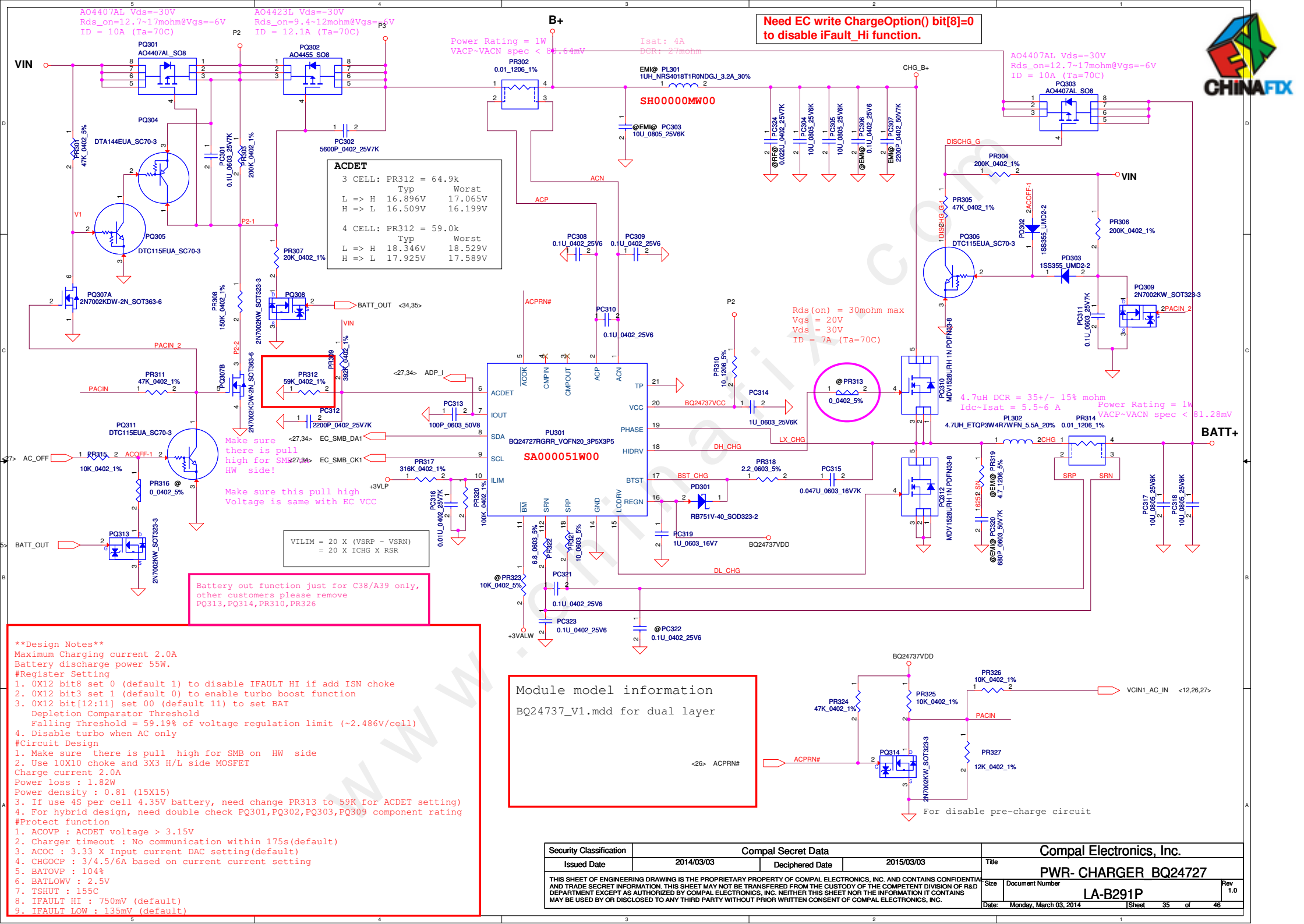
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title	DC Interface
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ADP_ID		
AC Adapter	90W	65W
R(K ohm)	open	10
ADP_ID(V)	3.3	1.65
Detection voltage	>2.64	1.32~1.98

RTC Battery

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Date: Monday, March 03, 2014				Sheet	33 of 46



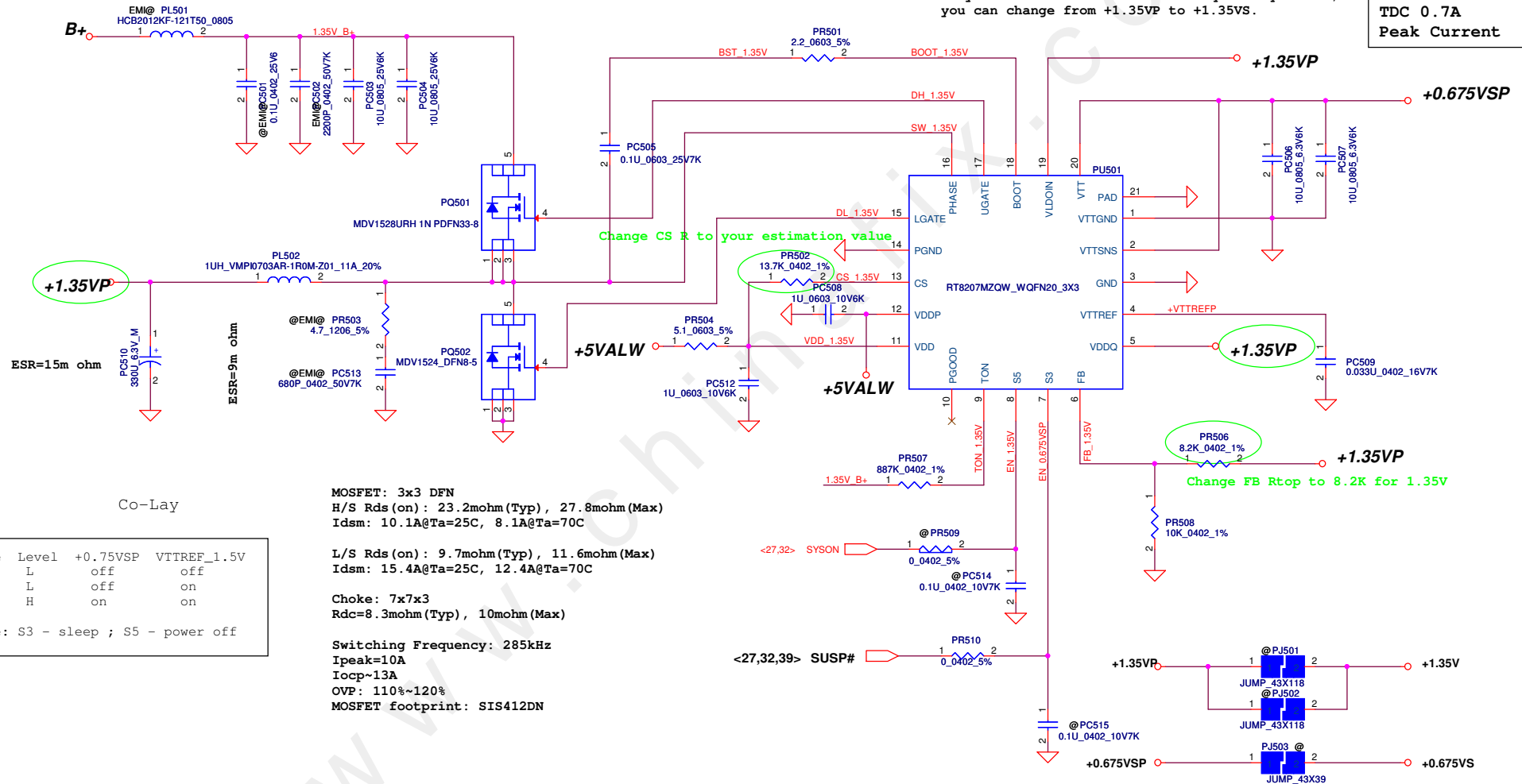


Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

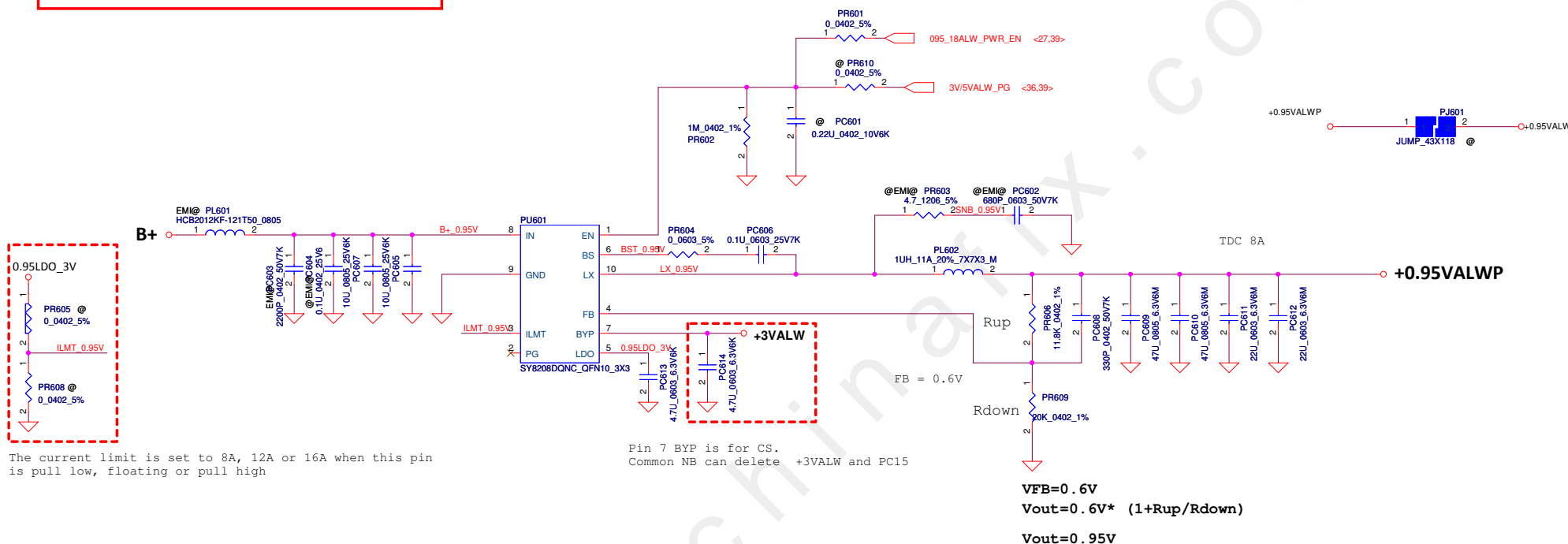


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Module model information

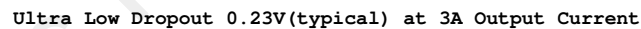
SY8208D_V2.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

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$$V_{out} = 0.8V * (1 + R_{up}/R_{down})$$

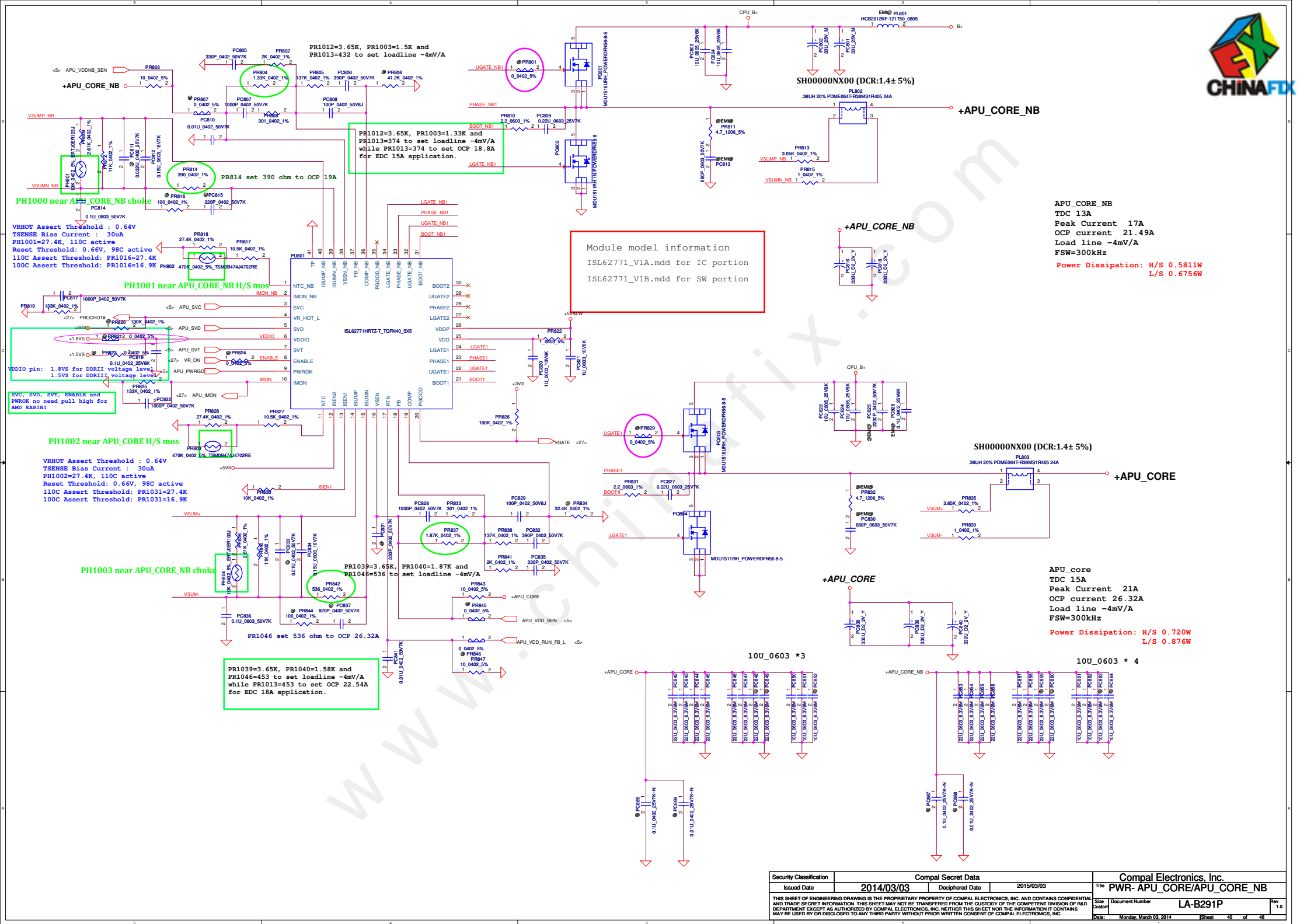
APL5930_V2.mdd

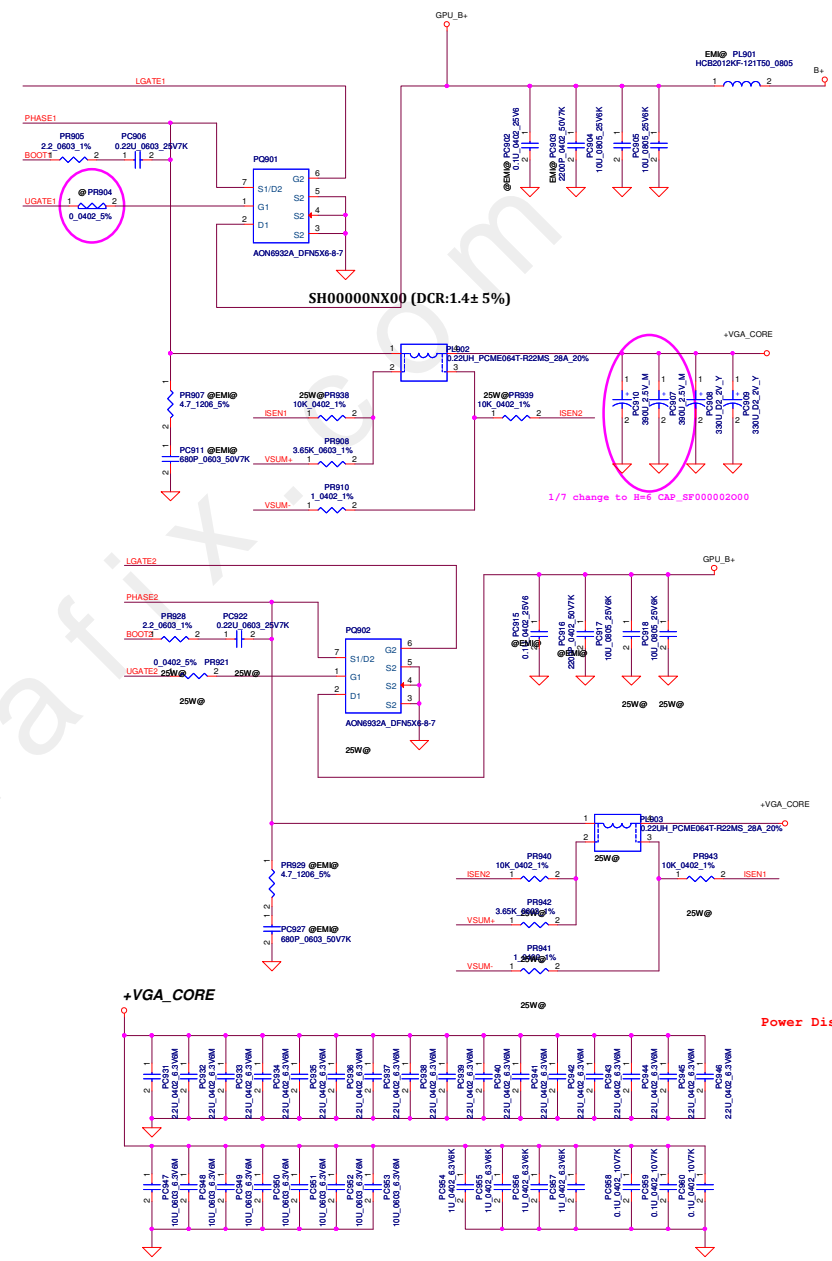
Compal Electronics, Inc.
PWR- +1.8VALW/ +1.5VS

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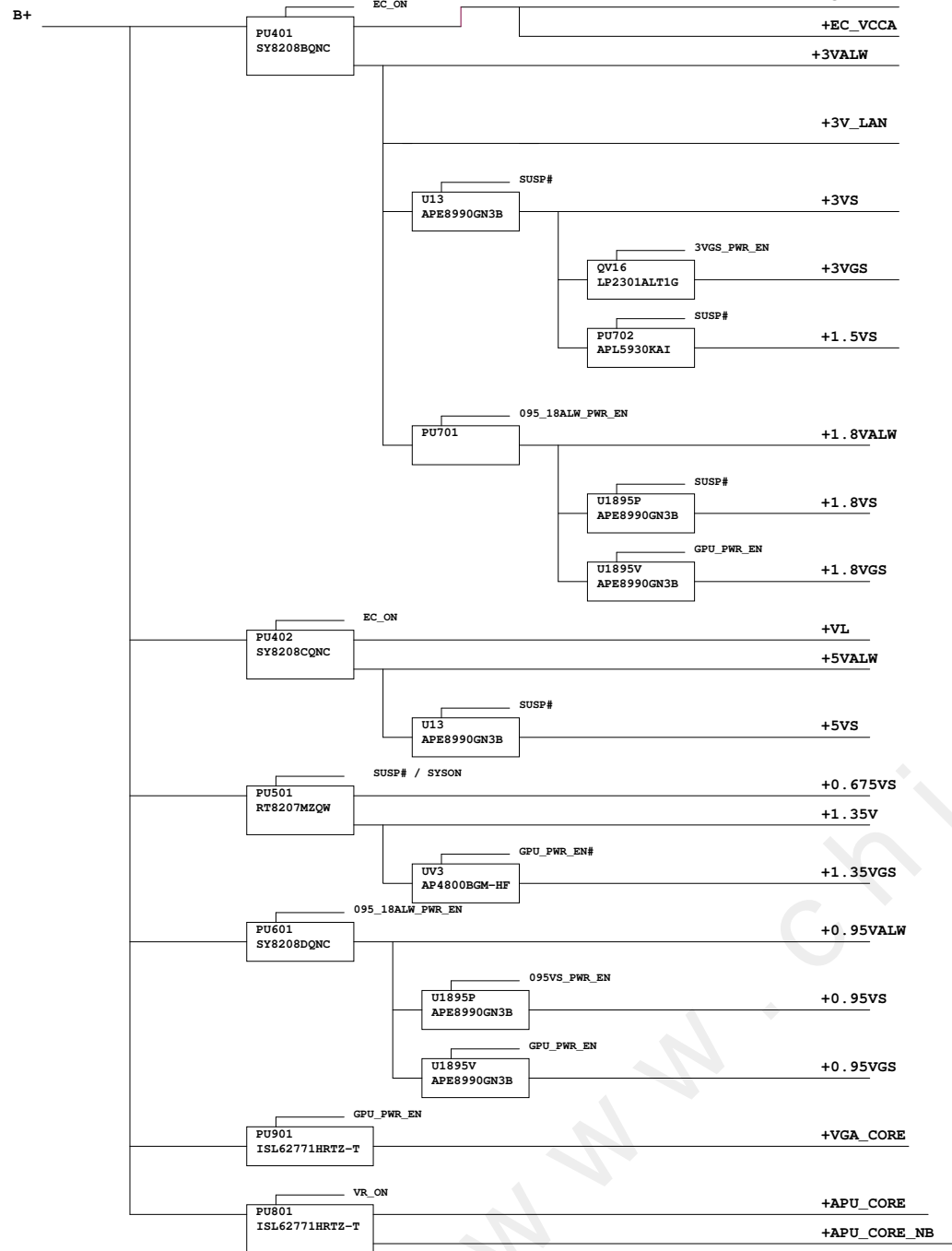
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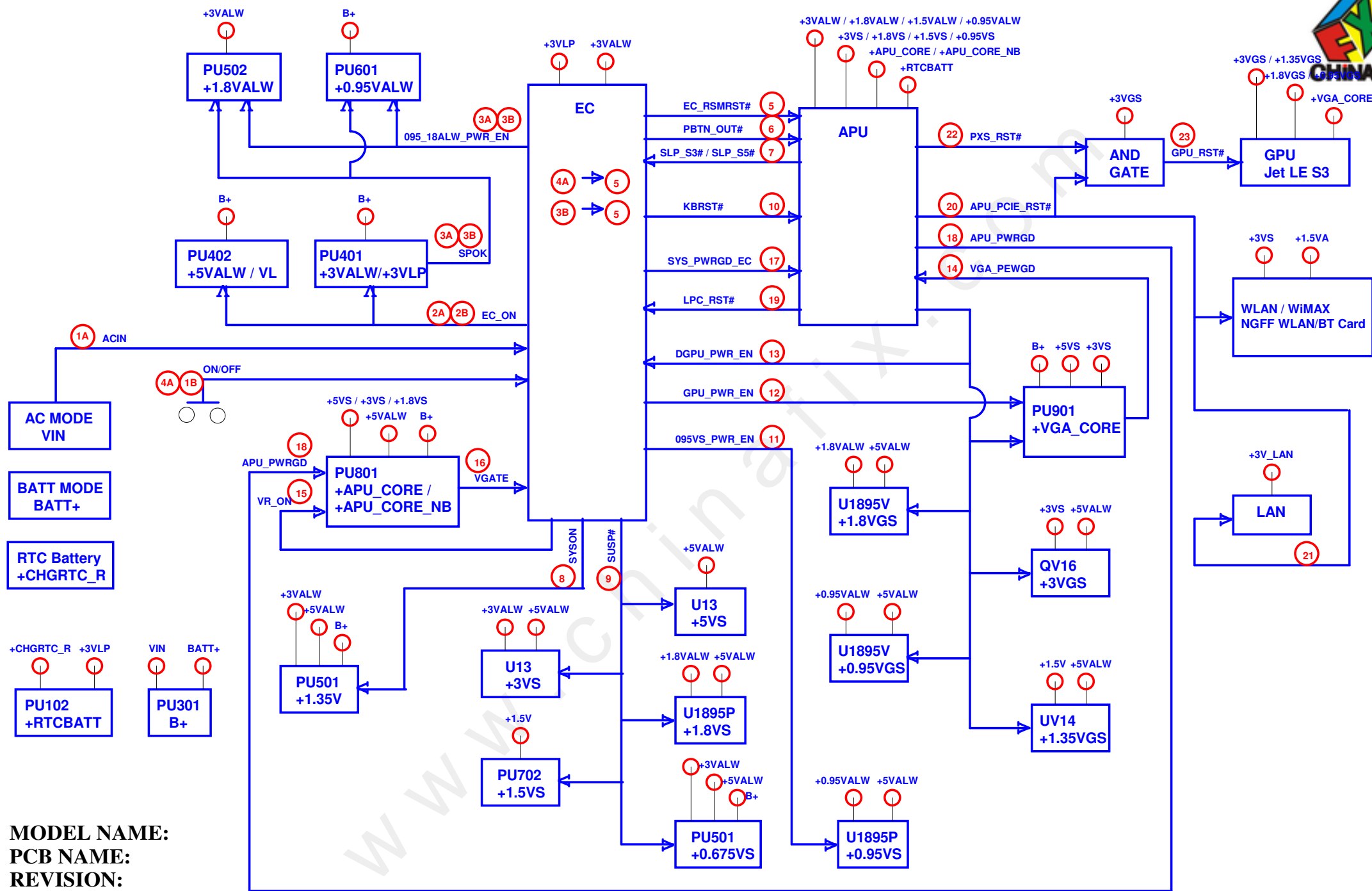




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MODEL NAME:
PCB NAME:
REVISION:
DATE: 2014/03/03

COMPAL CONFIDENTIAL

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Issued Date	2014/03/03	Deciphered Date	2015/03/03	Power Sequence Block	
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				Date:	Monday, March 03, 2014
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