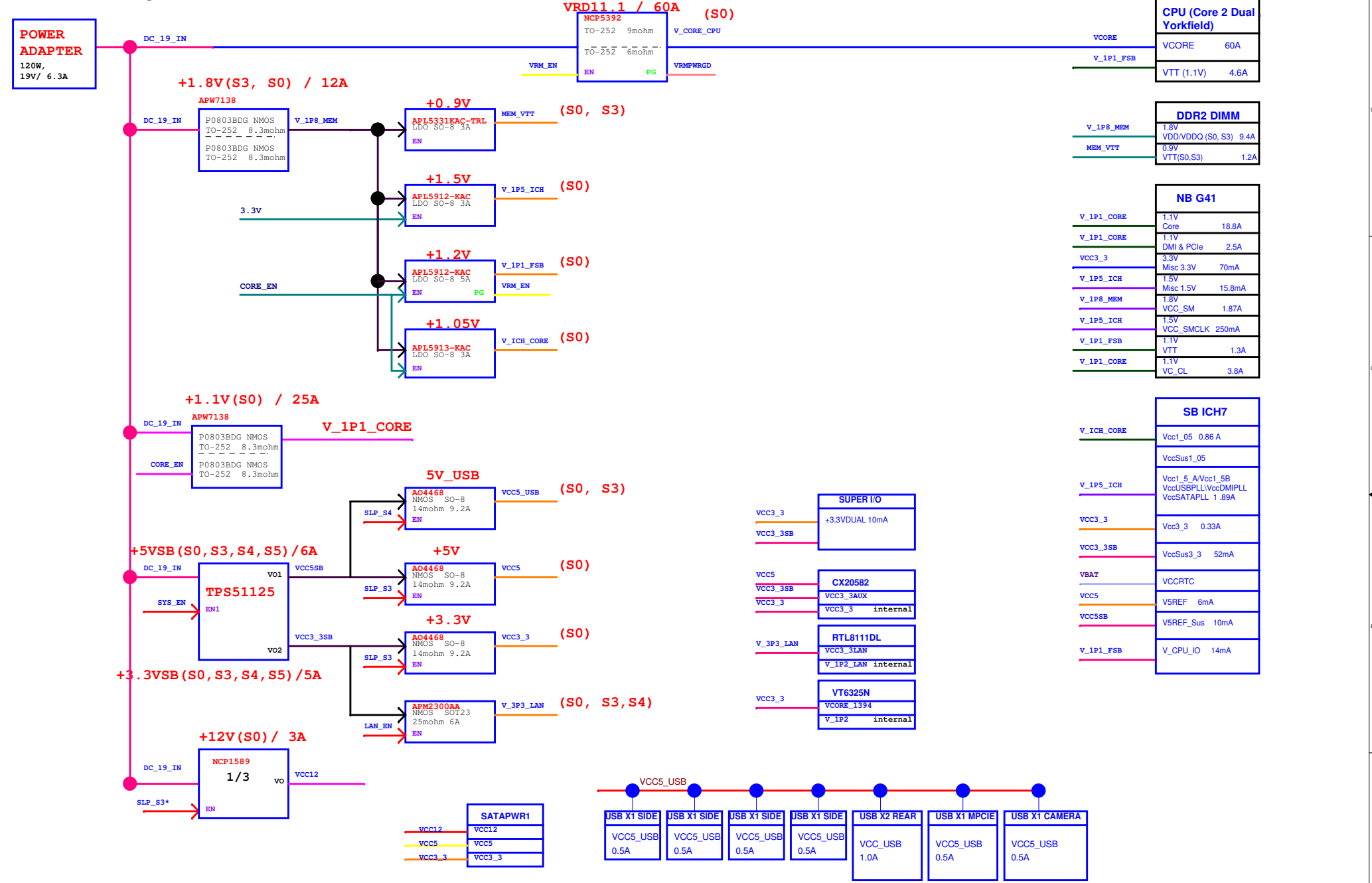
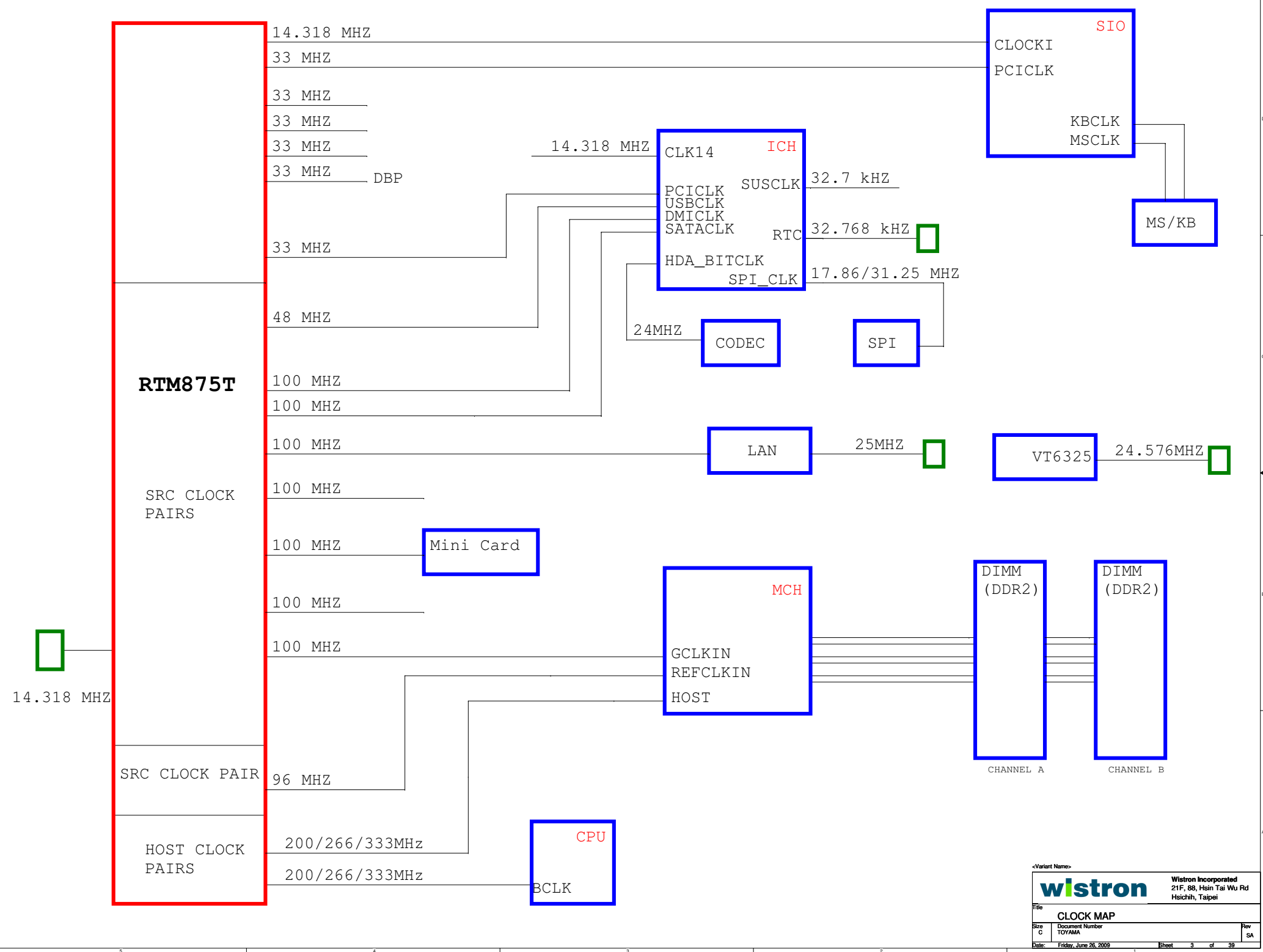


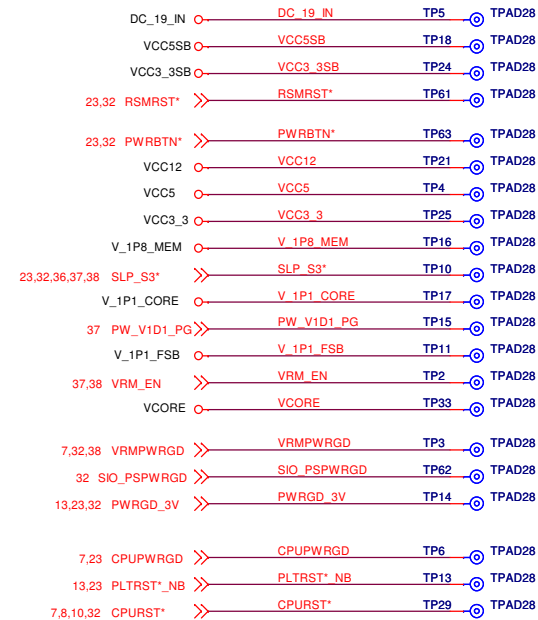
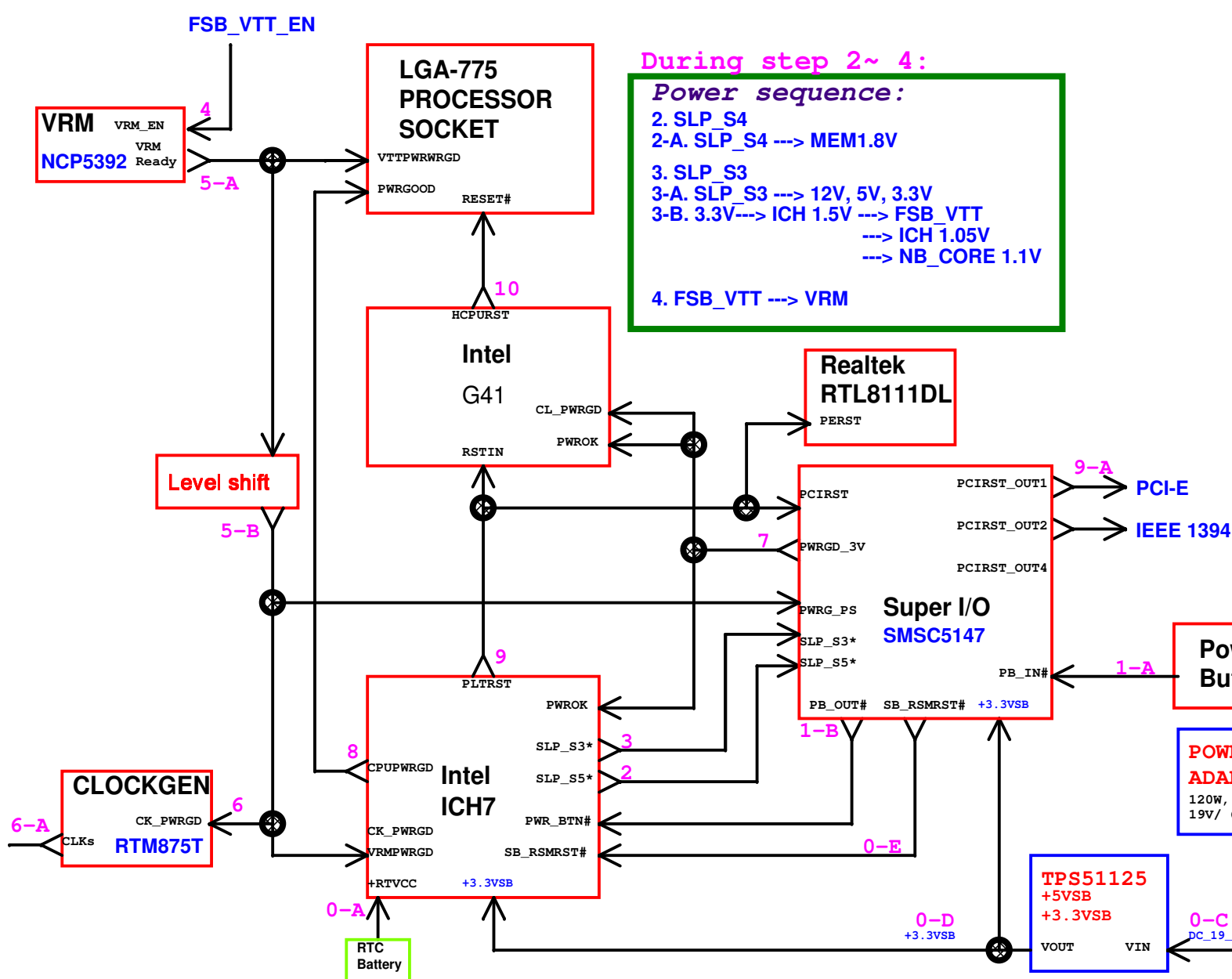
SHEET	
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Sheet 3	CLOCK MAP
Sheet 4	SEQUENCE MAP
Sheet 5	GPIO/HOLE/EMI CAP
Sheet 6	CLOCK GEN RTM875T
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Sheet 8	LGA-775 - Host Bus
Sheet 9	LGA-775 - VCORE & GND
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Sheet 11	EAGLELAKE-G DMI & PCI-E 16X
Sheet 12	EAGLELAKE-G DDR Channel A&B
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Sheet 14	EAGLELAKE-G POWER & PLL
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Sheet 24	ICH7 POWER & GND
Sheet 25	SATA CONN
Sheet 26	USB CONN
Sheet 27	AUDIO CX20582-10Z
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Sheet 30	Mini PCIE SLOT
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Sheet 36	VCC_12 & VCC5 & VCC3_3
Sheet 37	VCC_1.8_DIMM / VCC_1.1_CORE
Sheet 38	VRD 11.1
Sheet 39	TEST COUPON

BOM Cofiguration
(R) : Unmount
(E) : EUP circuit
(F) : card reader and 1394
(X) : remove after MP
(N) : For without 1394 and carder sku

Westlake Power Map







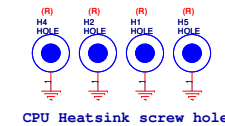
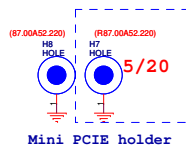
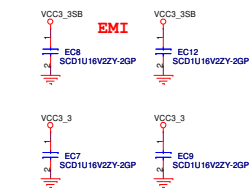
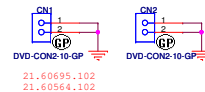
ICH 7

SCH 5147

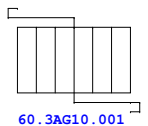
PIN NAME	PIN#	POWER WELL	USAGE	Default Type	DURING RESET	Default Setting	NOTES
GPIO0	AB18	MAIN	ICH_BM_BUSY	GPI	*****	*****	
GPIO1	C8	MAIN	P_REQ_N5	GPI	*****	*****	
GPIO2	G8	MAIN	PIRQJE	GPI	*****	*****	
GPIO3	F7	MAIN	PIRQJF	GPI	*****	*****	
GPIO4	F8	MAIN	PIRQJG	GPI	*****	*****	
GPIO5	G7	MAIN	PIRQJH	GPI	*****	*****	
GPIO6	AC21	MAIN	W_DETECT_N	GPI	*****	*****	For wireless LAN card detected (L: existed)
GPIO7	AC18	MAIN	CB_DET_N	GPI	*****	*****	For PWR BT&LED cable detected (L: existed)
GPIO8	E21	RESUME	non-use	GPI	*****	*****	
GPIO9	E20	RESUME	PANEL_DET	GPI	*****	*****	For ICH7 inform scalar chip function
GPIO10	A20	RESUME	IO_SMI*	GPI	*****	*****	For SIO_SMI* function(low Active)
GPIO11	B23	RESUME	LPC_PME*	Native	*****	*****	For SIO LPC_PME* function(low Active)
GPIO12	F19	RESUME	non-use	GPI	*****	*****	
GPIO13	E19	RESUME	GSNDSOR_INT	GPI	*****	*****	For G Sensor
GPIO14	R4	RESUME	AUD_EXPMUTE*	GPI	*****	*****	For AUDIO output Mute function (default : High)
GPIO15	E22	RESUME	non-use	GPI	*****	*****	
GPIO16	AC22	MAIN	AUD_SPKMUTE*	GPO	*****	High	I/P/D 20K/For Speaker Mute function (default : High)
GPIO17	D8	MAIN	P_GNT_N5	GPO	*****	*****	INTEGRATED P/U 20K
GPIO18	A20	MAIN	W_DISABLE*	GPO	*****	High	For wireless LAN disable(default : High enable)
GPIO19	AH18	MAIN	INV_DET*	GPI	*****	*****	For Inverter cable detected (L: existed)
GPIO20	AF21	MAIN	non-use	GPO	*****	*****	
GPIO21	AF19	MAIN	LVDS_DET*	GPI	*****	*****	For LVDS cable detected (L: existed)
GPIO22	A13	MAIN	P_REQ_N4	Native	*****	*****	
GPIO23	AA5	MAIN	non-use	Native	*****	*****	Multiplexed with LDRQ1#
GPIO24	R3	RESUME	LAN_EN	GPO	*****	Out Low	For LAN power enable (Default :Low enable)
GPIO25	D20	RESUME	DMI_MODE	GPO	*****	Low	DMI use AC mode
GPIO26	A21	RESUME	non-use	GPO	*****	*****	
GPIO27	B21	RESUME	SUSLED*	GPO	*****	Out	For Suspend LED function
GPIO28	E23	RESUME	PWRLED*	GPO	*****	Out	For PWR LED function
GPIO29	C3	RESUME	OC*5	Native	*****	*****	
GPIO30	A2	RESUME	OC*67	Native	*****	*****	
GPIO31	B3	RESUME	OC*67	Native	*****	*****	
GPIO32	AG18	MAIN	non-use	GPO	*****	*****	
GPIO33	AC19	MAIN	non-use	GPO	*****	*****	
GPIO34	U2	MAIN	non-use	GPO	*****	High	
GPIO35	AD21	MAIN	CAMERA_EN	GPO	*****	High	For Webcam enable function (default : High enable)
GPIO36	AH19	MAIN	BOARD_ID_1	GPI	*****	*****	Multiplexed with SATA2GP
GPIO37	AE19	MAIN	BOARD_ID_2	GPI	*****	*****	Multiplexed with SATA3GP
GPIO38	AD20	MAIN	RISER1_DET	GPI	*****	*****	For Rear IO cable1 detected (L: existed)
GPIO39	AE20	MAIN	RISER2_DET	GPI	*****	*****	For Rear IO cable2 detected (L: existed)
GPIO48	A14	MAIN	P_GNT_N4	Native	*****	*****	
GPIO49	AG24	CPU	CPU_PWRGD	Native	*****	*****	

GPIO #	Usage	BIOS Post Value	I/O	IN-POWER	OUT-POWER
GP10	PLTRST*_I394	Native(nPCIRST_OUT3)	O	N/A	AUX (VTR)
GP11	PLTRST*_RISER	Native(nPCIRST_OUT1)	O	N/A	AUX (VTR)
GP12	PLTRST*_LAN	Native(nPCIRST_OUT2)	O	N/A	AUX (VTR)
GP14	PLTRST*_DBP	Native(nPCIRST_OUT4)	O	N/A	AUX (VTR)
GP15	non-use	non-use		N/A	MAIN (VCC)
GP16	PROCHOT*_L	PROCHOT* (Processor Hot Function) Default High, Over 85 degree, Enable PROCHOT Function	OD	N/A	AUX (VTR)
GP17	SYS_FAN2_CTRL_SIO	PM3	3/11	O	N/A
GP20	ICH_BM_BUSY	Native(PECI Request)	I	AUX (VTR)	MAIN (VCC)
GP21	KBDATA	Native(KBDATA)	O	AUX (VTR)	MAIN (VCC)
GP22	KBCLK	Native(KBCLK)	O	AUX (VTR)	MAIN (VCC)
GP27	IO_SMI*	Native (IO_SMI*)	O	AUX (VTR)	AUX (VTR)
GP32	MSDATA	Native(MSDATA)	O	AUX (VTR)	MAIN (VCC)
GP33	MSCLK	Native(MSCLK)	O	AUX (VTR)	MAIN (VCC)
GP36	KBRST*	Native(KBRST*)	O	AUX (VTR)	MAIN (VCC)
GP37	A20GATE	Native(A20GATE)	O	AUX (VTR)	MAIN (VCC)
GP40	TP_Det	TP_Det	6/22	AUX (VTR)	AUX (VTR)
GP41	non-use	non-use	I	AUX (VTR)	AUX (VTR)
GP42	LPC_PME*	Native(nIO_PME)	O	AUX (VTR)	AUX (VTR)
GP43	AUTO_COLOR_SIO	AUTO_COLOR_SIO(Default: High)	O	AUX (VTR)	MAIN (VCC)
GP50	Panel_FB	Panel_FB	I	AUX (VTR)	AUX (VTR)
GP51	SMBUS_ISP	H:ISP ,L:disable(default)	OD	AUX (VTR)	AUX (VTR)
GP52	CPU_GTLREF_CTRL_1	GPO (Default: Low)	O	AUX (VTR)	AUX (VTR)
GP53	CPU_GTLREF_CTRL_2	GPO (Default: High)	O	AUX (VTR)	AUX (VTR)
GP54	PRT_ISP	L:ISP ,H:disable(default)	OD	AUX (VTR)	AUX (VTR)
GP55	PANEL_SEL1	PANEL type select	OD	AUX (VTR)	AUX (VTR)
GP56	PANEL_SEL2	PANEL type select	OD	AUX (VTR)	AUX (VTR)
GP57	PANEL_SEL3	PANEL type select	OD	AUX (VTR)	AUX (VTR)
GP60	PECI_READY1	Native(PECI Ready)	I	AUX (VTR)	AUX (VTR)
GP61	PECT_SIO_R	Native(PECI IO)	I	AUX (VTR)	AUX (VTR)

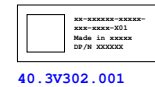
SMBUS MAP



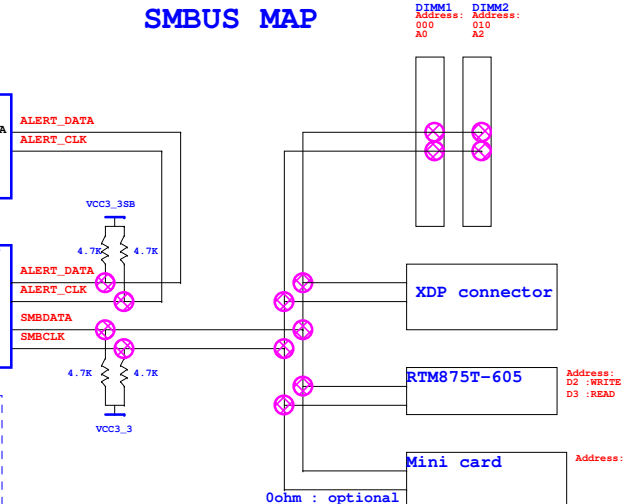
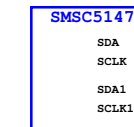
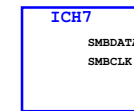
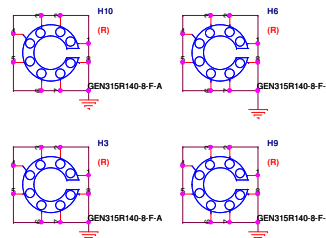
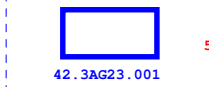
NB heatsink



2D label

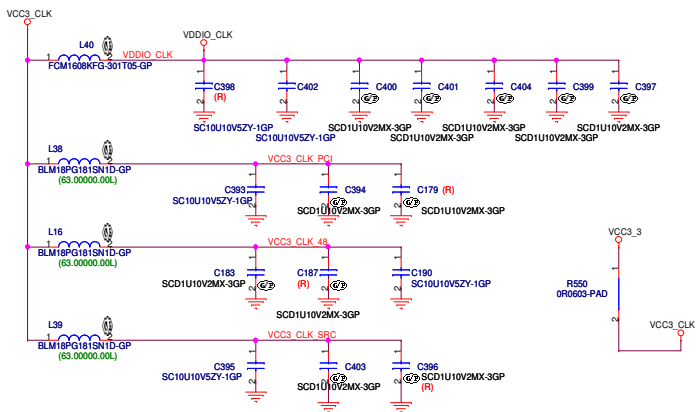


HLDR-SUPPORT * 4

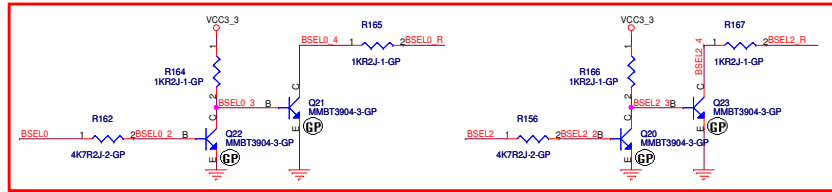


<Variant Name>

Decoupling for Clock Driver



	Trace Width	DIFF Space	Other DIFF/Trace Space	DIFF Impedance	DIFF Matched	NOTE
HOST CLK	4 mils	10 mils	18 mils	95 ohm	10 mils	NB-CPU= 1700 mils
PCI CLK	4 mils	10 mils	X	50 ohm ± 15%	X	
REF CLK	4 mils	10 mils	X	50 ohm ± 15%	X	
USB CLK	4 mils	10 mils	X	50 ohm ± 15%	X	
DREF CLK	4 mils	10 mils	18 mils	95 ohm	10 mils	
SRC CLK	4 mils	10 mils	18 mils	95 ohm	25 mils	

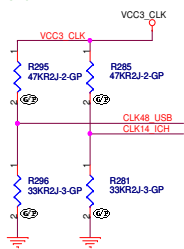


CPU	BSEL0 FSA	BSEL1 FSB	BSEL2 FSC
133	1	0	0
200	0	1	0
266	0	0	0
333	0	0	1

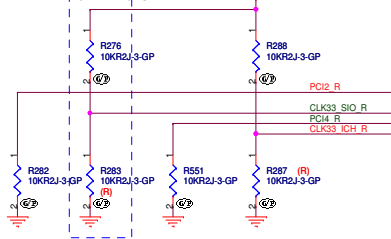
RTM875T Multi-function Pin at pin 4, 5, 6, 7

PIN	STRAP	STRAPPING MODE	NET NAME
4	TME	"HIGH" = Overclocking Enable "LOW" = Overclocking NOT Allowed	PCI2_R
5	SRC5_EN	"HIGH" = PIN29/30 is SRC-5, 100MHz diff. "LOW" = PIN29/30 is PCI_STOP/..	CLK333_SIO_R
7	ITP_EN	"HIGH" = PIN38/39 is CPUITP "LOW" = PIN38/39 is SRC8	CLK333_ICH_R
6	27M_SEL	"HIGH" = PIN17/18 of RTM875T is 27MHz/27MHz_SS PIN13/14 of RTM875T is SRC-0 diff. "LOW" = PIN17/18 of RTM875T is SRC-1 diff. PIN13/14 of RTM875T is DOT96 diff.	PCI4_R

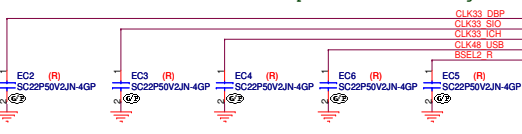
Design Note: BSEL BIASING RES. ALWAYS STUFF



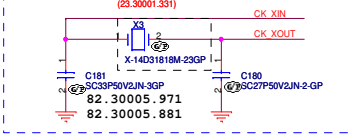
For RTM875T

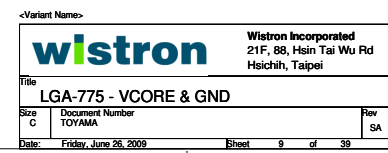


CLOCK EMI CAPS. DEFAULT EMPTY place close to clock gen.



Crystal

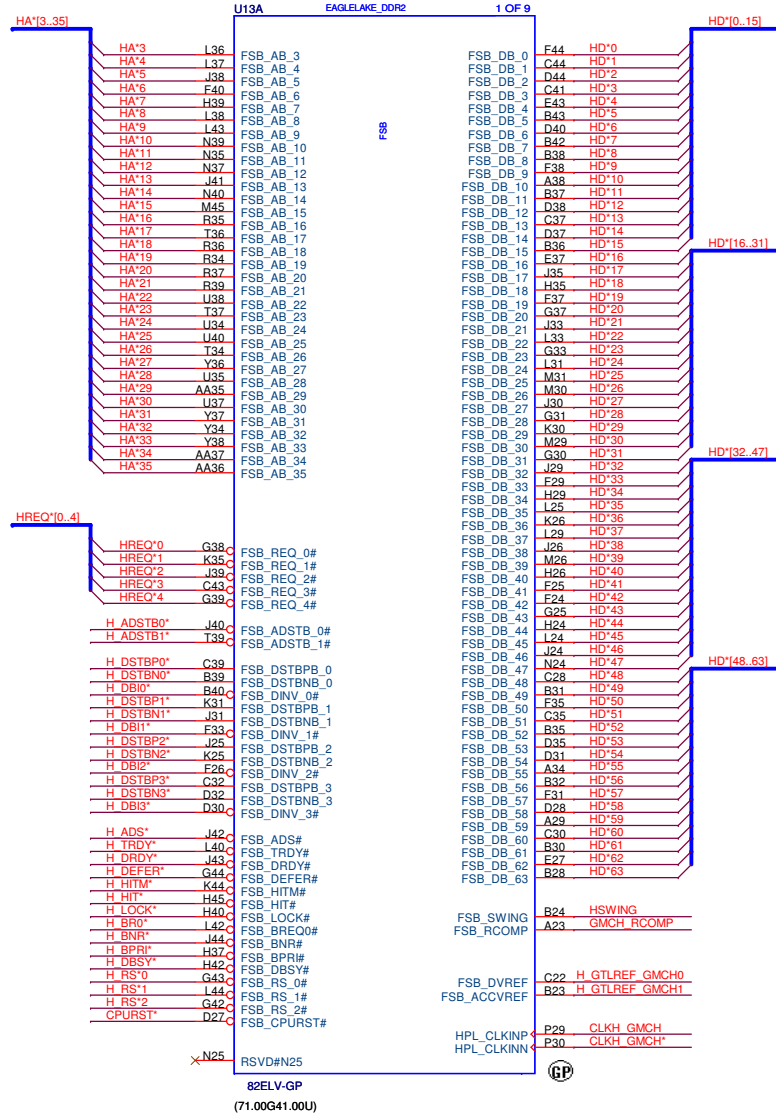




Host Interface

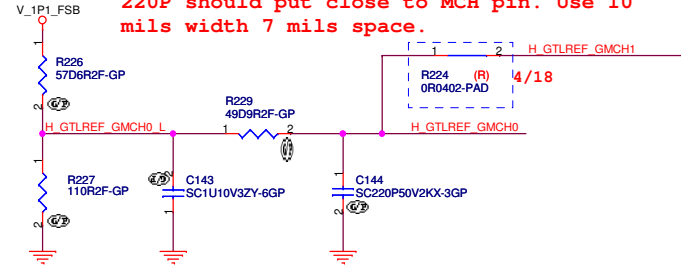
8	HA*[3..35]	HA*[3..35]
8	HREQ*[0..4]	HREQ*[0..4]
8	H_ADSTB0*	H_ADSTB0*
8	H_ADSTB1*	H_ADSTB1*
8	H_DSTBP0*	H_DSTBP0*
8	H_DSTBN0*	H_DSTBN0*
8	H_DBI0*	H_DBI0*
8	H_DSTBP1*	H_DSTBP1*
8	H_DSTBN1*	H_DSTBN1*
8	H_DBI1*	H_DBI1*
8	H_DSTBP2*	H_DSTBP2*
8	H_DSTBN2*	H_DSTBN2*
8	H_DBI2*	H_DBI2*
8	H_DSTBP3*	H_DSTBP3*
8	H_DSTBN3*	H_DSTBN3*
8	H_DBI3*	H_DBI3*
8	H_ADS*	H_ADS*
8	H_TRDY*	H_TRDY*
8	H_DRDY*	H_DRDY*
8	H_DEFER*	H_DEFER*
8	H_HITM*	H_HITM*
8	H_HIT*	H_HIT*
8	H_LOCK*	H_LOCK*
8	H_BR0*	H_BR0*
8	H_BNR*	H_BNR*
8	H_BPRI*	H_BPRI*
8	H_DBSY*	H_DBSY*
8	H_RS'0	H_RS'1
8	H_RS'1	H_RS'2
8	H_RS'2	CPURST*
4,7,8,32	CPURST*	

8	HD*[0..15]	HD*[0..15]
8	HD*[16..31]	HD*[16..31]
8	HD*[32..47]	HD*[32..47]
8	HD*[48..63]	HD*[48..63]
6	CLKH_GMCH	CLKH_GMCH
6	CLKH_GMCH*	CLKH_GMCH*

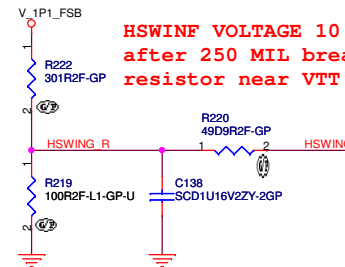


MCH_GTLREF VOLTAGE SHOULD BE
 $0.635 * V_{TT} = 0.7V$

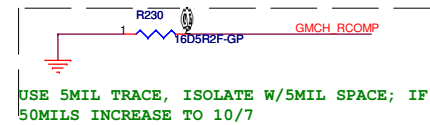
220P should put close to MCH pin. Use 10
 mils width 7 mils space.



HSWING VOLTAGE 10 mils width 10 mils space
 after 250 MIL breakout. Place divider
 resistor near VTT.



CHECK



USE 5MIL TRACE, ISOLATE W/5MIL SPACE; IF
 50MILS INCREASE TO 10/7

<Variant Name>

wistron

Wistron Incorporated
 21F, 88, Hsin Tai Wu Rd
 Hsichih, Taipei

Title
Eaglelake-G Host Bus

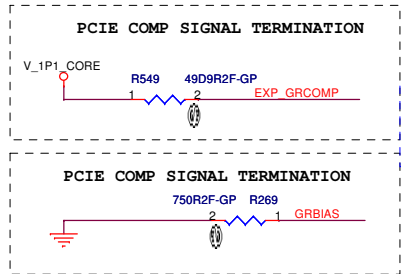
Size
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Rev
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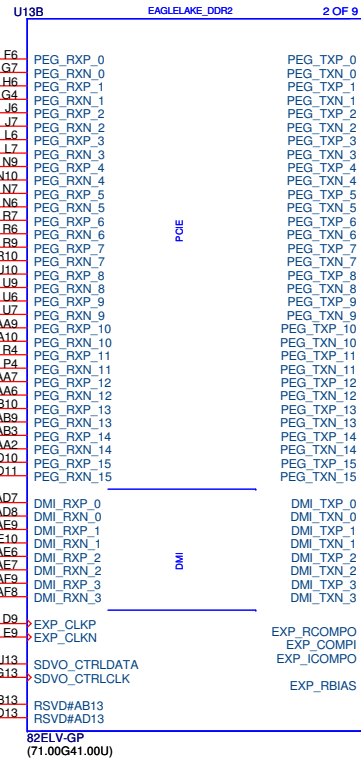
Date: Friday, June 26, 2009

Sheet 10 of 39

22 DMI0_MTXP_IRXP < DMI0_MTXP_IRXP
22 DMI0_MTXN_IRXN < DMI0_MTXN_IRXN
22 DMI1_MTXP_IRXP < DMI1_MTXP_IRXP
22 DMI1_MTXN_IRXN < DMI1_MTXN_IRXN
22 DMI2_MTXP_IRXP < DMI2_MTXP_IRXP
22 DMI2_MTXN_IRXN < DMI2_MTXN_IRXN
22 DMI3_MTXP_IRXP < DMI3_MTXP_IRXP
22 DMI3_MTXN_IRXN < DMI3_MTXN_IRXN
22 DMI0_MRX_P_ITXP < DMI0_MRX_P_ITXP
22 DMI0_MRXN_ITXN < DMI0_MRXN_ITXN
22 DMI1_MRX_P_ITXP < DMI1_MRX_P_ITXP
22 DMI1_MRXN_ITXN < DMI1_MRXN_ITXN
22 DMI2_MRX_P_ITXP < DMI2_MRX_P_ITXP
22 DMI2_MRXN_ITXN < DMI2_MRXN_ITXN
22 DMI3_MRX_P_ITXP < DMI3_MRX_P_ITXP
22 DMI3_MRXN_ITXN < DMI3_MRXN_ITXN
6 CLKSRC_GMCH < CLKSRC_GMCH
6 CLKSRC_GMCH* < CLKSRC_GMCH*



DMI0_MRX_P_ITXP AD7
DMI0_MRXN_ITXN AD8
DMI1_MRX_P_ITXP AE9
DMI1_MRXN_ITXN AE10
DMI2_MRX_P_ITXP AE6
DMI2_MRXN_ITXN AE7
DMI3_MRX_P_ITXP AE9
DMI3_MRXN_ITXN AE8
CLKSRC_GMCH D9
CLKSRC_GMCH* E9
TP44 1 TPAD24 SDVO_DATA J13
TP43 1 TPAD24 SDVO_CLK G13
AB13 RSVD#AB13
AD13 RSVD#AD13
82ELV-GP
(71.00G41.00U)



DMI_TXP_0 AC2
DMI_TXN_0 AD2
DMI_TXP_1 AD4
DMI_TXN_1 AE4
DMI_TXP_2 AE2
DMI_TXN_2 AE2
DMI_TXP_3 AE4
DMI_TXN_3 AG4
DMI0_MTXP_IRXP_C C417
DMI0_MTXN_IRXP_C C416
DMI1_MTXP_IRXP_C C420
DMI1_MTXN_IRXP_C C419
DMI2_MTXP_IRXP_C C415
DMI2_MTXN_IRXP_C C414
DMI3_MTXP_IRXP_C C427
DMI3_MTXN_IRXP_C C426

SCD1U10V2MX-3GP
SCD1U10V2MX-3GP
SCD1U10V2MX-3GP
SCD1U10V2MX-3GP
SCD1U10V2MX-3GP
SCD1U10V2MX-3GP
SCD1U10V2MX-3GP
SCD1U10V2MX-3GP

<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title Eaglelake-G DMI & PCI-E X16			
Size A3	Document Number TOYAMA		Rev SA
Date: Friday, June 26, 2009	Sheet 11		of 39

6 GMCH_BSEL0 >> GMCH_BSEL0
6 GMCH_BSEL1 >> GMCH_BSEL1
6 GMCH_BSEL2 >> GMCH_BSEL2

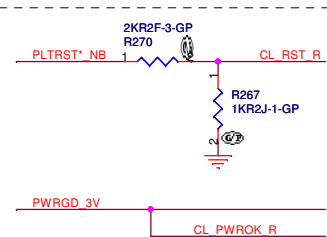
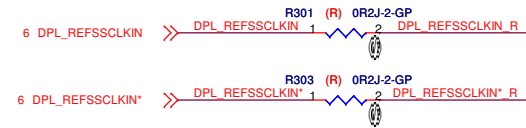
4,23 PLTRST*_NB >> PLTRST*_NB
23 GMCH_ICH_SYNC*_ >> GMCH_ICH_SYNC*
4,23 PLTRST*_NB >> PLTRST*_NB
4,23,32 PWRGD_3V >> PWRGD_3V

6 CLK96_DOT >> CLK96_DOT
6 CLK96_DOT* >> CLK96_DOT*

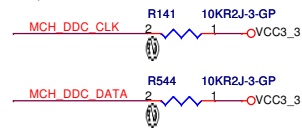
19,20 MCH_VGA_RED >> MCH_VGA_RED
19,20 MCH_VGA_GREEN >> MCH_VGA_GREEN
19,20 MCH_VGA_BLUE >> MCH_VGA_BLUE

19 HSYNC_3P3V >> HSYNC_NB
19 VSYNC_3P3V >> VSYNC_NB

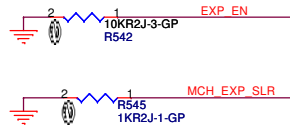
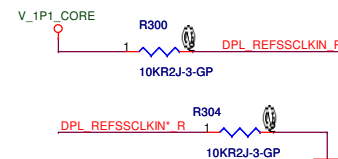
19 MCH_DDC_CLK >> MCH_DDC_CLK
19 MCH_DDC_DATA >> MCH_DDC_DATA



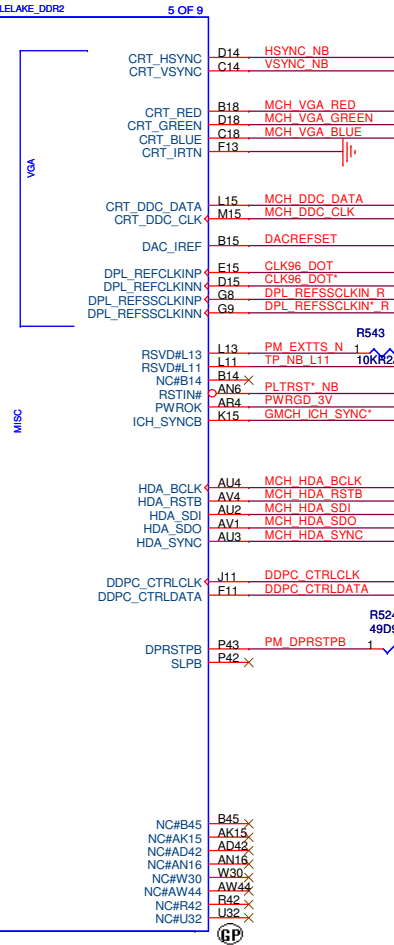
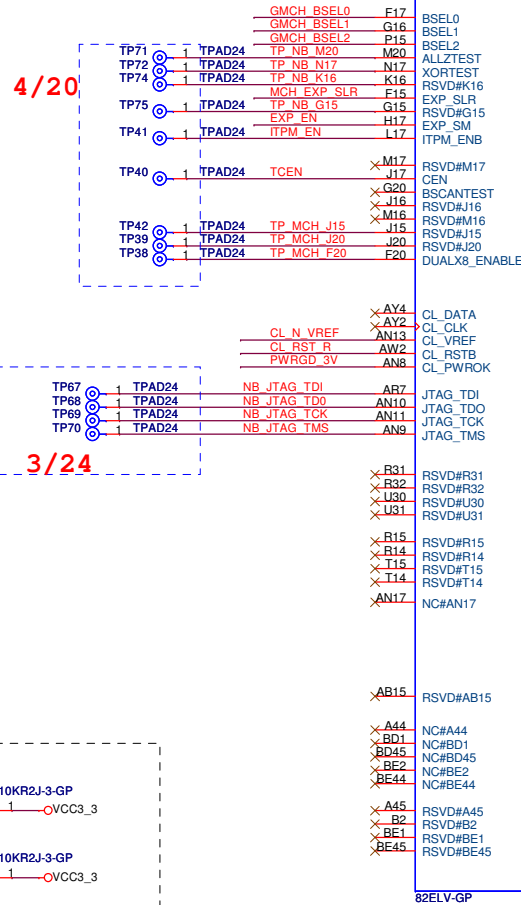
DDC CLK/DATA PULL-UP



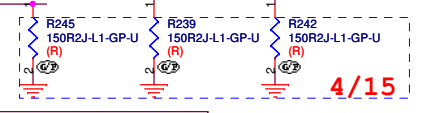
STUFF IF NOT SUPPORTING DISPLAY PORT



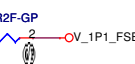
EXP_EN	EXP_SLR
0	Only SDVO or PCI Express Operational
1	SDVO and PCI Express operating simultaneously via PCI EXPRESS-G port; Support PCIE X1



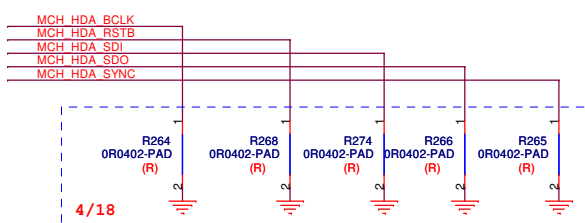
Layout Note: Place the resistor close to GMCH W/I 750 MILS



R261 1K02R2F-1-GP
Close to GMCH within 500mils to MCH Ball



HDMI Audio (non-used) 12/24



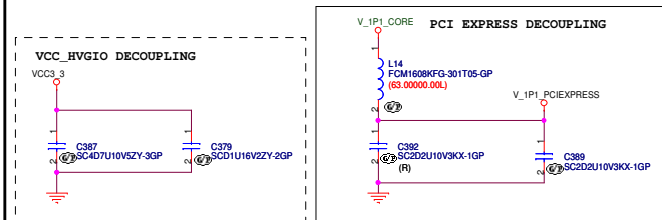
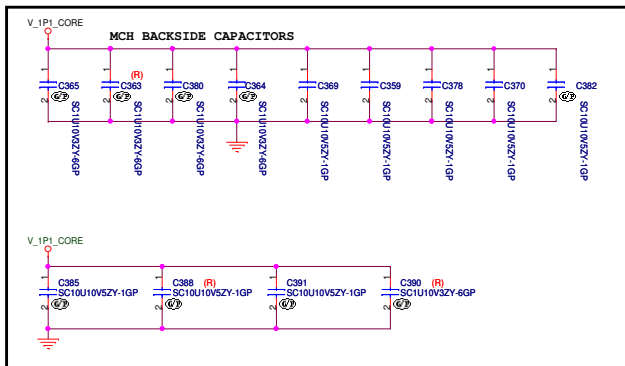
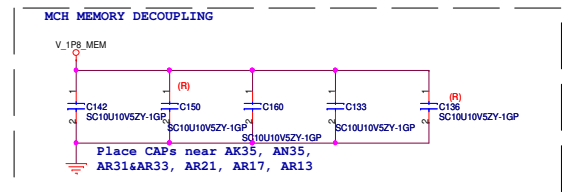
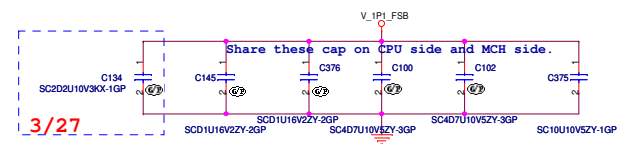
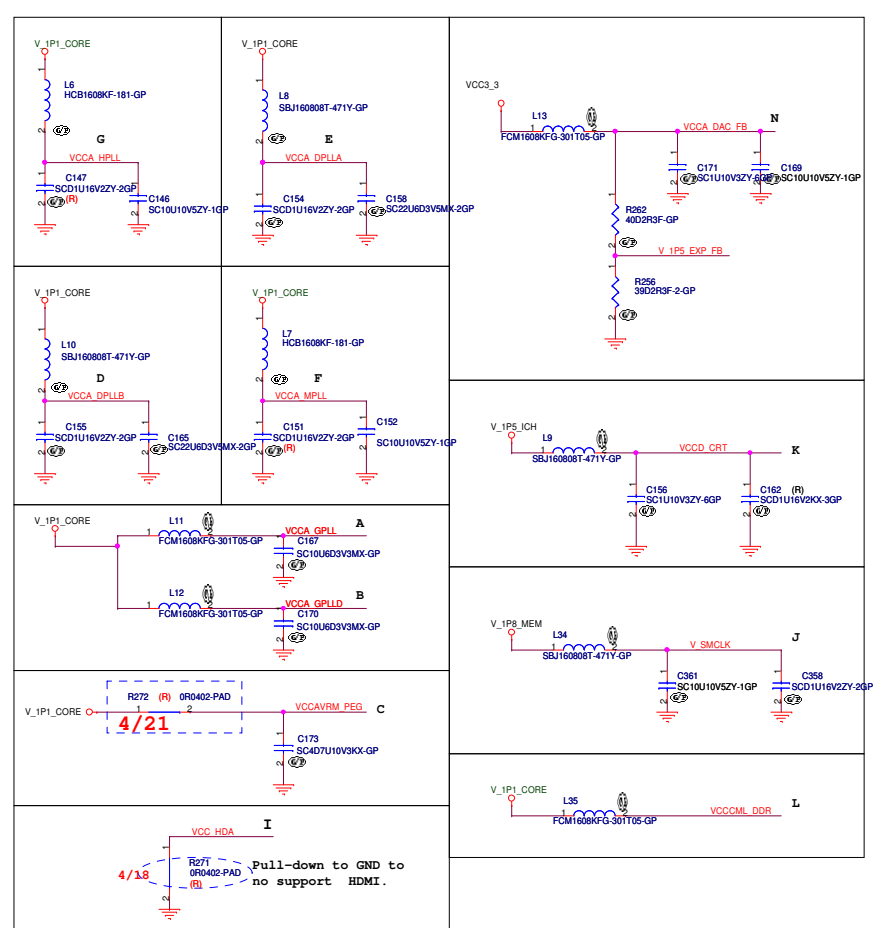
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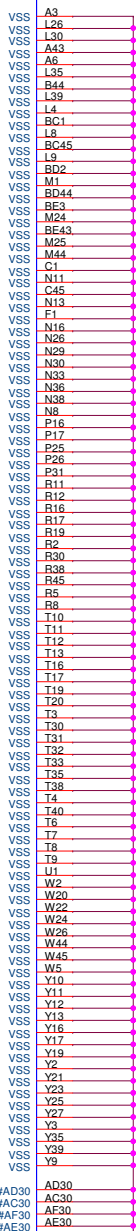
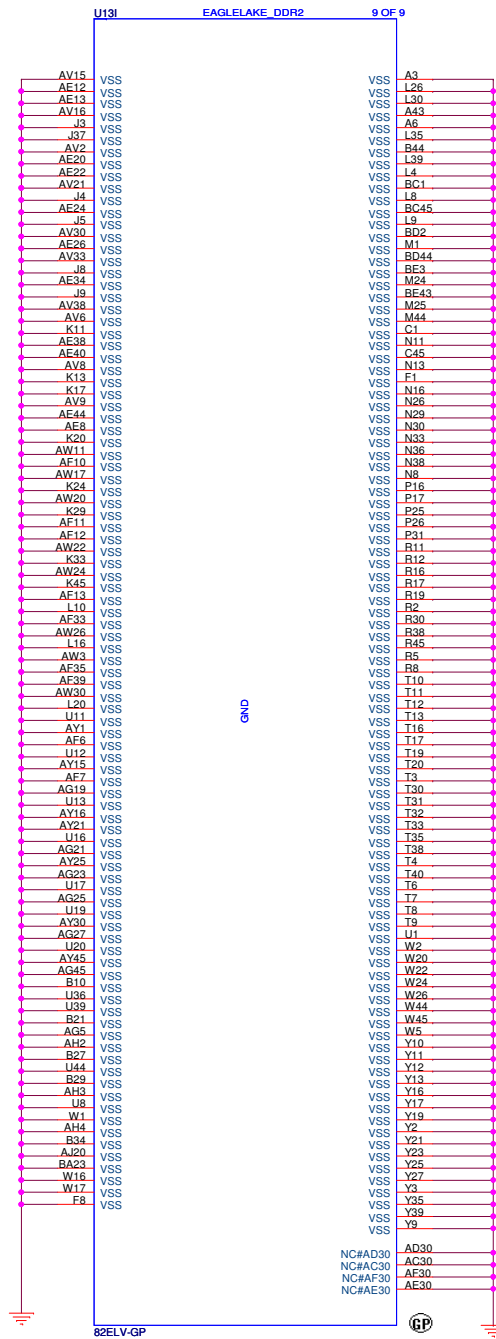
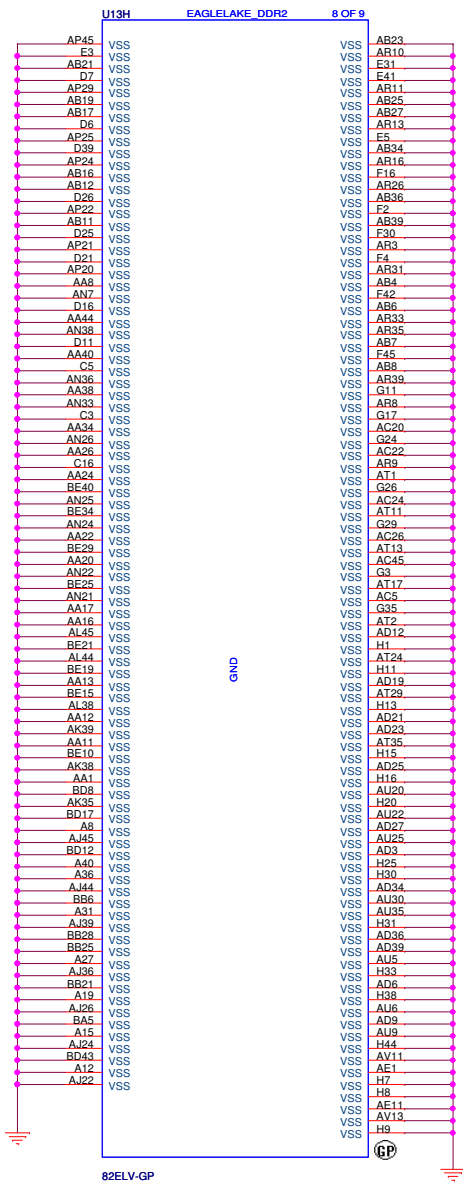
wistron Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title Eaglelake-G VGA

Size A3 Document Number TOYAMA Rev SA

Date: Friday, June 26, 2009 Sheet 13 of 39

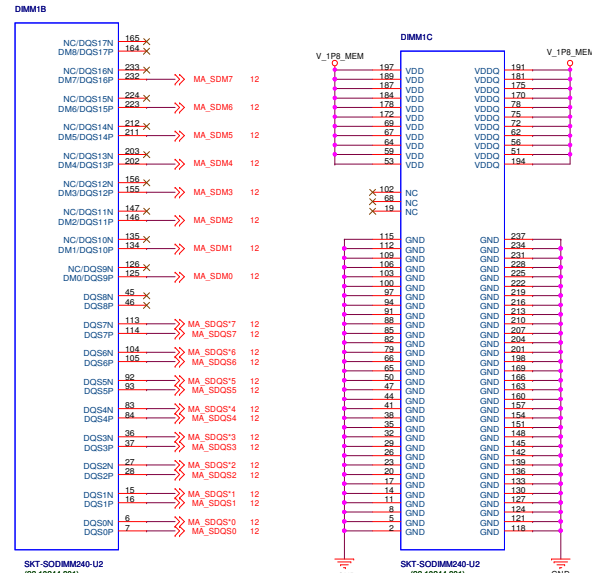
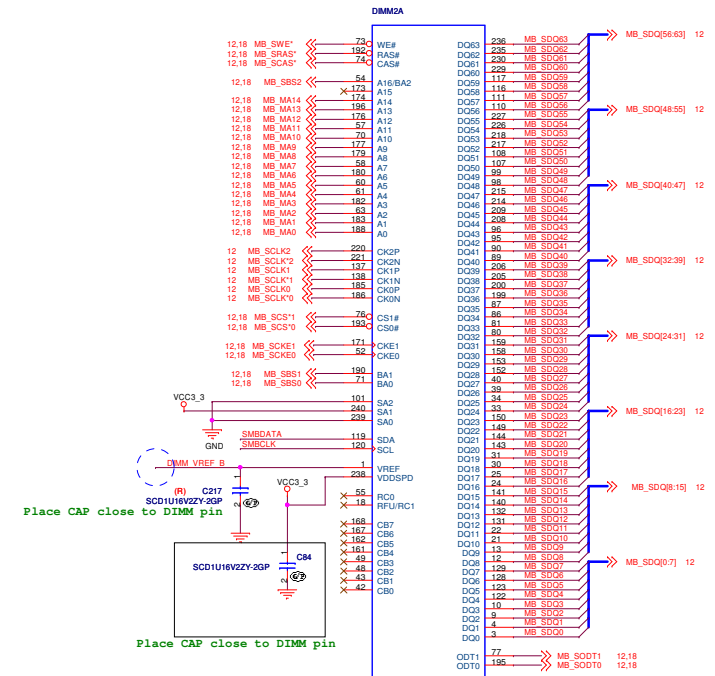




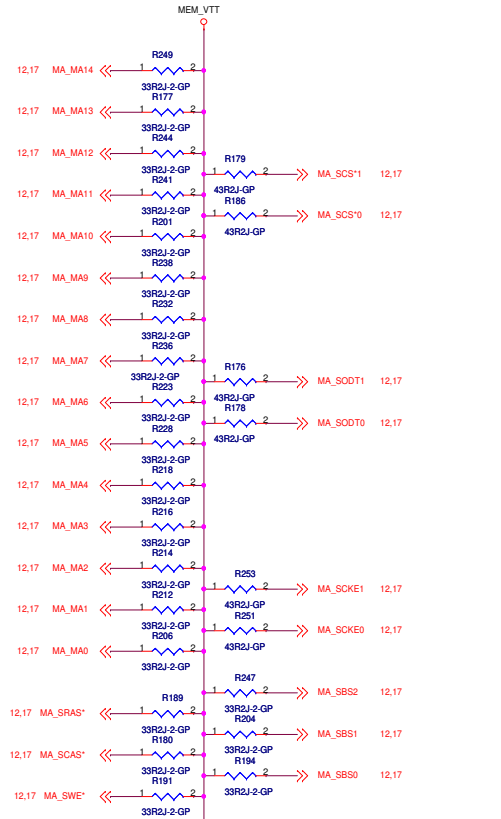
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wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsieh, Taipei	
Title Eaglelake-G GND			
Size	Document Number		Rev
Customer	TOYAMA		SA
Date:	Friday, June 26, 2009	Sheet	15 of 39

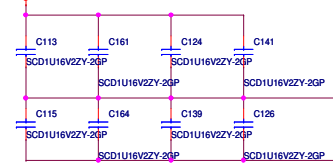
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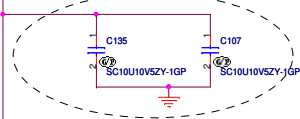
Channel A



Channel A Stitching Caps

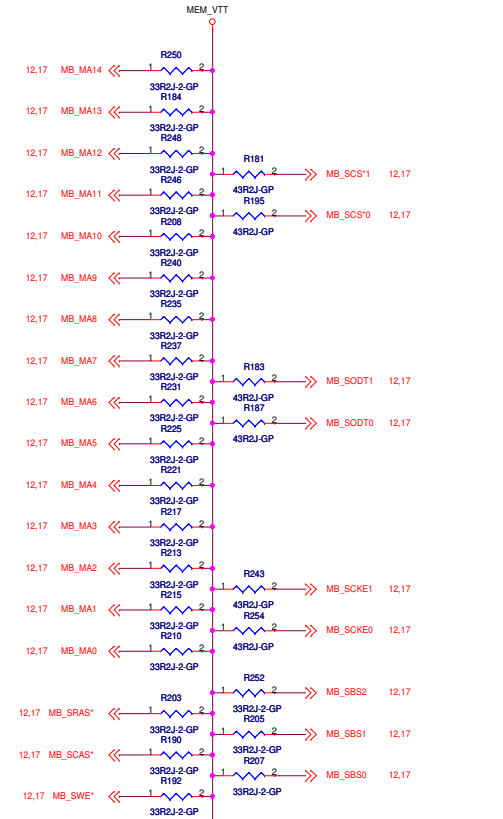


Channel A Decoupling Caps

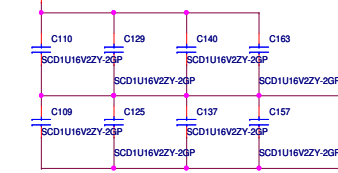


Place at opposite ends of the VTT island

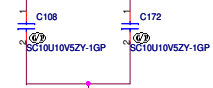
Channel B



Channel B Stitching Caps



Channel B Decoupling Caps



Place at opposite ends of the VTT island

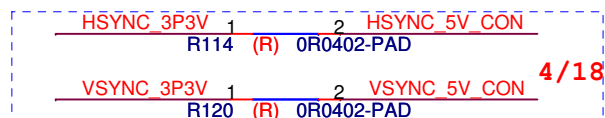
From MCH

13 HSYNC_3P3V
13 VSYNC_3P3V

HSYNC 3P3V
VSYNC 3P3V

13 MCH_DDC_CLK
13 MCH_DDC_DATA

MCH_DDC_CLK
MCH_DDC_DATA



13,20 MCH_VGA_RED
13,20 MCH_VGA_GREEN
13,20 MCH_VGA_BLUE

MCH_VGA_RED
MCH_VGA_GREEN
MCH_VGA_BLUE

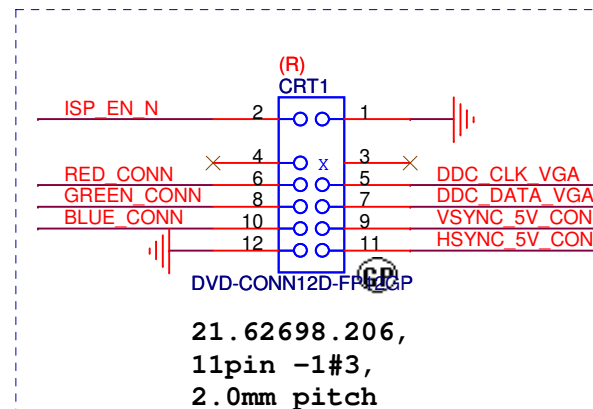
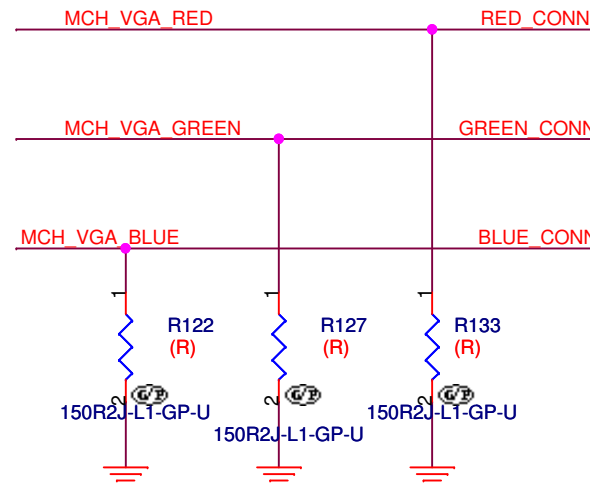
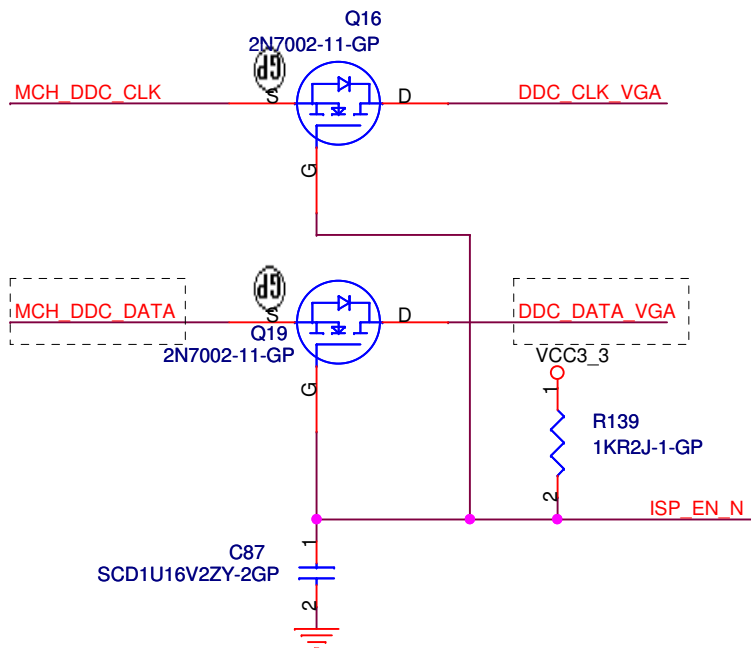
To SCALAR

20 DDC_CLK_VGA
20 DDC_DATA_VGA
20 VSYNC_5V_CON
20 HSYNC_5V_CON

DDC_CLK_VGA
DDC_DATA_VGA
VSYNC_5V_CON
HSYNC_5V_CON

13,20 RED_CONN
13,20 GREEN_CONN
13,20 BLUE_CONN

RED_CONN
GREEN_CONN
BLUE_CONN



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

VGA CONNECTOR

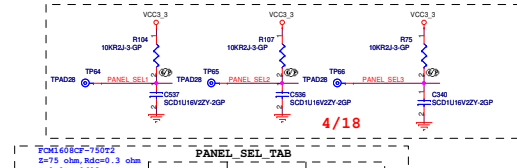
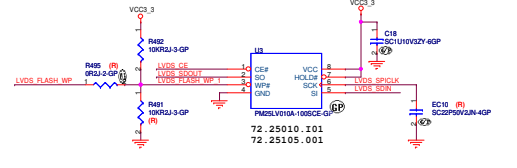
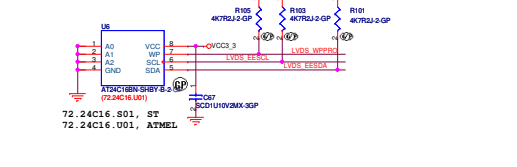
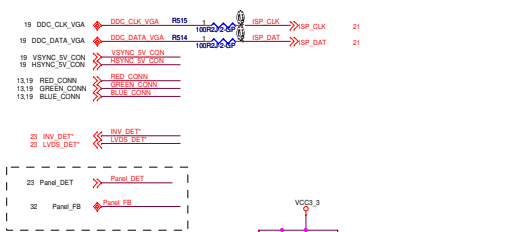
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Document Number
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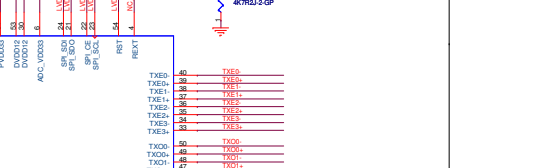
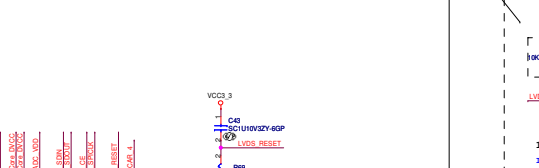
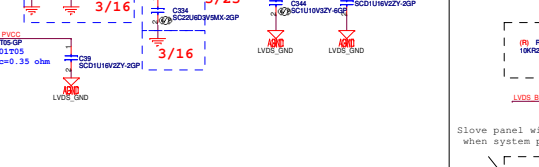
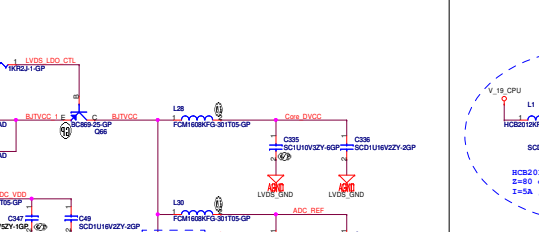
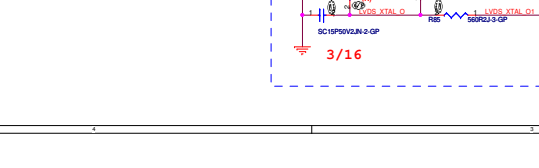
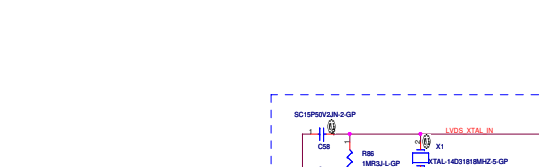
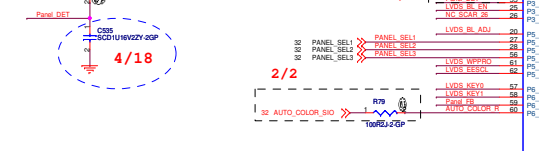
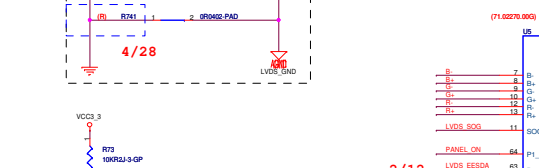
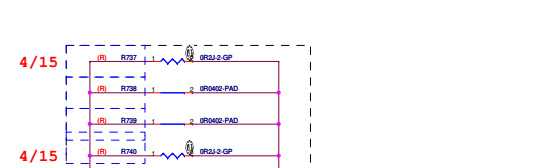
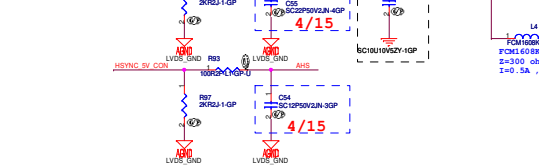
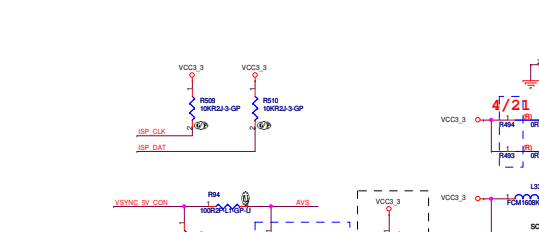
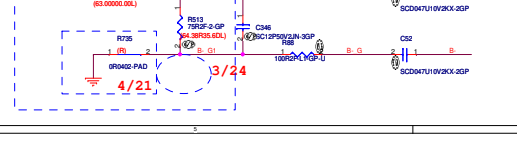
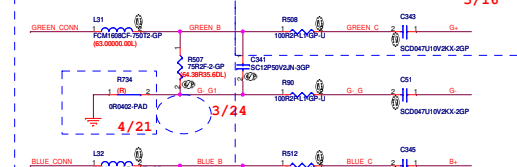
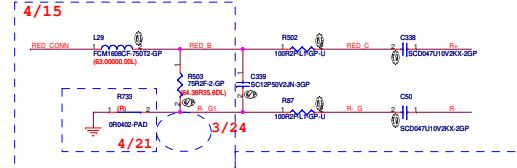
Rev
SA

Date: Friday, June 26, 2009

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1	0	1
1	1	0
1	0	0
0	1	1

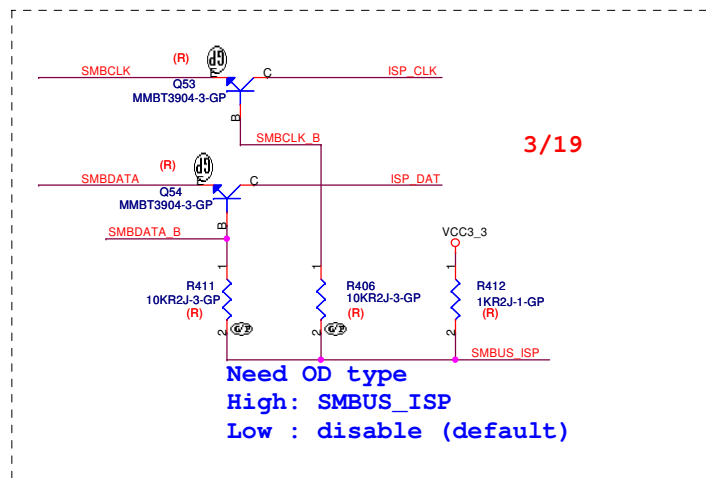
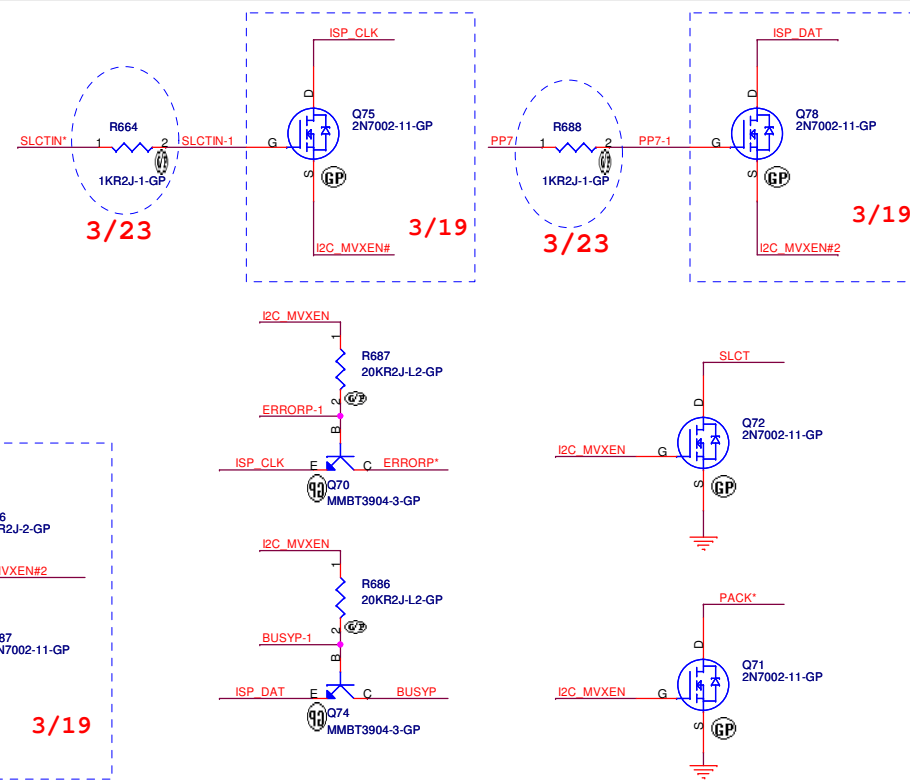
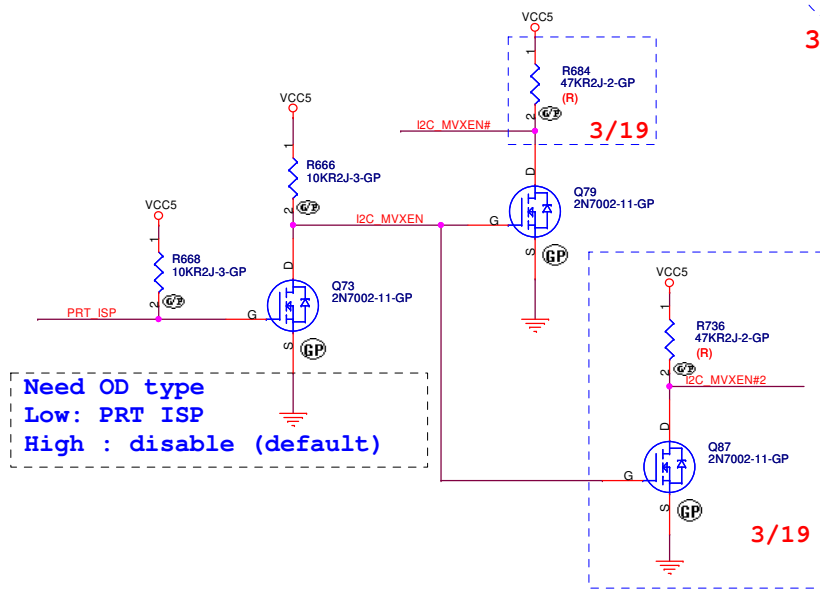


PARALLEL PORT

32,33	ERRORP*	ERRORP*
32,33	SLCTIN*	SLCTIN*
32,33	BUSYP	BUSYP
32,33	PP7	PP7
32,33	SLCT	SLCT
32,33	PACK*	PACK*

32	PRT_ISP	PRT_ISP
20	ISP_CLK	ISP_CLK
20	ISP_DAT	ISP_DAT

6,7,17,30,31,32	SMBCLK	SMBCLK
6,7,17,30,31,32	SMBDATA	SMBDATA
32	SMBUS_ISP	SMBUS_ISP



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

PRT and SMBUS ISP

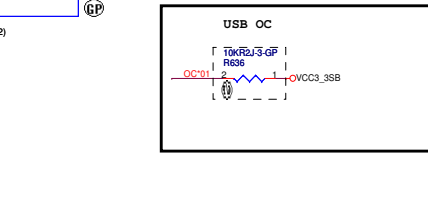
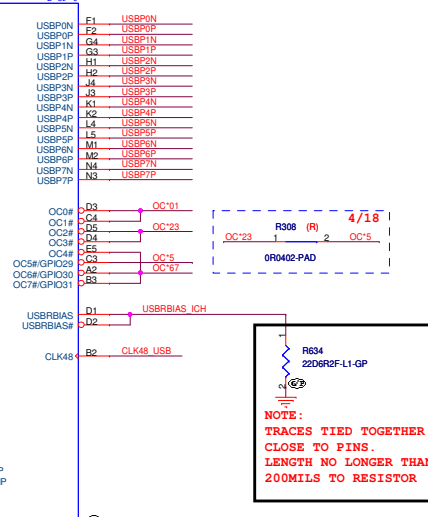
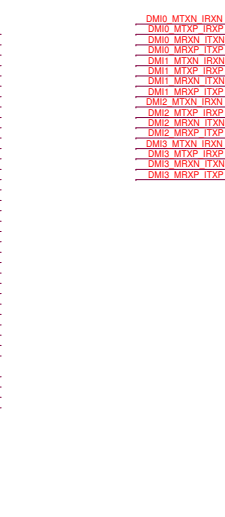
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Document Number
TOYAMA

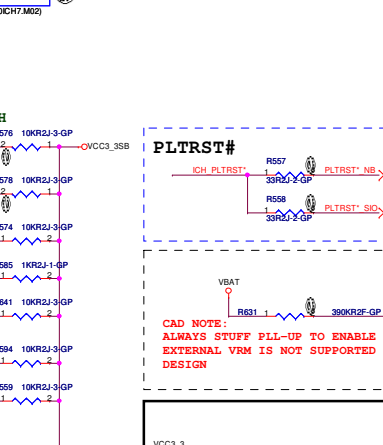
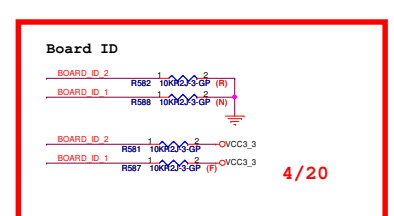
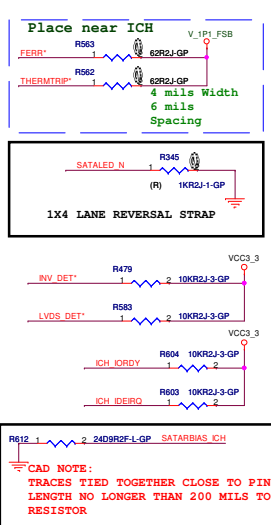
Rev
SA

Date: Friday, June 26, 2009

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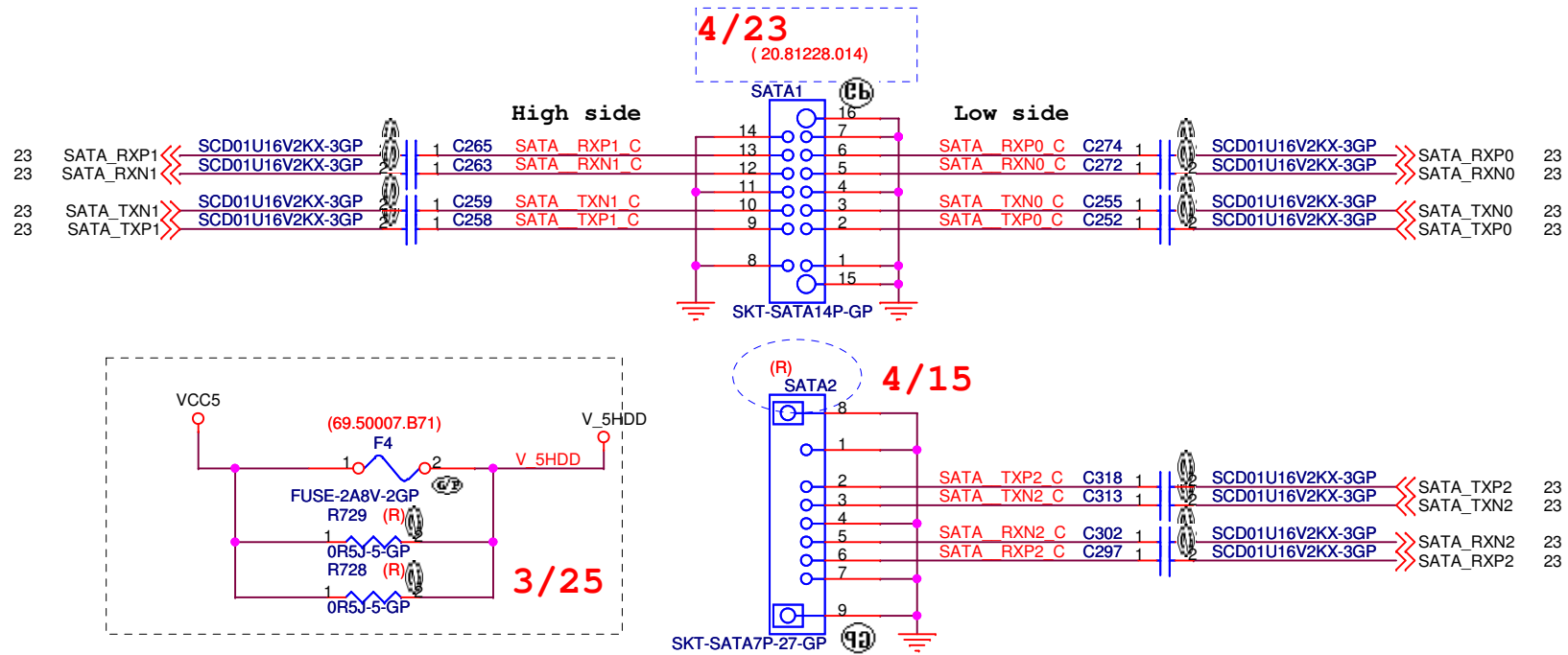


			B
			A
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Size C	Document Number TOYAMA	Rev SA	

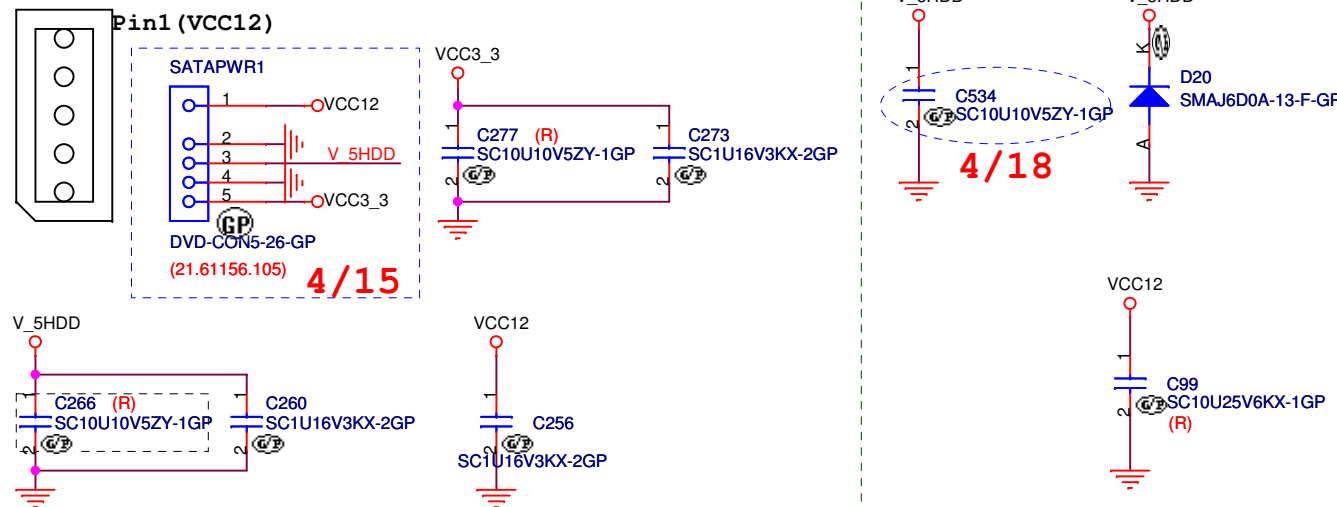


SATA CONNECTORS

SATA 2Port Right angle : 20.81227.014, 20.81228.014



Layout: Please put them together



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title **SATA CONN**

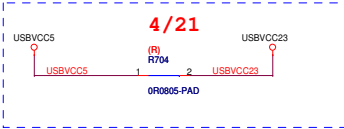
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Rev
SA

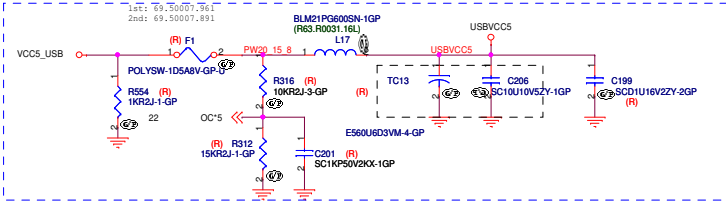
Date: Friday, June 26, 2009 Sheet 25 of 39

```
Side USB are Port 2, 3, 4, 5
Rear USB are Port 6, 7
Internal USB, Port 1 for Camera
Internal USB, Port 0 is for Mini PCIE slot
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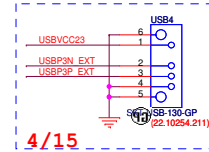
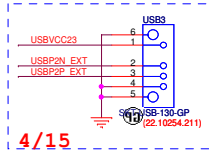
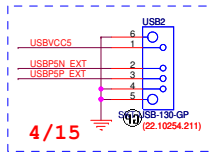
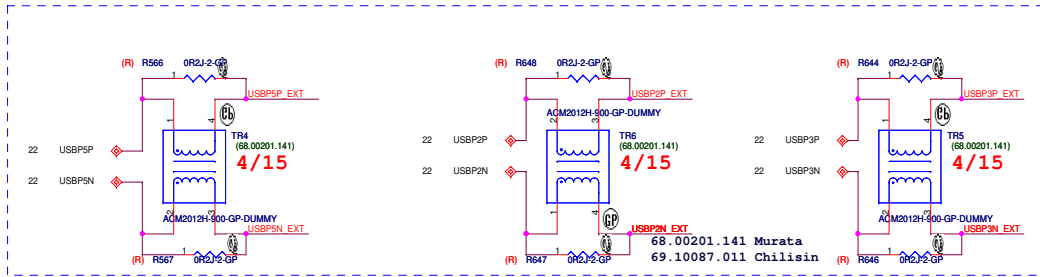
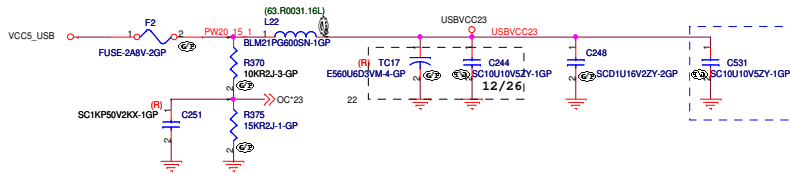


SIDE 2 USB PORT (5)

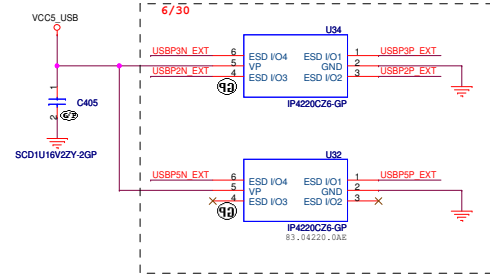
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2port USB : 22.10218.G71
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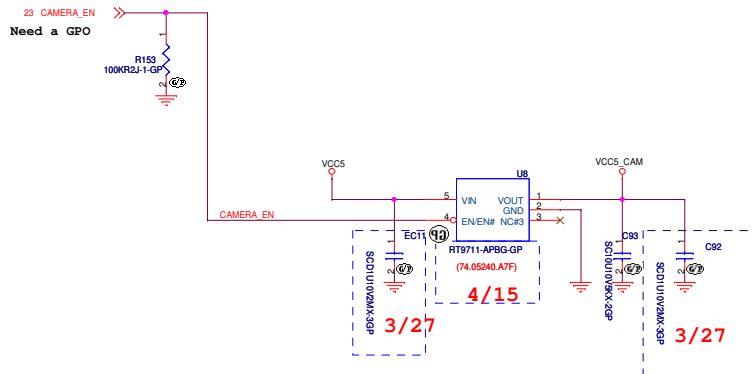
SIDE USB PORT (2/3)



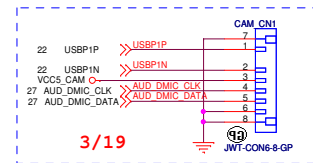
CLOSED TO USB CONNECTOR

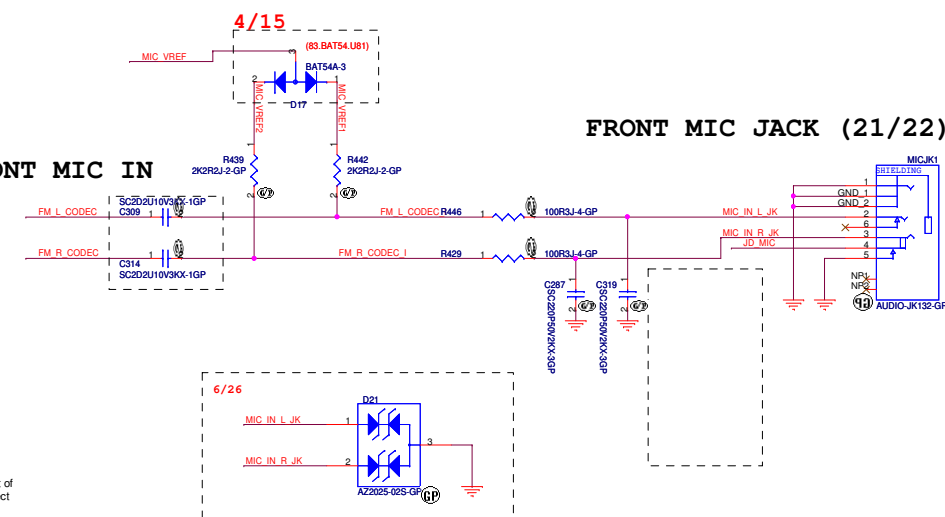
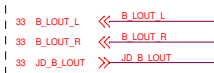


INTERNAL USB PORT (1)
for Camera, Digital Mic



Wrong part in X01 ,need to check it





6/26

D21

MIC IN L_JK 1

MIC IN R_JK 2

3

AD2025-02S-GP

GP



Please close to JKFHP1

F.HPO.L

R457 1 (R)

2 2N0603-PAD

HP.OUT.L.CON

F.HPO.R

R456 1 (R)

2 2N0603-PAD

HP.OUT.R.CON

10 HP

4/28

C321

SC220P50V2XK-3GP

C320

SC220P50V2XK-3GP

5V

NPN2

NPN3

19 AUDIO-JK132

6/26

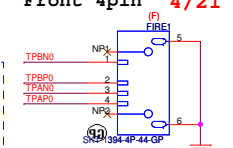
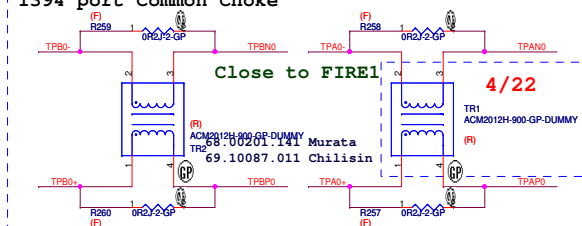
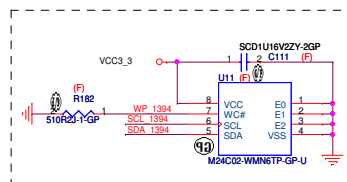
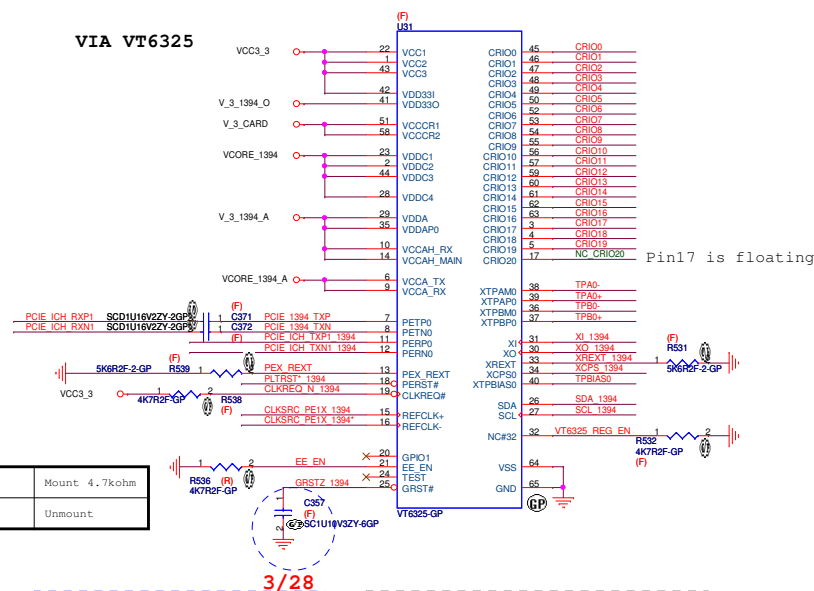
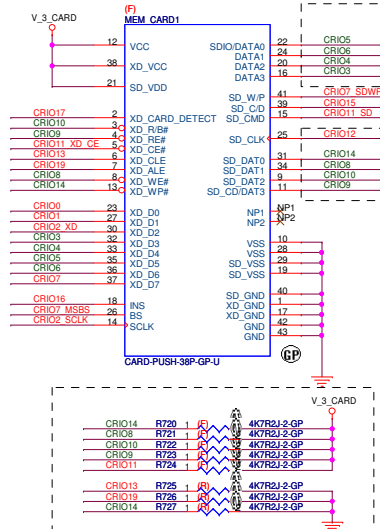
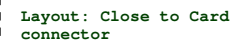
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HP.OUT.R.CON

D22

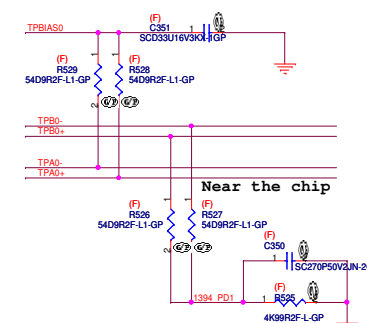
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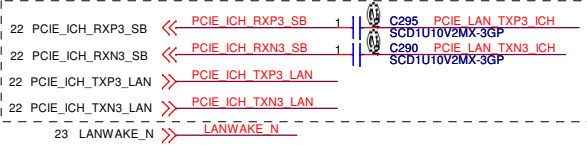
XCPS 1394

(F)
R530
1KR2F-3-GP

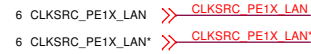


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<div> <div>Date:</div> <div>Friday, June 26, 2009</div> </div>		<div> <div>Sheet</div> <div>28 of 39</div> </div>	

Link to ICH



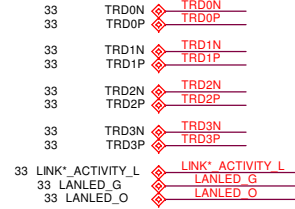
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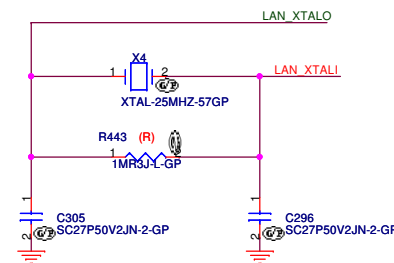
Link to SIO



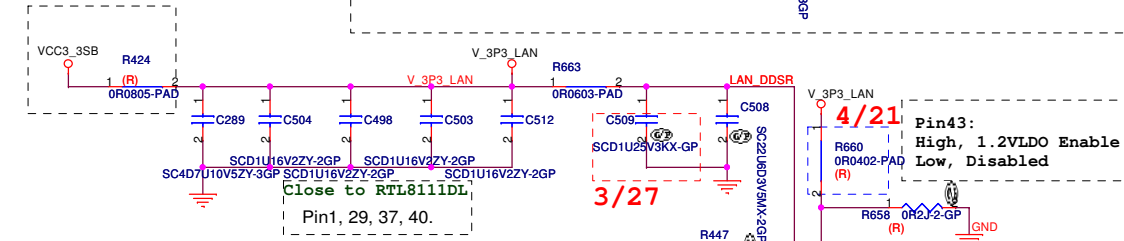
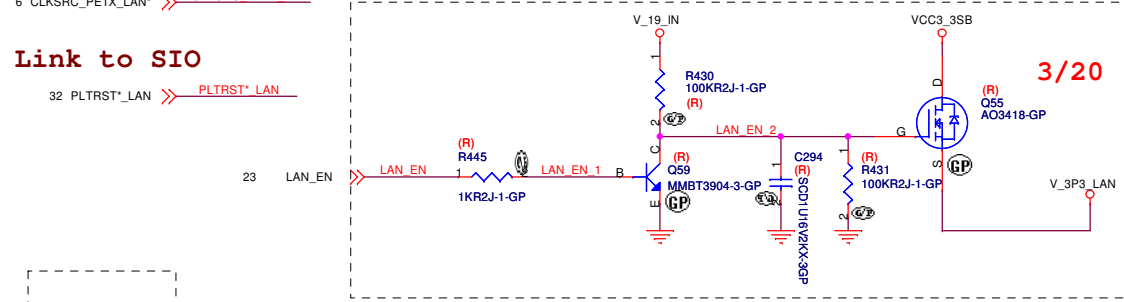
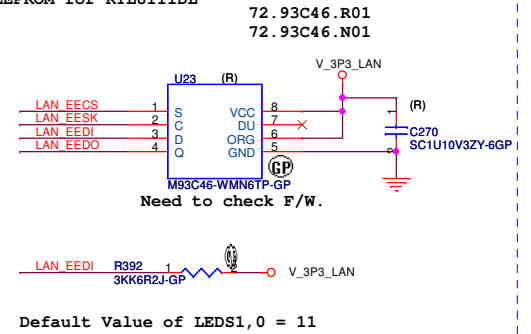
Link to RJ45(RISER1)



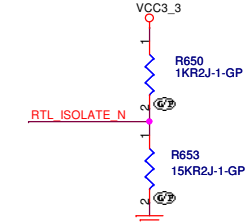
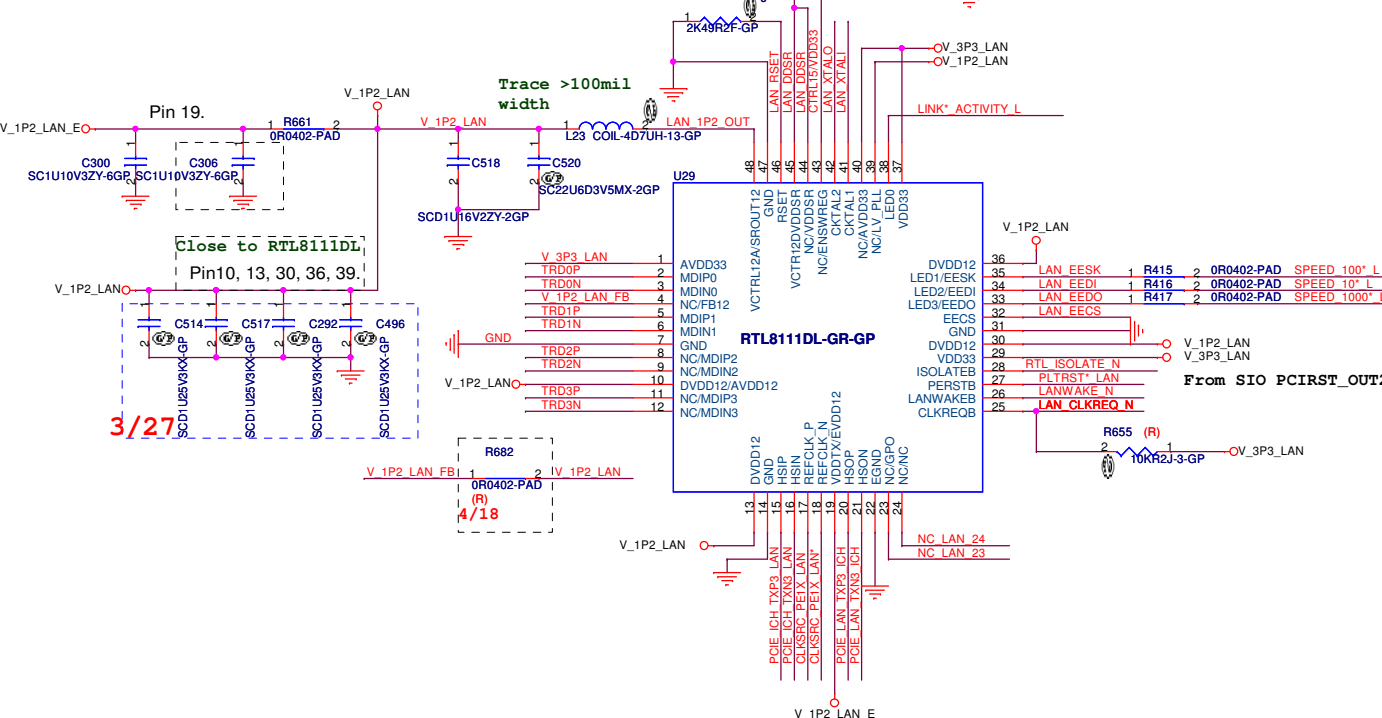
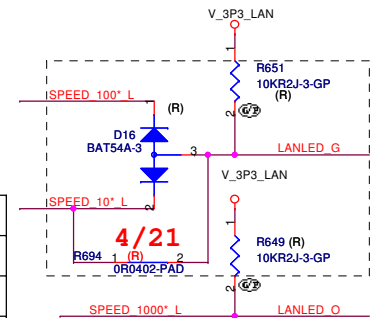
25MHz XTAL



EEPROM for RTL8111DL



	SPEED_10*_L	SPEED_100*_L	SPEED_1000*_L
10Mbps	L	H	H
100Mbps	H	L	H
1000Mbps	H	H	L



In layout

- The trace of Pin48 shall be within 200mil.
- The trace of Pin44,45 must be within 40mil.

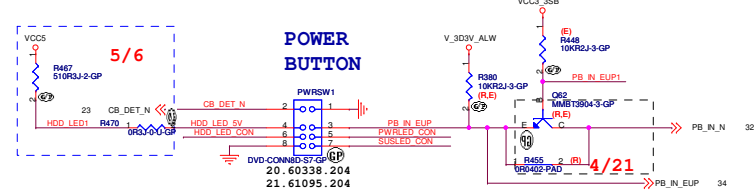
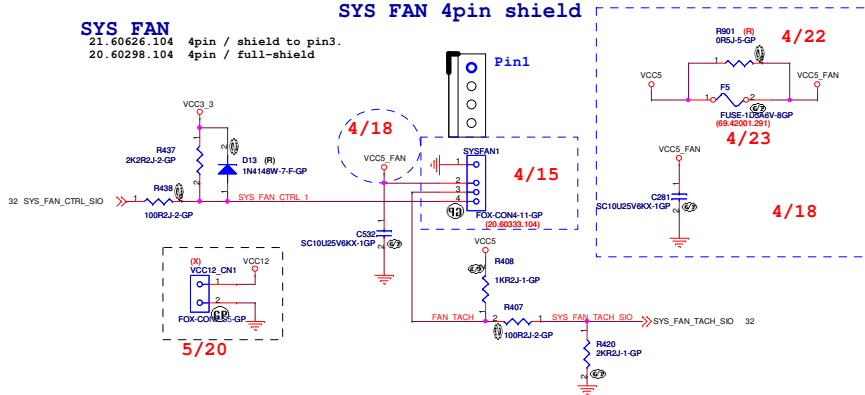
<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title Gb LAN RTL8111DL			
Size A3	Document Number TOYAMA		Rev SA
Date:	Friday, June 26, 2009	Sheet	29 of 39

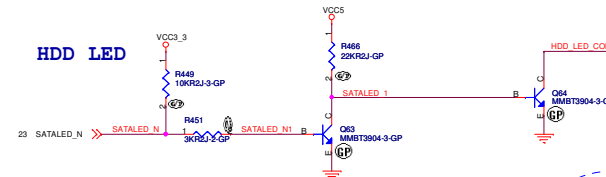
SYS FAN

21.60626.104 4pin / shield to pin3.
20.60298.104 4pin / full-shield

SYS FAN 4pin shield



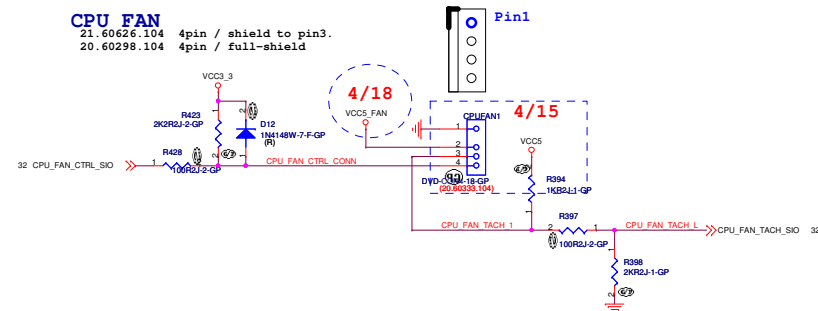
HDD LED



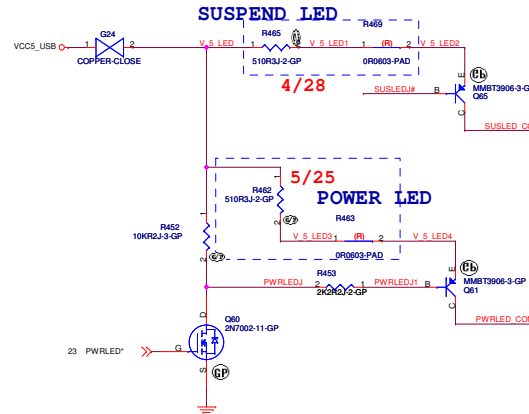
CPU FAN 4pin shield

CPU FAN

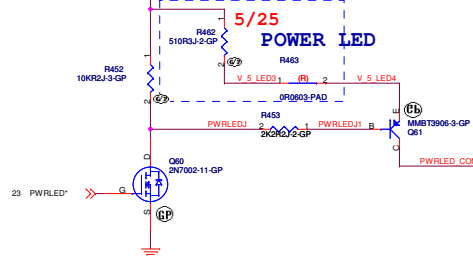
21.60626.104 4pin / shield to pin3.
20.60298.104 4pin / full-shield



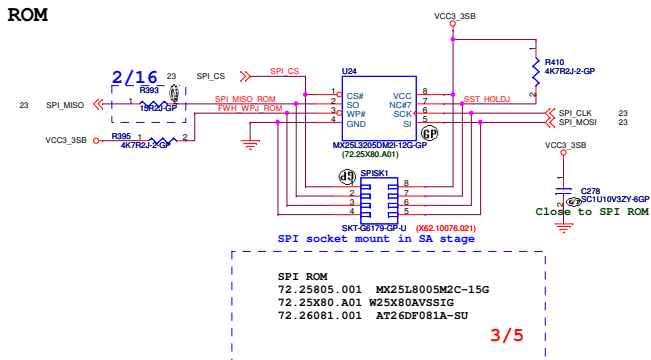
SUSPEND LED



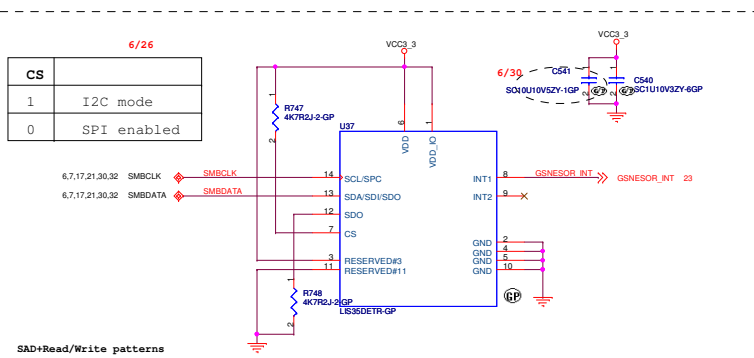
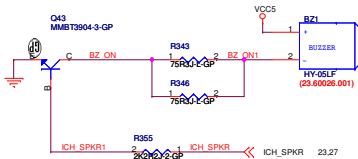
POWER LED



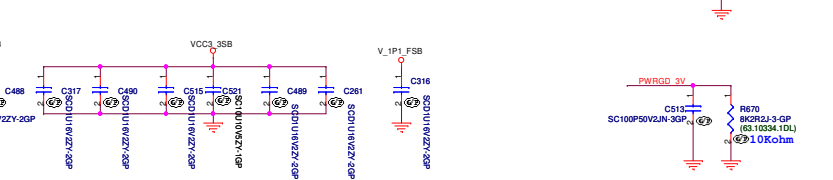
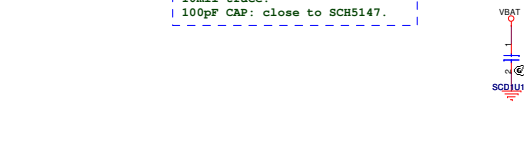
SPI ROM



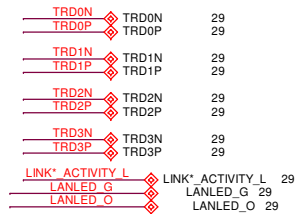
BUZZER



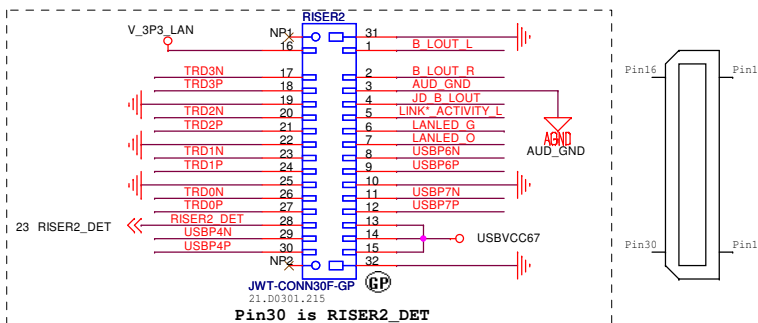
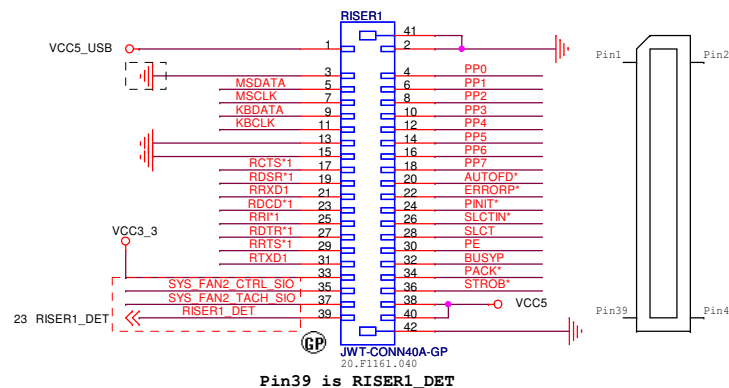
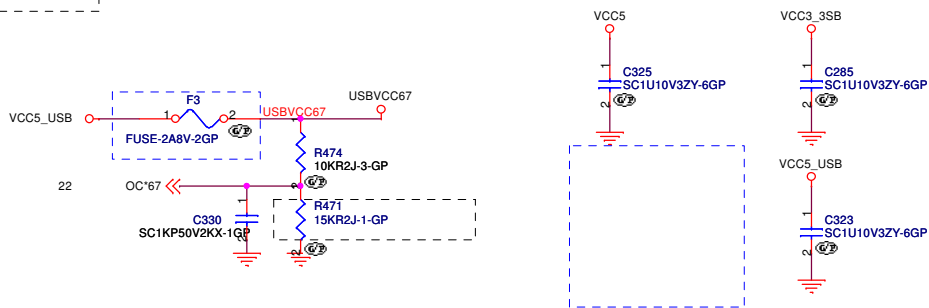
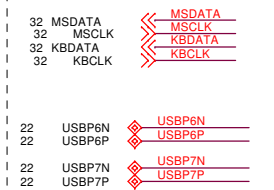
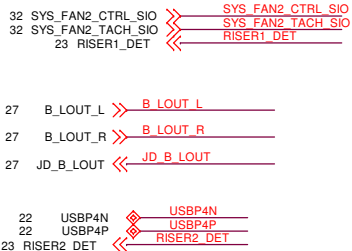
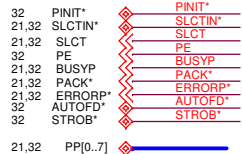
Command	SAD [6:1]	SAD [0]=SDO	R/W	SAD+R/W
Read	001110	0	1	00111001 (39h)
Write	001110	0	0	00111000 (38h)
Read	001110	1	1	00111011 (3bh)
Write	001110	1	0	00111010 (3ah)



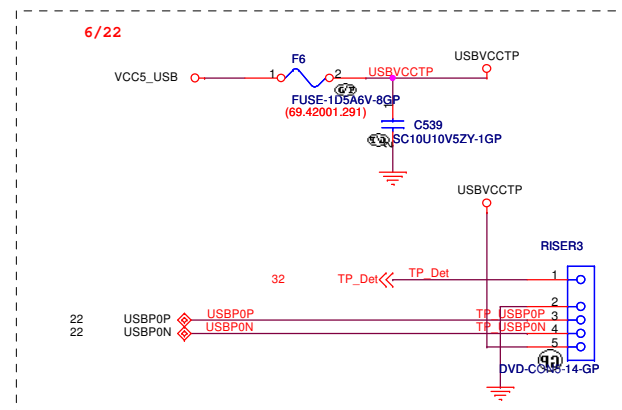
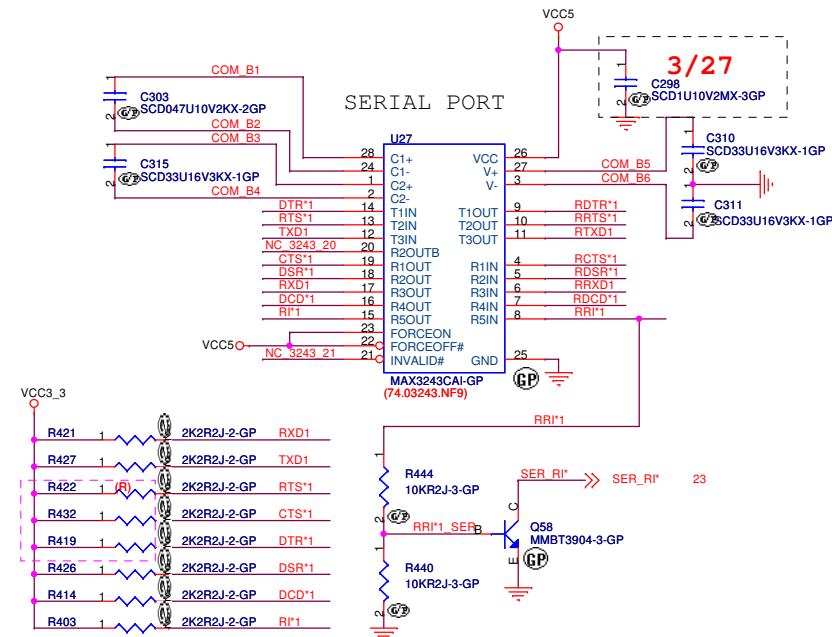
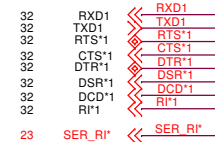
Gb LAN



PARALLEL PORT



SERIAL PORT



<Variant Name>

wistronWistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, TaipeiTitle
REAR IO RISERSize A3 Document Number
TOYAMA

Date: Friday, June 26, 2009

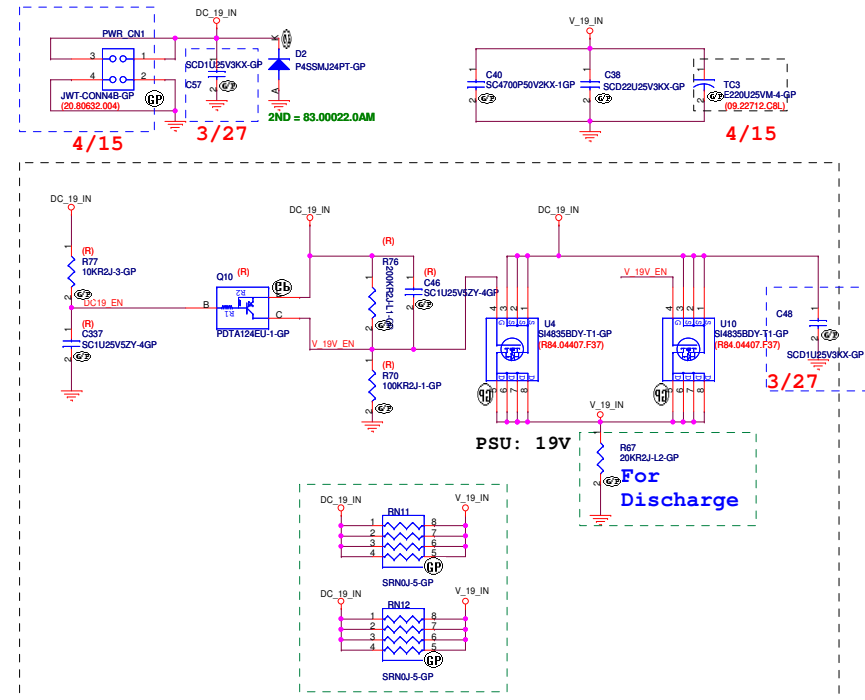
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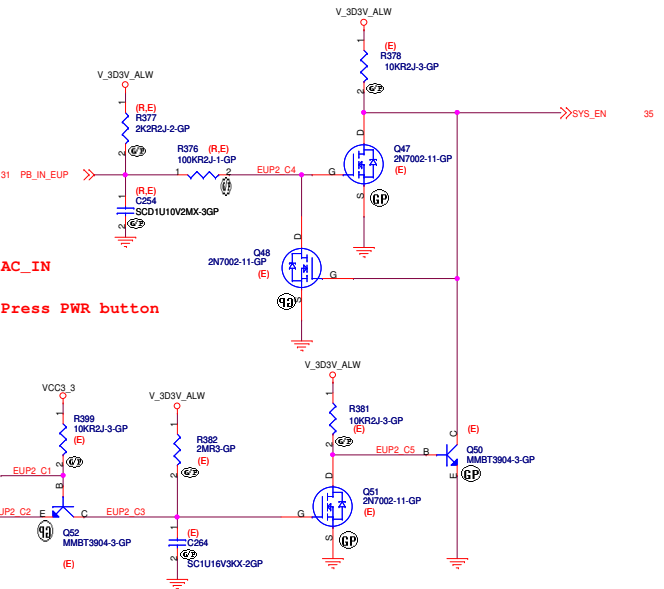
DC 19V IN

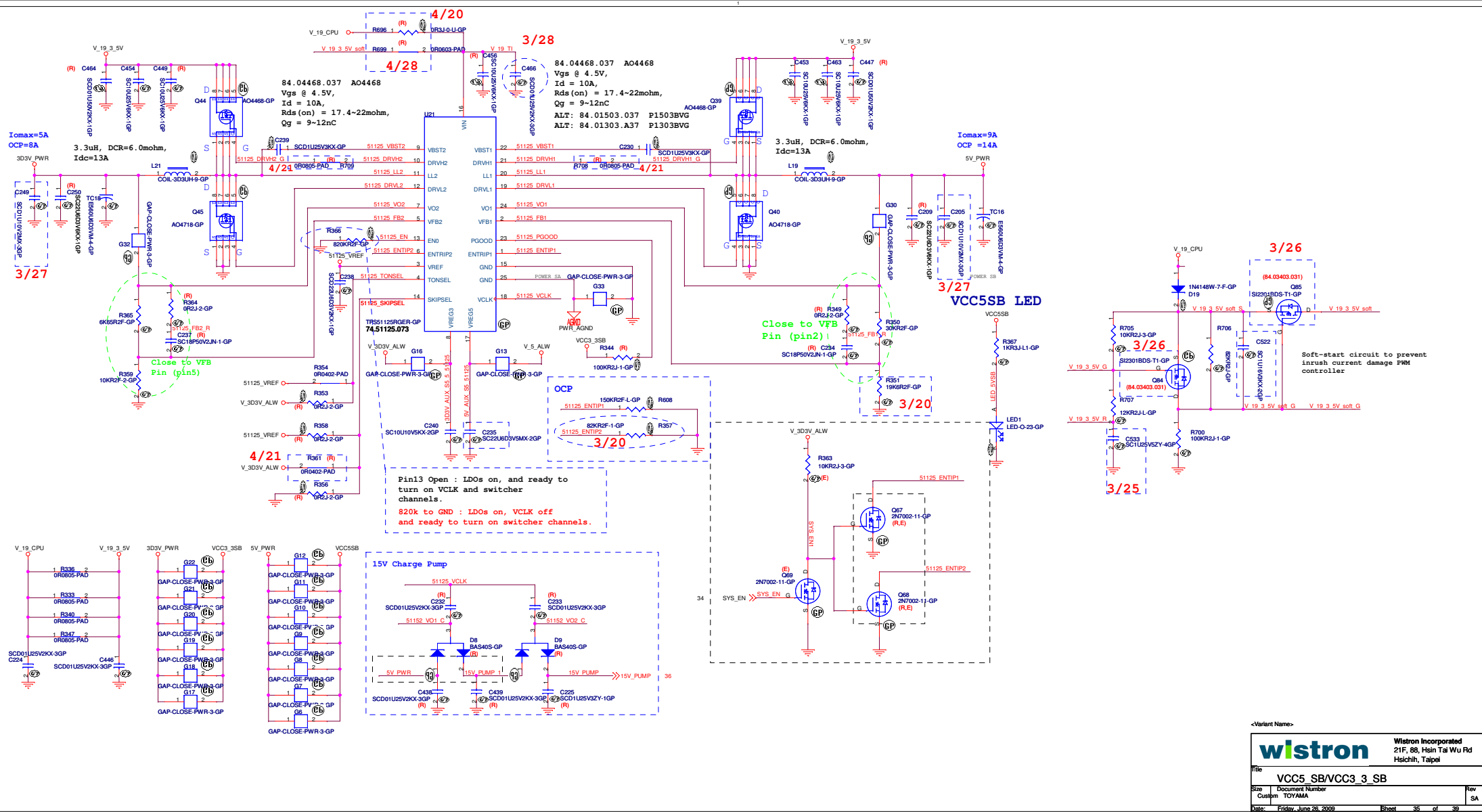
4	3
2	1

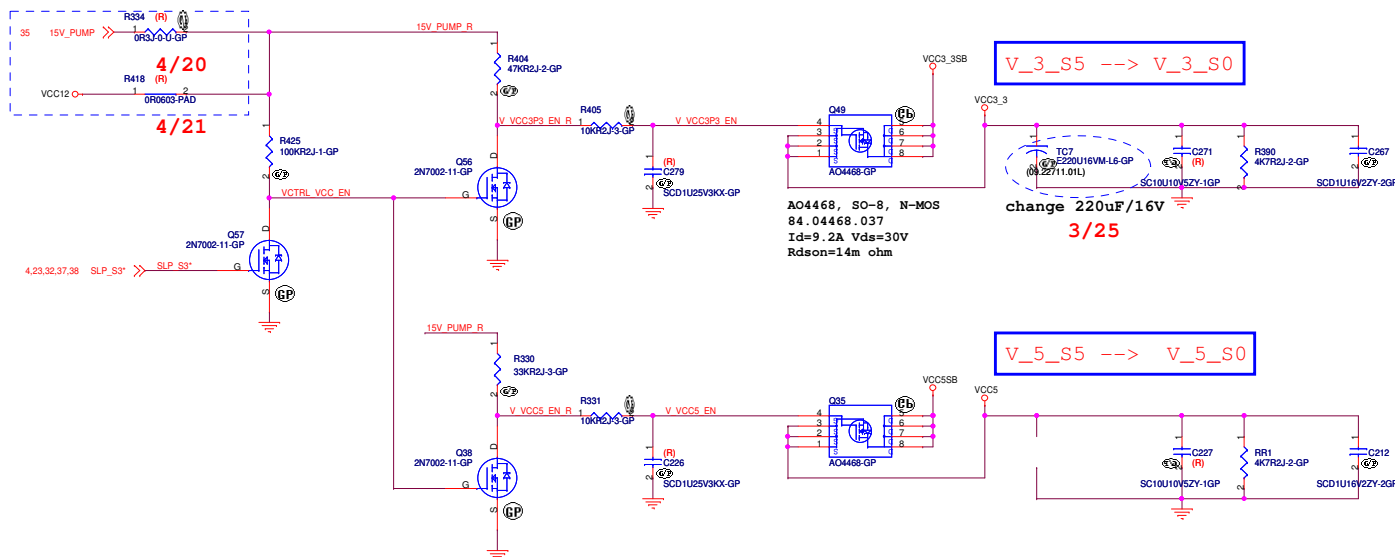
20.80991.004
20.80326.004



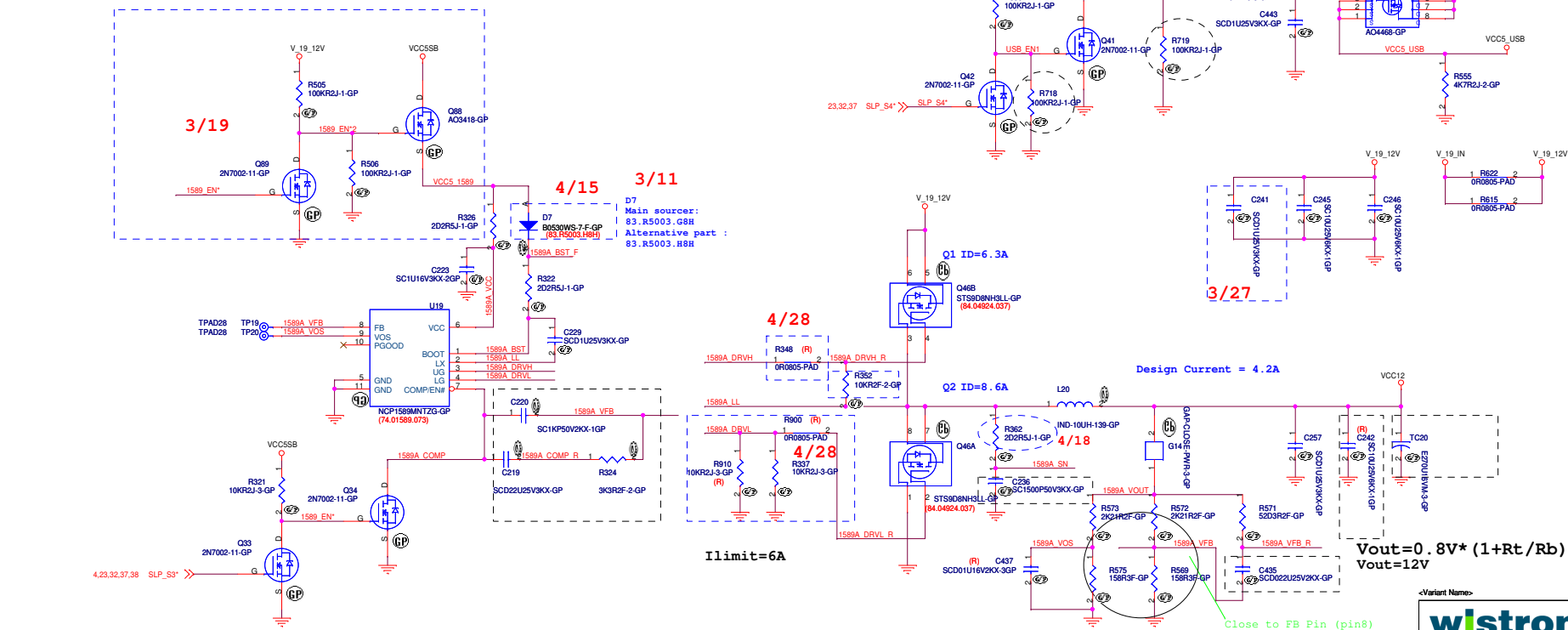
PB_IN_EUP	SLP_S5_N	SYS_EN
X	H	H
X	H	H
H	L	L
	L	H



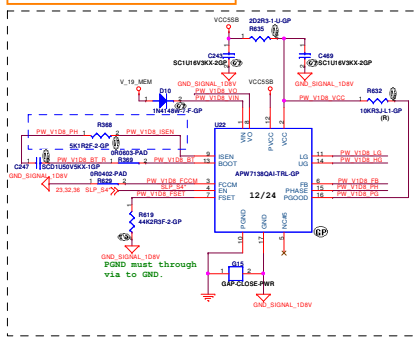




ADP_19V --> V_{12_S0}

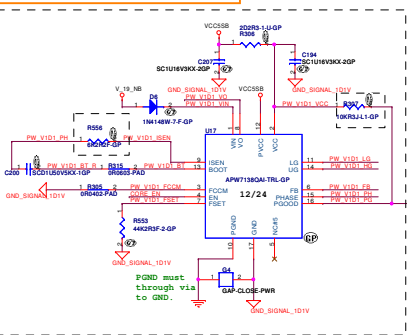


V_19_IN --> V_1P8_MEM

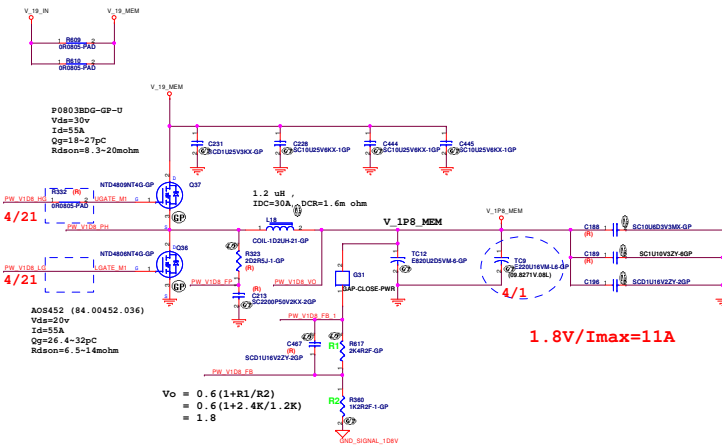
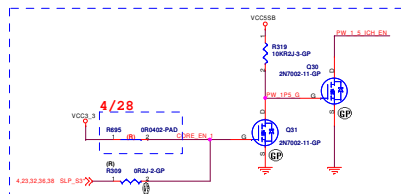


$$\begin{aligned} \text{Risen} &= 5.1k, \text{Rds (on)} = 9.4m\Omega \\ \text{OCP} &= (I_{oc} * \text{Risen}) / \text{Rds(on)} = I_{ocsp} \\ \text{OCP} &= (26u * 5.1k) / 9.4m = 14.1A \end{aligned}$$

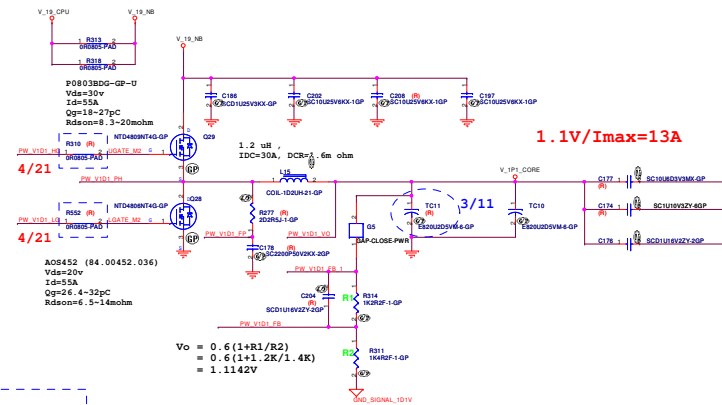
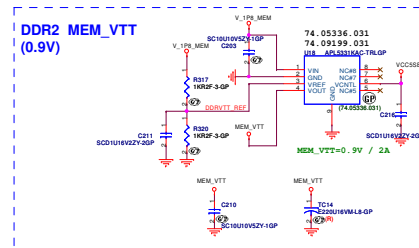
V_19_IN --> V_1P1V



$$\begin{aligned} \text{Risen} &= 6.2k, \text{Rds (on)} = 9.4m\Omega \\ \text{OCP} &= (I_{oc} * \text{Risen}) / \text{Rds(on)} = I_{ocsp} \\ \text{OCP} &= (26u * 6.2k) / 9.4m = 17.2A \end{aligned}$$

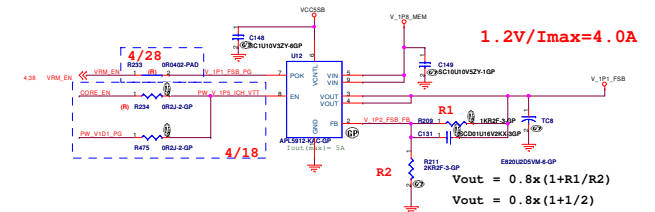


$$1.8V / I_{max} = 11A$$



$$1.1V / I_{max} = 13A$$

V_FSB_VTT support 65nm Quad-core Processors on Intel 4 series chipset

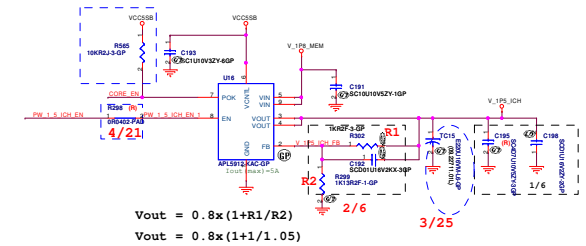


$$1.2V / I_{max} = 4.0A$$

$$\begin{aligned} V_{out} &= 0.8x(1+R1/R2) \\ V_{out} &= 0.8x(1+1/2) \end{aligned}$$

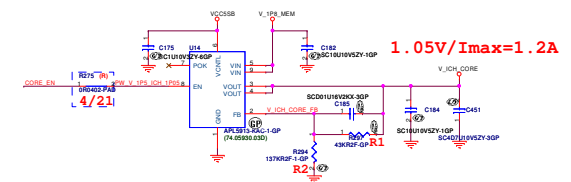
V_1P8_MEM --> V_1P5_Ich

$$\begin{aligned} 1.5V / I_{max} &= 2.8A \\ 2.3A &\text{ for ICH10,} \\ 0.5A &\text{ for Mini PCIE card.} \end{aligned}$$

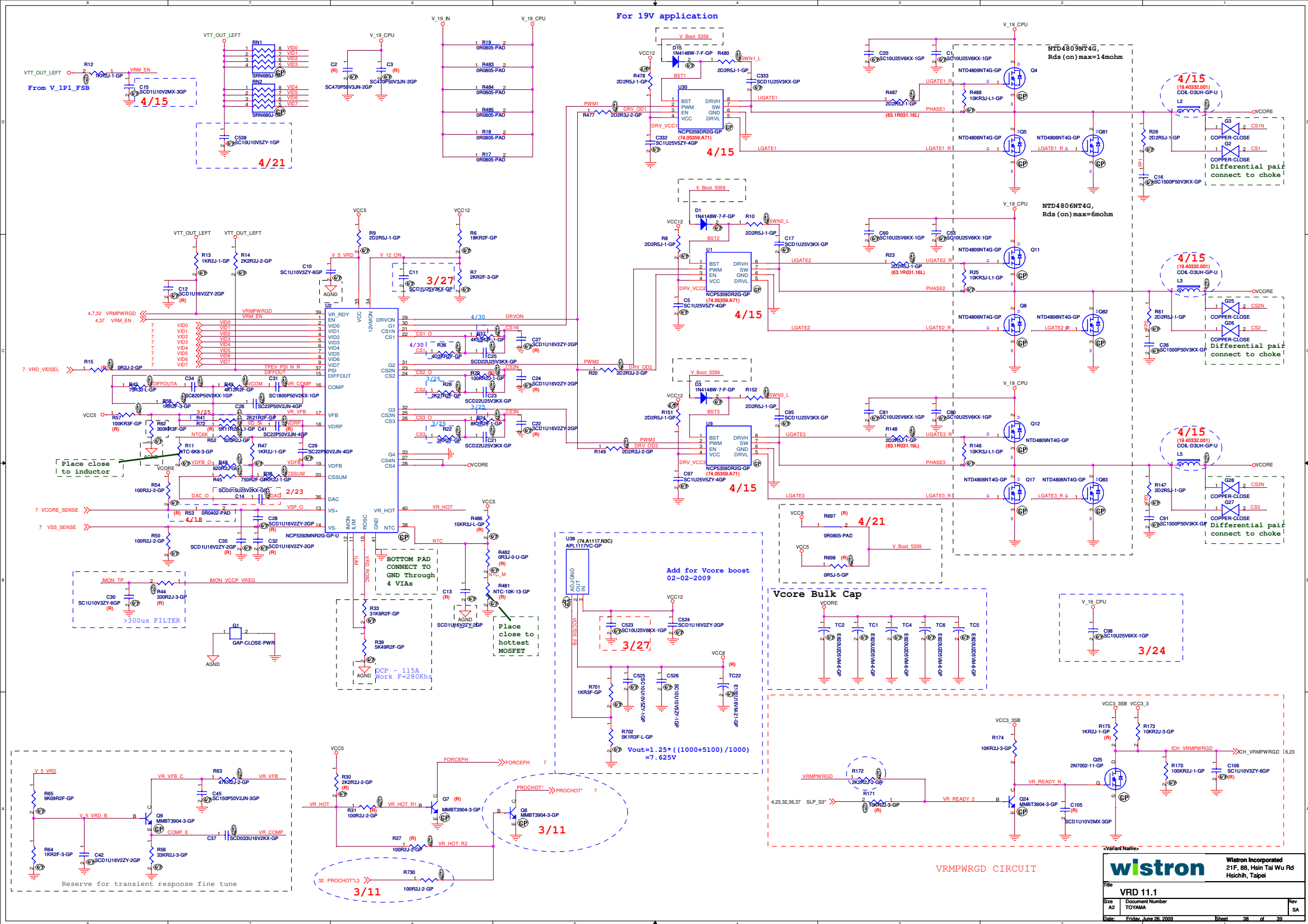


$$\begin{aligned} V_{out} &= 0.8x(1+R1/R2) \\ V_{out} &= 0.8x(1+1/1.05) \end{aligned}$$

Vout= V_1P05_Ich



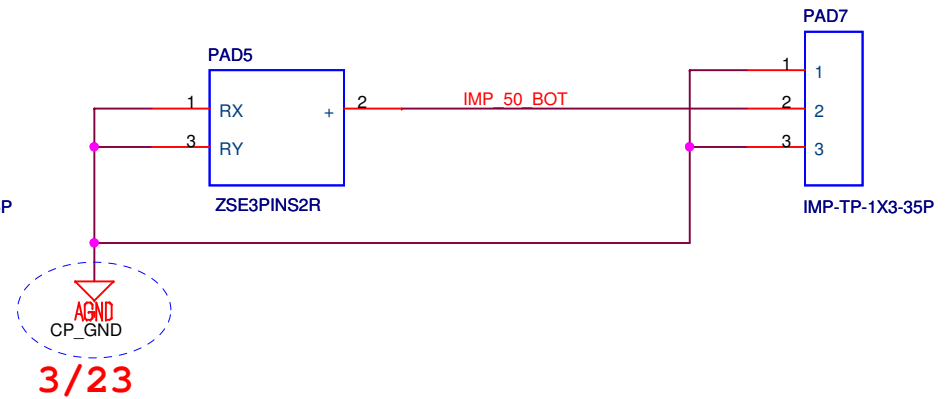
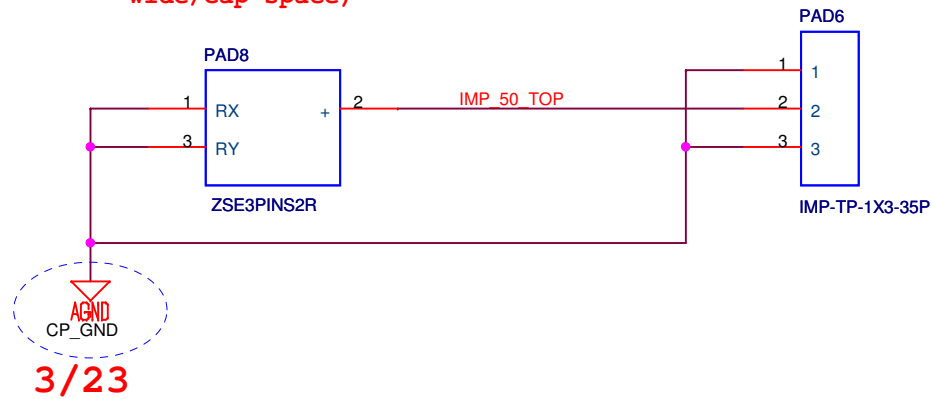
$$\begin{aligned} V_{out} &= 0.8x(1+R1/R2) \\ V_{out} &= 0.8x(1+43/137) \end{aligned}$$



Place these COUPON in V-cut

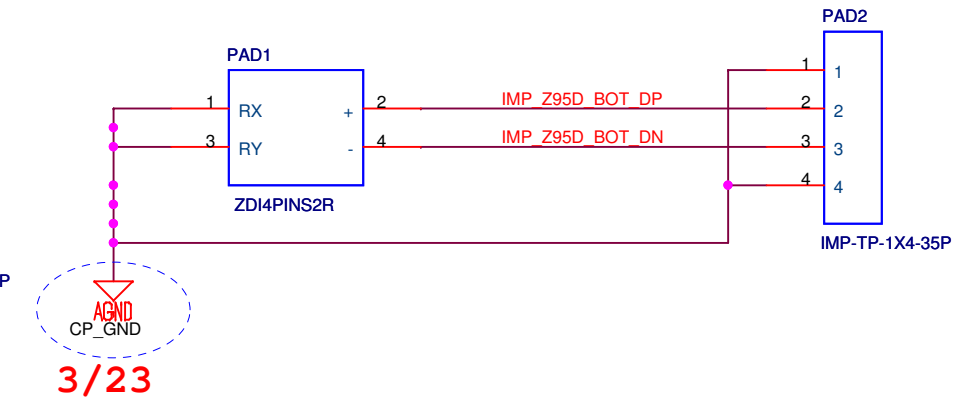
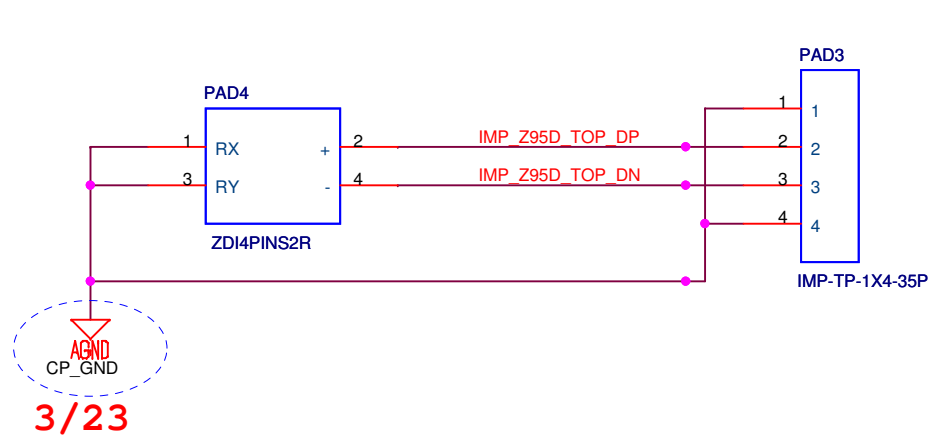
50 OHM TRACE

The traces rule of TOP and BOT is 4 (Trace wide/Gap space)



95 OHM TRACE

The traces rule of TOP and BOT is 4/8/4 (Trace wide/Gap space/Trace wide)



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

TEST COUPON

Size
A4

Document Number
TOYAMA

Rev
SA

Date: Friday, June 26, 2009

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