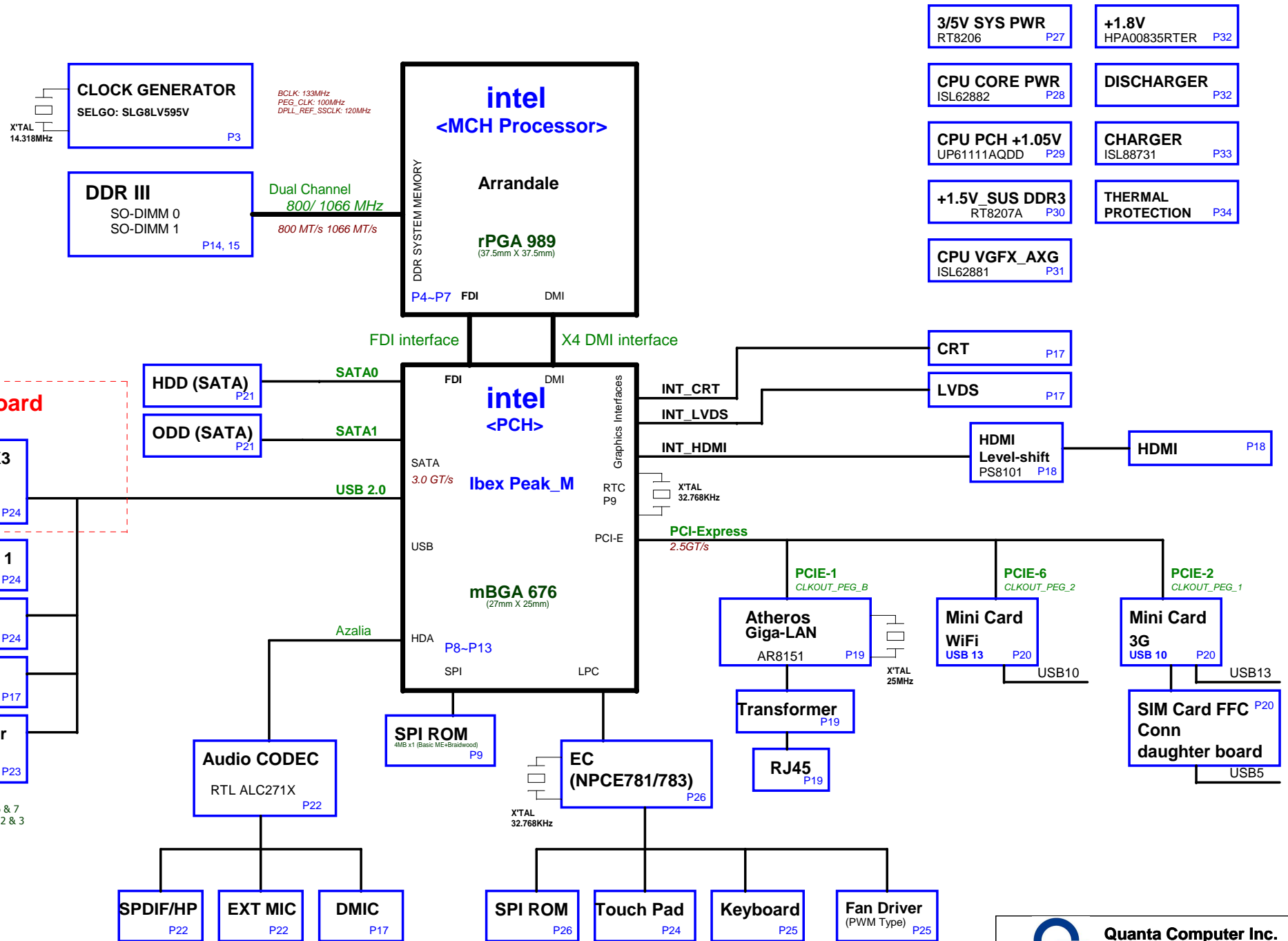


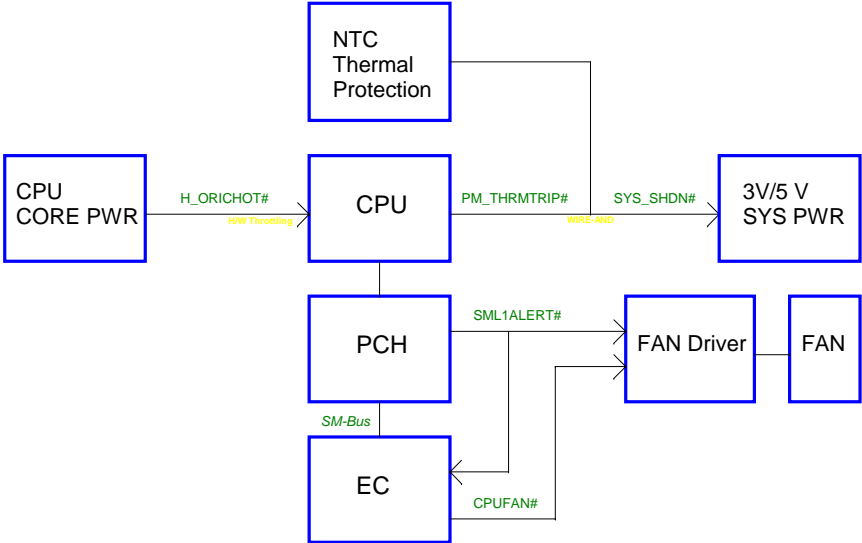
ZQ1(6Layer) BLOCK DIAGRAM



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER		S0~S5
+RTC_CELL	+3V~+3.3V	RTC		S0~S5
+3VPCU	+3.3V	8051 POWER	ALWON	S0~S5
+5VPCU	+5V	CHARGE POWER	ALWON	S0~S5
+15V	+15V	LARGE POWER	+15V_ALWP	S0~S5
3V_LAN_S5	+3.3V	LAN POWER	AUX_ON	
+5VSUS	+5V		SUSD	
+3VSUS	+3.3V		SUSD	
+1.5V_SUS	+1.5V	SODIMM POWER	SUSON	
+0.75V_DDR_VTT	+0.9V	SODIMM POWER	MAINON	
+5V	+5V		MAIND	
+3V	+3.3V		MAIND	
+1.8V	+1.8V		MAINON	
+1.5V	+1.5V	PCH POWER	MAIND	
+1.1V_VTT	+1.05V~+1.1V	CPU POWER	MAINON	
+1.05V	+1.05V	PCH POWER	MAINON	
+VCC_CORE	0V~+1.5V	CPU CORE POWER	VRON	
LCDVCC	+3.3V	LCD Power	LVDS_VDDEN	
MBAT+	+10V~+17V	MAIN BATTERY		
+5V_S5	+5V		S5_ON	
+3V_S5	+3.3V		S5D	

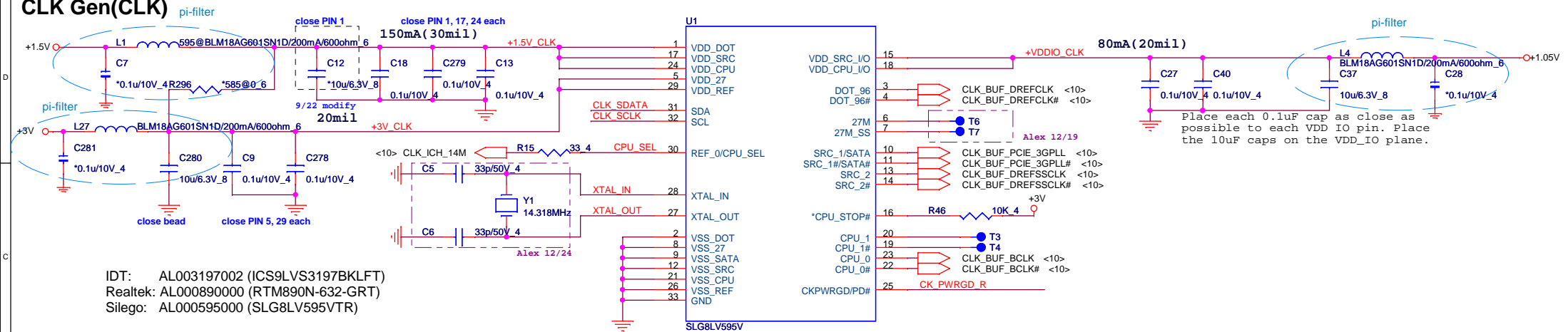
Thermal Follow Chart



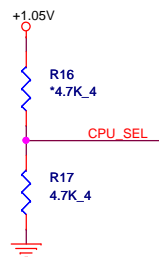
Quanta Computer Inc.
PROJECT : ZQ1(6Layer)

Size	Document Number	Rev
	PWR Status & THRM	1A
Date:	Friday, March 19, 2010	Sheet 2 of 35

CLK Gen(CLK)

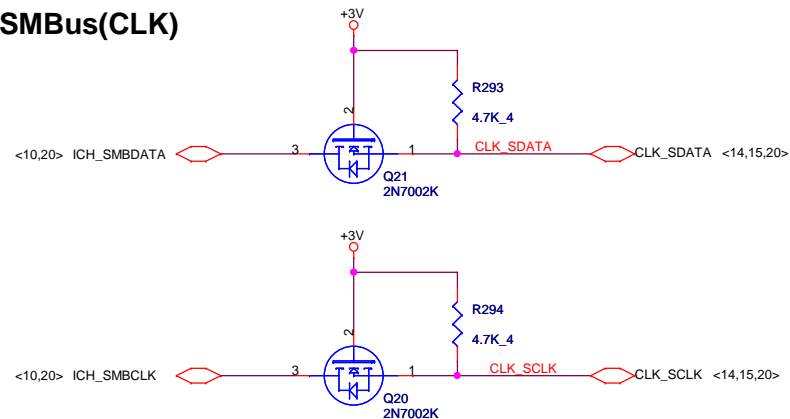


CPU_CLK select(CLK)

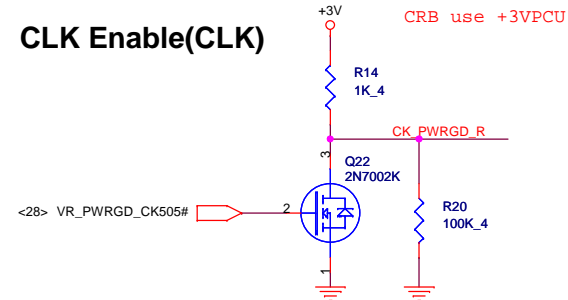


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus(CLK)



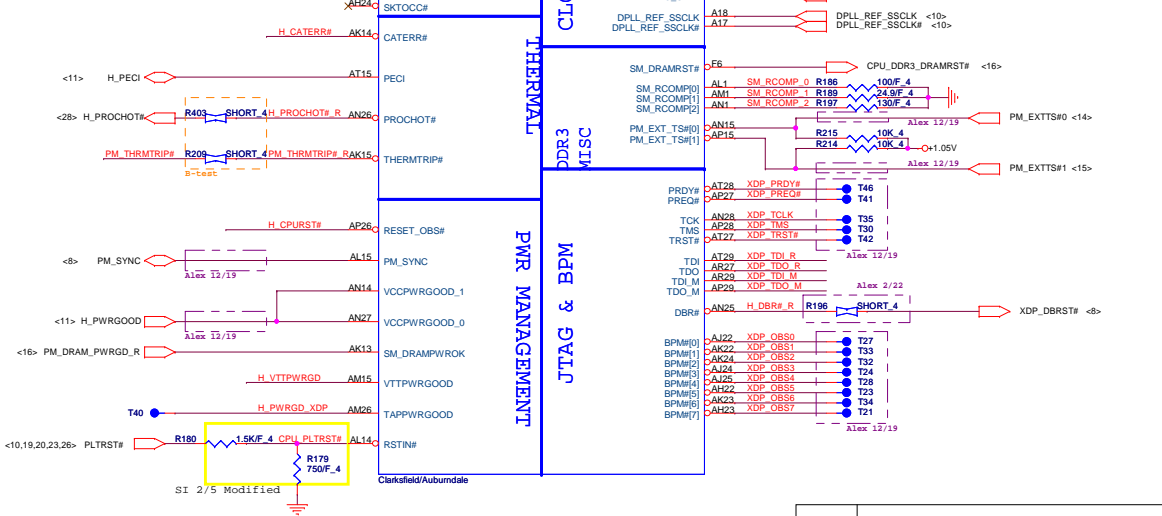
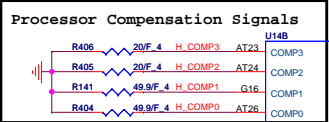
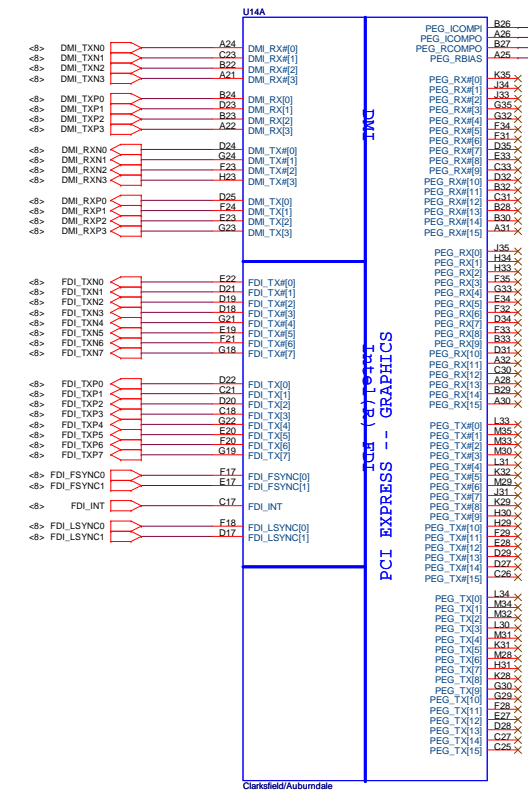
CLK Enable(CLK)

**Quanta Computer Inc.**

PROJECT : ZQ1(6Layer)

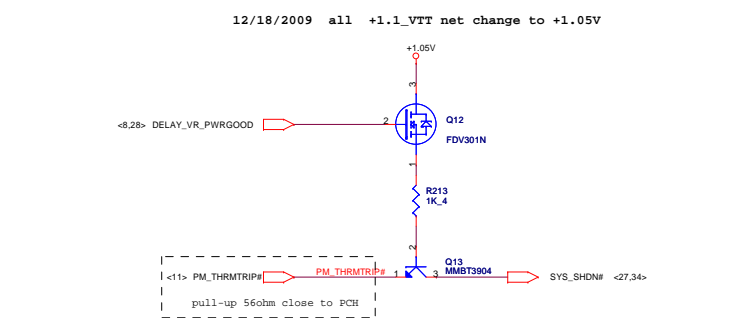
Size	Document Number Clock Generator	Rev 1A
Date:	Friday, March 19, 2010	Sheet 3 of 35

AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

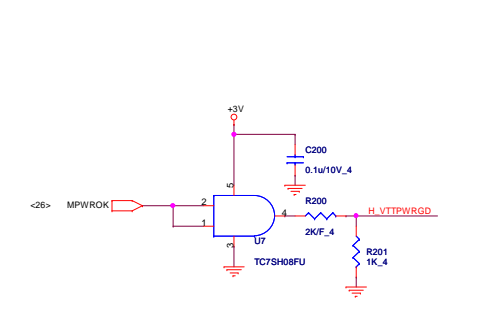


	STD
FOX	DGG*9000024
LTS	DGG*9000022
SUY	
MLX	
Standard: rpga989-aca-zif-069-k01-socket	
Reverse: PZ98927-364R-01F-SOCKET	

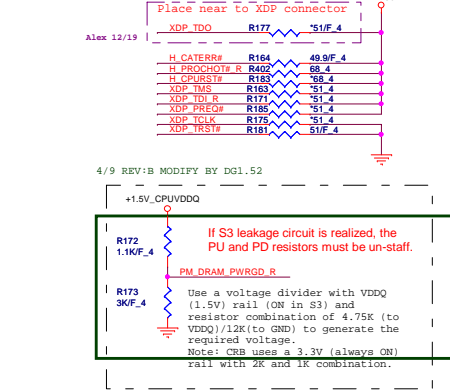
Thermaltrip protect(CPU)



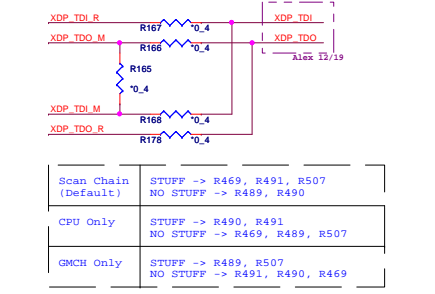
VTT PWR_Good(CPU)




Processor pull-up(CPU)



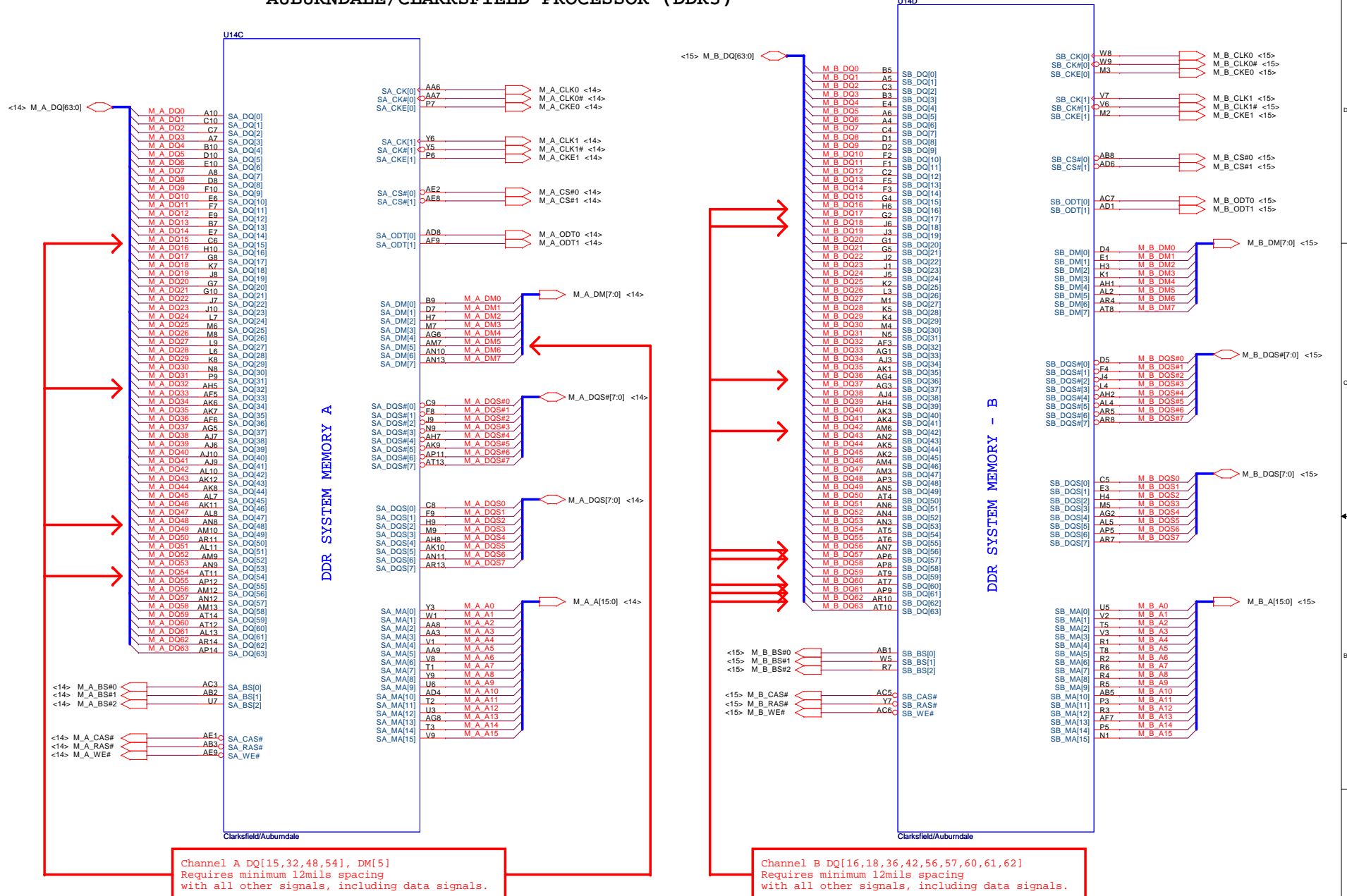
JTAG MAPPING(CPU)





Quanta Computer Inc.
PROJECT : ZQ1(6Layer)

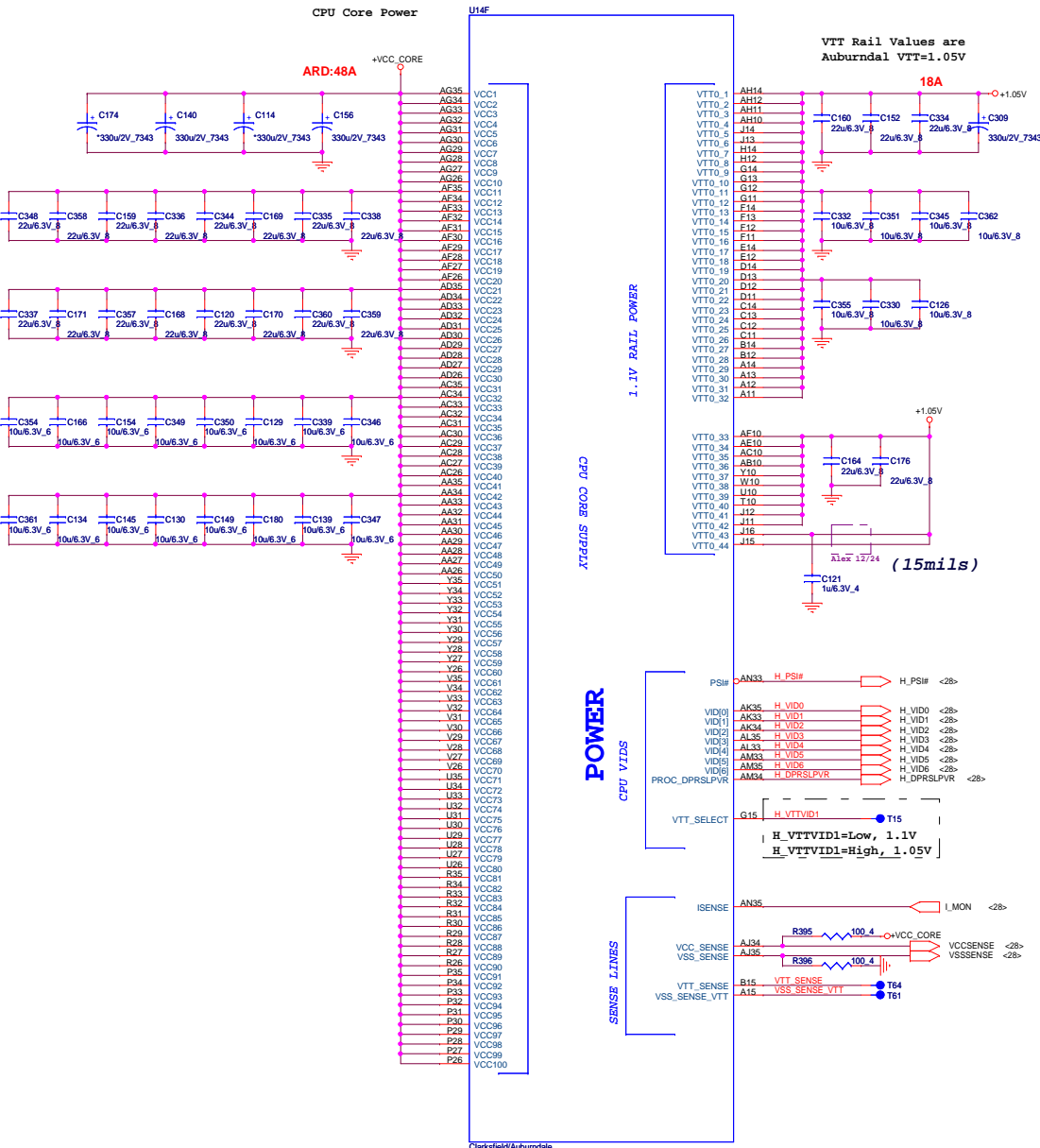
Size	Document Number	Rev
	AUBURND 1/4	1A
Date:	Friday, March 19, 2010	Sheet 4 of 35



Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

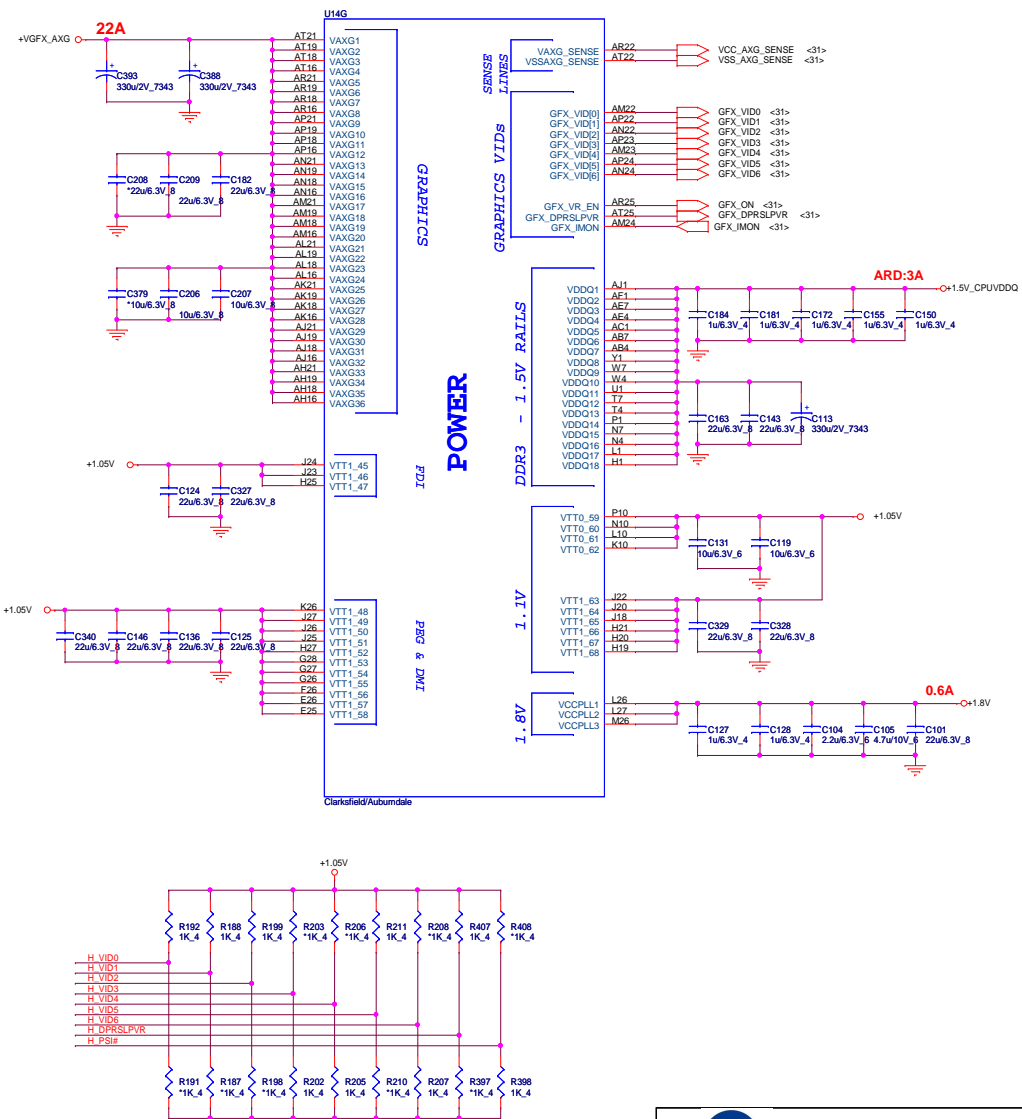
Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

Arrandale_3(CPU)




AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

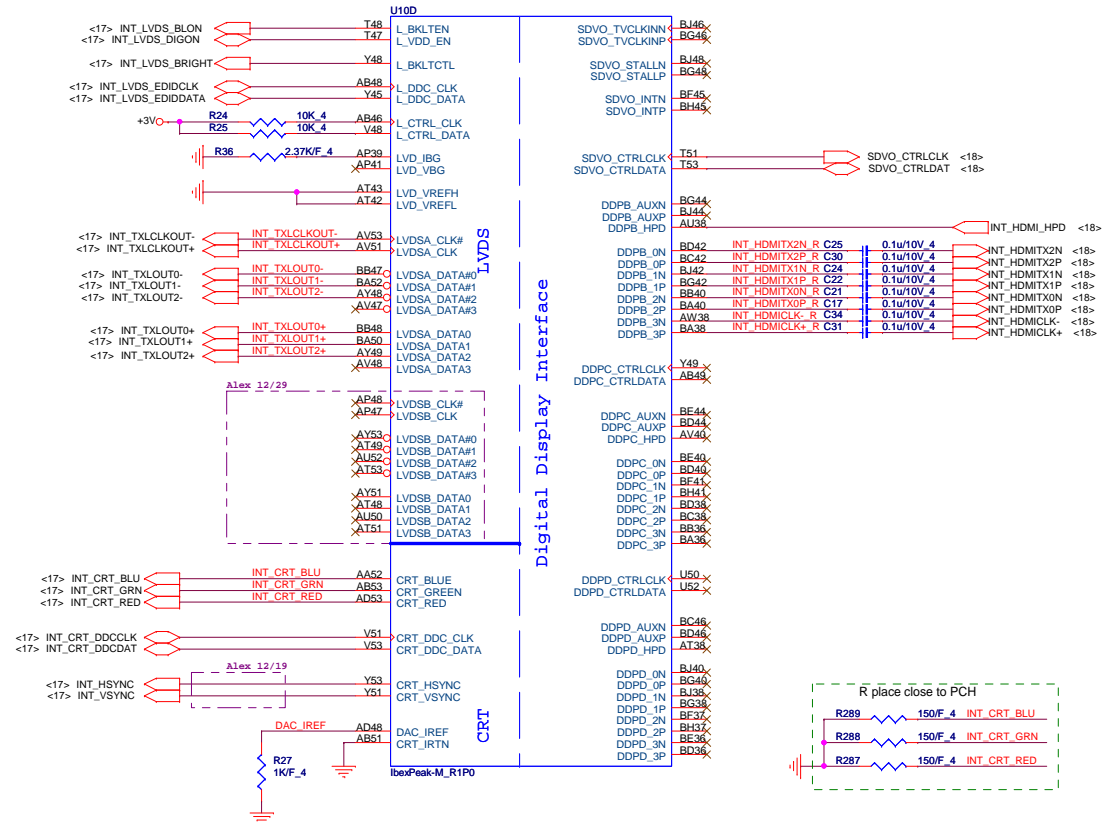
AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



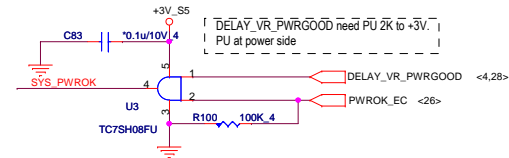
Note:	HFM_VID : Max 1.4V
For Validating IMVP VR R6451 should be STUFF	LFM_VID : Min 0.65V
and R2N1 NO STUFF	

 Quanta Computer Inc. PROJECT : ZQ1 (6Layer)	
Size	Document Number AUBURND 3/4 (PWR)
Date:	Friday, March 19, 2010
Sheet	6 of 35

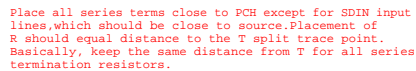
IBEX PEAK-M (LVDS, DDI)



System PWR_OK(CLG)



2

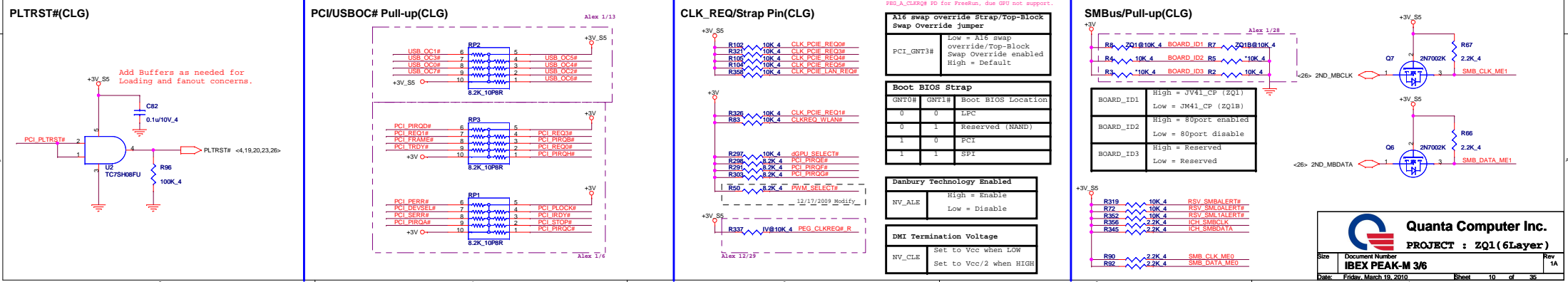


1

1

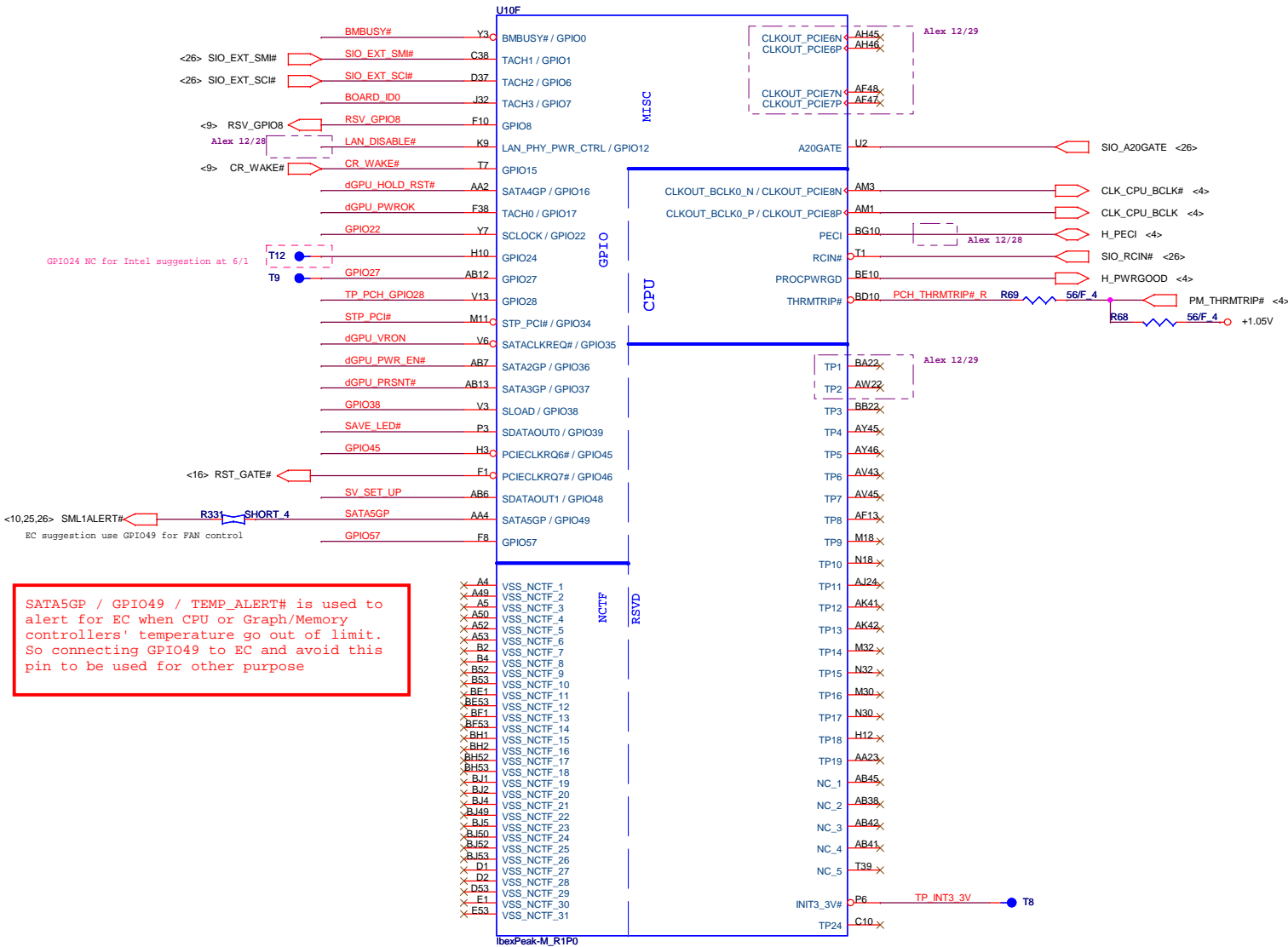
3

IBEX PEAK-M (PCI-E,SMBUS,CLK)

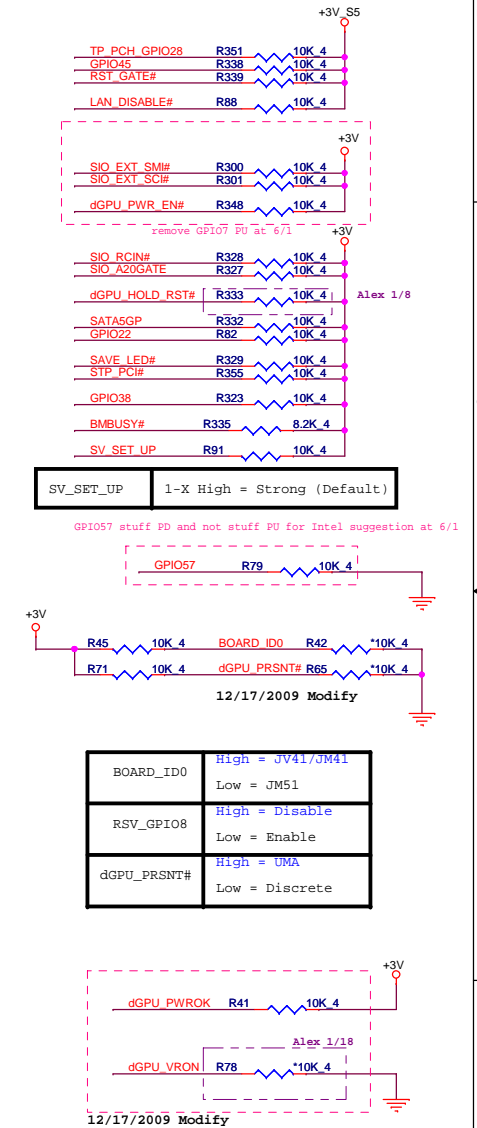


PCH4 (CLG)

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

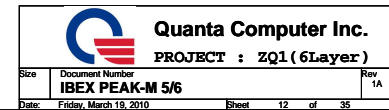


GPIO Pull-up/Pull-down(CLG)

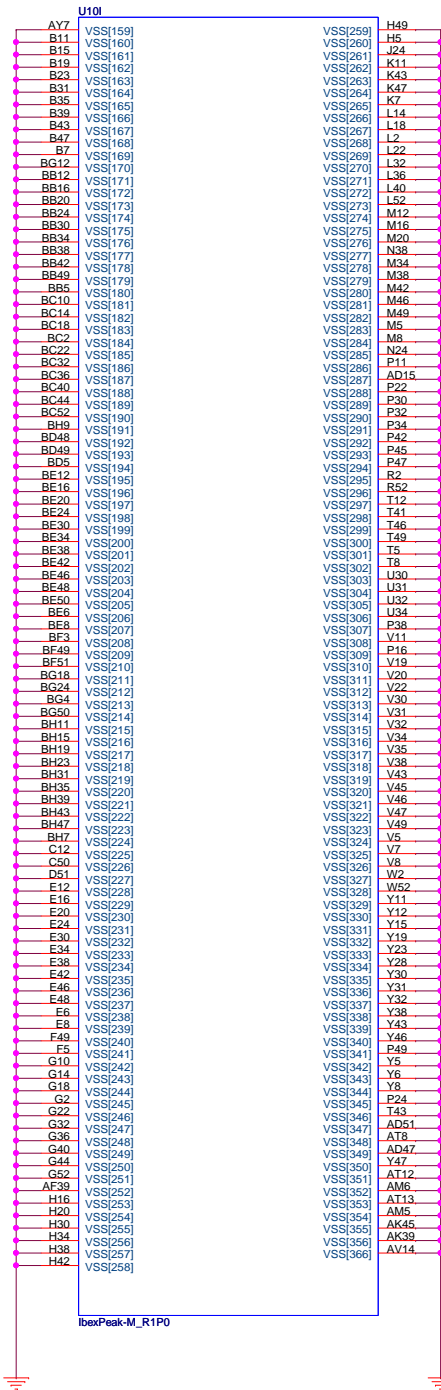
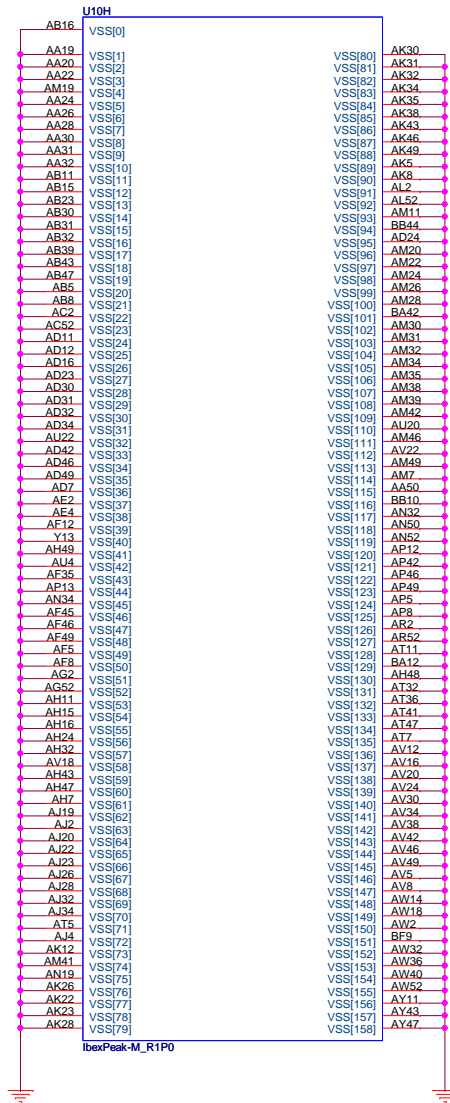


Quanta Computer Inc.
PROJECT : ZQ1 (6Layer)

IBEX PEAK-M (POWER)



IBEX PEAK-M (GND)

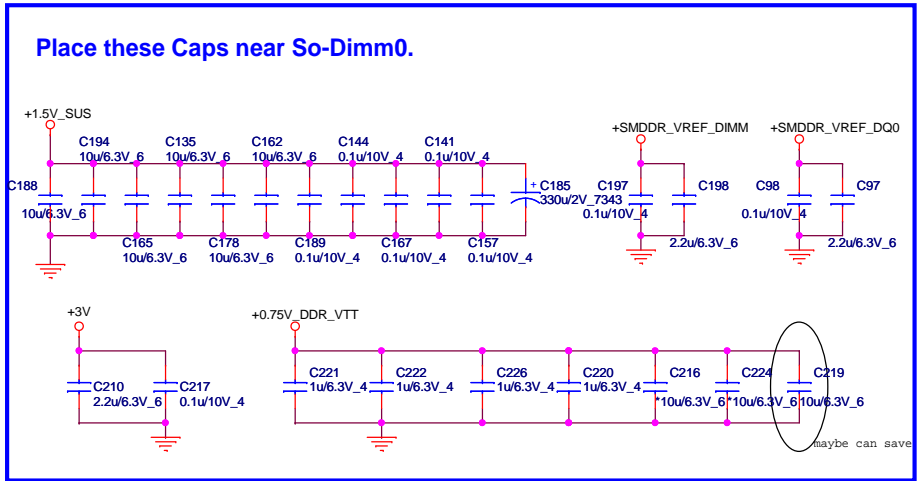
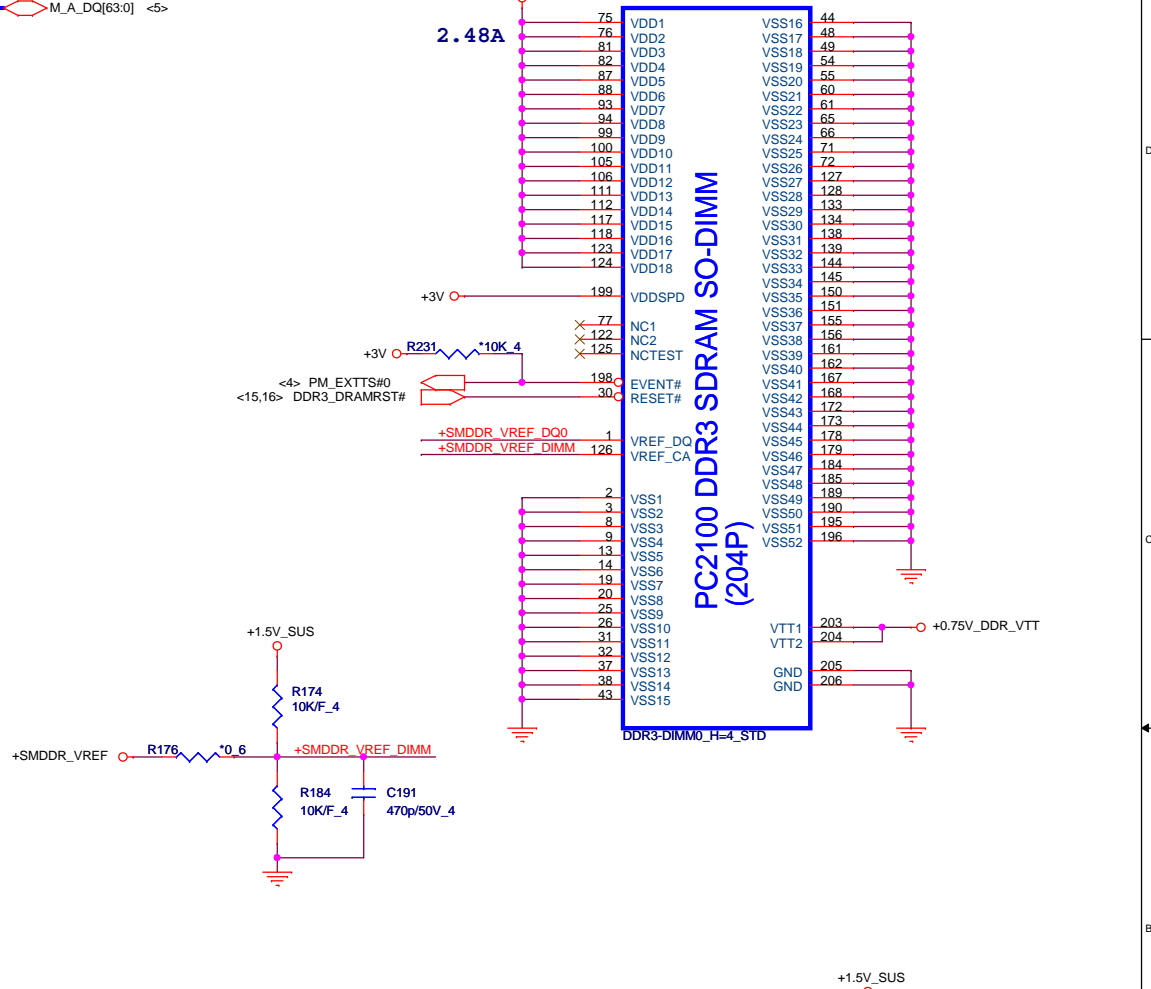
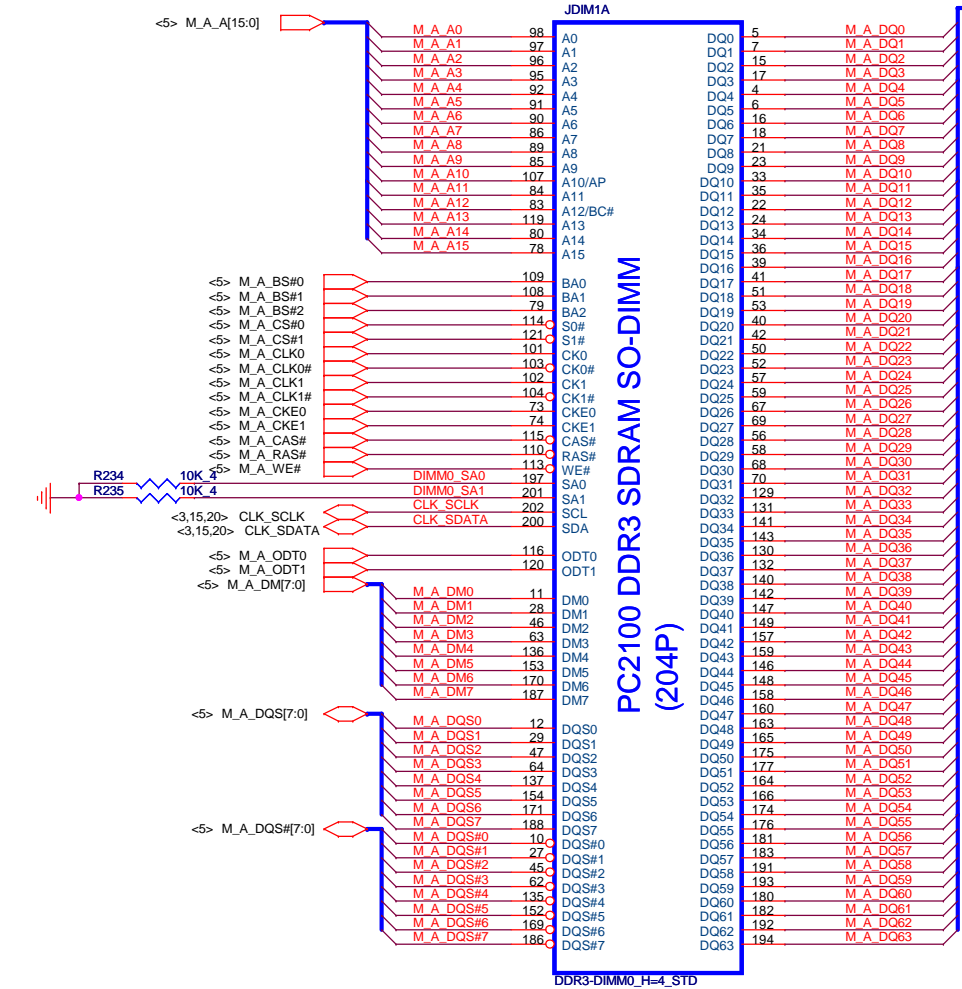


Quanta Computer Inc.

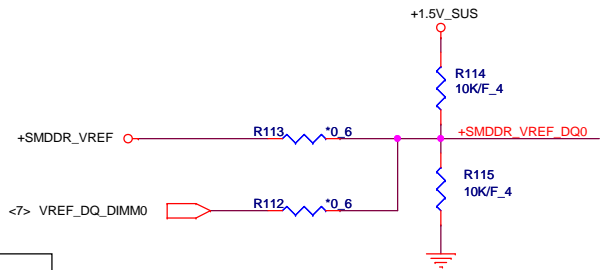
PROJECT : ZQ1 (6Layer)

Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A
Date:	Friday, March 19, 2010	Sheet 13 of 35

DDR_STD (DDR)



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 4H type:DDR-C-2013289-204p		

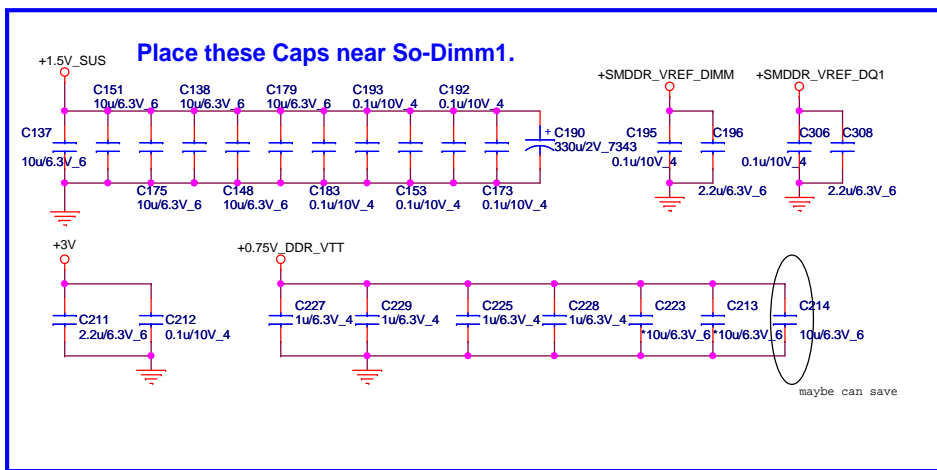
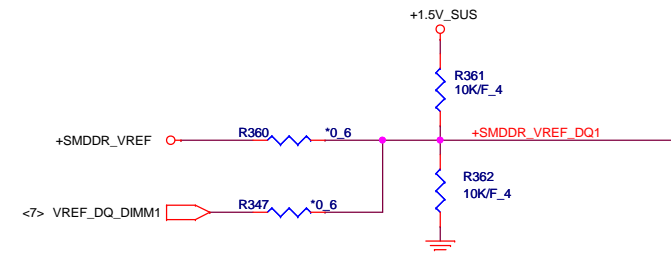
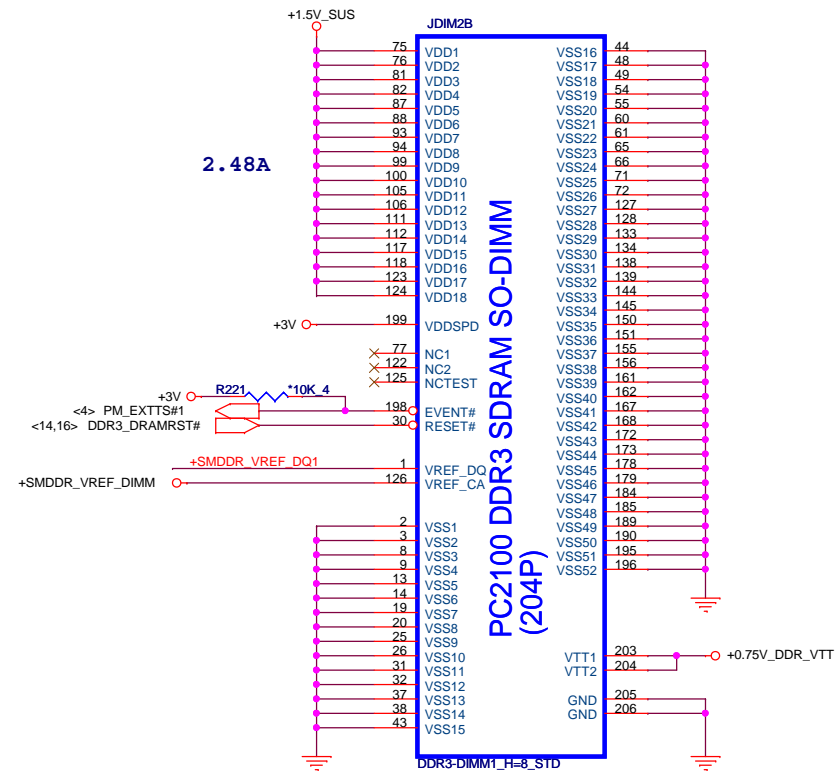
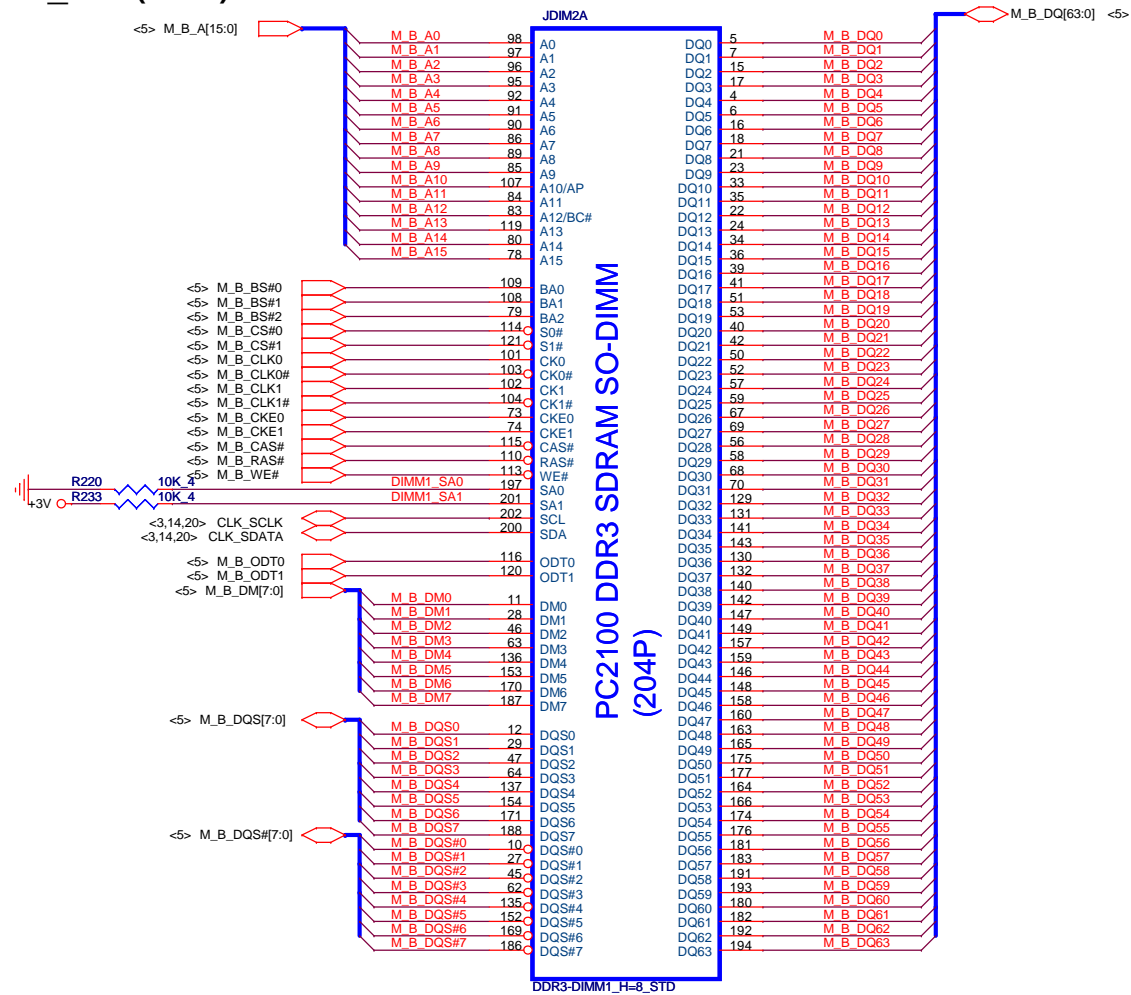


M1:PWR SMDRR_VREF
M1+:voltage divider(Default)
M3:CPU VREF_DQ_DIMM0

Quanta Computer Inc.
PROJECT : ZQ1(6Layer)

Size	Document Number	Rev
	DDRIII SO-DIMM-0	1A
Date: Friday, March 19, 2010	Sheet 14 of 35	

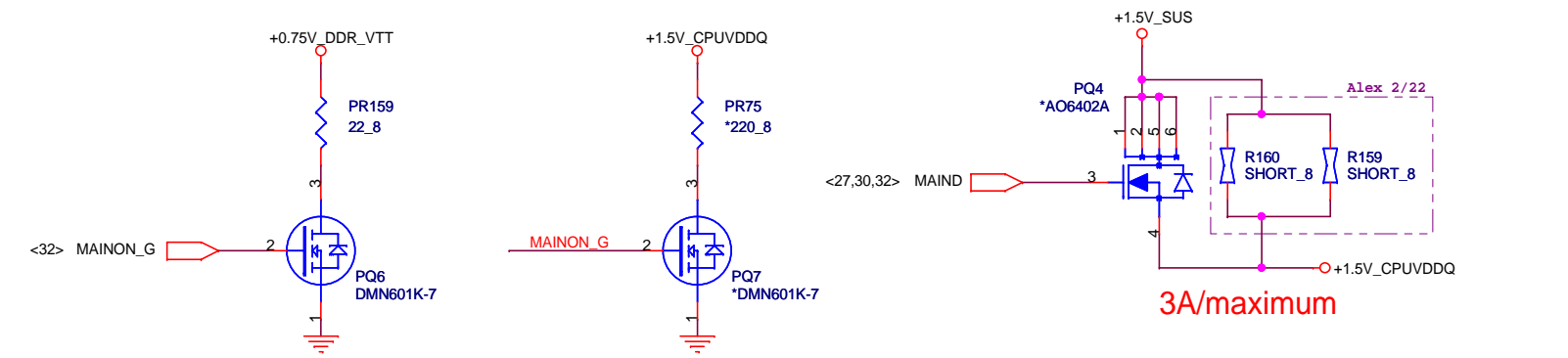
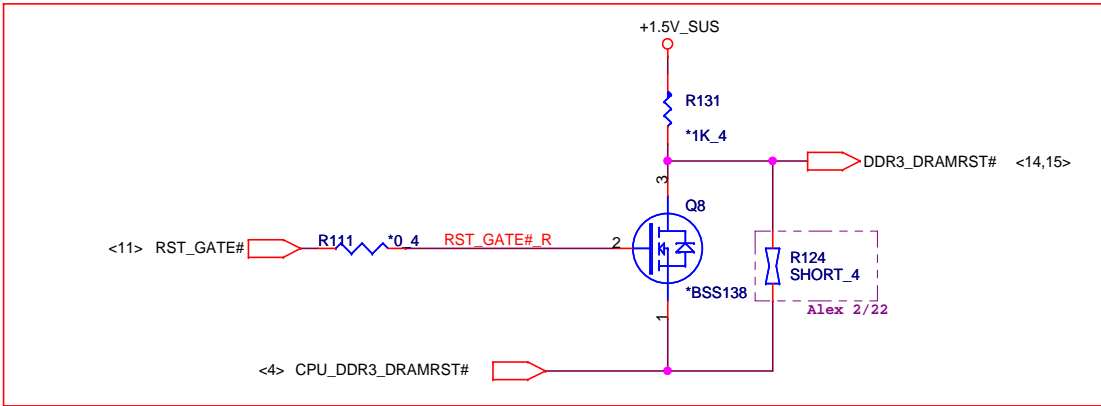
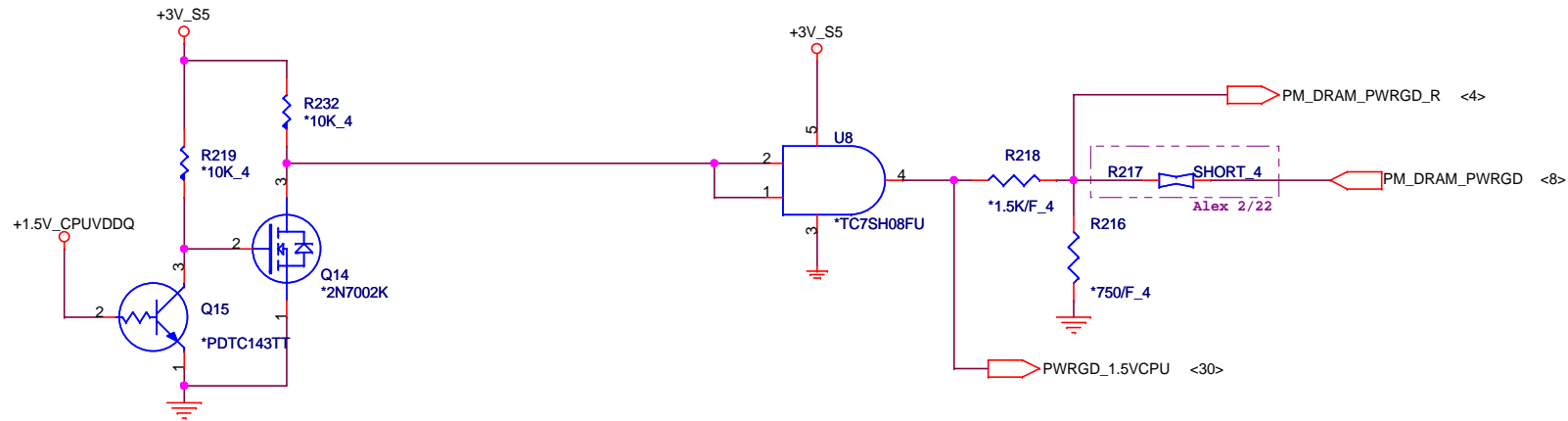
DDR_STD(DDR)



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 8H type:DDR-C-2013310-204p-1		

M1:PWR SMDRR_VREF
M1+:voltage divider(Default)
M3:CPU VREF_DQ_DIMM0

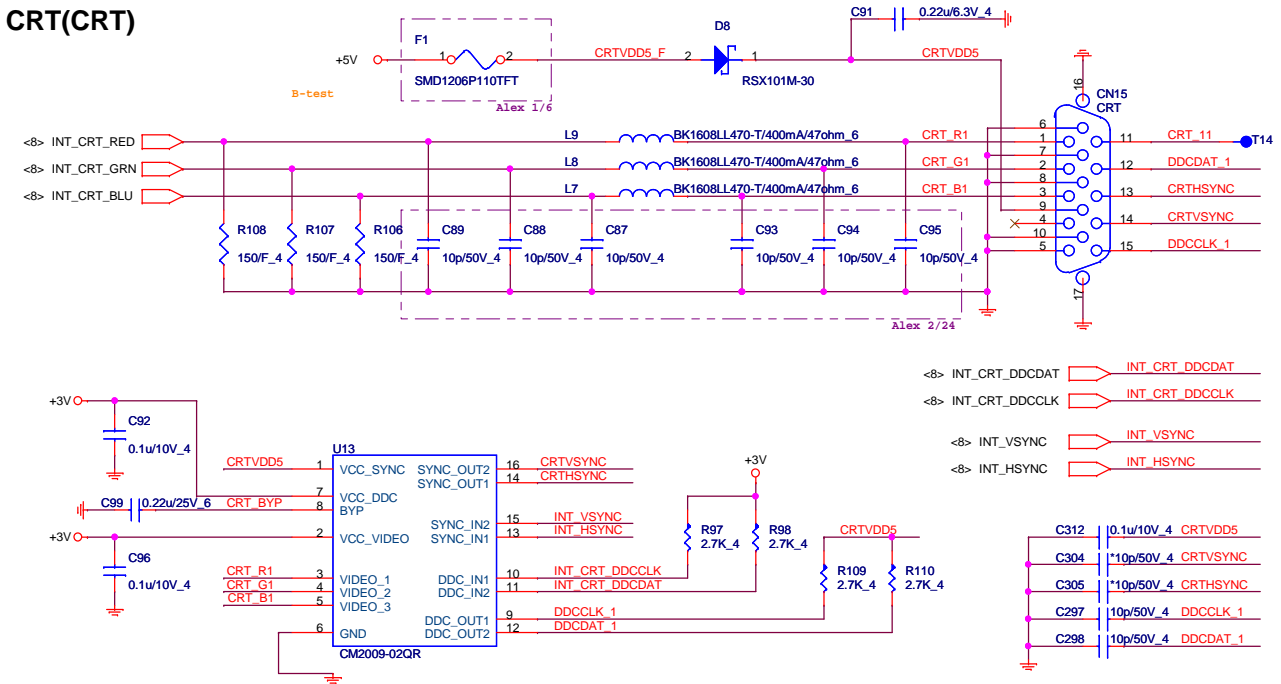
S3 leakage solution(CLG)



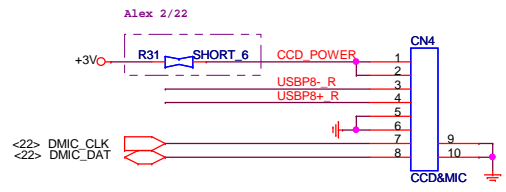
Quanta Computer Inc.
PROJECT : ZQ1(6Layer)

Size	Document Number	Rev
	S3 Power Saving	1A
Date:	Friday, March 19, 2010	Sheet 16 of 35

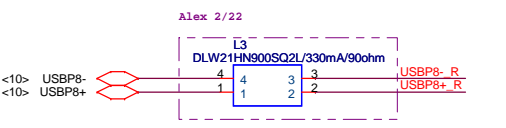
CRT(CRT)



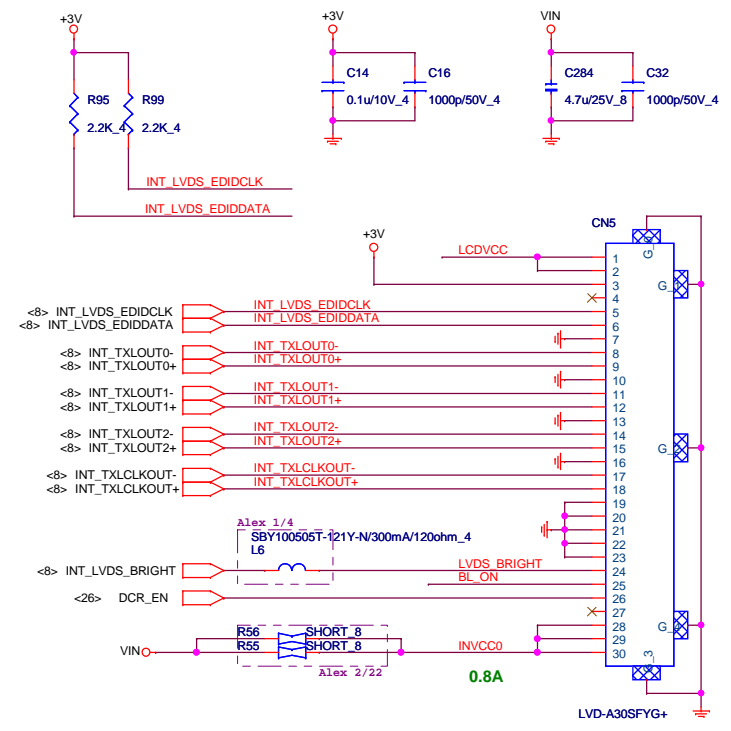
CCD&DMIC Conn.(CCD)



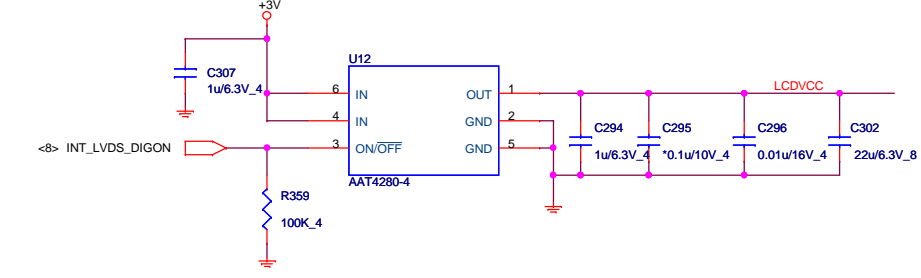
CAMERA Module(CCD)



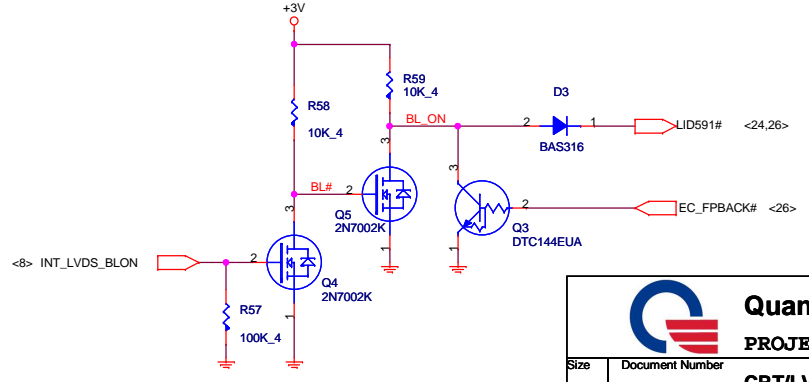
LVDS(LDS)




LCD Power(LDS)



Backlight Control(LDS)





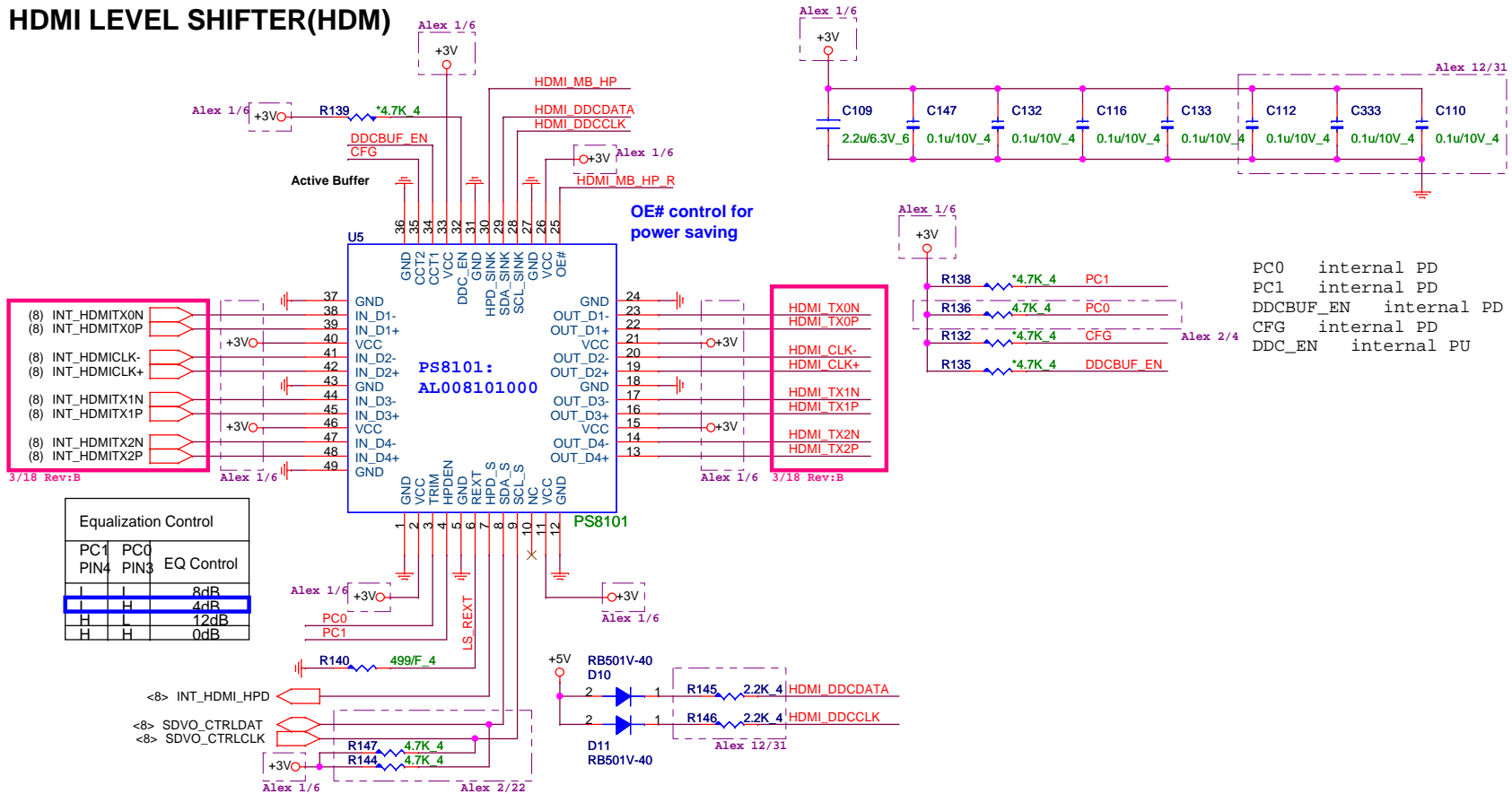
Quanta Computer Inc.

PROJECT : ZQ1(6Layer)

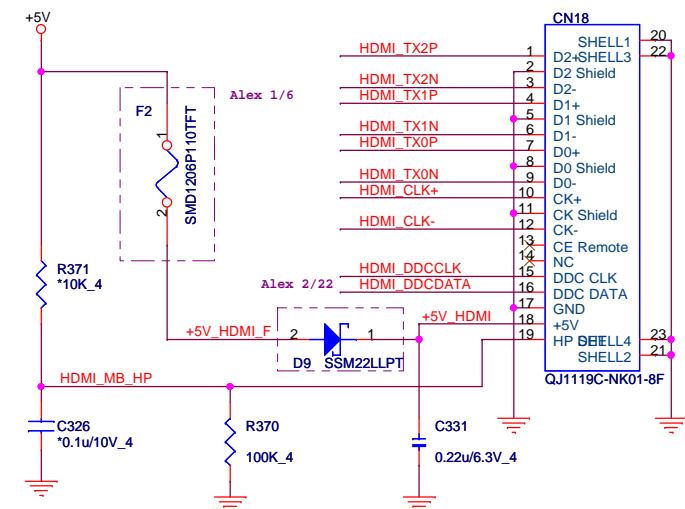
CRT/LVDS

Size	Document Number	Rev 1A
Date: Friday, March 19, 2010		Sheet 17 of 35

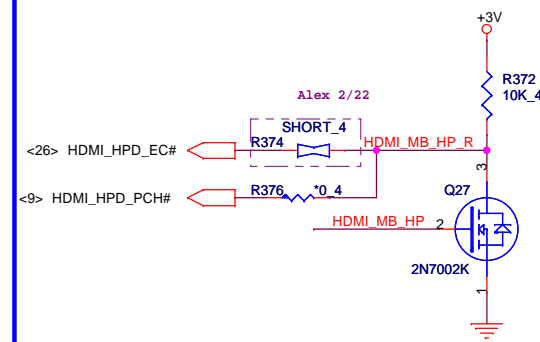
HDMI LEVEL SHIFTER(HDM)



HDMI connector(HDM)

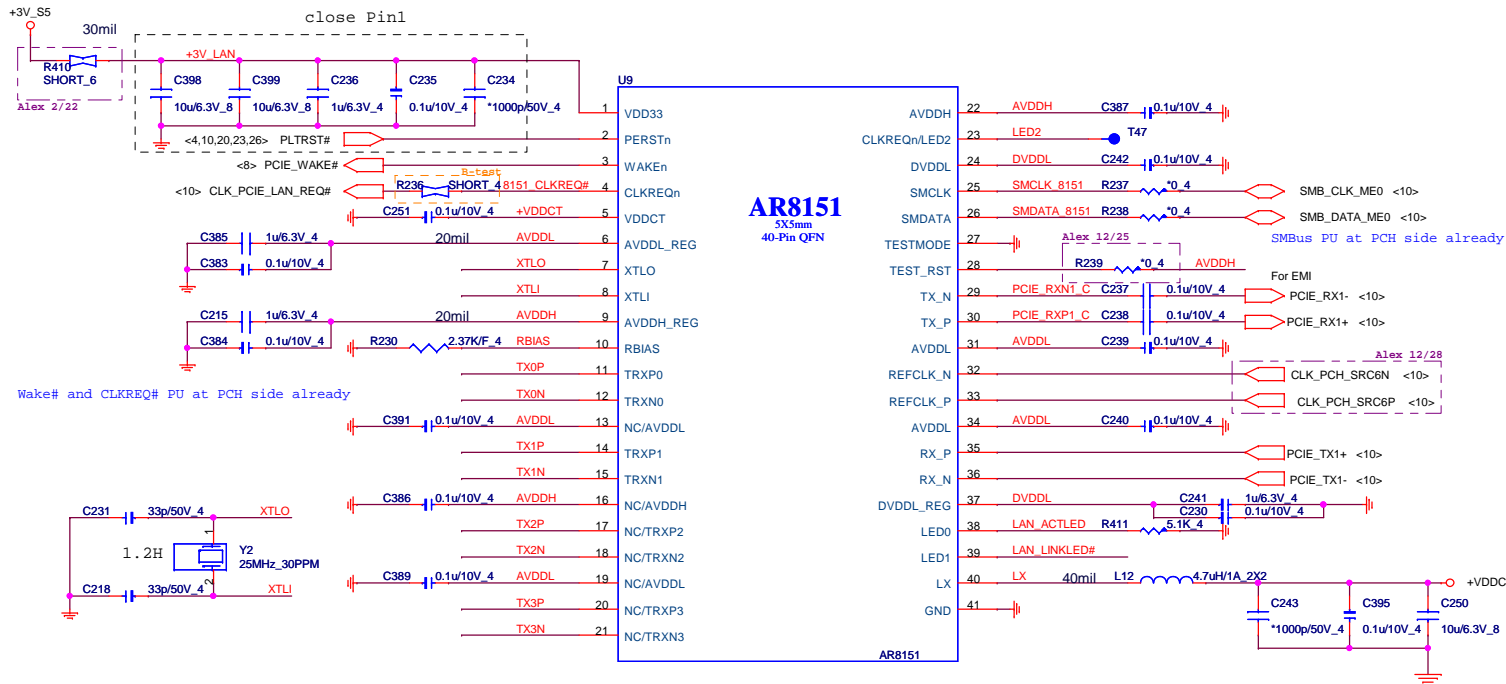


HDMI HPD(HDM)

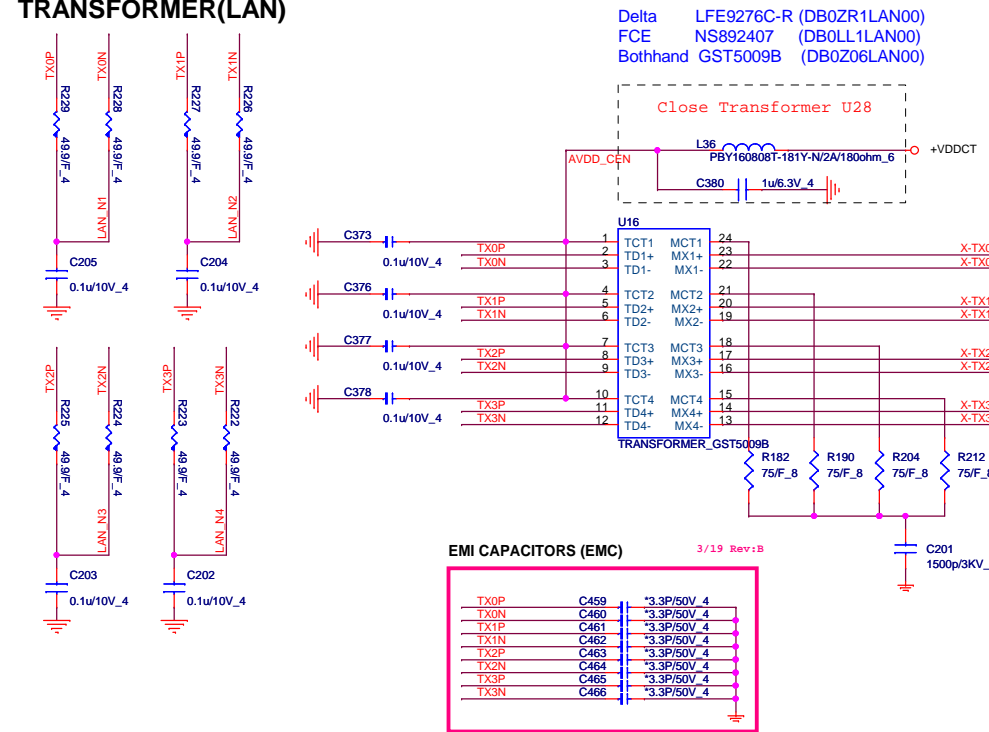


Quanta Computer Inc.
PROJECT : ZQ1(6Layer)

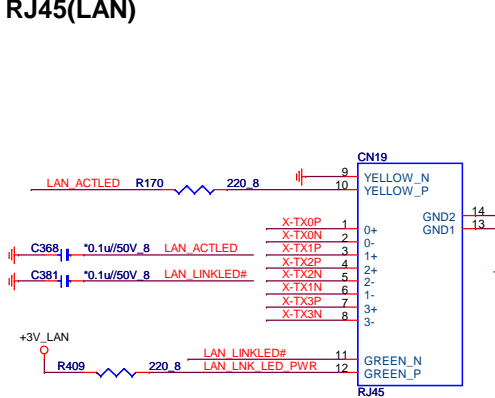
Giga-LAN AR8151(LAN)



TRANSFORMER(LAN)



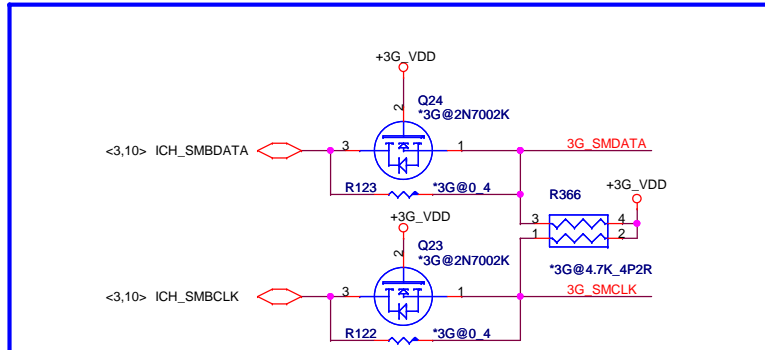
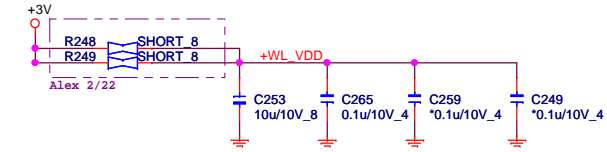
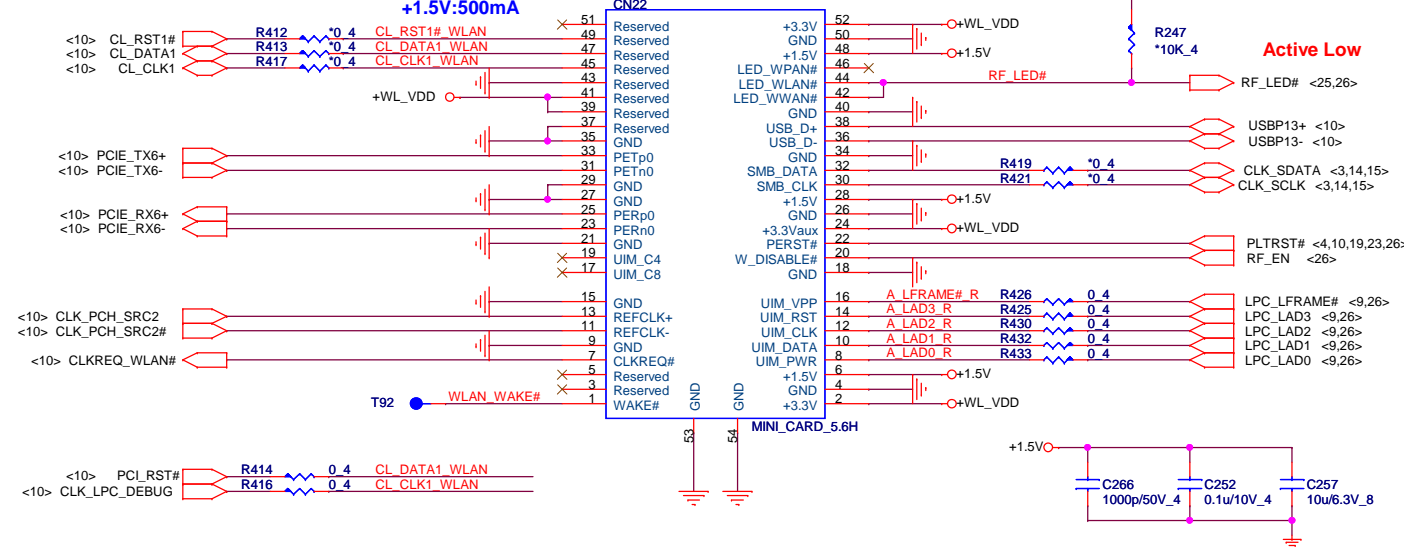
RJ45(LAN)



MINI-CARD WLAN(MPC)

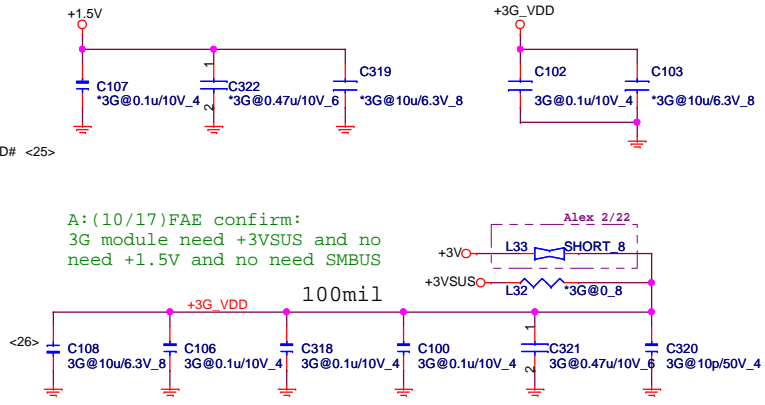
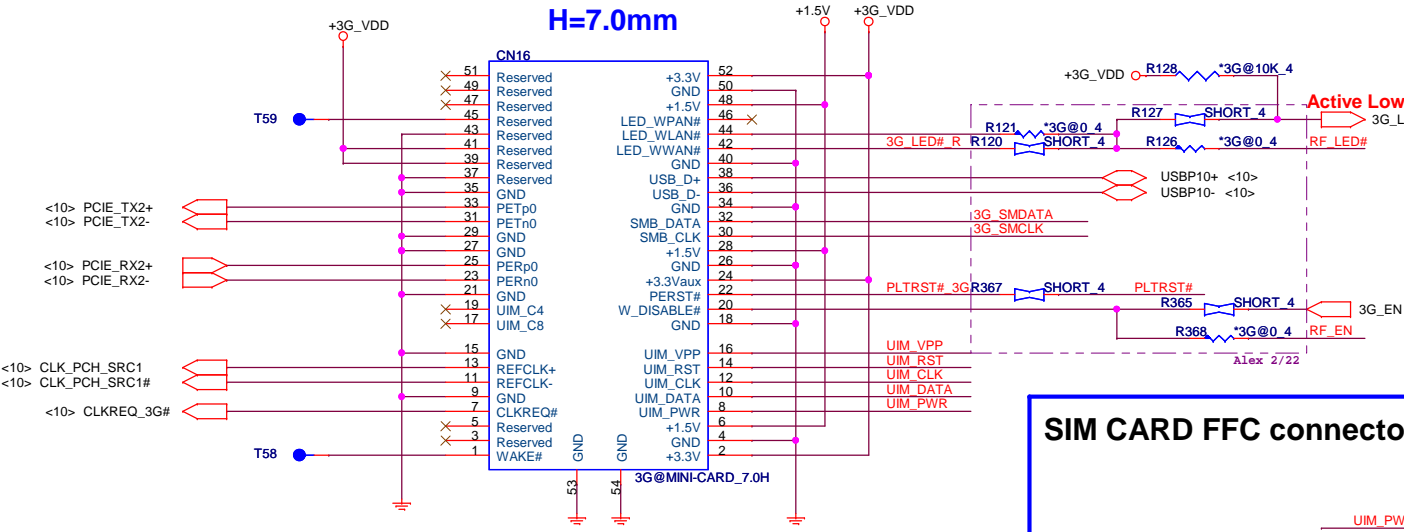
+3.3V: 1000mA
+3.3Vaux: 330mA
+1.5V: 500mA

H=5.6mm

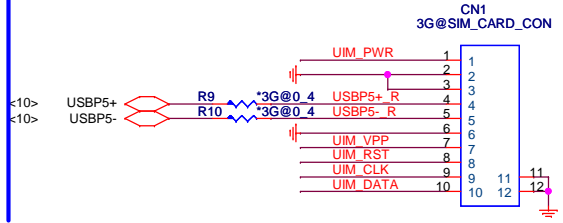



MINI-CARD 3G(MNC)Reserve for JV41-CP

H=7.0mm



SIM CARD FFC connector(RFM)





Quanta Computer Inc.
PROJECT : ZQ1 (6Layer)

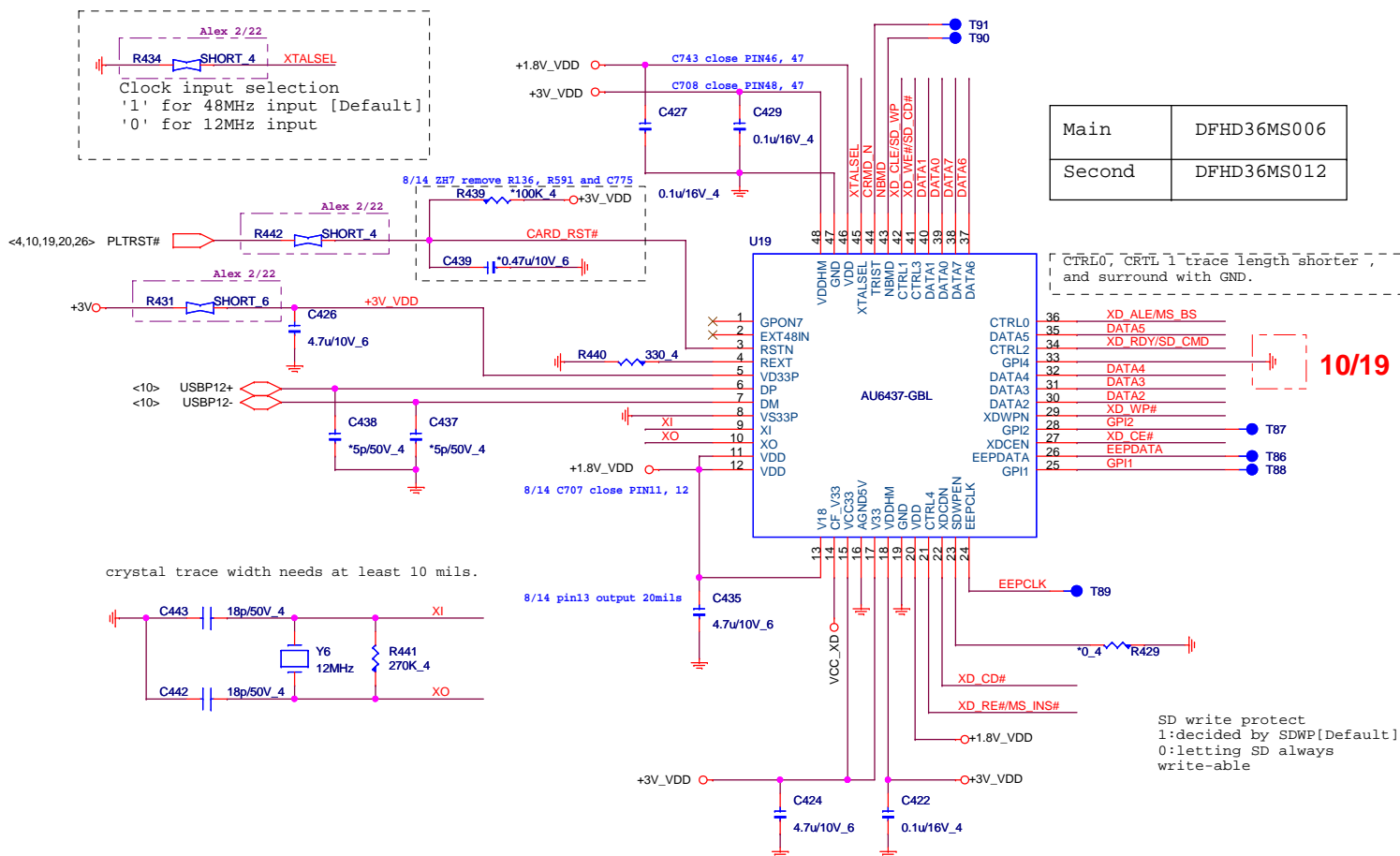
Size	Document Number	Rev
	Mini-Card/WL/3G/SIM	1A
Date:	Friday, March 19, 2010	Sheet 20 of 35

A

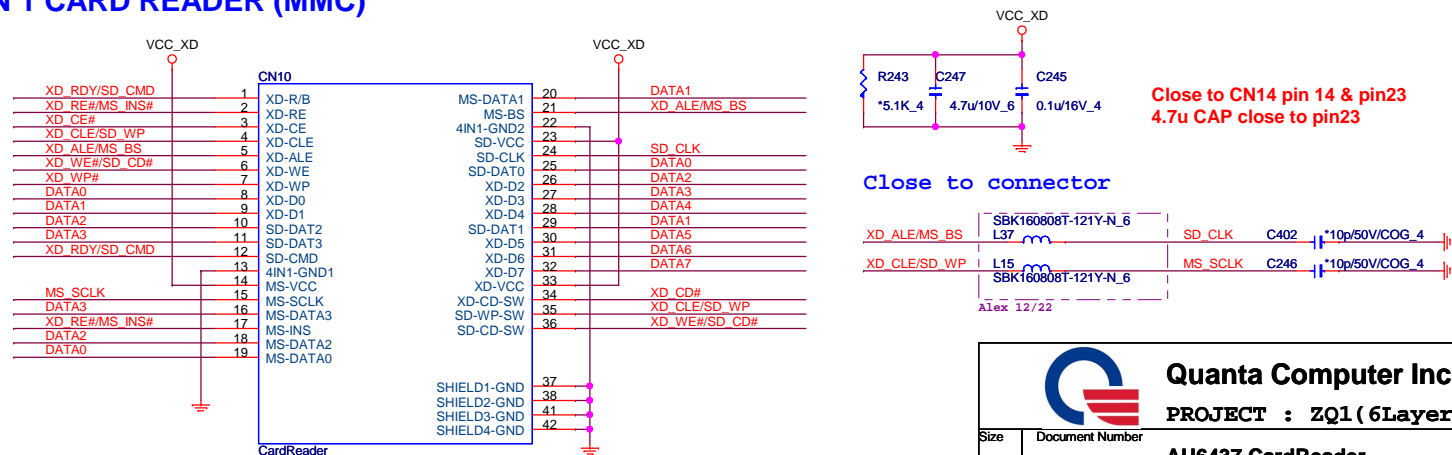


Date: Friday, March 19, 2010 Sheet 21 of 35

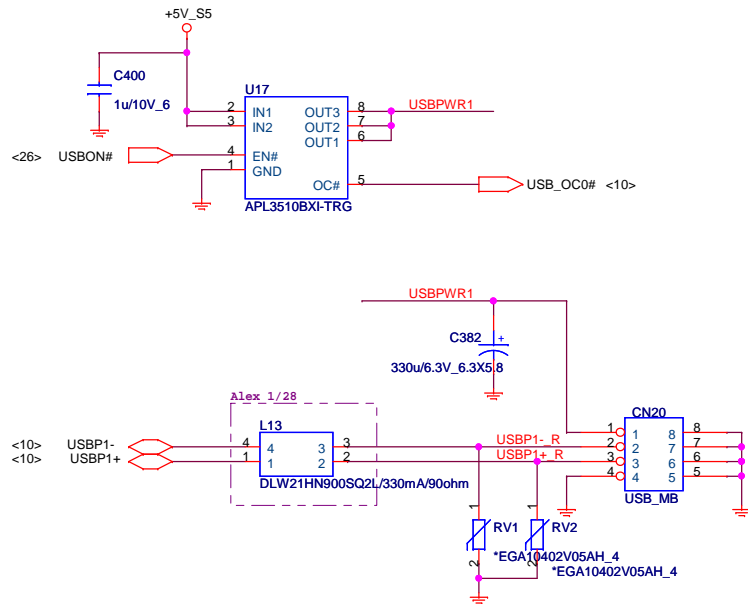
CARD READER Controller



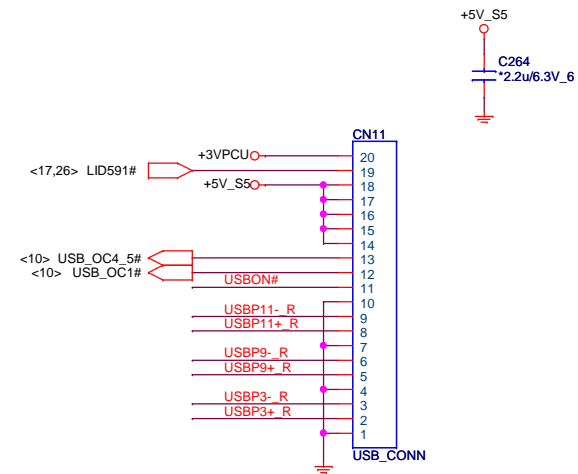
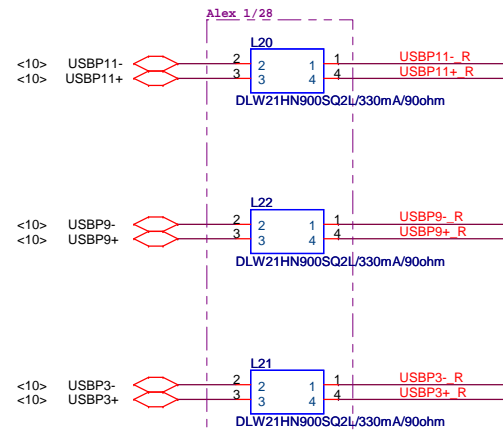
4 IN 1 CARD READER (MMC)



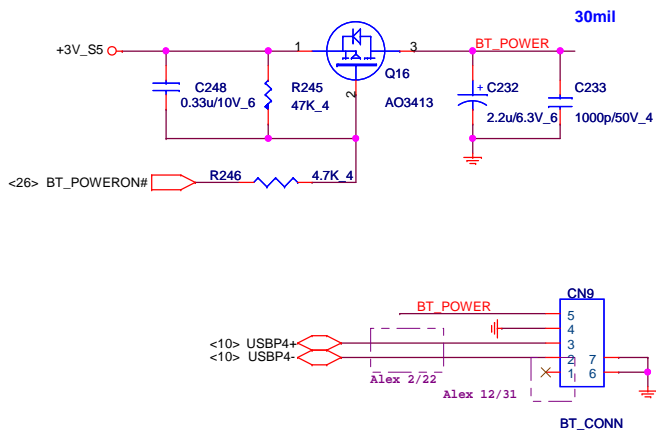
USB PORT(USB)



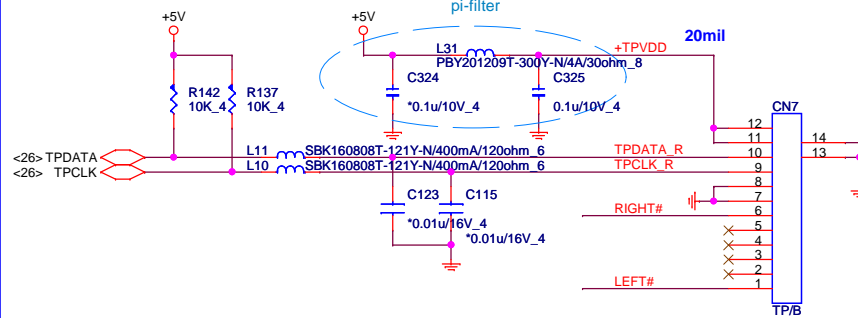
USB BOARD CONN(USB)



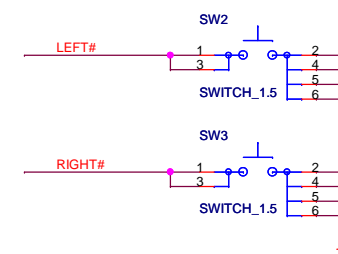
BLUETOOTH CONN(BTM)



TOUCHPAD BOARD CONN(TPD)



TP SWITCH(UIF)

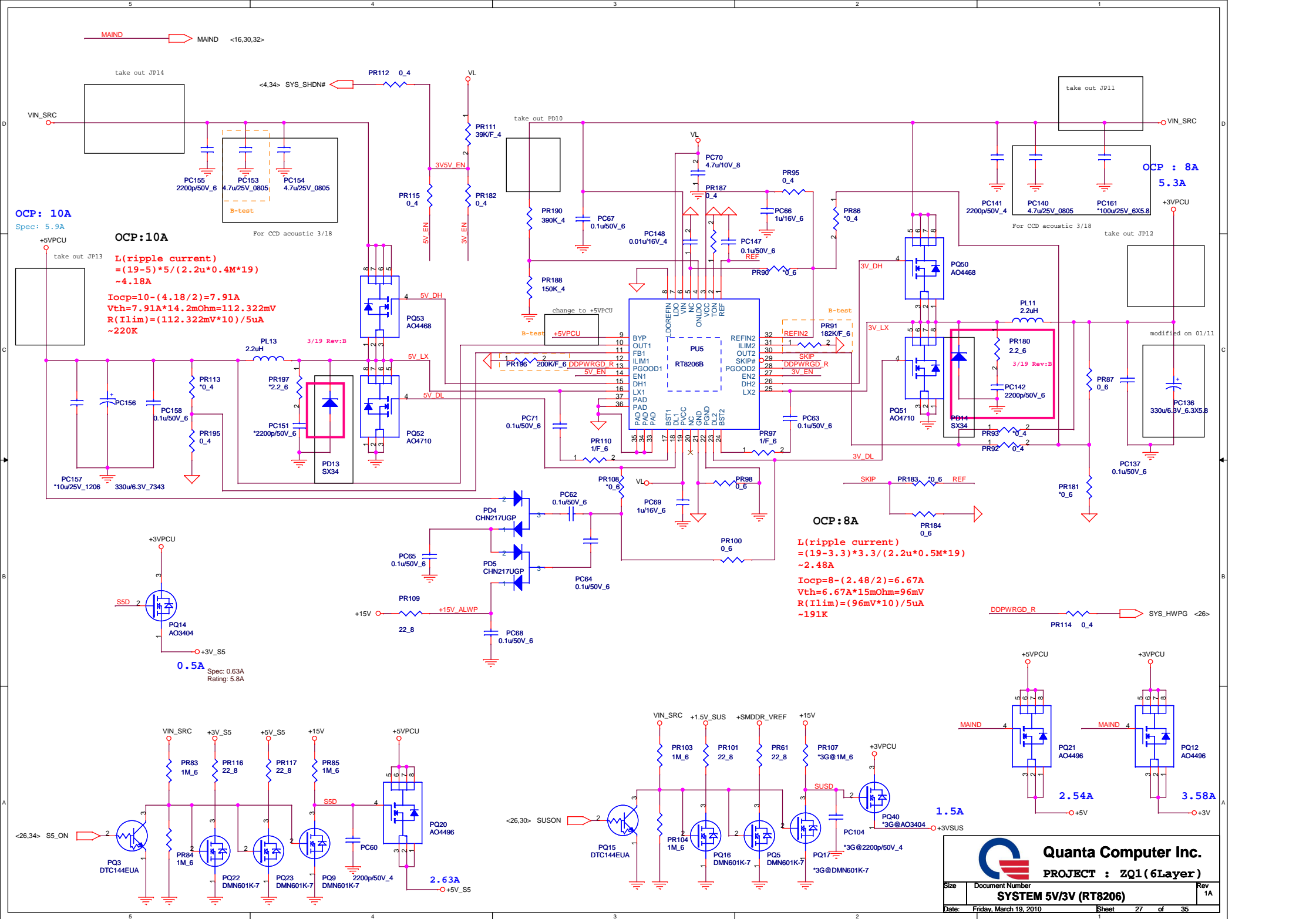


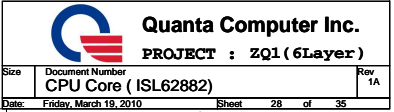
Quanta Computer Inc.

PROJECT : ZQ1(6Layer)

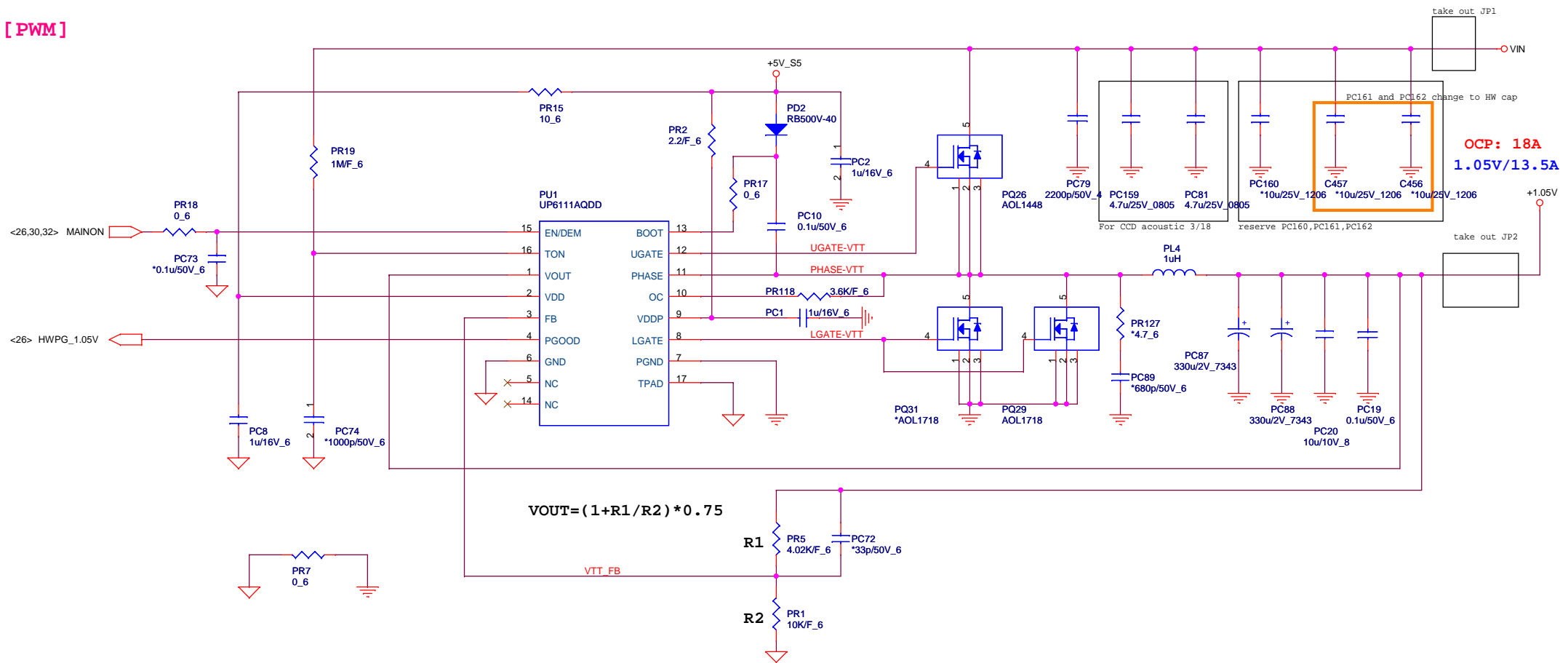
Size	Document Number	Rev
	eSATA/USB	1A
Date:	Friday, March 19, 2010	Sheet 24 of 35

Date: Friday, March 19, 2010 Sheet 24 of 35





[PWM]



$$TON = 3.85p \cdot RTON \cdot Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin \cdot TON)$$

$$TON = 3.85p \cdot 1M \cdot 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

AOL1718 Rdson=3~4.3mOhm

$$L(ripple\ current) = (19 - 1.05) \cdot 1.05 / (1u \cdot 272k \cdot 19) \sim 3.64A$$

$$4.3m \cdot 18 = RILIM \cdot 20uA$$

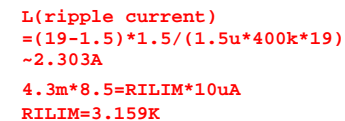
$$RILIM = 3.87K \text{ --- } 3.92K$$

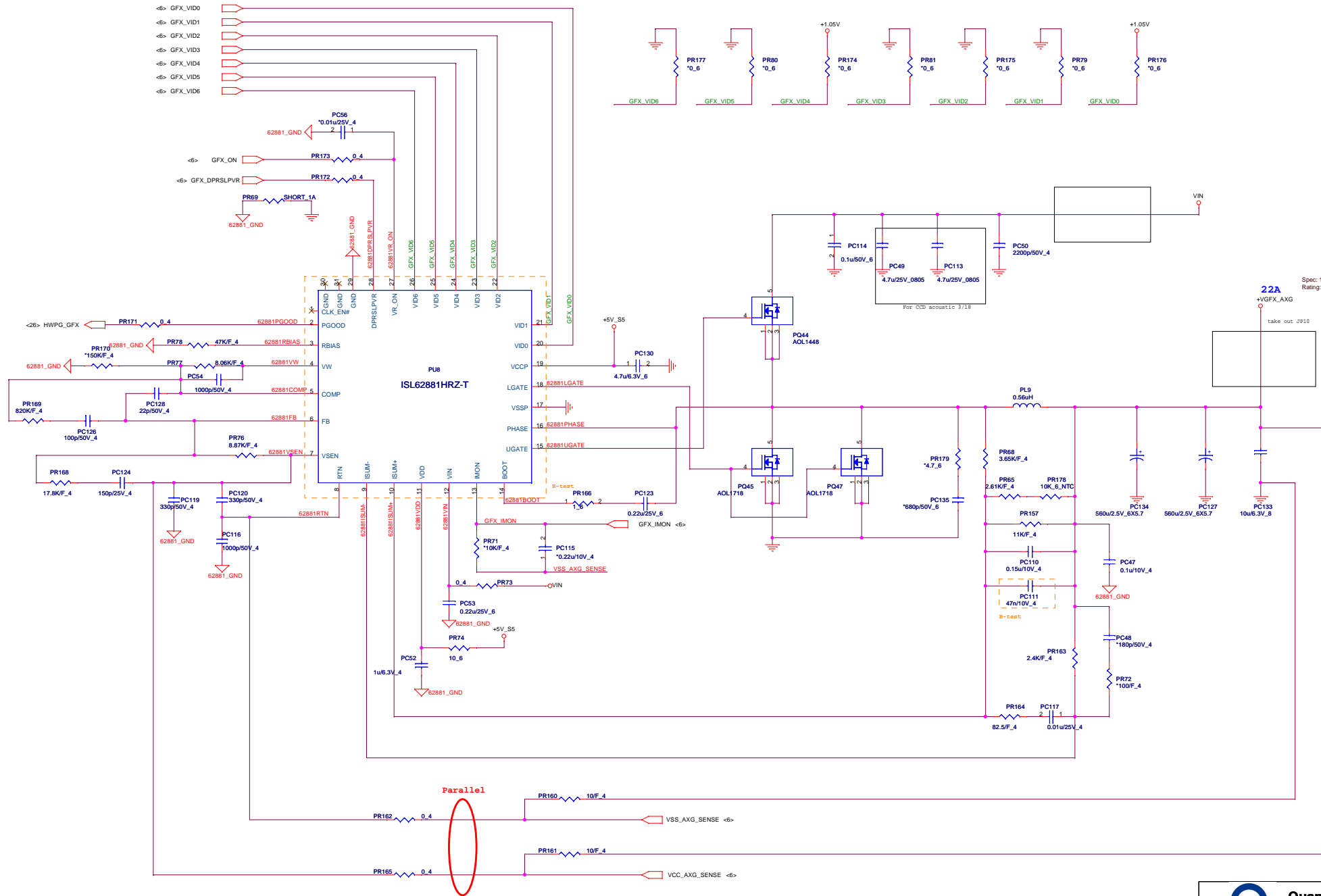


Quanta Computer Inc.

PROJECT : ZQ1 (6Layer)

Size	Document Number	Rev
	+1.05V (UP6111A)	1A
Date:	Friday, March 19, 2010	Sheet 29 of 35

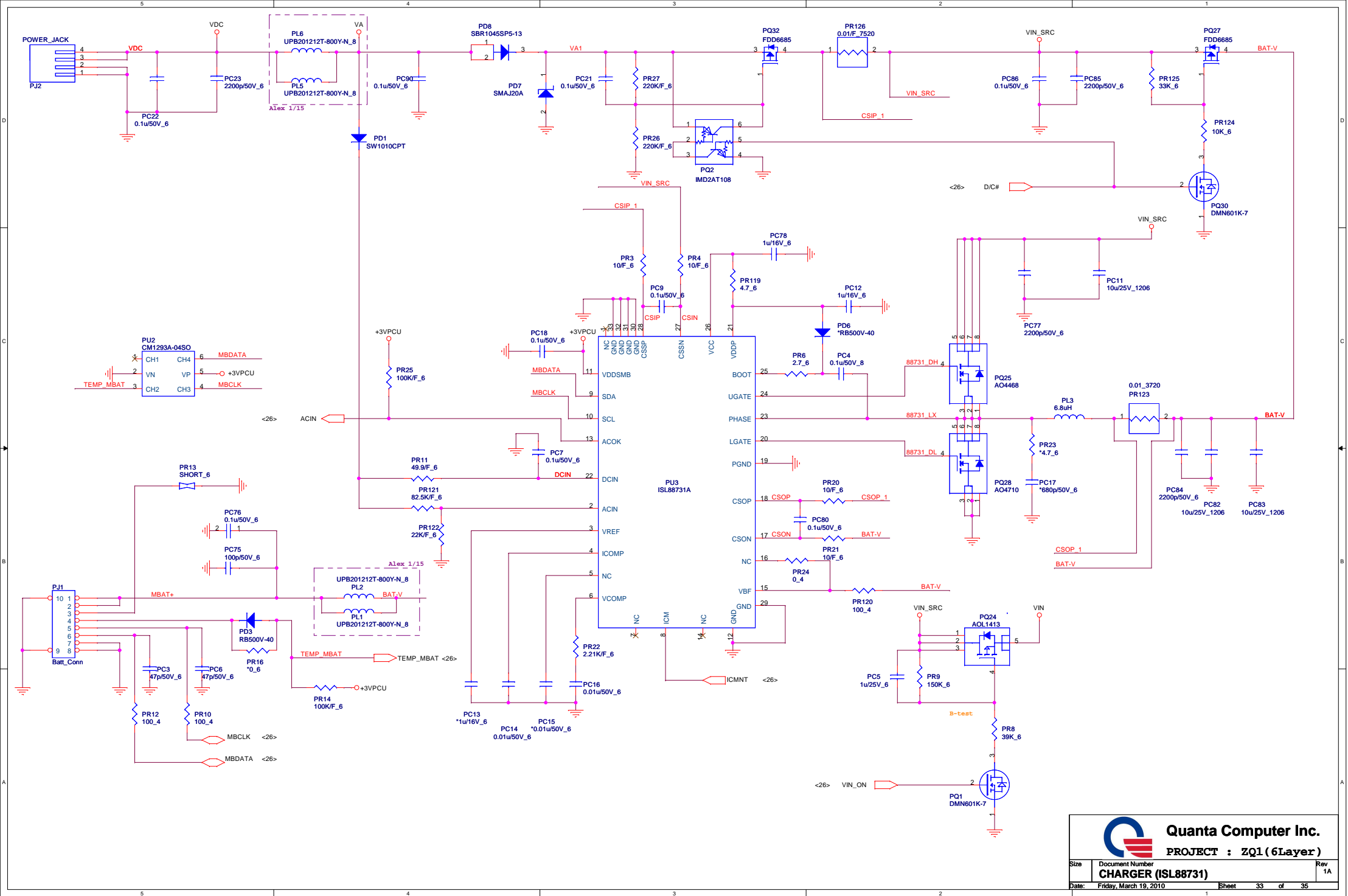





DRC=2.7~3mOhm/2

Load Line=7mV/A
3m*6.168=0.925m
0.925m/2.49K=371p
371p*2*8.87K=6.58m
OCP
20u/2*2.42K=24.2m
24.2m/0.6168=36.64m
36.64m/3m=12.21A

1.Level 1 Environment-related Substances should NEVER be used.
2.Purchase Ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



Model		REV	CHANGE LIST			MODEL	ZQ1U	
							FROM	To
ZQ1(6 Layer) MB	1A	ZQ1(6Layer) Schematic release 1/20 2010						
	2A	<p>3/4 Page 25, Stuff D1 for Non-Green ADP. Stuff R573 for Green ADP</p> <p>3/9 Page 26, D22,D23 change diode P/N: BC101M30200 for Green Adapter</p> <p>3/16 Page 12, Add C458 (22uF/6.3V) P/N : CH6221M9A07 for CRT Monitor issue</p> <p>3/17 Page 12, Remove VCCDAC Power CAP C15 (0.01uF)</p> <p>3/17 Page 26, Remove D22,R556 , D23 change P/N BCBAT54CZ04</p> <p>3/18 PC132, PC153, PC154, PC140, PC42, PC109, PC38, PC39, PC159, PC81, PC49, PC113 changed to 4.7u 0805 P/N CH5474KEA06</p> <p>3/18 Reserve PC161 and PC162</p> <p>3/18 PC129 changed part number to CH733RY8802</p> <p>3/18 Page 26, Reserve R267,R244,Q45 for Green Adapter</p> <p>3/19 Page 19, Reserve C459,C460,C461,C462,C463,C464,C465,C466 (3.3pF/50V P/N: CH-3306TB04) by EMI</p> <p>3/19 Page 25, Add C15 (1000pF/50V P/N: CH21006JB10) by EMI</p> <p>3/19 Page 25, Stuff EC1,EC1(22uF/25V P/N: CH411006K911) by EMI</p> <p>3/19 Page 25, Modify RV3 Footprint name to SLP2-1X0, 6-65-2P (Reserve ESD part)</p> <p>3/19 Page 26, Stuff C363 (2200p/50V P/N: CH22206KB16) by EMI</p> <p>3/19 Page 27, Stuff PR180 (2.2 ohm) ,PC142 (2200p/50V P/N: CH22206KB16) by EMI</p> <p>3/19 Page 27, Add PD13,PD14</p>						
DOC NO.		PROJECT MODEL : ZQ1(6Layer)		APPROVED BY:	DATE: 2010/01/20	<div> Quanta Computer Inc. PROJECT : ZQ1(6Layer) Change list</div>		
PART NUMBER:		31ZQ1MB00XX		DRAWING BY:	Alex Lin			
						Rev 1A		