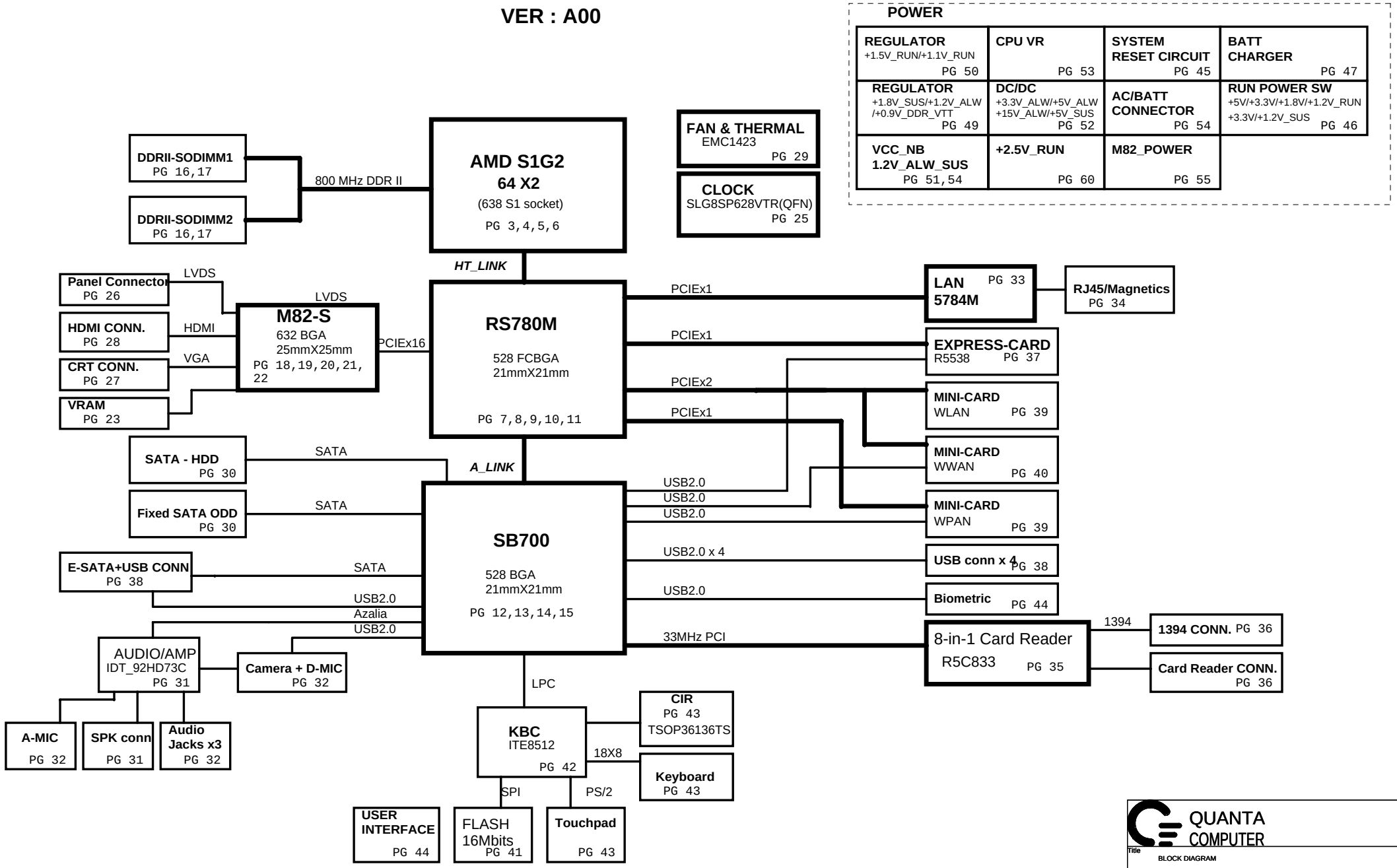
Hepburn AMD Discrete GFX

VER : A00



QUANTA COMPUTER

Title	BLOCK DIAGRAM	
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Pg#	Description
1	Schematic Block Diagram
2	Index/Power States and USB/PCI/PCIe map
3-6	CPU page
7-11	RS780M page
12-15	SB700 page
16-17	DDRII SO-DIMM(200P)
18-23	M82-S
24	LCD/CRT HYBRID
25	Clock Generator
26	LCD Conn.
27	CRT Conn
28	HDMI
29	FAN /THERMAL
30	SATA (HDD&CD_ROM)
31-32	Audio CODEC(92HD73)/Phone Jack
33-34	LOM /Switch
35-36	PC CARD/1394
37	EXPRESS
38	USB
39	Mini Card
40	WWAN
41	Flash ROM, RTC
42	ITE8512
43	TP/KB/CIR/BT
44	Switch,Keyboard & LED
45	System Reset Circuit
46	RUN POWER
47	Battery Charger
48	DCIN,Batt
49	1.8V_SUS,0.9VTT
50	1.5V_RUN AND 1.1V_RUN
51	+VCC_NB
52	+3.3V_ALW/+5V_SUS
53	VCC_VCORE
54	+1.2V_ALW_SUS
55	VGA_M82
56	Power Rail for system
57	Power Sequence Diagram
58	SMBUS BLOCK
59	Stitch caps and Screw hole.

USB PORT# DESTINATION

SB700	0	Left side USB.
	1	Left side USB.
	2	IO board
	3	IO board
	4	WLAN
	5	WWAN
	6	WPAN
	7	EXPRESS
	10	Biometric
	11	Camera

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
CardBus	AD17	REQ#1/GNT#1	IRQ_SERIRQ IRQD

PCI EXPRESS	DESTINATION
Lane 1	WLAN
Lane 2	WPAN
Lane 3	LOM
Lane 4	EXPRESS CARD
Lane 5	WWAN

POWER STATES

State \ Signal	SLP S3#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON)	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF)	LOW	LOW	ON	OFF	OFF	OFF

PM TABLE

State \ power plane	+15V_ALW +5V_ALW +3.3V_ALW	+5V_SUS +3.3V_SUS +1.8V_SUS +0.9V_DDR_VTT +1.2V_ALW_SUS	+5V_RUN +3.3V_RUN +2.5V_RUN +1.8V_RUN +1.2V_RUN +1.5V_RUN +VCC_CORE +NB_VCORE
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4 on Battery	OFF	OFF	OFF

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Title	Index	
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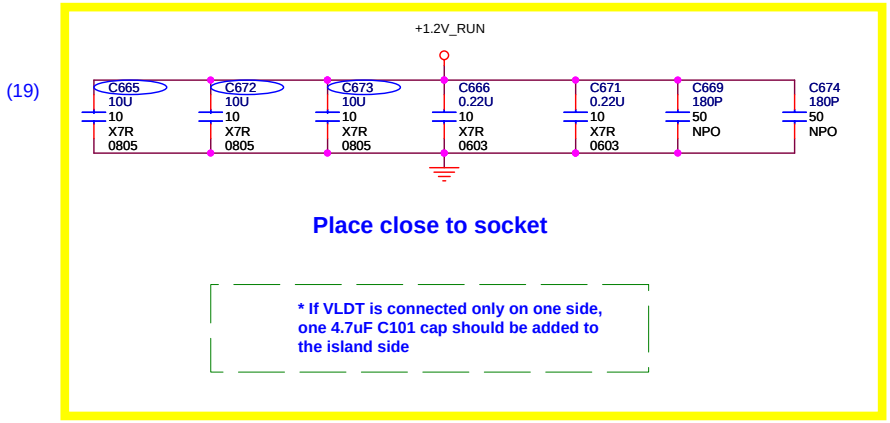

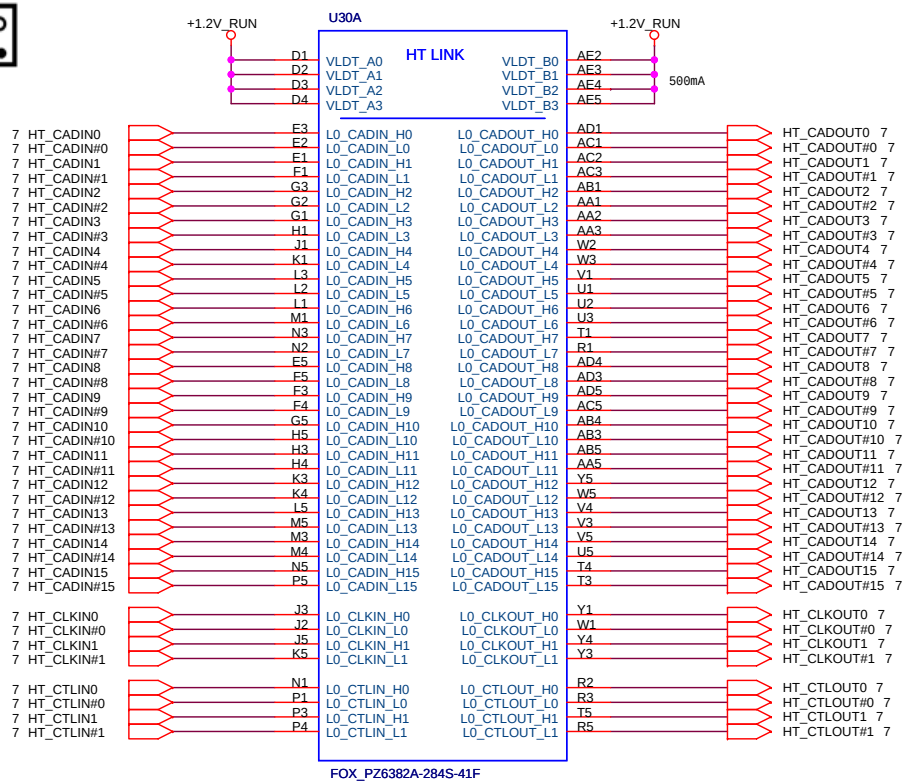

QUANTA COMPUTER

Title	S1G2 HT I/F	
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VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

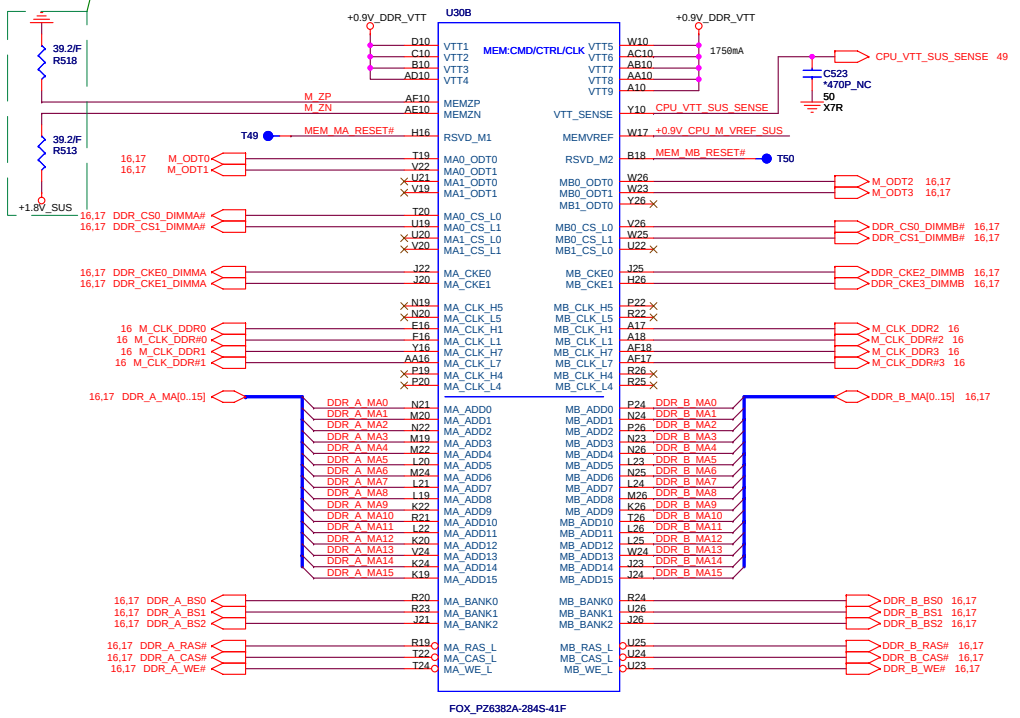
Notes for the SODIMM locations:
DIMMA = CN5
DIMMB = CN6

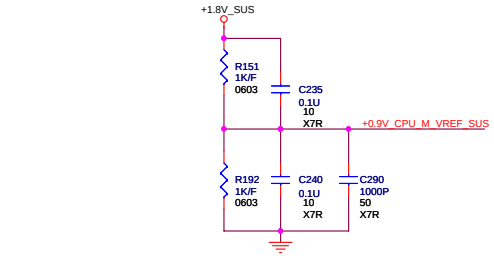
Processor DDR2 Memory Interface

CPU_VTT_SUS_SENSE should be routed as 10mils and 10mils spacing from any adjacent signals in X, Y, Z directions.

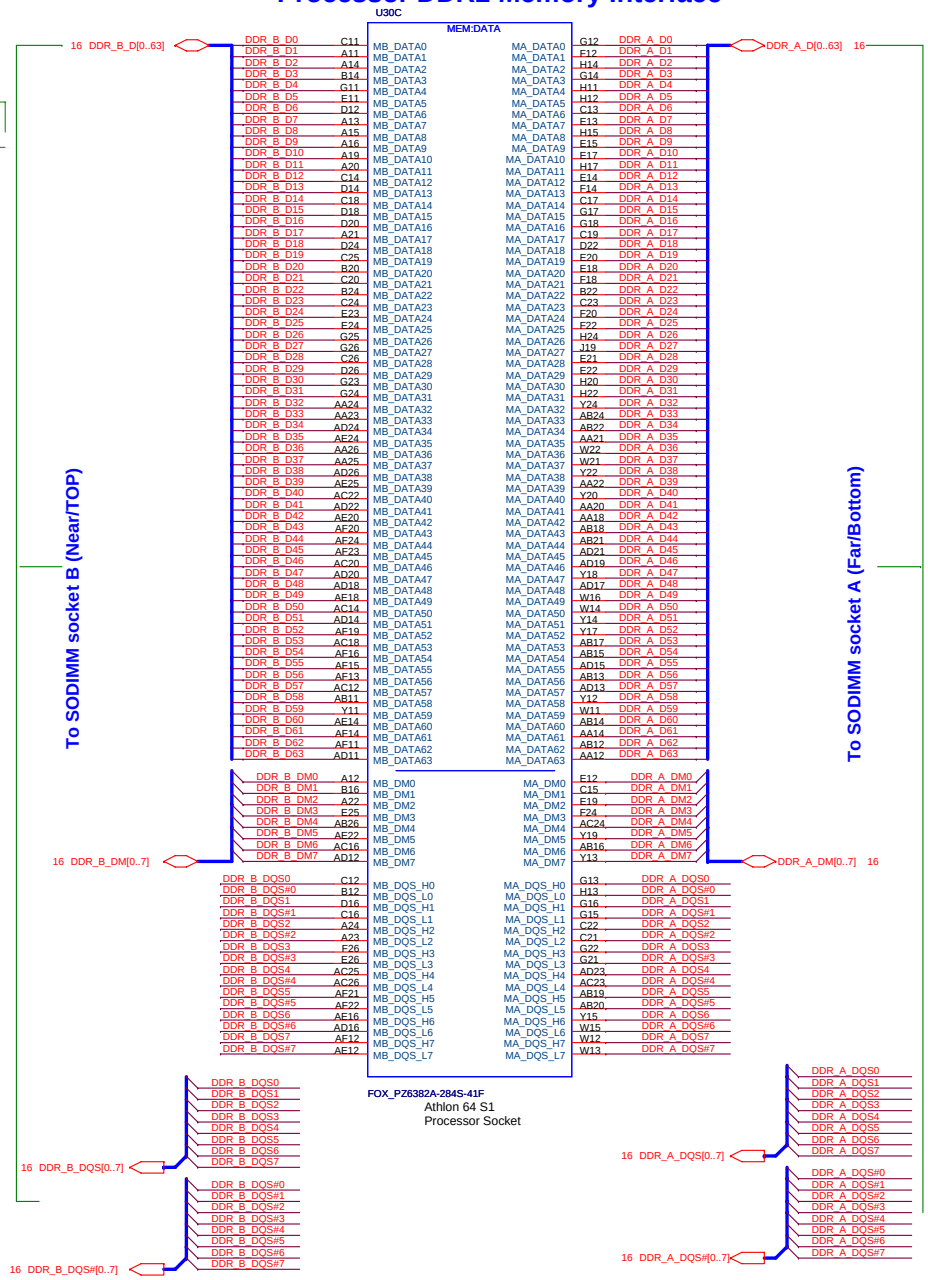
KEEP TRACE TO RESISTORS LESS THAN 1.0" FROM CPU PIN

Place Capacitors for +0.9V_CPU_M_VREF_SUS < 1" from the RS780. +0.9V_CPU_M_VREF_SUS trace length < 6", trace width > 15mils and 20mils spacing from any adjacent signals in X, Y, Z directions.





PLACE CLOSE TO CPU
sensing point for op-amp feedback routed near CPU



QUANTA COMPUTER

Title	S1G2 DDRII MEMORY		
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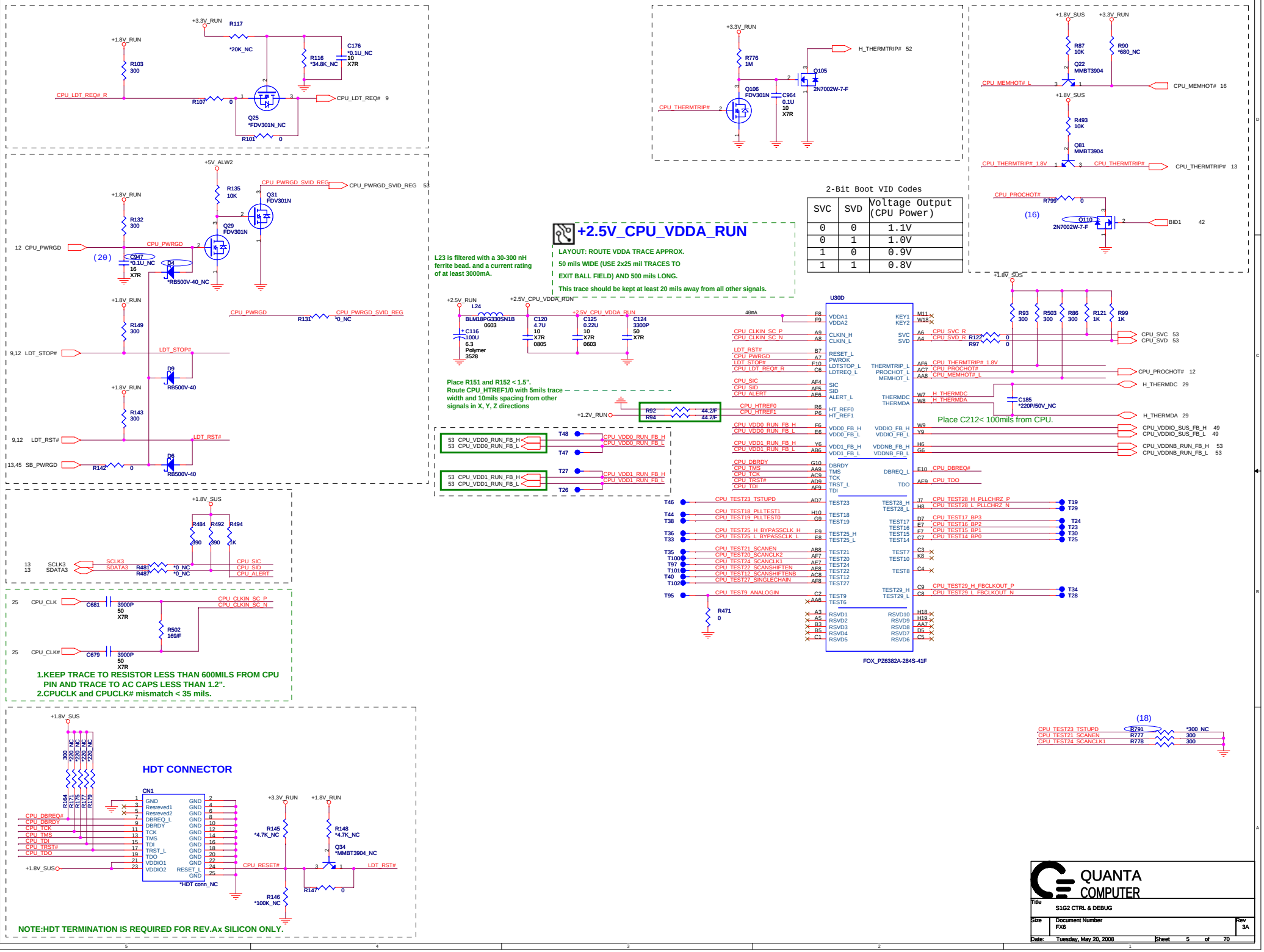
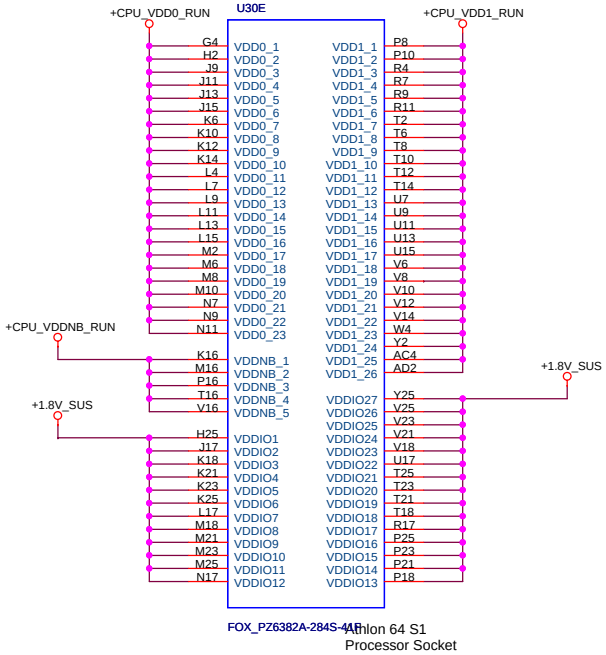
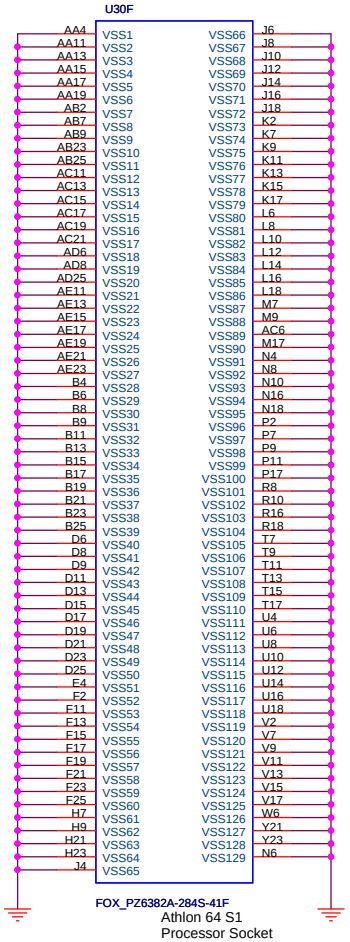


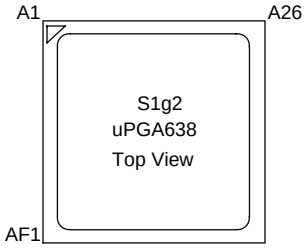
2-Bit Boot VID Codes

SVC	SVD	Voltage Output (CPU Power)
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

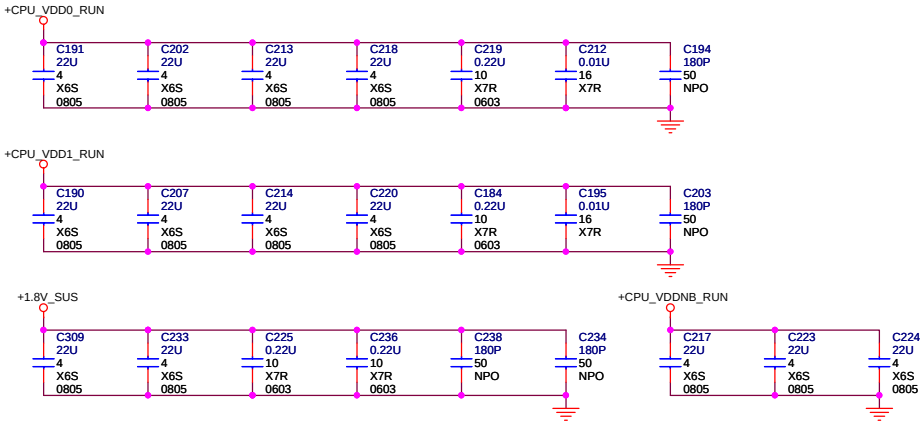
PROCESSOR POWER AND GROUND



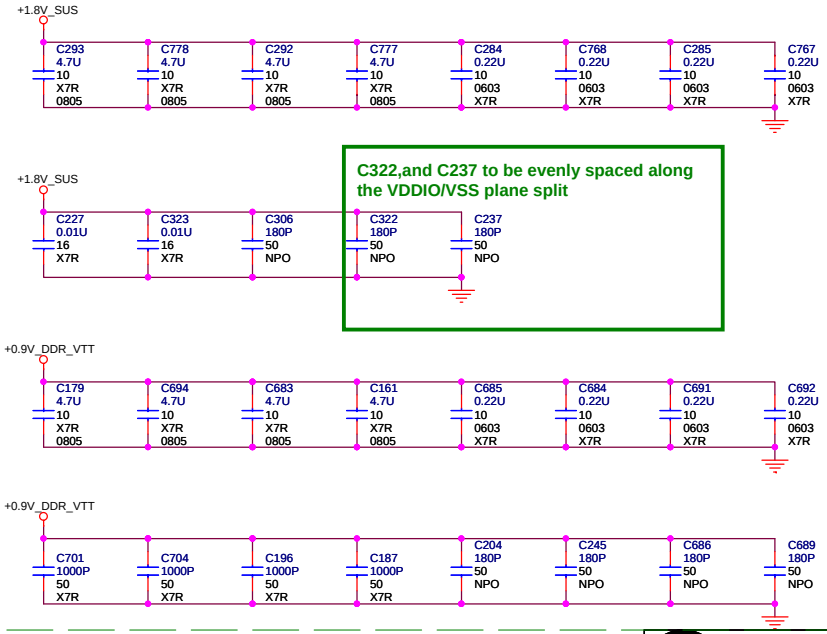




BOTTOMSIDE DECOUPLING



DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE



QUANTA COMPUTER

Title	S1G2 PWR & GND	
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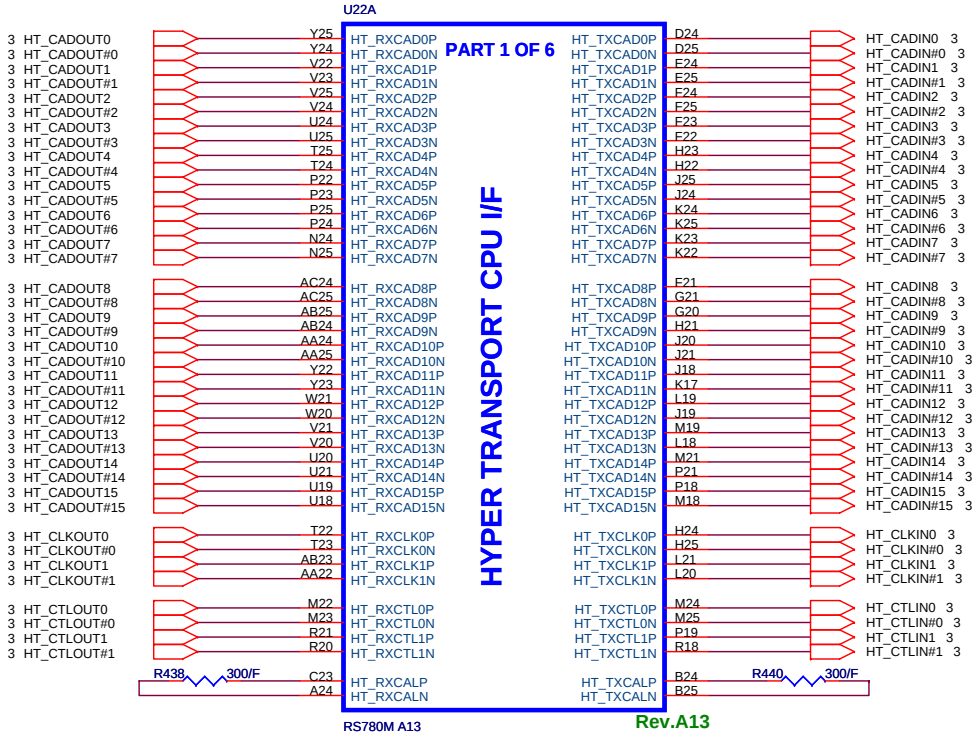

	R438,R440
RS780	301
RX780	1.21K

QUANTA COMPUTER

Title	RS780-HT LINK I/F
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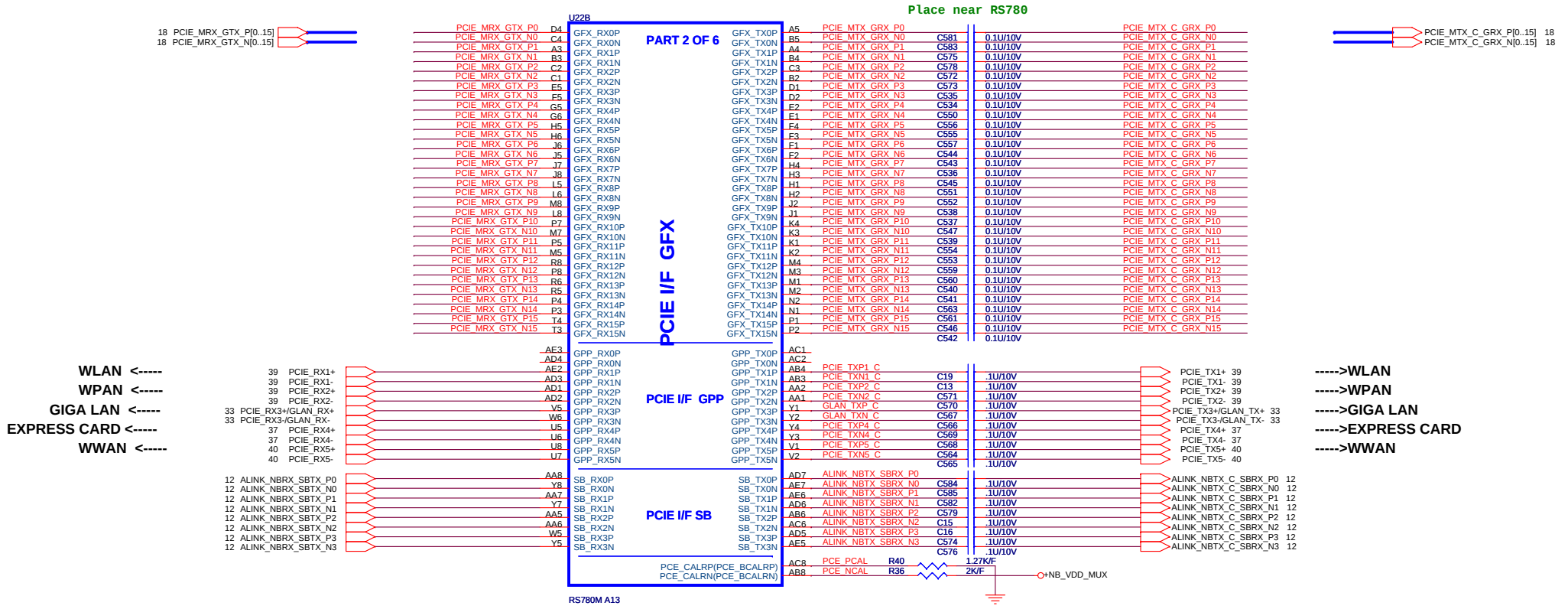

QUANTA COMPUTER

Title	RS780-PCIE I/F		
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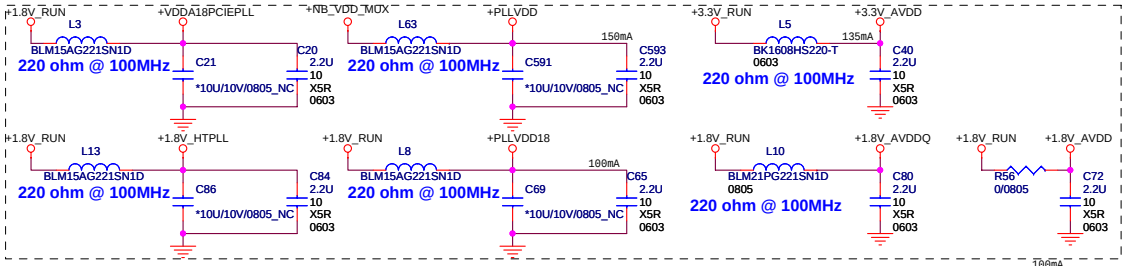
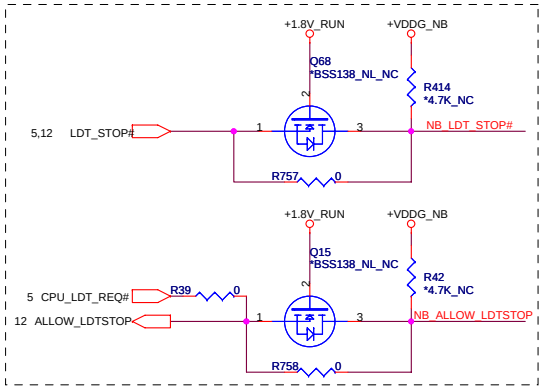
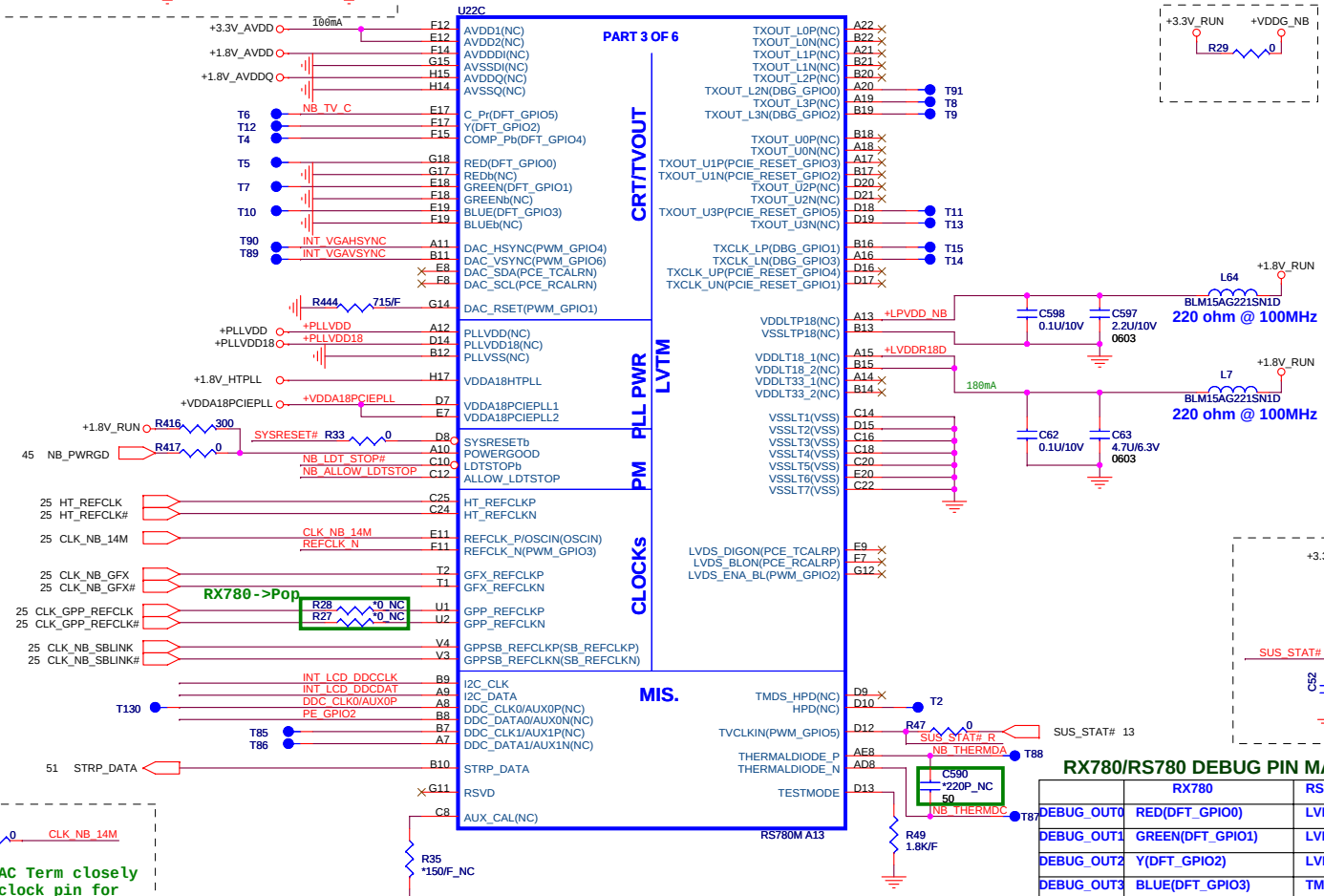


RS740/RX780/RS780 POWER DIFFERENCE

TABLE NAME	RX780	RS780
AVDD	NC	+3.3V
AVDDDI	NC	+1.8V
AVDDQ	NC	+1.8V
PLLVDD	NC	+1.1V
PLLVDD19	NC	+1.8V
VDDA18PCIEPLL	+1.8V	+1.8V
VDDA18HTPLL	+1.8V	+1.8V
VDDLTP18	NC	+1.8V
VDDLT18	NC	+1.8V
VDDLT33	NC	NC

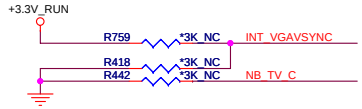




STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
RX780:NB_TV_C; RS740:RS740_DFT_GPIO5; RS780:VSYNC#

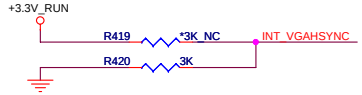
RS740/RS780	RX780
1 Disable	Enable
0 Enable	Disable



RS740/RS780: Enables Side port memory

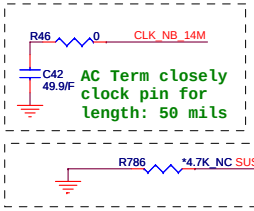
RS740:RS740_DFT_GPIO0
RS780:HSYNC#

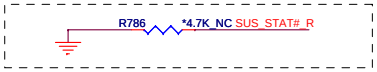
Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

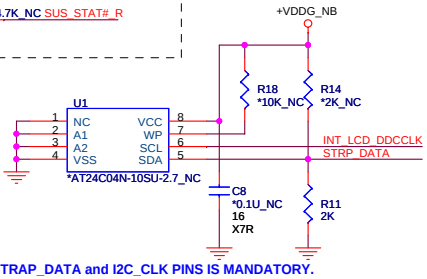


DFT_GPIO1: LOAD_EEPROM_STRAPS

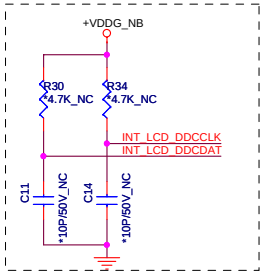
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740/RX780: RS780_AUX_CAL RS780:SUS_STAT

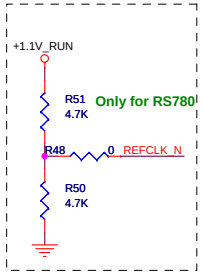






NOTE: ACCESS TO STRAP_DATA and I2C_CLK PINS IS MANDATORY.





Place C590 close to U22.

RX780/RS780 DEBUG PIN MAPPING

	RX780	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLON
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	AUX_CAL
	COMB_Pb(DFT_GPIO4)	X
	C_Pr(DFT_GPIO5)	X

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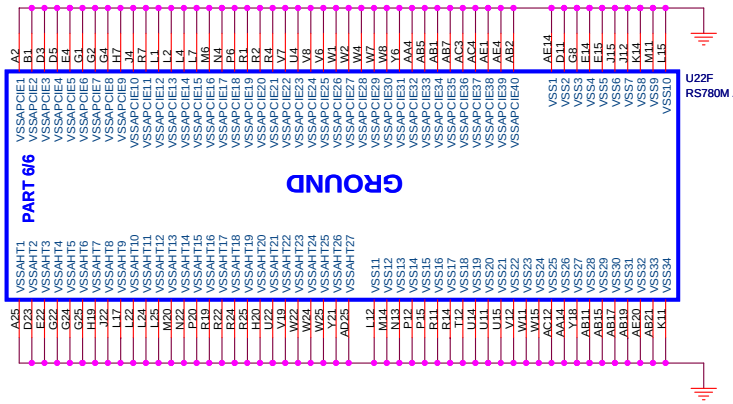
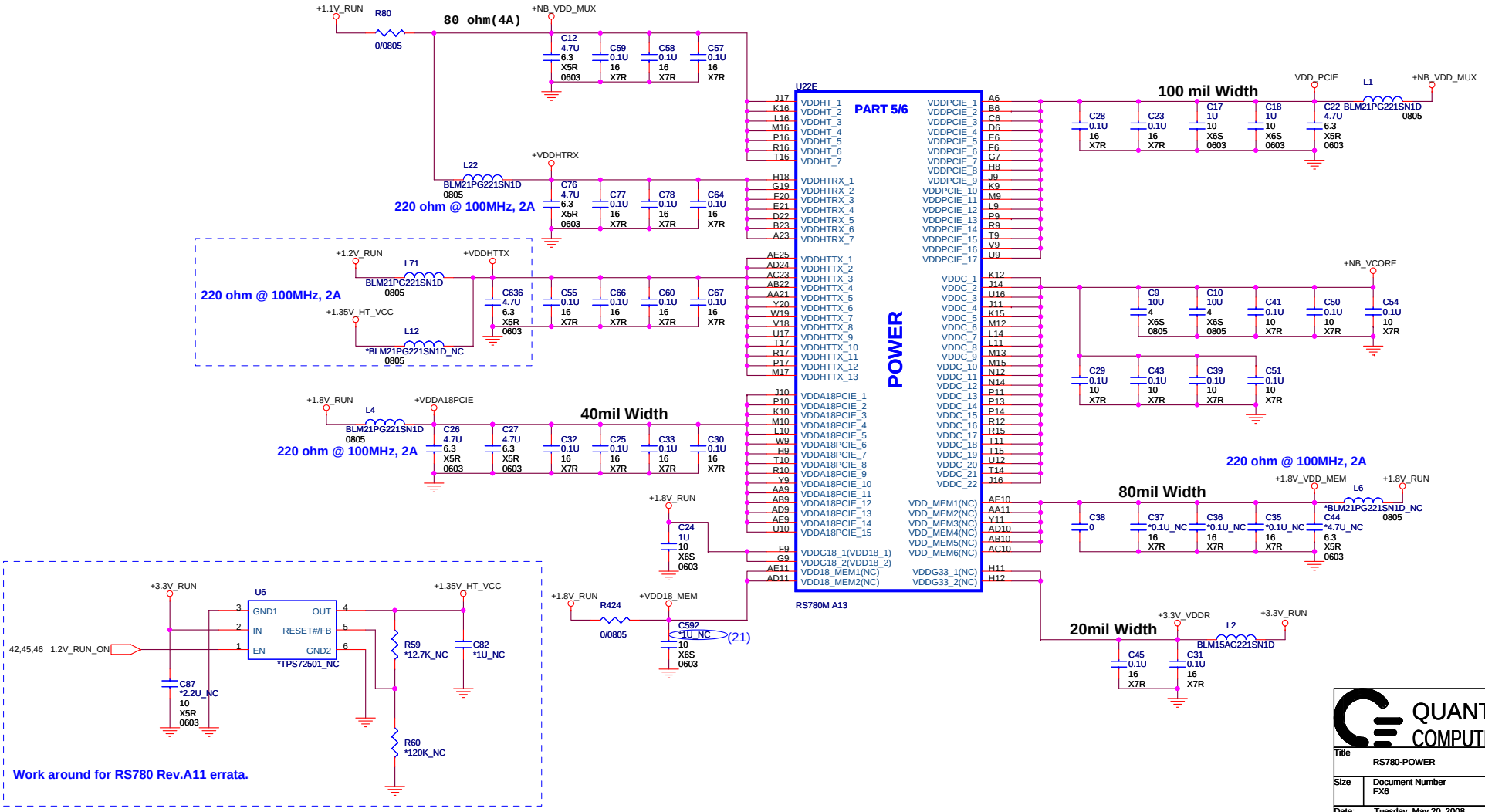
RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V
VDDHTRX	+1.1V	+1.1V
VDDHTTX	+1.2V	+1.2V
VDDA18PCIE	+1.8V	+1.8V
VDDG18	+1.8V	+1.8V
VDD18_MEM	NC	+1.8V
VDDPCIE	+1.1V	+1.1V
VDDC	+1.1V	+1.1V
VDD_MEM	NC	+1.8V/1.5V DDR2/DDR3
VDDG33	NC	+3.3V

*** : Depopulate for RX780.





QUANTA COMPUTER

Title	RS780-POWER	
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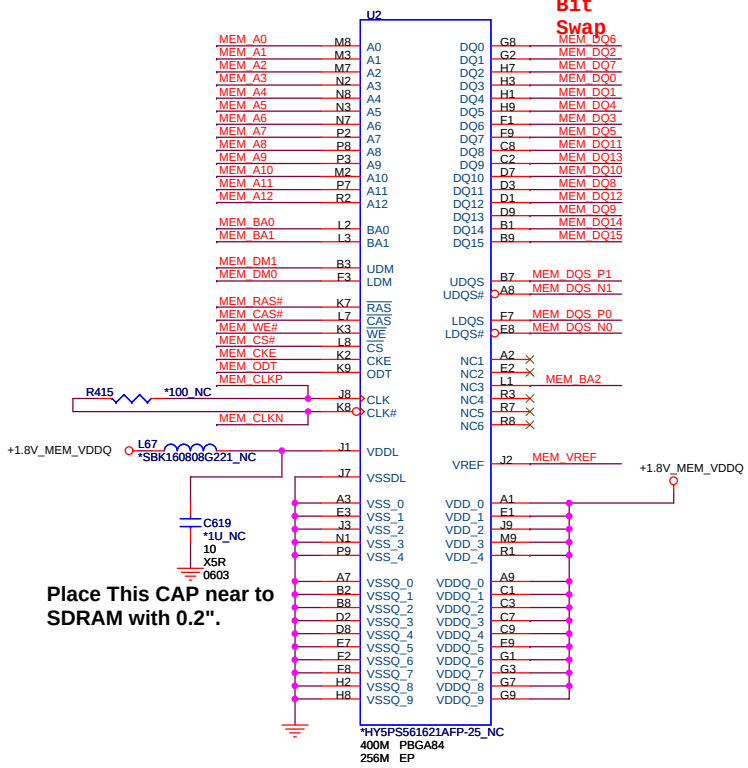
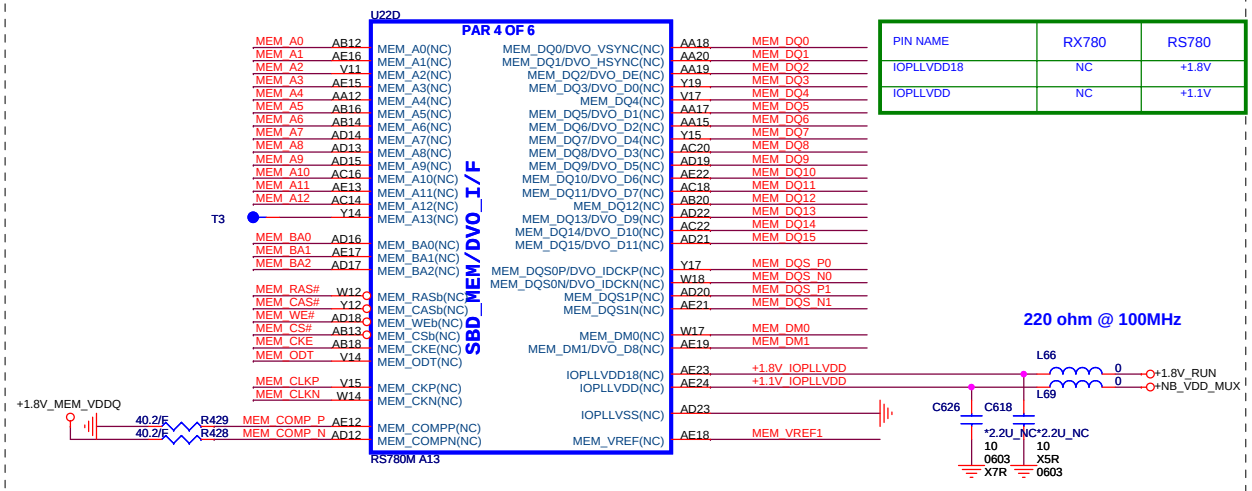
256-Mbit DDR2 16Mbit*16(4bank)



Place This CAP near to SDRAM with 0.2".

RS740/RX780/RS780 POWER DIFFERENCE TABLE

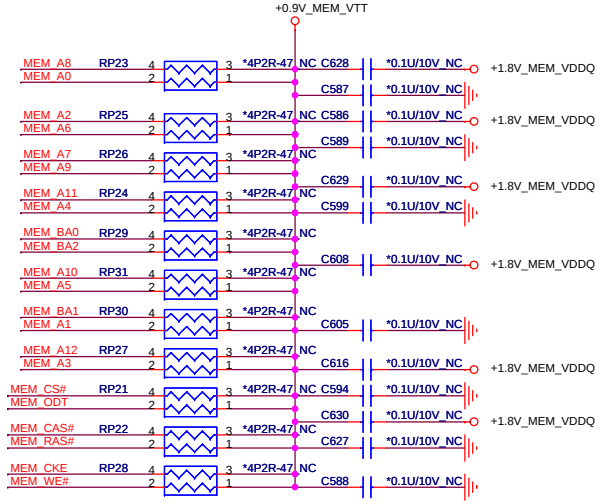
PIN NAME	RX780	RS780
IOPLLVDD18	NC	+1.8V
IOPLLVDD	NC	+1.1V



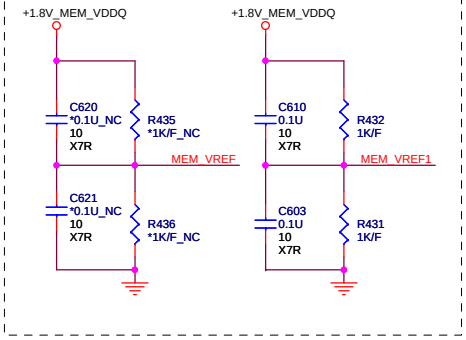
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions

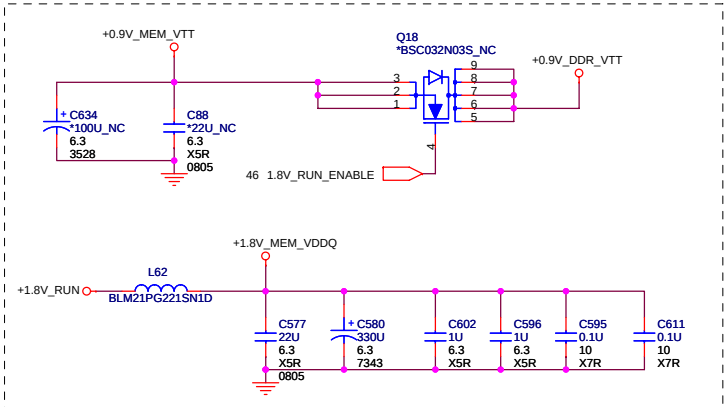
ALL external components connected to SPMEM signals must be removed for RX780.

At least 200mils wide and locate after DDR2 SDRAM



Only for RS780





Local Frame Buffer(64MB) DDRII Power

QUANTA COMPUTER

Title	RS780-SIDE PORT I/O	
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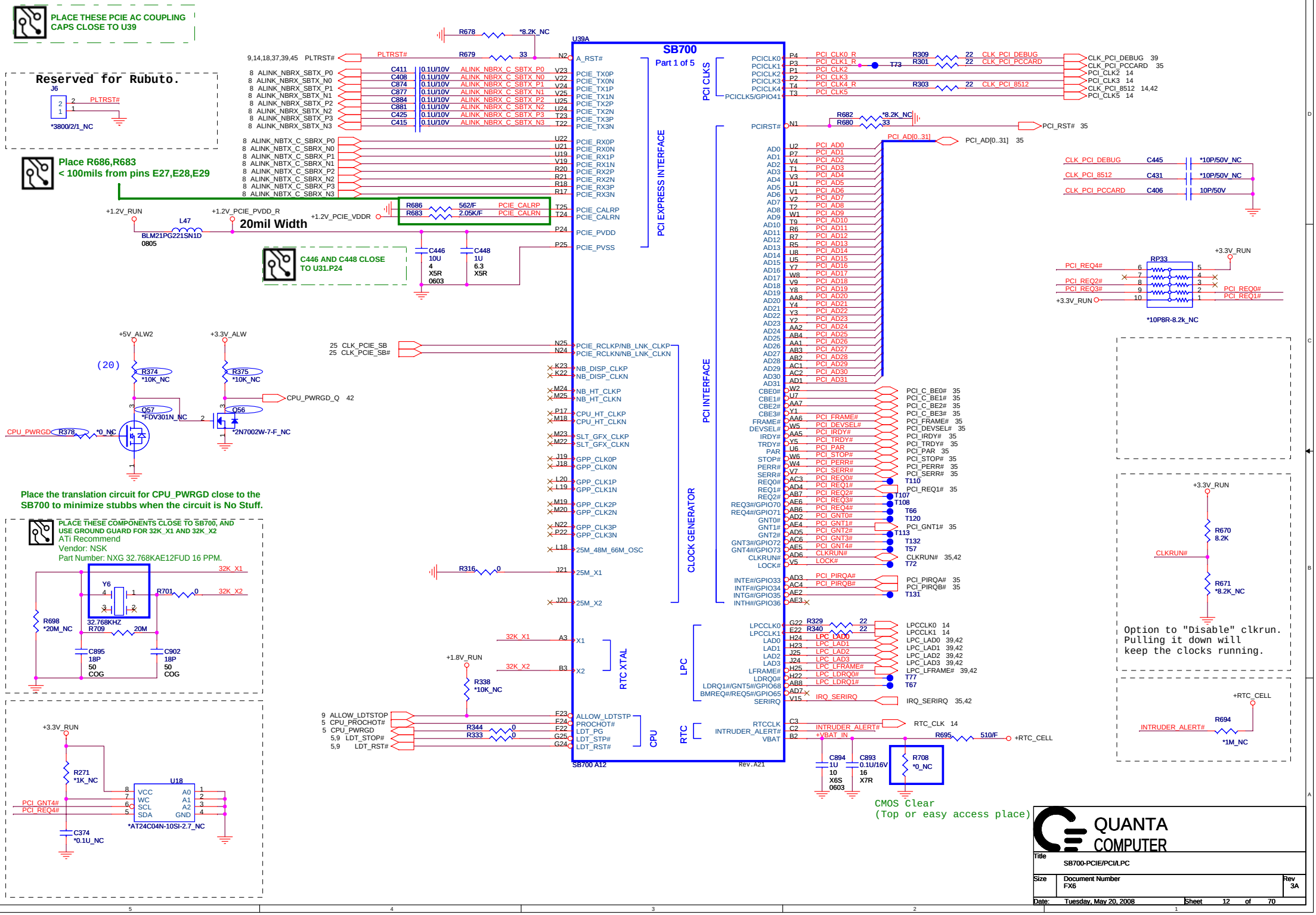
PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U39
Reserved for Rubuto.
J6
*3800/2/1_NC
Place R686,R683 < 100mils from pins E27,E28,E29
20mil Width
L47
BLM21PG221SN1D
0805
C446 AND C448 CLOSE TO U31.P24
C446 10U 4 X5R 0603
C448 1U 6.3 X5R
U39A
SB700
Part 1 of 5
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
RTC XTAL
LPC
CPU
RTC
SB700 A12
Rev.A21
Place the translation circuit for CPU_PWRGD close to the SB700 to minimize stubbs when the circuit is No Stuff.
PLACE THESE COMPONENTS CLOSE TO SB700, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2
ATi Recommend
Vendor: NSK
Part Number: NXG 32.768KAE12FUD 16 PPM.
Y6
32.768KHZ
R698 *20M_NC
R709 20M
C895 18P 50 COG
C902 18P 50 COG
U18
*AT24C04N-10SI-2.7_NC
R271 *1K_NC
C374 *0.1U_NC
Option to "Disable" clkrun. Pulling it down will keep the clocks running.
CMOS Clear (Top or easy access place)
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SB700-PCIE/PCI/LPC
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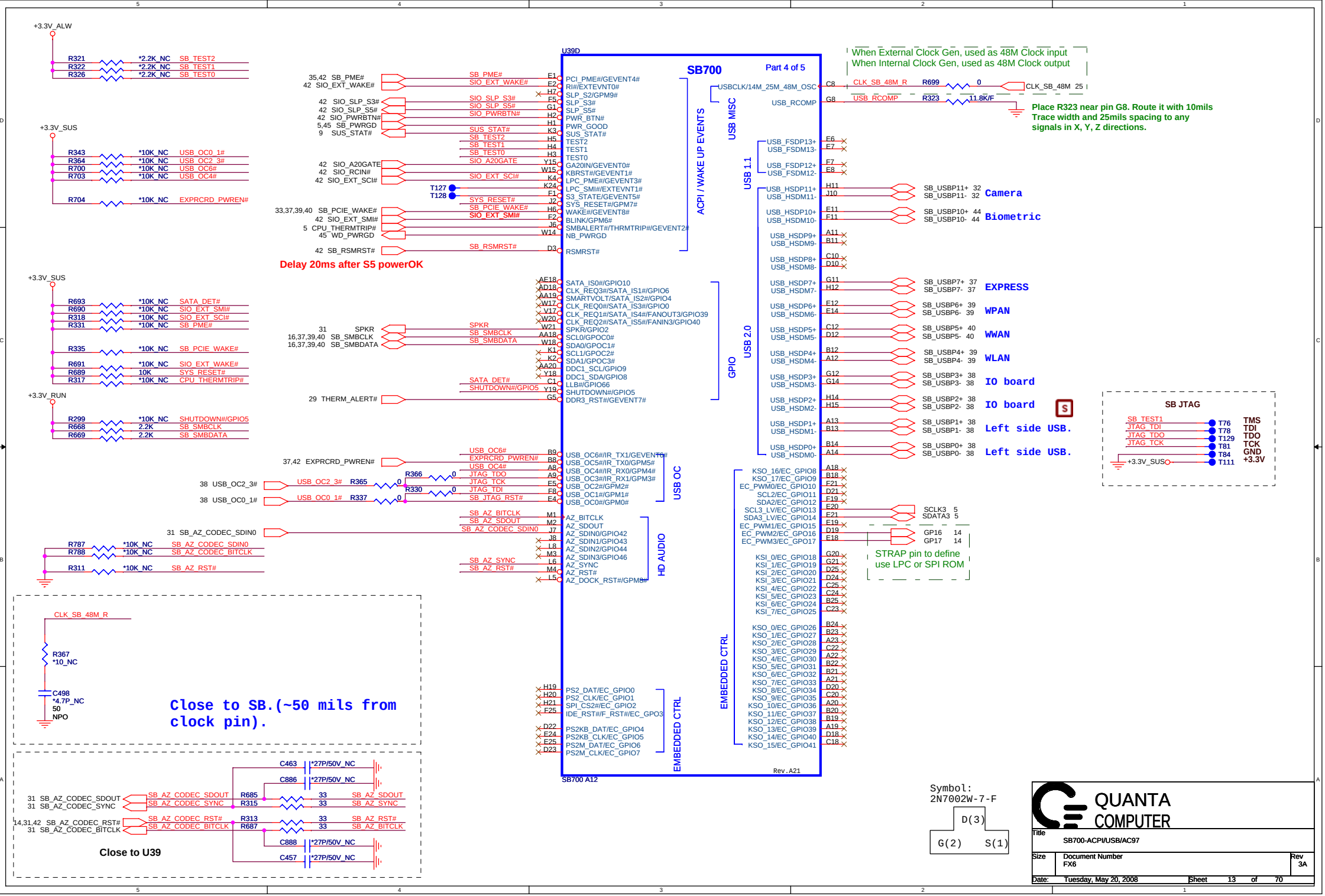
SB700
Part 4 of 5
U39D
SB700 A12
Rev.A21
When External Clock Gen, used as 48M Clock input
When Internal Clock Gen, used as 48M Clock output
Place R323 near pin G8. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.
Delay 20ms after S5 powerOK
Close to SB.(~50 mils from clock pin).
Close to U39
STRAP pin to define use LPC or SPI ROM
SB JTAG
Camera
Biometric
EXPRESS
WPAN
WWAN
WLAN
IO board
IO board
Left side USB.
Left side USB.
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
EMBEDDED CTRL
Symbol:
2N7002W-7-F
D(3)
G(2)
S(1)
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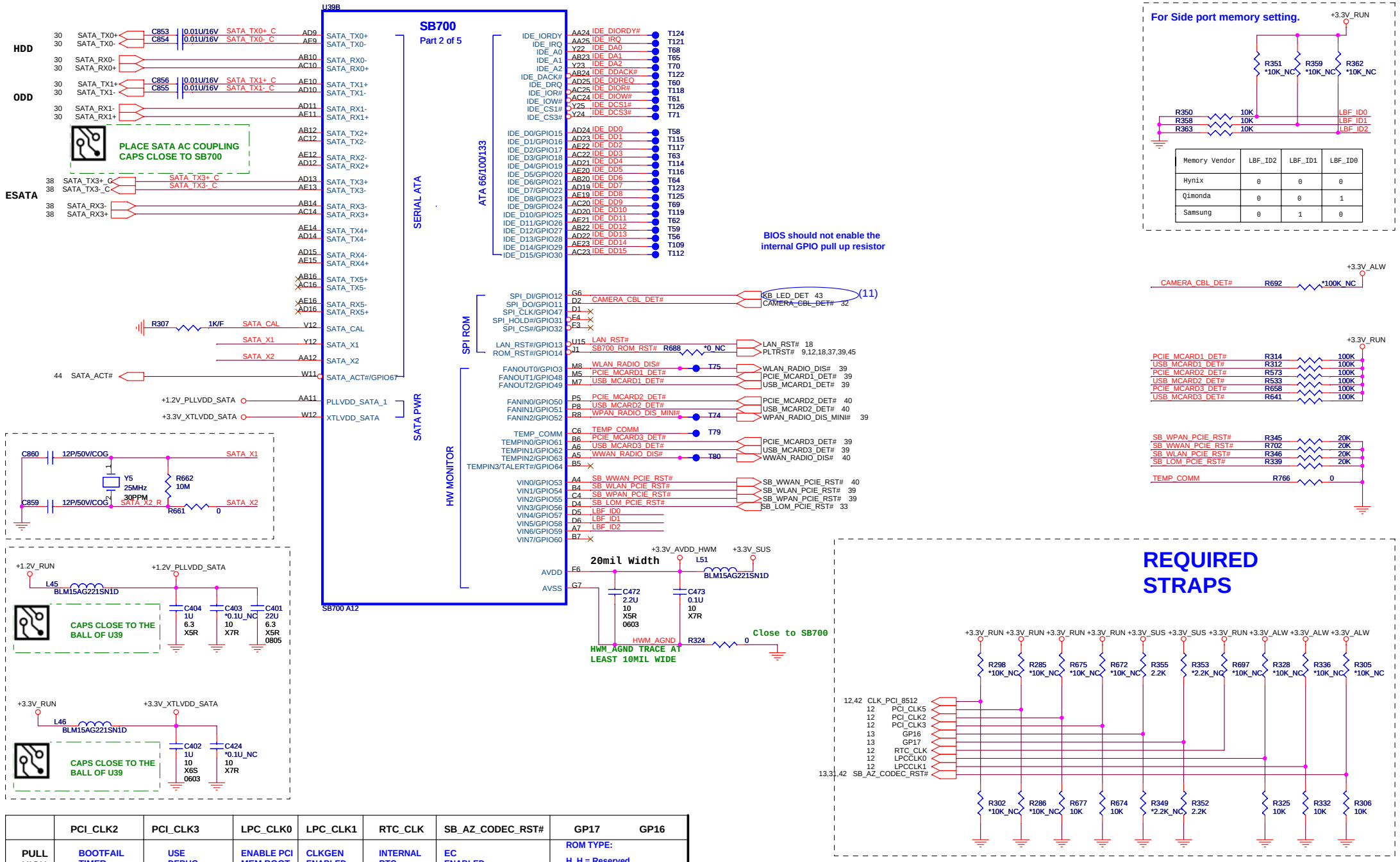


Memory Vendor	LBF_ID2	LBF_ID1	LBF_ID0
Hynix	0	0	0
Qimonda	0	0	1
Samsung	0	1	0

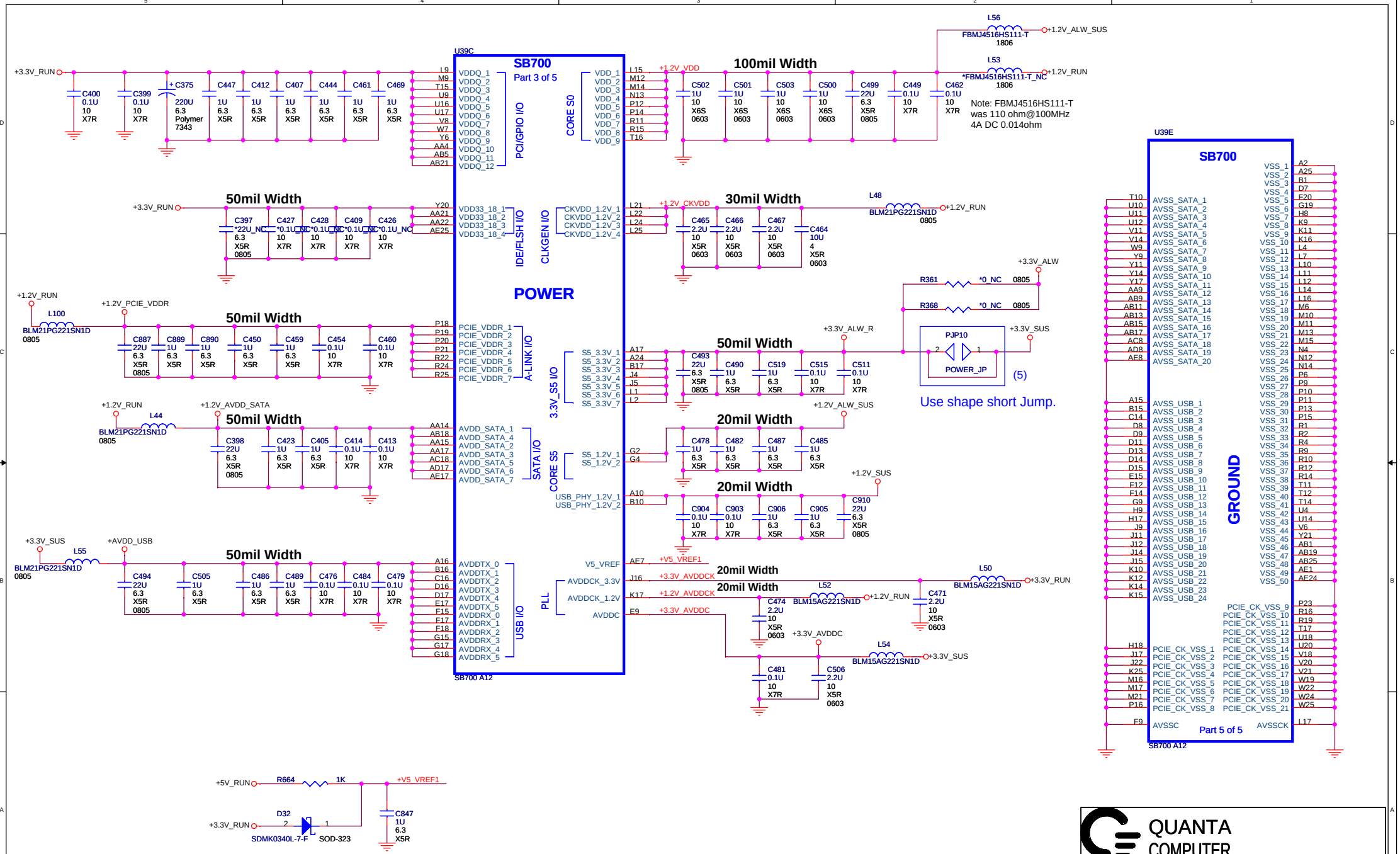
	PCI_CLK2	PCI_CLK3	LPC_CLK0	LPC_CLK1	RTC_CLK	SB_AZ_CODEC_RST#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	

QUANTA COMPUTER

Title: SB700-HDD/POWER

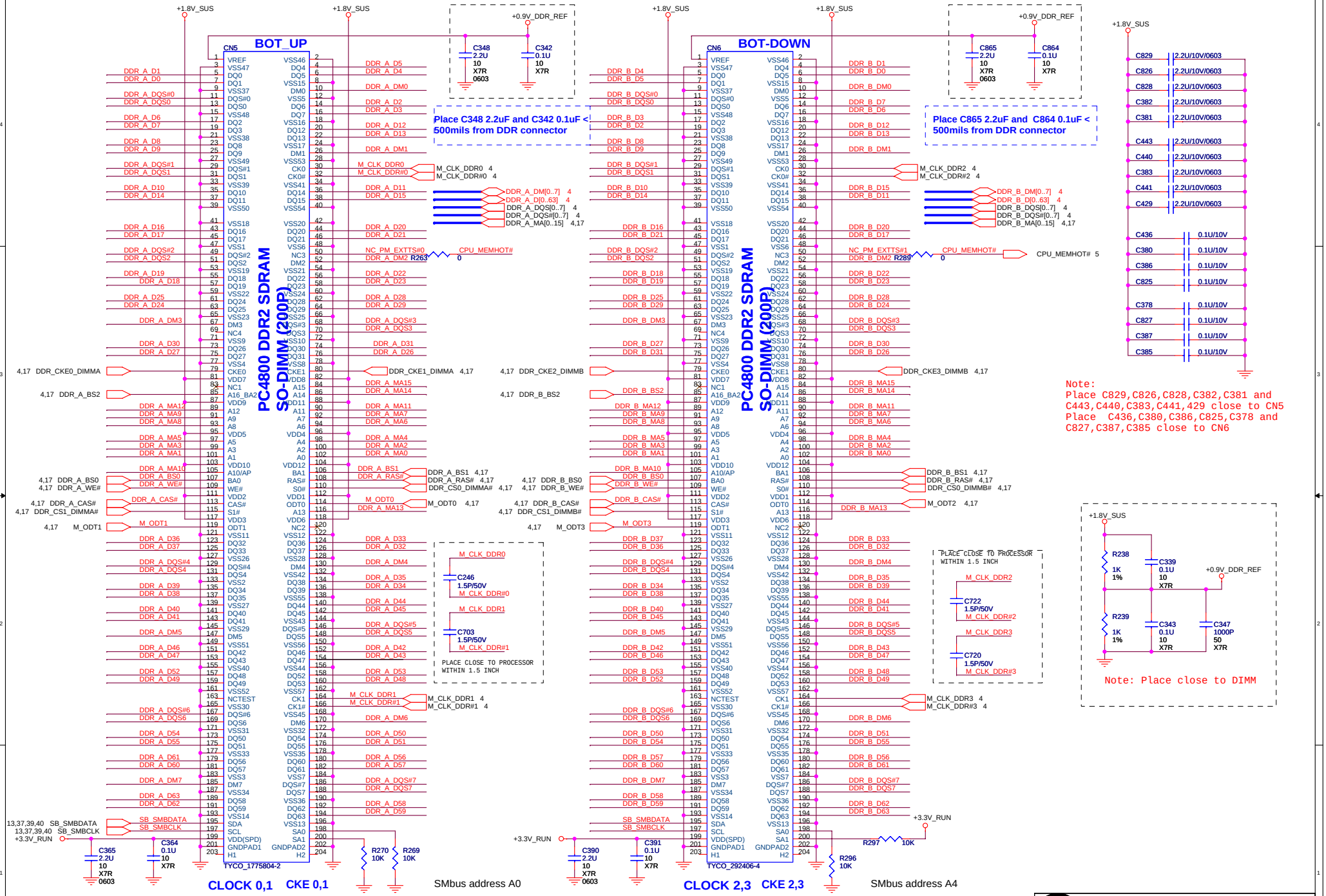
Size: Document Number FX6 Rev 3A

Date: Tuesday, May 20, 2008 Sheet 14 of 70



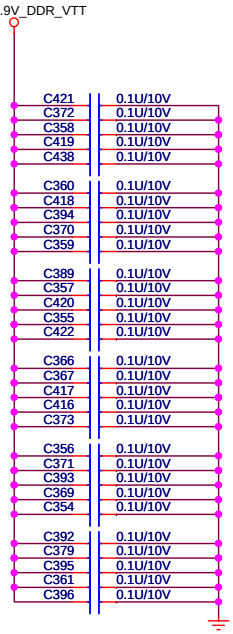
QUANTA COMPUTER

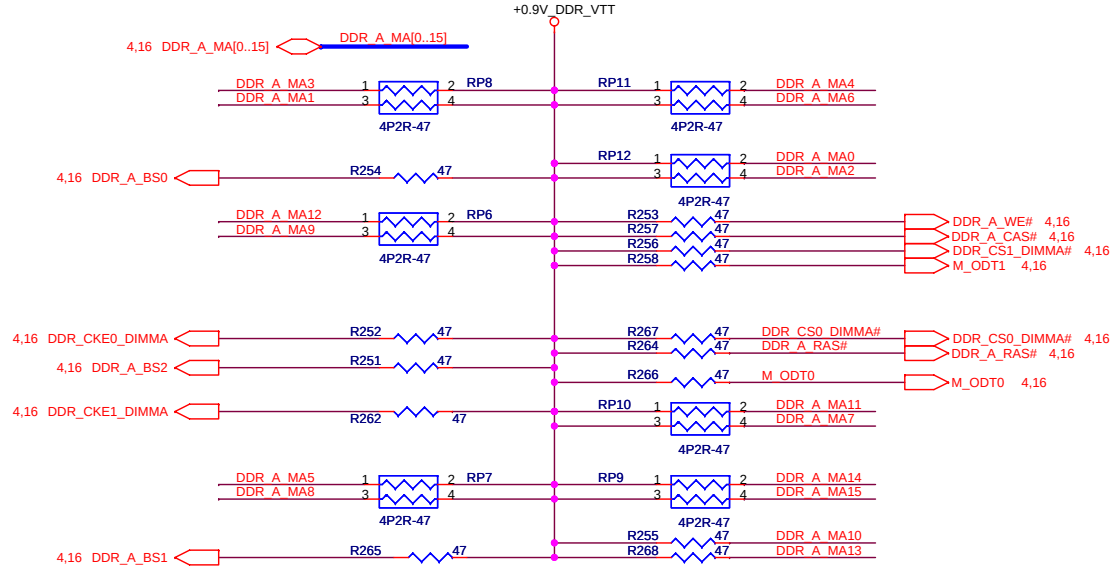
Title	SB700-POWER
Size	Document Number FX6
Rev	3A
Date:	Tuesday, May 20, 2008
Sheet	15 of 70



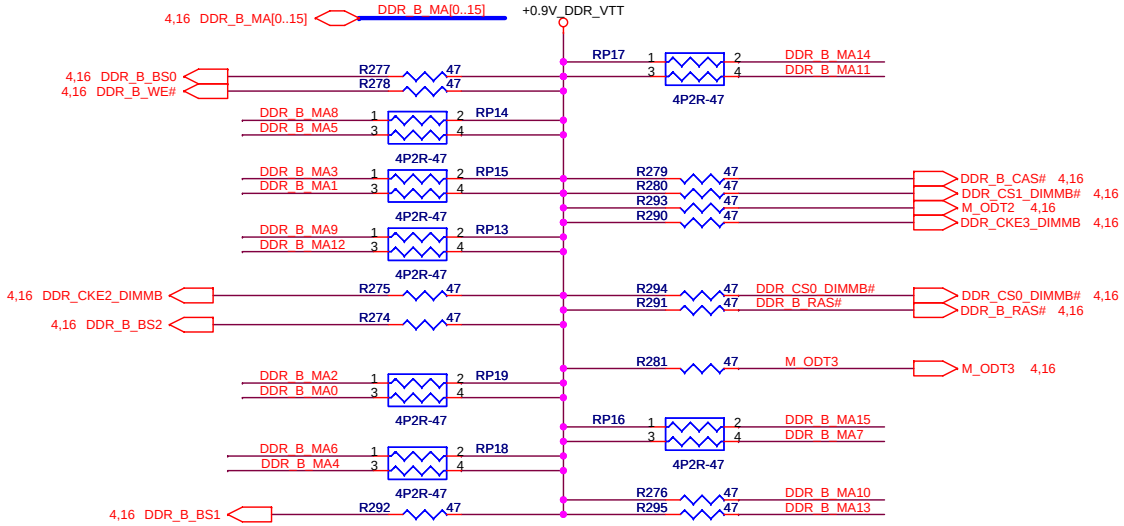
QUANTA COMPUTER

Title	DDRII SODIMMX2		
Size	Document Number FX6		Rev 3A
Date: Tuesday, May 20, 2008	Sheet 16 of 70		

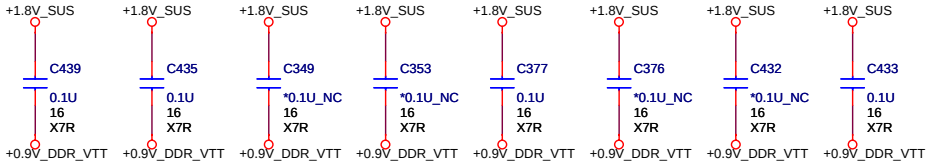




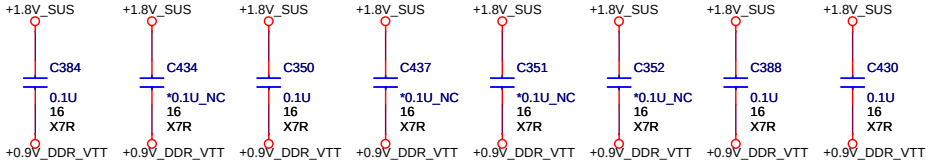
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT



Note: Reserve stitching function for CN5.

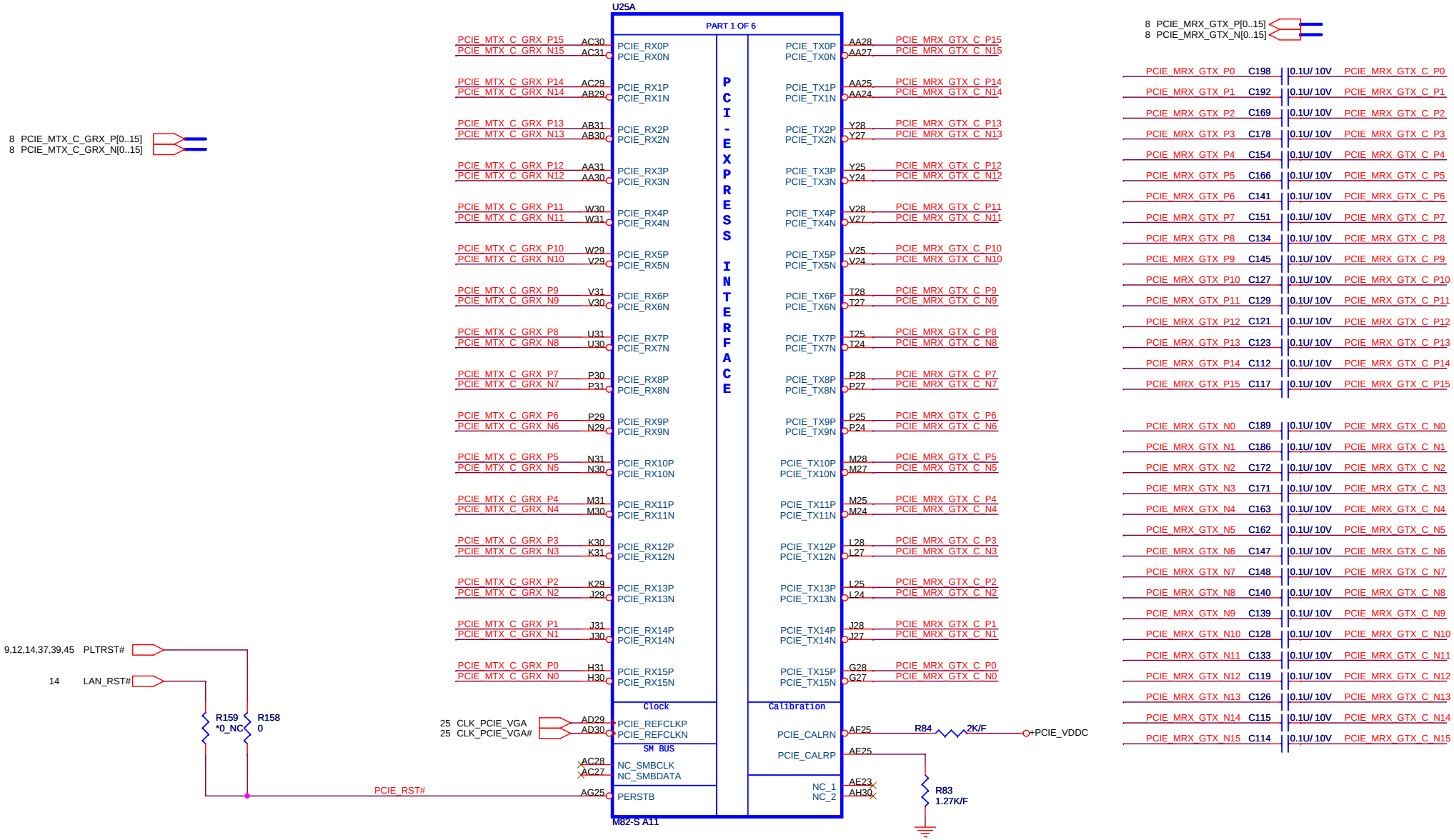


Note: Reserve stitching function for CN6.



QUANTA COMPUTER

Title	DDRII TERMINATION	
Size	Document Number FX6	Rev 3A
Date: Tuesday, May 20, 2008	Sheet 17 of 70	



Title	M82S_PCIE		
Size B	Document Number FX6		Rev 3A
Date: Tuesday, May 20, 2008		Sheet 18 of 70	

MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	RAM_CFG3 GPIO9	RAM_CFG2 GPIO13	RAM_CFG1 GPIO12	RAM_CFG0 GPIO11
128MB	X	0	0	0
256MB	X	0	0	1
64MB	X	0	1	0
512MB	X	1	0	0

+3.3V_DELAY

R497 10K RAM_CFG0
R489 *10K_NC RAM_CFG1
R498 *10K_NC RAM_CFG2
R111 *10K_NC RAM_CFG3

MEMORY STRAPS	RAM_TYPE _CFG3	RAM_TYPE _CFG2	RAM_TYPE _CFG1	RAM_TYPE _CFG0
400MHz 256MB(32M*16) Samsung	0	0	1	0
400MHz 256MB(32M*16) Hynix	0	0	1	1
500MHz 256MB(32M*16) Samsung	0	1	1	0
500MHz 256MB(32M*16) Qimonda	0	1	0	0

+1.8V_RUN

R468 *10K_NC RAM_TYPE_CFG0
R467 *10K_NC RAM_TYPE_CFG1
R469 10K RAM_TYPE_CFG2
R470 *10K_NC RAM_TYPE_CFG3

GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	ATI Usage	FX6 Usage
GPIO0	PCIE FULL TX OUTPUT SWING	X	1
GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	1
GPIO2	ATI reserved configuration straps.	RSVD	0
GPIO3	ATI reserved configuration straps.	RSVD	0
GPIO4	DEBUG SIGNALS MUXED OUT	0	0
GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
GPIO6	ATI Internal use only	0	0
GPIO10	Serial ROM clock to ROM.		0
ATI Usage recommended settings	0= DO NOT INSTALL RESISTOR, X = DESIGN DEPENDANT, RSVD = ATI RESERVED (DO NOT INSTALL)		

+3.3V_DELAY

R104 10K GPIO0
R485 10K GPIO1
R480 *10K_NC GPIO2
R102 *10K_NC GPIO3
R491 *10K_NC GPIO4
R490 *10K_NC GPIO5
R106 *10K_NC GPIO6
R488 *10K_NC GPIO10
R110 10K HDMI_HD_EN
R126 *10K_NC TEMP_FAIL#
R100 10K GFX_CLKREQ#
R72 10K VGAHSYNC

Strap pin for HDMI enable.

R125 10K TEMP_FAIL#

25 CLK_VGA_27M_SS — R476 *0_NC — CLK_VGA_27M_SS_R

Layout Note:
Place R476, R461, R474, R473 close to M82.

R461 *10K_NC

25 CLK_VGA_27M_NSS — R474 100/F — R473 120/F — R462 0 — XTAIN

U25B

PART 2 OF 6

INTEGRATED TMDS/DP PORT

Pin	Signal	Pin	Signal	Net
AJ4	TXCM_DPA0P	AK9	TXCM_DPB0P	HDMI_CLK- 28
AJ5	TXCP_DPA0N	AL9	TXCP_DPB0N	HDMI_CLK+ 28
AL5	TX0M_DPA1P	AJ9	TX0M_DPB1P	HDMI_TX0- 28
AK5	TX0P_DPA1N	AJ10	TX0P_DPB1N	HDMI_TX0+ 28
AL6	TX1M_DPA2P	AL10	TX1M_DPB2P	HDMI_TX1- 28
AK6	TX1P_DPA2N	AK10	TX1P_DPB2N	HDMI_TX1+ 28
AK8	TX2M_DPA3P	AL11	TX2M_DPB3P	HDMI_TX2- 28
AL8	TX2P_DPA3N	AK11	TX2P_DPB3N	HDMI_TX2+ 28

AD9 DVALID
AE7 PSYNC_NEW

DPA_PVDD AL7 — +TPVDD
DPA_PVSS AK7
DPB_PVDD AE11
DPB_PVSS AF11
DPA_VDDR_1 AJ12 — +DPA_VDDR
DPA_VDDR_2 AJ13
DPB_VDDR_1 AK13 — +DPB_VDDR
DPB_VDDR_2 AL13
DPB_VSSR_5 AL12
DPB_VSSR_4 AK12
DPB_VSSR_3 AJ11
DPB_VSSR_2 AH9
DPB_VSSR_1 AH11
DPA_VSSR_5 AJ8
DPA_VSSR_4 AF7
DPA_VSSR_3 AG7
DPA_VSSR_2 AJ7 — VIP_3 — R472 0
DPA_VSSR_1 AH7
DP_CALR AG11 — R95 150
HPD1 AA8 — HDMI_DET 28

AK4 DVPCNTL_MVP_0
AL3 DVPCNTL_MVP_1
V2 DVPCNTL_0
V1 DVPCNTL_1
W3 DVPCNTL_2
W1 DVPCLK

EXT TMDS DVO

Y1 DVPDATA_0
Y2 DVPDATA_1
Y3 DVPDATA_2
AA2 DVPDATA_3
AA3 DVPDATA_4
AB1 DVPDATA_5
AB2 DVPDATA_6
AB3 DVPDATA_7
AC1 DVPDATA_8
AC3 DVPDATA_9
AD1 DVPDATA_10
AD2 DVPDATA_11
AD3 DVPDATA_12
AE3 DVPDATA_13
AG3 DVPDATA_14
AH3 DVPDATA_15
AG1 DVPDATA_16
AH2 DVPDATA_17
AH1 DVPDATA_18
AJ3 DVPDATA_19
AJ1 DVPDATA_20
AJ2 DVPDATA_21
AK2 DVPDATA_22
AK3 DVPDATA_23

RAM_TYPE_CFG0 AJ1
RAM_TYPE_CFG1 AJ2
RAM_TYPE_CFG2 AK2
RAM_TYPE_CFG3 AK3

DAC1 / CRT

R AL28 — R466 0 VGA_RED — VGA_RED 27
RB AK28
G AL27 — R458 0 VGA_GRN — VGA_GRN 27
GB AK27
B AL26 — R455 0 VGA_BLU — VGA_BLU 27
BB AK26
HSYNC AK29 — VGAHSYNC — VGAHSYNC 27
VSYNC AK30 — VGAVSYNC 27
RSET AJ28 — R76 499/F
AVDD AL29 — +AVDD
AVSSQ AH28
VDD1DI AJ27 — +VDD1D_2D
VSS1DI AJ26

WITH M8x ASIC
INSTALL M8x STRAP RESISTORS
AND
DO NOT INSTALL M7x STRAP RESISTORS
WITH M7x ASIC
INSTALL M7x STRAP RESISTORS
AND
DO NOT INSTALL M8x STRAP RESISTORS

DIS only

VGA_RED
VGA_GRN
VGA_BLU

R465 150/F — R464 150/F — R463 150/F

Layout Note:
Place 150 ohm termination resistors close to ATI CHIP.

GENERAL PURPOSE I/O

GPIO0 Y4
GPIO1 V3
GPIO2 V4
GPIO3 V5
GPIO4 U3
GPIO5 U2
GPIO6 T4
T5 — 42 PANEL_BKEN
HDMI_HD_EN T7
RAM_CFG3 T8
GPIO10 R1
RAM_CFG0 R2
RAM_CFG1 R3
RAM_CFG2 P1
P3 — T98 PAD
N1 — R499 0 — 55 GFX_CORE_CNTRL0
CLK_VGA_27M_SS_R N2
P4 — R113 0 — 22 THERMAL_INT#
P7 — T31 PAD
P8 — TEMP_FAIL# — R112 0 — 20 TEMP_FAIL# — 55 GFX_CORE_CNTRL1 — 20 BB_ENA
P5
V7
N3 — T99 PAD
Y5 — GFX_CLKREQ# — R127 1K
M4
M5 — T37 PAD
M7 — T42 PAD
M8 — T43 PAD
L8 — T32 PAD
Y8 — T21 PAD
Y7 — T20 PAD
V8 — T22 PAD
AH6 — T93 PAD
AG6 — T94 PAD

GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7_BLON
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HPD2
GPIO_15_PWRCNTL0
GPIO_16_SSIN
GPIO_17_THERMAL_INT
GPIO_18_HPD3
GPIO_19_CTF
GPIO_20_PWRCNTL1
GPIO_21_BB_EN
GPIO_22_ROMCSB
GPIO_23_CLKREQB
GPIO_24_JMODE
GPIO_25_TDI
GPIO_26_TCK
GPIO_27_TMS
GPIO_28_TDO

GEN_A
GEN_B
GEN_C
GEN_D_HPD4
GEN_E

DAC2 (TV/CRT2)

R2 AL17
R2B AK17
G2 AL15
G2B AK15
B2 AL14
B2B AK14
C AJ17
Y AJ15
COMP AJ14
V2SYNC AE16
H2SYNC AE16
A2VDD AH14 — +A2VDD
A2VDDQ AH16 — +A2VDDQ
A2VSSQ AG16
VDD2DI AF18 — +VDD1D_2D
VSS2DI AF18
R2SET AG14 — R96 715/F

OPTIONAL 0 OHM STRAPS TO GROUND
FOR RB,GB,BB AND R2B,G2B,B2B
SEE DAC1_RGB AND DAC2_RGB SHEETS

PLACE OR RESISTORS CLOSE TO ASIC

+1.8V_RUN

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = .6V)
PLACE VREF DIVIDER
AND CAP CLOSE TO ASIC

R82 499/F
R74 249/F
C94 0.1U 10 X7R

AC11 VREFG

+DPLL_PVDD AH12 DPLL_PVDD
AG12 DPLL_PVSS
+PCIE_PVDD AH31 PCIE_PVDD
+MPVDD A9 MPVDD
B9 MPVSS
+DPLL_VDDC AE12 DPLL_VDDC
AJ31 XTALIN
AJ30 XTALOUT

PLL & XTAL

R70 1K — AH26 TESTEN — TEST
AD12 PLLTEST

SERIAL BUSES

SCL AA5
SDA AA4
DDC1DATA AJ29 — LCD_DDCDAT — LCD_DDCDAT 26
DDC1CLK AH29 — LCD_DDCCLK — LCD_DDCCLK 26
DDC2DATA AC5
DDC2CLK AC4
DDC3DATA_DP3_AUXN AF4 — HDMI_SDA 28
DDC3CLK_DP3_AUXP AH4 — HDMI_SCL 28
DDC4DATA_DP4_AUXN AF9 — G_DAT_DDC2_L — R79 0 — G_DAT_DDC2 27
DDC4CLK_DP4_AUXP AG9 — G_CLK_DDC2_L — R77 0 — G_CLK_DDC2 27

THERMAL

TS_FDO AE14
DPLUS AE5 — VGA_THERMDP 22
DMINUS AE4 — VGA_THERMDN 22

+3.3V_DELAY

LCD_DDCDAT — R1 2.2K
LCD_DDCCLK — R5 2.2K

3.3V TO 5V LEVEL SHIFT LOGIC REQUIRED
IF DDC1,DDC2 USED ON M8x OR DDC1,DDC2,DDC3
(DDC4 NOT AVAILABLE) USED ON M7x
DDC3,DDC4 ARE 5V TOLERANT ON M8x

M82-S A11

Title	M82S_IO	
Size Custom	Document Number FX6	Rev 3A
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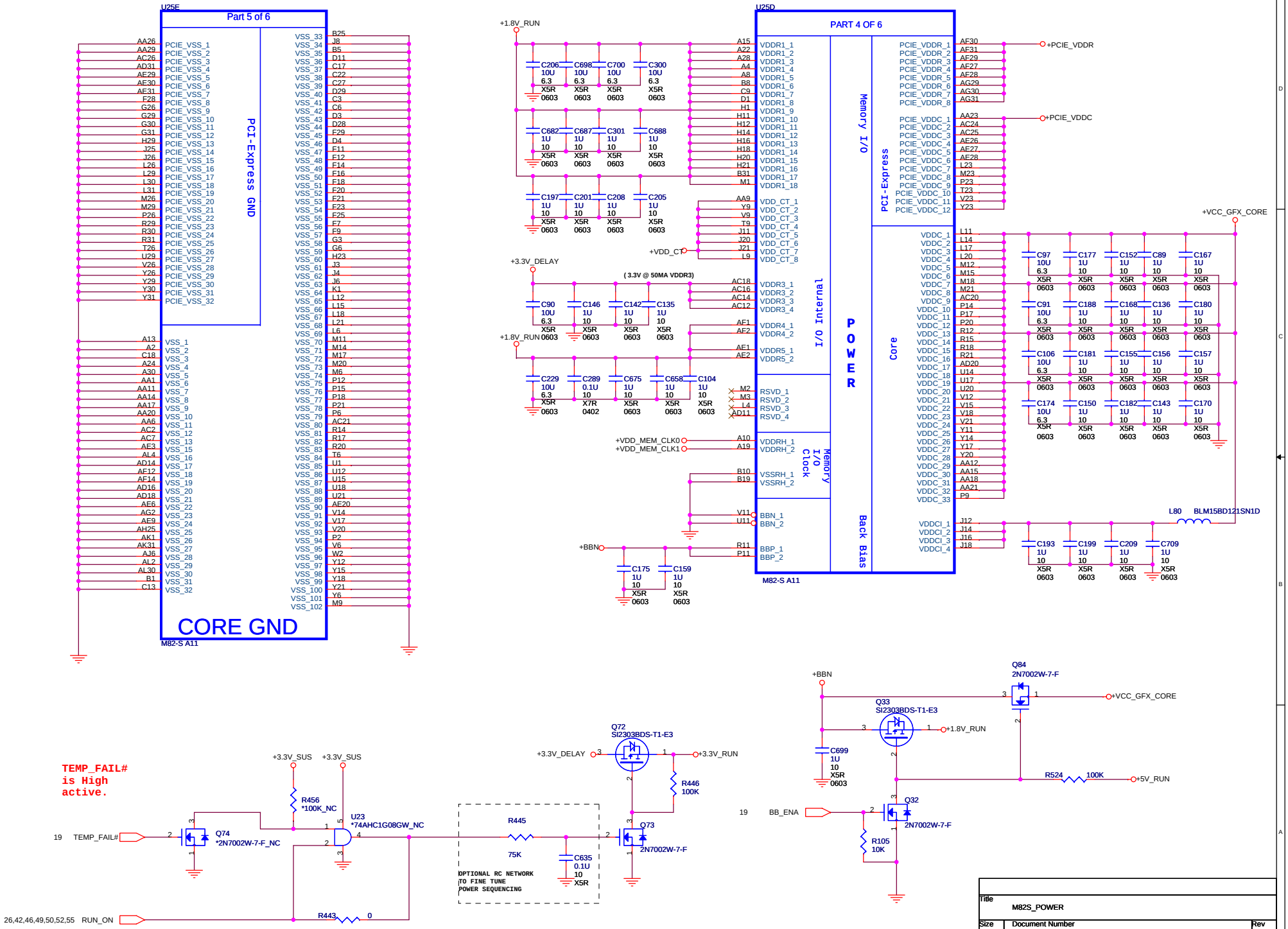
U25E
Part 5 of 6
PCI-Express GND
CORE GND
M82-S A11
U25D
PART 4 OF 6
Memory I/O
PCI-Express
I/O Internal
POWER
Core
Memory I/O Clock
Back Bias
M82-S A11
+1.8V_RUN
+3.3V_DELAY
(3.3V @ 50MA VDDR3)
+VDD_CT
+VDD_MEM_CLK0
+VDD_MEM_CLK1
+BBN
+PCIE_VDDR
+PCIE_VDDC
+VCC_GFX_CORE
L80 BLM15BD121SN1D
TEMP_FAIL#
is High
active.
+3.3V_SUS
R456
*100K_NC
U23
*74AHC1G08GW_NC
Q74
*2N7002W-7-F_NC
19 TEMP_FAIL#
26,42,46,49,50,52,55 RUN_ON
R443 0
Q72
SI2303BDS-T1-E3
+3.3V_RUN
R446
100K
R445
75K
C635
0.1U
Q73
2N7002W-7-F
OPTIONAL RC NETWORK
TO FINE TUNE
POWER SEQUENCING
Q84
2N7002W-7-F
Q33
SI2303BDS-T1-E3
+1.8V_RUN
+VCC_GFX_CORE
C699
1U
R524 100K
+5V_RUN
19 BB_ENA
Q32
2N7002W-7-F
R105
10K
Title
M82S_POWER
Size Custom
Document Number
FX6
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3A
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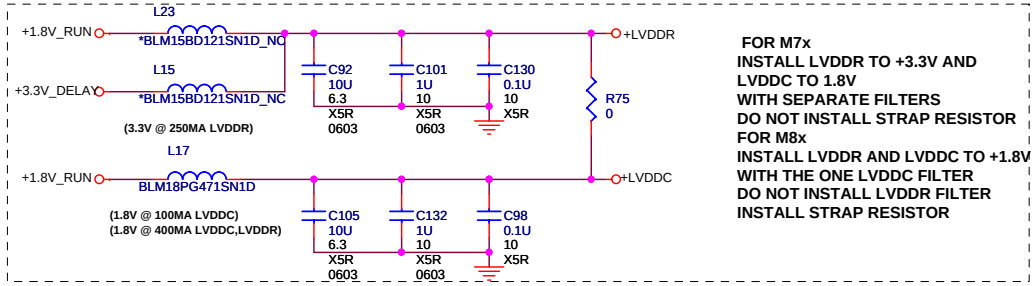
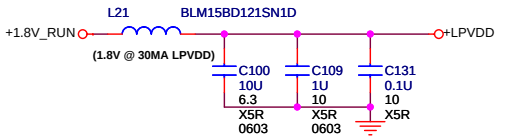
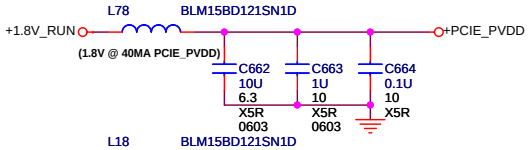
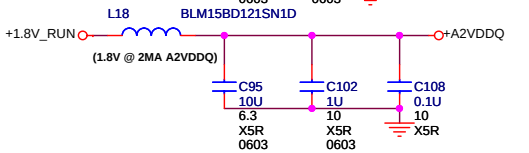
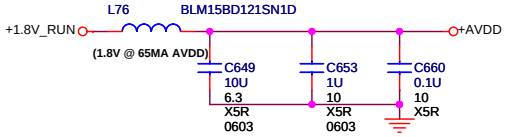
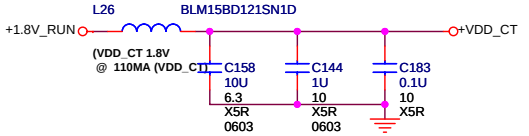


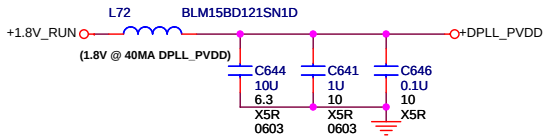


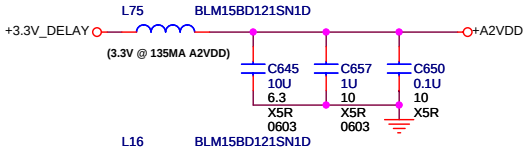


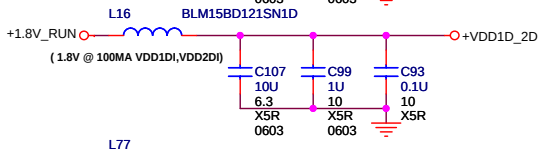


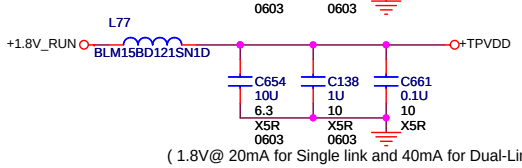




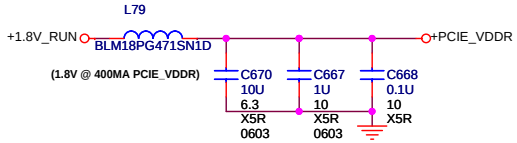


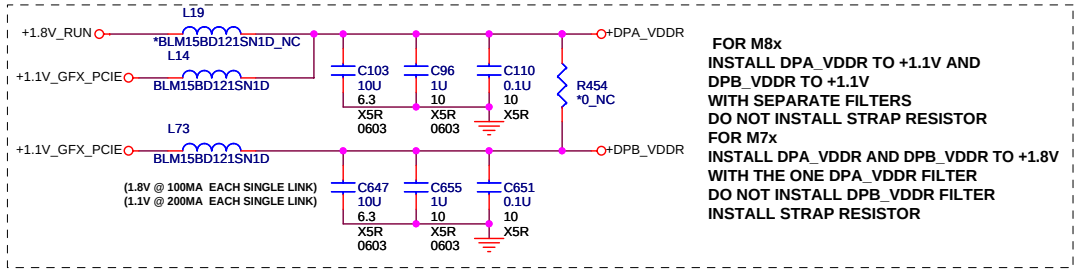


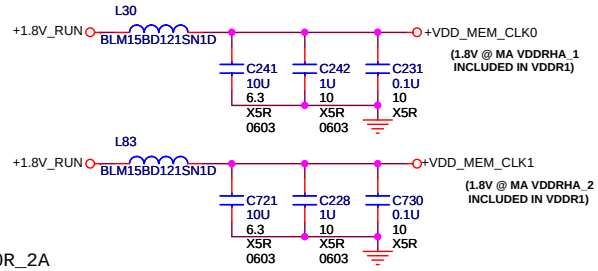




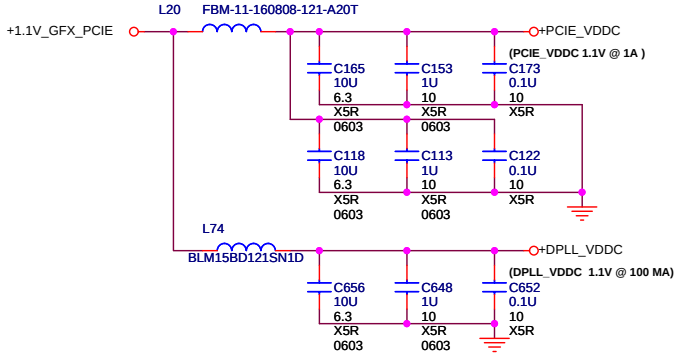
(1.8V@ 20mA for Single link and 40mA for Dual-Link)



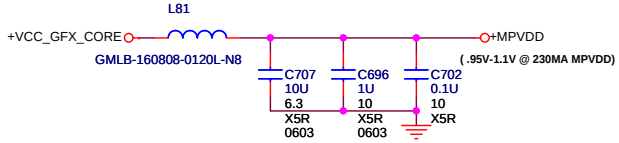




120R_2A



120R_450mA



PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE

QUANTA COMPUTER

Title	M82S_POWER RAIL SELECT
Size	Document Number FX6
Rev	3A
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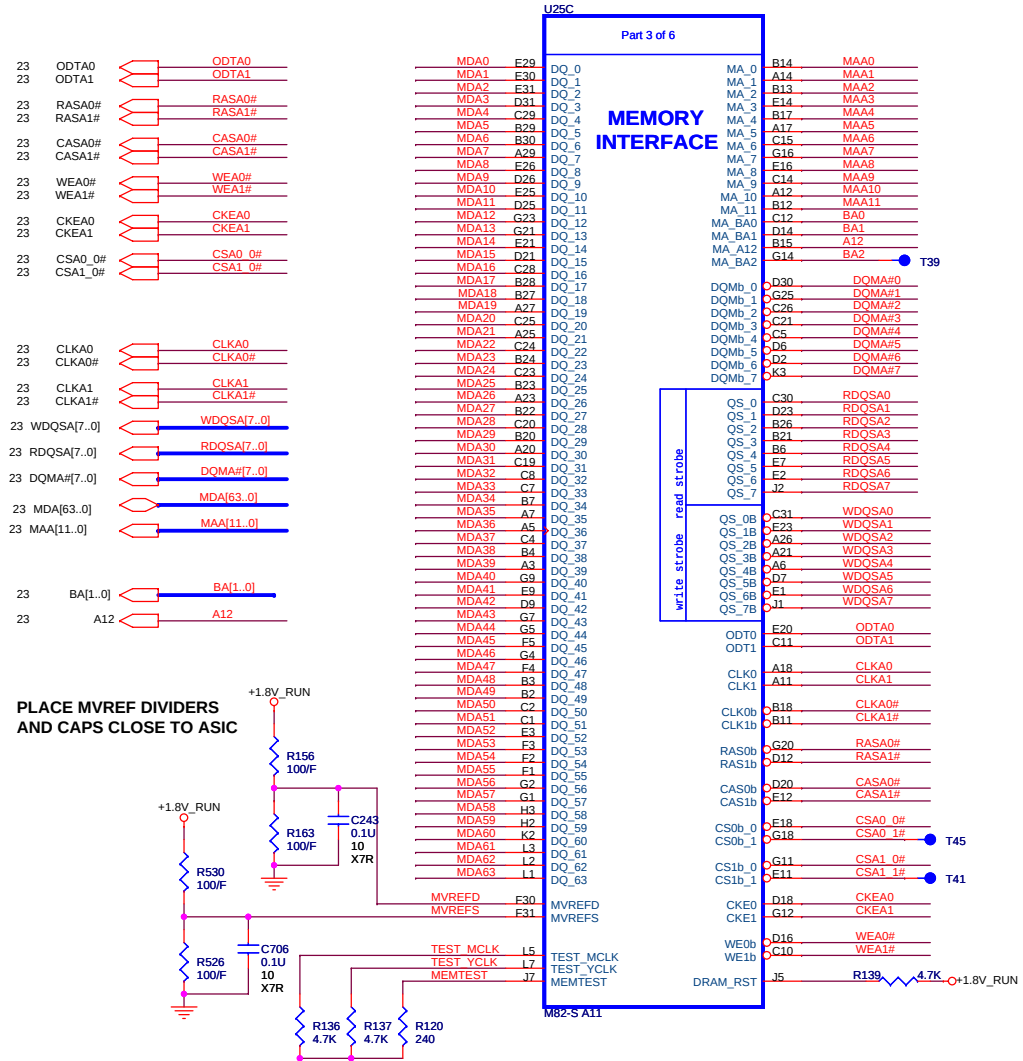
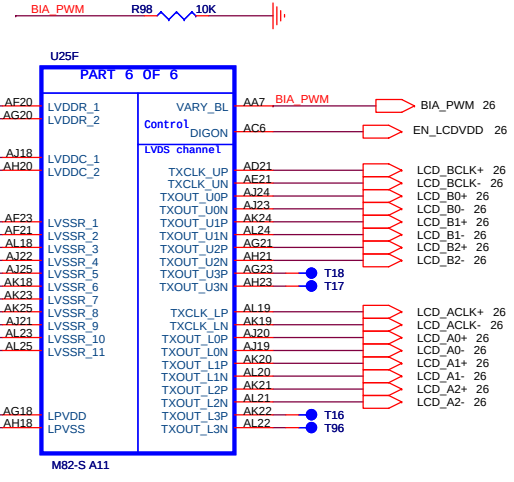
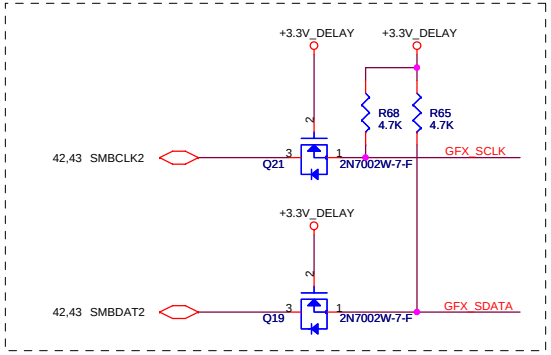




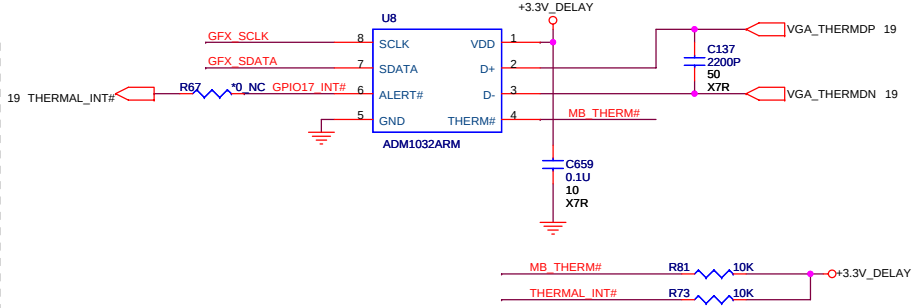
PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

FOR DUAL RANK CONNECTIONS USE THE CSxB_1 CHIP SELECT PINS

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



THERMAL MONITOR



Title	M82S_MEMORY/LVDS/THERM		
Size Custom	Document Number FX6		Rev 3A
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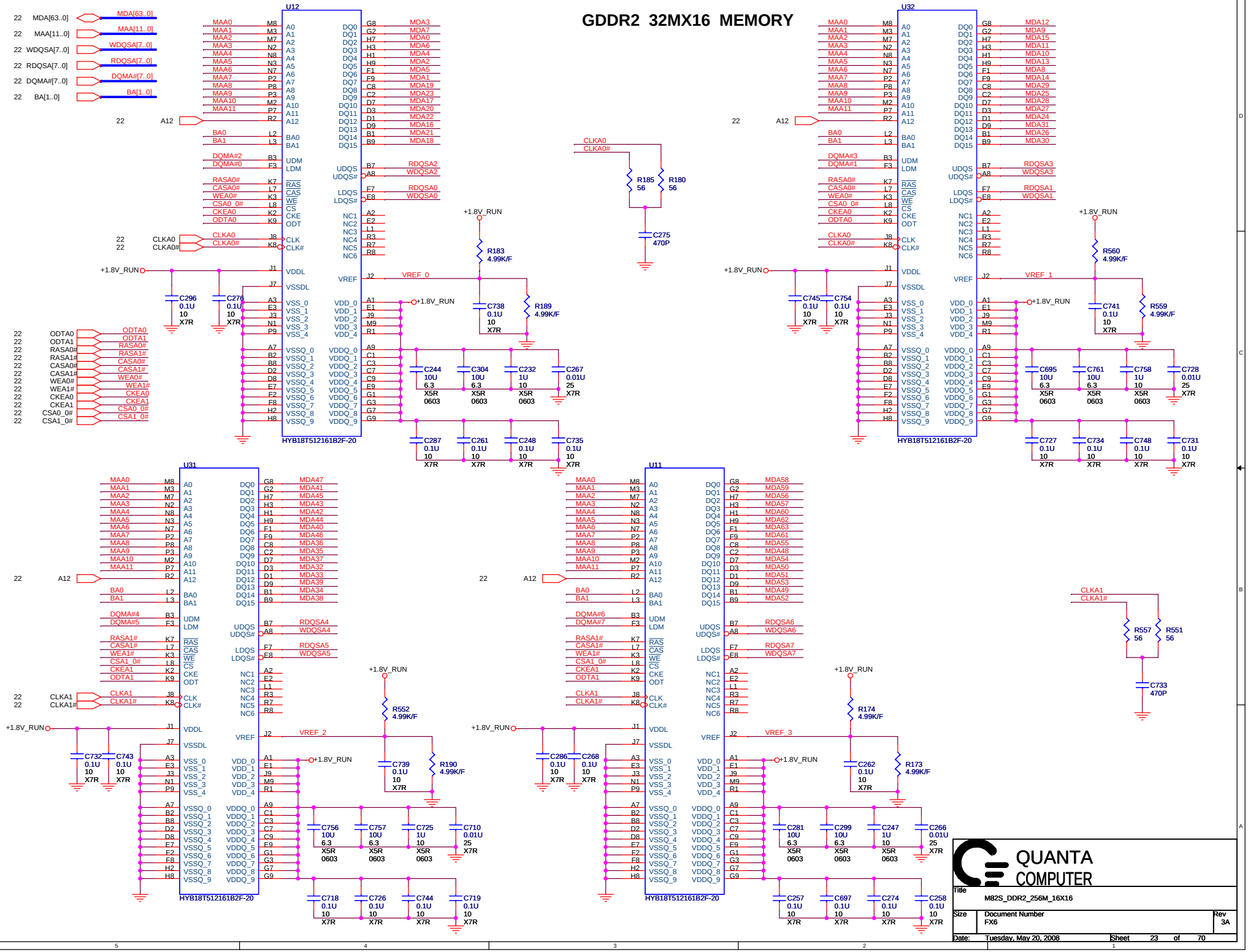
GDDR2 32MX16 MEMORY



BLANK PAGE

Title	LVDS HYBRID	
Size Custom	Document Number FX6	Rev 3A
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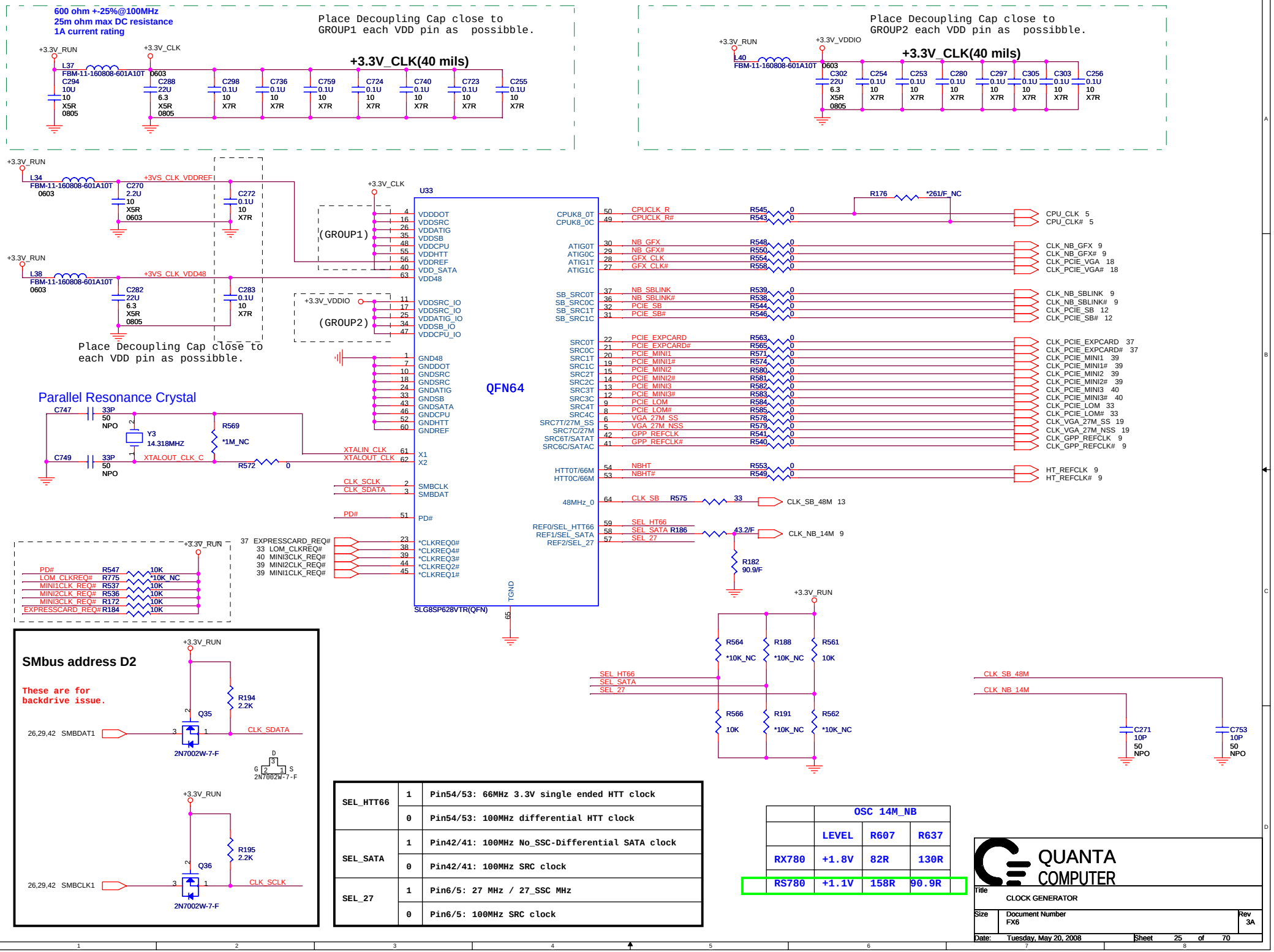

SEL_HTT66	1	Pin54/53: 66MHz 3.3V single ended HTT clock
	0	Pin54/53: 100MHz differential HTT clock
SEL_SATA	1	Pin42/41: 100MHz No_SSC-Differential SATA clock
	0	Pin42/41: 100MHz SRC clock
SEL_27	1	Pin6/5: 27 MHz / 27_SSC MHz
	0	Pin6/5: 100MHz SRC clock

	OSC 14M_NB		
	LEVEL	R607	R637
RX780	+1.8V	82R	130R
RS780	+1.1V	158R	90.9R

QUANTA COMPUTER

Title: CLOCK GENERATOR

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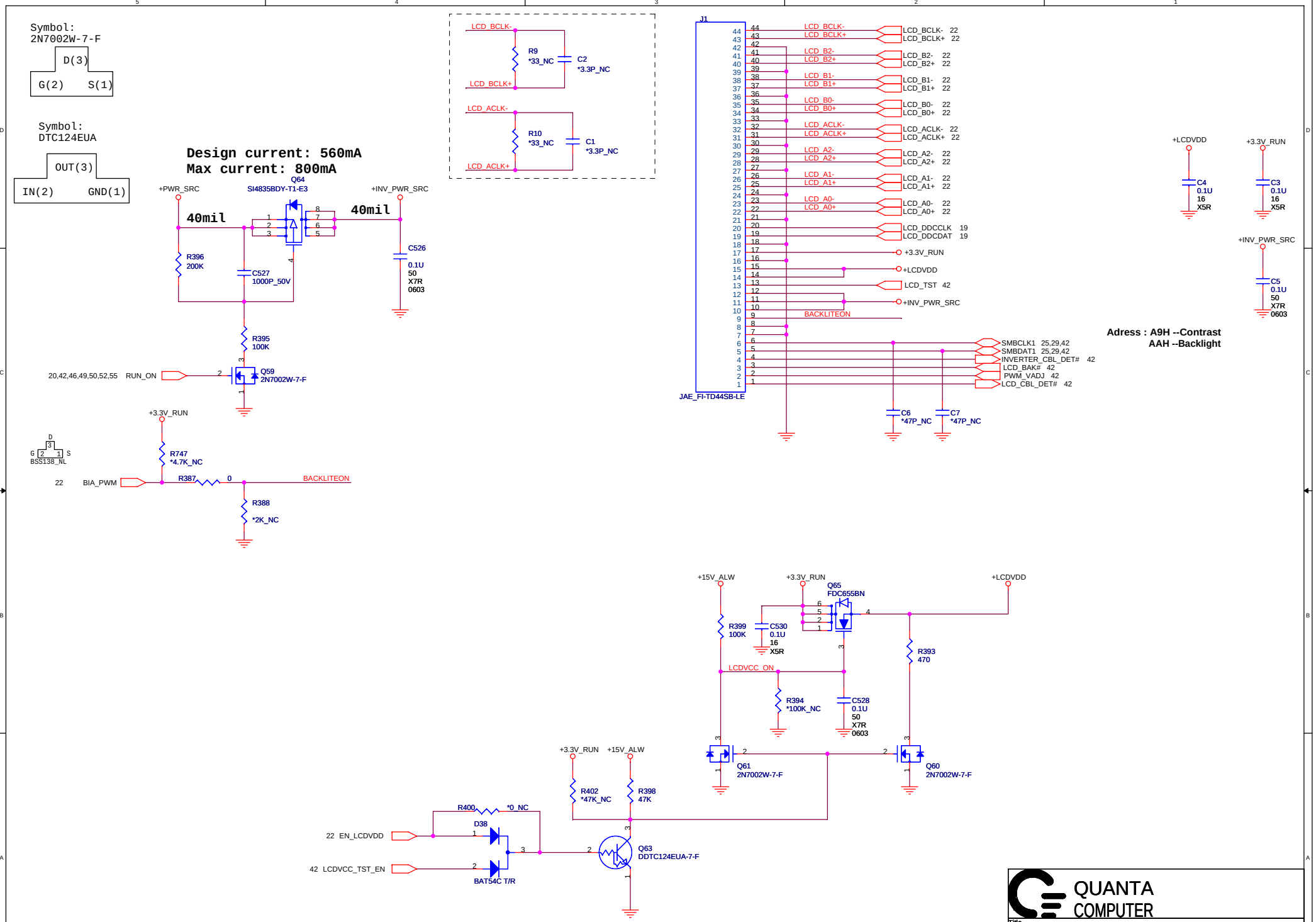
Symbol:
2N7002W-7-F
D(3)
G(2) S(1)
Symbol:
DTC124EUA
OUT(3)
IN(2) GND(1)
Design current: 560mA
Max current: 800mA
Q64
SI4835BDY-T1-E3
+PWR_SRC
+INV_PWR_SRC
40mil
40mil
R396
200K
C527
1000P_50V
C526
0.1U
50
X7R
0603
R395
100K
20,42,46,49,50,52,55 RUN_ON
Q59
2N7002W-7-F
+3.3V_RUN
R747
*4.7K_NC
BSS138_NL
22 BIA_PWM
R387 0
BACKLITEON
R388
*2K_NC
LCD_BCLK-
LCD_BCLK+
R9
*33_NC
C2
*3.3P_NC
LCD_ACLK-
LCD_ACLK+
R10
*33_NC
C1
*3.3P_NC
J1
JAE_FI-TD44SB-LE
LCD_BCLK- 22
LCD_BCLK+ 22
LCD_B2- 22
LCD_B2+ 22
LCD_B1- 22
LCD_B1+ 22
LCD_B0- 22
LCD_B0+ 22
LCD_ACLK- 22
LCD_ACLK+ 22
LCD_A2- 22
LCD_A2+ 22
LCD_A1- 22
LCD_A1+ 22
LCD_A0- 22
LCD_A0+ 22
LCD_DDCCLK 19
LCD_DDCDAT 19
+3.3V_RUN
+LCDVDD
LCD_TST 42
+INV_PWR_SRC
BACKLITEON
SMBCLK1 25,29,42
SMBDAT1 25,29,42
INVERTER_CBL_DET# 42
LCD_BAK# 42
PWM_VADJ 42
LCD_CBL_DET# 42
C6
*47P_NC
C7
*47P_NC
+LCDVDD
C4
0.1U
16
X5R
+3.3V_RUN
C3
0.1U
16
X5R
+INV_PWR_SRC
C5
0.1U
50
X7R
0603
Adress : A9H --Contrast
AAH --Backlight
+15V_ALW
+3.3V_RUN
Q65
FDC655BN
+LCDVDD
R399
100K
C530
0.1U
16
X5R
R393
470
LCDVCC_ON
R394
*100K_NC
C528
0.1U
50
X7R
0603
Q61
2N7002W-7-F
Q60
2N7002W-7-F
+3.3V_RUN +15V_ALW
R402
*47K_NC
R398
47K
R400 *0_NC
D38
22 EN_LCDVDD
42 LCDVCC_TST_EN
BAT54C T/R
Q63
DDTC124EUA-7-F
QUANTA
COMPUTER
Title
LCD CONN,CK-SSCD
Size
Document Number
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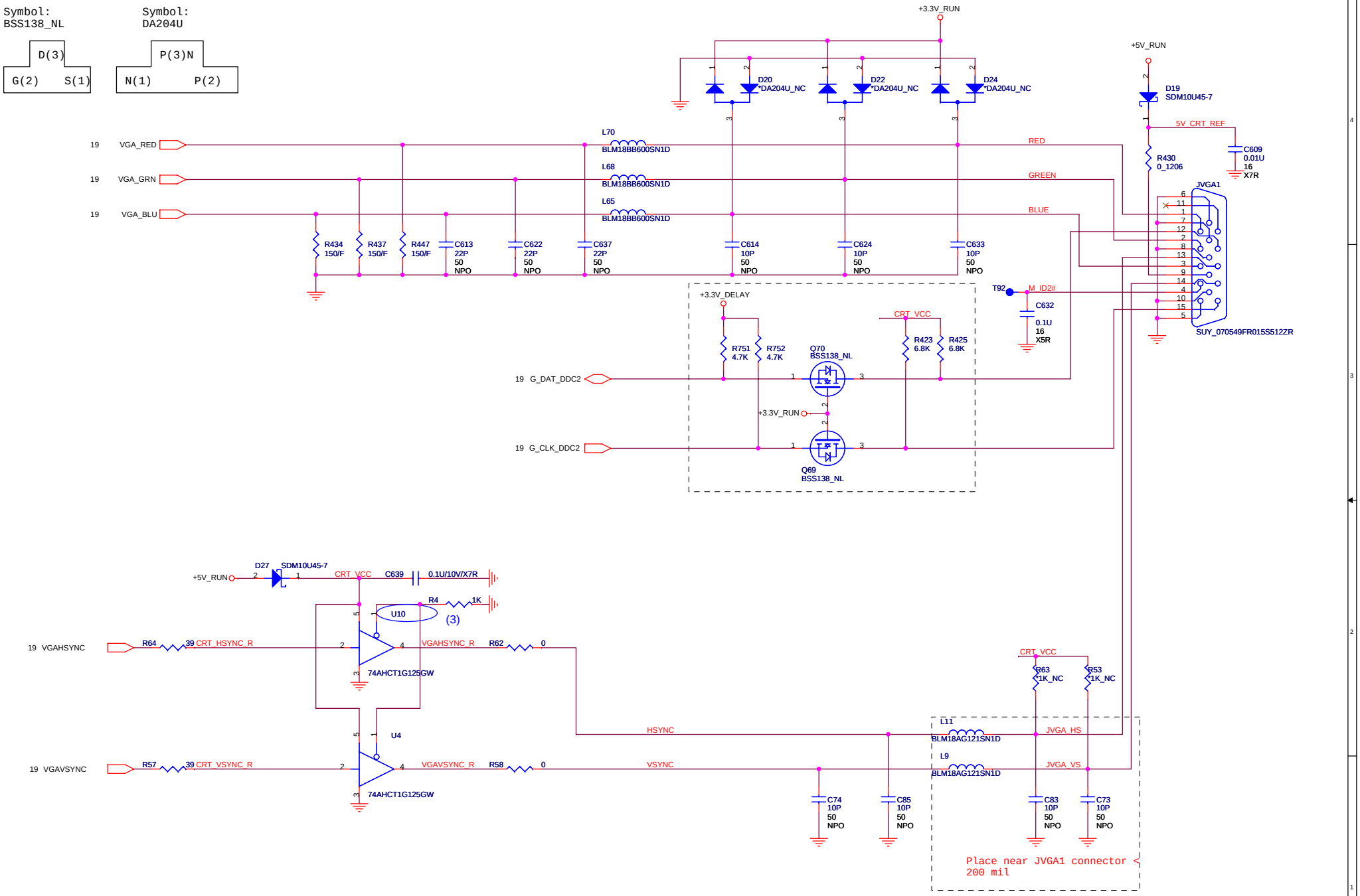

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Title	CRT CONN	
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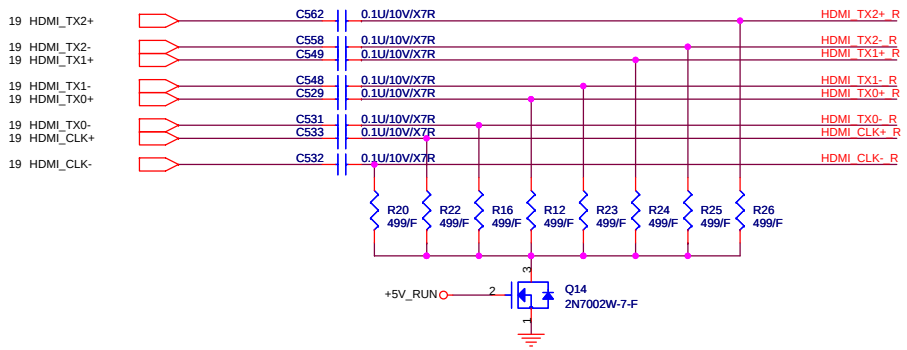
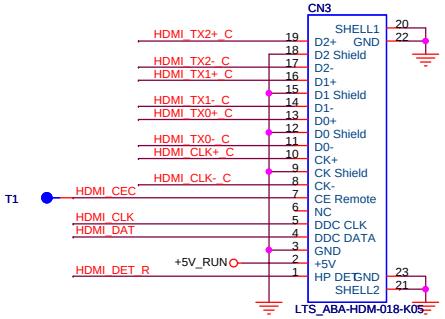
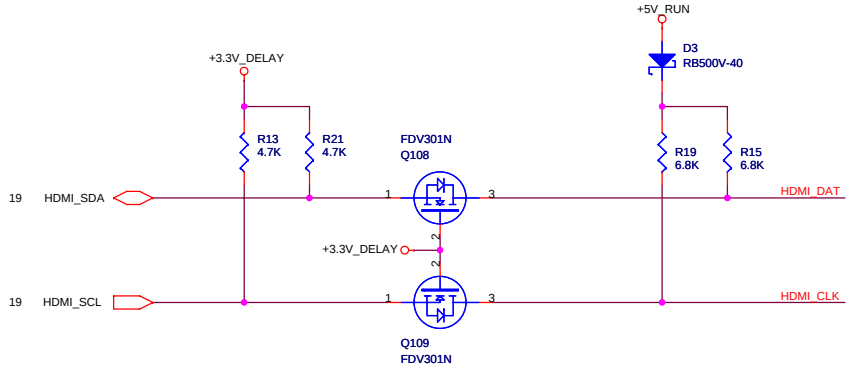
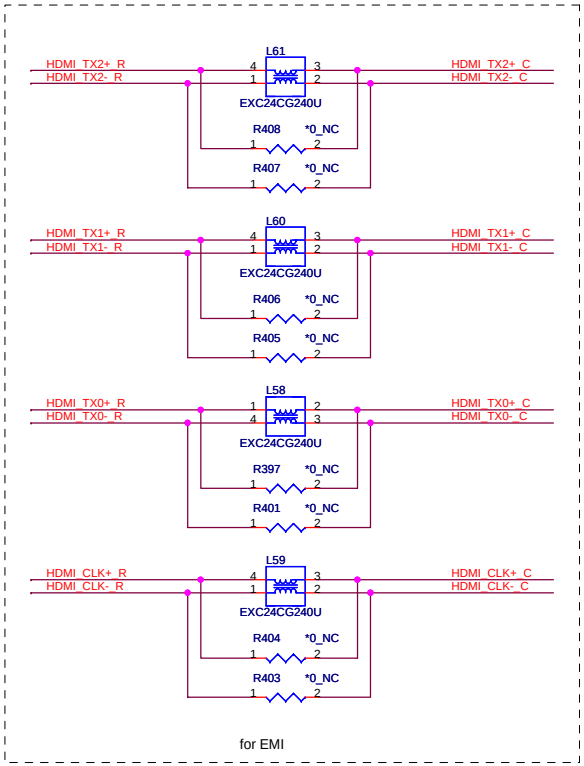
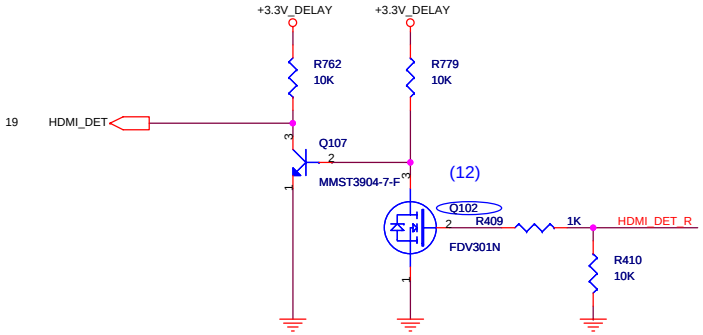
HDMI Connector











QUANTA COMPUTER

Title	HDMI	
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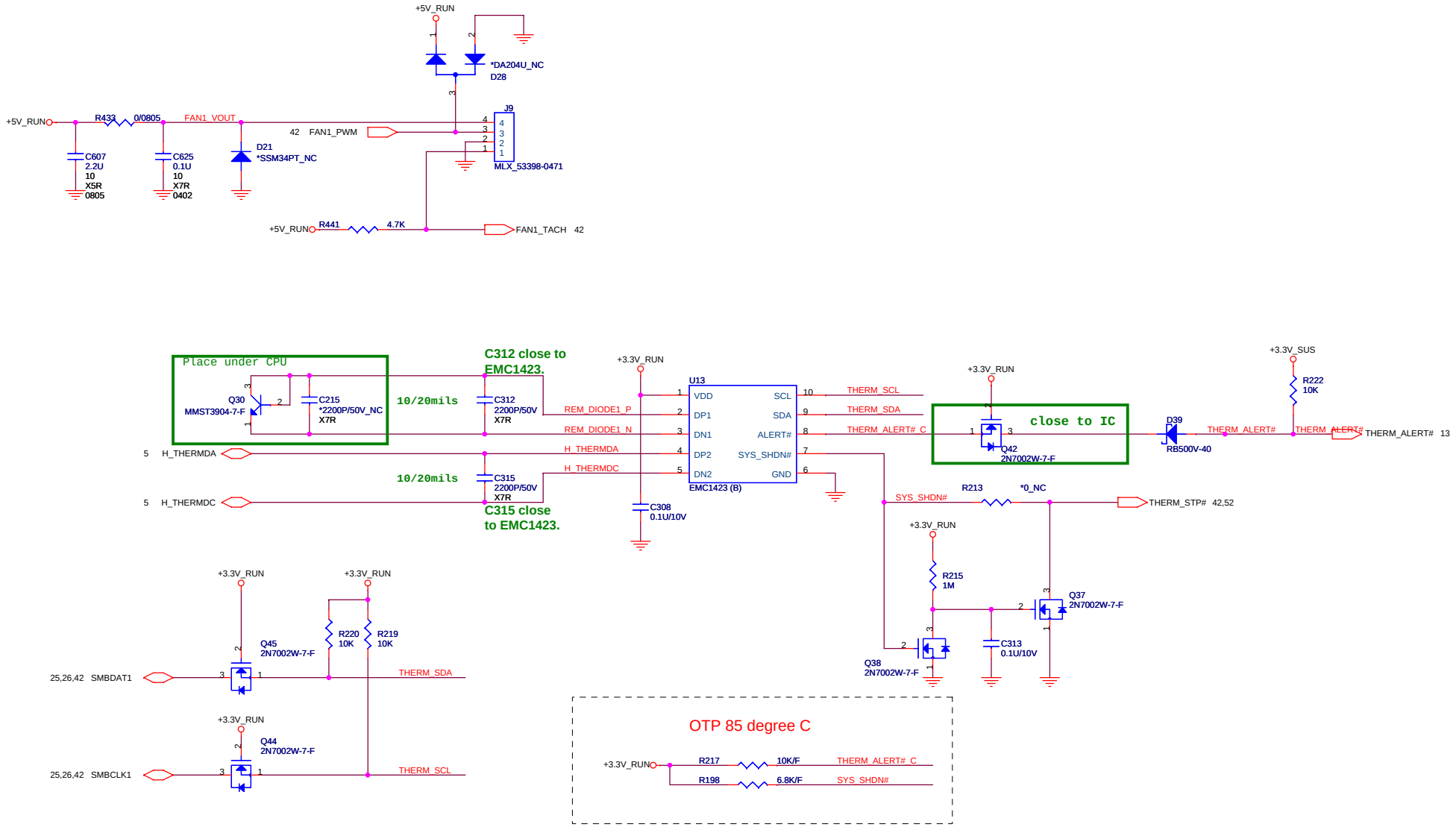

QUANTA COMPUTER

Title	FAN/THERMAL	
Size	Document Number FX6	Rev 3A
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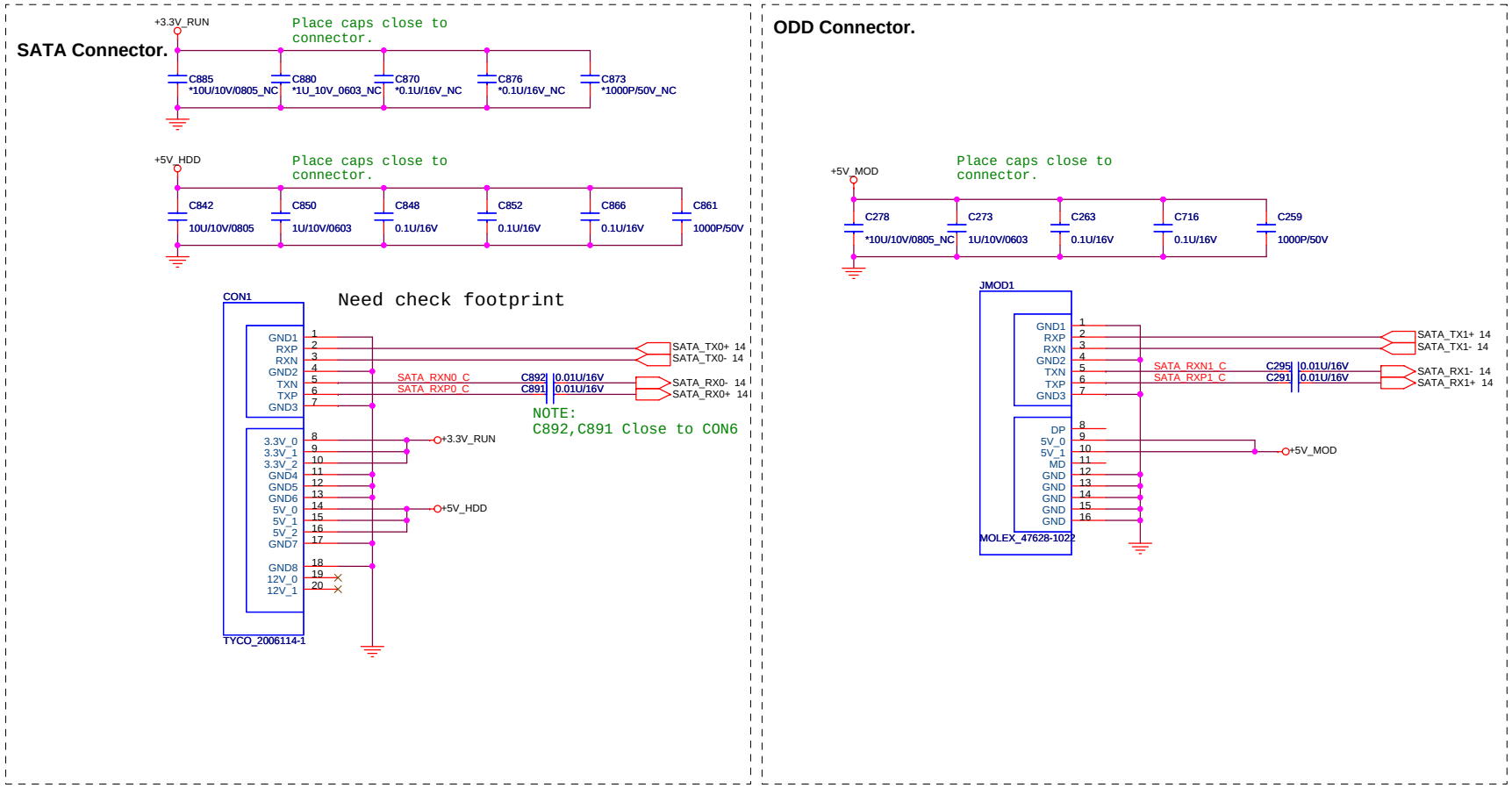
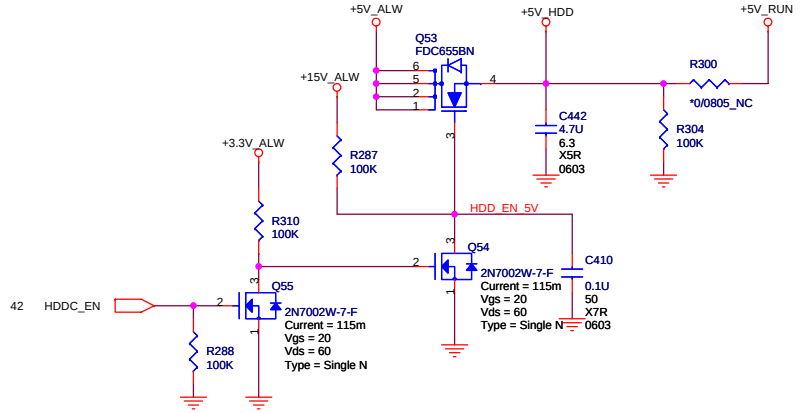
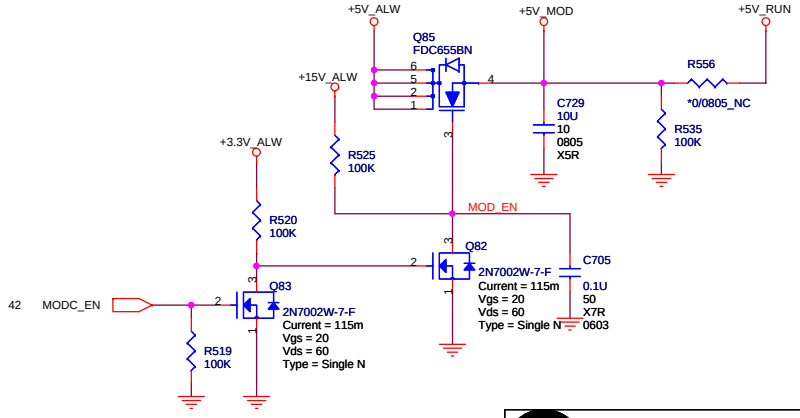


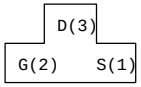
Design current: 1050mA
Max current: 1500mA

Design current: 700mA
Max current: 1000mA





Symbol:
2N7002W-7-F



QUANTA COMPUTER

Title	SATA (HDD&CD_ROM)	
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GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

INTERNAL SPEAKER AMP

	TPA6040	MAX9789
C922	Pop	Depop
R713	Depop	Pop

AZALIA (HD) CODEC

U40 TPA6040A4 QFN 32PIN

U41 92HD73C/STAC9228

Layout Note: Place close U40 pin 30.

Layout Note: Close to U41 Pin 34

Layout Note: Place close to pin 18.

Layout Note: Place close U40.

Layout Note: Close to U41 Pin 13

Depop R710,C920 for using 92HD73C

Depop R734, R732, R711,R740
Pop R741, R716, R731 ,R742
for using 92HD73C
R732,R741 close to U41, Let DVDD width be 10-mils

	TPA6040	MAX9789
C926	Pop	Depop
R718	Depop	Pop

Layout Note: Place close to U40 pin 8.

Close to U41.

EMI Request

QUANTA COMPUTER

Title: AZALIA(HD) CODEC

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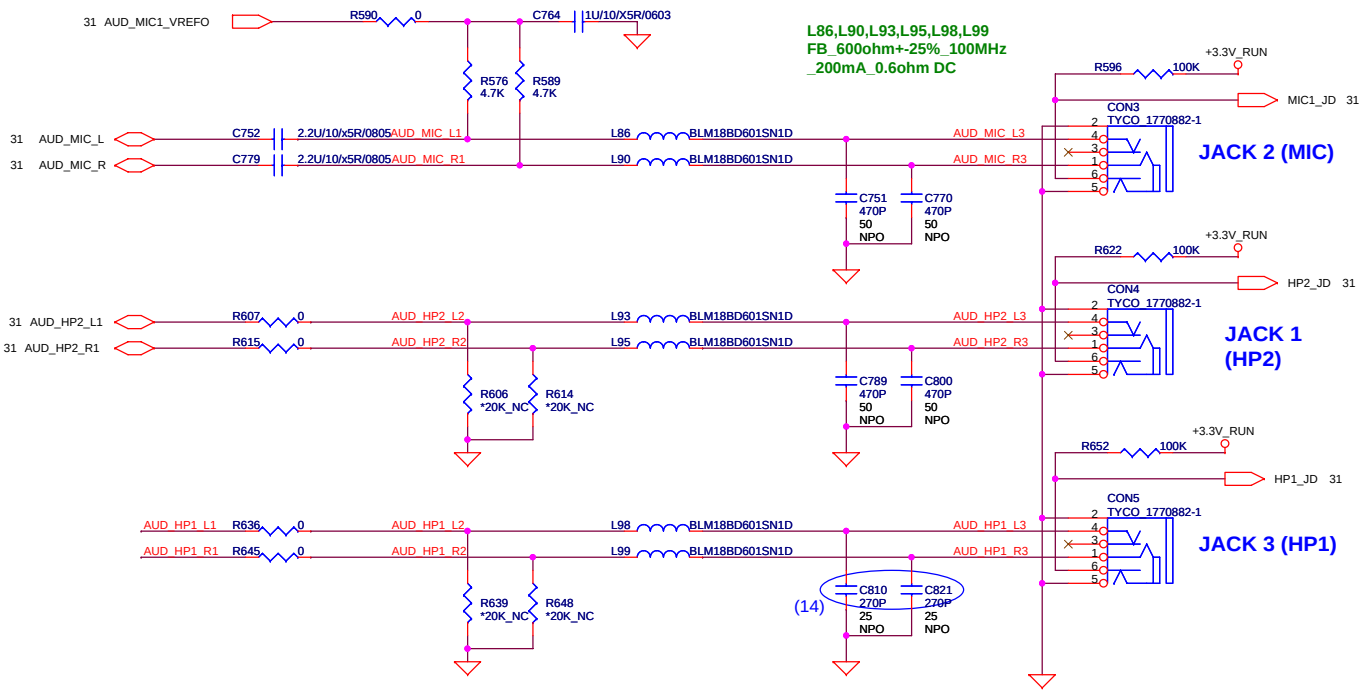
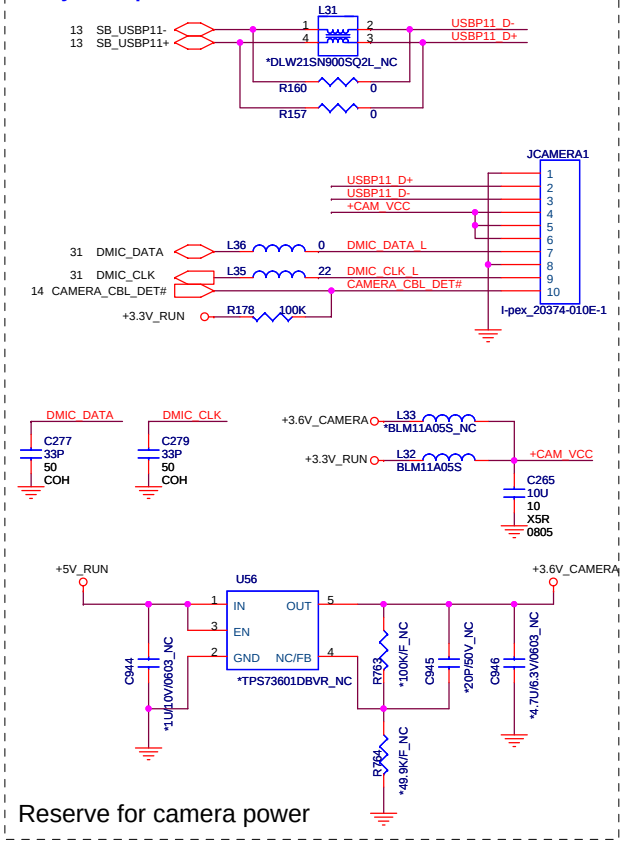
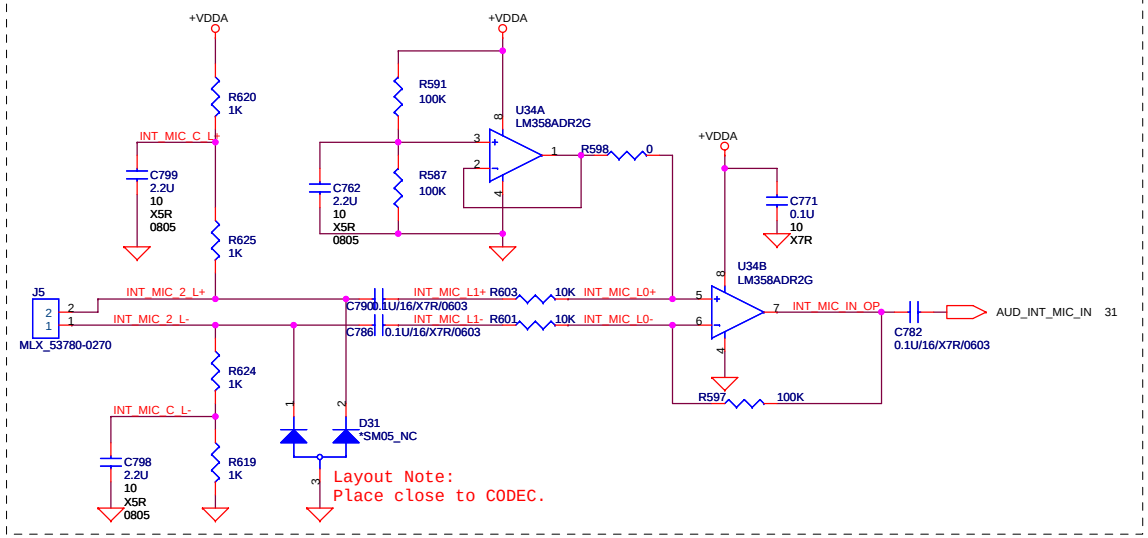
Headphone Jack
Stereo MIC Jack

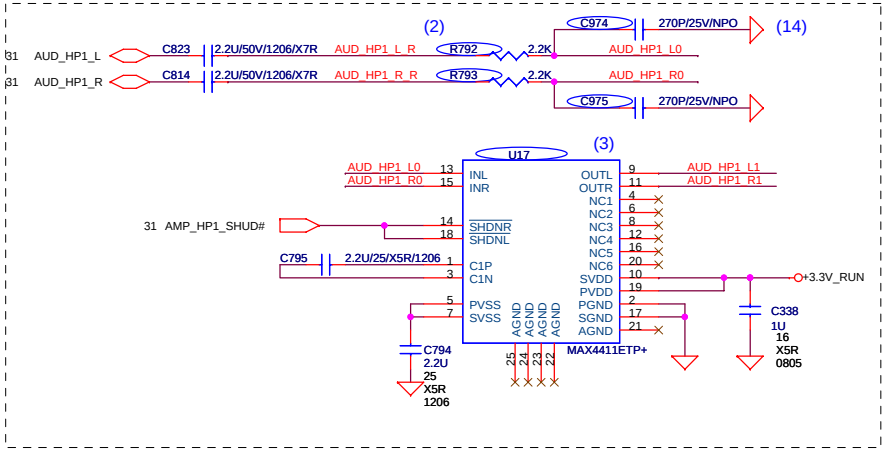


Array Microphone & Camera



Reserve for camera power





QUANTA COMPUTER

Title	AUDIO CONN	
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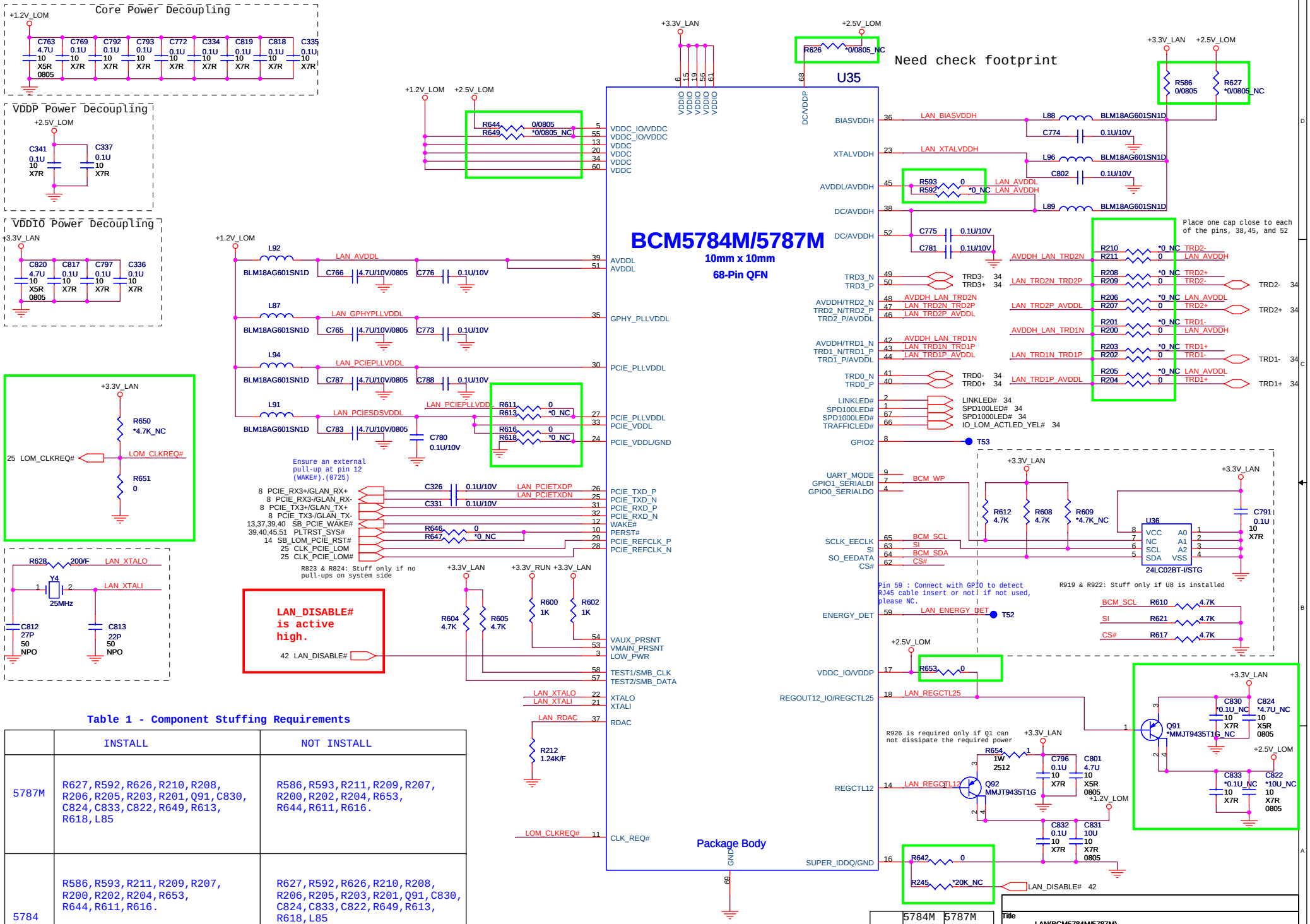

Table 1 - Component Stuffing Requirements

	INSTALL	NOT INSTALL
5787M	R627,R592,R626,R210,R208,R206,R205,R203,R201,Q91,C830,C824,C833,C822,R649,R613,R618,L85	R586,R593,R211,R209,R207,R200,R202,R204,R653,R644,R611,R616.
5784	R586,R593,R211,R209,R207,R200,R202,R204,R653,R644,R611,R616.	R627,R592,R626,R210,R208,R206,R205,R203,R201,Q91,C830,C824,C833,C822,R649,R613,R618,L85

	5784M	5787M
R642	39k	0
R245	20k	*20k_NC

Title	LAN(BCM5784M/5787M)
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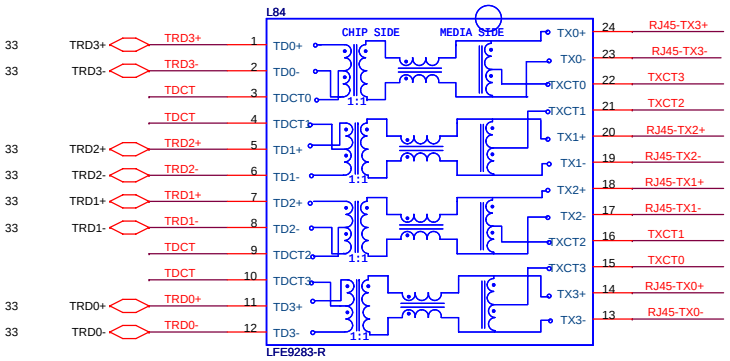
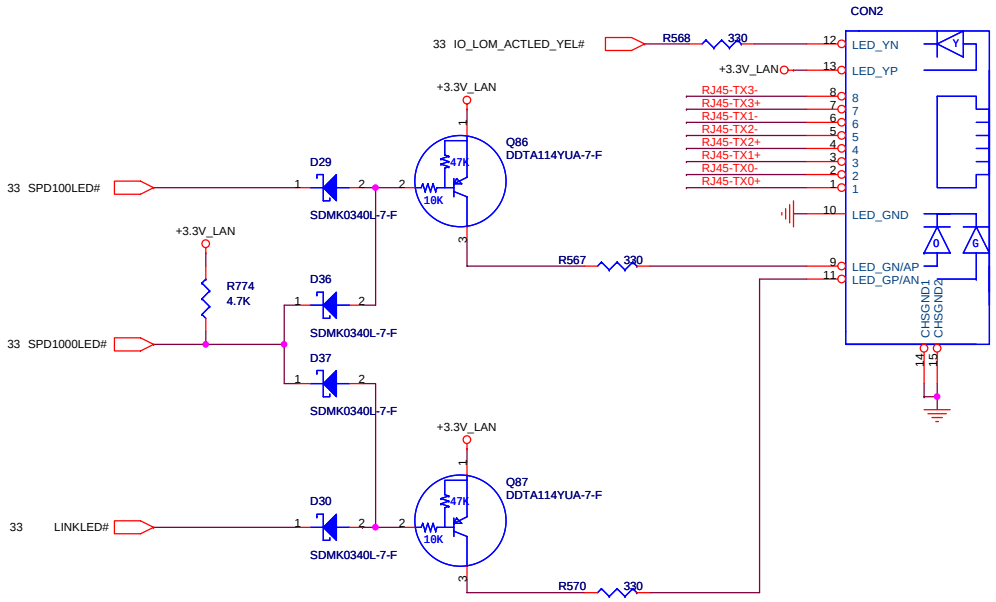
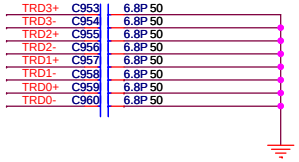
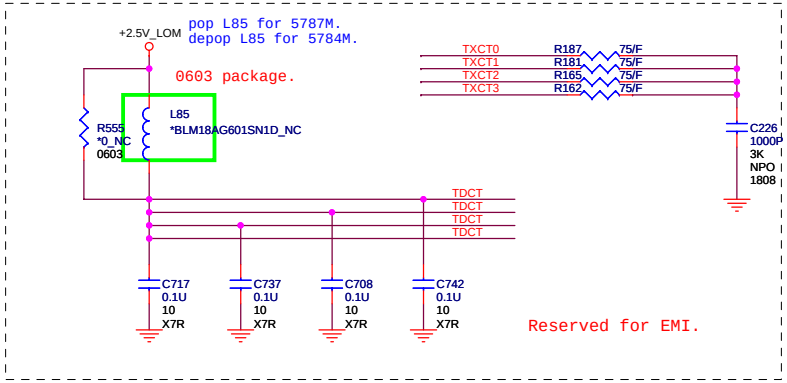
RJ-45 Connector

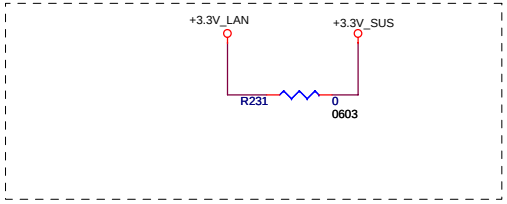
TRANSFORM











QUANTA COMPUTER

Title	LAN SWITCH	
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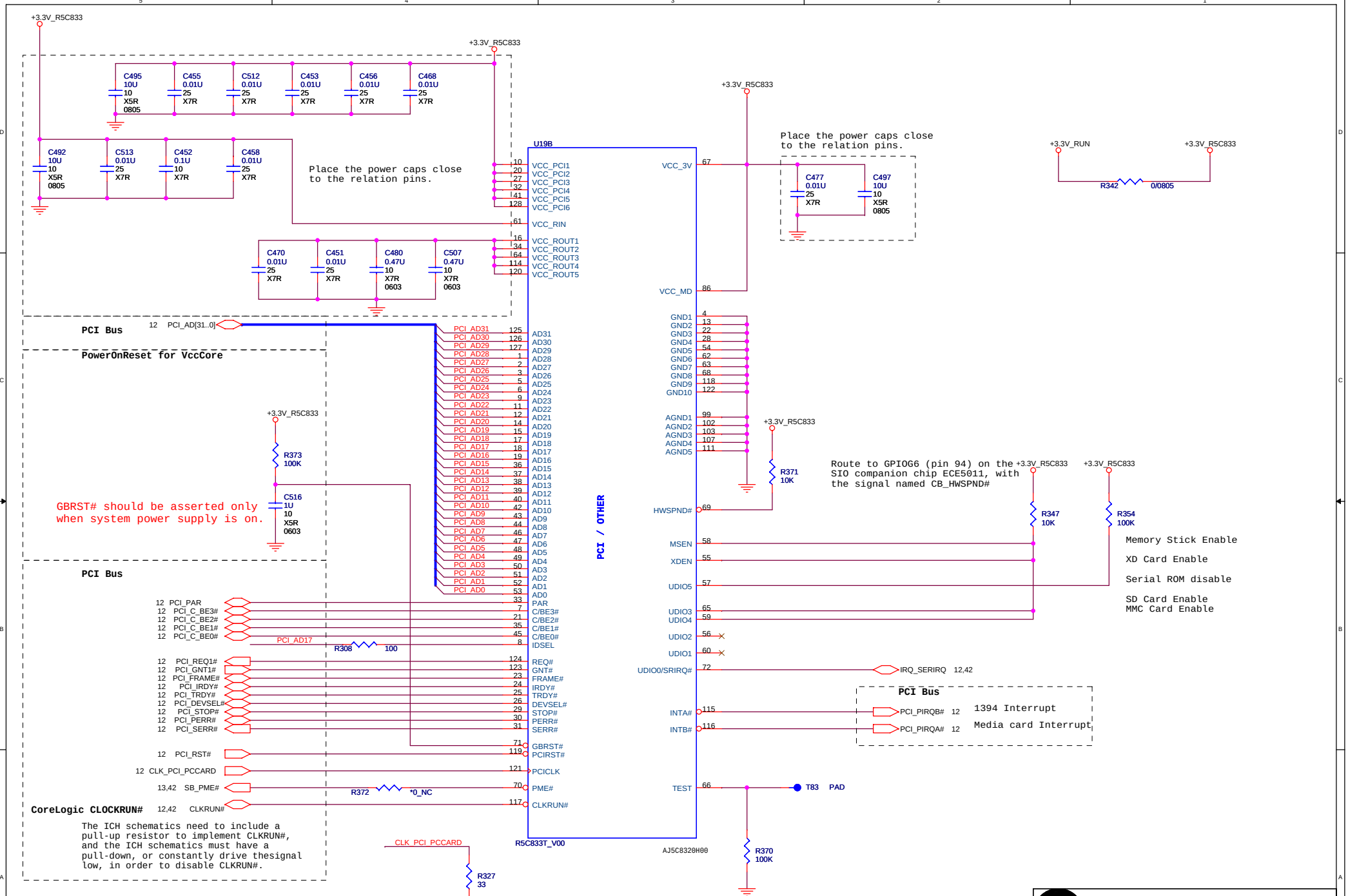
+3.3V_R5C833
C495 10U 10 X5R 0805
C455 0.01U 25 X7R
C512 0.01U 25 X7R
C453 0.01U 25 X7R
C456 0.01U 25 X7R
C468 0.01U 25 X7R
C492 10U 10 X5R 0805
C513 0.01U 25 X7R
C452 0.1U 10 X7R
C458 0.01U 25 X7R
Place the power caps close to the relation pins.
C470 0.01U 25 X7R
C451 0.01U 25 X7R
C480 0.47U 10 X7R 0603
C507 0.47U 10 X7R 0603
U19B
VCC_PCI1
VCC_PCI2
VCC_PCI3
VCC_PCI4
VCC_PCI5
VCC_PCI6
VCC_RIN
VCC_ROUT1
VCC_ROUT2
VCC_ROUT3
VCC_ROUT4
VCC_ROUT5
VCC_3V
VCC_MD
C477 0.01U 25 X7R
C497 10U 10 X5R 0805
+3.3V_RUN
R342 0/0805
PCI Bus
12 PCI_AD[31..0]
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_AD23
PCI_AD22
PCI_AD21
PCI_AD20
PCI_AD19
PCI_AD18
PCI_AD17
PCI_AD16
PCI_AD15
PCI_AD14
PCI_AD13
PCI_AD12
PCI_AD11
PCI_AD10
PCI_AD9
PCI_AD8
PCI_AD7
PCI_AD6
PCI_AD5
PCI_AD4
PCI_AD3
PCI_AD2
PCI_AD1
PCI_AD0
PCI / OTHER
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
AGND1
AGND2
AGND3
AGND4
AGND5
R371 10K
PowerOnReset for VccCore
R373 100K
C516 1U 10 X5R 0603
GBRST# should be asserted only when system power supply is on.
HWSPND#
Route to GPIOG6 (pin 94) on the SIO companion chip ECE5011, with the signal named CB_HWSPND#
R347 10K
R354 100K
MSEN
XDEN
UDIO5
UDIO3
UDIO4
UDIO2
UDIO1
UDIO0/SRIRQ#
IRQ_SERIRQ 12,42
Memory Stick Enable
XD Card Enable
Serial ROM disable
SD Card Enable
MMC Card Enable
PCI Bus
12 PCI_PAR
12 PCI_C_BE3#
12 PCI_C_BE2#
12 PCI_C_BE1#
12 PCI_C_BE0#
PCI_AD17
R308 100
12 PCI_REQ1#
12 PCI_GNT1#
12 PCI_FRAME#
12 PCI_IRDY#
12 PCI_TRDY#
12 PCI_DEVSEL#
12 PCI_STOP#
12 PCI_PERR#
12 PCI_SERR#
12 PCI_RST#
12 CLK_PCI_PCCARD
13,42 SB_PME#
R372 *0_NC
CoreLogic CLOCKRUN#
12,42 CLKRUN#
The ICH schematics need to include a pull-up resistor to implement CLKRUN#, and the ICH schematics must have a pull-down, or constantly drive thesignal low, in order to disable CLKRUN#.
INTA#
INTB#
PCI_PIRQB# 12
PCI_PIRQA# 12
1394 Interrupt
Media card Interrupt
TEST
T83 PAD
R5C833T_V00
AJ5C8320H00
CLK_PCI_PCCARD
R327 33
C475 12P 50 COG
R370 100K
QUANTA COMPUTER
Title
R5C833/PCI
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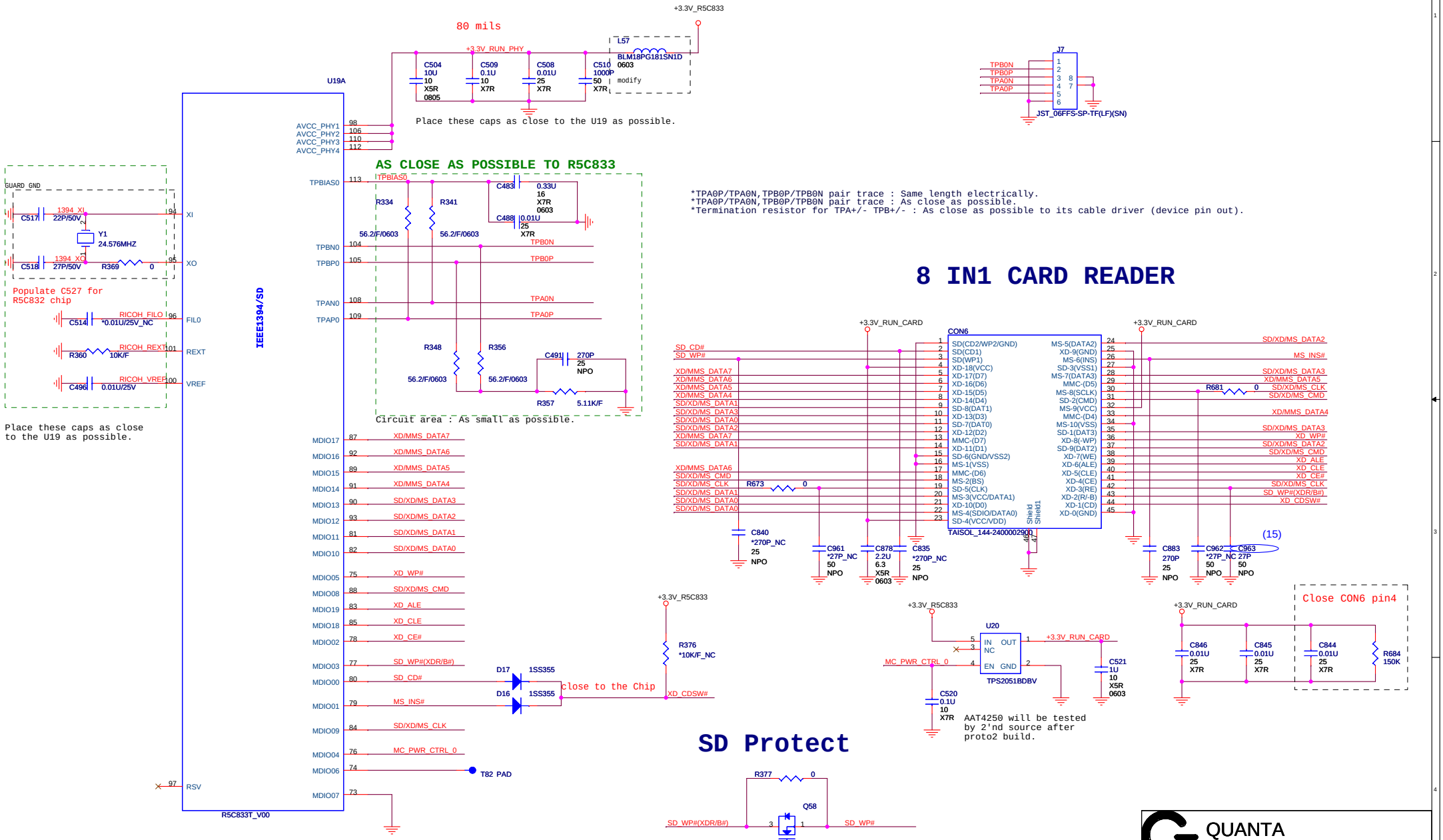
8 IN1 CARD READER
SD Protect
IEEE1394/SD
U19A
R5C833T_V00
80 mils
+3.3V_RUN_PHY
+3.3V_R5C833
L57
BLM18PG181SN1D
0603
modify
C504 10U 10 X5R 0805
C509 0.1U 10 X7R
C508 0.01U 25 X7R
C510 1000P 50 X7R
Place these caps as close to the U19 as possible.
AS CLOSE AS POSSIBLE TO R5C833
Circuit area : As small as possible.
GUARD_GND
C517 1394_XI 22P/50V
Y1 24.576MHZ
C518 1394_XO 27P/50V
R369 0
Populate C527 for R5C832 chip
C514 RICOH_FILO *0.01U/25V_NC
R360 RICOH_REXT 10K/F
C496 RICOH_VREF 0.01U/25V
Place these caps as close to the U19 as possible.
R334 56.2/F/0603
R341 56.2/F/0603
C483 0.33U 16 X7R 0603
C488 0.01U 25 X7R
R348 56.2/F/0603
R356 56.2/F/0603
C491 270P 25 NPO
R357 5.11K/F
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).
J7
JST_06FFS-SP-TF(LF)(SN)
+3.3V_RUN_CARD
CON6
TAISOL_144-2400002900
C840 *270P_NC 25 NPO
C961 *27P_NC 50 NPO
C878 2.2U 6.3 X5R 0603
C835 *270P_NC 25 NPO
C883 270P 25 NPO
C962 *27P_NC 50 NPO
C963 27P 50 NPO
R673 0
R681 0
(15)
R376 *10K/F_NC
D17 1SS355
D16 1SS355
close to the Chip
T82 PAD
U20
TPS2051BDBV
MC_PWR_CTL_0
C520 0.1U 10 X7R
C521 1U 10 X5R 0603
AAT4250 will be tested by 2'nd source after proto2 build.
Close CON6 pin4
C846 0.01U 25 X7R
C845 0.01U 25 X7R
C844 0.01U 25 X7R
R684 150K
R377 0
Q58
*2N7002W-7-F_NC
SD_WP#(XDR/B#)
XD_CDSW#
QUANTA COMPUTER
Title IEEE1394/CARD READER
Size Document Number FX6 Rev 3A
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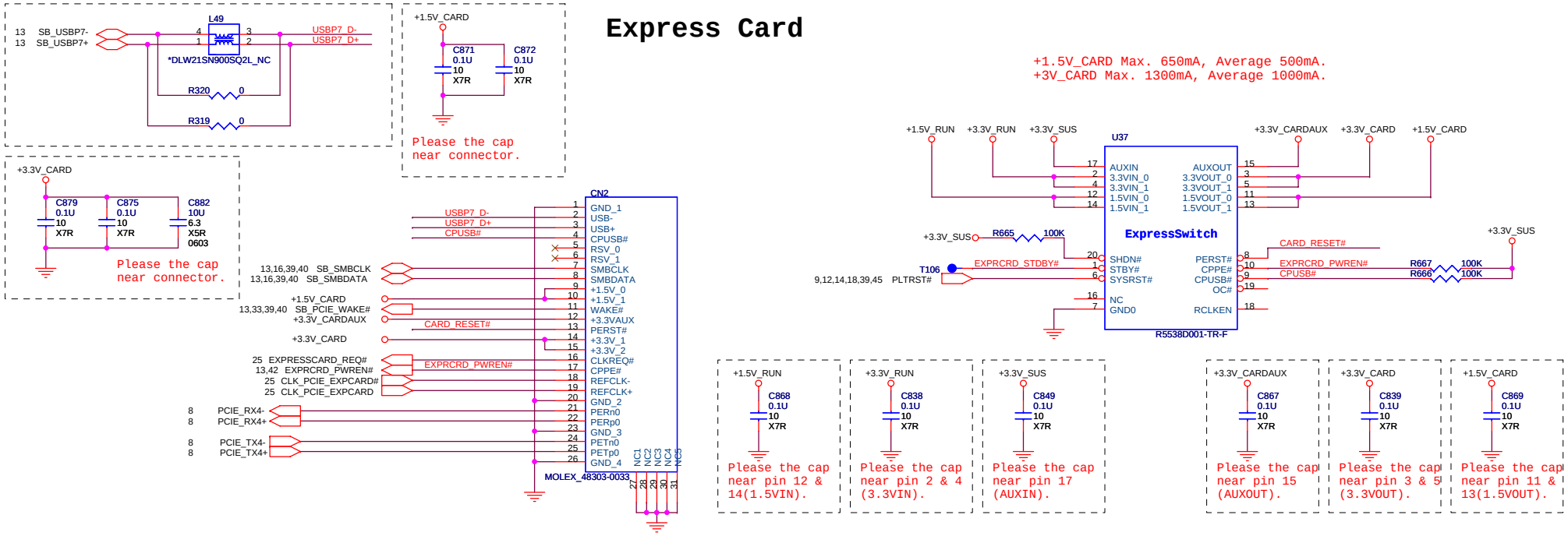
Express Card



QUANTA COMPUTER

Title	EXPRESS		
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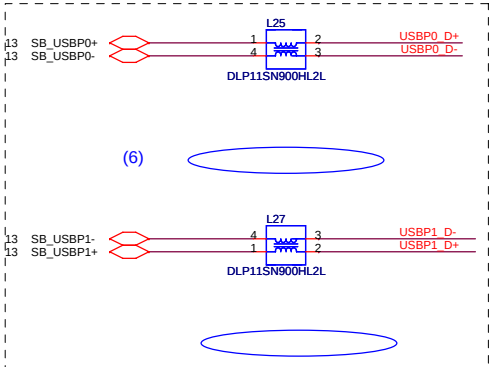
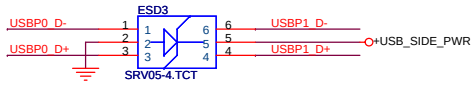
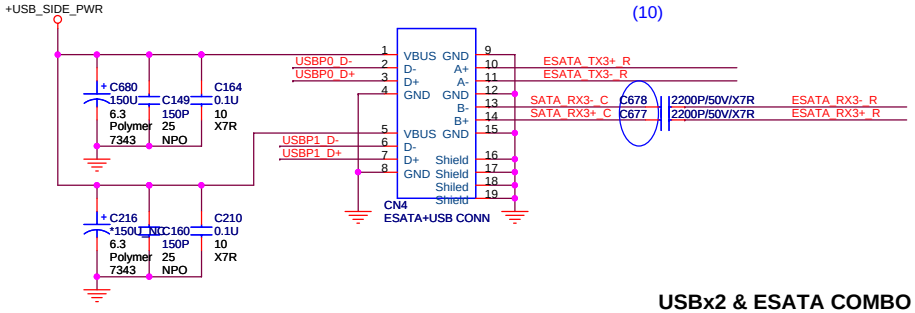
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



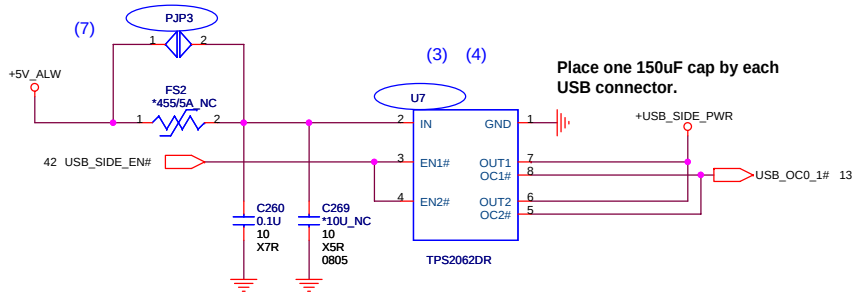
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



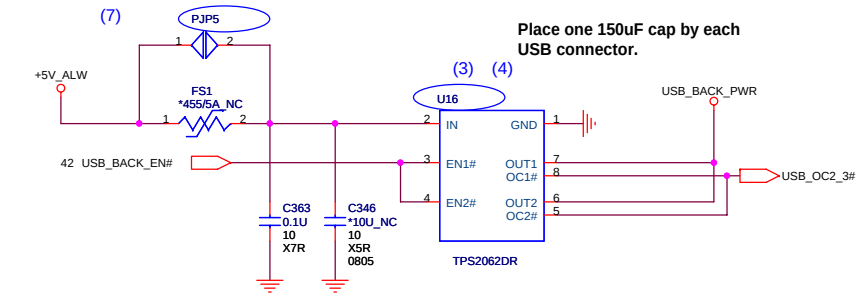
Side External USBX2



USBx2 & ESATA COMBO

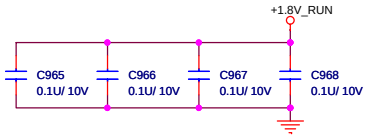


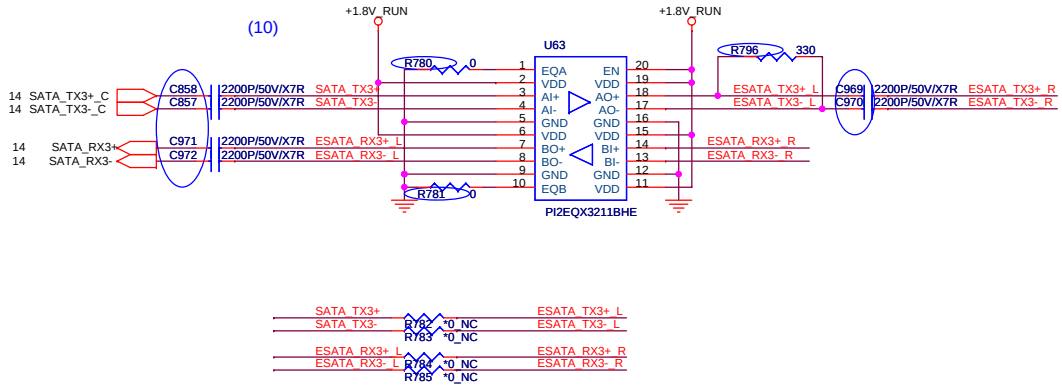
Place one 150uF cap by each USB connector.



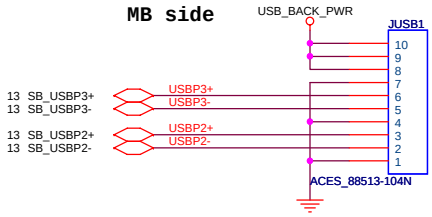
Place one 150uF cap by each USB connector.

E-SATA Re-driver





MB side



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Title	USB	
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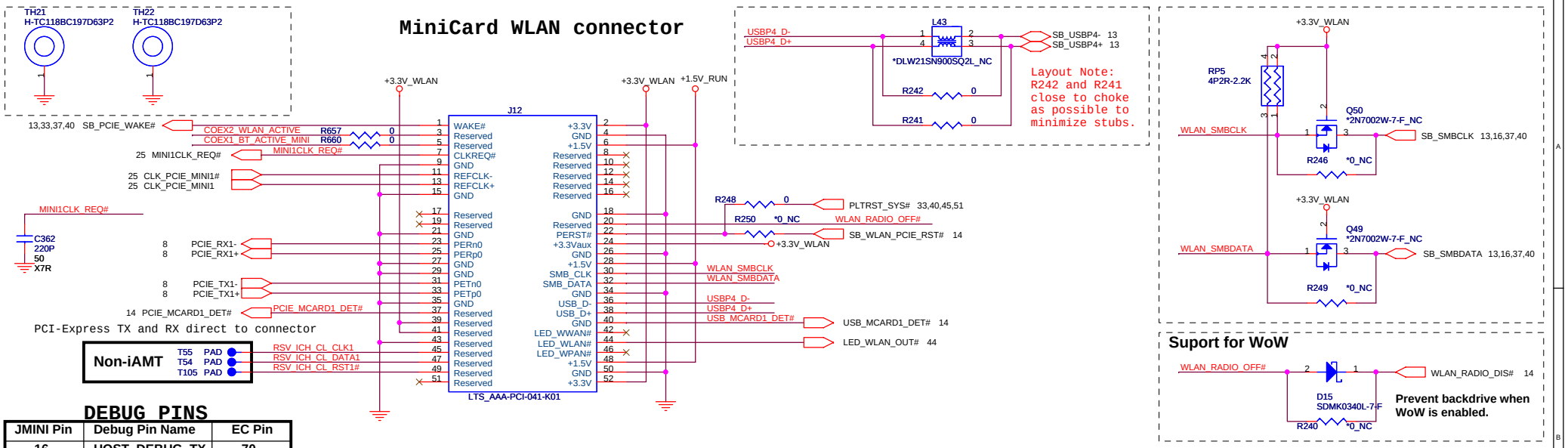
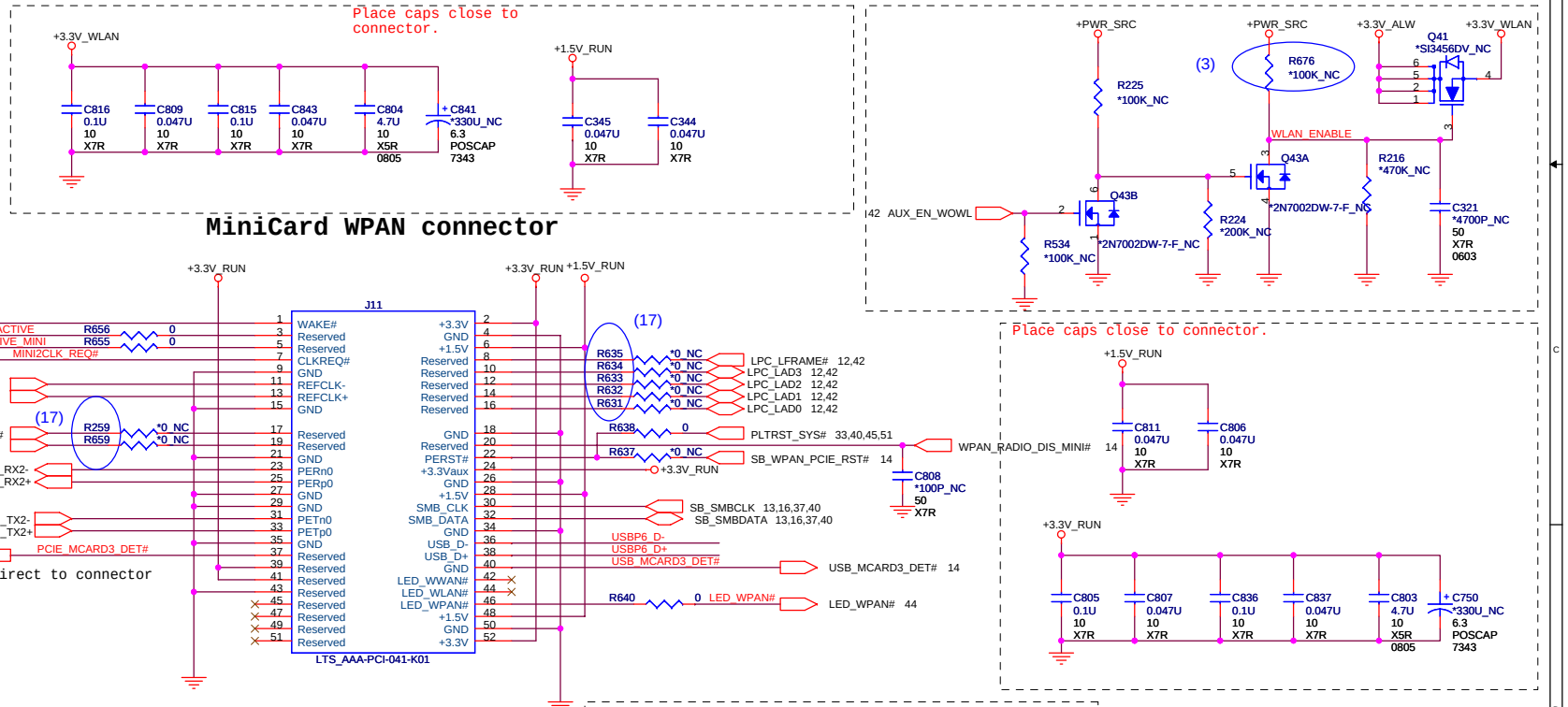
MiniCard WLAN connector



DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81



MiniCard WPAN connector

QUANTA COMPUTER

Title	MINI CARD	
Size	Document Number FX6	Rev 3A
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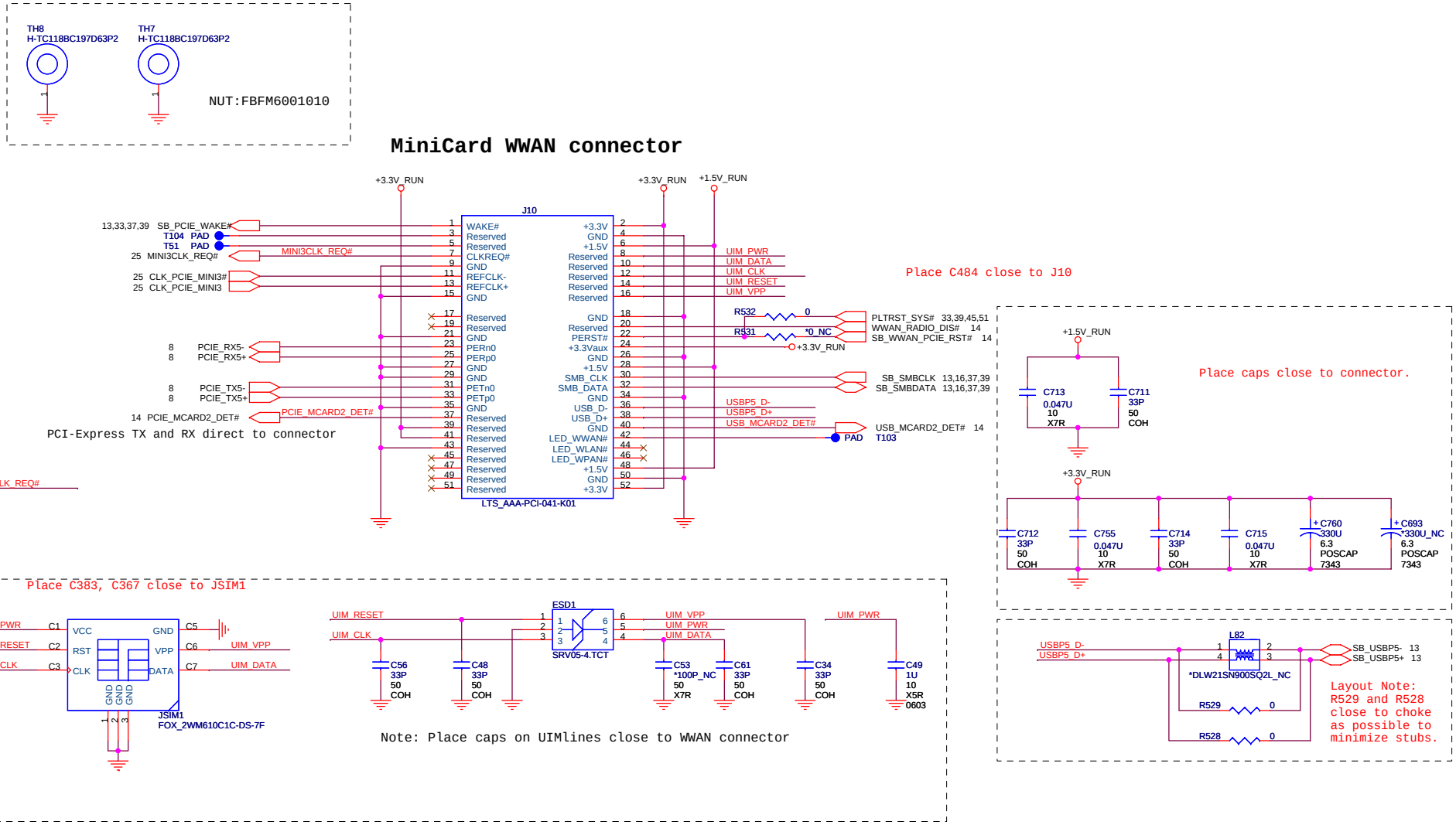

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Title	WWAN		
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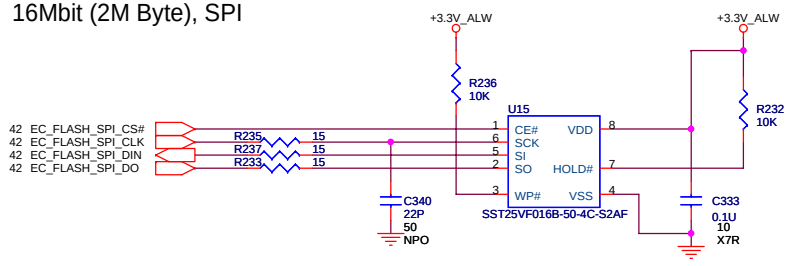
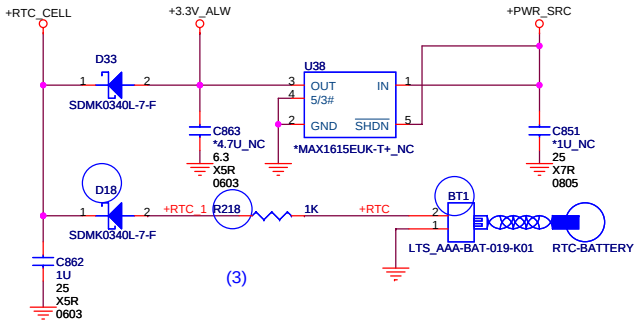
16Mbit (2M Byte), SPI



RTC BATTERY



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Title	FLASH /RTC	
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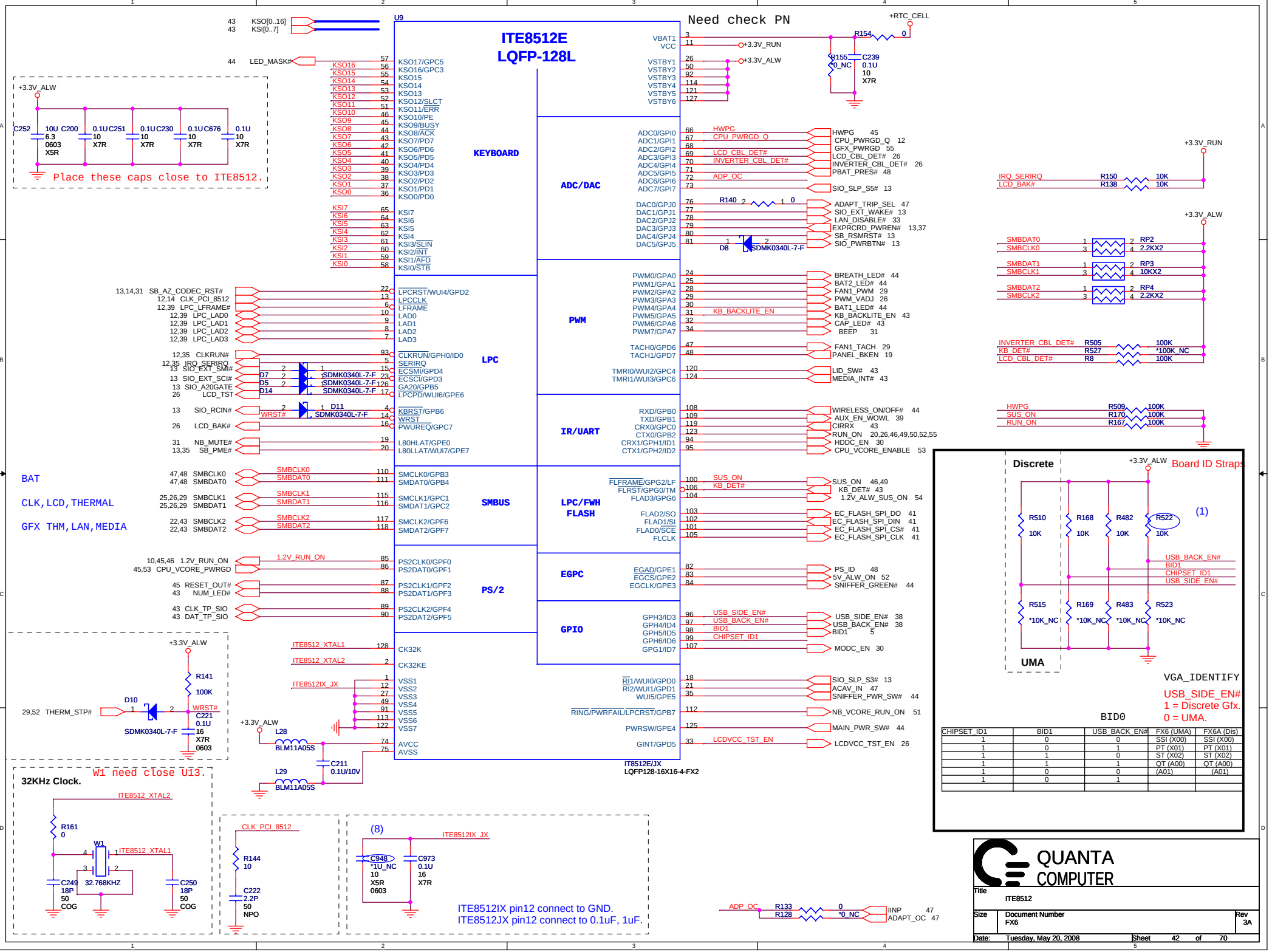
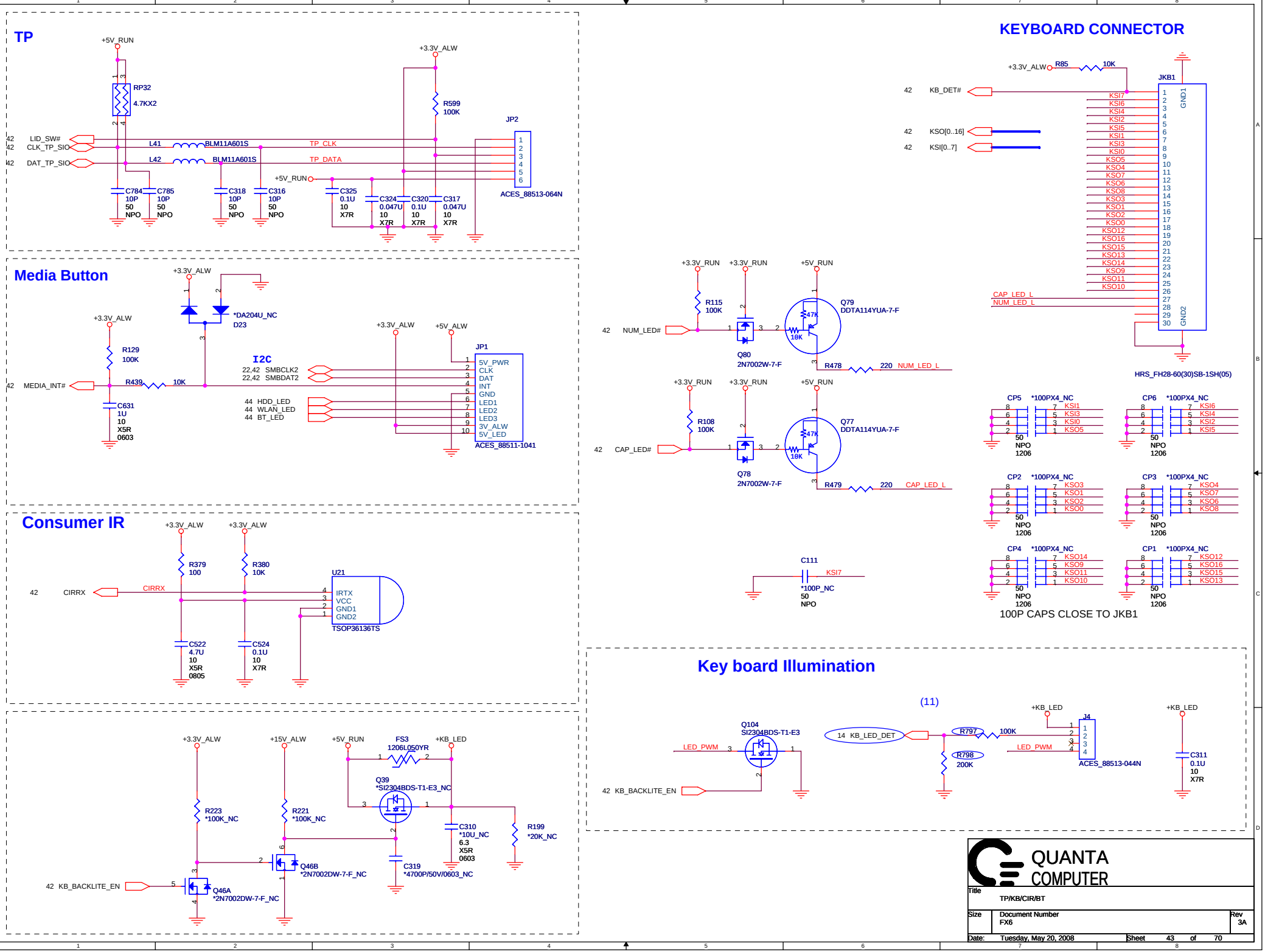


CHIPSET_ID1	BID1	USB_BACK_EN#	FX6 (UMA)	FX6A (Dis)
1	0	0	SSI (X00)	SSI (X00)
1	0	1	PT (X01)	PT (X01)
1	1	0	ST (X02)	ST (X02)
1	1	1	QT (A00)	QT (A00)
1	0	0	(A01)	(A01)
1	0	1		


TP
+5V_RUN
RP32
4.7KX2
+3.3V_ALW
R599
100K
JP2
42 LID_SW#
42 CLK_TP_SIO
42 DAT_TP_SIO
L41 BLM11A601S
L42 BLM11A601S
TP_CLK
TP_DATA
+5V_RUN
C784 10P 50 NPO
C785 10P 50 NPO
C318 10P 50 NPO
C316 10P 50 NPO
C325 0.1U 10 X7R
C324 0.047U 10 X7R
C320 0.1U 10 X7R
C317 0.047U 10 X7R
ACES_88513-064N
Media Button
+3.3V_ALW
*DA204U_NC
D23
+3.3V_ALW
R129
100K
42 MEDIA_INT#
R439 10K
C631 1U 10 X5R 0603
I2C
22,42 SMBCLK2
22,42 SMBDAT2
44 HDD_LED
44 WLAN_LED
44 BT_LED
+3.3V_ALW
+5V_ALW
JP1
5V_PWR
CLK
DAT
INT
GND
LED1
LED2
LED3
3V_ALW
5V_LED
ACES_88511-1041
Consumer IR
+3.3V_ALW
+3.3V_ALW
R379 100
R380 10K
42 CIRRX
CIRRX
U21
IRTX
VCC
GND1
GND2
TSOP36136TS
C522 4.7U 10 X5R 0805
C524 0.1U 10 X7R
+3.3V_ALW
+15V_ALW
+5V_RUN
FS3 1206L050YR
+KB_LED
Q39 *SI2304BDS-T1-E3_NC
R223 *100K_NC
R221 *100K_NC
C310 *10U_NC 6.3 X5R 0603
R199 *20K_NC
Q46B *2N7002DW-7-F_NC
C319 *4700P/50V/0603_NC
42 KB_BACKLITE_EN
Q46A *2N7002DW-7-F_NC
KEYBOARD CONNECTOR
+3.3V_ALW
R85 10K
JKB1
42 KB_DET#
42 KSO[0..16]
42 KSI[0..7]
KSI7 KSI6 KSI4 KSI2 KSI5 KSI1 KSI3 KSI0 KSO5 KSO4 KSO7 KSO6 KSO8 KSO3 KSO1 KSO2 KSO0 KSO12 KSO16 KSO15 KSO13 KSO14 KSO9 KSO11 KSO10
GND1
GND2
CAP_LED_L
NUM_LED_L
HRS_FH28-60(30)SB-1SH(05)
+3.3V_RUN
+3.3V_RUN
+5V_RUN
R115 100K
42 NUM_LED#
Q80 2N7002W-7-F
Q79 DDTA114YUA-7-F
47K
10K
R478 220 NUM_LED_L
+3.3V_RUN
+3.3V_RUN
+5V_RUN
R108 100K
42 CAP_LED#
Q78 2N7002W-7-F
Q77 DDTA114YUA-7-F
R479 220 CAP_LED_L
C111
KSI7
*100P_NC 50 NPO
CP5 *100PX4_NC KSI1 KSI3 KSI0 KSO5
CP6 *100PX4_NC KSI6 KSI4 KSI2 KSI5
CP2 *100PX4_NC KSO3 KSO1 KSO2 KSO0
CP3 *100PX4_NC KSO4 KSO7 KSO6 KSO8
CP4 *100PX4_NC KSO14 KSO9 KSO11 KSO10
CP1 *100PX4_NC KSO12 KSO16 KSO15 KSO13
50 NPO 1206
100P CAPS CLOSE TO JKB1
Key board Illumination
(11)
Q104 SI2304BDS-T1-E3
LED_PWM
42 KB_BACKLITE_EN
14 KB_LED_DET
R797 100K
R798 200K
+KB_LED
J4
LED_PWM
ACES_88513-044N
+KB_LED
C311 0.1U 10 X7R
QUANTA COMPUTER
Title TP/KB/CIR/BT
Size
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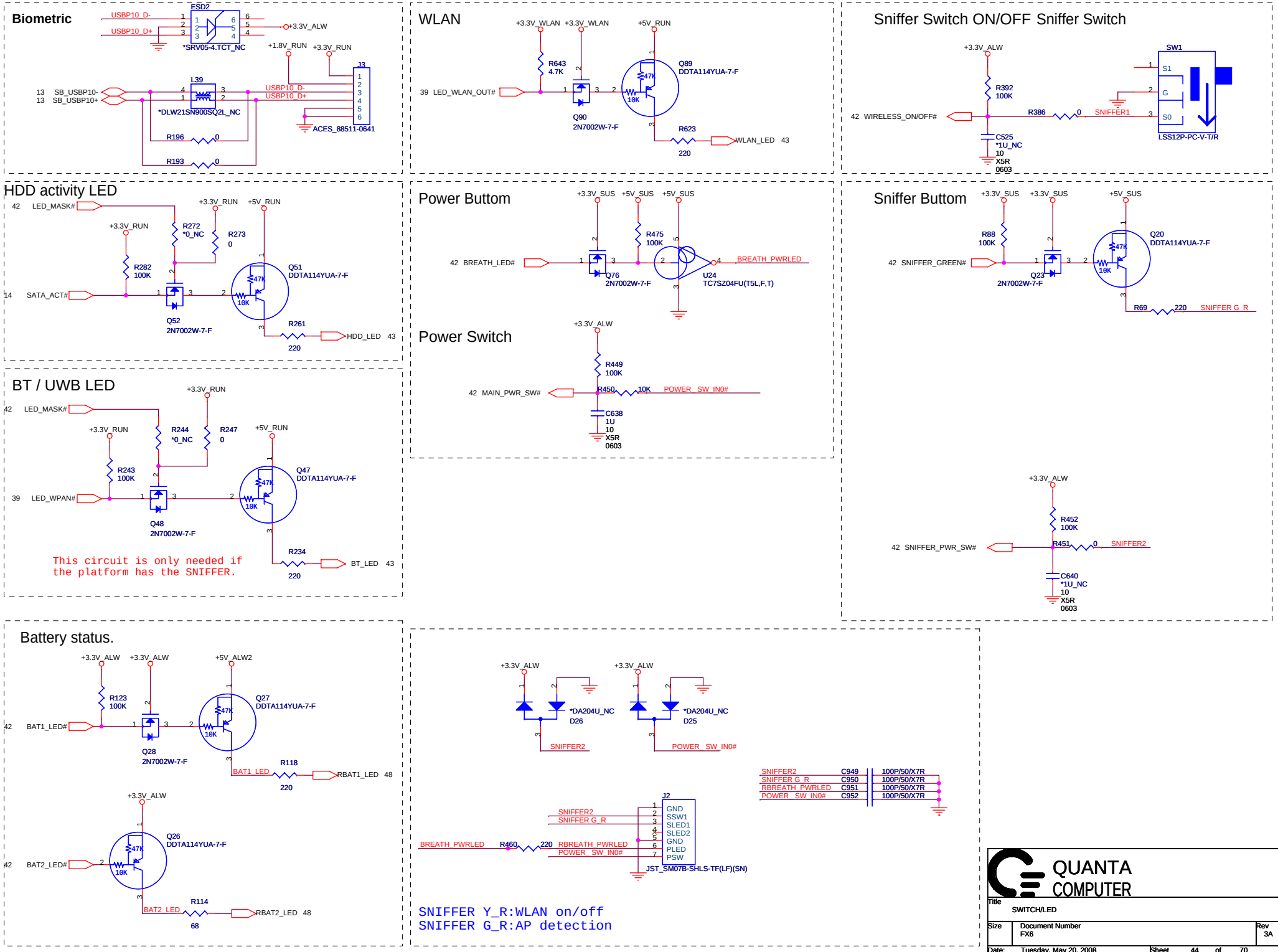
Biometric
ESD2
USBP10_D-
USBP10_D+
+3.3V_ALW
*SRV05-4.TCT_NC
+1.8V_RUN
+3.3V_RUN
J3
13 SB_USBP10-
13 SB_USBP10+
L39
*DLW21SN900SQ2L_NC
USBP10_D-
USBP10_D+
ACES_88511-0641
R196 0
R193 0
WLAN
+3.3V_WLAN +3.3V_WLAN
+5V_RUN
R643 4.7K
39 LED_WLAN_OUT#
Q89 DDTA114YUA-7-F
Q90 2N7002W-7-F
R623 220
WLAN_LED 43
Sniffer Switch ON/OFF Sniffer Switch
+3.3V_ALW
SW1
R392 100K
42 WIRELESS_ON/OFF#
R386 0 SNIFFER1
C525 *1U_NC 10 X5R 0603
LSS12P-PC-V-T/R
HDD activity LED
42 LED_MASK#
+3.3V_RUN +5V_RUN
R272 *0_NC
R273 0
R282 100K
14 SATA_ACT#
Q51 DDTA114YUA-7-F
Q52 2N7002W-7-F
R261 220
HDD_LED 43
Power Buttom
+3.3V_SUS +5V_SUS +5V_SUS
R475 100K
42 BREATH_LED#
BREATH_PWRLED
Q76 2N7002W-7-F
U24 TC7SZ04FU(T5L,F,T)
Power Switch
+3.3V_ALW
R449 100K
42 MAIN_PWR_SW#
R450 10K POWER_SW_IN0#
C638 1U 10 X5R 0603
Sniffer Buttom
+3.3V_SUS +3.3V_SUS +5V_SUS
R88 100K
42 SNIFFER_GREEN#
Q20 DDTA114YUA-7-F
Q23 2N7002W-7-F
R69 220 SNIFFER G_R
BT / UWB LED
42 LED_MASK#
+3.3V_RUN
R244 *0_NC
R247 0
R243 100K
39 LED_WPAN#
Q47 DDTA114YUA-7-F
Q48 2N7002W-7-F
R234 220
BT_LED 43
This circuit is only needed if
the platform has the SNIFFER.
+3.3V_ALW
R452 100K
42 SNIFFER_PWR_SW#
R451 0 SNIFFER2
C640 *1U_NC 10 X5R 0603
Battery status.
+3.3V_ALW +3.3V_ALW +5V_ALW2
R123 100K
42 BAT1_LED#
Q27 DDTA114YUA-7-F
Q28 2N7002W-7-F
BAT1_LED
R118 220
RBAT1_LED 48
+3.3V_ALW
Q26 DDTA114YUA-7-F
42 BAT2_LED#
BAT2_LED
R114 68
RBAT2_LED 48
+3.3V_ALW +3.3V_ALW
*DA204U_NC D26
*DA204U_NC D25
SNIFFER2
POWER_SW_IN0#
SNIFFER2 C949 100P/50/X7R
SNIFFER G_R C950 100P/50/X7R
RBREATH_PWRLED C951 100P/50/X7R
POWER_SW_IN0# C952 100P/50/X7R
J2
SNIFFER2
SNIFFER G_R
BREATH_PWRLED
R460 220
RBREATH_PWRLED
POWER_SW_IN0#
GND
SSW1
SLED1
SLED2
GND
PLED
PSW
JST_SM07B-SHLS-TF(LF)(SN)
SNIFFER Y_R:WLAN on/off
SNIFFER G_R:AP detection
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Title
SWITCH/LED
Size
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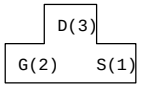
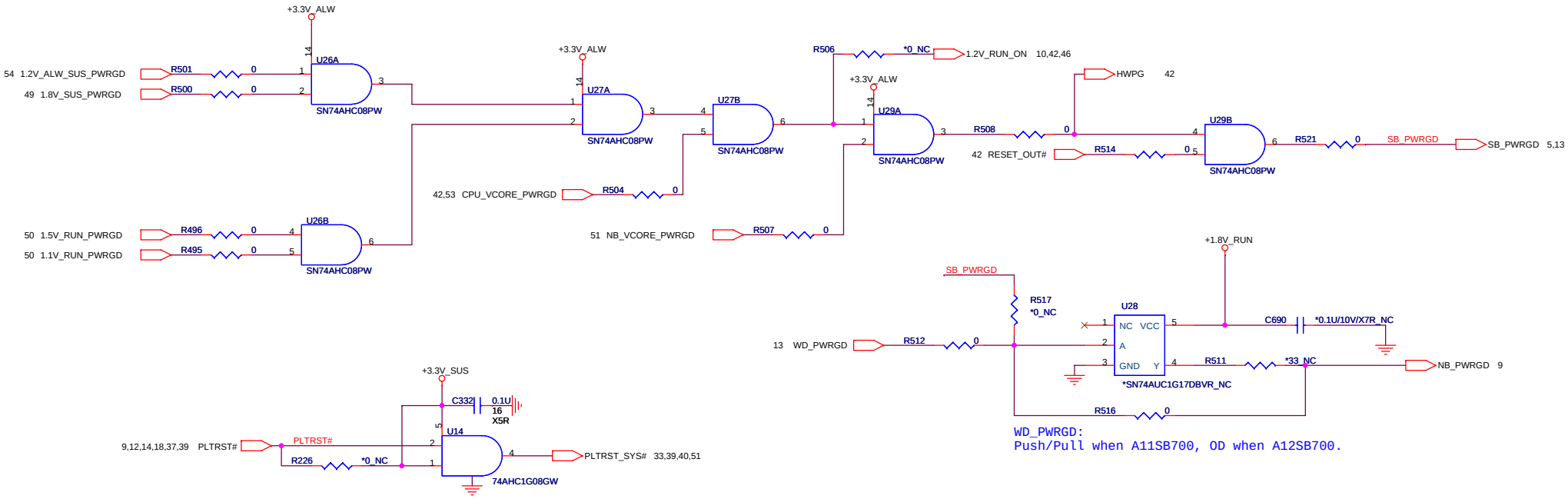
Symbol:
2N7002W-7-F





WD_PWRGD:
Push/Pull when A11SB700, OD when A12SB700.

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Title	System Reset Circuit	
Size	Document Number FX6	Rev 3A
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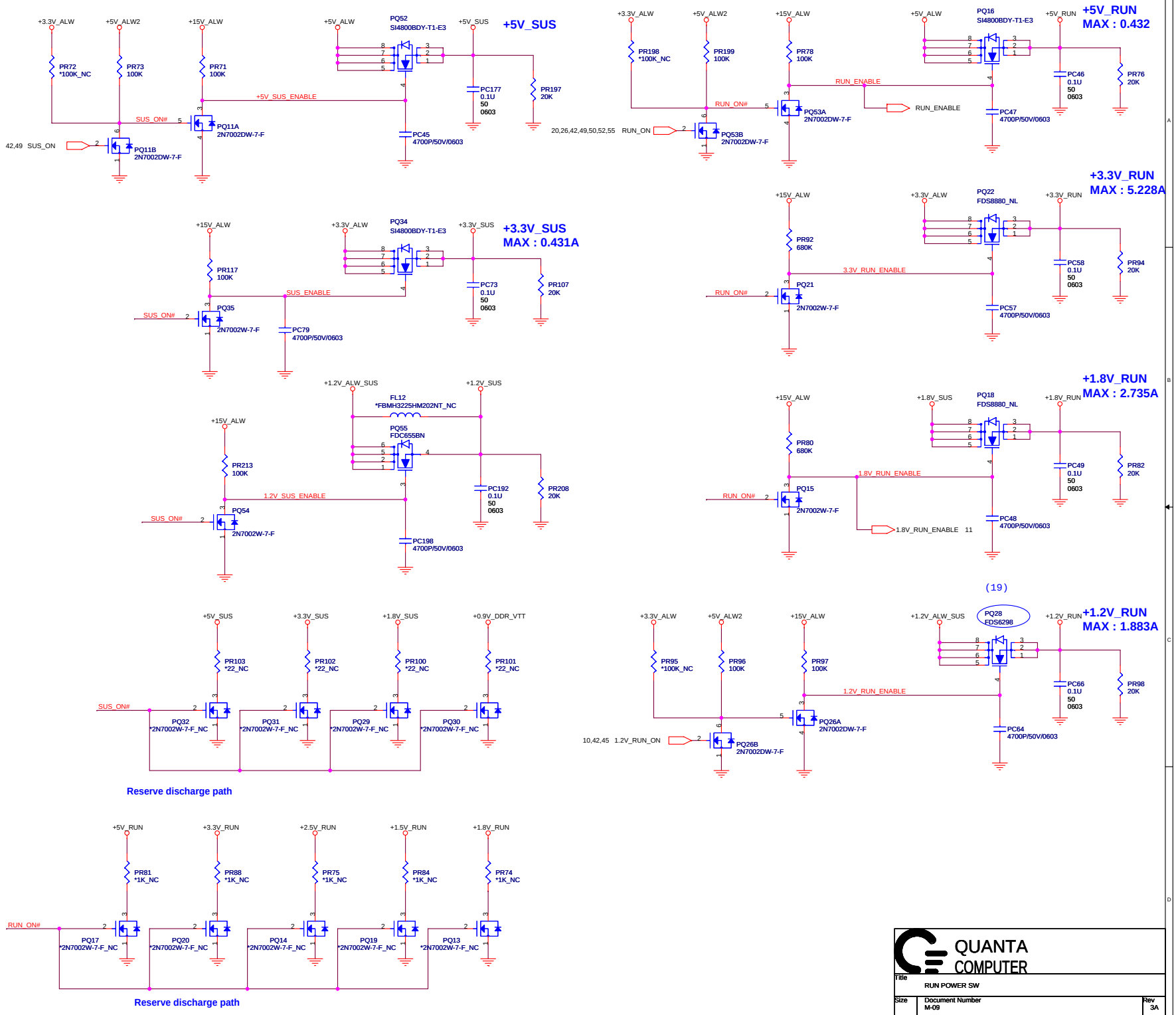

(19)

QUANTA COMPUTER

Title	RUN POWER SW		
Size	Document Number M-09		Rev 3A
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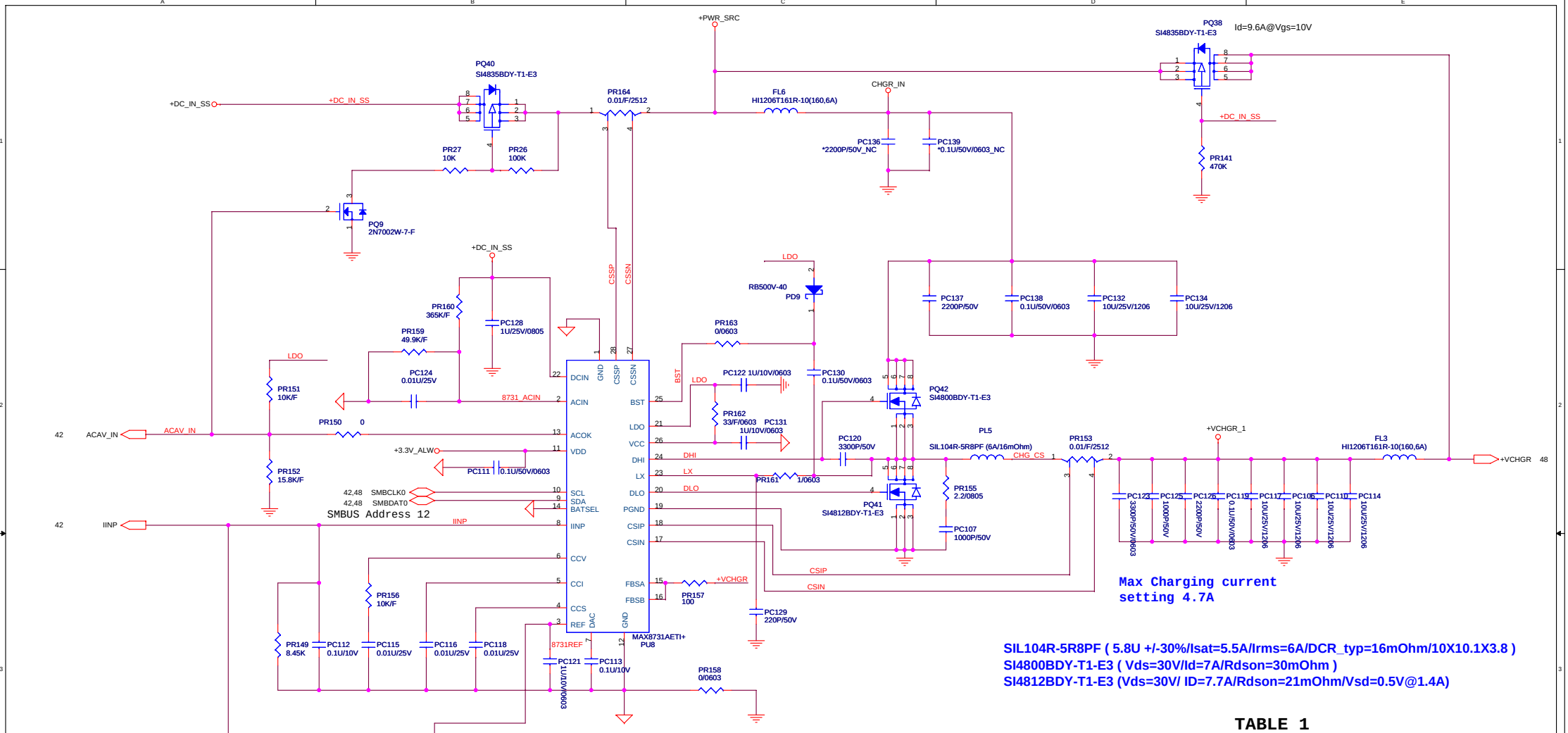

Max Charging current setting 4.7A

SIL104R-5R8PF (5.8U +/-30%/Isat=5.5A/Irms=6A/DCR_typ=16mOhm/10X10.1X3.8)
SI4800BDY-T1-E3 (Vds=30V/Id=7A/Rdson=30mOhm)
SI4812BDY-T1-E3 (Vds=30V/ ID=7.7A/Rdson=21mOhm/Vsd=0.5V@1.4A)

TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	Ra	Rb	Rc	**Rd
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K

**PR119 is popluated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

For GPRS immunity place PC41 & PC39 as close to the IC as possible

QUANTA COMPUTER

Title	BATTERY CHARGER
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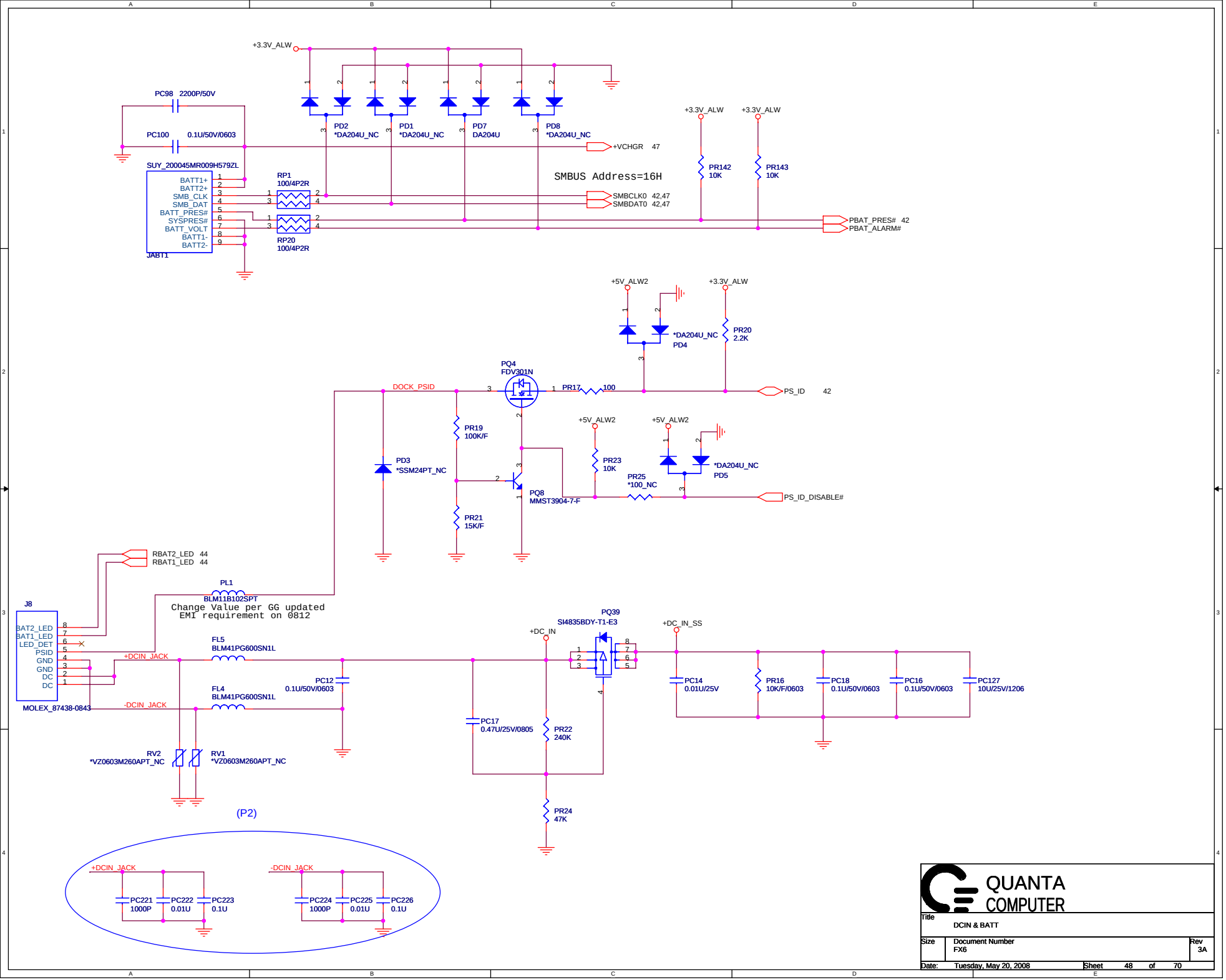
+3.3V_ALW
PC98 2200P/50V
PC100 0.1U/50V/0603
PD2 *DA204U_NC
PD1 *DA204U_NC
PD7 DA204U
PD8 *DA204U_NC
+VCHGR 47
SUY_200045MR009H579L
BATT1+
BATT2+
SMB_CLK
SMB_DAT
BATT_PRES#
SYSPRES#
BATT_VOLT
BATT1-
BATT2-
JABT1
RP1 100/4P2R
RP20 100/4P2R
SMBUS Address=16H
SMBCLK0 42,47
SMBDAT0 42,47
PR142 10K
PR143 10K
PBAT_PRES# 42
PBAT_ALARM#
+5V_ALW2
*DA204U_NC PD4
PR20 2.2K
PQ4 FDV301N
DOCK_PSID
PR17 100
PS_ID 42
PR19 100K/F
PD3 *SSM24PT_NC
PR21 15K/F
PQ8 MMST3904-7-F
PR23 10K
PR25 *100_NC
*DA204U_NC PD5
PS_ID_DISABLE#
RBAT2_LED 44
RBAT1_LED 44
J8
BAT2_LED
BAT1_LED
LED_DET
PSID
GND
GND
DC
DC
MOLEX_87438-0843
PL1 BLM11B102SPT
Change Value per GG updated
EMI requirement on 0812
+DCIN_JACK
-DCIN_JACK
FL5 BLM41PG600SN1L
FL4 BLM41PG600SN1L
PC12 0.1U/50V/0603
RV2 *VZ0603M260APT_NC
RV1 *VZ0603M260APT_NC
PQ39 SI4835BDY-T1-E3
+DC_IN
+DC_IN_SS
PC17 0.47U/25V/0805
PR22 240K
PR24 47K
PC14 0.01U/25V
PR16 10K/F/0603
PC18 0.1U/50V/0603
PC16 0.1U/50V/0603
PC127 10U/25V/1206
(P2)
PC221 1000P
PC222 0.01U
PC223 0.1U
PC224 1000P
PC225 0.01U
PC226 0.1U
QUANTA COMPUTER
Title
DCIN & BATT
Size
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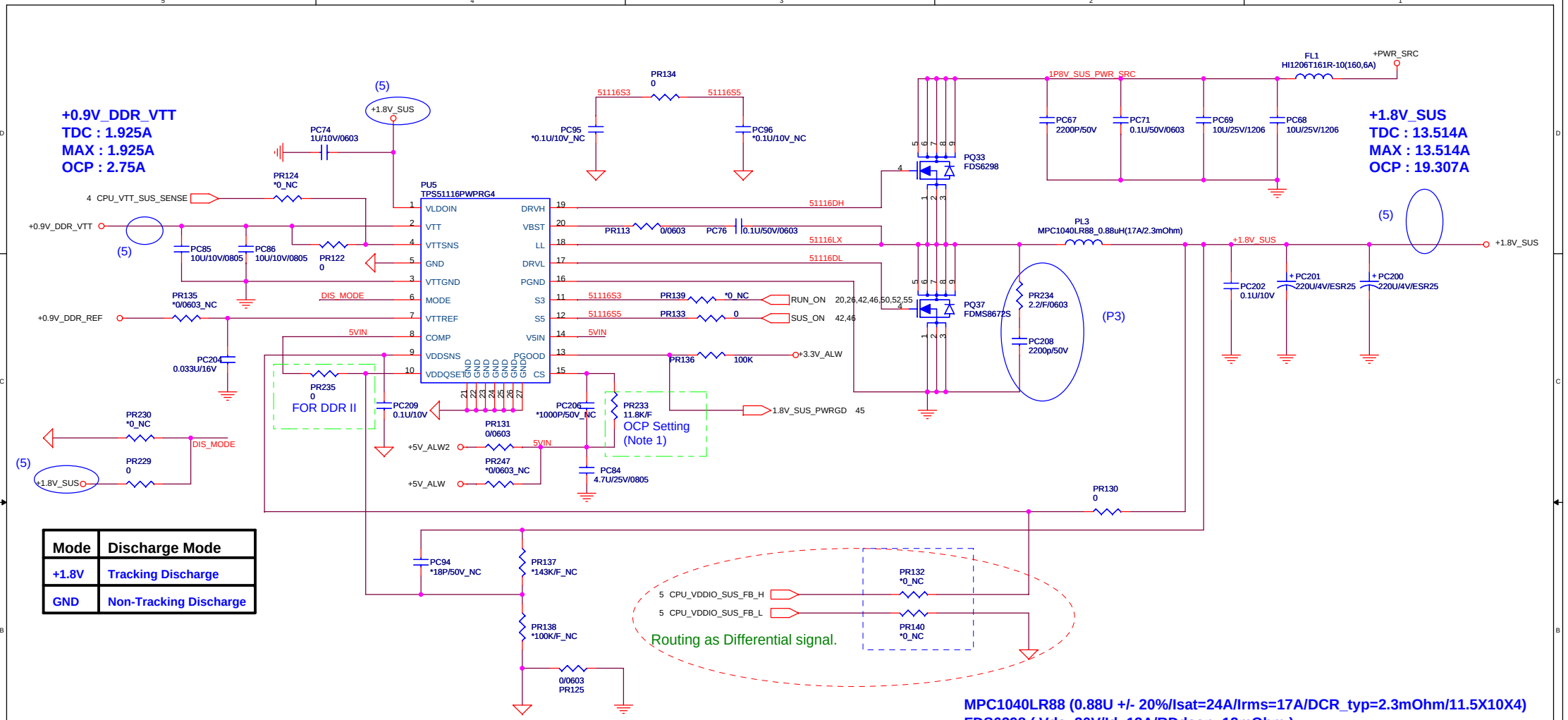

Mode	Discharge Mode
+1.8V	Tracking Discharge
GND	Non-Tracking Discharge

Frequency=400KHz

(Note 1) Current Limiting Setting :
Rtrip(Kohm)=100*(Iocp-0.5*Iripple)*Rds(on)

MPC1040LR88 (0.88U +/- 20%/Isat=24A/Irms=17A/DCR_typ=2.3mOhm/11.5X10X4)
FDS6298 (Vds=30V/Id=13A/RDdson=12mOhm)
FDMS8670S (Vds=30V/ Id=17A/Rdson=5mOhm)

QUANTA COMPUTER

Title	1.8V_SUS&0.9VTT		
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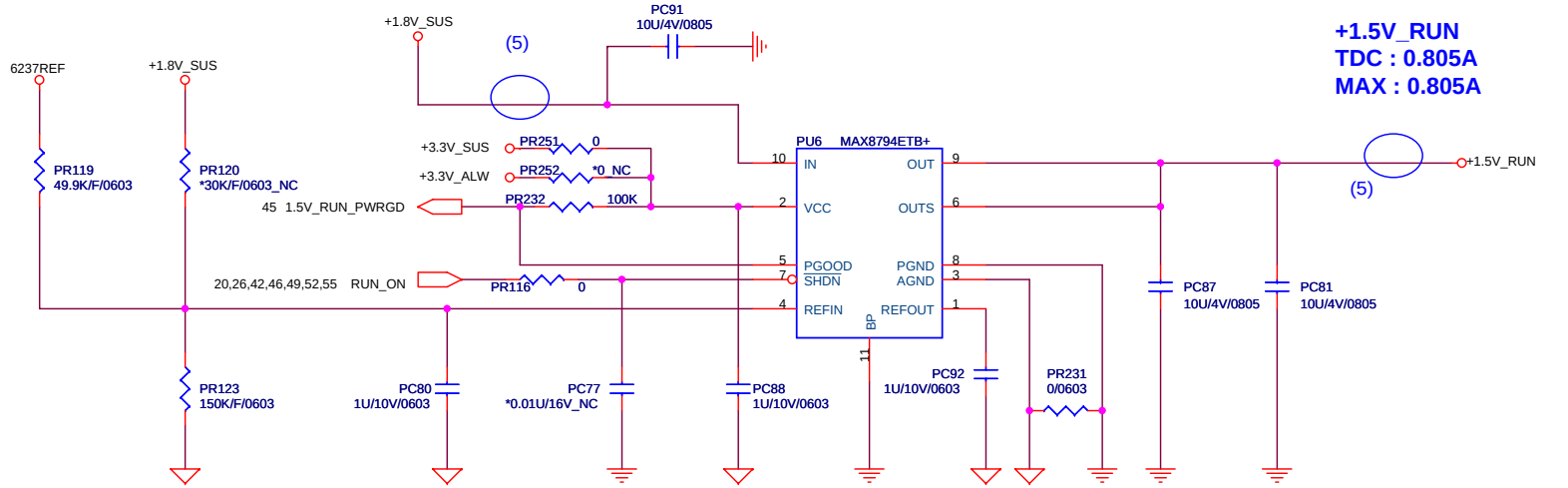

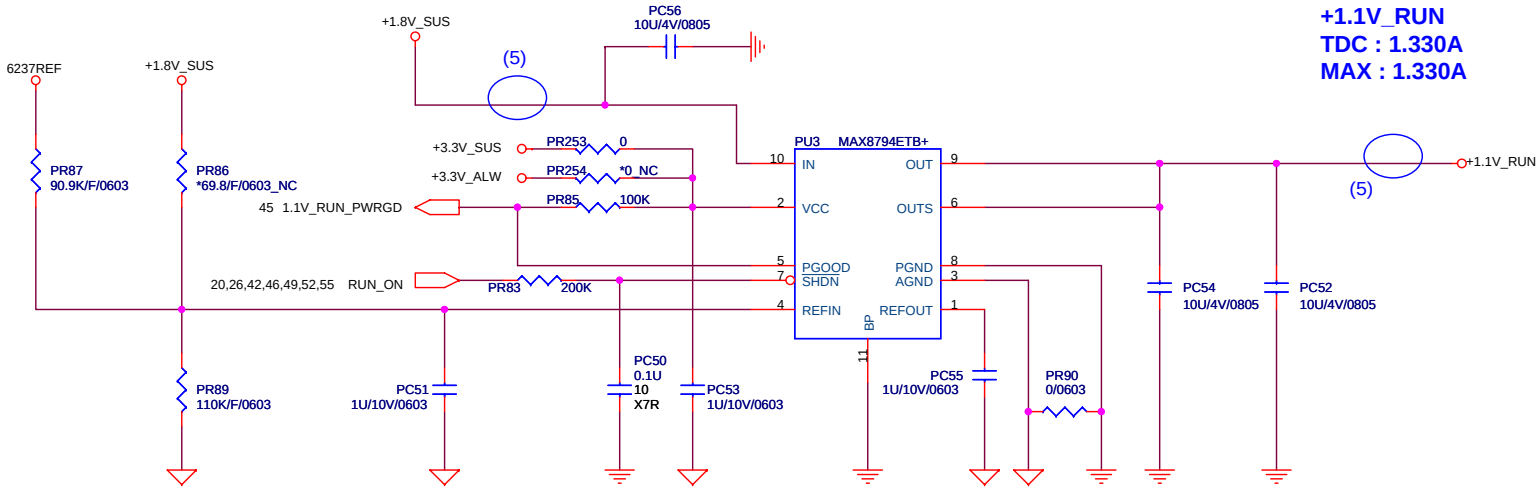

QUANTA COMPUTER

Title	1.5V_RUN&1.1V_RUN
Size	Document Number FX6
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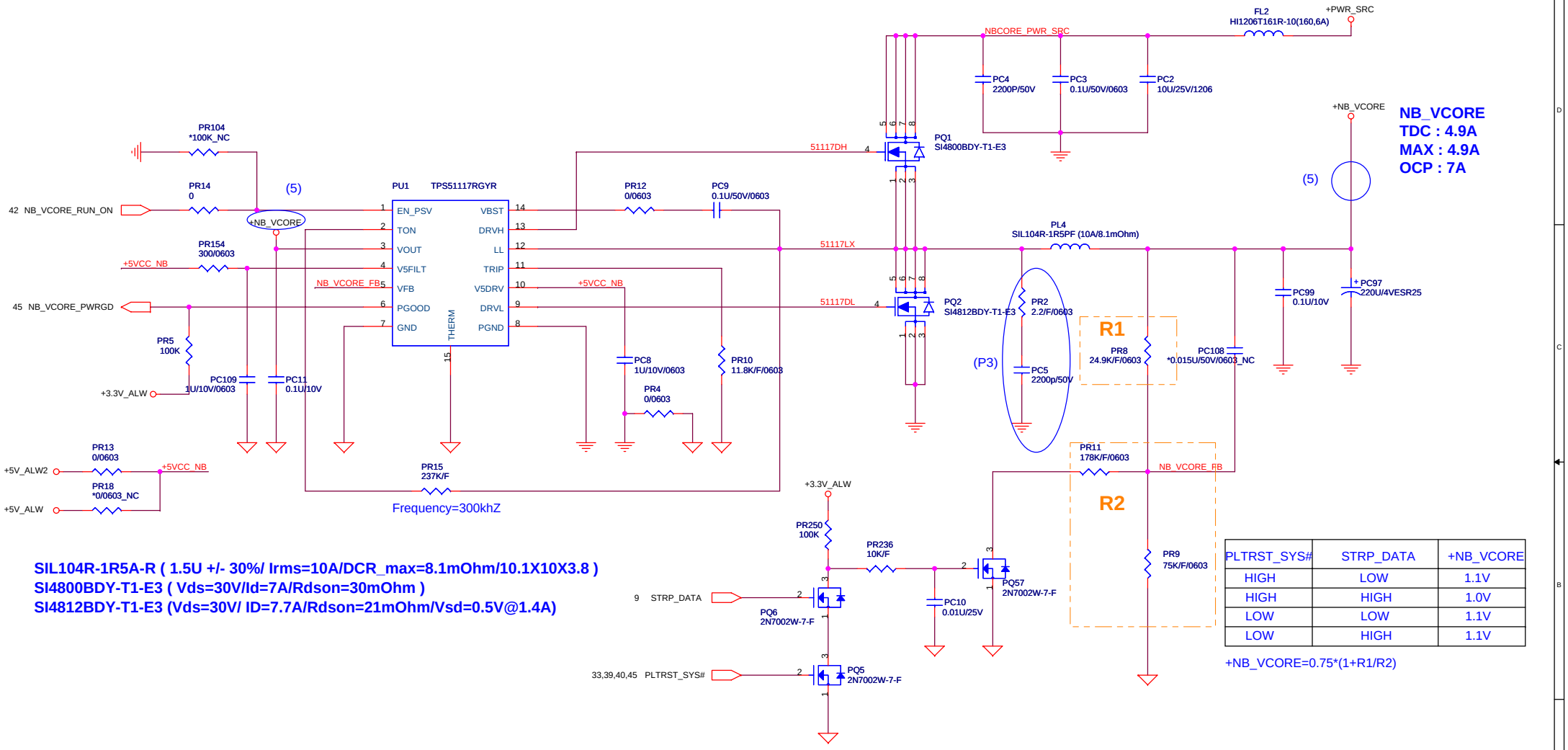

SIL104R-1R5A-R (1.5U +/- 30%/ Irms=10A/DCR_max=8.1mOhm/10.1X10X3.8)
SI4800BDY-T1-E3 (Vds=30V/Id=7A/Rdson=30mOhm)
SI4812BDY-T1-E3 (Vds=30V/ ID=7.7A/Rdson=21mOhm/Vsd=0.5V@1.4A)

PLTRST_SYS#	STRP_DATA	+NB_VCORE
HIGH	LOW	1.1V
HIGH	HIGH	1.0V
LOW	LOW	1.1V
LOW	HIGH	1.1V

+NB_VCORE=0.75*(1+R1/R2)

QUANTA COMPUTER

Title	VCC_NB	
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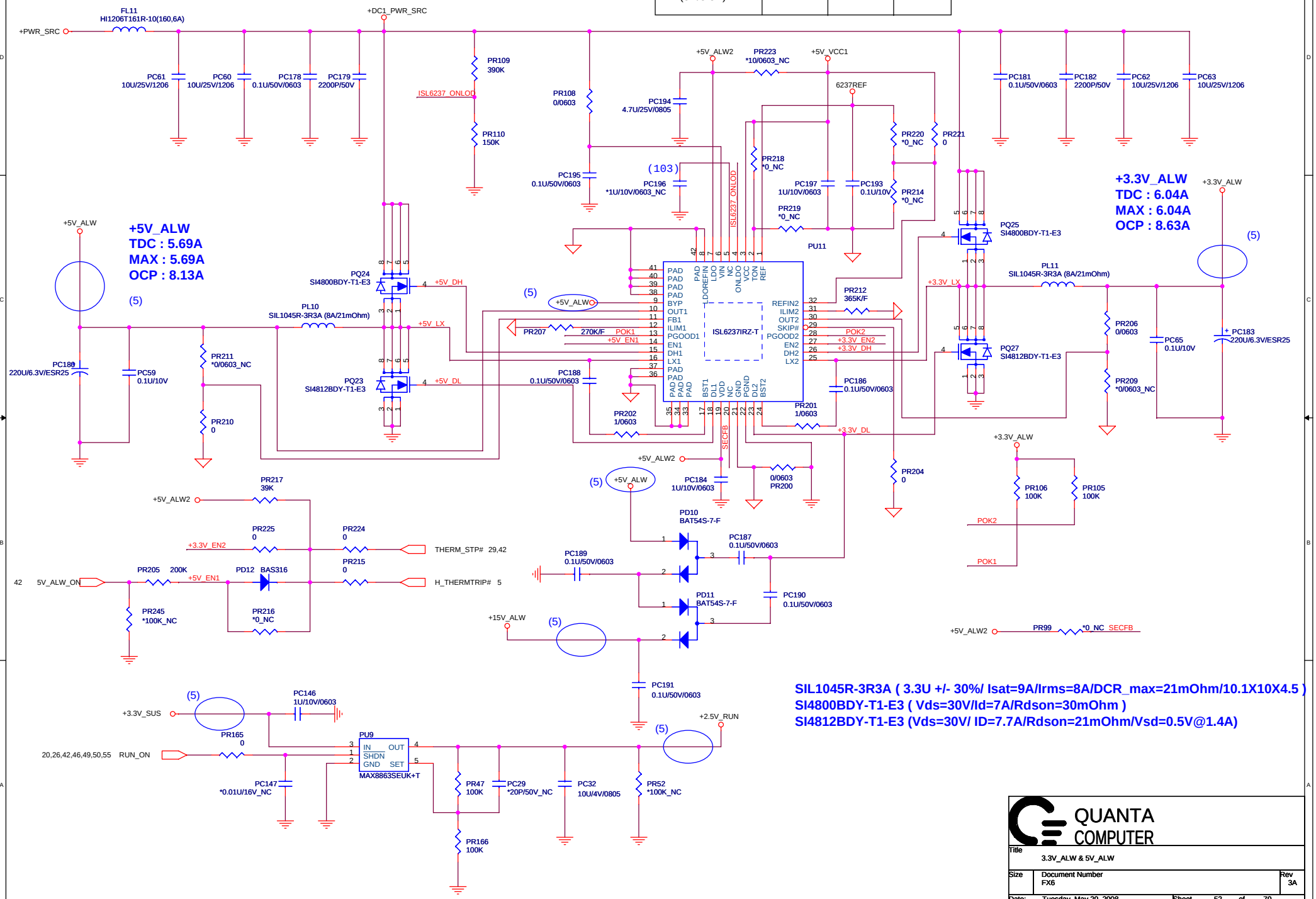
TON	GND	OPEN	VCC
Frequency (KHz) (5V/3.3V)	400/500	400/300	200/300



QUANTA COMPUTER

Title: 3.3V_ALW & 5V_ALW

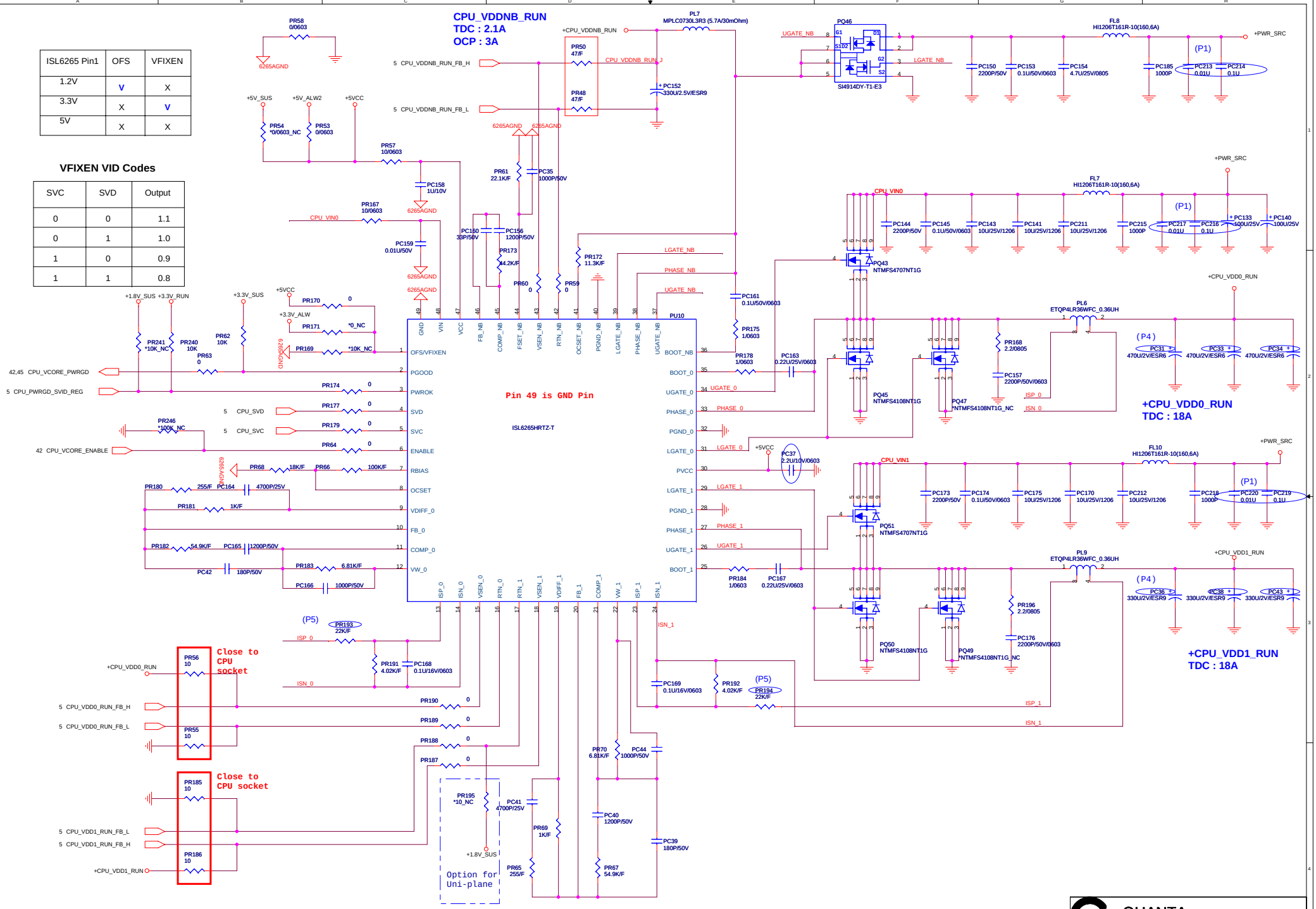
Size: | Document Number: FX6 | Rev: 3A

Date: Tuesday, May 20, 2008 | Sheet 52 of 70

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



QUANTA COMPUTER

Title	CPU_CORE_POWER	
Size	Document Number FX6	Rev 3A
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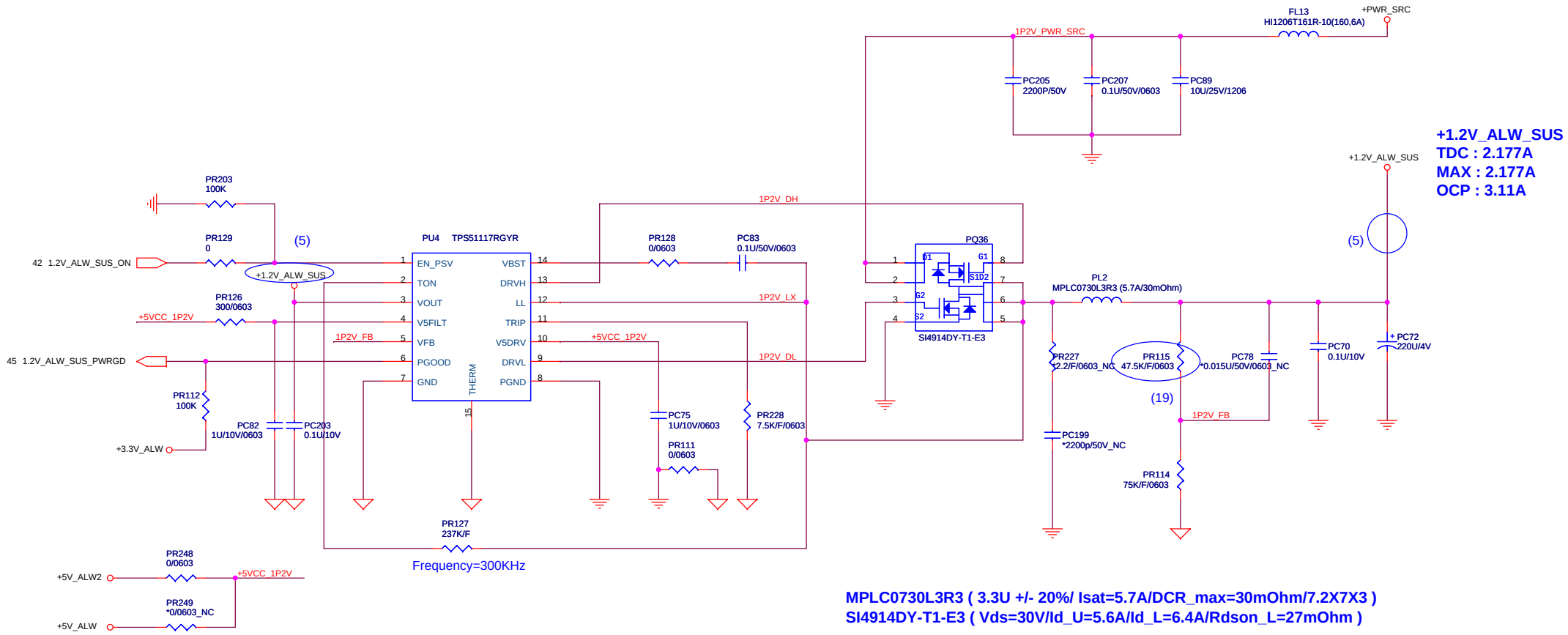

QUANTA COMPUTER

Title	1.2V_ALW_SUS	
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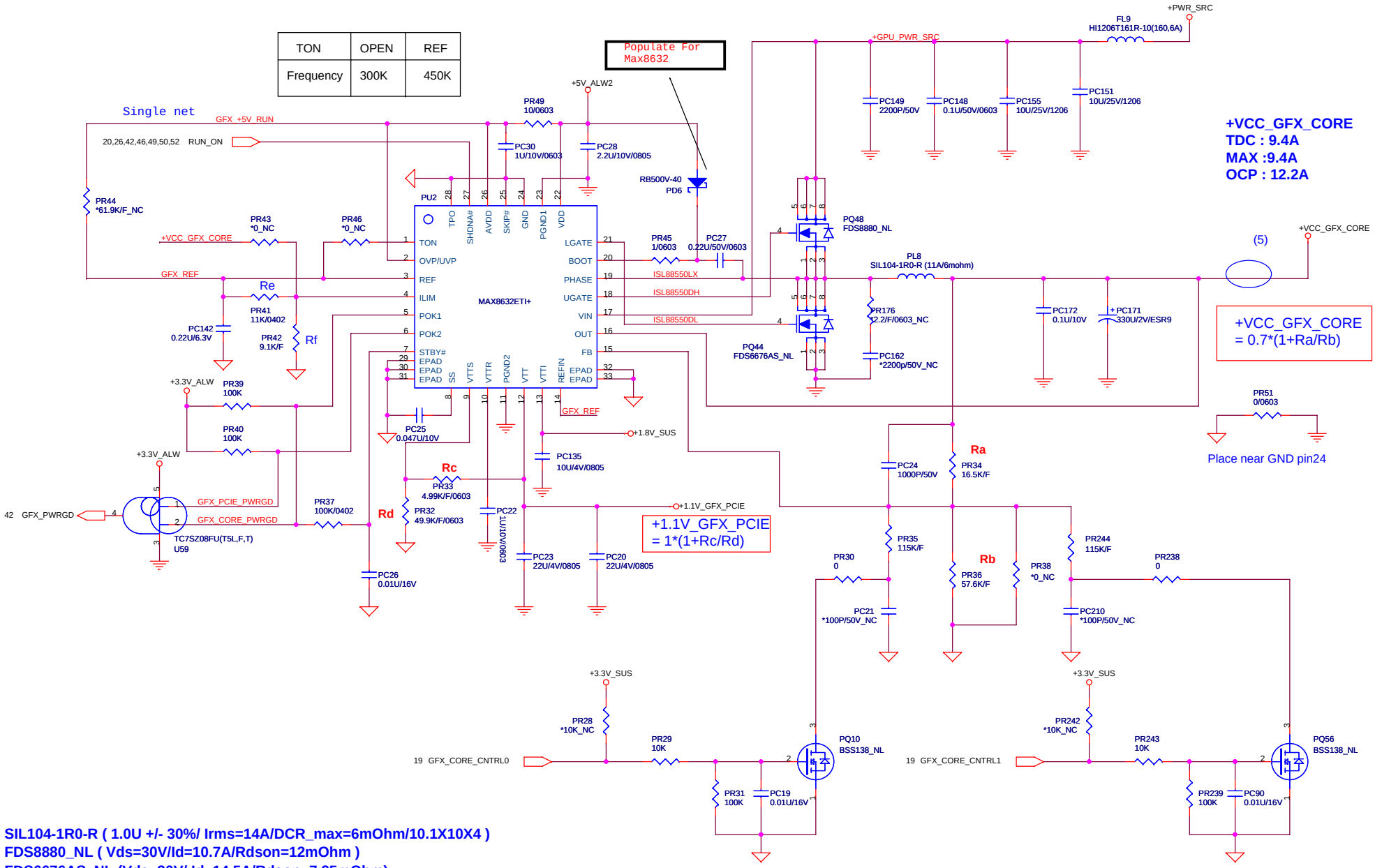
TON	OPEN	REF
Frequency	300K	450K



+VCC_GFX_CORE
TDC : 9.4A
MAX :9.4A
OCP : 12.2A

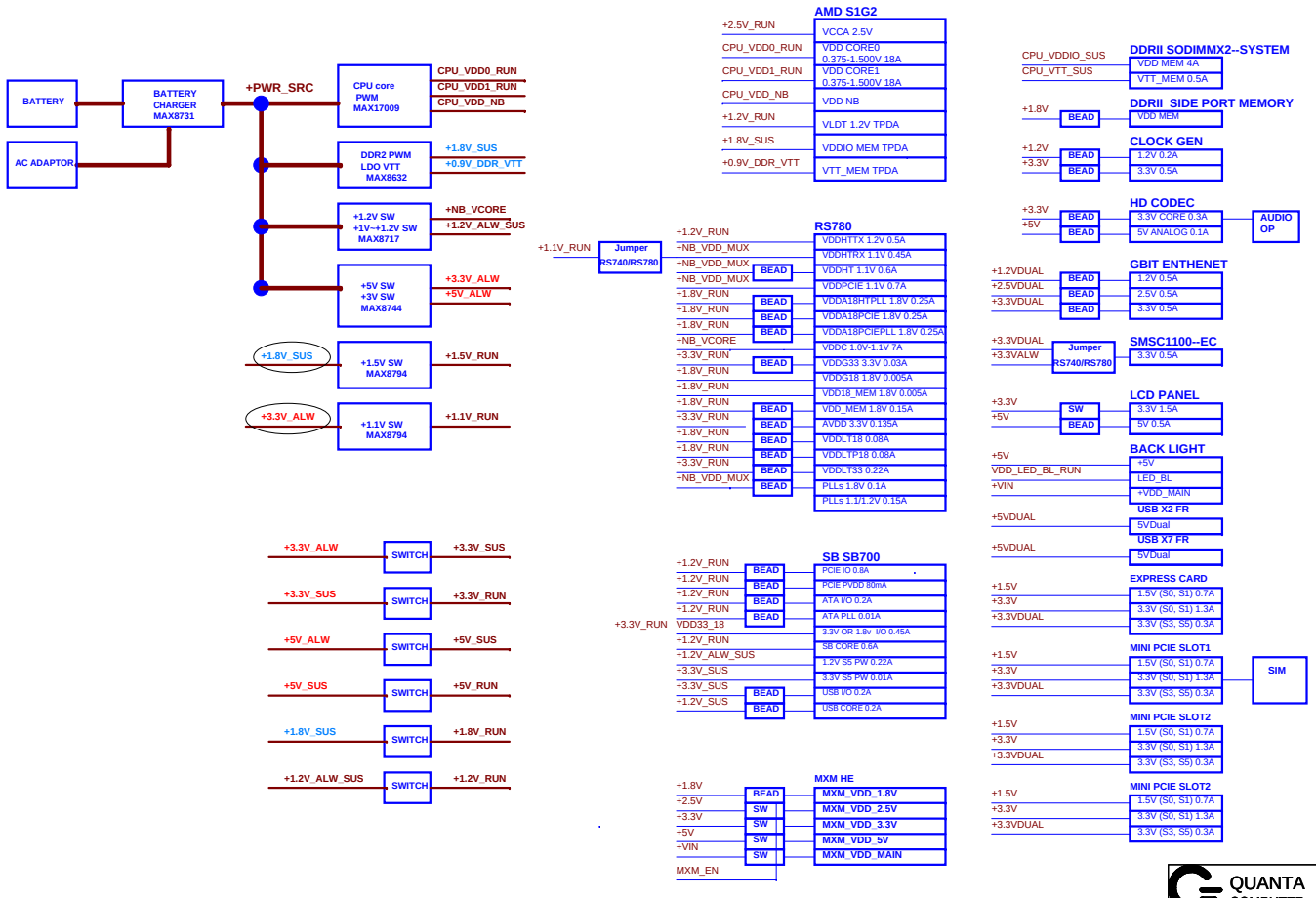
SIL104-1R0-R (1.0U +/- 30%/ Irms=14A/DCR_max=6mOhm/10.1X10X4)
FDS8880_NL (Vds=30V/Id=10.7A/Rdson=12mOhm)
FDS6676AS_NL (Vds=30V/ Id=14.5A/Rdson=7.25mOhm)

TON	AVDD=200KHz,OPEN=300KHz,REF=450KHz,GND=600KHz
ILIM	Iovp=(2*(Rf/(Re+Rf))*0.1*(1/RDSON)+(I_DELTA/2)
SKIP#	AVDD = Low-noise, forced-PWM mode. GND = Pulse-skipping operation.
OVP/UVP	The overvoltage limit is 116% of Vout. The undervoltage limit is 70% of Vout.

GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9
HIGH	LOW	1.0V
HIGH	HIGH	1.1V

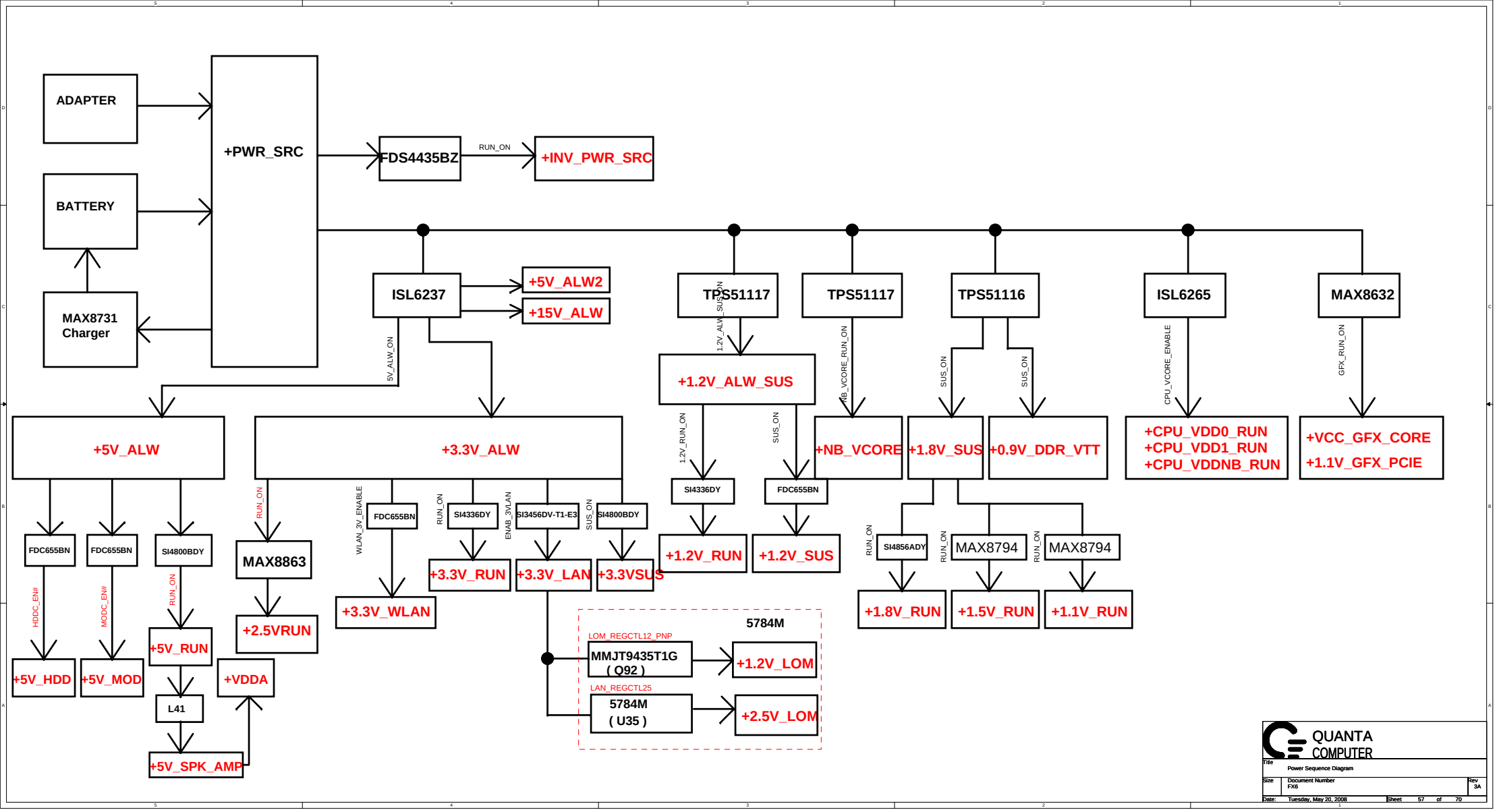
QUANTA COMPUTER

Title	VGA_M82	
Size	Document Number FX6	Rev 3A
Date: Tuesday, May 20, 2008	Sheet 55 of 70	



QUANTA COMPUTER

Title	Power Rail for system
Size	Document Number FX6
Rev	3A
Date: Tuesday, May 20, 2008	Sheet 56 of 70


ADAPTER
BATTERY
MAX8731 Charger
+PWR_SRC
FDS4435BZ
RUN_ON
+INV_PWR_SRC
ISL6237
+5V_ALW2
+15V_ALW
TPS51117
TPS51117
TPS51116
ISL6265
MAX8632
1.2V_ALW_SUS_ON
NB_VCORE_RUN_ON
SUS_ON
SUS_ON
CPU_VCORE_ENABLE
GFX_RUN_ON
5V_ALW_ON
+1.2V_ALW_SUS
+5V_ALW
+3.3V_ALW
1.2V_RUN_ON
SUS_ON
+NB_VCORE
+1.8V_SUS
+0.9V_DDR_VTT
+CPU_VDD0_RUN
+CPU_VDD1_RUN
+CPU_VDDNB_RUN
+VCC_GFX_CORE
+1.1V_GFX_PCIE
SI4336DY
FDC655BN
FDC655BN
FDC655BN
SI4800BDY
RUN_ON
WLAN_3V_ENABLE
FDC655BN
RUN_ON
SI4336DY
ENAB_3VLAN
SI3456DV-T1-E3
SUS_ON
SI4800BDY
+1.2V_RUN
+1.2V_SUS
RUN_ON
SI4856ADY
RUN_ON
MAX8794
RUN_ON
MAX8794
HDDC_EN#
MODC_EN#
RUN_ON
MAX8863
+3.3V_RUN
+3.3V_LAN
+3.3VSUS
+3.3V_WLAN
+1.8V_RUN
+1.5V_RUN
+1.1V_RUN
+5V_HDD
+5V_MOD
+5V_RUN
+2.5VRUN
+VDDA
L41
+5V_SPK_AMP
5784M
LOM_REGCTL12_PNP
MMJT9435T1G (Q92)
+1.2V_LOM
LAN_REGCTL25
5784M (U35)
+2.5V_LOM
QUANTA COMPUTER
Title
Power Sequence Diagram
Size
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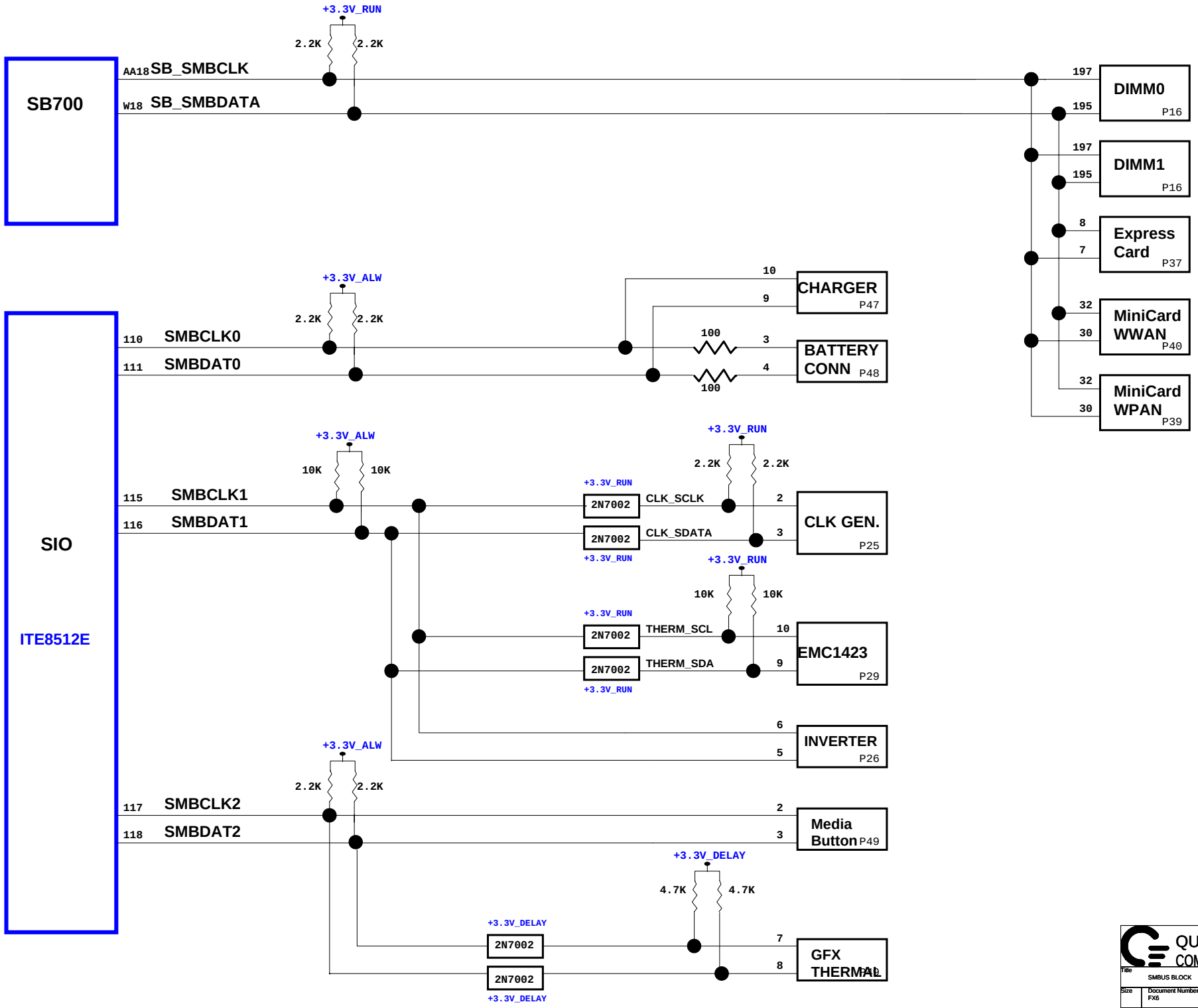
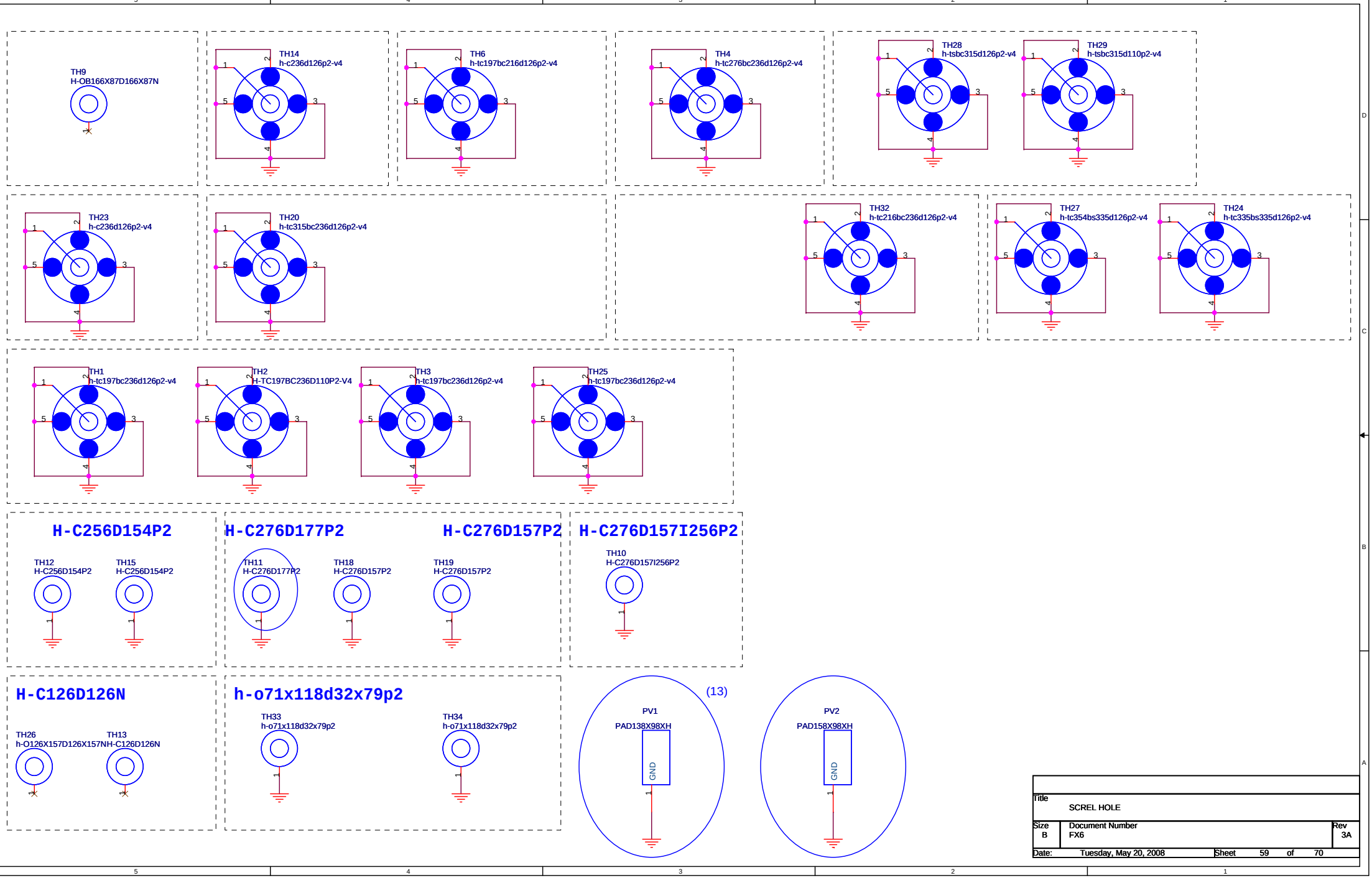


QUANTA COMPUTER

Title	SMBUS BLOCK	
Size	Document Number FX6	Rev 3A
Date: Tuesday, May 20, 2008	Sheet 58 of 70	



Title	SCREL HOLE	
Size B	Document Number FX6	Rev 3A
Date: Tuesday, May 20, 2008	Sheet 59 of 70	

Change List

Item	Page#	Date	T	Issue Description	Solution Description	Rev
				X00-1		
1	25	8/13/2007	EE	CLK_NB_14MB need resistor to a voltage divider. RS780 voltage level is +1.1V.	Chagne R607 from 33 ohm to 158/F, added R637 90.9/F, depop R608 10k for RS780.	X00-1
2	4	8/13/2007	EE	Remove R516 0 ohm reserved resistor for MEMVREF. FX6/GX3 use 1.8V/2	Remove R516 0 ohm.	X00-1
3	5,12	8/13/2007	EE	CPU_LDT_REQ#R should pull up to +1.8V_SUS.	POP R38 and Depop R415.	X00-1
4	8,51	8/13/2007	EE	Connect STRP_DATA to VCORE PWM of NB for Power play.	Connect STRP_DATA from U23.B10 to PQ1.2.	X00-1
5	13	8/13/2007	EE	IDE_RST#/F_RST#/IMC_GPO3 defaults to output driven low.	Remove R720 PD 20k.	X00-1
6	14	8/13/2007	EE	GP16,GP17 for ROM sel. Hepburn connect to EC spi rom. For SB, EC is on LPC bus.	Depop R430 and pop R420. For LPC.	X00-1
7	14	8/13/2007	EE	ATI recommend that AVDD should tie to +3.3V_S5 power rail.	Chagne L46 from +3.3V_SUS to +3.3V_ALW.	X00-1
8	14	8/13/2007	EE	ATI recommend that AZ_RST#, LPCCLK0, LPCCLK1 should pull up to +3.3V_S5 with a 10-k.	Chagne R378,R396,R408 from +3.3V_SUS to +3.3V_ALW.	X00-1
9	8	8/13/2007	EE	S1G2 didn't use DDR_CS2_DIMMA/B# pin.	Remove DDR_CS2_DIMMA/B# from CN5,CN6	X00-1
				Chagne from X00-1 to X00-2		
10	08	8/14/2007	EE	Follow ATI recommend.	Change Q59,Q20 from MMBT3904 to FDV301N and remove R54,R492.	X00-2
11	5	8/14/2007	EE	Follow ATI recommend.	Modify VID table.	X00-2
12	16	8/14/2007	EE	Remove single net DDR_CS3_DIMMA/B#	Remove single net CN5.120,CN6.120	X00-2
13	5	8/14/2007	EE	Change the CPU_PWRGD,LDT_STOP#, LDT_RST# from +1.8V_RUN to +1.8V_SUS.	Pull-up R193,R180,R184 from +1.8V_RUN to +1.8V_SUS(VDDIO).	X00-2
14	5	8/14/2007	EE	Follow ATI recommend.CPU pin C2 need pull-down with 0 ohm.	Pop R536 0 ohm.	X00-2
15	5	8/14/2007	EE	To save the space. There is no need to have these resister in Griffin system.	Remove R556,R169,R161,R554,R553,R555,R172,R191,R165,R168,R196,R205	X00-2
16	5	8/14/2007	EE	Follow ATI.The HDT we have (you have) right now is Purple Possum system. It's 1.8V level design.	Pop R213 0 ohm and depop R212,Q35,R216.	X00-2
17	5,53	8/14/2007	EE	CPU_PWRGD_SVID_REG should be level shifted to 3.3V for the ISL6265. Vih(min) is 2V.	Added Q76,R161.	X00-2
18	5	8/14/2007	EE	Diode D7 blocks a low input to the CPU MEMHOT_L so the circuit would not work as drawn	Remove D7 and reserved R159 680 ohm for DDRII thermal IC in the future.	X00-2
19	19	8/14/2007	EE	HDMI strap is on Hsync.Add 10k-ohm PU (to 3.3V) on VGAHSYNC before buffer U6. Discrete only.	Pull up R191 10k ohm to +3.3V_RUN at VGASYNC	X00-2
20	8,28	8/14/2007	EE	DDC3 is 5V tolerance. There is no need to add level shifters, Discrete only.	Remove R18,R19,R22,R30,Q12,Q18. Remove off page HDMI_SCL,HDMI_SDA.Add TP on U23.A8	X00-2
21	39	8/14/2007	EE	For LPC connect to WPAN socket: Reserve 0ohm, and NC when PD.	Added R720,R763~R766 0 ohm for LPC signals.	X00-2
				Chagne from X00-2 to X00-3		
22	29	8/15/2007	EE	Reserve the caps for any noise coupling issue happening.	Depop C338 and close Q37. Added C920 and close EMC1423.	X00-3
23	29	8/15/2007	EE	Added Q77 2N7002 isolation circuit.	Added Q77 instead R406 ohm and change Q42 from +3.3V_SUS to +3.3V_RUN.	X00-3
24						X00-3
25						X00-3
26	49	8/15/2007	P	FAE Suggetion for OCP setting	Change PR97 from 7.15K to 8.45K	X00-3
27	52	8/15/2007	P	Charge pump from +5V LDO, might cause high ripple voltage	Add P112 to reduce ripple voltage	X00-3
28	52	8/15/2007	P	PR219 no need such hige rating component	Change PR219 from 0805 to 0603 and remove one	X00-3

Change List

Item	Page#	Date	T	Issue Description	Solution Description	Rev
29	52	8/15/2007	P	PC474 should populated for filter	Populate PC474	X00-3
30	52	8/15/2007	P	Reserve feedback circuit for testing	Add PR169 and PR218	X00-3
31	28	8/15/2007	EE	No need to implement shunt resistors for HDMI on M82S Discrete only.	Remove R159,R160,R163,R164 180 ohm.	X00-3
32	36	8/15/2007	EE	Follow vendor review. Added RC to include more different memory card.	Pop C860 270pF and added C921 0.01u, R456 150k.	X00-3
33	19,27	8/15/2007	EE	Follow M82-S reference schematic. Discrete only.	There is double PU for CRT DDC.Remove R522,R519 2.2k and change R520,R486,R521,R485 to 2.2k.	X00-3
				Chagne from X00-3 to X00-4		
34	42	8/16/2007	P	Load switch voltage drop is out of spec.	Change PQ13 from SI4800BDY to SI4856BDY	X00-4
35	42	8/16/2007	P	Load switch voltage drop is out of spec.	Change PQ29 from SI4800BDY to SI4336DY	X00-4
36	42	8/16/2007	P	Load switch voltage drop is out of spec.	Change PQ20 from SI4800BDY to SI4336DY	X00-4
37	5,29	8/16/2007	EE	Follow SMSC feedback.	Change C341 from 220p to 2200p and depop C212	X00-4
38	15	8/16/2007	EE	Follow ATI SB700 checklist.	Change C518,C519,C529 to 1uF, C524 to 22uF.	X00-4
39	15	8/16/2007	EE	Follow ATI SB700 checklist.	Change C496,C494,C495,C489 to 2.2uF.	X00-4
			EE	**Chagne from X00-4 to X00-5**		
40	19	8/17/2007	EE	Move CLK_VGA_27M_SS to GPIO16 and reserved it for spread spectrum. Discrete only.	Reserved R196 0 ohm for EXT CLK GEN.	X00-5
41	29,43,44	8/17/2007	EE	Added ESD diode.	Added D35,D36,D37,D38	X00-5
42	38	8/17/2007	EE	Follow ATI SB700 checklist.	Change C96,C208 from 0.01u to 0.1u to meet SB700 checklist.	X00-5
				Chagne from X00-5 to X00-6		
43	8	8/20/2007	EE	Change VGAH(V)SYNC to INT_VGAH(V)SYNC from PU to PD for disable side prot memry. Discrete only.	Depop R497 and pop R500.	X00-6
44	25	8/20/2007	EE	It's no need to reserve 49.9 ohm and change R243,R235 from 47.5 to 0 ohm, depop R236 261/F.	Remove 49.9 ohm, change R243,R235 from 47.5 to 0 ohm and depop R236.	X00-6
45	25	8/20/2007	EE	Follow FAE feedback. Added Decoupling caps for U16's VDDIO.	Added Decoupling caps C685,C924~C930 and L93 for U16's VDDIO.	X00-6
46	12,20	8/20/2007	EE	Follow ATI FAE recommend. Set GPIO to turn on M82 +3.3V_DELAY.	Connect GFX_RUN_ON from SB700 pin AC6 to R513.	X00-6
47	12,14,18	8/20/2007	EE	Follow ATI FAE recommend to change the M82 reset signal for power express.	Added R458,R457,D39,D40,R205 for power express.	X00-6
48	14	8/20/2007	EE	Follow ATI FAE recommend.	Change R421,R429 from 10k to 2.2k.	X00-6
49	34	8/20/2007	EE	Follow BCM FAE recommend to remove external RC termination.	Remove (R690~R697 and C794~C797)	X00-6
50	33	8/20/2007	EE	Follow BCM recommend to add the required grounding for all the package signals and powertermination.	Add U29 pin 69 thermal GND pad.	X00-6
				Chagne from X00-6 to X00-7		
51	42	8/21/2007	EE	Follow Card reader vendor recommend to add PU resistor for IRQ_SERIRQ.	Add R267 10K ohm to pull-up +3.3V_RUN.	X00-7
52	41	8/21/2007	EE	There is no +3.3V_RTC_LDO power rail.	Change the +3.3V_RTC_LDO to +3.3V_ALW.	X00-7
53	21	8/21/2007	EE	Added +1.8V_GFX power rail for M82-S power express	Change the M82-S +1.8V_RUN to +1.8V_GFX and added +1.8V_GFX power switch.	X00-7
54	51	8/21/2007	P	Connect thermal pad to AGND	Add pin15 to AGND	X00-7
55	52	8/21/2007	P	Preserve component for MAX8778	Add PC115	X00-7
56	54	8/21/2007	P	Connect thermal pad to AGND	Add pin15 to AGND	X00-7

Change List

Item	Page#	Date	T	Issue Description	Solution Description	Rev
57	55	8/21/2007	P	Change feedback resistor for 1.1V output	Change PR66 to 63.4K	X00-7
58	55	8/21/2007	P	Change feedback resistor for +1.1V_GFX_PCIE output	Change PR68 to 4.53K	X00-7
				Chagne from X00-7 to X00-8		
59	12,35	8/22/2007	EE	Change the PCI_PIRQD to PCI_PIRQB. ATI must use INTH#/GPIO36 to control M82-S reset signal.	Change the PCI_PIRQD to PCI_PIRQB and move to U31.AC4	X00-8
60	12	8/22/2007	EE	ATI use INTH#/GPIO36 (PE_GPIO0) to control M82-S reset signal.	Added PE_GPIO0 on U31.AE3 to control M82-S reset.	X00-8
61	48	8/22/2007	P	Pin define is wrong.	Change JABT1 pin define	X00-8
62	48	8/22/2007	P	Remove AC_OFF function	Remove PQ24	X00-8
63	9	8/23/2007	EE	Remove 0 ohm resistor for RX780 power rail option (will not support RX780) and CRT 150 ohm.	Remove R490,R42,R84,R32,R63,R112,R119,R131 for RX780.	X00-8
64	22	8/23/2007	EE	Added level shift on M82-S thermal IC SMBUS2. Discrete only.	Added Q88,Q87 and remove R144,R137 0 ohm.	X00-8
65	34	8/23/2007	EE	Follow FM6 to modify the +3.3V_LAN power source form +3.3V_ALW to +3.3V_SUS.	Depop +3.3V_ALW to +3.3V_LAN switch circuit and added R767 to connect +3.3V_SUS to +3.3V_LAN.	X00-8
66	55	8/23/2007	EE	We don't use RUNPWROK and use GFX_RUN_ON to turn on GFX power.	Remove PR169.	X00-8
67	12	8/23/2007	EE	Follow ATI checklist. Reserved J13 for Rubuto.	Added J13 for Rubuto system.	X00-8
68	34	8/23/2007	EE	Follow Dell. Change the LED signals.	LINKLED connect to G_LED.SPD100LED connect to amber LED.	X00-8
				Chagne from X00-8 to X00-9		
69	9	8/24/2007	EE	Check the CLK GEN vendor (RT&CLG). They don't have PA_RS7X0A1 issue.	Remove R29,R33,R37,R34 and connect to GPP_SB_REFCLK directly from CLK GEN SB_SRC CLK.	X00-9
70	26	8/24/2007	EE	Added OR gate to support backlight from EC and NB.	Added U225,C932 and pop R464.	X00-9
71	45	8/24/2007	EE	Added AND gate in system reset circuit.	Remove R204,R209 and added U226,U227.	X00-9
72	31,32	8/24/2007	EE	Change the audio to IDT STAC9228/92HD73C.	Change the audio to IDT STAC9228/92HD73C.	X00-9
73	25	8/24/2007	EE	Follow RS780 check list to change the ferrite bead for CLK GEN power.	Change the L34 ,L93 and added L107,L108 to FBM-11-160808-601A10T	X00-9
74	11	8/24/2007	EE	Follow RS780 check list.	Added C997,C998 1U and change L15 from 4.7U to 1U.	X00-9
				Chagne from X00-9 to X00-10		
75	22,26	8/28/2007	EE	Added reduce WWAN interference solution.	Added C1001~C1008, R835,R836.	X00-10
76	42,43	8/28/2007	EE	Chagne MEDIA_INT to active low. MEDIA_INT# need pull-up +3.3V_ALW.	Move R217 to page 43, pull-up to +3.3V_ALW. Added RC to MEDIA_INT#.	X00-10
77	44	8/28/2007	EE	Chagne power switch and sniffer switch power rail.	Chagne R461,R21 from +RTC_CELL to +3.3V_ALW.	X00-10
78	42,53	8/28/2007	EE	Chagne CPU_VCORE_PWRGD pull up power rail.	Chagne PR35 from +3.3V_ALW to +3.3V_SUS and depop R574.	X00-10
79	43	8/28/2007	EE	Added the NUM, CAP low active circuit and swap keyboard signals.	Added CP7 and Q80,Q82,Q81,Q83,R834,R832.	X00-10
80	39	8/28/2007	EE	Depop debug board's 0 ohm.	Depop debug board's 0 ohm R322,R685,R720,R763,R764,R765,R766	X00-10
81	30	8/28/2007	EE	ODD SATA is not need +3.3V_RUN. Remove +3.3V_RUN decoup caps for ODD SATA.	Remove R745,R747,R307,R744,R313.	X00-10
82	46	8/28/2007	P	USB Charger Function	Add +5V_ALW to +5V_SUS Load Switch for USB Charger	X00-10
83	52	8/28/2007	P	USB Charger Function	Change +5V_ALW to +5V_ALW2	X00-10
84	52	8/28/2007	P	USB Charger Function	Change +5V_SUS to +5V_ALW	X00-10
85	52	8/28/2007	P	USB Charger Function	Remove PR213 and PD1	X00-10

Change List

Item	Page#	Date	T	Issue Description	Solution Description	Rev
86	52	8/28/2007	P	USB Charger Function	Change +3.3V_DL to +5V_DL	X00-10
87	51	8/28/2007	P	FAE Suggest 237K for 300KHz frequency	Change from 178K to 237K	X00-10
88	54	8/28/2007	P	FAE Suggest 237K for 300KHz frequency	Change from 178K to 237K	X00-10
89	49	8/28/2008	P	FAE Suggest connect to GND	Change to connect to GND	X00-10
90	49	8/28/2008	EE	Follow AMD recomment. Added buffer work around circuit to NB_PWRGD.	Added U234 buffer to seperate NB_PWRGD and WD_PWRGD.	X00-10
				Chagne from X00-10 to X00-11		
91	25	8/29/2008	EE	Added MINI3CLK_REQ#,EXPRESSCARD_REQ# pull-up resistor.	Added R837,R859 10k pull up to +3.3V_RUN.	X00-11
92	9	8/29/2008	EE	pop R495 and remove PANEL_BKEN from RS7800	pop R495 0 ohm and remove R806.	X00-11
93	28,44	8/29/2008	EE	Add ESD, Choke for Biometric and HDMI.	Add ESD3 for Biometric and L109~L112 for HDMI.	X00-11
94	24	8/29/2008	EE	Follow AMD recomment. Change the voltage level for hybrid IC SEL pin.	Change R89 from 0 ohm to 8.2k ohm.	X00-11
95	10	8/30/2008	EE	Add work around TPS72501 to create 1.35V to RS780 VDDHTTX power rail. RS780 Rev.A11 only.	Used TPS72501 to create +1.35V_HT_VCC and added L113 for option.	X00-11
96	9	8/30/2008	EE	Added PD resistor 2.7k for INT_EN_LCDVDD.	Added R863 2.7k for INT_EN_LCDVDD.	X00-11
97	10	8/30/2008	EE	Follow ATI checklist. Added L114 to reduce noise for VDDPCIE.	Added L114 to VDD_PCIE.	X00-11
98	46	8/30/2007	P	For more suitable RDSON	Change to SI4800BDY	X00-11
99	48	8/30/2007	P	Footprint is not correct	Change to new footprint "BAT-200045MR009H577ZR-9P-R-V"	X00-11
100	49	8/30/2007	P	MPL104S-0R9 is not PSL	Change to MPC1040LR88	X00-11
101	52	8/30/2007	P	Reserve GPIO for USB Charger	Add 5V_ALW_ON GPIO for USB charger enable	X00-11
102	52	8/30/2007	P	FAE suggest connect to +3.3V_DL	Connect to +3.3V_DL	X00-11
103	52	8/30/2007	P	For Uni material	Change to 0.1u/0603	X00-11
104	53	8/30/2007	P	MPL73-3R3 is not PSL	Change to MPLC0730L3R3	X00-11
105	53	8/30/2007	P	FAE Suggest PR43=18K, PR42=100K	Change to PR43=18K, PR42=100K	X00-11
106	53	8/30/2007	P	FAE Suggest PR198=16.2K, PR205=4.02K	Change to PR198=16.2K, PR205=4.02K	X00-11
107	53	8/30/2007	P	FAE Suggest PR199=16.2K, PR200=4.02K	Change to PR199=16.2K, PR200=4.02K	X00-11
108	54	8/30/2007	P	MPL73-4R7 is not PSL	Change to MPLC0730L4R7	X00-11
109	54	8/30/2007	P	For High=1.0, Low=0.9 Output	Change PR207 to 20K/F	X00-11
110	55	8/30/2007	P	For High=1.0, Low=0.9 Output	Change PR64 to 69.8K/F	X00-11
111	56	8/30/2007	P	For High=1.0, Low=0.9 Output	Change PR66 to 22.6K/F	X00-11
				Chagne from X00-11 to X00-12		
112	32	8/31/2007	EE	Follow ME feedback. Used MIC connector in MB side.	Pop J14 and remove M1	X00-12
113	19,20	8/31/2007	EE	Follow ATI FAE. Reserved GFX thermal protect function.	Added U241,Q98,Q99,R870,R871.R872	X00-12
114	53	9/1/2007	P	FAE Suggest to remove sense resistor for saving space	Remove PR179, PR180	X00-12
115	53	9/1/2007	P	FAE Suggest to remove sense resistor for saving space	Remove PR194, PR195	X00-12

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Item	Page#	Date	T	Issue Description	Solution Description	Rev
116	55	9/01/2008	P	Change to hight rating mosfet for 9.4A	Change to FDS8880_NL	
117	55	9/01/2008	P	Change to hight rating mosfet for 9.4A	Change to FDS6676AS_NL	
118	55	9/01/2008	P	Change to hight rating mosfet for 9.4A	Change to SIL104R-1R0	
119	47	9/01/2008	P	Cancel this function. It's no use.	Remove PR74, PQ15	
120	29	9/01/2008	EE	Follow FAE feedback. Pull up resistor to +3.3V_SUS.	Added R877 10k ohm to pull up +3.3V_SUS.	X00-12
121	36	9/01/2008	EE	Follow FAE feedback. Added C1032 270p_NC to SD_CD#	Added C1032 270p_NC to CON5 pin 2 SD_CD#.	X00-12
122	15	9/01/2008	EE	Follow AMD feedback. Change SB700 VDD power rail from +1.2V_RUN to +1.2V_ALW_SUS.	Added L90 and connect to +1.2V_ALW_SUS. Depop L39.	X00-12
123	24	9/01/2008	EE	Follow AMD feedback. Change R89 from 0 ohm to 8.2k ohm.	Change R89 from 0 ohm to 8.2k ohm.	X00-12
124	26	9/01/2008	EE	Reserved caps for reduce SMBUS1 overshoot and under shoot.	Reserved C1011,C1012 47p in J1 pin5,6	X00-12
125	52	9/03/2008	P	Reserved for MAX8778	Add PR114	X00-12
126	55	9/03/2008	P	Reserved snubber	Add PR245, PC211	X00-12
127	42	9/03/2008	EE	ITE 8512 FAE concern pin 126,pin 23,pin 4,pin 15 have leakage .	Added D43~D46 to U13 pin 126, pin 23, pin 4, pin 15.	X00-12
128	5	9/03/2008	EE	Follow AMD feedback. Added 2 * MOSFET for CPU_PWRGD_SVID_REG level shift.	Added Q100,R881and modify Q76 to gate by CPU_PWRGD.	X00-12
				Chagne from X00-12 to X00-13		X00-12
129	49,51,54	9/04/2008	P	Dell suggest to add 0.1u cap near IC feedback pin to reduce feedback noise.	Add 0.1u cap	X00-13
130	51	9/04/2008	P	FAE suggest to add PR460,PC451 and PQ115 for voltage shift function.	Aadd PR460,PC451 and PQ115 for voltage shift function.	X00-13
131	19	9/04/2008	EE	Follow ATI feedback.	Reserved R889 1M for Y2 27Mhz.	X00-13
132	42	9/04/2008	EE	Added D47	Added D47 to connect WRST# and THERM_STP#	X00-13
133	33	9/04/2008	EE	Reserved BCM5784M SUPER_IDDQ circuit.	Reserved R888 20k ohm.	X00-13
134	9,27	9/04/2008	EE	Add RS780 CRT I2C function.	Connect U13 pin E8,F8 to CRT DDC bus.	X00-13
135	9,28	9/04/2008	EE	Add RS780 HDMI I2C function.	Connect U13 pin A8,B8 to HDMI DDC bus and Added level shift(R886,R887,Q101,Q102)	X00-13
				Chagne from X00-13 to X00-14		
136	31	9/05/2008	EE	Added 4 * 0 ohm for EMI.	Added R898~R901 to JSPK1.	X00-14
137	55	9/05/2008	EE	Footprint is different with PL9 sepc.	Change PL9 footprint to SIL104.	X00-14
138	24	9/05/2008	EE	ATI has update power express circuit.	Added R890~R897and depop Q3~Q10.	X00-14
139	13,39	9/05/2008	EE	Added SB_USBP8 to WLAN.	Added L115, R902, R903.	X00-14
140				**Chagne from X00-14 to X00-15**		X00-15
141	43	9/06/2008	EE	Added KB BACKLITE power switch circuit.	Added Q104,Q103,C1033,C1034,R190,R907,R908,R909 to option +KB_LED power source.	X00-15
142	43	9/06/2008	EE	Added TP power rail and change LID_SW# power rail	Added C385 and PU to +3.3V_SUS to JP2.5. Change R455 to +3.3V_ALW.	X00-15
				Chagne from X00-15 to X00-16		
143	9	9/11/2008	EE	There is on need pull-up resistor to work around for RS780 A11.	Depop R416	X00-16
144	44	9/12/2008	EE	There is not work in DC IN LED for SSI build.	Depop Q16, Q17, R44, R45	X00-16

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145	9	9/14/2007	EE	Follow ATI FAE feedback. Change the RS780 strap pin.	Depop R419 and pop R420.	X00-16
				Chagne from X00-16 to X01-1		
1	9	10/01/2007	EE	Follow ATI FAE feedback. Don't need LDT_STOP#, CPU_LDT_REQ# level shift.	Depop the level shift Q68,Q15,R414,R42 and added R757, R758 0 ohm.	X01-1
2	9	10/01/2007	EE	Follow ATI FAE feedback. Change the RS780 debug strap pin.	Added R759 3k ohm to PU +3.3V_RUN and depop the R418.	X01-1
3	9,24,27	10/01/2007	EE	Added CRT power express function.	Added R743,R744,R745,C943,R750~R756,Q100,Q101,U53~U55.	X01-1
4	9,24,26	10/01/2007	EE	Follow ATI FAE feedback(AN_RS780B1). Change the LVDS power express circuit.	Change LCD DDC circuit to isolation logic and LCD BACKLIGHT,PWM,LCD power to Wired OR.	X01-1
5	19	10/01/2007	EE	Remove M82-S Xtal circuit.	Remove R459,R457,R448,C643,C642,Y2.	X01-1
6	28	10/02/2007	EE	Follow ATI FAE feedback(AN_RS780B1). Added isolation logic on HDMI_DET.	Added Q102,R762.	X01-1
P1	46,47,48	10/02/2007	P	+5V_ALW issue when USB charger disabled in S5	Change +5V_ALW to +5V_ALW2	X01-1
P2	52	10/02/2007	P	ALW_PWRGD_3V_5V is dummy net	Remove PR104,PR203 and change connect to +3.3V_ALW	X01-1
P3	47	10/02/2007	P	To solve EE noise made by charger	Change charger output Cap 10U/25V from X6S to X5R CAP (PN: CH6104K9207)	X01-1
7	21	10/03/2007	EE	+5V_ALW issue when USB charger disabled in S5	Connect power trace from +5V_ALW to +5V_ALW2	X01-1
8	12	10/26/2007	EE	Follow AMD SCL.	Depop R694 1M ohm.	X01-1
9	19	10/26/2007	EE	The DVPDATA20~DVPDATA23 need pull-up with VDDR4/5 same power rail(+1.8V_GFX).	Change R467~R468 pull-up power rail from +3.3V_RUN to +1.8V_GFX.	X01-1
10	19	10/26/2007	EE	Swap G_DAT_DDC2/G_CLK_DDC2 signals.	Swap G_DAT_DDC2/G_CLK_DDC2 signals on R79/R77	X01-1
P4	51	10/30/2007	P	Change capacitor to resistor for reserve pull low	Change PC13 to PR104	X01-1
P5	51	10/30/2007	P	NB_VCORE will OVP when voltage switch	Follow FAE suggestion to put PR236 and PR237	X01-1
P6	47,51,52	10/30/2007	P	SI4810 EOL Issue	Change PQ41,PQ2,PQ23,PQ27 to SI4812	X01-1
P7	51,54	10/30/2007	P	To reduce Vo jitter issue	Change PC97 and PC72 to 220u/2.5V/ESR15	X01-1
11	10	10/31/2007	EE	RS780M change form A11 to A12 and don't need work around.	Pop L71 and Depop L12,C87,U6,R59,R60,C82.	X01-1
12	13	10/31/2007	EE	Added Express card power enable on SB700. It's for Express card hot plug.	Change U39.B8 from USB_OC5# to EXPRCRD_PWREN# and connect to CN2.	X01-1
13	28	10/31/2007	EE	Follow ANT HDMI detect circuit.	Added Q102,R762, pop R43 and remove D18, R411	X01-1
14	32	10/31/2007	EE	Added +3.6V_CAMERA Camera power circuit	Added U56,C944,C945,C946,R763,R764.Remove C264. Modify JCAMERA1 pin define and L33 power rail.	X01-1
15	38	10/31/2007	EE	Added USB charge circuit for leakage.	Added Q103,R765,U57,U58.	X01-1
16	42	10/31/2007	EE	Swap U9.31 NUM_LED# and U9.98 KB_BACKLITE_EN	Swap U9.31 NUM_LED# and U9.98 KB_BACKLITE_EN	X01-1
17	44	10/31/2007	EE	Depop SNIFFER_YELLOW LED circuit. and Swap WIRELESS_ON/OFF#, SNIFFER_PWR_SW# circuit.	Depop R477,Q75,Q71,R453 and Swap R392, R452 signals	X01-1
18	43	10/31/2007	EE	Change KB_LED pwoer ciruit.	Pop R214, Add Q104 and Depop R221,R223,Q46,Q39,C319,C310,R199 and modify J4 pin define.	X01-1
19	9,45	10/31/2007	EE	Depop SB700 A11 WD_PWRGD work around circuit.	Depop U28,C690,R511 and pop R516,R416.	X01-1
20	42	11/01/2007	EE	Change GPIO and remove SNIFFER_YELLOW function.	Move 5V_ALW_ON to U9.83, Move NUM_LED# to U9.88 and remove R477,Q75,Q71,R453	X01-1
				Chagne from X01-1 to X01-2		
P8	55	11/01/2007	EE	Added tree level GFX voltage control.	Added PR238,PC210,PR242,PR243,PR239,PC90,PQ56	X01-2
21	19	11/01/2007	EE	Added tree level GFX voltage control.	Pop R112 and change it from GFX_CORE_CNTRL0 to GFX_CORE_CNTRL1	X01-2

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22	5,12	11/01/2007	EE	+5V_ALW issue when USB charger disabled in S5	Change R135,R374 from +5V_ALW to +5V_ALW2	X01-2
23	33,34	11/02/2007	EE	Change BCM5787M to BCM5784M.	Change BCM5787M to BCM5784M.	X01-2
24	31	11/02/2007	EE	Change STAC9228 to 92HD73C.	Change STAC9228 to 92HD73C.	X01-2
25	14	11/05/2007	EE	Follow ATI SCL and feedback.	Added R766 0 ohm connect U39.C6 TEMP_COMM to GND.	X01-2
26	13,39	11/05/2007	EE	Change WLAN from USB port 8 to USB port 4.	Change WLAN from SB_USBP8+/- to SB_USBP4+/- and Move to U39.B12,U39.A12.	X01-2
27	19	11/05/2007	EE	Change M82-S pin straps from +3.3V_RUN to +3.3V_DELAY. It will avoid leakage during power-up.	Change M82-S GPIO to +3.3V_DELAY	X01-2
28	38	11/05/2007	EE	Co-lay USB Q-switch and 0 ohm	Reserved R767~R770 0 ohm with U57 pin 2,3,5,6,U58 pin 2,3,5,6.	X01-2
P9	46	11/05/2007	P	Modify +5V_SUS load switch	Remove PQ12	X01-2
P10	53	11/05/2007	P	FAE suggest to reserve	Add PR241	X01-2
P11	54	11/05/2007	P	Modify current limit value	Change PR228 from 10K to 5.9K	X01-2
P12	55	11/05/2007	P	Update the resistor value	Update PR34,PR35,PR36,PR30,PR244,PR238	X01-2
P13	49,51,53,54,55	11/05/2007	P	To solve power good glitch issue	Connect IC power to +5V_ALW2	X01-2
P14	49	11/05/2007	P	Set tracking discharge mode	PR229 populate and PR230 NC	X01-2
P15	52	11/05/2007	P	5V_ALW_ON pull low at initial state	Add PR245	X01-2
P16	53	11/05/2007	P	CPU_VCORE_ENABLE pull low at initial state	Add PR246	X01-2
29	42,44,48	11/06/2007	EE	Remove DC IN LED circuit and change signal name DCIN_DETECT_LED# to CHIPSET_ID1.	Remove R44,Q17,Q16,R45 and change U9.99 signal name DCIN_DETECT_LED# to CHIPSET_ID1.	X01-2
P17	51,54	11/06/2007	P	For space saving.	Remove PC1,PC93.	X01-2
30	42	11/07/2007	EE	Add BID1 to EC pin98	Connect R482,R483 to U9.98	X01-2
31	42	11/07/2007	EE	Remove double pull-up resistor.	Remove R152,R542	X01-2
				Chagne from X01-2 to X01-3		
32	5	11/09/2007	EE	Solve glitch from CPU_PWRGD.	Added C947 0.1uF on CPU_PWRGD.	X01-3
33	14,42	11/09/2007	EE	Solve S5 leakage.	Connect L51 from +3.3V_ALW to +3.3V_SUS and remove R134 for SIO_SLP_S5#.	X01-3
P18	51	11/12/2007	P	Follow AMD FAE suggest +NB_VCORE dynamic voltage design	Remove PQ7,PC15,PR18,PR13	X01-3
P19	49,51,54	11/12/2007	P	Reserve for solving giltch issue caused by IC power rail	Add PR247,PR13,PR18,PR248,PR249	X01-3
P20	54	11/12/2007	P	To solve jitter issue	Change PL2 from 4R7 to 3R3	X01-3
34	5	11/15/2007	EE	Follow ANT reference to solve S3 leakage.	Change R103,R149,R143,R132 pull-up from +1.8V_SUS to +1.8V_RUN.	X01-3
35	12	11/15/2007	EE	Solve CPU_PWRGD voltage too low(+1.5V).	Change Q57 from MMBT3904 to FDV301N.	X01-3
36	42	11/15/2007	EE	Check with power team and EC. The charge IC INP pin can be read with EC ADC function.	Pop R133 0 ohm and depop R128 0 ohm.	X01-3
37	14,33,36,42	11/15/2007	EE	Follow XTAL vendor feedback to change the XTAL caps.	Change C249, C250 to 18pF. C518 to 27pF. C813 to 22pF, C859, C860 to 12pF	X01-3
38	43	11/15/2007	EE	Follow Dell recommend.	Change R214 0 ohm to FS3.	X01-3
39	31,32	11/16/2007	EE	Follow IDT recommend to change caps for batter Audio Precision.	Change C932, C927, C823, C814 from 1uF to 2.2uF.	X01-3
40	5,12	11/16/2007	EE	Follow ANT 3.2 reference schematic to remove CPU_PROCHOT# level shift.	Remove R89, R91, Q24.	X01-3

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				Chagne from X01-3 to X01-4		
41	14	11/19/2007	EE	Follow AMD SB700 design guideline to add series resistor.	Add R771, R772 4.99 ohm at U39 AD13,AE13 SATA_TX3+/- for ESATA signals.	X01-4
42	9,12,24,28	11/19/2007	EE	Follow AN_RS780B1 to modify the PX circuit and update RS780M symbol.	Move PE_GPIO2 to U22.B8), NB_LCD_BKL_EN from SB700.AE2 to R413. Remove Q12,Q13.	X01-4
43	44	11/19/2007	EE	Sniffer should be during S5.Dell define our Sniffer switch need to stay 'ON' after the WiFi can be enable.	change R392 to +3.3V_ALW.	X01-4
P21	46	11/19/2007	P	Reduce RUN/SUS PW switch circuit.	Remove PR(118,121,222,226,77,79,93,91) and change PQ(15,21,35,54) to 2N7002W-7-F.	X01-4
P22	46	11/19/2007	P	Reduce RUN/SUS PW switch circuit.	PC73,PC46,PC192,PC177,PC62,PC58,PC49 from 10U/1206 to 0.1U/0603	X01-4
44	38	11/20/2007	EE	Depop Q-switch function on PT build.	Depop Q103,R765,U57,U58 and pop R767~R770.	X01-4
45	19	11/20/2007	EE	Remove double pull-up resistor.	Remove R66,R71 pull-up resistor.	X01-4
P23	49	11/20/2007	P	Reduce Jitter	Change PC201 and PC200 from 330u/ESR15 to 220u/ESR25	X01-4
P24	52	11/20/2007	P	PC185 is no use for schematic	Remove PC185	X01-4
P25	53	11/20/2007	P	To reduce input ripple	Add PC211 and PC212	X01-4
P26	55	11/20/2007	P	Reduce Jitter	Change PC171 to 330uF/2V/ESR9	X01-4
P27	47,48,55	11/20/2007	P	2nd Source suggest to change	Change PD9 and PD6 to RB500V-40 , PQ4 to FDV301N	X01-4
P28	47	11/20/2007	P	UL schemaitc are going to be replaced by EC control	UL schemaitc component are NC.	X01-4
46	42	11/21/2007	EE	Follow ITE feedback to reserve caps for ITE8512JX.	Add C948, R773 to U9 pin 12.	X01-4
47	38	11/21/2007	EE	Change USB Q-switch power rail from +3.3V_RUN to +3.3V_SUS.	Change U57 pin 8, U58 pin 8 from +3.3V_RUN to +3.3V_SUS, Q103 pin2 from RUN_ON to SUS_ON.	X01-4
48	19	11/21/2007	EE	Strengthen PCIE FULL TX OUTPUT SWING and TRANSMITTER DE-EMPHASIS.	Pop R104, R485 10k ohm.	X01-4
49	33,34	11/21/2007	EE	Modify LAN 1000 LED circuit to solve BCM5784M LED issue.	Add D38,R774 to solve BCM5784M 1000 LED issue.	X01-4
50	28	11/22/2007	EE	Change HDMI connector symbol.	Change CN3 connector symbol.	X01-4
51	32	11/22/2007	EE	Remove these 20K ohm resistors because it is for desktop design or codec internal headphone amplifier.	Depop R606, R614, R639, and R648.	X01-4
52	38	11/22/2007	EE	For EMI solution to pop choke.	Pop L25,L27 and depop R119, R109,R130,R124.	X01-4
53	44	11/23/2007	EE	For EMI solution to add caps.	Add C949~C952 100pF.	X01-4
54	50	11/23/2007	EE	Base on RS780M T13 timing. +1.8V_RUN rise need before then +1.1V_RUN.	Change PR83 from 0 ohm to 200k ohm and depop PC50 from 0.01u to 0.1u.	X01-4
P29	53	11/24/2007	P	EMI Solution	Add PC185,PC213,PC214,PC215,PC217,PC216,PC218,PC220,PC219	X01-4
P30	48	11/24/2007	P	For ESD protect	EMI Suggestion PD7 populate	X01-4
55	25	11/23/2007	EE	EMI Solution	EMI Suggestion C753, C271 populate	X01-4
56	12	11/23/2007	EE	EMI Solution	EMI Suggestion C406 populate	X01-4
57	32	11/23/2007	EE	EMI Solution	EMI Suggestion C789,C800,C770,C751 change form 220pF to 470pF.	X01-4
58	32	11/23/2007	EE	IDT had found out the resonance on portA and suggested change 220pF to 47pF for EMI.	Change C770, C751 from 220pF to 47pF.	X01-4
				Chagne from X01-3 to X01-4		
59	41	11/26/2007	EE	BT1 connector pin define is different before.	Change BT1 pin 2 to GND, pin 1 to +RTC.	X01-5
60	42	11/26/2007	EE	Sniffer power switch needs to wake up EC, when battery only. So it needs to use WUI pin.	Swap U9.108 SNIFFER_PWR_SW# and U9.35 WIRELESS_ON/OFF#	X01-5

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61	36	11/26/2007	EE	EMI Solution	Add C961~C963 27pF for EMI solution.	X01-5
P31	51	11/26/2007	P	FAE suggest to reserve RC to slow down voltage switch	add the R/C at PQ57 to slow down PQ57 switcher to against OVP, and remove R/C in front of PQ5	X01-5
P32	51,54	11/26/2007	P	Got more performance for jitter issue	Change PC97 and PC72 from 220u/2.5V/ESR15 to 220u/4V/ESR40	X01-5
P33	49	11/26/2007	P	More suitable OCP Value	Change PR233 to 11.8K	X01-5
62	32	11/26/2007	EE	Follow FAE suggest.	Change U16 pin 21~25 to NC.	X01-5
63	38	11/26/2007	EE	EMI Solution	Populate ESD3 for EMI suggest.	X01-5
64	5	11/26/2007	EE	Solve system shut down issue from CPU_THERMTRIP#.	Add Q105,Q106,R776,C964 and connect H_THERMTRIP# to 3V, 5V ALW circuit.	X01-5
65	5	11/26/2007	EE	Follow ANT 3.2 schematic PX circuit to change M82-S reset signal from LAN_RST# to PLTRST#	Depop R159 and pop R158.	X01-5
66	12	11/28/2007	EE	Follow ANT 3.2 schematic.	Depop R678, R682.	X01-5
67	33	11/28/2007	EE	Follow Broadcom FAE feedback. BCM5784M CLKREQ# can't work.	Pop R651 ohm and depop R650 4.7k ohm before CLKREQ can work.	X01-5
				Chagne from X01-5 to X02-1		
1	5	12/28/2007	EE	Follow AMD Griffin sighting Dec 18.pdf to reserve resistor for system hang or shut downboot issue.	Add R777,R778 and pop R164 300 ohm for system hang or shut down issue.	X02-1
2	43	1/2/2008	EE	Change MMB pin 1 power source to 5V_ALW to fix LED flash issue when AC/Bat plug in.	Change JP1.1 from +5V_ALW2 to +5V_ALW.	X02-1
3	43	1/4/2008	EE	Change Num, Cap power rail to +5V_RUN to fix Num, Cap LED flash issue when AC/Bat plug in.	Change Q77~Q80, R108, R115 power rail to +5V_RUN.	X02-1
4	22	1/8/2008	EE	Follow REF132-9.Change M82-S GPIO/DDC to +3.3V_DELAY. It will reduce leakage to +3.3V_DELAY.	Change SMBUS(Q19, Q21), Thermal monitor (U8) power rail from +3.3V_RUN to +3.3V_DELAY.	X02-1
5	38	1/10/2008	EE	Fulfill Reliability team request.	Connect JUSB1.8 to USB_BACK_PWR.	X02-1
6	43	1/11/2008	EE	Avoid system can enter S3 mode but wake up fail problem.	Change the lid switch IC power source from 3.3V_SUS to 3.3V_ALW.	X02-1
7	32	1/11/2008	EE	Change L35 to 22 ohm. It will help DMIC_CLK_L performance.	Change L35 to from 0 ohm to 22 ohm.	X02-1
8	38	1/11/2008	EE	Remove USB charge function.	Remove R765, Q103, U57, U58, R767~R770.	X02-1
9	38	1/14/2008	EE	Follow AMD AN_SB700AB5. Added re-driver IC to increase signal stress for ESATA.	Remove R771, R772 4.99 ohm. Added U63 3211B,R780~R785 0 ohm, C965~C968 0.1u, C969~C972 0.01u.	X02-1
10	28	1/14/2008	EE	Modify HDMI detect circuit.	Added Q107,R779 10k and change R762 to 10k ohm.	X02-1
11	42	1/14/2008	EE	Change EC from ITE8512IX to ITE8512JX. The pin12 need connect to 0.1uF, 1uF.	Change R773 to C973 0.1u, pop C948 1u and for EC ITE8512 rev change.	X02-1
12	12,14,	1/16/2008	EE	Follow DELL recommand to void the PCICLK5 emission issue even AMD solved it in BIOS code	Move R301 22 ohm and CLK_PCI_PCCARD signal form PCICLK5 to PCICLK1.	X02-1
P1	47	1/21/2008	P	Change to X6S material due to not support pulse charge	Change PC114, PC110, PC106 and PC117 to X6S material	X02-1
P2	51	1/21/2008	P	Derating team suggest for WCETPA	Change PR10 from 10K ohm to 11.8K ohm.	X02-1
P3	51	1/21/2008	P	Reduce output ripple voltage	Change PC97 ESR from 40m ohm to 25m ohm.	X02-1
P4	52	1/21/2008	P	Derating team suggest for WCETPA	Change PR212 from 294K ohm to 340K ohm.	X02-1
P5	54	1/21/2008	P	Derating team suggest for WCETPA	Change PR228 from 5.9K ohm to 7.5K ohm.	X02-1
P6	55	1/24/2008	P	To combine MFG P/N	Change PQ10, PQ56 P/N from BAM01380016 to BAM01380008	X02-1
13	28	1/25/2008	P	HDMI ID 7-13: DDC Capacitance over spec 50pf. We will add level shift circuit to reduce Capacitance.	Add level shift Q108, Q109 FDV301N to reduce the DDC Capacitance.	X02-1
				Chagne from X02-1 to X02-2		X02-1
14	9,11,12,18~24 ,26~28	1/28/2008	P	Remove Power Express function.	Remove LCD, CRT hybrid function and depop side port memory.	X02-2

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Item	Page#	Date	T	Issue Description	Solution Description	Rev
15	15	1/29/2009	EE	Follow AMD feedback.IDE and Flash Interface Not Implemented: Decoupling caps not used.	Depop C397, C427, C428, C409, C420.	X02-2
16	15	1/29/2010	EE	Follow AMD SB700 checklist item 1-34, 1-35.	Change L48 to BLM21PG221SN1D, C464 to 10U.	X02-2
17	9, 13	1/29/2010	EE	Follow AMD RS780M item 8-7, SB700 item 7-1, 7-2 checklist to reserve PD resistor.	Reserve R786 4.7k and R787, R788 10k ohm.	X02-2
18	12	1/29/2010	EE	Follow AMD SB700 checklist item 12-4 to depop RP33.	Depop RP34 8.2k ohm.	X02-2
19	9	1/30/2008	EE	Follow AMD SB700 checklist item 24-17. Change PU resistor to 300 ohm.	Change R416 4.7k to 300 ohm.	X02-2
20	13	1/30/2008	EE	Follow AMD SB700 checklist item 24-24. Depop PU resistor.	Depop R335 10k ohm.	X02-2
21	10, 11	1/30/2008	EE	Follow AMD checklist 1-7~1-21,17-2,17-4,17-6. Depop resistors and caps without side port memory.	Depop R415, RP21~RP31 47 ohm, relate side port memory caps and connect VDD_MEM to GND	X02-2
22	28	1/30/2008	EE	Follow EMI suggest to pop comon mode choke for HDMI.	Pop L58, L59, L60, L61, EXC24CG240Uand depop R397, R401, R403~R408 0 ohm.	X02-2
23	38	1/30/2008	EE	Follow EMI suggest to pop comon mode choke for USB.	Pop L25, L27 DLP11SN900HL2L. Depop R119, R109, R124, R130 0 ohm.	X02-2
24	29	1/31/2008	EE	OTP change to 85C and THERM_ALERT#_C, SYS_SHDN# leakage will affect OTP thermal limit.	Change OTP resistor to 10k, 6.8k ohm. Add D39 to prevent leakage.	X02-2
25	27	1/31/2008	EE	Follow EMI suggest to pop caps for CRT.	Pop C613, C622, C637 22pF and C614, C624, C633, C83, C73 10pF.	X02-2
26	9,25	2/1/2008	EE	Follow CLK Gen vendor feedback to solve EA fail.	Change R146 to 43.2 ohm, R40 to 0 ohm, C50 to 49.9 ohm.	X02-2
27	42	2/12/2008	EE	Use ITE8512 pin 22 detect SB_AZ_CODEC_RST# to mute speaker pop noise.	Connect SB_AZ_CODEC_RST# and U9 pin 22.	X02-2
28	5	2/12/2008	EE	Follow ANT 4.1d. CPU_TEST23_TSTUPD need PD 300 ohm.	PD R791 300 ohm for CPU_TEST23_TSTUPD.	X02-2
29	43	2/12/2008	EE	Add JP1 pin 10 to +3.3V_ALW, let +3.3V_ALW get lower drop voltage on MMB side.	Add JP1 pin 10 to +3.3V_ALW.	X02-2
P7	50,52	2/13/2008	P	Change PU3, PU5 and PU9 VCC power rail to reduce S5 power consumption.	Change PJP.1 to +3.3V_SUS and add PR251~PR254 0 ohm.	X02-2
30	38	2/22/2008	EE	Pop ESATA re-driver for stress ESATA signals on formal build.	Depop R782~R785, change C857,C858,C971, C972 to 0.01u and pop U63,C965~C968.	X02-2
31	31	2/22/2008	EE	Dell recommend change caps for IDT AP test on formal build.	Change C916, C917 to 6800pF.	X02-2
32	46	2/22/2008	EE	To meet M82 sequence spec. +1.8V_RUN need ramp after +VCC_GFX_CORE.	Change PR80, PR92 to 680K ohm.	X02-2
				Chagne from X02-2 to A00-1		
1	42	3/14/2008	EE	Change board ID for A00.	Pop R522 and depop R523.	A00-1
P1	53	3/14/2008	P	Follow EMI suggest.	Pop PC213, PC217, PC220 0.01u and PC214, PC216, PC219 0.1u.	A00-1
2	31,32	3/14/2008	EE	Need meet WLP4.0 : 1. Add 2.2K-ohm resistors to prevent amplifier clipping.	Add R792~R795 2.2k ohm.	A00-1
				Need meet WLP4.0 : 2. Add 220PF capacitors to allow proper dynamic range measurent.	Add C974, C975 220pF and pop C928, C929 to 220pF.	A00-1
3	27,32,38,,39,41	3/17/2008	EE	Follow Safety request. Change USB power control IC, RTC location same as Intel location.	Swap U7 and U10, U16 and U17. U7 and U16 are 2062AD. Change D34 to D18. Swap R676 and R218.	A00-1
4	38	3/18/2008	EE	TI can't finish some necessary legal submission for new 2062AD. Change to old part 2062DR.	Change U7, U16 to 2062DR (AL002062005).	A00-1
5	15,49,50,51 ,52,55	3/18/2008	EE	Short +3.3V_ALW_R Jump and Remove Power Jump for A00.	Remove PJP1, PJP2, PJP4, PJP6~PJP9, PJP11~PJP18 and short PJP10	A00-1
6	38	3/18/2008	EE	Follow QSMC request to remove USB co-lay 0 ohm.	Remove R109, R119, R124, R130 0 ohm.	A00-1
7	38	3/19/2008	EE	Change the USB Power Jump to short pad fp.	Change PJP3, PJP5 fp to SHORT-10A.	A00-1
8	42	3/19/2008	EE	Follow IT8512JX glitch.doc FA report. Depop 1uF for ITE8512JX pin 12.	Depop C948 1uF.	A00-1
10	38	3/20/2008	EE	Pericom request. Add 330ohm to reduce output swing, change AC caps to 2.2nF and set EQ to GND.	Add R796 330 ohm. Chagne C677,C678,C857,C858,C969~C972 to 2.2nF and PD U63 pin1, pin10 to GND.	A00-1

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Item	Page#	Date	T	Issue Description	Solution Description	Rev
11	14, 43	3/20/2008	EE	Follow Dell request. Add LED KB BK detect function.	Add R797 100k ohm , PD R798 200k ohm to J4 pin2 and connect to U39 pin G6	A00-1
12	28	3/20/2008	EE	Change to FDV301N will pass HDMI 7-12 HDMI detect test.	Change Q102 from MM3904 to FDV301N.	A00-1
13	59	3/26/2008	EE	Follow EMI team request, add two EMI SPRING near sniffer switch area nad HDMI connector.	Add PV1 near SW1. PV2 near CN3.	A00-1
14	32	3/26/2008	EE	Follow IDT request, change 220pF to 270pF will over 80db on DTM.	Change C810, C821, C974, C975 from 220pF to 270pF.	A00-1
15	36	3/27/2008	EE	Follow EMI team request, add a 27p capacitor for 8 in 1 card reader.	Pop C963 27pF for EMI.	A00-1
P2	48	3/27/2008	EE	Follow EMI team request, add two set of 1000pF, 0.01uF, 0.1uF on J8 +DCIN_JACK , -DCIN_JACK.	Add PC221~PC223 on J8 +DCINI_JACK, PC224~PC226 on J8 -DCIN_JACK.	A00-1
P3	49, 51	3/27/2008	EE	Follow EMI team request, pop PR2, PC5 for NB_VCORE and pop PR234, PC208 for +1.8V_SUS	pop PR2, PC5 for NB_VCORE and pop PR234, PC208 for +1.8V_SUS	A00-1
16	5, 42	3/27/2008	EE	Use BID1 to control CPU_PROCHOT#. When system need change state to P1 by HTC.	Add Q110 2N7002W-7-F , R799 0 ohm for use BID1 to control CPU_PROCHOT#.	A00-1
17	39	3/28/2008	EE	Remove debug board resistor.	Depop R631~R635, R659, R259 0 ohm.	A00-1
18	5	4/09/2008	EE	Follow ANT 5.0e to depop R791 since the PD is for desktop CPU but Griffin	Depop R791 300 ohm.	A00-1
19	3, 46, 54	4/15/2008	EE	Fixed VLDTA&B Vmin not exceeded 1140mV.	Change C665,C672,C673 to 10uF, PR115 to 47.5k, PQ28 to FDS6298.	A00-1
20	5, 12	4/15/2008	EE	Follow AMD feeback. CPU_PWRGD need meet 0.01V/ns.	Depop C947, D4, R374, R375, R378, Q56, Q57.	A00-1
P4	53	4/15/2008	P	To Solve K11 NPT Transient Response Failed	Change PC31, PC33 to 470uF/ESR6 and pop PC34 to 470uF/ESR6	A00-1
	53	4/15/2008	P	To Solve K11 NPT Transient Response Failed	Change PC36, PC38 to 330uF/ESR9 and pop PC43 to 330uF/ESR9.	A00-1
P5	53	4/28/2008	P	Due to the high temperature will cause the OCP drop closed to TDC 18A. It's margin for worst conditions, in order to more safely without trigger OCP easily while changed the resister from 18K to 22K.	Change PR193, PR195 from 16.2K to 22K.Set OCP at 35A to meet AMD Spec.	A00-1
				Chagne from A00-1 to A00-2		
21	44	5/20/2008	EE	Tune RBAT2_LED(Amber) Light	Change R114 from 220 ohm to 68 ohm.	