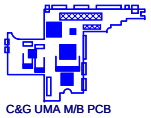



# Cosica / Gilligan UMA

**VER : 2B**

**POWER**

**SYSTEM RESET CIRCUIT** PG 38

**BATT CHARGER** PG 40

**RUN POWER SW** PG 39
+3.3V_SUS/+5V_SUS/+3.3V_M
+5V/+3.3V/+1.8V/+1.25_RUN
PG 41

**AC/BATT CONNECTOR** PG 41

**Merom**
(478 Micro-FCPGA)
PG 3,4
(Symbol Rev.09)

667/800 MHz FSB

**POWER**

**REGULATOR** PG 43
+1.5V_RUN/+1.05V_VCCP

**REGULATOR** PG 42
+1.8V_SUS/+1.25V_SRC_M
+1.05V_M/+0.9V_DDR_VTT

**CPU VR** PG 45

**DC/DC** PG 44
+3.3V_ALW/+5V_ALW/+15V_ALW

**CLOCK gen.**
CK505
PG 17

**Crestline**
1299 uFCBGA
PG 5,6,7,8,9,10
(Symbol Rev.09)

LVDS → **Panel Connector** PG 18

TVOUT → **S-Video CONN.** PG 19

VGA → **CRT CONN.** PG 19

**DDR2-SODIMM1** PG 15,16 — 533/667 MHZ DDR II

**DDR2-SODIMM2** PG 15,16 — 533/667 MHZ DDR II

USB2.0 (P0,P1) (EXT SIDE)
USB2.0 (P2,P3) (EXT BACK)
→ **USB X 4** PG 27

**Fix ODD** PG 23 — IDE

DMI interface

**ICH8-M**
676 BGA
PG 11,12,13,14
(Symbol Rev.09)

33MHz PCI → **R5C833 Controller** PG 20-22
→ **1394 & Conn.** PG 21
→ **8 in 1 Conn.** PG 22

**SATA - HDD** PG 23 — SATA

33MHz PCI → **LOM BCM4401 B0** PG 35,36

IHDA

PCIEx1
USB2.0 (P6)
→ **EXPRESS-CARD** PG 26

PCIEX3
USB2.0 (P7,P9)
→ **MINI-CARD x3** WPAN & WWAN & WLAN PG 24,25

**AUDIO/AMP** PG 32,33

**MDC BTB connector.** PG 26

**S/PDIF** PG 20

**Audio jack BTB Conn.** PG 33

SPI

LPC

USB2.0 (P5) → **Dig Camera** PG 33

PG 28

To connector for Media board/Touch pad/KBC module PG 31

BC
PS/2
Media board Controller signal

**SIO**
MEC5025
128KB Flash
TMKBC
128 Pins VTQFP
PG 28

BC

**SIO**
ECE5011
Expander
GPIOs
128 Pins VTQFP
PG 29

SPI

**FLASH** PG 30

**CIR** PG 31

**USER INTERFACE** PG 37

**FAN & THERMAL** EMC4001 PG 34



QUANTA COMPUTER

| | | |
|---|---|---|
| Title | Schematic Block Diagram1 | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Thursday, January 25, 2007 | Sheet 1 of 60 | |

## INDEX

| Pg# | Description | DNI LIST |
|---|---|---|
| 1 | Schematic Block Diagram | |
| 2 | Front Page | |
| 3-4 | Merom | |
| 5-10 | Crestline | |
| 11-14 | ICH8M | |
| 15-16 | DDRII SO-DIMM(200P) | |
| 17 | Clock Generator | |
| 18-19 | VGA/LVDS/CRT/S-Video | |
| 20 | 8 in 1 controller | |
| 21 | 1394 function | |
| 22 | 8 in 1 connector | |
| 23 | SATA & IDE Conn | |
| 24-25 | Mini Card (WLAN/WPAN/WWAN) | |
| 26 | Express Card + MDC BTB Connector | |
| 27 | USB Conn. | |
| 28 | SIO (MEC5025) | |
| 29 | SIO (MEC5011) | |
| 30 | Flash / RTC | |
| 31 | TP/KB/Media/CIR Conn. | |
| 32-33 | Audio CODEC(STAC9200)/Phone Jack | |
| 34 | FAN & Thermal | |
| 35-36 | LOM (BCM4401) | |
| 37 | Dash/LED/BT Conn. | |
| 38 | System reset CKT. | |
| 39 | RUN Power Switch | |
| 40 | Battery Charger | |
| 41 | DCIN/Batt Conn. | |
| 42 | 1.25V,1.8V,0.9V | |
| 43 | 1.5VSUS,1.05V(VTT) | |
| 44 | D/D Power | |
| 45 | CPU_ISL6260(3phase) | |
| 46 | EMI CAP & Screw Hole. | |

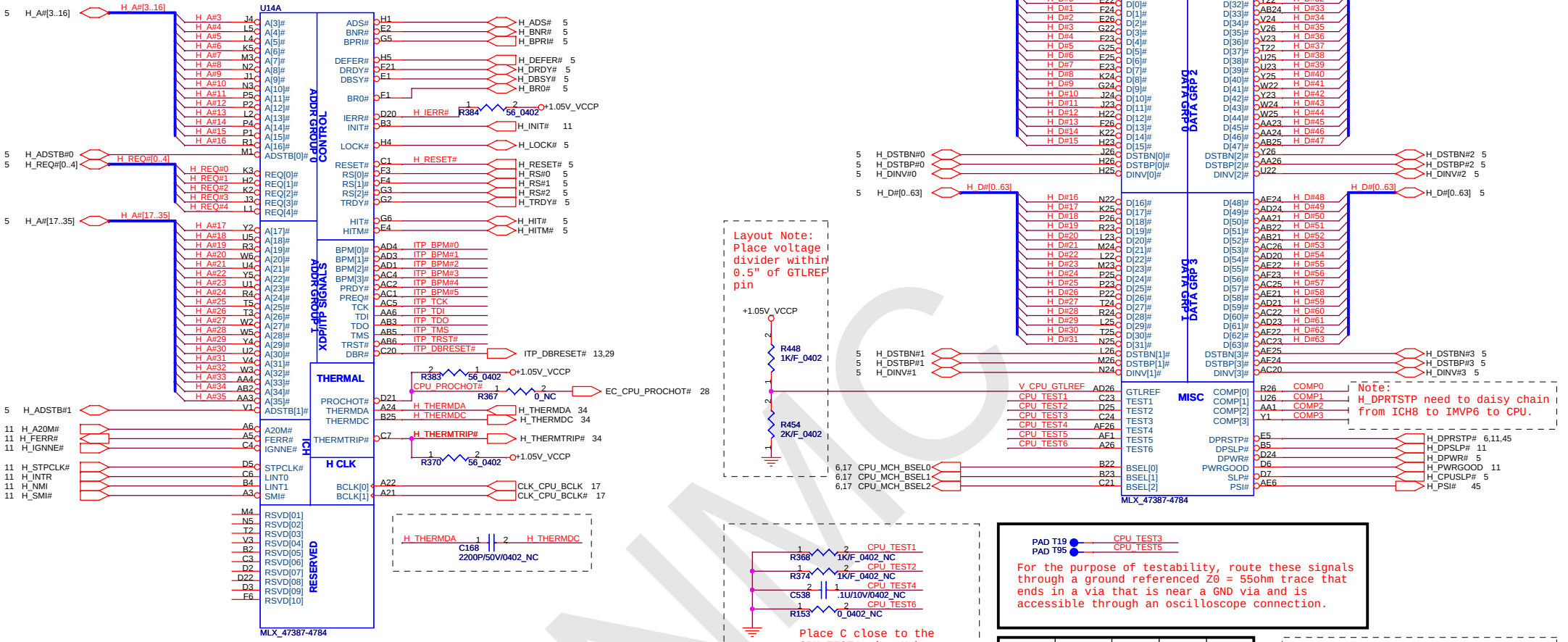
## Power & Ground

| Label | Pg# | Description | Control Signal |
|---|---|---|---|
| DC_IN+ | | AC ADAPTER (19V) | |
| PBATT+ | | MAIN BATTERY + (10~17V) | |
| PBATT+ | | SECOND BATTERY + (10~17V) | |
| PWR_SRC | | MAIN POWER (10~19V) | |
| RTC_PWR3_3V | | RTC & +3.3V_RTC_LDO(3.3V) | |
| +VCC_CORE | | CPU CORE POWER (1.5V) | RUNPWROK |
| +15V_ALW | | LARGE POWER (15V) | SUS_ON |
| +3.3V_RUN | | SLP_S3# CTRLD POWER | RUN_ON |
| +3.3V_SUS | | SLP_S5# CTRLD POWER | SUS_ENABLE |
| +3.3V_ALW | | 8051 POWER (3.3V) | ALWON/THERM_STP# |
| +5V_RUN | | SLP_S3# CTRLD POWER | RUN_ON |
| +5V_SUS | | SLP_S5# CTRLD POWER | SUS_ON |
| +5V_HDD | | HDD POWER (5V) | +5V_RUN |
| +5V_MOD | | MODULE POWER (5V) | HDD_EN |
| +5V_ALW | | LCD/CHARGE POWER (5V) | |
| +VDDA | | AUDIO ANALOG POWER (5V) | AUDIO_AVDD_ON |
| +1.5V_RUN | | CALISTOGA/ICH7 POWER | RUN_ON |
| +1.05V_VCCP | | CPU/CALISTOGA/ICH7 POWER | RUN_ON |
| +1_8V_SUS | | SODIMM POWER | SUSPWROK_5V |
| +1.8V_RUN | | SDVO POWER | RUN_ON |
| +0.9V_DDR_VTT | | SODIMM POWER | RUN_ON |
| +3.3V_LAN | | LAN POWER | AUX_EN |
| | | | |
| | | | |
| GND | ALL PAGES | DIGITAL GROUND | |
| AGND_ISL6260 | | CPU GND | |
| AGND_TPS51120 | | DC/DC POWER GND | |
| AGND1 | | VTT POWER GND | |
| AGND2 | | VTT POWER GND | |
| 8731AGND | | CHARGER GND | |
| | | | |



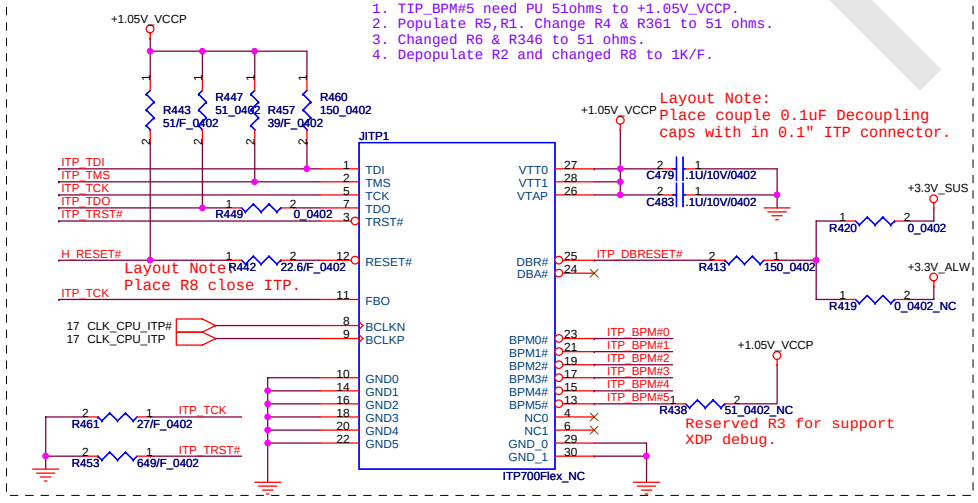
QUANTA COMPUTER

| | | |
|---|---|---|
| Title | Index, DNI, Power & Ground | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 2 of 60 | |




## Populate ITP700Flex for bringup

For Support XDP:
1. TIP_BPM#5 need PU 51ohms to +1.05V_VCCP.
2. Populate R5,R1. Change R4 & R361 to 51 ohms.
3. Changed R6 & R346 to 51 ohms.
4. Depopulate R2 and changed R8 to 1K/F.



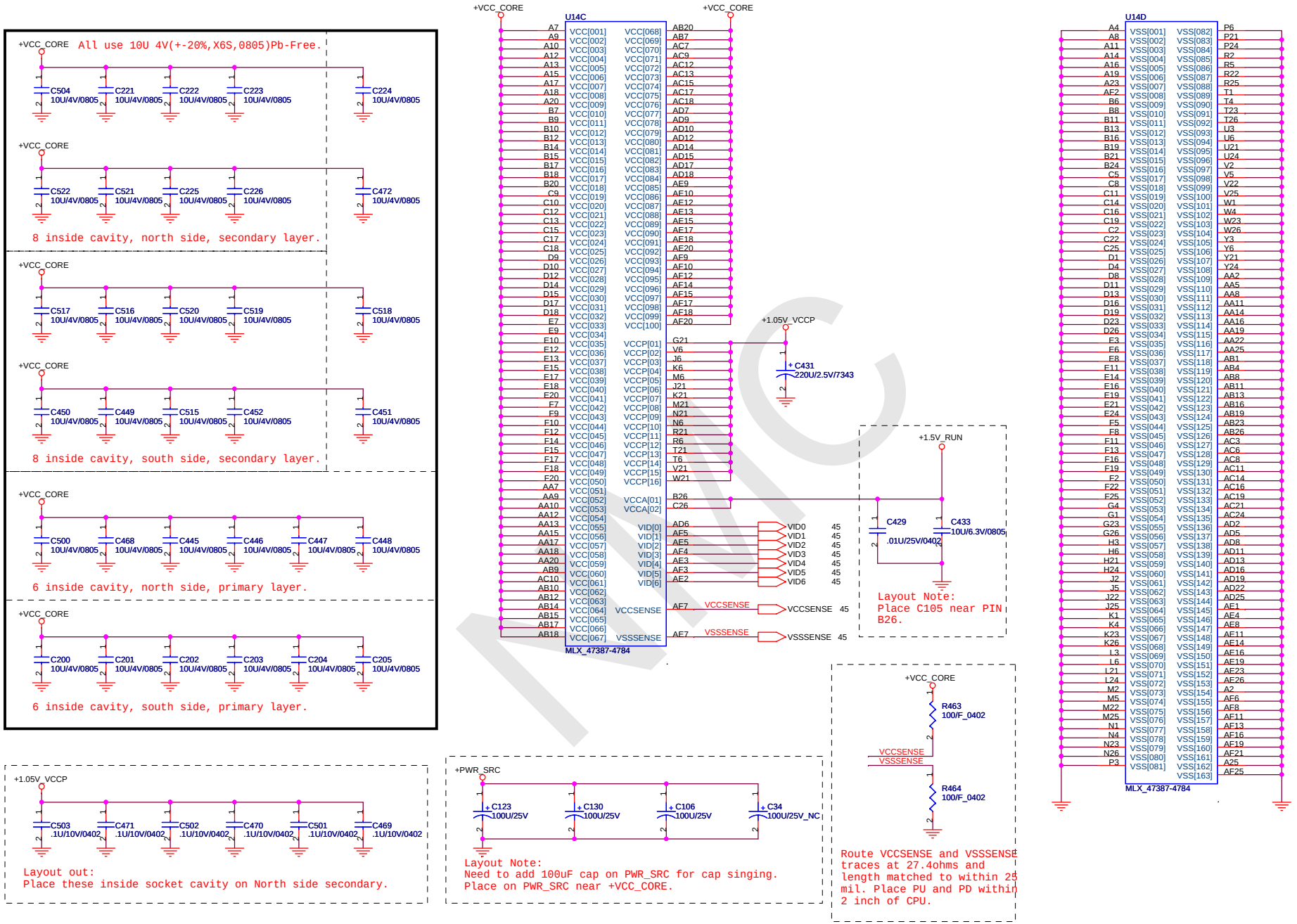

| FSB | BCLK | BSEL2 | BSEL1 | BSEL0 |
|---|---|---|---|---|
| 533 | 133 | 0 | 0 | 1 |
| 667 | 166 | 0 | 1 | 1 |
| 800 | 200 | 0 | 1 | 0 |

ITP700 layout guidelines

| Signal | Resistor Value | Connect To | Resistor Placement |
|---|---|---|---|
| TDI | 150 ohm ± 5% | VCCP | Place the pull-up near CPU |
| TMS | 39 ohm ± 1% | VCCP | Within 200ps of ITP connector |
| TRST# | 500 to 680 ohm ± 5% | GND | Place the pull-down near CPU |
| TCK | 27 ohm ± 1% | GND | Connect to TCK pin of CPU and then connect it to FBO pin of ITP connector in daisy chain. Place the pull-down near TCK0 pin of ITP connector |
| TDO | 51 ohm ± 5% | VCCP | Place the pull-up near ITP |
| RESET# | 22.6 ohm ± 1% series resistor and pullup 51 ohm ± 1%. | VCCP | Connect to CPURST# pin of GMCH through the series resistor placed within 200ps of ITP connector. Place the pull-up after the series resistor from ITP connector. |

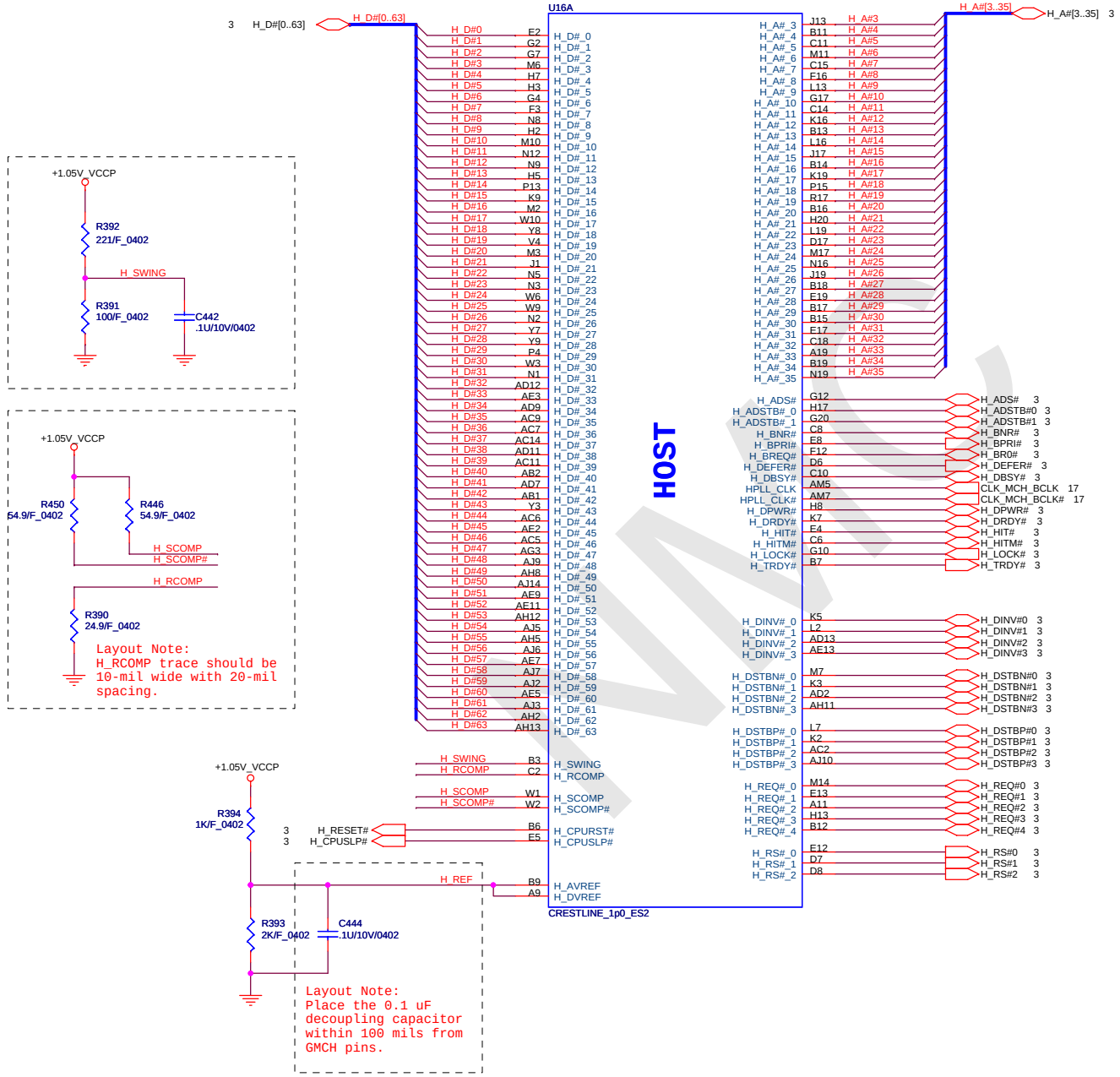
QUANTA COMPUTER

| | | |
|---|---|---|
| Title | Merom Processor (HOST BUS) | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 3 of 60 | |

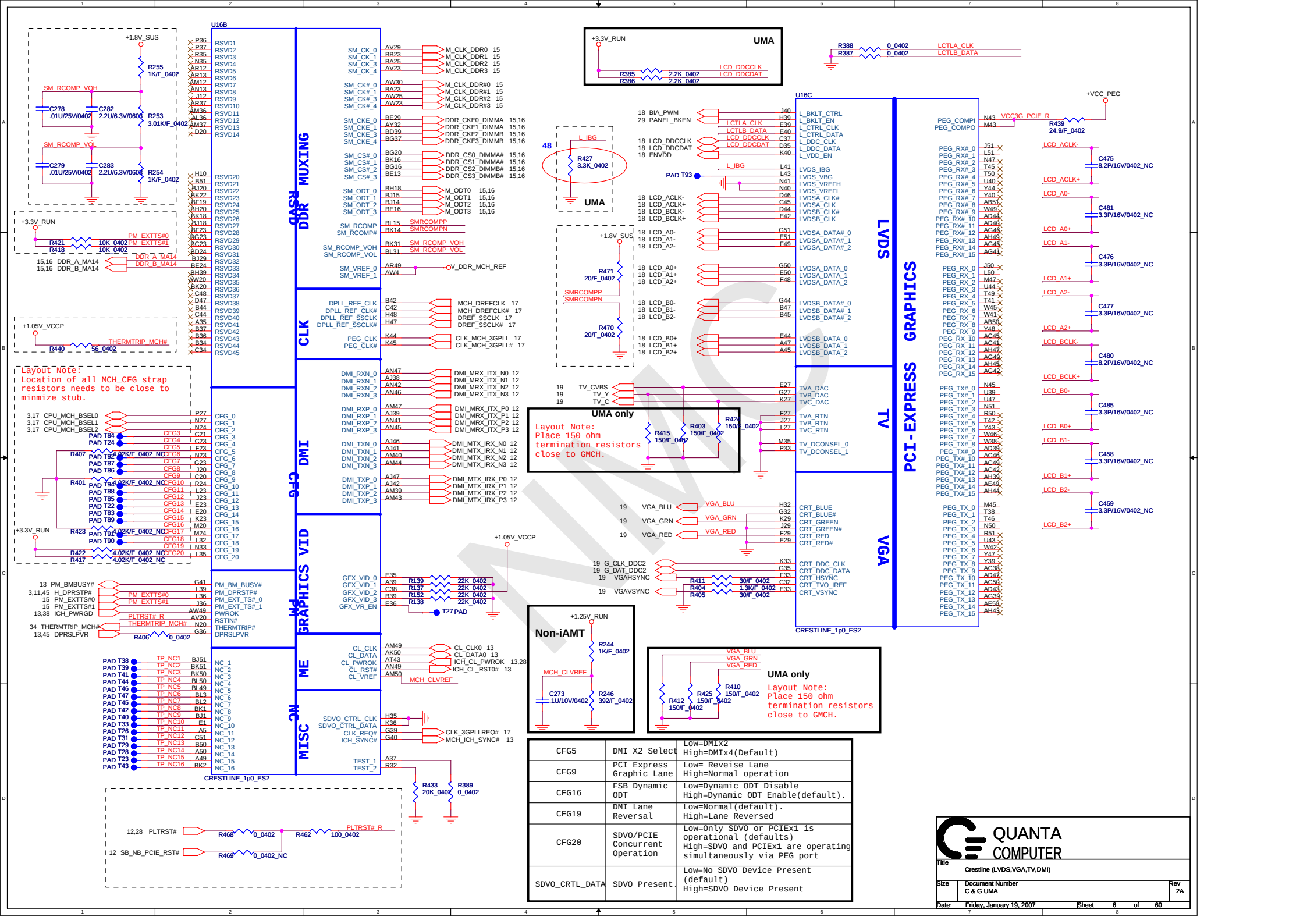



QUANTA COMPUTER

| | | |
|---|---|---|
| Title | Merom Processor (POWER) | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 4 of 60 | |



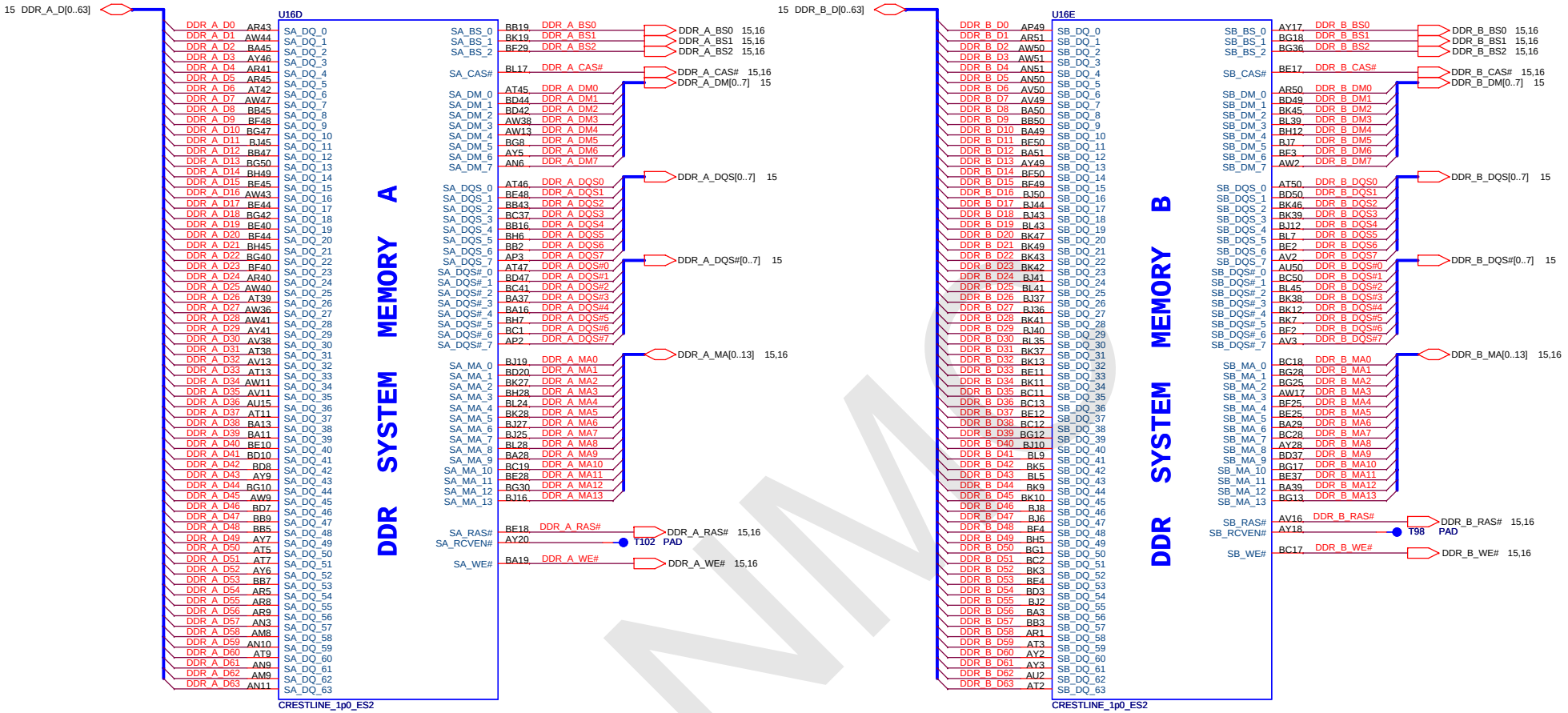

| | | |
|---|---|---|
| QUANTA COMPUTER | | |
| Title | Crestline (HOST) | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 5 of 60 | |




| | | |
|---|---|---|
| CFG5 | DMI X2 Select | Low=DMIx2<br>High=DMIx4(Default) |
| CFG9 | PCI Express Graphic Lane | Low= Reveise Lane<br>High=Normal operation |
| CFG16 | FSB Dynamic ODT | Low=Dynamic ODT Disable<br>High=Dynamic ODT Enable(default). |
| CFG19 | DMI Lane Reversal | Low=Normal(default).<br>High=Lane Reversed |
| CFG20 | SDVO/PCIE Concurrent Operation | Low=Only SDVO or PCIEx1 is operational (defaults)<br>High=SDVO and PCIEx1 are operating simultaneously via PEG port |
| SDVO_CRTL_DATA | SDVO Present | Low=No SDVO Device Present (default)<br>High=SDVO Device Present |

QUANTA COMPUTER

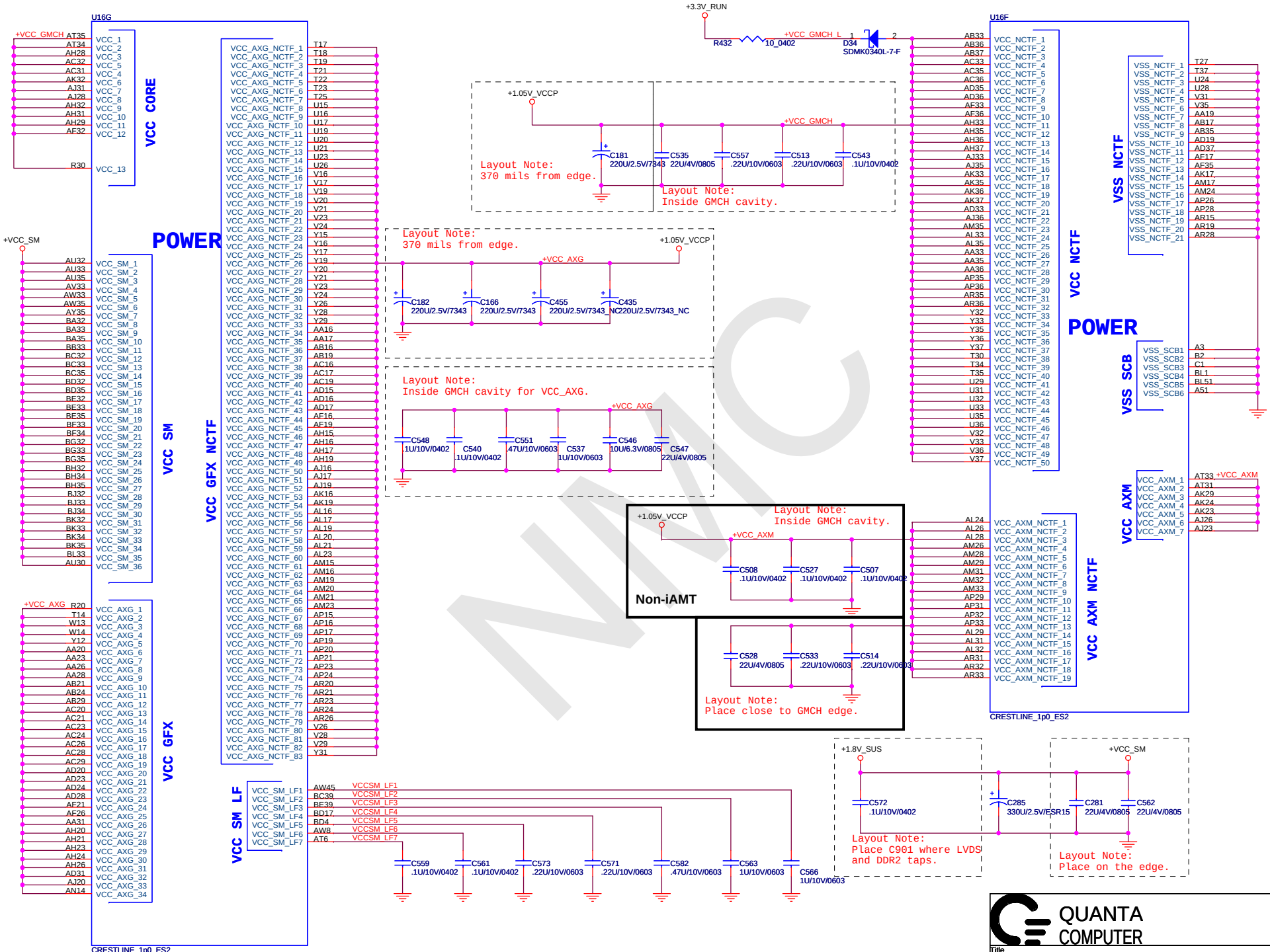
| | | |
|---|---|---|
| Title | Crestline (LVDS,VGA,TV,DMI) | |
| Size | Document Number<br>C & G UMA | Rev<br>2A |
| Date: Friday, January 19, 2007 | Sheet 6 of 60 | |

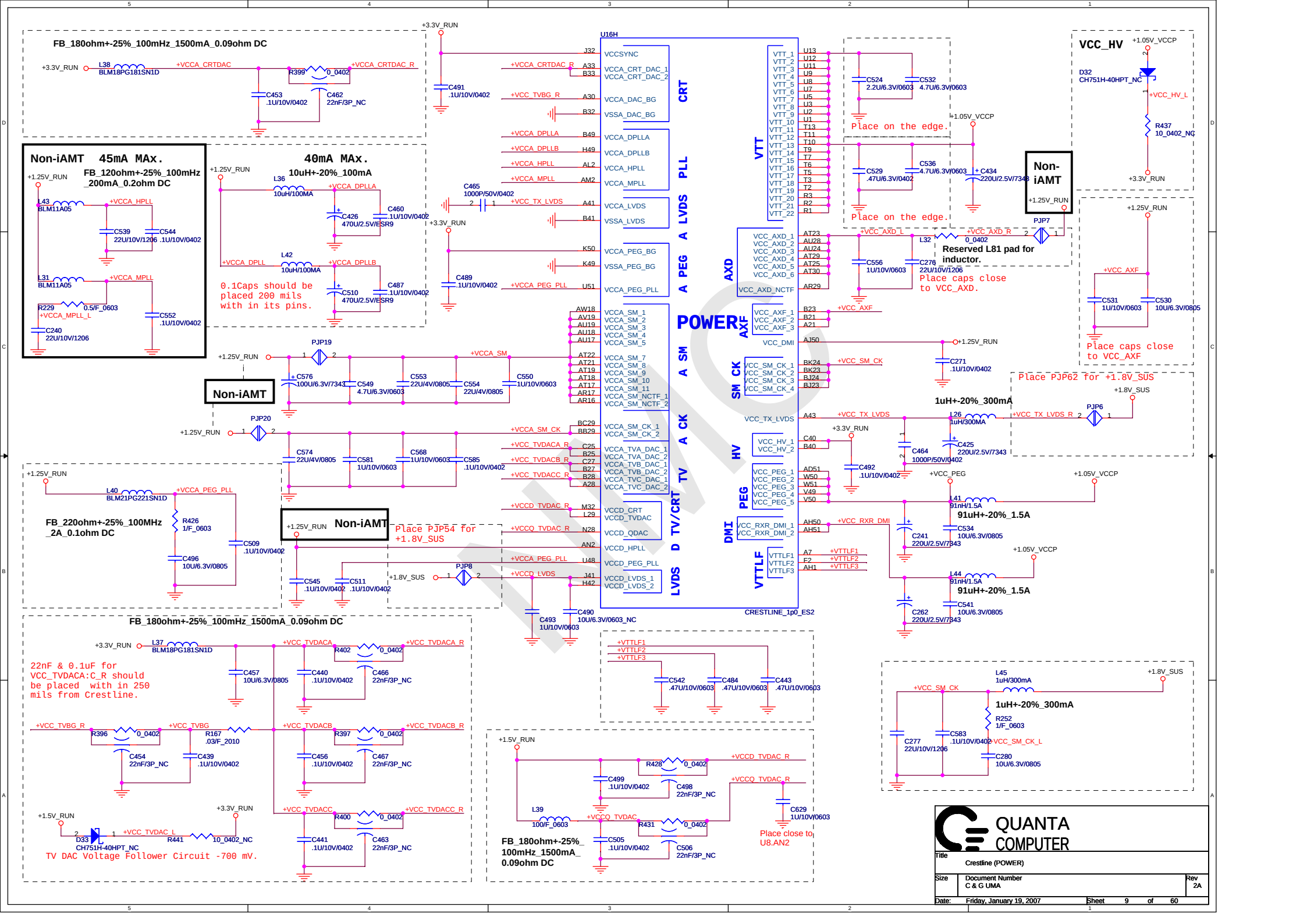


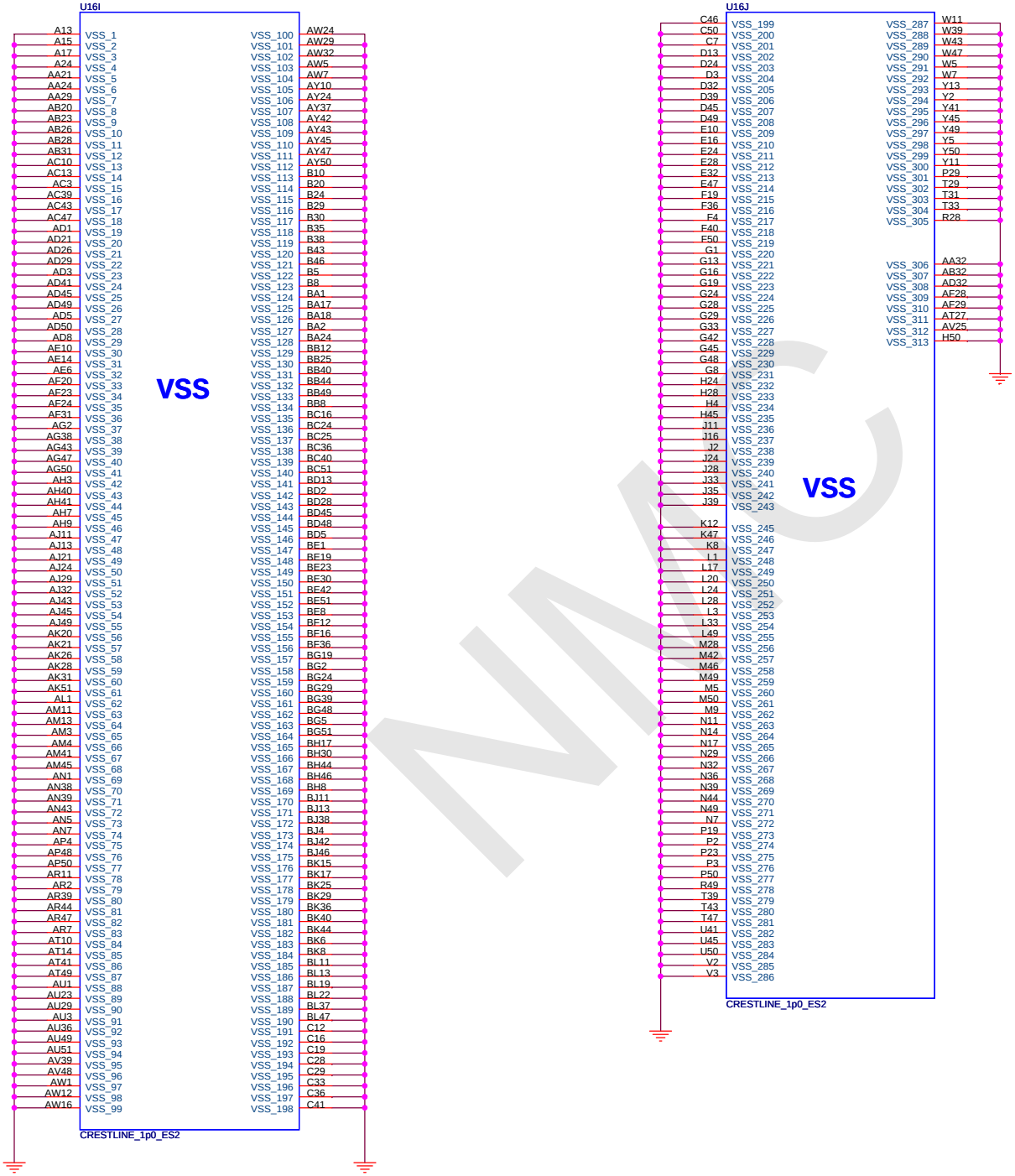



QUANTA COMPUTER

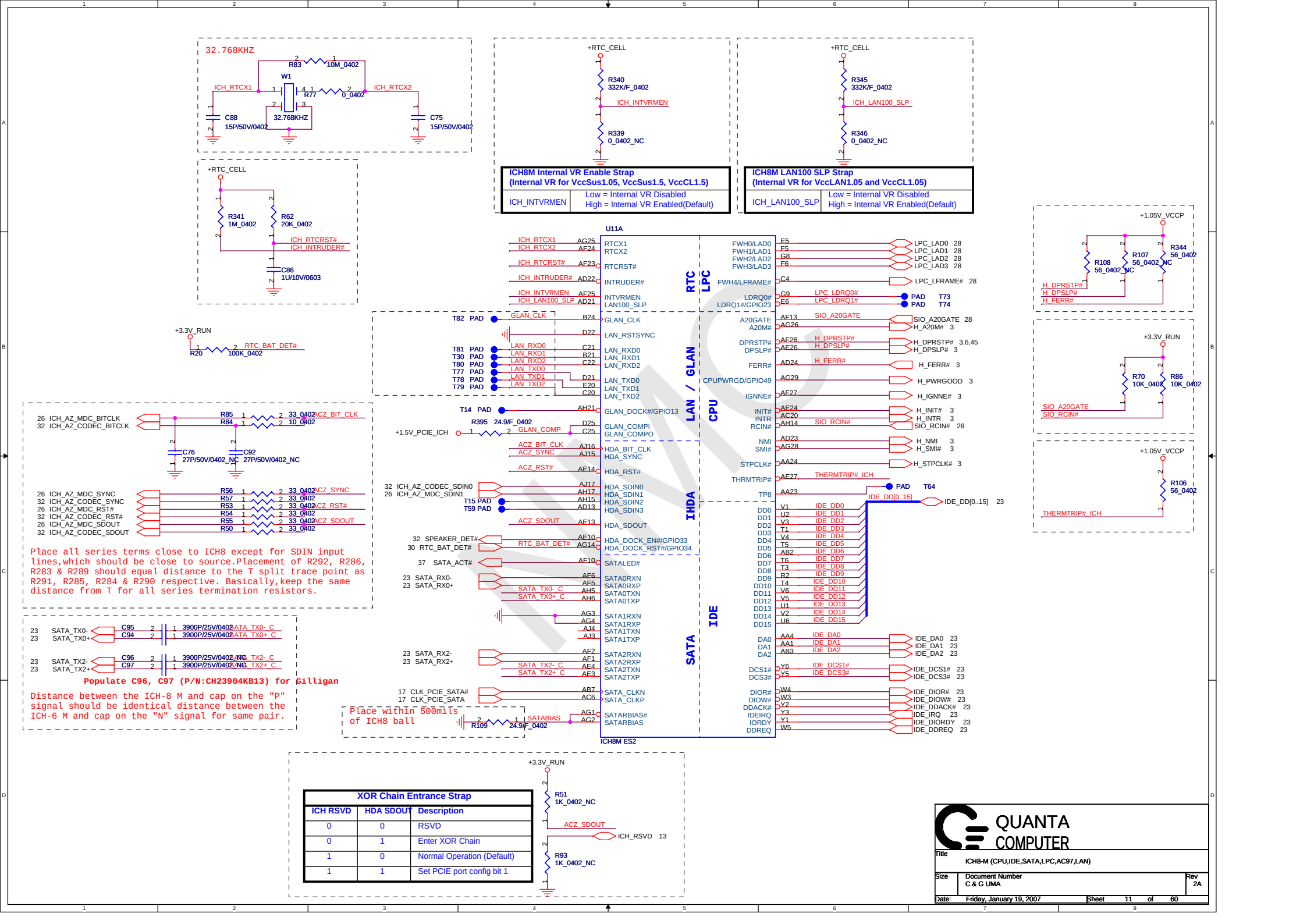
| | | |
|---|---|---|
| Title | Crestline (DDR2) | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 7 of 60 | |


U16G
VCC CORE
VCC GFX NCTF
VCC SM
VCC GFX
VCC SM LF
POWER
CRESTLINE_1p0_ES2
U16F
VCC NCTF
VSS NCTF
VSS SCB
VCC AXM
VCC AXM NCTF
POWER
CRESTLINE_1p0_ES2
+3.3V_RUN
R432
10_0402
+VCC_GMCH_L
D34
SDMK0340L-7-F
+1.05V_VCCP
+VCC_GMCH
C181 220U/2.5V/7343
C535 22U/4V/0805
C557 .22U/10V/0603
C513 .22U/10V/0603
C543 .1U/10V/0402
Layout Note:
370 mils from edge.
Layout Note:
Inside GMCH cavity.
+VCC_SM
+VCC_AXG
+VCC_AXM
+1.8V_SUS
Layout Note:
370 mils from edge.
C182 220U/2.5V/7343
C166 220U/2.5V/7343
C455 220U/2.5V/7343_NC
C435 220U/2.5V/7343_NC
Layout Note:
Inside GMCH cavity for VCC_AXG.
C548 .1U/10V/0402
C540 .1U/10V/0402
C551 .47U/10V/0603
C537 1U/10V/0603
C546 10U/6.3V/0805
C547 22U/4V/0805
Layout Note:
Inside GMCH cavity.
C508 .1U/10V/0402
C527 .1U/10V/0402
C507 .1U/10V/0402
Non-iAMT
C528 22U/4V/0805
C533 .22U/10V/0603
C514 .22U/10V/0603
Layout Note:
Place close to GMCH edge.
C559 .1U/10V/0402
C561 .1U/10V/0402
C573 .22U/10V/0603
C571 .22U/10V/0603
C582 .47U/10V/0603
C563 1U/10V/0603
C566 1U/10V/0603
C572 .1U/10V/0402
C285 330U/2.5V/ESR15
C281 22U/4V/0805
C562 22U/4V/0805
Layout Note:
Place C901 where LVDS
and DDR2 taps.
Layout Note:
Place on the edge.
QUANTA COMPUTER
Title
Crestline (VCC,NCTF)
Size
Document Number
C & G UMA
Rev
2A
Date:
Friday, January 19, 2007
Sheet
8
of
60


FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC
Non-iAMT 45mA MAx.
FB_120ohm+-25%_100mHz_200mA_0.2ohm DC
40mA MAx.
10uH+-20%_100mA
0.1Caps should be placed 200 mils with in its pins.
Non-iAMT
Non-iAMT
Non-iAMT
FB_220ohm+-25%_100MHz_2A_0.1ohm DC
Place PJP54 for +1.8V_SUS
FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC
22nF & 0.1uF for VCC_TVDACA:C_R should be placed with in 250 mils from Crestline.
TV DAC Voltage Follower Circuit -700 mV.
FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC
Place close to U8.AN2
U16H
CRESTLINE_1p0_ES2
POWER
CRT
PLL
LVDS
PEG
AXD
AXF
SM CK
HV
DMI
TV/CRT
VTT
VTTLF
Place on the edge.
Place on the edge.
Reserved L81 pad for inductor.
Place caps close to VCC_AXD.
Place caps close to VCC_AXF
Place PJP62 for +1.8V_SUS
1uH+-20%_300mA
91uH+-20%_1.5A
1uH+-20%_300mA
VCC_HV
Non-iAMT
QUANTA COMPUTER
Title: Crestline (POWER)
Size: Document Number C & G UMA
Rev: 2A
Date: Friday, January 19, 2007
Sheet 9 of 60




| | |
|---|---|
| Title | Crestline (VSS) |
| Size | Document Number: C & G UMA |
| Rev | 2A |
| Date: | Friday, January 19, 2007 |
| Sheet | 10 of 60 |


32.768KHZ
R83 10M_0402
W1
ICH_RTCX1
R77 0_0402
ICH_RTCX2
C88 15P/50V/0402
32.768KHZ
C75 15P/50V/0402
+RTC_CELL
R341 1M_0402
R62 20K_0402
ICH_RTCRST#
ICH_INTRUDER#
C86 1U/10V/0603
+3.3V_RUN
R20 100K_0402
RTC_BAT_DET#
+RTC_CELL
R340 332K/F_0402
ICH_INTVRMEN
R339 0_0402_NC
ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)
ICH_INTVRMEN
Low = Internal VR Disabled
High = Internal VR Enabled(Default)
+RTC_CELL
R345 332K/F_0402
ICH_LAN100_SLP
R346 0_0402_NC
ICH8M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)
ICH_LAN100_SLP
Low = Internal VR Disabled
High = Internal VR Enabled(Default)
U11A
RTC
LPC
LAN / GLAN
CPU
IHDA
IDE
SATA
ICH8M ES2
+1.05V_VCCP
R344 56_0402
R108 56_0402_NC
R107 56_0402_NC
H_DPRSTP#
H_DPSLP#
H_FERR#
+3.3V_RUN
R70 10K_0402
R86 10K_0402
SIO_A20GATE
SIO_RCIN#
+1.05V_VCCP
R106 56_0402
THERMTRIP#_ICH
26 ICH_AZ_MDC_BITCLK
32 ICH_AZ_CODEC_BITCLK
R85 33_0402
R84 10_0402
C76 27P/50V/0402_NC
C92 27P/50V/0402_NC
ACZ_BIT_CLK
26 ICH_AZ_MDC_SYNC
32 ICH_AZ_CODEC_SYNC
26 ICH_AZ_MDC_RST#
32 ICH_AZ_CODEC_RST#
26 ICH_AZ_MDC_SDOUT
32 ICH_AZ_CODEC_SDOUT
R56 33_0402
R57 33_0402
R53 33_0402
R54 33_0402
R55 33_0402
R50 33_0402
ACZ_SYNC
ACZ_RST#
ACZ_SDOUT
Place all series terms close to ICH8 except for SDIN input lines,which should be close to source.Placement of R292, R286, R283 & R289 should equal distance to the T split trace point as R291, R285, R284 & R290 respective. Basically,keep the same distance from T for all series termination resistors.
T82 PAD
T81 PAD
T30 PAD
T80 PAD
T77 PAD
T78 PAD
T79 PAD
T14 PAD
R395 24.9/F_0402
+1.5V_PCIE_ICH
GLAN_COMP
T15 PAD
T59 PAD
32 SPEAKER_DET#
30 RTC_BAT_DET#
37 SATA_ACT#
23 SATA_RX0-
23 SATA_RX0+
SATA_TX0- C
SATA_TX0+ C
23 SATA_TX0-
23 SATA_TX0+
C95 3900P/25V/0402
C94 3900P/25V/0402
23 SATA_TX2-
23 SATA_TX2+
C96 3900P/25V/0402_NC
C97 3900P/25V/0402_NC
Populate C96, C97 (P/N:CH23904KB13) for Gilligan
Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.
23 SATA_RX2-
23 SATA_RX2+
SATA_TX2- C
SATA_TX2+ C
17 CLK_PCIE_SATA#
17 CLK_PCIE_SATA
Place within 500mils of ICH8 ball
R109 24.9/F_0402
SATABIAS
T73 PAD
T74 PAD
T64 PAD
IDE_DD[0..15]
IDE_DD[0..15] 23
SIO_A20GATE 28
H_A20M# 3
H_DPRSTP# 3,6,45
H_DPSLP# 3
H_FERR# 3
H_PWRGOOD 3
H_IGNNE# 3
H_INIT# 3
H_INTR 3
SIO_RCIN# 28
H_NMI 3
H_SMI# 3
H_STPCLK# 3
THERMTRIP# ICH
IDE_DA0 23
IDE_DA1 23
IDE_DA2 23
IDE_DCS1# 23
IDE_DCS3# 23
IDE_DIOR# 23
IDE_DIOW# 23
IDE_DDACK# 23
IDE_IRQ 23
IDE_DIORDY 23
IDE_DDREQ 23
XOR Chain Entrance Strap
ICH RSVD | HDA SDOUT | Description
0 | 0 | RSVD
0 | 1 | Enter XOR Chain
1 | 0 | Normal Operation (Default)
1 | 1 | Set PCIE port config bit 1
+3.3V_RUN
R51 1K_0402_NC
ACZ_SDOUT
ICH_RSVD 13
R93 1K_0402_NC
QUANTA COMPUTER
Title
ICH8-M (CPU,IDE,SATA,LPC,AC97,LAN)
Size
Document Number
C & G UMA
Rev
2A
Date: Friday, January 19, 2007
Sheet 11 of 60

Place TX DC blocking caps close ICH8.

25 PCIE_TX1- C162 1 2 .1U/10V/0402 PCIE_TXN1_C
25 PCIE_TX1+ C165 1 2 .1U/10V/0402 PCIE_TXP1_C

24 PCIE_TX2- C172 1 2 .1U/10V/0402 PCIE_TXN2_C
24 PCIE_TX2+ C169 1 2 .1U/10V/0402 PCIE_TXP2_C

24 PCIE_TX3- C179 1 2 .1U/10V/0402 PCIE_TXN3_C
24 PCIE_TX3+ C174 1 2 .1U/10V/0402 PCIE_TXP3_C

26 PCIE_TX4- C188 1 2 .1U/10V/0402 PCIE_TXN4_C
26 PCIE_TX4+ C184 1 2 .1U/10V/0402 PCIE_TXP4_C

U11D

25 PCIE_RX1- PERN1 P27
25 PCIE_RX1+ PERP1 P26
PCIE_TXN1_C PETN1 N29
PCIE_TXP1_C PETP1 N28
WWAN

24 PCIE_RX2- PERN2 M27
24 PCIE_RX2+ PERP2 M26
PCIE_TXN2_C PETN2 L29
PCIE_TXP2_C PETP2 L28
WLAN

24 PCIE_RX3- PERN3 K27
24 PCIE_RX3+ PERP3 K26
PCIE_TXN3_C PETN3 J29
PCIE_TXP3_C PETP3 J28
WPAN

26 PCIE_RX4- PERN4 H27
26 PCIE_RX4+ PERP4 H26
PCIE_TXN4_C PETN4 G29
PCIE_TXP4_C PETP4 G28
Express Card

PERN5 F27
PERP5 E26
PETN5 E29
PETP5 E28

PERN6/GLAN_RXN D27
PERP6/GLAN_RXP D26
PETN6/GLAN_TXN C29
PETP6/GLAN_TXP C28

PCI-Express Direct Media Interface

DMI0RXN V27 DMI_MTX_IRX_N0 6
DMI0RXP V26 DMI_MTX_IRX_P0 6
DMI0TXN U29 DMI_MRX_ITX_N0 6
DMI0TXP U28 DMI_MRX_ITX_P0 6

DMI1RXN Y27 DMI_MTX_IRX_N1 6
DMI1RXP Y26 DMI_MTX_IRX_P1 6
DMI1TXN W29 DMI_MRX_ITX_N1 6
DMI1TXP W28 DMI_MRX_ITX_P1 6

DMI2RXN AB26 DMI_MTX_IRX_N2 6
DMI2RXP AB25 DMI_MTX_IRX_P2 6
DMI2TXN AA29 DMI_MRX_ITX_N2 6
DMI2TXP AA28 DMI_MRX_ITX_P2 6

DMI3RXN AD27 DMI_MTX_IRX_N3 6
DMI3RXP AD26 DMI_MTX_IRX_P3 6
DMI3TXN AC29 DMI_MRX_ITX_N3 6
DMI3TXP AC28 DMI_MRX_ITX_P3 6

DMI_CLKN T26 CLK_PCIE_ICH# 17
DMI_CLKP T25 CLK_PCIE_ICH 17

DMI_ZCOMP Y23
DMI_IRCOMP Y24 DMI_COMP
R350 2 1 24.9/F_0402 +1.5V_PCIE_ICH

Place within 500mils of ICH8

ICH_USBP5- C652 2 12pF/50V/0402_NC 1 ICH_USBP5+

USB[1B]
USB[1A]
USB[2B]
USB[2A]
3rd Mini Card
CAMERA
Express Card
Blue tooth
USB[3]
WWAN

USBP0N G3 ICH_USBP0- 27
USBP0P G2 ICH_USBP0+ 27
USBP1N H5 ICH_USBP1- 27
USBP1P H4 ICH_USBP1+ 27
USBP2N H2 ICH_USBP2- 27
USBP2P H1 ICH_USBP2+ 27
USBP3N J3 ICH_USBP3- 27
USBP3P J2 ICH_USBP3+ 27
USBP4N K5 ICH_USBP4- 24
USBP4P K4 ICH_USBP4+ 24
USBP5N K2 ICH_USBP5- 33
USBP5P K1 ICH_USBP5+ 33
USBP6N L3 ICH_USBP6- 26
USBP6P L2 ICH_USBP6+ 26
USBP7N M5 ICH_USBP7- 37
USBP7P M4 ICH_USBP7+ 37
USBP8N M2 ICH_USBP8- 27
USBP8P M1 ICH_USBP8+ 27
USBP9N N3 ICH_USBP9- 25
USBP9P N2 ICH_USBP9+ 25

USB

USBRBIAS# F2
USBRBIAS F3 USBRBIAS
R174 2 22.6/F_0402 1

ICH8M ES2

Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

Layout Note:
Place R288,R688 and R282 within 500 mils from ICH.

28 ICH_EC_SPI_CLK R408 1 2 15_0402 ICH_EC_SPI_CLK_R C23 SPI_CLK
ICH_SPI_CS# B23 SPI_CS0#
ICH_SPI_CS1#_R E22 SPI_CS1#
28 ICH_EC_SPI_DO R409 1 2 15_0402 ICH_EC_SPI_DO_R D23 SPI_MOSI
28 ICH_EC_SPI_DIN F21 SPI_MISO

SPI

+3.3V_ALW
U30
SPI_CS0# R434 15_0402_NC R435 0_0402 7SH08_NC R436 15_0402 ICH_SPI_CS#
SIO_SPI_CS# 28

27 USB_OC0_1# USB_OC0_1# AJ19 OC0#
27 USB_OC2_3# USB_OC2_3# AG16 OC1#/GPIO40
AG15 OC2#/GPIO41
AE15 OC3#/GPIO42
25 OC4# AE15 OC4#/GPIO43
OC5# AG17 OC5#/GPIO29
OC6# AD12 OC6#/GPIO30
27 USB_OC8# USB_OC8# AD14 OC7#/GPIO31
OC9# AH18 OC8#
OC9#

Non-iAMT
35 OC4# R569 2 10K_0402 1 +3.3V_SUS
OC7# OC9# OC5# OC6# RP35 10P8R-10K USB_OC0_1# USB_OC2_3# USB_OC8#
25

35 C661 .1U/10V/0402_NC USB_OC0_1#
C662 .1U/10V/0402_NC USB_OC2_3#
25 C663 .1U/10V/0402_NC USB_OC8#
C664 .1U/10V/0402_NC OC5#
C665 .1U/10V/0402_NC OC6#
C666 .1U/10V/0402_NC OC7#
C667 .1U/10V/0402_NC OC9#

ICH_SPI_CS1#_R
PCI_GNT0#
R201 2 1K_0402 1
R379 1 1K_0402_NC 2

| Boot BIOS Strap | | | |
|---|---|---|---|
| | | GNT0# | SPI_CS1# |
| LPC | 11 | No stuff | No stuff |
| PCI | 10 | No stuff | Stuff |
| SPI | 01 | Stuff | No stuff |

PCI Pullups

+3.3V_RUN
RP19 10P8R-8.2K
PCI_FRAME# PCI_DEVSEL# PCI_REQ1#
RP20 10P8R-8.2K
SB_WLAN_PCIE_RST# SB_NB_PCIE_RST# PCI_PIRQD#
PCI_STOP# PCI_SERR# SB_MCARD3_PCIE_RST# PCI_TRDY#
29
RP21 10P8R-8.2K
PCI_REQ0# PCI_PLOCK# PCI_PERR#
PCI_PIRQC# PCI_PIRQB# PCI_PIRQA# PCI_IRDY#

20,35 PCI_AD[0..31]

U11B

PCI

| | | | |
|---|---|---|---|
| PCI_AD0 | D20 | AD0 | |
| PCI_AD1 | E19 | AD1 | |
| PCI_AD2 | D19 | AD2 | |
| PCI_AD3 | A20 | AD3 | |
| PCI_AD4 | D17 | AD4 | |
| PCI_AD5 | A21 | AD5 | |
| PCI_AD6 | A19 | AD6 | |
| PCI_AD7 | C19 | AD7 | |
| PCI_AD8 | A18 | AD8 | |
| PCI_AD9 | B16 | AD9 | |
| PCI_AD10 | A12 | AD10 | |
| PCI_AD11 | E16 | AD11 | |
| PCI_AD12 | A14 | AD12 | |
| PCI_AD13 | G16 | AD13 | |
| PCI_AD14 | A15 | AD14 | |
| PCI_AD15 | B6 | AD15 | |
| PCI_AD16 | C11 | AD16 | |
| PCI_AD17 | A9 | AD17 | |
| PCI_AD18 | D11 | AD18 | |
| PCI_AD19 | B12 | AD19 | |
| PCI_AD20 | C12 | AD20 | |
| PCI_AD21 | D10 | AD21 | |
| PCI_AD22 | C7 | AD22 | |
| PCI_AD23 | F13 | AD23 | |
| PCI_AD24 | E11 | AD24 | |
| PCI_AD25 | E13 | AD25 | |
| PCI_AD26 | E12 | AD26 | |
| PCI_AD27 | D8 | AD27 | |
| PCI_AD28 | A6 | AD28 | |
| PCI_AD29 | E8 | AD29 | |
| PCI_AD30 | D6 | AD30 | |
| PCI_AD31 | A3 | AD31 | |

REQ0# A4 PCI_REQ0# PCI_REQ0# 35
GNT0# D7 PCI_GNT0# PCI_GNT0# 35
REQ1#/GPIO50 E18 PCI_REQ1# PCI_REQ1# 20
GNT1#/GPIO51 C18 PCI_GNT1# PCI_GNT1# 20
REQ2#/GPIO52 B19 SB_WWAN_PCIE_RST# SB_WWAN_PCIE_RST# 25
GNT2#/GPIO53 F18
REQ3#/GPIO54 A11 SB_LOM_PCIE_RST#
GNT3#/GPIO55 C10

C/BE0# C17 PCI_C_BE0# 20,35
C/BE1# E15 PCI_C_BE1# 20,35
C/BE2# E16 PCI_C_BE2# 20,35
C/BE3# E17 PCI_C_BE3# 20,35

IRDY# C8 PCI_IRDY# PCI_IRDY# 20,35
PAR D9 PCI_PAR 20,35
PCIRST# G6 PCI_RST# G
DEVSEL# D16 PCI_DEVSEL# PCI_DEVSEL# 20,35
PERR# A7 PCI_PERR# PCI_PERR# 20,35
PLOCK# B7 PCI_PLOCK# PCI_PLOCK#
SERR# E10 PCI_SERR# PCI_SERR# 20,35
STOP# C16 PCI_STOP# PCI_STOP# 20,35
TRDY# C9 PCI_TRDY# PCI_TRDY# 20,35
FRAME# A17 PCI_FRAME# PCI_FRAME# 20,35

PLTRST# AG24 PCI_PLTRST#
PCICLK B10 CLK_PCI_ICH CLK_PCI_ICH 17
PME# G7 ICH_PME# 29

SB_NB_PCIE_RST#
R209 2 1K_0402_NC 1

| A16 away override strap. | |
|---|---|
| PCI_GNT3# | Low = A16 swap override enabled.<br>High = Default. |

Interrupt I/F

PCI_PIRQA# F9 PIRQA# PIRQE#/GPIO2 E8 SB_MCARD3_PCIE_RST# SB_MCARD3_PCIE_RST# 24
PCI_PIRQB# B5 PIRQB# PIRQF#/GPIO3 G11 SB_WLAN_PCIE_RST# SB_WLAN_PCIE_RST# 24
PCI_PIRQC# C5 PIRQC# PIRQG#/GPIO4 F12 SB_NB_PCIE_RST# SB_NB_PCIE_RST# 6
PCI_PIRQD# A10 PIRQD# PIRQH#/GPIO5 B3 PCIE_MCARD2_DET# 25
29

35 PCI_PIRQB#
20 PCI_PIRQC#
20 PCI_PIRQD#

PCI_PIRQB: for LOM
PCI_PIRQC: for Media Card
PCI_PIRQD: for 1394

ICH8M ES2

| LOM | REQ0 | GNT0 | PIRQB |
|---|---|---|---|
| Card reader with 1394 | REQ1 | GNT1 | PIRQC<br>PIRQD |

SB_LOM_PCIE_RST# R207 2 1 20K_0402_NC
SB_WWAN_PCIE_RST# R202 2 1 20K_0402
SB_WLAN_PCIE_RST# R372 2 1 20K_0402_NC
SB_MCARD3_PCIE_RST# R203 2 1 20K_0402
SB_NB_PCIE_RST# R208 2 1 20K_0402_NC

BIOS should not enable the internal GPIO pull up resistor.

CLK_PCI_ICH
39 R200 2 33_0402 1
C220 2 9P/50V/0402 1

Reserved for EMI. Place resister and cap close to ICH.

Non-iAMT

Add Buffers as needed for Loading and fanout concerns.

+3.3V_SUS
C153 .047U/10V/0402
U12 TC7SZ32FU
PCI_RST# G PCI_RST# 20,35

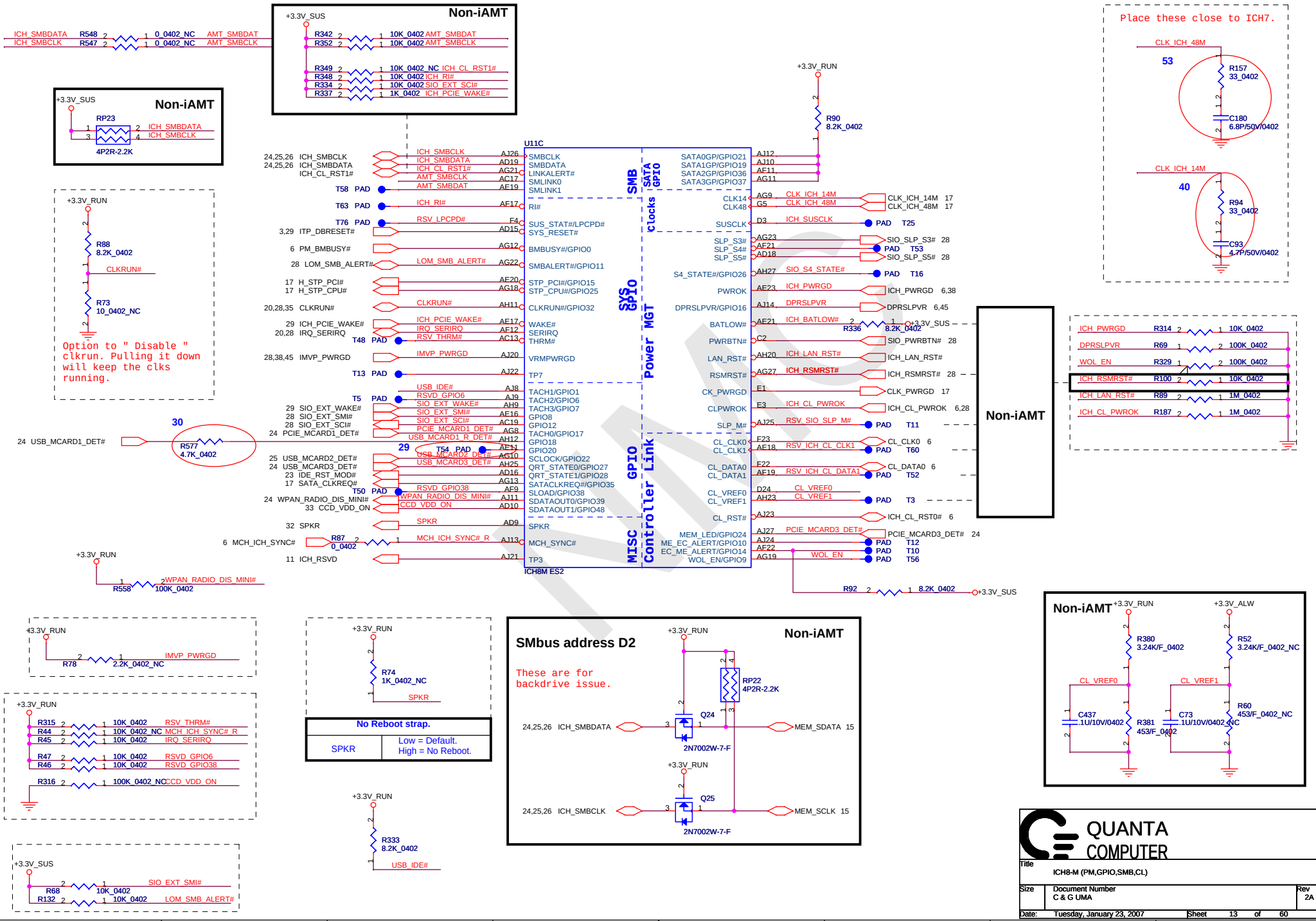
C115 .047U/10V/0402
U6 TC7SZ32FU
PCI_PLTRST# PLTRST1# 24,25,26

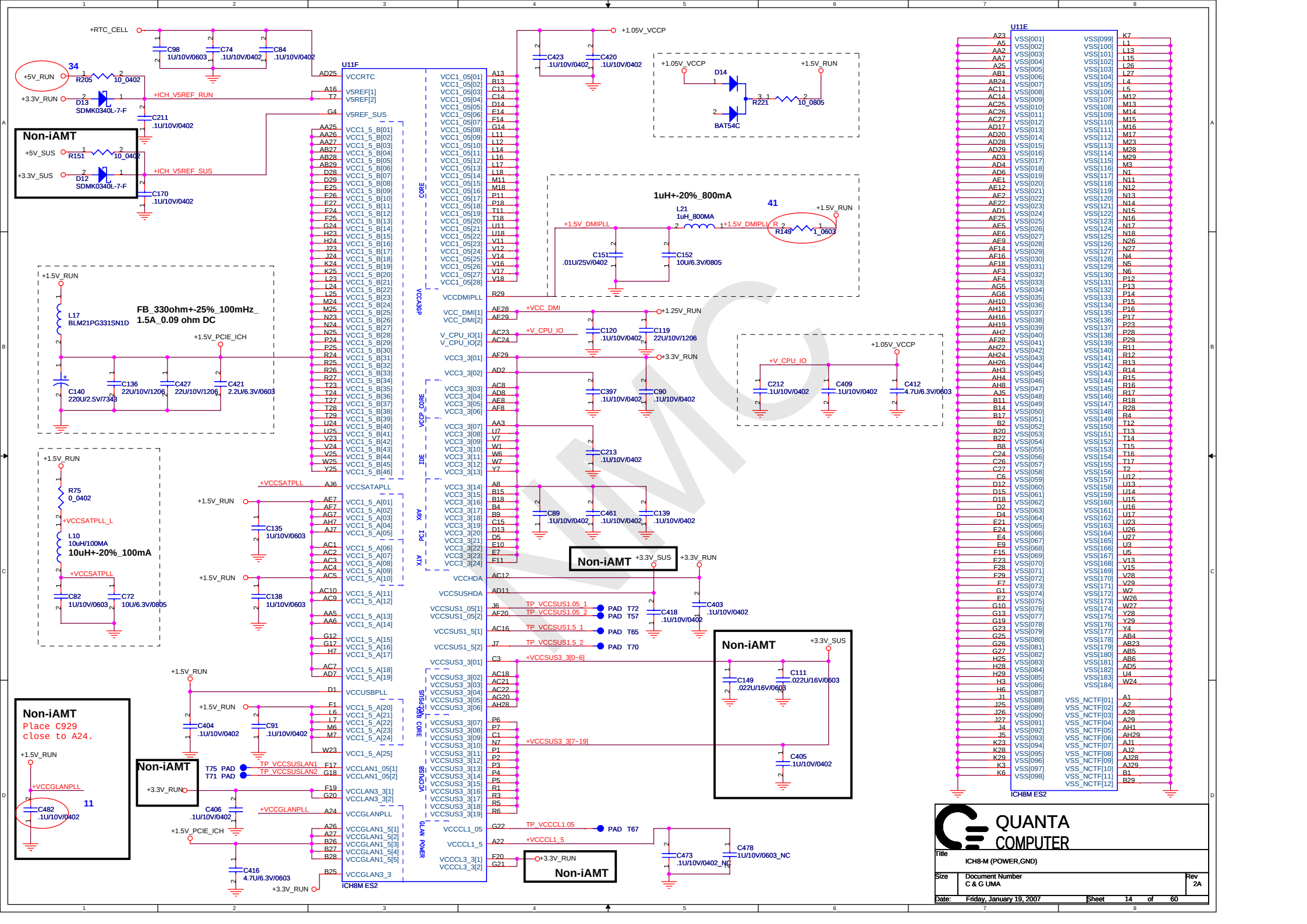
C128 .047U/10V/0402
U9 TC7SZ32FU
PCI_PLTRST# PLTRST# 6,28

PLTRST1# for WWAN/WLAN/WPAN/Express card
PLTRST# for MCH/SIO

QUANTA COMPUTER

| | | |
|---|---|---|
| Title | ICH8-M (USB,DMI,PCIE,PCI) | |
| Size | Document Number<br>C & G UMA | Rev<br>2A |
| Date: Friday, January 19, 2007 | Sheet 12 of 60 | |


Non-iAMT
Place these close to ICH7.
CLK_ICH_48M
53
R157 33_0402
C180 6.8P/50V/0402
CLK_ICH_14M
40
R94 33_0402
C93 4.7P/50V/0402
U11C
ICH8M ES2
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SMBus address D2
These are for backdrive issue.
Q24
Q25
2N7002W-7-F
RP22 4P2R-2.2K
No Reboot strap.
SPKR
Low = Default.
High = No Reboot.
Option to " Disable " clkrun. Pulling it down will keep the clks running.
QUANTA COMPUTER
Title
ICH8-M (PM,GPIO,SMB,CL)
Size
Document Number
C & G UMA
Rev
2A
Date: Tuesday, January 23, 2007
Sheet 13 of 60


+RTC_CELL
C98 1U/10V/0603
C74 .1U/10V/0402
C84 .1U/10V/0402
34
+5V_RUN
R205 10_0402
+3.3V_RUN
D13 SDMK0340L-7-F
+ICH_V5REF_RUN
C211 .1U/10V/0402
Non-iAMT
+5V_SUS
R151 10_0402
+3.3V_SUS
D12 SDMK0340L-7-F
+ICH_V5REF_SUS
C170 .1U/10V/0402
U11F
VCCRTC
V5REF[1]
V5REF[2]
V5REF_SUS
VCC1_5_B[01]
VCC1_5_B[02]
VCC1_5_B[03]
VCC1_5_B[04]
VCC1_5_B[05]
VCC1_5_B[06]
VCC1_5_B[07]
VCC1_5_B[08]
VCC1_5_B[09]
VCC1_5_B[10]
VCC1_5_B[11]
VCC1_5_B[12]
VCC1_5_B[13]
VCC1_5_B[14]
VCC1_5_B[15]
VCC1_5_B[16]
VCC1_5_B[17]
VCC1_5_B[18]
VCC1_5_B[19]
VCC1_5_B[20]
VCC1_5_B[21]
VCC1_5_B[22]
VCC1_5_B[23]
VCC1_5_B[24]
VCC1_5_B[25]
VCC1_5_B[26]
VCC1_5_B[27]
VCC1_5_B[28]
VCC1_5_B[29]
VCC1_5_B[30]
VCC1_5_B[31]
VCC1_5_B[32]
VCC1_5_B[33]
VCC1_5_B[34]
VCC1_5_B[35]
VCC1_5_B[36]
VCC1_5_B[37]
VCC1_5_B[38]
VCC1_5_B[39]
VCC1_5_B[40]
VCC1_5_B[41]
VCC1_5_B[42]
VCC1_5_B[43]
VCC1_5_B[44]
VCC1_5_B[45]
VCC1_5_B[46]
CORE
VCCP
VCCDMIPLL
VCC_DMI[1]
VCC_DMI[2]
V_CPU_IO[1]
V_CPU_IO[2]
VCC3_3[01]
VCC3_3[02]
VCC3_3[03]
VCC3_3[04]
VCC3_3[05]
VCC3_3[06]
VCC3_3[07]
VCC3_3[08]
VCC3_3[09]
VCC3_3[10]
VCC3_3[11]
VCC3_3[12]
VCC3_3[13]
VCC3_3[14]
VCC3_3[15]
VCC3_3[16]
VCC3_3[17]
VCC3_3[18]
VCC3_3[19]
VCC3_3[20]
VCC3_3[21]
VCC3_3[22]
VCC3_3[23]
VCC3_3[24]
VCCHDA
VCCSUSHDA
VCCSUS1_05[1]
VCCSUS1_05[2]
VCCSUS1_5[1]
VCCSUS1_5[2]
VCCSUS3_3[01]
VCCSUS3_3[02]
VCCSUS3_3[03]
VCCSUS3_3[04]
VCCSUS3_3[05]
VCCSUS3_3[06]
VCCSUS3_3[07]
VCCSUS3_3[08]
VCCSUS3_3[09]
VCCSUS3_3[10]
VCCSUS3_3[11]
VCCSUS3_3[12]
VCCSUS3_3[13]
VCCSUS3_3[14]
VCCSUS3_3[15]
VCCSUS3_3[16]
VCCSUS3_3[17]
VCCSUS3_3[18]
VCCSUS3_3[19]
VCCCL1_05
VCCCL1_5
VCCCL3_3[1]
VCCCL3_3[2]
VCCSUS3_3
SUS CORE
VCCPUSB
PLAN POWER
ICH8M ES2
C423 .1U/10V/0402
C420 .1U/10V/0402
+1.05V_VCCP
D14 BAT54C
+1.5V_RUN
R221 10_0805
1uH+-20%_800mA
41
L21 1uH_800MA
+1.5V_DMIPLL
+1.5V_DMIPLL_R
R149 1_0603
C151 .01U/25V/0402
C152 10U/6.3V/0805
+VCC_DMI
+1.25V_RUN
+V_CPU_IO
C120 .1U/10V/0402
C119 22U/10V/1206
C212 .1U/10V/0402
C409 .1U/10V/0402
C412 4.7U/6.3V/0603
C397 .1U/10V/0402
C90 .1U/10V/0402
C213 .1U/10V/0402
C89 .1U/10V/0402
C461 .1U/10V/0402
C139 .1U/10V/0402
Non-iAMT
+3.3V_SUS
C403 .1U/10V/0402
C418 .1U/10V/0402
TP_VCCSUS1.05_1
TP_VCCSUS1.05_2
PAD T72
PAD T57
TP_VCCSUS1.5_1
PAD T65
TP_VCCSUS1.5_2
PAD T70
+VCCSUS3_3[0~6]
+VCCSUS3_3[7~19]
C149 .022U/16V/0603
C111 .022U/16V/0603
C405 .1U/10V/0402
TP_VCCCL1.05
PAD T67
+VCCCL1_5
C473 .1U/10V/0402_NC
C478 1U/10V/0603_NC
+1.5V_RUN
L17 BLM21PG331SN1D
FB_330ohm+-25%_100mHz_
1.5A_0.09 ohm DC
+1.5V_PCIE_ICH
C140 220U/2.5V/7343
C136 22U/10V/1206
C427 22U/10V/1206
C421 2.2U/6.3V/0603
R75 0_0402
+VCCSATPLL_L
L10 10uH/100MA
10uH+-20%_100mA
+VCCSATPLL
C82 1U/10V/0603
C72 10U/6.3V/0805
C135 1U/10V/0603
C138 1U/10V/0603
C404 .1U/10V/0402
C91 .1U/10V/0402
Non-iAMT
Place C929
close to A24.
+VCCGLANPLL
11
C482 .1U/10V/0402
T75 PAD
T71 PAD
TP_VCCSUSLAN1
TP_VCCSUSLAN2
+3.3V_RUN
C406 .1U/10V/0402
C416 4.7U/6.3V/0603
U11E
VSS[001]
VSS[002]
VSS[003]
VSS[004]
VSS[005]
VSS[006]
VSS[007]
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VSS[009]
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VSS[180]
VSS[181]
VSS[182]
VSS[183]
VSS[184]
VSS_NCTF[01]
VSS_NCTF[02]
VSS_NCTF[03]
VSS_NCTF[04]
VSS_NCTF[05]
VSS_NCTF[06]
VSS_NCTF[07]
VSS_NCTF[08]
VSS_NCTF[09]
VSS_NCTF[10]
VSS_NCTF[11]
VSS_NCTF[12]
ICH8M ES2
QUANTA COMPUTER
Title
ICH8-M (POWER,GND)
Size
Document Number
C & G UMA
Rev
2A
Date:
Friday, January 19, 2007
Sheet
14
of
60

A is required to route to Top SoDIMM for AMTto function. Ch.A SODIMM needs to be populated for Intel AMT support.

TOP REV

BOT STD

JDIM1

JDIM2

PC4800 DDR2 SDRAM SO-DIMM (200P)

FOX_ AS0A426-N2RN-7F

FOX_ AS0A426-N2SN-7F

CLOCK 0,1
CKE 0,1

CLOCK 2,3
CKE 2,3

SMbus address A0

SMbus address A4

Non-iAMT

Place these Caps near So-Dimm1.

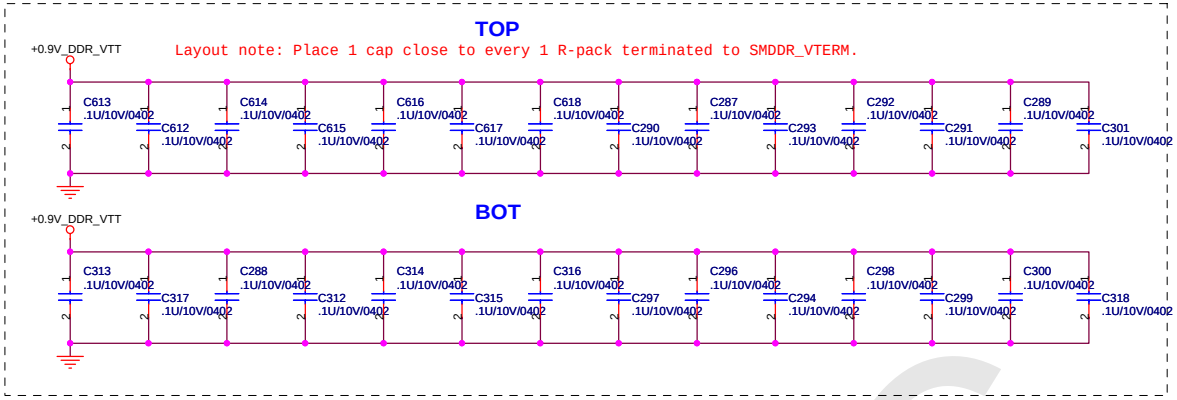
Place these Caps near So-Dimm2.

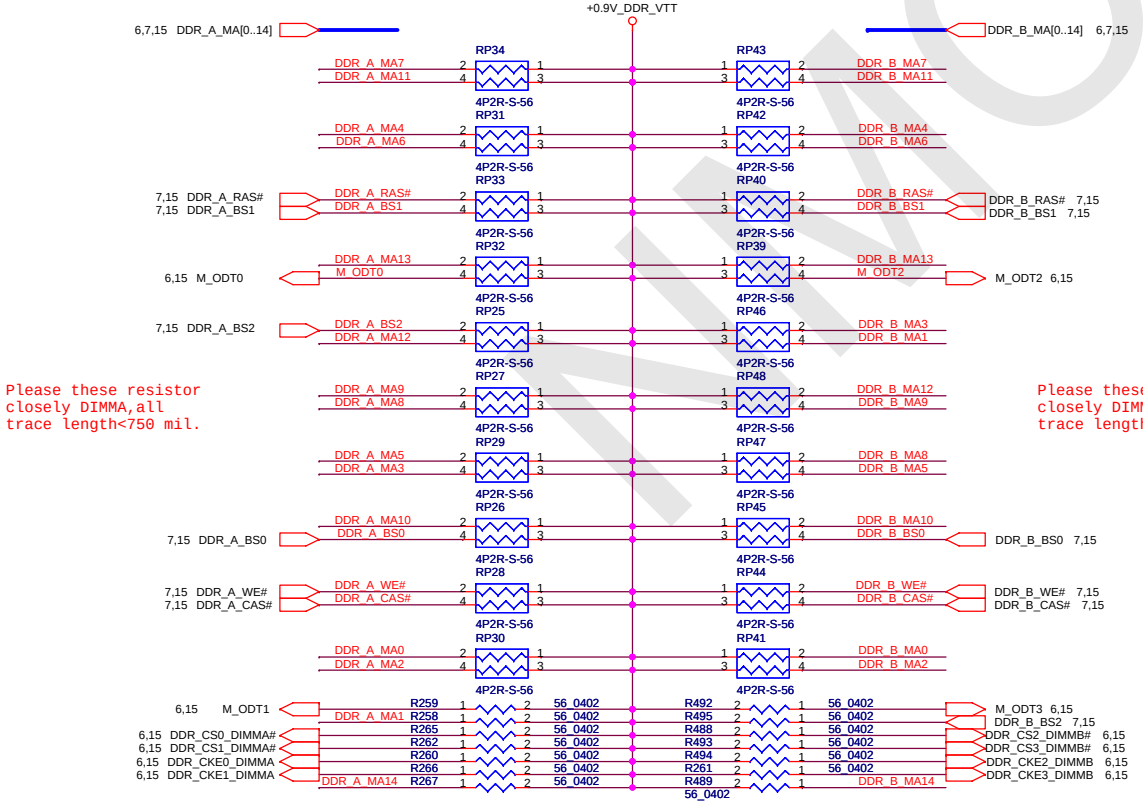
Place these Caps near So-Dimm1.

Place these Caps near So-Dimm2.

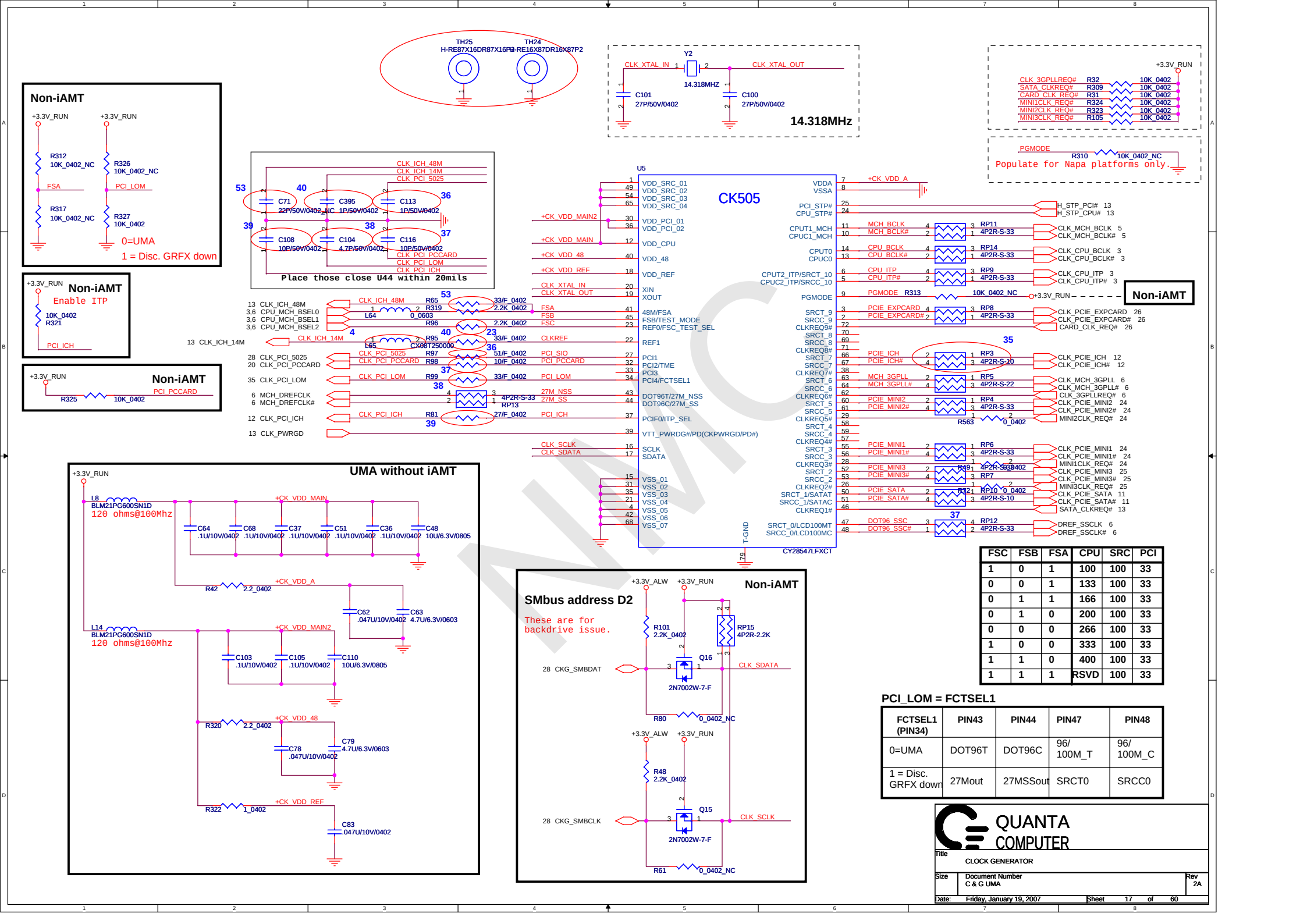
QUANTA COMPUTER

| | | |
|---|---|---|
| Title | DDR2 SO-DIMM (200P) X 2 | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 15 of 60 | |




| | | |
|---|---|---|
| QUANTA COMPUTER | | |
| Title: DDR2 RES ARRAY | | |
| Size | Document Number: C & G UMA | Rev: 2A |
| Date: Friday, January 19, 2007 | Sheet 16 of 60 | |



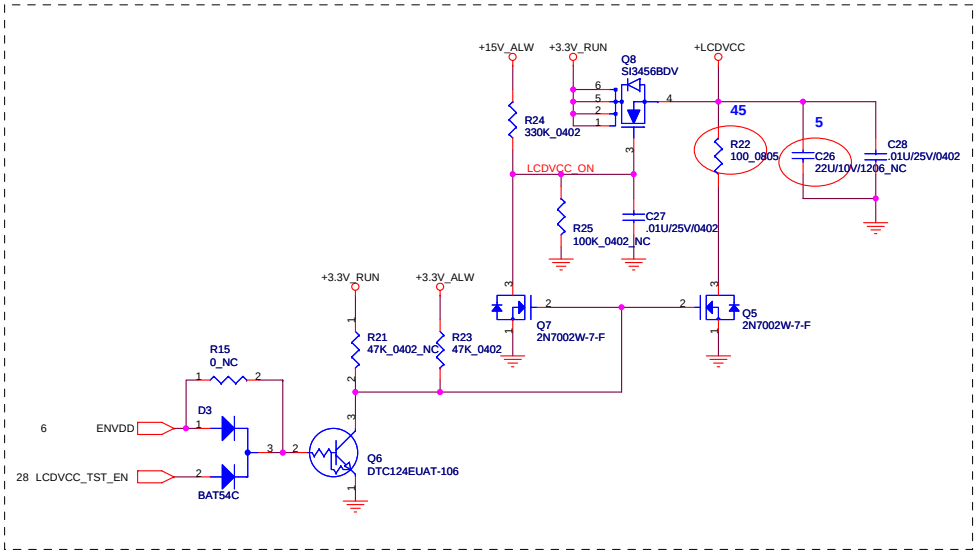

| FSC | FSB | FSA | CPU | SRC | PCI |
|---|---|---|---|---|---|
| 1 | 0 | 1 | 100 | 100 | 33 |
| 0 | 0 | 1 | 133 | 100 | 33 |
| 0 | 1 | 1 | 166 | 100 | 33 |
| 0 | 1 | 0 | 200 | 100 | 33 |
| 0 | 0 | 0 | 266 | 100 | 33 |
| 1 | 0 | 0 | 333 | 100 | 33 |
| 1 | 1 | 0 | 400 | 100 | 33 |
| 1 | 1 | 1 | RSVD | 100 | 33 |

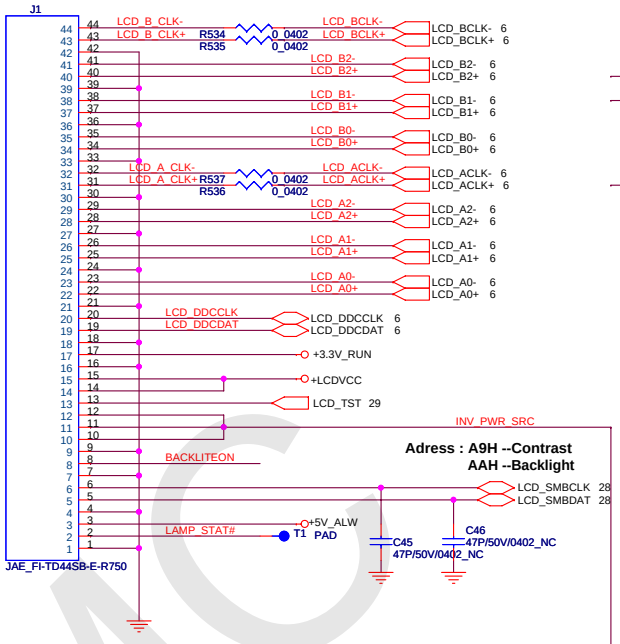
PCI_LOM = FCTSEL1

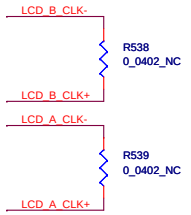
| FCTSEL1 (PIN34) | PIN43 | PIN44 | PIN47 | PIN48 |
|---|---|---|---|---|
| 0=UMA | DOT96T | DOT96C | 96/ 100M_T | 96/ 100M_C |
| 1 = Disc. GRFX down | 27Mout | 27MSSout | SRCT0 | SRCC0 |

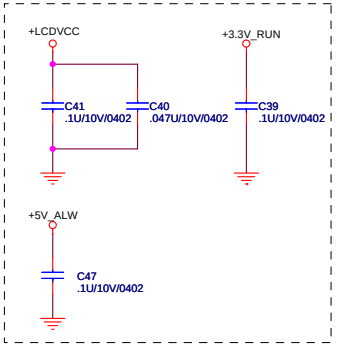
QUANTA COMPUTER

| | | |
|---|---|---|
| Title | CLOCK GENERATOR | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 17 of 60 | |

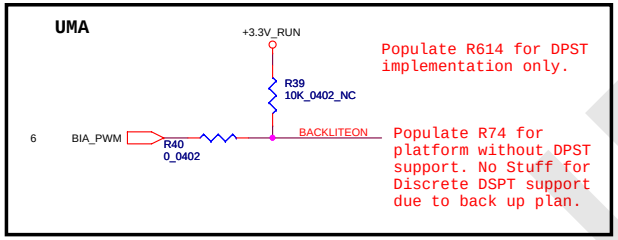


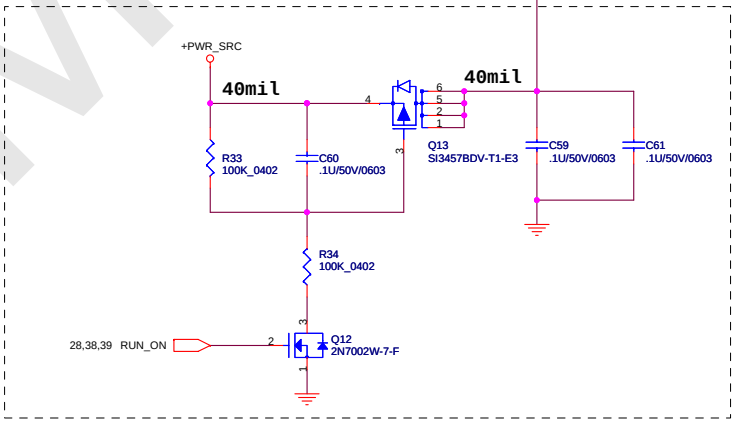




**Adress : A9H --Contrast**
**AAH --Backlight**

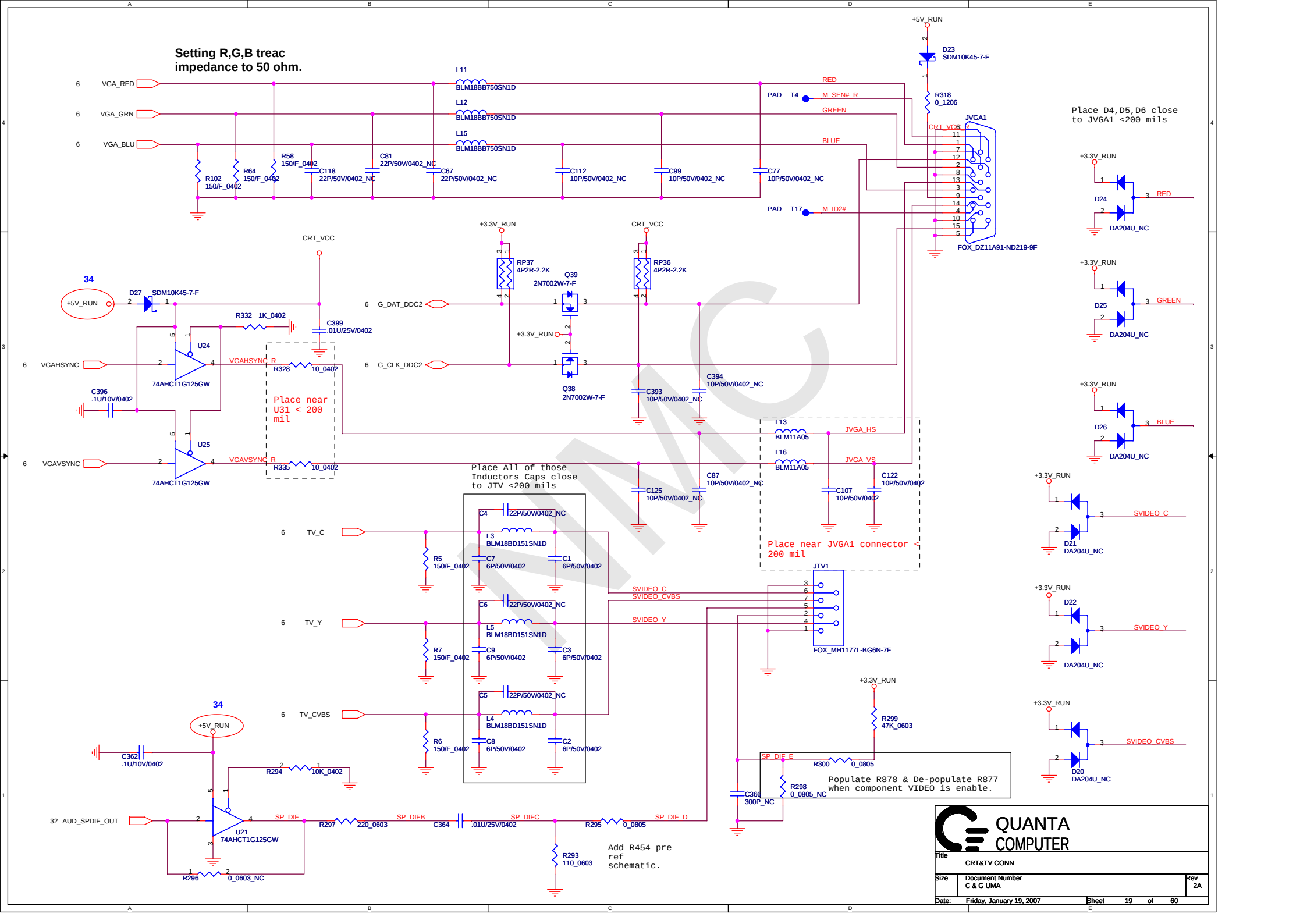


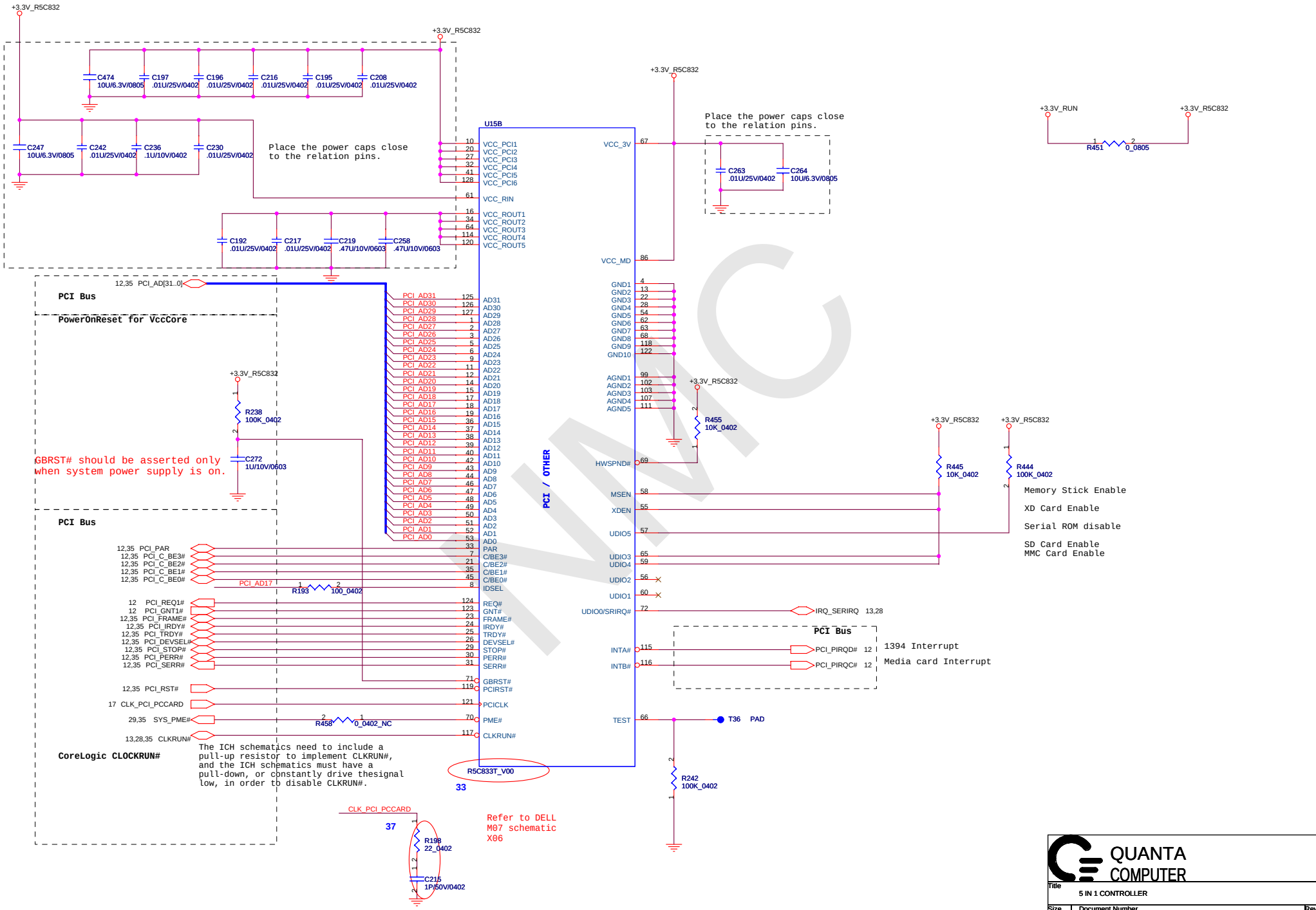



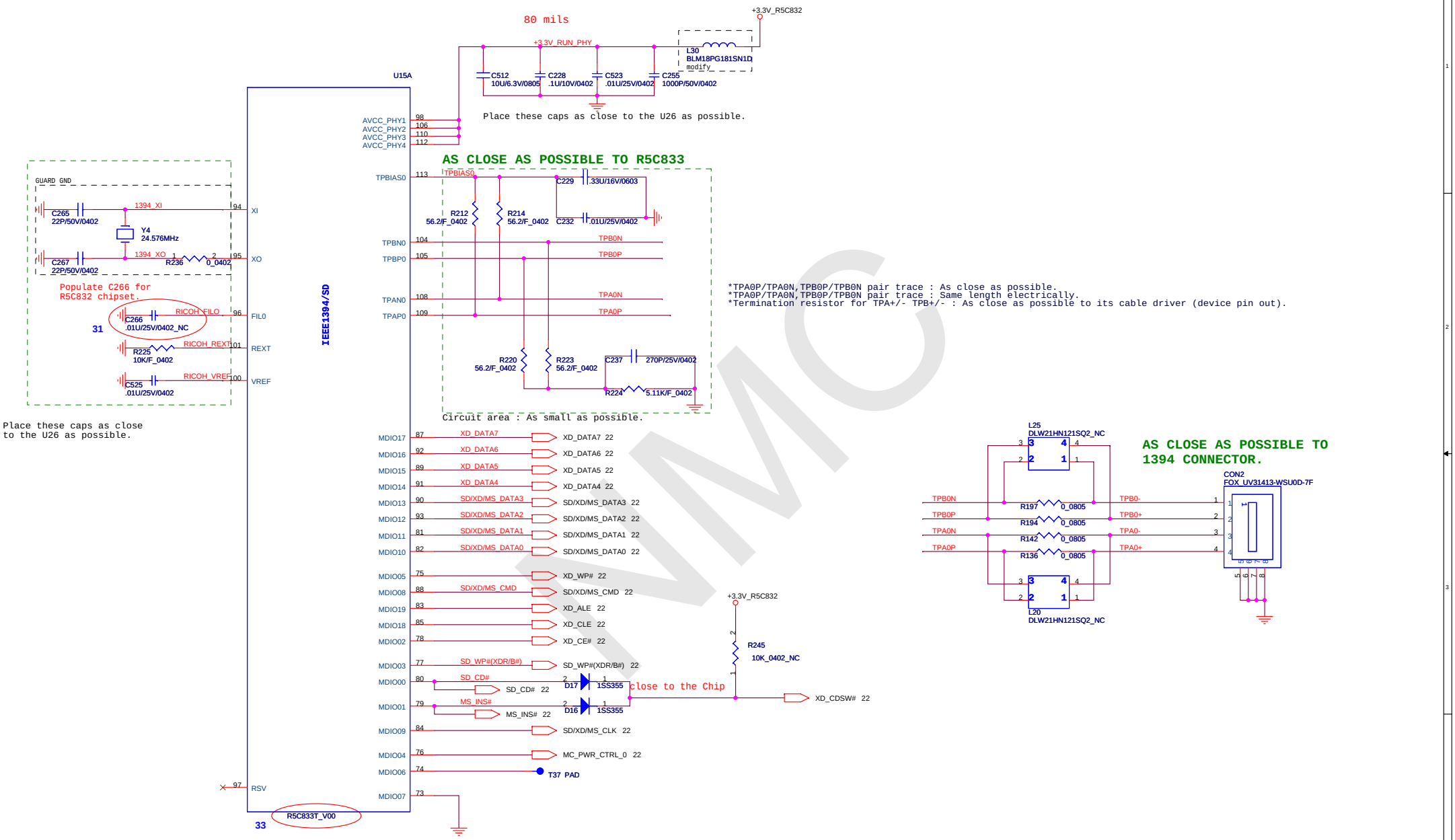



QUANTA COMPUTER

| | | |
|---|---|---|
| Title | LCD CONN | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 18 of 60 | |

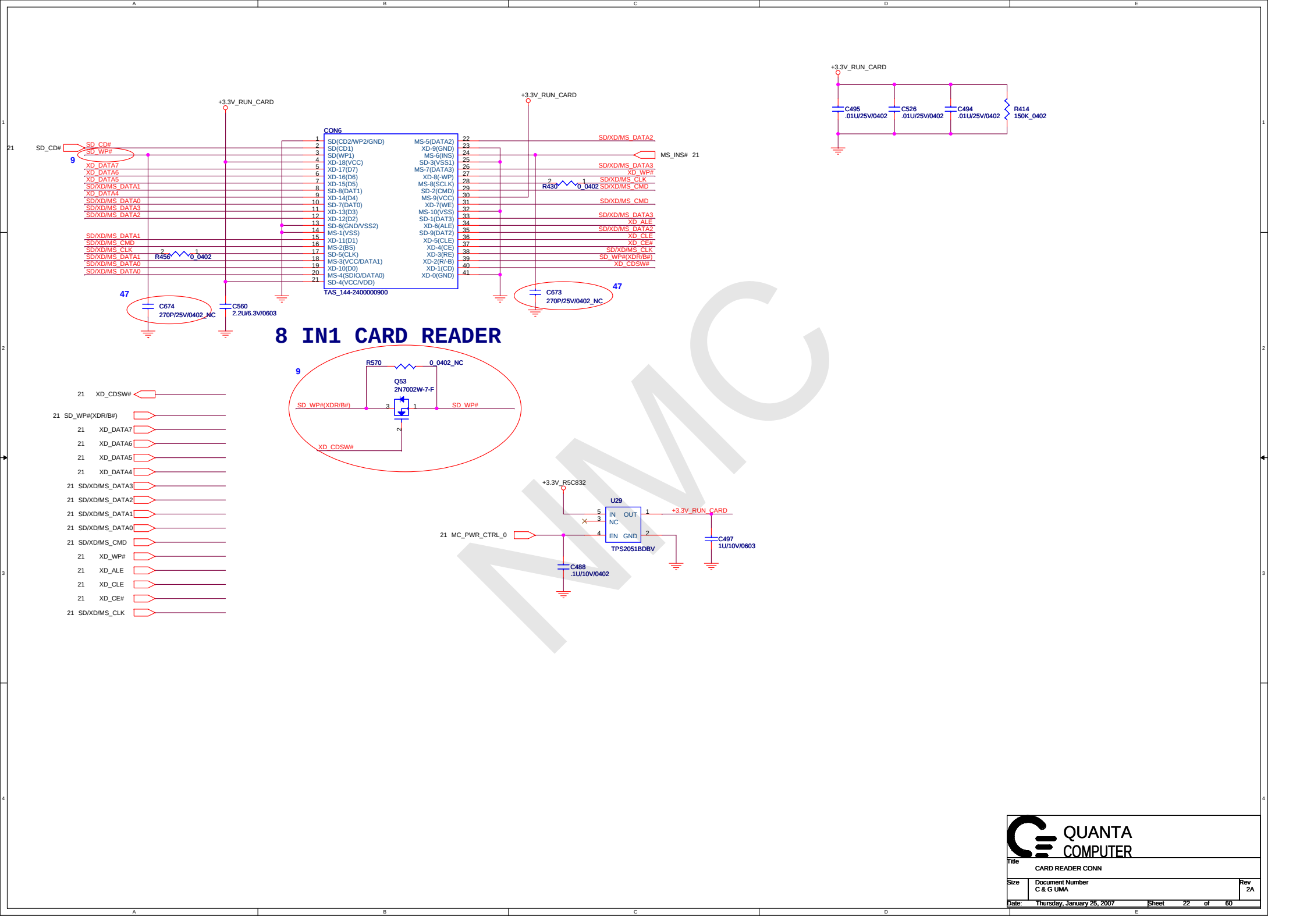

Setting R,G,B treac impedance to 50 ohm.
VGA_RED
VGA_GRN
VGA_BLU
L11 BLM18BB750SN1D
L12 BLM18BB750SN1D
L15 BLM18BB750SN1D
R102 150/F_0402
R64 150/F_0402
R58 150/F_0402
C118 22P/50V/0402_NC
C81 22P/50V/0402_NC
C67 22P/50V/0402_NC
C112 10P/50V/0402_NC
C99 10P/50V/0402_NC
C77 10P/50V/0402_NC
RED
GREEN
BLUE
PAD T4
M_SEN#_R
PAD T17
M_ID2#
+5V_RUN
D23 SDM10K45-7-F
R318 0_1206
JVGA1
CRT_VCC
FOX_DZ11A91-ND219-9F
Place D4,D5,D6 close to JVGA1 <200 mils
D24 DA204U_NC
D25 DA204U_NC
D26 DA204U_NC
34
D27 SDM10K45-7-F
R332 1K_0402
C399 .01U/25V/0402
U24
74AHCT1G125GW
VGAHSYNC
VGAHSYNC_R
R328 10_0402
U25
74AHCT1G125GW
VGAVSYNC
VGAVSYNC_R
R335 10_0402
C396 .1U/10V/0402
Place near U31 < 200 mil
+3.3V_RUN
RP37 4P2R-2.2K
RP36 4P2R-2.2K
Q39 2N7002W-7-F
Q38 2N7002W-7-F
G_DAT_DDC2
G_CLK_DDC2
C394 10P/50V/0402_NC
C393 10P/50V/0402_NC
C87 10P/50V/0402_NC
C125 10P/50V/0402_NC
L13 BLM11A05
L16 BLM11A05
JVGA_HS
JVGA_VS
C107 10P/50V/0402
C122 10P/50V/0402
Place near JVGA1 connector < 200 mil
Place All of those Inductors Caps close to JTV <200 mils
TV_C
TV_Y
TV_CVBS
C4 22P/50V/0402_NC
C6 22P/50V/0402_NC
C5 22P/50V/0402_NC
L3 BLM18BD151SN1D
L5 BLM18BD151SN1D
L4 BLM18BD151SN1D
R5 150/F_0402
R7 150/F_0402
R6 150/F_0402
C7 6P/50V/0402
C9 6P/50V/0402
C8 6P/50V/0402
C1 6P/50V/0402
C3 6P/50V/0402
C2 6P/50V/0402
SVIDEO_C
SVIDEO_CVBS
SVIDEO_Y
JTV1
FOX_MH1177L-BG6N-7F
D21 DA204U_NC
D22 DA204U_NC
D20 DA204U_NC
R299 47K_0603
SP_DIF_E
R300 0_0805
R298 0_0805_NC
C366 300P_NC
Populate R878 & De-populate R877 when component VIDEO is enable.
C362 .1U/10V/0402
R294 10K_0402
U21
74AHCT1G125GW
32 AUD_SPDIF_OUT
SP_DIF
R297 220_0603
SP_DIFB
C364 .01U/25V/0402
SP_DIFC
R295 0_0805
SP_DIF_D
R296 0_0603_NC
R293 110_0603
Add R454 pre ref schematic.
QUANTA COMPUTER
Title CRT&TV CONN
Size Document Number C & G UMA Rev 2A
Date: Friday, January 19, 2007 Sheet 19 of 60


+3.3V_R5C832
C474 10U/6.3V/0805
C197 .01U/25V/0402
C196 .01U/25V/0402
C216 .01U/25V/0402
C195 .01U/25V/0402
C208 .01U/25V/0402
C247 10U/6.3V/0805
C242 .01U/25V/0402
C236 .1U/10V/0402
C230 .01U/25V/0402
Place the power caps close to the relation pins.
C192 .01U/25V/0402
C217 .01U/25V/0402
C219 .47U/10V/0603
C258 .47U/10V/0603
U15B
VCC_PCI1
VCC_PCI2
VCC_PCI3
VCC_PCI4
VCC_PCI5
VCC_PCI6
VCC_RIN
VCC_ROUT1
VCC_ROUT2
VCC_ROUT3
VCC_ROUT4
VCC_ROUT5
VCC_3V
VCC_MD
C263 .01U/25V/0402
C264 10U/6.3V/0805
Place the power caps close to the relation pins.
+3.3V_RUN
R451 0_0805
12,35 PCI_AD[31..0]
PCI Bus
PowerOnReset for VccCore
R238 100K_0402
C272 1U/10V/0603
GBRST# should be asserted only when system power supply is on.
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_AD23
PCI_AD22
PCI_AD21
PCI_AD20
PCI_AD19
PCI_AD18
PCI_AD17
PCI_AD16
PCI_AD15
PCI_AD14
PCI_AD13
PCI_AD12
PCI_AD11
PCI_AD10
PCI_AD9
PCI_AD8
PCI_AD7
PCI_AD6
PCI_AD5
PCI_AD4
PCI_AD3
PCI_AD2
PCI_AD1
PCI_AD0
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
PCI / OTHER
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
AGND1
AGND2
AGND3
AGND4
AGND5
R455 10K_0402
HWSPND#
MSEN
XDEN
UDIO5
UDIO3
UDIO4
UDIO2
UDIO1
UDIO0/SRIRQ#
IRQ_SERIRQ 13,28
R445 10K_0402
R444 100K_0402
Memory Stick Enable
XD Card Enable
Serial ROM disable
SD Card Enable
MMC Card Enable
12,35 PCI_PAR
12,35 PCI_C_BE3#
12,35 PCI_C_BE2#
12,35 PCI_C_BE1#
12,35 PCI_C_BE0#
PCI_AD17
R193 100_0402
C/BE3#
C/BE2#
C/BE1#
C/BE0#
PAR
IDSEL
12 PCI_REQ1#
12 PCI_GNT1#
12,35 PCI_FRAME#
12,35 PCI_IRDY#
12,35 PCI_TRDY#
12,35 PCI_DEVSEL#
12,35 PCI_STOP#
12,35 PCI_PERR#
12,35 PCI_SERR#
REQ#
GNT#
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PERR#
SERR#
12,35 PCI_RST#
17 CLK_PCI_PCCARD
29,35 SYS_PME#
13,28,35 CLKRUN#
GBRST#
PCIRST#
PCICLK
PME#
CLKRUN#
R458 0_0402_NC
PCI Bus
PCI_PIRQD# 12
PCI_PIRQC# 12
1394 Interrupt
Media card Interrupt
INTA#
INTB#
TEST
T36 PAD
R242 100K_0402
CoreLogic CLOCKRUN#
The ICH schematics need to include a pull-up resistor to implement CLKRUN#, and the ICH schematics must have a pull-down, or constantly drive thesignal low, in order to disable CLKRUN#.
R5C833T_V00
33
CLK_PCI_PCCARD
37
R198 22_0402
C215 1P/50V/0402
Refer to DELL M07 schematic X06
QUANTA COMPUTER
Title
5 IN 1 CONTROLLER
Size
Document Number
C & G UMA
Rev
2A
Date: Friday, January 19, 2007
Sheet 20 of 60




QUANTA COMPUTER

| | | |
|---|---|---|
| Title | IEEE 1394 | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 21 of 60 | |



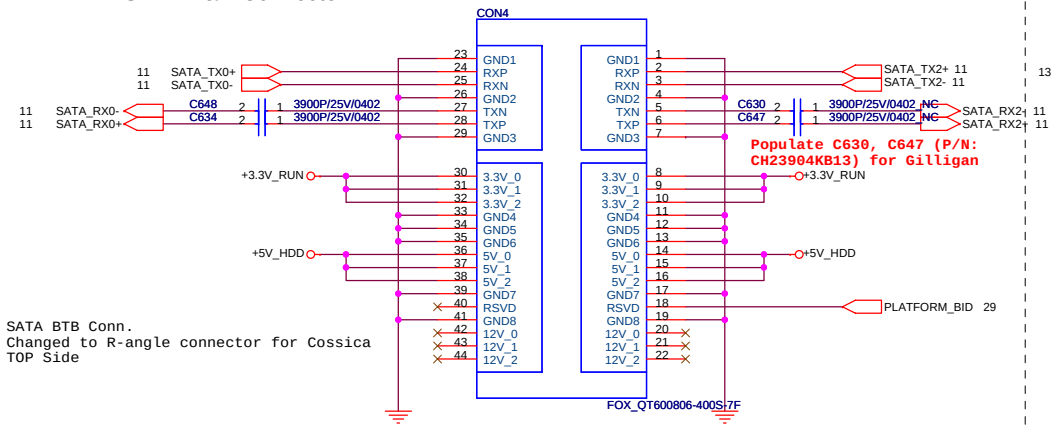



QUANTA COMPUTER

| | | |
|---|---|---|
| Title | CARD READER CONN | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Thursday, January 25, 2007 | Sheet 22 of 60 | |

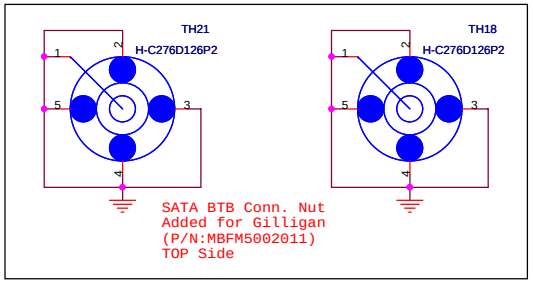
## SATA 1 & 2 Connector.

Change CON4 P/N to DFHS44FS611 for Gilligan.



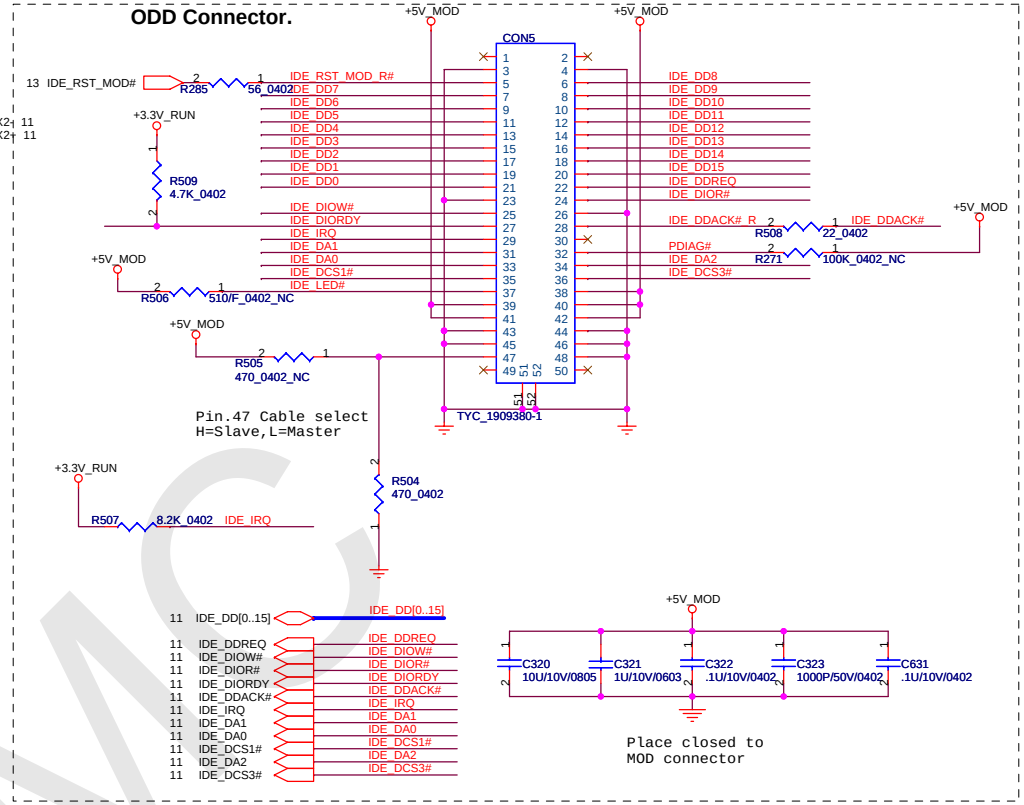

Populate C630, C647 (P/N: CH23904KB13) for Gilligan

SATA BTB Conn.
Changed to R-angle connector for Cossica
TOP Side




SATA BTB Conn. Nut
Added for Gilligan
(P/N:MBFM5002011)
TOP Side

## ODD Connector.




Pin.47 Cable select
H=Slave,L=Master



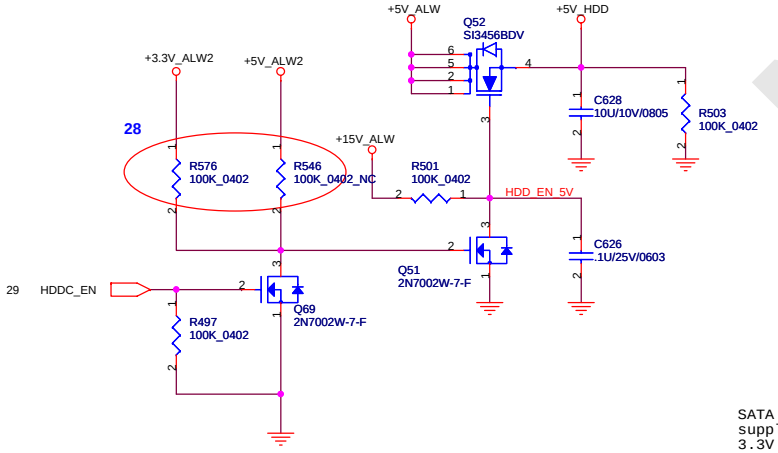


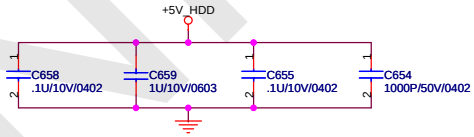




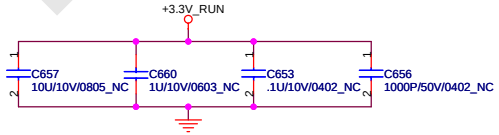

Place closed to
MOD connector

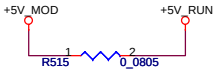
## SATA 1 PWR




Removed C654,C655,
C658,C659 for Gilligan.



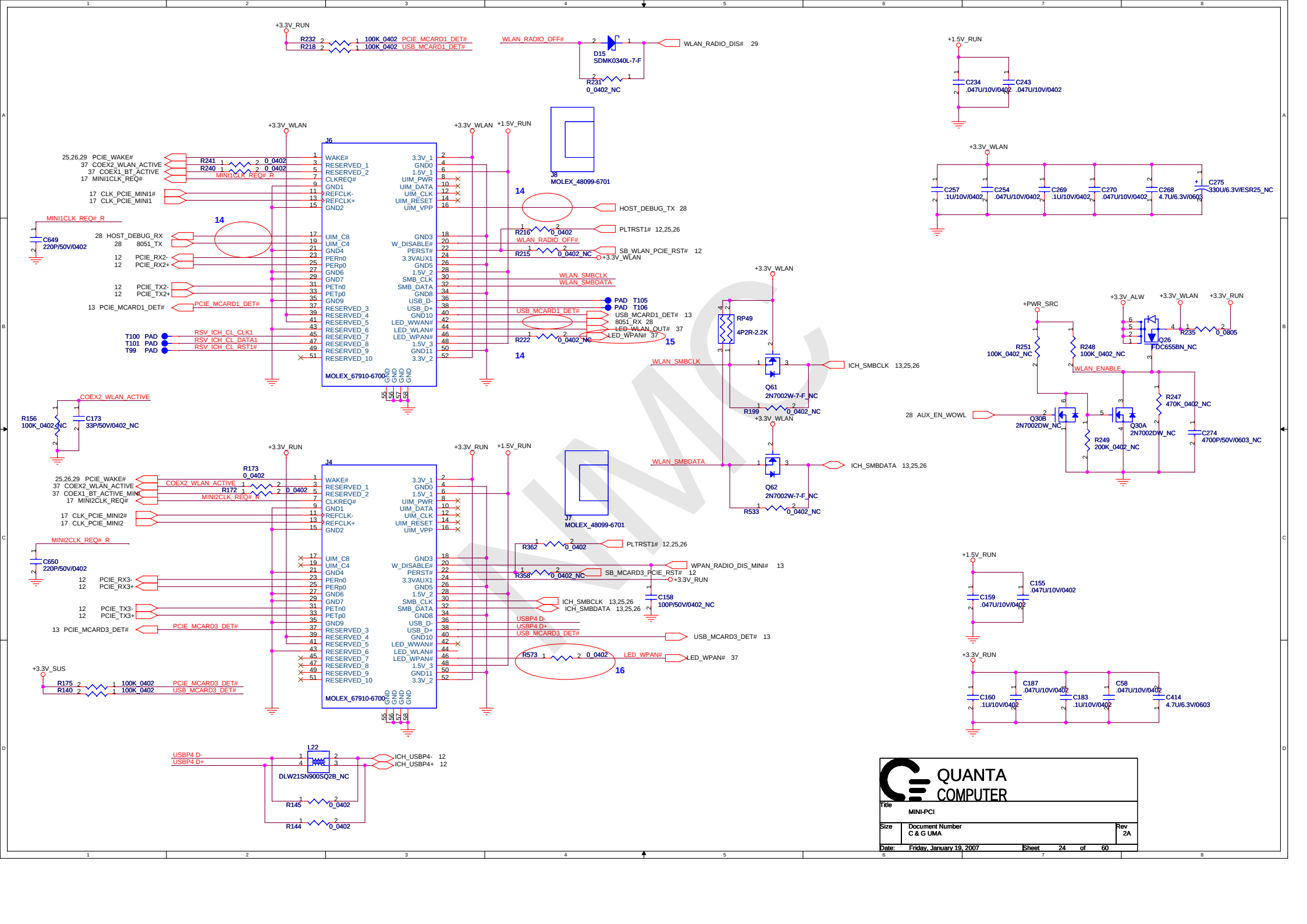




SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

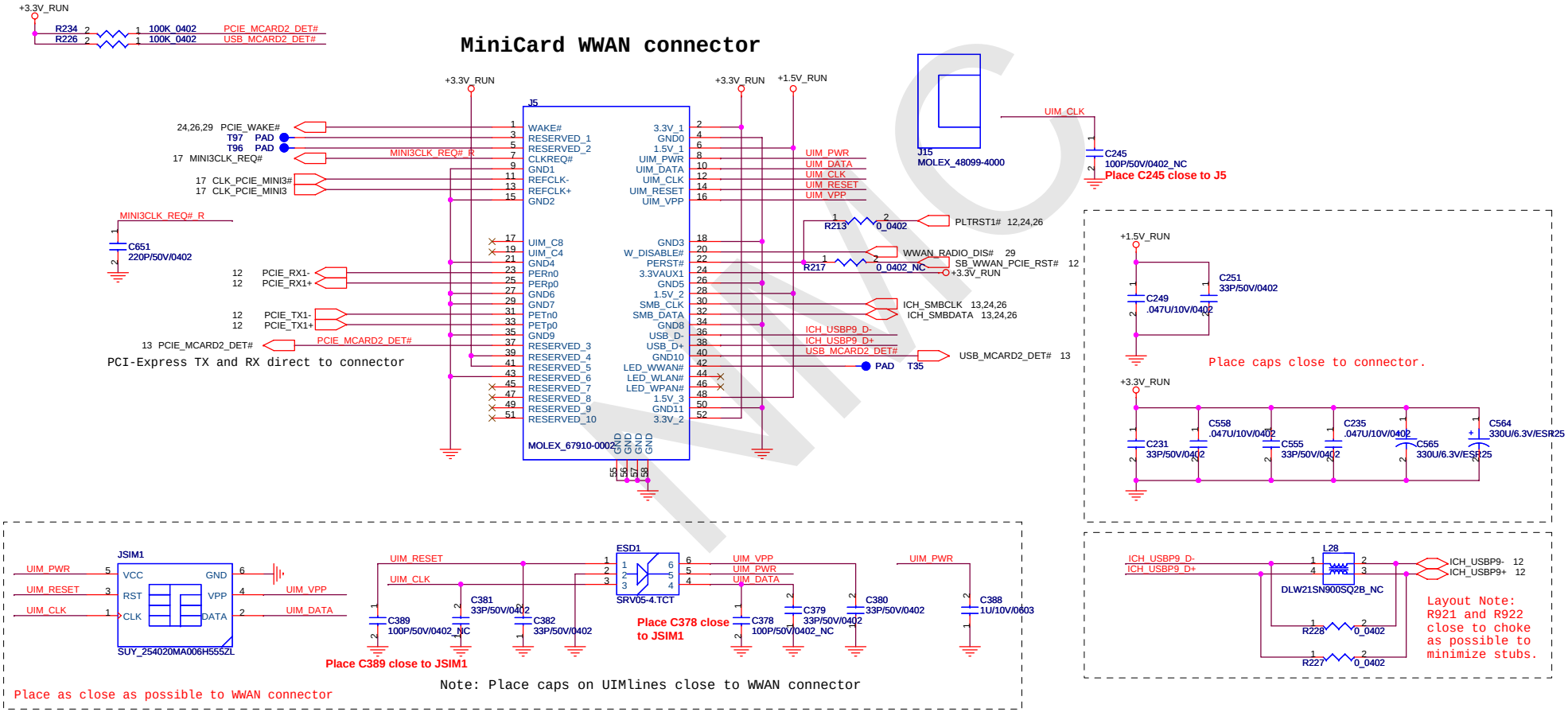
Power Estimate:
SATA drive power consumption estimate at MobileMark is 1.1W. An additional 150mW can be saved using Intel's IMST driver.

QUANTA COMPUTER

| | | |
|---|---|---|
| Title | SATA (HDD&CD_ROM) | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 23 of 60 | |


+3.3V_RUN
R232 100K_0402 PCIE_MCARD1_DET#
R218 100K_0402 USB_MCARD1_DET#
WLAN_RADIO_OFF#
D15 SDMK0340L-7-F
WLAN_RADIO_DIS# 29
R231 0_0402_NC
+1.5V_RUN
C234 .047U/10V/0402
C243 .047U/10V/0402
+3.3V_WLAN
J6
J8 MOLEX_48099-6701
25,26,29 PCIE_WAKE#
37 COEX2_WLAN_ACTIVE
37 COEX1_BT_ACTIVE
17 MINI1CLK_REQ#
R241 0_0402
R240 0_0402
MINI1CLK_REQ# R
17 CLK_PCIE_MINI1#
17 CLK_PCIE_MINI1
C649 220P/50V/0402
28 HOST_DEBUG_RX
28 8051_TX
12 PCIE_RX2-
12 PCIE_RX2+
12 PCIE_TX2-
12 PCIE_TX2+
13 PCIE_MCARD1_DET#
T100 PAD
T101 PAD
T99 PAD
RSV_ICH_CL_CLK1
RSV_ICH_CL_DATA1
RSV_ICH_CL_RST1#
HOST_DEBUG_TX 28
PLTRST1# 12,25,26
R216 0_0402
R215 0_0402_NC
SB_WLAN_PCIE_RST# 12
WLAN_SMBCLK
WLAN_SMBDATA
PAD T105
PAD T106
USB_MCARD1_DET# 13
8051_RX 28
LED_WLAN_OUT# 37
LED_WPAN# 37
R222 0_0402_NC
C257 .1U/10V/0402
C254 .047U/10V/0402
C269 .1U/10V/0402
C270 .047U/10V/0402
C268 4.7U/6.3V/0603
C275 330U/6.3V/ESR25_NC
RP49 4P2R-2.2K
Q61 2N7002W-7-F_NC
R199 0_0402_NC
ICH_SMBCLK 13,25,26
Q62 2N7002W-7-F_NC
R533 0_0402_NC
ICH_SMBDATA 13,25,26
+PWR_SRC
+3.3V_ALW
R251 100K_0402_NC
R248 100K_0402_NC
R235 0_0805
Q26 FDC655BN_NC
WLAN_ENABLE
28 AUX_EN_WOWL
Q30B 2N7002DW_NC
Q30A 2N7002DW_NC
R247 470K_0402_NC
R249 200K_0402_NC
C274 4700P/50V/0603_NC
COEX2_WLAN_ACTIVE
R156 100K_0402_NC
C173 33P/50V/0402_NC
J4
J7 MOLEX_48099-6701
R173 0_0402
25,26,29 PCIE_WAKE#
37 COEX2_WLAN_ACTIVE
37 COEX1_BT_ACTIVE_MINI
17 MINI2CLK_REQ#
R172 0_0402
MINI2CLK_REQ# R
17 CLK_PCIE_MINI2#
17 CLK_PCIE_MINI2
C650 220P/50V/0402
12 PCIE_RX3-
12 PCIE_RX3+
12 PCIE_TX3-
12 PCIE_TX3+
13 PCIE_MCARD3_DET#
R362 0_0402
R358 0_0402_NC
WPAN_RADIO_DIS_MINI# 13
C158 100P/50V/0402_NC
USBP4 D-
USBP4 D+
USB_MCARD3_DET# 13
R573 0_0402
LED_WPAN# 37
C155 .047U/10V/0402
C159 .047U/10V/0402
+3.3V_SUS
R175 100K_0402
R140 100K_0402
C160 .1U/10V/0402
C187 .047U/10V/0402
C183 .1U/10V/0402
C58 .047U/10V/0402
C414 4.7U/6.3V/0603
L22 DLW21SN900SQ2B_NC
ICH_USBP4- 12
ICH_USBP4+ 12
R145 0_0402
R144 0_0402
QUANTA COMPUTER
Title MINI-PCI
Size
Document Number C & G UMA
Rev 2A
Date: Friday, January 19, 2007
Sheet 24 of 60

# MiniCard WWAN connector

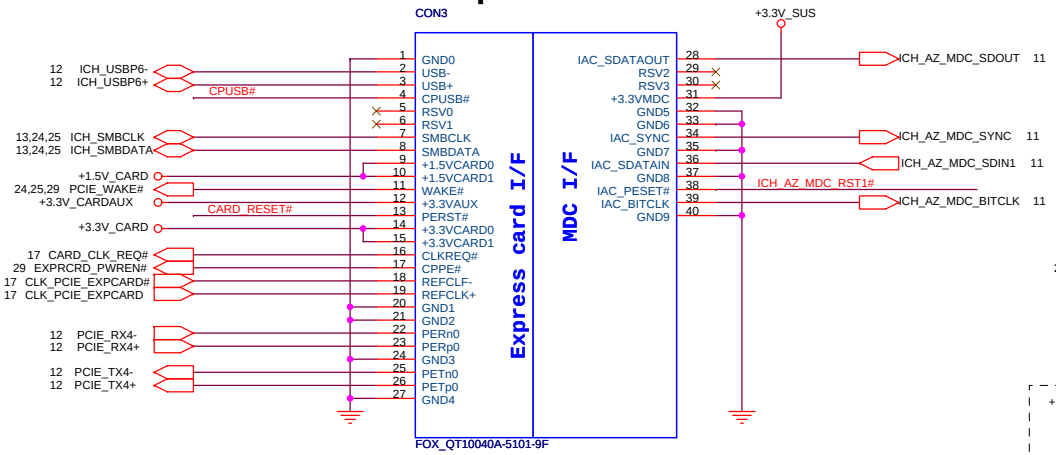


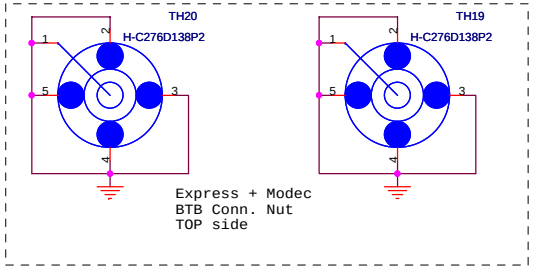

QUANTA COMPUTER

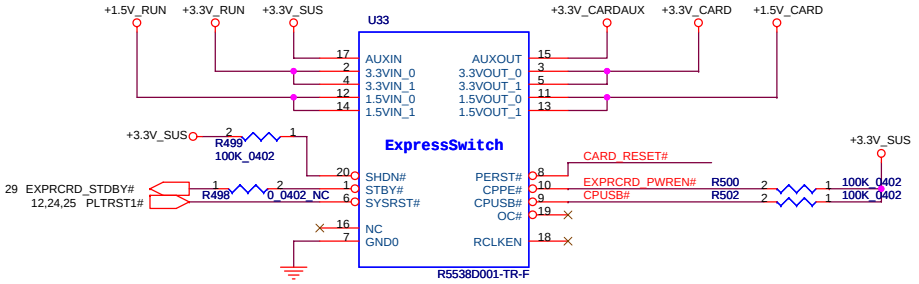
| | | |
|---|---|---|
| Title | WWAN | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 25 of 60 | |

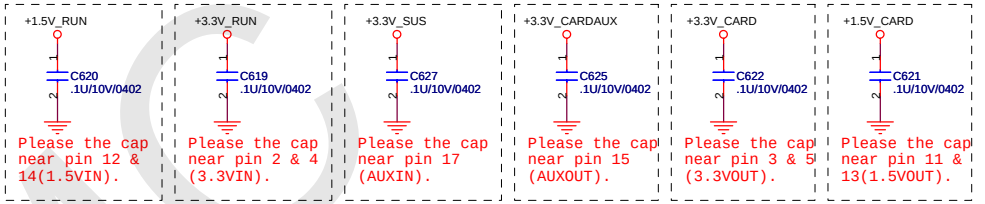
# EXPRESS+MDC
# Update PN

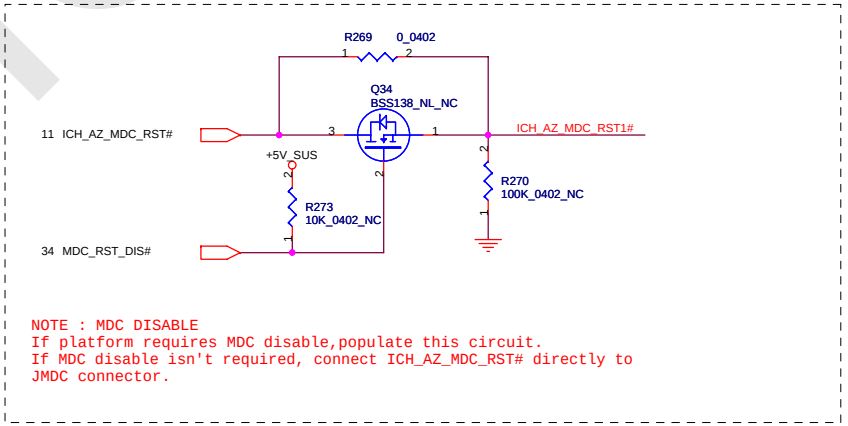
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



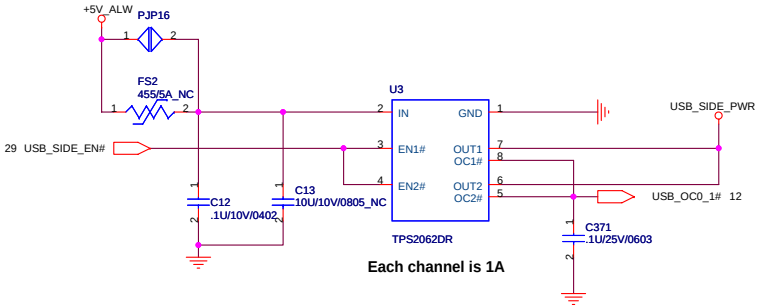



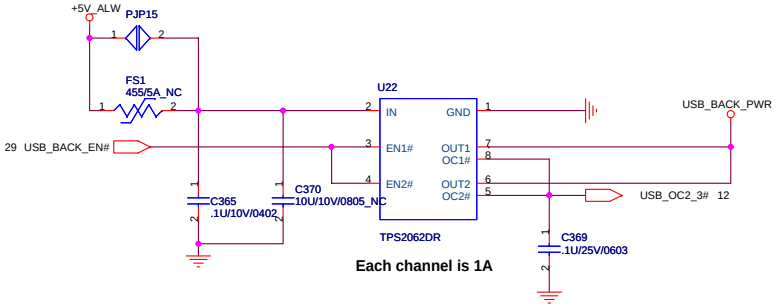



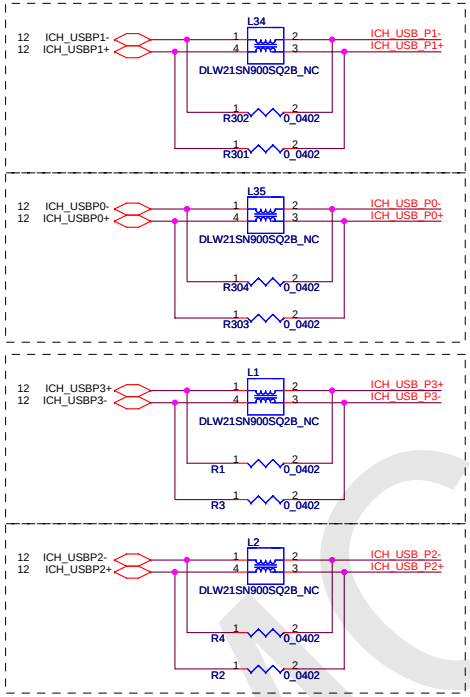



QUANTA COMPUTER

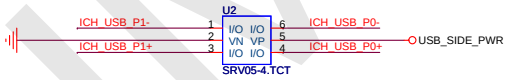
| | | |
|---|---|---|
| Title | ExpressCard/SmartCard | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 26 of 60 | |



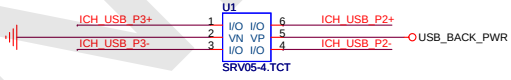



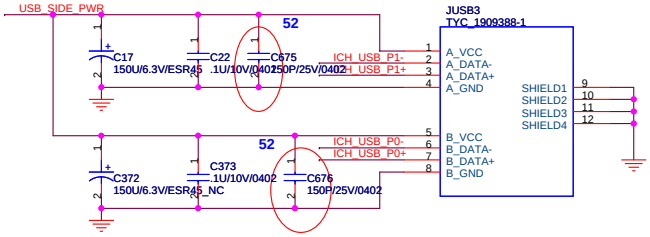

Place ESD diodes as close as USB connector.



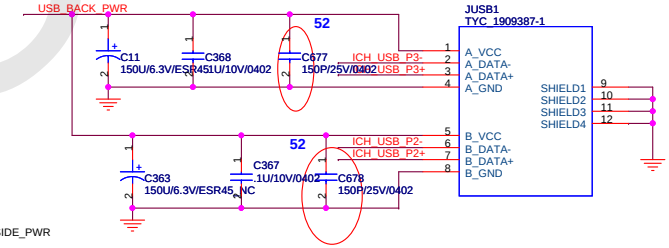

Place ESD diodes as close as USB connector.



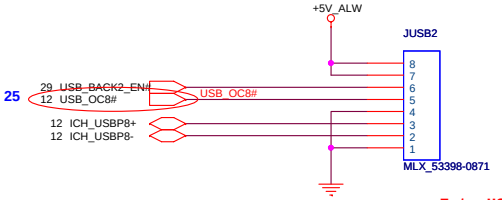

## Right




## Back




## For Gilligan

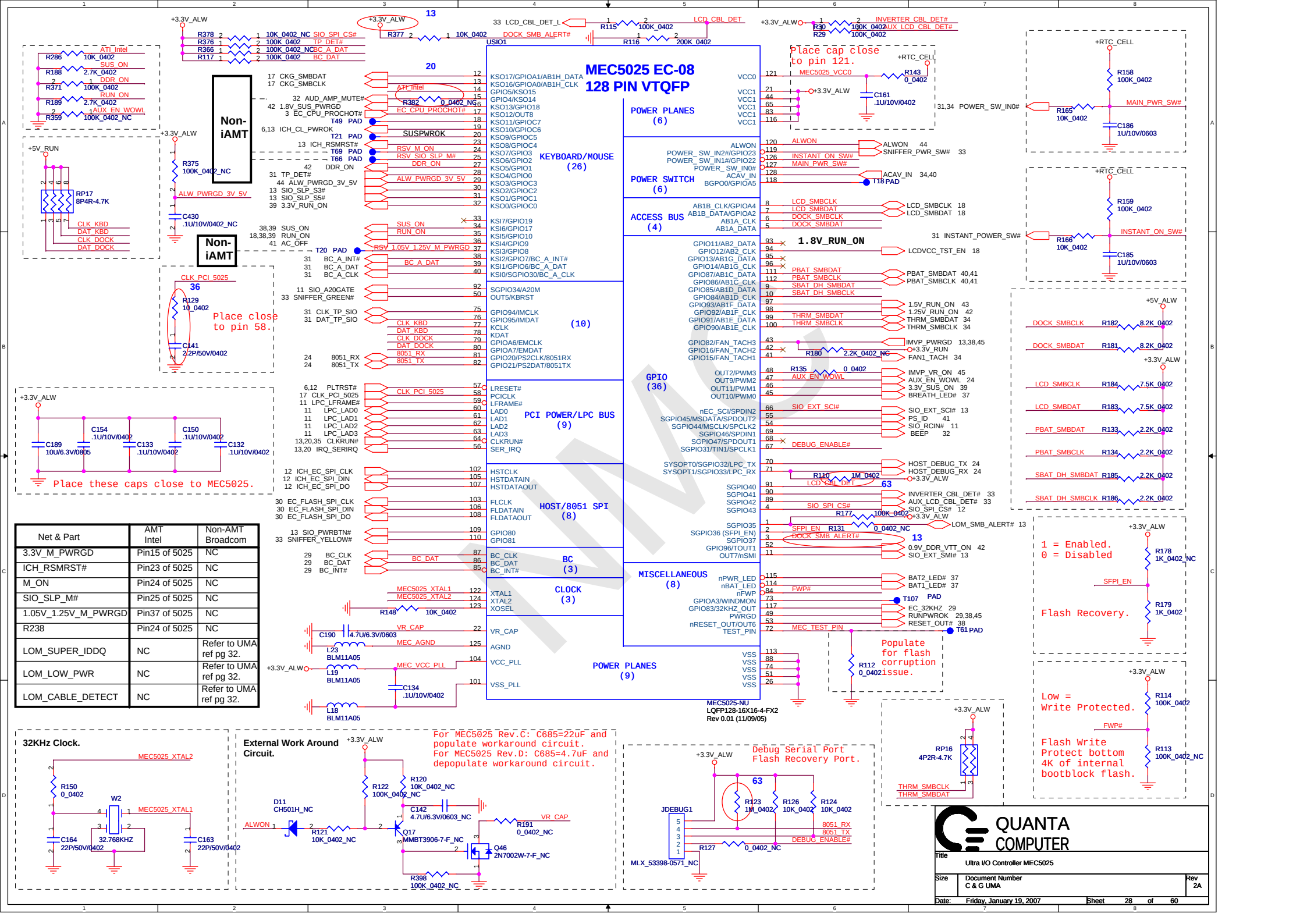



**Ext. USB WTB Conn.**
**Populate for Gilligan**
**(P/N: DFHD08MS731)**
**TOP Side**



QUANTA COMPUTER

| | | |
|---|---|---|
| Title | External USB | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 27 of 60 | |




| Net & Part | AMT Intel | Non-AMT Broadcom |
|---|---|---|
| 3.3V_M_PWRGD | Pin15 of 5025 | NC |
| ICH_RSMRST# | Pin23 of 5025 | NC |
| M_ON | Pin24 of 5025 | NC |
| SIO_SLP_M# | Pin25 of 5025 | NC |
| 1.05V_1.25V_M_PWRGD | Pin37 of 5025 | NC |
| R238 | Pin24 of 5025 | NC |
| LOM_SUPER_IDDQ | NC | Refer to UMA ref pg 32. |
| LOM_LOW_PWR | NC | Refer to UMA ref pg 32. |
| LOM_CABLE_DETECT | NC | Refer to UMA ref pg 32. |

55

**Update to 5021:**

Depopulate R549, R550, R551, R552, R170, R176, R553, R554, R555, R556, R557, C178, C442, C175, C176, C199, C218, C209, L24.
Populate R542, C349.

USIO2

**ECE5021 128 Pin VTQFP**

GPIOs
USB
CIRCC
POWER
VSS
SIO Reset
BC
MISCELLANEOUS

ECE5021-NU

| BID3 | BID2 | BID1 | BID0 | Board Revision |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | SST (X00) |
| 0 | 0 | 0 | 1 | PT (X01) |
| 0 | 0 | 1 | 0 | ST (X02) |
| 0 | 0 | 1 | 1 | QT (A00) |
| 0 | 0 | 0 | 0 | RAMP(A01) |

PROCHOT# change to CPU_PROCHOT# per ref schematic.

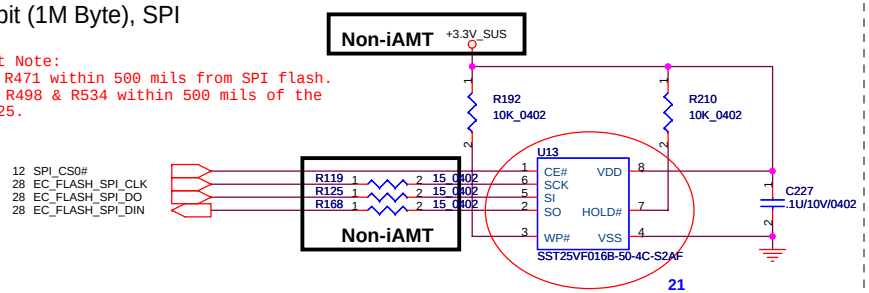
Place C349 close to USIO2.8

| | |
|---|---|
| Title | SIO (GPIO/BC/USB/CIRR) |
| Size | Document Number: C & G UMA |
| Rev | 2A |
| Date: | Friday, January 19, 2007 |
| Sheet | 29 of 60 |

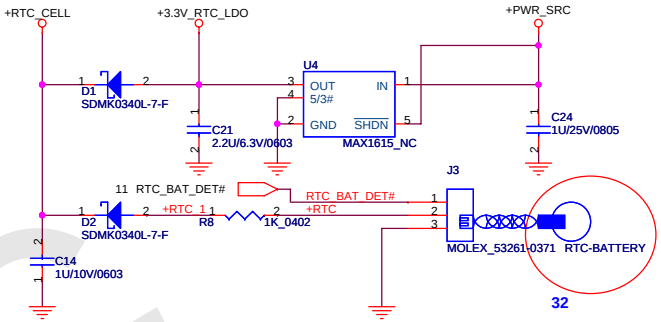
QUANTA COMPUTER

## 8Mbit (1M Byte), SPI

Layout Note:
Place R471 within 500 mils from SPI flash.
Place R498 & R534 within 500 mils of the MEC5025.



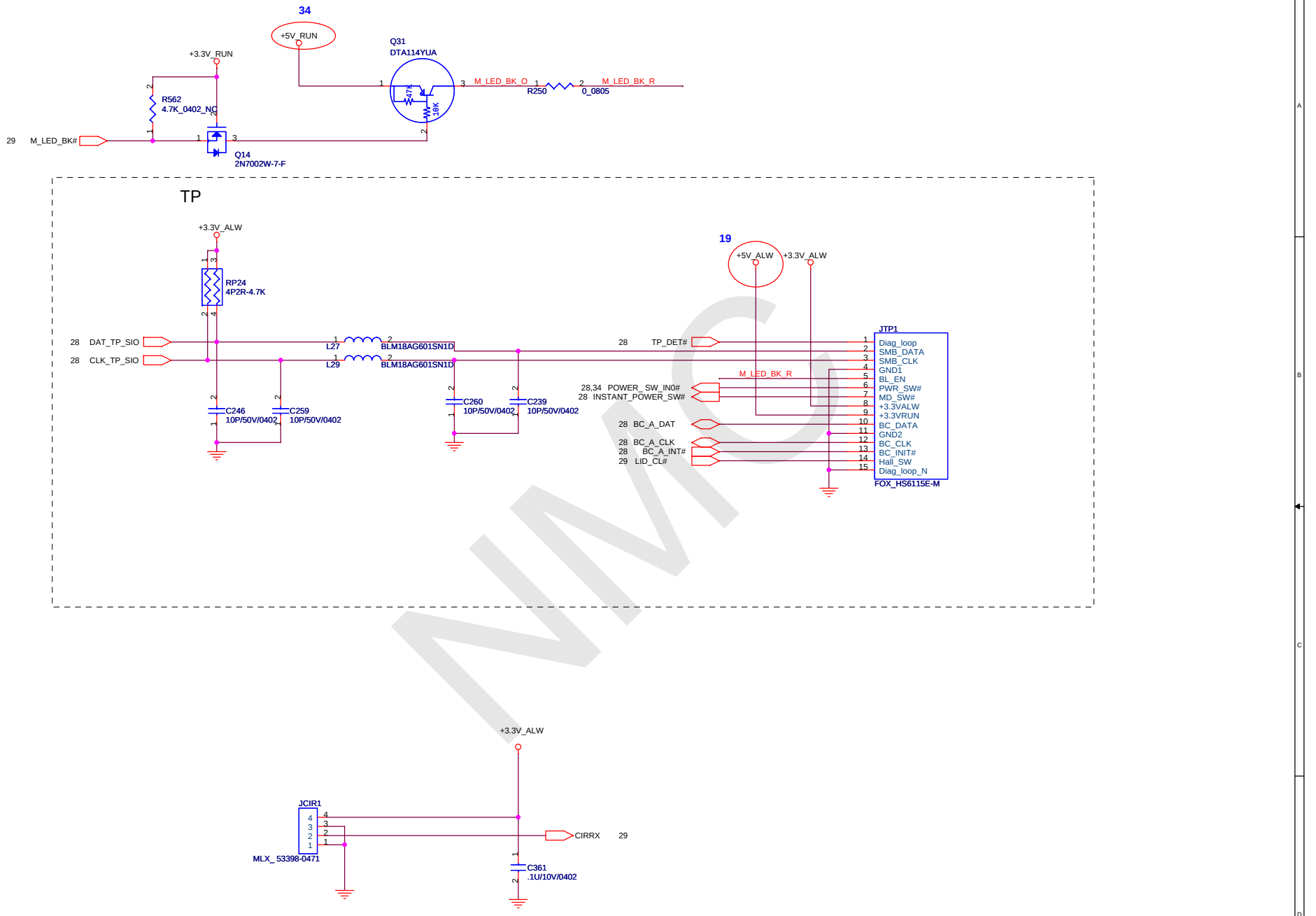

## RTC BATTERY






QUANTA COMPUTER

| | | |
|---|---|---|
| Title | FLASH, RTC & KC | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 30 of 60 | |






QUANTA COMPUTER

| | | |
|---|---|---|
| Title | TP/KB/Media/CIR Conn. | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 31 of 60 | |

# INTERNAL SPEAKER AMP

Package 1206 for THD+N performance for Vista Logo requirements.

MAX9789A
TQFN 32PIN

U19
MAX9789AETJ+

For TPA6040A,pop R530,depop R531.

C1425/C331 value need to match with C326/C290. This value be chosen in PT phase

For TPA6040A,pop C640,depop R529.

For TPA6040A,pop C331,depop R406.

L35
FB_600ohm+-25%_100MHz _200mA_0.6ohm DC

FB_60ohm+-25%_100MHz _3A_0.05ohm DC

Layout Note: Place close U22.

Layout Note: Place close to pin 18.

Layout Note: Place close to pin 8.

Layout Note: Close to Pin 13.

EMI Request

| GAIN1 | GAIN2 | GAIN |
|---|---|---|
| 0 | 0 | 6dB |
| 0 | 1 | 10dB |
| 1 | 0 | 15.6dB |
| 1 | 1 | 21.6dB |

# AZALIA (HD) CODEC

STAC9205
LQFP 48PIN

U18
STAC9205_B2

For tuning.

Depop R441 & pop C394 & C312 for AD1984.

Pop C315 & R603 for AD1984.
C288 need change to 1uF.

Close to pin 6.

Close to pin 5.

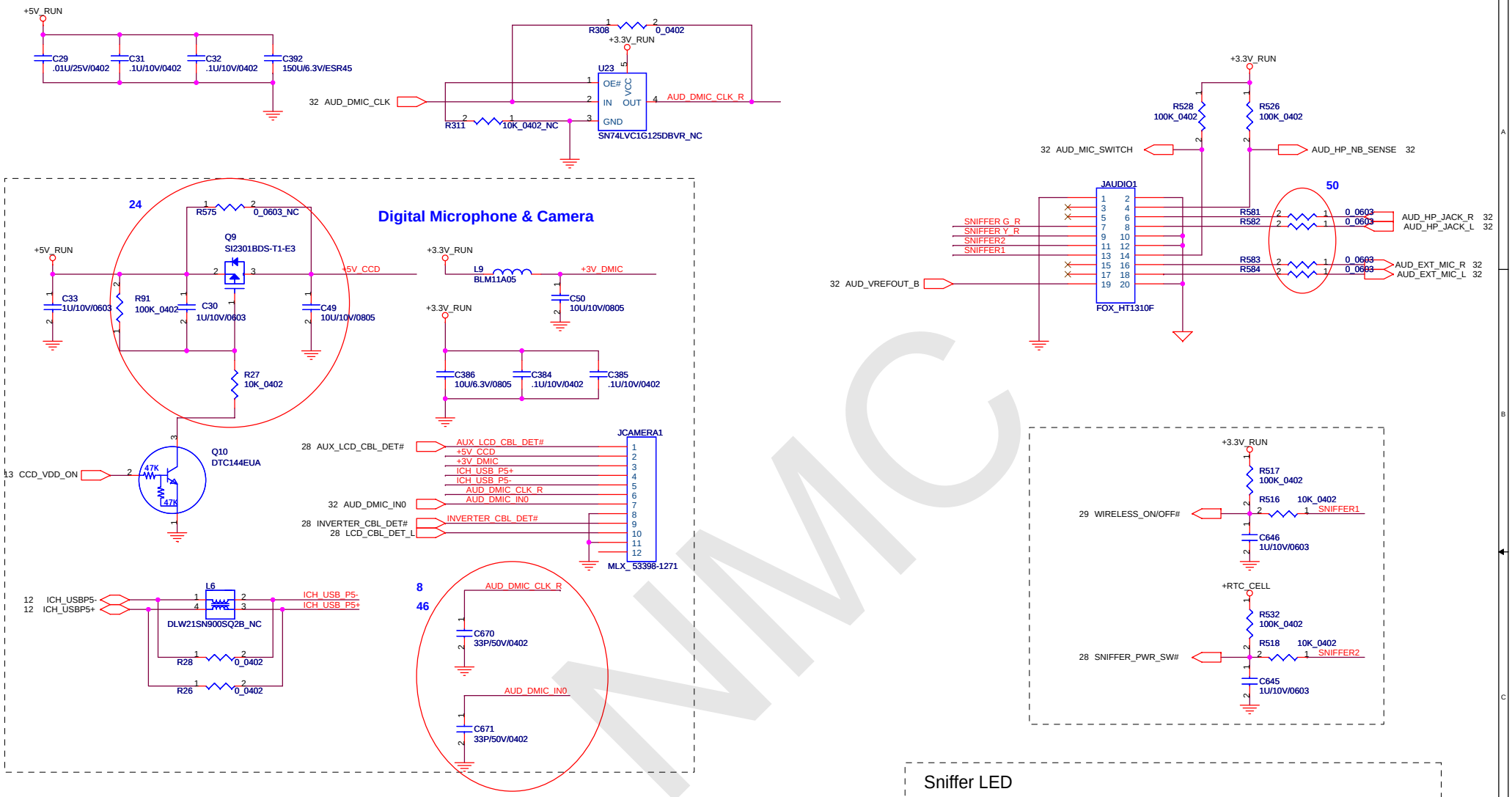
Close to U17.

U17
74LVC1G86GW



QUANTA COMPUTER

| | | |
|---|---|---|
| Title | Azelia CODEC(STAC9205)) | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: | Tuesday, January 23, 2007 | Sheet 32 of 60 |

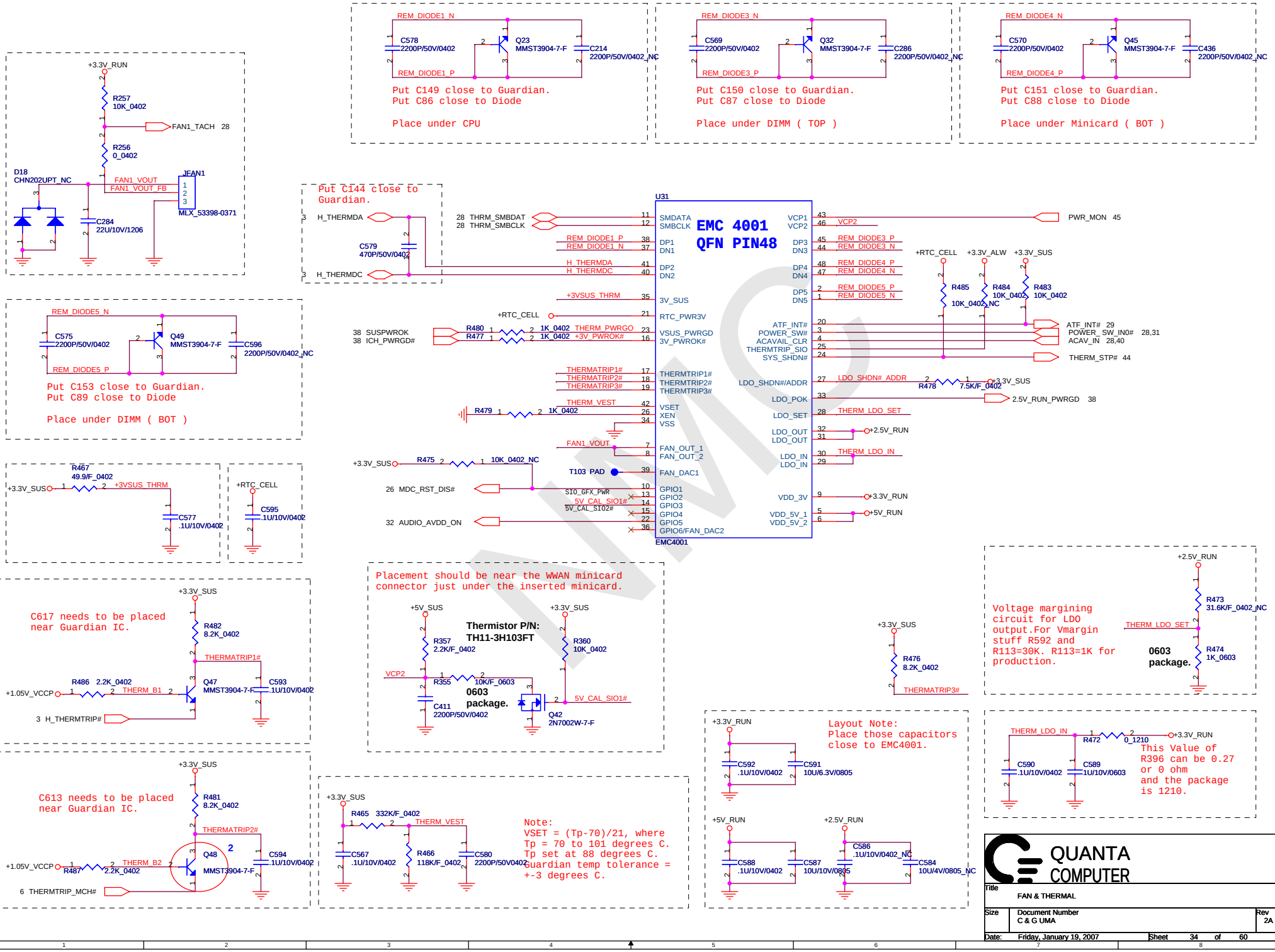


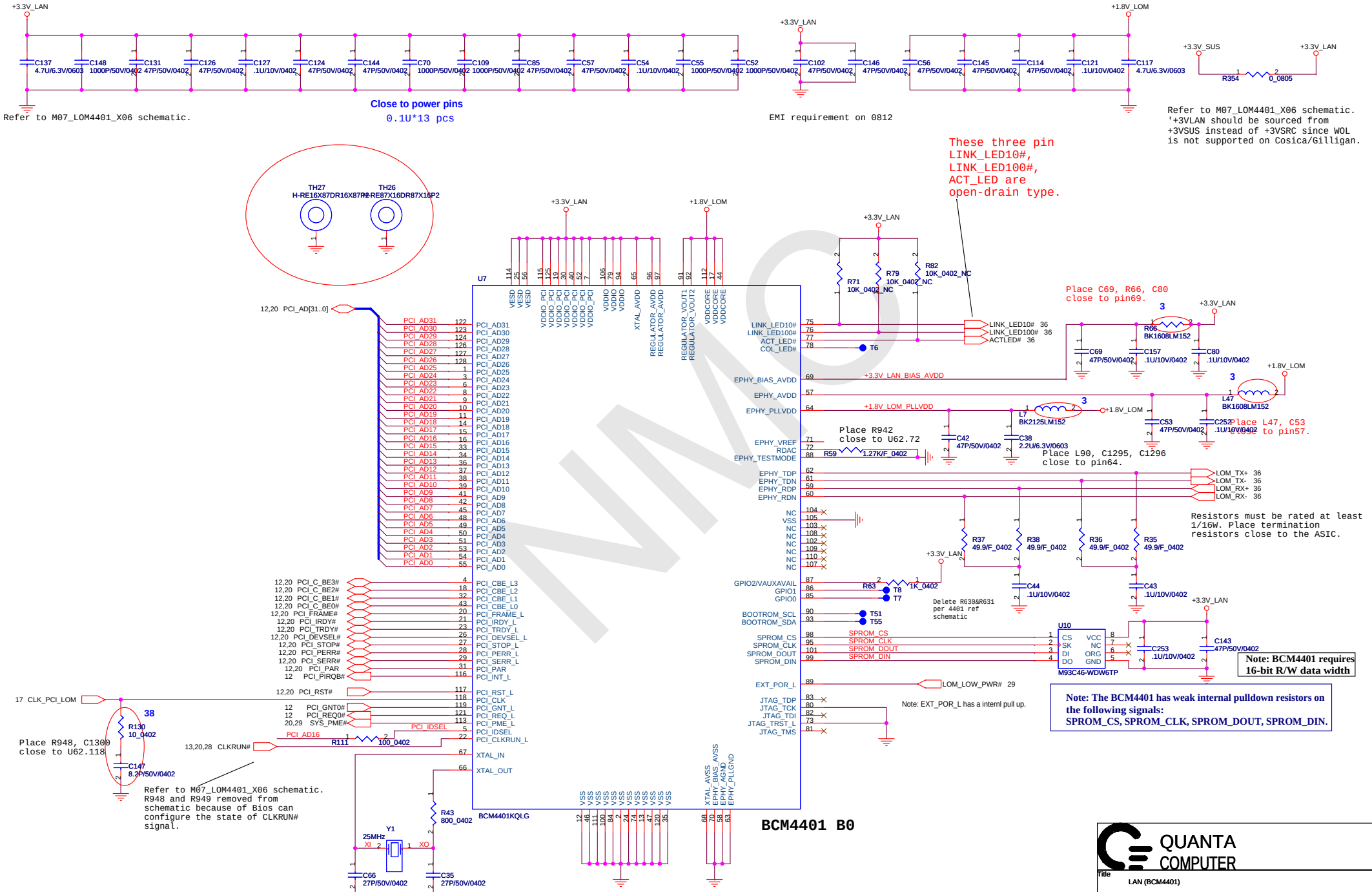

| | | |
|---|---|---|
| 1 | Diag Loop | Diag MB connector (Local Loop) |
| 2 | Mic Signal | |
| 3 | Mic Pwr | Mic Power 3.3v (run) |
| 4 | Mic clock | Mic Clock |
| 5 | GND | |
| 6 | USB Signal | |
| 7 | USB Pwr | Camera Power 3.3v (Camera) |
| 8 | USB Clock | |
| 9 | Diag CAM | Diag Camera/Inverter |
| 10 | Diag LVDS | Diag 5v return (LVDS connector) |
| 11 | Diag Loop | Diag MB connector (Local Loop) |

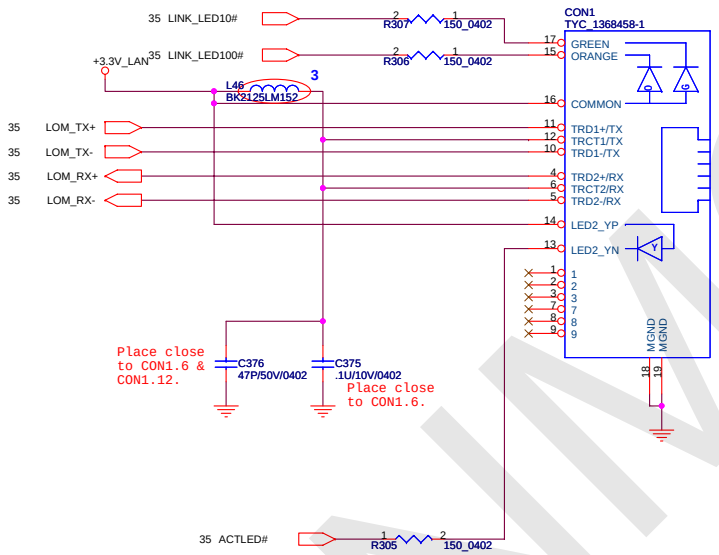


QUANTA COMPUTER

| | | | |
|---|---|---|---|
| Title | AUDIO&Sniffer&Camera CONN. | | |
| Size | Document Number C & G UMA | | Rev 2A |
| Date: | Tuesday, January 23, 2007 | Sheet 33 of 60 | |


REM_DIODE1_N
C578 2200P/50V/0402
Q23 MMST3904-7-F
C214 2200P/50V/0402_NC
REM_DIODE1_P
Put C149 close to Guardian.
Put C86 close to Diode
Place under CPU
REM_DIODE3_N
C569 2200P/50V/0402
Q32 MMST3904-7-F
C286 2200P/50V/0402_NC
REM_DIODE3_P
Put C150 close to Guardian.
Put C87 close to Diode
Place under DIMM ( TOP )
REM_DIODE4_N
C570 2200P/50V/0402
Q45 MMST3904-7-F
C436 2200P/50V/0402_NC
REM_DIODE4_P
Put C151 close to Guardian.
Put C88 close to Diode
Place under Minicard ( BOT )
+3.3V_RUN
R257 10K_0402
FAN1_TACH 28
R256 0_0402
D18 CHN202UPT_NC
FAN1_VOUT
FAN1_VOUT_FB
JFAN1
MLX_53398-0371
C284 22U/10V/1206
Put C144 close to Guardian.
H_THERMDA
C579 470P/50V/0402
H_THERMDC
U31
EMC 4001
QFN PIN48
28 THRM_SMBDAT
28 THRM_SMBCLK
SMDATA
SMBCLK
REM_DIODE1_P
REM_DIODE1_N
DP1
DN1
H_THERMDA
H_THERMDC
DP2
DN2
+3VSUS_THRM
3V_SUS
+RTC_CELL
RTC_PWR3V
38 SUSPWROK
38 ICH_PWRGD#
R480 1K_0402 THERM_PWRGD
R477 1K_0402 +3V_PWROK#
VSUS_PWRGD
3V_PWROK#
THERMTRIP1#
THERMTRIP2#
THERMTRIP3#
R479 1K_0402
VSET
XEN
VSS
FAN1_VOUT
FAN_OUT_1
FAN_OUT_2
+3.3V_SUS
R475 10K_0402_NC
T103 PAD
FAN_DAC1
26 MDC_RST_DIS#
SI0_GFX_PWR
5V_CAL_SIO1#
5V_CAL_SI02#
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6/FAN_DAC2
32 AUDIO_AVDD_ON
EMC4001
VCP1
VCP2
DP3
DN3
DP4
DN4
DP5
DN5
ATF_INT#
POWER_SW#
ACAVAIL_CLR
THERMTRIP_SIO
SYS_SHDN#
LDO_SHDN#/ADDR
LDO_POK
LDO_SET
LDO_OUT
LDO_OUT
LDO_IN
LDO_IN
VDD_3V
VDD_5V_1
VDD_5V_2
PWR_MON 45
VCP2
REM_DIODE3_P
REM_DIODE3_N
REM_DIODE4_P
REM_DIODE4_N
REM_DIODE5_P
REM_DIODE5_N
+RTC_CELL
+3.3V_ALW
+3.3V_SUS
R485 10K_0402_NC
R484 10K_0402
R483 10K_0402
ATF_INT# 29
POWER_SW_IN0# 28,31
ACAV_IN 28,40
THERM_STP# 44
LDO_SHDN# ADDR
R478 7.5K/F_0402
+3.3V_SUS
2.5V_RUN_PWRGD 38
THERM_LDO_SET
+2.5V_RUN
THERM_LDO_IN
+3.3V_RUN
REM_DIODE5_N
C575 2200P/50V/0402
Q49 MMST3904-7-F
C596 2200P/50V/0402_NC
REM_DIODE5_P
Put C153 close to Guardian.
Put C89 close to Diode
Place under DIMM ( BOT )
R467 49.9/F_0402
+3.3V_SUS
+3VSUS_THRM
C577 .1U/10V/0402
+RTC_CELL
C595 .1U/10V/0402
C617 needs to be placed near Guardian IC.
+3.3V_SUS
R482 8.2K_0402
THERMATRIP1#
R486 2.2K_0402
+1.05V_VCCP
THERM_B1
Q47 MMST3904-7-F
C593 .1U/10V/0402
3 H_THERMTRIP#
Placement should be near the WWAN minicard connector just under the inserted minicard.
+5V_SUS
Thermistor P/N:
TH11-3H103FT
+3.3V_SUS
R357 2.2K/F_0402
R360 10K_0402
VCP2
R355 10K/F_0603
0603 package.
C411 2200P/50V/0402
5V_CAL_SIO1#
Q42 2N7002W-7-F
R476 8.2K_0402
THERMATRIP3#
Voltage margining circuit for LDO output.For Vmargin stuff R592 and R113=30K. R113=1K for production.
+2.5V_RUN
R473 31.6K/F_0402_NC
THERM_LDO_SET
0603 package.
R474 1K_0603
C613 needs to be placed near Guardian IC.
+3.3V_SUS
R481 8.2K_0402
THERMATRIP2#
Q48
2
+1.05V_VCCP
R487 2.2K_0402
THERM_B2
MMST3904-7-F
C594 .1U/10V/0402
6 THERMTRIP_MCH#
+3.3V_SUS
R465 332K/F_0402
THERM_VEST
C567 .1U/10V/0402
R466 118K/F_0402
C580 2200P/50V/0402
Note:
VSET = (Tp-70)/21, where
Tp = 70 to 101 degrees C.
Tp set at 88 degrees C.
Guardian temp tolerance =
+-3 degrees C.
+3.3V_RUN
Layout Note:
Place those capacitors close to EMC4001.
C592 .1U/10V/0402
C591 10U/6.3V/0805
+5V_RUN
+2.5V_RUN
C588 .1U/10V/0402
C587 10U/10V/0805
C586 .1U/10V/0402_NC
C584 10U/4V/0805_NC
THERM_LDO_IN
R472 0_1210
+3.3V_RUN
C590 .1U/10V/0402
C589 1U/10V/0603
This Value of R396 can be 0.27 or 0 ohm and the package is 1210.
QUANTA COMPUTER
Title
FAN & THERMAL
Size
Document Number
C & G UMA
Rev
2A
Date:
Friday, January 19, 2007
Sheet
34
of
60


+3.3V_LAN
C137 4.7U/6.3V/0603
C148 1000P/50V/0402
C131 47P/50V/0402
C126 47P/50V/0402
C127 .1U/10V/0402
C124 47P/50V/0402
C144 47P/50V/0402
C70 1000P/50V/0402
C109 1000P/50V/0402
C85 47P/50V/0402
C57 47P/50V/0402
C54 .1U/10V/0402
C55 1000P/50V/0402
C52 1000P/50V/0402
Refer to M07_LOM4401_X06 schematic.
Close to power pins
0.1U*13 pcs
+3.3V_LAN
C102 47P/50V/0402
C146 47P/50V/0402
EMI requirement on 0812
+1.8V_LOM
C56 47P/50V/0402
C145 47P/50V/0402
C114 47P/50V/0402
C121 .1U/10V/0402
C117 4.7U/6.3V/0603
+3.3V_SUS
+3.3V_LAN
R354 0_0805
Refer to M07_LOM4401_X06 schematic.
'+3VLAN should be sourced from
+3VSUS instead of +3VSRC since WOL
is not supported on Cosica/Gilligan.
These three pin
LINK_LED10#,
LINK_LED100#,
ACT_LED are
open-drain type.
TH27 H-RE16X87DR16X87P2
TH26 H-RE87X16DR87X16P2
U7
BCM4401KQLG
12,20 PCI_AD[31..0]
PCI_AD31 122
PCI_AD30 123
PCI_AD29 124
PCI_AD28 126
PCI_AD27 127
PCI_AD26 128
PCI_AD25 1
PCI_AD24 3
PCI_AD23 6
PCI_AD22 8
PCI_AD21 9
PCI_AD20 10
PCI_AD19 11
PCI_AD18 14
PCI_AD17 15
PCI_AD16 16
PCI_AD15 33
PCI_AD14 34
PCI_AD13 36
PCI_AD12 37
PCI_AD11 38
PCI_AD10 39
PCI_AD9 41
PCI_AD8 42
PCI_AD7 45
PCI_AD6 48
PCI_AD5 49
PCI_AD4 50
PCI_AD3 51
PCI_AD2 53
PCI_AD1 54
PCI_AD0 55
12,20 PCI_C_BE3# 4
12,20 PCI_C_BE2# 18
12,20 PCI_C_BE1# 32
12,20 PCI_C_BE0# 43
12,20 PCI_FRAME# 20
12,20 PCI_IRDY# 21
12,20 PCI_TRDY# 23
12,20 PCI_DEVSEL# 26
12,20 PCI_STOP# 27
12,20 PCI_PERR# 28
12,20 PCI_SERR# 29
12,20 PCI_PAR 31
12 PCI_PIRQB# 116
12,20 PCI_RST# 117
12 PCI_GNT0# 118
12 PCI_REQ0# 119
20,29 SYS_PME# 121
PCI_IDSEL 113
PCI_AD16
R111 100_0402
13,20,28 CLKRUN# 22
17 CLK_PCI_LOM
R130 10_0402
C147 8.2P/50V/0402
Place R948, C1300
close to U62.118
Refer to M07_LOM4401_X06 schematic.
R948 and R949 removed from
schematic because of Bios can
configure the state of CLKRUN#
signal.
R43 800_0402
Y1 25MHz
C66 27P/50V/0402
C35 27P/50V/0402
XTAL_IN 67
XTAL_OUT 66
LINK_LED10# 75
LINK_LED100# 76
ACT_LED# 77
COL_LED# 78
R71 10K_0402_NC
R79 10K_0402_NC
R82 10K_0402_NC
LINK_LED10# 36
LINK_LED100# 36
ACTLED# 36
T6
Place C69, R66, C80
close to pin69.
R66 BK1608LM152
C69 47P/50V/0402
C157 .1U/10V/0402
C80 .1U/10V/0402
EPHY_BIAS_AVDD 69
+3.3V_LAN_BIAS_AVDD
EPHY_AVDD 57
EPHY_PLLVDD 64
+1.8V_LOM_PLLVDD
L47 BK1608LM152
L7 BK2125LM152
C53 47P/50V/0402
C252 .1U/10V/0402
Place L47, C53
close to pin57.
Place R942
close to U62.72
EPHY_VREF 71
RDAC 72
EPHY_TESTMODE 88
R59 1.27K/F_0402
C42 47P/50V/0402
C38 2.2U/6.3V/0603
Place L90, C1295, C1296
close to pin64.
EPHY_TDP 62
EPHY_TDN 61
EPHY_RDP 59
EPHY_RDN 60
LOM_TX+ 36
LOM_TX- 36
LOM_RX+ 36
LOM_RX- 36
NC 104
VSS 105
NC 103
NC 108
NC 102
NC 109
NC 110
NC 107
Resistors must be rated at least
1/16W. Place termination
resistors close to the ASIC.
R37 49.9/F_0402
R38 49.9/F_0402
R36 49.9/F_0402
R35 49.9/F_0402
C44 .1U/10V/0402
C43 .1U/10V/0402
GPIO2/VAUXAVAIL 87
GPIO1 86
GPIO0 85
R63 1K_0402
T8
T7
Delete R630&R631
per 4401 ref
schematic
BOOTROM_SCL 90
BOOTROM_SDA 93
T51
T55
SPROM_CS 98
SPROM_CLK 95
SPROM_DOUT 101
SPROM_DIN 99
U10
M93C46-WDW6TP
C253 .1U/10V/0402
C143 47P/50V/0402
Note: BCM4401 requires
16-bit R/W data width
EXT_POR_L 89
LOM_LOW_PWR# 29
Note: EXT_POR_L has a internl pull up.
JTAG_TDP 83
JTAG_TCK 80
JTAG_TDI 82
JTAG_TRST_L 73
JTAG_TMS 81
Note: The BCM4401 has weak internal pulldown resistors on
the following signals:
SPROM_CS, SPROM_CLK, SPROM_DOUT, SPROM_DIN.
BCM4401 B0
QUANTA COMPUTER
Title
LAN (BCM4401)
Size
Document Number
C & G UMA
Rev
2A
Date: Friday, January 19, 2007
Sheet 35 of 60

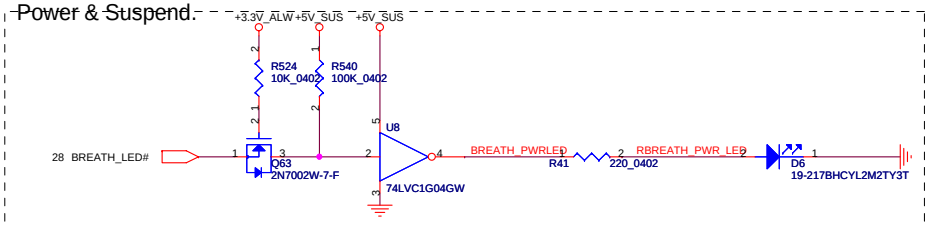




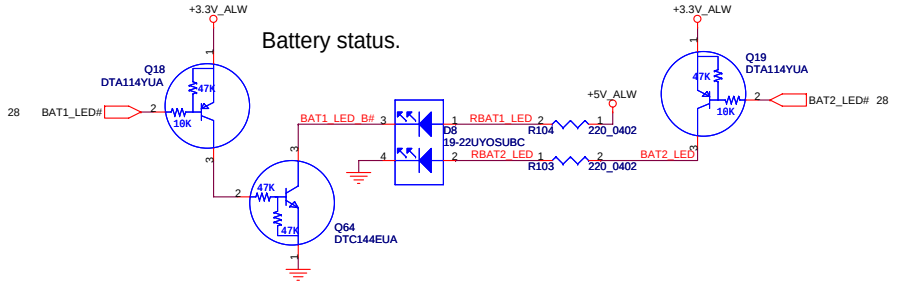

QUANTA COMPUTER

| | | |
|---|---|---|
| Title | LAN Jack | |
| Size | Document Number<br>C & G UMA | Rev<br>2A |
| Date: Friday, January 19, 2007 | Sheet 36 of 60 | |

## Power & Suspend.

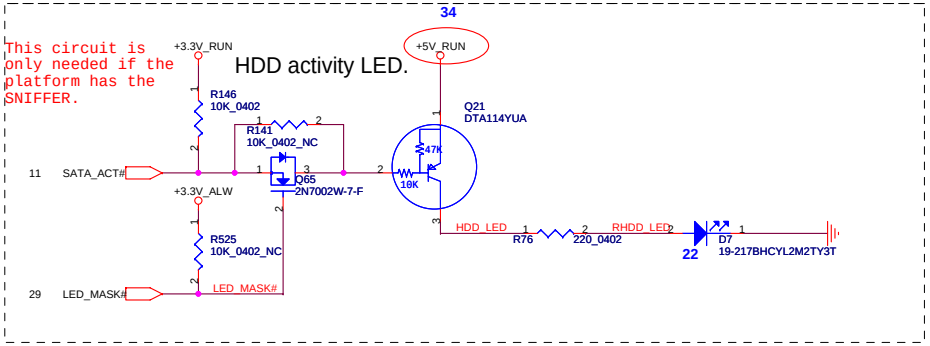



## Battery status.

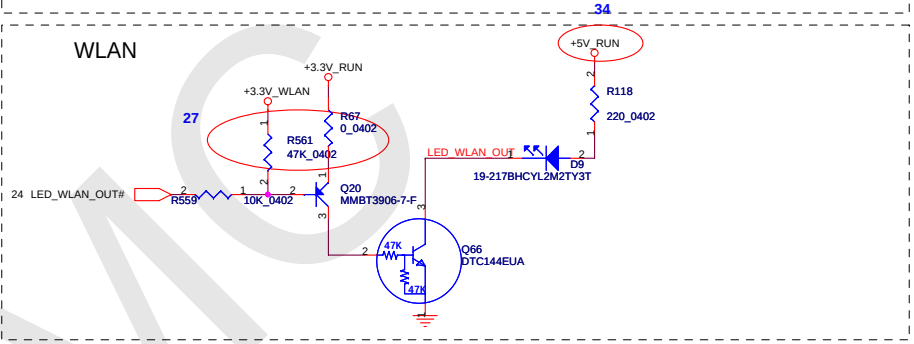



## HDD activity LED.

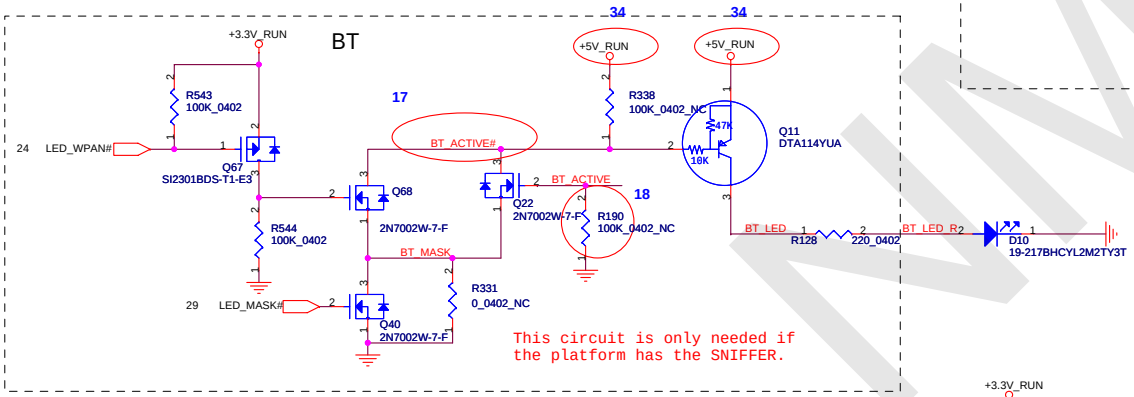
This circuit is only needed if the platform has the SNIFFER.

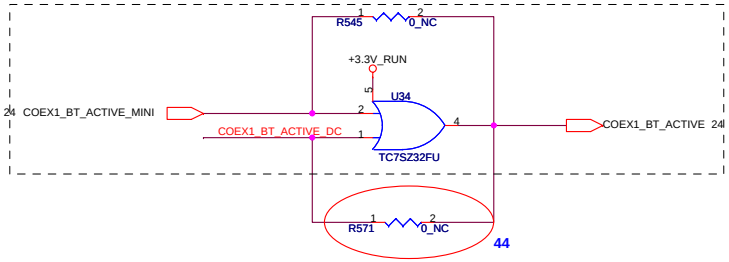


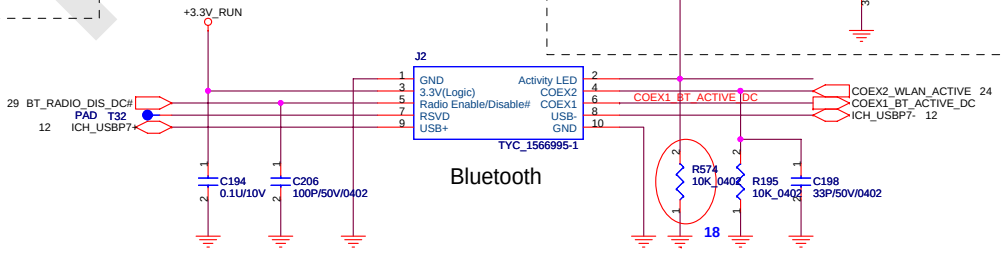

## WLAN

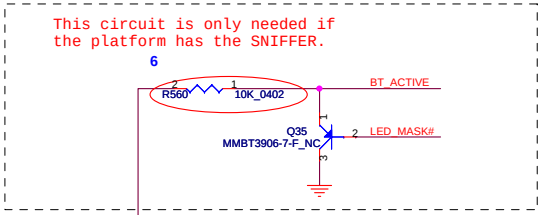



## BT



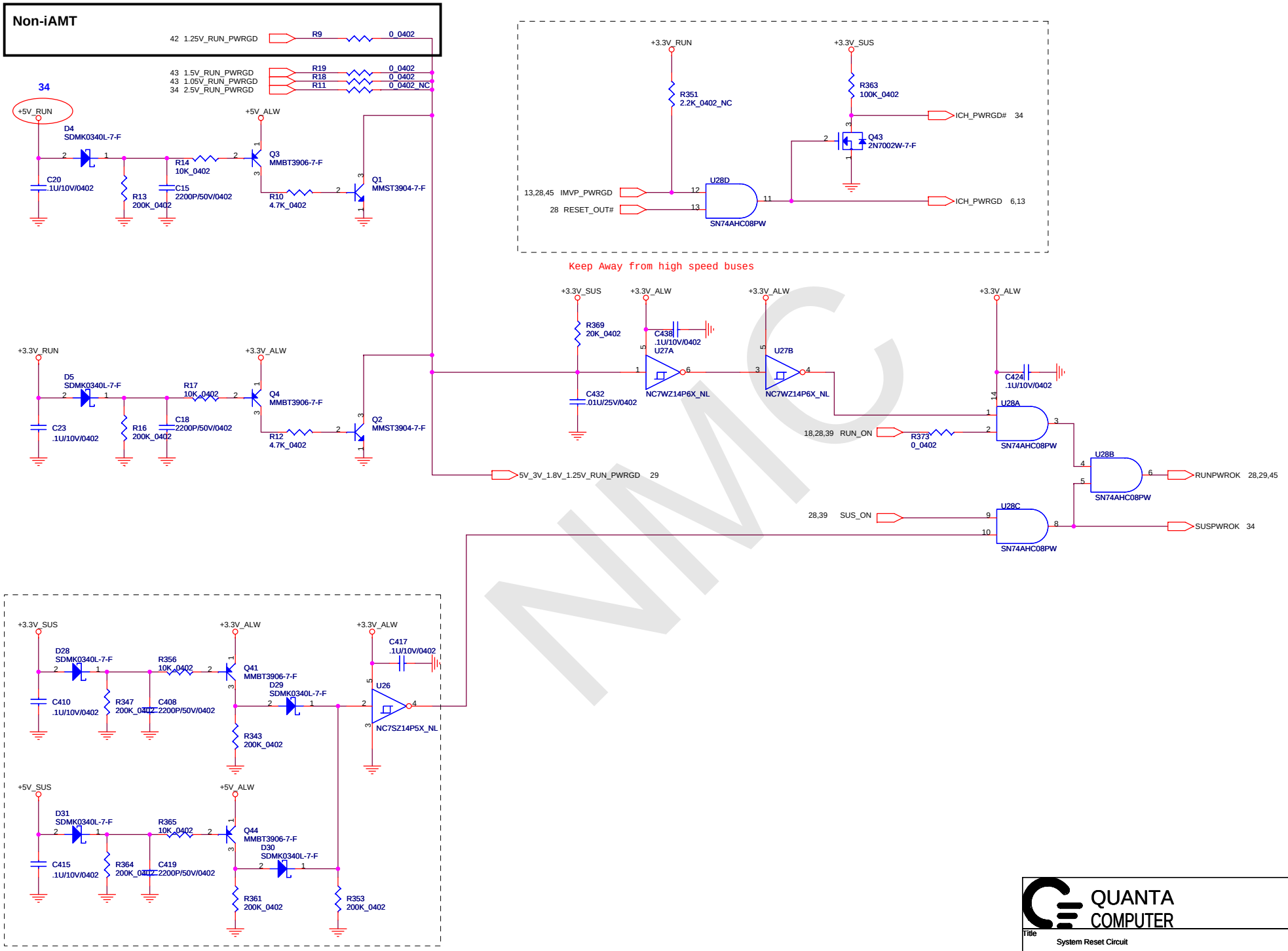



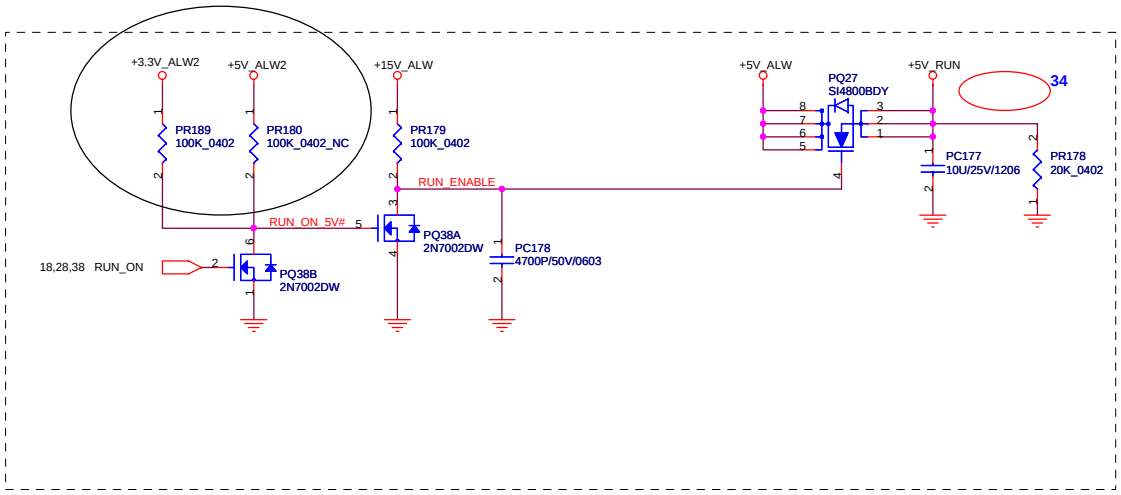



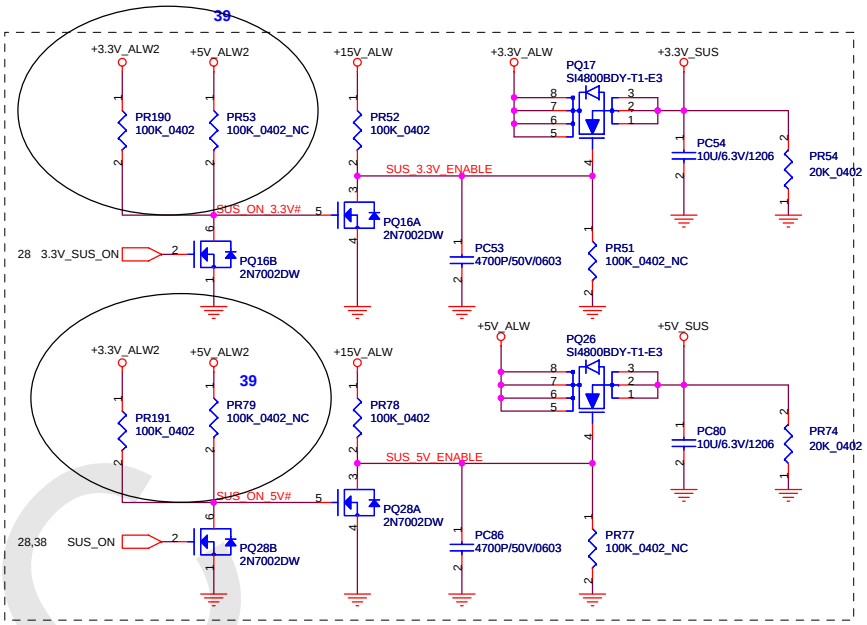


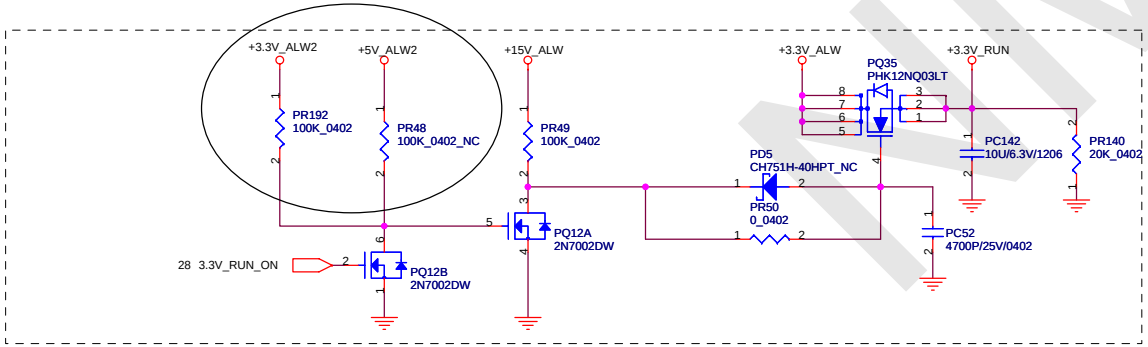

QUANTA COMPUTER

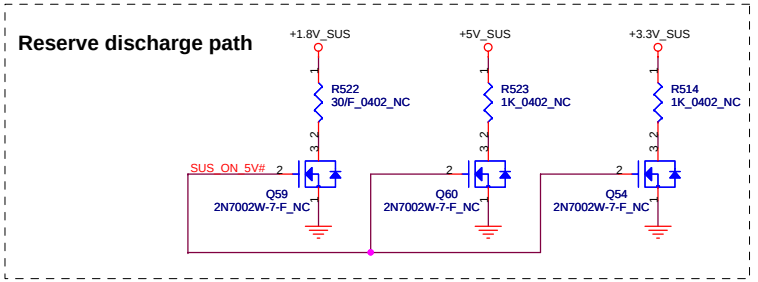
| | | |
|---|---|---|
| Title | SWITCH & LED | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Tuesday, January 23, 2007 | Sheet 37 of 60 | |

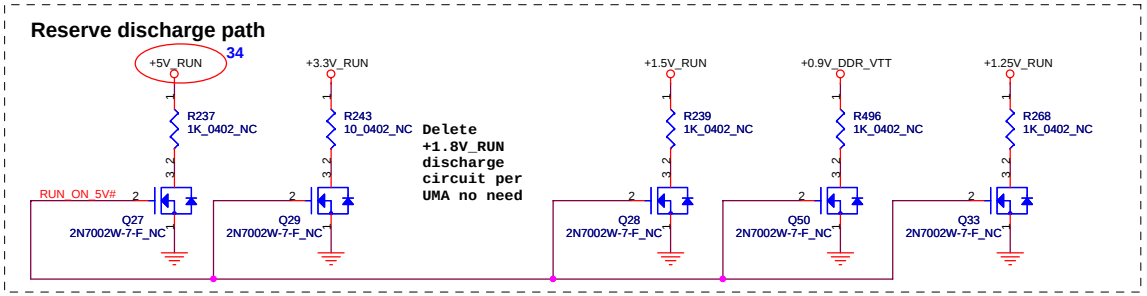

Non-iAMT
42 1.25V_RUN_PWRGD
R9
0_0402
43 1.5V_RUN_PWRGD
43 1.05V_RUN_PWRGD
34 2.5V_RUN_PWRGD
R19
R18
R11
0_0402
0_0402
0_0402_NC
34
+5V_RUN
D4
SDMK0340L-7-F
+5V_ALW
Q3
MMBT3906-7-F
Q1
MMST3904-7-F
C20
.1U/10V/0402
R13
200K_0402
C15
2200P/50V/0402
R14
10K_0402
R10
4.7K_0402
+3.3V_RUN
+3.3V_SUS
R351
2.2K_0402_NC
R363
100K_0402
ICH_PWRGD# 34
Q43
2N7002W-7-F
13,28,45 IMVP_PWRGD
28 RESET_OUT#
U28D
SN74AHC08PW
ICH_PWRGD 6,13
Keep Away from high speed buses
+3.3V_RUN
D5
SDMK0340L-7-F
+3.3V_ALW
Q4
MMBT3906-7-F
Q2
MMST3904-7-F
C23
.1U/10V/0402
R16
200K_0402
C18
2200P/50V/0402
R17
10K_0402
R12
4.7K_0402
+3.3V_SUS
+3.3V_ALW
R369
20K_0402
C438
.1U/10V/0402
U27A
NC7WZ14P6X_NL
C432
.01U/25V/0402
U27B
NC7WZ14P6X_NL
C424
.1U/10V/0402
U28A
SN74AHC08PW
18,28,39 RUN_ON
R373
0_0402
U28B
SN74AHC08PW
RUNPWROK 28,29,45
5V_3V_1.8V_1.25V_RUN_PWRGD 29
28,39 SUS_ON
U28C
SN74AHC08PW
SUSPWROK 34
+3.3V_SUS
+3.3V_ALW
+3.3V_ALW
D28
SDMK0340L-7-F
Q41
MMBT3906-7-F
D29
SDMK0340L-7-F
C417
.1U/10V/0402
U26
NC7SZ14P5X_NL
C410
.1U/10V/0402
R347
200K_0402
C408
2200P/50V/0402
R356
10K_0402
R343
200K_0402
+5V_SUS
+5V_ALW
D31
SDMK0340L-7-F
Q44
MMBT3906-7-F
D30
SDMK0340L-7-F
C415
.1U/10V/0402
R364
200K_0402
C419
2200P/50V/0402
R365
10K_0402
R361
200K_0402
R353
200K_0402
QUANTA COMPUTER
Title
System Reset Circuit
Size
Document Number
C & G UMA
Rev
2A
Date: Friday, January 19, 2007
Sheet 38 of 60



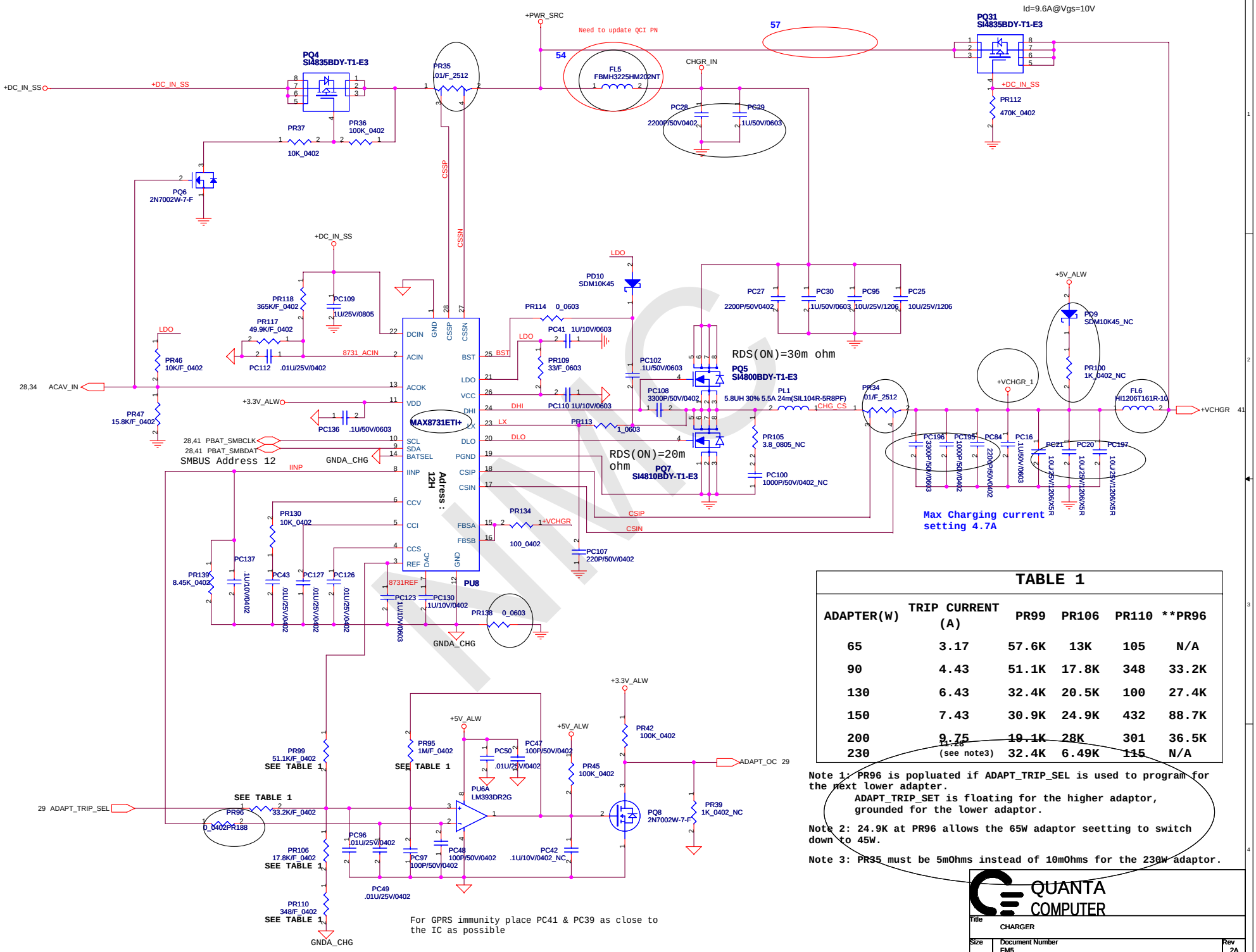




QUANTA COMPUTER

| | | |
|---|---|---|
| Title | RUN POWER SW | |
| Size | Document Number M-08 | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 39 of 60 | |




## TABLE 1

| ADAPTER(W) | TRIP CURRENT (A) | PR99 | PR106 | PR110 | **PR96 |
|---|---|---|---|---|---|
| 65 | 3.17 | 57.6K | 13K | 105 | N/A |
| 90 | 4.43 | 51.1K | 17.8K | 348 | 33.2K |
| 130 | 6.43 | 32.4K | 20.5K | 100 | 27.4K |
| 150 | 7.43 | 30.9K | 24.9K | 432 | 88.7K |
| 200 | 9.75 | 19.1K | 28K | 301 | 36.5K |
| 230 | (see note3) | 32.4K | 6.49K | 115 | N/A |

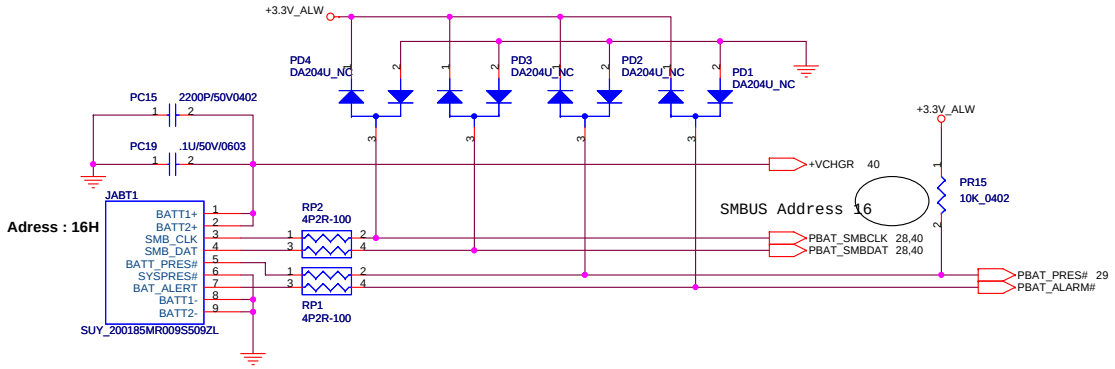
Note 1: PR96 is popluated if ADAPT_TRIP_SEL is used to program for the next lower adapter.
ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

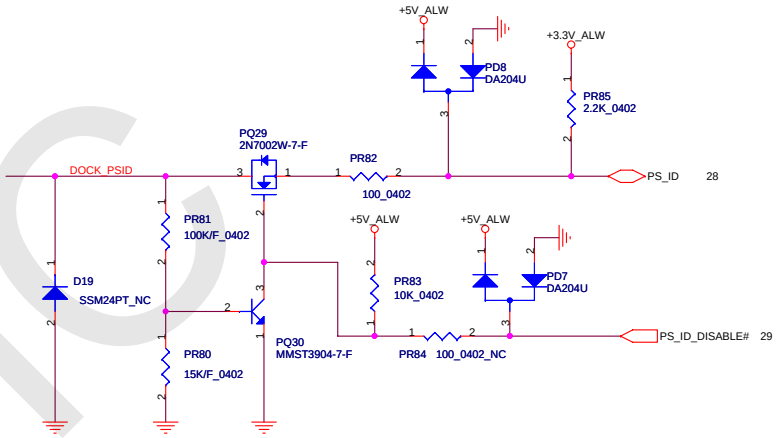
Note 2: 24.9K at PR96 allows the 65W adaptor seetting to switch down to 45W.

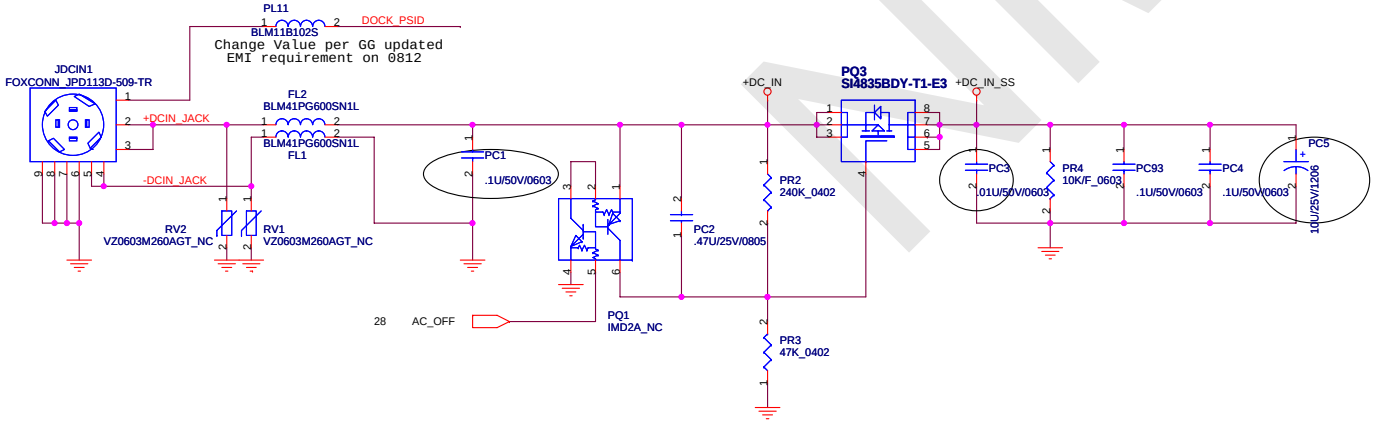
Note 3: PR35 must be 5mOhms instead of 10mOhms for the 230W adaptor.

QUANTA COMPUTER

| | | |
|---|---|---|
| Title | CHARGER | |
| Size | Document Number FM5 | Rev 2A |
| Date: Tuesday, January 23, 2007 | Sheet 40 of 60 | |

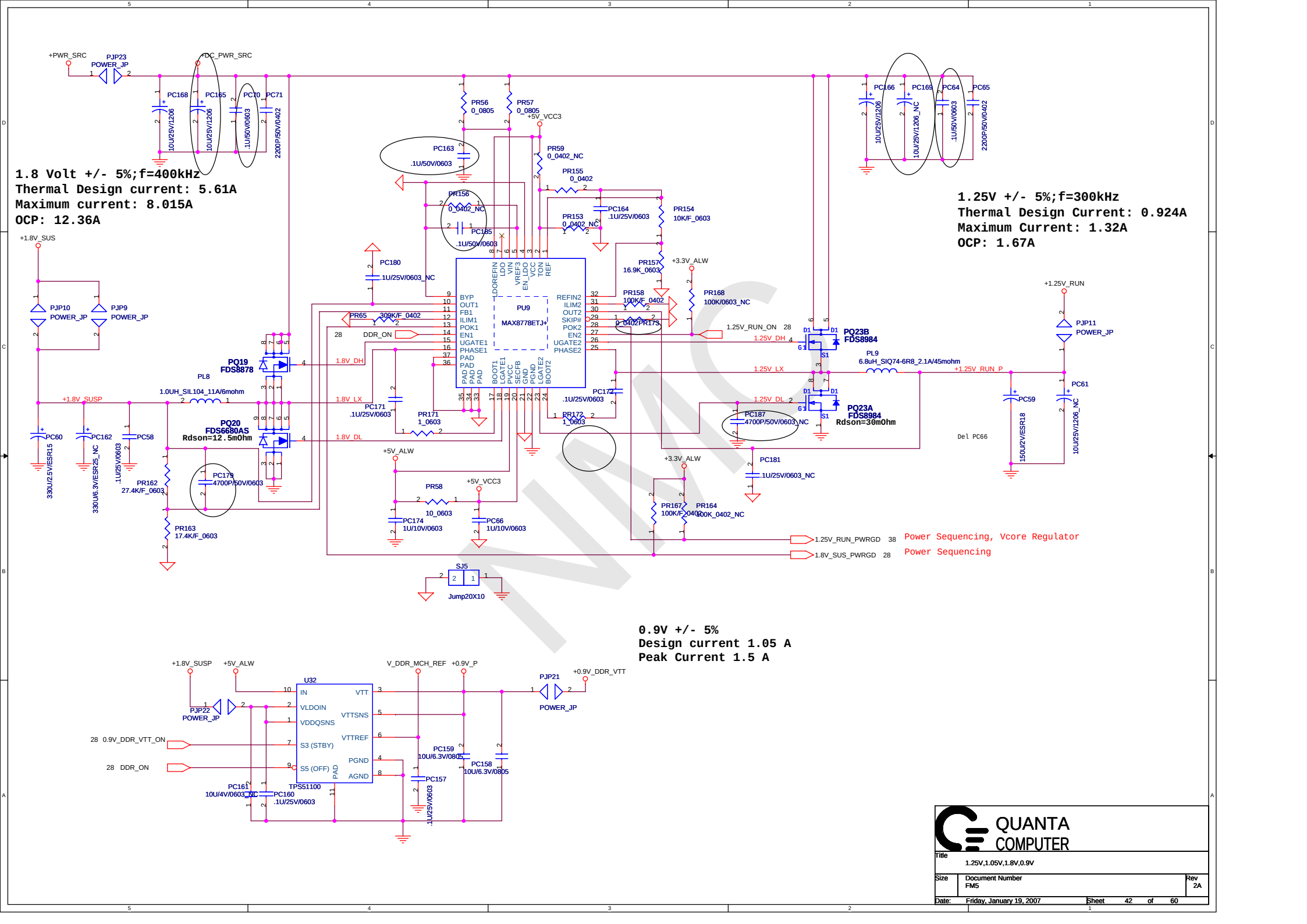




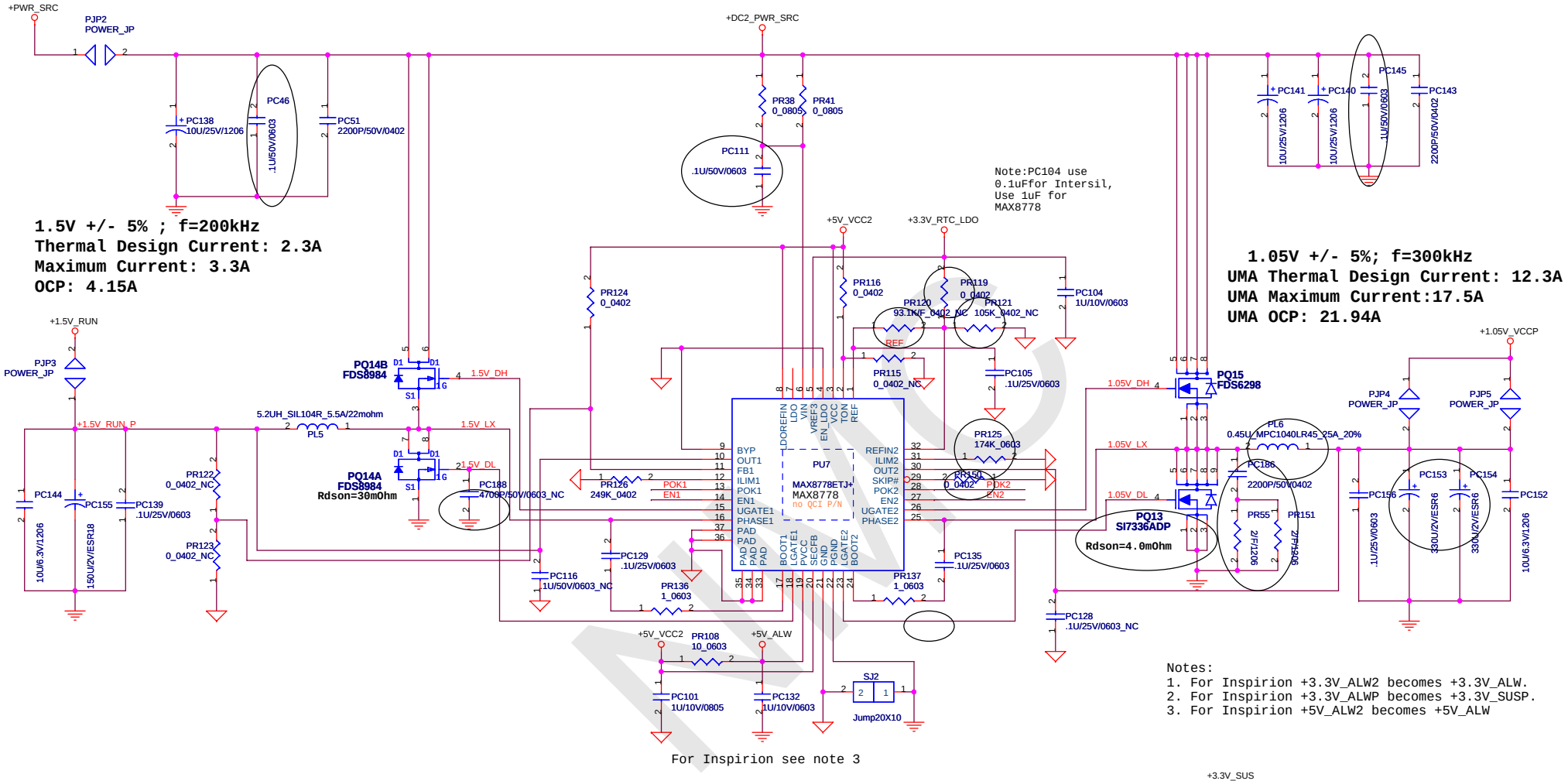

| | | |
|---|---|---|
| Title | DCIN,BATT CONNECTOR | |
| Size | Document Number FM5 | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 41 of 60 | |




| | | |
|---|---|---|
| Title | 1.25V,1.05V,1.8V,0.9V | |
| Size | Document Number FM5 | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 42 of 60 | |

QUANTA COMPUTER

# +1.5V_RUN /+1.05V_VCCP /+3.3V_ALW /+3.3_RTC_LDO




| | | |
|---|---|---|
| QUANTA COMPUTER | | |
| Title: 1.5V,1.05V | | |
| Size | Document Number: C & G UMA | Rev: 2A |
| Date: Friday, January 19, 2007 | Sheet 43 of 60 | |

# DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

Ton:OUT1/OUT2 Switching Frequency
VDD 200kHz/300kHz
OPEN (REF): 400kHz/300kHz
GND: 400kHz/500kHz

**3.3 Volt +/- 5%**
**Design Current:7.18A**
**Maximum current:10.25A**
**OCP: 12.36A**

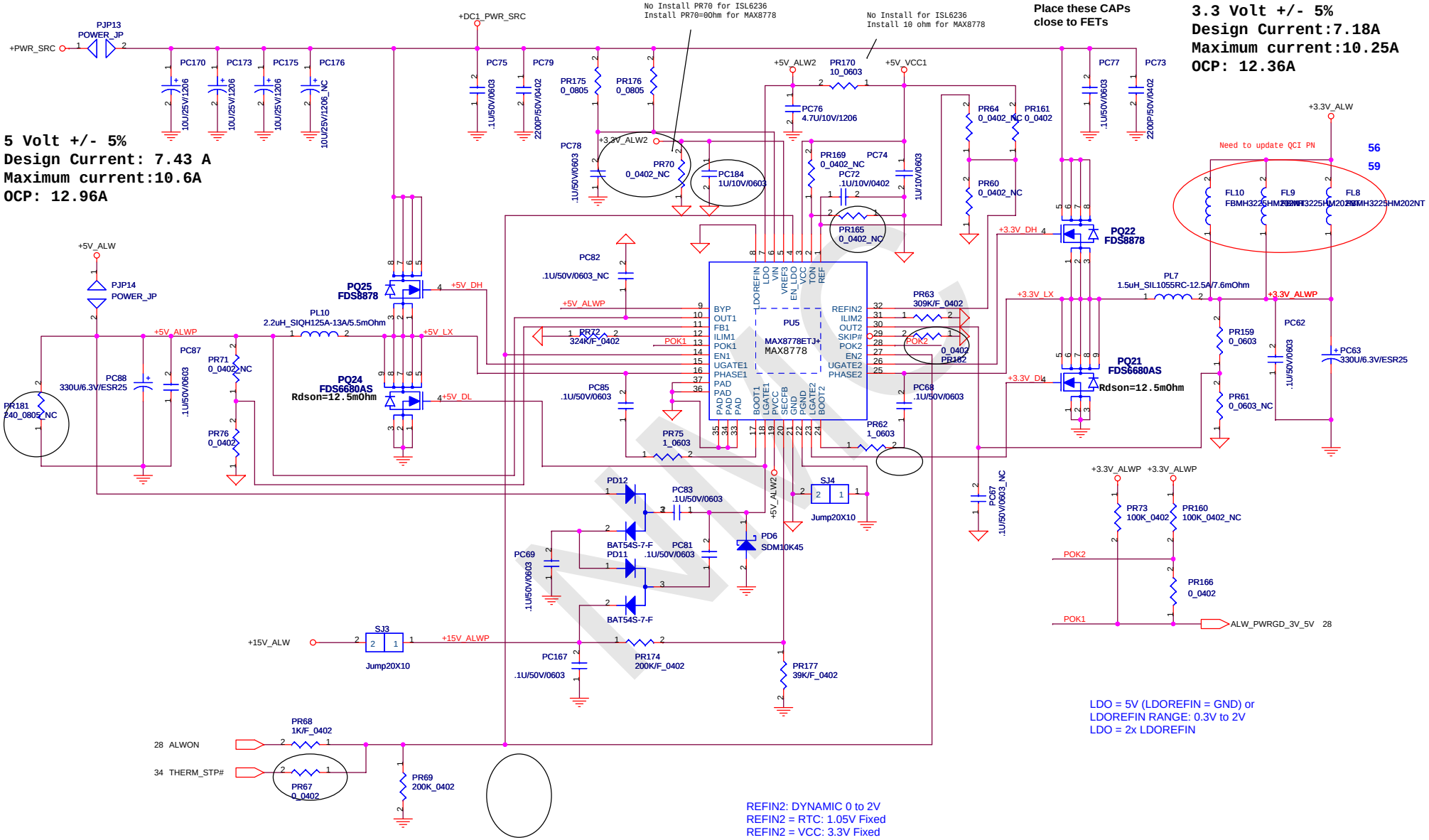
**5 Volt +/- 5%**
**Design Current: 7.43 A**
**Maximum current:10.6A**
**OCP: 12.96A**

Place these CAPs close to FETs

Place these CAPs close to FETs

No Install PR70 for ISL6236
Install PR70=0Ohm for MAX8778

No Install for ISL6236
Install 10 ohm for MAX8778



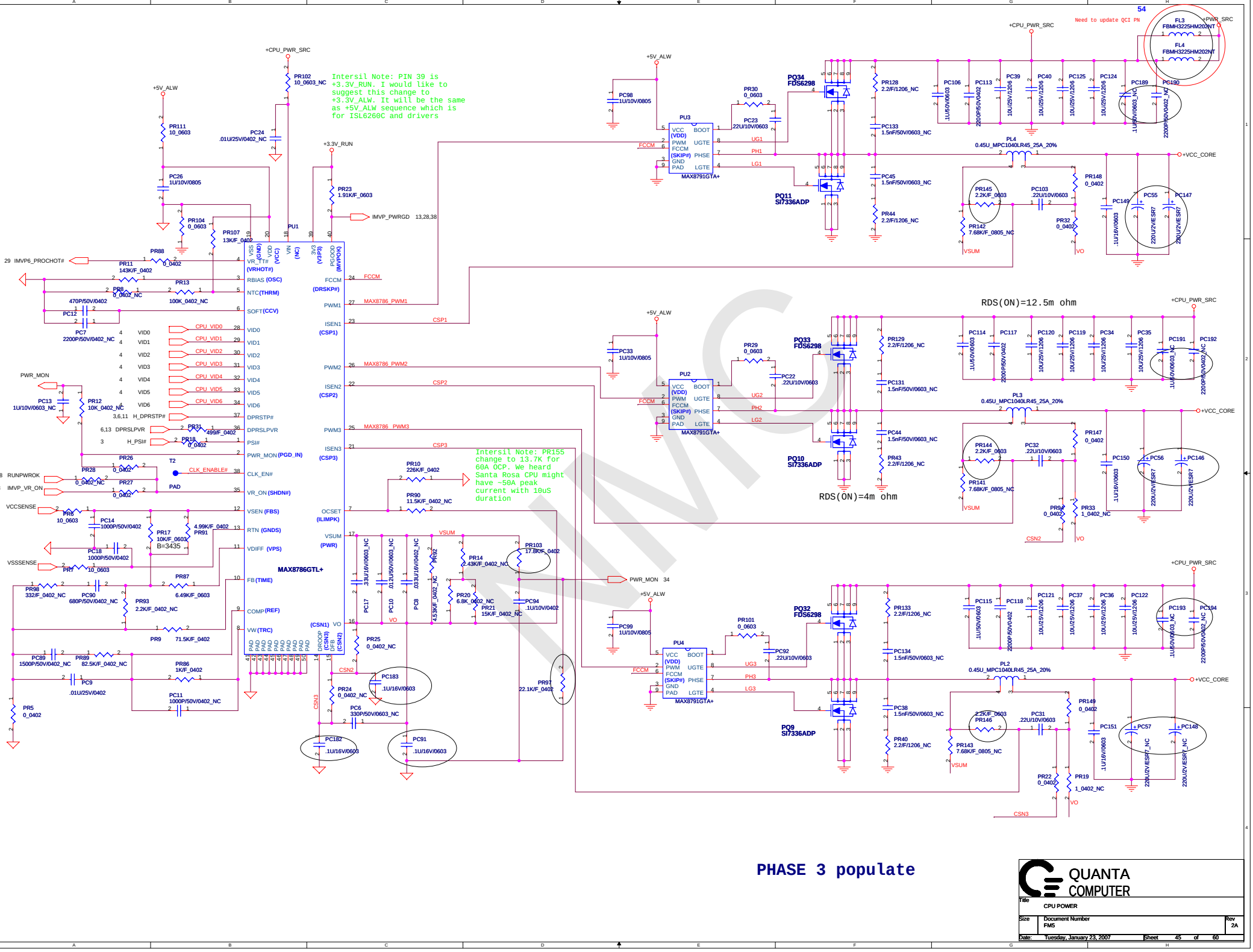

LDO = 5V (LDOREFIN = GND) or
LDOREFIN RANGE: 0.3V to 2V
LDO = 2x LDOREFIN

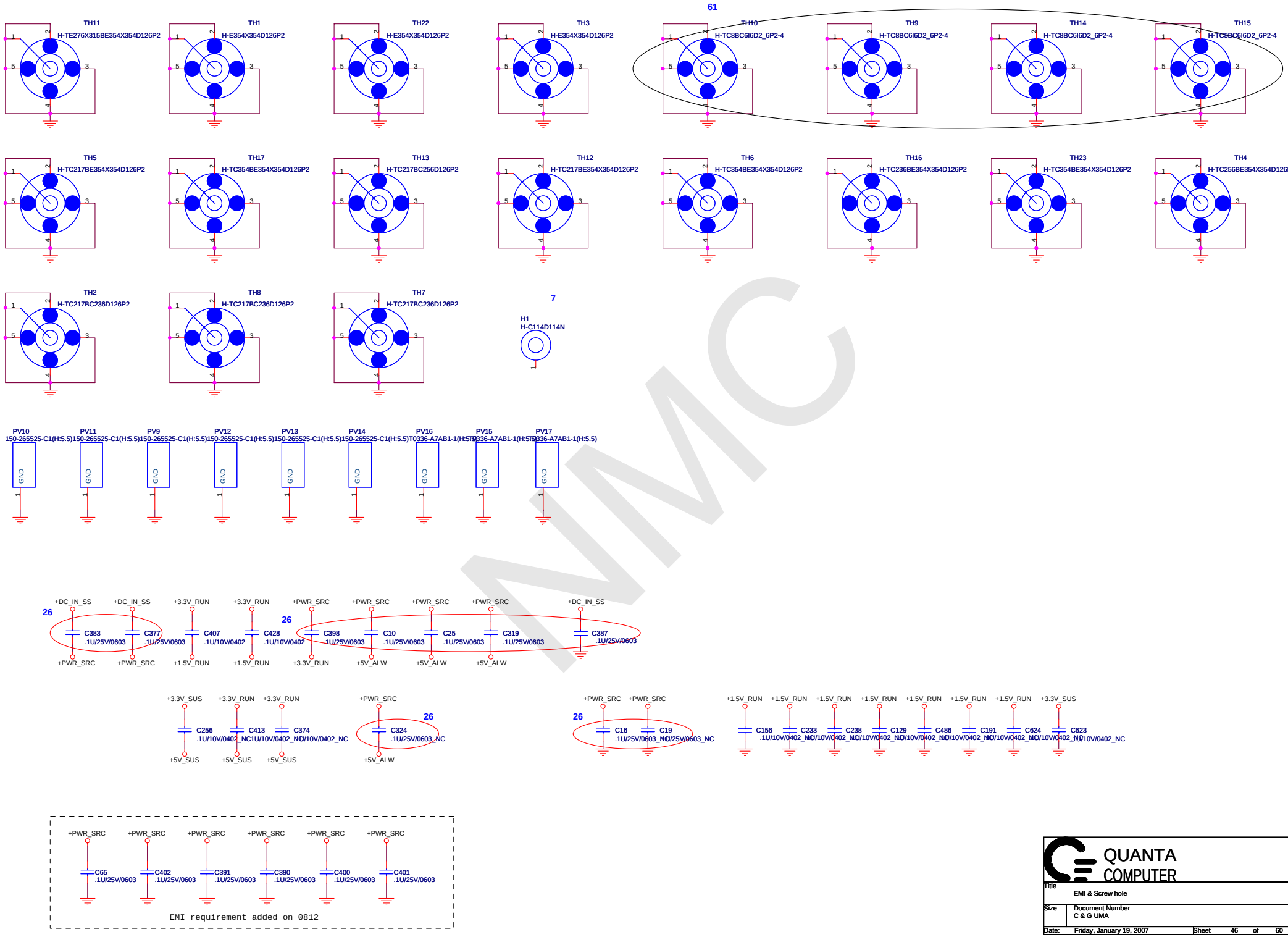
REFIN2: DYNAMIC 0 to 2V
REFIN2 = RTC: 1.05V Fixed
REFIN2 = VCC: 3.3V Fixed



QUANTA COMPUTER

| | | |
|---|---|---|
| Title | 3VALW,5V,3V, power on | |
| Size | Document Number FM5 | Rev 2A |
| Date: Tuesday, January 23, 2007 | Sheet 44 of 60 | |


54
Need to update QCI PN
+CPU_PWR_SRC
+PWR_SRC
FL3 FBMH3225HM202NT
FL4 FBMH3225HM202NT
+5V_ALW
+3.3V_RUN
Intersil Note: PIN 39 is +3.3V_RUN. I would like to suggest this change to +3.3V_ALW. It will be the same as +5V_ALW sequence which is for ISL6260C and drivers
PU1
MAX8786GTL+
PU3
PU2
PU4
MAX8791GTA+
PQ34 FDS6298
PQ11 SI7336ADP
PQ33 FDS6298
PQ10 SI7336ADP
PQ32 FDS6298
PQ9 SI7336ADP
PL4 0.45U_MPC1040LR45_25A_20%
PL3 0.45U_MPC1040LR45_25A_20%
PL2 0.45U_MPC1040LR45_25A_20%
+VCC_CORE
RDS(ON)=12.5m ohm
RDS(ON)=4m ohm
Intersil Note: PR155 change to 13.7K for 60A OCP. We heard Santa Rosa CPU might have ~50A peak current with 10uS duration
IMVP_PWRGD 13,28,38
PWR_MON
RUNPWROK
IMVP_VR_ON
IMVP6_PROCHOT#
VCCSENSE
VSSSENSE
VSUM
VO
CSN2
CSN3
PHASE 3 populate
QUANTA COMPUTER
Title CPU POWER
Size Document Number FM5 Rev 2A
Date: Tuesday, January 23, 2007 Sheet 45 of 60






QUANTA COMPUTER

| | | |
|---|---|---|
| Title | EMI & Screw hole | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 46 of 60 | |

## POWER STATES

| State \ Signal | SLP S3# | SLP S4# | SLP S5# | S4 STATE# | SLP M# | ALWAYS PLANE | M PLANE | SUS PLANE | RUN PLANE | CLOCKS |
|---|---|---|---|---|---|---|---|---|---|---|
| S0 (Full ON) / M0 | HIGH | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON | ON |
| S3 (Suspend to RAM) / M1 | LOW | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | OFF | ON |
| S4 (Suspend to DISK) / M1 | LOW | HIGH | HIGH | LOW | HIGH | ON | ON | ON | OFF | ON |
| S5 (SOFT OFF) / M1 | LOW | HIGH | LOW | LOW | HIGH | ON | ON | ON | OFF | ON |
| S3 (Suspend to RAM) / M-OFF | LOW | HIGH | HIGH | HIGH | LOW | ON | OFF | ON | OFF | OFF |
| S4 (Suspend to DISK) / M-OFF | LOW | LOW | HIGH | LOW | LOW | ON | OFF | OFF | OFF | OFF |
| S5 (SOFT OFF) / M-OFF | LOW | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF | OFF |

## PM TABLE

| State \ power plane | +3.3V_ALW<br>+3.3V_RTC_LDO<br>+3.3V_WLAN<br>+5V_ALW<br>+15V_ALW | +1.8V_SUS<br>+1.8V_LOM<br>+3.3V_LAN<br>+3.3V_SUS<br>+5V_SUS | +0.9V_DDR_VTT<br>+1.05V_VCCP<br>+1.25V_RUN<br>+1.5V_CARD<br>+1.5V_RUN<br>+3.3V_CARD<br>+3.3V_CARDAUX<br>+3.3V_R5C832<br>+3.3V_RUN | +3.3V_RUN_CARD<br>+2.5V_RUN<br>+5V_MOD<br>+5V_RUN<br>+5V_SPK_AMP<br>+CPU_PWR_SRC<br>+VCC_CORE<br>+VDDA | +DC_IN<br>+DC_IN_SS<br>+PWR_SRC<br>+RTC_CELL |
|---|---|---|---|---|---|
| S0 | ON | ON | ON | | ON |
| S3 | ON | ON | OFF | | ON |
| S5 S4/AC | ON | OFF | OFF | | ON |
| S5 S4/AC don't exist | OFF | OFF | OFF | | ON |

## PCI TABLE

| PCI DEVICE | IDSEL | REQ#/GNT# | PIRQ |
|---|---|---|---|
| BCM4401B | AD16 | REQ#0 / GNT#0 | PIRQB |
| R5C833 | AD17 | REQ#1 / GNT#1 | PIRQC: Card reader<br>PIEQD: 1394 |

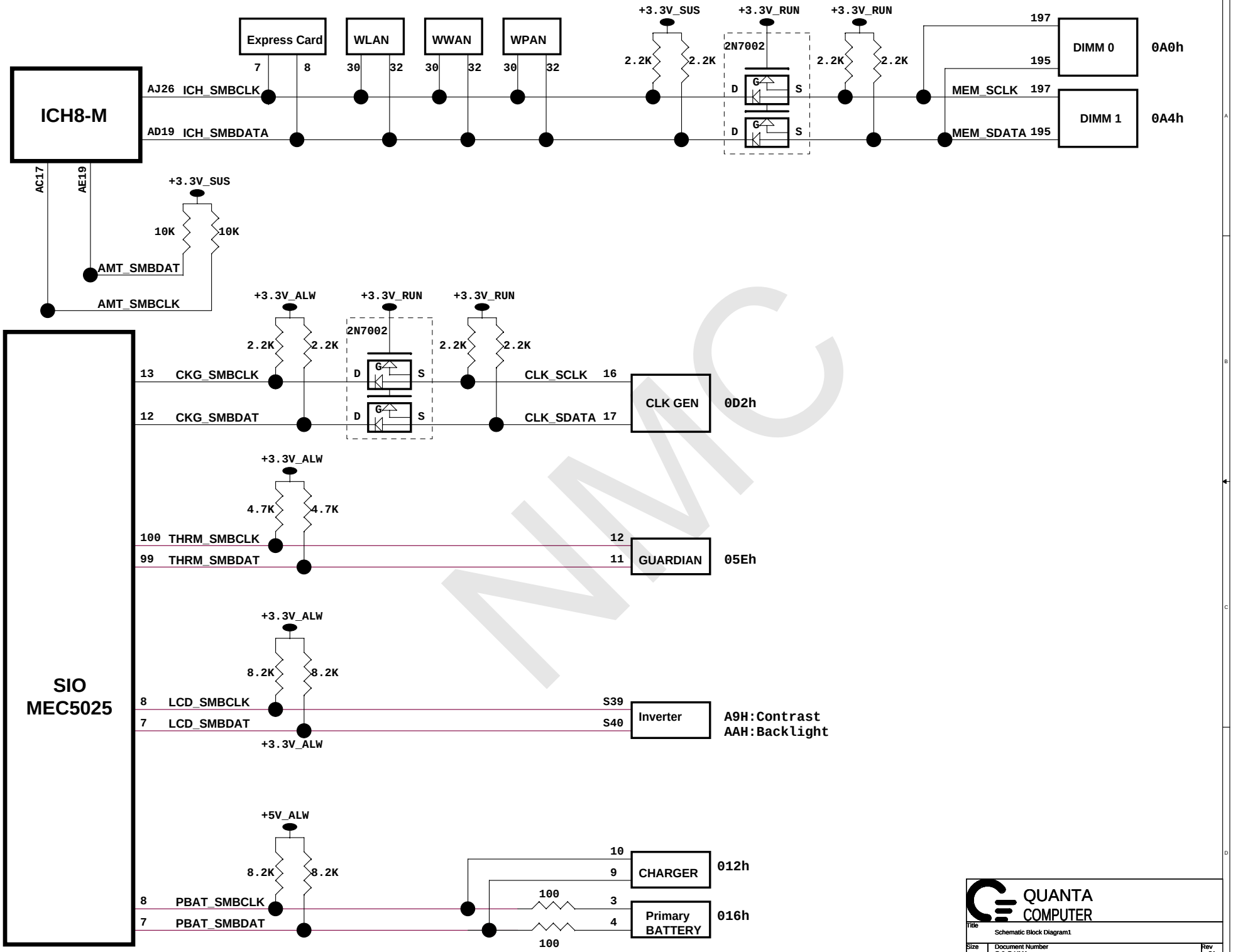
| | USB PORT# | DESTINATION |
|---|---|---|
| ICH8-M | 0 | Right Top |
| | 1 | Right Bottom |
| | 2 | Side TOP |
| | 3 | Side Bottom |
| | 4 | Ext. USB TOP |
| | 5 | DIgital Camera |
| | 6 | Express Card |
| | 7 | WPAN/Bluetooth |
| | 8 | Ext. USB Bottom |
| | 9 | WWAN |
| ECE 5011 | 1 | None |
| | 2 | None |
| | 3 | None |
| | 4 | None |

| PCI EXPRESS | DESTINATION |
|---|---|
| Lane 1 | MINI CARD-1 WWAN |
| Lane 2 | MINI CARD-2 WLAN |
| Lane 3 | MINI CARD-3 WPAN |
| Lane 4 | Express Card |
| Lane 5 | None |
| Lane 6 | None |



QUANTA COMPUTER

| | | |
|---|---|---|
| Title | Schematic Block Diagram1 | |
| Size | Document Number<br>C & G UMA | Rev<br>2A |
| Date: Friday, January 19, 2007 | Sheet 47 of 60 | |






QUANTA COMPUTER

| | | |
|---|---|---|
| Title | Schematic Block Diagram1 | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 48 of 60 | |

| Model | Item | Page | Date | Rev. | Description |
|---|---|---|---|---|---|
| C & G UMA | 1 | P.3 | 0619 | 1A | Update no populated ITP schmatic per ref. Intel checklist V:1.201a. And added ITP to XDP implement txt. |
| | 2 | P.23,25,46 | 0620 | 1A | Update Screw hole per ME update. |
| | 3 | P.17 | 0620 | 1A | Update SRC CLK per followed Discrete schematic changed. |
| | 4 | P.12 | 0620 | 1A | Swap RP21.2, RP21.3, RP52.3, RP52.4, RP52.6 net for layout requirement. |
| | 5 | P.15,16 | 0620 | 1A | Swap RP14.2, RP14.4, JDIM2.136, JDIM2.137, JDIM2.141, JDIM2.143 per layout requirement. |
| | 6 | P.13,28 | 0620 | 1A | Change USIO2.28 net name from SIO_S4_STATE# to TP_DET# and delete U25.AH27. |
| | 7 | P.18 | 0620 | 1A | Update +LCDVCC circuit per ref. CD_Diag_0619.ppt file. |
| | 8 | P.33 | 0620 | 1A | Added AUX_LCD_CBL_DET#, INVERTER_CBL_DET#, LCD_CBL_DET Pull-up resistor. |
| | 9 | P.13,28 | 0620 | 1A | Delete WOL_EN of U25.AG19 and R571. Changed USIO2.94 net-name from WOL_EN to EC_ENVDD per ref BITS WI74741. |
| | 10 | P.32 | 0620 | 1A | Update JSPK1 and added SPK DET. PU Resistor. |
| | 11 | P.28 | 0620 | 1A | Delete R479 per ref BITS WI75517 |
| | 12 | P.24,28 | 0620 | 1A | Added WoWL power SW circuit per ref BITS WI74552. |
| | 13 | P.6 | 0620 | 1A | Delete all of NC pins connected to test pad per ref. BITS issue WI75504. |
| | 14 | P.6 | 0620 | 1A | Populate R1, R5, R9 per implement ITP function. |
| | 15 | P.31 | 0621 | 1A | DAT_TP_SIO & CLK_TP_SIO pull up to +3.3V_ALW, Added PU to +3.3V_ALW for TP_DET#. |
| | 16 | P.33 | 0621 | 1A | Correction LCD_CBL_DET pull up circuit. |
| | 17 | P.11,30 | 0621 | 1A | Change RTC_BAT_DET# PU resistor from 10K to 100K and moved to P.30 |
| | 18 | P.11,32 | 0621 | 1A | Change SPEAKER_DET# PU resistor from 10K to 100K and moved to P.32 |
| | 19 | P.24,25 | 0621 | 1A | Change Mini card DET. PU resistor from 10K to 100K. |
| | 20 | P.29 | 0621 | 1A | Delete PBAT_ALERT# per M08 GPIO table removed. |
| | 21 | P.39-45 | 0621 | 1A | Update power schematic per ref power team updated schematic. |
| | 22 | P.22 | 0622 | 1A | Per TaiSol suggest, the CD2/WP2 is a dynamic pin; CD1 is a fixed pin, CD2 will touch CD1 when SD card insert into connecter |
| | 23 | P.22 | 0622 | 1A | After discussion withe Taisol's FAE, pin-1 must connect to GND |
| | 24 | P.20 | 0622 | 1A | Ricoh check result: UDIO3 &UDIO4 apply NC required. Removed pull high resistor from UDIO3 and UDIO4. |
| | 25 | P.20 | 0622 | 1A | Ricoh check result: INTA# and INTB# interrupt line hange required. Please apply PCI_PIRQC# interrupt line for INTA#, PCI_PIRQD# interrupt line for INTB# |
| | 26 | P.21 | 0622 | 1A | Ricoh check result: Shield GND for XTAL for XO/XI Please apply shield GND for XTAL for XO/XI to reduce external noise for XTAL. |
| | 27 | P.12,20 | 0627 | 1A | Changed REQ2/GNT2 to REQ1/GNT1 and swap PIRQD/PIRQC for C&G card reader+1394. |
| | 28 | P.12,35 | 0627 | 1A | Changed REQ3/GNT3 to REQ0/GNT0 and change PIRQB for C&G LOM. |
| | 29 | P.35 | 0629 | 1A | L90 changed to BLM11A601. |
| | 30 | P.24,25 | 0629 | 1A | Update PCI-E chennals. Update WPAN LED signal circuit. |
| | 31 | P.23 | 0629 | 1A | Delete SATA power2 for ref. Discrete schematic. |
| | 32 | P.9 | 0629 | 1A | De-populate C1 per Intel review update. |
| | 33 | P.13 | 0629 | 1A | Delete ICH_CL_RST1# per Intel review.Delete AMT_SMBCLK & AMTSMBDAT per not support AMT function. |
| | 34 | P.39 | 0703 | 1A | Added ALW power transfer circuit per power changed. |
| | 35 | P.25 | 0703 | 1A | Change ESD2 from CDA6C05GTH to SRV05-4 per refer Dawson schematic update. |
| | 36 | P.40-45 | 0704 | 1A | Power update schematic. |
| | 37 | P.29 | 0705 | 1A | The net name of IMVP6_PROCHOT# is for pin32 not for pin33. So, I change the the net name of IMVP6_PROCHOT# from pin 33 to pin 32. |
| | 38 | P.27 | 0707 | 1A | Ref Discrete schematic, changed the pin define of JCAMERA2 between pin 5 & pin6 |



QUANTA COMPUTER

| | | | |
|---|---|---|---|
| Title | EMI & Screw hole | | |
| Size | Document Number C & G UMA | | Rev 2A |
| Date: | Friday, January 19, 2007 | Sheet 49 of 60 | |

| Model | Item | Page | Date | Rev. | Description |
|---|---|---|---|---|---|
| *C & G UMA* | 39 | P.26 | 0707 | 1A | Ref Discrete schematic, Move R24 and C25 to DB. |
| | 40 | P.26 | 0707 | 1A | Ref Discrete schematic, Move R317 and C405 to DB. |
| | 41 | P.26 | 0707 | 1A | Ref Discrete schematic, Move C293 and C396 to DB. |
| | 42 | P.27 | 0707 | 1A | Ref Discrete schematic, Add a fuse on U64 |
| | 43 | P.27 | 0707 | 1A | Ref Discrete schematic, Add a fuse on U67 |
| | 44 | P.32 | 0707 | 1A | Ref Discrete schematic, added a net name SPEAKER_DET# on U21.4. Delete off-page connection from JSPK1. |
| | 45 | P.11 | 0707 | 1A | Ref Discrete schematic, deleted off-page connection from U25.AE10 |
| | 46 | P.32 | 0707 | 1A | Ref Discrete schematic, added an offpage connection name SPDIF_SHDN on U21.30. |
| | 47 | P.37 | 0707 | 1A | Ref Discrete schematic, changed LED schematic of BT based on Discrete schemaitc. Remove U72, R23, D6 and Q7. Add Q?, R? and D? on page 37. |
| | 48 | P.29 | 0707 | 1A | Ref Discrete schematic, USIO.98 pull up to +3.3V_ALW through a 10k ohm. |
| | 49 | P.29 | 0707 | 1A | Ref Discrete schematic, USIO.66 pull up to +3.3V_ALW through a 10k ohm. |
| | 50 | P.29 | 0707 | 1A | Ref Discrete schematic, USIO.76 pull up to +3.3V_ALW through a 10k ohm. |
| | 51 | P.29 | 0707 | 1A | Ref Discrete schematic, USIO.29 pull up to +3.3V_ALW through a 10k ohm. |
| | 52 | P.29 | 0707 | 1A | Ref Discrete schematic, USIO.28 pull up to +3.3V_ALW through a 100k ohm. |
| | 53 | P.21 | 0710 | 1A | Per vendor check result, UDIO3 and UDIO4 pull-up resistor through a 10K ohm. (UDIO3 pull-up: SD enabled, UDIO4 pull-up: MMC enabled) |
| | 54 | P.24 | 0711 | 1A | Ref Discrete schematic, connect 0 ohm from J10 pin 22 to Sourth Bridge SB_WLAN_PCIE_RST#. |
| | 55 | P.12 | 0711 | 1A | Ref Discrete schematic, U25B.F18: change the net name from PCI_GNT2# to SB_WLAN_PCIE_RST#; Add 20K pull down resistor at U25B pin F18 |
| | 56 | P.24 | 0711 | 1A | Ref Discrete schematic, connect 0 ohm from J9 pin 22 to Sourth Bridge SB_MCARD3_PCIE_RST#. |
| | 57 | P.12 | 0711 | 1A | Ref Discrete schematic, U25B.F8: connect 0 ohm population option to J9.22. GPIO table suggests that we add 20k pull down. Dis NO. |
| | 58 | P.25 | 0711 | 1A | Ref Discrete schematic, connect 0 ohm from J16 pin 22 to Sourth Bridge SB_WWAN_PCIE_RST#. |
| | 59 | P.12 | 0711 | 1A | Ref Discrete schematic, U25B.B19: change the net name from PCI_REQ2# to SB_WWAN_PCIE_RST#; Add 20K pull down resistor at U25B pin B19 |
| | 60 | P.25 | 0711 | 1A | Ref Discrete schematic, UIM_DATA: add a 100pF(NC) capacitor at the point nearest the SIM connector. |
| | 61 | P.25 | 0711 | 1A | Ref Discrete schematic, change the net name of J16 pin 40 from USB_MCARD3_DET# to USB_MCARD2_DET# |
| | 62 | P.24 | 0711 | 1A | Ref Discrete schematic, change the net name of J9 pin 40 from USB_MCARD2_DET# to USB_MCARD3_DET# |
| | 63 | P.33 | 0711 | 1A | Ref Discrete schematic, Reserve SN74LVC1G125DBVR buffer and Add 0 ohm between buffer input and output pin for AUD_DMIC_CLK |
| | 64 | P.31 | 0711 | 1A | Ref Discrete schematic, Remove R451 between JTP1 pin 1 and +3.3V_ALW |
| | 65 | P.19 | 0711 | 1A | Ref Discrete schematic, Remove RP45,Q54 and Q55 from G_DAT_DDC2 and G_CLK_DDC2 |
| | 66 | P.32 | 0711 | 1A | Per GG item 7 and Discrete schematic, C&G can remove this reserve circuit without no docking support. U59 pin1 pull down 10K. EC pin79 NC. Del R867 |
| | 67 | P.19 | 0711 | 1A | Per GG item 7 and Discrete schematic, C&G can remove this reserve circuit without no docking support. U59 pin1 pull down 10K. EC pin79 NC. Del R867 |
| | 68 | P.29 | 0711 | 1A | Per GG item 7 and Discrete schematic, C&G can remove this reserve circuit without no docking support. U59 pin1 pull down 10K. EC pin79 NC. Del R867 |
| | 69 | P.32 | 0711 | 1A | Ref Discrete schematic, Reserve R603 and C315 at U21 pin 33 |
| | 70 | P.32 | 0711 | 1A | Ref Discrete schematic, Reserve R441,C394 and C312 at U21 pin 1. |
| | 71 | P.32 | 0711 | 1A | Ref Discrete schematic, Remove 3.3V_LAN_PWRGD circuit. |
| | 72 | P.27 | 0712 | 1A | Ref Discrete schematic, Add common choke |
| | 73 | P.26 | 0712 | 1A | Common choke and capacitor move to DB, delete L25,R145,R142,C180,C183,C656,C654,C198. |
| | 73 | P.28<br>P.3 | 0712 | 1A | Ref Discrete schematic, USIO2.17 change the net name from DDR_ON to EC_CPU_PROCHOT#<br>Ref Discrete schematic, U9.D21 connect to EC_CPU_PROCHOT# through a 0 ohm. |

QUANTA COMPUTER

| | | |
|---|---|---|
| Title | EMI & Screw hole | |
| Size | Document Number<br>C & G UMA | Rev<br>2A |
| Date: Friday, January 19, 2007 | Sheet 50 of 60 | |

| Model | Item | Page | Date | Rev. | Description |
|---|---|---|---|---|---|
| C & G UMA | 74 | P.28 | 0712 | 1A | Ref Discrete schematic, Add net name ALW_PWRGD_3V_5V on USIO.18 Per GPIO table,Del. RC circuit. 100K and 0.1 uF. |
| | 75 | P.28<br>P.13 | 0712 | 1A | Ref Discrete schematic, USIO2.27 change the net name from SIO_SLP_S4# to DDR_ON and then add a 100k pull down.<br>U25.AF21: change to TEST PAD |
| | 76 | P.28 | 0712 | 1A | Ref Discrete schematic and GG item 41, AUX_EN_WOWL add 100K pull down |
| | 77 | P.28 | 0712 | 1A | Ref Discrete schematic, change net name IMVP_PWRGD from USIO2 pin3 to USIO2 pin43. |
| | 78 | P.28 | 0712 | 1A | Ref Discrete schematic, add a off-page connection at USIO2 pin66 |
| | 79 | P.28<br>P.13 | 0712 | 1A | Ref Discrete schematic, SB side add test pad. EC side ME_EC_ALERT change net name to LOM_SMB_ALERT# reserver pull high. |
| | 80 | P.28 | 0712 | 1A | Ref Discrete schematic,USIO2 pin 3 change signal name to DOCK_SMB_PME# and Add Pull up to +3.3V_ALW by 10K resister. |
| | 81 | P.28 | 0712 | 1A | Ref Discrete schematic,USIO2 pin 4 reserve 10K NC resister Pull high to +3.3V_ALW. |
| | 82 | P.28<br>P.18 | 0712 | 1A | Per GPIO pin table 0.1, UMA Use "LCDVCC_TST_EN" signal name for LCD TST.Change net name from EC_ENVDD to LCDVCC_TST_EN. |
| | 83 | P.28 | 0712 | 1A | Per Dell's Diag implementation and ref Discrete schematic,USIO2 pin 28 add 10K resister Pull high to +3.3V_ALW. |
| | 84 | P.32<br>P.29 | 0712 | 1A | Per GG list, AUD_HP_NB_SENSE/NB_MUTE# come into a AND gate output to U22 pin22 HP EN.<br>Delete AUD_HP_NB_SENSE from USIO1 pin 81. |
| | 85 | P.29 | 0712 | 1A | Ref Discrete schematic, Delete R658 between USIO1 and NB_MUTE# |
| | 86 | P.29 | 0712 | 1A | Ref Discrete schematic, Add Pull down 100K. |
| | 87 | P.29 | 0712 | 1A | Ref Discrete schematic, USIO1 pin 95 add a off-page connection named WLAN_RADIO_DIS# |
| | 88 | P.29 | 0712 | 1A | Ref Discrete schematic, Add a TEST PAD on USIO1.35 |
| | 89 | P.29<br>P.31 | 0712 | 1A | Ref Discrete schematic,USIO1 pin 61 Add 100K ohm and 0.047uF cap. RC circuit to+3.3V_ALW and serial 10 ohm resister.<br>Change net name of JTP1 from LID_CL_SIO# to LID_CL# |
| | 90 | P.29 | 0712 | 1A | Ref Discrete schematic, delete net name DOCK_SIO_ALERT# from RP59 |
| | 91 | P.29 | 0712 | 1A | Ref Discrete schematic, USIO1 pin 75 pull down through a 100k. |
| | 92 | P.29<br>P.23 | 0712 | 1A | Ref Discrete schematic, USIO1 pin 31 add an off-page connection named MODC_EN#<br>Ref Discrete schematic, Reserve MODC_EN# circuit. |
| | 93 | P.12 | 0712 | 1A | Ref Discrete schematic, U25C pin AE19 pull high to +3.3V_SUS |
| | 94 | P.12 | 0712 | 1A | Ref Discrete schematic, U25C pin AC17 pull high to +3.3V_SUS |
| | 95 | P.12 | 0712 | 1A | Ref Discrete schematic, U25C pin AG21 pull high to +3.3V_SUS<br>Ref Discrete schematic, add a off-page connection at AG21 |
| | 96 | P.12 | 0712 | 1A | Ref Discrete schematic, add a off-page connection at F4 |
| | 97 | P.12 | 0712 | 1A | Ref Discrete schematic, U25.AJ18 reserve 8.2K pull up to +3.3V_RUN |
| | 98 | P.12 | 0712 | 1A | Per GG list, DOCKED# should pull high to +3.3V_SUS. |
| | 99 | P.25 | 0712 | 1A | Ref Discrete schematic, delete off-page connection ICH_LAN_RST# and add TEST PAD |
| | 100 | P.12 | 0712 | 1A | Ref Discrete schematic, U25 pin AG19 pull down through a 100k |
| | 101 | P.17 | 0712 | 1A | Added C788-C793 per GG updated. |
| | 102 | P.34 | 0712 | 1A | Added VCP2 circuit per GG updated. |
| | 103 | P.6 | 0713 | 1A | TV_DCONSEL_0 & TV_DCONSEL_1 connected to GND. |
| | 104 | P.11 | 0713 | 1A | Update LAN function circuit per ref Discrete update. |
| | 105 | P.12 | 0713 | 1A | SB_LOM_PCIE_RST# Pull High to +3.3V_RUN per ref GPIO recommend. SB_NB_PCIE_RST# pull down per refer Discrete added. |
| | 106 | P.13 | 0713 | 1A | Change SIO_EXT_SMI# pull up power from +3.3V_ALW to +3.3V_SUS. |
| | 107 | P.17 | 0713 | 1A | Update CLK Gen. circuit per GG & Discrete update. |

QUANTA COMPUTER

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|---|---|---|
| Title | EMI & Screw hole | |
| Size | Document Number<br>C & G UMA | Rev<br>2A |
| Date: Friday, January 19, 2007 | Sheet 51 of 60 | |

| Model | Item | Page | Date | Rev. | Description |
|---|---|---|---|---|---|
| C & G UMA | 108 | P.17 | 0713 | 1A | Update CLK Gen. circuit per GG & Discrete update. |
| | 109 | P.18 | 0713 | 1A | Update LVDS power control method per ref JM7. |
| | 110 | P.19 | 0713 | 1A | Update SPDIF CIRCUIT per ref Discrete & GG. |
| | 111 | P.24,25 | 0713 | 1A | Update WLAN,WPAN,WWAN circuit per GG requirement. |
| | 112 | P.26 | 0713 | 1A | Update MDC_RST_DIS# circuit per GG requirement. |
| | 113 | P.27 | 0713 | 1A | Correction USB connector side signals name. |
| | 114 | P.28,29 | 0713 | 1A | Update SIO circuit per ref GG requirement and GPIO list. |
| | 115 | P.32,33 | 0713 | 1A | Update Audio,AMP,SPK circuit per refer GG. |
| | 116 | P.39 | 0713 | 1A | Populated PC10,PC13,PC63,PC66 per GG requirement. |
| | 117 | P.39-45 | 0713 | 1A | Power updated schematic.(File name changed to FM5 MB UMA-0714_JM-5) |
| | 118 | P.46 | 0714 | 1A | Per ME's drawing, add clips. |
| | 119 | P.31 | 0714 | 1A | Depopulate RP61 per GG requirement |
| | 120 | P.27 | 0714 | 1A | Added C313 & C323 per GG requirement. |
| | 121 | P.6 | 0714 | 1A | Populate R411 per GG requirement. |
| | 122 | P.17 | 0714 | 1A | Populate R487 per GG requirement |
| | 123 | P.11,30 | 0714 | 1A | Changed RTC_BAT_DET# PU from P.30 to P.11 per GG requirement. |
| | 124 | P.12 | 0714 | 1A | Changed SB_LOM_PCIE_RST# to PD. Delete PCI_PIRQA# off page symbol. |
| | 125 | P.13 | 0714 | 1A | Added R529, De-pop R655, R657, C936 per GG requirement. |
| | 126 | P.16 | 0714 | 1A | Added C690,C702 per GG requirement. |
| | 127 | P.24 | 0714 | 1A | Populate Q67 per support Sniffer function. |
| | 128 | P.31 | 0714 | 1A | Removed C3 & R436 to DB per GG requirement. |
| | 129 | P.24 | 0717 | 1A | De-populate WoWL power SW circuit. |
| | 130 | P.17 | 0717 | 1A | Removed R429 & R859 per Vendor review update. |
| | 131 | P.9,28,38,39 | 0718 | 1A | Removed +1.8V_RUN power for UMA no need. |
| | 132 | P.31 | 0718 | 1A | Populate RP61 per provide TP AMB BUS driving. |
| | 133 | P.6,12,24 25,26,28 | 0718 | 1A | Split PLTRST to 2 single gate. PLTRST1# for WWAN?WLAN/WPAN/Express Card. PLTRST2# for MCH/SIO. |
| | 134 | P.37 | 0719 | 1A | Added BT circuit. |
| | 135 | P.25 | 0719 | 1A | De-populate C1249 per ref JM7 schematic update. |
| | 136 | P.39-45 | 0720 | 1A | Power update schematic. |
| | 137 | P.9 | 0720 | 1A | Added R429,R436,R456,R461 pull up/down for Crestline sighting report V:9.0 P.16 update. |
| | 138 | P.6,12,28 | 0720 | 1A | Change net name from PLTRST2# to PLTRST# for same as Discrete. |
| | 139 | P.14 | 0720 | 1A | Change R253 package from 0402 to 0603. |
| | 140 | P.29 | 0724 | 1A | Delete R927, Change R929 value from 12K/F to 10K per SMSC revier updated. |
| | 141 | P.28 | 0724 | 1A | Changed R325&R265 vlaue from 1M to 47K per SmSC review updated. |
| | 142 | P.31 | 0724 | 1A | Added Media board LED control signal cirfuit, changed enable signals to low active per GG updated. |
| | 143 | P.29,33 | 0724 | 1A | Added CCD control power circuit, DMIC filter circuit, USB common choke circuit, per GG requirement. |
| | 144 | P.23 | 0724 | 1A | Added R927 and R595. Depopulate R917,R918 per GG updated. |
| | 145 | P.6 | 0724 | 1A | LCTLA_CLK/LCTLA_DATA changed to connect GND per GG updated. |
| | 146 | P.27,29 | 0724 | 1A | Change Signal net from Gilligan USB EN# to USB_BACK2_EN# per GG updated. |
| | 147 | P.24 | 0724 | 1A | Change Signal net PCIE_MCARD3_DET#/USB_MCARD3_DET# PU to +3.3V_SUS per GG updated. |
| | 148 | P.39-45 | 0725 | 1A | Update power schematic for layout requirement and checked updated. |
| | 149 | P.29 | 0727 | 1A | Added R647 for BC_DAT pull-up per Dell requirement. |
| | 149 | P.28,29 | 0727 | 1A | Update GPIO table per DELL update A12 include ITP_DBRESET# / BEEP / PS_ID |



QUANTA COMPUTER

| | | |
|---|---|---|
| Title | EMI & Screw hole | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 52 of 60 | |

| Model | Item | Page | Date | Rev. | Description |
|---|---|---|---|---|---|
| *C & G UMA* | 1 | 24 | 9/18/2006 | 2A | Add SMBus isolation circuitry for WLAN.Add isolation circuitry for SMBus on WLAN. |
| | 2 | 37 | 9/18/2006 | 2A | Update footprint name of D8. |
| | 3 | 39- 45 | 9/21/2006 | 2A | Per Power schematic 0920, update power schematic. |
| | 4 | 27 | 10/02/2006 | 2A | Update footprint name of JUSB2, and change to 8 pin. |
| | 5 | 12 | 10/02/2006 | 2A | Delete ICH_USBP8+ and ICH_USBP8- |
| | 6 | 19 | 10/02/2006 | 2A | Update footprint name of JVGA1. |
| | 7 | 31 | 10/02/2006 | 2A | Update footprint name and QCI PN of JTP1. |
| | 8 | 25 | 10/02/2006 | 2A | Update footprint name and QCI PN of JSIM1. |
| | 9 | 11&23 | 10/16/2006 | 2A | Changed SATA port1 to port2 for Gilligan used. |
| | 10 | 18 | 10/16/2006 | 2A | De-populate C45&C46 for LCD SMBUS rise/fall time issue. |
| | 11 | 12&24 | 10/16/2006 | 2A | Update USB ports assigment |
| | 12 | 18 | 10/16/2006 | 2A | Update LVDS per EMC requirement. |
| | 13 | 35 | 10/23/2006 | 2A | Added L47, Change R66 to bead, Change L7 vlaue, Change C42, C69, C143, C145, C56, C114, C124, C144, C102, C126, C57, C146, C109, C70, C55, C148 pre Dell RF EMI requirement. |
| | 14 | 36 | 10/23/2006 | 2A | Added L46 and changed C376 value for Dell RF EMI requirement. |
| | 15 | 13 | 10/24/2006 | 2A | Change R67 value from 100K to 10K per GG list checked. Because GPIO update, Delete R67 by change item 49. |
| | 16 | 34 | 10/24/2006 | 2A | Change R360 power up rail from +5V_SUS to +3.3V_SUS pwe GG updated. |
| | 17 | 28 & 33 | 10/24/2006 | 2A | Per change Sniffer control same as M07 of GG list, Change Q55, Q56 from 3904 to DTA114YUA, delete R131, R132, R524, R525. |
| | 18 | 28 | 10/24/2006 | 2A | Change R188&R189 value from 1M to 2.7K per GG requirement. |
| | 19 | 23 | 10/24/2006 | 2A | Change HDD EN control power rail from +5V_ALW to +5V_ALW2 per GG requirement. |
| | 20 | 13 | 10/24/2006 | 2A | Depopulate R329 and change R92 value from 10K to 8.2K per GG requirement. |
| | 21 | 17 | 10/24/2006 | 2A | Change Single End serial damping value for fine tune value per GG requirement. |
| | 22 | 11&37 | 10/25/2006 | 2A | Changed the LED control method. Move SATA LED mask to P.37. 1109 JM: Corrected LED of WLAN circuit. |
| | 23 | 13 | 10/25/2006 | 2A | Depopulate R342, R352 per GG requirement. |
| | 24 | 46 | 10/25/2006 | 2A | Pop C377, C407, C428, C383, C398, C10, C25, C319, C387 with 0.1uF caps for GG requirement |
| | 25 | 24 & 25 | 10/25/2006 | 2A | Remove C252, C157, C253 per Mini-card no used +3V_LAN. |
| | 26 | 24 | 10/25/2006 | 2A | Add R541 and non-populate for GG requirement, Changed PD on P.28 |
| | 27 | 24 | 10/25/2006 | 2A | Added 2 TP for GG requirement. |
| | 28 | 25 | 10/25/2006 | 2A | Added R542 and non-populate per GG requirement. |
| | 29 | 24 & 37 | 10/25/2006 | 2A | Moved the LED_MASK# circuit to 37 and followed GG to update BT LED control method, for this change, added R543,R544, Q67,Q68. Change Q11 from DTA114YUA to 2N7002W-7-F. Change R383 from 10K to 100K. Change R128 from 220 to 2K. |
| | 30 | 24 | 10/25/2006 | 2A | Change the net of pin 5 of J4 from "COEX1_BT_ACTIVE" to "COEX1_BT_ACTIVE_Mini" per GG requirement. |
| | 31 | 37 | 10/25/2006 | 2A | Change the net of pin 6 of J2 from "COEX1_BT_ACTIVE" to "COEX1_BT_ACTIVE_DC" pre GG requirement |
| | 32 | 37 | 10/25/2006 | 2A | Added U34 Circuit per GG requirement. |
| | 33 | 33 | 10/25/2006 | 2A | Update Audio DB BTB circuit per update connector pin define. |
| | 35 | 11 | 10/27/2006 | 2A | Change CODEC bitclok with 10 ohm damping resistor per GG requirement. |
| | 36 | 24 | 10/27/2006 | 2A | Added "BT_ACTIVE#" with 0_NC on J3.46 per GG requirement. |
| | 37 | 17 | 10/27/2006 | 2A | Change RP10 from 33 to 10, RP3, RP5 from 33 to 22 per EA updated. |
| | 38 | 17 | 10/27/2006 | 2A | Pop C71, C395, C113, C108, C104, C116 with 22p caps per GG requirement. |
| | 39 | 39 | 10/27/2006 | 2A | Change +3.3V_SUS & +5V_SUS EN power up to +5V_ALW2 per GG requirement. |
| | 40 | 32 | 10/27/2006 | 2A | Change C331, 332 to 0.033uF/16V/X7R/1206 & C351, C354 to 1uF/16V/X7R/1206 per Gg requirement. |
| | 41 | 29 | 10/27/2006 | 2A | Depopulate EC non control resistor. Dell don't agree to do it. |
| | 42 | 28 | 10/27/2006 | 2A | Depopulate EC non control resistor. Dell don't agree to do it. |
| | 43 | 13&28 | 10/27/2006 | 2A | Per GPIO A14, changed U11.AG22 to LOM_SMB_ALERT#. |
| | 44 | 28&29 | 10/27/2006 | 2A | Per GPIO A14, Swap DOCK_SMB_ALERT# and DOCK_SMB_PME. |



QUANTA COMPUTER

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|---|---|---|
| Title | EMI & Screw hole | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 53 of 60 | |

| Model | Item | Page | Date | Rev. | Description |
|---|---|---|---|---|---|
| *C & G UMA* | 45 | 28&38 | 10/27/2006 | 2A | Per GPIO A14, changed USIO1.14 to ATI_Intel. Delete 3.3V_LAN_PWRGD. |
| | 46 | 28&32 | 10/27/2006 | 2A | Reserved the AUD_AMP_MUTE# for 'PO' noise back up solution. |
| | 47 | 28 & 38 | 10/27/2006 | 2A | Per GPIO A14, swap USIO1.18 & USIO1.29. Base on Dawson, delete '3V_5V_SUS_PWRGD' and added TP. |
| | 48 | 29&13 | 10/27/2006 | 2A | Per GPIO A14, change USIO2.66 to PWRUSB_OC#. CCD_VDD_ON changed to U11.AD10. |
| | 49 | 13 | 10/27/2006 | 2A | Per GPIO A14, change U11.AC19 to SIO_EXT_SCI#. |
| | 50 | 29&37 | 10/27/2006 | 2A | Per Comm. requirement, Change USIO2.25 & J2.5 net-name from "BT_RADIO_DIS#" to "BT_RADIO_DIS_DC#" |
| | 51 | 13 | 10/30/2006 | 2A | Change LOM_SMB_ALERT# PU to +3.3V_SUS per GG requirement. |
| | 52 | 28 | 10/30/2006 | 2A | Change R183,R184 to 7.5K per EA fine tune requirement. |
| | 53 | 9 | 10/30/2006 | 2A | Change L39 to BLM18PG101SN1D and added C629 for Intel requirement. |
| | 54 | 39-45 | 10/30/2006 | 2A | Power update schematic. |
| | 55 | 29 | 10/30/2006 | 2A | Added 5021 co-layout schematic. |
| | 56 | 13 & 24 | 10/30/2006 | 2A | Update WPAN_RADIO_DIS_MINI# circuit. |
| | 57 | 23 | 10/30/2006 | 2A | Change SATA RX caps from DB to MB. |
| | 58 | 14 | 11/01/2006 | 2A | Chnage R205 from 100 to 10 per GG requirement. |
| | 59 | 39 | 11/01/2006 | 2A | Change PC52 to 4700pF pre GG requirement. |
| | 60 | 24 | 11/01/2006 | 2A | Depopulate R156 & C173 & C158 per WWAN requirement. |
| | 61 | 23&24 | 11/01/2006 | 2A | Added C649, C650, C651, R541, R561, R562 on CLK_REQ# per EMI requirement. |
| | 62 | 32 | 11/01/2006 | 2A | Populate C639 and changed to 0.1uF per EMI requirement. |
| | 63 | 39-45 | 11/02/2006 | 2A | Update power schematic1102-1 per power update. |
| | 64 | 17 | 11/03/2006 | 2A | Added 0_0402 RSV resistor per EMI requirement. |
| | 65 | 46 | 11/03/2006 | 2A | Added 2EMI spring for EMI requirement. |
| | 66 | 17 | 11/07/2006 | 2A | Leverage JM7 to added ferri bead on FSA for EMI solution. PT used 0ohms for fine tune. |
| | 67 | 17 | 11/07/2006 | 2A | Change R319 to 2.2K per Intel recommend value. |
| | 68 | 34 | 11/07/2006 | 2A | De-populate Q48 to prevent thermal strip issue. |
| | 69 | 12 | 11/08/2006 | 2A | Added C652 for EMI solve CCD USB issue. |
| | 70 | 32 | 11/08/2006 | 2A | Added U35 & R541 per audio 'po' issue reserved. |
| | 71 | 17 | 11/09/2006 | 2A | Reserve L65 and used 0 ohms for Dawson check 14M noise emilination solution |
| | 72 | 14,19,31, 37,38,39 | 11/09/2006 | 2A | Reserve PR66 (0 ohms) for RF concern 14M noise coupling from +5V_RUN power trace. |
| | 73 | 23 | 11/09/2006 | 2A | Added decoupling caps of +5V_HDD for Cosica. |
| | 74 | 12 | 11/10/2006 | 2A | Added OC# docupling caps per refer Dawson solution to avoid 48MHz noise. |
| | 75 | 11,32 | 11/10/2006 | 2A | For 'PO' noise, change SPEAKER_DET# from U18.4 to U11.AE10. Change U35.1 connection to U18.4. |



QUANTA COMPUTER

| | | |
|---|---|---|
| Title | EMI & Screw hole | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 54 of 60 | |

| Model | Item | Page | Date | Rev. | Description |
|---|---|---|---|---|---|
| *C & G UMA* | 38 | 17,35 | 01/10/2006 | 3A | Per fine-tune table, change R99 from 91ohm to 33 ohm,and pop R133 and change from 33 to 10, C104 change to 4.7P,Pop C147 and change to 8.2P |
| | 39 | 12,17 | 01/10/2006 | 3A | Per fine-tune table, change R81 from 91ohm to 33 ohm,and pop R200 and change to 33,C108 change to 10P,Pop C320 and change to 9P. |
| | 40 | 13,17 | 01/10/2006 | 3A | Per fine-tune table, change R95 from 100ohm to 33 ohm,and pop R94 and change to 33, C395 change to 1P, Pop C93 |
| | 41 | 14 | 01/10/2006 | 3A | Footprint not match, change footprint size of R149 from 0402 to 0603 |
| | 42 | 29 | 01/11/2006 | 3A | Per GG list item 31, Chnage the net name of 112 as CHIPSET_ID1 |
| | 43 | 29 | 01/11/2006 | 3A | For ST board ID, Pop R163, Depop R164 |
| | 44 | 37 | 01/11/2006 | 3A | Per GG list item 33, Add 0ohm_NC(R571) resistor pad connected from Coex1_BT_Active_MINI to Coex1_BT_Active |
| | 45 | 18 | 01/15/2006 | 3A | Per GG list item 38, change R22 from 470 ohme to 100 ohms for LCD on/off timing EA requirement. |
| | 46 | 33 | 01/15/2006 | 3A | Per GG list item 35, change C670,C671 to 33P |
| | 47 | 22 | 01/15/2006 | 3A | Per RICHO's check result, apply 270pF(NC) for SD_CD# and MS_CD#. |
| | 48 | 6 | 01/16/2006 | 3A | Per GG list item 40, Change R427 from 2.4K to 3.3K |
| | 49 | 32 | 01/17/2006 | 3A | Audio solution for pass EMI 225MHz and 451MHz radiation emission test.<br>Added R572, R578, R579 and R580 on AUD_SPK_L1, AUD_SPK_L2, AUD_SPK_R1, AUD_SPK_R2 trace |
| | 50 | 33 | 01/17/2006 | 3A | Audio solution for pass EMI 225MHz and 451MHz radiation emission test.<br>Added R581, R582, R583 and R584 on AUD_LINE_OUT,AUD_HP_OUT |
| | 51 | 32 | 01/17/2006 | 3A | Added L48, L49 on +.3.3V_RUN and +VADD -- 600 ohm power bead. |
| | 52 | 27 | 01/17/2006 | 3A | USB device radiates strong R/W noise when the full device normal working,especially USB daughter board and PCI express card.we suggest EE solution as follow.<br>Added C675, C676, C677, C678 150pF. |
| | 53 | 13,17 | 01/17/2006 | 3A | Per fine-tune table, change R65 to 33 ohm,and depop C71,R157 change to 33,Pop C180 and change to 6.8P. |
| | 54 | 40,45 | 01/18/2006 | 3A | FL3,FL4 and FL5: Change footprint size as RC1210 and PN to FBMH3225HM202NT |
| | 55 | 40 | 01/18/2006 | 3A | Add FL7 between PQ31 and +PWR_SRC |
| | 56 | 44 | 01/18/2006 | 3A | Add FL8 and FL9 between +3.3V_ALW and +3.3V_ALWP |
| | 57 | 40 | 01/19/2006 | 3A | Remove FL7 between PQ31 and +PWR_SRC. Because there is no spacing for layout. |
| | 58 | 44 | 01/19/2006 | 3A | Remove PJP12 |
| | 59 | 44 | 01/19/2006 | 3A | For current ration concern, add a FL10 |
| | 60 | 32 | 01/19/2006 | 3A | Based on David mail, The pin 1, 9 need to populate both 0.1 uF // 560pF in Codec's +3.3V run power node. Added one .1uF on pin 40 for EMI requirement.-JM(0119) |
| | 61 | 46 | 01/19/2006 | 3A | Update TH9,TH10,TH14,TH15 footprint for ESC concern. |
| | 62 | 32 | 01/19/2006 | 3A | C331,C332 change PN to CH33306KL14 |
| | 63 | 28 | 01/19/2006 | 3A | R110 and R123 change to 1M |



QUANTA COMPUTER

| | | |
|---|---|---|
| Title | EMI & Screw hole | |
| Size | Document Number<br>C & G UMA | Rev<br>2A |
| Date: Friday, January 19, 2007 | Sheet 54 of 60 | |

| Model | Item | Page | Date | Rev. | Description |
|---|---|---|---|---|---|
| *C & G UMA* | 1 | 29 | 21/12/2006 | 3A | Add R564,move the 'PLATFORM_BID' signal from SATA DB to MB |
| | 2 | 34 | 21/12/2006 | 3A | Pop Q48, per JM's mail. |
| | 3 | 35,36 | 21/12/2006 | 3A | Base on internal notice,Change L7,L46 P/N from CX8LM152000 to CX5LM152000;L47,R66 P/N from CX5LM152000 to CX8LM152000. |
| | 4 | 17 | 21/12/2006 | 3A | Base on internal notice, L65: Change QCI PN from CS00003J951 to CX08T250000 |
| | 5 | 18 | 21/12/2006 | 3A | Base on internal notice, Delete location C26 at CH31004KB17 |
| | 6 | 37 | 21/12/2006 | 3A | Per "Reference Schematic & Checklist Updates" mail, Change R560 from 0 to 10K |
| | 7 | 46 | 01/02/2006 | 3A | Add a TH. |
| | 8 | 32,33 | 01/02/2006 | 3A | Per EMI request, to reserve the filtering components for MIC signals. |
| | 9 | 22 | 01/02/2006 | 3A | Add a switch, to prevnet XD card no detect issue. 0110: Reserve R570 |
| | 10 | 39-45 | 01/02/2006 | 3A | Power update schematic. |
| | 11 | 14 | 01/03/2006 | 3A | C482 change the footprint to CC0402-C. |
| | 12 | 32 | 01/04/2006 | 3A | Per GG list item 2:add 100kohm resistor (R567) between pin 40 and +3.3V_RUN and a 1000pF cap (C672 below) from Pin 40 to ground |
| | 13 | 28,29 | 01/04/2006 | 3A | Per GG list item 3:DOCK_SMB_PME# should be pulled up to +5V_ALW DOCK_SMB_ALERT# should be pulled up to +3.3V_ALW |
| | 14 | 24 | 01/04/2006 | 3A | Per GG list item 6: add series resistors(0ohm) on host debug signal. |
| | 15 | 24 | 01/05/2006 | 3A | Per GG list item 7: Change the pin BT_ACTIVE# to LED_WPAN# |
| | 16 | 24 | 01/05/2006 | 3A | Per GG list item 10: Add a series 0ohm resistor on the trace of pin 46 of J3 |
| | 17 | 37 | 01/05/2006 | 3A | Per GG list item 11: Delete the offpage connection of BT_ACTIVE# |
| | 18 | 37 | 01/05/2006 | 3A | Per GG list item 12:Add a 10K pull down on J2 pin2. and R190 100K NC. |
| | 19 | 31 | 01/05/2006 | 3A | Per GG list item 13: Change TP MB connecter JTP1 pin9 from +3.3V_RUN to +5V_ALW |
| | 20 | 28 | 01/05/2006 | 3A | Per GG list item 17: NC R382 |
| | 21 | 29 | 01/05/2006 | 3A | Per GG list item 20: BIOS ROM 1M change to 2M |
| | 22 | 32 | 01/05/2006 | 3A | Per GG list item 24: Pop R274 |
| | 23 | 17 | 01/05/2006 | 3A | Per GG list item 18: R96 change to 2.2K |
| | 24 | 33 | 01/05/2006 | 3A | Per GG list item 19: CCD soft-start circuit correct and Add reserve 0 ohm for remove Camera VCCD_ON. JM: For layout placement spacing concern, I need removed R569,R570,R571,R572. |
| | 25 | 12,27 | 01/05/2006 | 3A | Per GG list item 25: USB_OC4_8# channel separate |
| | 26 | 46 | 01/08/2006 | 3A | Per Derating report, C383,C377,C398,C10,C25,C319,C387,C16,C19,C324 change part number to CH41004M912 |
| | 27 | 37 | 01/08/2006 | 3A | Per GG list item 15, R67 47K change to 0 ohm and R561 10K change to 47K. |
| | 28 | 23 | 01/08/2006 | 3A | Per GG list item 1:+5V_ALW2 changes to +3.3V_ALW2 Pop R576, Depop R546 |
| | 29 | 12,13 | 01/08/2006 | 3A | Per GG list item 15: PCIE_MCARD2_DET# from GPIO20 to ICH8 GPIO5/PIRQH# pin B3.( GPIO20 add test pad) |
| | 30 | 13 | 01/08/2006 | 3A | Per GG list item 15: Add R577 (4.7K) series resistor at ICH8 pin AH12 (USB_MCARD1_DET#). |
| | 31 | 21 | 01/08/2006 | 3A | Depop C266, for R5C833 |
| | 32 | 30 | 01/08/2006 | 3A | Delete RTC battery PN for moving to ME BOM |
| | 33 | 20,21 | 01/08/2006 | 3A | Change U15 PN from 5C832 to R5C833 |
| | 34 | 14,19,31 37,38,39 | 01/09/2006 | 3A | RF had requiest split +5V_RUN for 14MHz noise fine tune resistor PR66 on PT stage. Now removed PR66 and change net name from +5V_RUN2 to +5V_RUN. |
| | 35 | 17 | 01/10/2006 | 3A | Per fine-tune table, change PR3 from 22 ohm to 10 ohm. |
| | 36 | 17,28 | 01/10/2006 | 3A | Per fine-tune table, change R97 from 100ohm to 51 ohm,and pop R129,C113 change to 10P,Pop C141 and change to 2.2P |
| | 37 | 17,20 | 01/10/2006 | 3A | Per fine-tune table, change R98 from 100ohm to 10 ohm,and pop R198 and change from 10 to 22, C116 change to 10P, Pop C215 and change to 1P |

QUANTA COMPUTER

| | | |
|---|---|---|
| Title | EMI & Screw hole | |
| Size | Document Number C & G UMA | Rev 2A |
| Date: Friday, January 19, 2007 | Sheet 55 of 60 | |