

Compal confidential

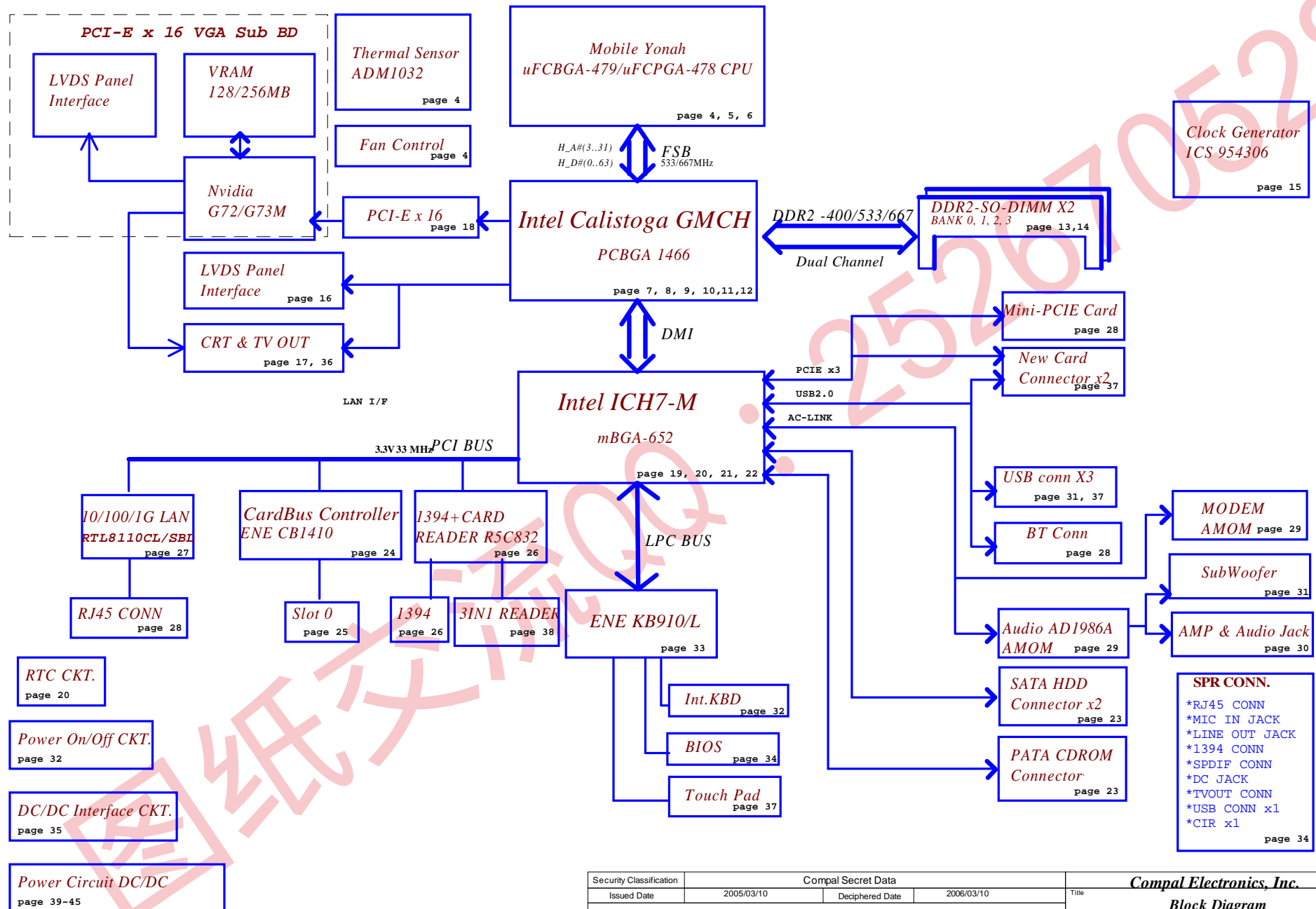
HGT30/31 Schematics Document

Mobile Yonah uFCPGA with Intel
Calistoga_GM/PM+ICH7-M core logic

2006-02-15

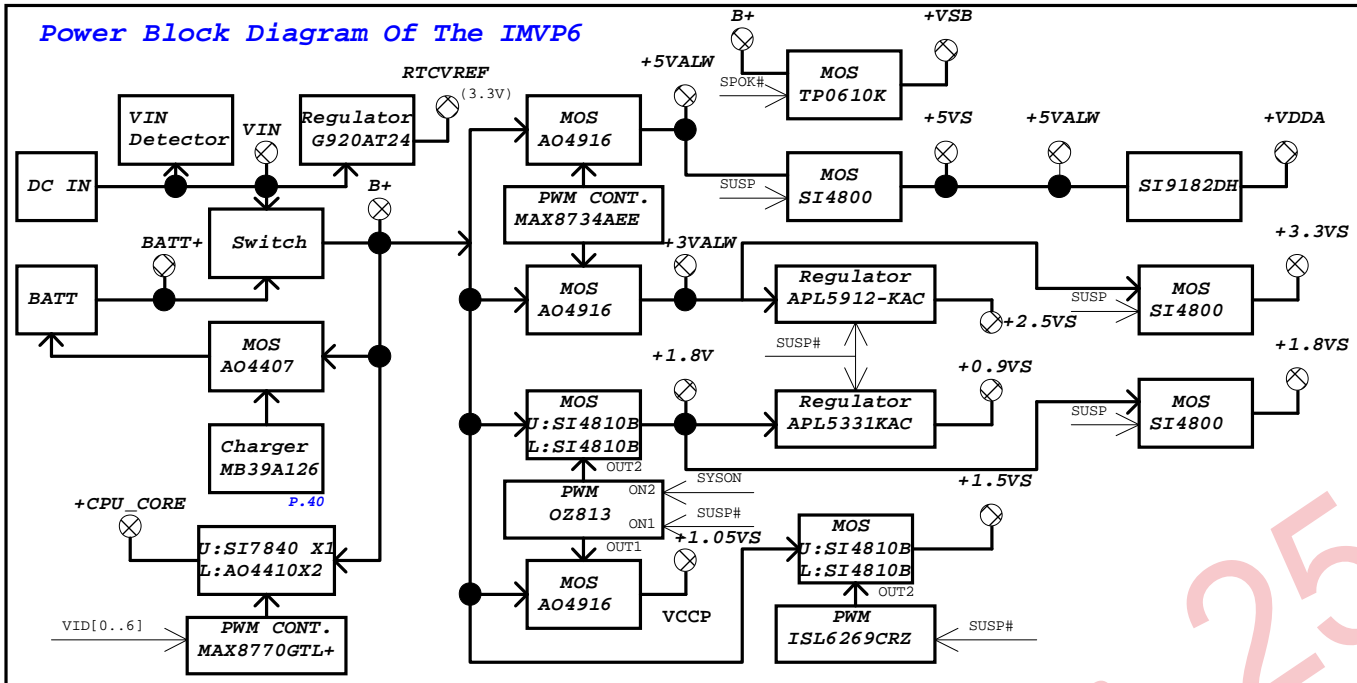
REV:0.3

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Power Block Diagram Of The IMVP6



PCI DEVICES

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS CB1410	AD20	2	PCI_PIRQA#
CARD READER & 1394 R5C832	AD22	0	PCI_PIRQG# PCI_PIRQH#
LAN CONTROLLER RTL8110SBL/CL	AD17	3	PCI_PIRQF#

Voltage Rails

State	+B LDO3 LDO5	+5VALW +3VALW	+1.8V +5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +VGA CORE +1.2VS +0.9VS +CPU CORE +VCCP
S4 : STD	O	O	O	O
S4 : SOFT OFF	O	O	O	O
S0	O	O	O	O
S1	O	O	O	O
S3 : STR	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

PCIE LANE

LANE	DEVICE
1	Express Card
2	Mini Card

USB

PORT	DEVICE
0	LEFT SIDE
1	BLUE TOOTH
2	RIGHT SIDE
3	NC
4	RIGHT SIDE
5	NC
6	NC

I2C / SMB Address

DEVICE	ADDRESS R/W
KB910/L (SM1-Pulled-Up 5V)	
AT24C16AN	A3/A2 H
SMART BATTERY	17/16 H
KB910/L (SM2-Pulled-Up 3.3V)	
ADM1032AR	99/98 H
G7xM (I2CC-Pulled-Up 3.3V)	
G781-1 (RESERVED)	9B/9A
ICH7M SM Bus	
ICS9LPR325AKLFT	D3/D2 H (3.3V)
DDR II DIMM0	A1/A0 H (3.3V)
DDR II DIMM1	A3/A2 H (3.3V)
Express Card	NC (2.5V)
Mini-Express	NC (2.5V)

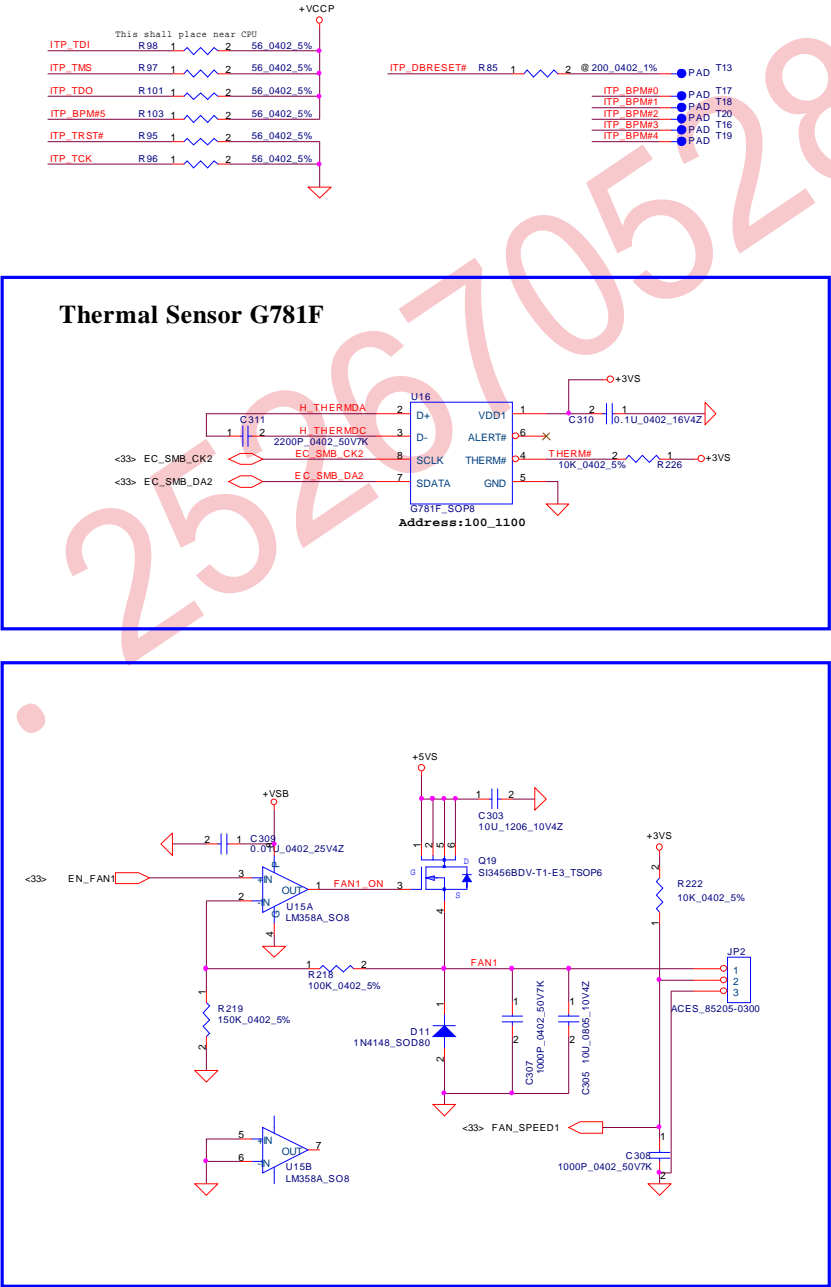
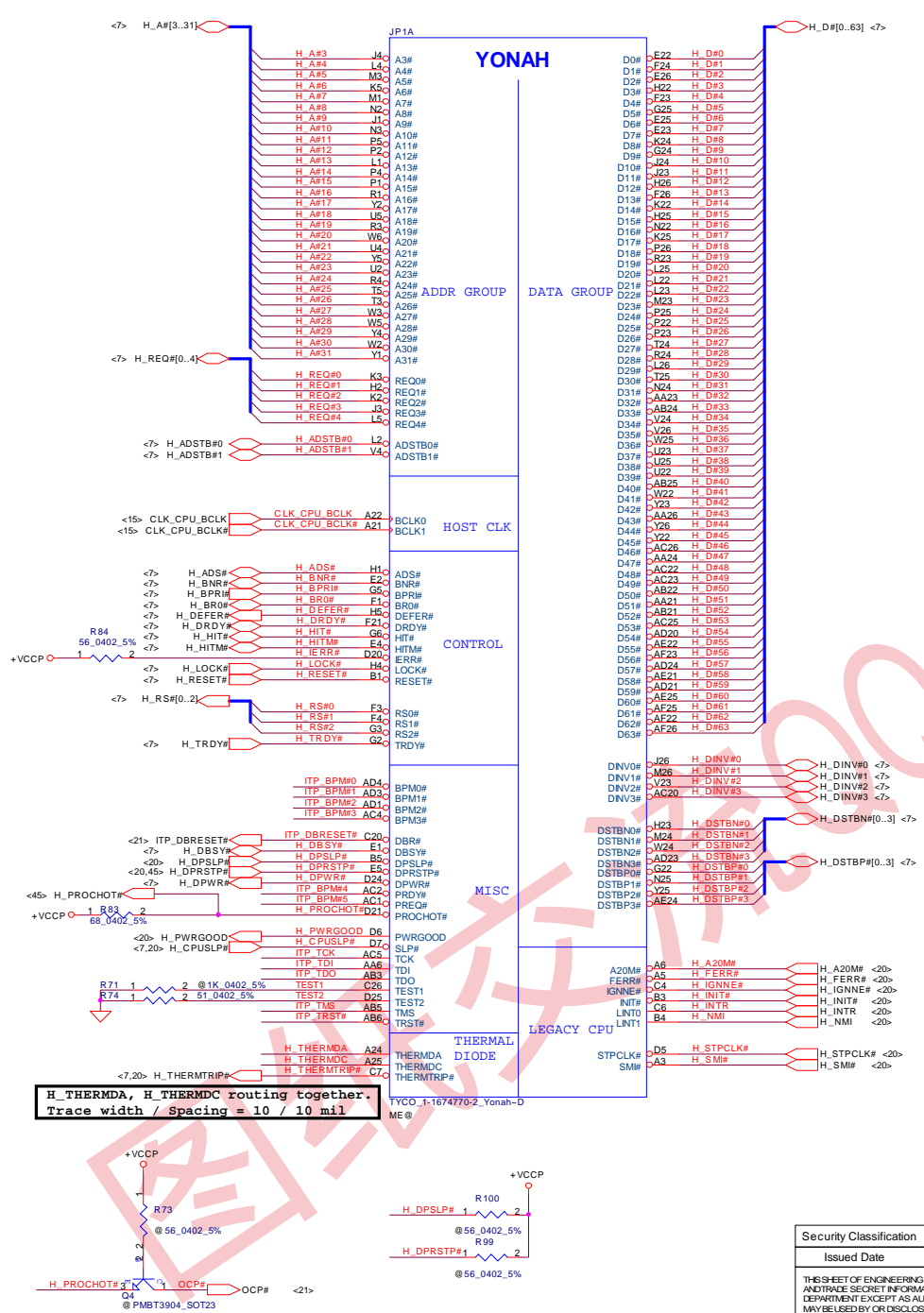
BOM Structure

MARK	FUNCTION
@	NO FOR ALL
EXP@	PCIE-NEW CARD
BT@	BLUE TOOTH
UMA@	Internal 945GM
VGA@	External G7xM
SUBWOOFER@	SUBWOOFER
HGT30@	HGT30
CB@	PCMCIA/CARD BUS
GIGA@	8110SBL (SCL) Giga LAN
10/100@	8110CL 10/100Mb LAN

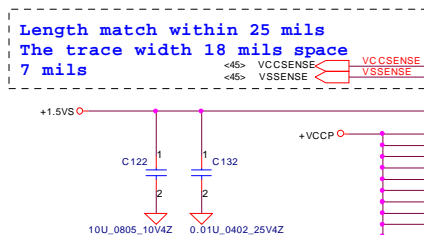
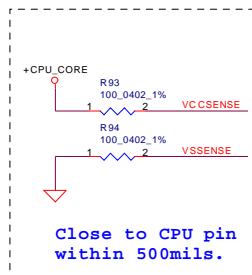
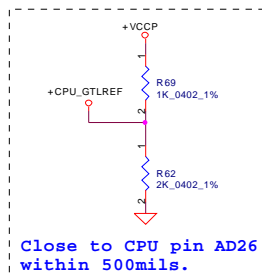
MB ID	P NAME
0	HGT-30
1	HGT-31

ID	MB REV#	R115(Rb)	Vab
0	R01 (EVT)	0	0V
1	R02 (DVT)	8.2K	0.25V
2	R03	18K	0.50V
3	R04	33K	0.82V
4		56K	1.19V
5		100K	1.65V
6		200K	2.20V
7		NC	3.30V

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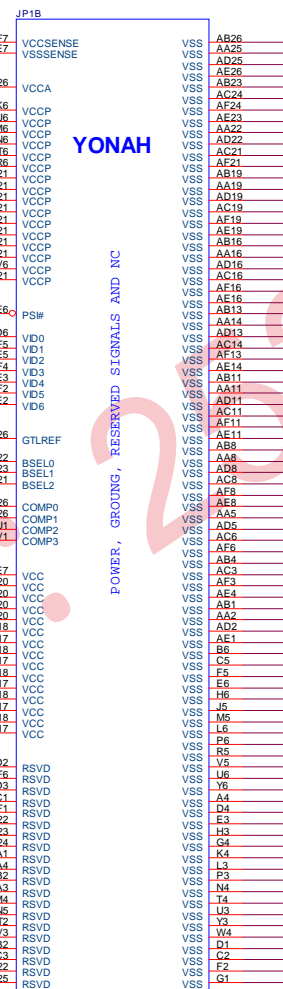
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.

JP1B

YONAH

POWER, GROUND, RESERVED SIGNALS AND NC



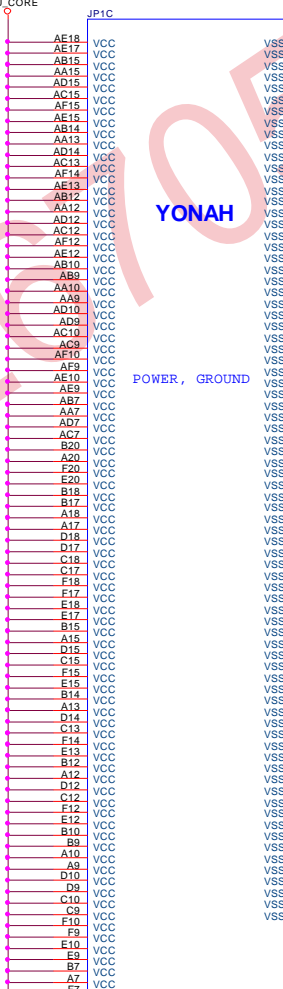
TYCO_1-1674770-2_Yonah-D
ME@

+CPU_CORE

JP1C

YONAH

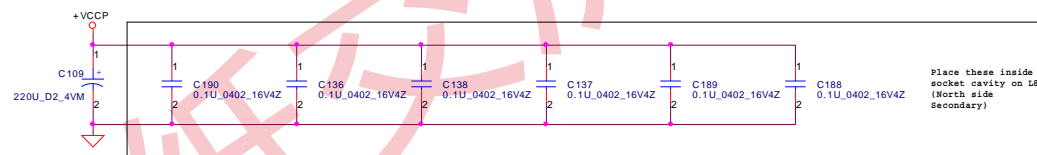
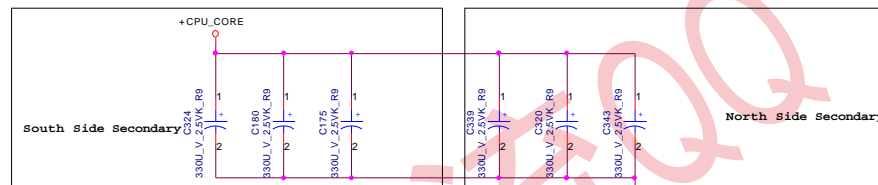
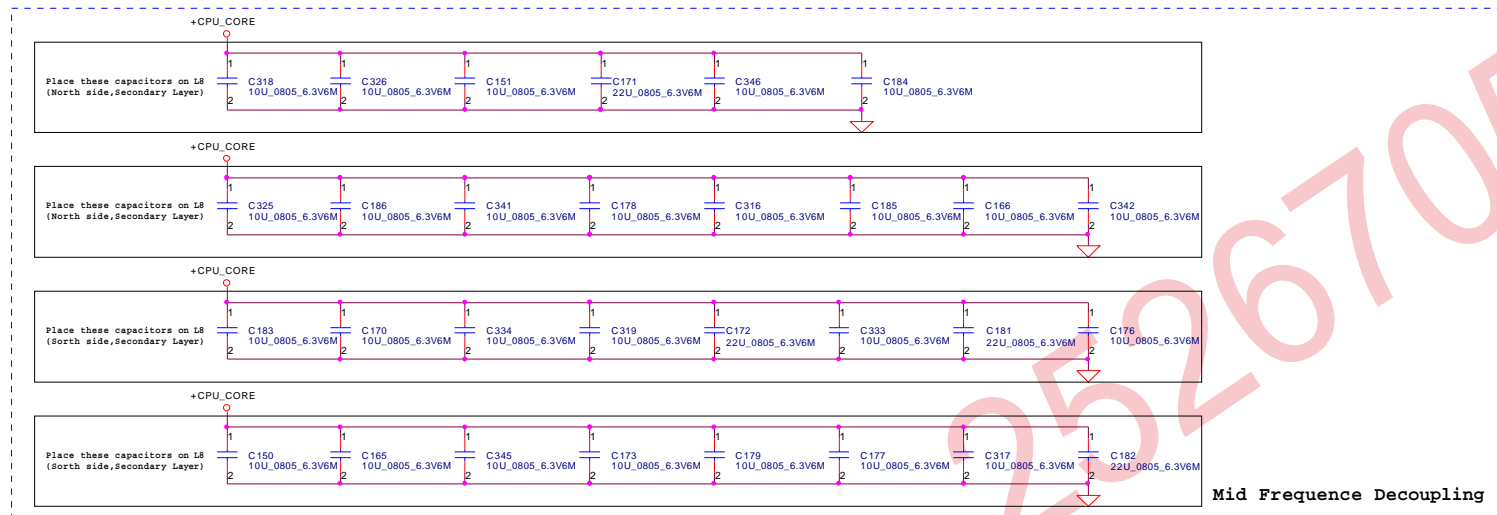
POWER, GROUND



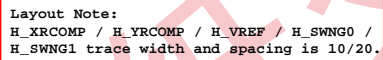
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ME@

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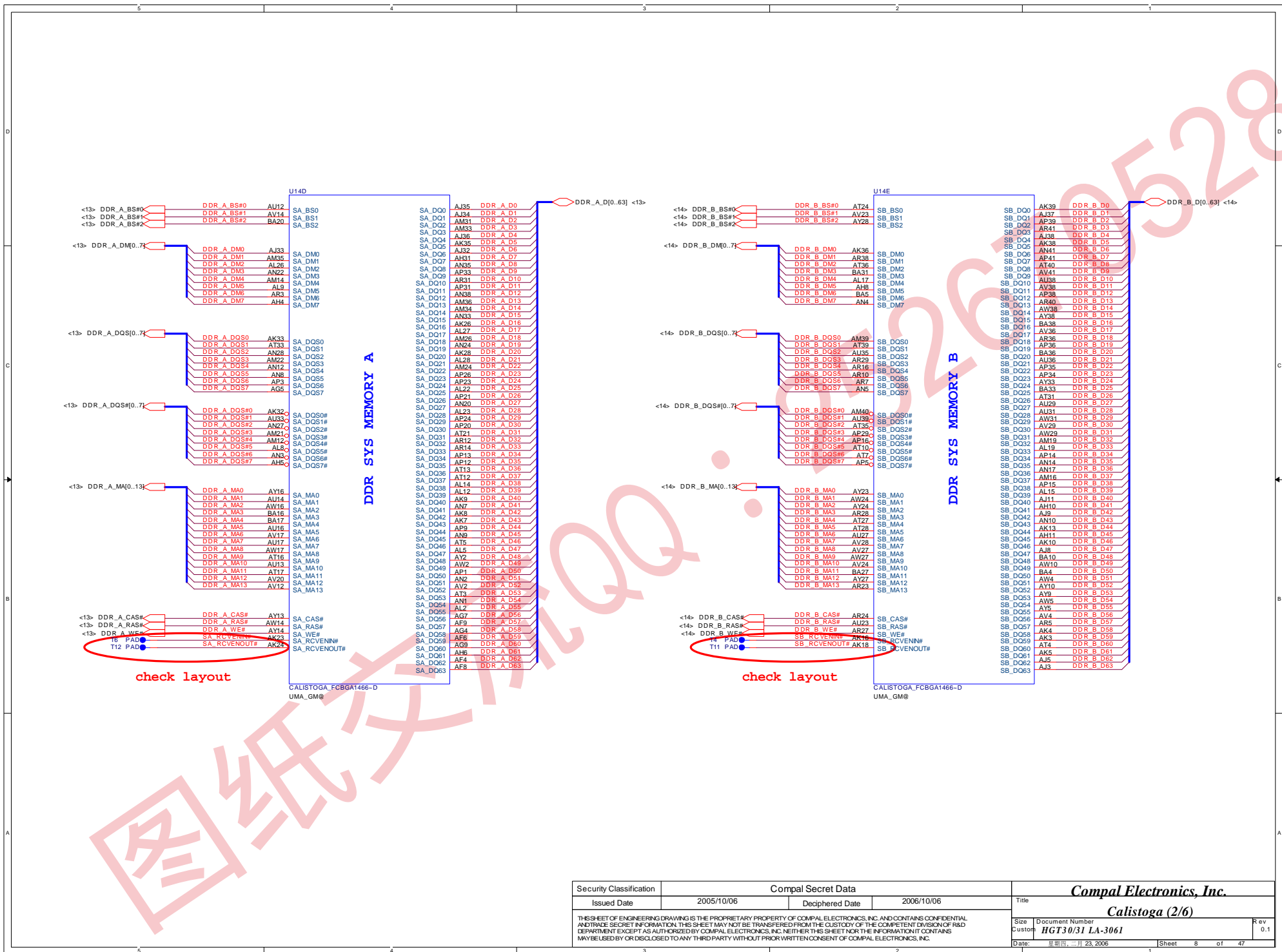
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Yonah CPU in mFCPGA479	
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2006/02/23	

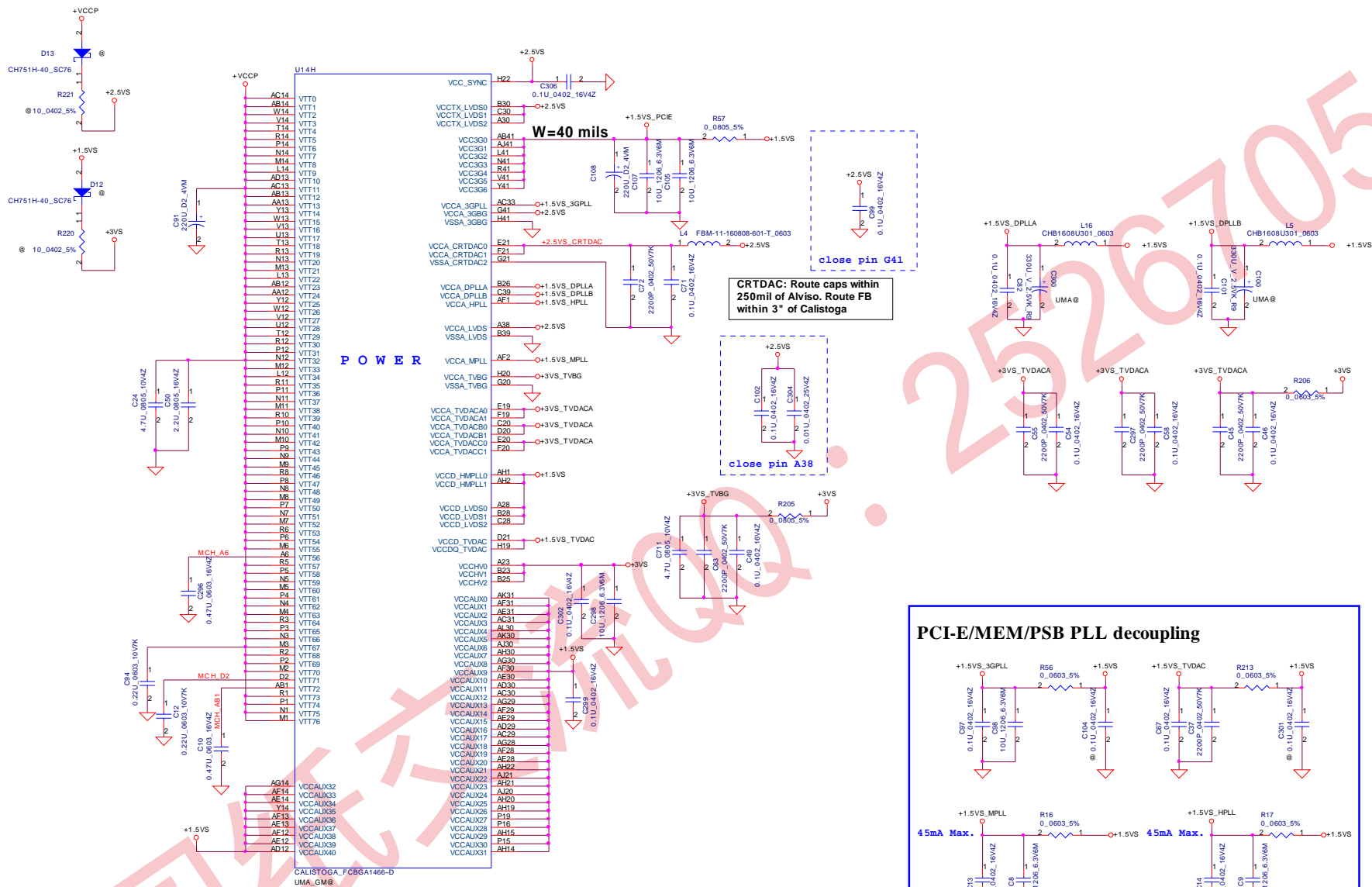


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Strap Pin Table

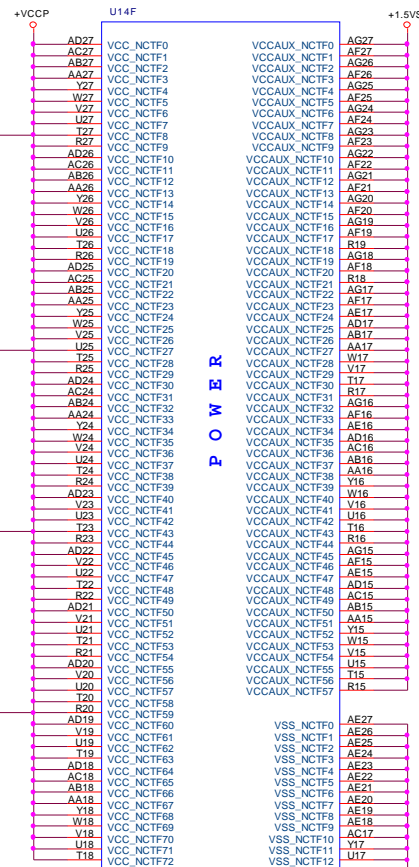
CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU * (Default)
CFG8	0 = Lane Reversal Enable 1 = Normal Operation (Default) *
CFG6	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All 7 Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG10 CFG18	10 = 1.05V * (Default) 01 = 1.5V
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.

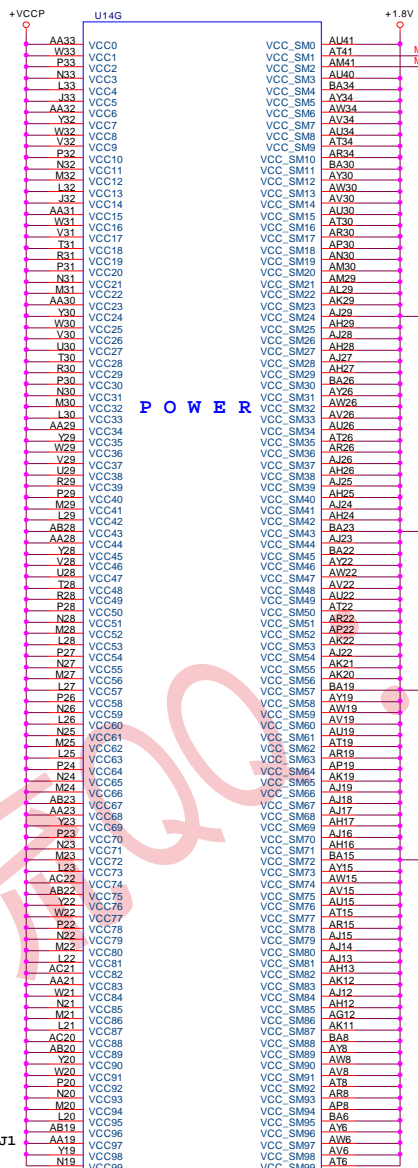
<7> CFG5 R32 1 2 @ 2.2K 0.402 5%
<7> CFG7 R40 1 2 @ 2.2K 0.402 5%
<7> CFG8 R37 1 2 @ 2.2K 0.402 5%
<7> CFG11 R35 1 2 @ 2.2K 0.402 5%
<7> CFG12 R34 1 2 @ 2.2K 0.402 5%
<7> CFG13 R38 1 2 @ 2.2K 0.402 5%
<7> CFG16 R33 1 2 @ 2.2K 0.402 5%

<7> CFG18 R48 1 2 @ 1K 0.402 5%
<7> CFG19 R50 1 2 @ 1K 0.402 5%
<7> CFG20 R51 1 2 @ 1K 0.402 5%



CALISTOGA_FCBGA1466-D
UMA_GM0

Place near pin AV1 & AJ1



CALISTOGA_FCBGA1466-D
UMA_GM0

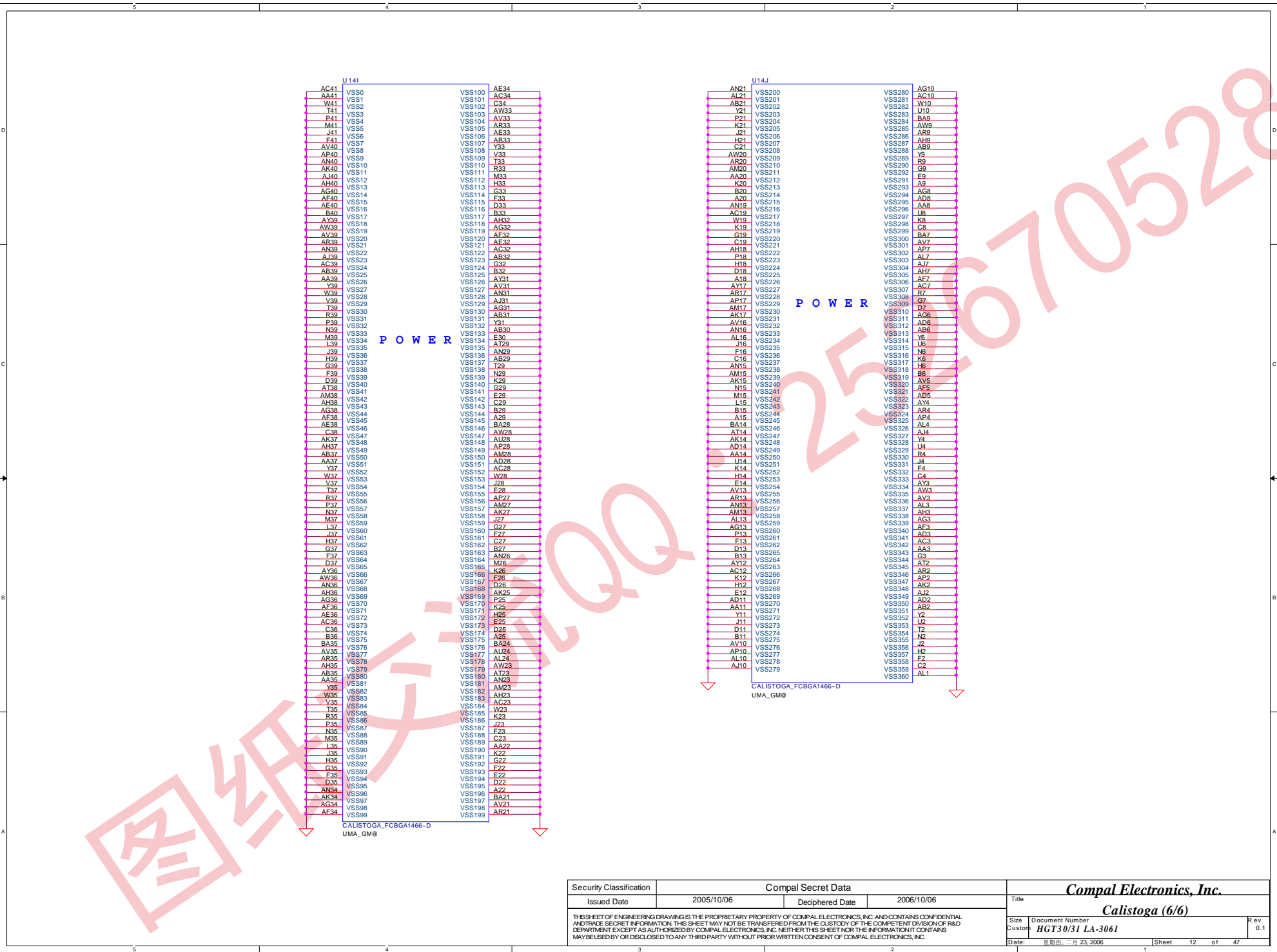
Place near pin AT41 & AM41

Place near pin BA23

Place near pin BA15

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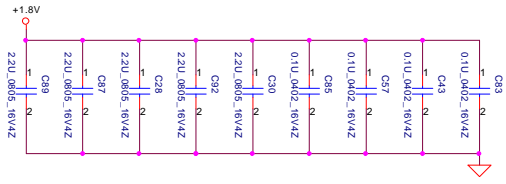
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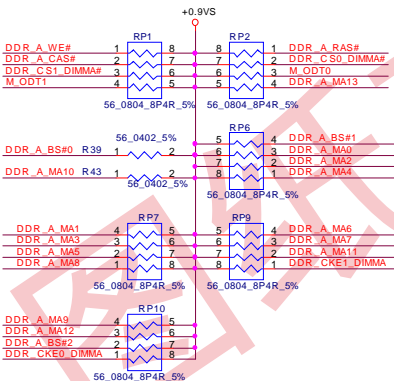
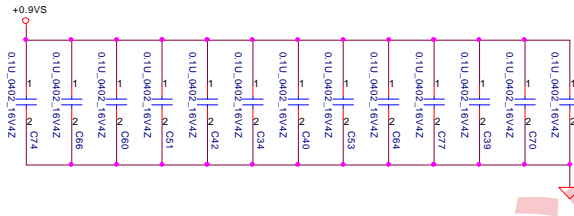
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<8> DDR_A_DQS# [0..7]
 <8> DDR_A_D [0..63]
 <8> DDR_A_DM [0..7]
 <8> DDR_A_DQS [0..7]
 <8> DDR_A_MA [0..13]

Layout Note:
Place near JP41

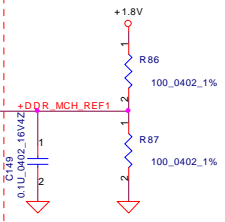


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP41, all trace length Max=1.5"

Layout Note:
+DDR_MCH_REF trace width and spacing is 20/20.



<14,33> EC_P80_DATA

<7> DDR_CKE0_DIMMA

<14,33> EC_P80_CLK
 <8> DDR_A_BS#2

<8> DDR_A_BS#0
 <8> DDR_A_WE#

<8> DDR_A_CAS#
 <7> DDR_CS1_DIMMA#

<7> M_ODT1

DDR_A_D37
 DDR_A_D36

DDR_A_DQS#4
 DDR_A_DQS4

DDR_A_D35
 DDR_A_D32

DDR_A_D40
 DDR_A_D44

DDR_A_D41
 DDR_A_D46

DDR_A_D48

DDR_A_DQS#6
 DDR_A_DQS6

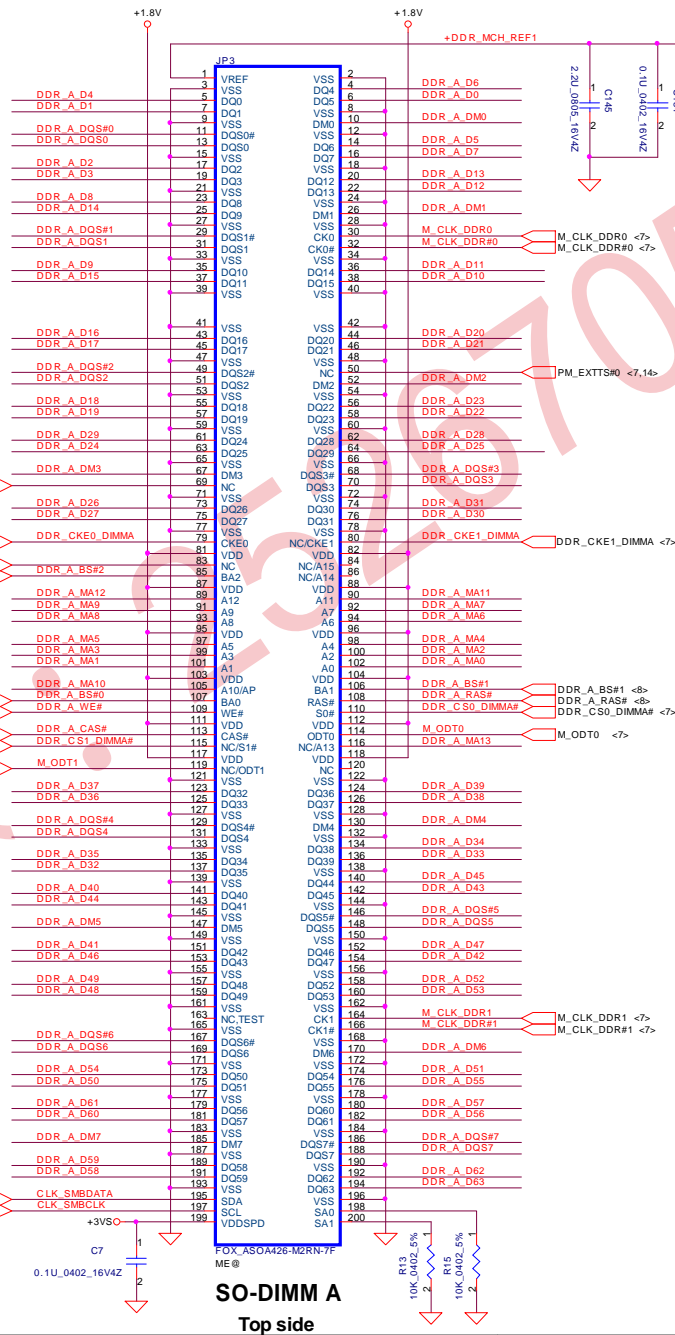
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 DDR_A_D50

DDR_A_D61
 DDR_A_D60

DDR_A_DM7
 DDR_A_D59

DDR_A_D58

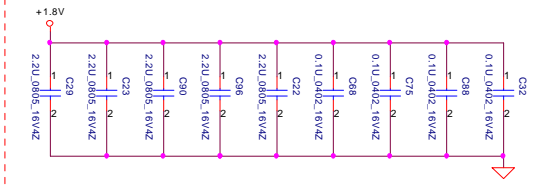
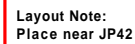
<14,15> CLK_SMBDATA
 <14,15> CLK_SMBCLK



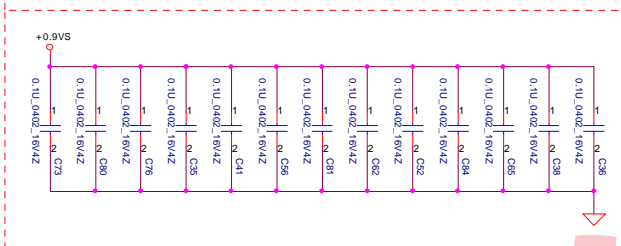
SO-DIMM A

Top side

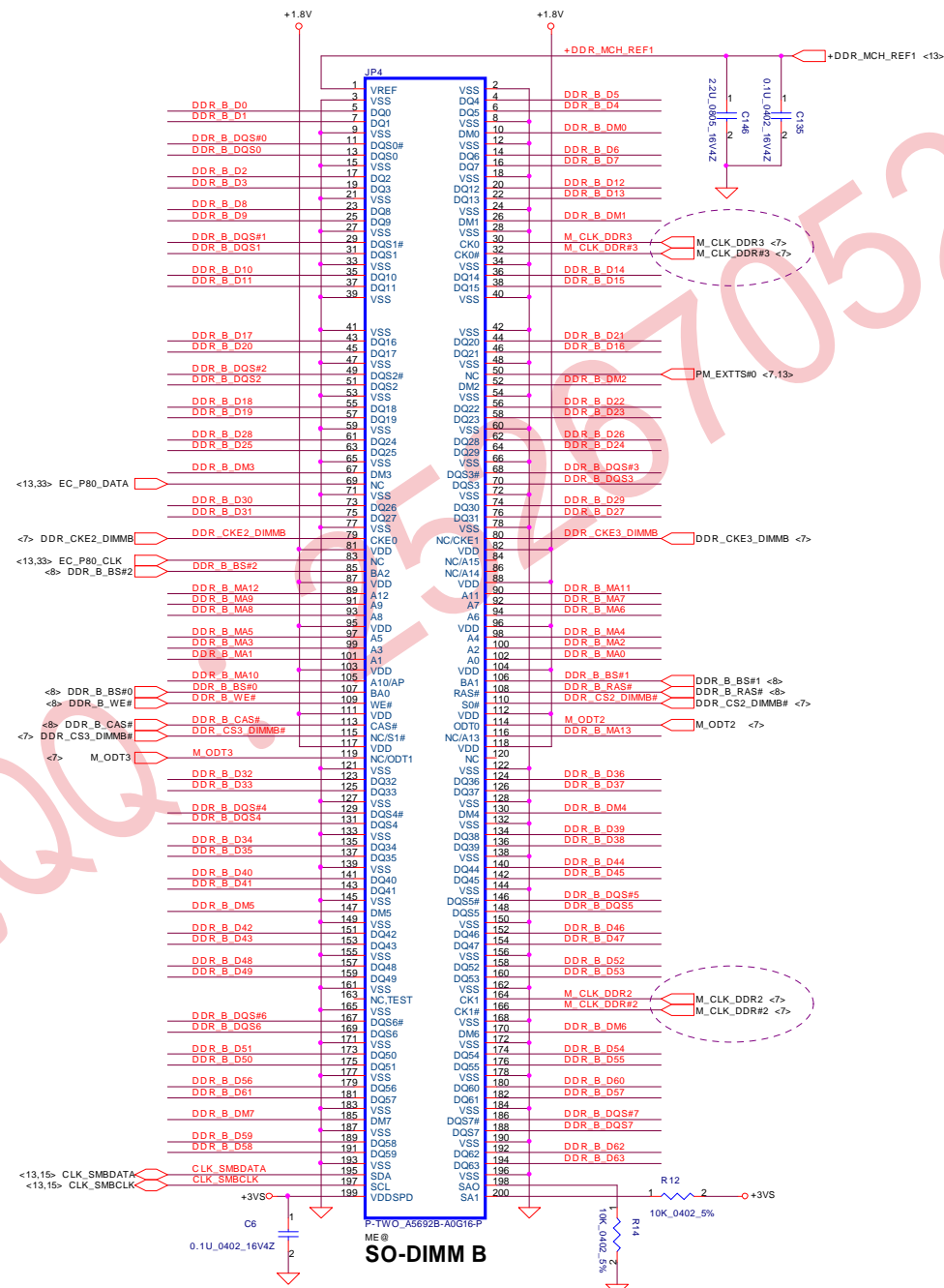
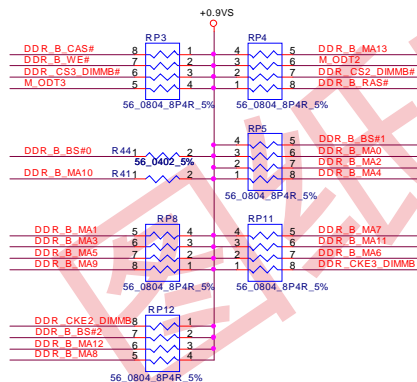
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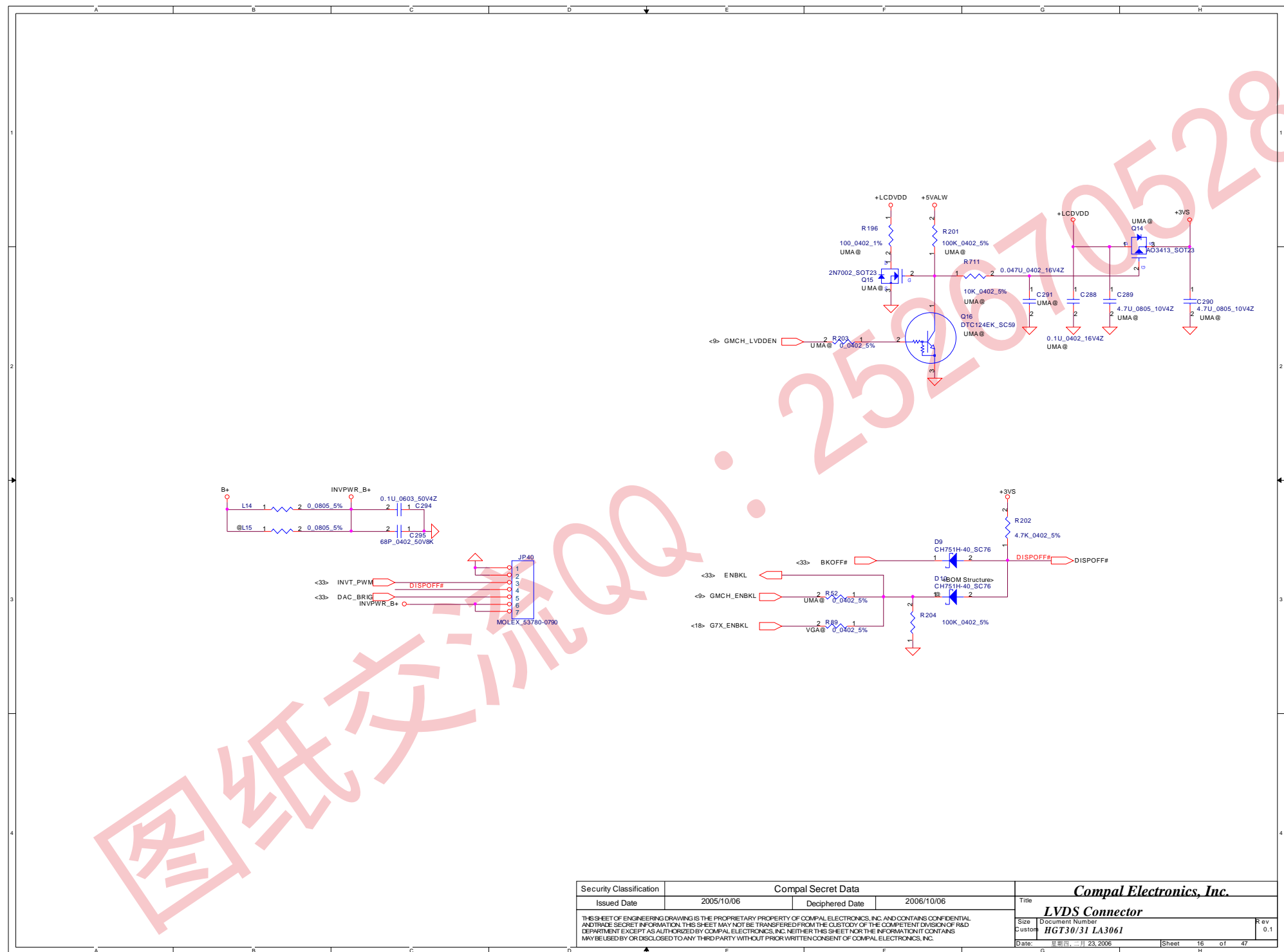
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor
closely JP42,all
trace length Max=1.5"

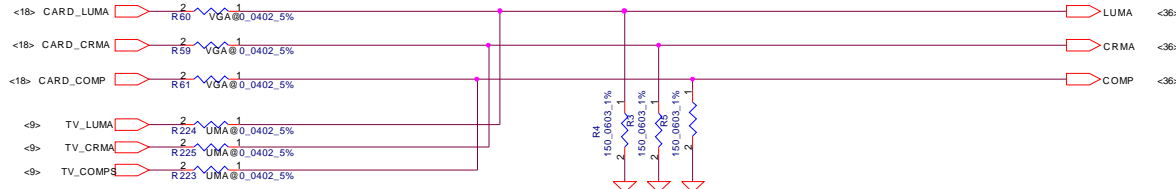


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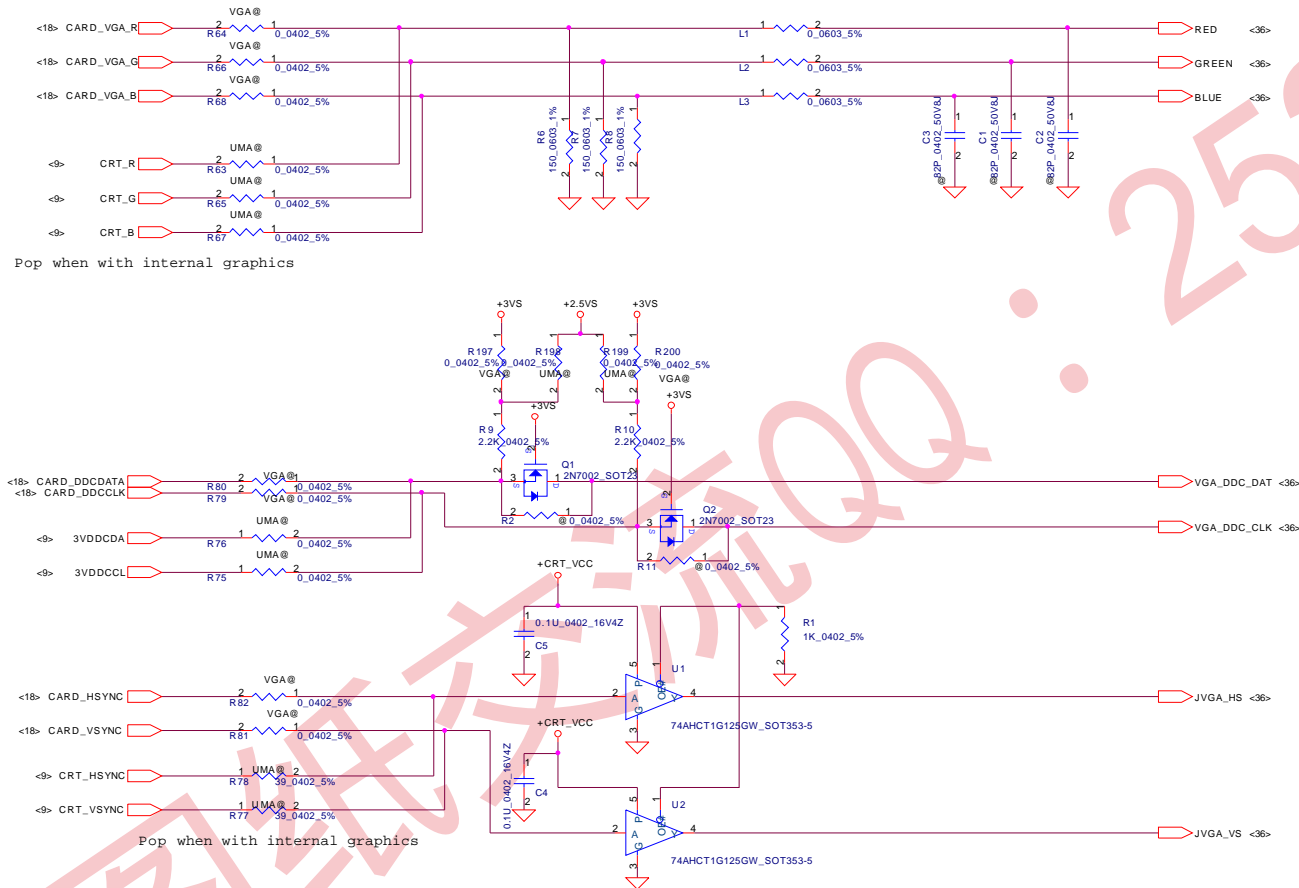


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				Size Document Number
				Custom HGT30/31 LA3061
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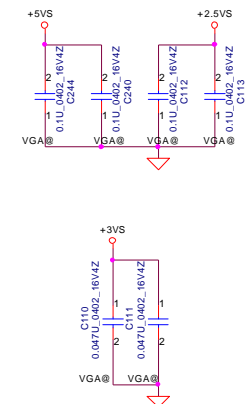
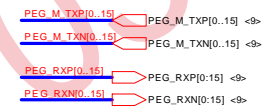
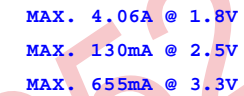
TV-OUT Conn.



CRT Conn.



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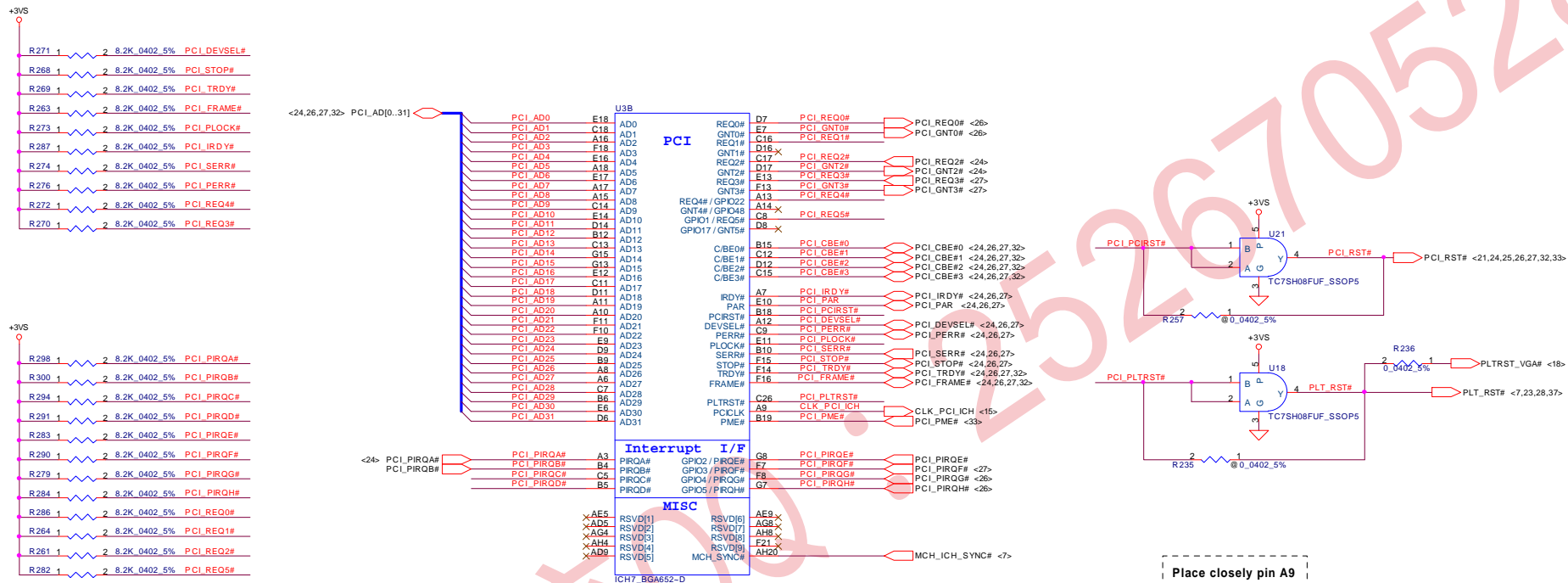
VGA/B connector

Size	Document Number
Custom	HGT30/31 LA3061

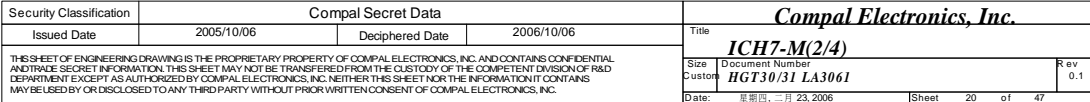
Date: 星期四, 二月 23, 2006

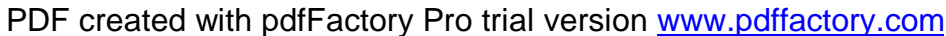
Date: 星期四, 二月 23, 2006 Sheet 18 of 47

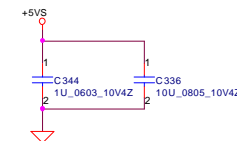
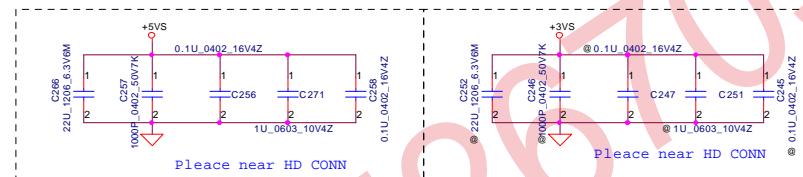
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Size	Document Number	HGT30/31 LA3061		Rev
Date	2006/02/23	Sheet	19	of 47





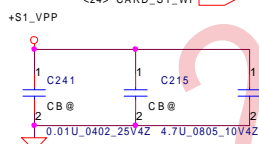


Security Classification		Compal Secret Data		<div> <div>Compal Electronics, Inc.</div> <div> <div>HDD & CDROM</div> <div> <div>Size</div> <div>Document Number</div> <div> <div>HGT30/31 LA3061</div> <div>Rev 0.</div> </div> </div> </div> </div>	
Issued Date	2005/10/06	Deciphered Date	2006/10/06		
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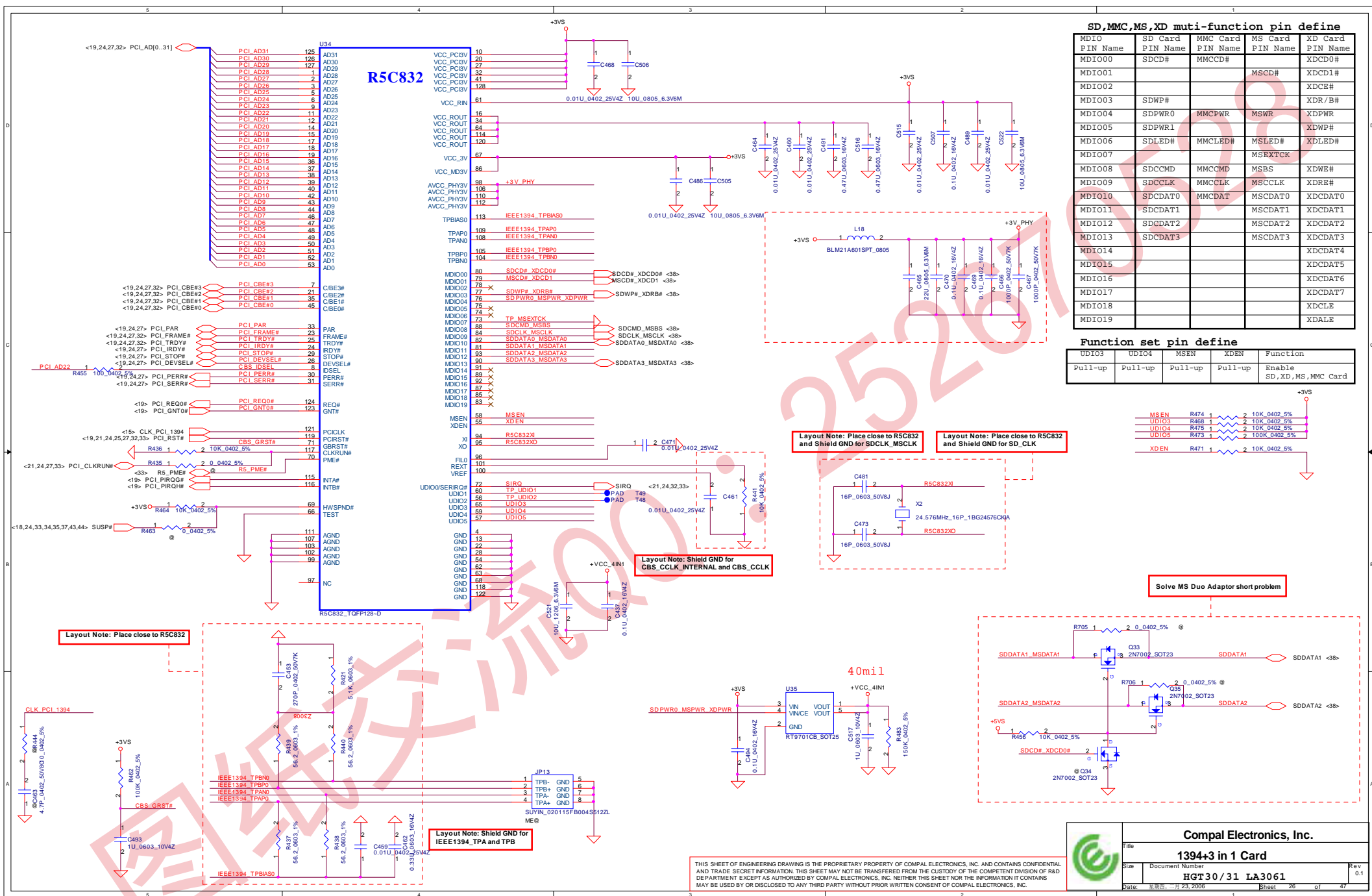
The schematic diagram illustrates the power supply configuration for the CP-22T11-SSOP16 component. The power pins are connected to external sources and decoupling capacitors as follows:

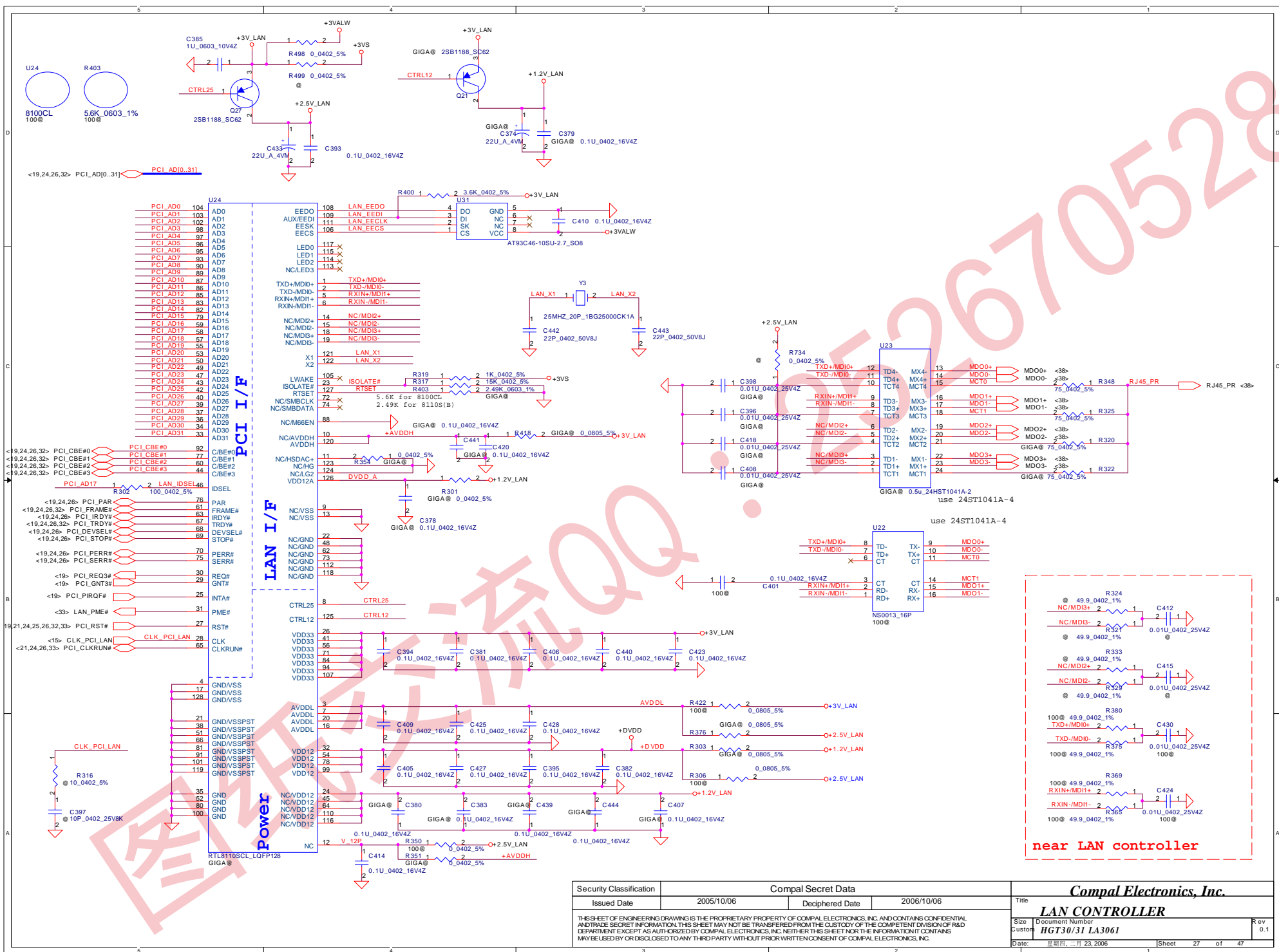
- VCC (13, 12, 11):** Connected to +12V (pin 9).
- VPP (10):** Connected to +S1_VPP (pin 1).
- VCCD0 (1), VCCD1 (2):** Connected to +5VS (pin 1) through decoupling capacitors C193 and C194 (10U_1206_10V4Z, 0.1U_0402_16V4Z).
- VPPD0 (15), VPPD1 (14):** Connected to +3VS (pin 1) through decoupling capacitors C197 and C198 (0.1U_0402_16V4Z).
- OC (8):** Connected to +S1_VCC (pin 1) through decoupling capacitor C210 (0.1U_0402_16V4Z).
- GND (7, 16):** Connected to GND (pin 7).
- STBDN (16):** Connected to GND (pin 7).

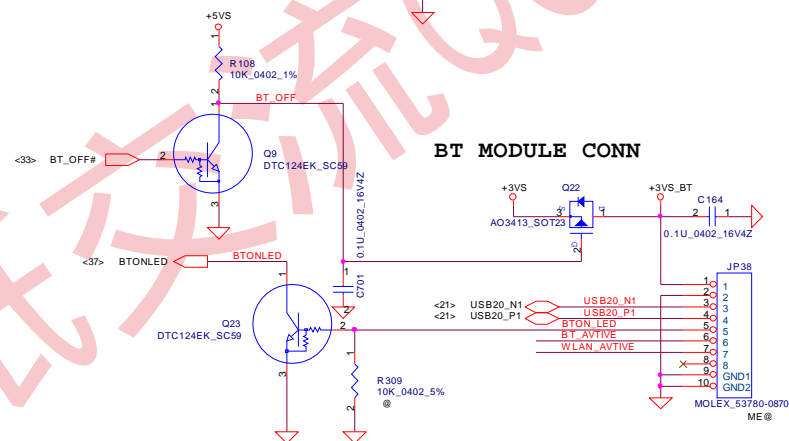
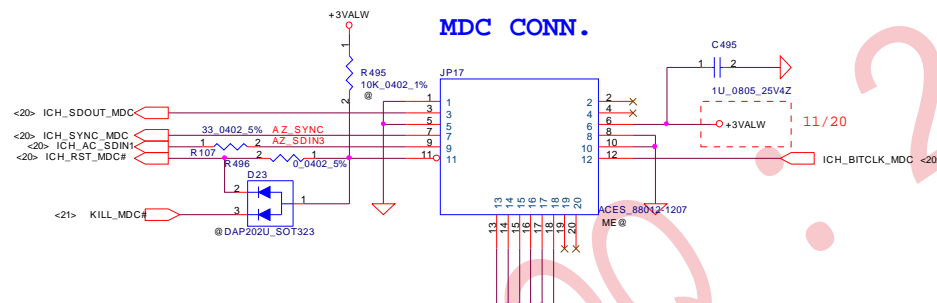
The component is labeled US, and the package is CP-22T11-SSOP16.



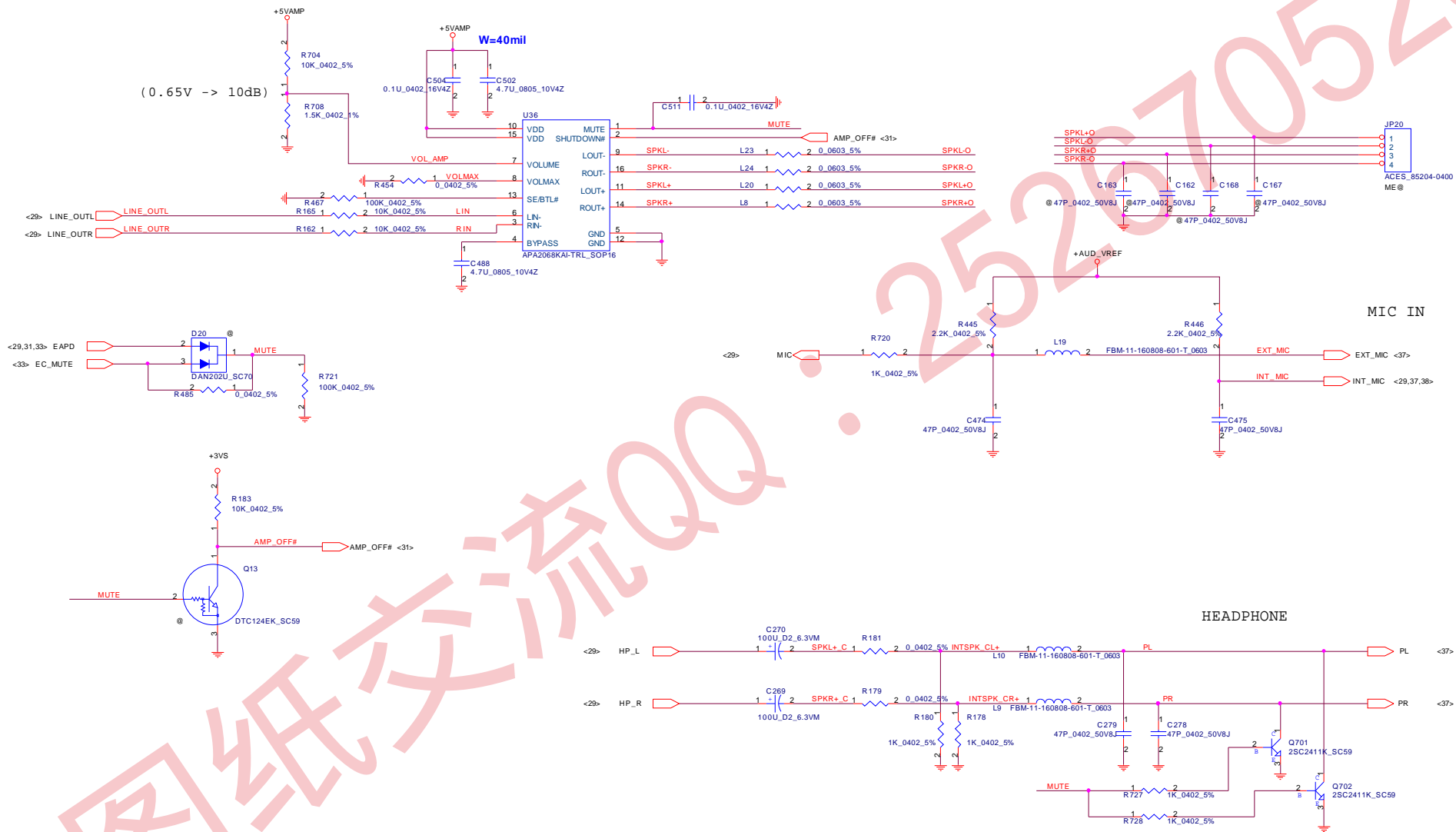
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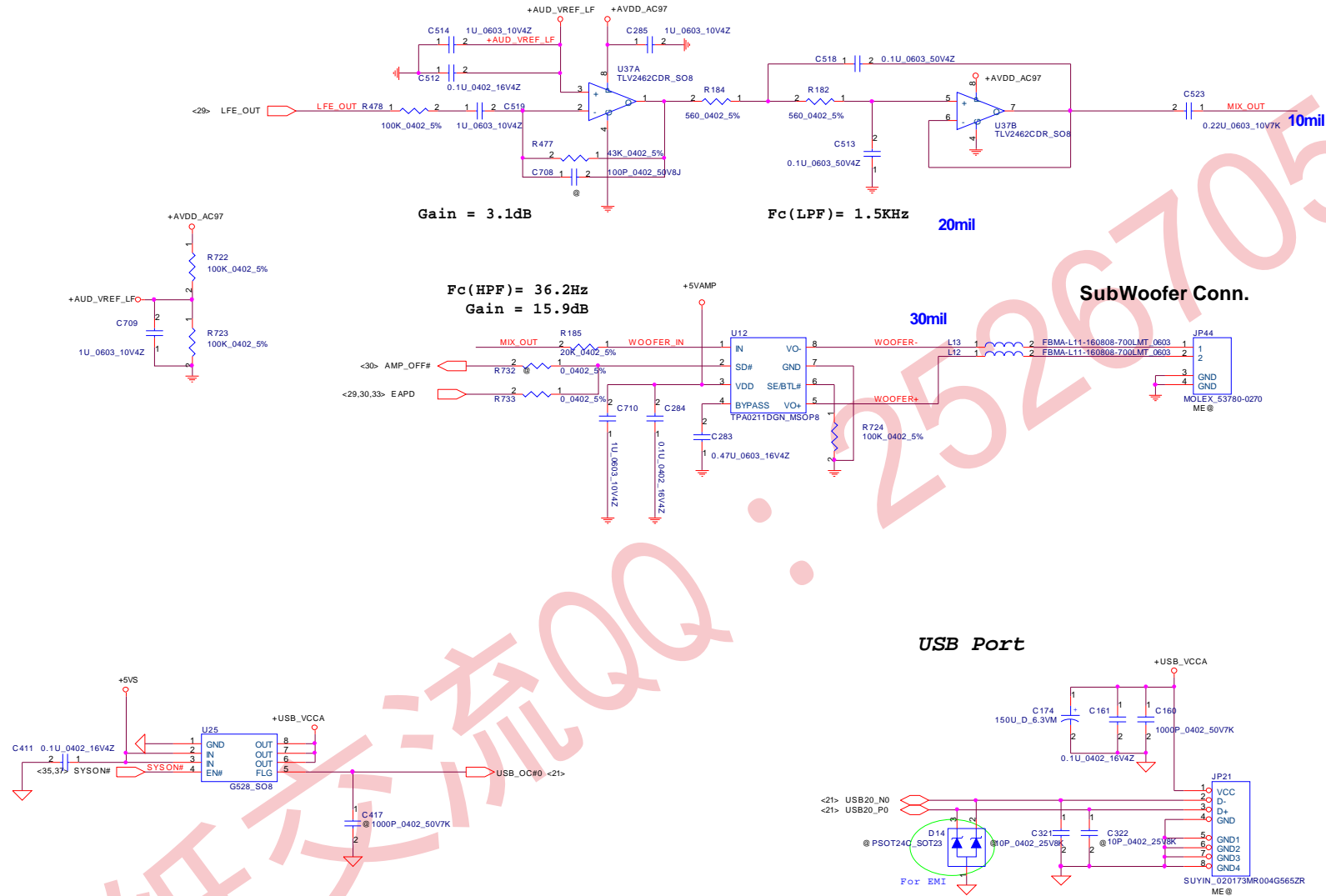
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Issued Date	2005/10/06	Deciphered Date	2006/10/06		
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				Custom	0.
				Document Number HGT30/31 LA3061	
Date:		星期四, 二月 23, 2006		Sheet	28 of 47



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				Size Document Number Custom HGT30/31 LA3061
Date: 2006/03/23	Rev	0.1	Sheet	30 of 47

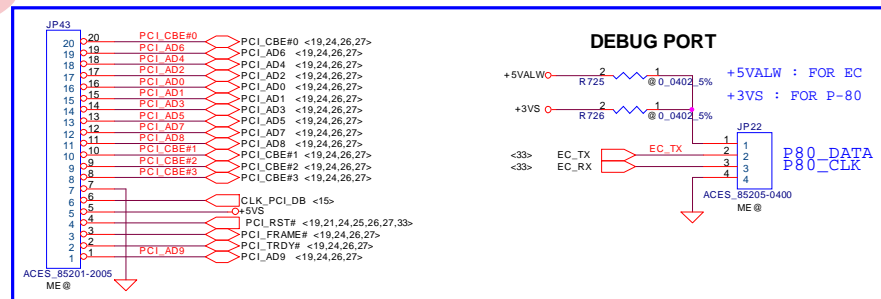
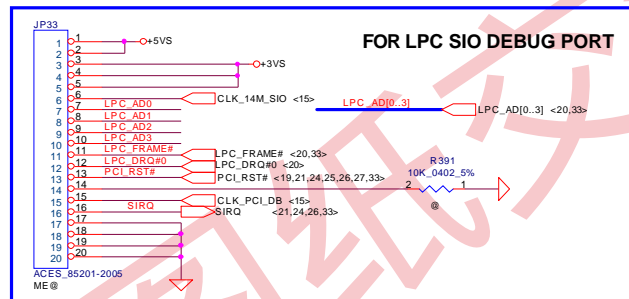
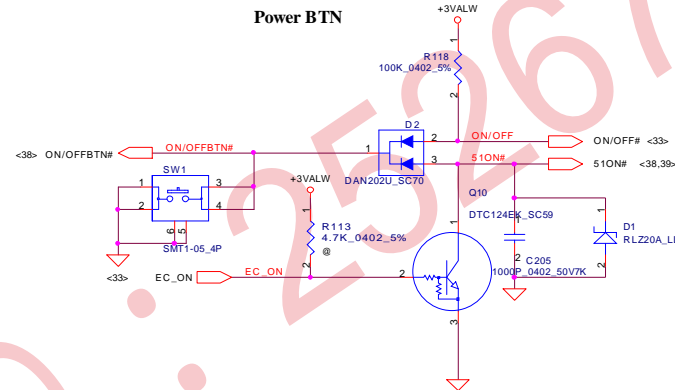
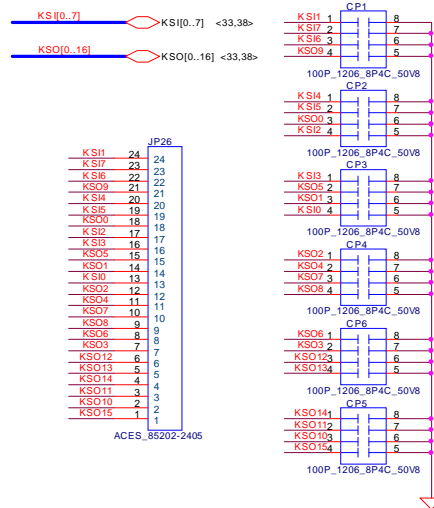
SUBWOOFER (Reserved for C38)

WOOFER@

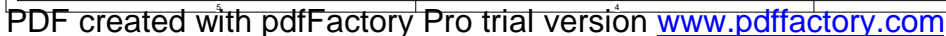


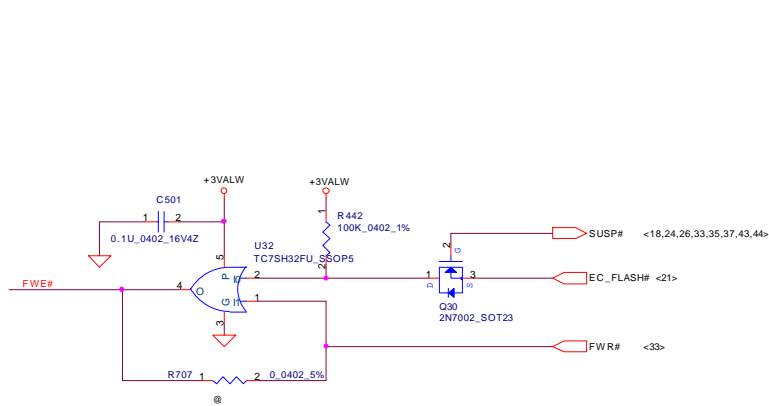
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Size	Document Number	Rev		
Custom	HGT30/31 LA3061	0.1		
Date	星期二, 二月 23, 2006	Sheet	31 of 47	

INT_KBD CONN.(TYPE "D" KB)



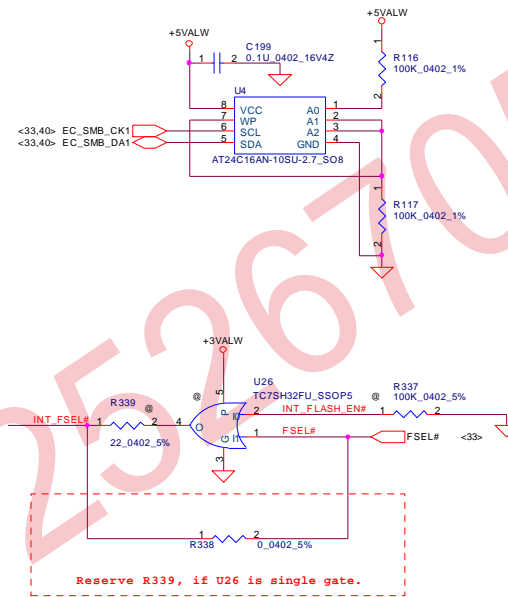
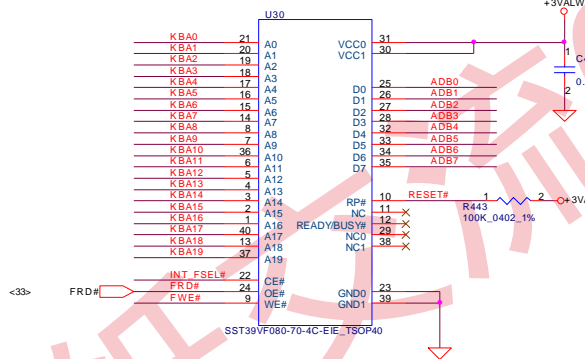
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Issued Date		Deciphered Date		Title	
2005/10/06		2006/10/06		KBD,ON/OFF,T/P,LED/B,DEBUG	
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		Date:		Rev	
		2006/03/23		0.1	
		Sheet		32 of 47	



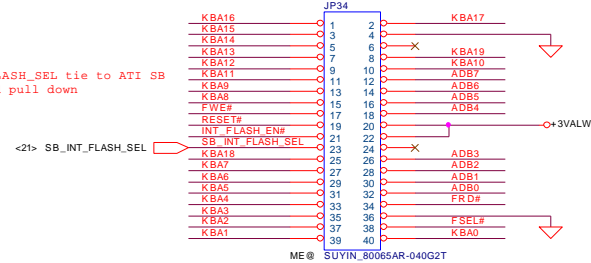


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<33> ADB[0..7] ADB[0..7]

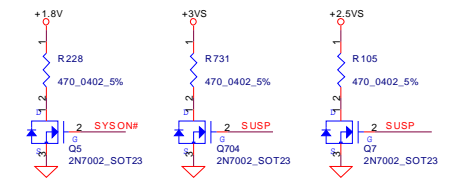
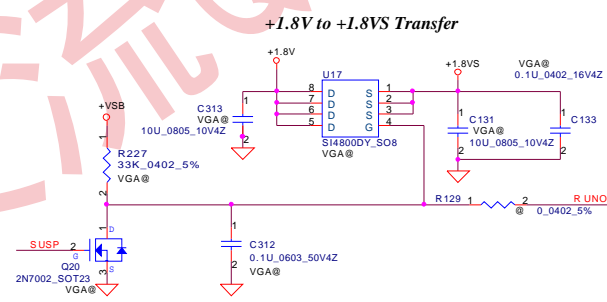
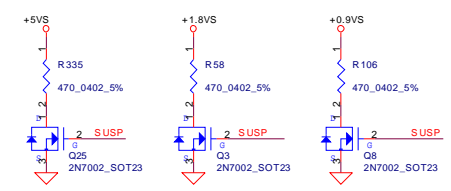
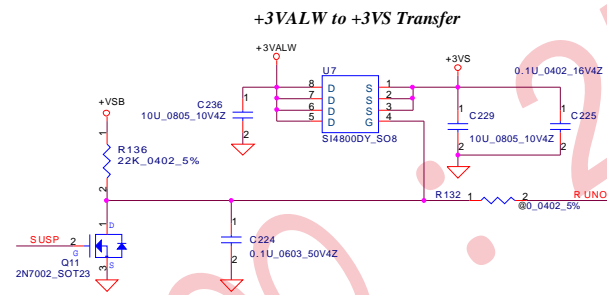
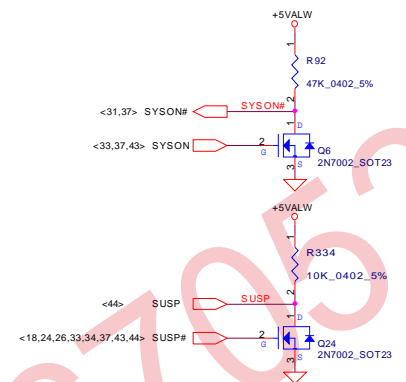
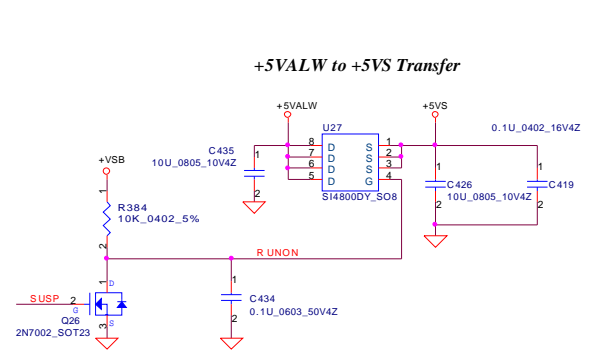
1MB Flash ROM



1MB ROM Socket



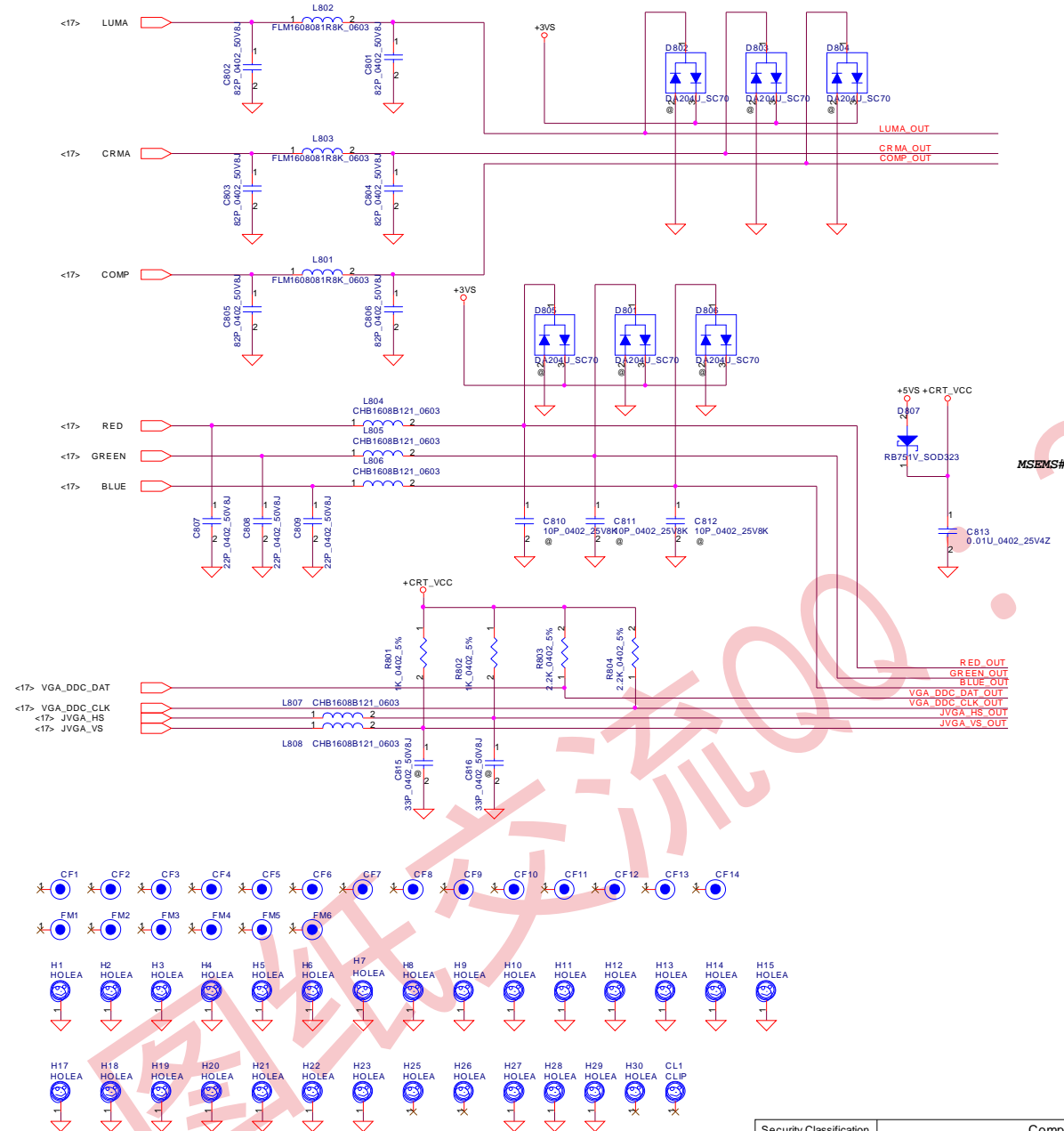
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Size Custom				Document Number
Date				HGT30/31 LA3061
Date				Rev 0.1
Date				Sheet 34 of 47



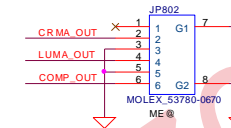
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				Size
				Custom
				Document Number
				HGT30/31 LA3061
				Rev
				0.1
				Date
				星期四, 三月 23, 2006
				Sheet
				35 of 47

CLOSE TO JTVOUT1

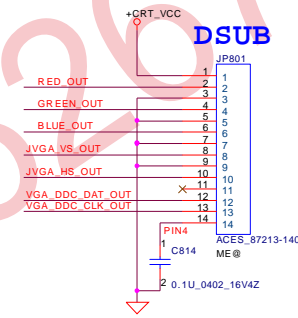
VGA I/O PORT Connector



S-VIDEO



DSUB

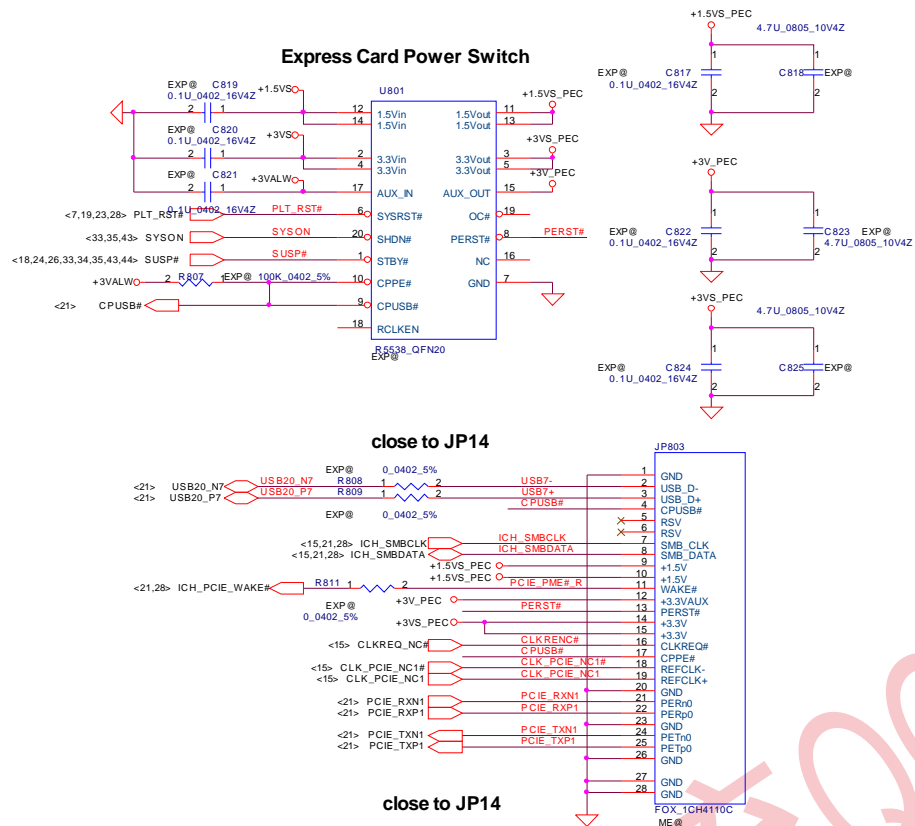


PIN ASSIGNMENT

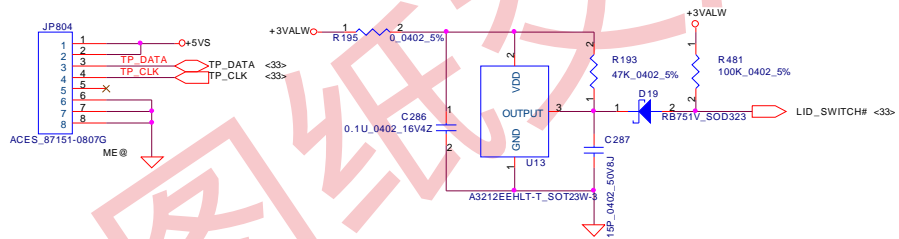
PIN	D-SUB	FUNCTION	PIN	SVIDEO	FUNCTION
1	9	+CRT_VCC	1	1	NC
2	1	RED	2	4	CRMA
3	6	GND	3	2	GND
4	2	GREEN	4	3	LUMA
5	7	GND	5	5	GND
6	3	BLUE	6	6	CVBS
7	8	GND			
8	14	VSYNC			
9	10	GND			
10	13	HSYNC			
11	11	SENSE			
12	12	SM_DAT			
13	15	SM_CLK			
14	4	PIN4			

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				Date	Rev 0.1
				Sheet	36 of 47

NEW CARD FOR C38

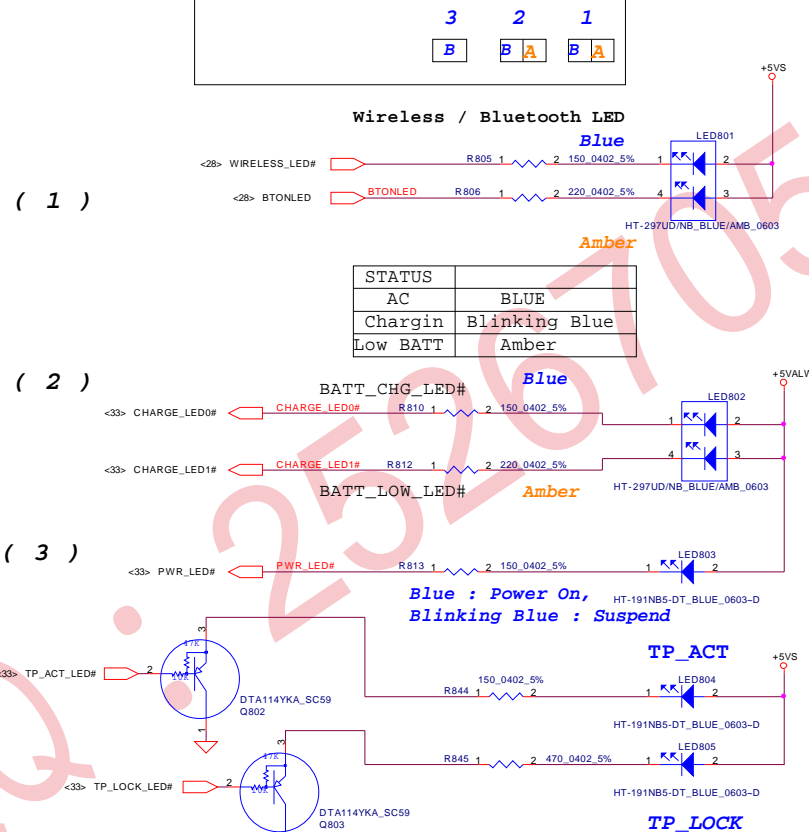


T/P Board

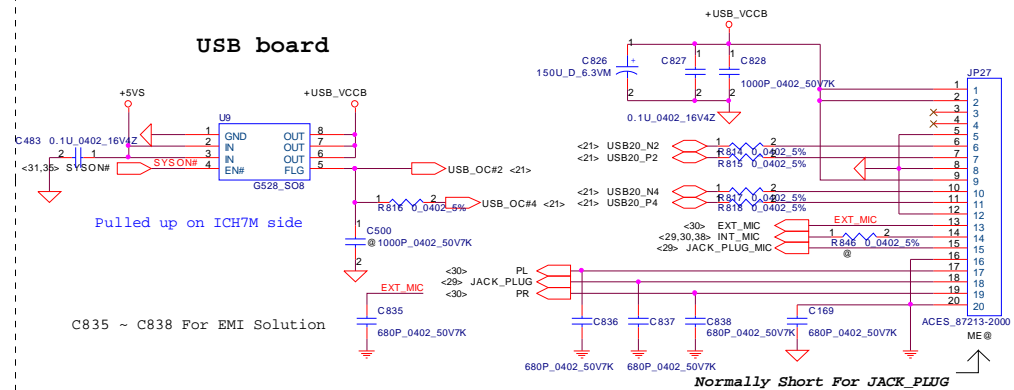


LID Switch

LED Indicator ON M/B



USB board



Normally Short For JACK_PLUG

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				Custom	HGT30/31 LA3061	0.
				Date:	星期四, 二月 23, 2006	Sheet 37 of 47

3 IN 1 Card Reader

JP806
3 IN 1 MS/SD/MMC Connector

MS INTERFACE
SD INTERFACE

TAISO_143-2300302900_23P_LB

ME @

Connections:

- SDATA2, SDATA3, SDCMD, MSBS, +VCC_4IN1, SDCLK_MSCLK, SDATA0, MSDATA0, SDATA1, SDCD#, XDCD0#, SDWP#, XDRB#
- VSS_MS, VCC_MS, SCLK_MS, DAT3_MS, INS_MS, DAT2_MS, VSS_SD, DAT0_SD, DAT1_SD, GND_SD, WP_SD, GND_SD, GND
- SDCLK_MSCLK, SDATA3, MSDATA3, MSCD#, XDCD1, SDATA2, SDATA0, MSDATA0, SDATA1, SDCMD, MSBS
- VCC_4IN1, SDCLK_MSCLK, SDATA3, MSDATA3, MSCD#, XDCD1, SDATA2, SDATA0, MSDATA0, SDATA1, SDCMD, MSBS, SDCMD_MSBS

UMA LCD/PANEL Conn.

JP805 (60 MIL)

Connections:

- GND, LCDVDD, +3VS, EDID_CLK_LCD, EDID_DAT_LCD, LVDSB0+, LVDSB0-, LVDSB1+, LVDSB1-, LVDSB2+, LVDSB2-, LVDSB3+, LVDSB3-, LVDSB4+, LVDSB4-, LVDSB5+, LVDSB5-, LVDSB6+, LVDSB6-, LVDSB7+, LVDSB7-, LVDSB8+, LVDSB8-, LVDSB9+, LVDSB9-, LVDSB10+, LVDSB10-, LVDSB11+, LVDSB11-, LVDSB12+, LVDSB12-, LVDSB13+, LVDSB13-, LVDSB14+, LVDSB14-, LVDSB15+, LVDSB15-, LVDSB16+, LVDSB16-, LVDSB17+, LVDSB17-, LVDSB18+, LVDSB18-, LVDSB19+, LVDSB19-, LVDSB20+, LVDSB20-, LVDSB21+, LVDSB21-, LVDSB22+, LVDSB22-, LVDSB23+, LVDSB23-, LVDSB24+, LVDSB24-, LVDSB25+, LVDSB25-, LVDSB26+, LVDSB26-, LVDSB27+, LVDSB27-, LVDSB28+, LVDSB28-, LVDSB29+, LVDSB29-, LVDSB30+, LVDSB30-

FOX_GS23302-1010S-7F

ME @

Pinout diagram for the FOX GS23302-10T05-FP LCD module. The diagram shows a 30-pin connector on the left and a 60 MIL connector on the right. Pin 1 is GND, Pin 2 is GND, Pin 3 is GND, Pin 4 is EDID_CLK_LCD, Pin 5 is EDID_DAT_LCD, Pin 6 is EDID_CLK_LCD, Pin 7 is EDID_DAT_LCD, Pin 8 is LVDSB0+, Pin 9 is LVDSB0-, Pin 10 is LVDSB1+, Pin 11 is LVDSB1-, Pin 12 is LVDSB2+, Pin 13 is LVDSB2-, Pin 14 is LVDSB3+, Pin 15 is LVDSB3-, Pin 16 is LVDSB0+, Pin 17 is LVDSB0-, Pin 18 is LVDSB1+, Pin 19 is LVDSB1-, Pin 20 is LVDSB2+, Pin 21 is LVDSB2-, Pin 22 is LVDSB3+, Pin 23 is LVDSB3-, Pin 24 is LVDSB0+, Pin 25 is LVDSB0-, Pin 26 is LVDSB1+, Pin 27 is LVDSB1-, Pin 28 is LVDSB2+, Pin 29 is LVDSB2-, Pin 30 is LVDSB3+, Pin 31 is GND, Pin 32 is GND. The diagram also shows connections for +LCDVDD, +3VS, and LVDSB0+ to LVDSB3+.

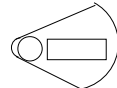
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SWITCH BD

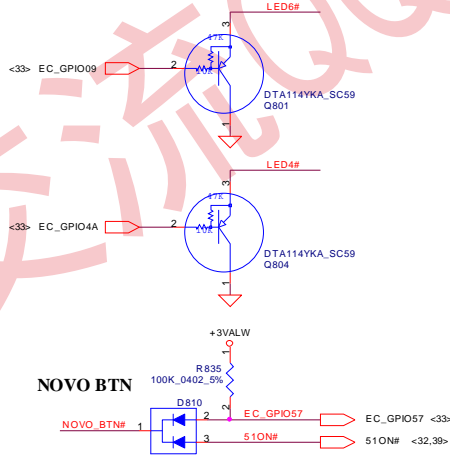
LED Indicator BD					
1	2	3	4	5	6
L		M			H

Function

KEY Matrix	K016	K017
KS10	DW-UP	DW-DOWN
KS11	DW-ENTER	MUTE



Dial Wheel



LED6#

LED4#

+3VALW

R835 100K_0402_5%

D810

NOVO_BTN#

EC_GPIO57

S10N#

EC_GPIO57 <33>

S10N# <32,39>

DAN202U_SC70



2520

NOVA_BTN#

+5VALW

+5VS

+VCC5_LED

C829

1 2

1000P_0402_50V7K

R519 0_0402_5%

R820 0_0402_5%

R821 1 2 220_0402_5%

R822 1 2 220_0402_5%

R823 1 2 220_0402_5%

R824 1 2 220_0402_5%

R825 1 2 220_0402_5%

R826 1 2 220_0402_5%

KSO16

KSO17

KSI0

KSI1

LED6#

LED4#

EC_GPIO55

EC_GPIO1D

EC_GPIO4D

EC_GPIO4C

<29,30,37> INT_MIC

0.1U_0402_16V4Z

0.1U_0402_16V4Z

0.1U_0402_16V4Z

C830 1 2

C831 1 2

C832 1 2

ON/OFFBTN#

EC_GPIO59

WIRE_LAN_BTN#

NOVO_BTN#

HDD

SATA_LED#

CD-ROM

ODD_LED#

CAPS_LED#

NUM_LED#

D808

D809

CH751H-40_SC76

CH751H-40_SC76

R829 100K_0402_5%

R830 100K_0402_5%

R831 100K_0402_5%

R832 1 2 220_0402_5%

R833 1 2 220_0402_5%

R834 1 2 220_0402_5%

+3VS

JP808

20

19

18

17

16

15

14

13

12

11

10

9

8

7

6

5

4

3

2

1

ME@

ACES_87151-2007L-N

C839 1000P_0402_50V7K

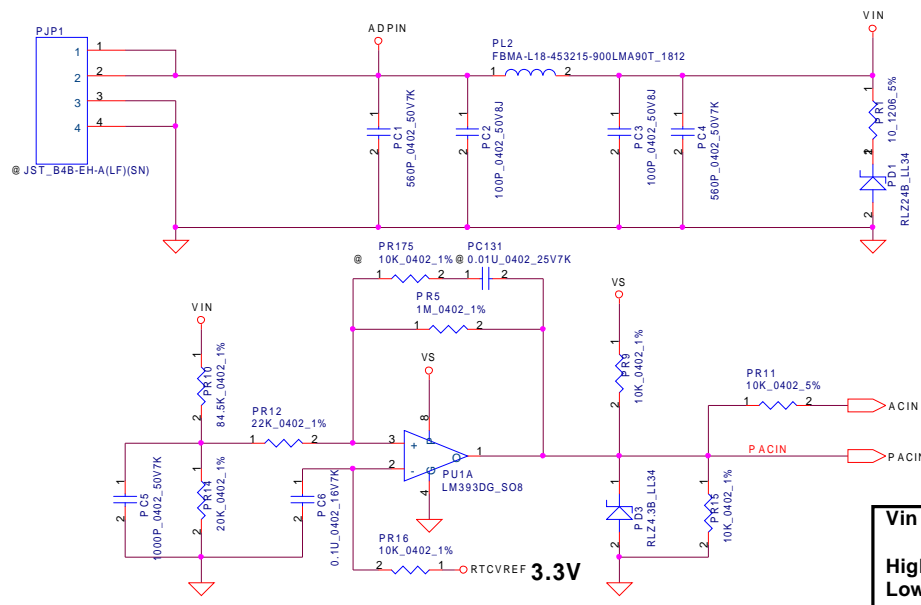
C841 470P_0402_50V8J

C842 1000P_0402_50V7K

C839, C841, C842 For EMI Solution

✓

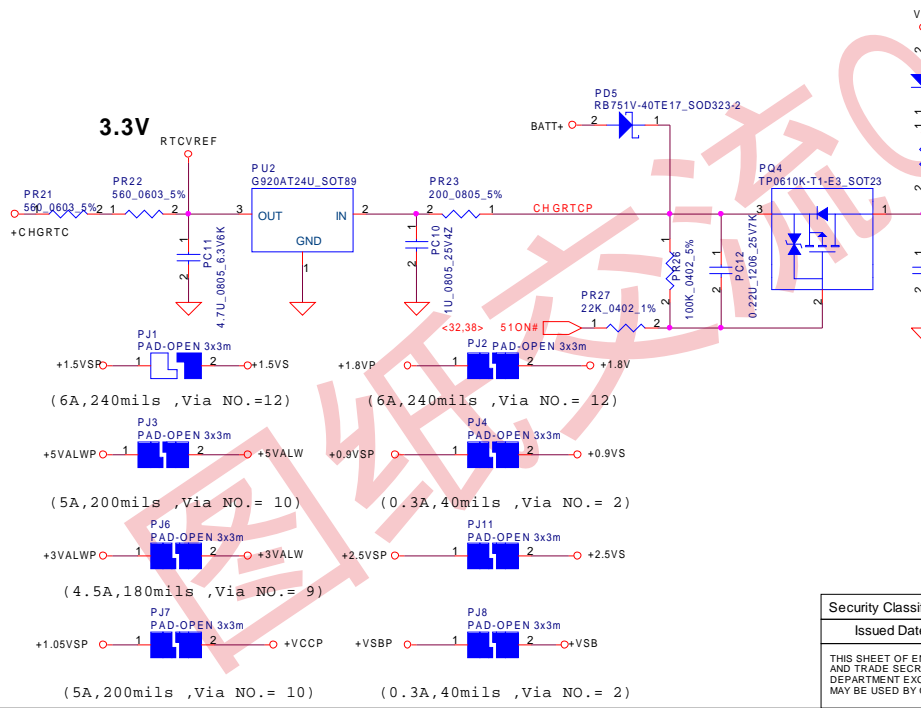
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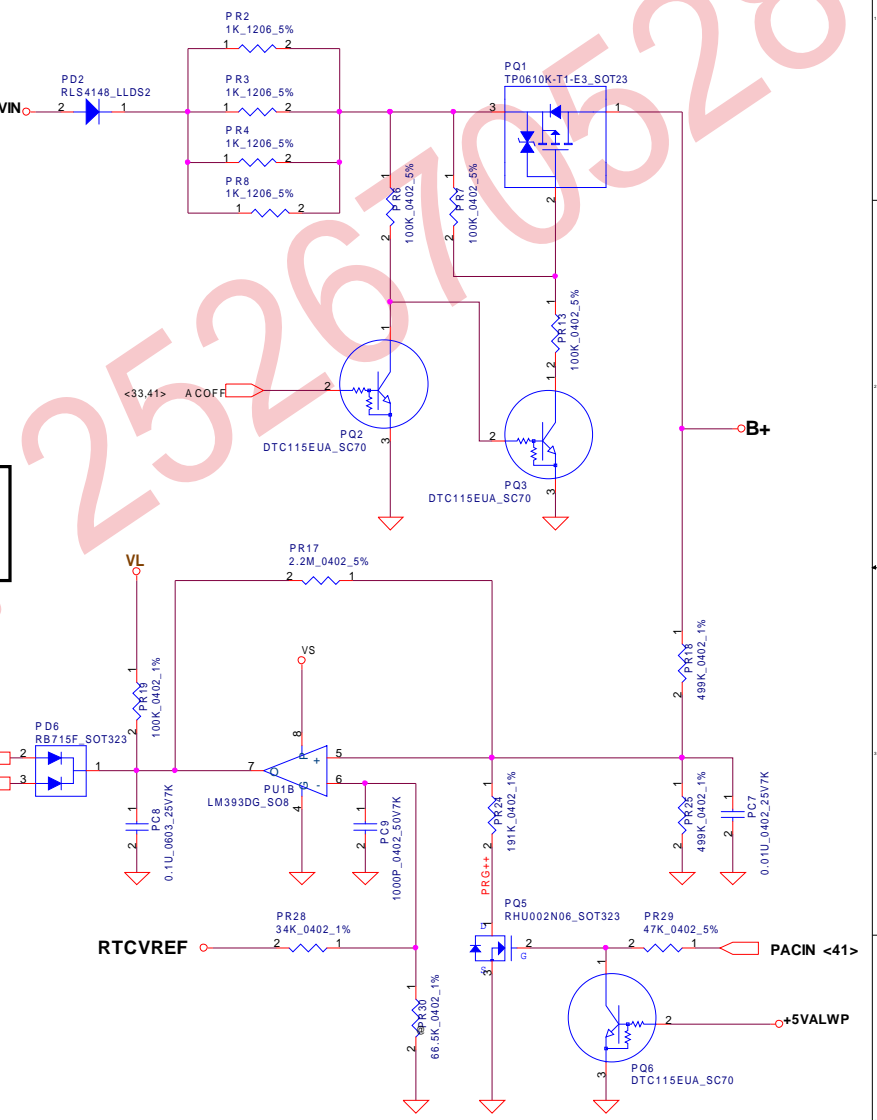
Vin Detector			
High	18.384	17.901	17.430
Low	17.370	16.907	16.630

ACIN			
Precharge detector			
	Min.	typ.	Max.
H-->L	14.620V	14.853V	15.245V
L-->H	15.534V	15.970V	16.421V

BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H-->L	6.169V	6.231V	6.361V
L-->H	7.168V	7.349V	7.537V



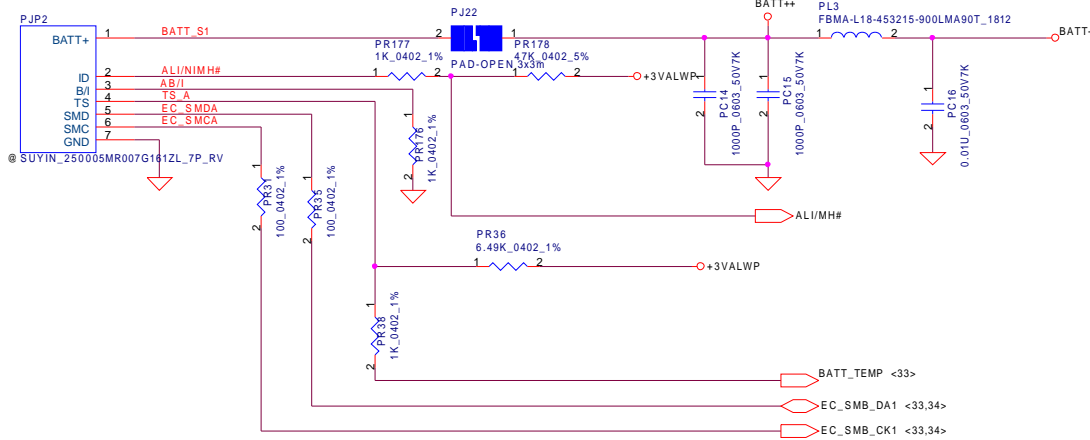
Vin Detector			
High	18.384	17.901	17.430
Low	17.370	16.907	16.630



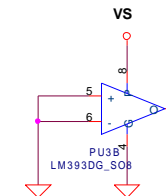
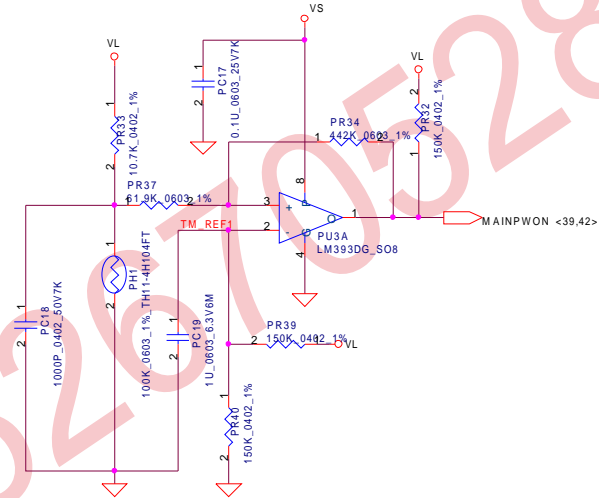
Security Classification	Compal Secret Data	
Issued Date	2005/08/01	Deciphered Date
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PH1 under CPU bottom side :
 CPU thermal protection at 85 degree C
 Recovery at 70 degree C

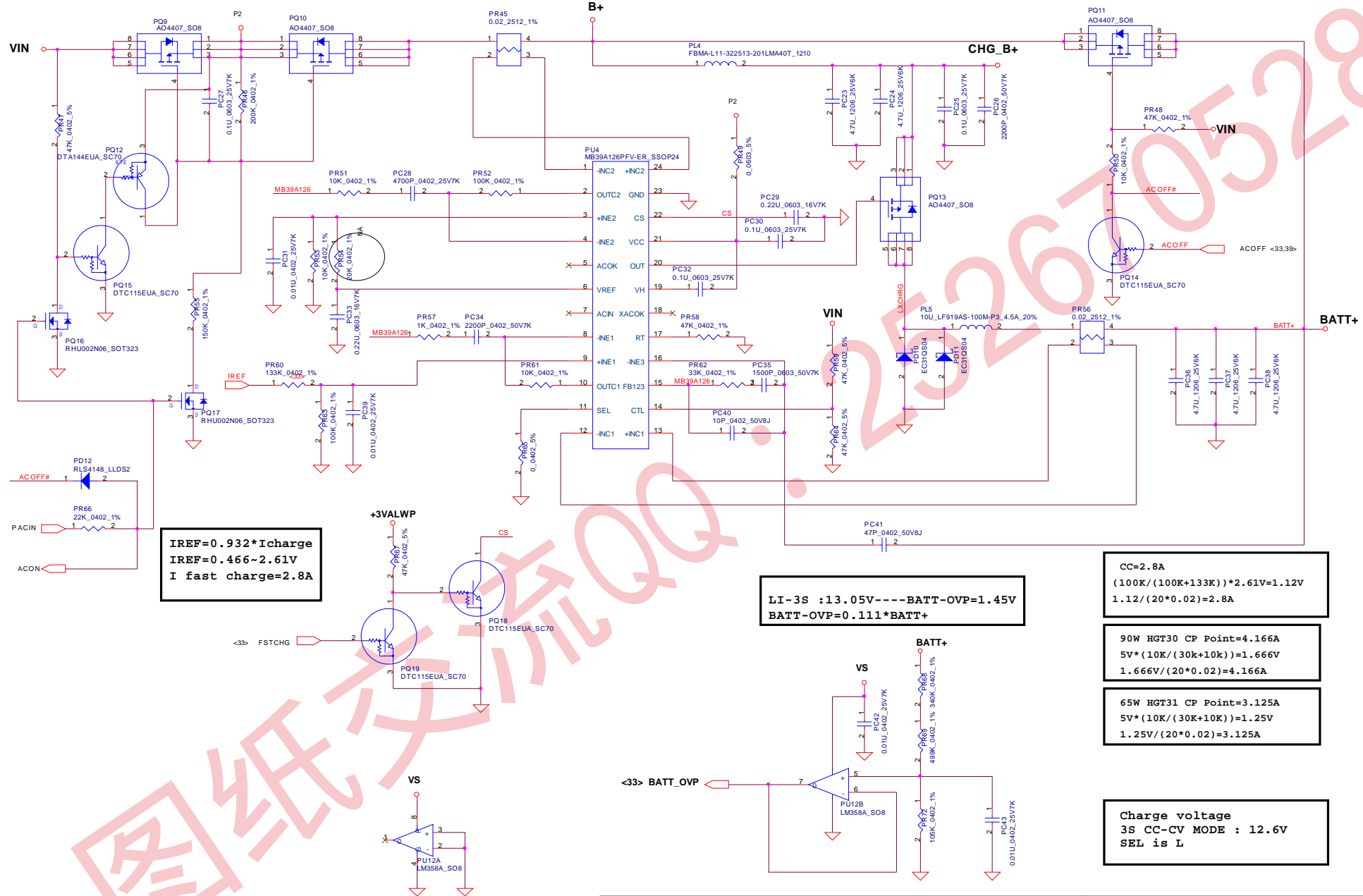


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				BATTERY CONN. / OTP	
				Size	Document Number
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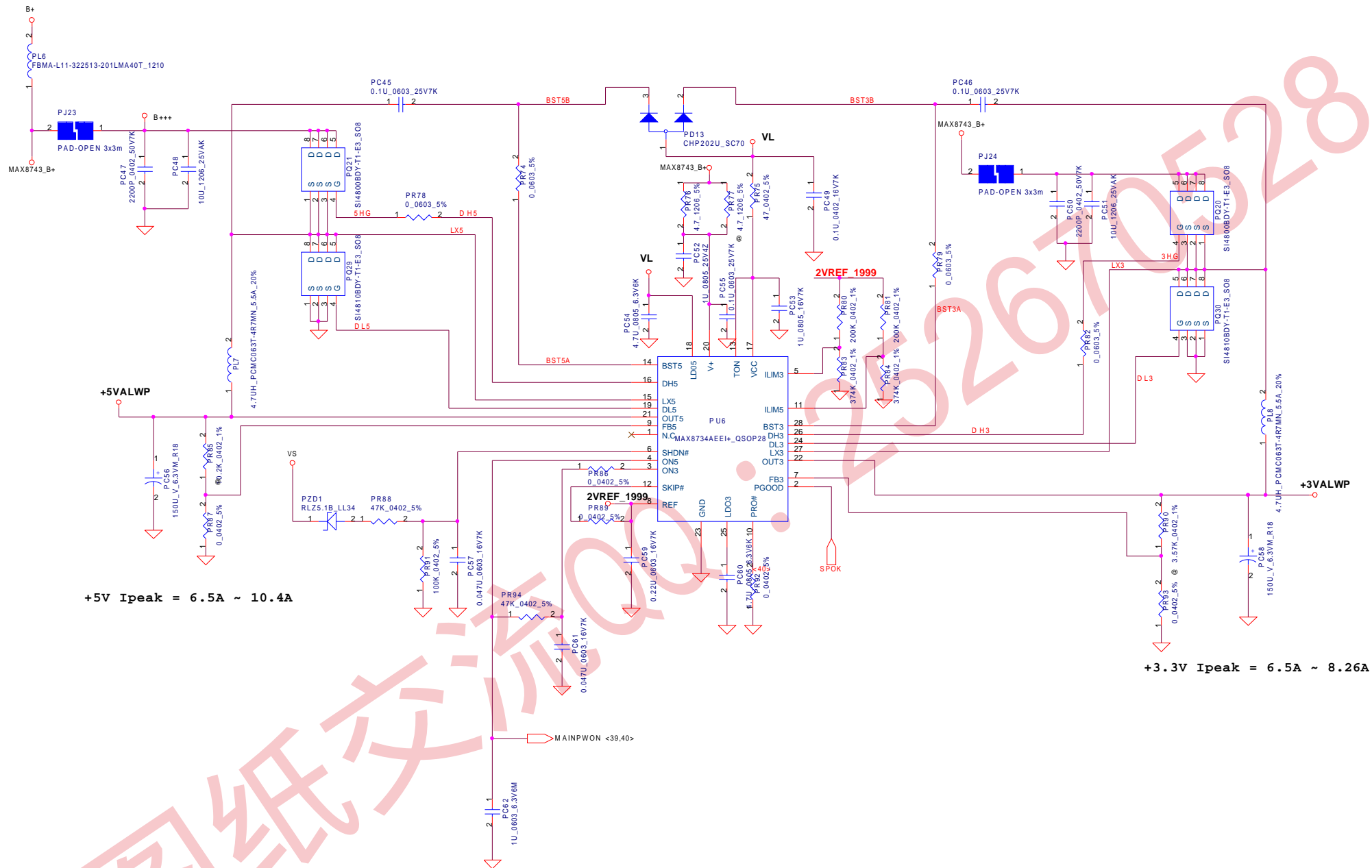
65W PR45=0.02_2512_1% PR54=30K_0402_1% Iadp=0~3.125A
90W PR45=0.02_2512_1% PR54=20K_0402_1% Iadp=0~4.166A

Fosc=14100/Rt=14100/47=300KHz

Charger

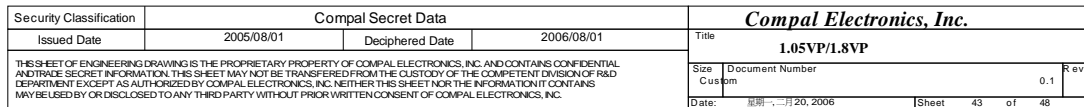


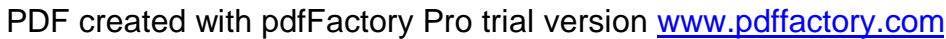
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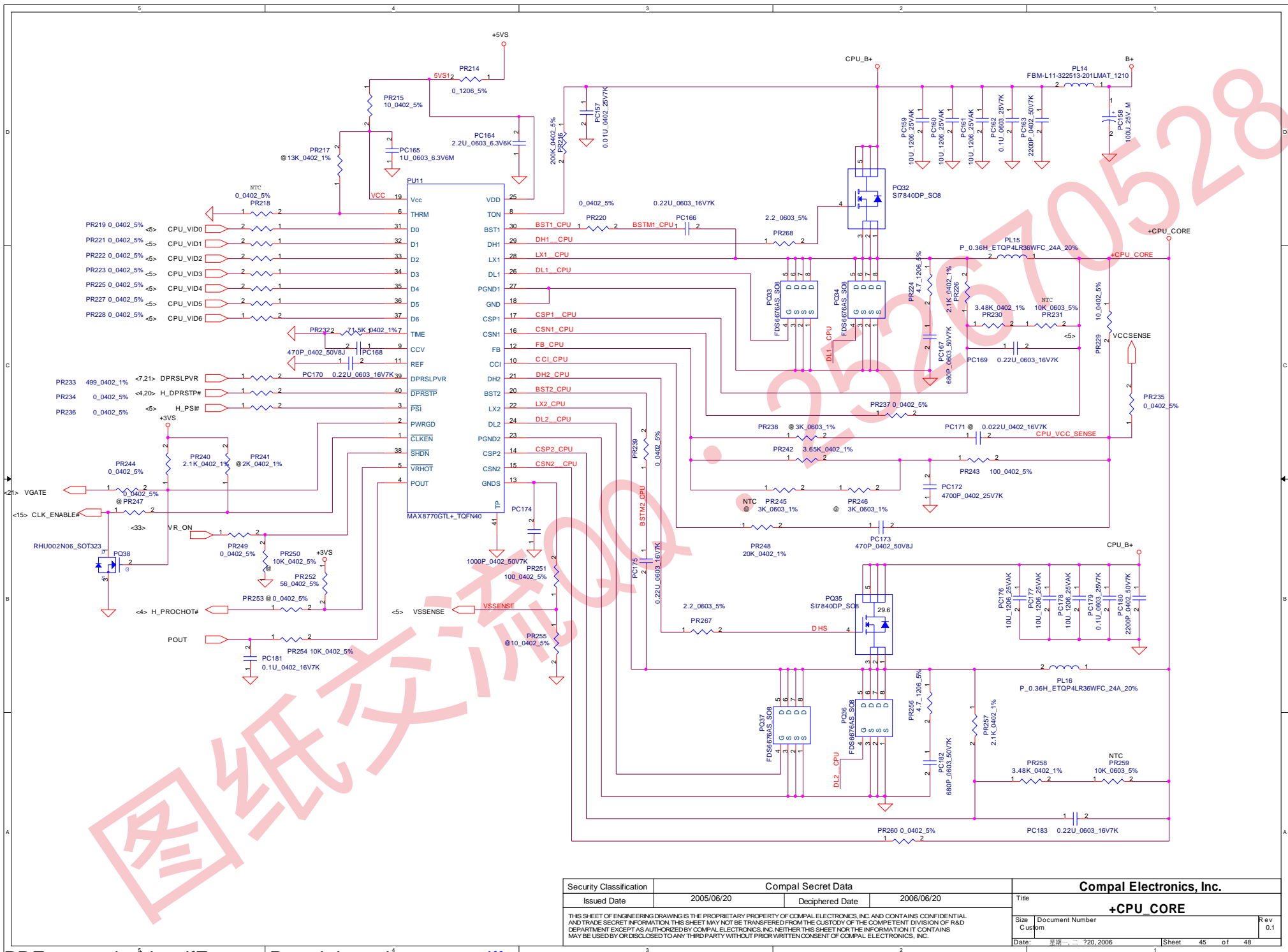


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Issued Date	2005/08/01	Deciphered Date	2006/08/01	Title	
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+1.05VSP Ilimit=6.33A~10.03A







Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		MODIFY 3V/5V current limit to 6.5A~8.1A/6.5A to 10.2A		42	MODIFY PR83/PR84 FROM 499K TO 374K		DVT
2		ADD or decrease CPU CORE ring with EMI solution : snubber		45	Reserve PR224//PR256: 4.7 1206 ,add PC167/PC182:680P		DVT
3		Reserve PR267,PR268 seperate in CPU CORE high side gate for EMI require		45	Reserve PR267,PR268:0 0603		DVT
4		change PJP1 from 5 pin to 4 pin		39	change PJP1 from 5 pin to 4 pin		DVT
5		modify sequecce		43	change PR179 to 100k, PC132 =0.1U		DVT
6		modify Vgate		45	add PQ38:RHU002N06,PR240:2K,delete PR247		
7							
8							
9							
10							
11							
8							
9							

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Version change list (P.I.R. List)

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I tem	Fixed Issue	Rev.	PG#	Modify List	B.Ver#	Phase
1	Add EC_Port80 Signals to DDR2 DIMM1 & DIMM2	0.2	P.13 P.14	1.Connect U6.91 (EC_P80_CLK) through a 0 Ohm R to JP3.83 & JP4.83 2.Connect U6.92 (EC_P80_DATA) through a 0 Ohm R to JP3.69 & JP4.69	0.2	DVT
2	Impedance not match for both CRT & TV Out	0.2	P.17	R3, R4, R5, R6, R7, R8 Change from NC to 150 Ohm	0.2	DVT
3	LCD Panel will flash white frame when power on	0.2	P.16	no stuff D10 (CH751H), stuff R204 (100K)	0.2	DVT
4	ICH7's GPIO configuration modification	0.2	P.21	GPIO10 connect to ACIN GPIO7 connect to G7X_THER_ALERT# GPIO39 connect to KILL_MDCH	0.2	DVT
5	<New Add> MDC supports S4/S5 resuming	0.2	P.28	MDC power connection change to +3VALW from +3VS	0.2	DVT
6	Audio Circuit modification for : 1. Line-Out connection change from Pin.35/Pin.36 to Pin.43/Pin.45 2. Audio-OUT Auto-Switch by HP Plugging In 3. MicPhone Noise Reduction 4. Cleared off BO Sound from both entry of Windows XP & Power Off	0.2	P.29-31	Line-Out connection change from Pin.35/Pin.36 to Pin.43/Pin.45 Connect Pin.32 (LFE_OUT) through 2 uF Cap to Pin.43/Pin.45 +Audio_VREF_LF connection change to 1/2 +AVDD_AC97 Int.MIC connection changes to Pin31/Pin32 through 1uF for each New Add a JACK_PLUG_MIC signal from MIC JACK EAPD signal connect to EC's GPIO4B APA2068's 13PIN(SE/BTL#) connect to GND	0.2	DVT
7	EC GPIO configuration modification	0.2	P.33	New add Port80 information OUT from Pin34(CLK), pin35(DATA) LED4 connection changes from GPIO17(35 PIN) to GPIO4A(91 PIN) New Add DAC's EAPD connect to EC's GPIO4B (92PIN). SKU_ID (GPIO3B) Changes to BRD_ID New Add WL_OFF# (GPIO1F, 46PIN) New Add BT_OFF# (GPIO50, 84PIN) New Add TP_ACT_LED# (GPIO3F, 80PIN) New Add TP_LOCK_LED# (GPIO12, 30PN)	0.2	DVT
8	Lid Switch changes from USB BD to M/B	0.2	P.37	Circuit of Lid SW changes from USB BD to M/B (DEL Lid SW on USB BD)	0.2	DVT
9	Blue LED too dark when active due to VF too High on blue LED	0.2	P.37-38	Changes LED power from +3VS(+3VALW) to +5VS(+5VALWS)	0.2	DVT
10	New Add LED Buffer for LED4, TP_LOCK_LED#, TP_ACT_LED#	0.2	P.37 P.38	TP_ACT_LED# connect to Q802.2, and Q802.1 to GND, then connect to LED804 through a 220 Ohm R TP_LOCK_LED# connect to Q803.2, and Q802.1 to GND, then connect to LED805 through a 220 Ohm R EC_GPIO4A connect to Q804.2, and Q804.1 to GND, then connect to R283 (220 Ohm)	0.2	DVT
11	leakage of electricit when System is running S3 mode	0.2		NC For R458, R402, R411, R128, R831, R829	0.2	DVT

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Version change list (P.I.R. List)

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Item	Fixed Issue	Rev.	PG#	Modify List	B.Ver#	Phase
12	GIGA LAN function failed for both Loopback or PXE on RTL8110SCL solution	0.3	P.27	1. Add a R734 (0 Ohm) resistor between +2.5V_LAN & VTCT for MAC 2. Removed all of the bypass Cap.(C398, C396, C418, C408) for MAC's TCT pins 3. Removed all of pulled down resistors (49.9 Ohm) & Cap.(0.01u)	0.3	PVT
13	Subwoofer still make POP Sound	0.3	P.31	1. Add 0 Ohm resistors, R732 (0 Ohm) connection between AMP_OFF# & U12.2 (SD#) for reserved 2. a 0 Ohm connection between EAPD & U12.2(SD#)	0.3	PVT
14	Mic Switch between Int. & Ext. be Failed	0.3	P.29	1. R717.1 Disconnect from U11.17 2. R717.1 connect to U11.16	0.3	PVT
15	Wrong parts	0.3	P.35	Change package of C434, C224 & C312 from 0402 to 0603	0.3	PVT
16	Add a discharging path of +3.3VS	0.3	P.35	1. Connect +3.3VS to R731.1 2. Connect R731.2 to Q704.1 3. Connect Q704.2 to NET : SUSP signal 4. Connect Q704.3 to GND	0.3	PVT

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