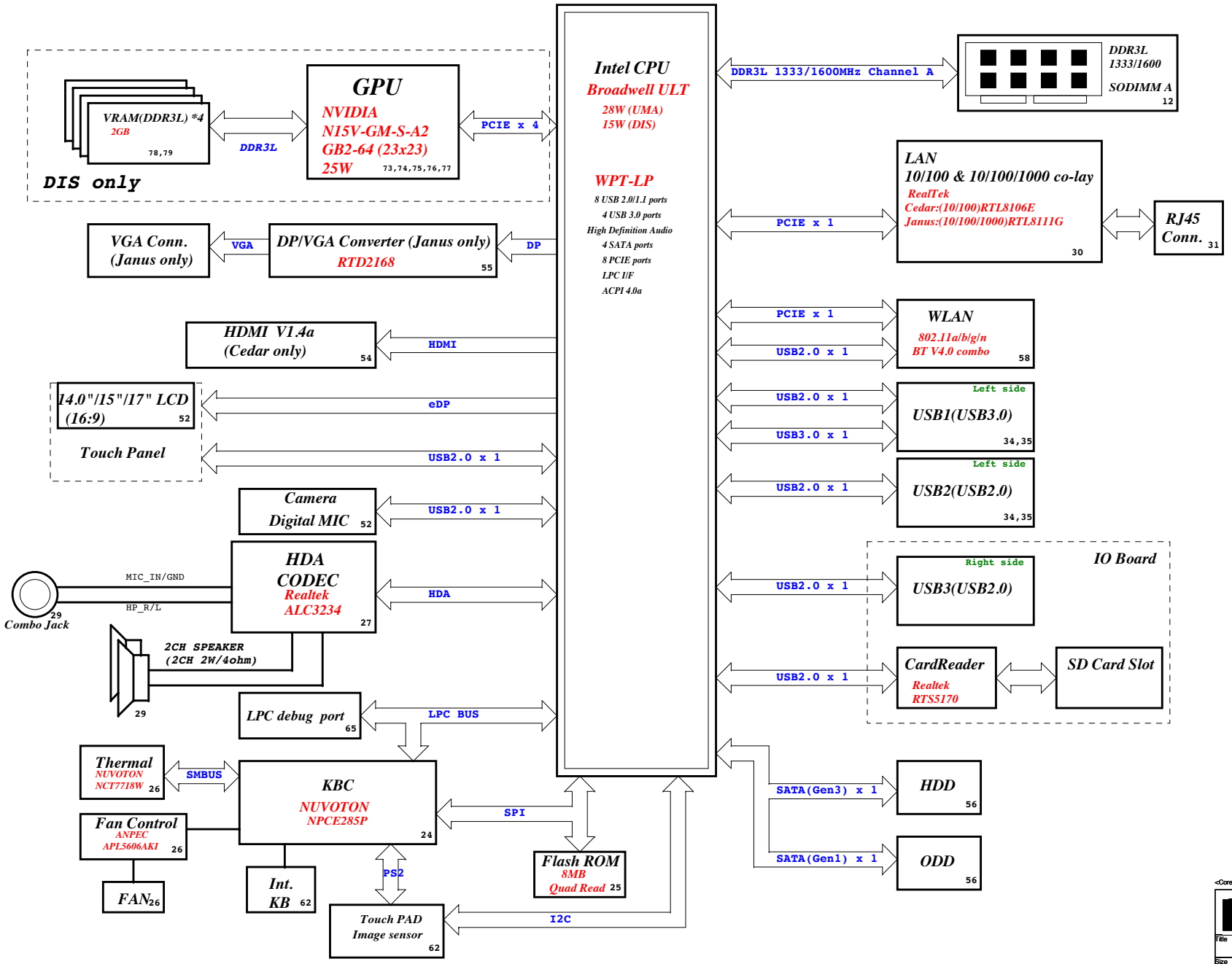
Project code:4PD00I010001
PCB P/N: 13269-1
Revision: X02

Cedar/Janus Block Diagram



CHARGER	
HPA02224RGRR-1-GP 44	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC	
TPS51225RUKR-GP 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5

CPU Core Power	
ISL95813HRZ-GP 46,47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

DDR3L SUS	
TPS51716RUKR-GP 49	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D65V_S0

CPU 1.05V	
RT8237CZQW-2-GP 48	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

CPU 1D5V_S0	
TLV70215DBVR-GP 51	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

Switches 36 83	
INPUTS	OUTPUTS
1D35V_S3	1D35V_S0
5V_S5	5V_S0
3D3V_S5	3D3V_S0
1D05V_S0	1D05V_VGA_S0
3D3V_S0	3D3V_VGA_S0
1D35V_S3	1D35V_VGA_S0

PCB LAYER

L1:Top
L2:VCC
L3:Signal
L4:Signal
L5:GND
L6:Signal

<Core Design>

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Title: Block Diagram

Size	Document Number	Rev
C	Janus HSW 40/50/70	X02

Date: Friday, February 07, 2014 Sheet 2 of 104

(Blanking)

<Core Design>

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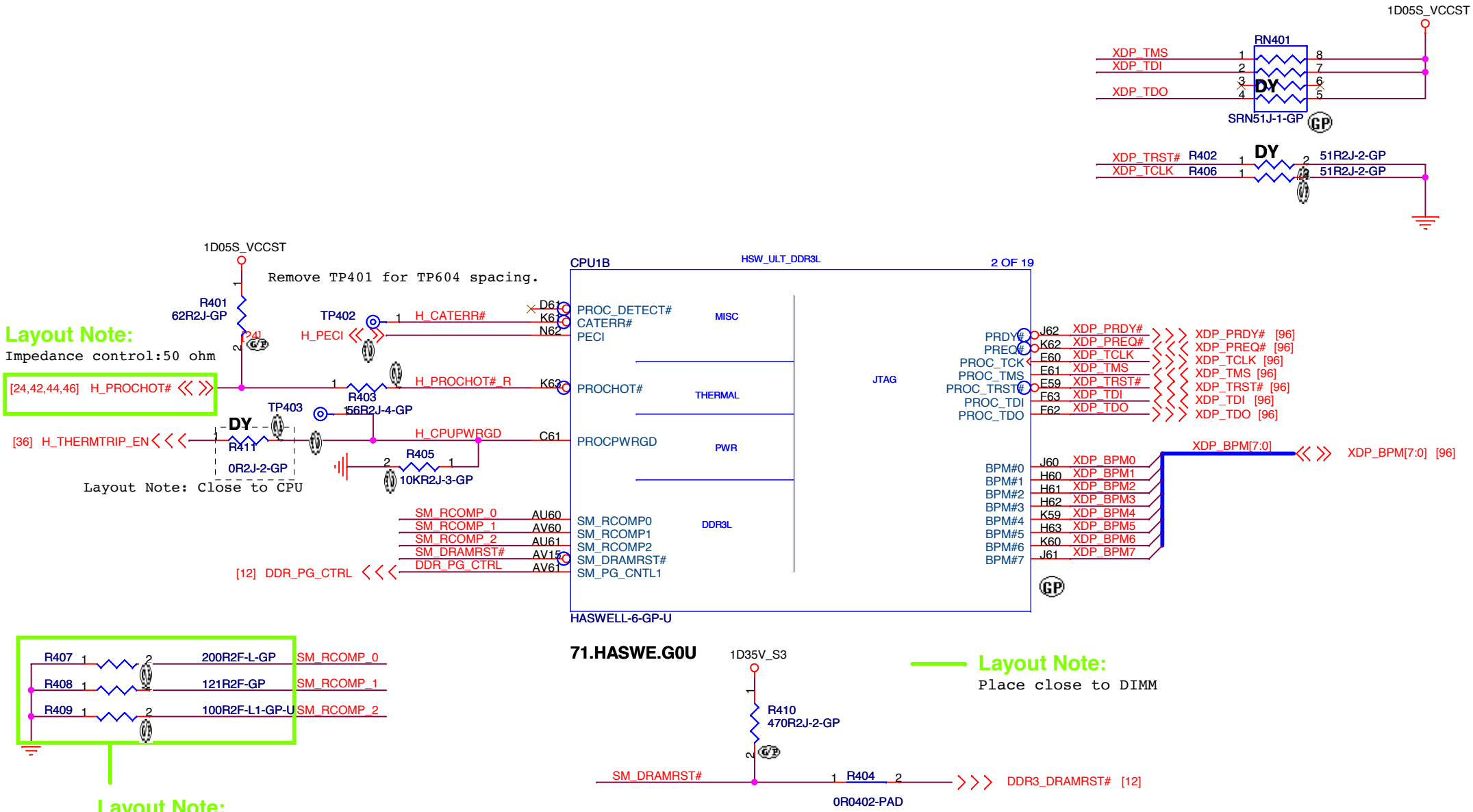
Title

(Reserved)

Size	Document Number	Rev
A4	***Janus HSW 40/50/70***	***A00***

Date: Friday, February 07, 2014 Sheet 3 of 104

SSID = CPU



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

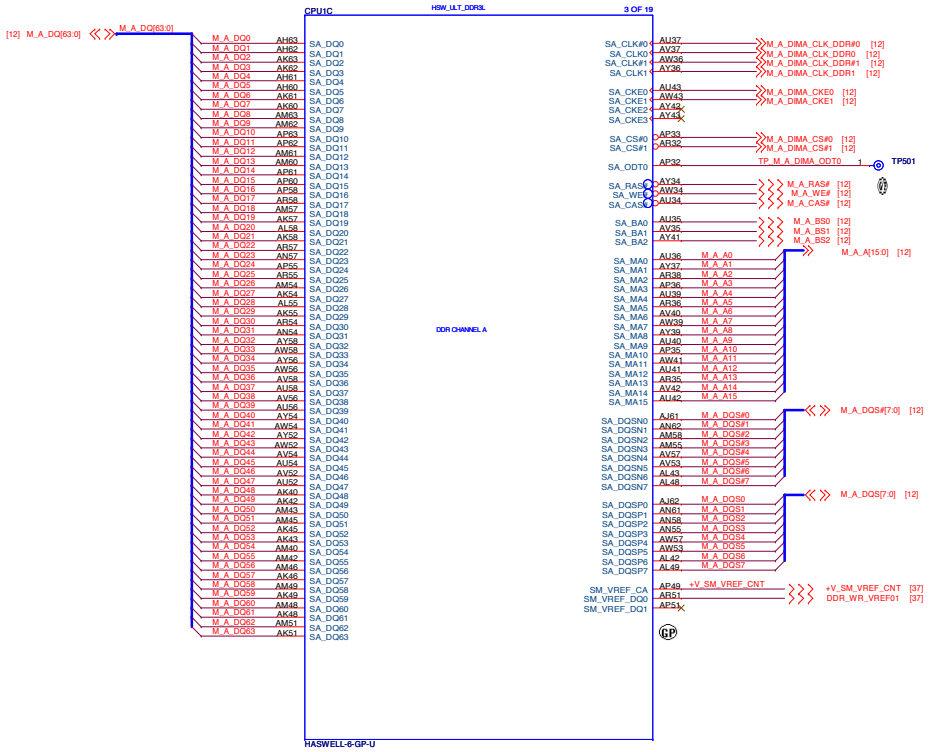
Title: ***CPU (THERMAL/MISC/PM)***

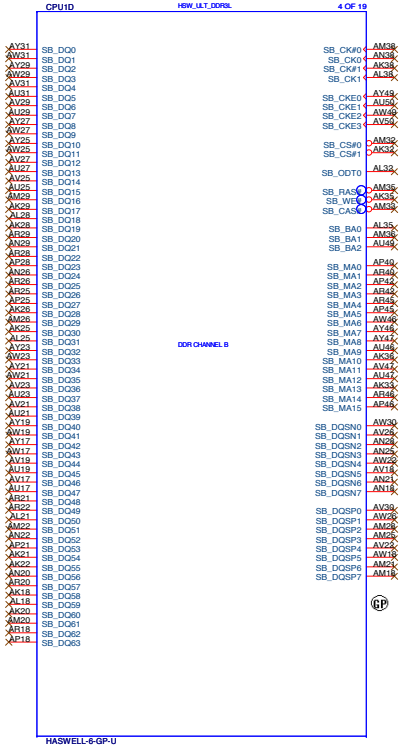
Size	Document Number	Rev
A4	***Janus HSW 40/50/70***	***A00***

Date: Friday, February 07, 2014 Sheet 4 of 104

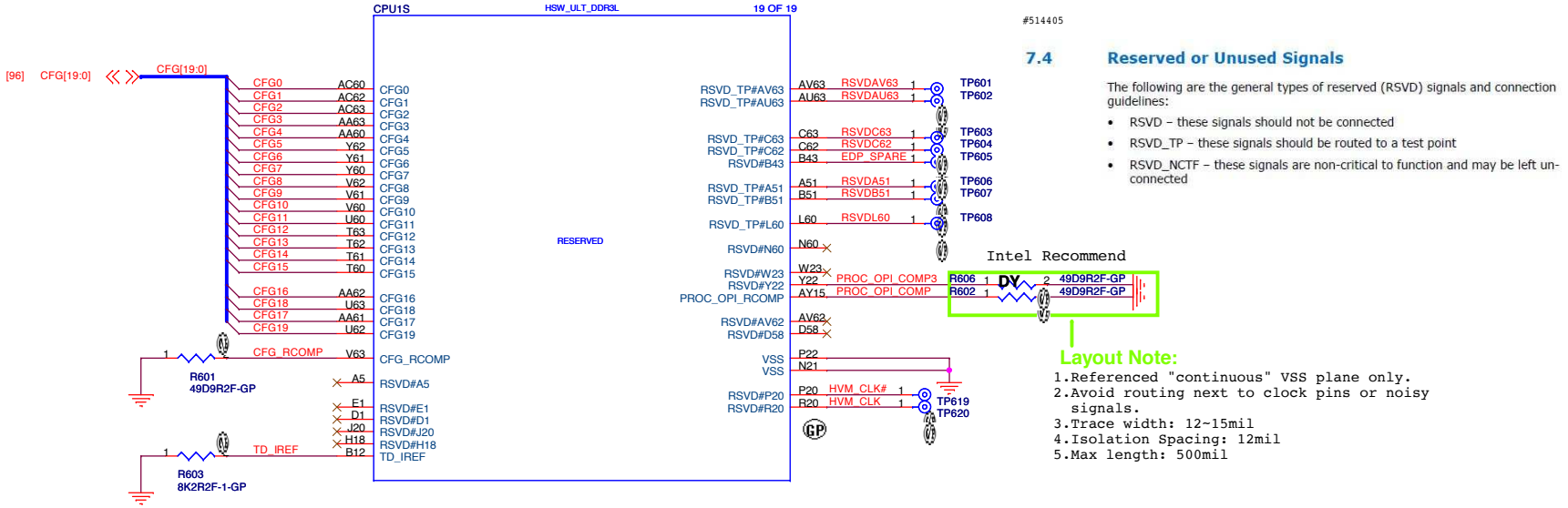
SSID = CPU

DDR3L ball type: Non-Interleaved Type





SSID = CPU



#514405

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected

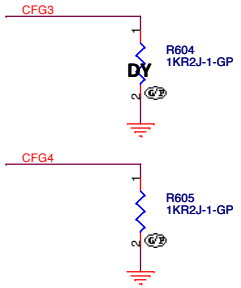
Intel Recommend

Layout Note:

1.Referenced "continuous" VSS plane only.
2.Avoid routing next to clock pins or noisy signals.
3.Trace width: 12~15mil
4.Isolation Spacing: 12mil
5.Max length: 500mil

#514405 **PCH strap pin:**

Signal Name	Description	Direction / Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate Platform Design Guide for pull-down recommendations when a logic low is desired. • **CFG[2:0]:** Reserved configuration lane. A test point may be placed on the board for these lanes. • **CFG[3]: MSR Privacy Bit Feature** – 1 = Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting – 0 = IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden • **CFG[4]: eDP enable** – 1 = Disabled – 0 = Enabled • **CFG[19:5]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
	1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

<Core Design>

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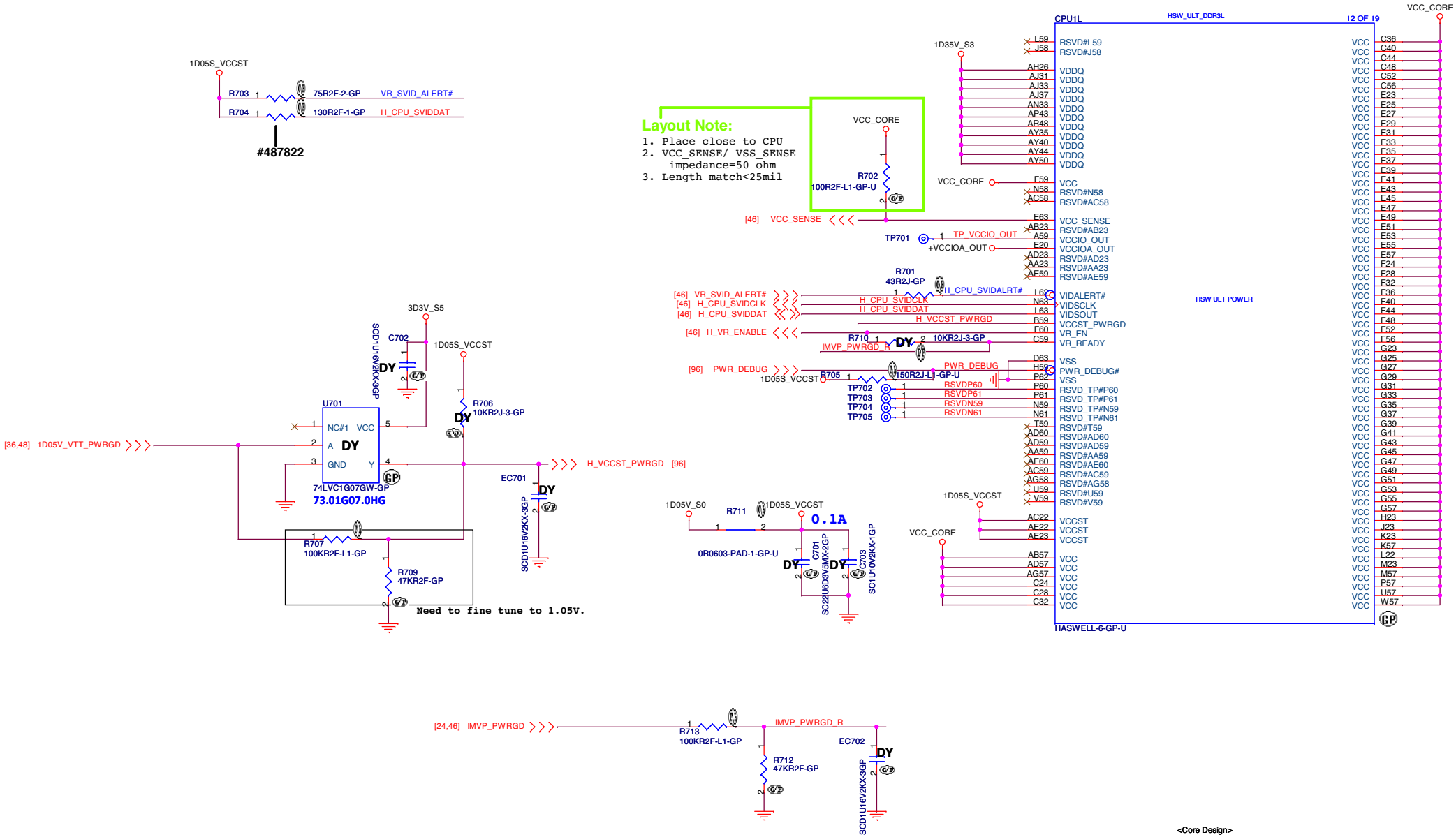
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CFG)

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 6 of 104

SSID = CPU



<Core Design>

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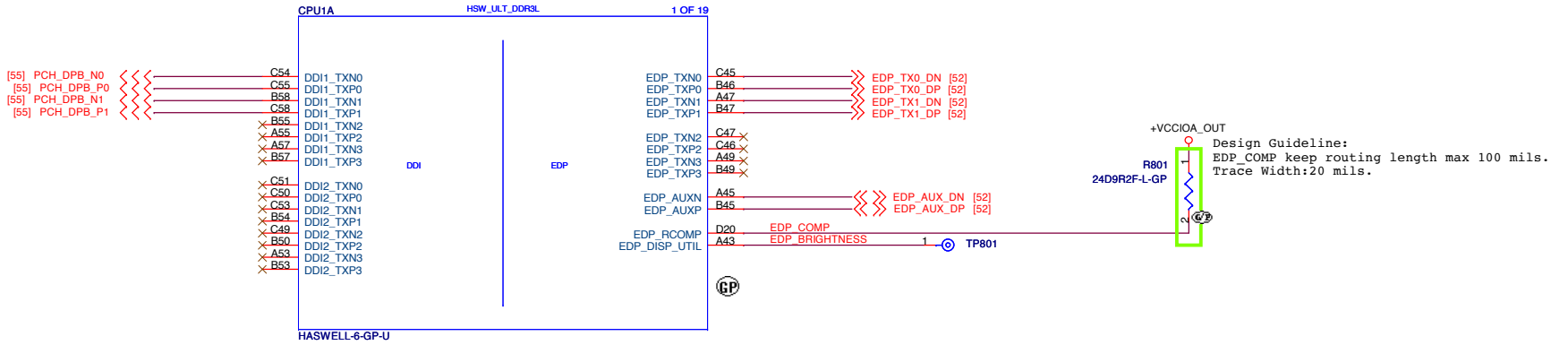
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (VCC CORE)	
Size A3	Document Number: Janus HSW 40/50/70	Rev A00
Date: Friday, February 07, 2014	Sheet 7 of 104	

SSID = CPU

DP to VGA Converter



<Core Design>

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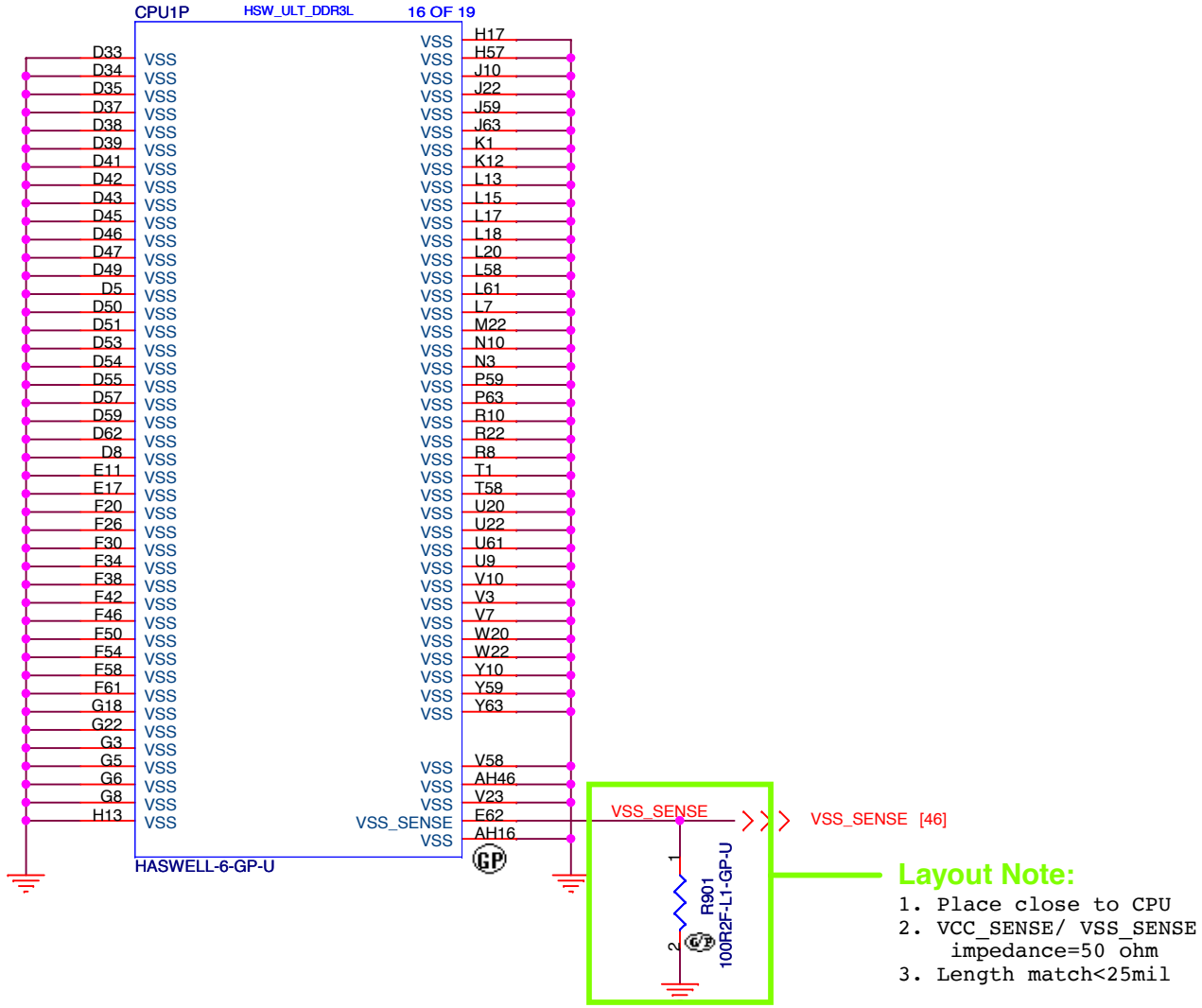
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDI/EDP)		
Size: A3	Document Number: Janus HSW 40/50/70	Rev: X02
Date: Friday, February 07, 2014	Sheet 8 of 104	

SSID = CPU



Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

<Core Design>

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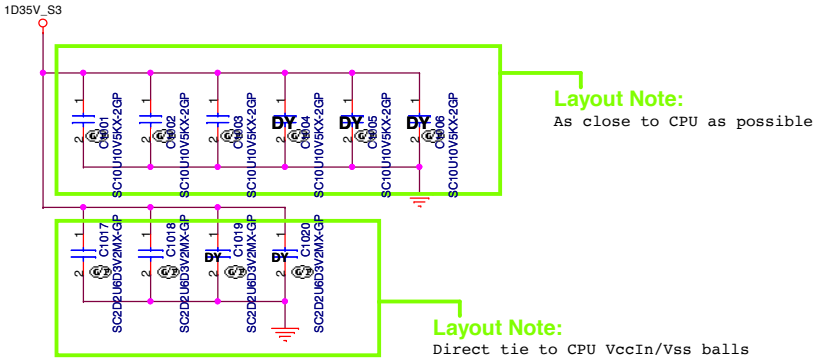
Taipei Hsien 221, Taiwan, R.O.C.

Title	***CPU (VSS)***	
Size: A4	Document Number: ***Janus HSW 40/50/70***	Rev: ***A00***
Date: Friday, February 07, 2014	Sheet 9 of 104	

SSID = CPU



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

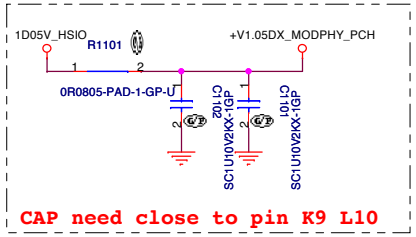
Title: CPU (Power CAP1)

Size	Document Number	Rev
A3	Janus HSW 40/50/70	A00

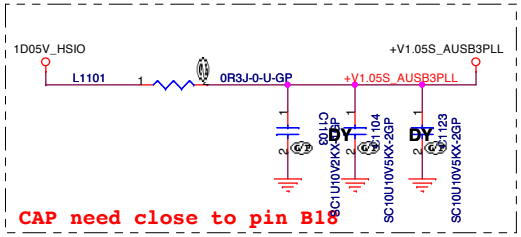
Date: Friday, February 07, 2014 Sheet 10 of 104

MAX: 1.92A

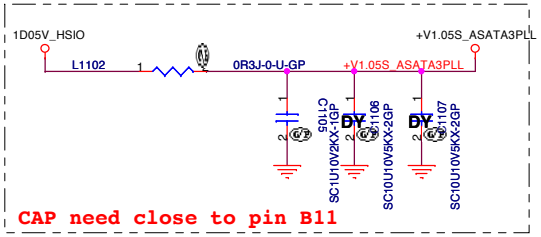
1.838A



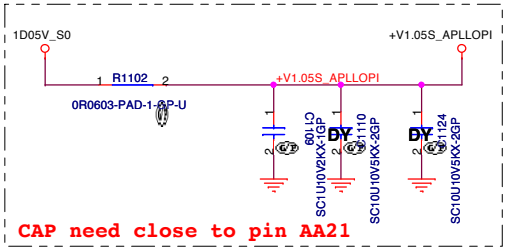
41mA



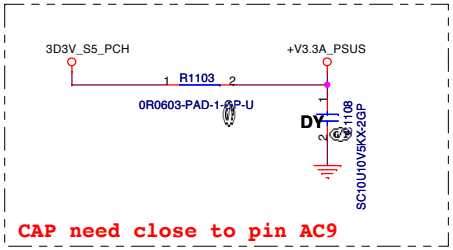
42mA



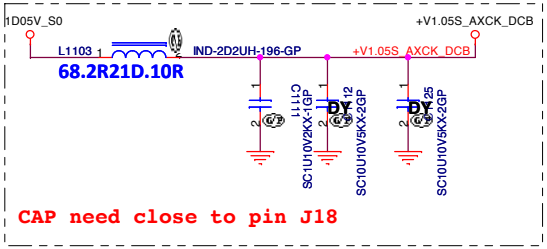
57mA



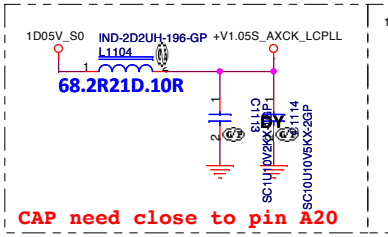
62mA



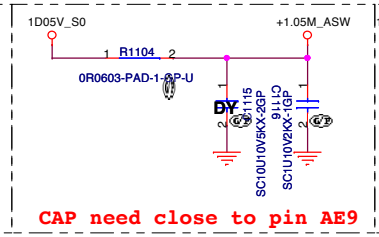
185mA



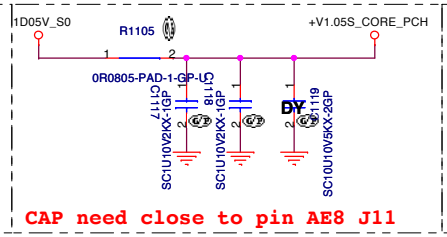
31mA



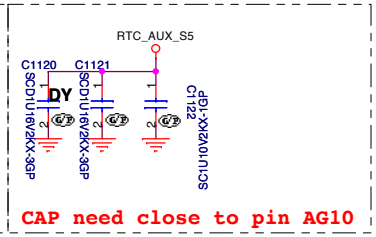
658mA



1.632A



1mA



<Core Design>

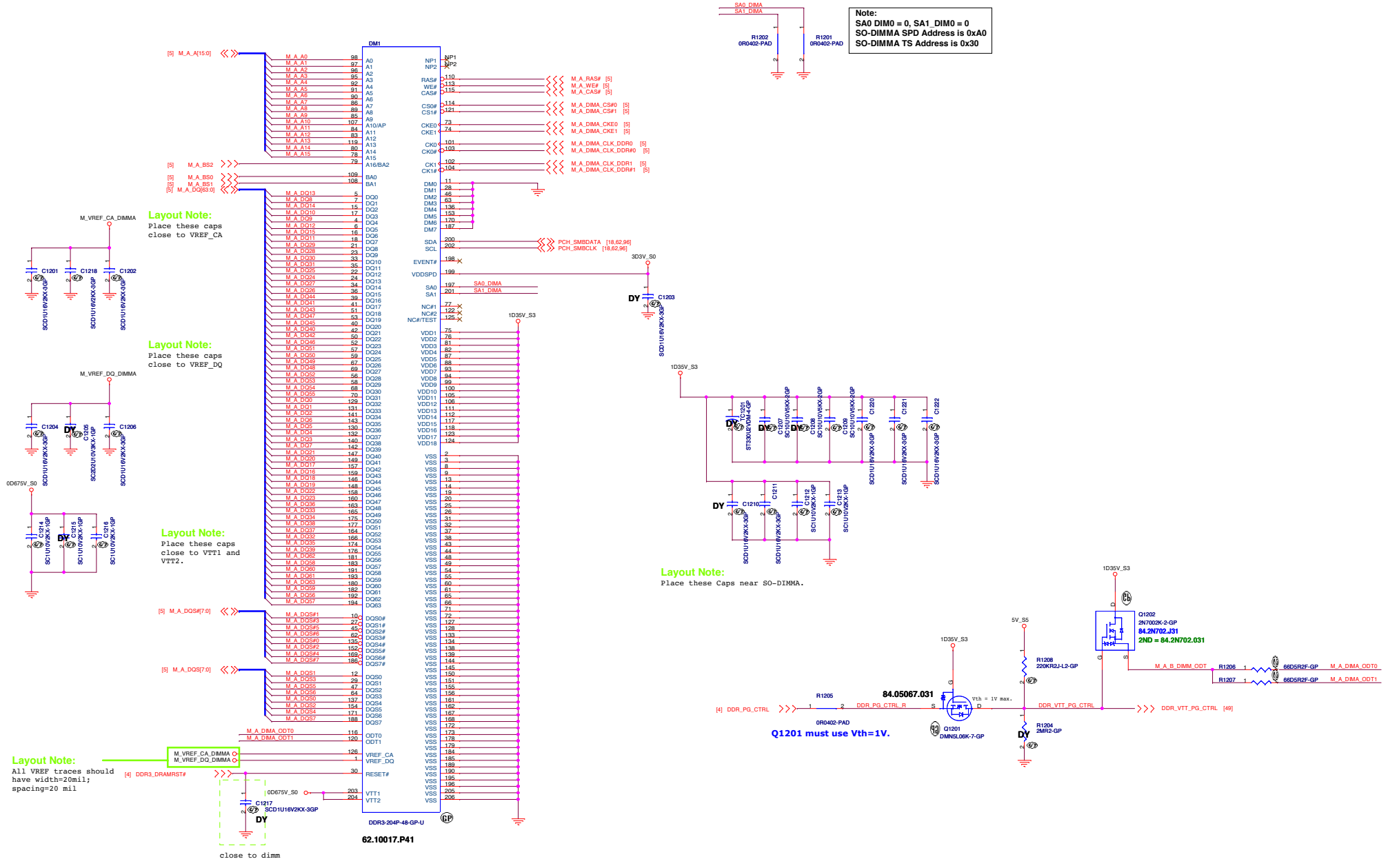
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Power CAP2)

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 11 of 104

SSID = MEMORY



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR3-SODIMM1**

Size: A2 | Document Number: **Janus HSW 40/50/70** | Rev: **A00**

Date: Friday, February 07, 2014 | Sheet 12 of 104

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)DDR3-SODIMM2*

Size: A3 | Document Number: *Janus HSW 40/50/70* | Rev: *A00*

Date: Friday, February 07, 2014 | Sheet 13 of 104

(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)_SODIMM _SODIMM4*

Size	Document Number	Rev
A4	*Janus HSW 40/50/70*	*A00*

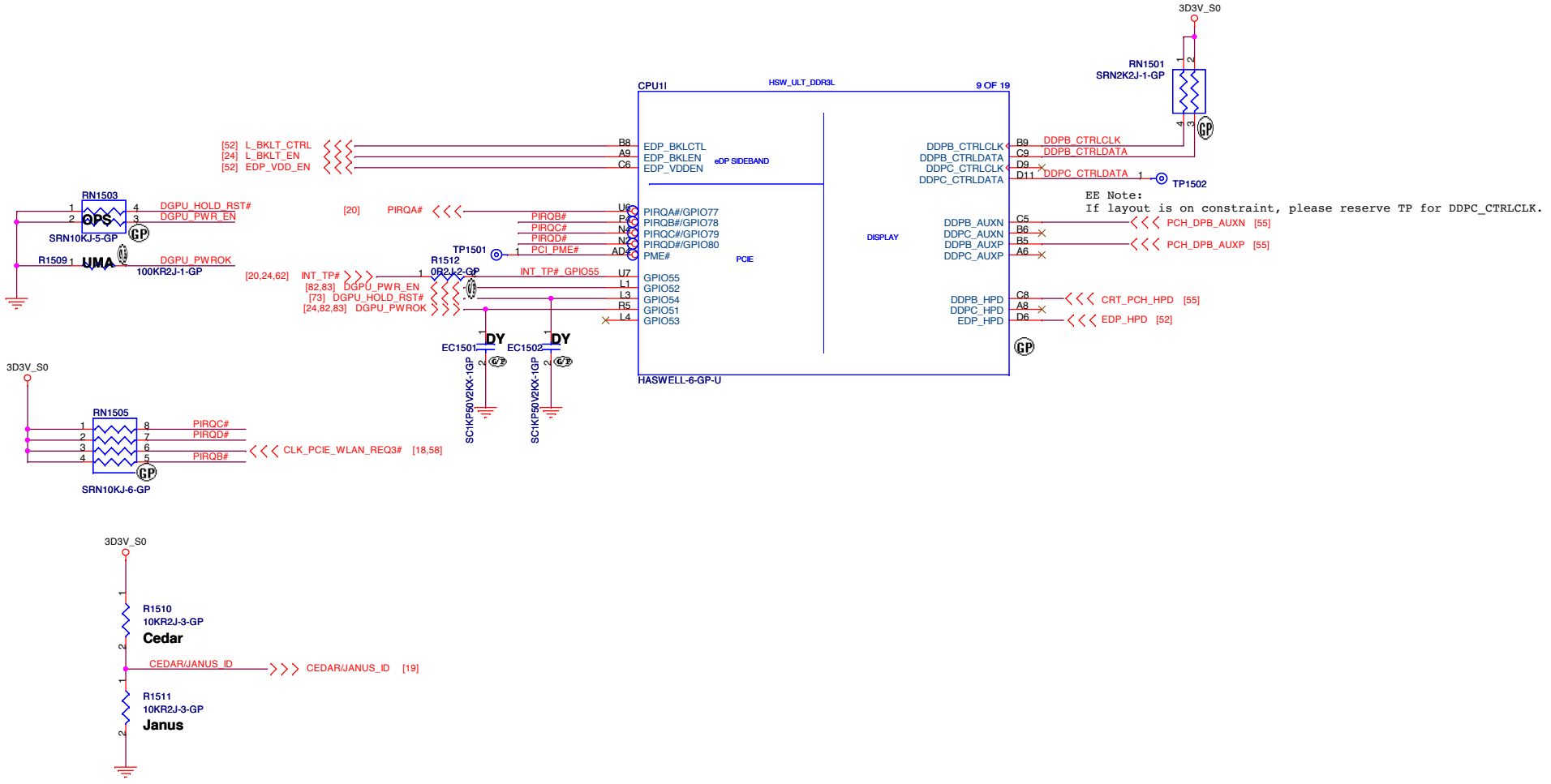
Date: Friday, February 07, 2014 Sheet 14 of 104

SSID = CPU

PCH strap pin:

Port B Detected	
DDPB_CTRLDATA	* Low = Disable Port B (default) High = Enable Port B
DDPC_CTRLDATA	* Low = Disable Port C (default) High = Enable Port C

The internal pull-down is disabled after PLTRST# deasserts



<Core Design>

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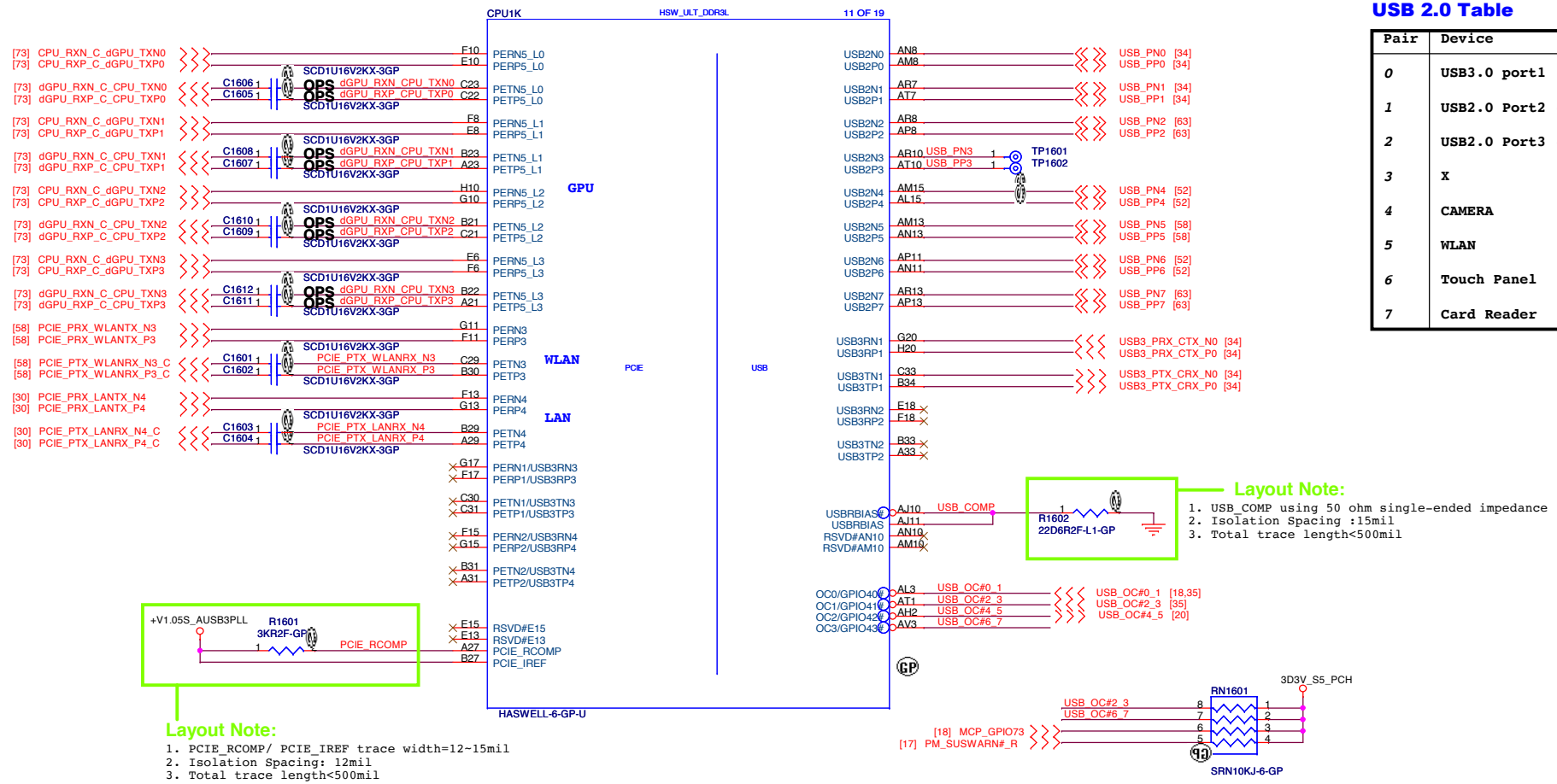
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (EDP/GPIO/DDI)	
Size A3	Document Number Janus HSW 40/50/70	Rev X02
Date: Friday, February 07, 2014	Sheet 15 of 104	

SSID = PCH



USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB2.0 Port2 (Debug Port)
2	USB2.0 Port3 (IOBD)
3	X
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader

Layout Note:

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

Layout Note:

1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN	
5(L0~L3)	GPU	
6(L3)	HDD	SATA0
6(L2)	ODD	SATA1
6(L0~L1)	N/A	

#515621

Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port3	USB 3.0 Port4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD GPU	PCIe* Port 5 Lane 1 SSD GPU	PCIe* Port 5 Lane 2 GPU	PCIe* Port 5 Lane 3 GPU	SATA 6Gb/s Port 3	SATA 6Gb/s Port 2	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD							PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	PCIe* Port 6 Lane 2	PCIe* Port 6 Lane 3
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port3	USB 3.0 Port4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD GPU	PCIe* Port 5 Lane 1 SSD GPU	PCIe* Port 5 Lane 2 GPU	PCIe* Port 5 Lane 3 GPU	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD										

<Core Design>

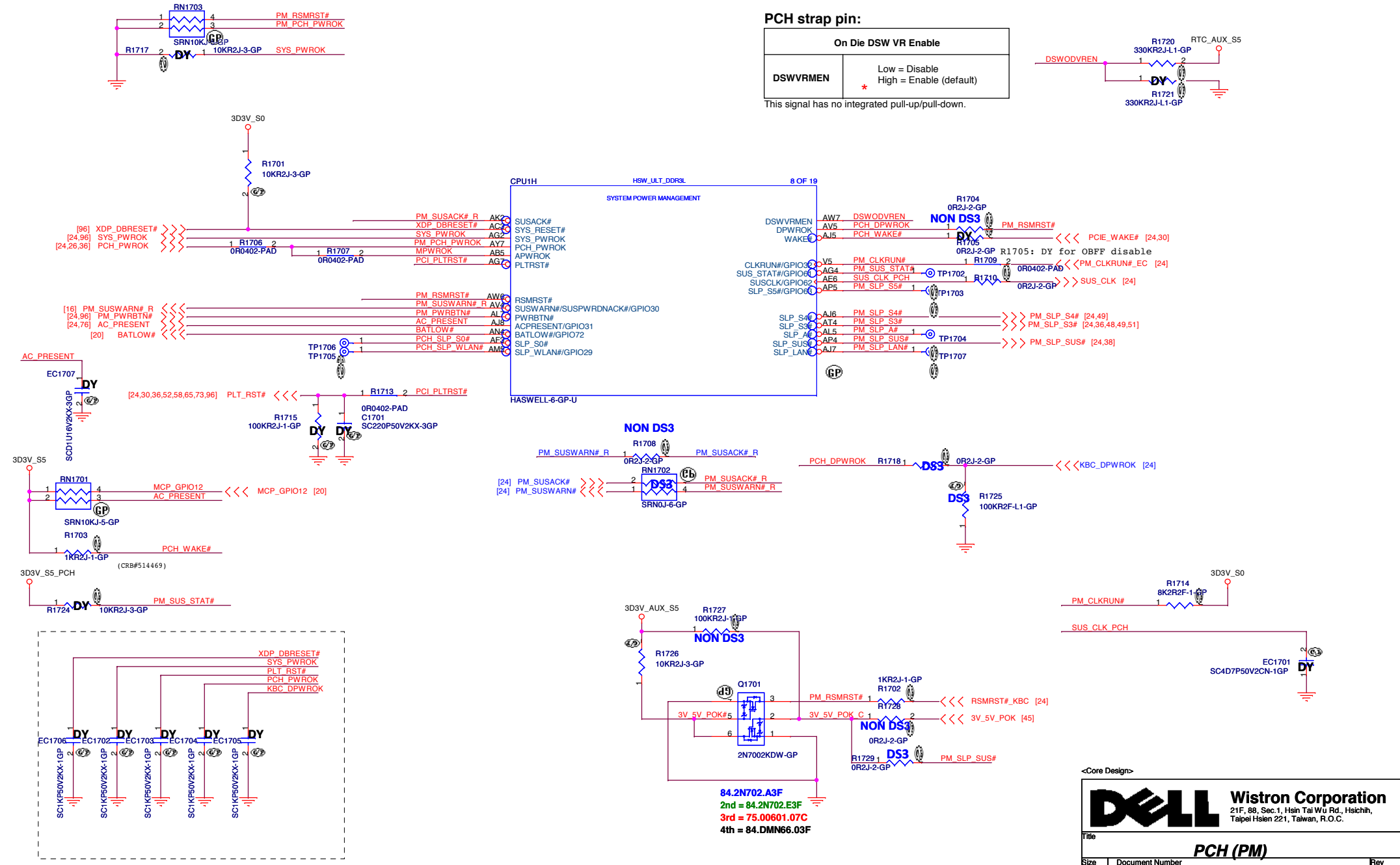
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCIE/USB)

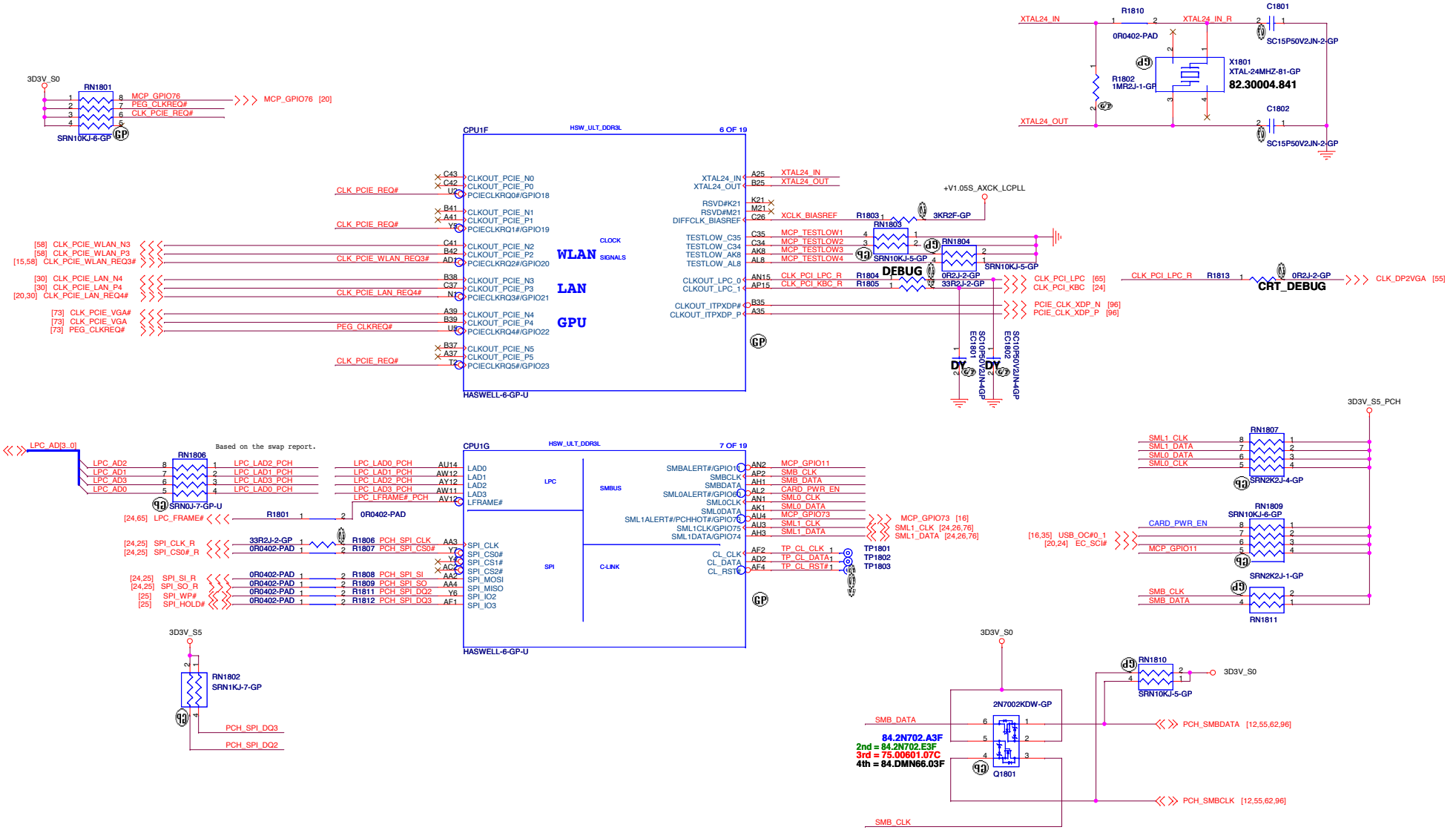
Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 16 of 104

SSID = PCH


PCH strap pin:
On Die DSW VR Enable
DSWVRMEN
Low = Disable
High = Enable (default)
*
This signal has no integrated pull-up/pull-down.
CPU1H
HSW_ULT_DDR3L
8 OF 19
SYSTEM POWER MANAGEMENT
HASWELL-6-GP-U
NON DS3
DS3
DY
3D3V_S0
3D3V_S5
3D3V_S5_PCH
3D3V_AUX_S5
RTC_AUX_S5
Q1701
2N7002KDW-GP
84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C
4th = 84.DMN66.03F
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (PM)
Size A3
Document Number
Janus HSW 40/50/70
Rev A00
Date: Friday, February 07, 2014
Sheet 17 of 104

SSID = PCH



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (CLOCK/SMBUS/CL/LPC/SPI)

Size	Document Number	Rev
Custom	Janus HSW 40/50/70	X02

Date: Friday, February 07, 2014 Sheet 18 of 104

SSID = CPU

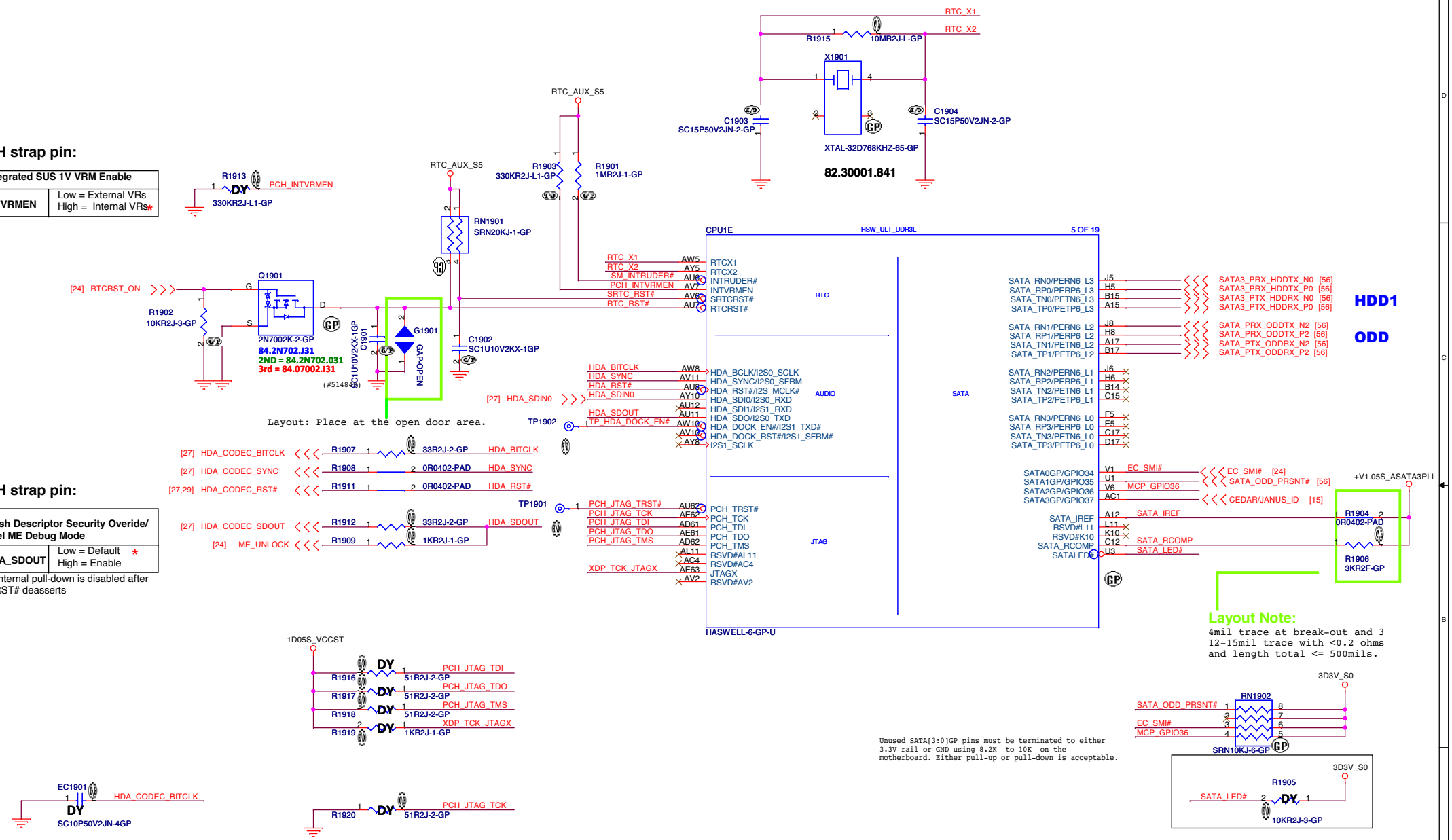
PCH strap pin:

Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs*

PCH strap pin:

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts



<Core Design>

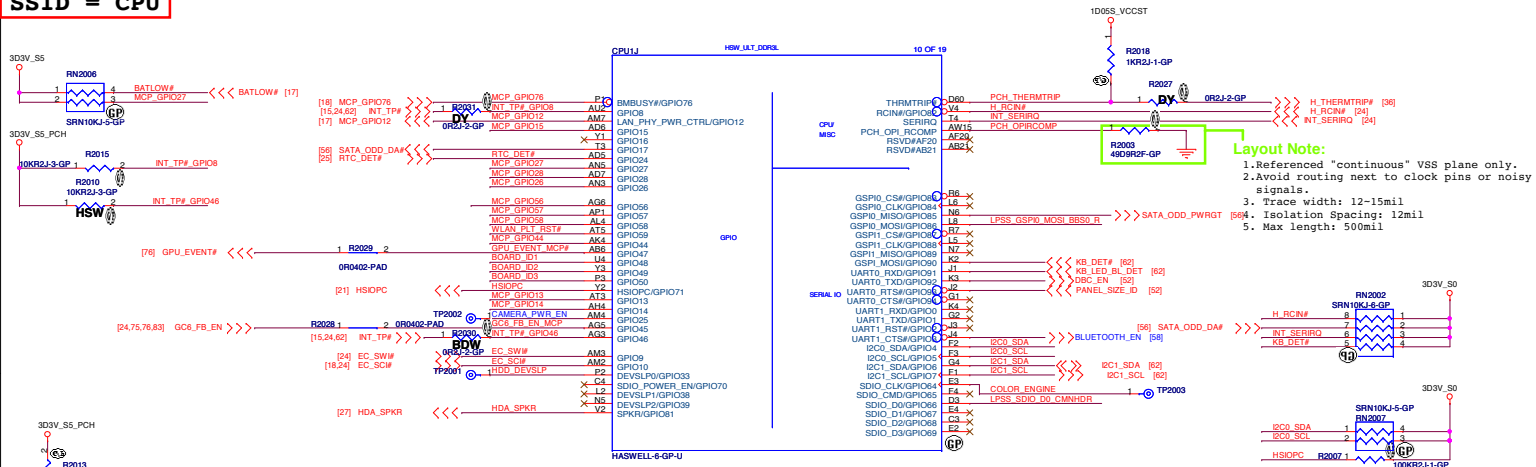
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

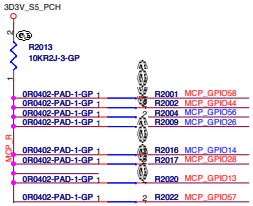
Title: PCH (RTC/SATA/HDA/JTAG)

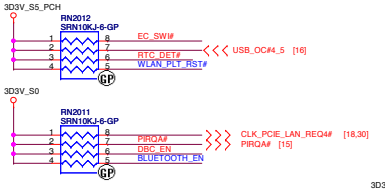
Size	Document Number	Rev
A3	Janus HSW 40/50/70	A00

Date: Friday, February 07, 2014 Sheet 19 of 104

SSID = CPU

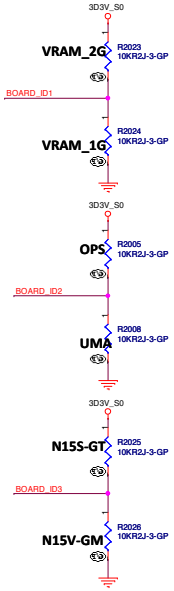






BIOS strap pin:

BIOS VRAM Size Strap pin	BOARD_ID1
1G	0
2G	1



BIOS strap pin:

BIOS UMA/DIS Strap pin	BOARD_ID2
UMA	0
DIS	1

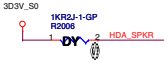
BIOS strap pin:

BIOS UMA/DIS Strap pin	BOARD_ID3
N15V-GM-S(DVC40/50)	0
N15S-GT (DVC70)	1

PCH strap pin:

NO REBOOT	
HDA_SPKR	* Low = Enable (Default) High = Disable

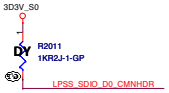
The internal pull-down is disabled after PLTRST# deasserts



PCH strap pin:

Top-Block Swap Override mode	
SDIO_D0 / GPIO66	High = Enable "Top-Block swap" mode * Low = Disable "Top-Block swap" mode (Default)

The internal pull-down is disabled after PLTRST# deasserts

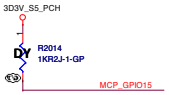


Need SW double confirm if that's needed Top-Block swap

PCH strap pin:

TLS Confidentiality	
GPIO15	*Low = Disable Intel ME Crypto TLS (Default) High = Enable Intel ME Crypto TLS

The internal pull-down is disabled after RSMRST# deasserts.



PCH strap pin:

Boot BIOS Strap Bit BBS	
Boot BIOS Destination	* Low = SPI (Default) High = LPC

The internal pull-down is disabled after PLTRST# deasserts

Need double confirm, GPIO table set to GPI if that's needed PH or PL

<Core Design>

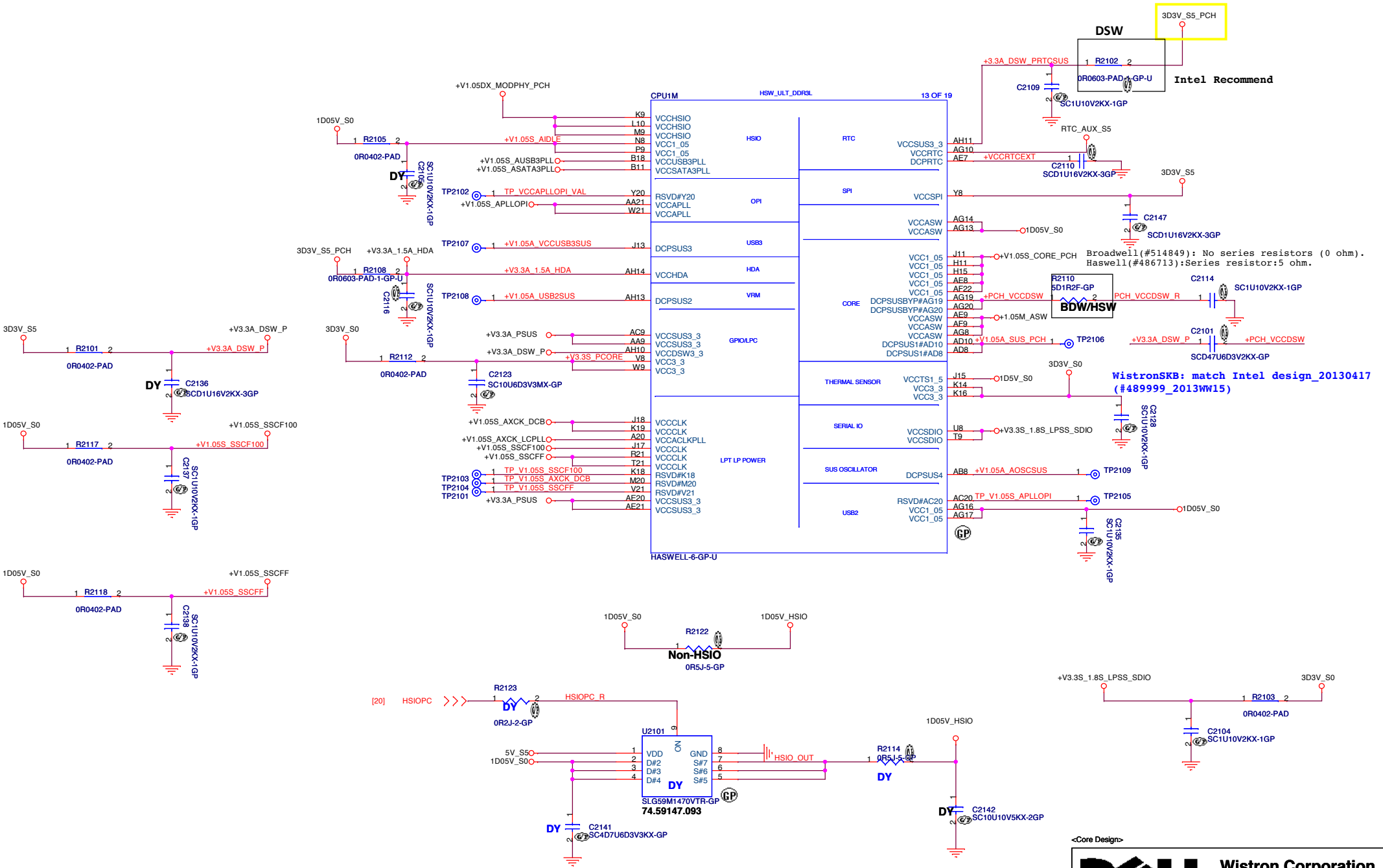
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (GPIO/MISC)

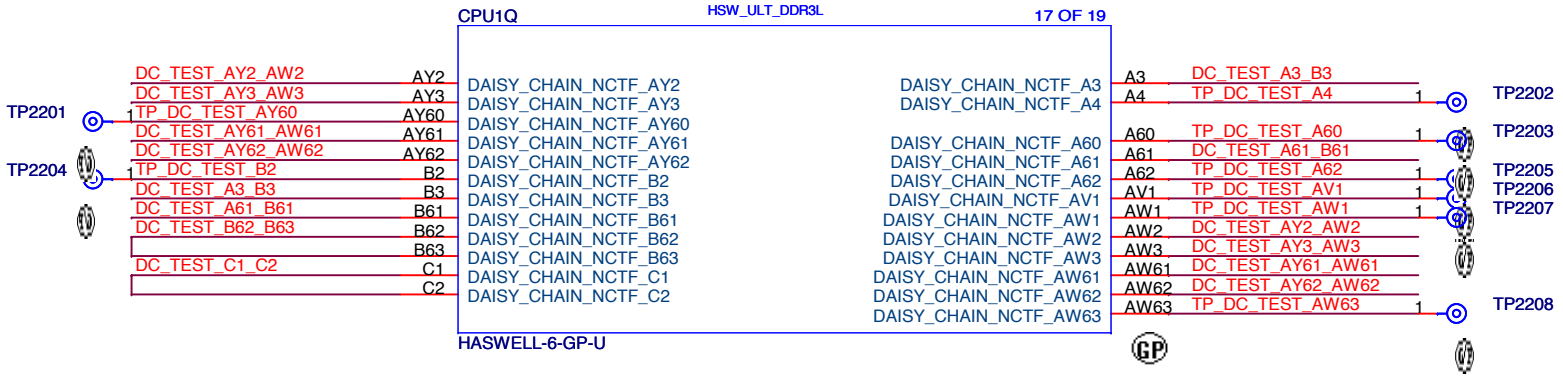
Size: A2 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 20 of 104

SSID = CPU


CPU1M
HSW_ULT_DDR3L
13 OF 19
HASWELL-6-GP-U
DSW
3D3V_S5_PCH
Intel Recommend
Broadwell(#514849): No series resistors (0 ohm).
Haswell(#486713):Series resistor:5 ohm.
BDW/HSW
WistronSKB: match Intel design_20130417 (#489999_2013WW15)
Non-HSIO
SLG59M1470VTR-GP
74.59147.093
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
CPU (POWER2)
Janus HSW 40/50/70
A00
Friday, February 07, 2014
21
104

SSID = PCH



<Core Design>

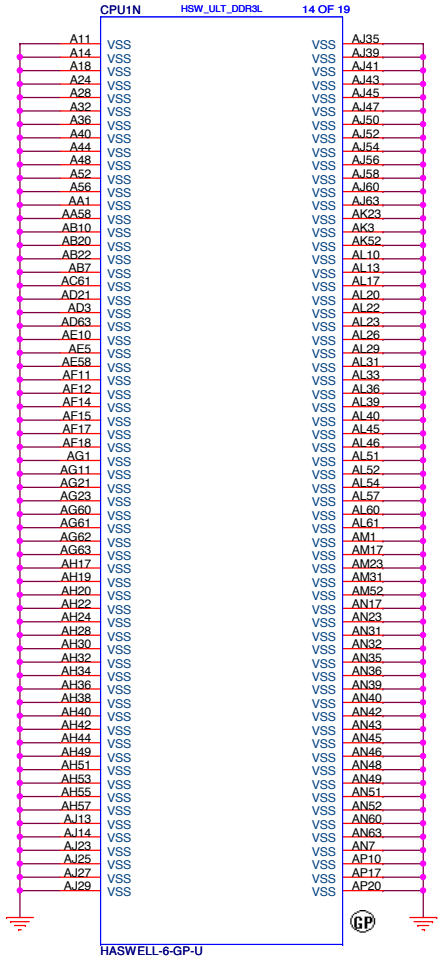
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

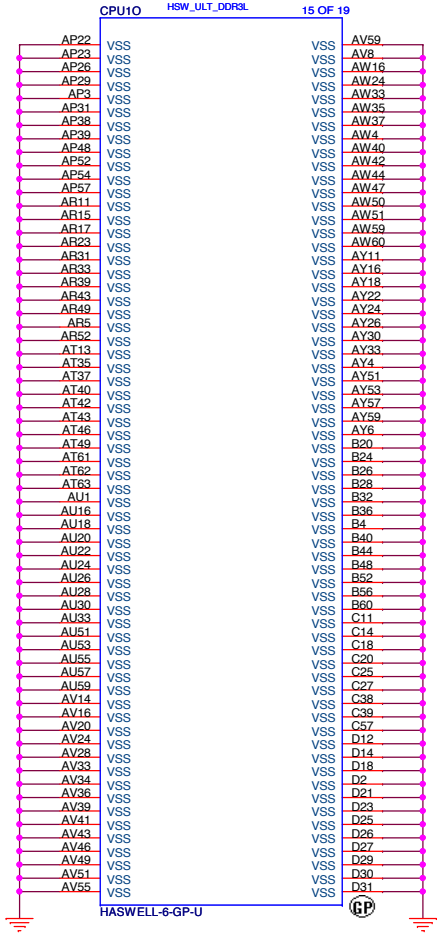
Title: ***CPU (RSVD)***

Size	Document Number	Rev
A4	***Janus HSW 40/50/70***	***A00***

Date: Friday, February 07, 2014 Sheet 22 of 104

SSID = PCH





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(VSS)

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 23 of 104

SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
X03	100.0K	47.0K	2.24V
A00	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO67)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
Janus-OPS	100.0K	10.0K/64.10035.4DU	3.0V
Janus-UMA	100.0K	13.7K/64.13725.4DU	2.902V
TBD	100.0K	17.8K/64.17825.4DU	2.801V
TBD	100.0K	22.1K/64.22125.4DU	2.702V
TBD	100.0K	27.4K/64.27525.4DU	2.598V
TBD	100.0K	32.4K/64.32525.4DU	2.492V
TBD	100.0K	37.4K/64.37425.4DU	2.402V
TBD	100.0K	43.2K/64.43225.4DU	2.304V
TBD	100.0K	49.9K/64.49925.4DU	2.201V
Cedar-OPS	100.0K	57.6K/64.57625.4DU	2.093V
Cedar-UMA	100.0K	64.9K/64.64925.4DU	2.001V
TBD	100.0K	73.3K/64.73225.4DU	1.903V
TBD	100.0K	82.5K/64.82525.4DU	1.808V
TBD	100.0K	93.1K/64.93125.4DU	1.709V
TBD	100.0K	107K/64.10735.4DU	1.594V
TBD	100.0K	120K/64.13035.4DU	1.499V
TBD	100.0K	137K/64.13735.4DU	1.392V
TBD	100.0K	154K/64.15435.4DU	1.299V
TBD	100.0K	200K/64.20035.4DU	1.099V
TBD	100.0K	332K/64.33235.4DU	0.894V

Layout Note:
Need very close to EC

ALL_SYS_PWRGD assert, delay 10ms; PCH_PWROK assert.

ALL_SYS_PWRGD de-assert, delay 100ms; SYS_PWROK assert.
LVDS backlight Control from PS8625

eDP backlight Control from PCH

071.00285.000G

Layout Note:
Connect GND and AGND planes via either 0R resistor or connect directly.

EC_GPIO47 High Active

Power Switch Logic(PSL)

Layout Note:
Need very close to EC

Layout Note:
Need very close to EC

Layout Note:
Need very close to EC

83.R2004.H8F

83.R2004.H8F

84.2N702.031
2ND = 84.2N702.031
3rd = 84.07002.151
4th = 84.2N702.W31

84.02130.051
2ND = 84.03413.A31

84.2N702.151
2ND = 84.2N702.031
3rd = 84.07002.151
4th = 84.2N702.W31

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

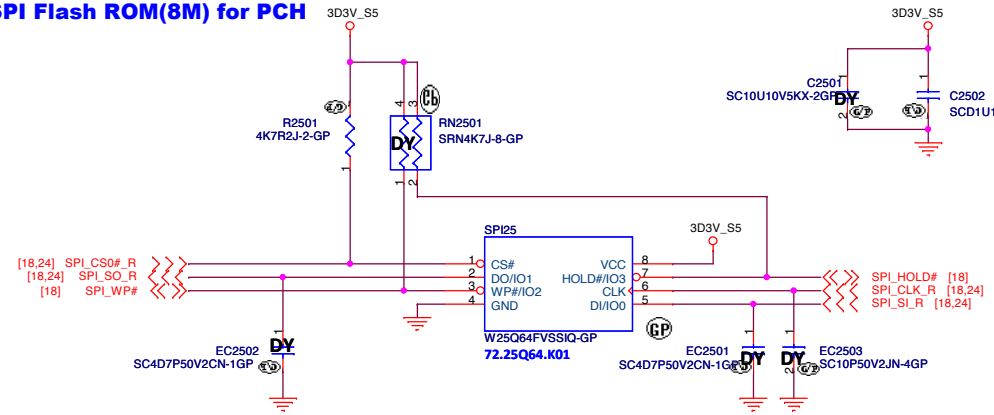
Title: KBC Nuvoton NPCE885

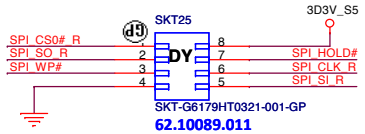
Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 24 of 104

SSID = Flash.ROM

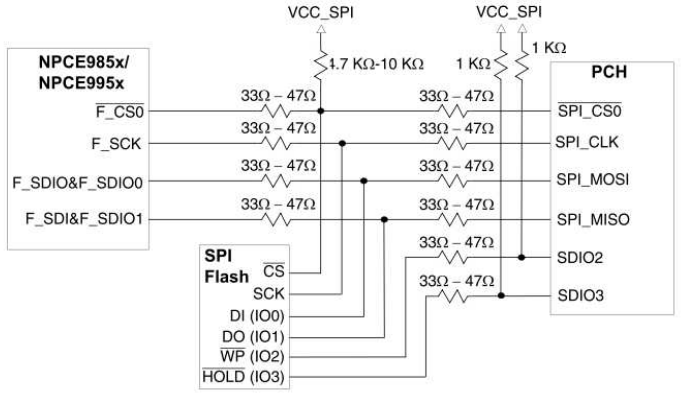
SPI Flash ROM(8M) for PCH





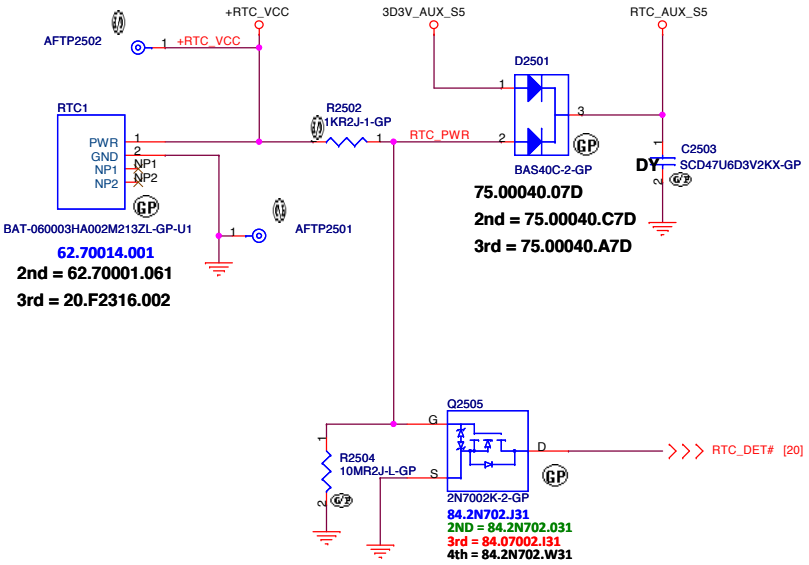
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	O	O
72.25647.00A	O	O
072.25B64.0001	O	O

Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

SSID = RBATT



<Core Design>

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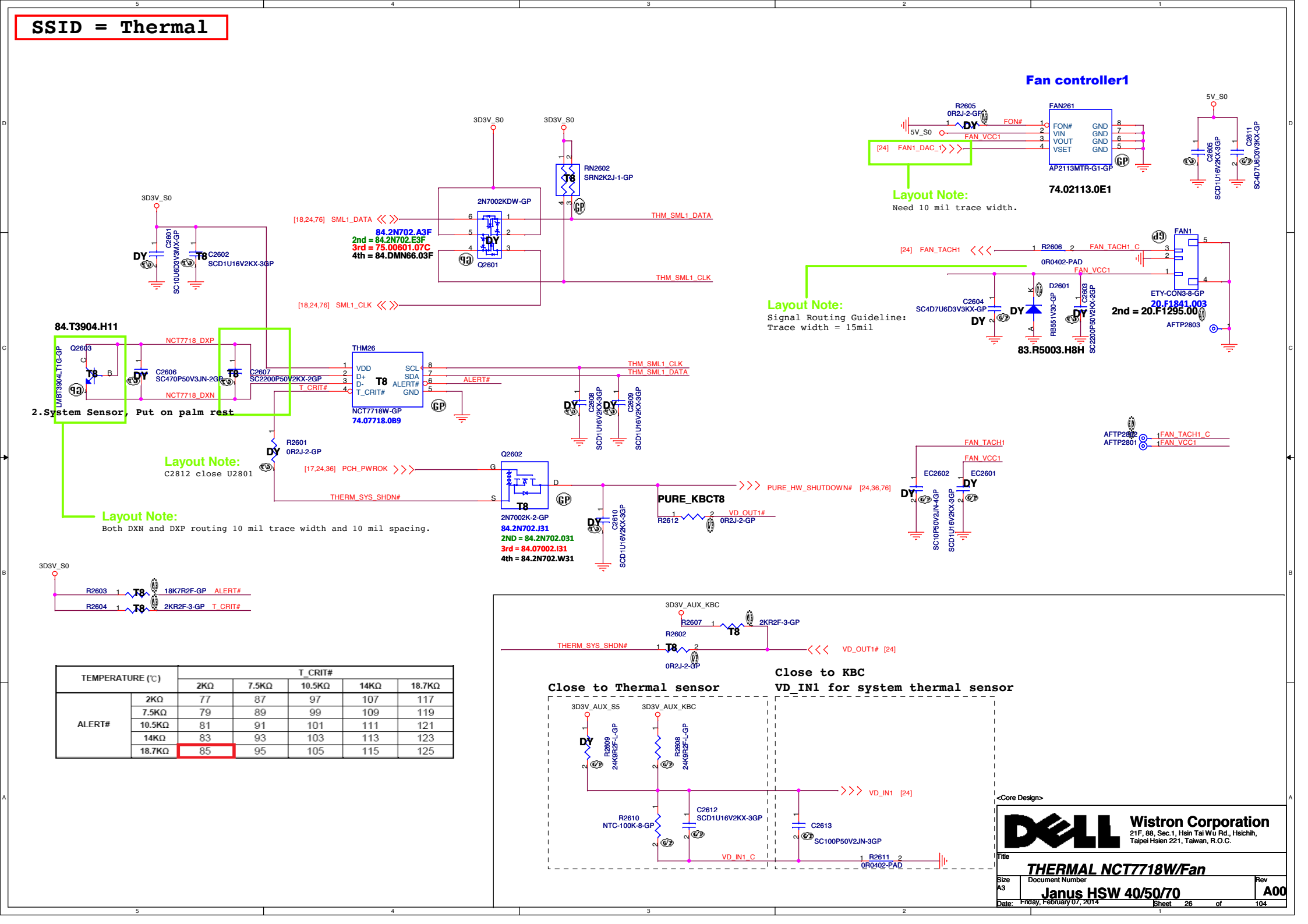
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC		
Size: A3	Document Number: Janus HSW 40/50/70	Rev: A00
Date: Friday, February 07, 2014	Sheet 25 of 104	

SSID = Thermal



TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

<Core Design>

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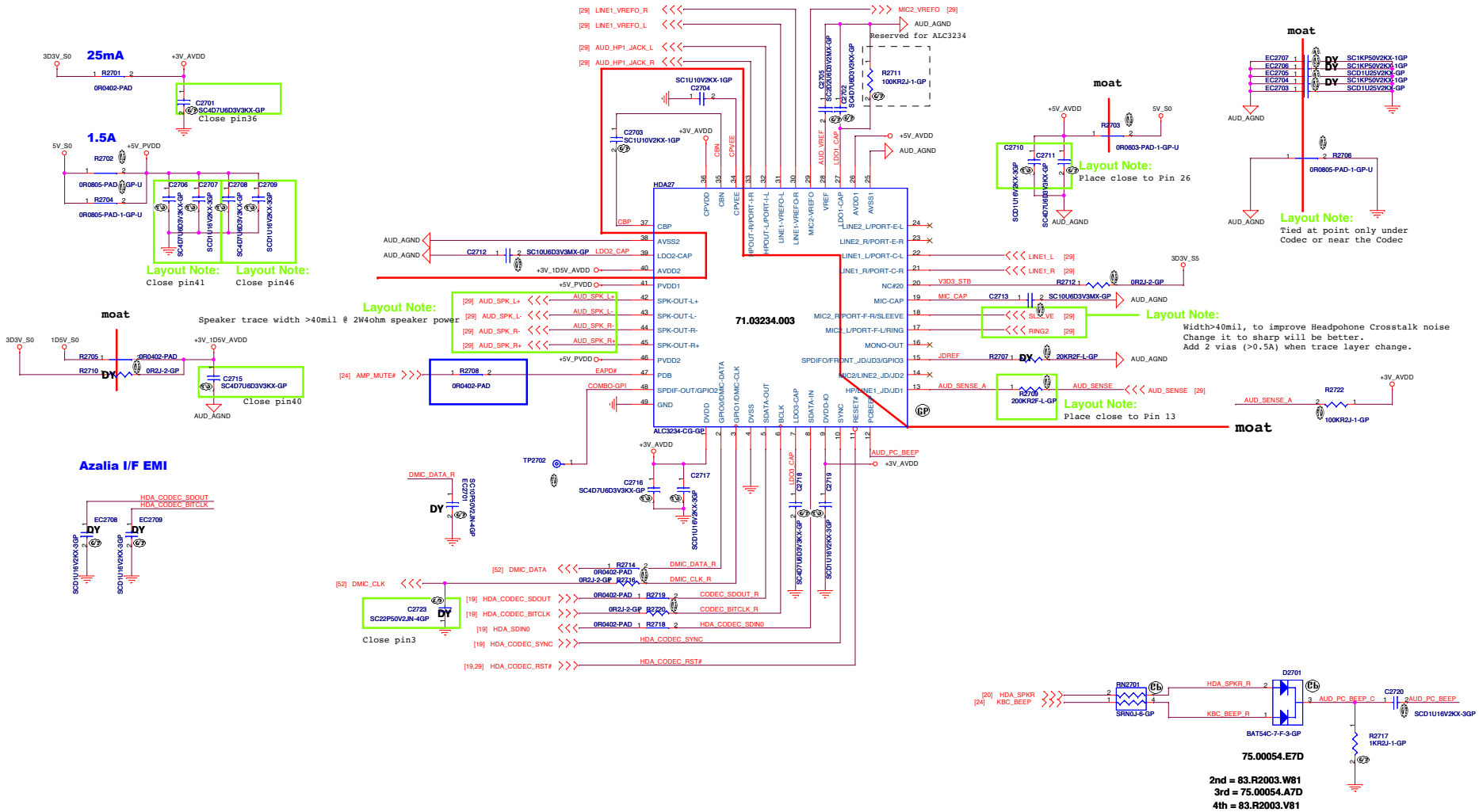
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 26 of 104

SSID = AUDIO



<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3234

Size	Document Number	Rev
A2	Janus HSW 40/50/70	A00

Date: Monday, February 10, 2014 Sheet 27 of 104

(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

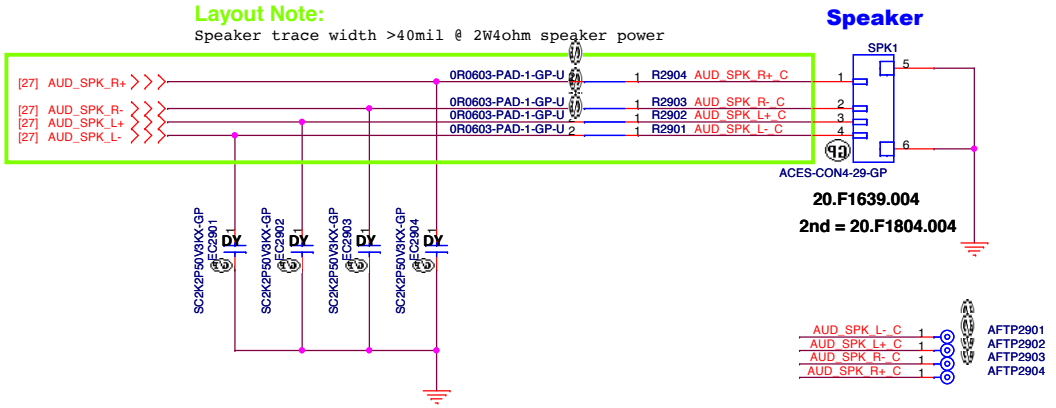
Reserved

Size	Document Number	Rev
A4	***Janus HSW 40/50/70***	***A00***

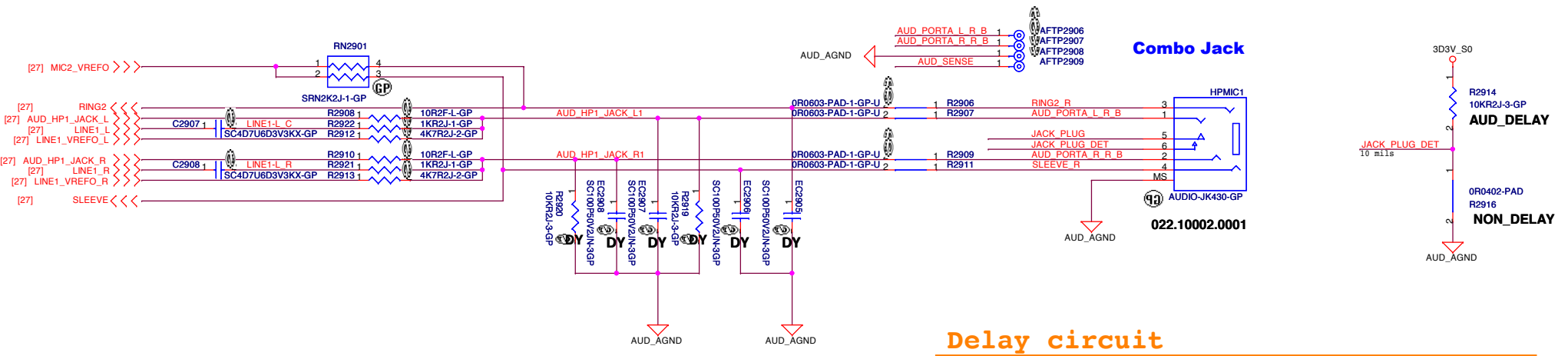
Date: Friday, February 07, 2014 Sheet 28 of 104

SSID = AUDIO

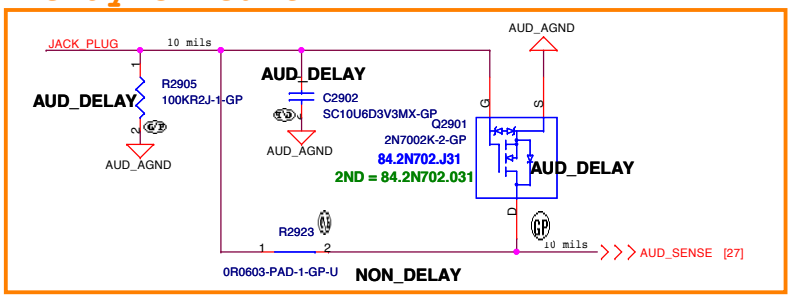
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

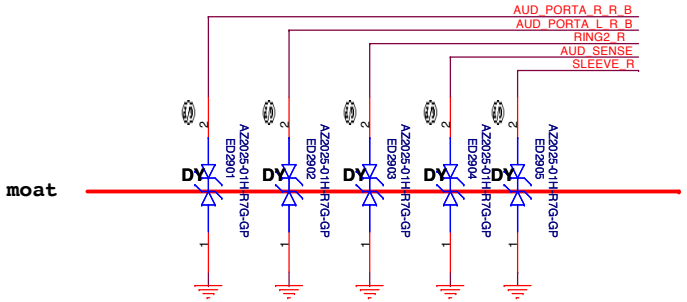


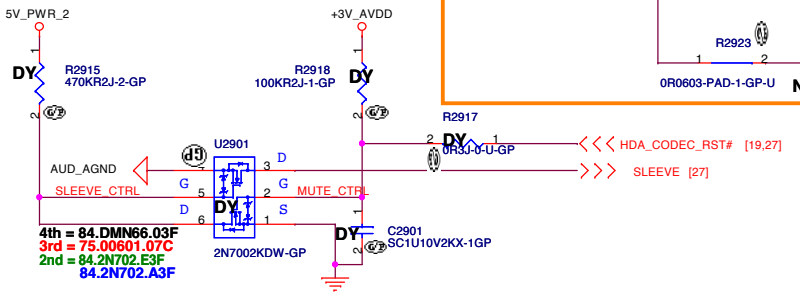
CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



Delay circuit







<Core Design>

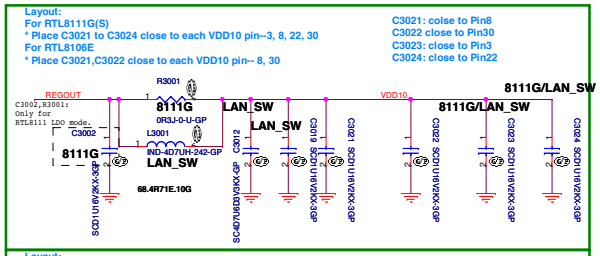
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

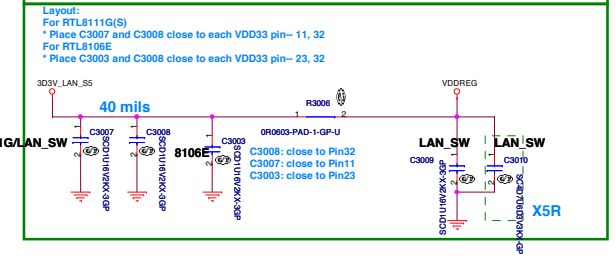
Title: Speaker/HPMIC

Size	Document Number	Rev
A3	Janus HSW 40/50/70	A00

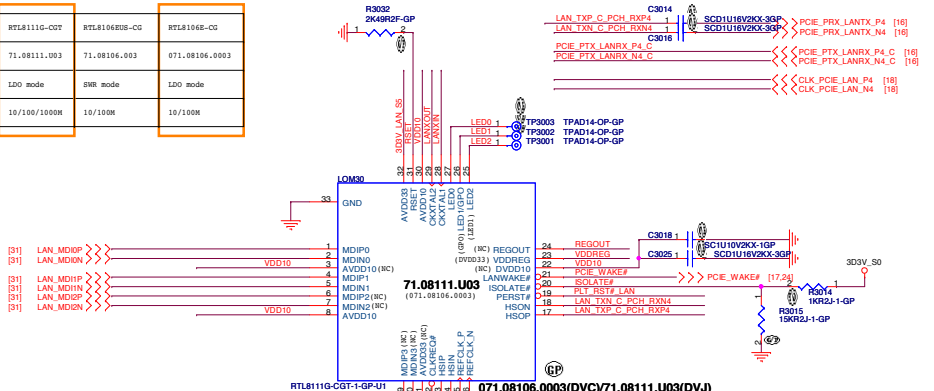
Date: Friday, February 07, 2014 Sheet 29 of 104

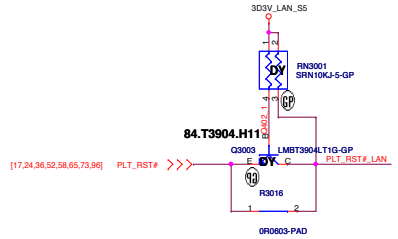
LAN CHIP (10/100/1000M & 10/100M co-lay)

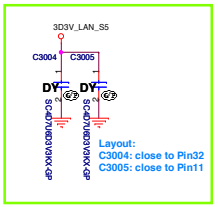


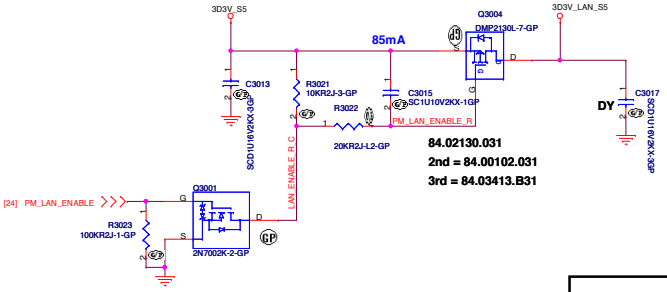


RTL8111GUS-CG	RTL8111G-CGT	RTL8106EUS-CG	RTL8106E-CG
71.08111.W03	71.08111.U03	71.08106.003	071.08106.0003
SWR mode	LDO mode	SWR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M

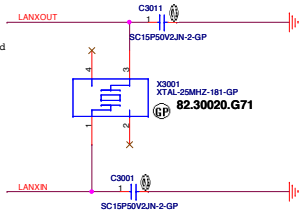


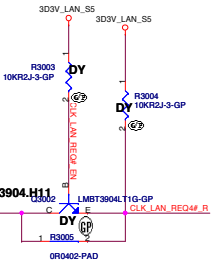






3D3V_LAN_S5 rise time must be controlled between 0.5 mS and 100 mS.





	1.0V Source	R3001	C3002	C3023	C3024	C3007	L3001	C3012	C3019	C3009	C3010	C3003
RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X	X	X	X	X	X
RTL8111GUS-CG (71.08111.W03)/ RTL8106EUS-CG (71.08106.003)	SWR	X	X	O	O	O	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	X	X	X	X	X	O

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8111/RTL8106

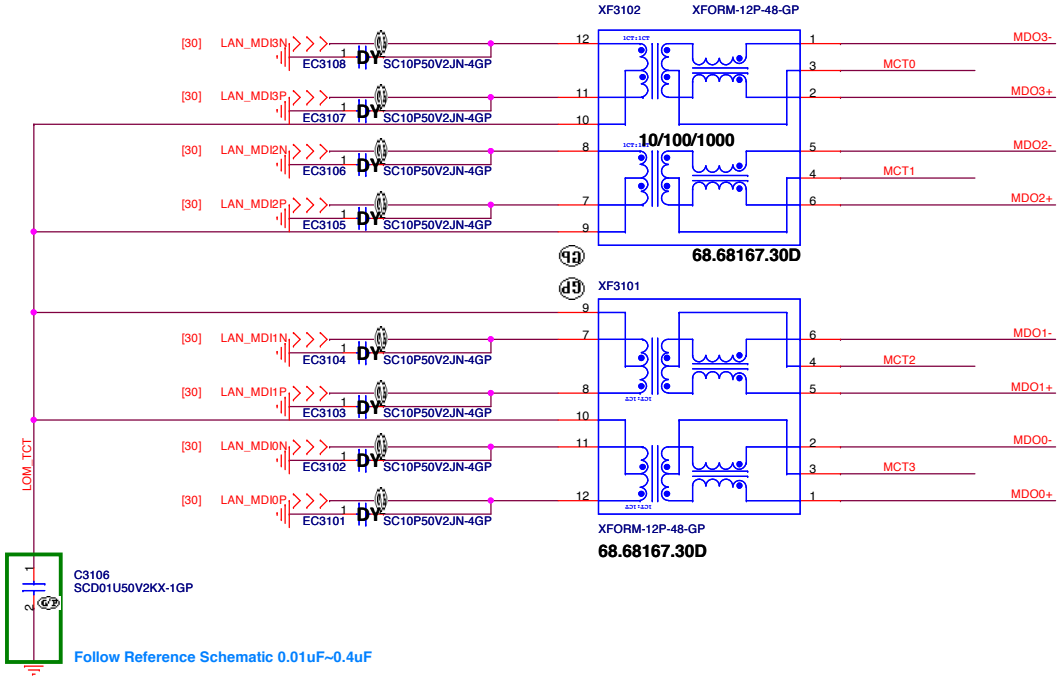
Size: A2 | Document Number: Janus HSW 40/50/70 | Rev: A00

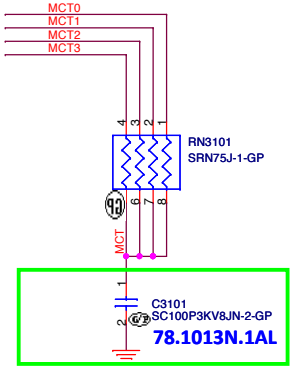
Date: Friday, February 07, 2014 | Sheet 30 of 104

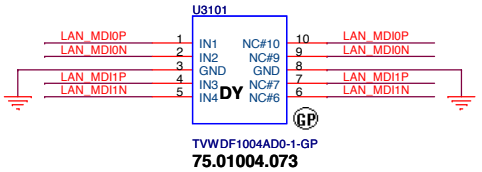
SSID = LOM

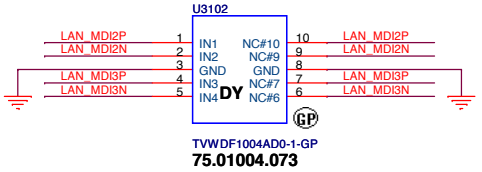
LAN TransFormer (10/100/1000M & 10/100M co-lay)

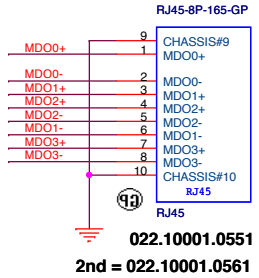
Layout note:
30 mil spacing between MDI differential pairs.



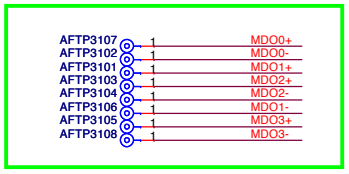








Layout:
Place near RJ45



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: XFOM&RJ45

Size	Document Number	Rev
A3	Janus HSW 40/50/70	A00

Date: Monday, February 10, 2014 Sheet 31 of 104

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)Card Reader

Size	Document Number	Rev
A4	***Janus HSW 40/50/70***	***A00***

Date: Friday, February 07, 2014 Sheet 32 of 104

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	***Janus HSW 40/50/70***	***A00***

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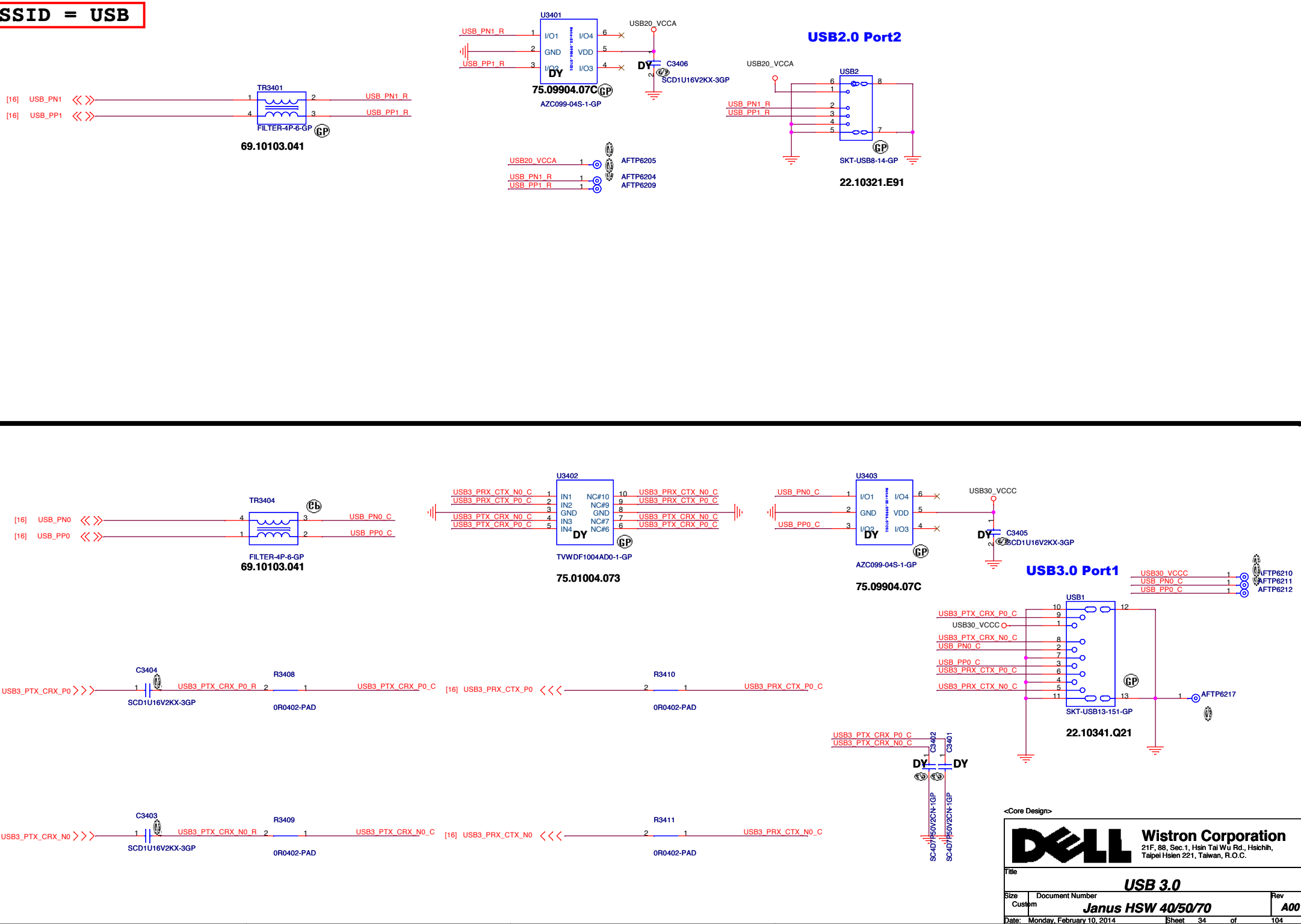
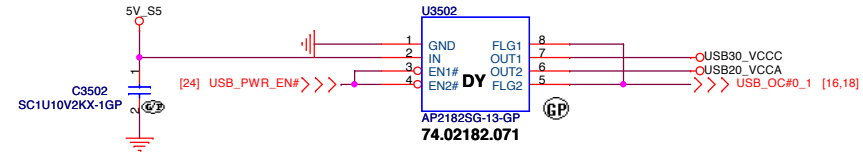
SSID = USB

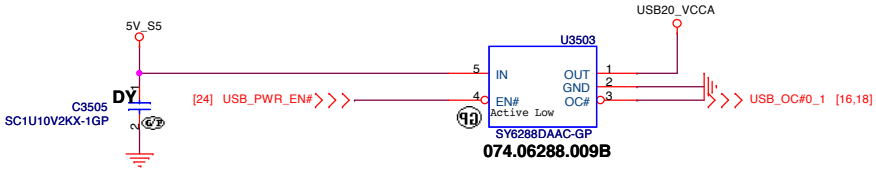


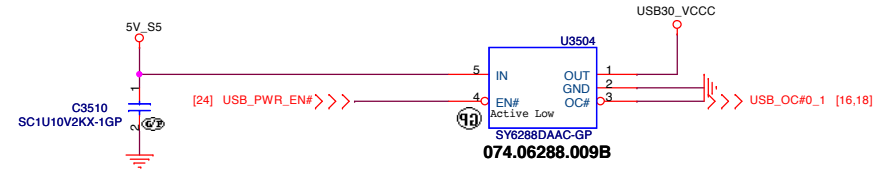
<Core Design>

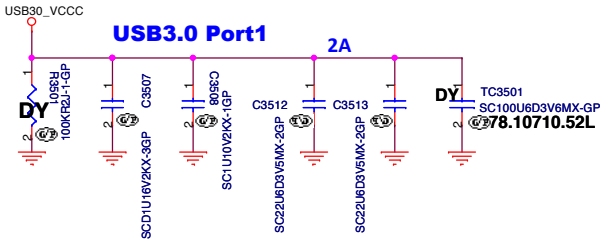
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

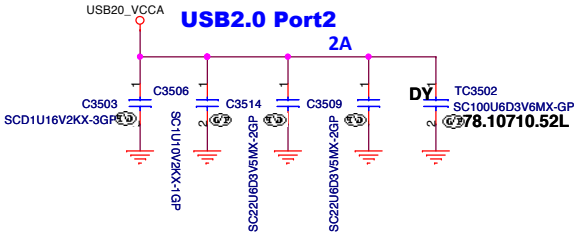
Title	USB 3.0	
Size: Custom	Document Number: Janus HSW 40/50/70	Rev: A00
Date: Monday, February 10, 2014	Sheet 34 of 104	



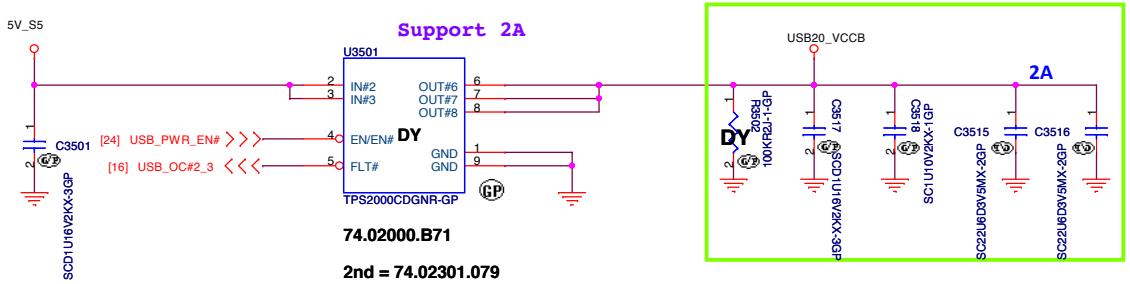




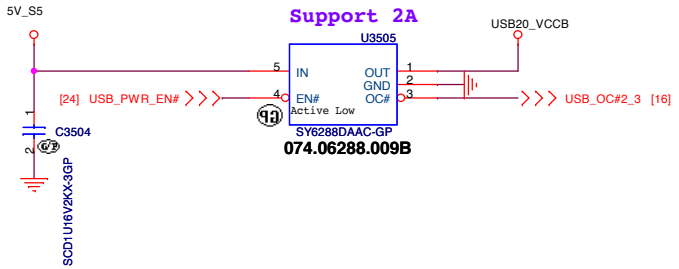




Layout Note: Close CON1



USB2.0 Port3 (IO Board)



<Core Design>

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Title	USB Power SW	
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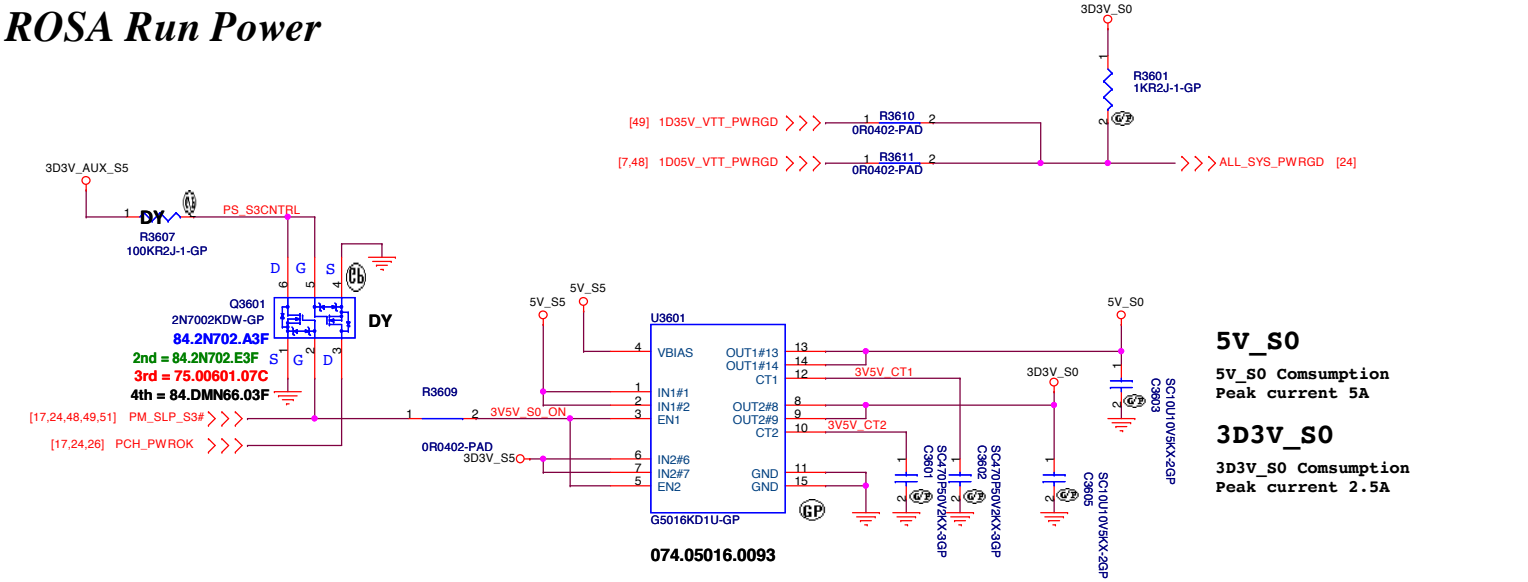
SSID = Reset.Suspend

Power Good

ROSA Run Power

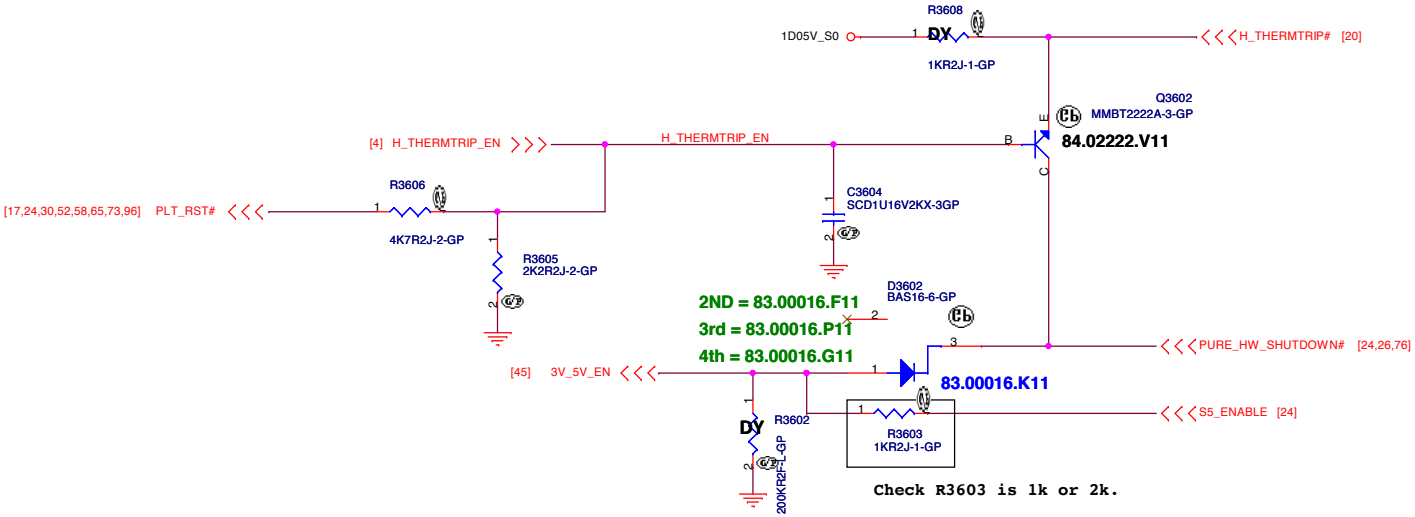


5V_S0

5V_S0 Comsumption
Peak current 5A

3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A



Check R3603 is 1k or 2k.

<Core Design>

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Title: Power Plane Enable

Size	Document Number	Rev
A3	Janus HSW 40/50/70	A00

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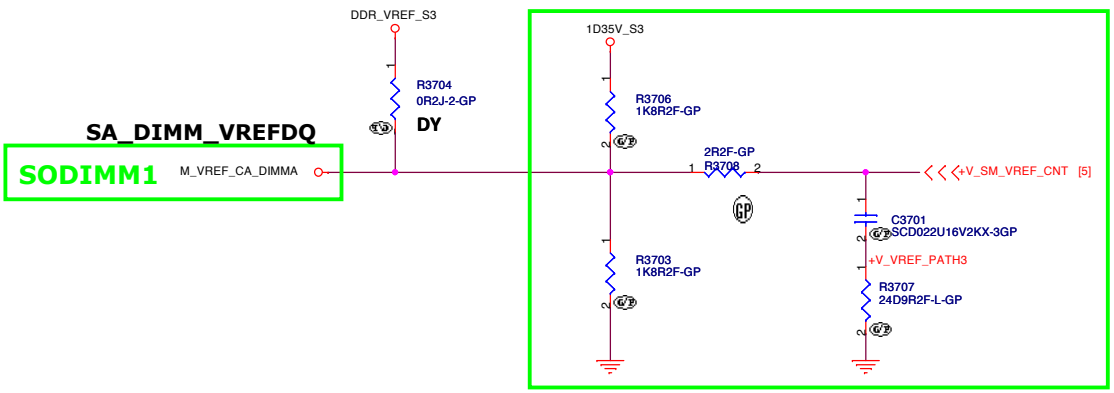
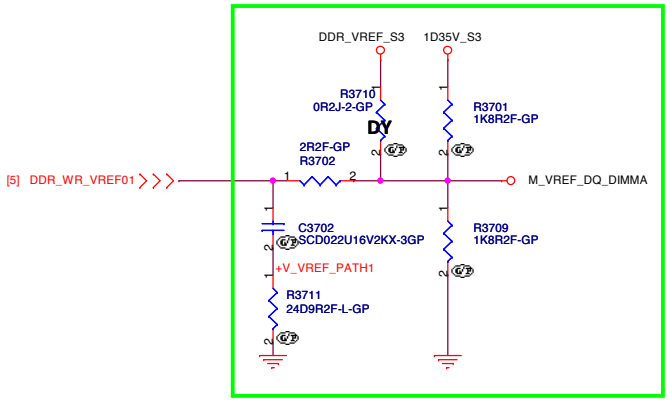
SSID = Reset.Suspend

Layout Note:
Place Close SO-DIMM1



Layout Note:
Place Close SO-DIMM1



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *S3 Reduction Circuit*

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

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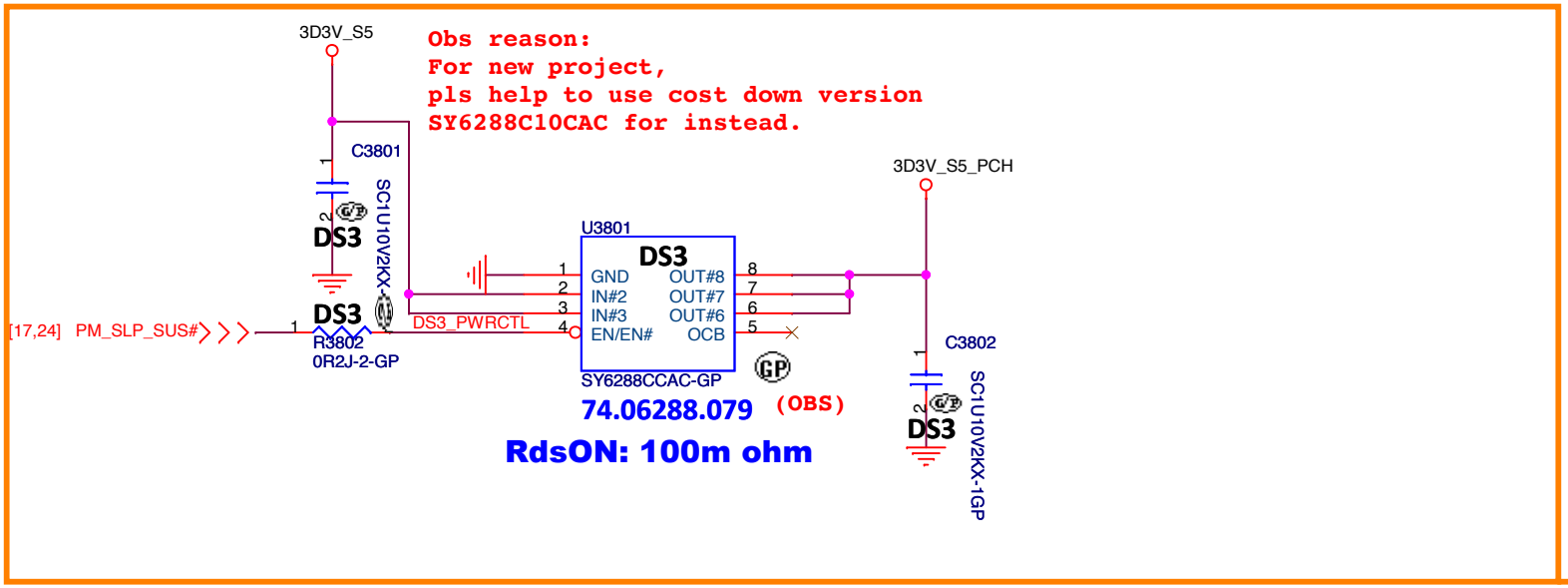

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *DSW*		
Size: A4	Document Number: *Janus HSW 40/50/70*	Rev: *A00*
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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved) 1D05_M*

Size	Document Number	Rev
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(Blanking)

<Core Design>

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Title
Reserved

Size	Document Number	Rev
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<Core Design>

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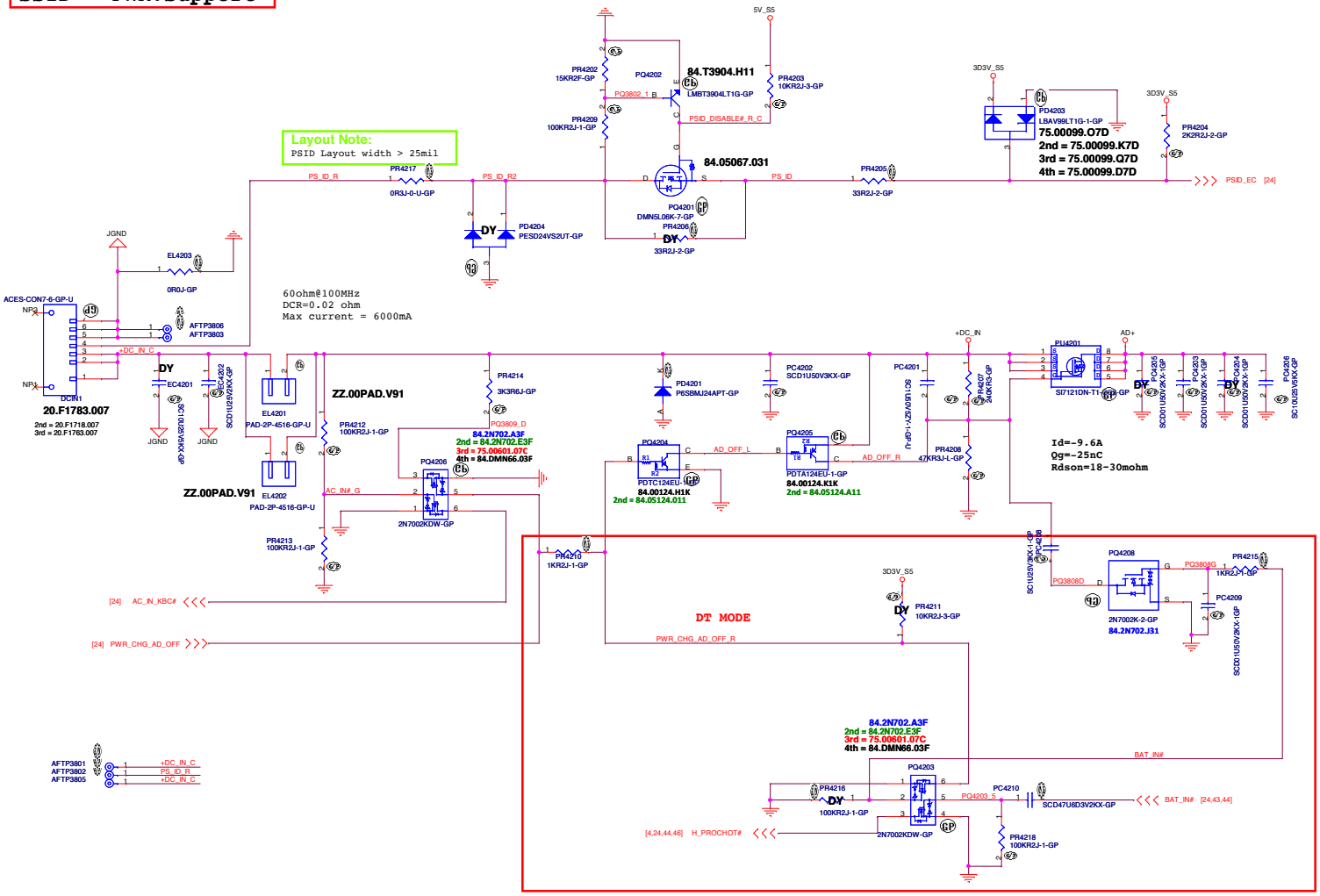
Title

Reserved

Size	Document Number	Rev
A4	***Janus HSW 40/50/70***	***A00***

Date: Friday, February 07, 2014 Sheet 41 of 104

SSID = PWR.Support



<Core Design>

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Title		
DCIN		
Size: A2	Document Number: Janus HSW 40/50/70	Rev: A00
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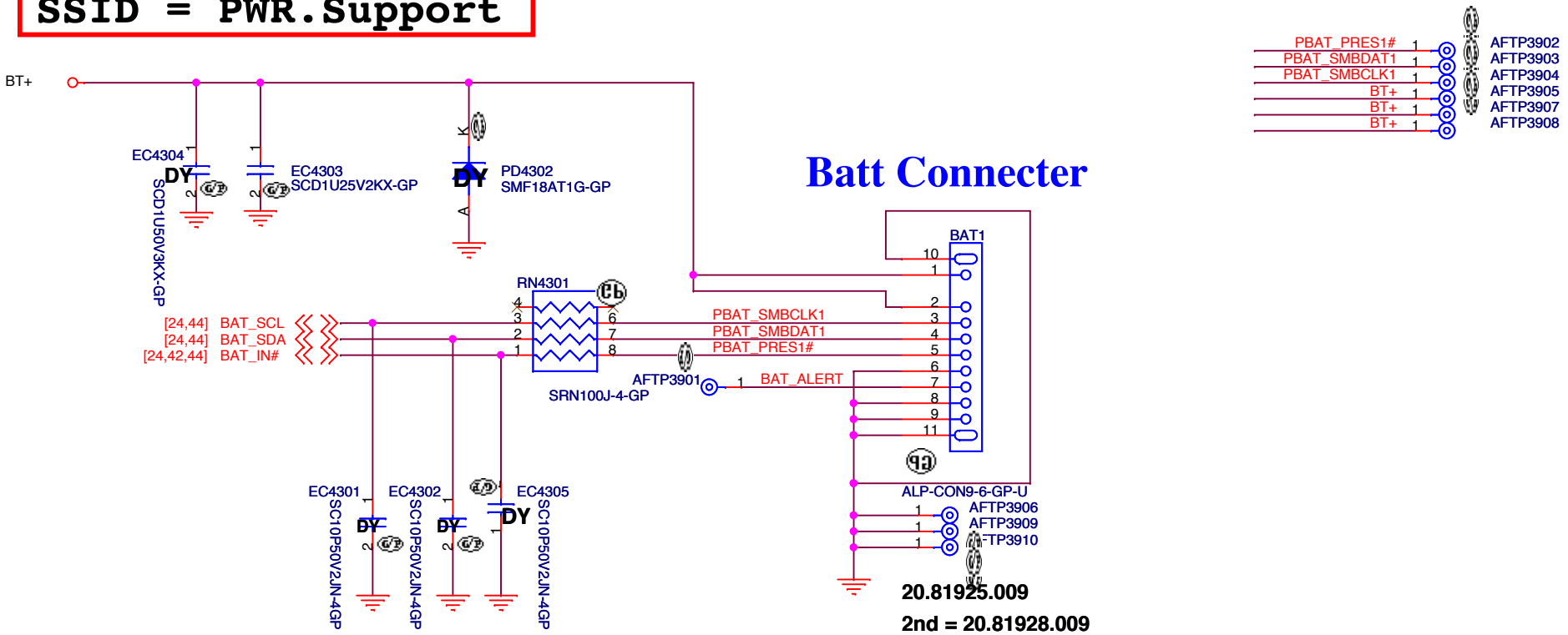
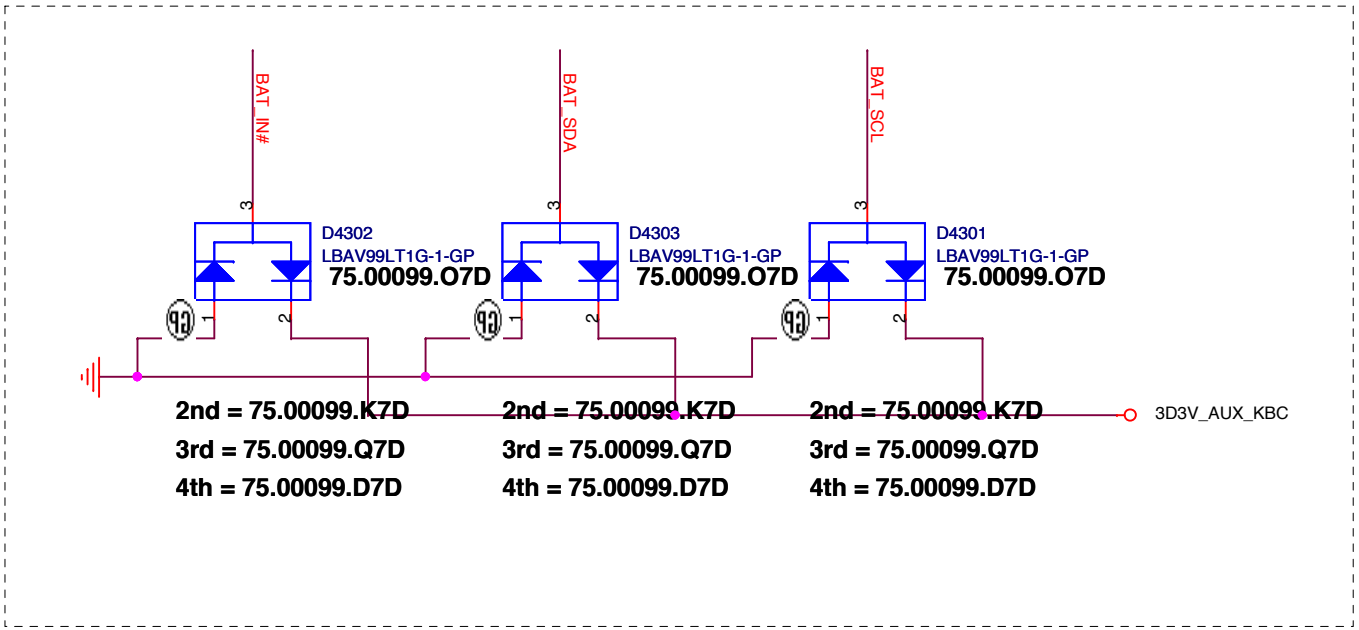
SSID = PWR.Support



Placement: Close to Batt Connector



<Core Design>

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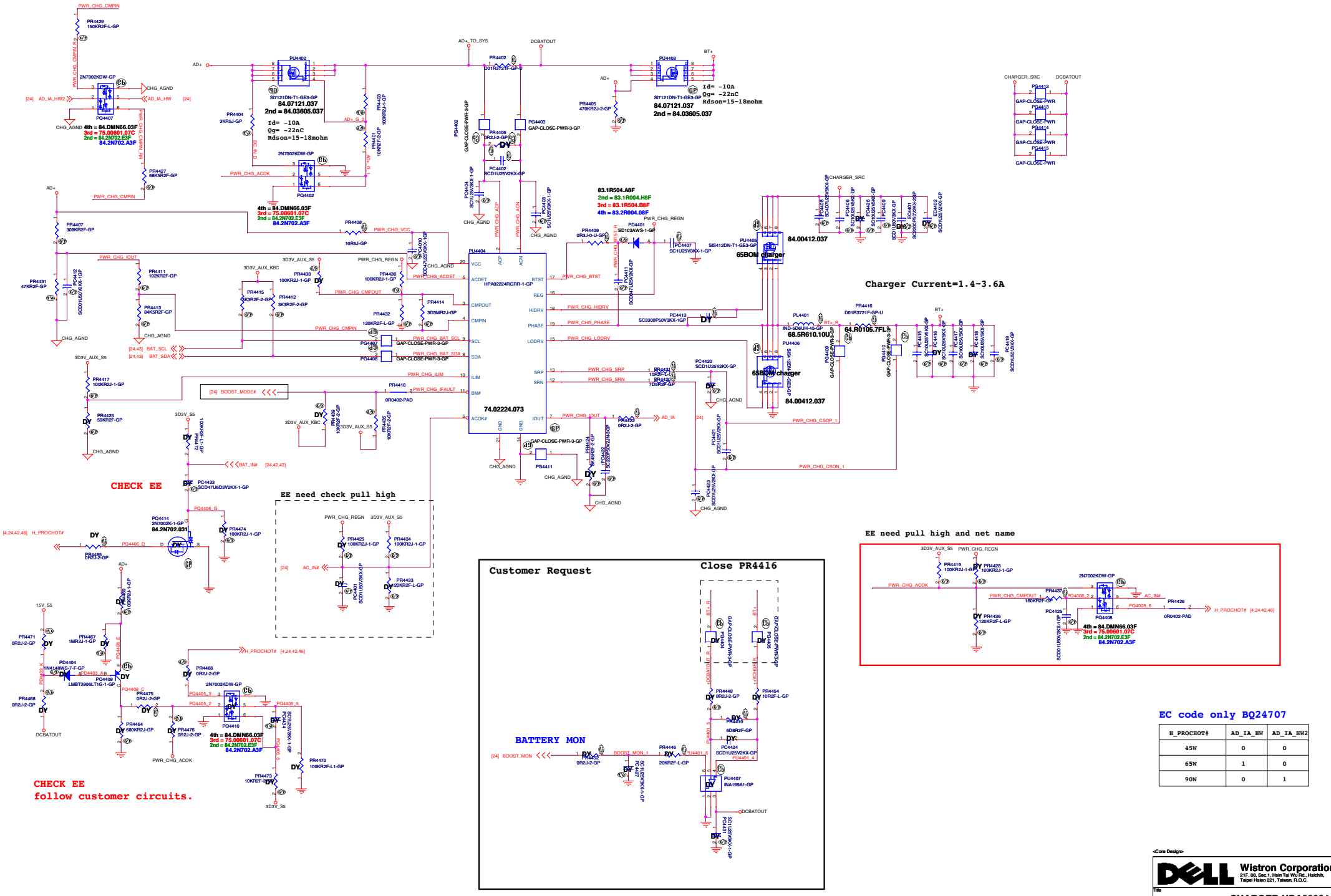
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BATT CONN**

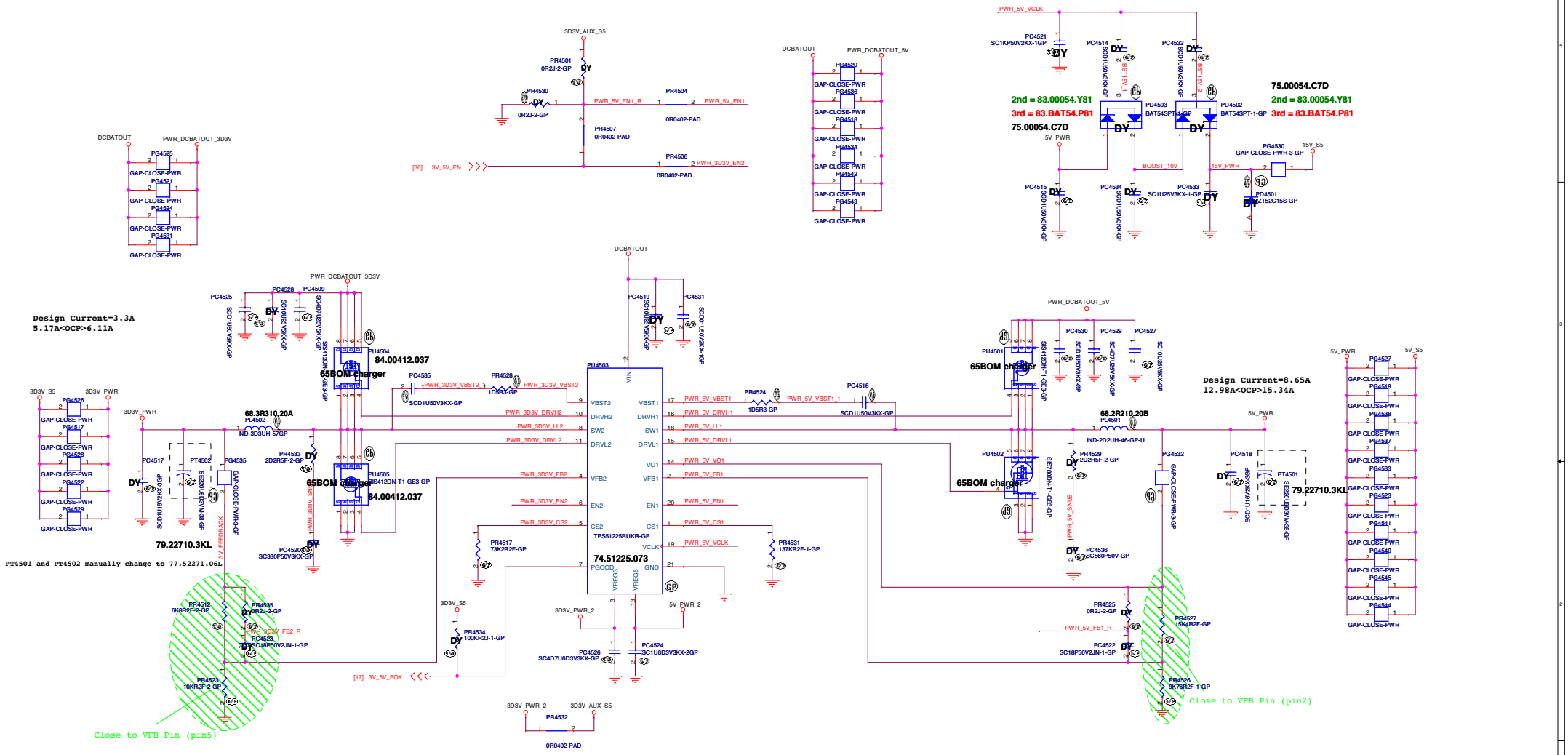
Size	Document Number	Rev
A4	Janus HSW 40/50/70	A00

Date: Friday, February 07, 2014 Sheet 43 of 104

SSID = Charger



SSID = PWR.Plane.Regulator_5v3p3v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap:CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuki/ 17mOhm / 77.52271.09L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

TPS51225 & TPS51285 Co-lay

	TPS51225	TPS51285
PR4510	45.3KK	9.09K
PR4511	110K	22.1K

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap:CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuki/ 17mOhm / 77.52271.09L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

<Core Design>

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Title: 3V/5V TPS51225

Size: A2 | Document Number: Janus HSW 40/50/70 | Rev: A00

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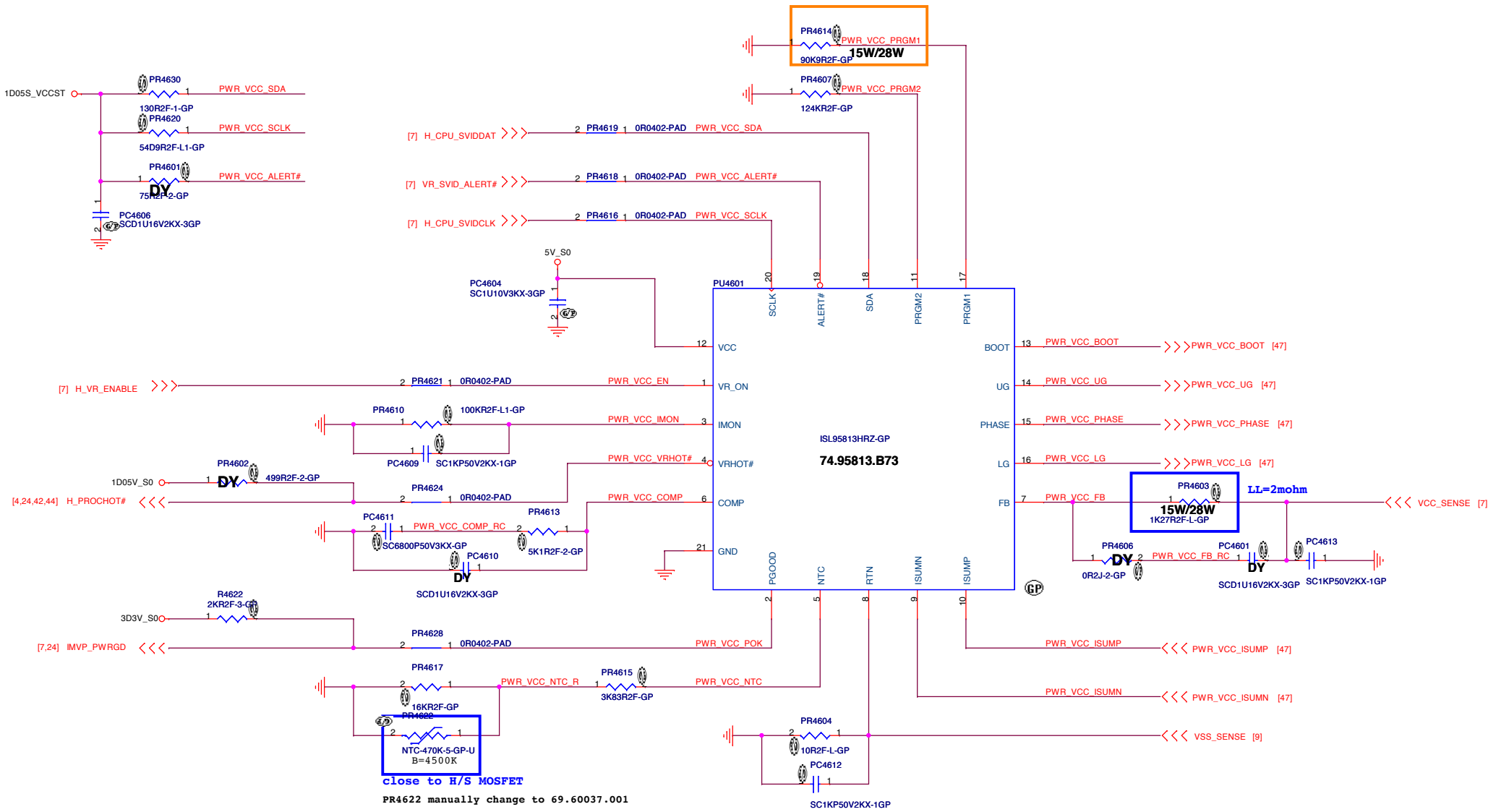
SSID = CPU.Regulator



	PR4603	PR4614
15W	1.27K 64.12715.6DL	90.9K 64.90925.6DL
28W	1.58K 64.15815.6DL	113K 64.11335.6DL

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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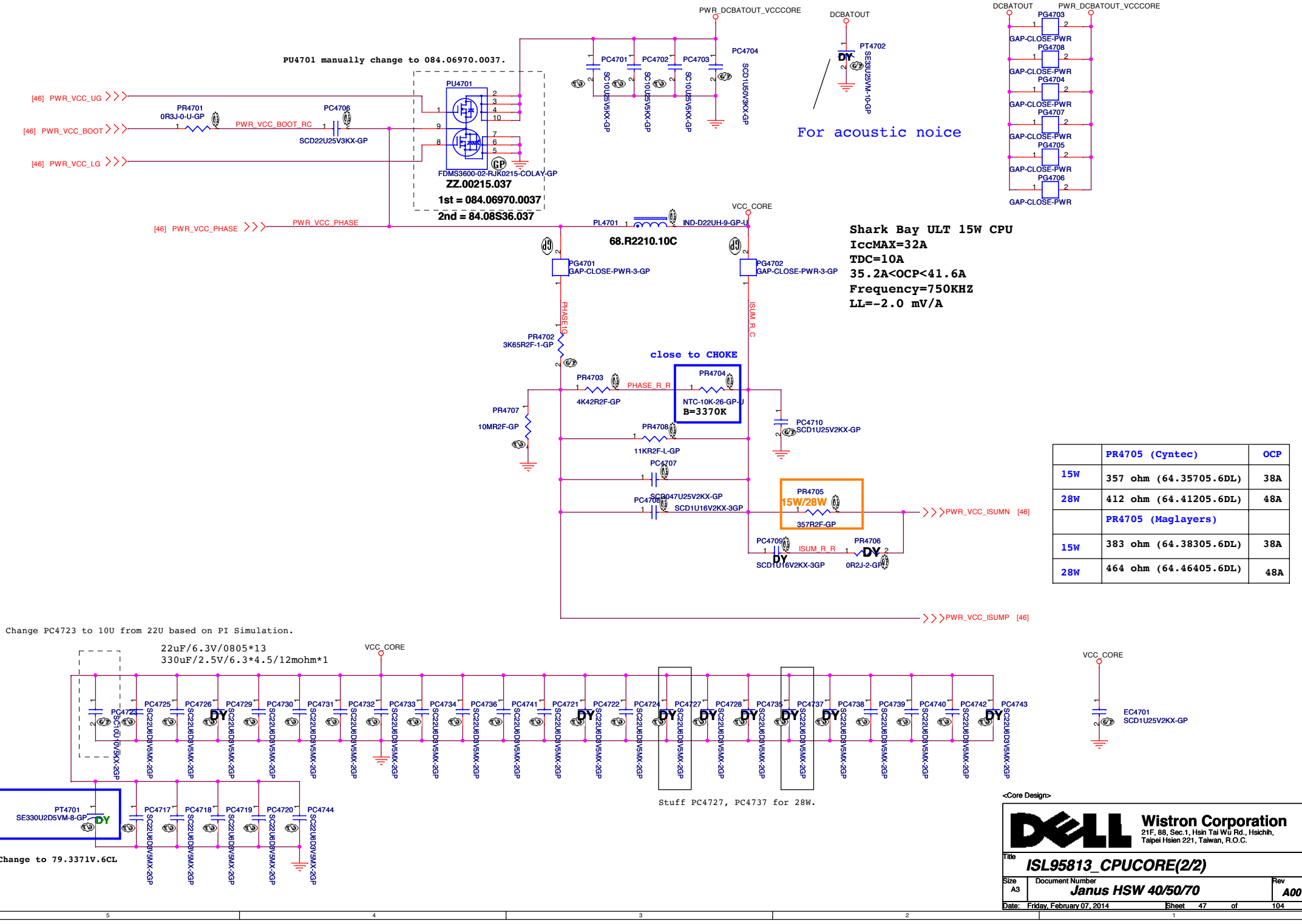
Title: ISL95813_CPUCORE(1/2)

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 46 of 104



	PR4705 (Cyntec)	OCP
15W	357 ohm (64.35705.6DL)	38A
28W	412 ohm (64.41205.6DL)	48A
	PR4705 (Maglayers)	
15W	383 ohm (64.38305.6DL)	38A
28W	464 ohm (64.46405.6DL)	48A

<Core Design>

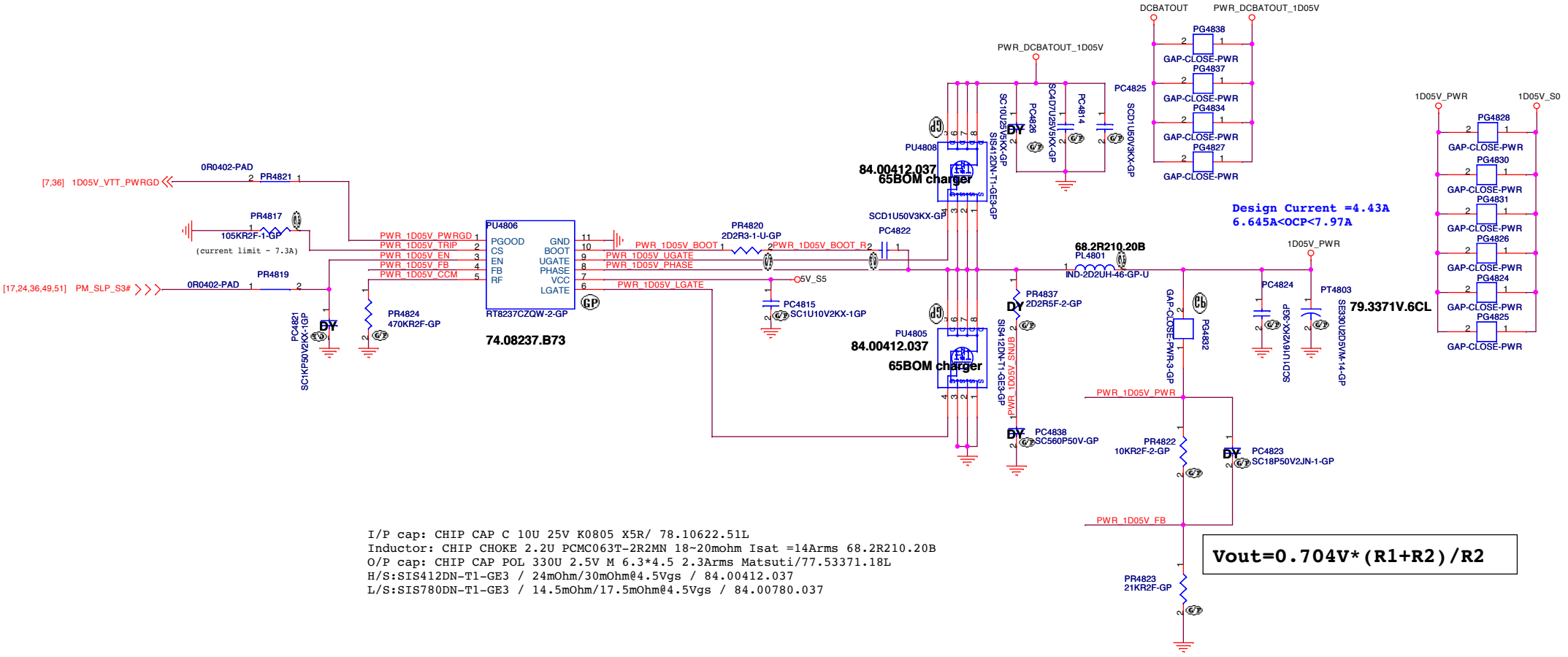
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95813_CPUCORE(2/2)

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 47 of 104

SSID = PWR.Plane.Regulator_1p05v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18~20mohm Isat =14Arms 68.2R210.20B
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780DN-T1-GE3 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

<Core Design>

Wistron Corporation
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Title	RT8237_1D05V	
Size A3	Document Number Janus HSW 40/50/70	Rev A00
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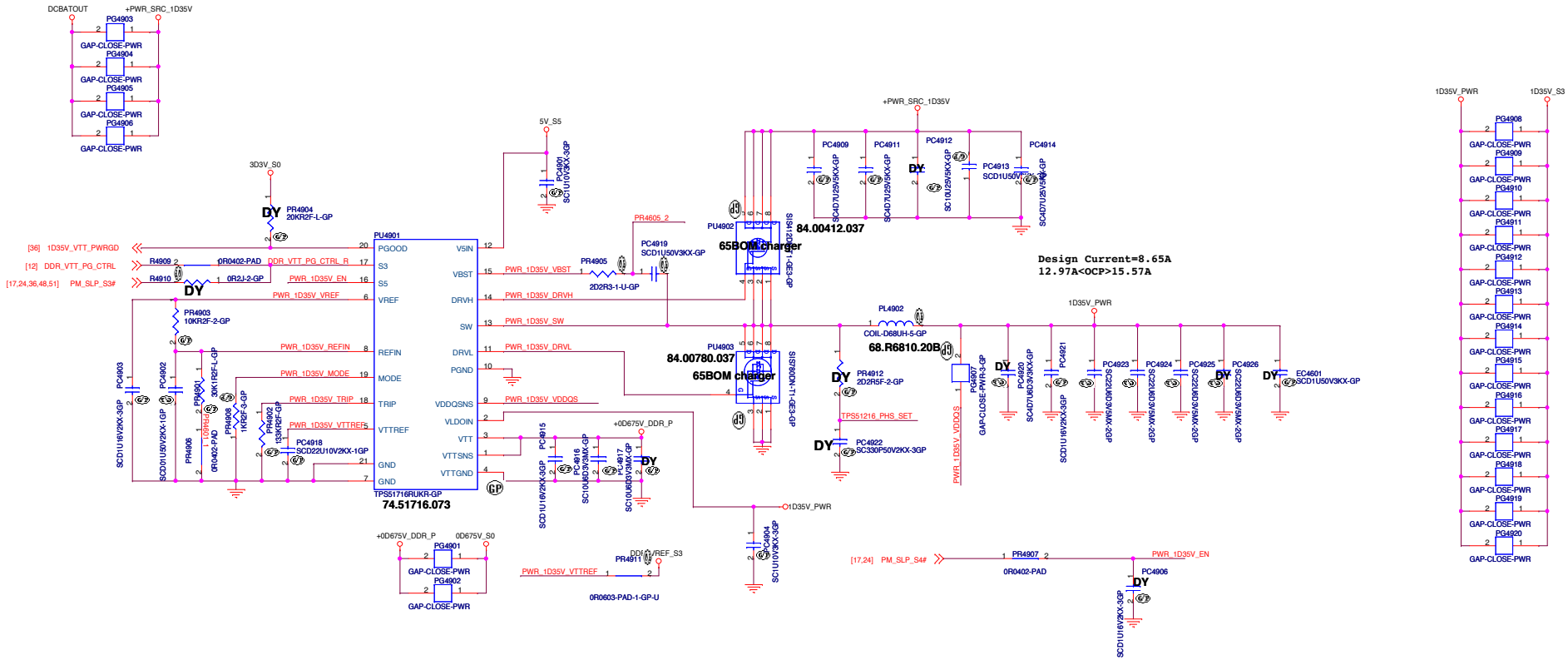
SSID = PWR.Plane.Regulator_1p35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 0.1UH M PCMC063T-R10MN 1.5~1.7mohm Isat =60Arms 68.R1010.10T
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
MOS: FET MOS FDMS3664S NC POWER56 / 84.03664.037 / Q1: 8.5~11mohm @Vgs=4.5V Q2: 2.6~3.2mohm @Vgs=4.5V

<Core Design>

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Title: TPS51716_1D35V_S3
Size: C
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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Janus HSW 40/50/70* | Rev: *A00*

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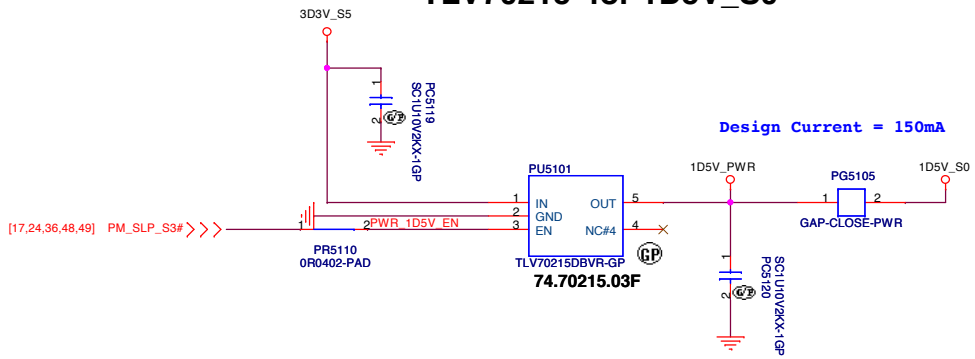
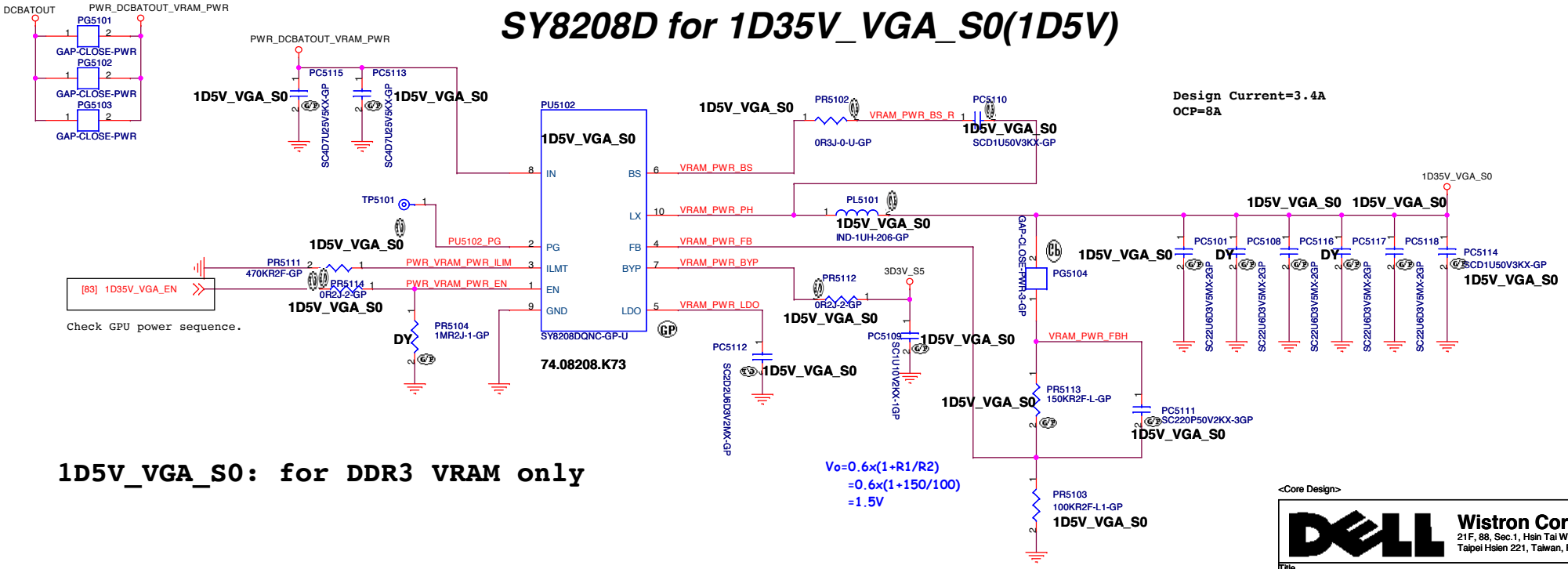
SSID = PWR.Plane.Regulator_1p5v

TLV70215 for 1D5V_S0



SY8208D for 1D35V_VGA_S0(1D5V)



1D5V_VGA_S0: for DDR3 VRAM only

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *TLV70215_1D5V / SY8208D_1D5V(VGA)*

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INVERTER POWER

CAM1

EE note: Never change R5229 to short pad after MP
Reserved for one time fuse: 69.43001.201

EE note: Never change R5211 to short pad after MP

EE note: Never change R5232 to short pad after MP
Reserved for one time fuse: 69.43001.201

LCD

Camera

Touch Panel

Brightness

EC (BIST MODE)

LCDVDD

Layout Note: Reduce the stubs.

Layout Note: Reduce the stubs.

Layout Note:
Trace width = 80mil

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter CONN

Size: A2 | Document Number: Janus HSW 40/50/70 | Rev: A00

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<Core Design>

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Title
(Reserved)

Size	Document Number	Rev
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Date: Friday, February 07, 2014 Sheet 53 of 104

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<Core Design>

Wistron Corporation
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Title
HDMI Level Shifter/Connector

Size	Document Number	Rev
A3	Janus HSW 40/50/70	X02

Date: Friday, February 07, 2014 Sheet 54 of 104

CRT Board Connector

CRT RGB
CRT H/VSYNC
CRT SMBUS

69.48001.081
2ND = 69.50011.081
3RD = 69.50013.101

020.20020.0015

83.R5003.H8H

Hsync & Vsync level shift

Layout note:
All cap need close to chip

CRT DEBUG

071.02168.0003

	POL1_SDA(PIN22)	
POL2_SCL(PIN23)	0	1
0	X	EP MODE
1	ROM ONLY MODE	EEPROM MODE

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

1- EEPROM with a size of 16K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

1	0	1	0	A_2	A_1	A_0	R/W

DEVICE ADDRESS

Figure 3. Slave Address Bits

<Core Design>

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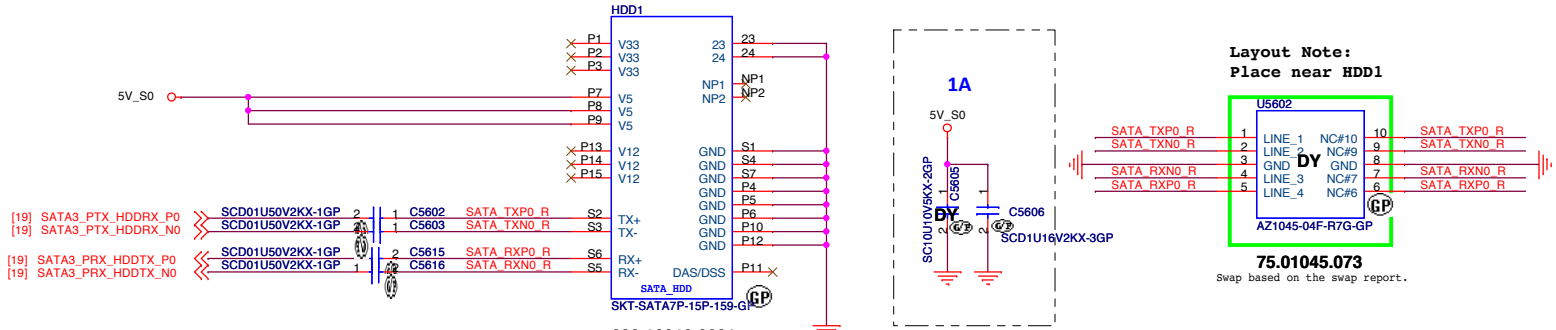
Title: (Reserved)DP to VGA Converter

Size: A2 | Document Number: Janus HSW 40/50/70 | Rev: X02

Date: Friday, February 07, 2014 | Sheet 55 of 104

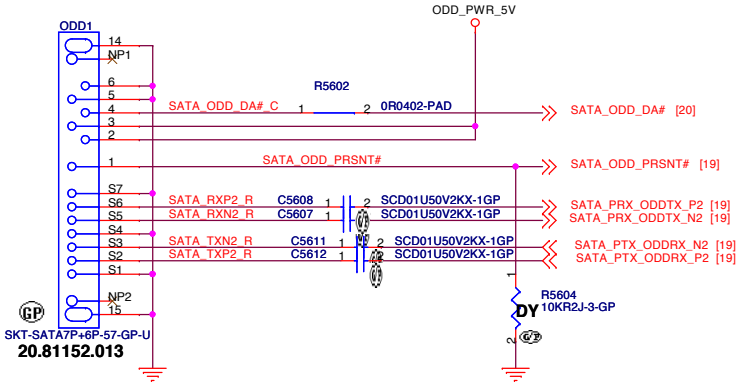
SSID = SATA

SATA HDD Connector

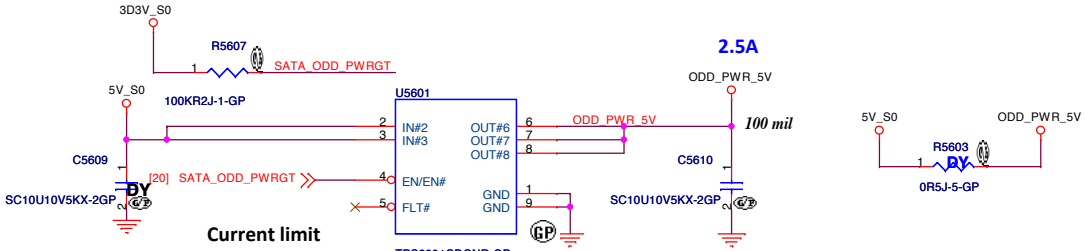


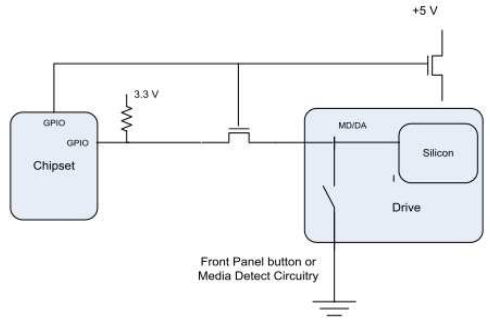
ME Note: New HDD conn symbol is not ready,
we will use original OAK HDD conn (22.10300.991) and shift to the correct position.

ODD Connector



SATA Zero Power ODD





<Core Design>

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Title		
HDD/ODD		
Size A3	Document Number: Janus HSW 40/50/70	Rev A00
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SSID = ESATA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ESATA		
Size: A3	Document Number: Janus HSW 40/50/70	Rev: A00
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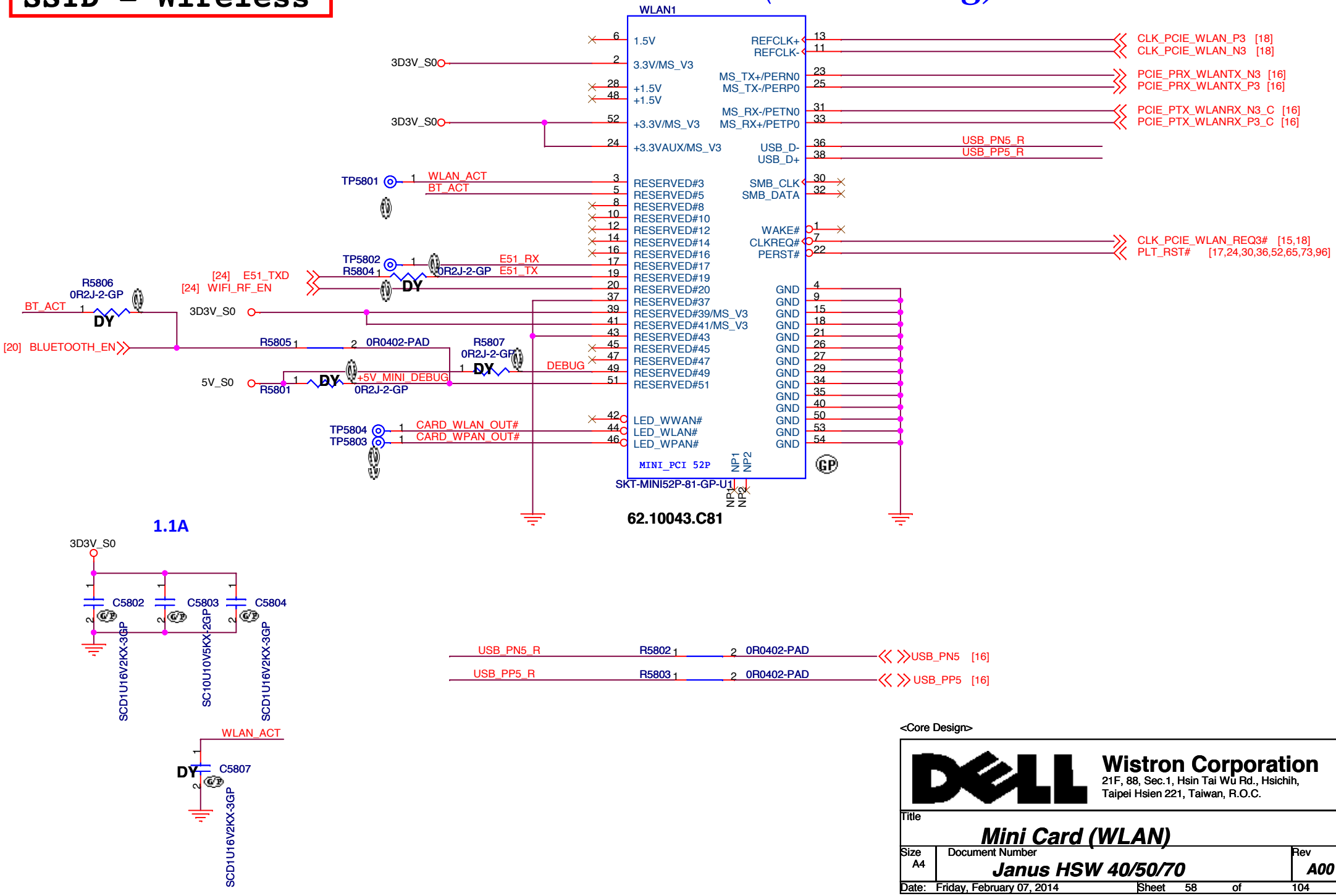
Mini Card Connector(802.11a/b/g)

SSID = Wireless



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Mini Card (WLAN)**		
Size: A4	Document Number: **Janus HSW 40/50/70**	Rev: **A00**
Date: Friday, February 07, 2014	Sheet 58 of 104	

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	*Janus HSW 40/50/70*	*A00*

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<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A4	***Janus HSW 40/50/70***	***A00***

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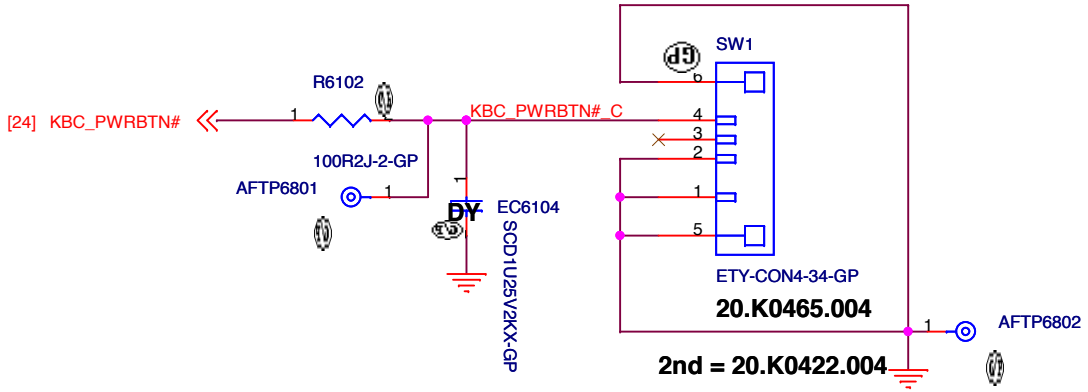
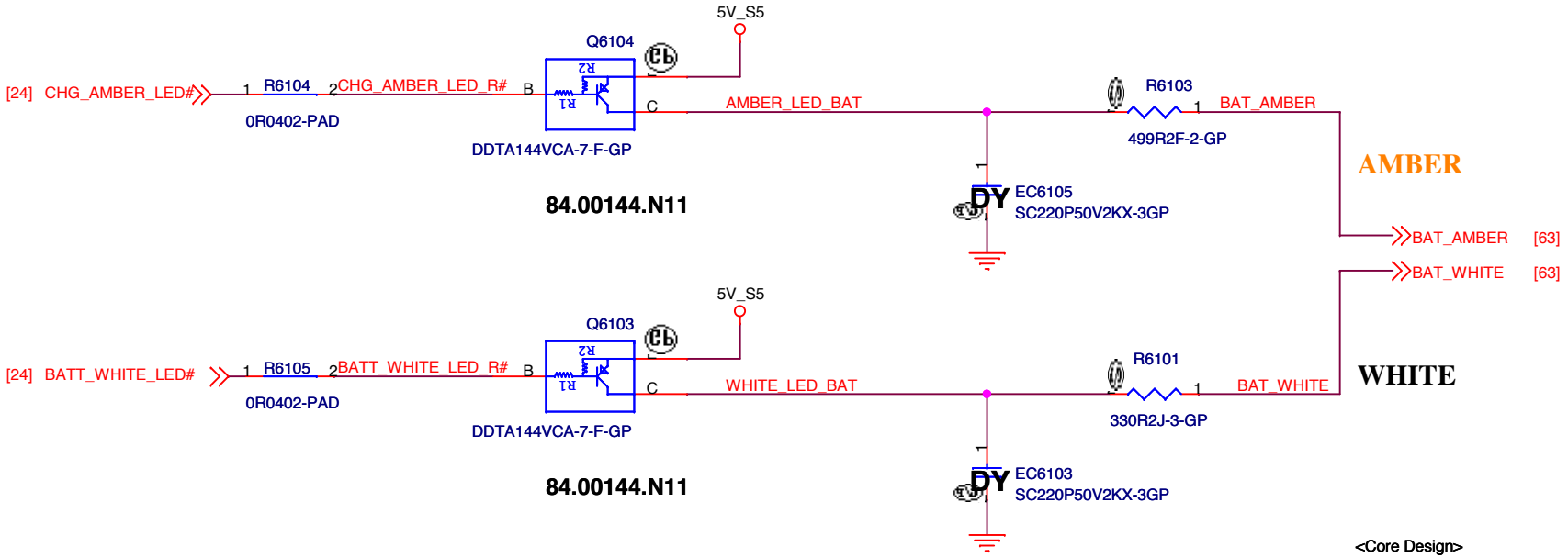
SSID = User.Interface

Power button



Battery LED1 (AMBER_LED)

Low actived from KBC GPIO



Battery LED2 (WHITE_LED)

Low actived from KBC GPIO

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Title: LED Bard/Power Button

Size	Document Number	Rev
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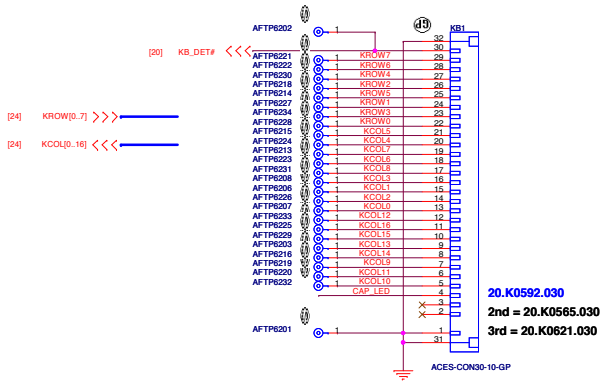
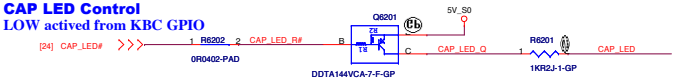
SSID = KBC

Internal Keyboard Connector (DVC40)



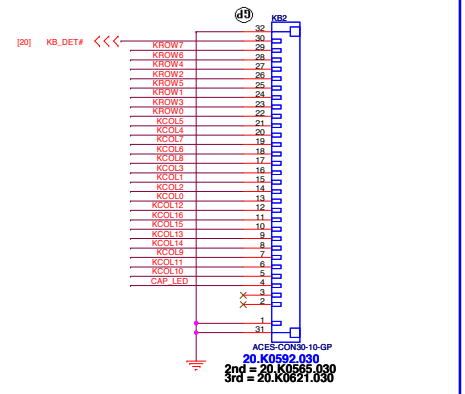
CAP LED Control

LOW actived from KBC GPIO



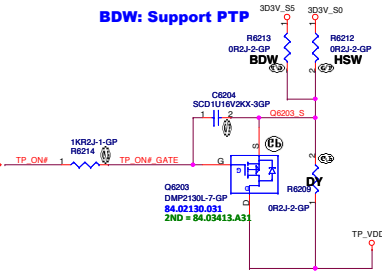
84.00144.N11

Internal Keyboard Connector (DVC50/DVC70)

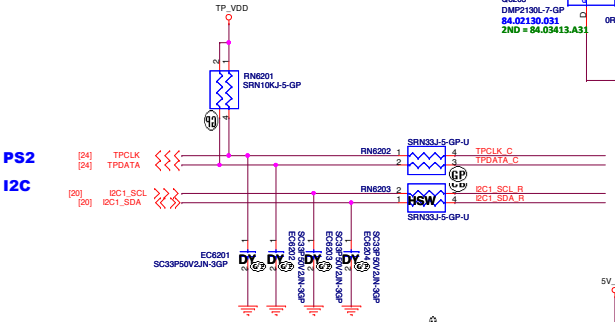


SSID = Touch.Pad

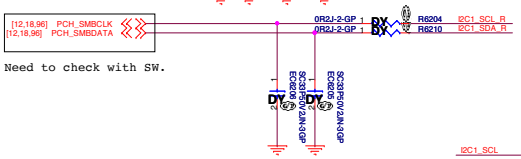
BDW: Support PTP



PS2 / I2C

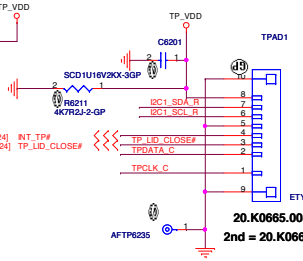


SMBUS



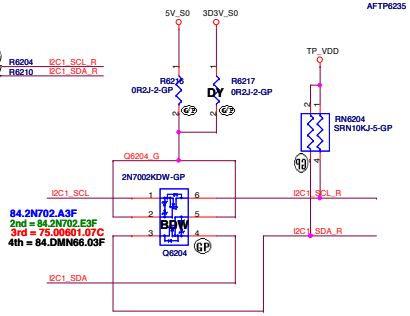
Need to check with SW.

Touch Pad Connector

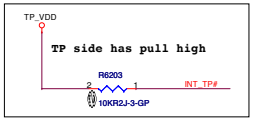


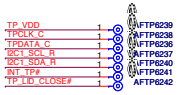
Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

20.K0665.008
2nd = 20.K0667.008

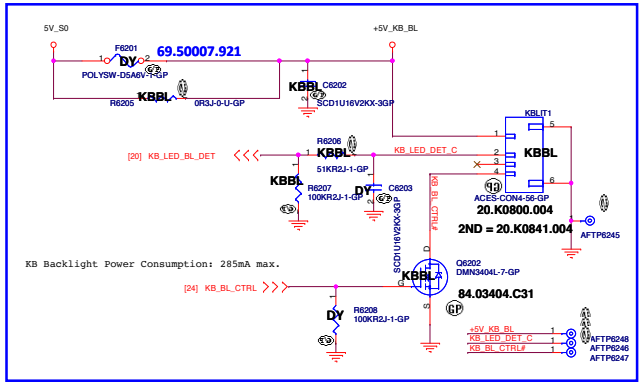


Need to check if it is Active High or Active Low and check if there is PH on TPAD side.





Keyboard Backlight (DVC70)



KB Backlight Power Consumption: 285mA max.

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Title		
Key Board/Touch Pad		
Size: A2	Document Number: Janus HSW 40/50/70	Rev: A00
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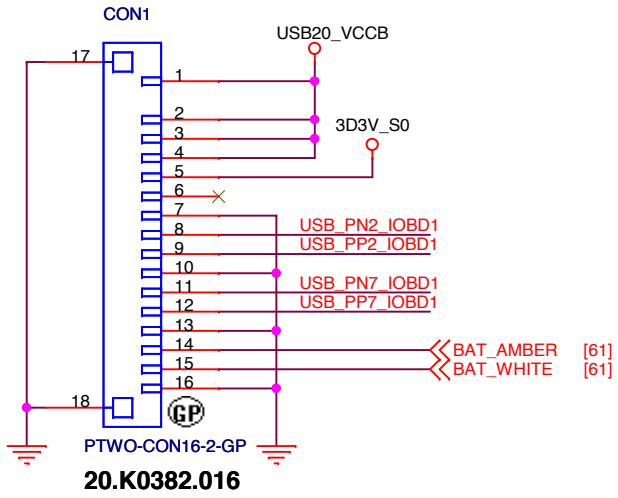
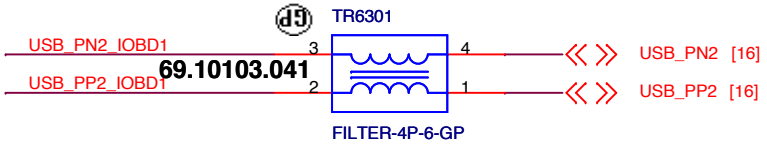
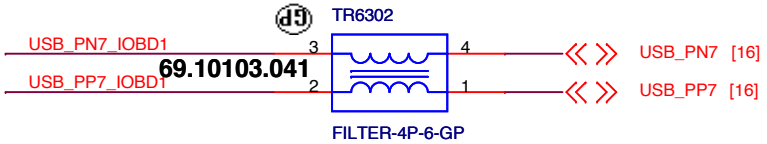


USB2.0 Port3

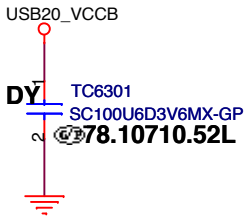
Card Reader

LED





The maximum range of the PMOS output current in RTS5170 (Card Reader IC) is 400mA



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Title: ***IO Board Connector***

Size	Document Number	Rev
A4	***Janus HSW 40/50/70***	***A00***

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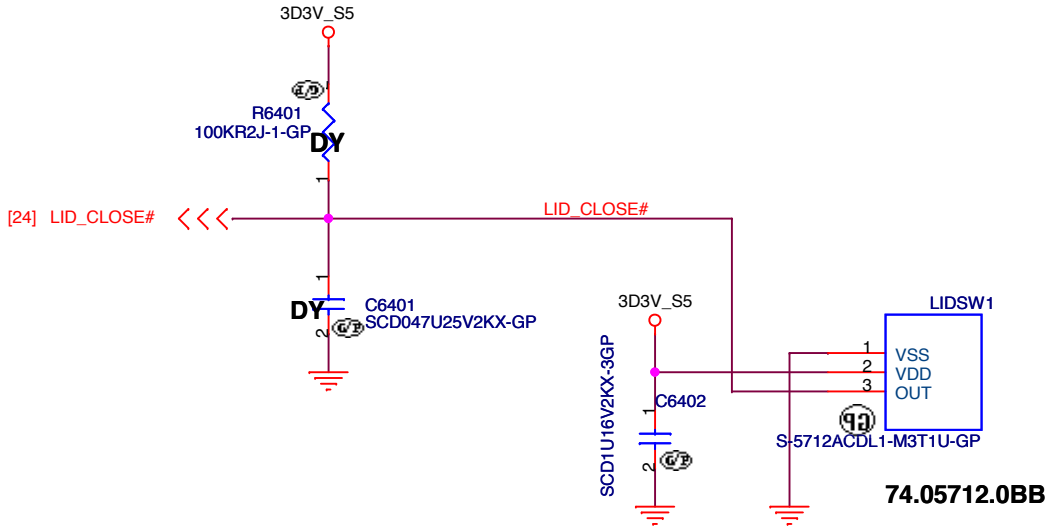
SSID = User.Interface



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Title: ***Hall Sensor***

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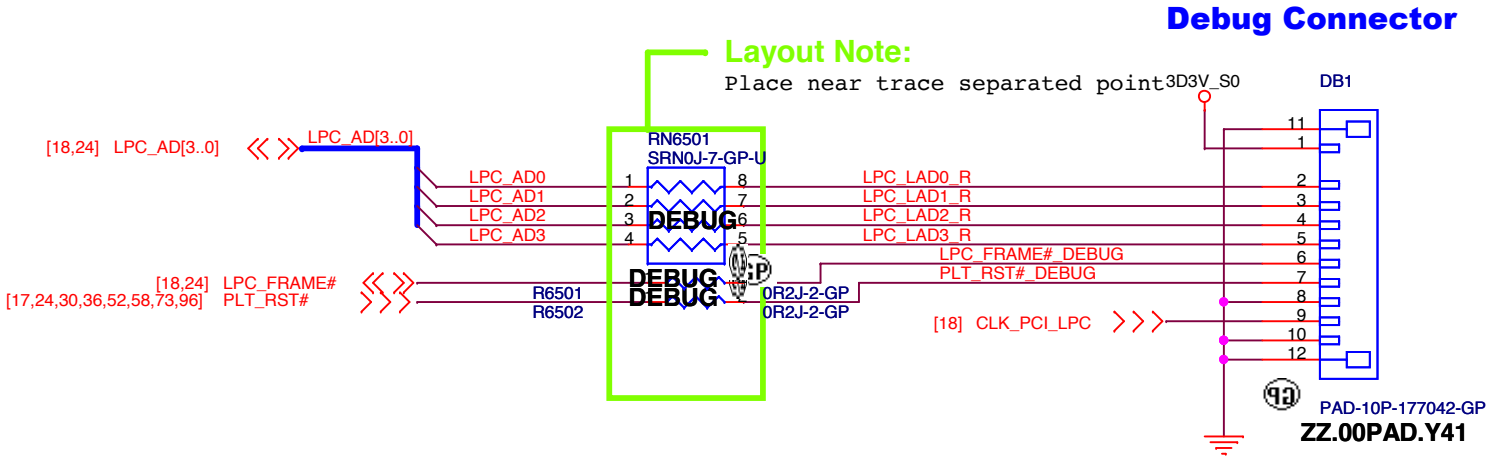
SSID = DEBUG PORT



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

<Core Design>

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Title	Dubug connector	
Size: A4	Document Number: Janus HSW 40/50/70	Rev: A00
Date: Friday, February 07, 2014	Sheet 65 of 104	

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Title

Reserved

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A4	***Janus HSW 40/50/70***	***A00***

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Title: *Reserved*

Size: A3 | Document Number: *Janus HSW 40/50/70* | Rev: *A00*

Date: Friday, February 07, 2014 | Sheet 67 of 104

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Title

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Size	Document Number	Rev
A3	*Janus HSW 40/50/70*	*A00*

Date: Friday, February 07, 2014 Sheet 68 of 104

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Title: USB3.0 PORT

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

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Title: *Reserved*

Size	Document Number	Rev
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Title: *Reserved*

Size: A3 | Document Number: *Janus HSW 40/50/70* | Rev: *A00*

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Title: *Reserved*

Size	Document Number	Rev
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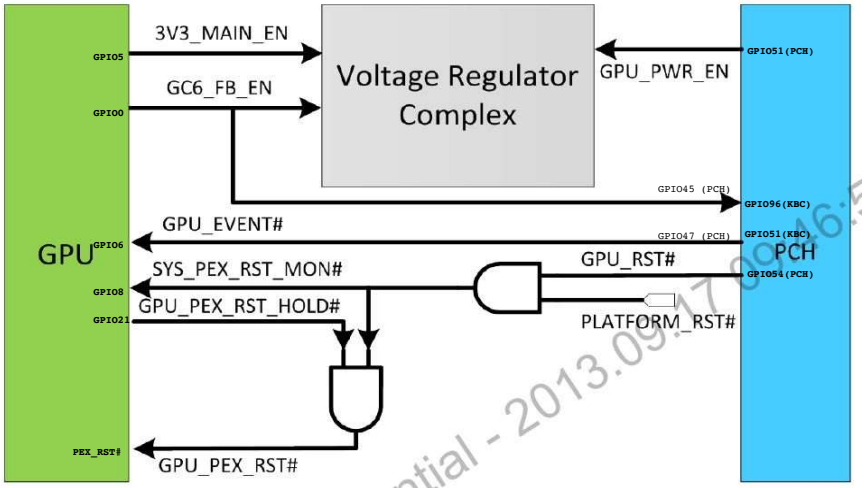

Figure 18-11. GC6 2.0 High-level Signal Connection Concept

N15V-GM-S-A2: 071.0N15V.0A0U
N15V-GM-S is GF117.
N15S-GT is GM108.

<Core Design>			
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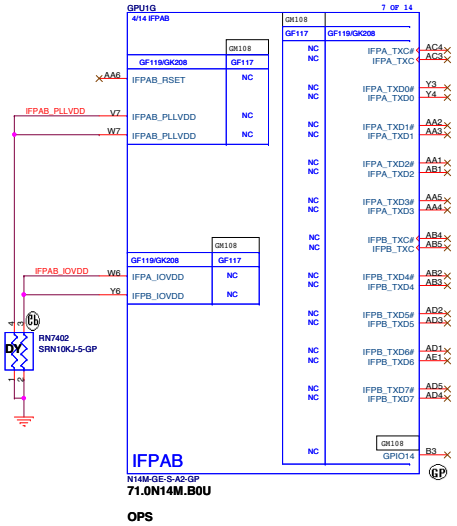
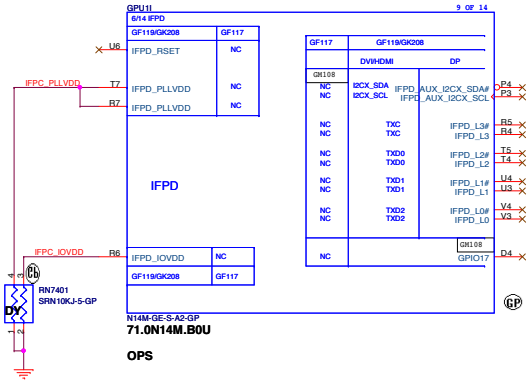
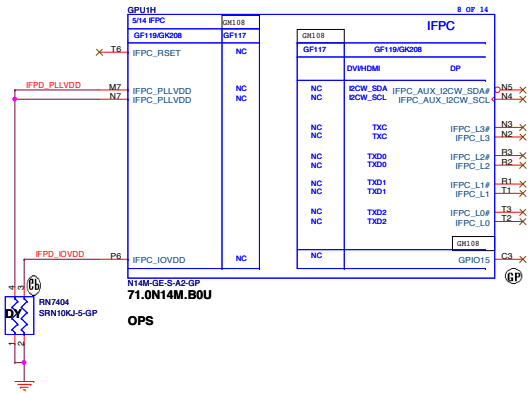
Title: GPU_PCIE/STRAPPING(1/5)			
Size: A2	Document Number: Janus HSW 40/50/70		Rev: A00
Date: Friday, February 07, 2014	Sheet 73 of 104		

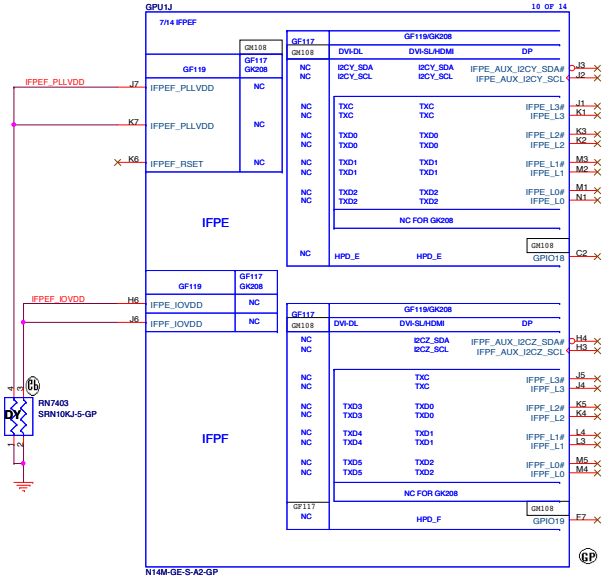
LVDS Interface





HDMI Interface





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Title: GPU Memory(2/5)

Size: A2 | Document Number: Janus HSW 40/50/70 | Rev: A00

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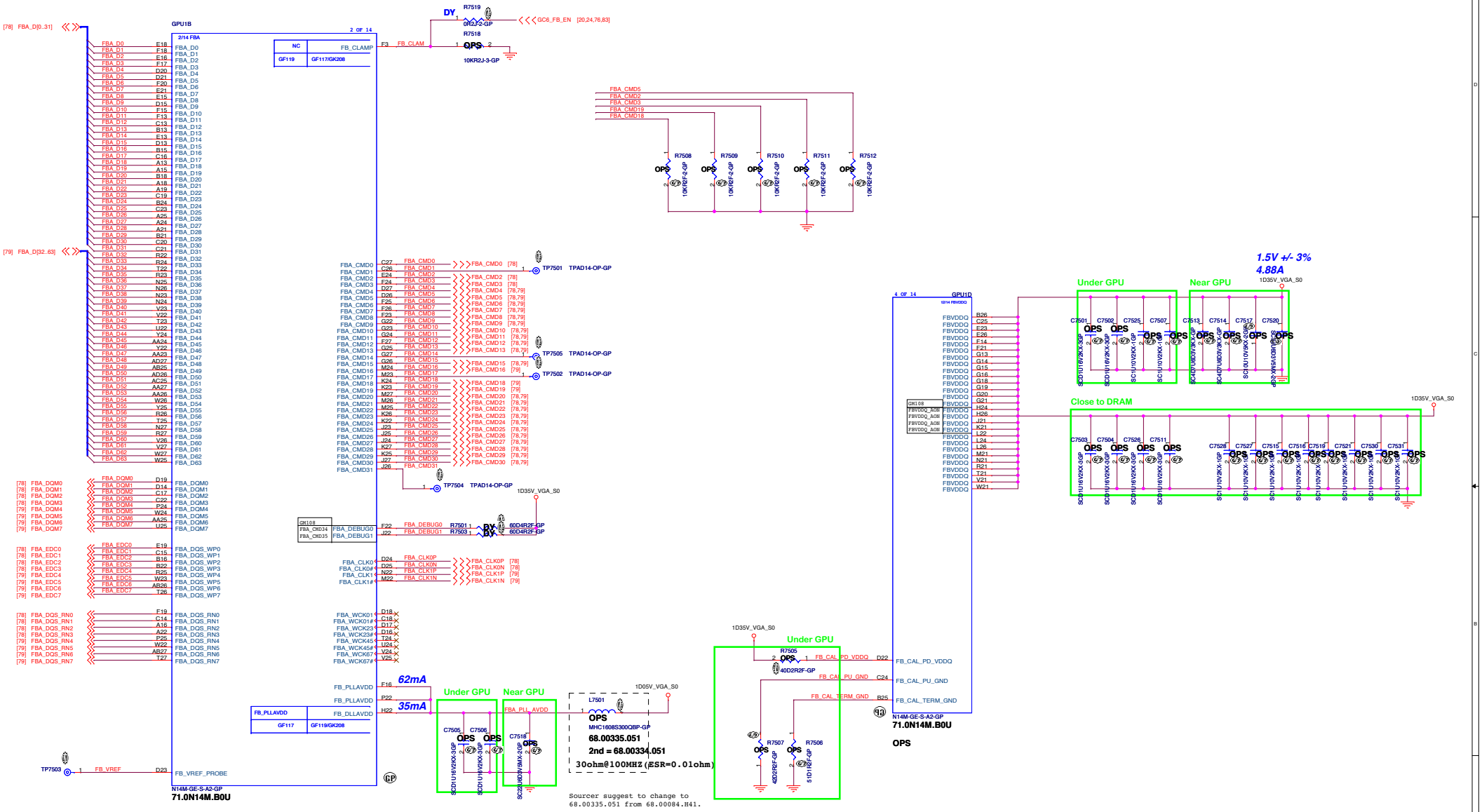

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Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A2 | Document Number: Janus HSW 40/50/70 | Rev: A00

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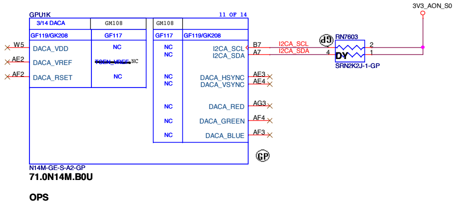
Straps



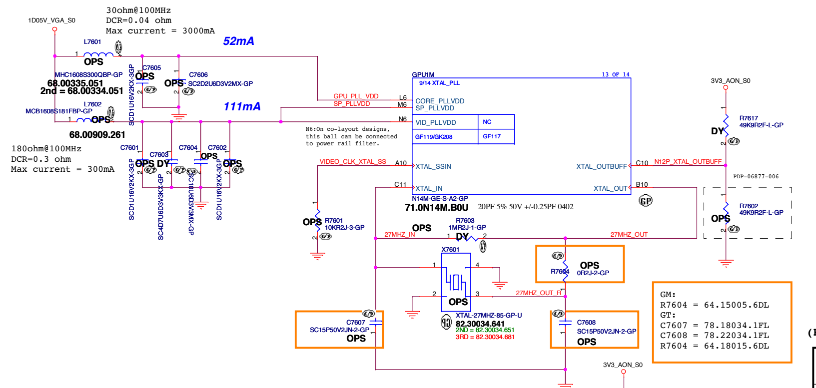
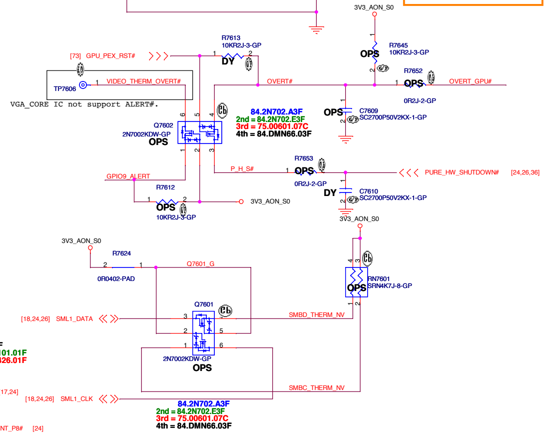


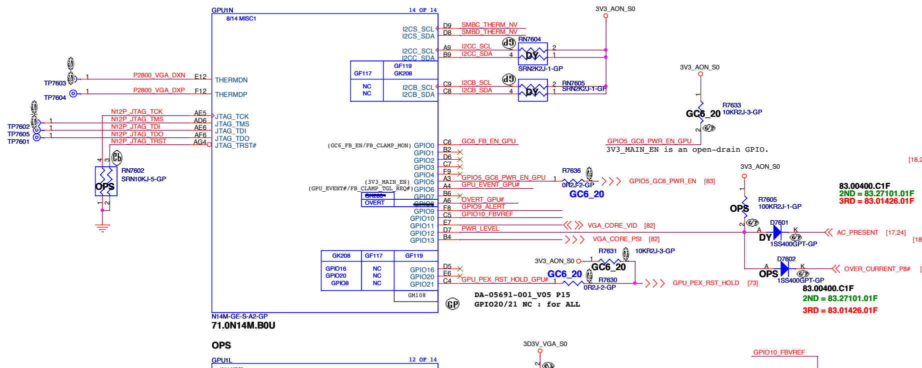
Table 3-32. GB2B-64 and GB4B-128 PLLVDD Filtering

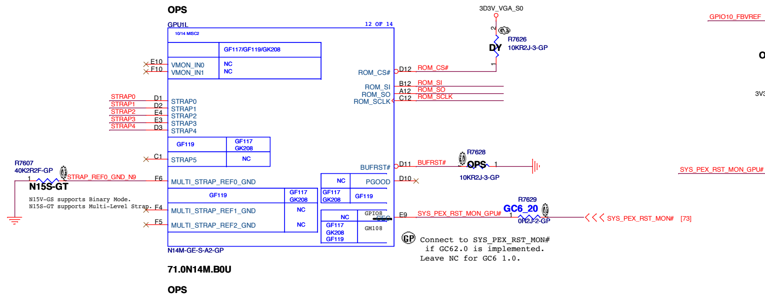
GPU Package	PLL Rail	Capacitor Type		Footprint	Population	Location
GB2B-64 and GB4B-128	PLLVDD	0.1 µF	X7R	0402	1	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.05)		0402	1	Near GPU

Table 3-33. SP_PLLVDD and VID_PLLVDD Power Rail Filtering Combined

GPU Package	PLL Rails	Capacitor Type		Footprint	Population	Location
GB2B-64 GB4B-128 GB3-256	SP_PLLVDD + VID_PLLVDD	0.1 µF	X7R	0402	1 per ball	Under GPU
		4.7 µF	X5R	0603	1	Near GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		180 Ω (ESR=0.2)		0603	1	Near GPU







(DS-06814-001)

Table 9. N15V-GM Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10kΩ	Pull-down to GND
ROM_SI	SUB_VENDOR	10kΩ	•Pull-up to 3V3 if VBIOS ROM exists •Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10kΩ	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10kΩ	See note below
STRAP1	RAM_CFG[1]	10kΩ	See note below
STRAP2	RAM_CFG[2]	10kΩ	See note below
STRAP3	RAM_CFG[3]	10kΩ	See note below
STRAP4	PCIE_MAX_SPEED	10kΩ	Pull-down to GND

(RVL-06891-001)N15V- GM -S DDR3L Recommended Memories

		Strap		STRAP3	STRAP2	STRAP1	STRAP0
128Mx16 DDR3L	Hynix	0xC	H5TC2G63FFR-11C	1	1	0	0
	Micron	0x1	MT41K128M16JT-107G:K	0	0	0	1
	Samsung	0x5	K4W2G1646E-BY11	0	1	0	1
256Mx16 DDR3L	Hynix	0x4	H5TC4G63AFR-11C	0	1	0	0
	Micron	0xD	MT41K256M16HA-107G:E	1	1	0	1
	Samsung	0x9	K4W4G1646D-BC1A	1	0	0	1

(DS-06814-001)

Table 10. Multi-Level Strap Differences

Physical Strapping Pin	GPU	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	N15S-GV	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
	N15S-GM/-GT	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	All GB2-64 N14 and GB2B-64 N15	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	N15S-GV	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
	N15S-GM/-GT	DEVID_SEL	PCIE_CFG		
STRAP0	N15S-GV	USER[3]	USER[2]	USER[1]	USER[0]
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and stuff 50kΩ pull-up)			
STRAP1	N15S-GV	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP2	N15S-GV	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP3	N15S-GV	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP4	N15S-GV	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			

(RVL-06891-001)N15V- GT -S DDR3L Recommended Memories

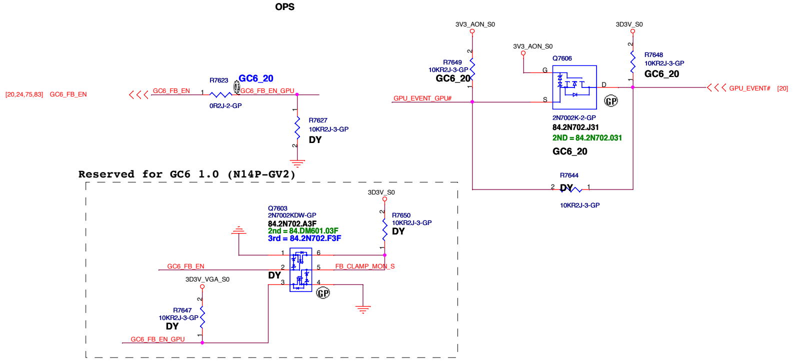
		Strap	
128Mx16 DDR3L	Hynix	0x9	H5TC2G63FFR-11C
	Micron	0xA	MT41K128M16JT-107G:K
	Samsung	0xB	K4W2G1646E-BY11
256Mx16 DDR3L	Hynix	0x3	H5TC4G63AFR-11C
	Micron	0x4	MT41K256M16HA-107G:E
	Samsung	0x5	K4W4G1646D-BC1A

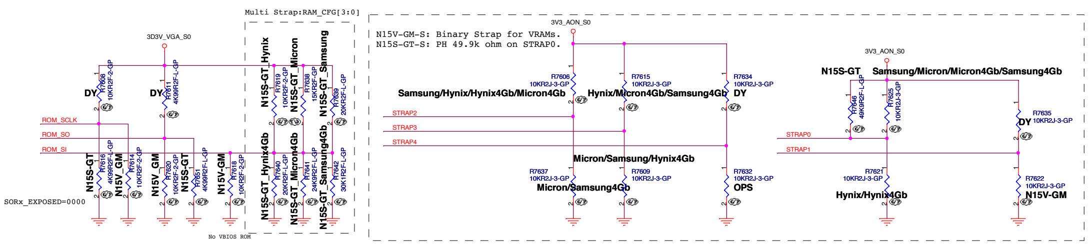
Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

NPN-06912 NPN-06975

	N15V-GM	N15S-GT
Chip	N15V-GM	N15S-GT
Device ID	0x1140	0x1341
Memory interface	sDDR3	SDDR3
Package	595 ball BGA 23x23mm	595 ball BGA 23 × 23 mm 908 ball BGA 29 × 29 mm





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Title: GPU_POWER(4/5)
Size: Custom | Document Number: Janus HSW 40/50/70 | Rev: A00
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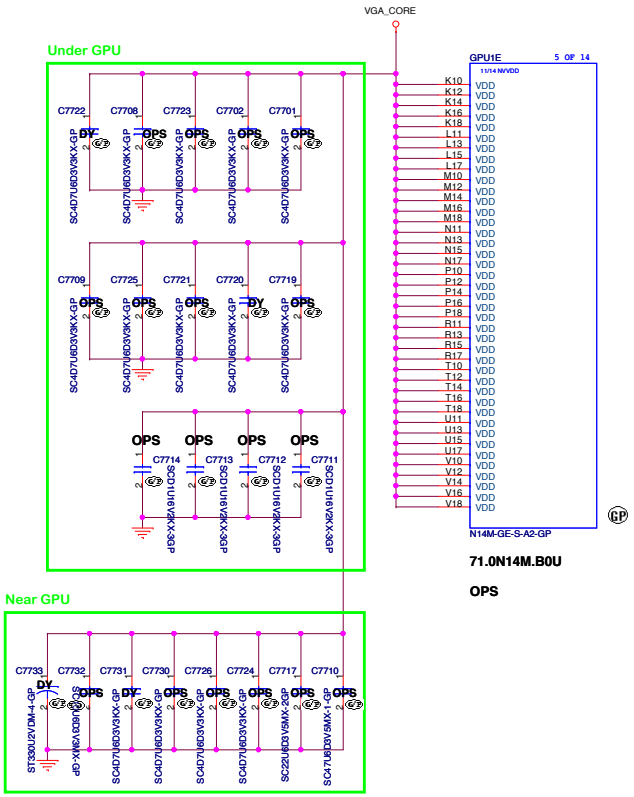
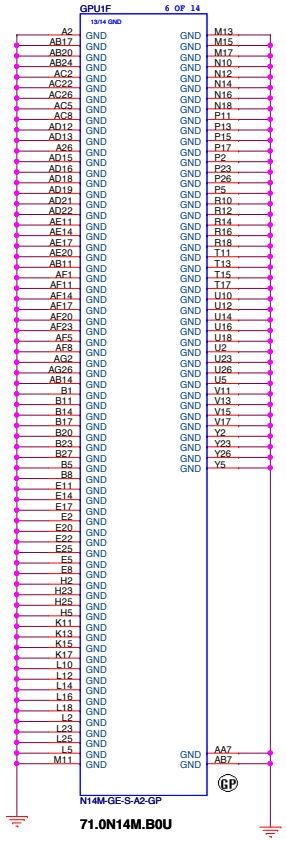
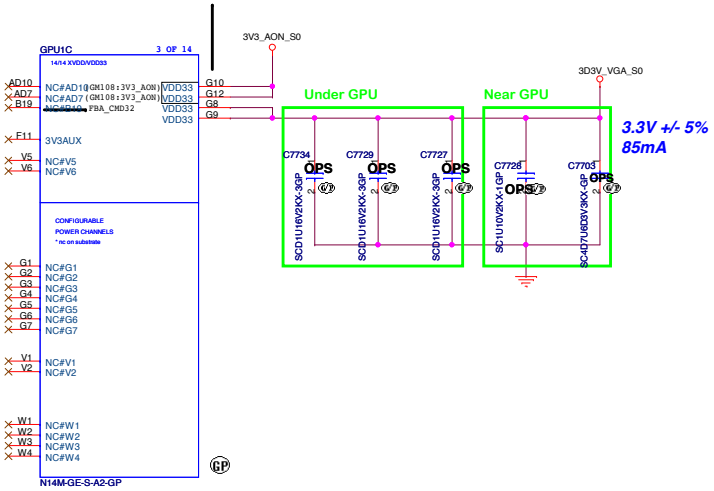




G10,G12:
If GC62.0 is implemented, connect to a 3V3 rail that will be on in GC6.
If GC62.0 is NOT implemented, connect to the same rail as VDD33.



<Core Design>

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Title: GPU_DPPWR/GND(5/5)

Size	Document Number	Rev
Custom	Janus HSW 40/50/70	A00

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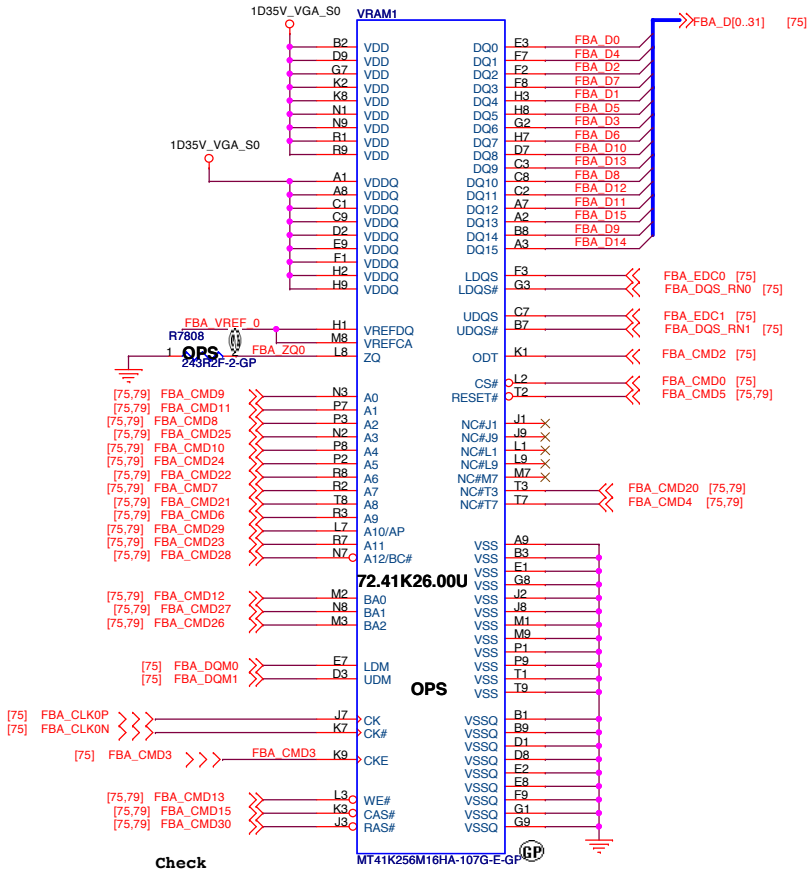
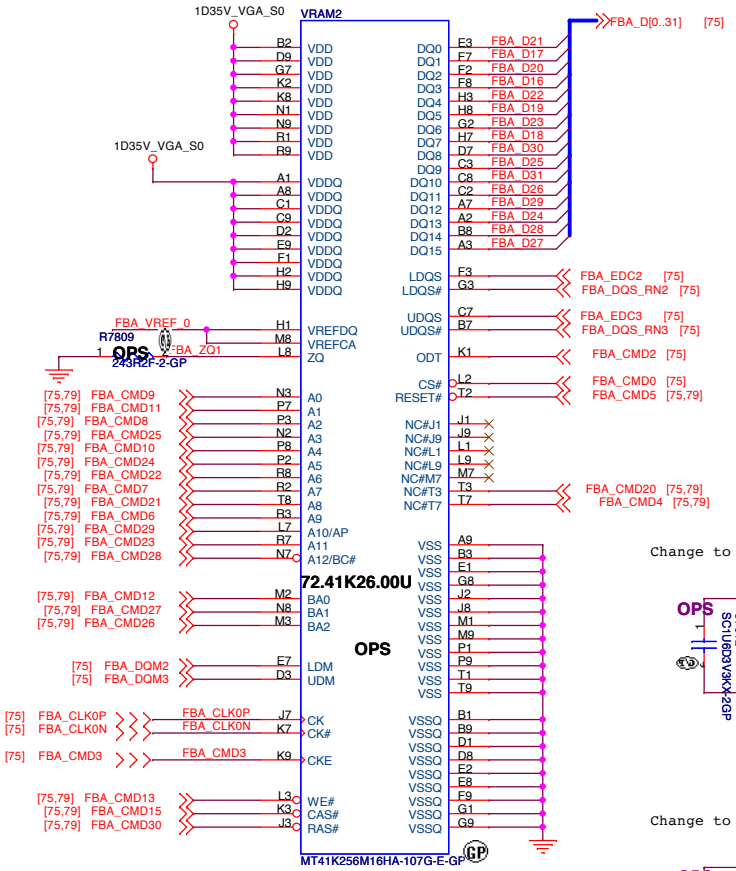
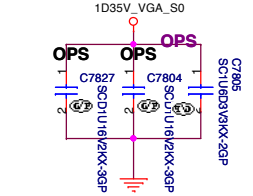
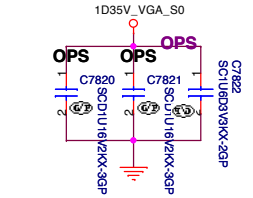




Place close VRAM1 VDD ball

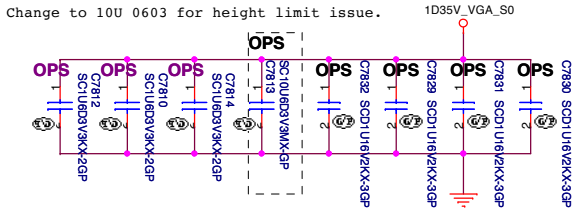


Place close VRAM2 VDD ball



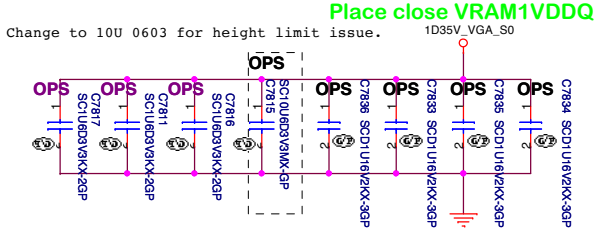
Place close VRAM1VDDQ ball

Change to 10U 0603 for height limit issue.

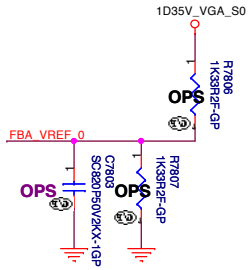


Place close VRAM1VDDQ ball

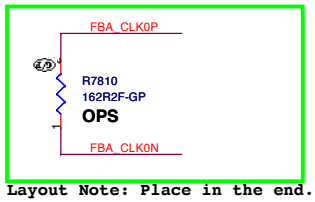
Change to 10U 0603 for height limit issue.



Frame Buffer Patition A-Lower Half



FBCLK Termination place on VRAM side



Layout Note: Place in the end.

FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

20110613

<Core Design>

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Title: GPU-VRAM1,2 (1/4)

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

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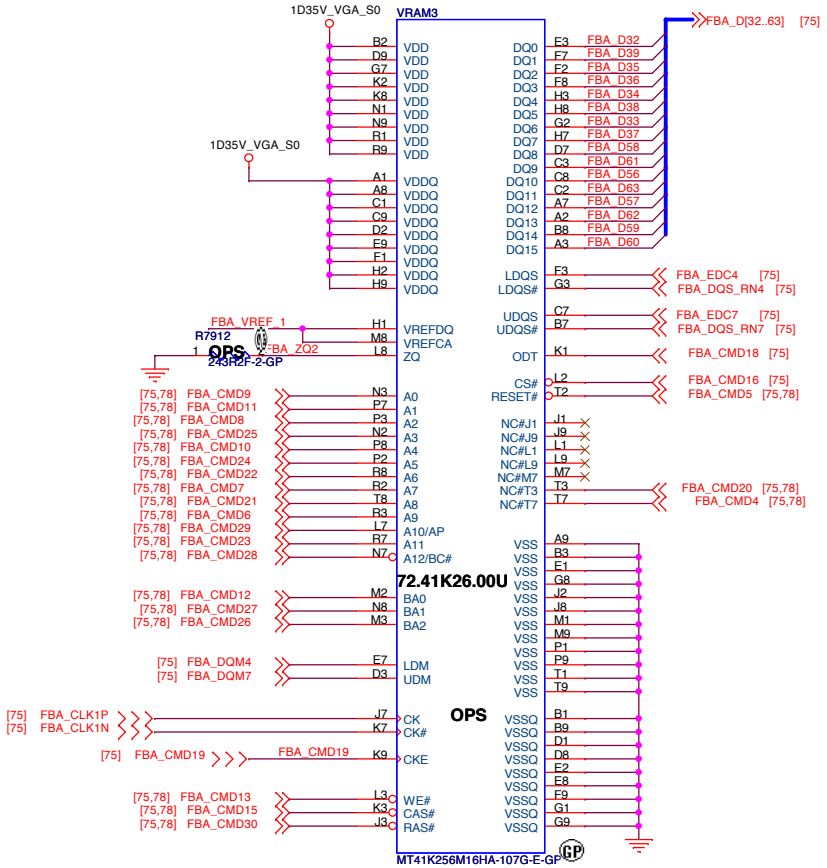
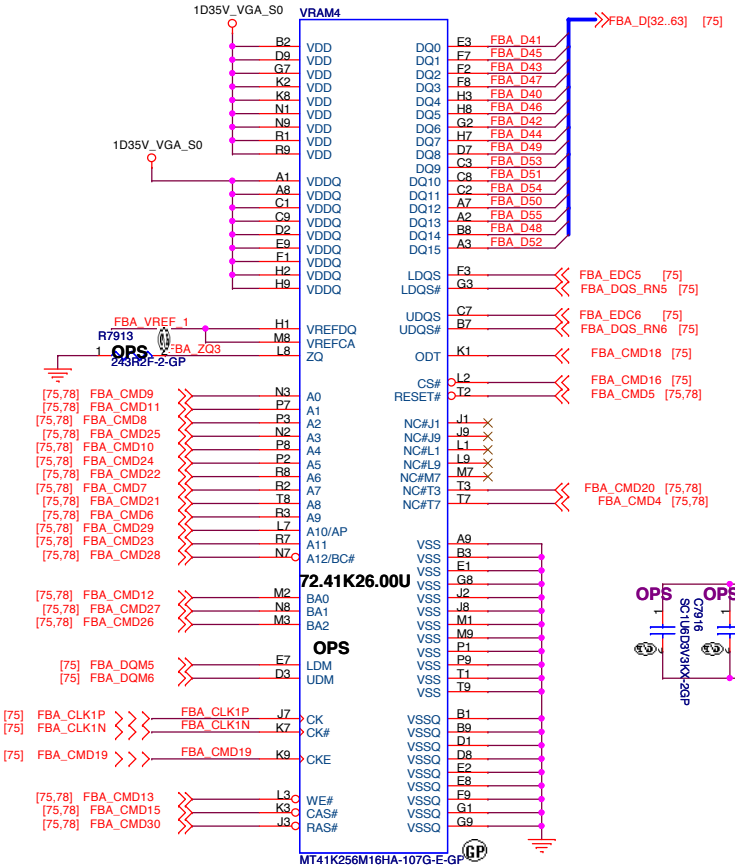
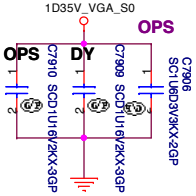
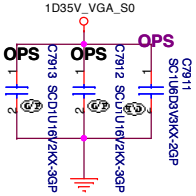




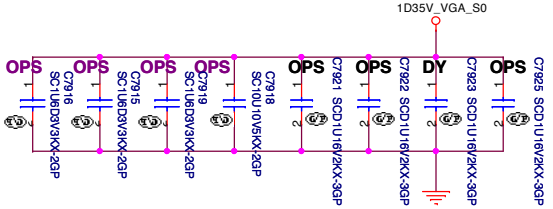
Place close VRAM3 VDD ball



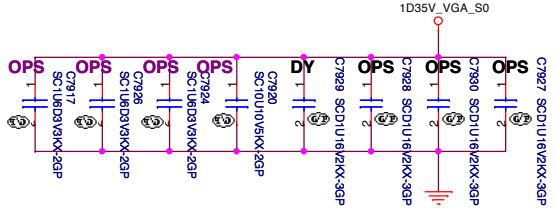
Place close VRAM4 VDD ball



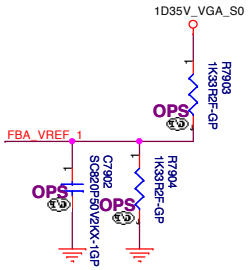
Place close VRAM3 VDDQ ball



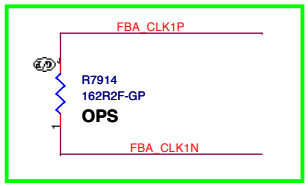
Place close VRAM4 VDDQ ball



Frame Buffer Patition A-Lower Half



FBCLK Termination place on VRAM side



Layout Note: Place in the end.

<Core Design>

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Title	*GPU-VRAM3,4 (2/4)*	
Size A3	Document Number: Janus HSW 40/50/70	Rev: A00
Date: Friday, February 07, 2014	Sheet 79 of 104	

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Title

GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
A3	Janus HSW 40/50/70	A00

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<Core Design>

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Title

GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
A3	Janus HSW 40/50/70	A00

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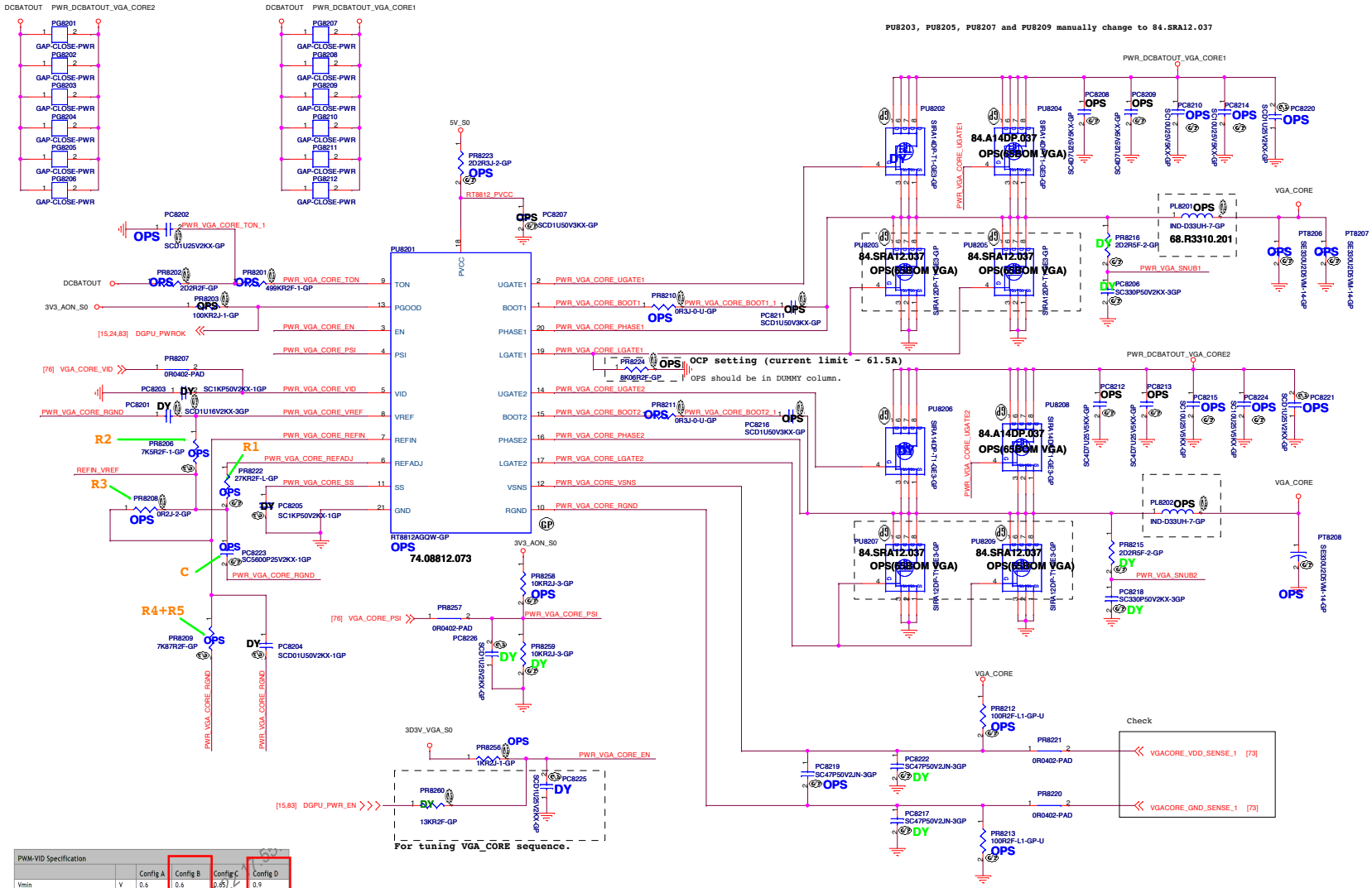

N15V_GM_S
Config D

Design Current=33.5A
56.65A <OCP< 66.7A

Component value	N15V-GM-S Config D	N15-S-GT-S Config B
R1 (PR8222)	27K 64.27025.6DL	20K 64.20025.6DL
R2 (PR8206)	7.5K 64.75015.6DL	20K 64.20025.6DL
R3 (PR8208)	0 63.R0034.1DL	2K 64.20015.6DL
R4+R5 (PR8209)	7.87K 64.78715.6DL	18K 64.18025.6DL
C (PC8223)	5.6nF 78.56222.2FL	2.7nF 78.27224.2FL

PWM-VID Specification					
		Config A	Config B	Config C	Config D
Vmin	V	0.6	0.6	0.65	0.9
Vmax	V	1.2	1.2	1.15	1.15
Vboot	V	0.875	0.9	0.9	1.028
Voltage Step Vstep	mV	6.25	12.5	25	12.5
Number of Voltage Levels N	level	96	96	20	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676	0.676
PWM Minimum Pulse Width T_{DMAX}	ns	9.26	9.26	74	74
VID Transient Time T	us	<100	<100	<100	<100
Component Value					
R1 (1%)	KΩ	39	20	39	27
R2 (1%)	KΩ	39	20	30	7.5
R3 (1%)	KΩ	1.5	2	3	0
R4 (1%)	KΩ	30	18	24	6.2
R5 (1%)	KΩ	1.5	0	3	1.74
C	nF	1.5	2.7	1.8	5.6

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor:CHIP CHOKE 0.22UH PCMC104T-R22/ 1mohm/ Isat =60A rms /68.R2210.10C
O/P cap: CHIP CAP EL 330U 2.5V M6.3*4.4 Chemi-con/79.3371V.6CL
H/S: SIRA14DP-T1-GE3 / 6.8mohm/8.5mOhm@4.5Vgs/ 84.A14DP.037
L/S:SIRA06DP-T1-GE3 / 2.75mohm/3.5mOhm@4.5Vgs/ 84.SRA06.037

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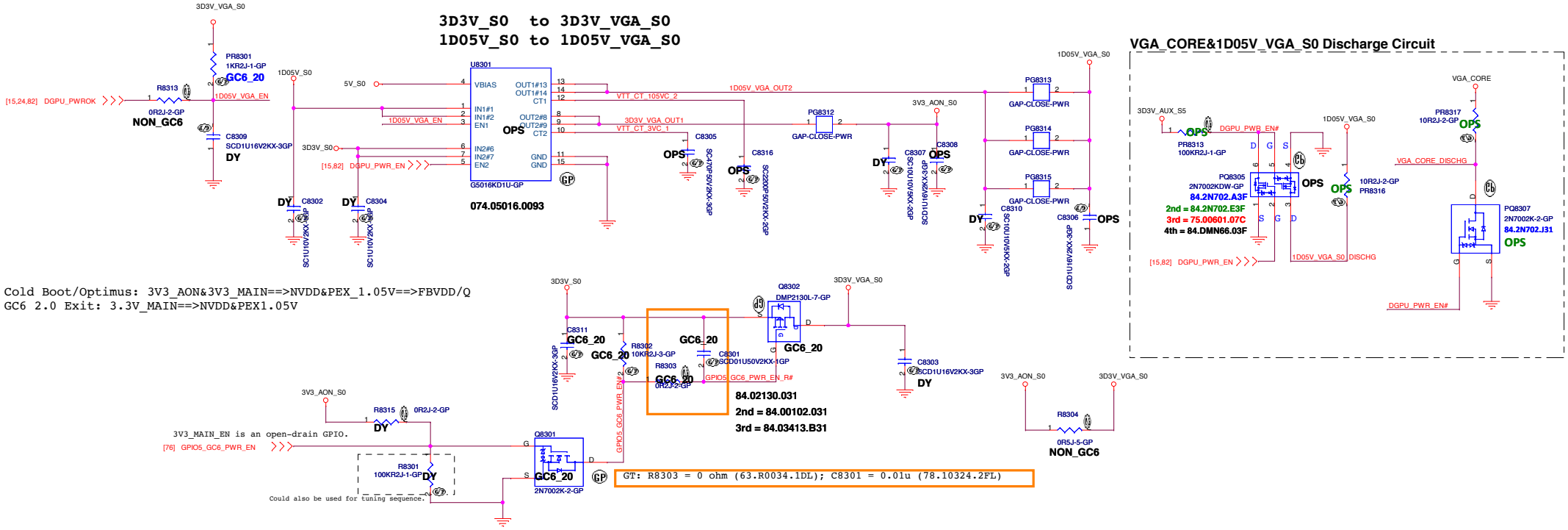
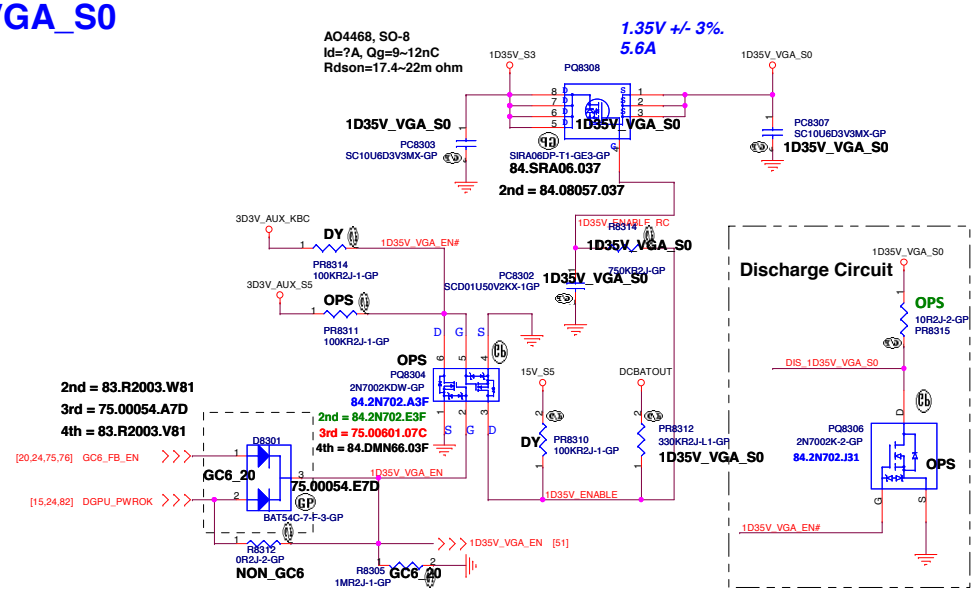
Title: RT8812 VGACORE
Size: A2 | Document Number: Janus HSW 40/50/70 | Rev: A00
Date: Friday, February 07, 2014 | Sheet 82 of 104

3D3V_VGA_S0
1D05V_VGA_S0

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D35V_VGA_S0 should ramp-up before 1D05V_VGA_S0



1D35V_VGA_S0



CTx (pF)	Rise Time (µs) 10% - 90%, COUT = 0.1µF @ VIN; VOUT=0 ohm load Typical values @ 25°C, 25V X7R 10% ceramic cap							
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	1V	0.8V
0	107	72	46	41	36	34	33	29
220	425	276	146	122	103	91	88	74
270	489	316	172	139	121	107	104	84
470	774	487	272	224	181	159	154	123
680	1108	708	375	317	242	221	213	168
1000	1561	1007	546	441	364	314	299	234
2200	3600	2289	1240	1019	817	681	665	539
4700	7757	5092	2674	2203	1808	1592	1516	1177
10000	15700	10310	5601	4659	3674	3401	3197	2562

Table 1. Rise time vs. CTx value

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Title: DISCRETE VGA POWER
Size: Custom | Document Number: Janus HSW 40/50/70 | Rev: A00
Date: Monday, February 10, 2014 | Sheet 83 of 104

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<Core Design>

Wistron Corporation
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Title: *Reserved*

Size: A3 | Document Number: *Janus HSW 40/50/70* | Rev: *A00*

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<Core Design>

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Title: *Reserved*

Size	Document Number	Rev
A3	*Janus HSW 40/50/70*	*A00*

SSID = Mechanical

S1
STF237R117H83-1-GP
34.4CK01.001
2nd = 34.4CK01.601
3rd = 34.4CK01.501

S2
STF237R117H83-1-GP
34.4CK01.001
2nd = 34.4CK01.601
3rd = 34.4CK01.501

H2
HOLE335R115-GP
ZZ.00PAD.D01

H5
HT85BE85R29-U-5-GP
ZZ.00PAD.D41

H6
HT85BE85R29-U-5-GP
ZZ.00PAD.D41

H1
HOLE335R115-GP
ZZ.00PAD.D01

H3
HOLE335R115-GP
ZZ.00PAD.D01

H4
HOLE256R115-GP
ZZ.00PAD.D11

SPR2
SPRING-102-GP
34.41V01.001

SPR3
SPRING-102-GP
34.41V01.001

SPR5
SPRING-63-GP
34.4Y806.001

SPR4
SPRING-43-GP-U
34.15J03.001

C1
HOLE197R166-1-GP
ZZ.00PAD.V71

C2
HOLE197R166-1-GP
ZZ.00PAD.V71

C3
HOLE197R166-1-GP
ZZ.00PAD.V71

SSID = EMI

Mind the voltage rating of the caps.

DCBATOUT

EC9701 EC9702 EC9703 EC9704 EC9708 EC9705 EC9706 EC9707 EC9709 EC9710
EC9717 EC9711 EC9712 EC9713 EC9716 EC9715 EC9714

5V_S0

EC9720 EC9719 EC9718 EC9723 EC9721 EC9722 EC9724

1D35V_VGA_S0

EC9727 EC9725 EC9726 EC9730 EC9728 EC9729 EC9731

AUD_AGND

EC9739 EC9744 EC9743 EC9745

DCBATOUT

EC9740 EC9741 EC9742 EC9747 EC9748 EC9749

3D3V_S0

EC9737 EC9735 EC9736 EC9738

5V_S5

EC9734 EC9732 EC9733

<Core Design>

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Title: UNUSED PARTS/EMI Capacitors
Size: A3
Document Number: Janus HSW 40/50/70
Rev: A00
Date: Friday, February 07, 2014
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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Janus HSW 40/50/70* | Rev: *A00*

Date: Friday, February 07, 2014 | Sheet 87 of 104

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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Janus HSW 40/50/70* | Rev: *A00*

Date: Friday, February 07, 2014 | Sheet 88 of 104

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<Core Design>

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Title: *(Reserved)Finger Print*

Size	Document Number	Rev
A4	*Janus HSW 40/50/70*	*A00*

Date: Friday, February 07, 2014 Sheet 89 of 104

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Free Fall Sensor*

Size	Document Number	Rev
A3	*Janus HSW 40/50/70*	*A00*

Date: Friday, February 07, 2014 Sheet 90 of 104

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<Core Design>

Wistron Corporation
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Title: *Reserved*

Size	Document Number	Rev
A3	*Janus HSW 40/50/70*	*A00*

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<Core Design>

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Title: Express Card

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 93 of 104

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LVDS_Switch*

Size	Document Number	Rev
A3	Janus HSW 40/50/70	A00

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CRT_Switch*

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

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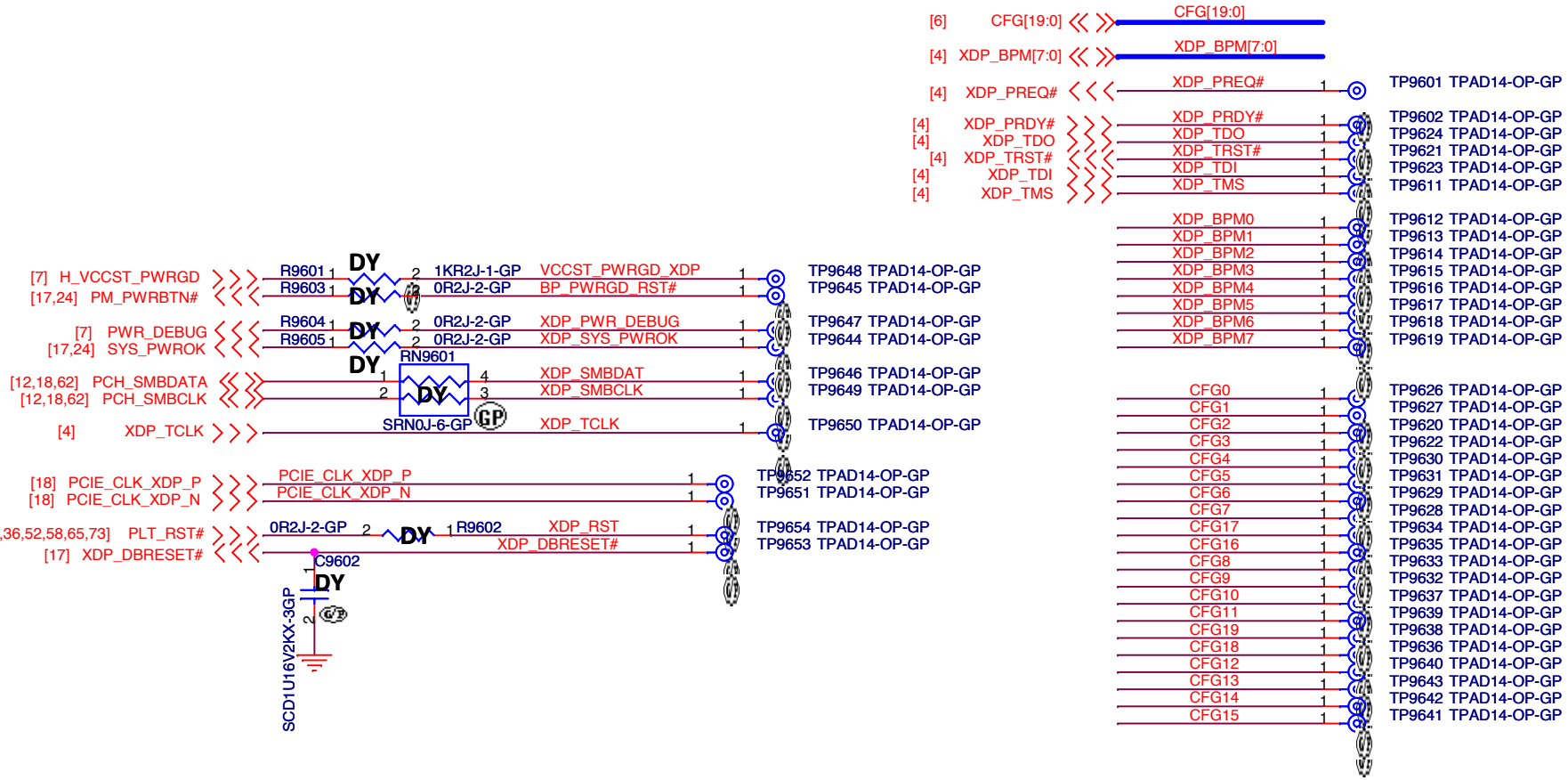
SSID = XDP

CPU XDP



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU/PCH XDP*

Size	Document Number	Rev
A4	Janus HSW 40/50/70	A00

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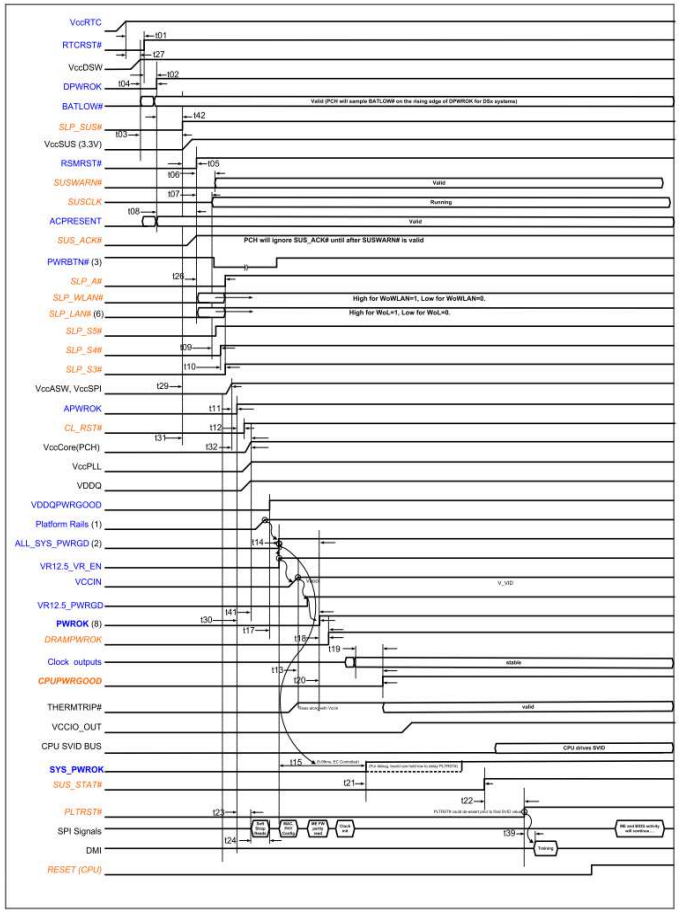
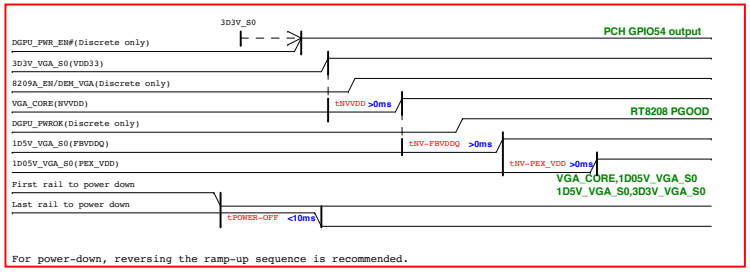
Shark Bay Platform Power Sequence

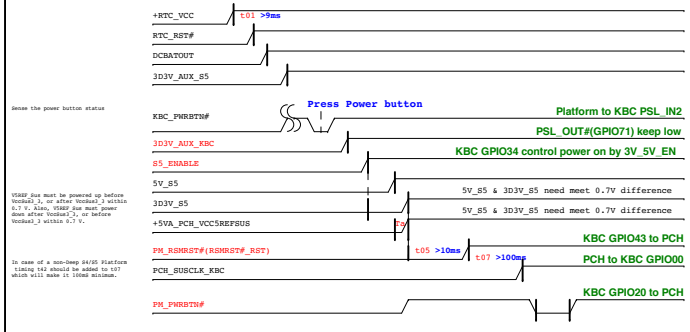


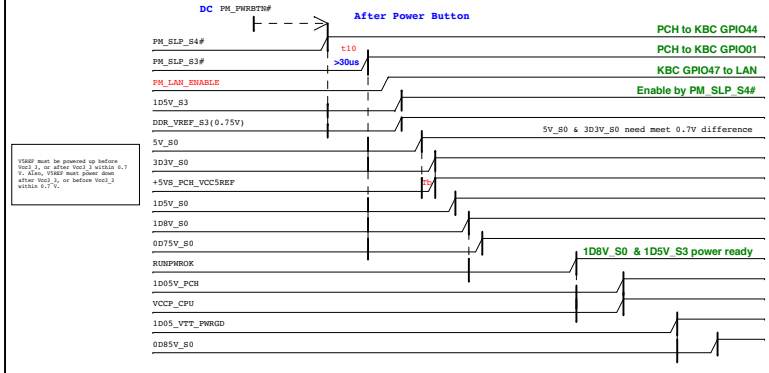
N14P-GT Power-Up/Down Sequence

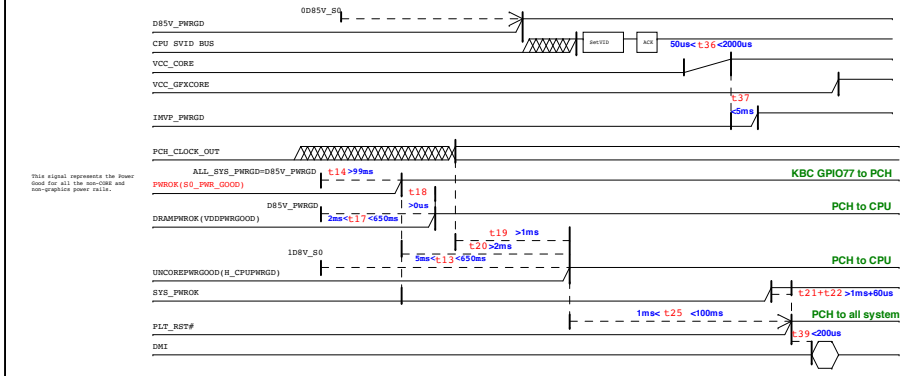


(DC mode)

Red Words: Controlled by EC GPIO







<Core Design>

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Title: Power Sequence

Size	Document Number	Rev
A1	Janus HSW 40/50/70	A00

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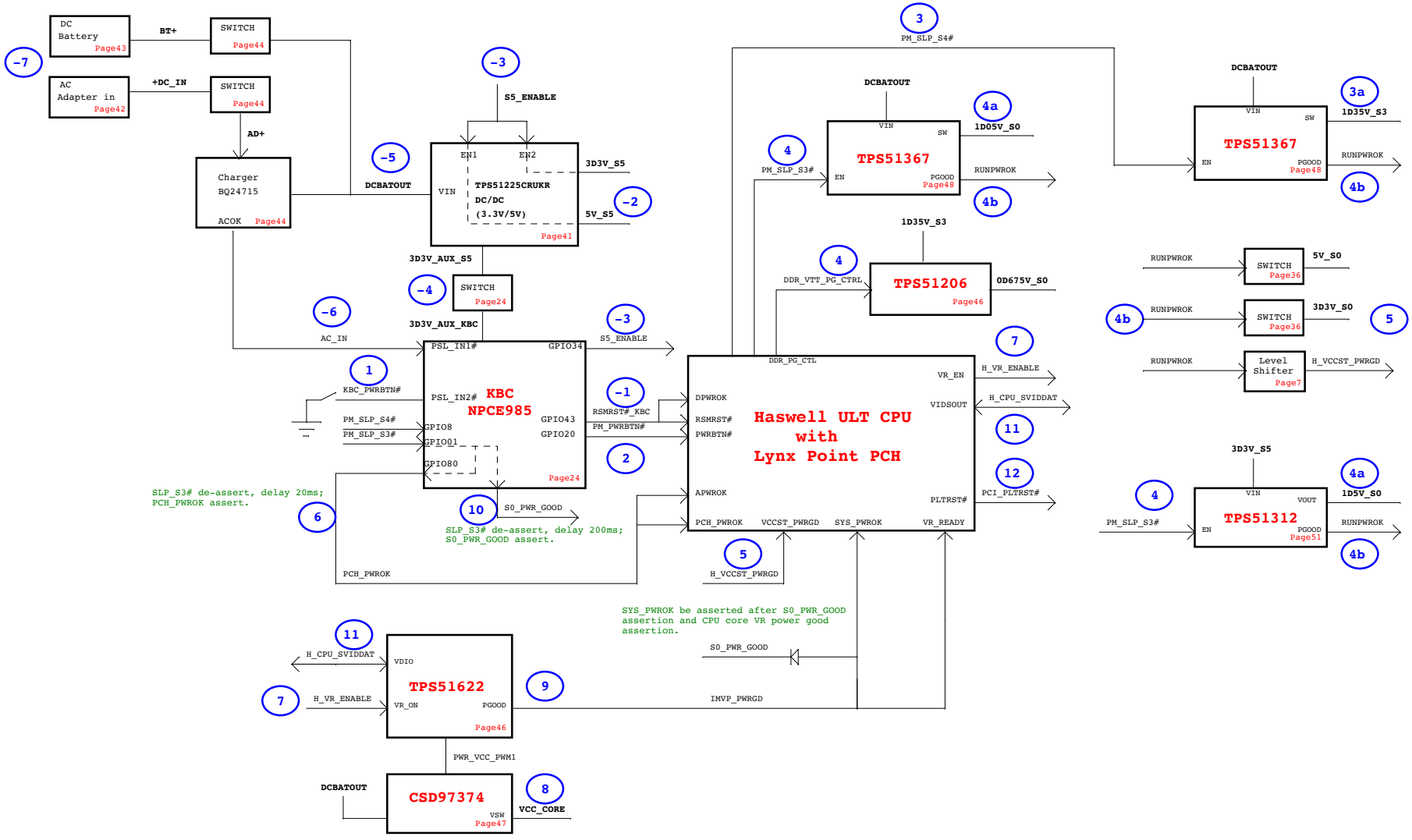
Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



1 → 2 → 3a → 4 → 4a → 4b → 5 → 6 → 7 → 8 → 9 → 10 → 11 → 12

<Core Design>

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Title: Power Sequence Diagram

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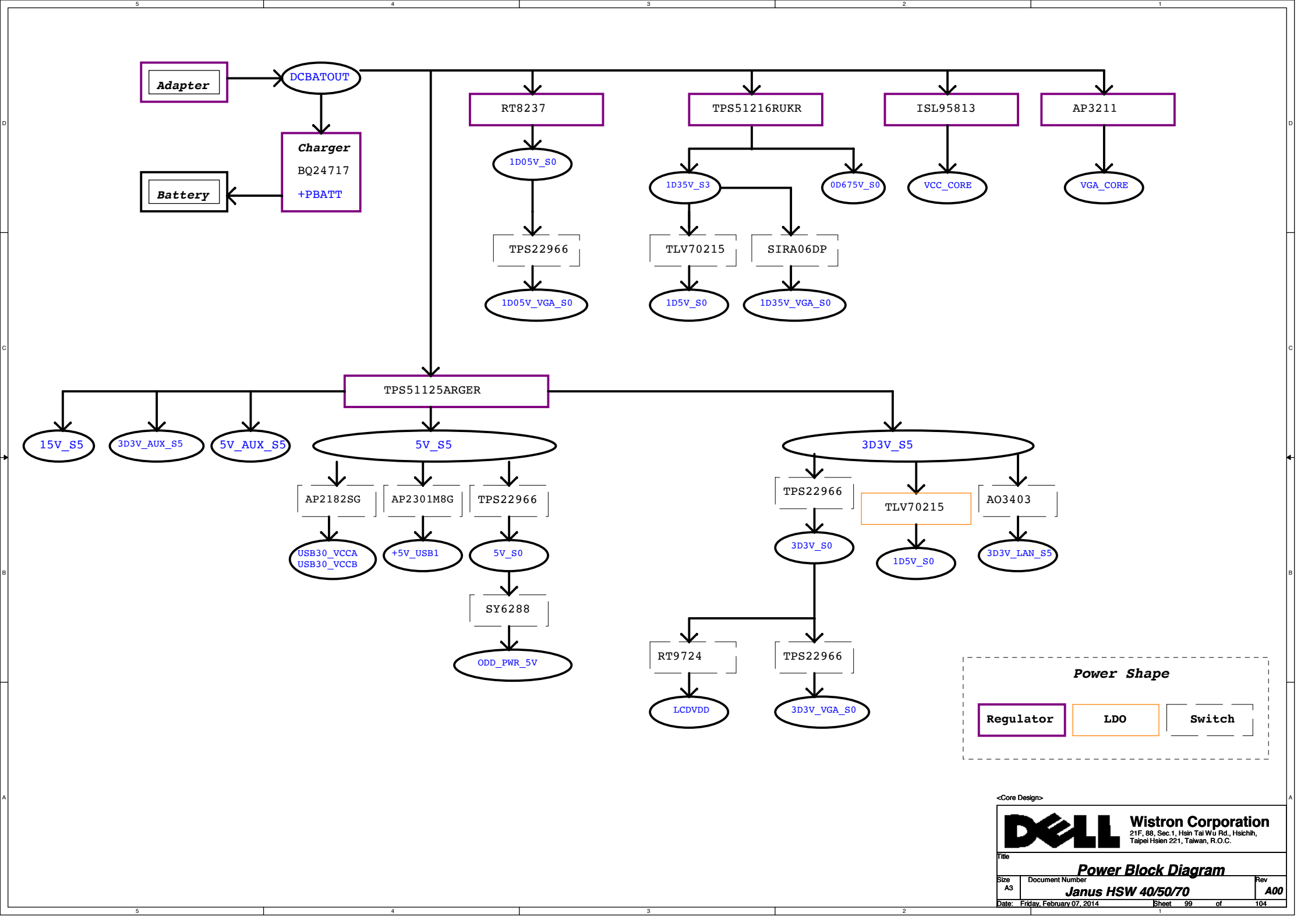

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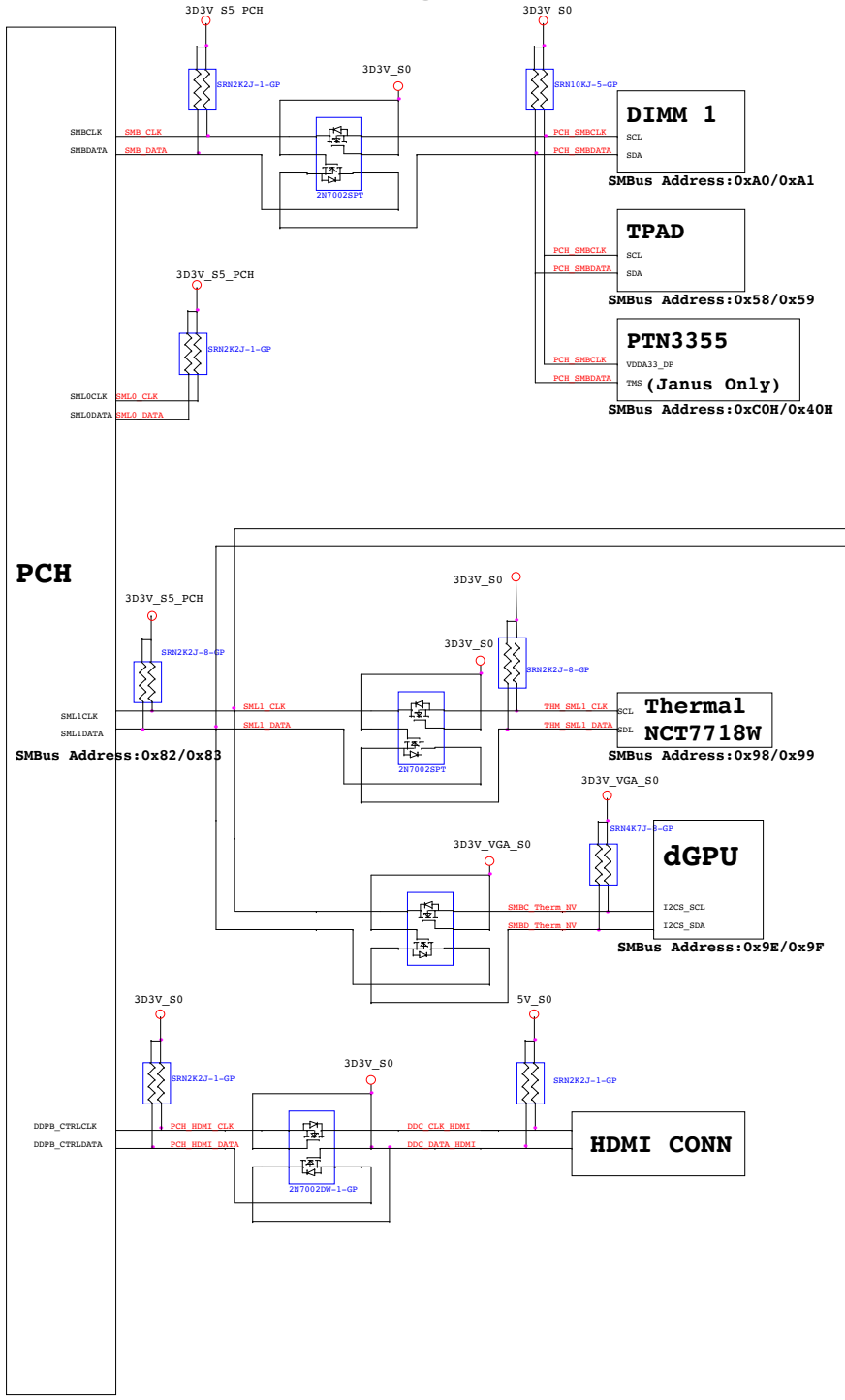
PCH SMBus Block Diagram



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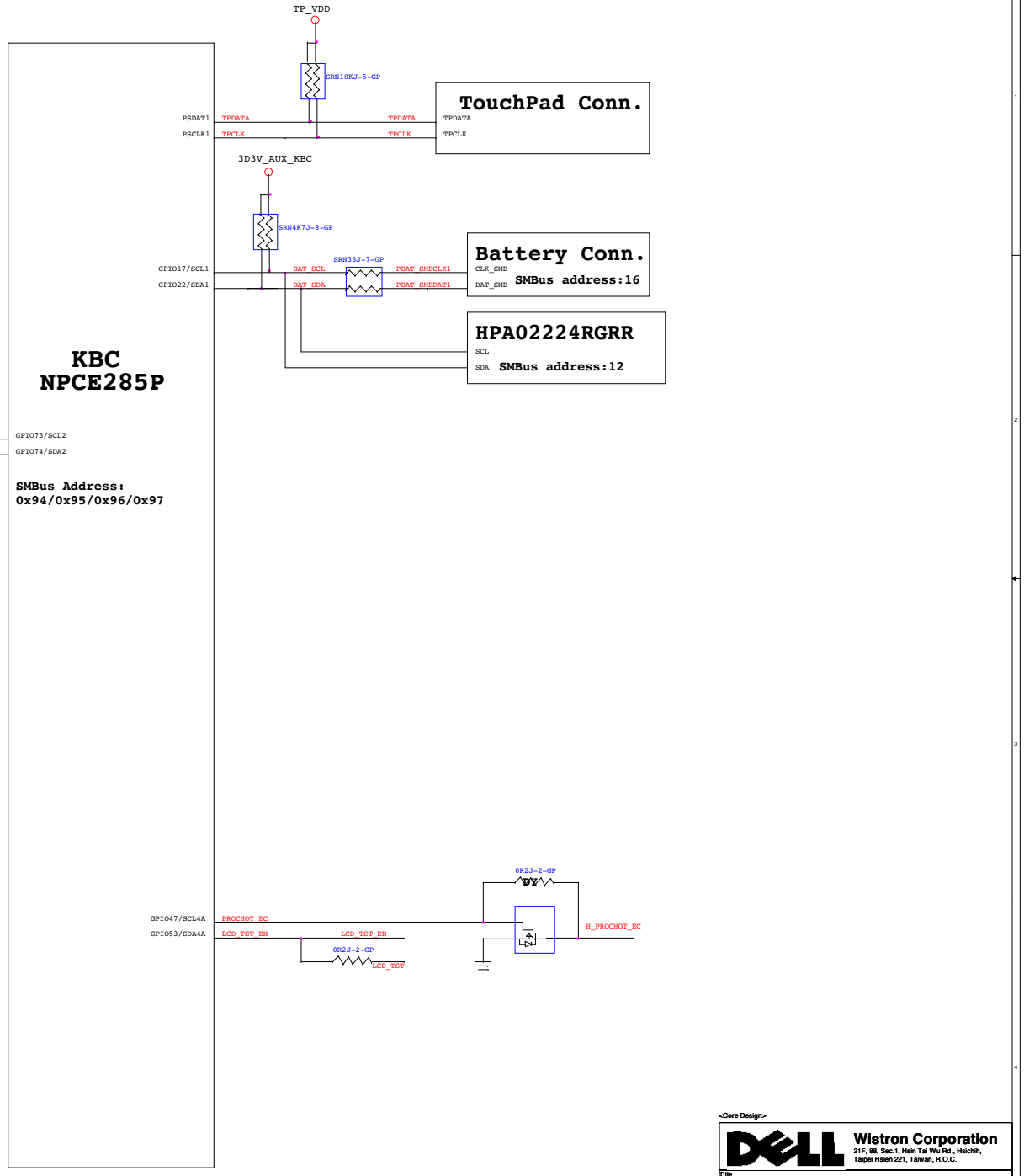

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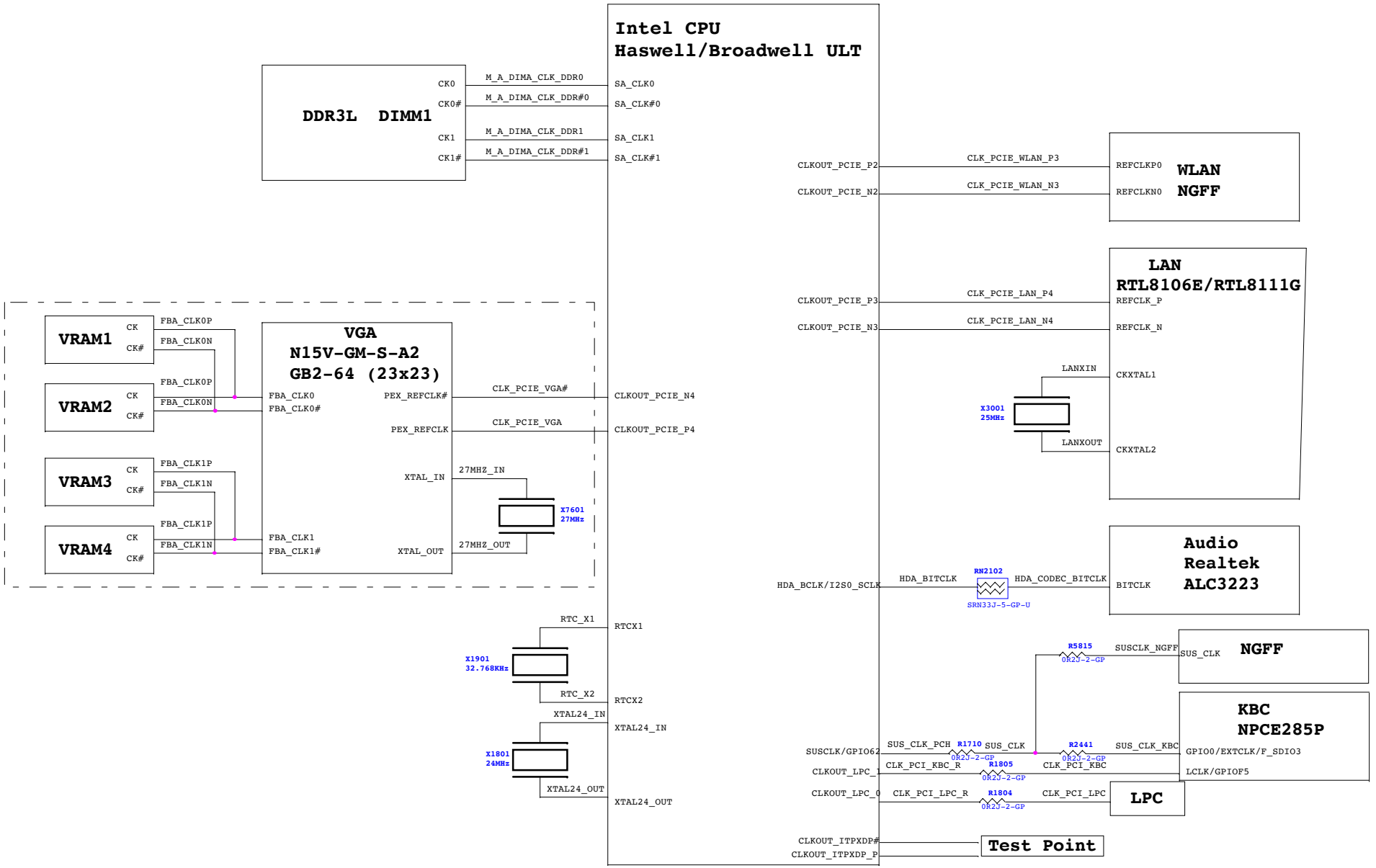
CLK Block Diagram



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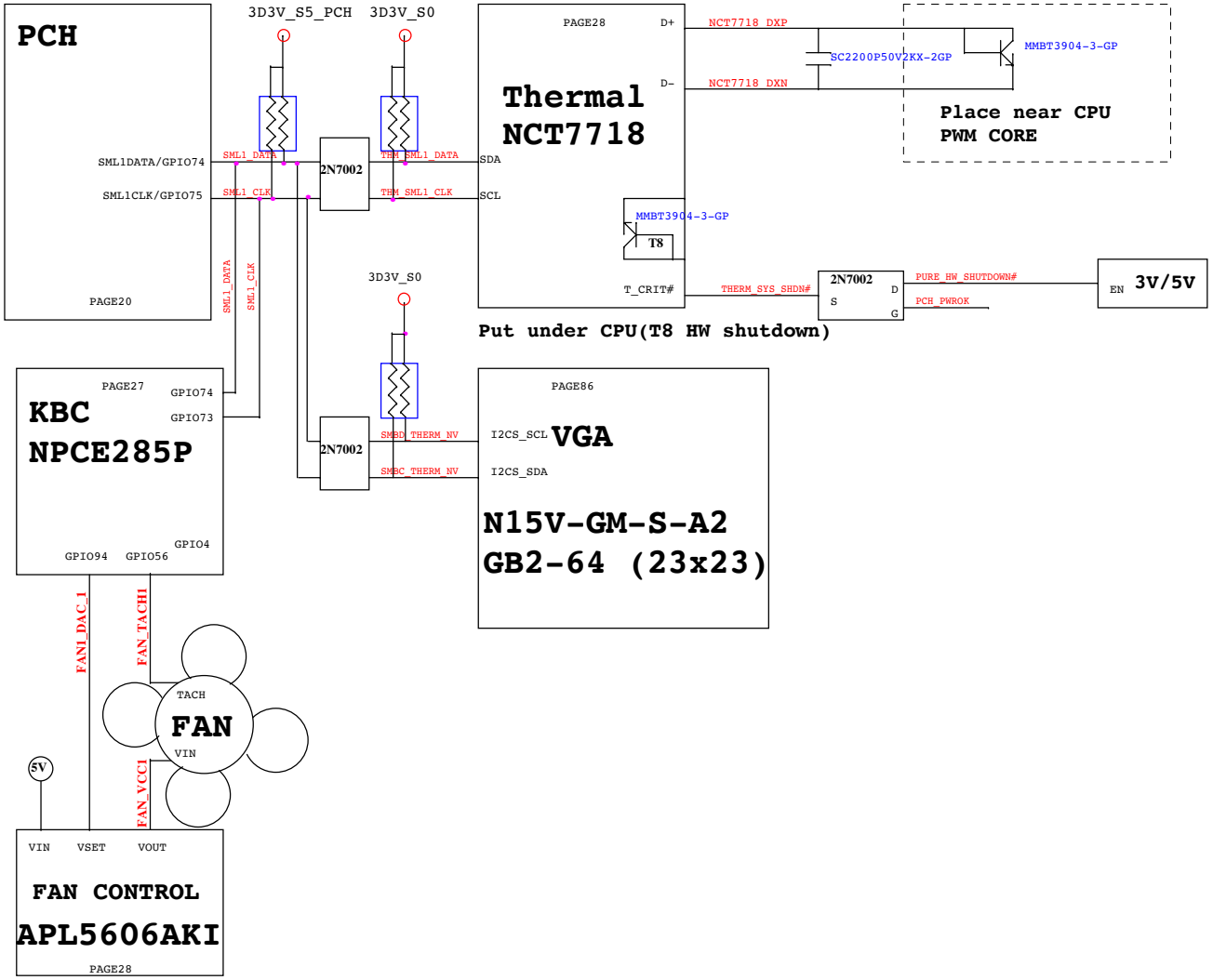
Thermal Block Diagram



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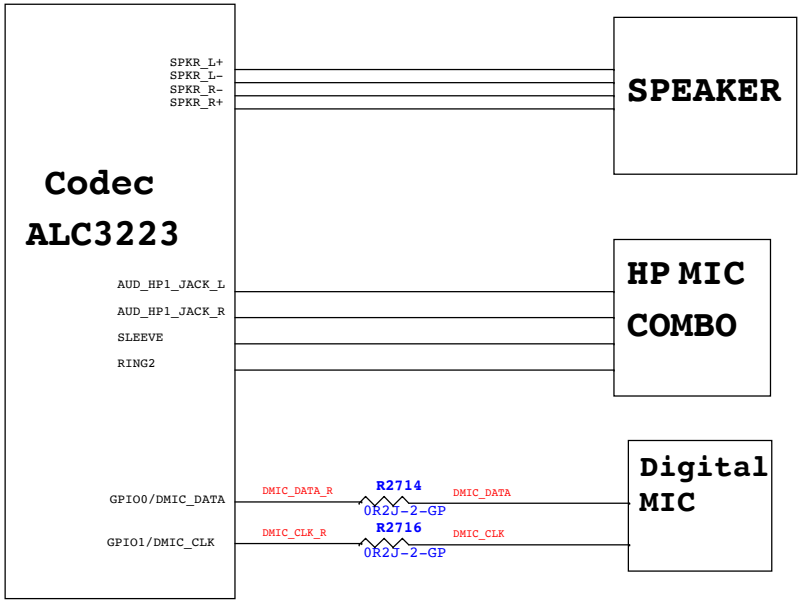

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