

POWER





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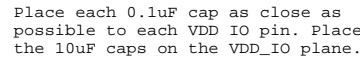
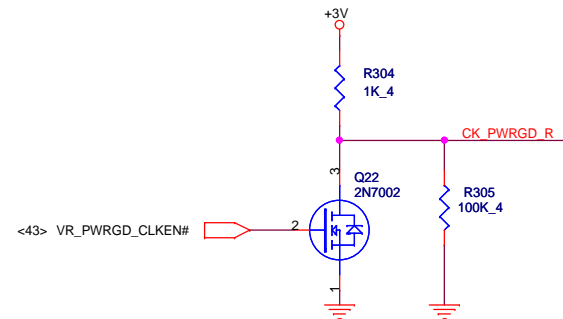
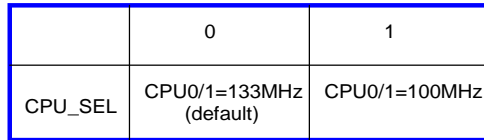
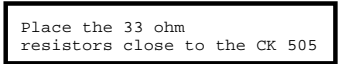
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Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER		S0~S5
+RTC_CELL	+3V~+3.3V	RTC		S0~S5
+3VPCU	+3.3V	8051 POWER	3V5V_EN	S0~S5
+5VPCU	+5V	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
+15V	+15V	LARGE POWER	3V5V_EN	S0~S5
VCC3_LAN	+3.3V	LAN POWER	LAN_ON	
+5VSUS	+5V	SLP_S4# CTRLD POWER	SUSON	
+3VSUS	+3.3V	SLP_S4# CTRLD POWER	SUSON	
+1.5VSUS	+1.5V	SODIMM POWER	SUSON	
+0.75V_DDR_VTT	+0.9V	SODIMM POWER	MAIN_ON	
+5V	+5V	SLP_S3# CTRLD POWER	MAIN_ON	
+3V	+3.3V	SLP_S3# CTRLD POWER	MAIN_ON	
+1.8V	+1.8V	CPU,PCH POWER	MAIN_ON	
+1.5V	+1.5V	PCH POWER	MAIN_ON	
+1.05V_VTT	+1.05V~+1.1V	CPU POWER	MAIN_ON	
+1.05V_PCH	+1.05V	PCH POWER	1.05V_RUN_ON	
VCC_CORE	0V~+1.5V	CPU CORE POWER	VRON	
LCDVCC	+3.3V	LCD Power	ENVDD	
BAT-V	+10V~+17V	MAIN BATTERY		
+5V_S5	+5V	PCH SUS POWER	S5_ON	
+3V_S5	+3.3V	Sys Management,PCH Resume Well	S5_ON	

GND PLANE	PAGE	DESCRIPTION
 LANGND	26	
 IT8512_AGND	36	
 ADOGND	27	
 GND	ALL	

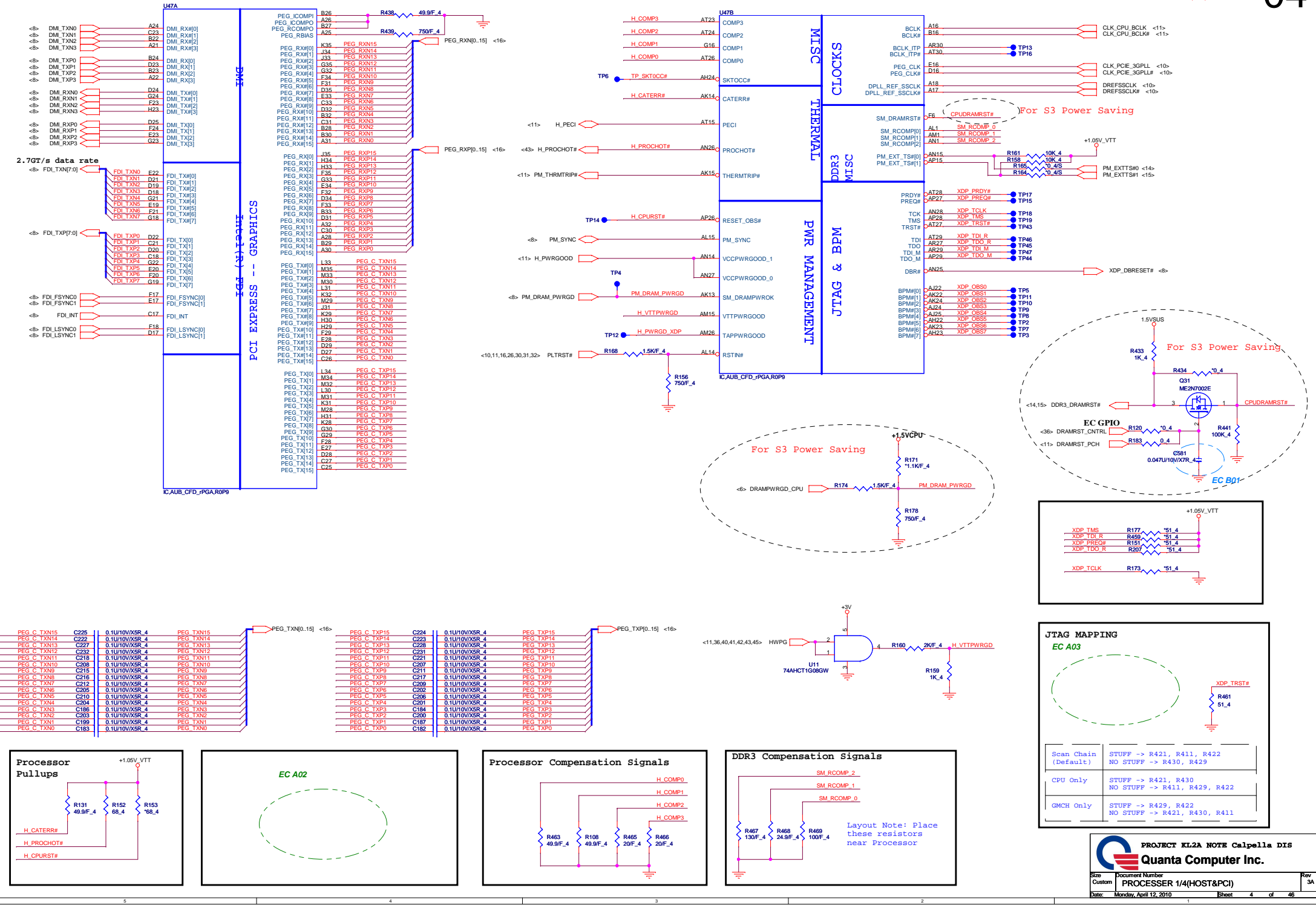
02



AUBURNDALE PROCESSOR (DMI,PEG,FDI)

<3,8,9,10,11,12,14,15,23,24,25,26,27,28,29,30,31,32,33,34,35,36,38,39,43,44> +3V
<3,6,8,9,10,11,12,38,41,43,45> +1.05V_VTT
<14,15,38,40,44> 1.5VSUS

04



AUBURNDALE PROCESSOR (DDR3)

05

U47C

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SA_DQ[1] C10
SA_DQ[2] C7
SA_DQ[3] A7
SA_DQ[4] B10
SA_DQ[5] D10
SA_DQ[6] E10
SA_DQ[7] A8
SA_DQ[8] D8
SA_DQ[9] F10
SA_DQ[10] E6
SA_DQ[11] F7
SA_DQ[12] E9
SA_DQ[13] B7
SA_DQ[14] E7
SA_DQ[15] C6
SA_DQ[16] H10
SA_DQ[17] G8
SA_DQ[18] K7
SA_DQ[19] J8
SA_DQ[20] G7
SA_DQ[21] G10
SA_DQ[22] J7
SA_DQ[23] J10
SA_DQ[24] L7
SA_DQ[25] M6
SA_DQ[26] M8
SA_DQ[27] L9
SA_DQ[28] L6
SA_DQ[29] K8
SA_DQ[30] N8
SA_DQ[31] P9
SA_DQ[32] AH5
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SA_DQ[60] AL13
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SA_DQ[63] AP14

DDR SYSTEM MEMORY A

IC:AUB_CFD_rPGA,R0P9

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SA_CKE[0] P7 M_A_CKE0 <14>

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SA_MA[7] T1 M_A_A7 <14>
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SA_MA[12] U3 M_A_A12 <14>
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<14> M_A_RAS# AB3 SA_RAS#
<14> M_A_WE# AE9 SA_WE#

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<15> M_B_BS#2 R7 SB_BS[2]

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<15> M_B_RAS# Y7 SB_RAS#
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U47D

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M_B_DQ[2] C3 SB_DQ[2]
M_B_DQ[3] B3 SB_DQ[3]
M_B_DQ[4] E4 SB_DQ[4]
M_B_DQ[5] A6 SB_DQ[5]
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M_B_DQ[8] D1 SB_DQ[8]
M_B_DQ[9] D2 SB_DQ[9]
M_B_DQ[10] F2 SB_DQ[10]
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M_B_DQ[16] H6 SB_DQ[16]
M_B_DQ[17] G2 SB_DQ[17]
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M_B_DQ[21] G5 SB_DQ[21]
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M_B_DQ[23] J1 SB_DQ[23]
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M_B_DQ[29] K4 SB_DQ[29]
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M_B_DQ[31] N5 SB_DQ[31]
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M_B_DQ[33] AG1 SB_DQ[33]
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M_B_DQ[58] AP8 SB_DQ[58]
M_B_DQ[59] AT7 SB_DQ[59]
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DDR SYSTEM MEMORY - B

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SB_CKE[0] M3 M_B_CKE0 <15>

SB_CK[1] V7 M_B_CLK1 <15>
SB_CK#1 V6 M_B_CLK1# <15>
SB_CKE[1] M2 M_B_CKE1 <15>

SB_CS#0 AB8 M_B_CS#0 <15>
SB_CS#1 AD6 M_B_CS#1 <15>

SB_ODT[0] AC7 M_B_ODT0 <15>
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SB_MA[12] R3 M_B_A12 <15>
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SB_MA[14] P5 M_B_A14 <15>
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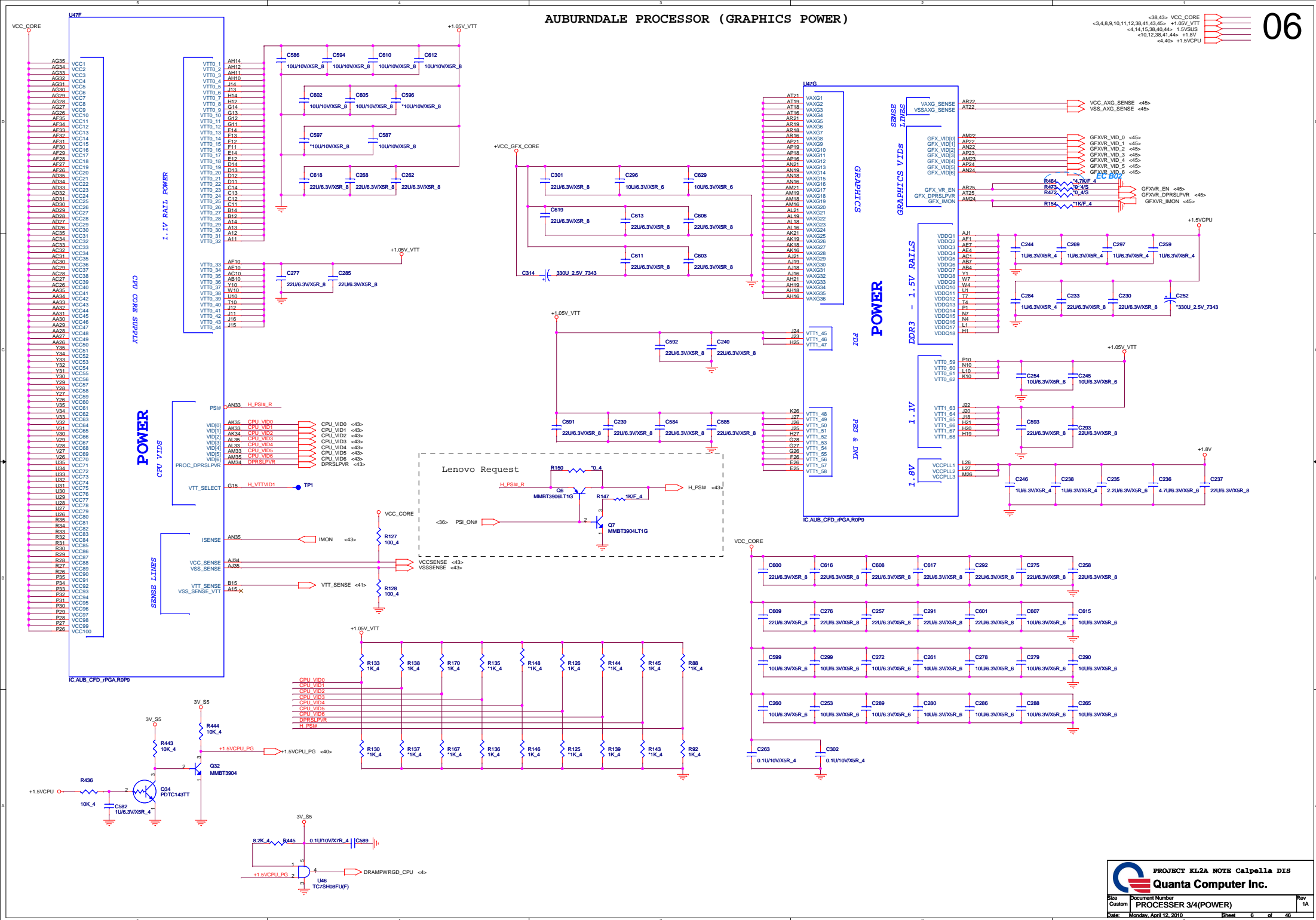
PROJECT KL2A NOTE Calpella DIS

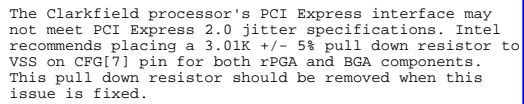
Quantia Computer Inc.


AUBURNDALE PROCESSOR (GRAPHICS POWER)

<38,43> VCC_CORE
 <3,4,8,9,10,11,12,36,41,43,45> +1.05V_VTT
 <4,14,15,36,40,44> +1.5V_CPU
 <10,12,38,41,44> +1.8V
 <4,40> +1.5V_CPU

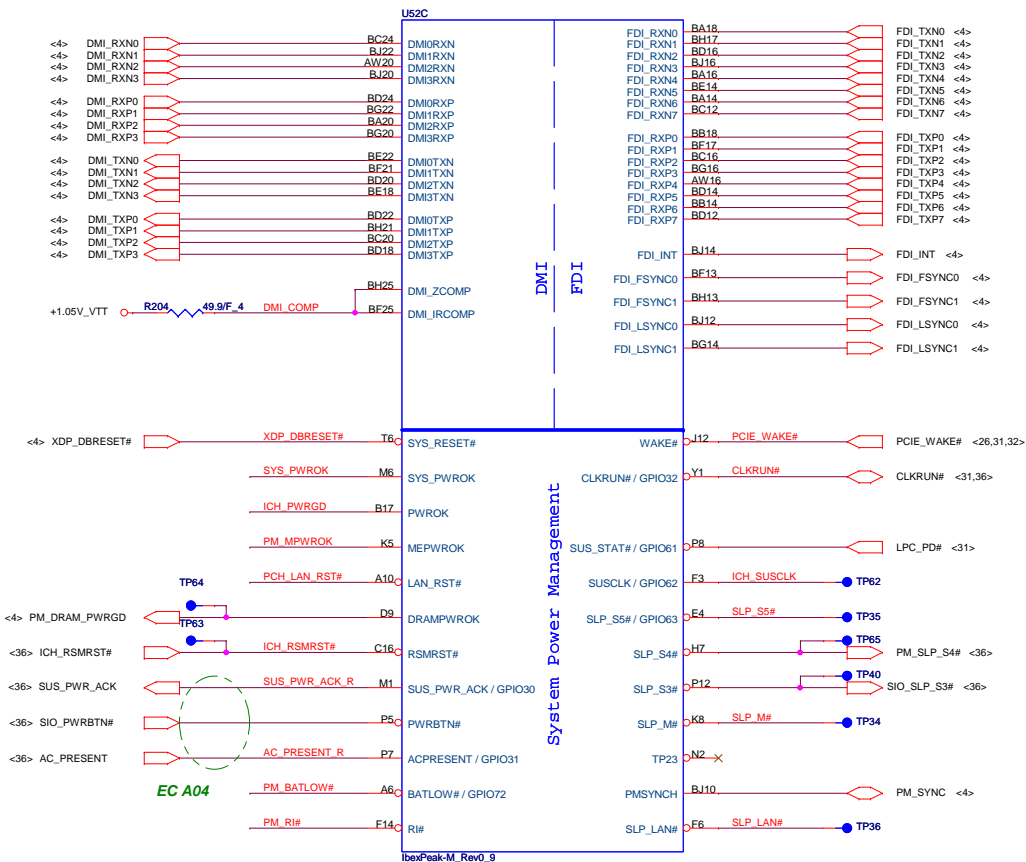
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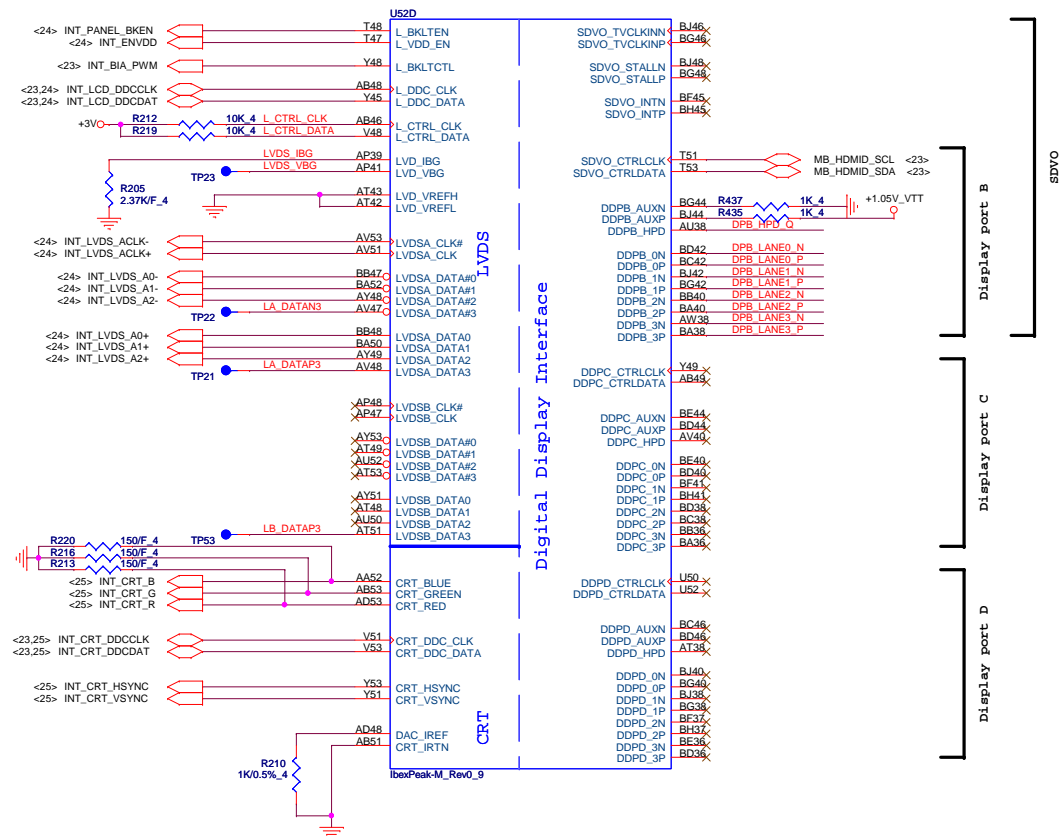


	PROJECT KL2A NOTE Calpella DIS	
	Quanta Computer Inc.	
Size Custom	Document Number PROCESSOR 4/4(GND)	Rev 1A
Date: Monday, April 12, 2010	Sheet 7 of 46	

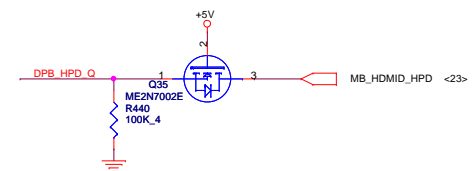
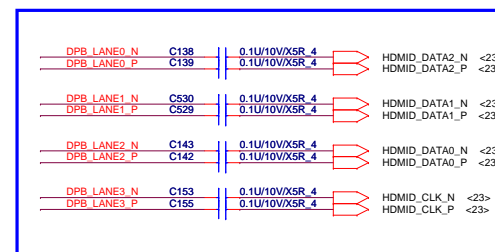
IBEX PEAK-M (DMI, FDI, GPIO)



IBEX PEAK-M (LVDS, DDI)



For UMA HDMI Function



RTC Circuitry

CMOS Settings	J5
Clear CMOS	1-2
Save CMOS	1-X (Default)

TPM Settings	J4
Clear ME RTC registers	1-2
Save ME RTC registers	1-X (Default)

IBEX PEAK-M (HDA,JTAG,SATA)

INVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

<27> ICH_AZ_CODEC_BITCLK

EC B25

<27> ICH_AZ_CODEC_SYNC

<27> ICH_AZ_CODEC_RST#

<27> ICH_AZ_CODEC_SDOOUT

Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

No Reboot Strap

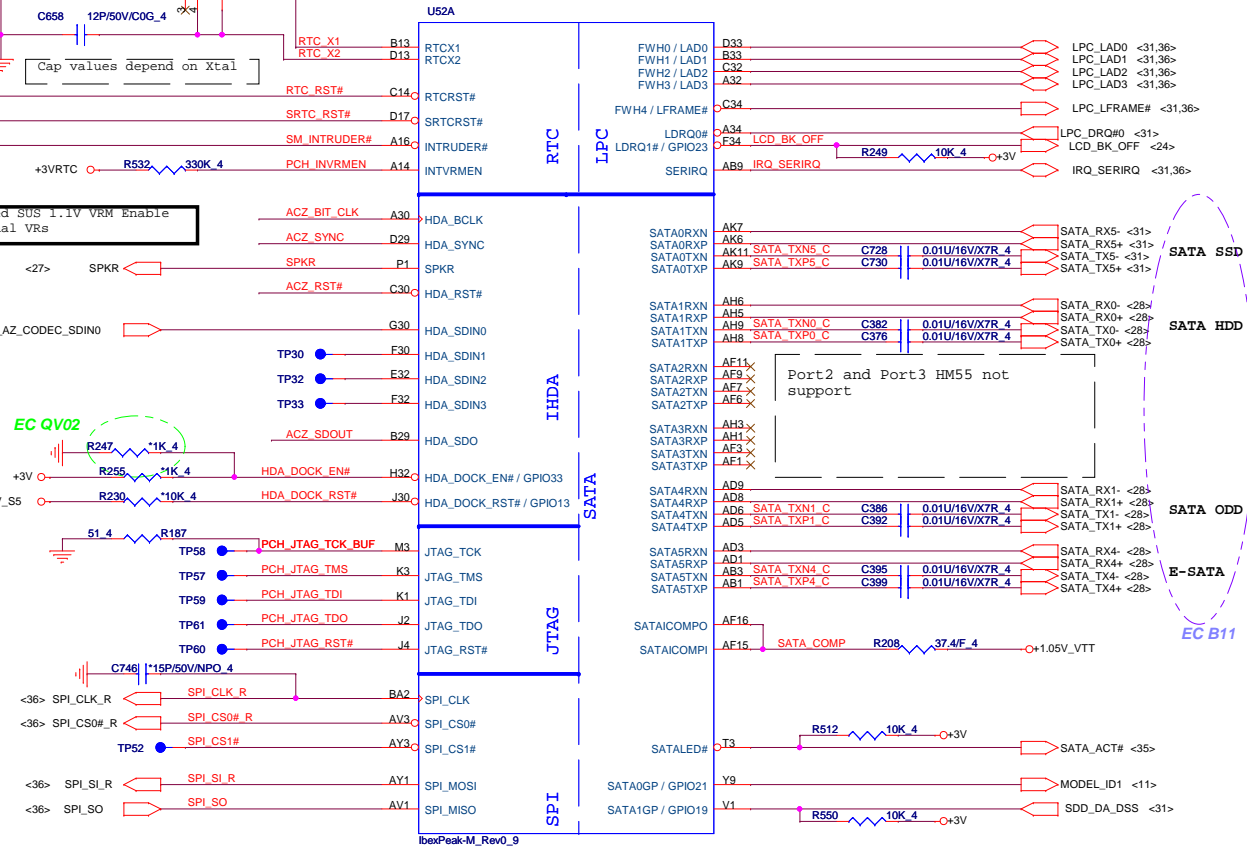
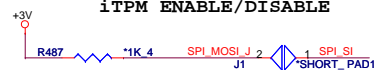
Place near connector

R515 *1K 4 SPKR

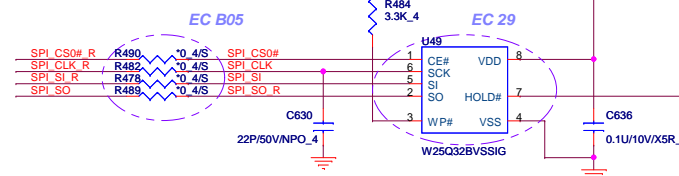
R236 *10K 4 IRQ_SERIRQ

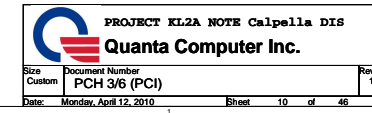
TPM Function	R487
Enable	Stuff
Disable	NC (Default)

iTPM ENABLE/DISABLE



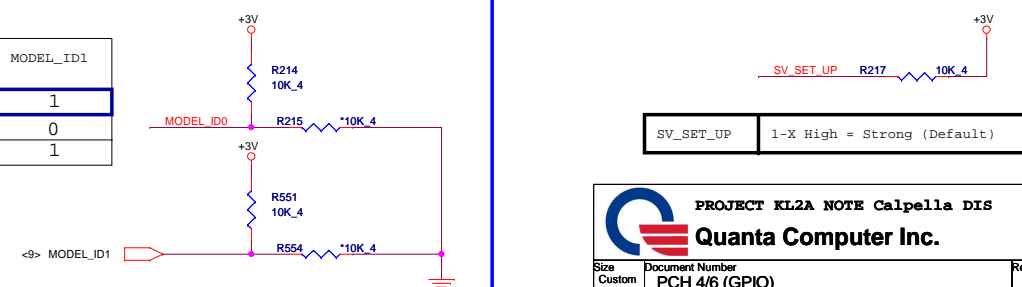
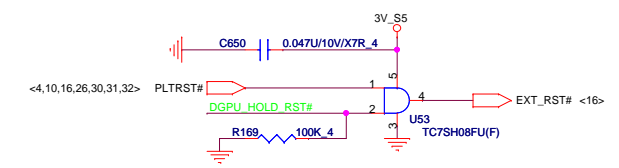
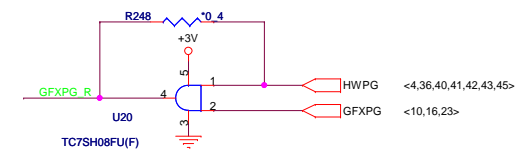
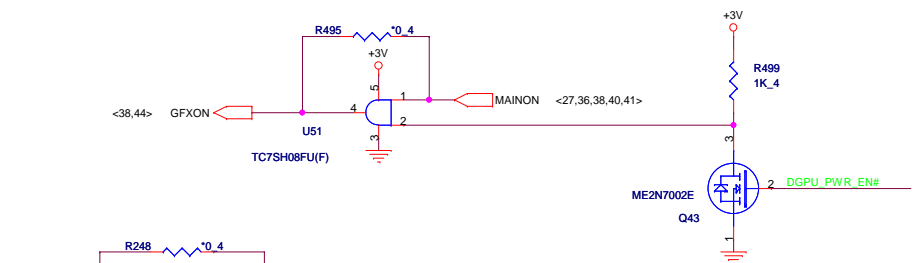
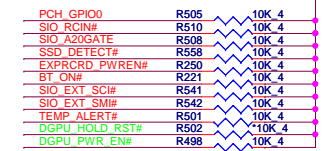
For PCH
32Mbit (4M Byte), SPI



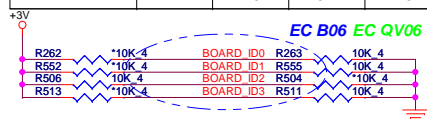


<3,4,8,9,10,12,14,15,23,24,25,26,27,28,29,30,31,32,33,34,35,36,38,39,43,44> +3V
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<3,4,6,8,9,10,12,38,41,43,45> +1.05V_VTT

PCH GPIO8	R260	10K 4
PCH GPIO12	R559	10K 4
PCH GPIO15	R222	1K 4
TP_PCH_GPIO028	R557	10K 4
CLK_PCIE_REQ6#	R544	10K 4
DRAMRST_PCH	R528	10K 4
WLAN_OFF#	R561	10K 4

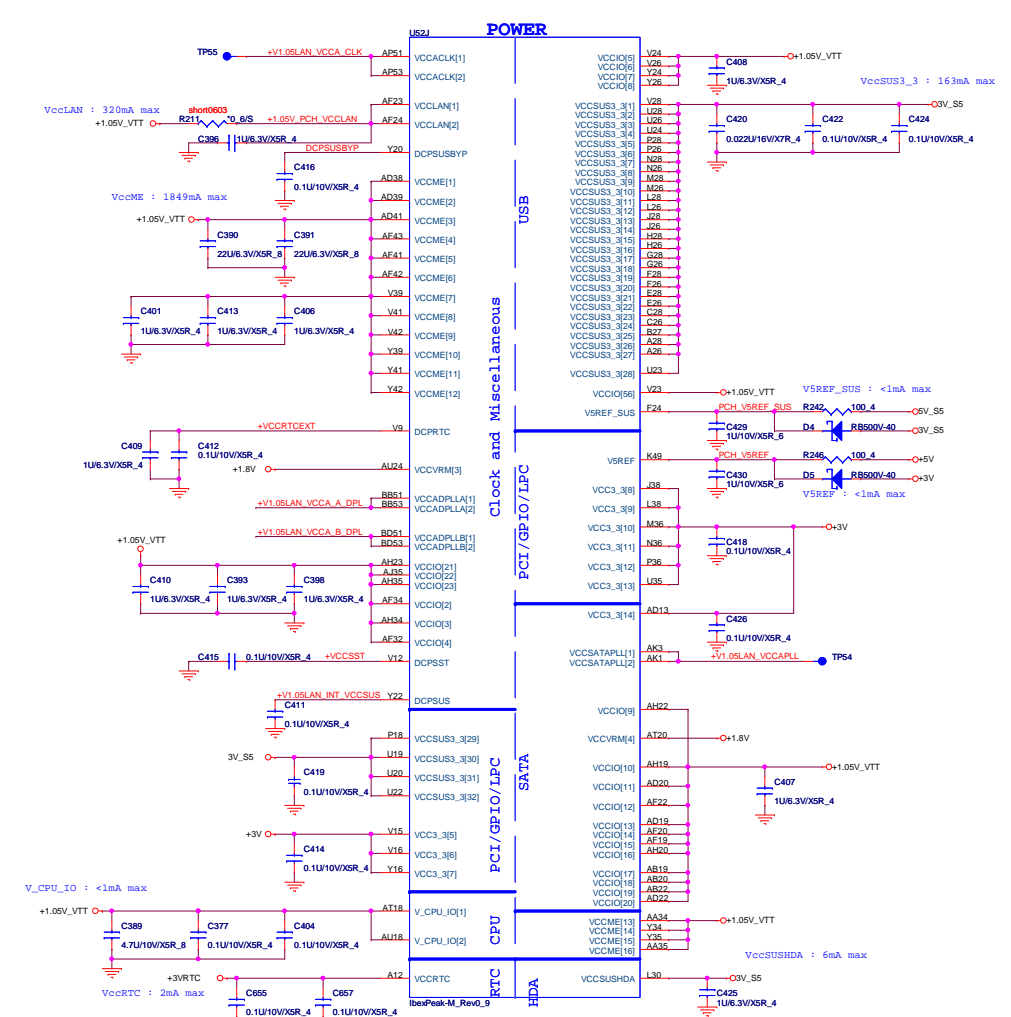


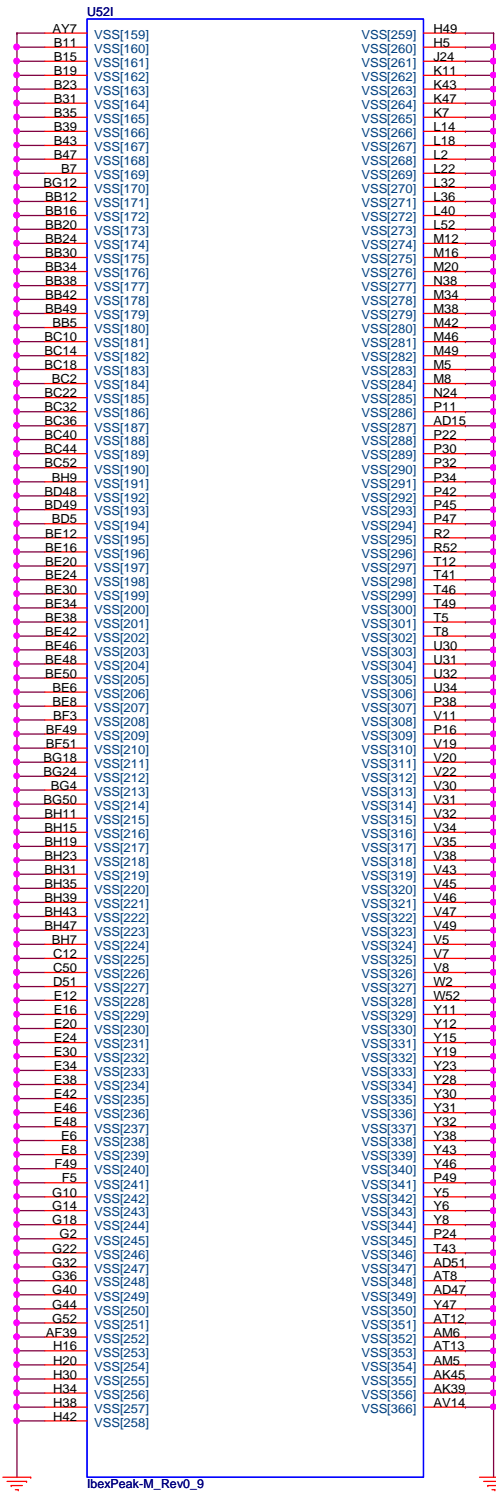
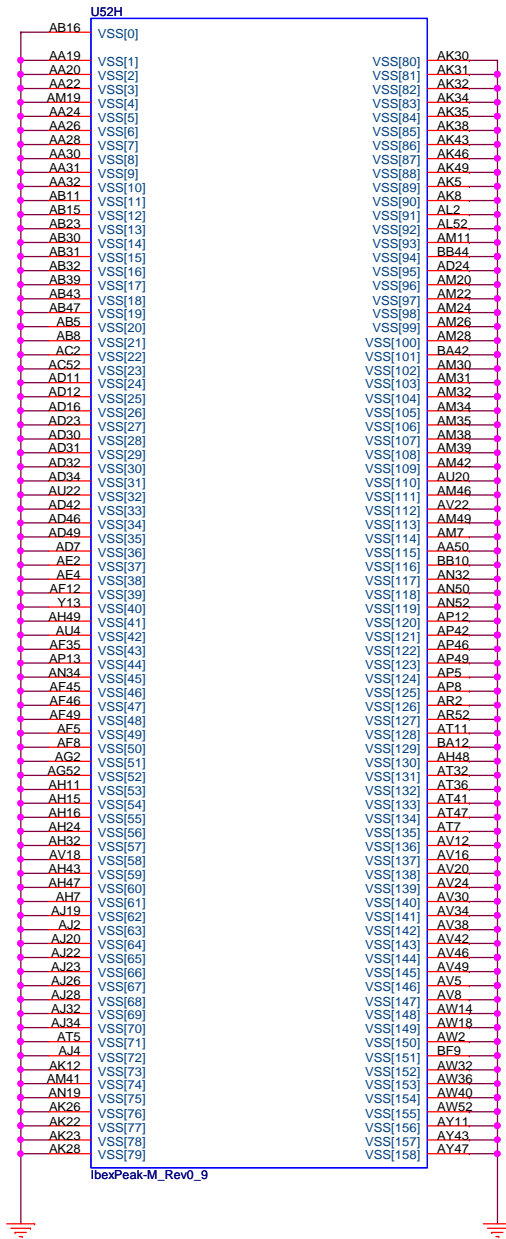
Board ID For Function	ID3 GPIO39	ID2 GPIO38	ID1 GPIO37	ID0 GPIO57
SDV	0	0	0	0
SIV	0	0	0	1
SIT	0	0	1	0
SVT	0	1	0	0
SOVF	1	0	0	0

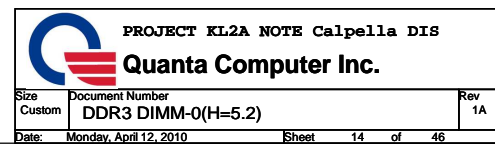


Model ID	MODEL_ID0	MODEL_ID1
14*	0	1
15*	1	0
KL2B	1	1

Model ID	MODEL_ID0	MODEL_ID1
14*	0	1
15*	1	0
KL2B	1	1







Place these Caps near So-Dimm0.

1.5VSUS

C614 10U/6.3V/X5R_6

C590 10U/6.3V/X5R_6

C250 10U/6.3V/X5R_6

C267 10U/6.3V/X5R_6

C620 10U/6.3V/X5R_6

C282 10U/6.3V/X5R_6

C604 0.1U/10V/X5R_4

C595 0.1U/10V/X5R_4

C242 0.1U/10V/X5R_4

C598 0.1U/10V/X5R_4

C273 0.1U/10V/X5R_4

C271 *330U/6.3V/ESR15_7343

+3V

C326 2.2U/6.3V/X5R_6

C327 0.1U/10V/X5R_4

0.75VSMDDR_VTERM

C333 1U/6.3V/X5R_4

C332 1U/6.3V/X5R_4

C346 1U/6.3V/X5R_4

C347 1U/6.3V/X5R_4

C334 10U/6.3V/X5R_6

C344 10U/6.3V/X5R_6

C335 10U/6.3V/X5R_6

SMDDR_VREF_DIMM

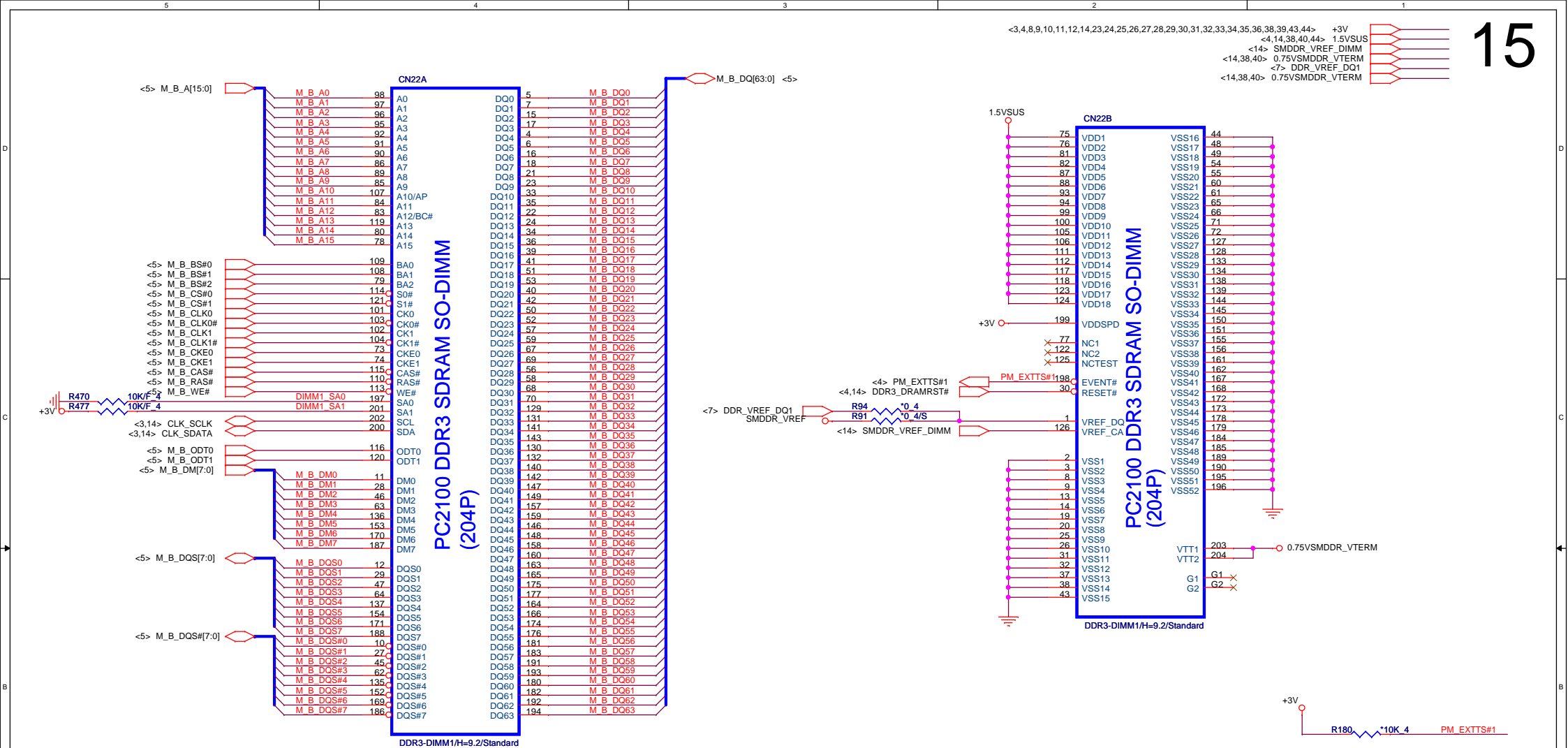
C621 0.1U/10V/X5R_4

C622 2.2U/6.3V/X5R_6

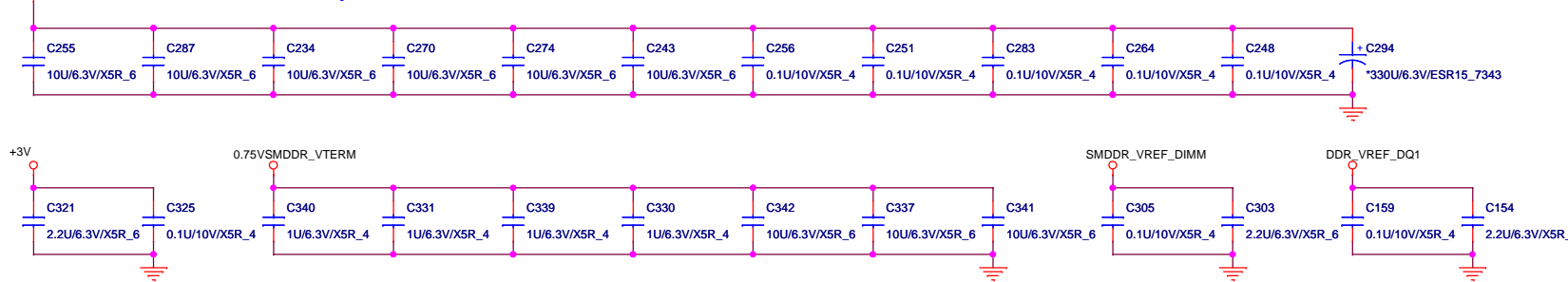
DDR_VREF_DQ0

C136 0.1U/10V/X5R_4

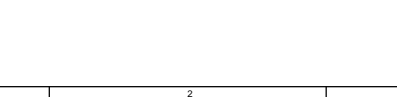
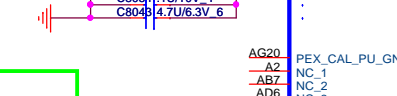
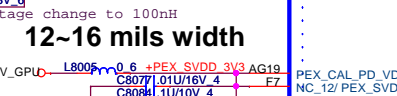
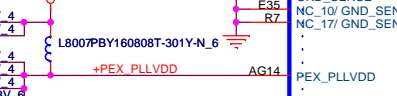
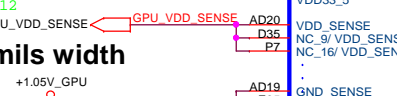
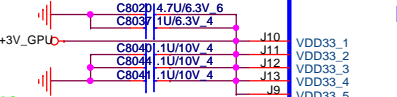
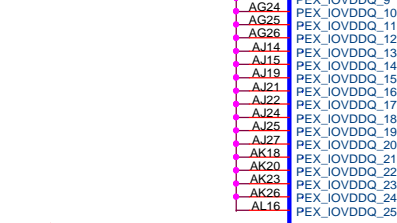
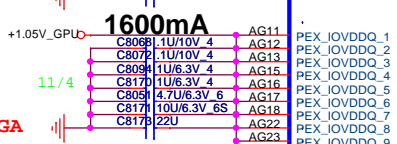
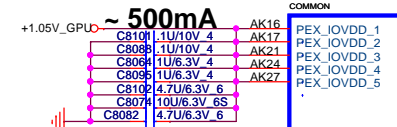
C141 2.2U/6.3V/X5R_6



Place these Caps near So-Dimm1.



PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD > 2.2A



U8006A
BGA985-NVIDIA-NB9P-GS
COMMON

PEX_IOVDD_1
PEX_IOVDD_2
PEX_IOVDD_3
PEX_IOVDD_4
PEX_IOVDD_5
PEX_IOVDDQ_1
PEX_IOVDDQ_2
PEX_IOVDDQ_3
PEX_IOVDDQ_4
PEX_IOVDDQ_5
PEX_IOVDDQ_6
PEX_IOVDDQ_7
PEX_IOVDDQ_8
PEX_IOVDDQ_9
PEX_IOVDDQ_10
PEX_IOVDDQ_11
PEX_IOVDDQ_12
PEX_IOVDDQ_13
PEX_IOVDDQ_14
PEX_IOVDDQ_15
PEX_IOVDDQ_16
PEX_IOVDDQ_17
PEX_IOVDDQ_18
PEX_IOVDDQ_19
PEX_IOVDDQ_20
PEX_IOVDDQ_21
PEX_IOVDDQ_22
PEX_IOVDDQ_23
PEX_IOVDDQ_24
PEX_IOVDDQ_25

VDD33_1
VDD33_2
VDD33_3
VDD33_4
VDD33_5
VDD33_6
VDD33_7
VDD33_8
VDD33_9
VDD33_10
VDD33_11
VDD33_12
VDD33_13
VDD33_14
VDD33_15
VDD33_16
VDD33_17
VDD33_18
VDD33_19
VDD33_20
VDD33_21
VDD33_22
VDD33_23
VDD33_24
VDD33_25

PEX_CAL_PU_GND/ NC
NC_1
NC_2
NC_3
NC_4
NC_5
NC_6
NC_7
NC_8
NC_9
NC_10
NC_11
NC_12
NC_13
NC_14
NC_15
NC_16
NC_17
NC_18
NC_19

PEX_CAL_PU_GND/ NC
NC_1
NC_2
NC_3
NC_4
NC_5
NC_6
NC_7
NC_8
NC_9
NC_10
NC_11
NC_12
NC_13
NC_14
NC_15
NC_16
NC_17
NC_18
NC_19

Reverse

PEX_RX0
PEX_RX1
PEX_RX2
PEX_RX3
PEX_RX4
PEX_RX5
PEX_RX6
PEX_RX7
PEX_RX8
PEX_RX9
PEX_RX10
PEX_RX11
PEX_RX12
PEX_RX13
PEX_RX14
PEX_RX15
PEX_TX0
PEX_TX1
PEX_TX2
PEX_TX3
PEX_TX4
PEX_TX5
PEX_TX6
PEX_TX7
PEX_TX8
PEX_TX9
PEX_TX10
PEX_TX11
PEX_TX12
PEX_TX13
PEX_TX14
PEX_TX15

PEX_RX0
PEX_RX1
PEX_RX2
PEX_RX3
PEX_RX4
PEX_RX5
PEX_RX6
PEX_RX7
PEX_RX8
PEX_RX9
PEX_RX10
PEX_RX11
PEX_RX12
PEX_RX13
PEX_RX14
PEX_RX15
PEX_TX0
PEX_TX1
PEX_TX2
PEX_TX3
PEX_TX4
PEX_TX5
PEX_TX6
PEX_TX7
PEX_TX8
PEX_TX9
PEX_TX10
PEX_TX11
PEX_TX12
PEX_TX13
PEX_TX14
PEX_TX15

PEX_RX0
PEX_RX1
PEX_RX2
PEX_RX3
PEX_RX4
PEX_RX5
PEX_RX6
PEX_RX7
PEX_RX8
PEX_RX9
PEX_RX10
PEX_RX11
PEX_RX12
PEX_RX13
PEX_RX14
PEX_RX15
PEX_TX0
PEX_TX1
PEX_TX2
PEX_TX3
PEX_TX4
PEX_TX5
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PEX_TX15

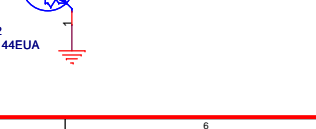
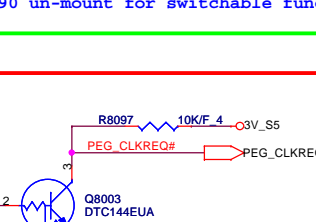
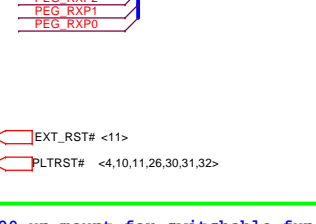
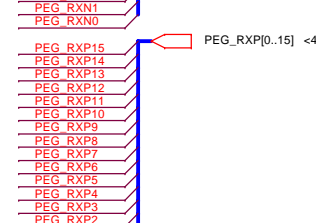
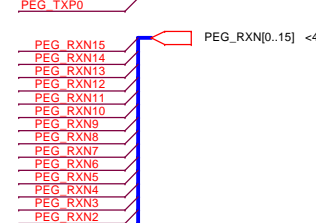
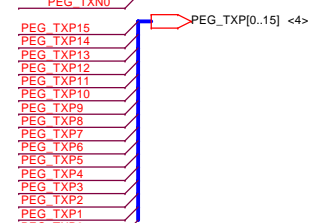
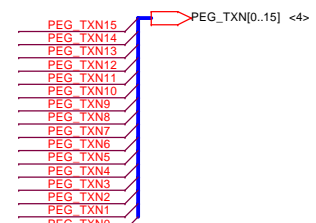
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PEX_RX5
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PEX_RX9
PEX_RX10
PEX_RX11
PEX_RX12
PEX_RX13
PEX_RX14
PEX_RX15
PEX_TX0
PEX_TX1
PEX_TX2
PEX_TX3
PEX_TX4
PEX_TX5
PEX_TX6
PEX_TX7
PEX_TX8
PEX_TX9
PEX_TX10
PEX_TX11
PEX_TX12
PEX_TX13
PEX_TX14
PEX_TX15

Reverse

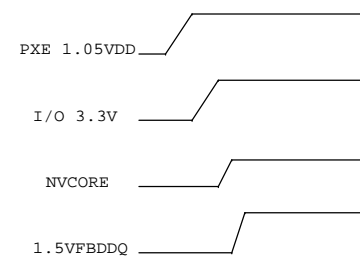
PEX_RX0
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PEX_RX9
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PEX_RX12
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PEX_RX14
PEX_RX15
PEX_TX0
PEX_TX1
PEX_TX2
PEX_TX3
PEX_TX4
PEX_TX5
PEX_TX6
PEX_TX7
PEX_TX8
PEX_TX9
PEX_TX10
PEX_TX11
PEX_TX12
PEX_TX13
PEX_TX14
PEX_TX15

PEX_RX0
PEX_RX1
PEX_RX2
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PEX_RX4
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PEX_TX15

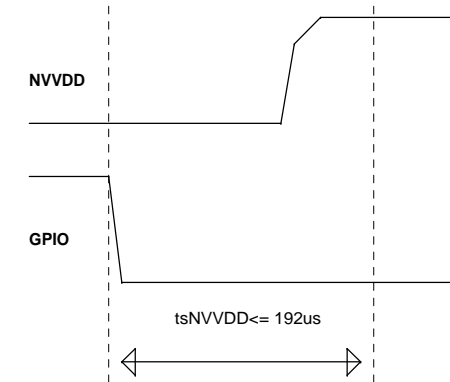
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PEX_RX9
PEX_RX10
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PEX_RX12
PEX_RX13
PEX_RX14
PEX_RX15
PEX_TX0
PEX_TX1
PEX_TX2
PEX_TX3
PEX_TX4
PEX_TX5
PEX_TX6
PEX_TX7
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PEX_TX9
PEX_TX10
PEX_TX11
PEX_TX12
PEX_TX13
PEX_TX14
PEX_TX15



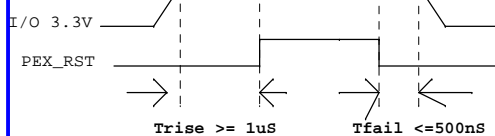
power up sequence



NB9M: VGACORE +0.90V (Normal) , +1.09V
NVVDD Maximum Settling Time

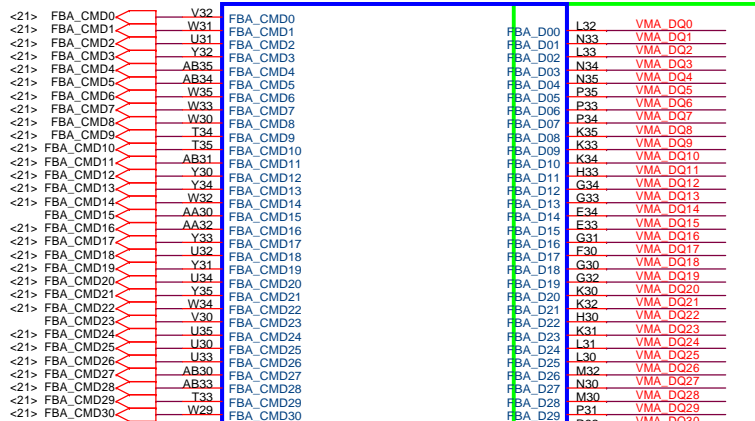
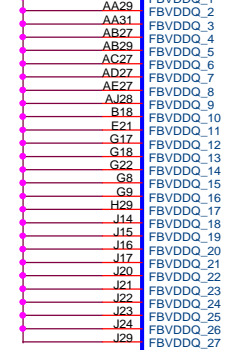
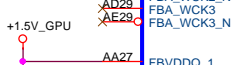
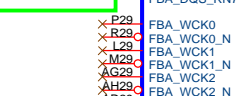
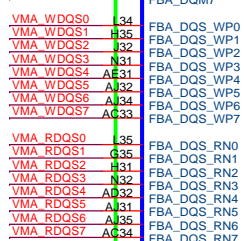
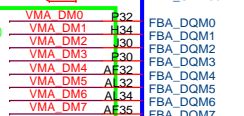


PEX_RST timing

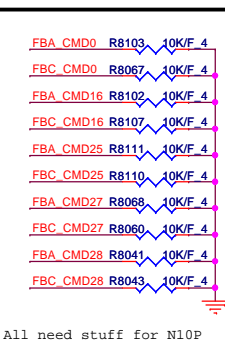
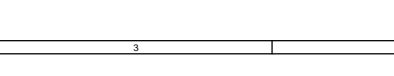
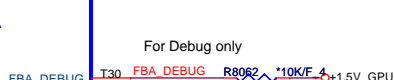
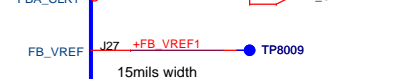
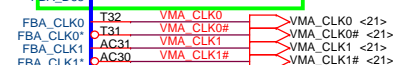


<17,18,38,44> +1.05V_GPU
<18,19,23,44> +3V_GPU

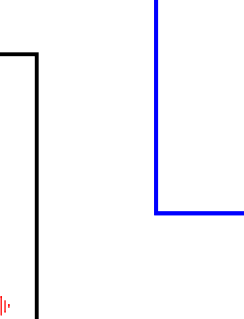
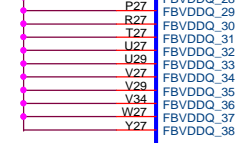
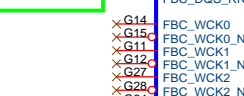
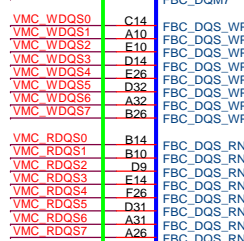
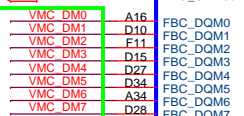
U8006B

BG9899-NVIDIA-NB9P-GS
COMMON12/02 modify
package for N1012/02 modify
package for N10

MEMORY I/F A

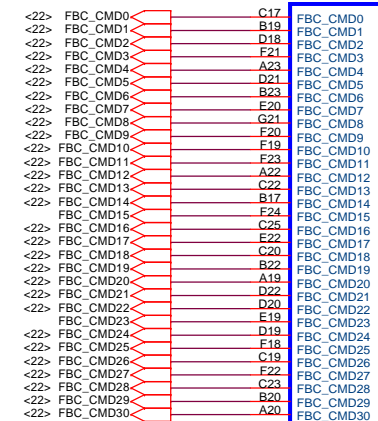
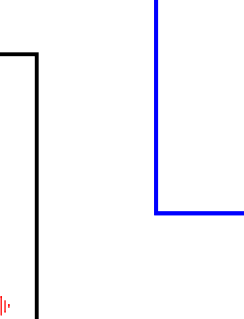
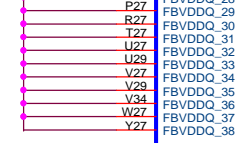
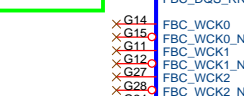
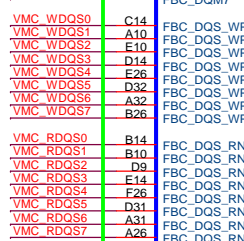
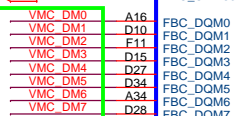


All need stuff for N10P

12/02 modify
package for N10

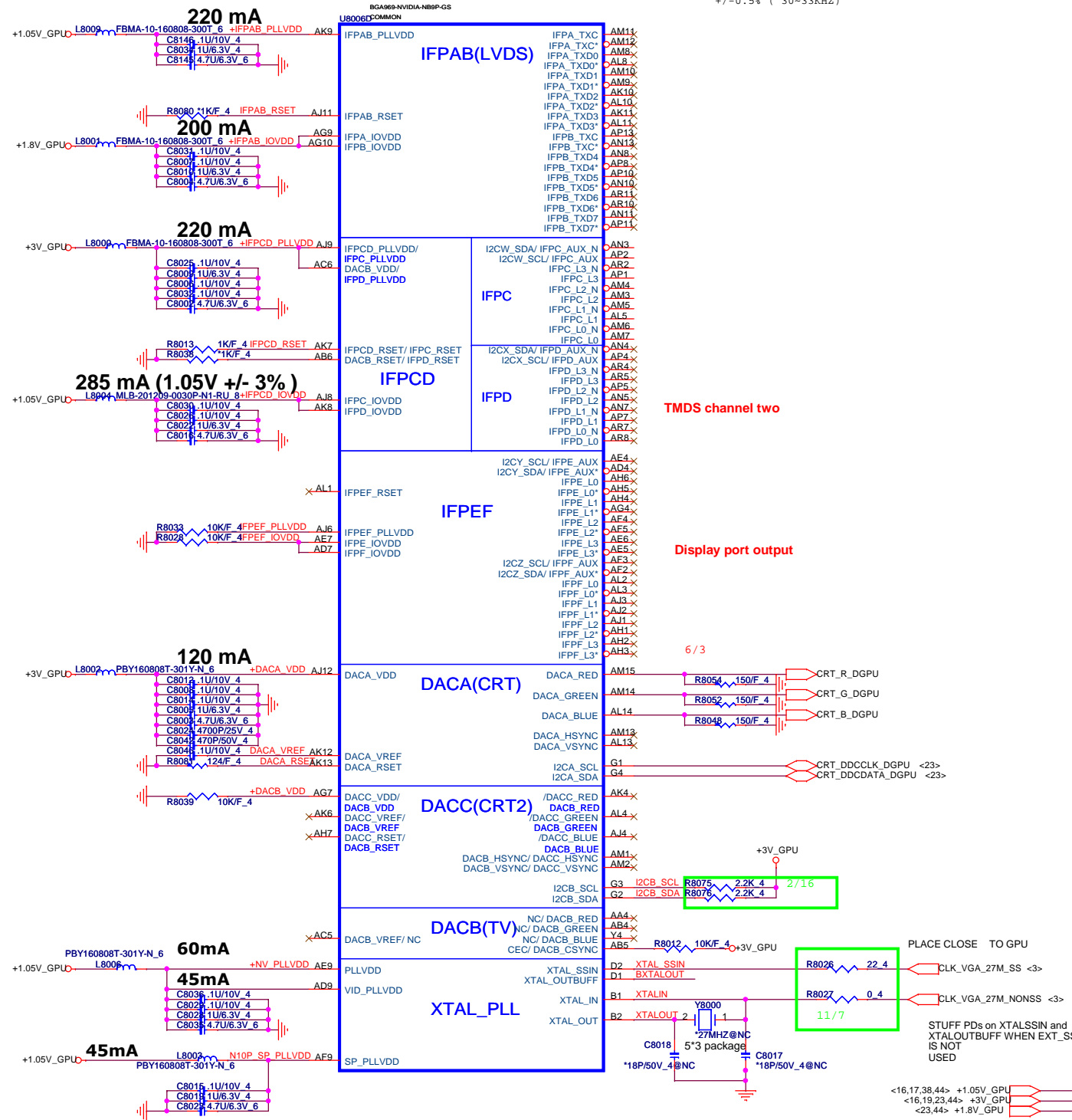
All need stuff for N10P

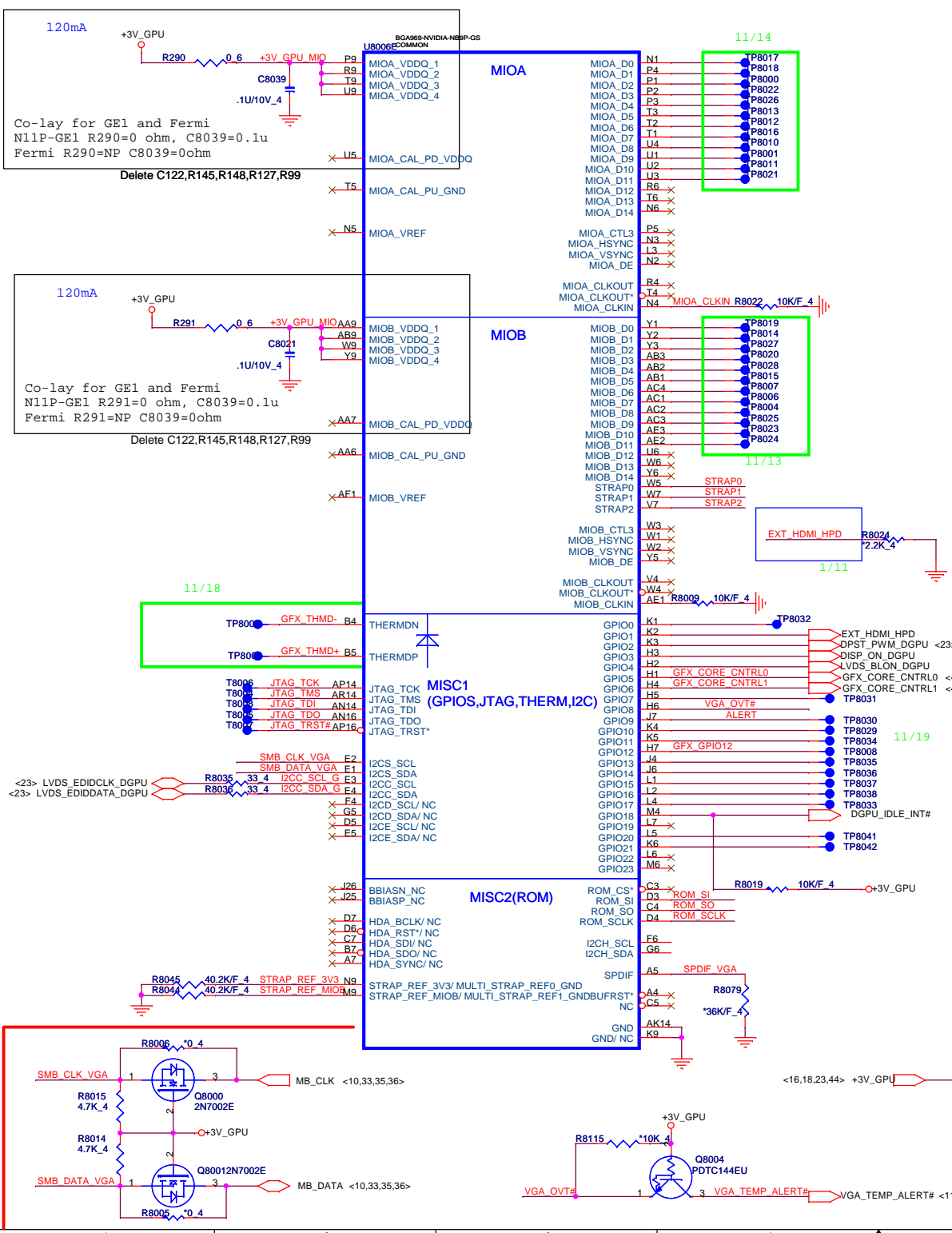
U8006C

BG9899-NVIDIA-NB9P-GS
COMMON12/02 modify
package for N1012/02 modify
package for N10

All need stuff for N10P

<16,18,38,44> +1.05V_GPU
<21,22,23,40> +1.5V_GPU





CHIP: N10P-GE, N10M-GE

PCI_DEVID	STRAP2	ROM_SCLK
0x0A28	1000 PU 5K	0010 PD 15K
0x0A68	1000 PU 5K	0010 PD 15K

CHIP: N11P-GS1, N11M-GS1, N11P-GE1

PCI_DEVID	STRAP2	ROM_SCLK
0x0CAF	1111 PU 45K	0010 PD 15K
0x0A35	0101 PD 30K	1010 PU 15K
	PU 10K	

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

(Ra)

Default: Hynix VRAM

For N11P-GE1

4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
 10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1%(0402)]
 15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1%(0402)]
 20K/F_4: CS32002FB29 [RES CHIP 20K 1/16W +1%(0402)]
 30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +1%(0402)]
 35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +1%(0402)]
 45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +1%(0402)]

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	NB10X	XCLX 417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK		PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI		RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2		PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1		3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0		USER[3]	USER[2]	USER[1]	USER[0]

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Reserved	IDGH1G-04A1F1C-16X	PD 10K
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	H5TQ1G63BFR-12C	PD 15K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	K4W1G1646E-HC12	PD 20K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung		
0101	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Reserved		
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

(Ra)

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVD VID0
6	OUT	N/A	NVVD VID1
7	OUT	N/A	NVVD VID2 ^{11/13}
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL ^{11/13}
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

HDCP ROM

Fill U36 to correct p/n as Top B/S P/N (AR0QT6VB002)

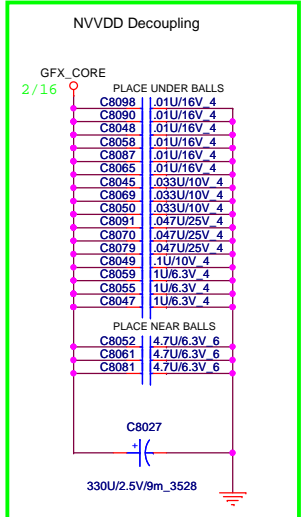
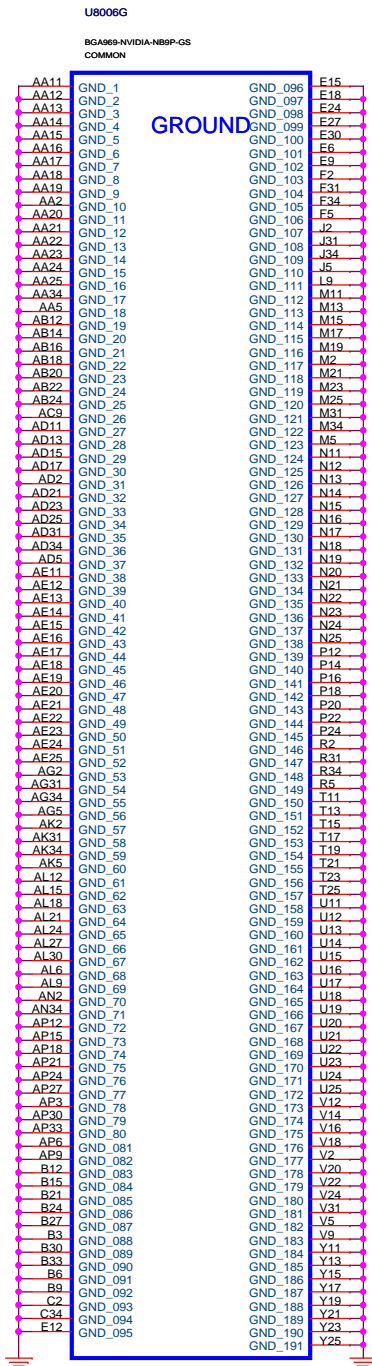
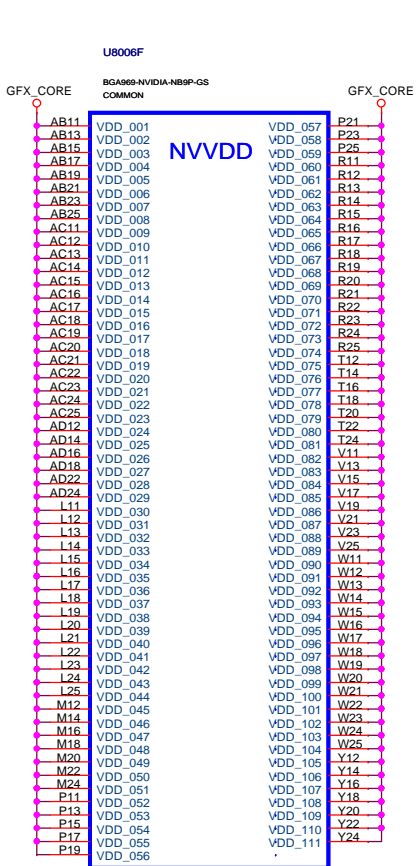
HDCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

PROJECT KL2A NOTE Calpella DIS

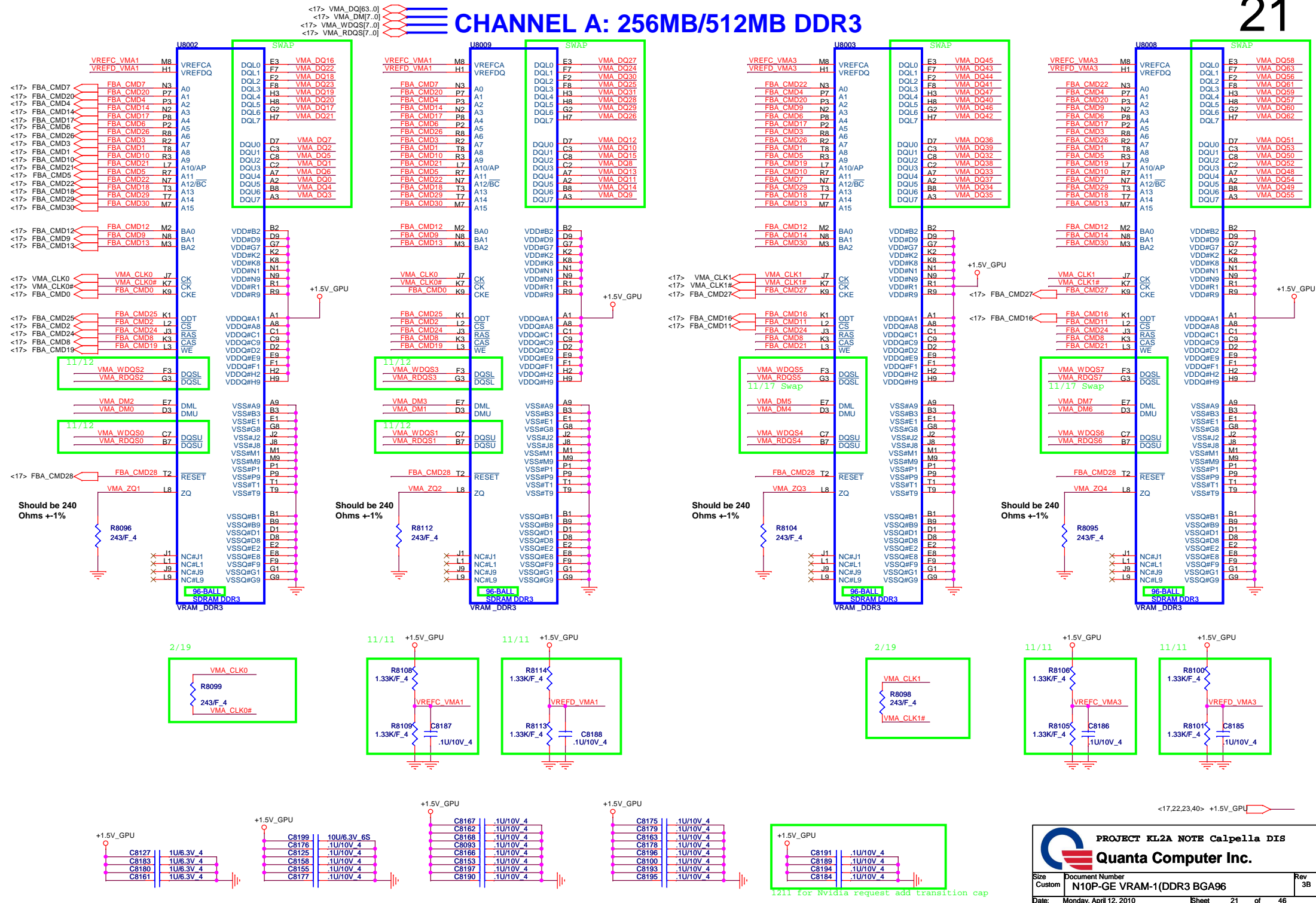
Quanta Computer Inc.

Size: Custom Document Number: N10P-GE (GPIO&STRAPS) 4/5 Rev: 3B

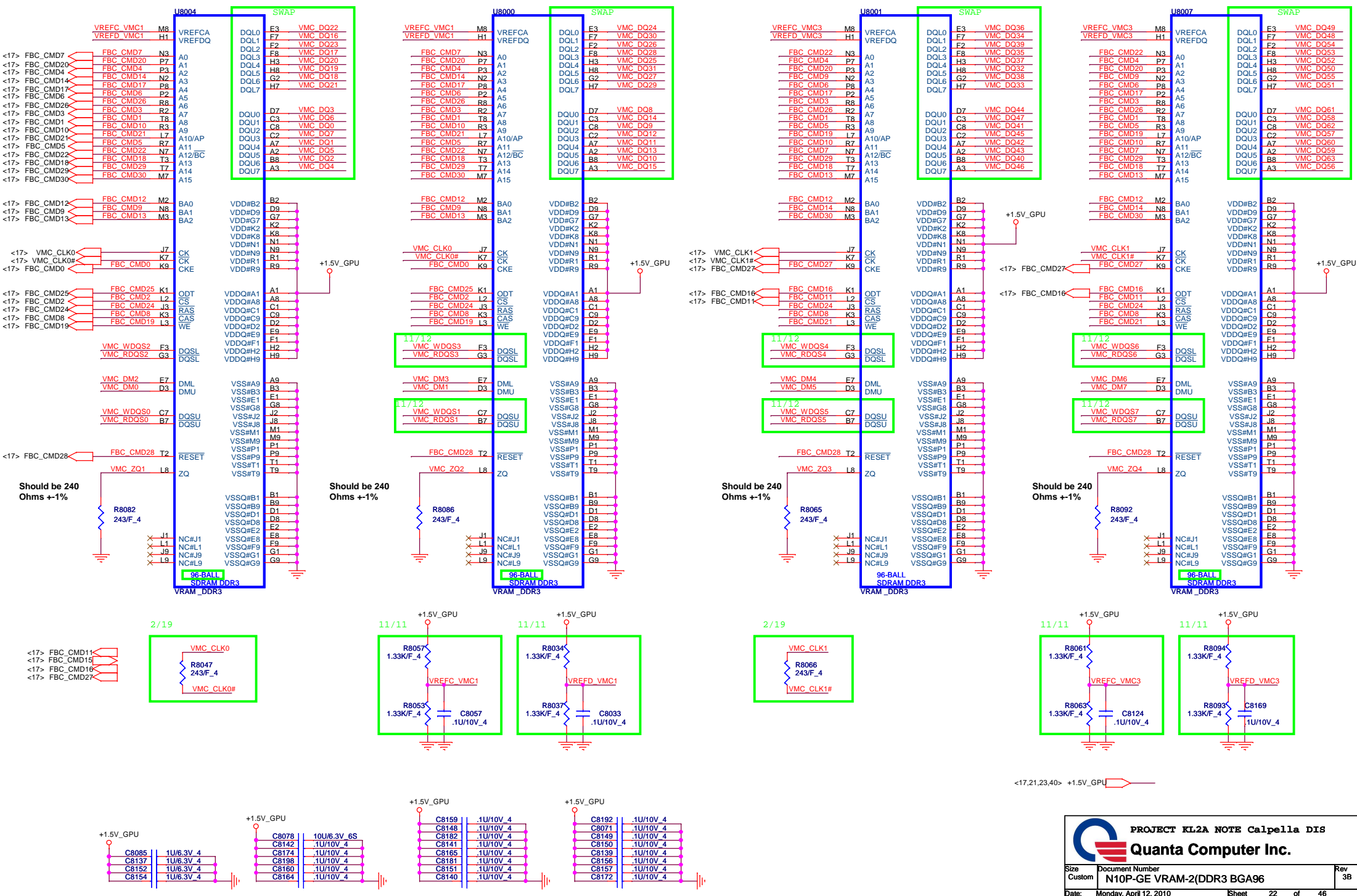
Date: Monday, April 12, 2010 Sheet: 19 of 46

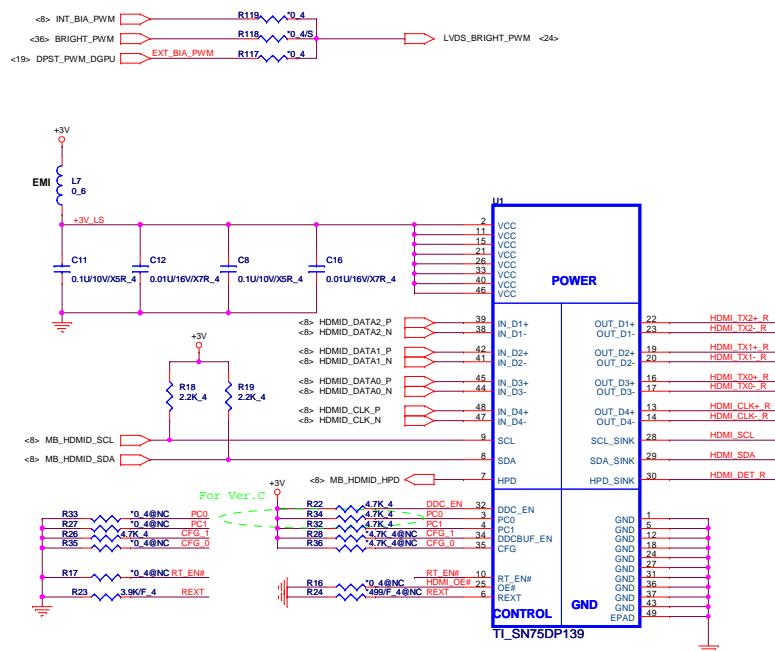


CHANNEL A: 256MB/512MB DDR3



CHANNEL B: 256MB/512MB DDR3

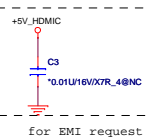




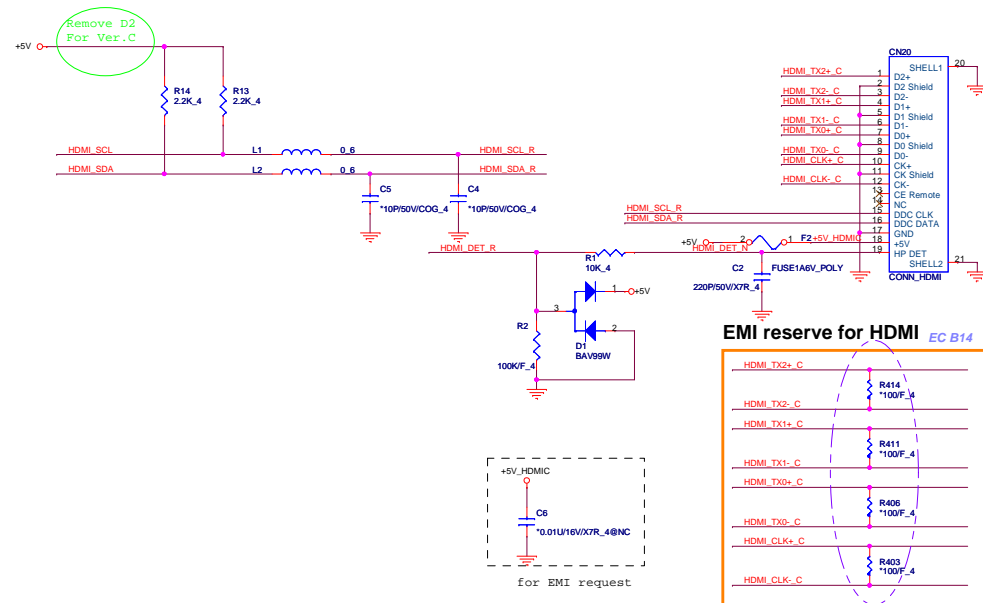
EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommended
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

PS8101 Pin34/35 is NC

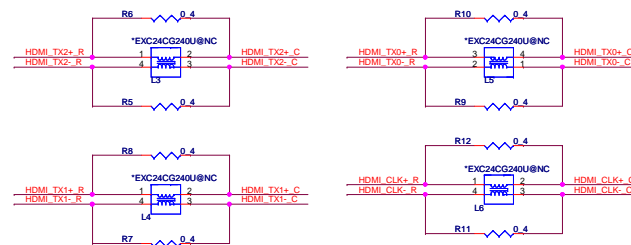
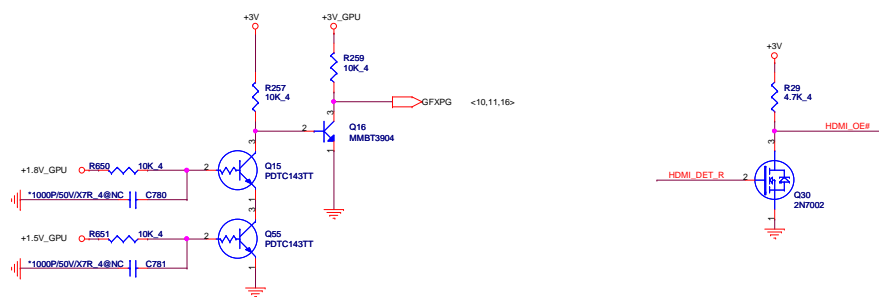
SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF4:CGF3=1:0 VIL:<0.41V VOL:<0.65V



HDMI

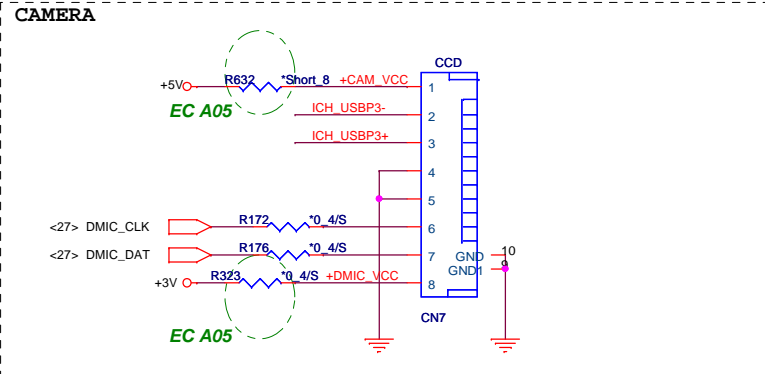
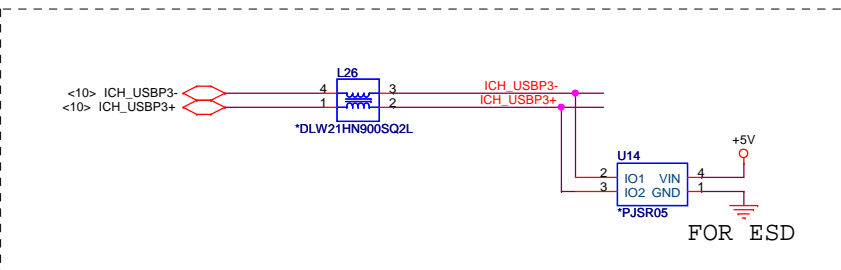
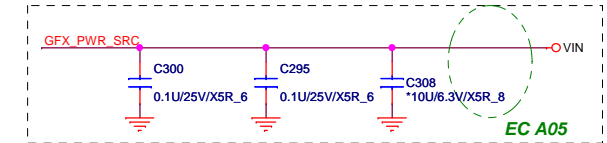
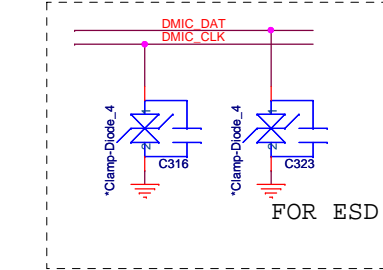
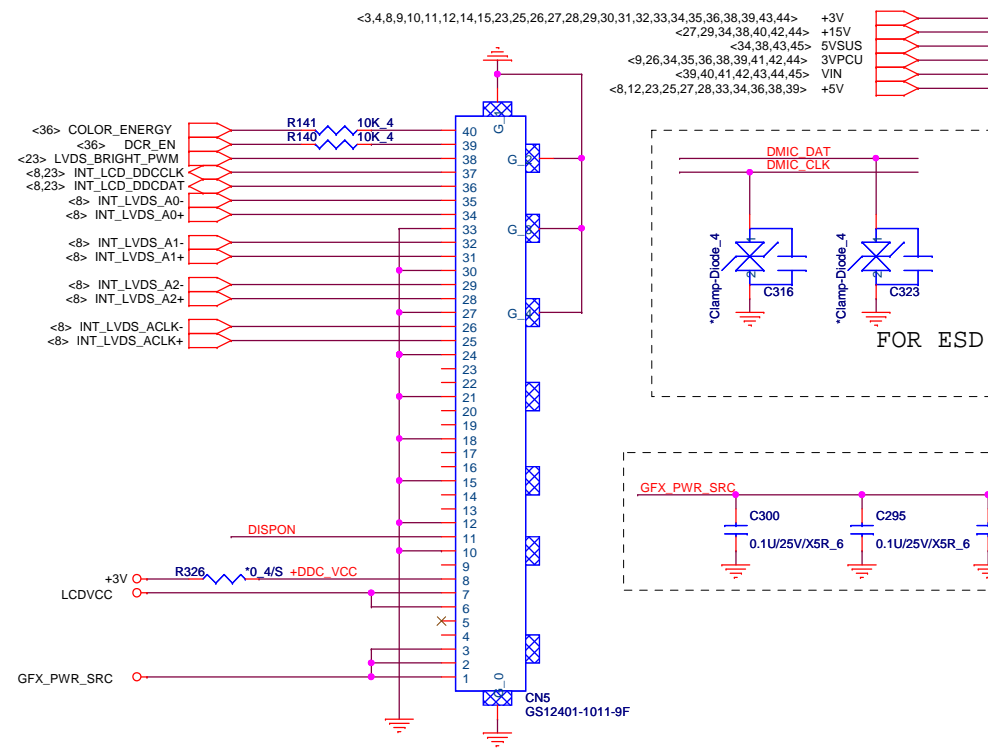
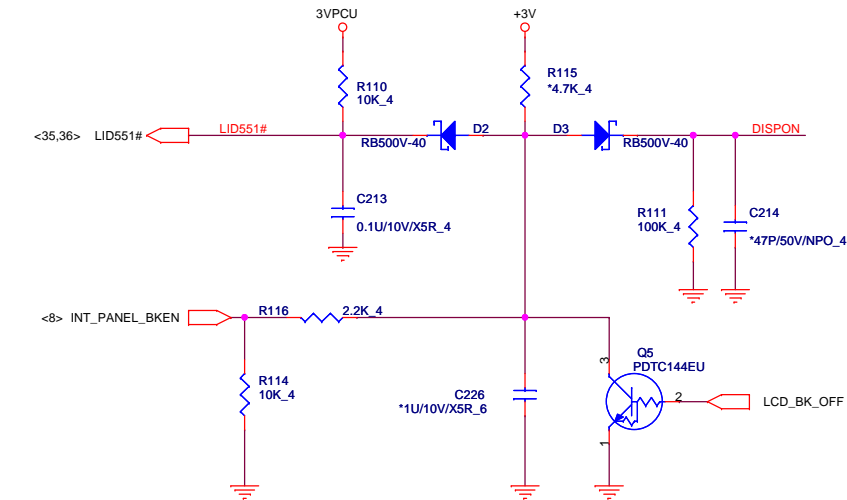
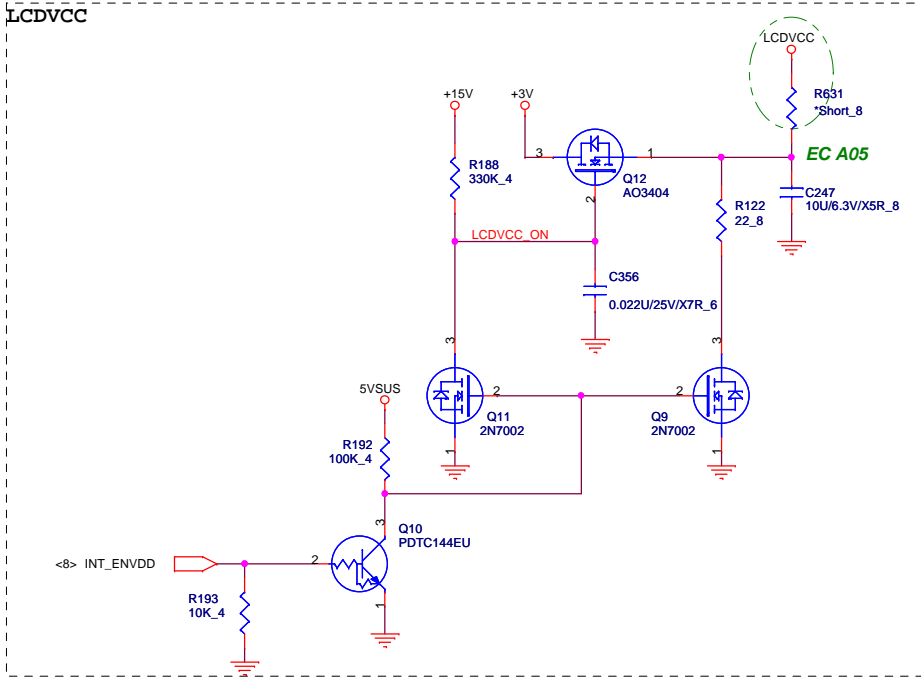


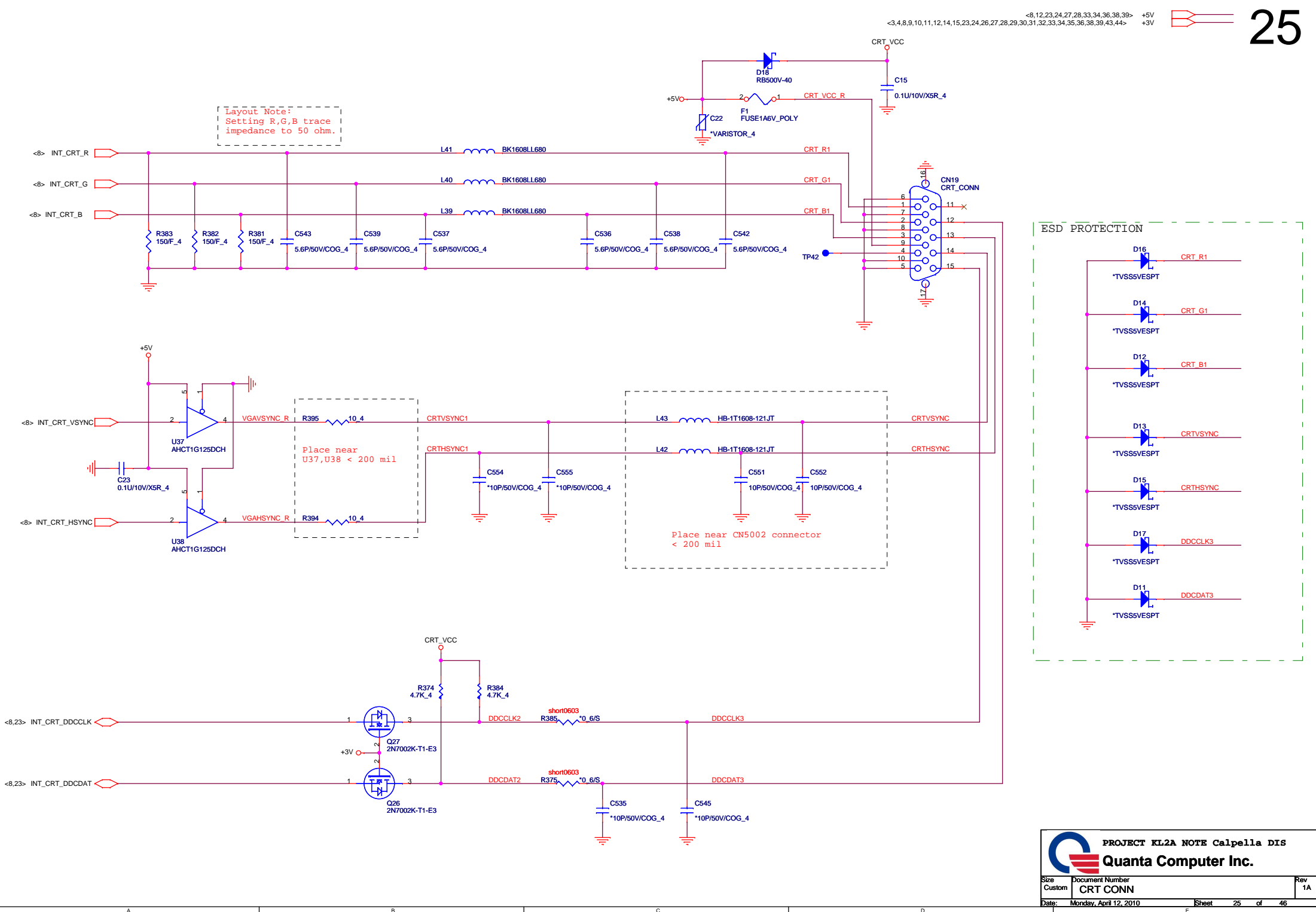
GPU all PWROK

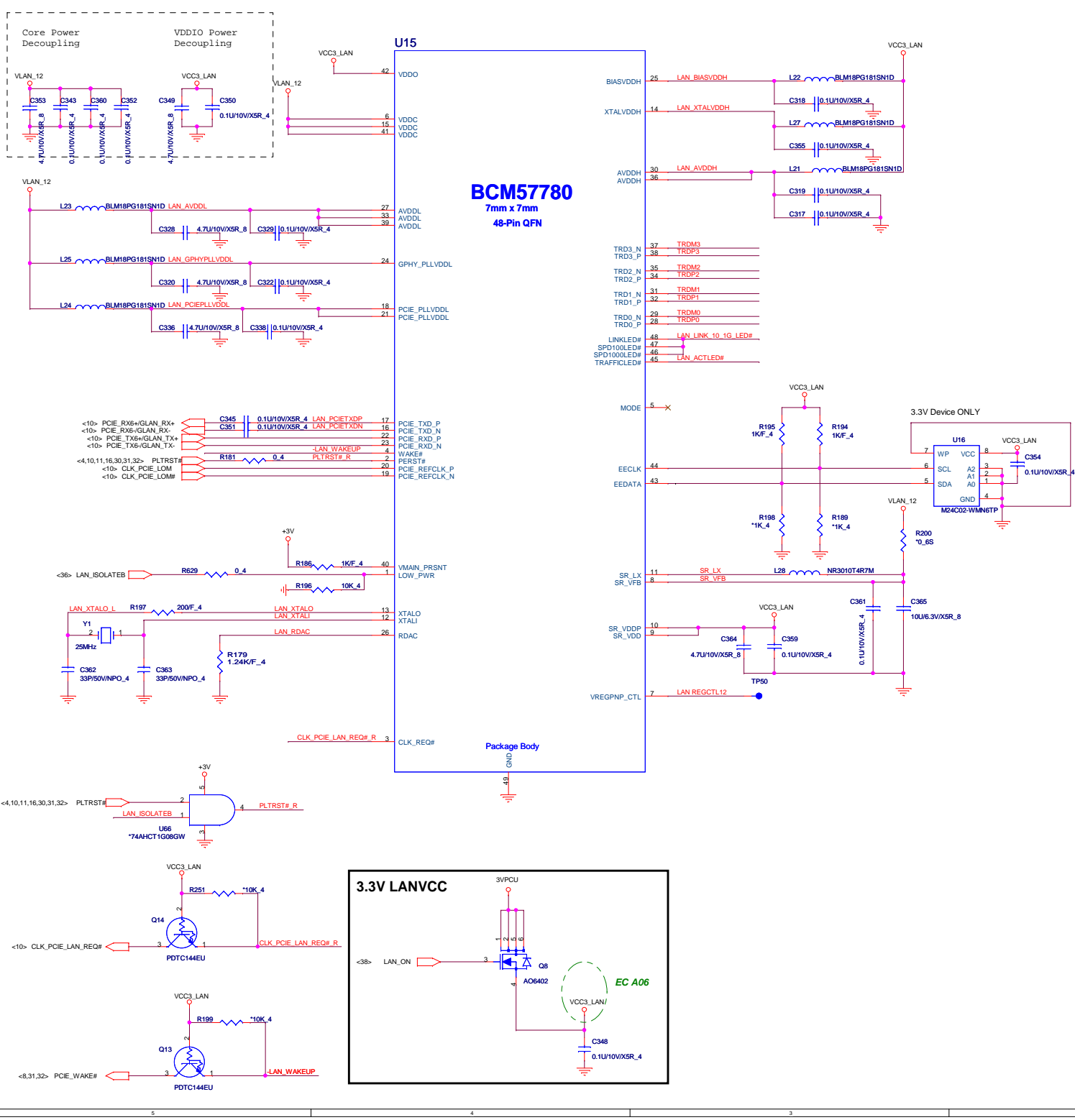


	<16,17,18,38,44>	+1.05V_GPU
	<17,21,22,40>	+1.5V_GPU
	<18,44>	+1.8V_GPU
	<16,18,19,44>	+3V_GPU
<3,4,8,9,10,11,12,14,15,24,25,26,27,28,29,30,31,32,33,34,35,36,38,39,43,44>		+3V
<8,12,24,25,27,28,33,34,36,38,39>		+5V

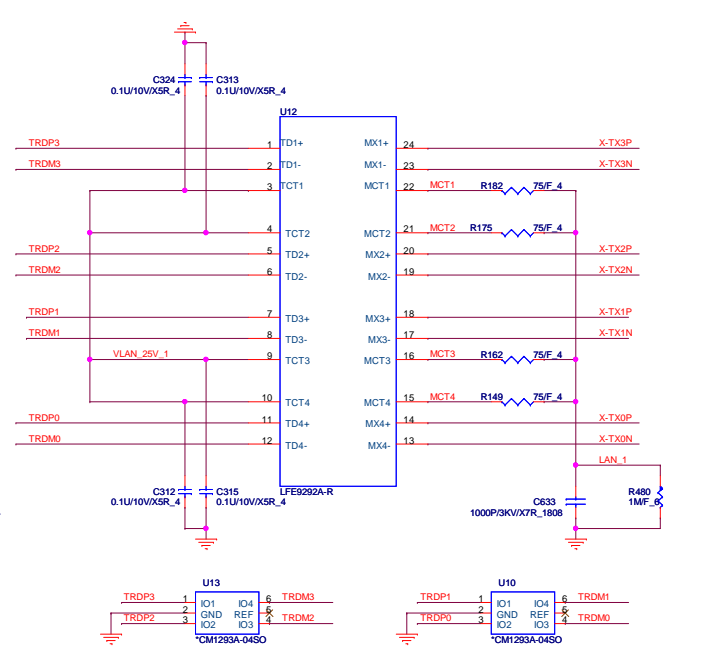
CAMERA



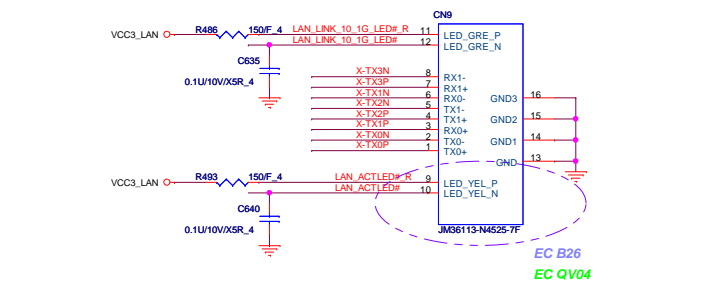




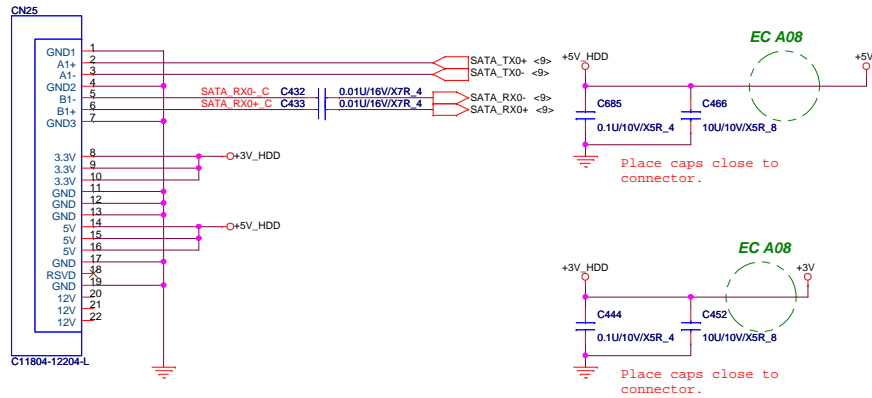
Transformer



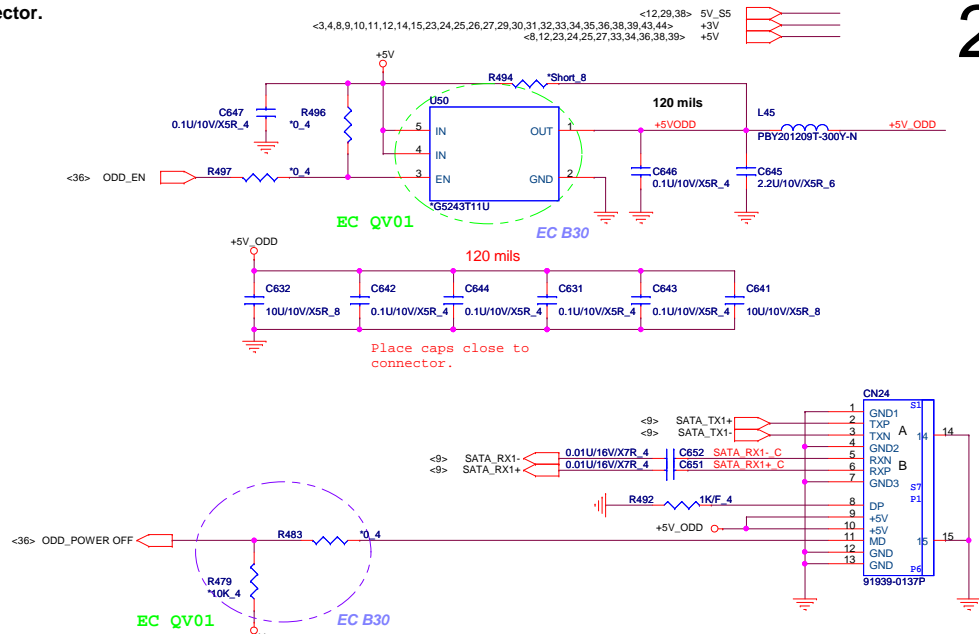
RJ45 Connector



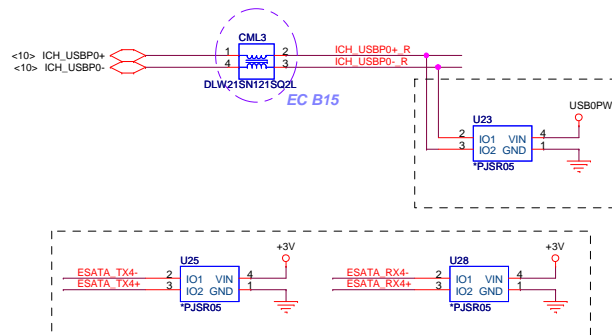
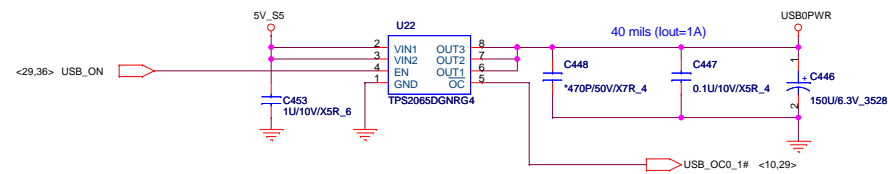
SATA HDD Connector.



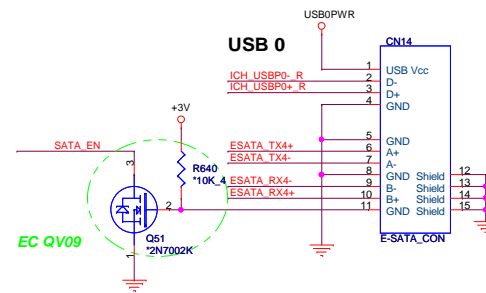
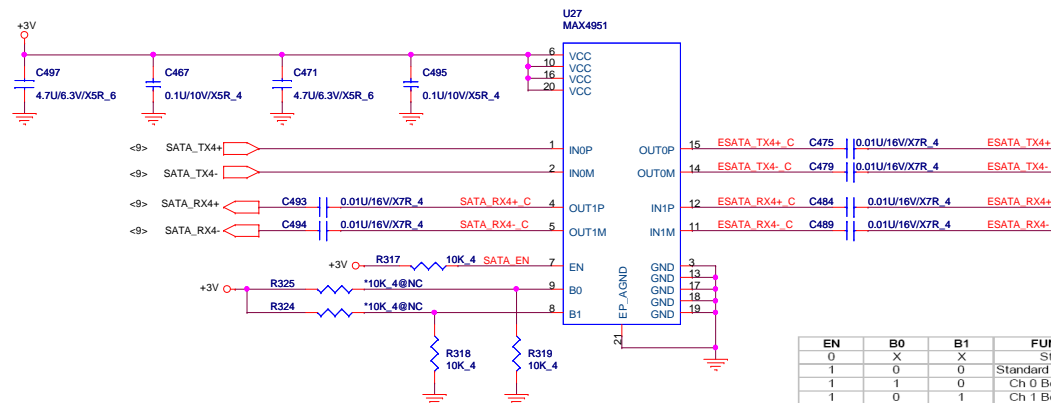
SATA ODD Connector.



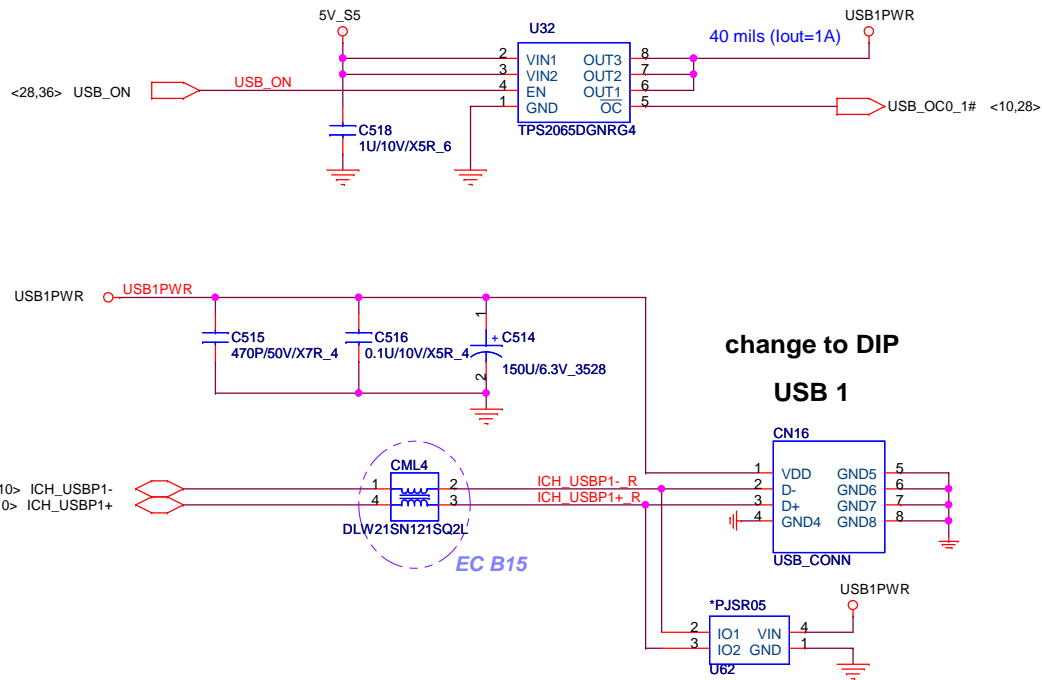
USB + E-SATA



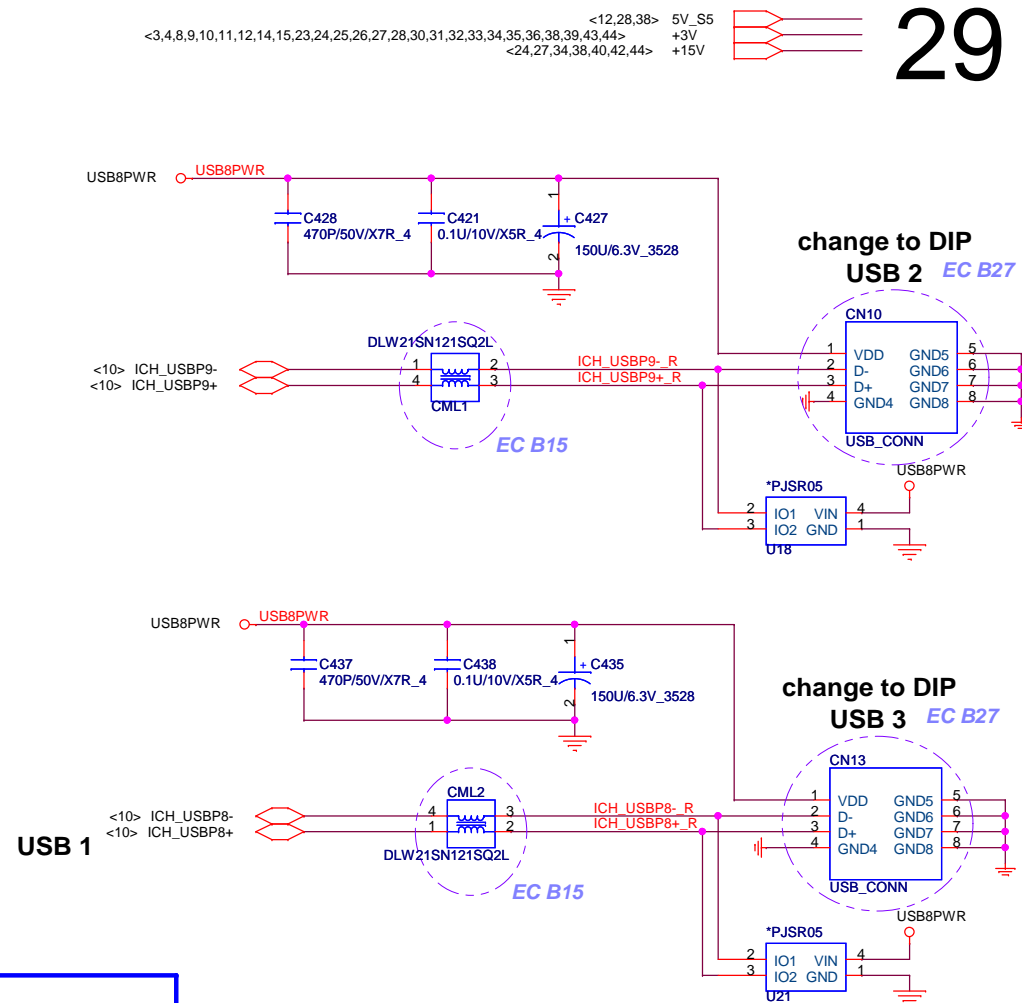
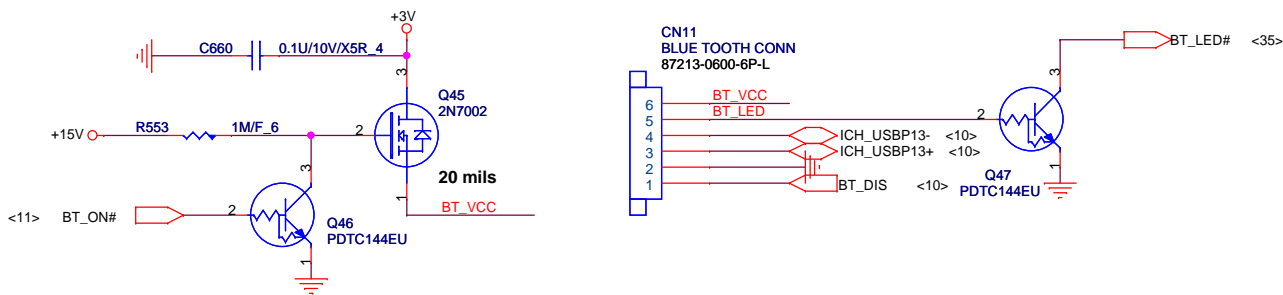
E-SATA RE-DRIVER

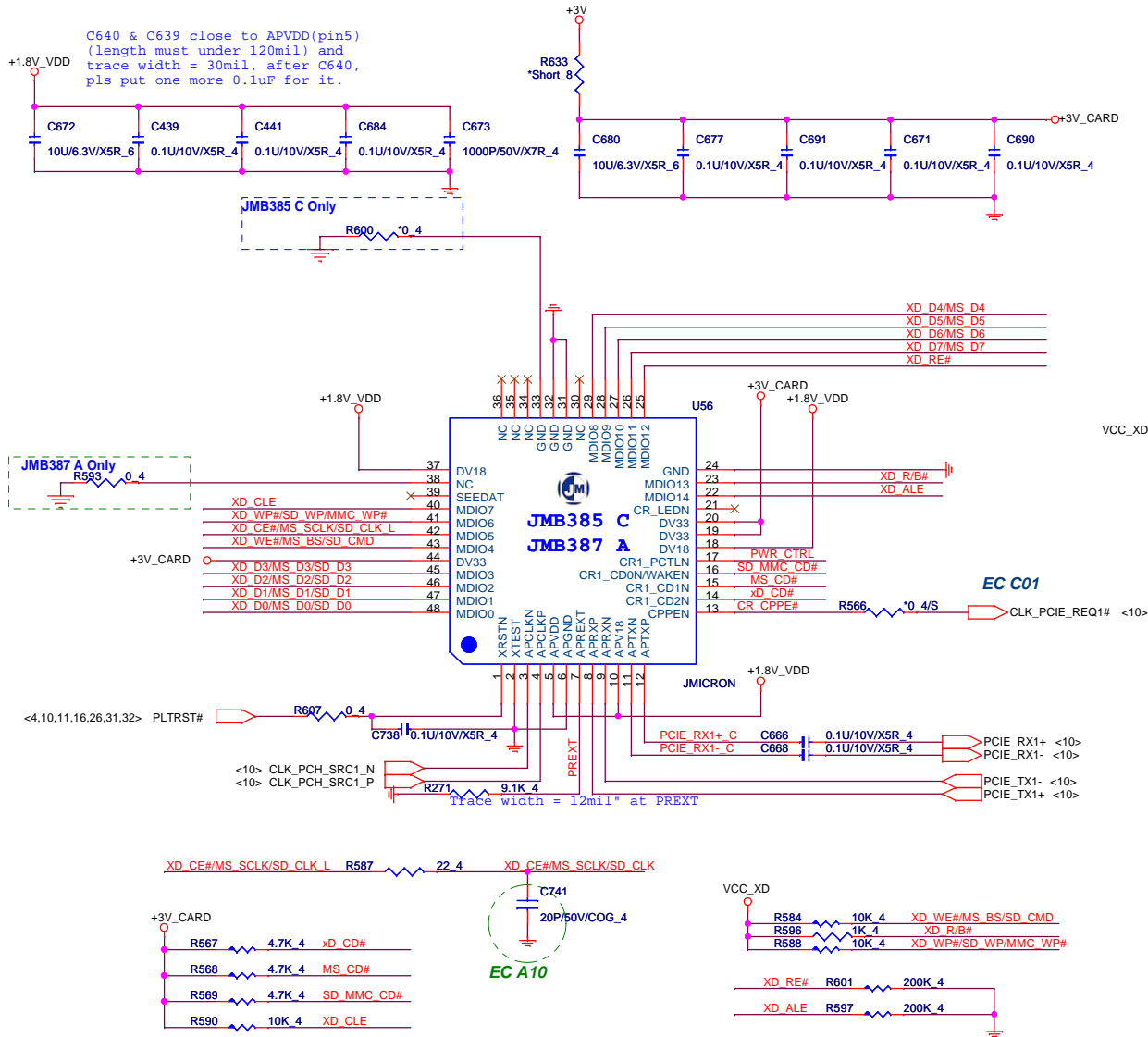


USBX3

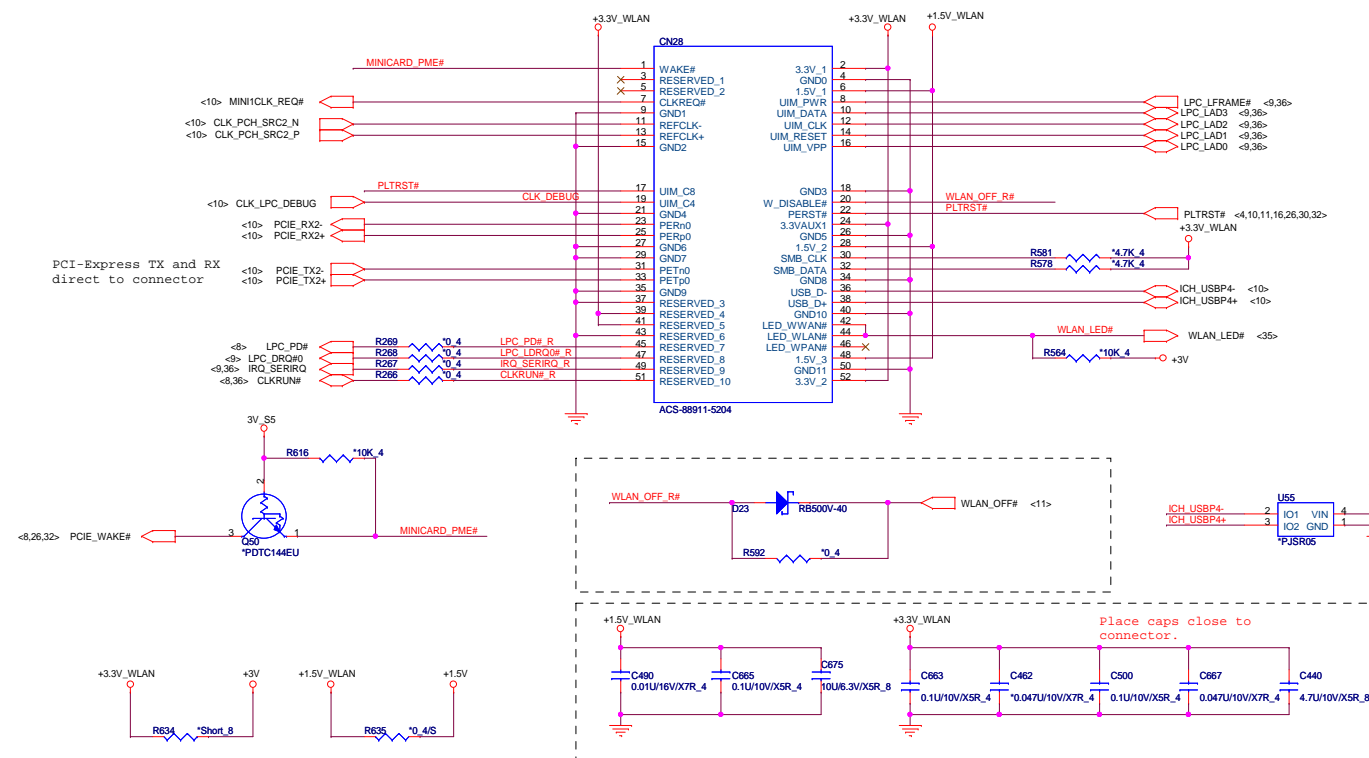


BLUETOOTH

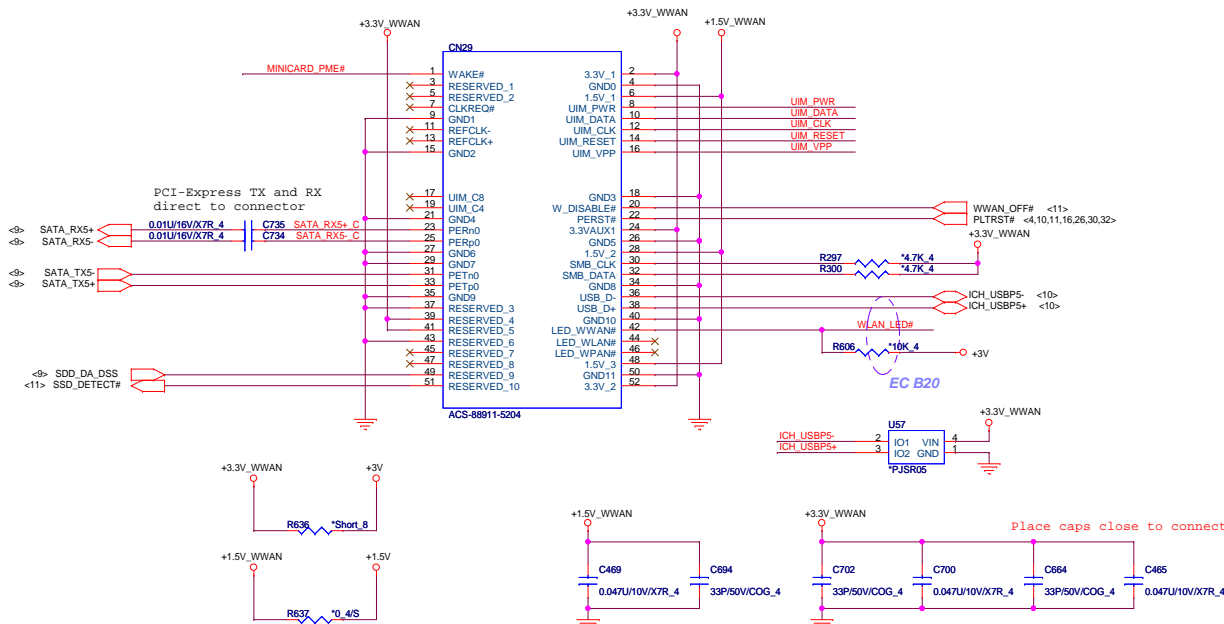




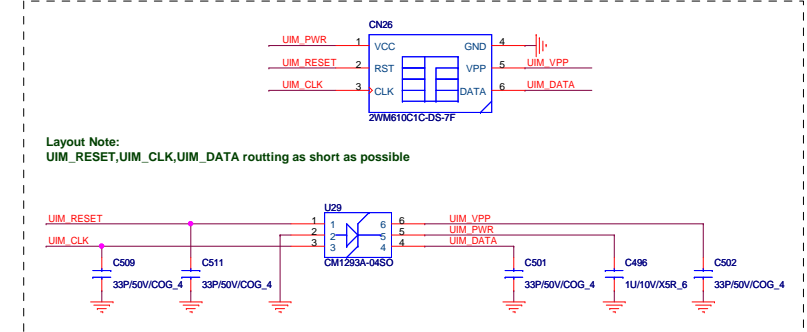
MiniCard WLA connector



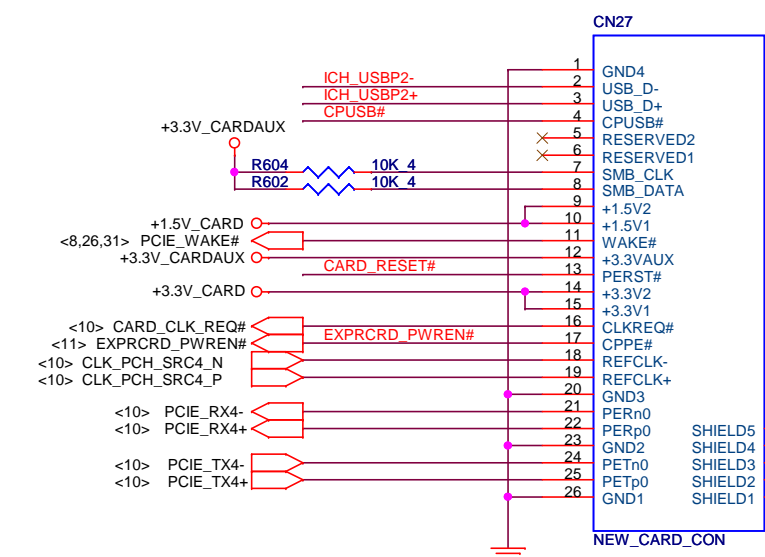
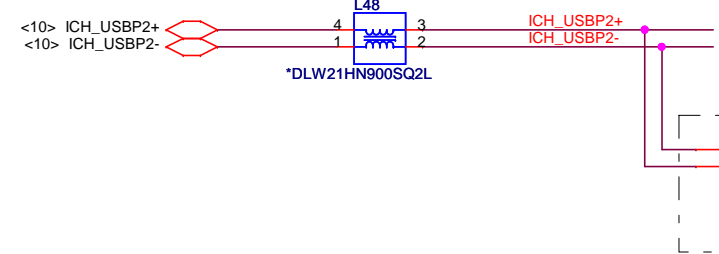
MiniCard WWAN/SATA SSD connector



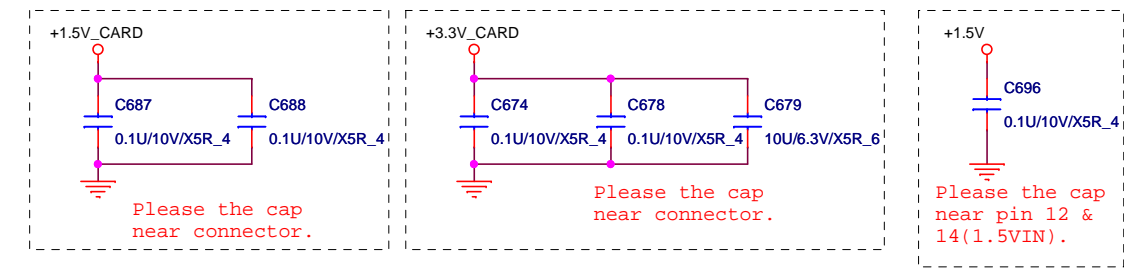
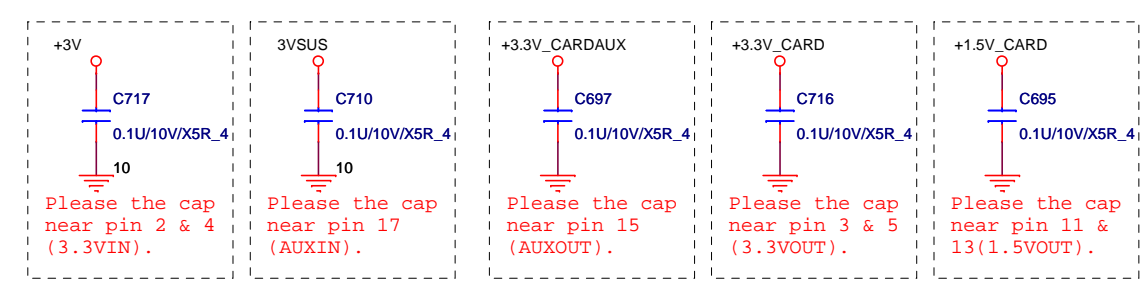
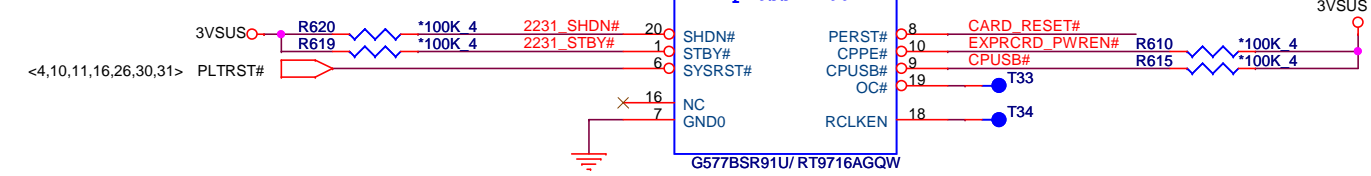
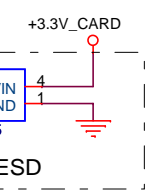
SIM Card CONN



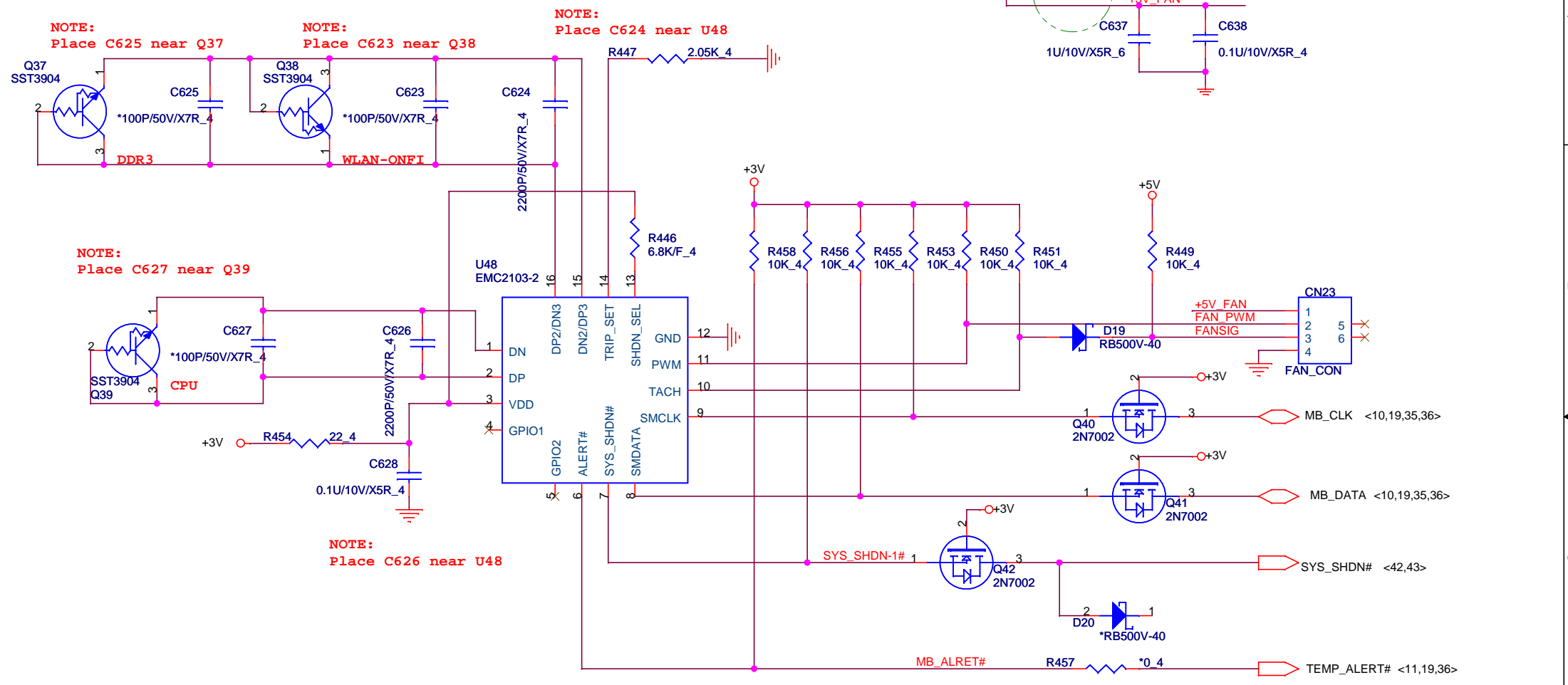
Express Card



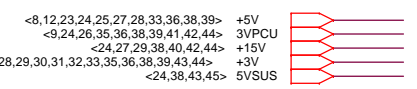
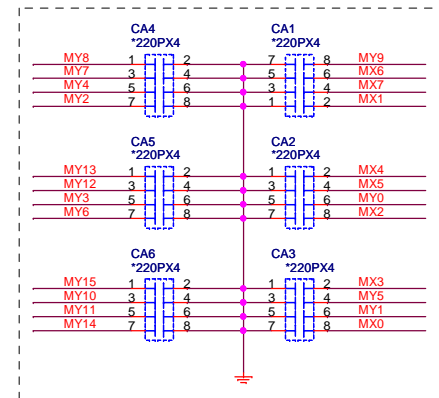
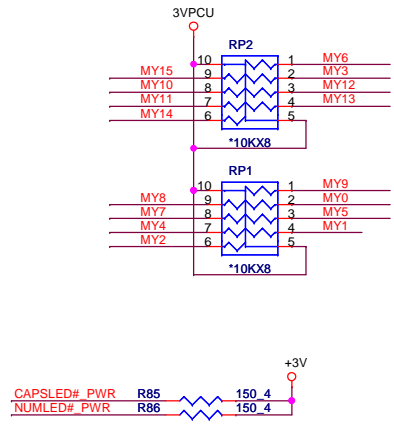
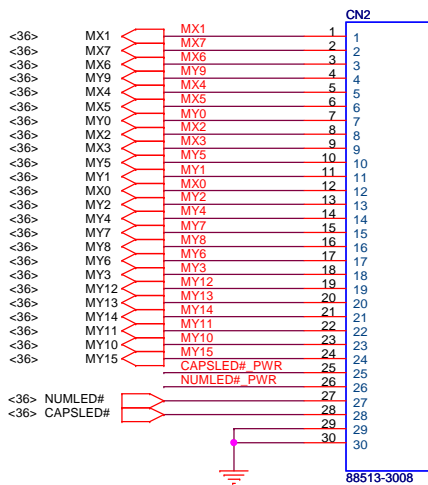
PCI-Express TX and RX direct to connector.
JAE PX10FS16PH-26P



FAN CONTROL

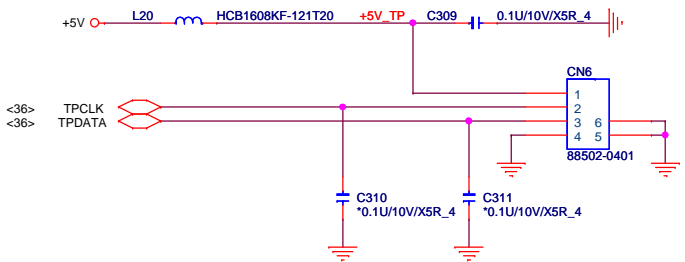


KEYBOARD

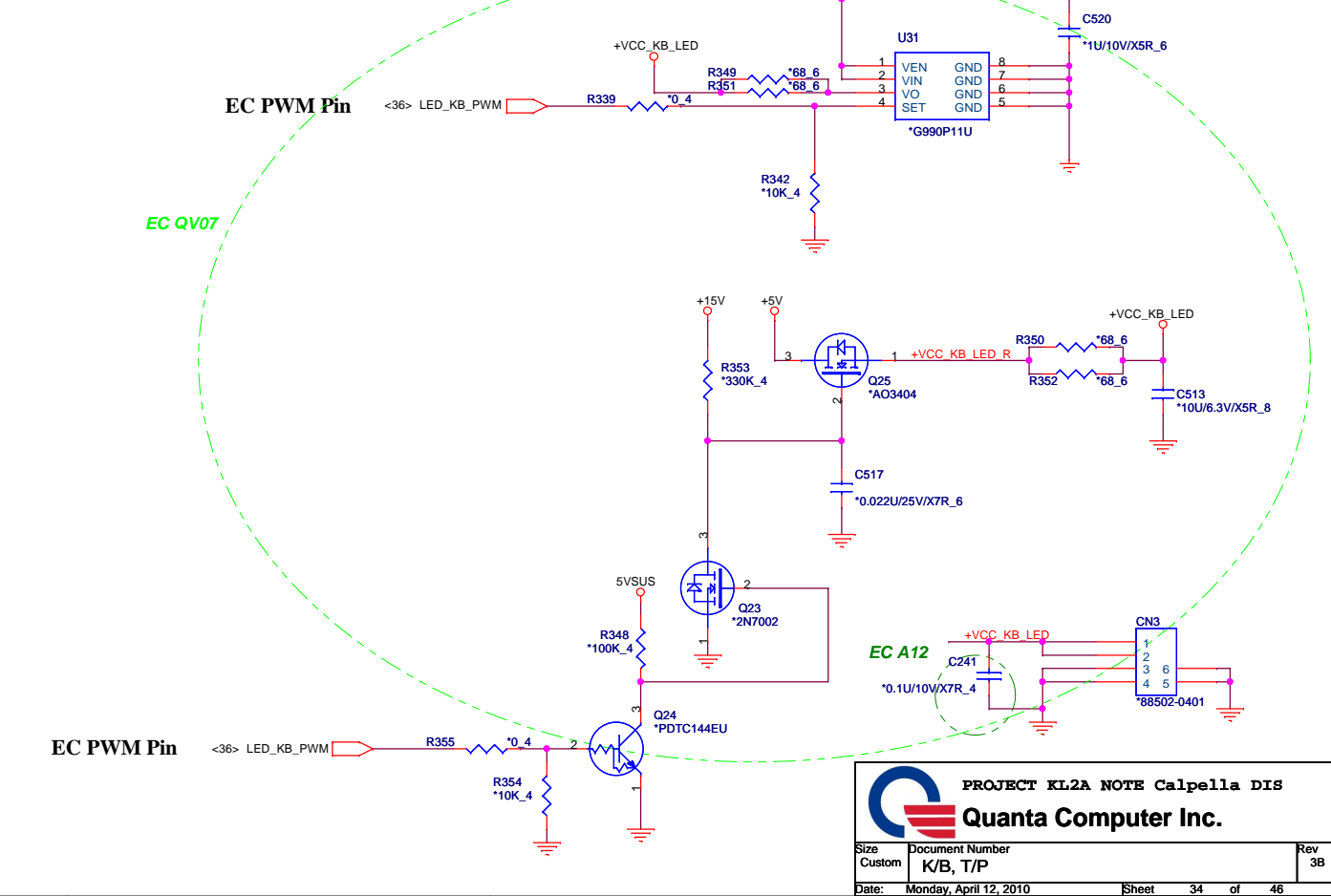


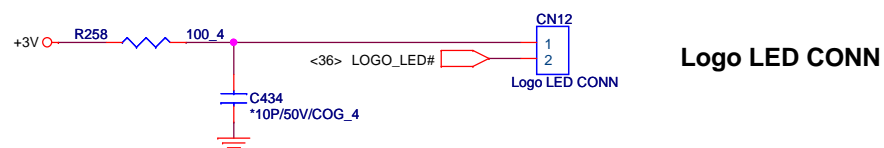
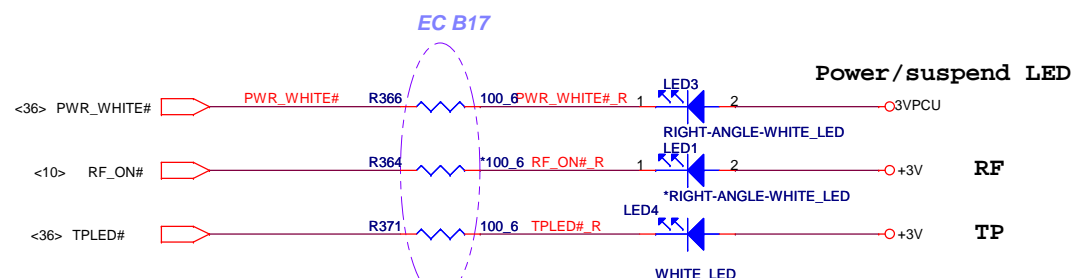
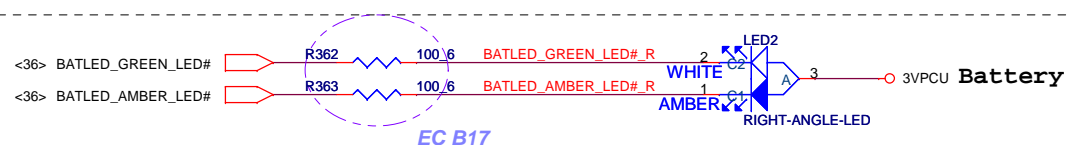
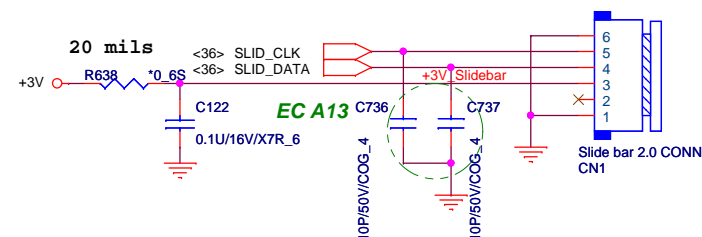
34

Touch pad

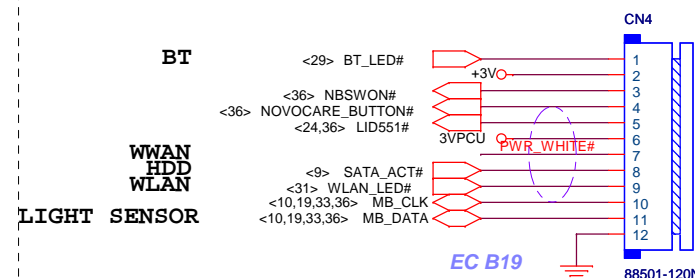


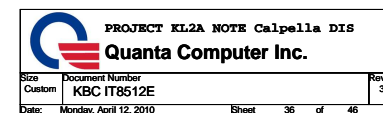
Backlight Keyboard Con.





POWER BOARD





MiniCard WLAN

HOLE28
H-TC197D79PT

HOLE30
H-TC197D79PT

MiniCard WWAN

HOLE29
H-TC197D79PT

HOLE31
H-TC197D79PT

Hole for PCH support

HOLE25
H-TC197D59PT

HOLE27
H-TC197D59PT

Drink Hole

ESD for ESATA

Hole for CPU support

HOLE4
*H-C142D142N

HOLE5
*H-C142D142N

HOLE7
*H-C142D142N

HOLE6
*h-bc142tc221d142pt

VGA nut

HOLE20
H-TC197BC138I102D102P2

HOLE22
H-TC197BC138I102D102P2

Bluetooth nut

Boundary Hole

HOLE1
*h-sd106p2-kl2

HOLE11
*H-C315I3146BO378D106P2

HOLE15
*H-C315I126D118N

HOLE18
*H-C315I126D106P2

HOLE19
*H-C315I126D106P2

HOLE13
*H-TC197BC256D106P2

HOLE17
*H-C315I126D106P2

HOLE16
*H-C315I126D106P2

HOLE14
*H-C118D118N

HOLE8
*H-TC197BC256D106P2

HOLE3
*H-C315I126D106P2

Boundary Hole

HOLE2
*H-TC197BC256D106P2

HOLE32
*O-KL2-1

HOLE33
*O-KL2-2

PAD

HOLE24
*SPAD-S79

HOLE26
*SPAD-S79

HOLE21
*SPAD-S83X71

HOLE23
*SPAD-S87X73

Break Hole

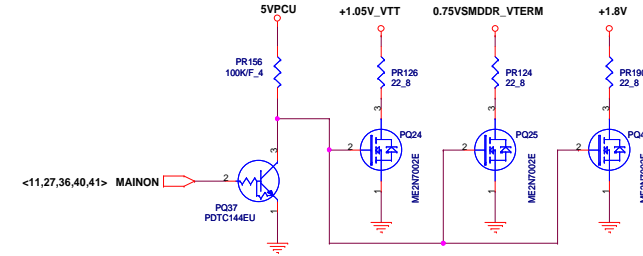
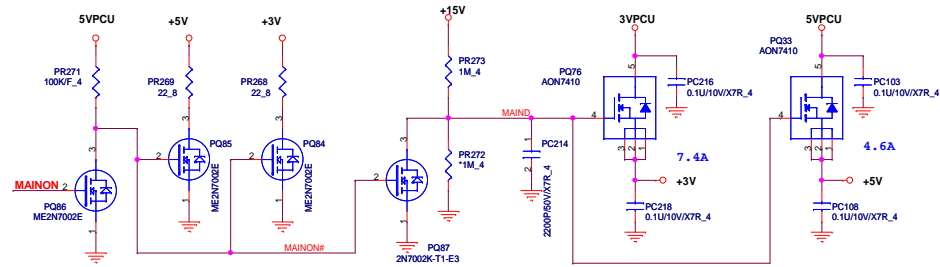
Boundary Hole (ODD)

HDD PAD
EC QV08

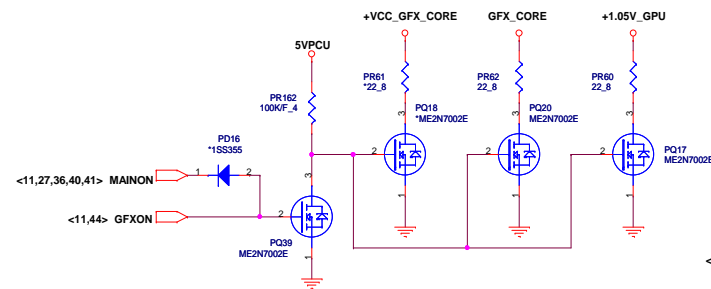
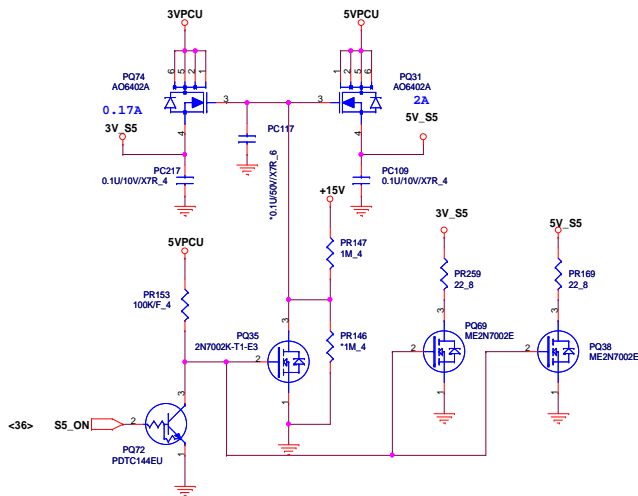
HOLE10
*H-O158X355D158X355N

DISCHARGE

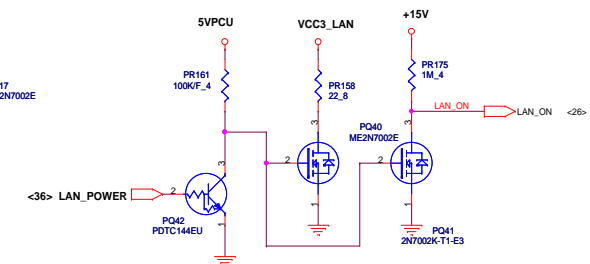
+3V, +5V



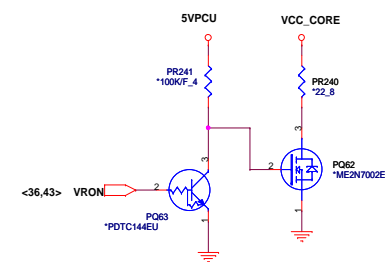
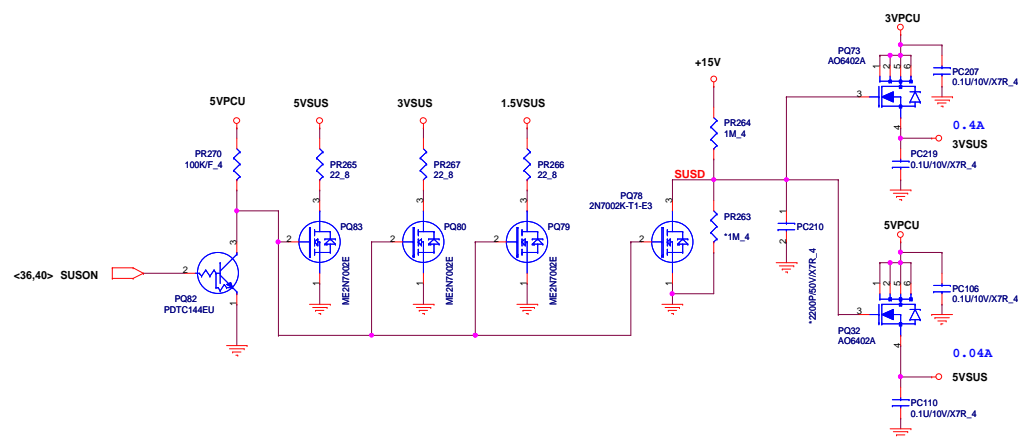
3V_S5, 5V_S5



LANVCC



3VSUS, 5VSUS



R138=0.02m ohm for 65W adapter-->current limit is 3A;

