ASUS CONFIDENTIAL

MODEL NAME : ***Elsa***

PCB NO : ***???***

ASUS P/N : ***???***

Lanai UMA Schematics Document

uFCPGA Mobile Merom
Intel Crestline-GM + ICH8M

2007-03-19

REV :1.2(DELL: X02)

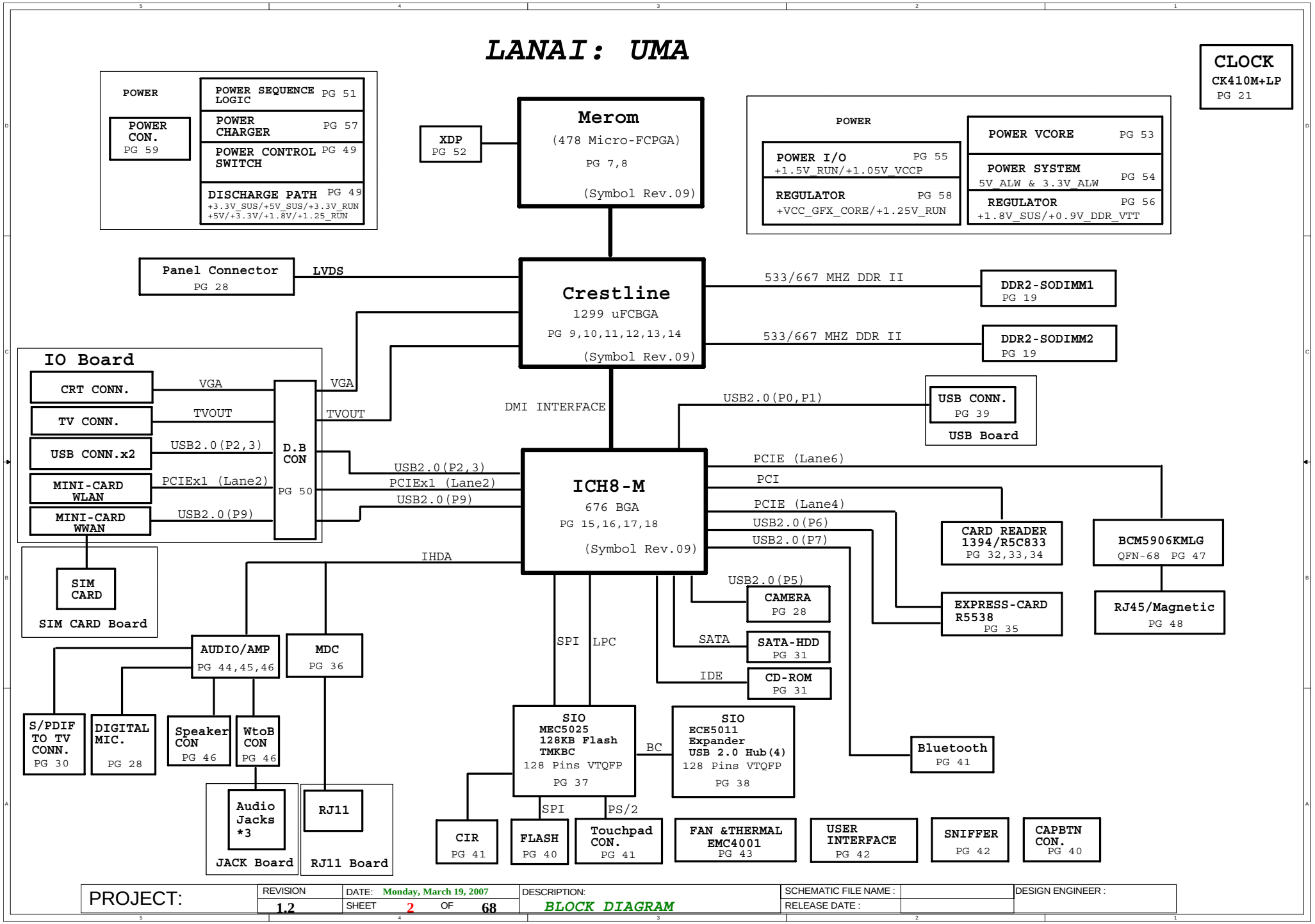
MB PCB

Part Number	Description
DA800004H0L	PCB 00B LA-3071P REV0 M/B

BOM NO. ???
PCB P/N: ???

PROJECT:	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET 1 OF 68	Cover Page	RELEASE DATE :	

LANAI: UMA



PROJECT:	REVISION 1.2	DATE: Monday, March 19, 2007 SHEET 2 OF 68	DESCRIPTION: BLOCK DIAGRAM	SCHEMATIC FILE NAME : RELEASE DATE :	DESIGN ENGINEER :

INDEX

Pg#	Description	DNI LIST
01	Cover Page	
02	Schematic Block Diagram	
03	INDEX	
04	Bus connection	
05	SMBUS BLOCK	
06	Power Rail	
07-08	CPU (Merom 、 Penryn)	
09-14	Crestline	
15-18	ICH8M	
19-20	DDRII SO-DIMM(533MHz 、 667MHz)	
21	Clock Generator (CK410M+LP)	
22-27	BLANK PAGE	
28	LVDS CON & Camera & DMIC	
29	RGB CON	
30	TV OUT CON	
31	SATA(HDD & CD_ROM)	
32-34	MEDIA CARD READER / 1394 (R5C833)	
35	PCI-Express Card	
36	MDC CONN	
37	EC (MEC5025)	
38	SIO (ECE5011)	
39	USB PORT x 2	
40	FLASH & RTC & CAPBTN CONN	
41	TOUCH PAD & BT & CIR & LID	
42	SWITCH & LED	
43	HARDWARE MONITOR (EMC4001)	
44-46	AUDIO CODEC & AMP	
47	LOM BCM5906	
48	Magnetics and RJ-45	
49	Power Control Switch	
50	BtoB CON	
51	Power Sequence Logic	
52	XDP	
53-59	Power Circuit	
60	SCREW PAD	
61	Change List 1	
62	Change List 2	

Pg#	Description	DNI LIST
63	POWER CIRCUIT CHANGE LIST	
64	Modem board cover page	
65	RJ-11 CONN	
66	Modem board change List	
67	USB board cover page	
68	USB PORT (SINGLE * 2)	

Footprint Definition

Resistor	Footprint is 0402 if there is no description
Capacitor	Footprint is 0402 if there is no description
Ferrite Bead	Footprint is 0603 if there is no description

Layout Note

For all of ESD diode, they should be placed as close as possible to connectors and the signals from connectors should be routed to ESD diodes first. There is no branch or via before diodes

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	PCI_AD17	PCI_REQ1# PCI_GNT1#	PCI_PIRQC# PCI_PIRQD#

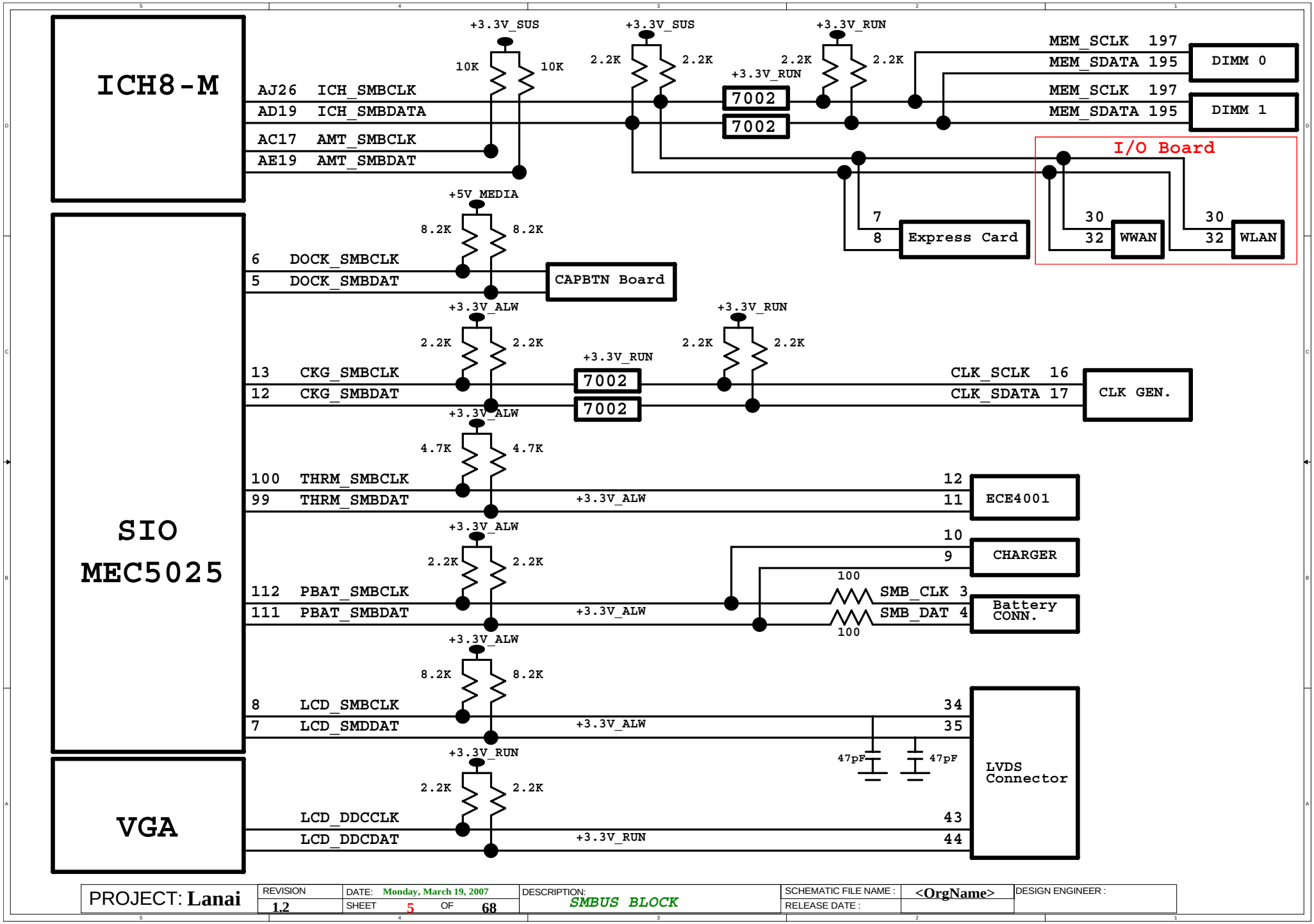
PCI Express TABLE

Lane 1	WWAN / Mini Card
Lane 2	WLAN / Mini Card
Lane 3	
Lane 4	ExpressCard
Lane 5	
Lane 6	LAN BCM5906KMLG

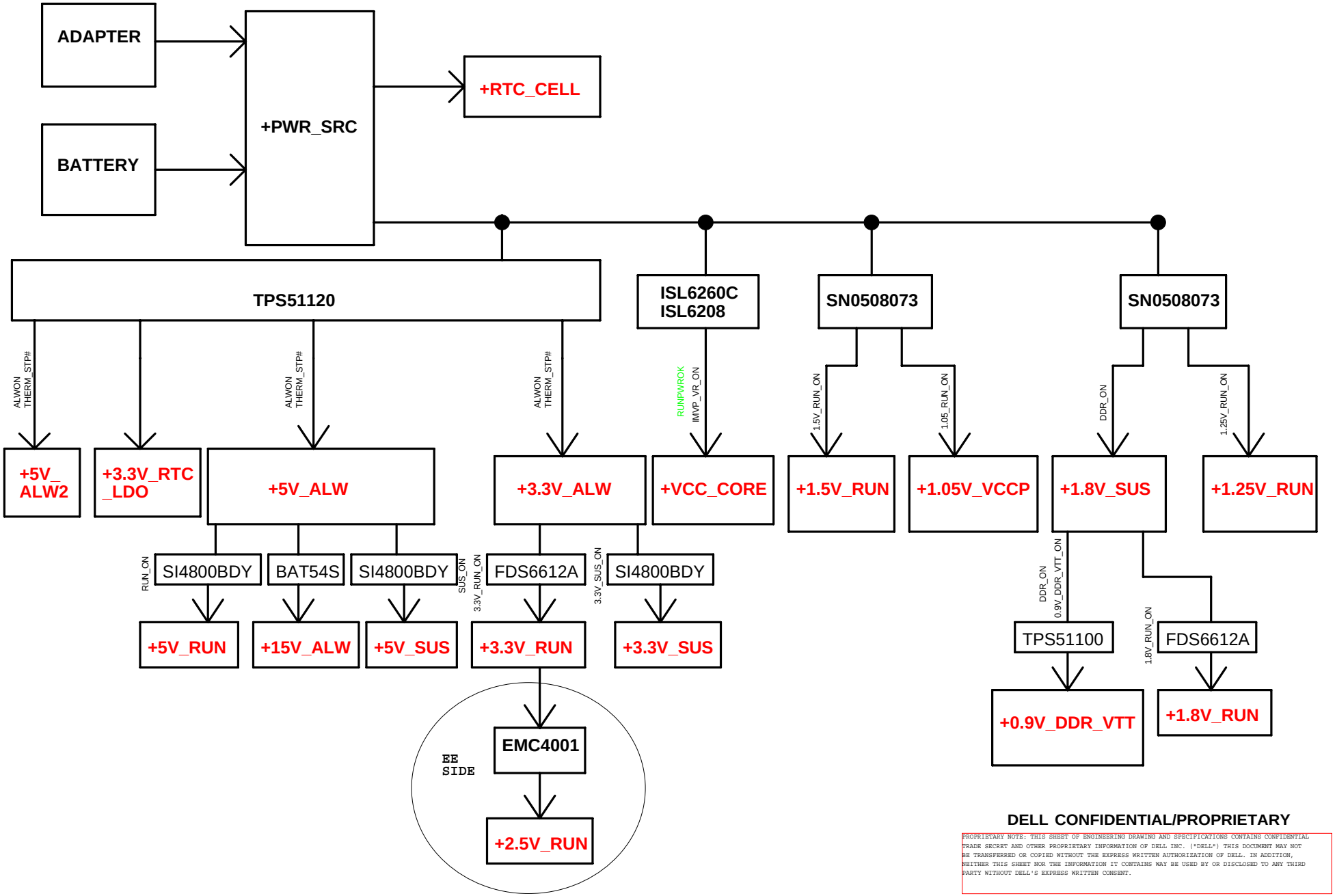
USB TABLE

ICH8-0 (EHCI#1)	User1 (Single port , in USB BD)
ICH8-1 (EHCI#1)	User2 (Single port , in USB BD)
ICH8-2 (EHCI#1)	User3 (Dual port-bottom , in I/O BD)
ICH8-3 (EHCI#1)	User4 (Dual port-top , in I/O BD)
ICH8-4 (EHCI#1)	
ICH8-5 (EHCI#1)	Camera
ICH8-6 (EHCI#2)	ExpressCard
ICH8-7 (EHCI#2)	BT Module
ICH8-8 (EHCI#2)	
ICH8-9 (EHCI#2)	WWAN / Mini Card

Note : No USB for WLAN

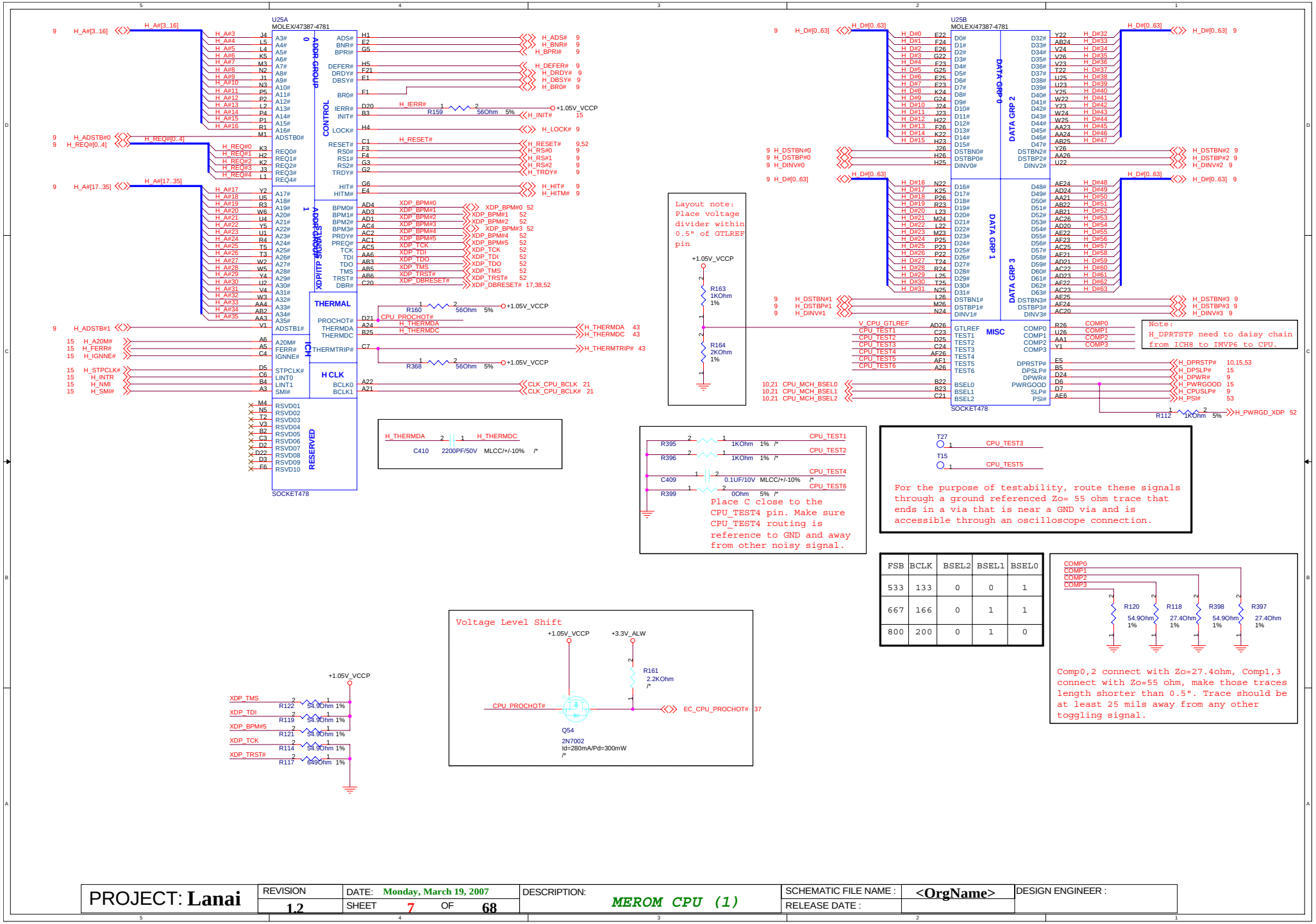


PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007 SHEET 5 OF 68	DESCRIPTION: SMBUS BLOCK	SCHEMATIC FILE NAME : RELEASE DATE :	<OrgName>	DESIGN ENGINEER :



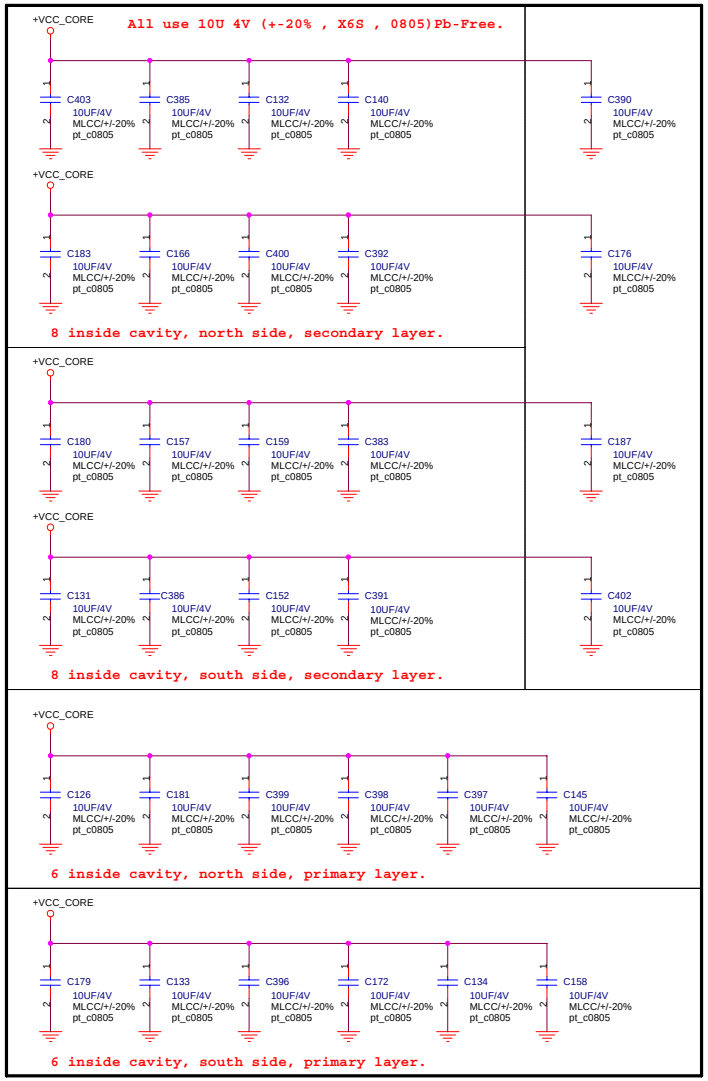
DELL CONFIDENTIAL/PROPRIETARY

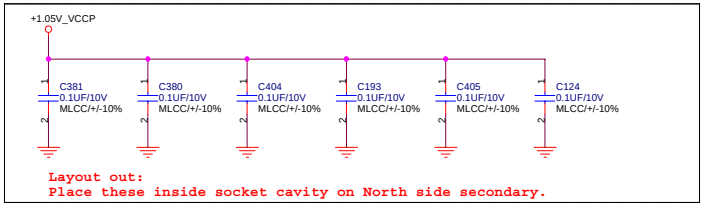
PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: Power Rail	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 6 OF 68		RELEASE DATE :	

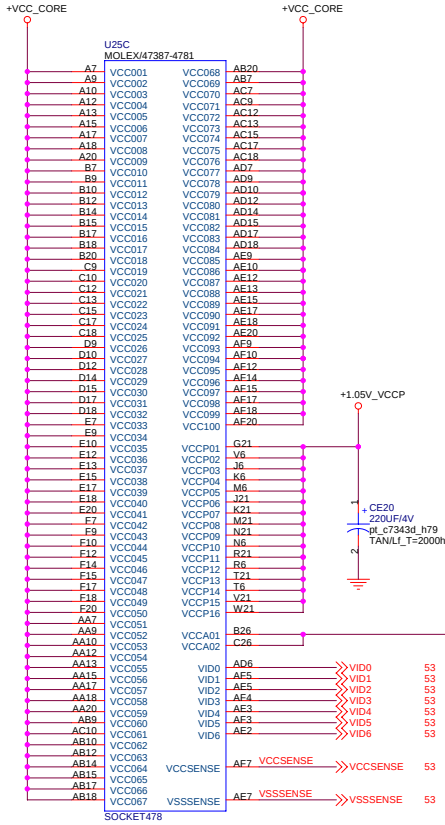


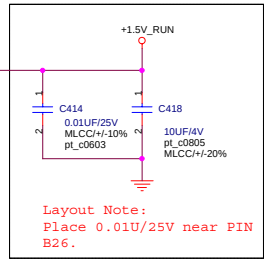
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

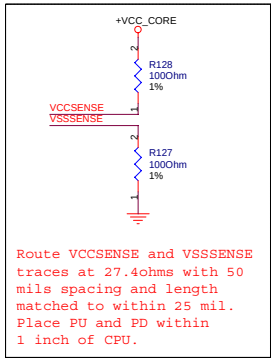
PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *MEROM CPU (1)*	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 7 OF 68		RELEASE DATE :	

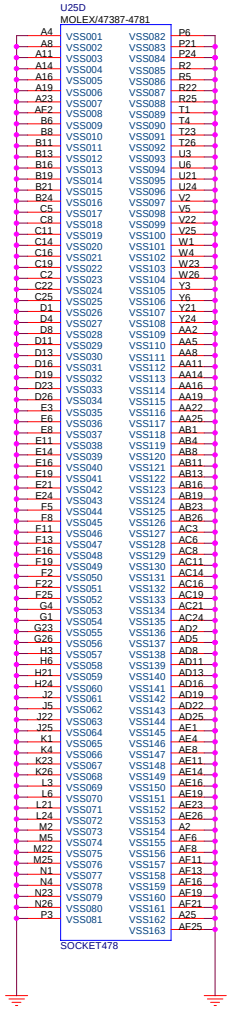




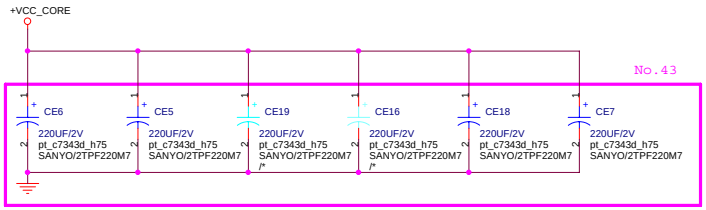




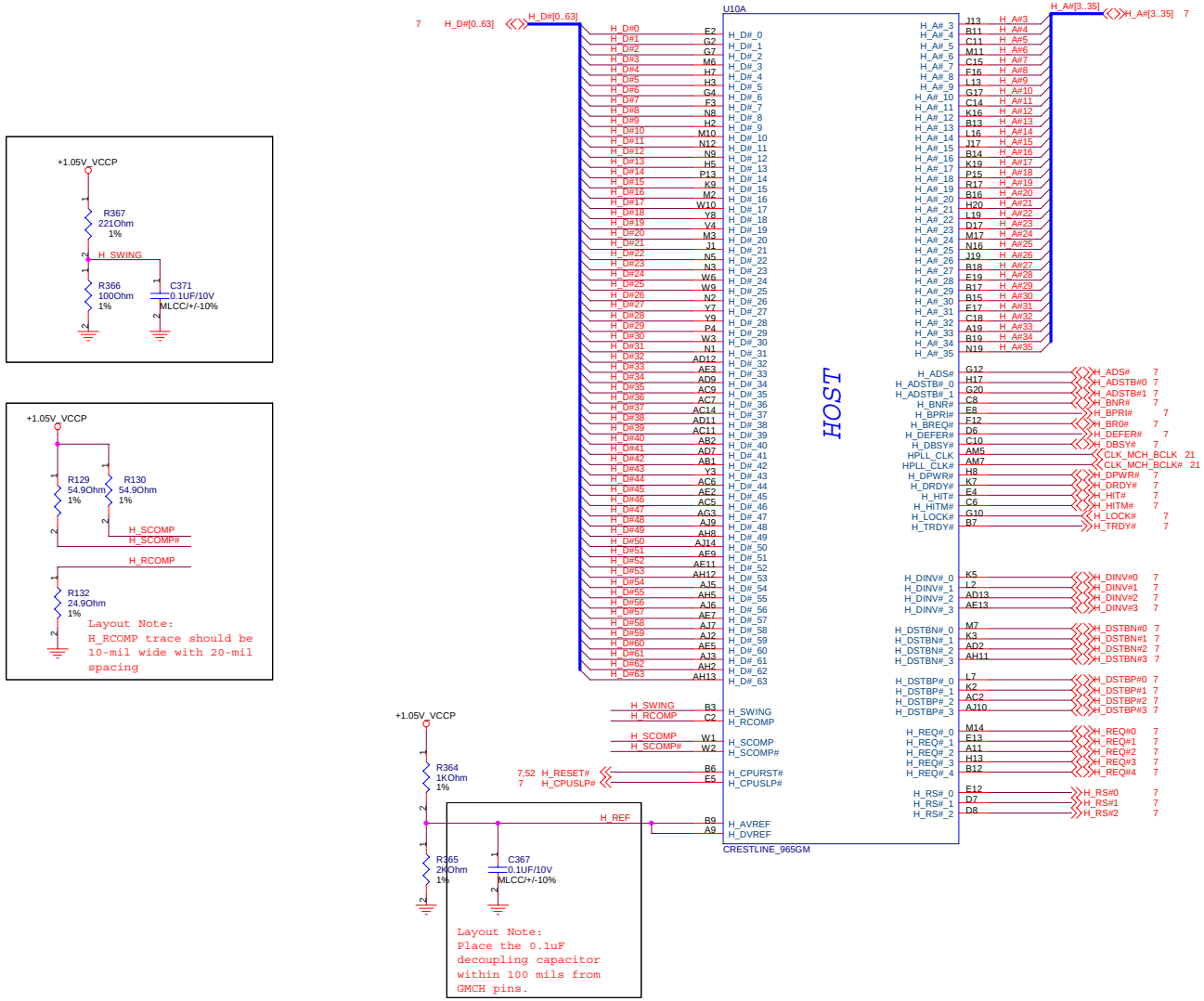




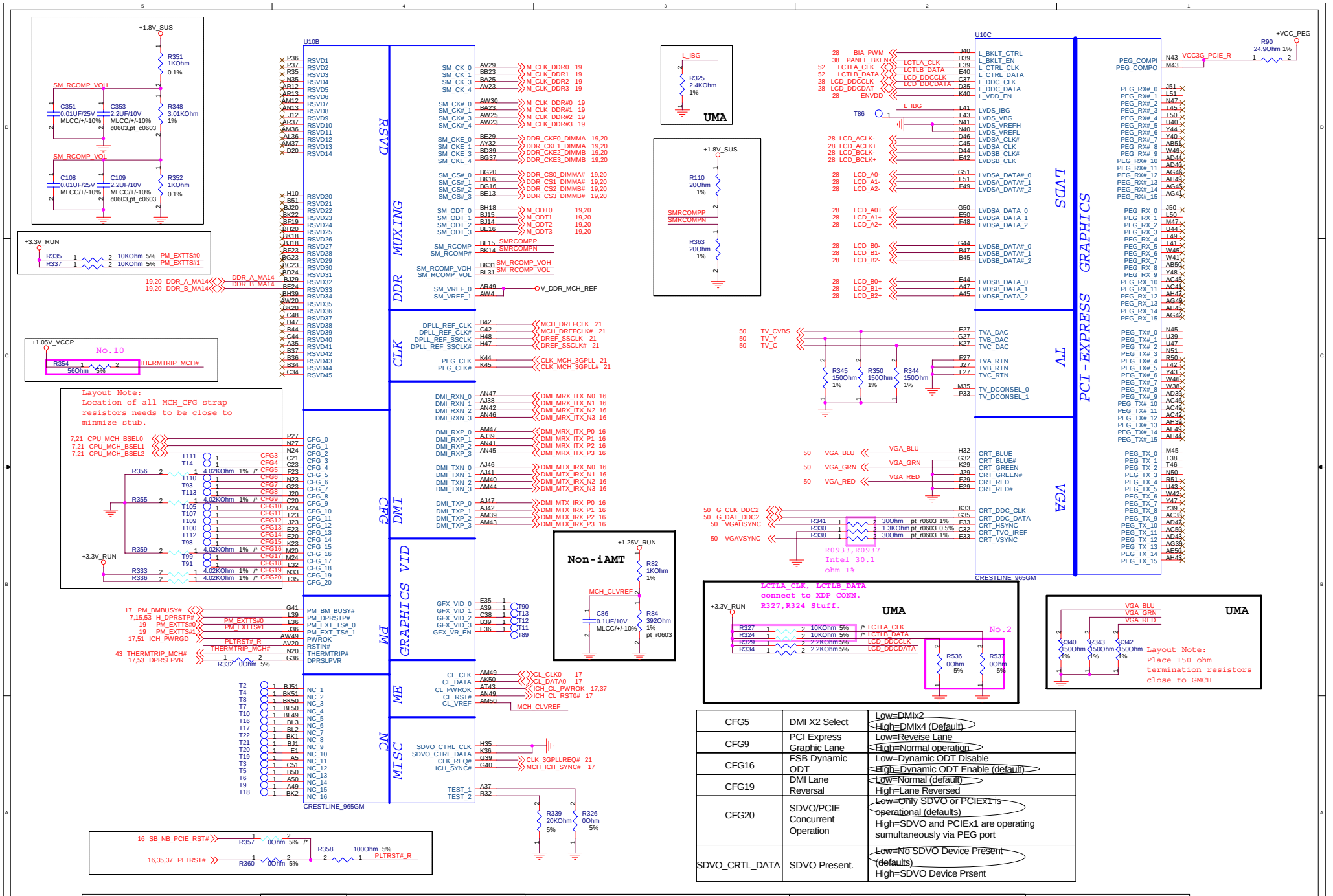
100U/25V *4 Remove to POWER CIRCUIT .



PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *Merom CPU (2)*	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 8 OF 68		RELEASE DATE :	

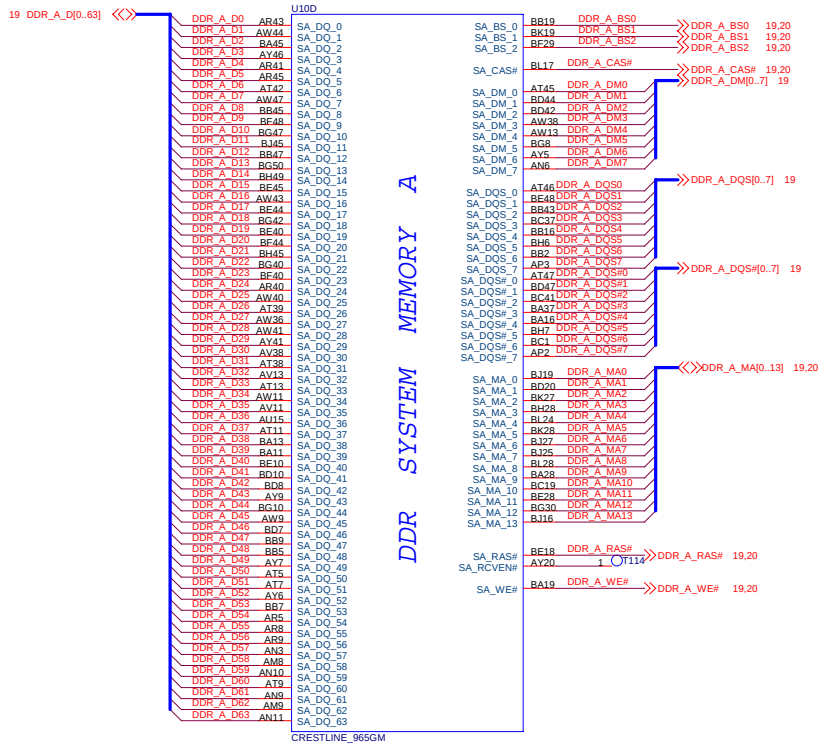


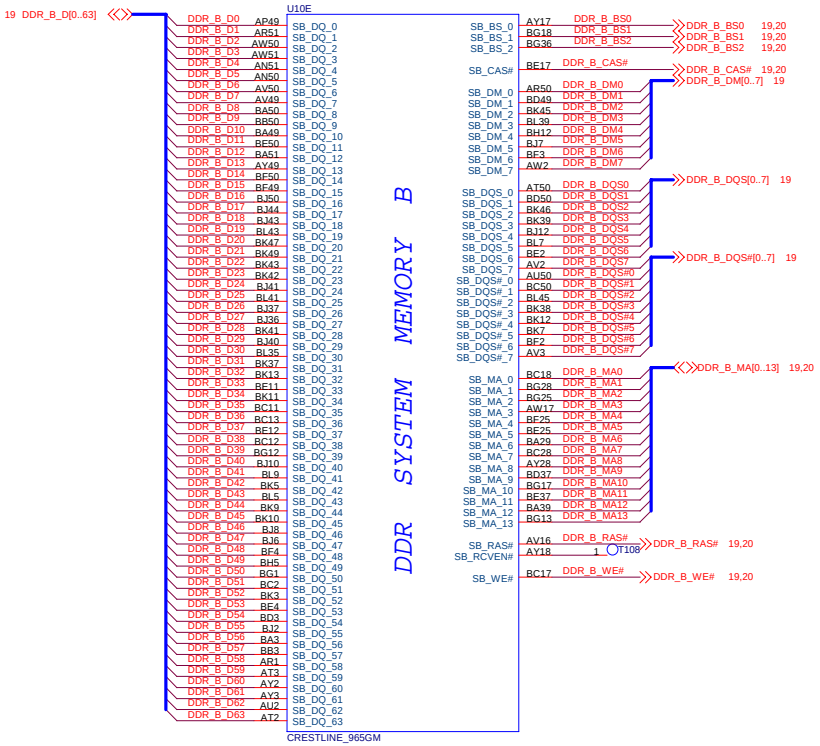
PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: Crestline(HOST)	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 9 OF 68		RELEASE DATE :	



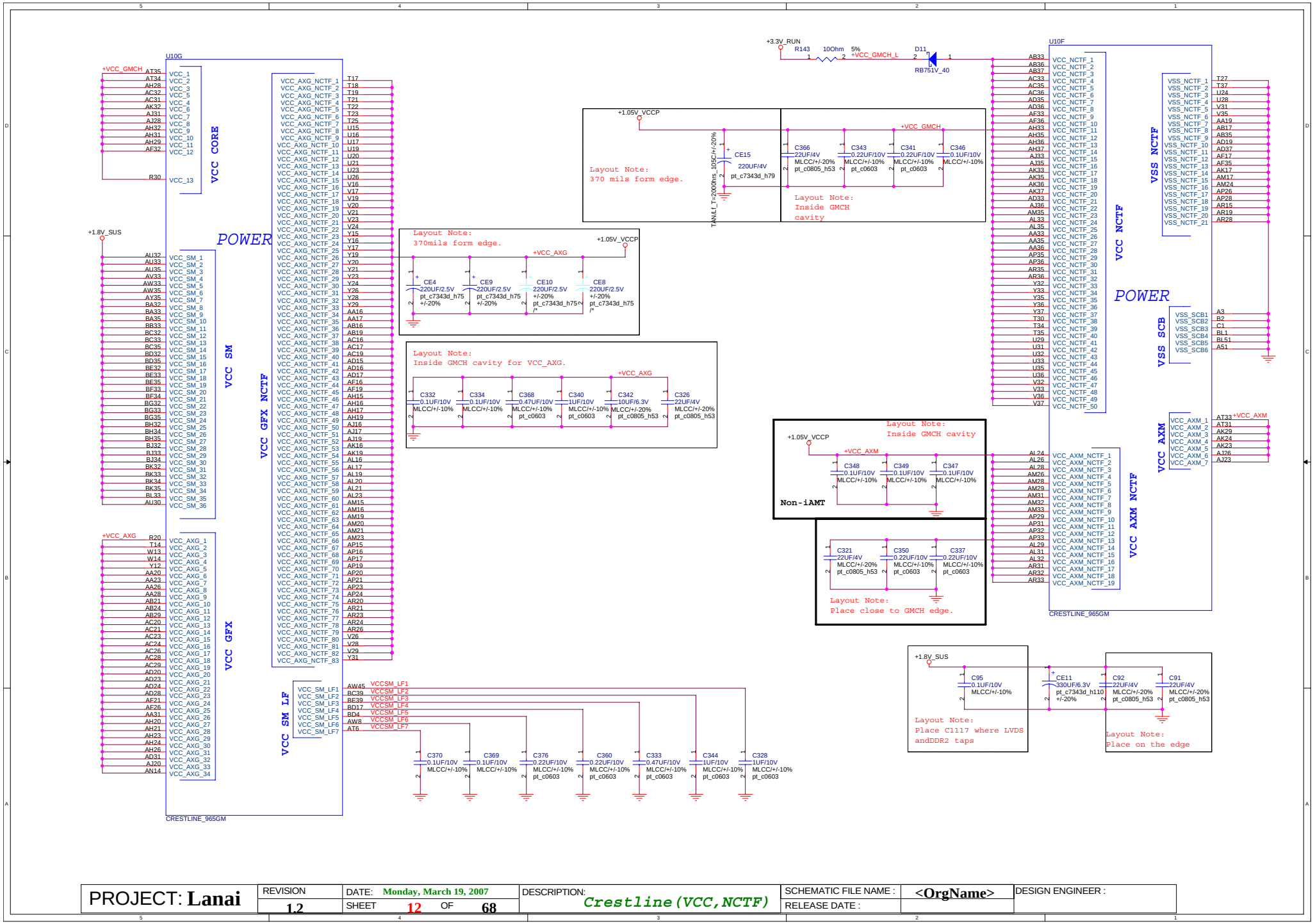
CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4 (Default)
CFG9	PCI Express Graphic Lane	Low=Reveise Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable (default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating sumultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present.	Low=No SDVO Device Present (defaults) High=SDVO Device Prsent

PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: Crestline(VGA,DMI)	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 10 OF 68		RELEASE DATE :	





PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: Crestline(DDR2)	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 11 OF 68		RELEASE DATE :		



PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *Crestline(VCC,NCTF)*	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
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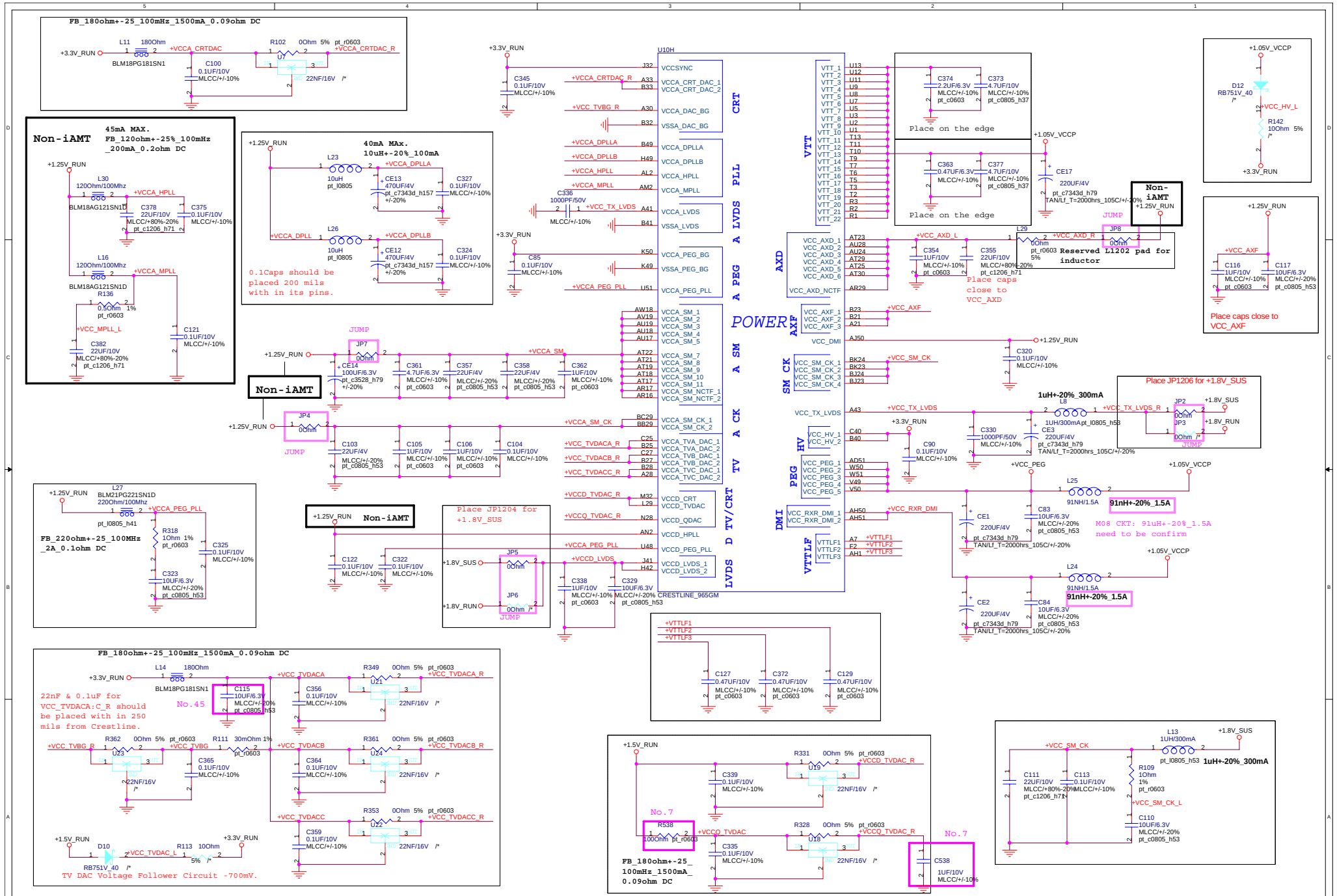
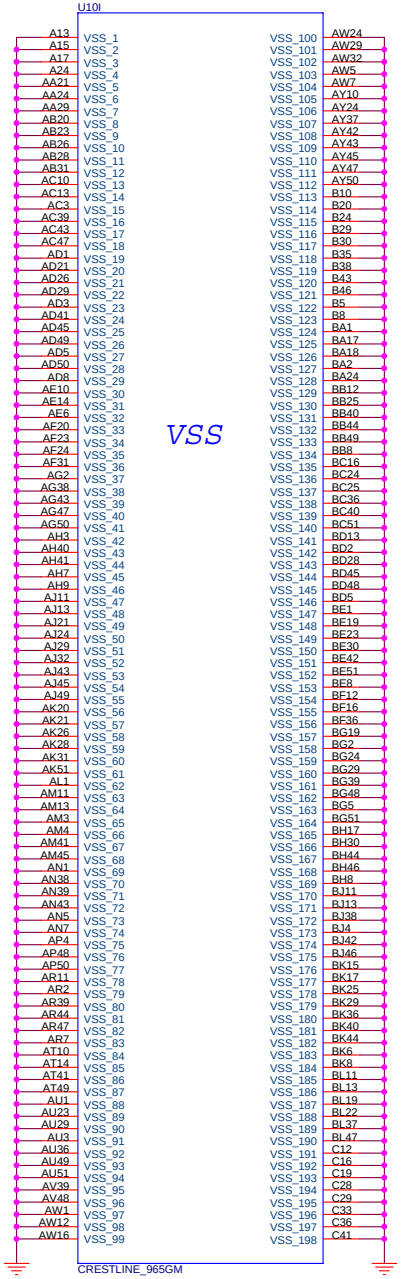
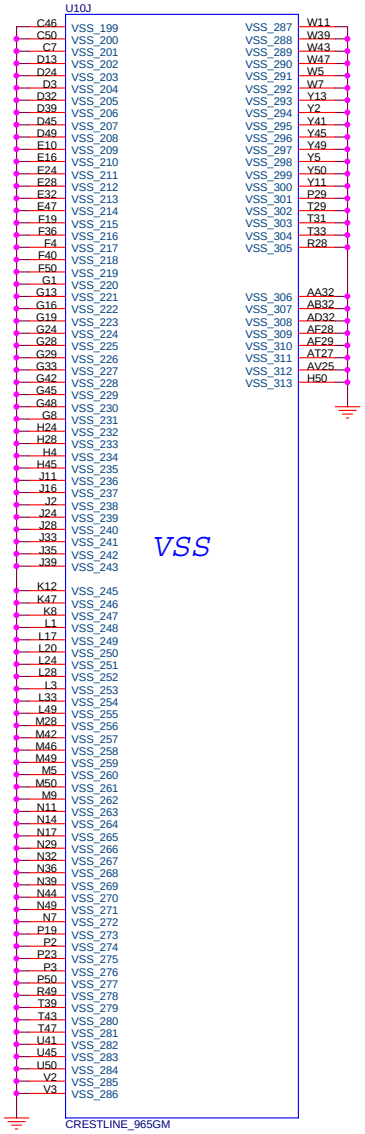
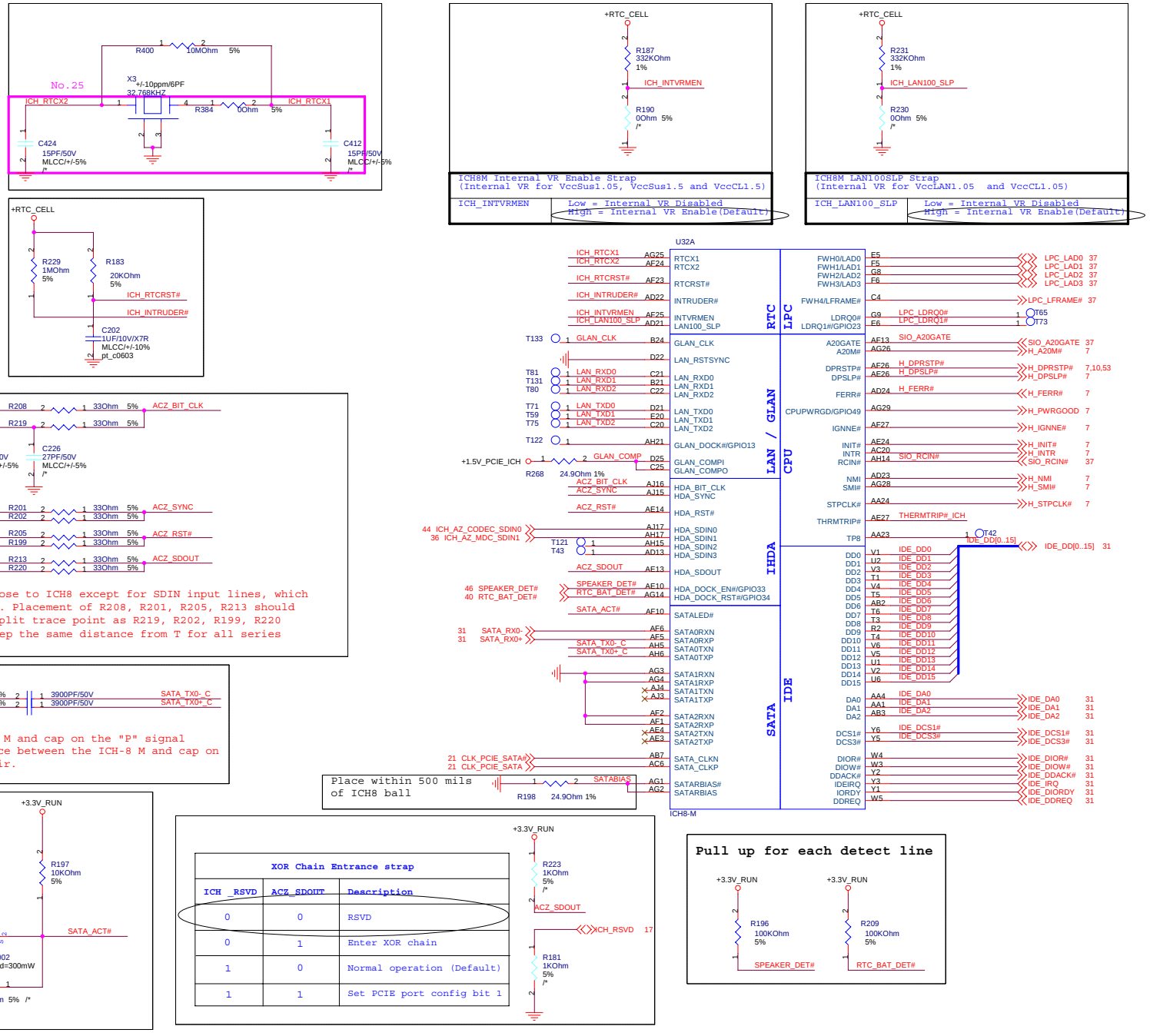


PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: Crestline(POWER)	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 13 OF 68		RELEASE DATE :		

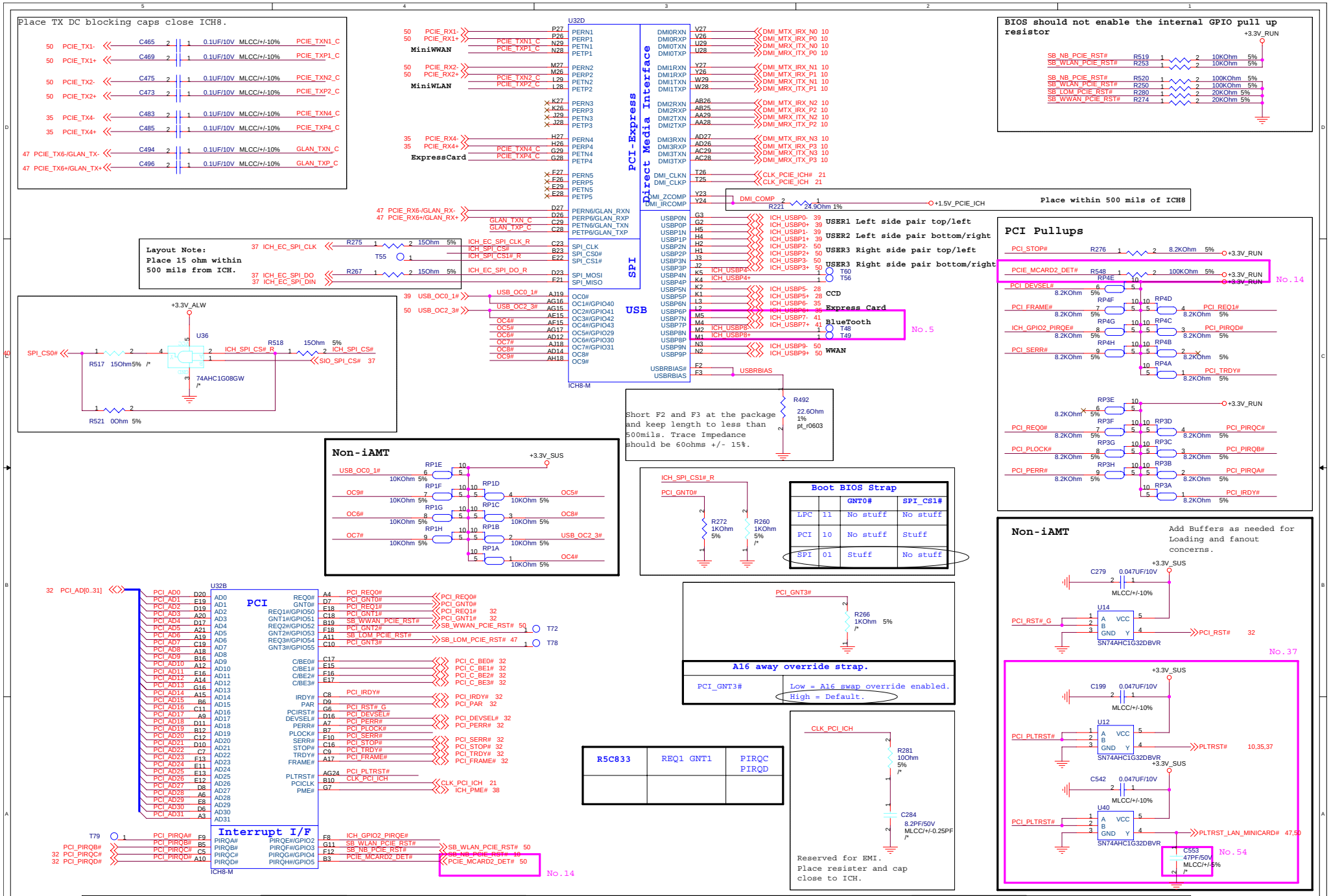




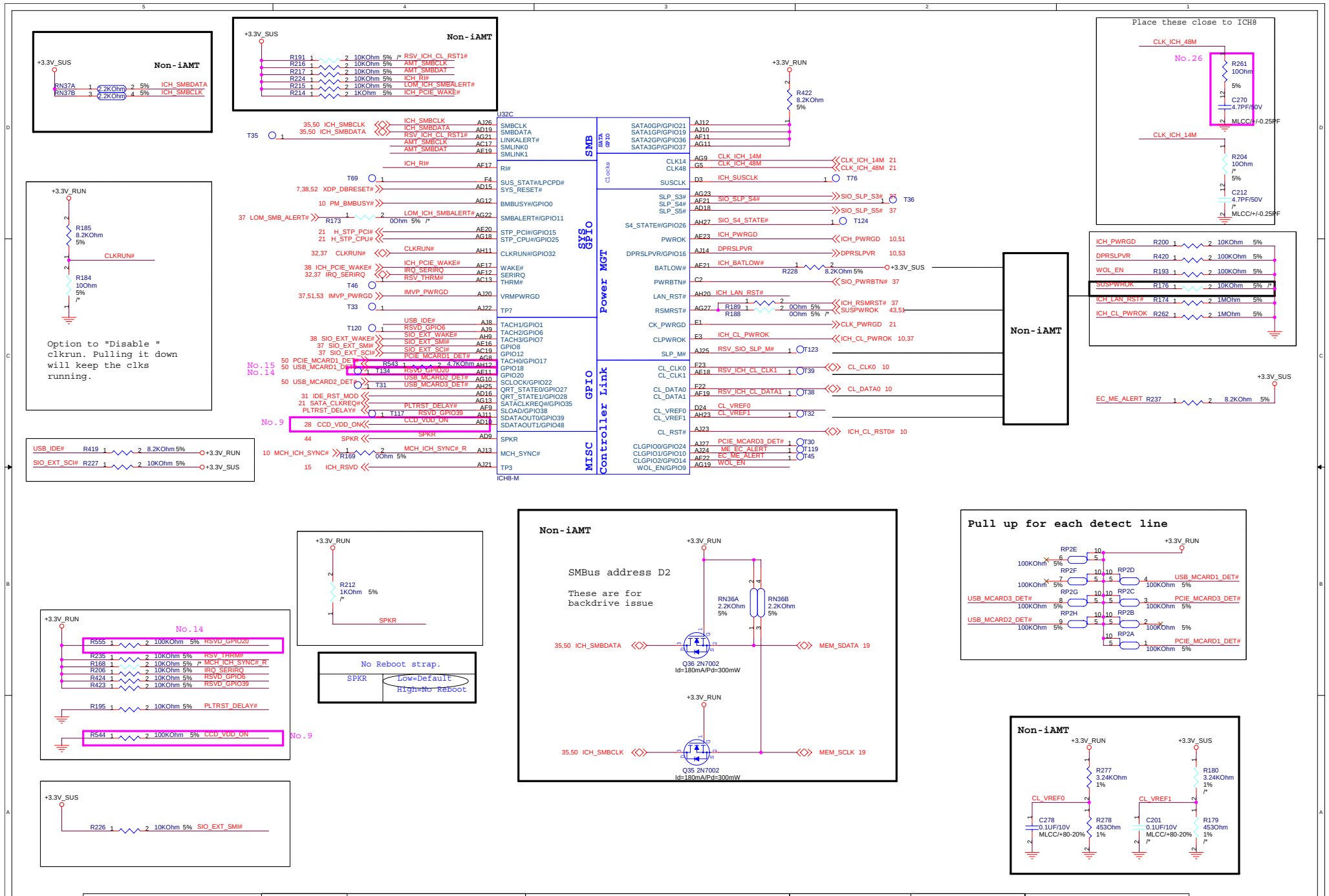
PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: *Crestline(VSS)*	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER :
		SHEET **14** OF **68**		RELEASE DATE :	



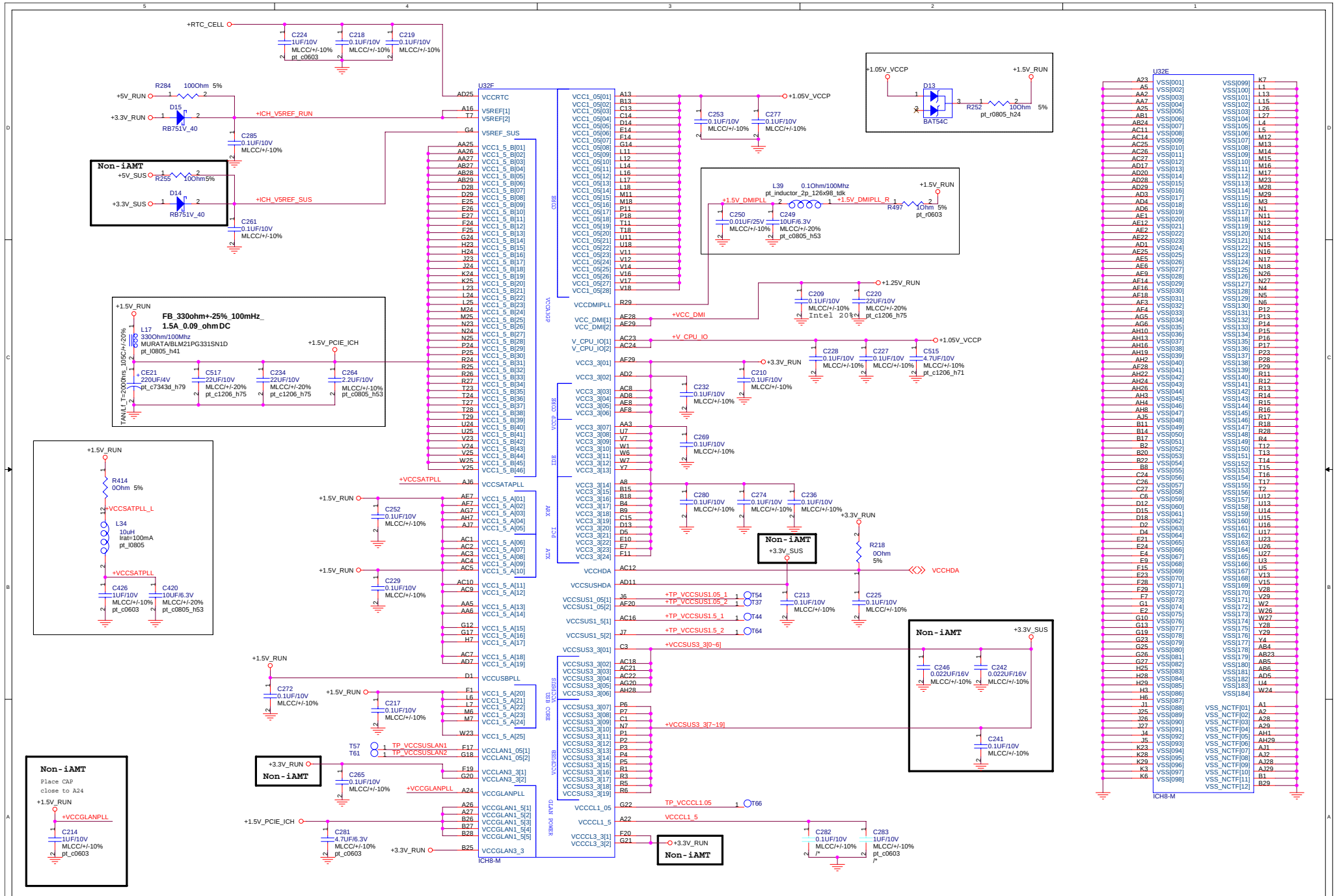
PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *ICH8: IDE/AC97/LPC/RTC*	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 15 OF 68		RELEASE DATE :		



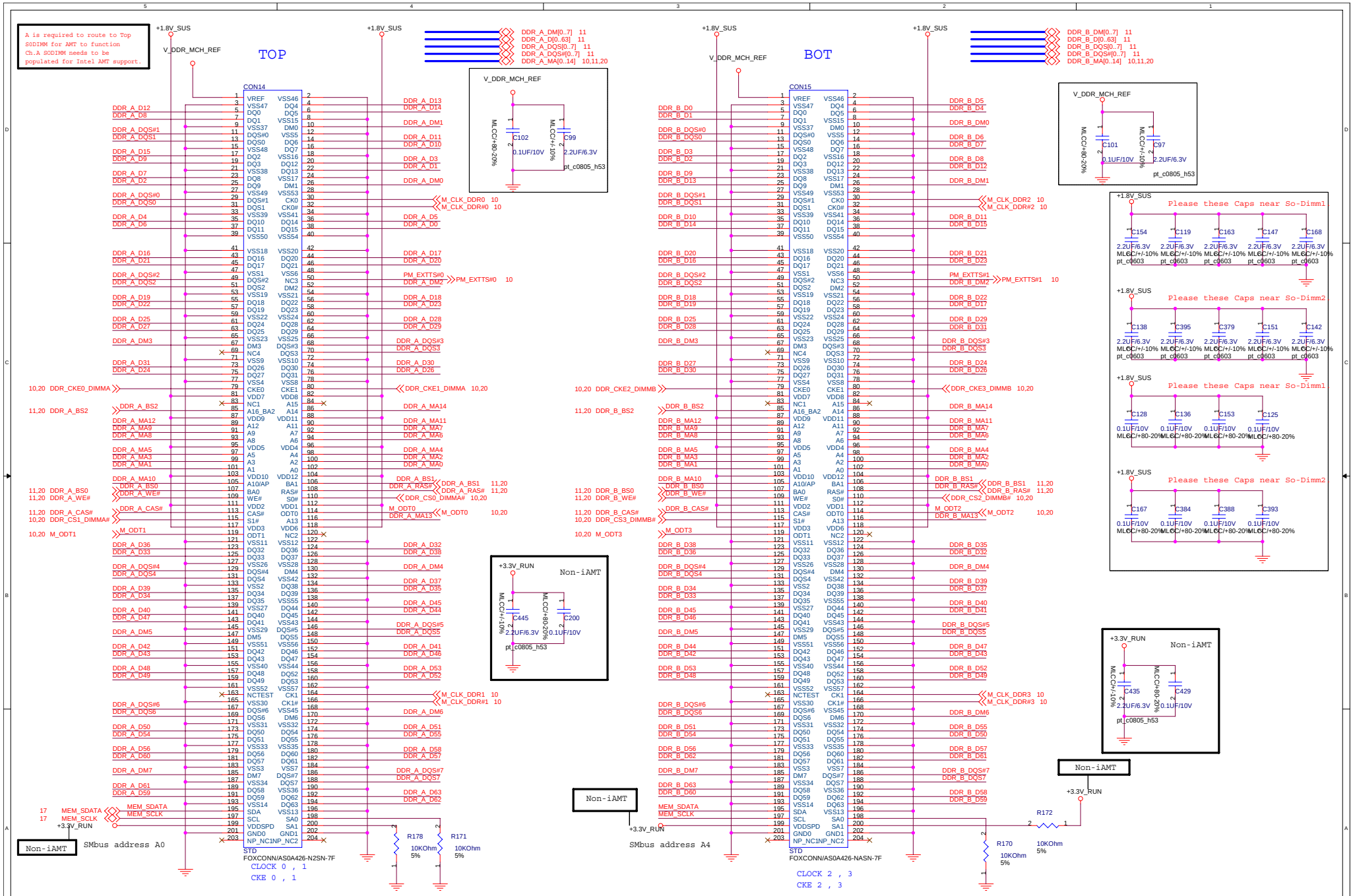
PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: ICH8: PCI/INT/DMI/USB	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 16 OF 68		RELEASE DATE :	



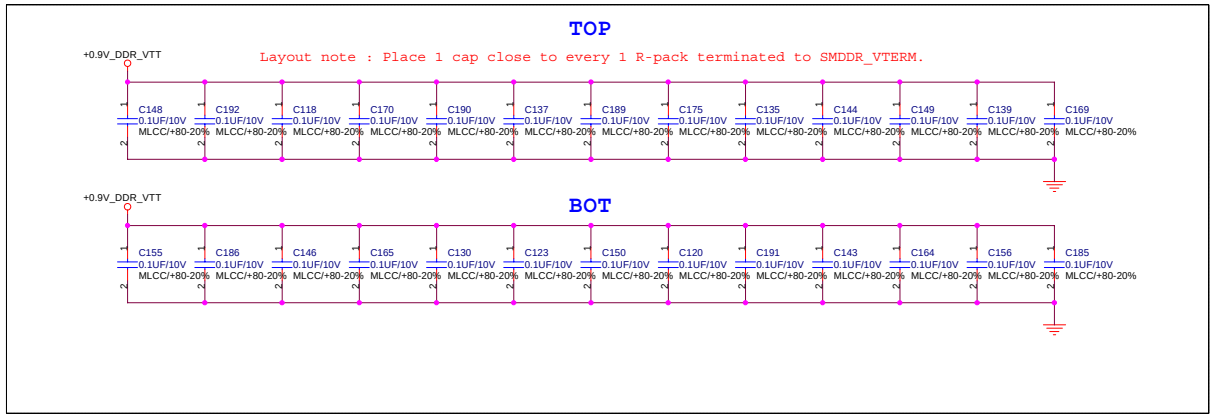
PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: ICH8: SMB/PWR/CLK/GPIO	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 17 OF 68		RELEASE DATE :	

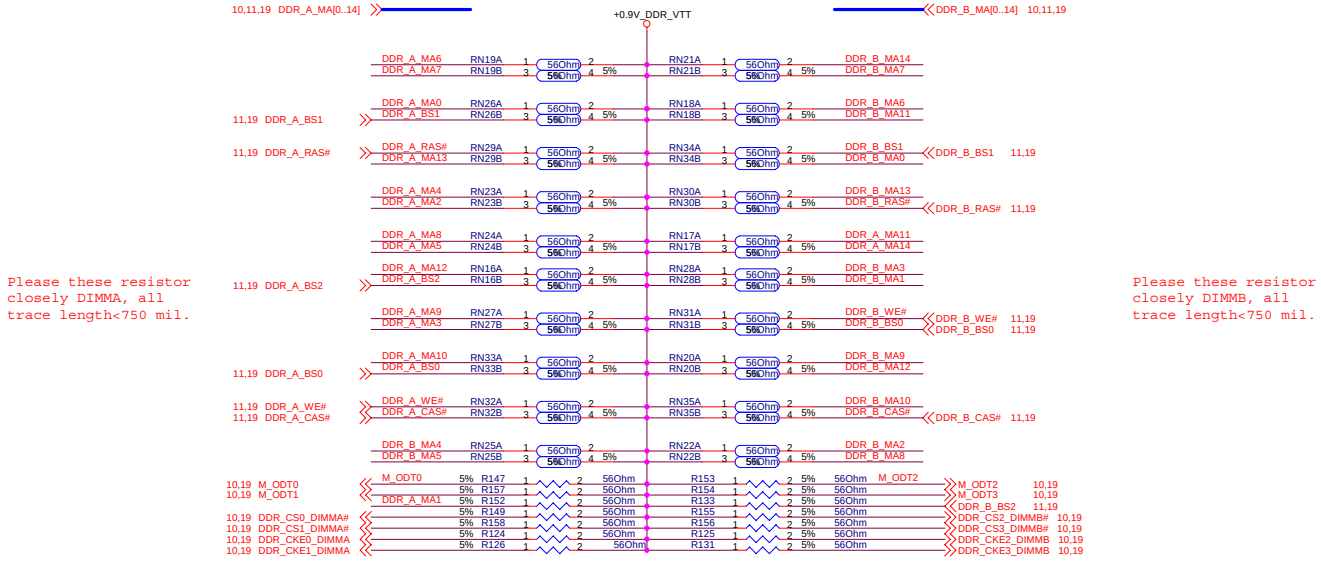


PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: ICH8-M(POWER,GND)	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 18 OF 68		RELEASE DATE :		



PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: DDR2 SO-DIMM (0)	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 19 OF 68		RELEASE DATE :	

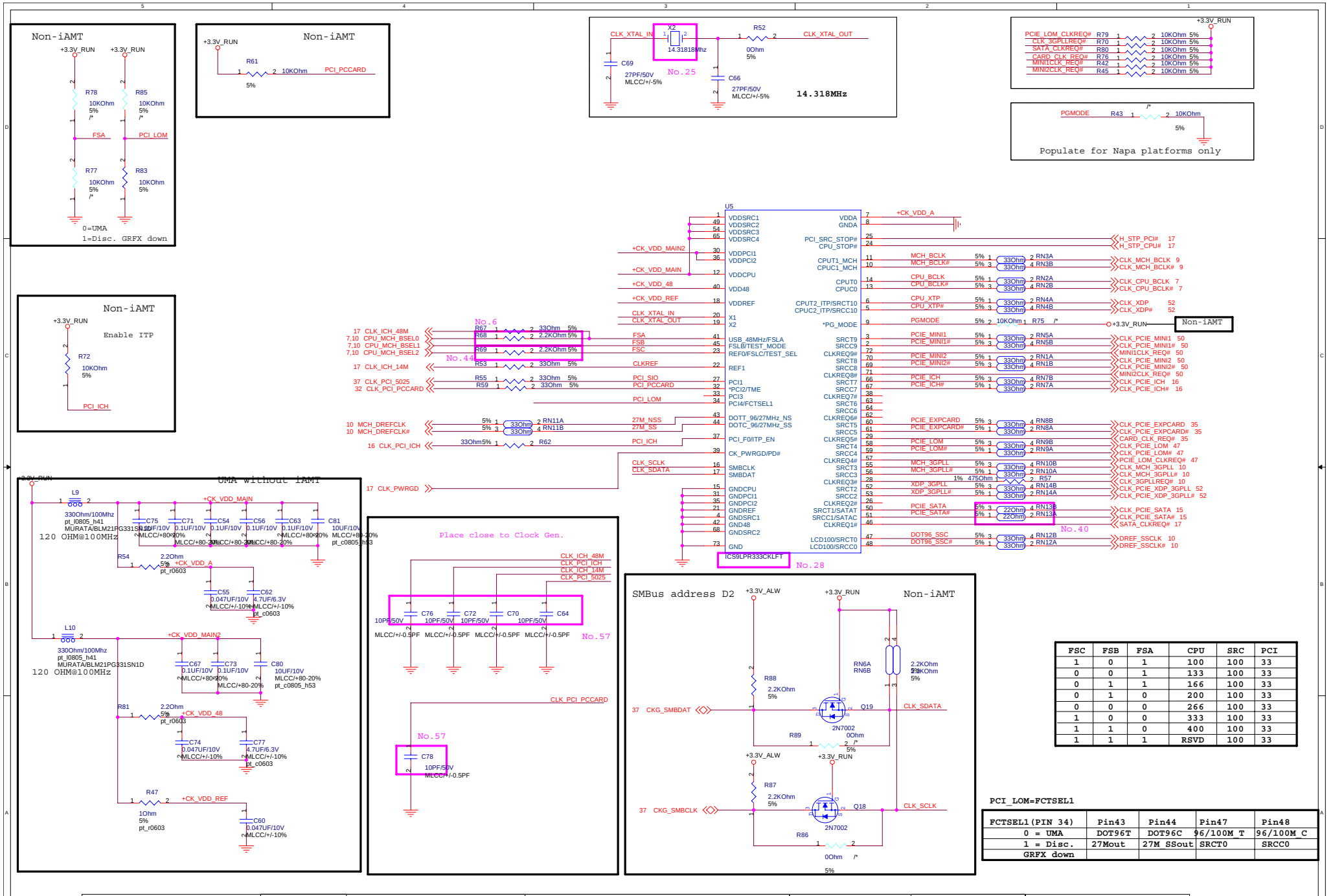




Please these resistor closely DIMMA, all trace length<750 mil.

Please these resistor closely DIMMB, all trace length<750 mil.

PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *DDR2 SO-DIMM (1)*	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 20 OF 68		RELEASE DATE :		



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PCI_LOM=FCTSEL1

FCTSEL1(PIN 34)	Pin43	Pin44	Pin47	Pin48
0 = UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc.	27Mout	27M_SSout	SRCT0	SRCC0
GRFX down				

PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: CLK GEN. CY28547	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 21 OF 68		RELEASE DATE :	

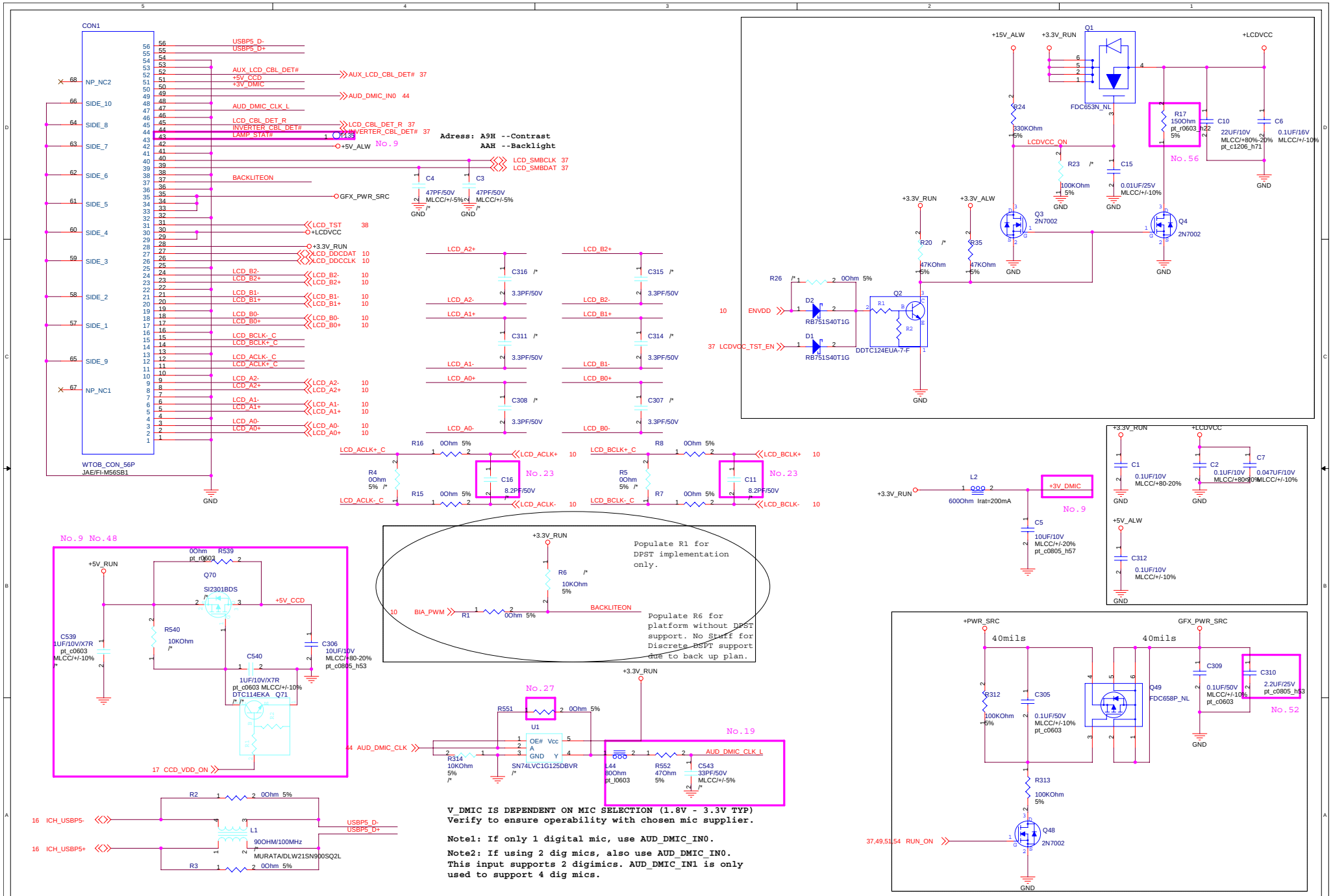
PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 23 OF 68		RELEASE DATE :		

PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 24 OF 68		RELEASE DATE :		

PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 25 OF 68		RELEASE DATE :		

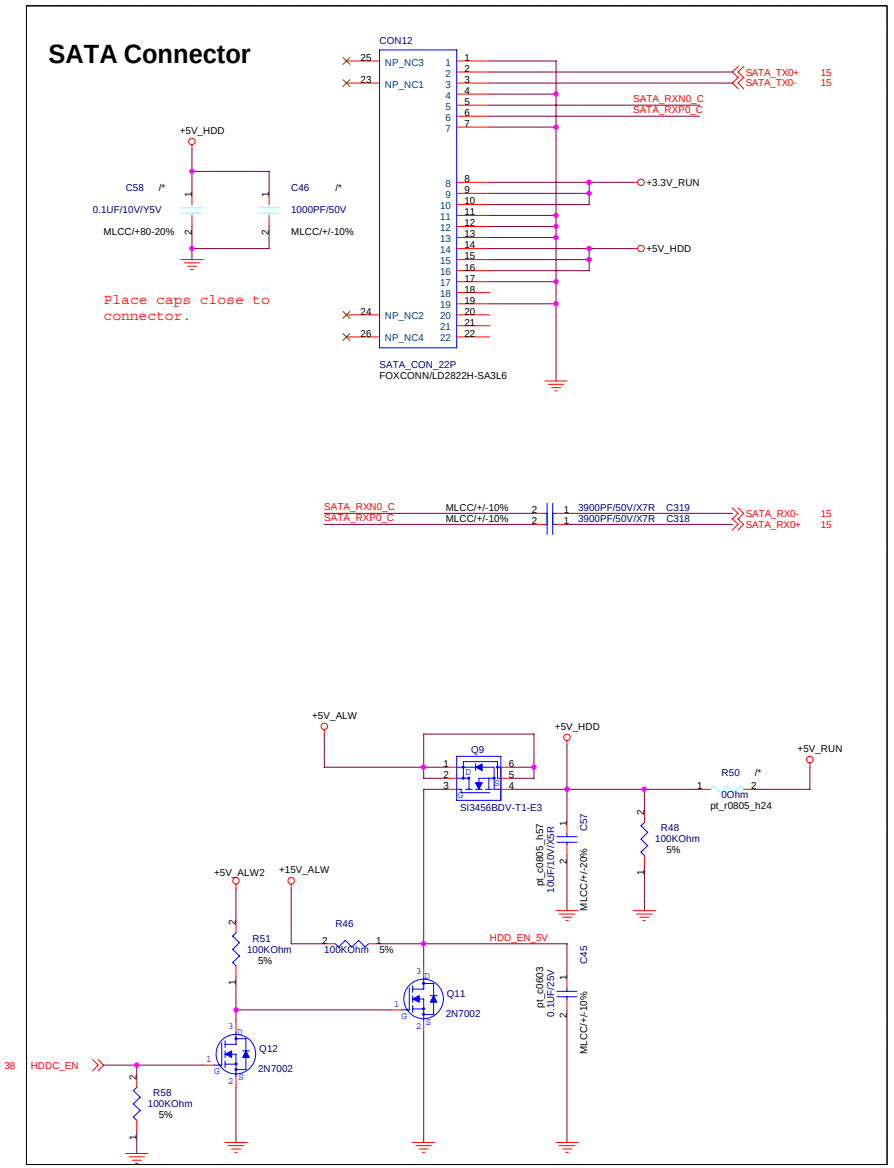
PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :		DESIGN ENGINEER :
	1.2	SHEET 26 OF 68		RELEASE DATE :		

PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :		DESIGN ENGINEER :
	1.2	SHEET 27 OF 68		RELEASE DATE :		*Sean Kuo*

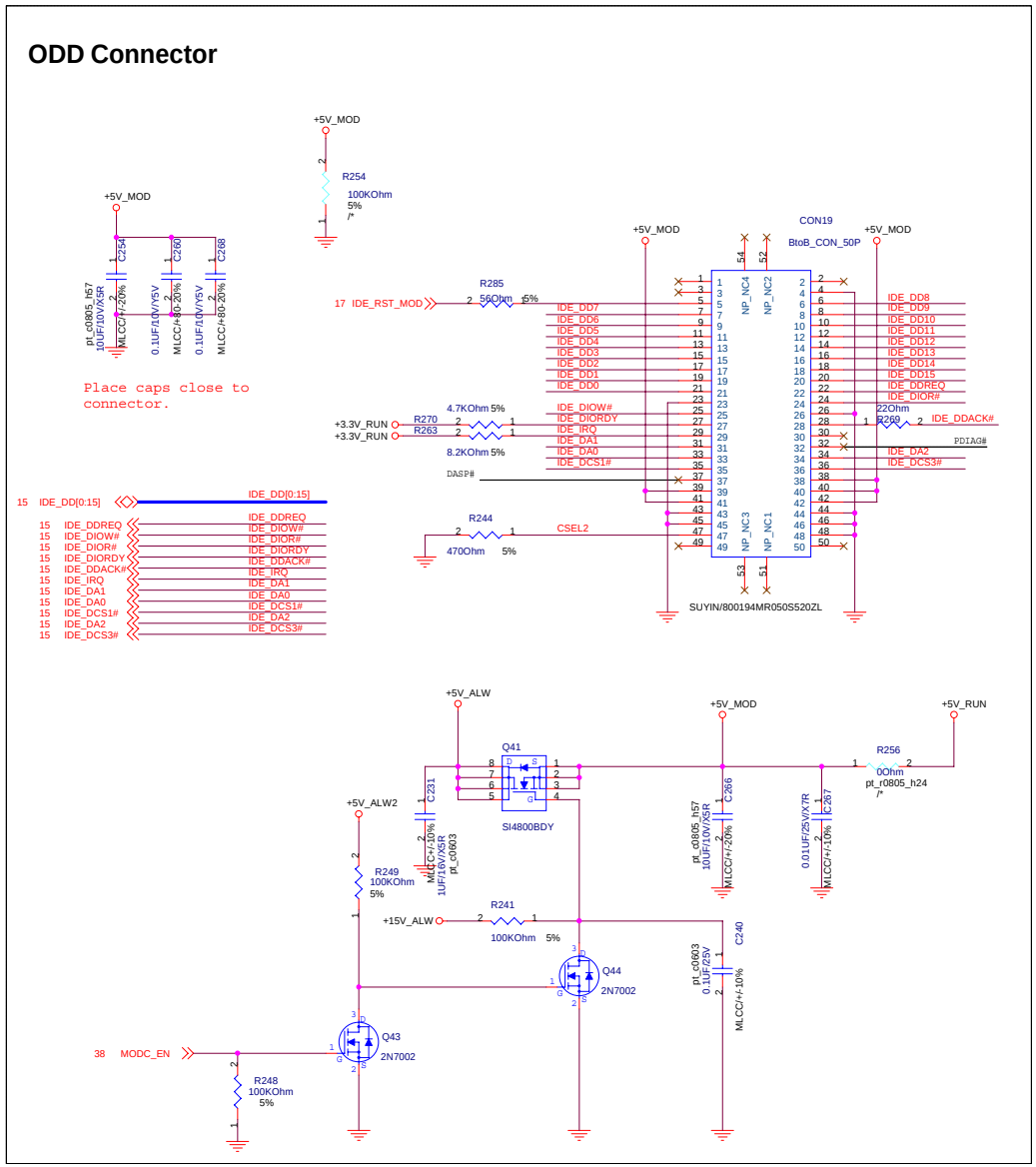


PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: LVDS CON	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 28 OF 68		RELEASE DATE :	

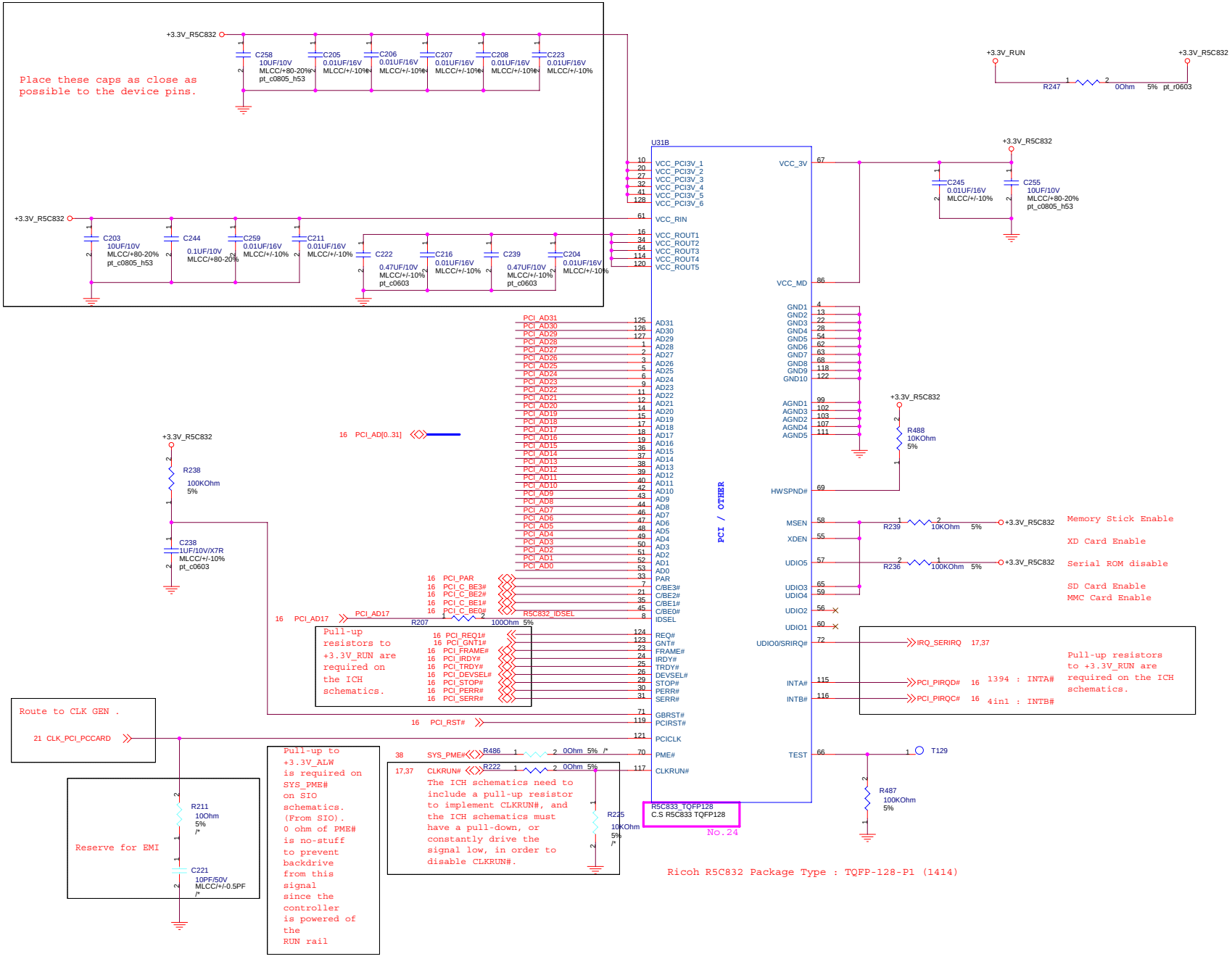
SATA Connector



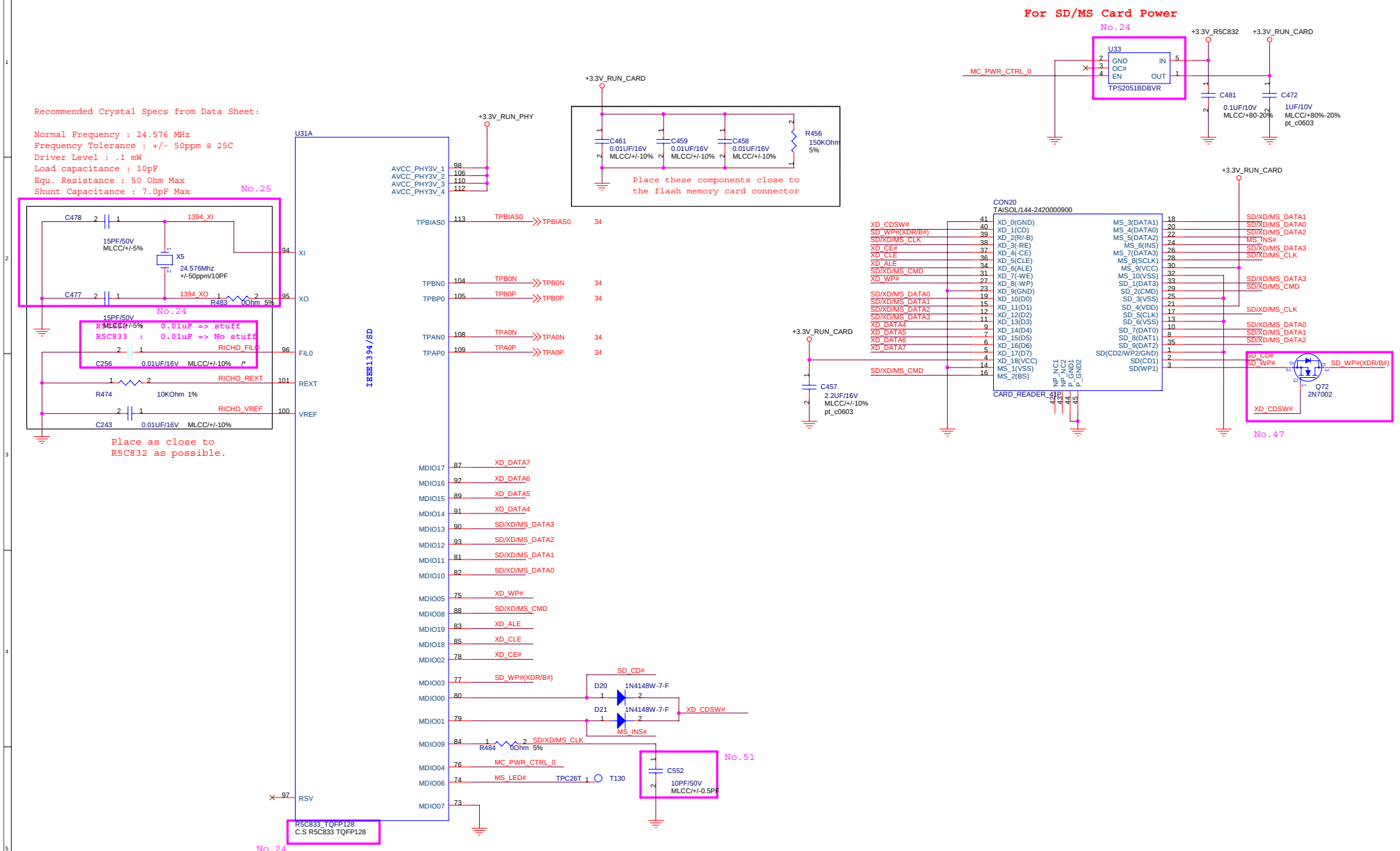
ODD Connector



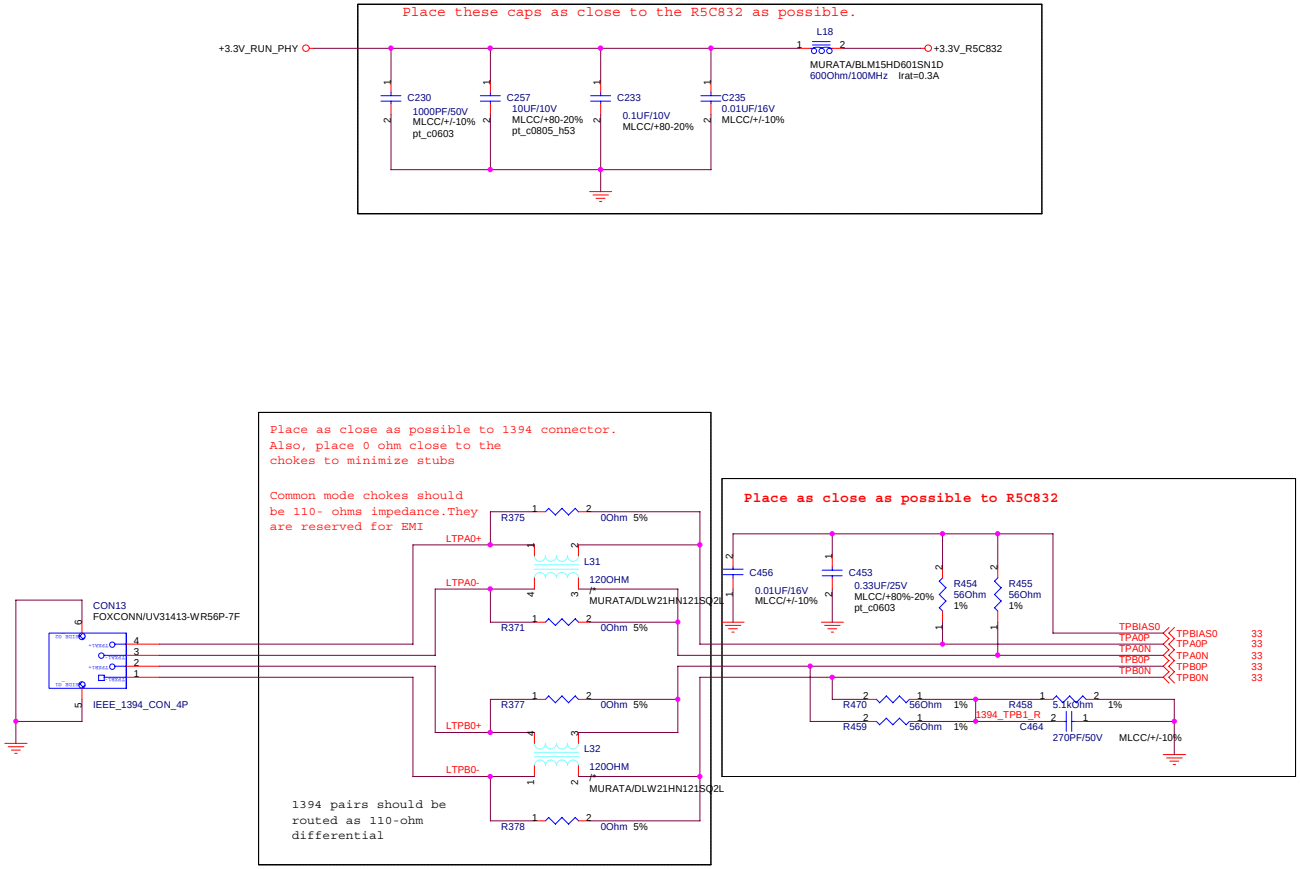
PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *SATA (HDD & CD_ROM)*	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 31 OF 68		RELEASE DATE :	



PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *R5C833 - PCI INTERFACE*	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 32 OF 68		RELEASE DATE :		

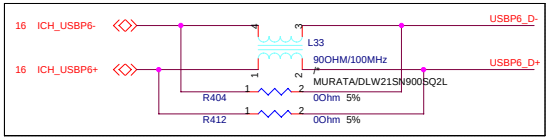


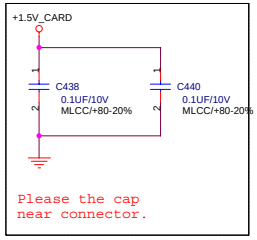
PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: R5C833 - FLASH MEMORY PART	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 33 OF 68		RELEASE DATE :		

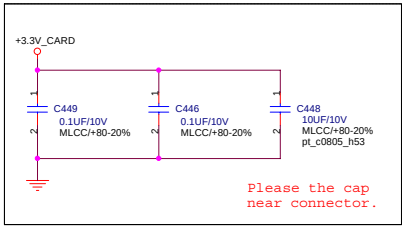


PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: R5C833 - IEEE1394 PART	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 34 OF 68		RELEASE DATE :		

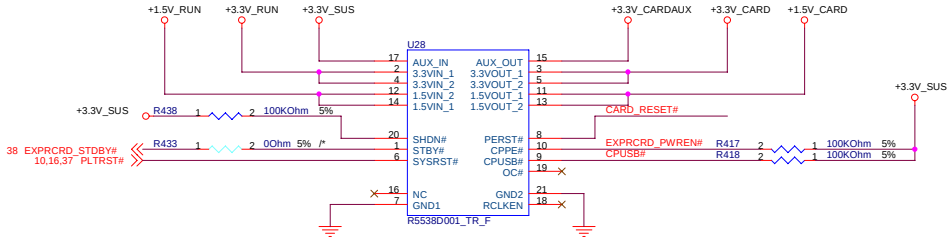
Express Card

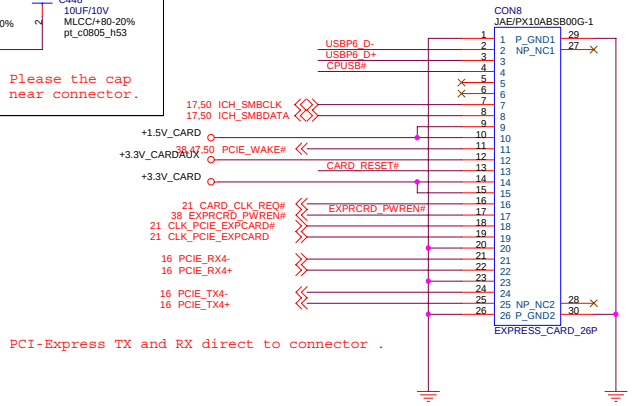




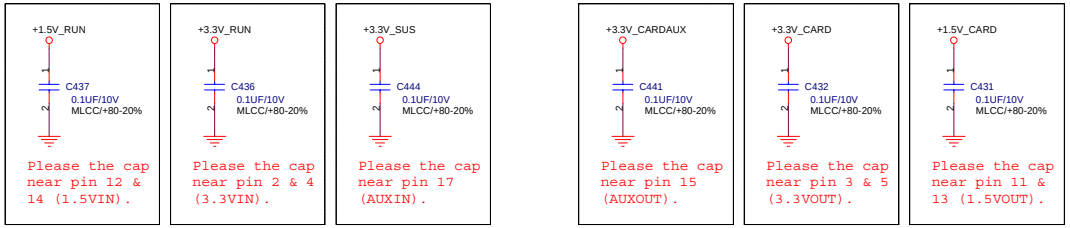


+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.

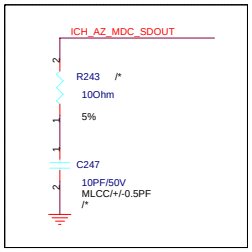


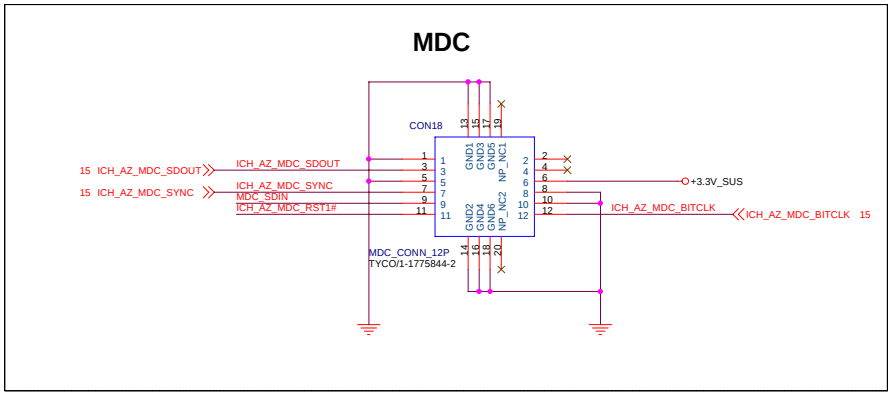


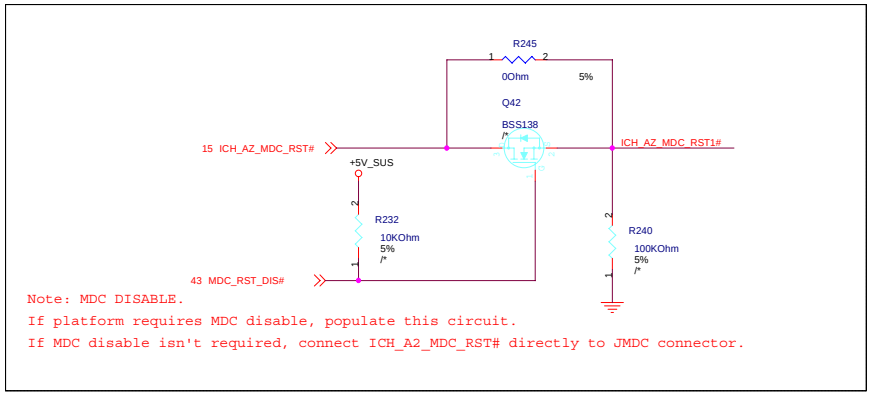
PCI-Express TX and RX direct to connector .

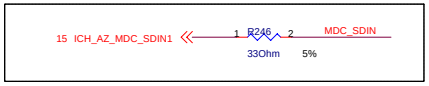


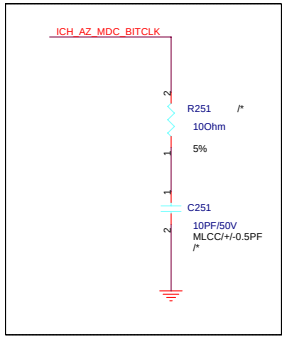
PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: PCI-Express Card	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Terry_Lin
		SHEET 35 OF 68		RELEASE DATE :	

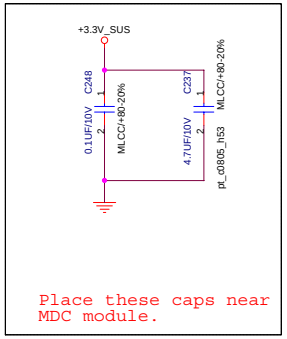




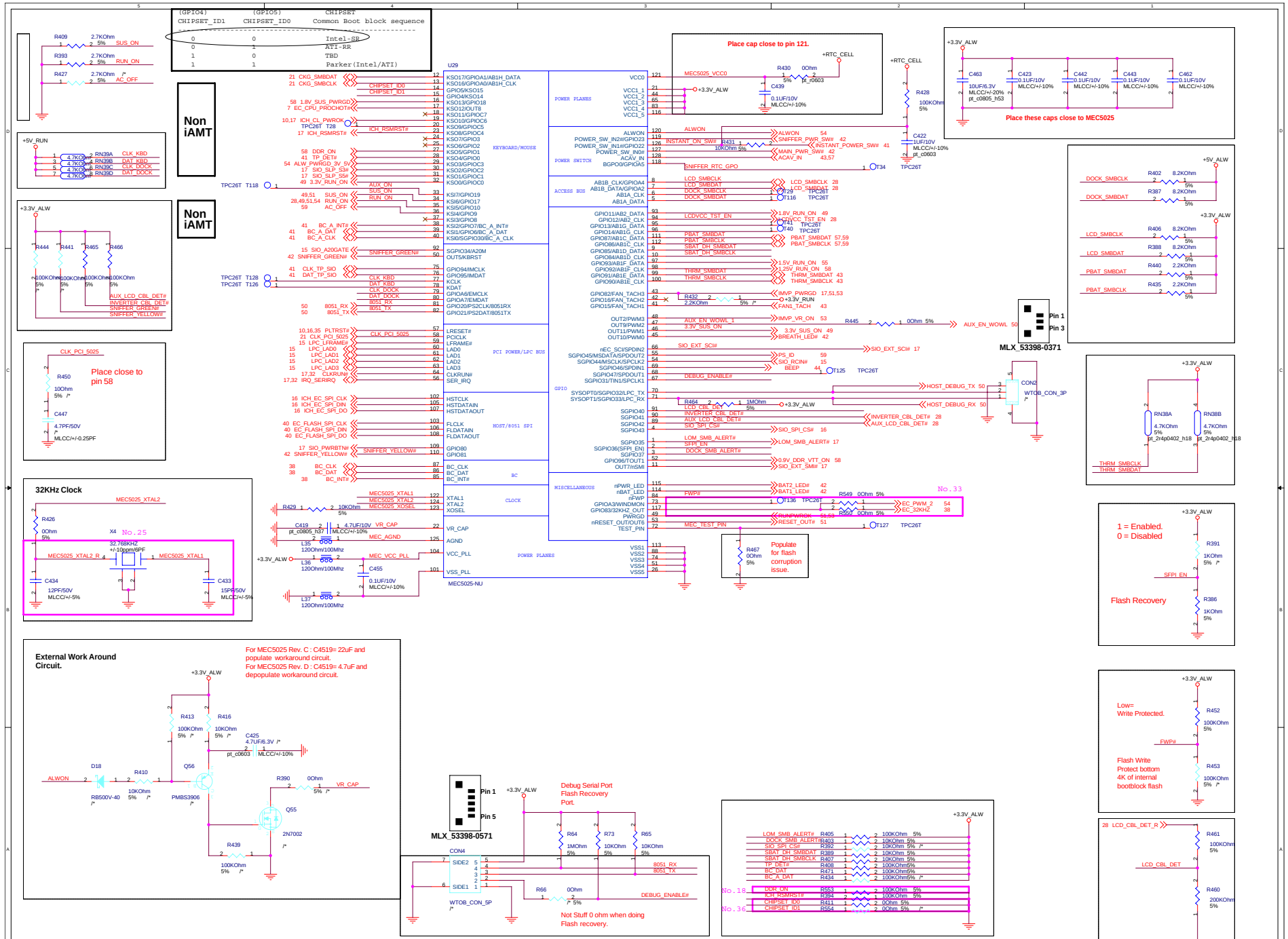


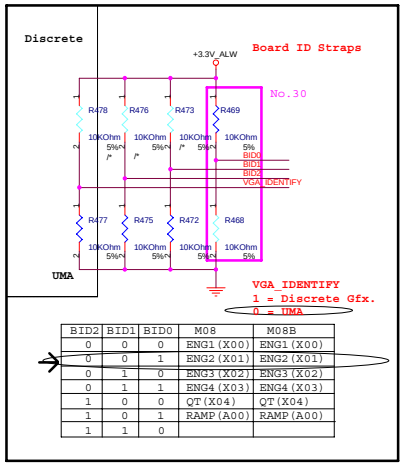






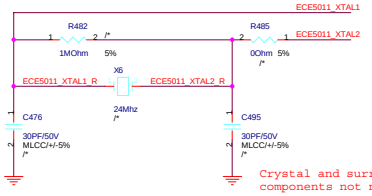
PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007 SHEET 36 OF 68	DESCRIPTION: MDC CONN	SCHEMATIC FILE NAME : <OrgName> RELEASE DATE :	DESIGN ENGINEER :


(GPIO4) (GPIO5) CHIPSET
CHIPSET_ID1 CHIPSET_ID0 Common Boot block sequence
0 0 Intel-SR
0 1 ATI-RR
1 0 TBD
1 1 Parker(Intel/ATI)
Non iAMT
Non iAMT
U29
MEC5025-NU
KEYBOARD/MOUSE
POWER SWITCH
ACCESS BUS
PCI POWER/LPC BUS
HOST/8051 SPI
BC
CLOCK
POWER PLANES
GPIO
MISCELLANEOUS
Place cap close to pin 121.
Place these caps close to MEC5025
Place close to pin 58
32KHz Clock
External Work Around Circuit.
For MEC5025 Rev. C : C4519= 22uF and populate workaround circuit.
For MEC5025 Rev. D : C4519= 4.7uF and depopulate workaround circuit.
MLX_53398-0371
Populate for flash corruption issue.
1 = Enabled.
0 = Disabled
Flash Recovery
Low= Write Protected.
Flash Write Protect bottom 4K of internal bootblock flash
Debug Serial Port Flash Recovery Port.
Not Stuff 0 ohm when doing Flash recovery.
PROJECT: Lanai
REVISION 1.2
DATE: Monday, March 19, 2007
SHEET 37 OF 68
DESCRIPTION: MEC5025
SCHEMATIC FILE NAME :
RELEASE DATE :
DESIGN ENGINEER : STANLY_HSU

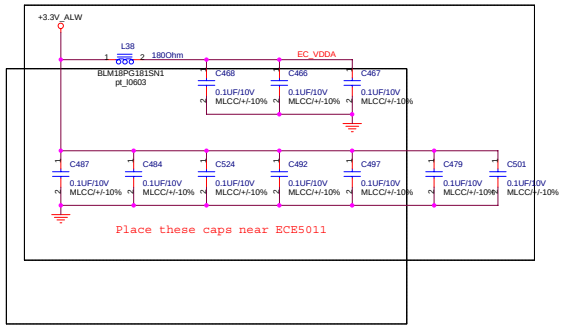


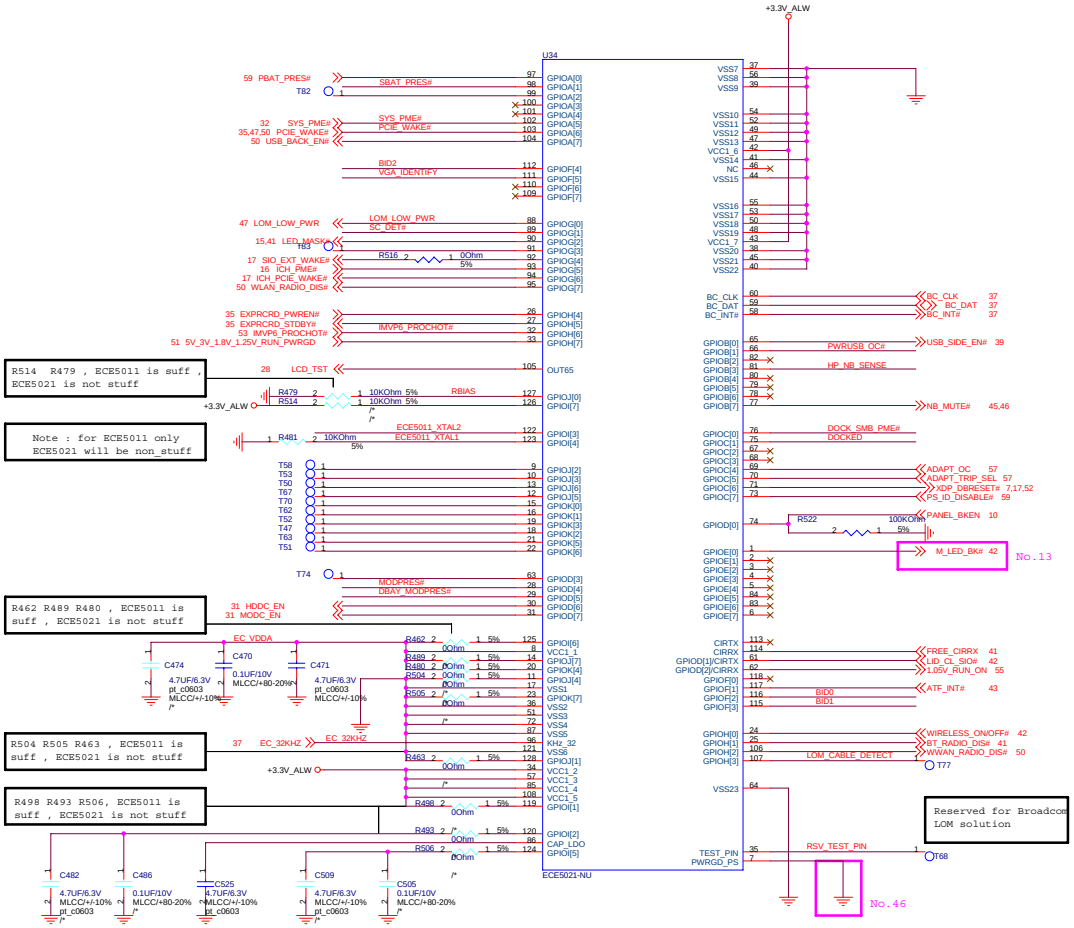
BID2	BID1	BID0	M08	M08B
0	0	0	ENG1(X00)	ENG1(X00)
0	0	1	ENG2(X01)	ENG2(X01)
0	1	0	ENG3(X02)	ENG3(X02)
0	1	1	ENG4(X03)	ENG4(X03)
1	0	0	QT(X04)	QT(X04)
1	0	1	RAMP(A00)	RAMP(A00)
1	1	0		

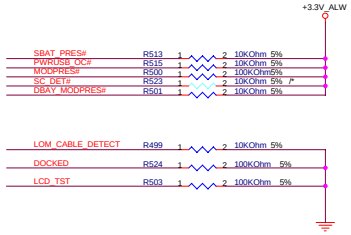
24MHz Clock

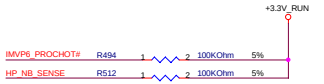


Crystal and surrounding components not needed unless SIO USB Hub is utilized

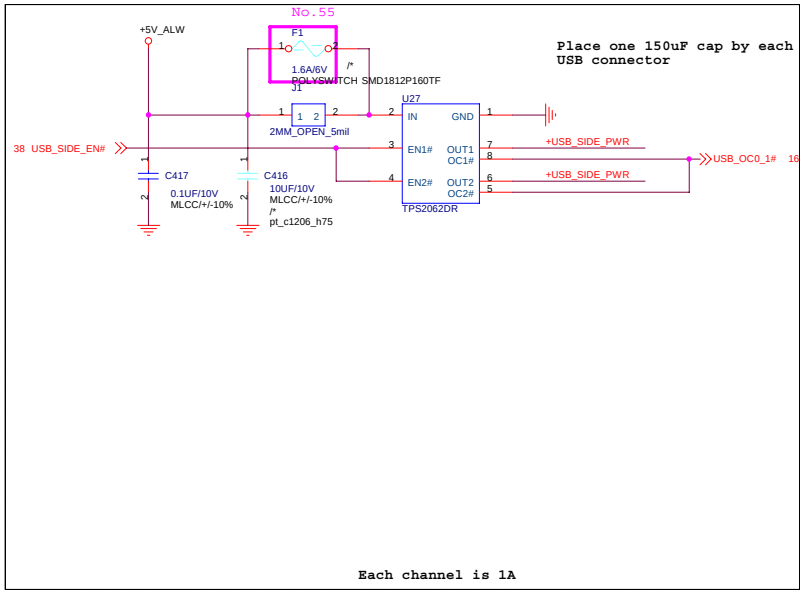


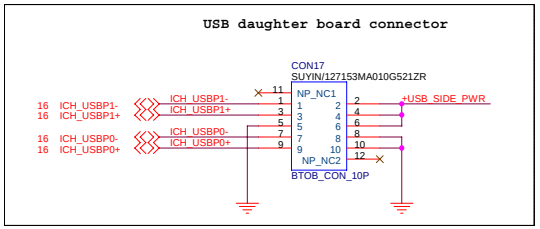




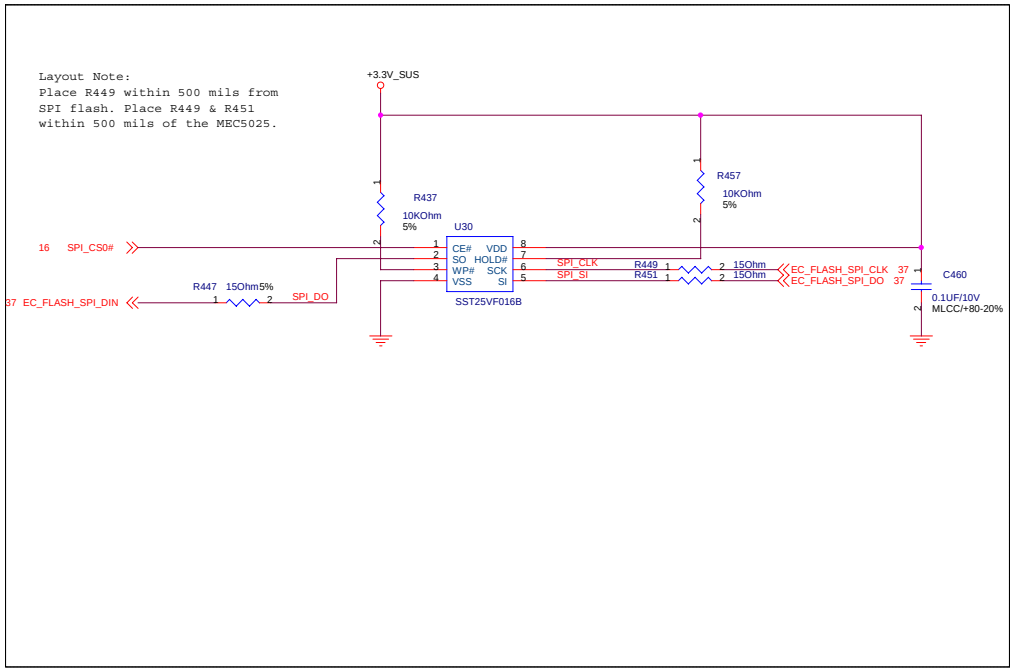


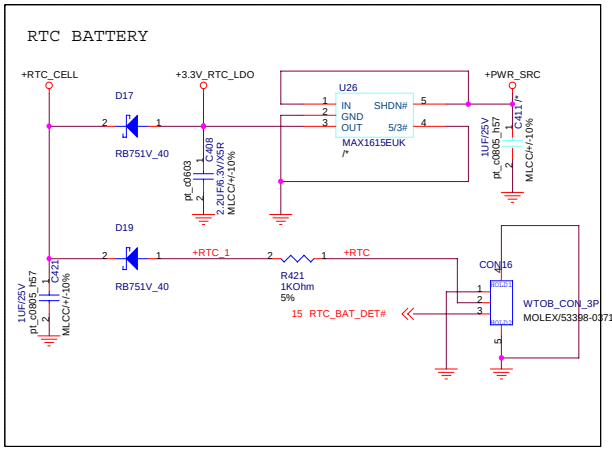
PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007 SHEET 38 OF 68	DESCRIPTION: SUPER IO ECE5011	SCHEMATIC FILE NAME : RELEASE DATE :	DESIGN ENGINEER : STANLY_HSU





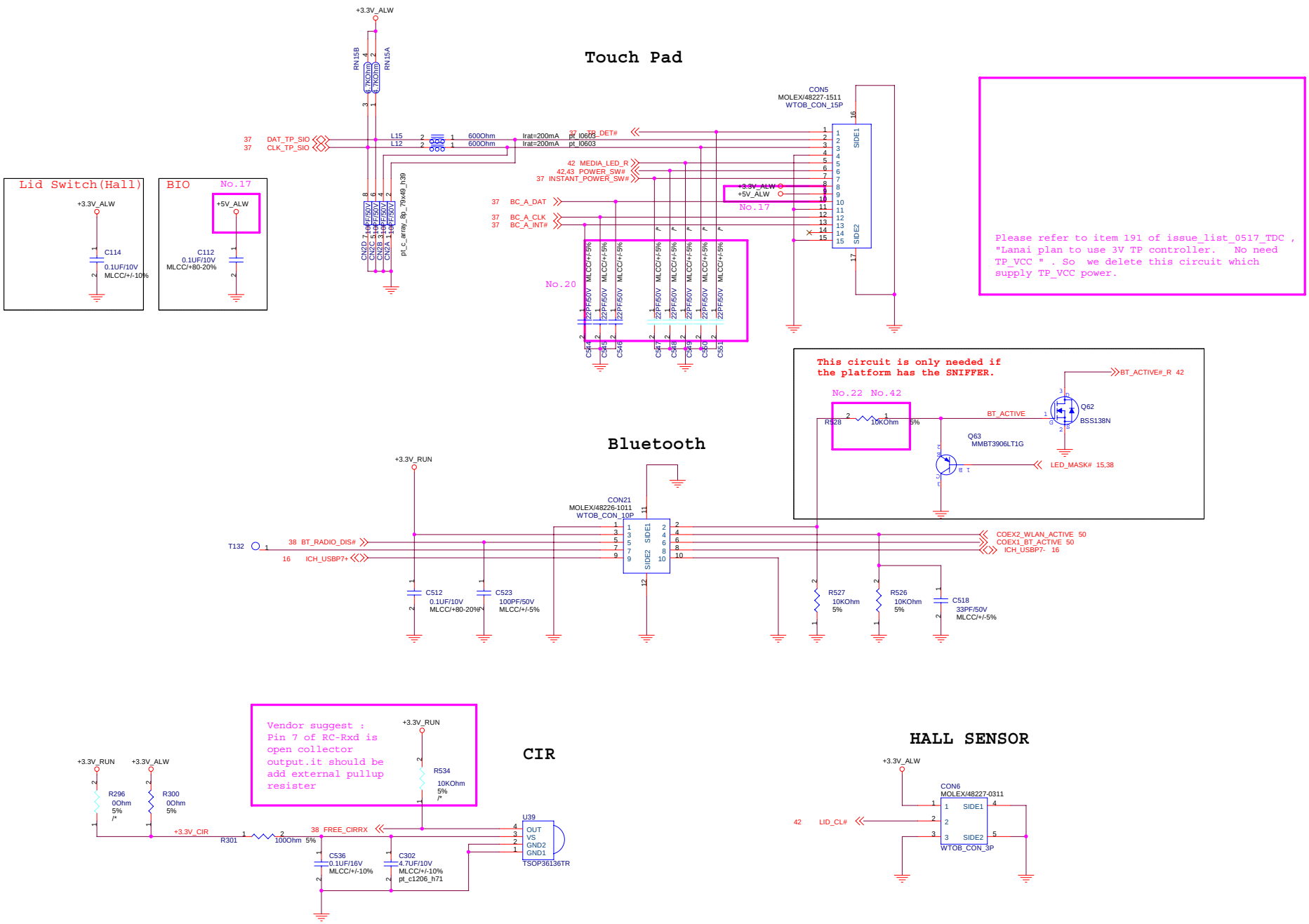
PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007 SHEET 39 OF 68	DESCRIPTION: *USB PORT x 2*	SCHEMATIC FILE NAME : <OrgName> RELEASE DATE :	DESIGN ENGINEER : *Terry_Lin*



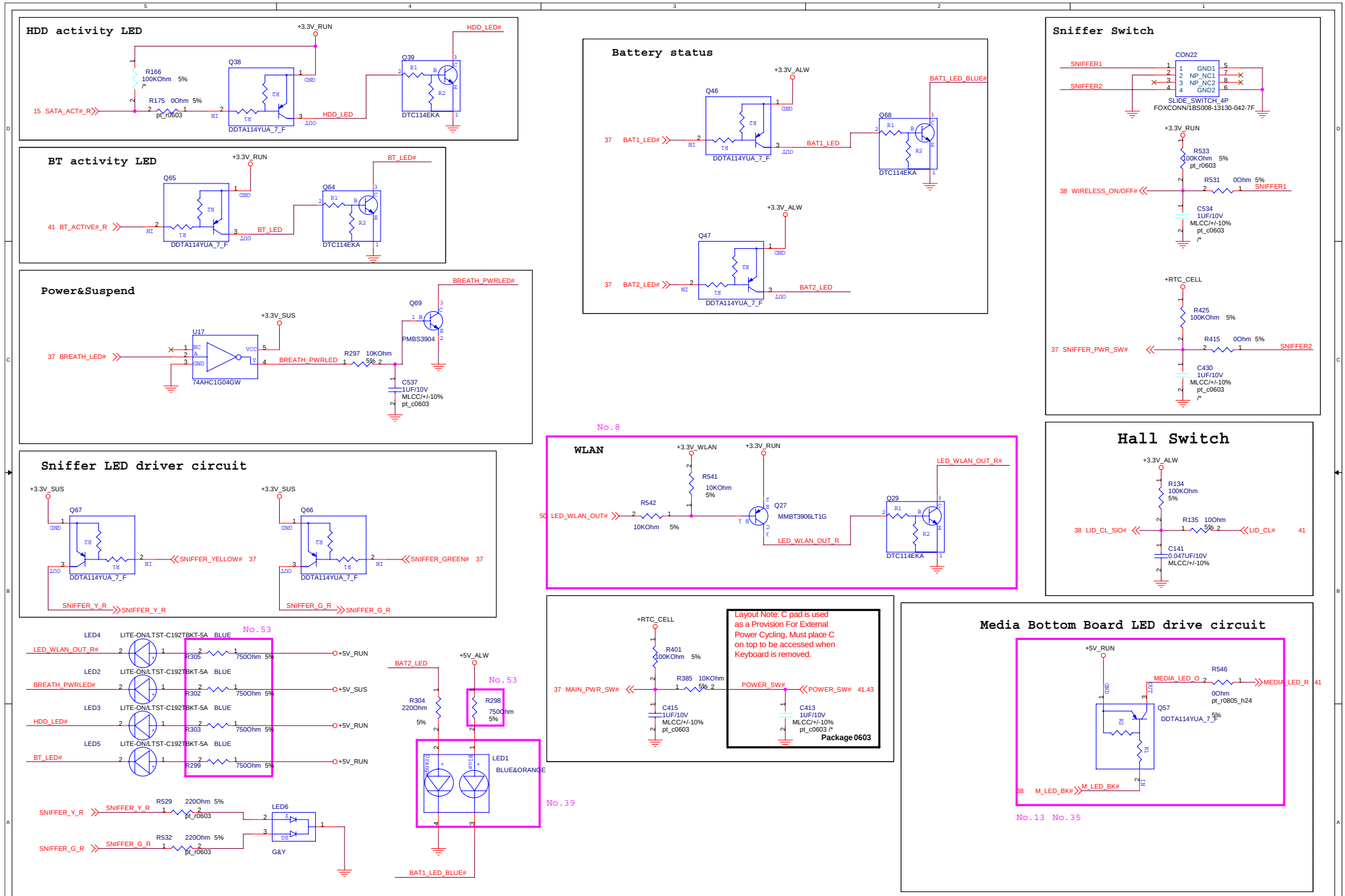


MLX_53398-0371

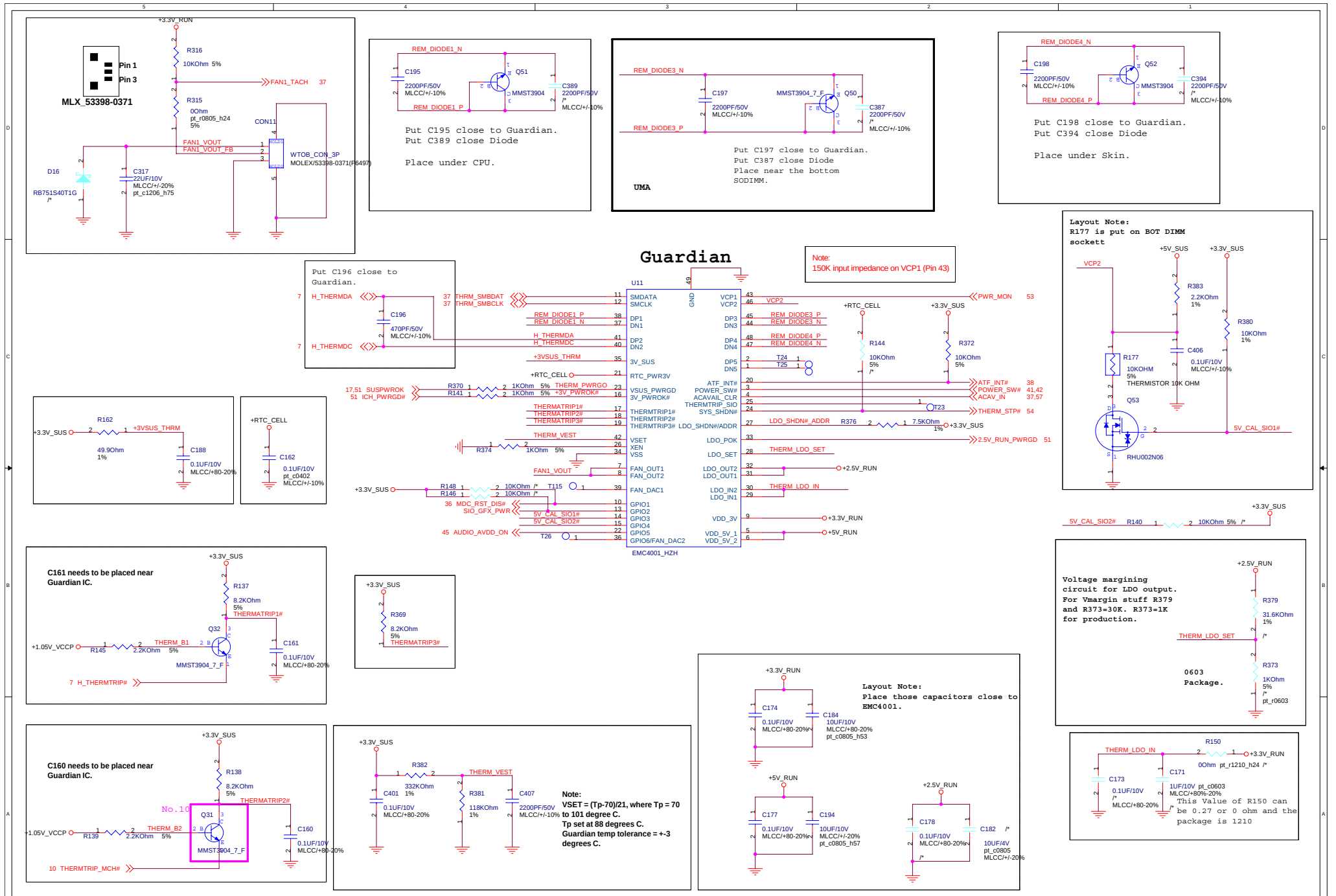
PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *FLASH & RTC*	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 40 OF 68		RELEASE DATE :		*C.L. Ho*



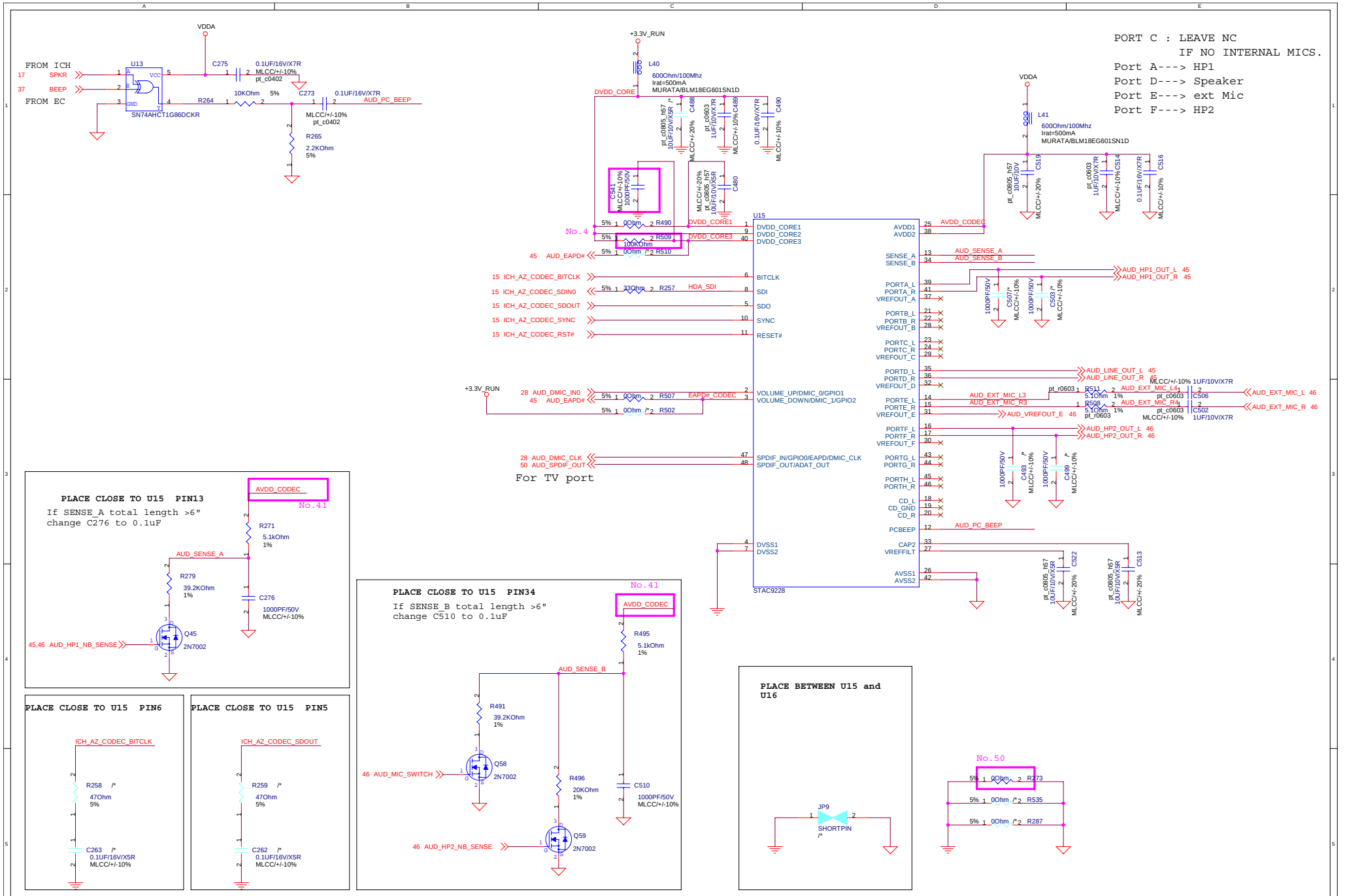
PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: TOUCH PAD & BT & CIR & HD	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 41 OF 68		RELEASE DATE :		



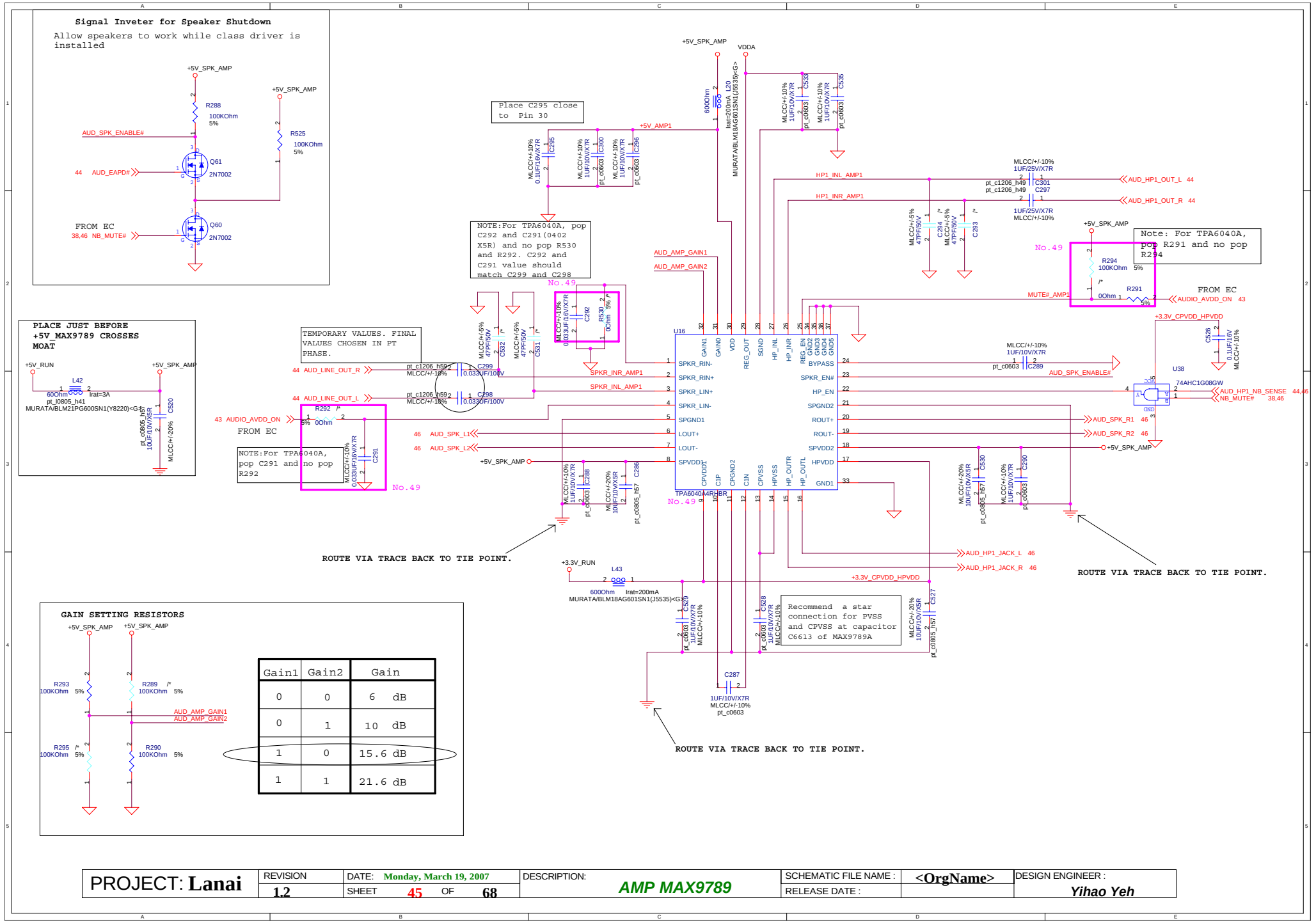
PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: SWITCH & LED	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : C
		SHEET 42 OF 68		RELEASE DATE :	

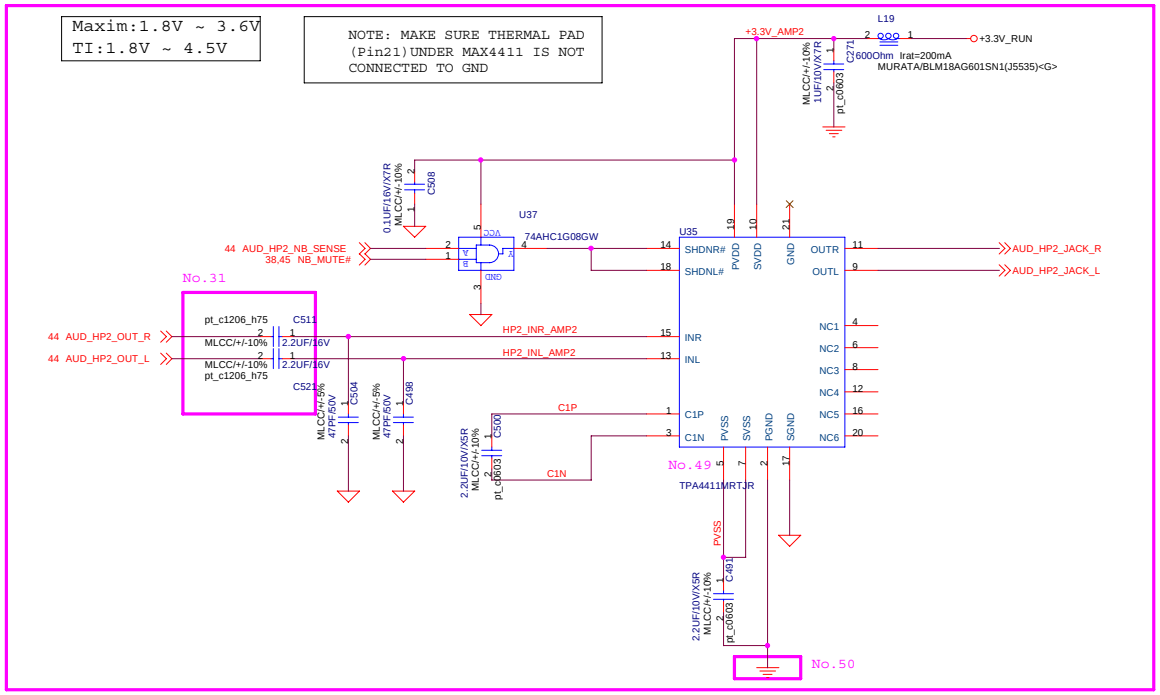


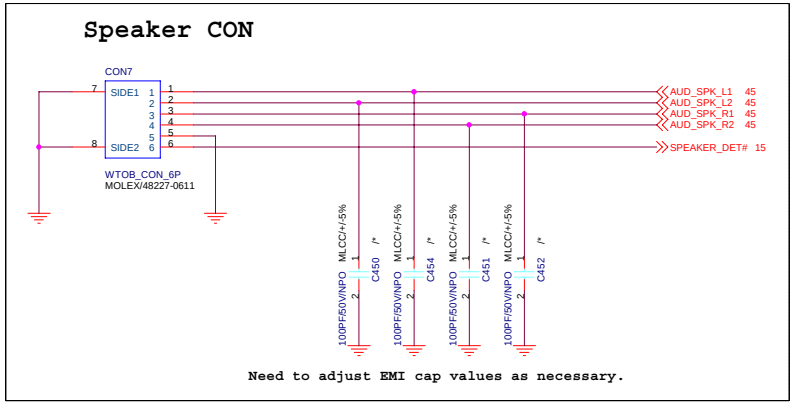
PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: EMC4001	SCHEMATIC FILE NAME :	DESIGN ENGINEER : N
		SHEET 43 OF 68		RELEASE DATE :	

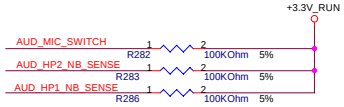


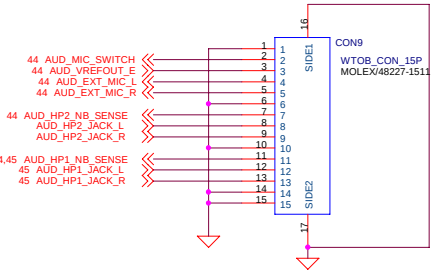
PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: STAC9228	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Yihao Yeh
		SHEET 44 OF 68		RELEASE DATE :	


Signal Inveter for Speaker Shutdown
Allow speakers to work while class driver is installed
+5V_SPK_AMP
R288 100KOhm 5%
R525 100KOhm 5%
AUD_SPK_ENABLE#
Q61 2N7002
44 AUD_EAPD#
FROM EC
38,46 NB_MUTE#
Q60 2N7002
PLACE JUST BEFORE +5V_MAX9789 CROSSES MOAT
+5V_RUN
L42 60Ohm Irat=3A
MURATA/BLM21PG600SN1(Y8220)<G>
C520 10UF/10V/X5R MLCC/+/-20%
Place C295 close to Pin 30
C295 C300 C296 C533 C535
+5V_AMP1
L20 600Ohm Irat=200mA MURATA/BLM18AG601SN1(J5535)<G>
VDDA
NOTE:For TPA6040A, pop C292 and C291(0402 X5R) and no pop R530 and R292. C292 and C291 value should match C299 and C298
TEMPORARY VALUES. FINAL VALUES CHOSEN IN PT PHASE.
44 AUD_LINE_OUT_R
44 AUD_LINE_OUT_L
43 AUDIO_AVDD_ON
FROM EC
R292 0Ohm
C299 0.033UF/100V
C298 0.033UF/100V
C532 C531 R530 0Ohm
NOTE:For TPA6040A, pop C291 and no pop R292
C291 0.033UF/10V/X7R
No.49
U16 TPA6040A4RHBR
SPKR_INR_AMP1
SPKR_INL_AMP1
46 AUD_SPK_L1
46 AUD_SPK_L2
AUD_AMP_GAIN1
AUD_AMP_GAIN2
HP1_INL_AMP1
HP1_INR_AMP1
AUD_HP1_OUT_L 44
AUD_HP1_OUT_R 44
C301 C297 1UF/25V/X7R
C294 47PF/50V C293
Note: For TPA6040A, pop R291 and no pop R294
R294 100KOhm 5%
R291 0Ohm 5%
MUTE#_AMP1
FROM EC
AUDIO_AVDD_ON 43
+3.3V_CPVDD_HPVDD
C526 0.1UF/16V
U38 74AHC1G08GW
AUD_HP1_NB_SENSE 44,46
NB_MUTE# 38,46
AUD_SPK_ENABLE#
AUD_SPK_R1 46
AUD_SPK_R2 46
AUD_HP1_JACK_L 46
AUD_HP1_JACK_R 46
ROUTE VIA TRACE BACK TO TIE POINT.
+3.3V_RUN
L43 600Ohm Irat=200mA MURATA/BLM18AG601SN1(J5535)<G>
+3.3V_CPVDD_HPVDD
C529 C528 C527
Recommend a star connection for PVSS and CPVSS at capacitor C6613 of MAX9789A
C287 1UF/10V/X7R MLCC/+/-10% pt_c0603
GAIN SETTING RESISTORS
R293 100KOhm 5%
R289 100KOhm 5%
R295 100KOhm 5%
R290 100KOhm 5%
AUD_AMP_GAIN1
AUD_AMP_GAIN2
Gain1 Gain2 Gain
0 0 6 dB
0 1 10 dB
1 0 15.6 dB
1 1 21.6 dB
PROJECT: Lanai
REVISION 1.2
DATE: Monday, March 19, 2007
SHEET 45 OF 68
DESCRIPTION: AMP MAX9789
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER : Yihao Yeh

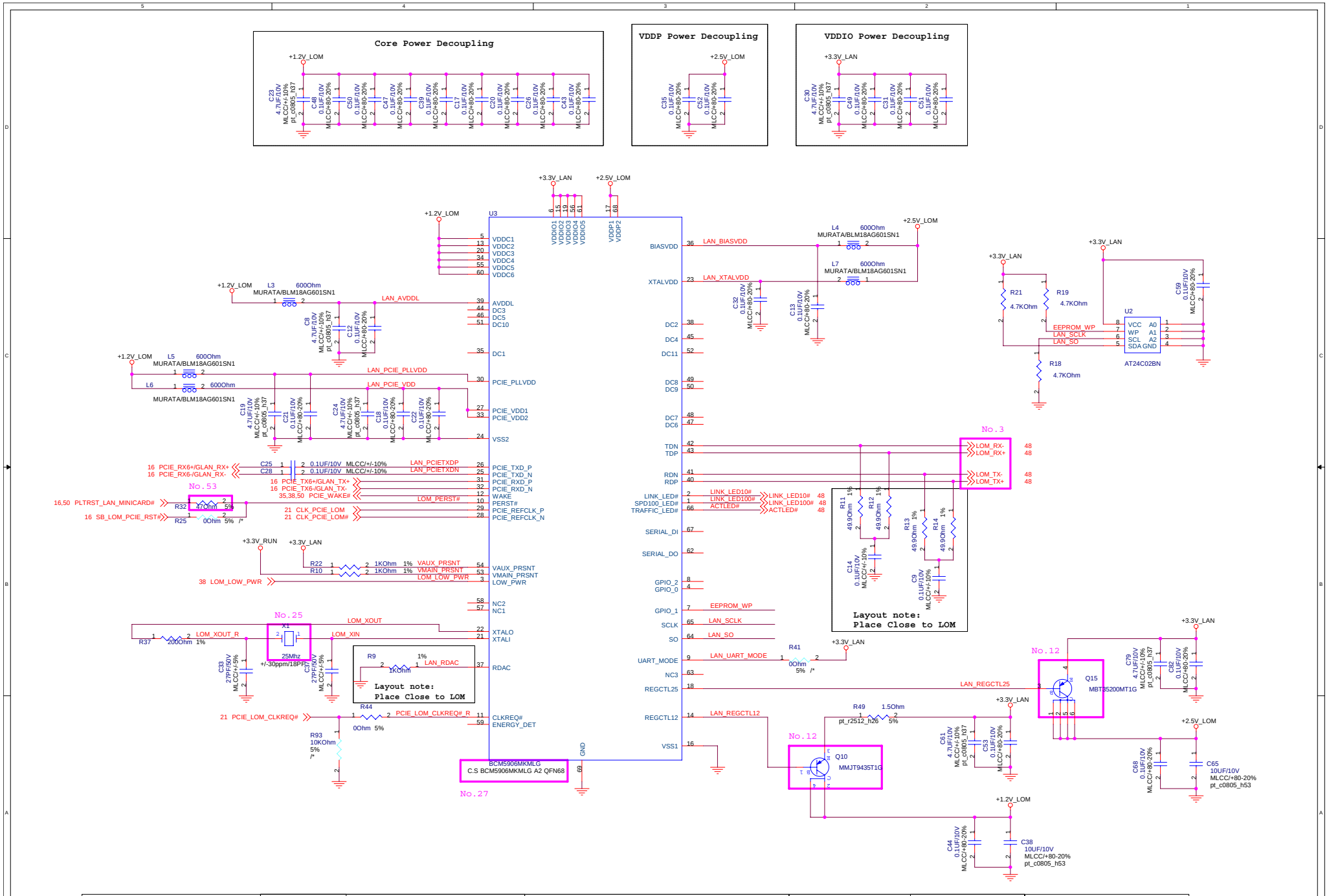




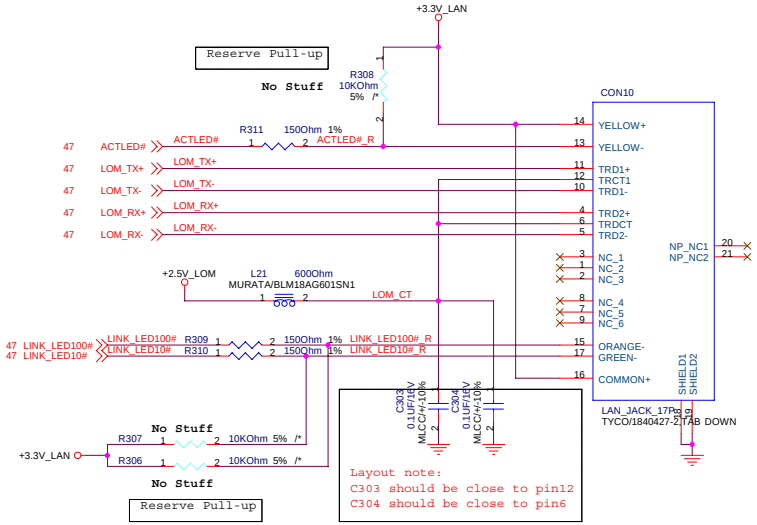




PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007 SHEET 46 OF 68	DESCRIPTION: *AMP MAX4411 & AUDIO JACK*	SCHEMATIC FILE NAME : RELEASE DATE :	<OrgName>	DESIGN ENGINEER : *Yihao Yeh*

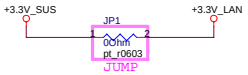


PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: LAN BCM5906MKMLG(QFN-68)	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Ivan_Chou
		SHEET 47 OF 68		RELEASE DATE :	

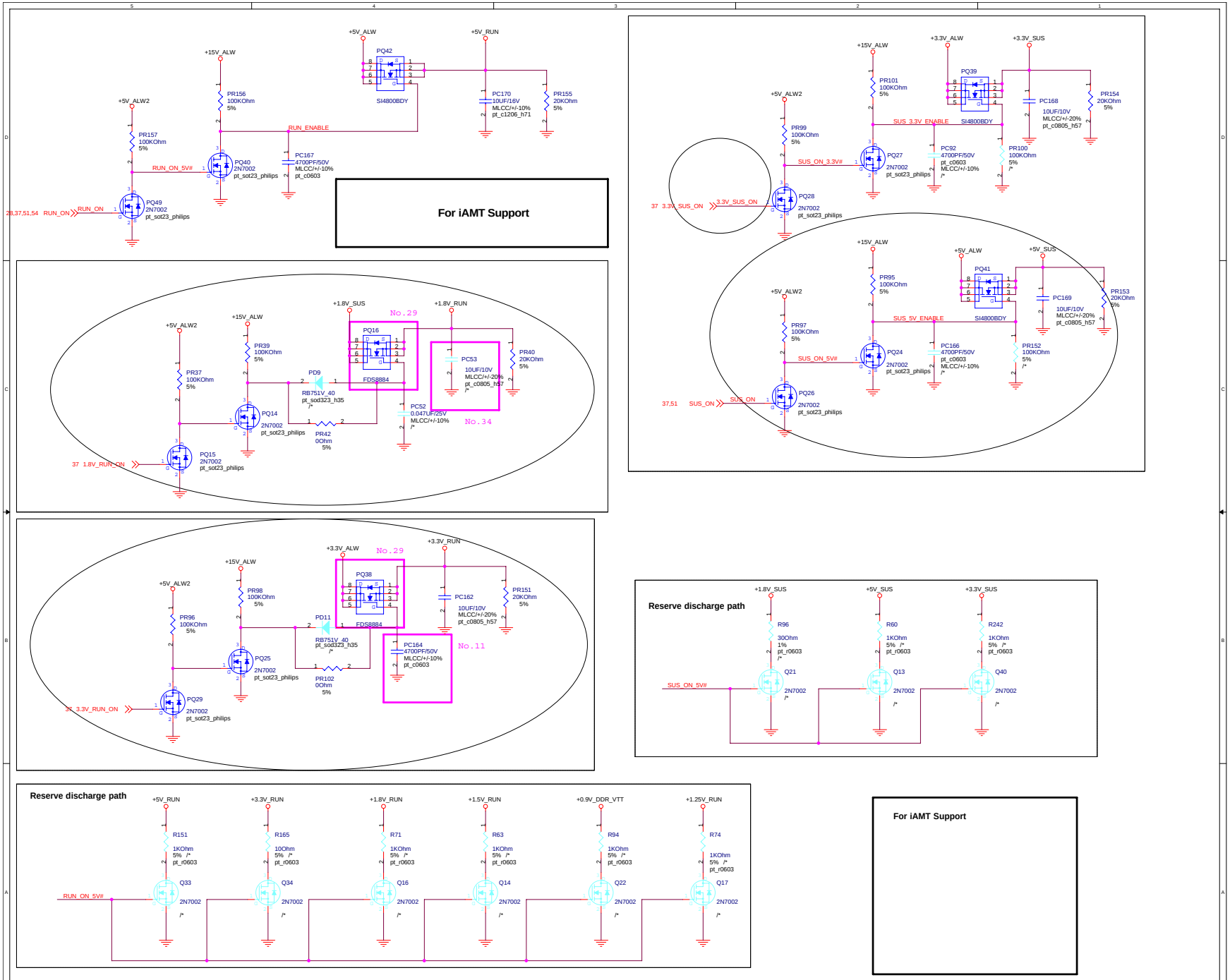


+3.3V_LAN Source Guideline:

1. Use +3.3V_SUS if Wake-on-LAN is NOT required out of S4, S5
2. Use +3.3V_SRC if Wake-on_LAN is required out of S4, S5

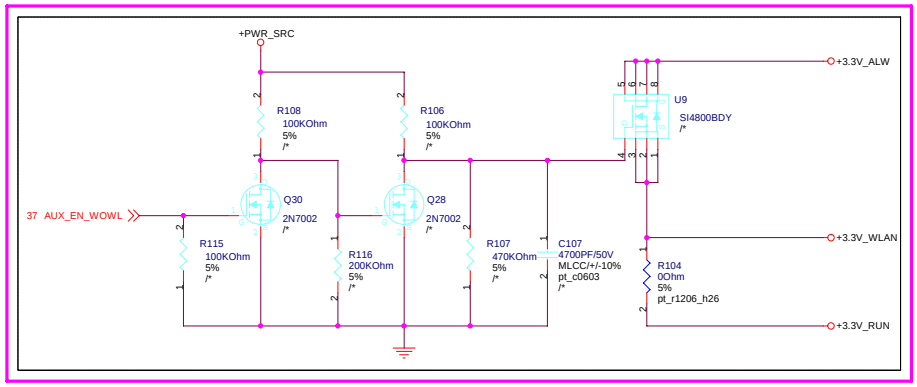


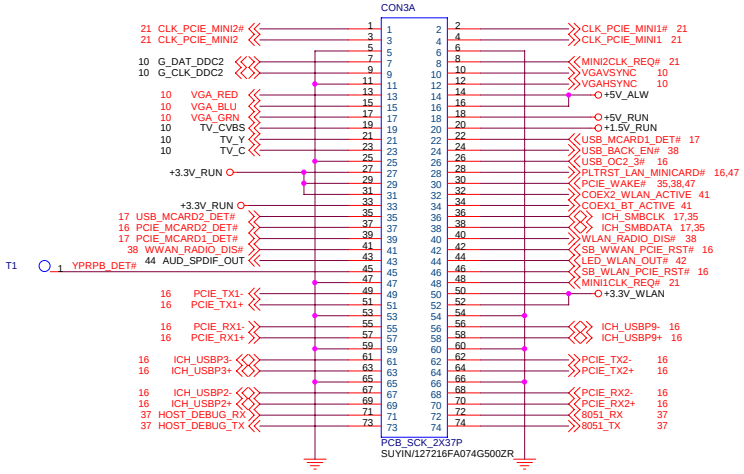
PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007 SHEET 48 OF 68	DESCRIPTION: *Magnetics and RJ-45*	SCHEMATIC FILE NAME : <OrgName> RELEASE DATE :	DESIGN ENGINEER : *Ivan_Chou*

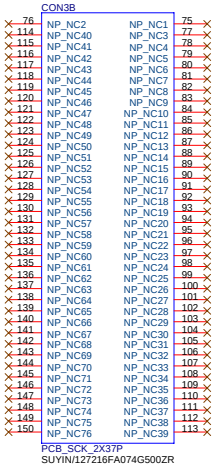


PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: Power Control Switch	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Eric Ko
		SHEET 49 OF 68		RELEASE DATE :	

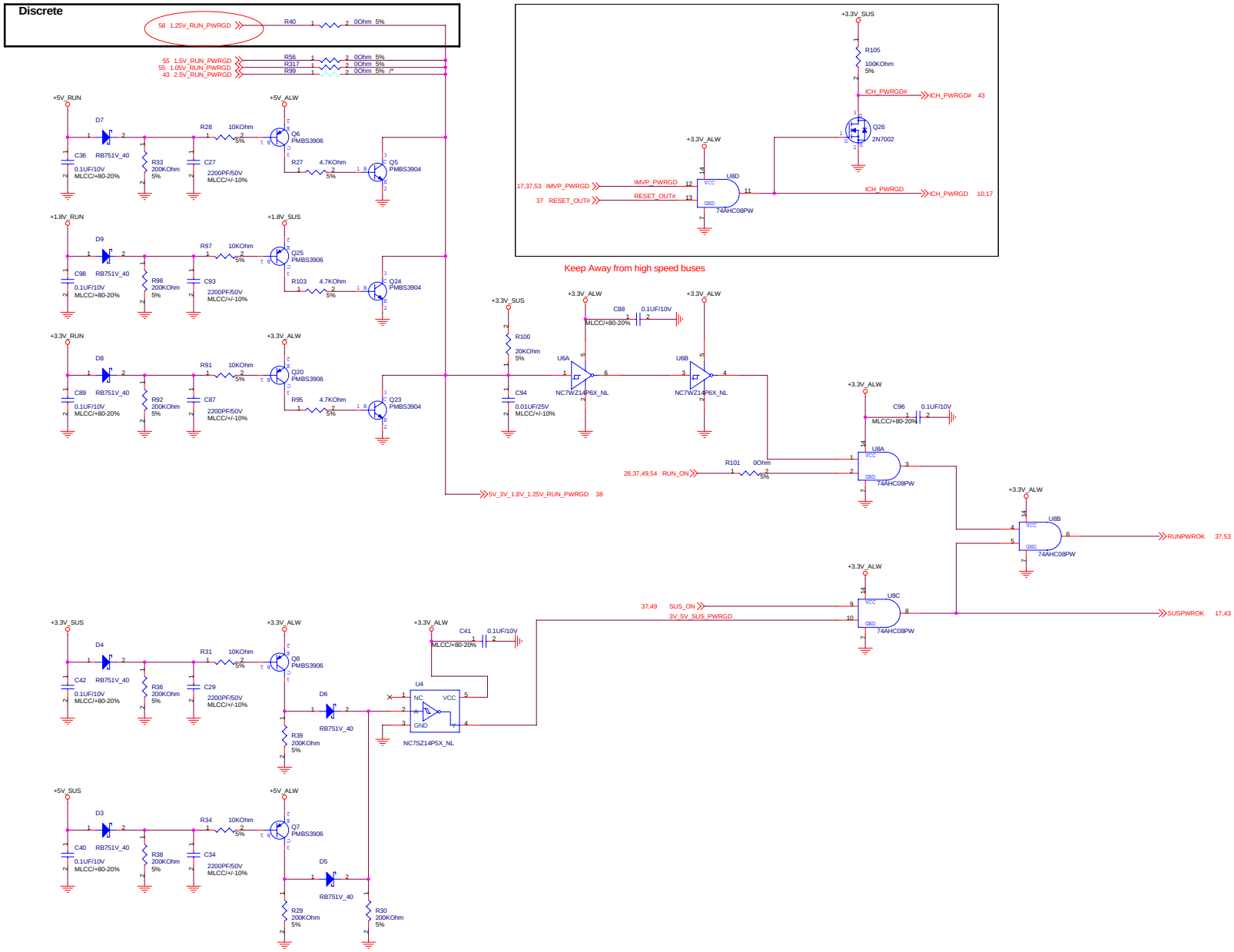
No.21





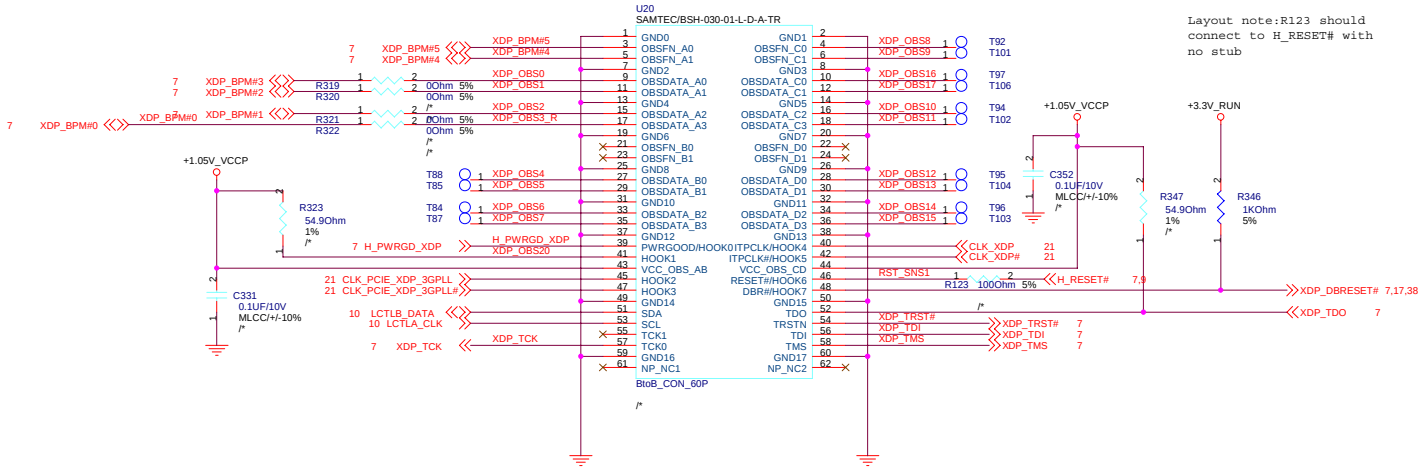


PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007 SHEET 50 OF 68	DESCRIPTION: *BtoB CON*	SCHEMATIC FILE NAME : <OrgName> RELEASE DATE :	DESIGN ENGINEER : *STANLY_HSU*



PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: Power Sequence Logic	SCHEMATIC FILE NAME :	DESIGN ENGINEER : C.L. Ho
		SHEET 51 OF 68		RELEASE DATE :	

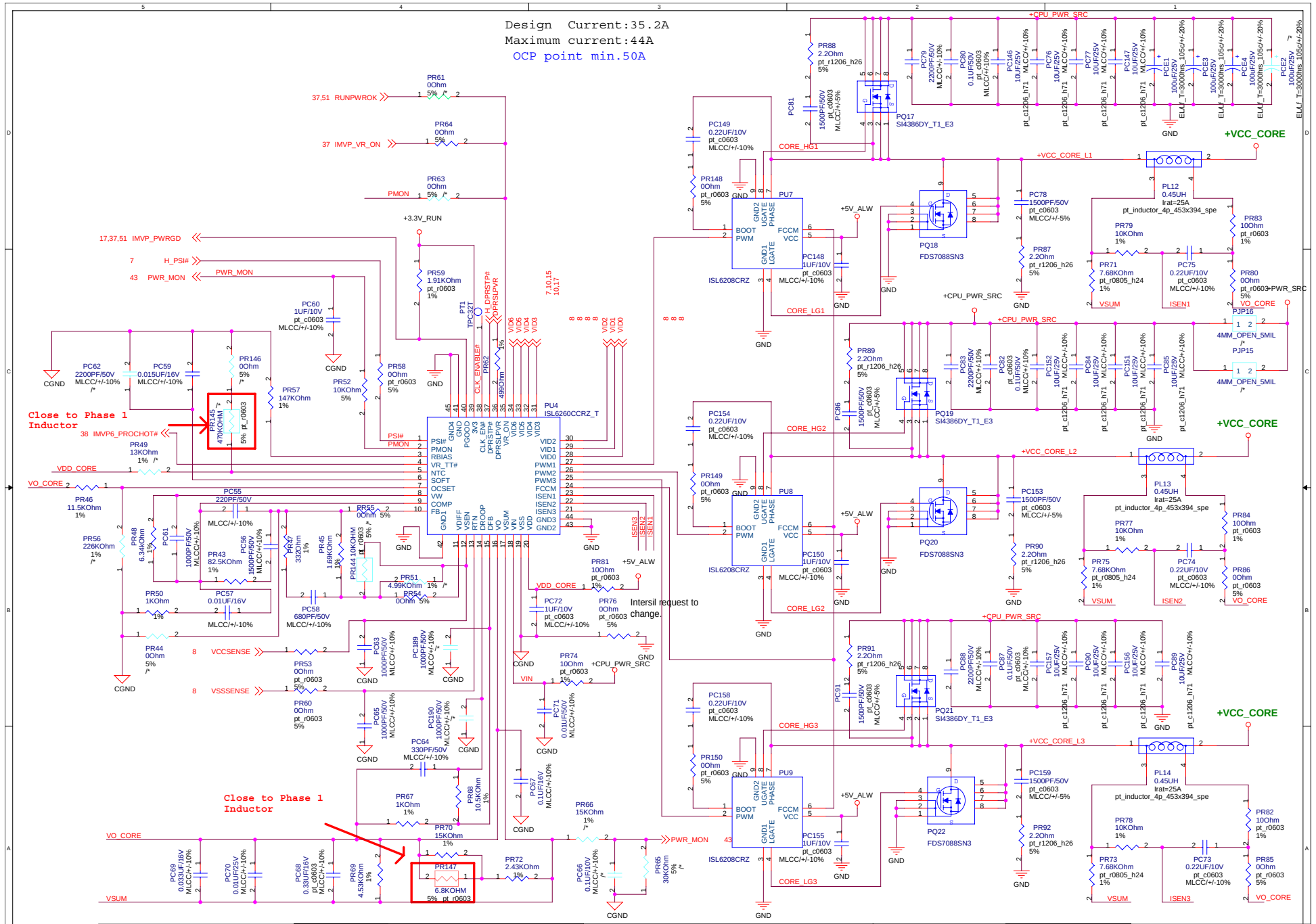
XDP



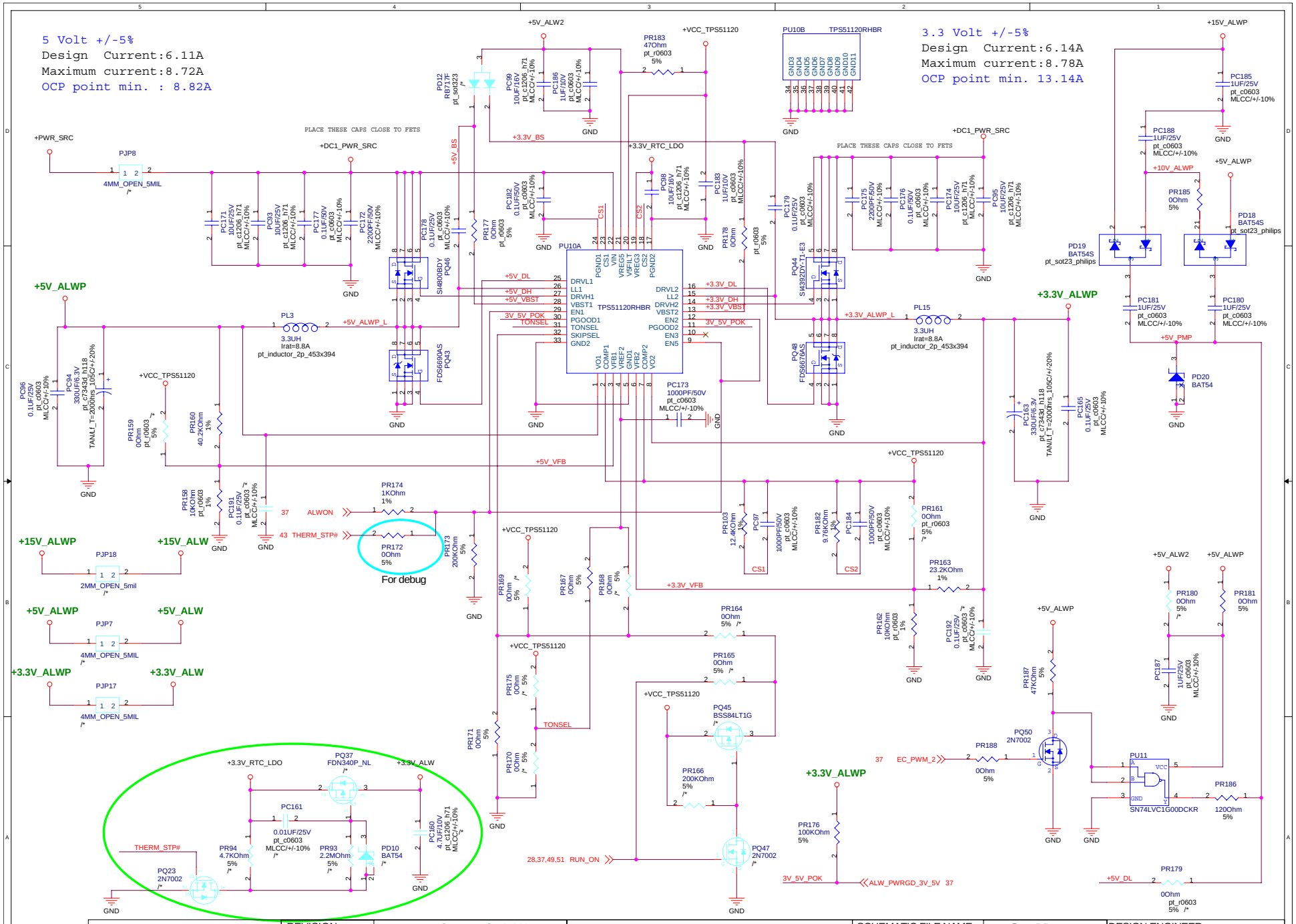
Layout note:R123 should connect to H_RESET# with no stub

CAD NOTE:
Place the XDP connector on the primary side of the CRB and place all components near the connector.

PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: XDP	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Terry_Lin
		SHEET 52 OF 68		RELEASE DATE :	



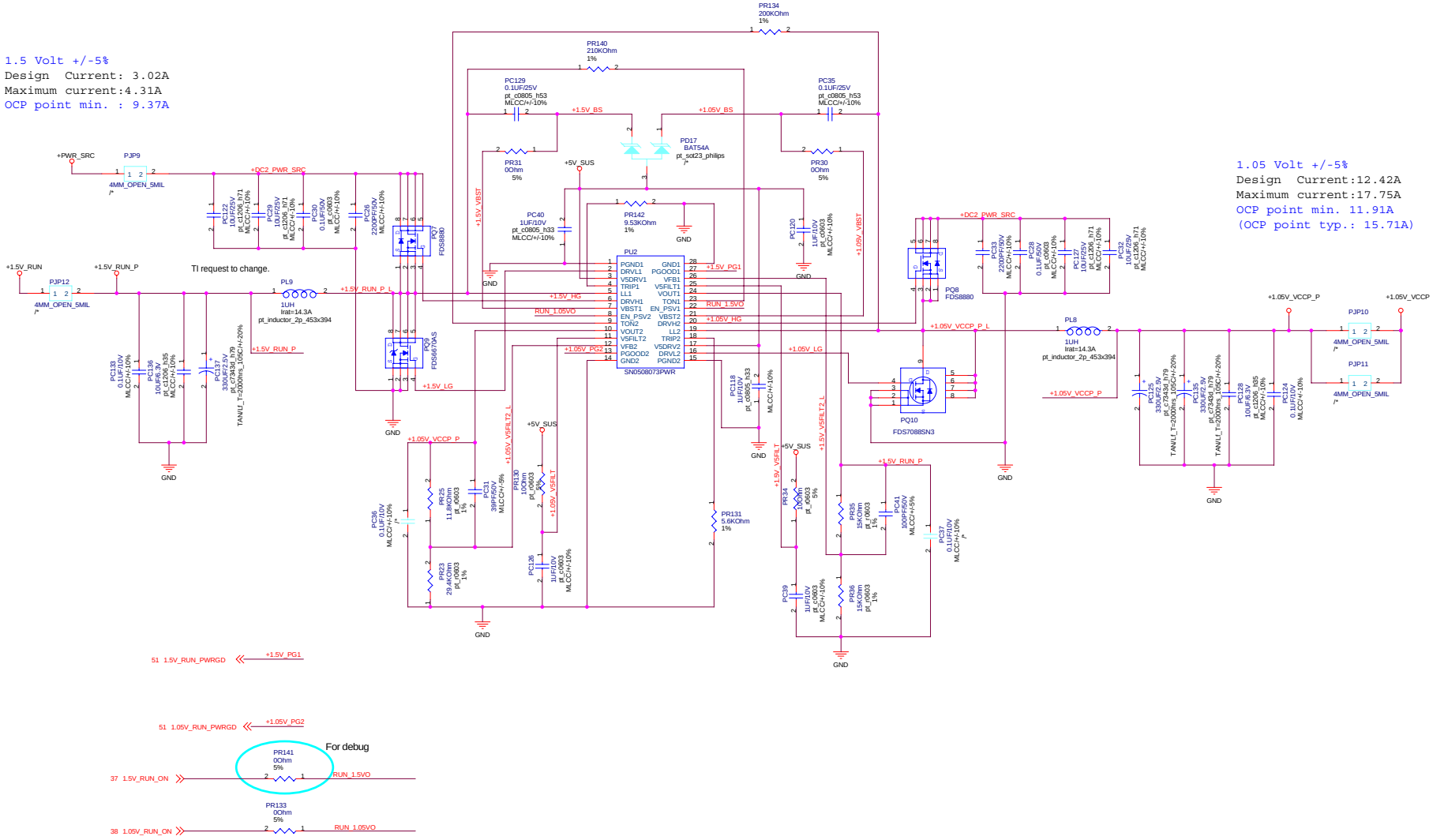
PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: POWER_VCORE	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : JEFF
		SHEET 53 OF 68		RELEASE DATE :	


5 Volt +/-5%
Design Current:6.11A
Maximum current:8.72A
OCP point min. : 8.82A
3.3 Volt +/-5%
Design Current:6.14A
Maximum current:8.78A
OCP point min. 13.14A
PU10A TPS51120RHBR
PU10B TPS51120RHBR
PLACE THESE CAPS CLOSE TO FETS
+PWR_SRC
+DC1_PWR_SRC
+5V_ALW2
+VCC_TPS51120
+3.3V_RTC_LDO
+15V_ALWP
+5V_ALWP
+3.3V_ALWP
+5V_ALW
+3.3V_ALW
+15V_ALW
+10V_ALWP
+5V_PMP
+5V_VFB
+3.3V_VFB
+3.3V_BS
+5V_BS
+5V_DL
+5V_DH
+5V_VBST
+3.3V_DL
+3.3V_DH
+3.3V_VBST
+5V_ALWP_L
+3.3V_ALWP_L
3V_5V_POK
TONSEL
ALWON
THERM_STP#
EC_PWM_2
RUN_ON
ALW_PWRGD_3V_5V
For debug
PROJECT: Lanai
REVISION 1.2
DATE: Monday, March 19, 2007
SHEET 54 OF 68
DESCRIPTION: POWER_SYSTEM 5V_ALW&3.3V_ALW
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER : JEFF

1.5 Volt +/-5%
Design Current: 3.02A
Maximum current:4.31A
OCP point min. : 9.37A

1.05 Volt +/-5%
Design Current:12.42A
Maximum current:17.75A
OCP point min. 11.91A
(OCP point typ.: 15.71A)

TI request to change.



PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007 SHEET 55 OF 68	DESCRIPTION: POWER I/O 1.5VS & 1.05VS	SCHEMATIC FILE NAME : <OrgName> RELEASE DATE :	DESIGN ENGINEER : JEFF

TOTAL POWER=65W
-->3.34A

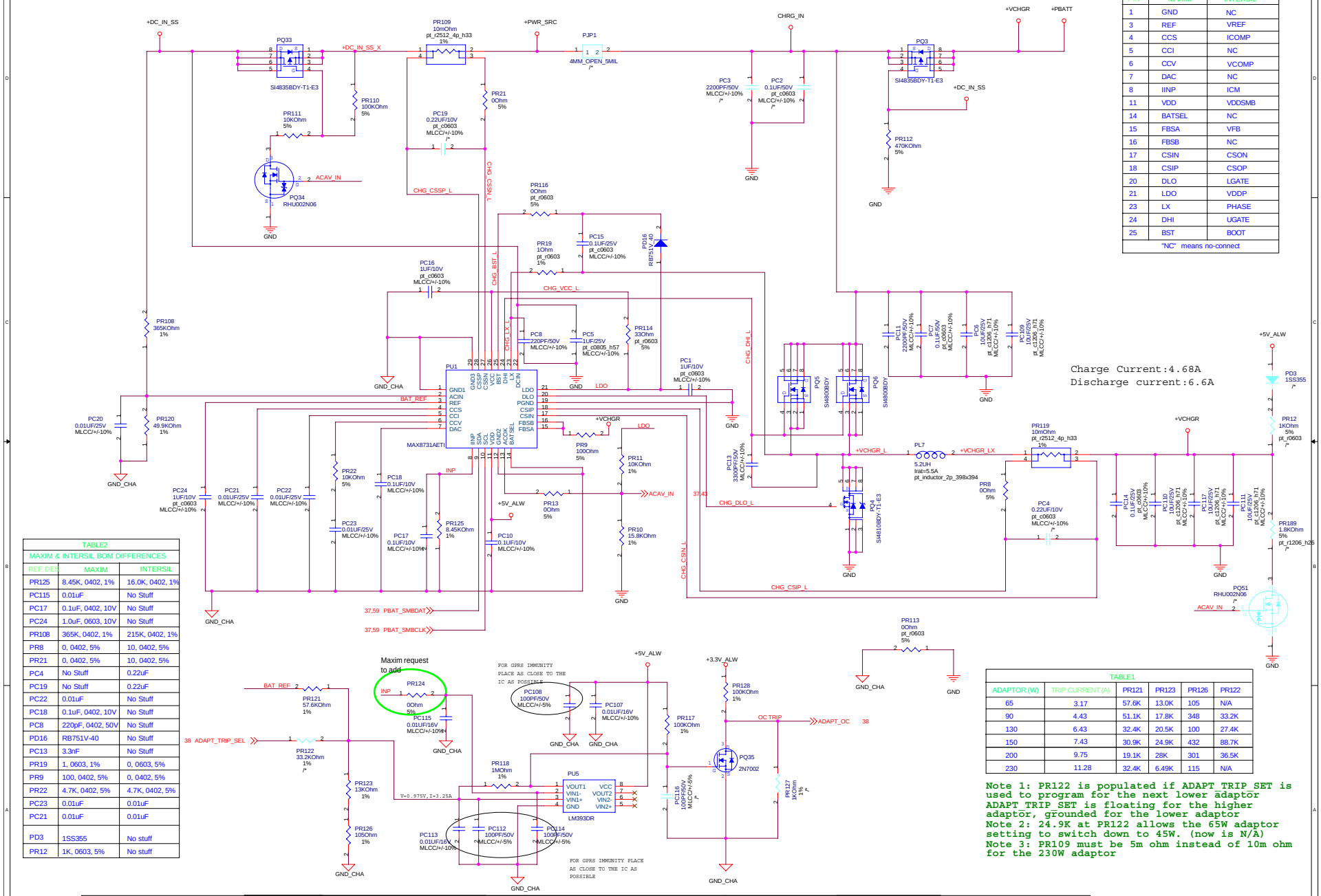


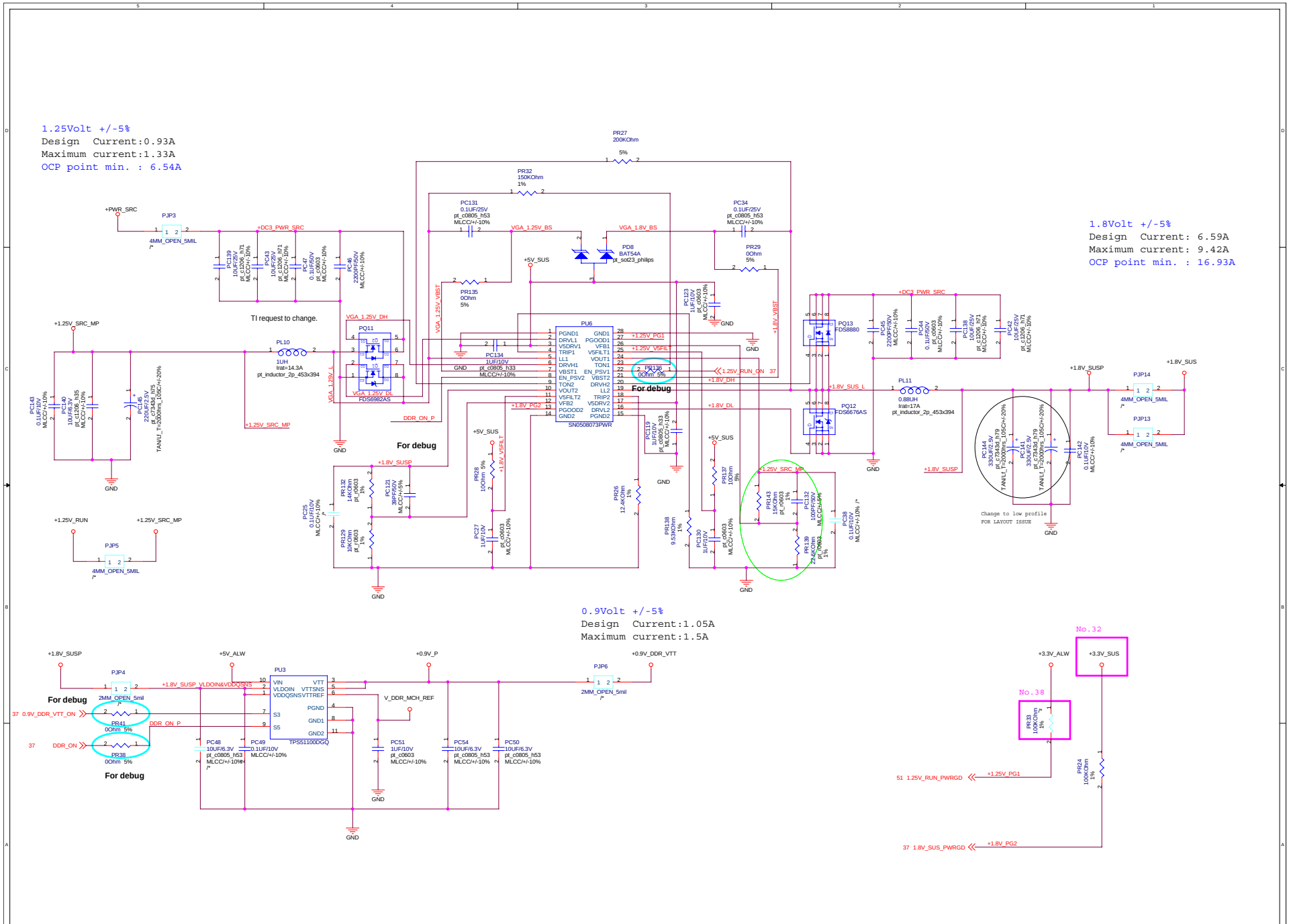
TABLE3		
PIN NAME DIFFERENCES		
PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT
"NC" means no-connect		

TABLE2		
MAXIM & INTERSIL BOM DIFFERENCES		
REF DES	MAXIM	INTERSIL
PR125	8.45K, 0402, 1%	16.0K, 0402, 1%
PC115	0.01uF	No Stuff
PC17	0.1uF, 0402, 10V	No Stuff
PC24	1.0uF, 0603, 10V	No Stuff
PR108	365K, 0402, 1%	215K, 0402, 1%
PR8	0, 0402, 5%	10, 0402, 5%
PR21	0, 0402, 5%	10, 0402, 5%
PC4	No Stuff	0.22uF
PC19	No Stuff	0.22uF
PC22	0.01uF	No Stuff
PC18	0.1uF, 0402, 10V	No Stuff
PC8	220pF, 0402, 50V	No Stuff
PD16	RB751V-40	No Stuff
PC13	3.3nF	No Stuff
PR19	1, 0603, 1%	0, 0603, 5%
PR9	100, 0402, 5%	0, 0402, 5%
PR22	4.7K, 0402, 5%	4.7K, 0402, 5%
PC23	0.01uF	0.01uF
PC21	0.01uF	0.01uF
PD3	1SS355	No stuff
PR12	1K, 0603, 5%	No stuff

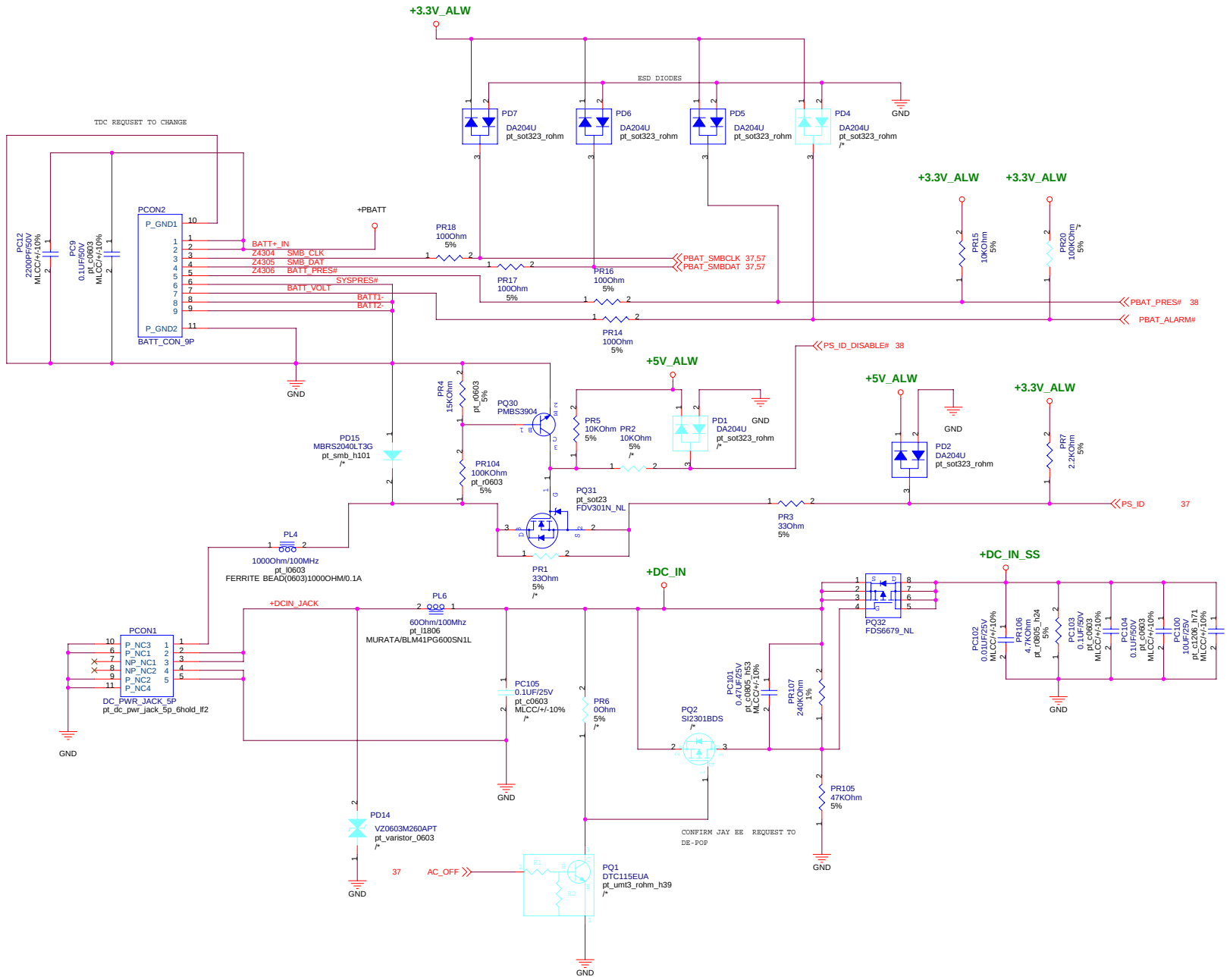
TABLE1					
ADAPTOR (W)	TRIP CURRENT (A)	PR121	PR123	PR126	PR122
65	3.17	57.6K	13.0K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28	32.4K	6.49K	115	N/A

Note 1: PR122 is populated if ADAPT_TRIP_SET is used to program for the next lower adaptor
ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor
Note 2: 24.9K at PR122 allows the 65W adaptor setting to switch down to 45W. (now is N/A)
Note 3: PR109 must be 5m ohm instead of 10m ohm for the 230W adaptor

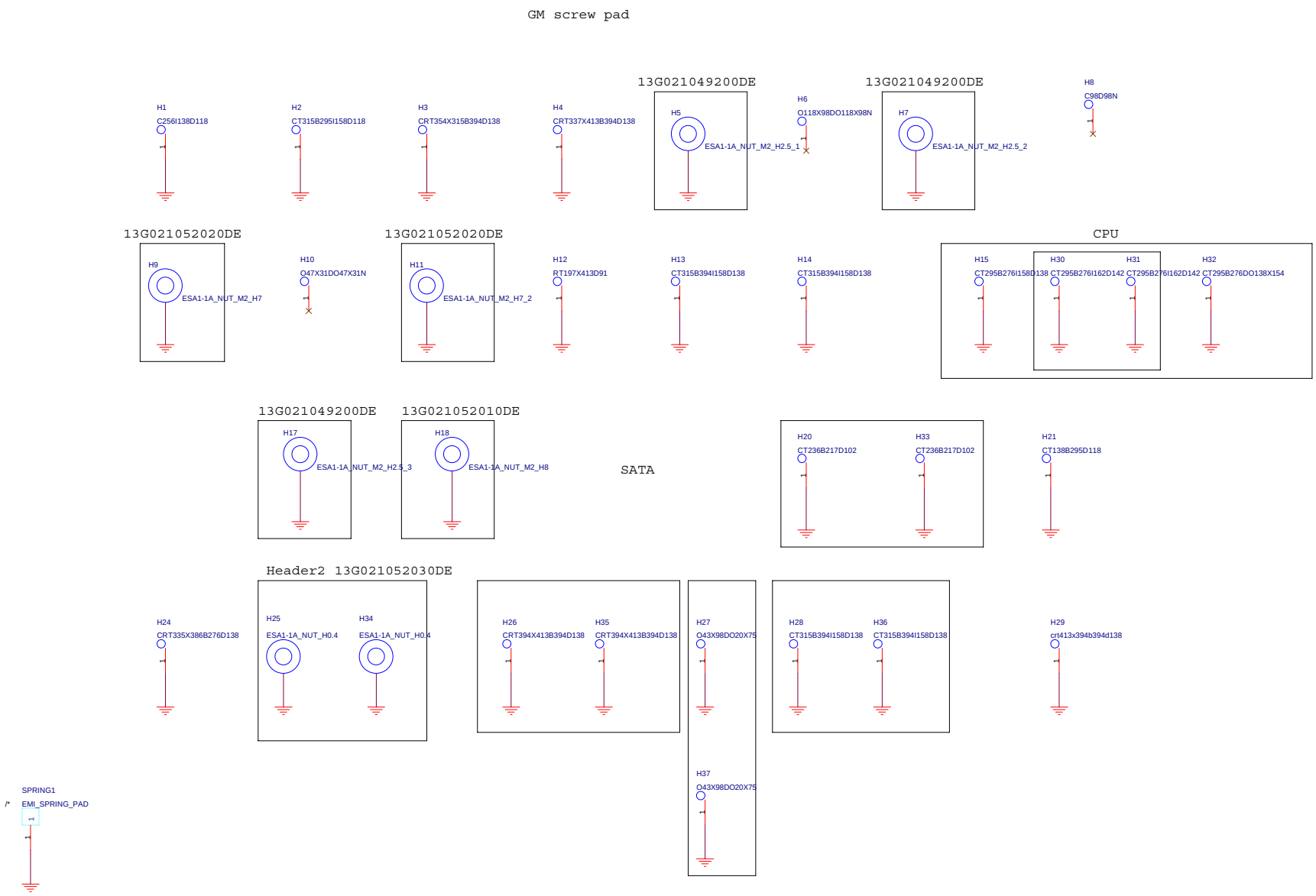
PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	SHEET 57 OF 68	DESCRIPTION: POWER_CHARGER	SCHEMATIC FILE NAME : <OrgName>	RELEASE DATE :	DESIGN ENGINEER : JEFF



PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: POWER VGA 1.25V & DDR & VTT	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Jeff
		SHEET 58 OF 68		RELEASE DATE :	



PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 59 OF 68	POWER_CONNECTOR	RELEASE DATE :		JEFF

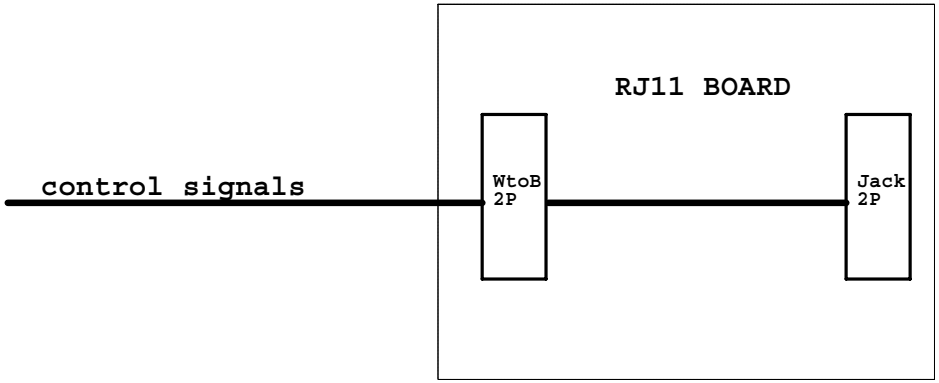


PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: SCREW PAD	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Sean Kuo
		SHEET 60 OF 68		RELEASE DATE :	

ASUS CONFIDENTIAL

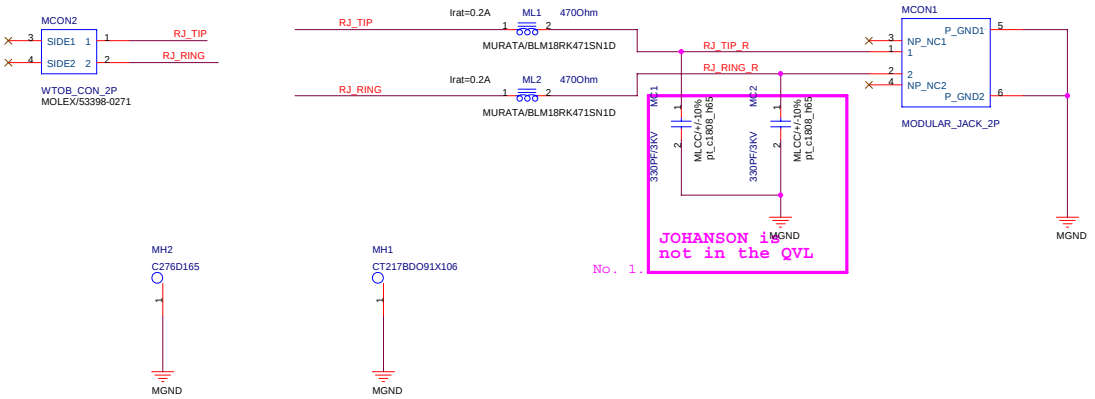
MODEL NAME : ***Elsa***

Lanai:Modem Board



REV : 1.1(DELL: X01)

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007** SHEET **64** OF **68**	DESCRIPTION: ***BLOCK DIAGRAM***	SCHEMATIC FILE NAME : RELEASE DATE :	DESIGN ENGINEER : ***Stanly Hsu***



PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007 SHEET 65 OF 68	DESCRIPTION: *RJ-11 CONN*	SCHEMATIC FILE NAME : <OrgName> RELEASE DATE :	DESIGN ENGINEER : *Stanly_Hsu*

ASUS CONFIDENTIAL

MODEL NAME : ***Elsa***

PCB NO : ***???***

ASUS P/N : ***???***

Lanai PP2 USB Board

REV : 1.1(DELL: X01)

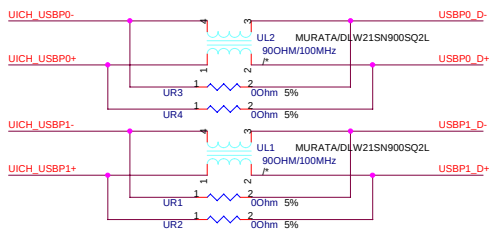
MB PCB

Part Number	Description
DA800004H0L	PCB 00B LA-3071P REV0 M/B

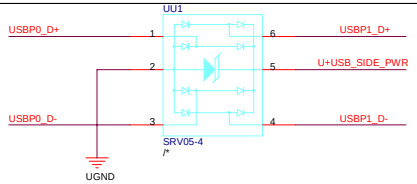
BOM NO. ???
PCB P/N: ???

PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007 SHEET 67 OF 68	DESCRIPTION: Cover Page	SCHEMATIC FILE NAME : RELEASE DATE :	DESIGN ENGINEER : Terry_Lin

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently .

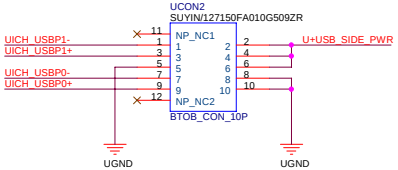


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

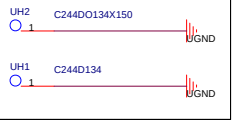


Place ESD diodes as close as USB connector. Semtech SRV05-4 can also be used but the Philips IP42220CZ6 have a lower input C (1pf vs 3pf).

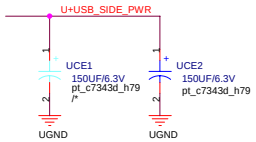
USB daughter board connector



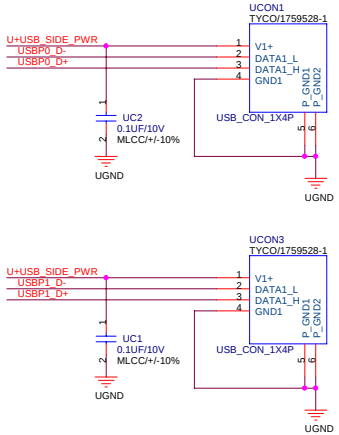
Screw hole



Place one 150uF cap by each USB connector



Each channel is 1A



Consult you ESD Engineer if you think you may need to add ESD Supression Components to your USB lines.
Add PADS ONLY until proven diodes are really needed.

PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *USB PORT (SINGLE * 2)*	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : *Terry_Lin*
		SHEET 68 OF 68		RELEASE DATE :	