


PAGE3;RESERVE RN65~71 P/L 49.9ohms for ICS951464
PAGE3;CHANGE R107,R108 from 47.5 ohms TO 0ohm;Need CHECK!!
PAGE14;CHANGE LCD1;PIN27 TO TP105;RESERVE FOR LIGHT SENSOR
PAGE14;CHANGE LCD1;PIN24 TO 5V POWER RAIL FOR LED DRIVER BOARD IC ENABLE PIN(HIGH ACTIVE)
PAGE14;CHANGE F1 TO 4A
PAGE14;P/U TMDS DDC DAT TO 3D3V S0,ADD R471
PAGE15;CHANGE R184,R185,R188 FROM 75ohms TO 150 ohms
PAGE19;SWAP USB PAIR OF FT AND MINICARD

PAGE27;CHANGE Q11 TO 84.00143.B1K
PAGE30;CHANGE C389,C390 TO 1uF,X5R
PAGE30;CHANGE R450,R453 TO 14Kohms
PAGE30;CHANGE R459,R463 TO 40.2ohms
PAGE30;CHANGE R458,R462 TO 33ohms
PAGE31;ADD R472 AND P/H TO 3D3V S0 FOR CAPA INT#
PAGE31;CHANGE R347 TO 4.7Kohms(E51_TxD P/L)-

- PAGE31
- 1.KBC Beep change from A_PWM0(32) to GPIO56(31)
 - 2.Power LED change from GPIO32(65) to A_PWM0(32)
 - 3.e-Button LED change from GPIO43(20) to A_PWM1(118)

LAYOUT

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title Change List			
Size A	Document Number Ferrari 7		Rev SA
Date:	Thursday, August 02, 2007	Sheet	1 of 47

Ferrari 7 Block Diagram

Friday Practice (SA)
Saturday Practice (SB)
Qualifying (SC)
Race (-1)

2006/04/17

Project code:
PCB P/N :
REVISION :

ezDockII/II+

USB/Express
Card/MediaBay/1394*2port
RJ45/RJ11/PS2*2/Serial
Port/Parallel
Port/CRT/TV/DVI-D/SPDIF/MC
in/Line in/Line out/AC Jack

PCB Layer Stackup

L1: Component
L2: GND
L3: Signal
L4: VCC
L5: Signal
L6: Signal
L7: GND
L8: Component

CPU V_CORE
ISL6264 38/39

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC
TPS51124 47

INPUT	OUTPUT
DCBATOUT	ID2V_S0 ID8V_S3

SYSTEM DC/DC
ISL6236 46

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO
TPS51100 48

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO
APL5915 48

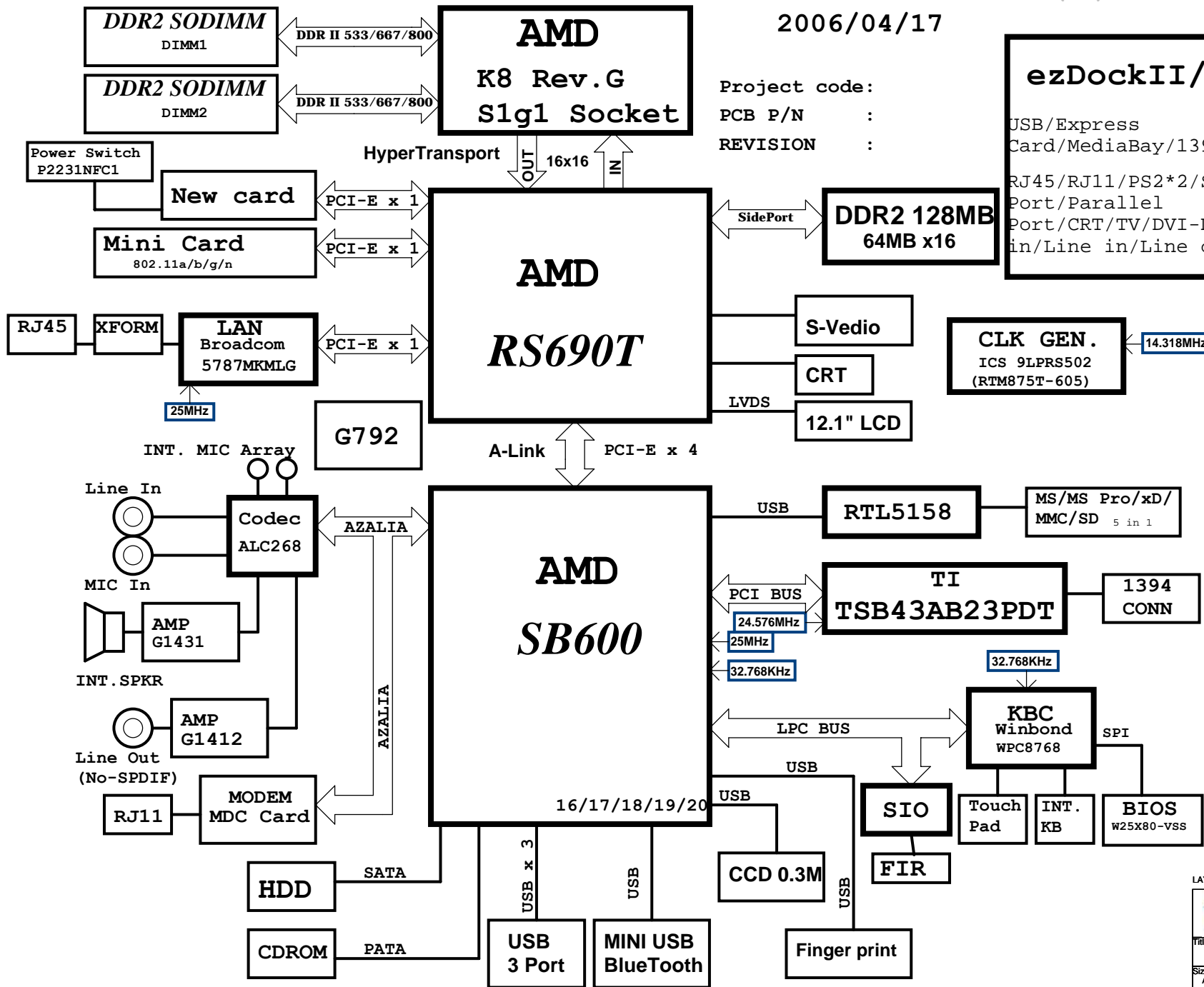
INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	ID2V_S5 2D5V_S0 ID5V_S0

SYSTEM LDO
ISL6236 46

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger
ISL6255 42

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT



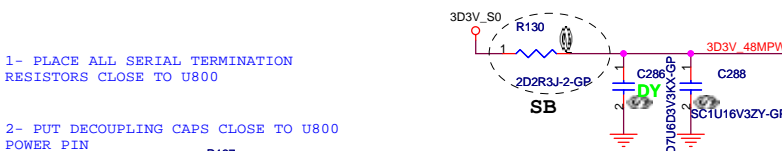
LAYOUT

wistron Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

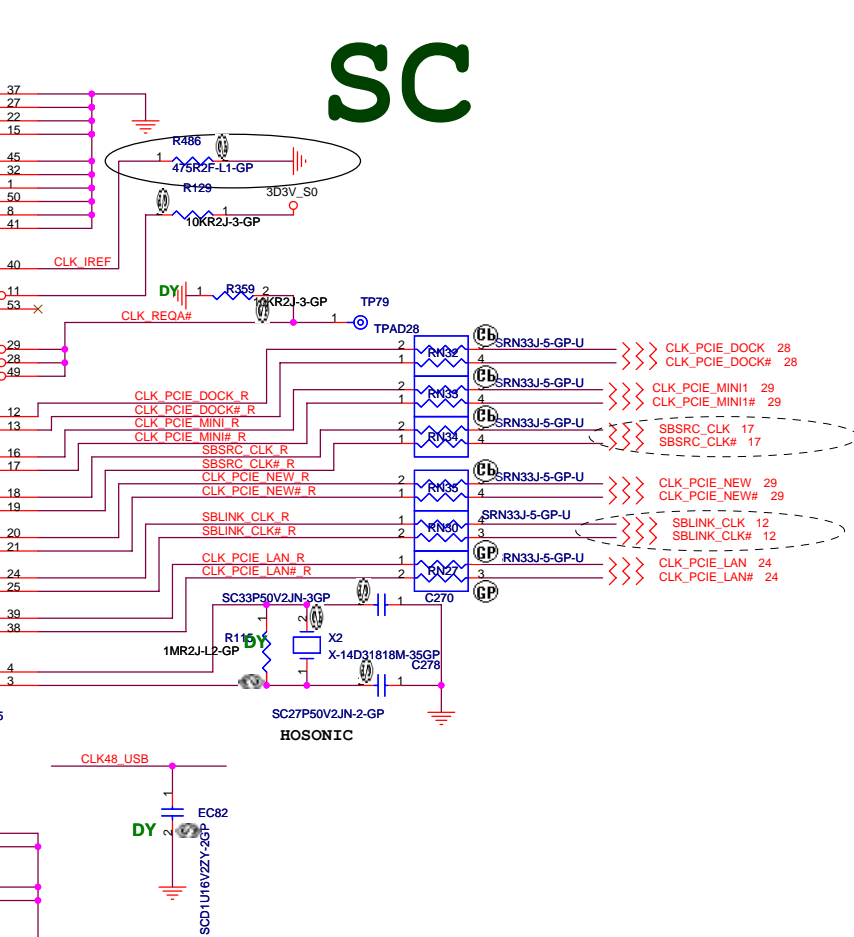
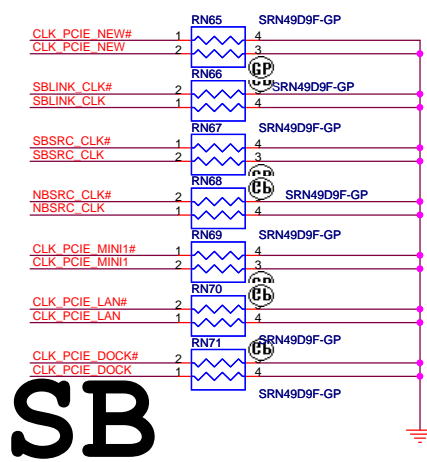
Title: **Interactive Circuit Map**

Size: A3 Document Number: **Ferrari 7** Rev: SA

Date: Thursday, August 02, 2007 Sheet: 2 of 47



FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation



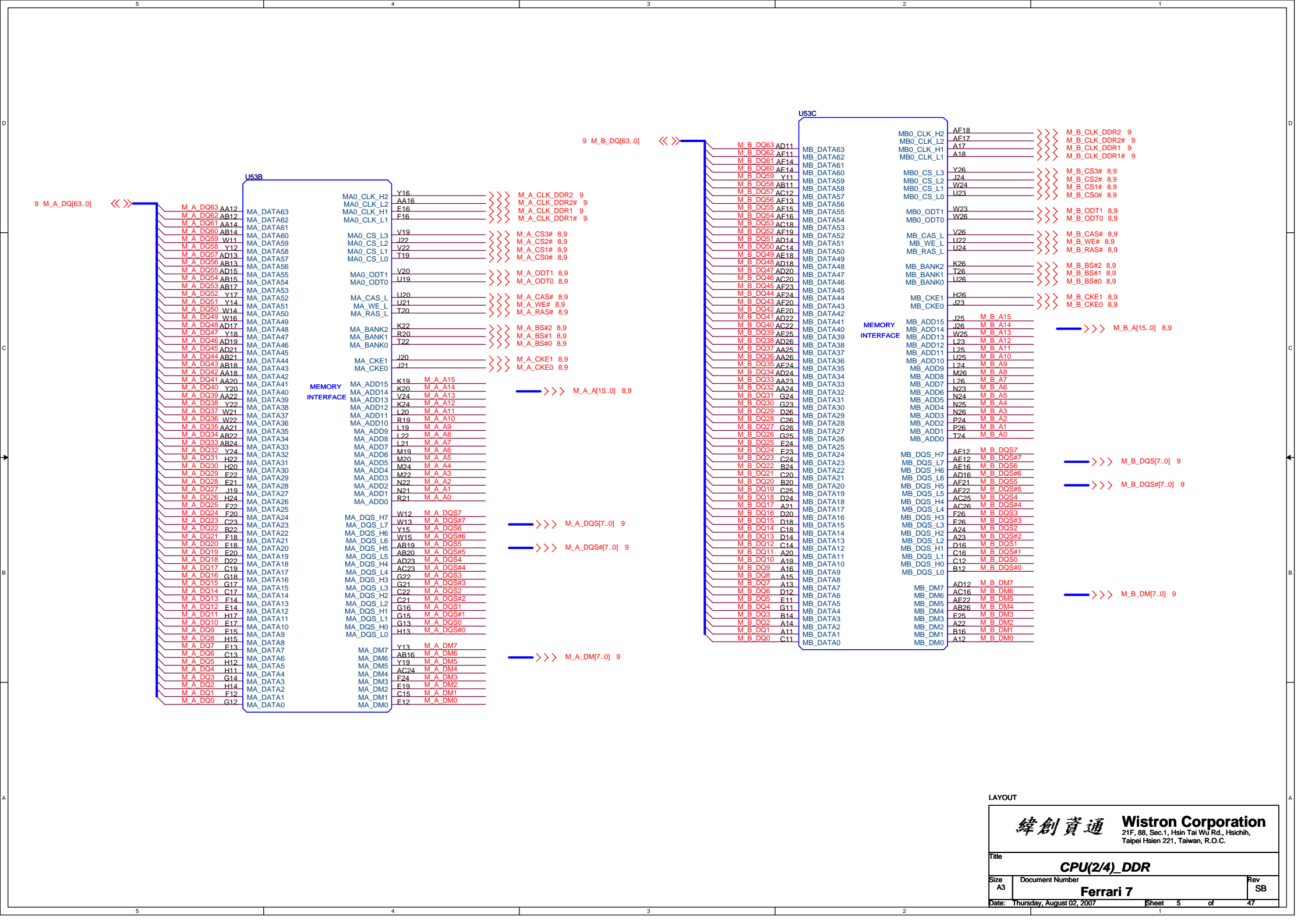
SC

CLK PCIE DOCK

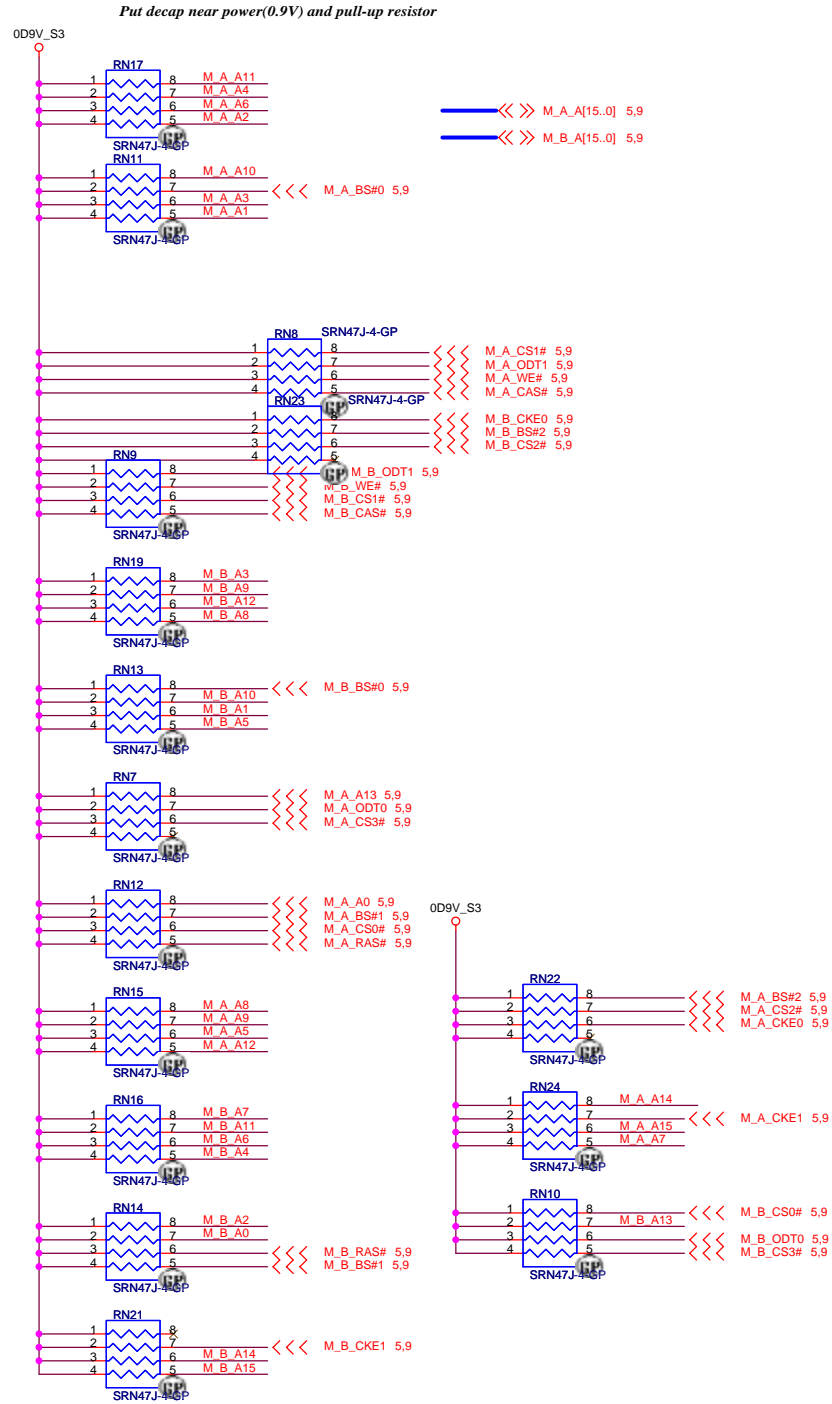
SB

		Wistron Corporation 21F, 88, Sec.1, Hsien Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CLKGEN_IC951464			
Size A3	Document Number	Rev SB	
Ferrari 7			
Date	Thursday, August 02, 2007	Sheet	3 of 47

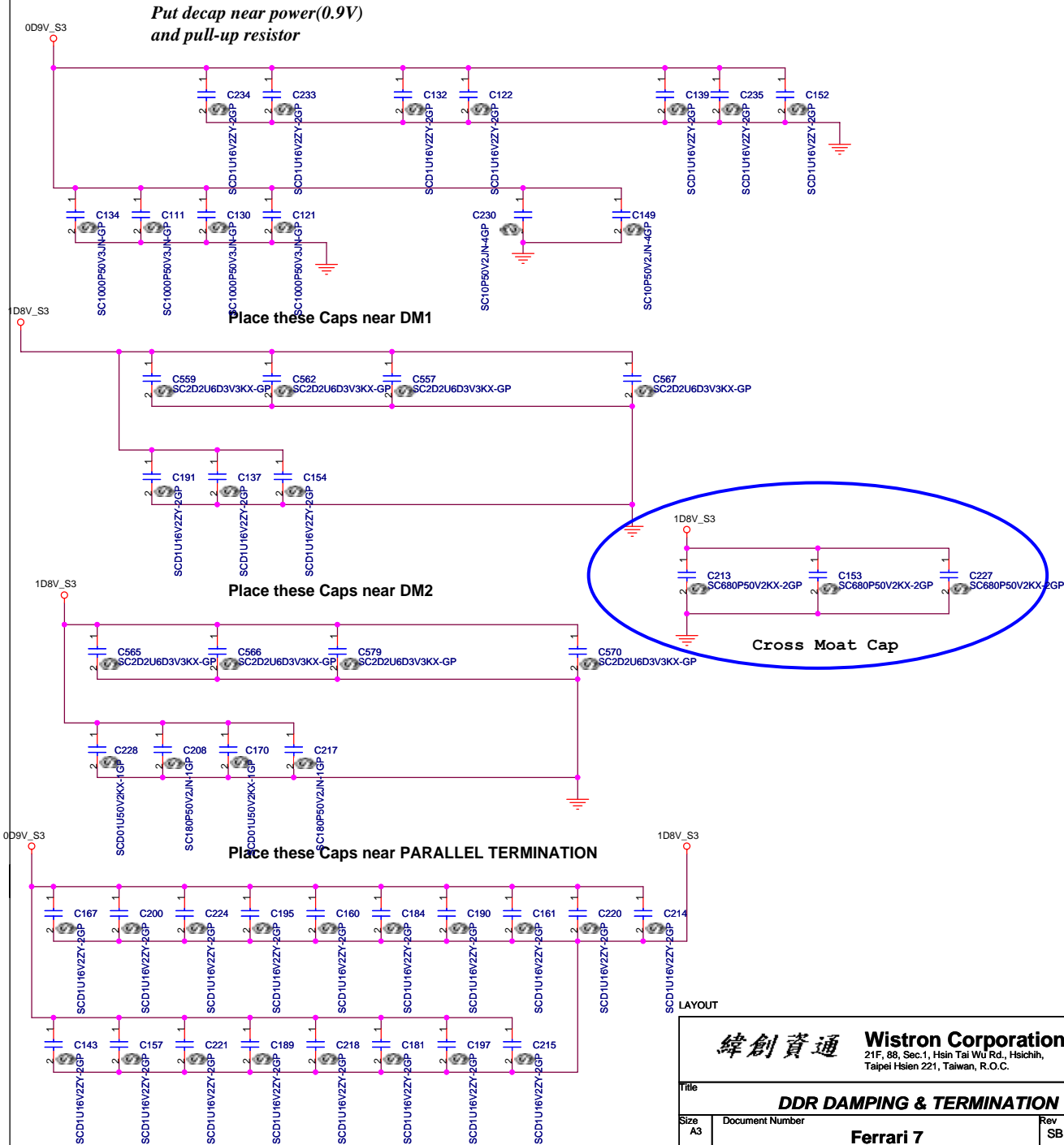




PARALLEL TERMINATION

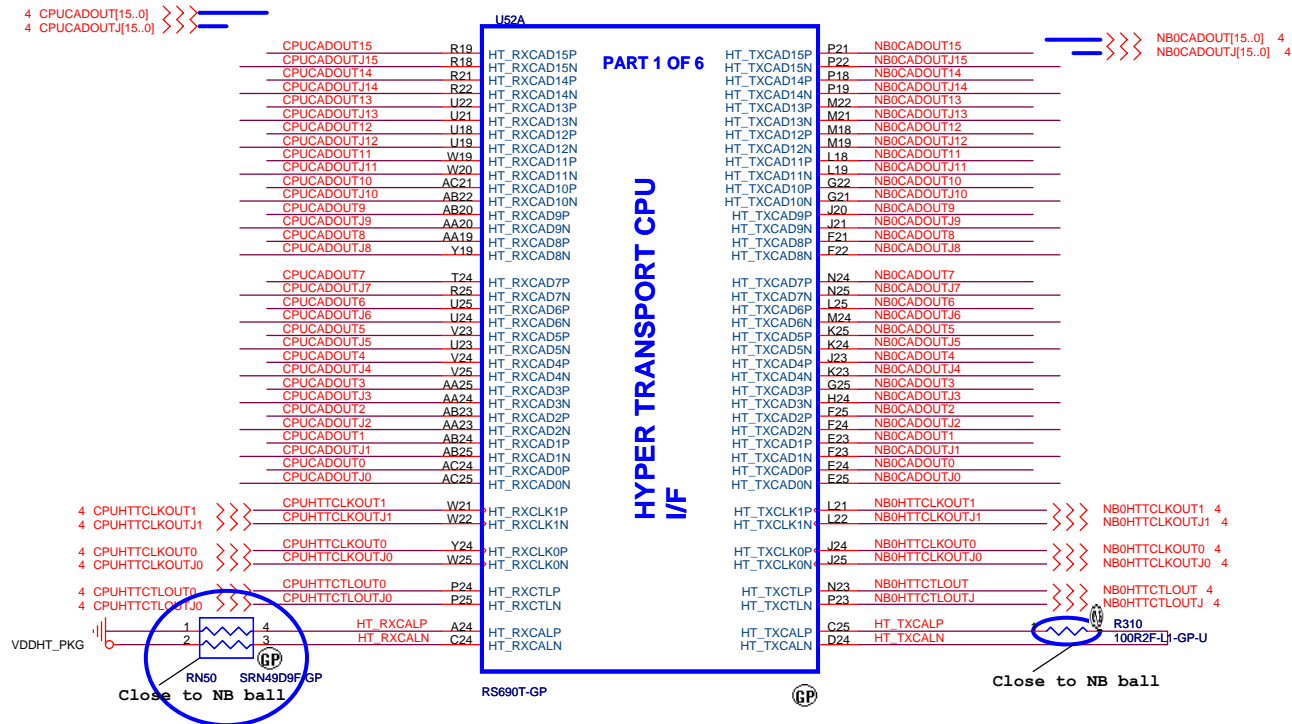


Decoupling Capacitor



CLAW HAMMER TO NB

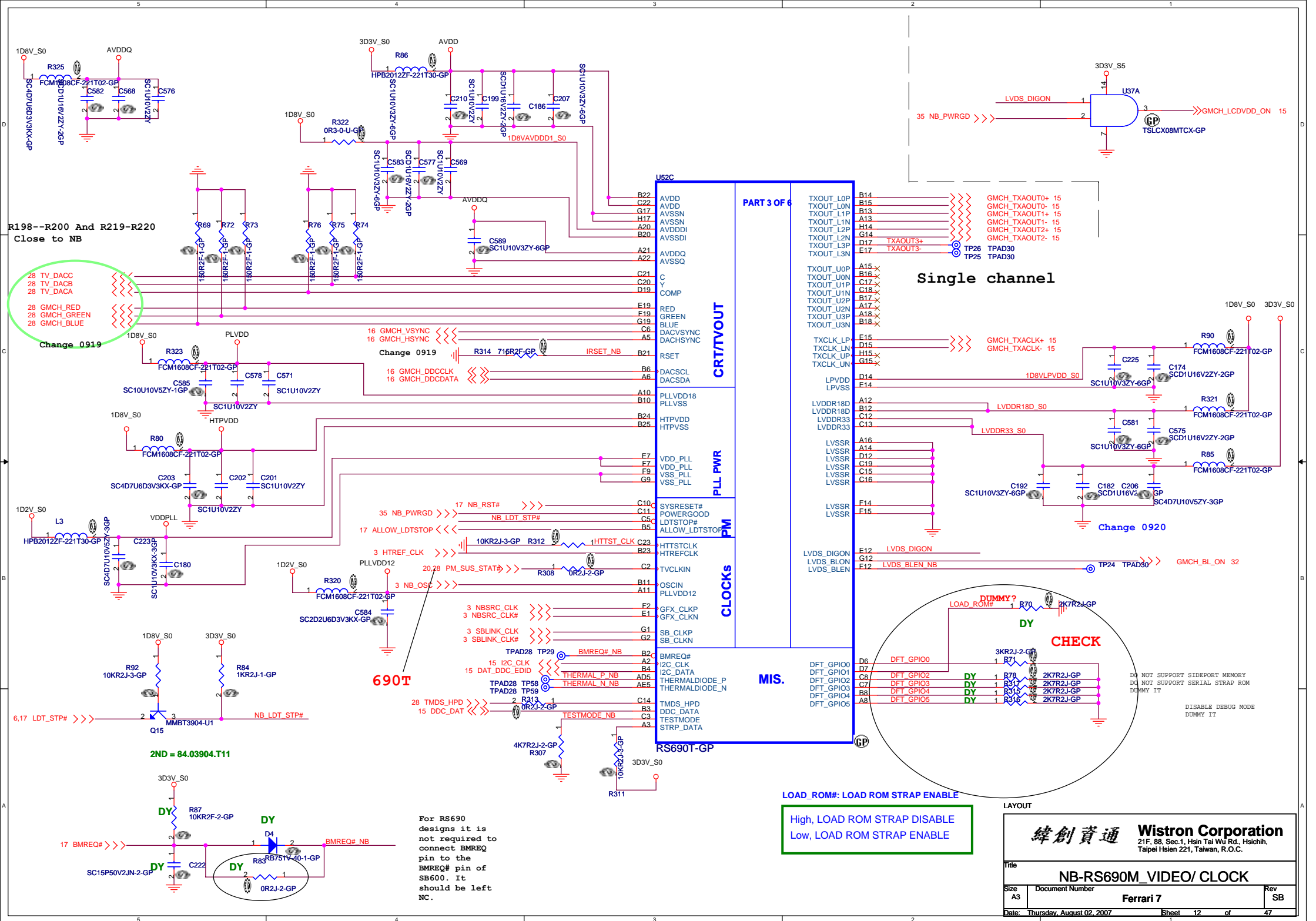
NB TO CLAW HAMMER

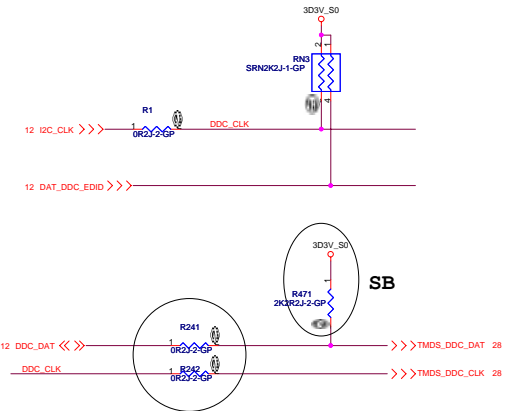
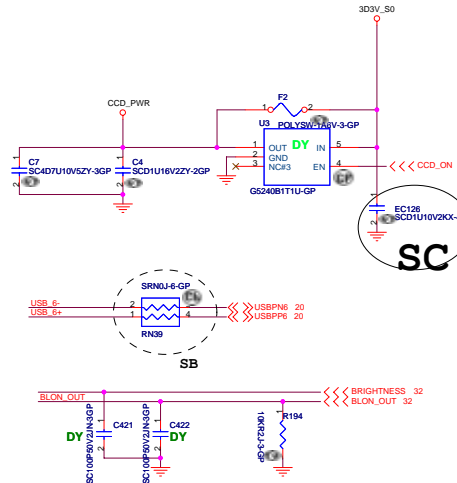
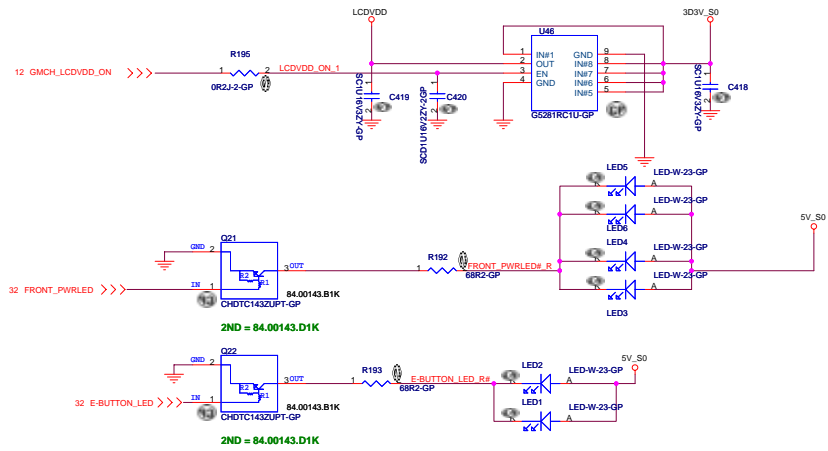


LAYOUT

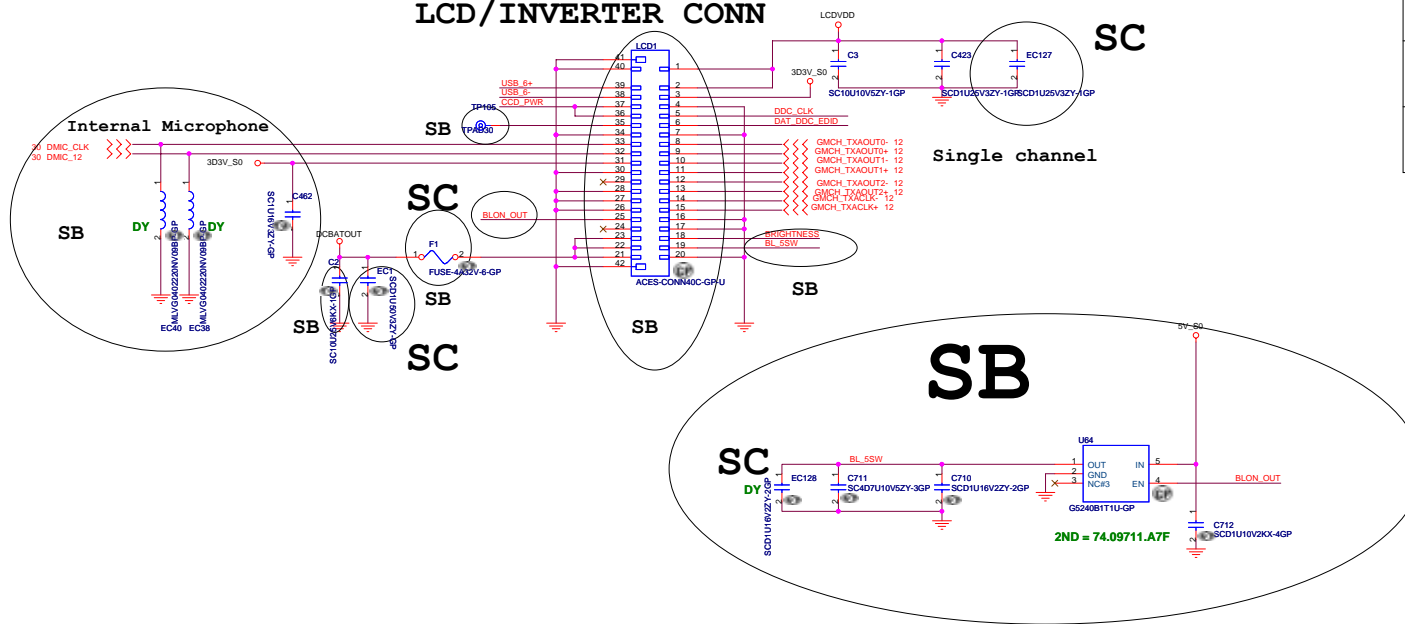
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			NB-RS690T HT	
Size	Document Number	Ferrari 7		Rev
A3				SB
Date: Thursday, August 02, 2007		Sheet	10 of 47	





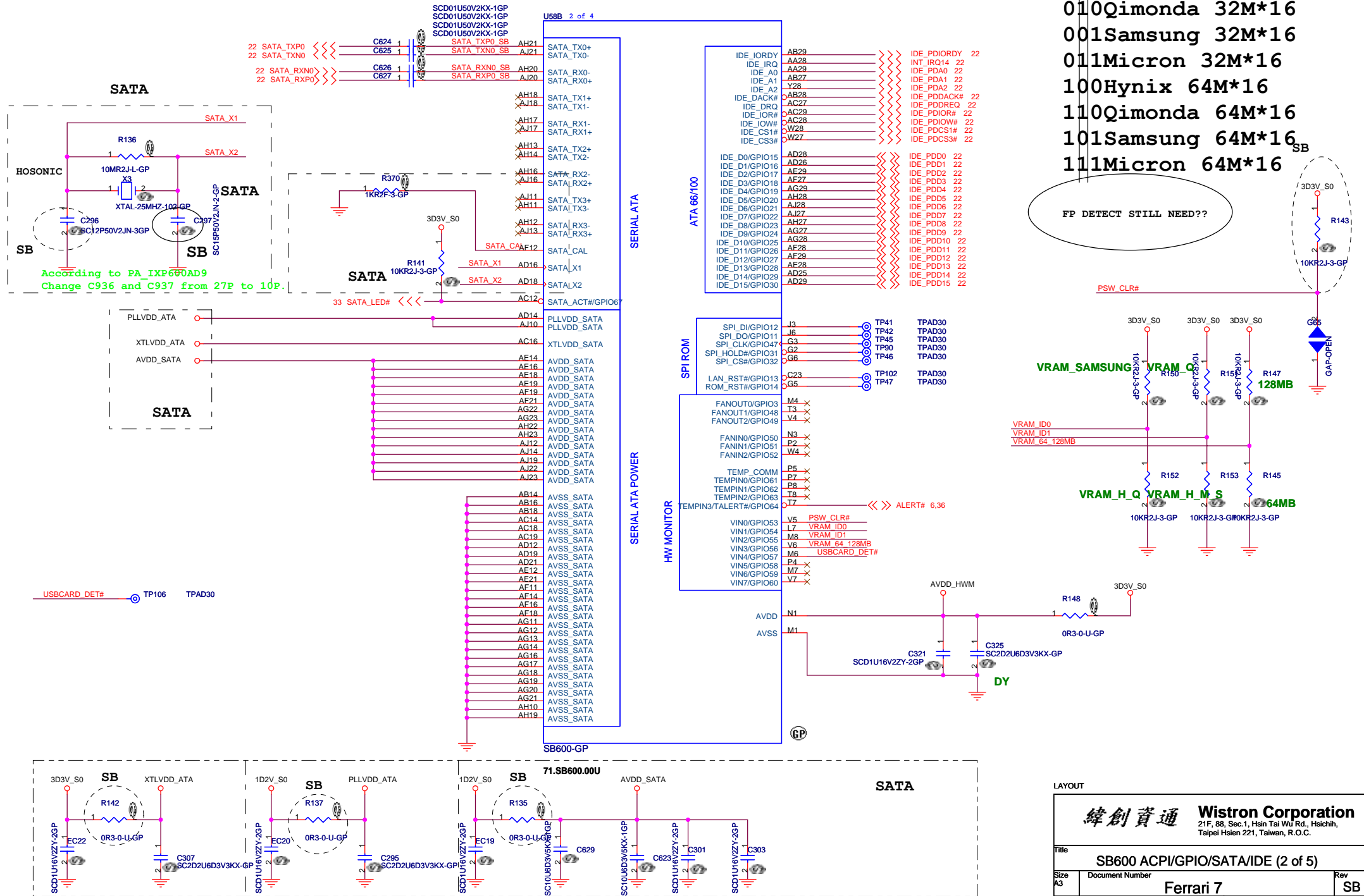
LCD/INVERTER CONN

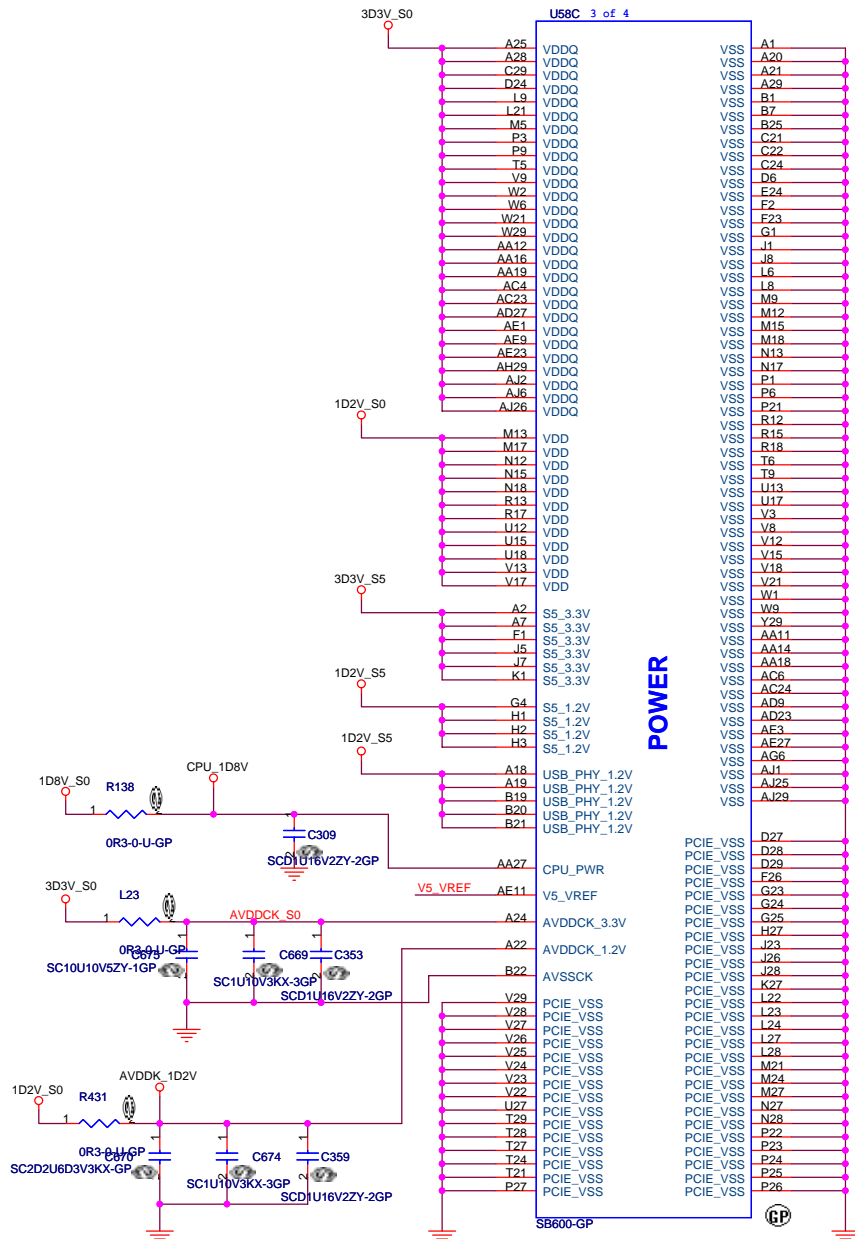
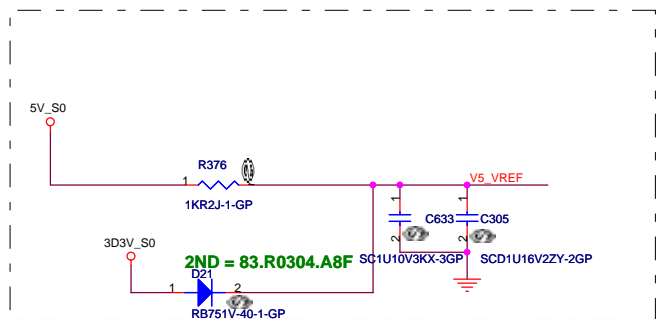
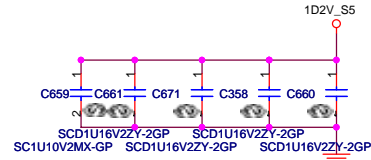
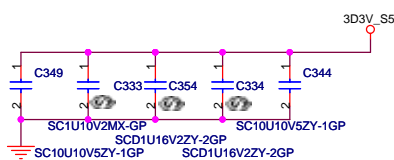
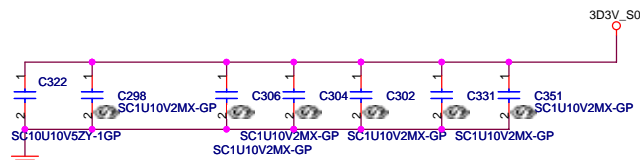
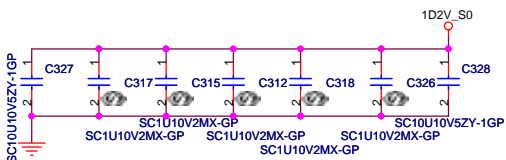


	LVDS	TMDS
I2C_CLK	I2C_CLK	I2C_CLK
I2C_DATA	I2C_DATA	
DDC_DATA		DDC_DATA

LAYOUT



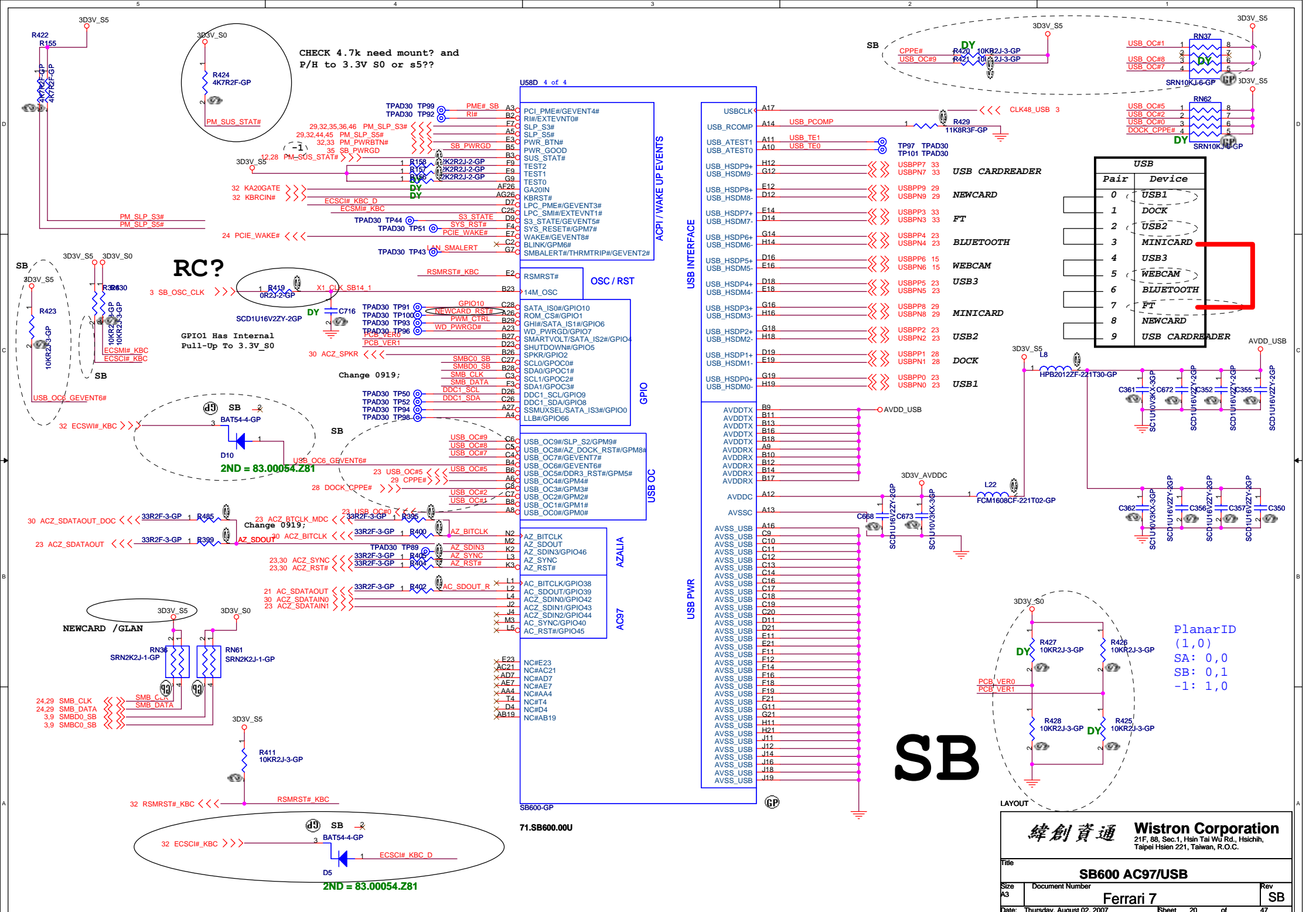




71.SB600.00U

LAYOUT

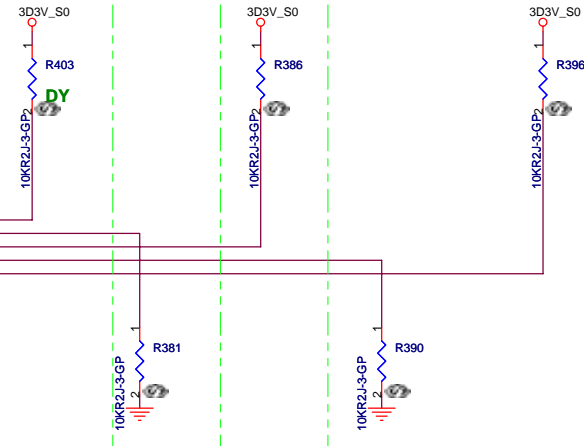
緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.		
Title SB600 POWER/DECOUPLING		
Size A3	Document Number	Rev SB
Date: Thursday, August 02, 2007 Sheet 19 of 47		



USB	
Pair	Device
0	USB1
1	DOCK
2	USB2
3	MINICARD
4	USB3
5	WEBCAM
6	BLUETOOTH
7	FT
8	NEWCARD
9	USB CARDREADER

PCI_CLK4
PCI_CLK6
PCI_CLK0
PCI_CLK1

20 AC_SDATAOUT
17,32 PCLK_KBC
17 CLK33_LPCROM
17,28 PCI_CLK0
17,26 PCLK_PCM



REQUIRED SYSTEM STRAPS

SB600					
	AC_SDOOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4	DEFAULT	

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]

DEBUG STRAPS

	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW				USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

LAYOUT

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

SB600 STRAPPING PIN

Size A3

Document Number

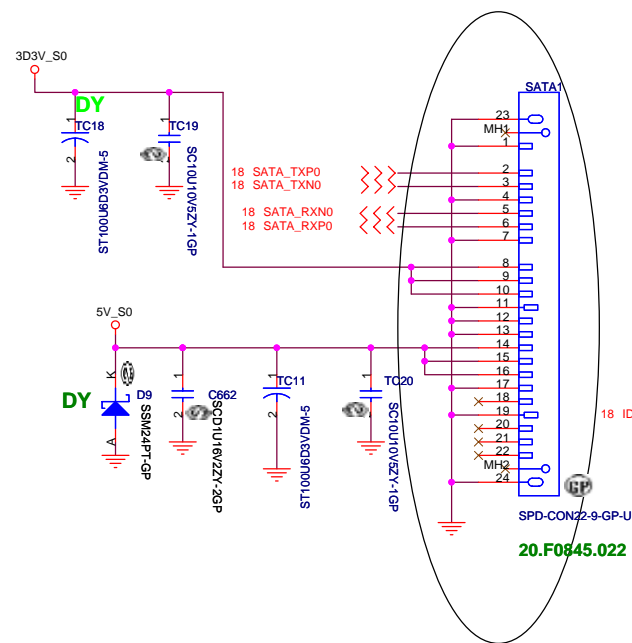
Ferrari 7

Rev SB

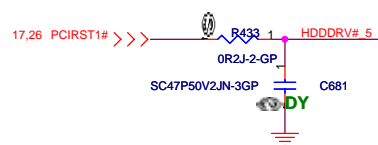
Date: Thursday, August 02, 2007

Sheet 21 of 47

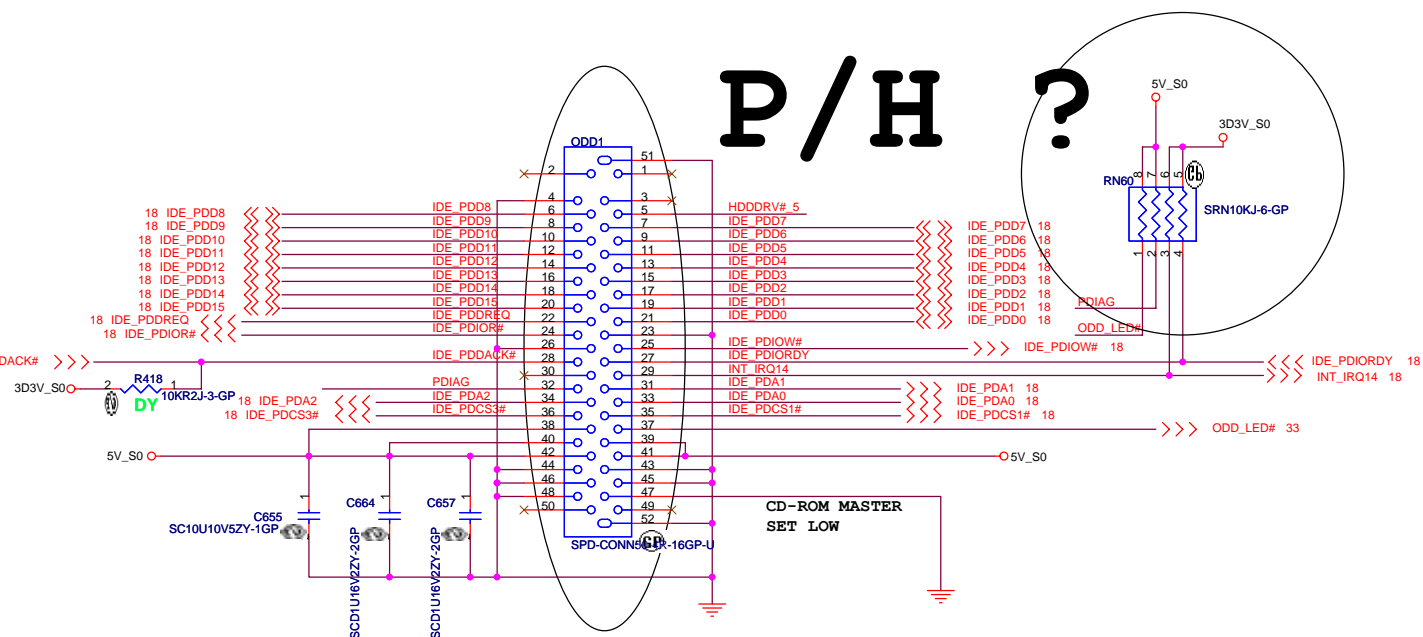
SATA HD Connector



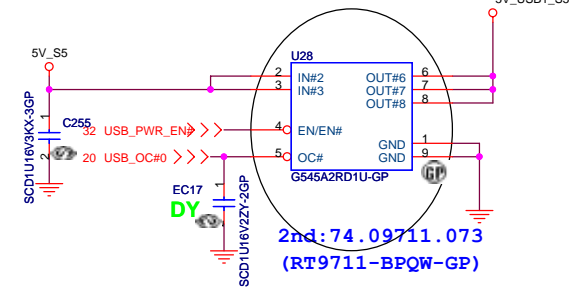
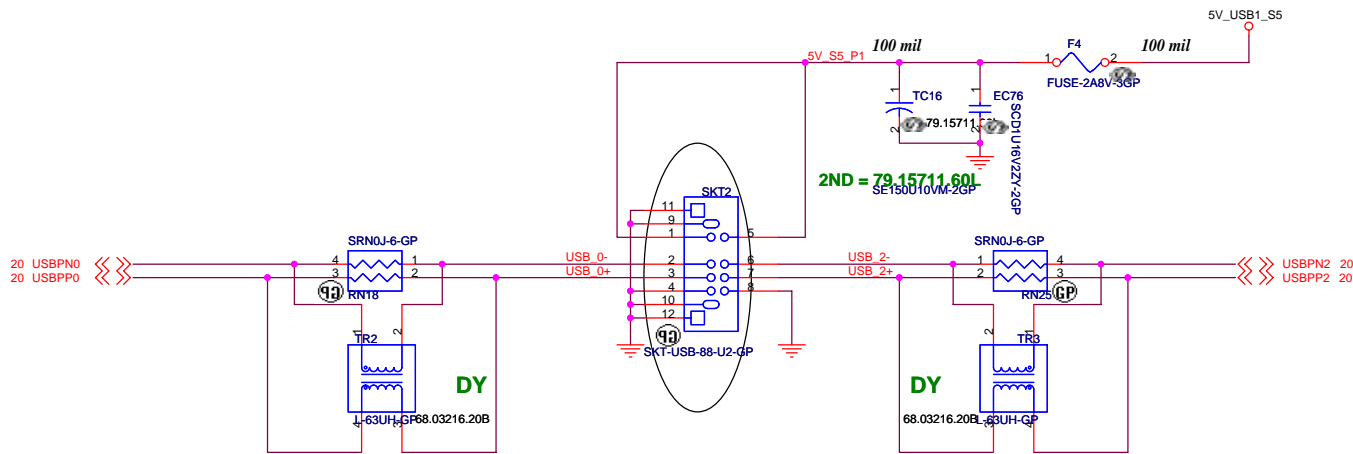
HDD Connector



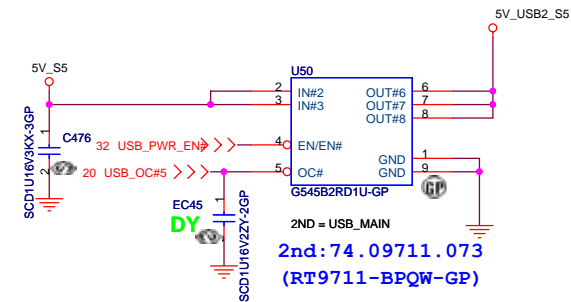
CD-ROM Connector



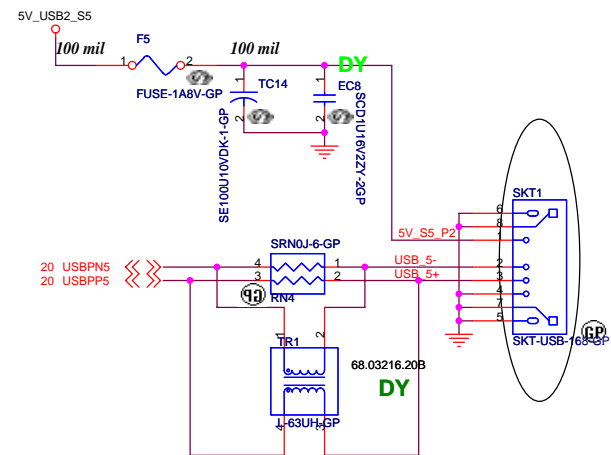
SB



SB



2nd: 74.09711.073
(RT9711-BPQW-GP)

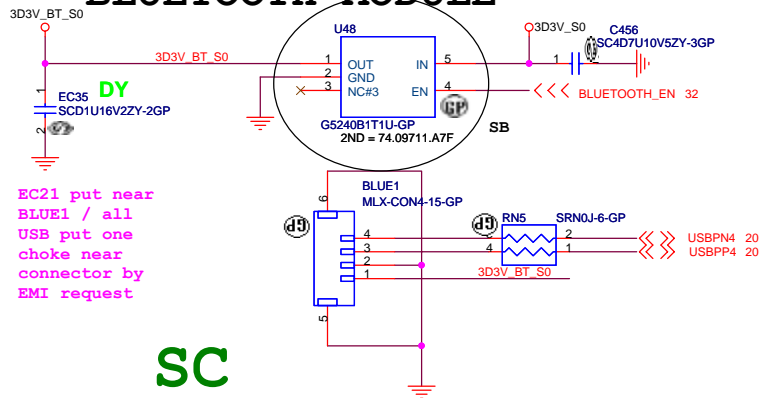


LAYOUT

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
USB / MDC / BLUETOOTH			
Size	Document Number		Rev
	Ferrari 7		SB
Date:	Thursday, August 02, 2007	Sheet	23 of 47

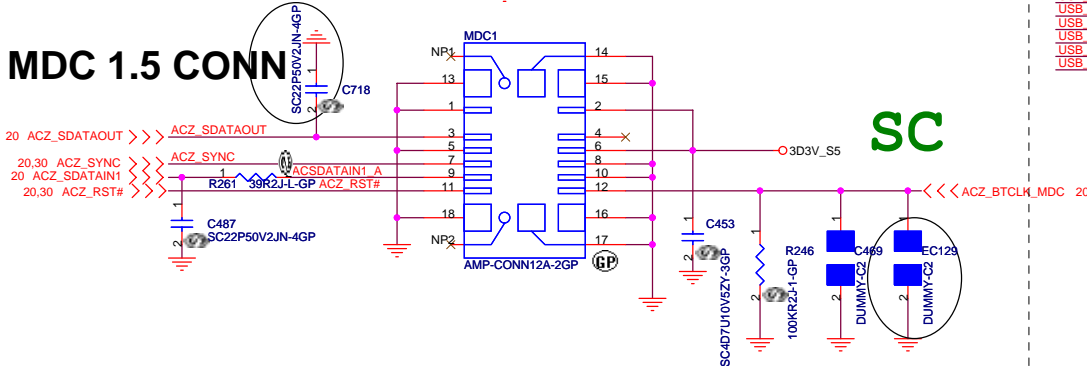
BLUETOOTH MODULE



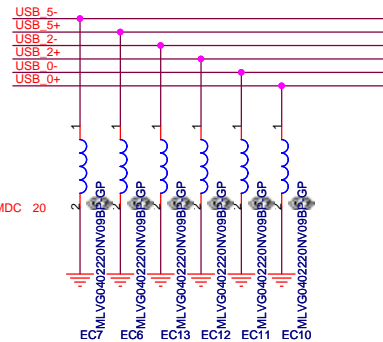
EC21 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request

SC

MDC 1.5 CONN

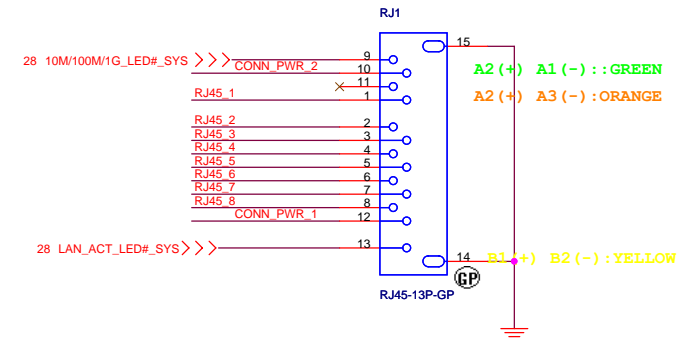
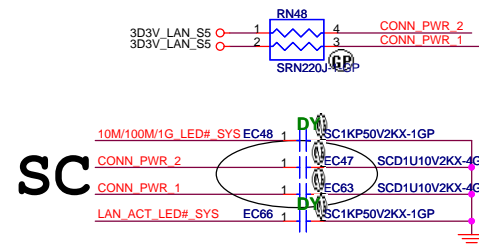


SC

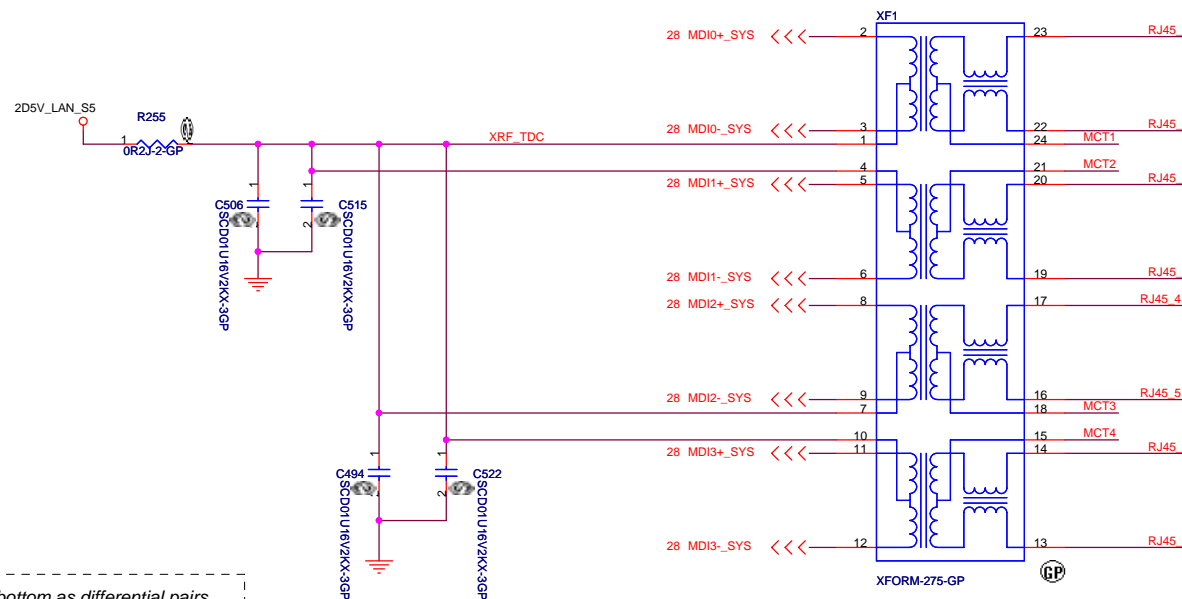


DY DY DY DY DY DY

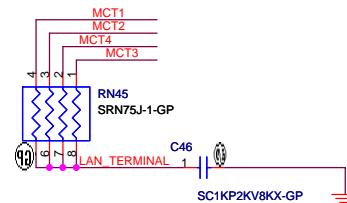
LAN Connector



GIGA Lan Transformer



- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.



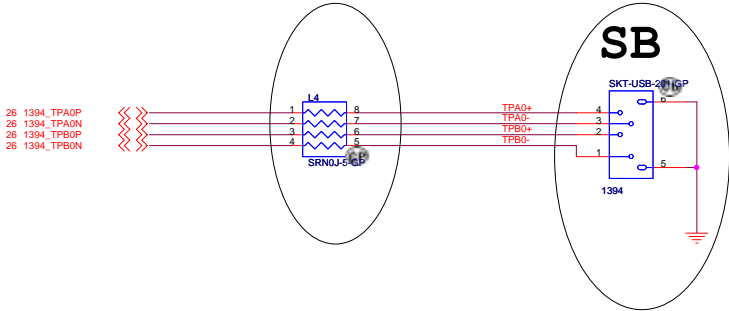
10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

LAYOUT

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

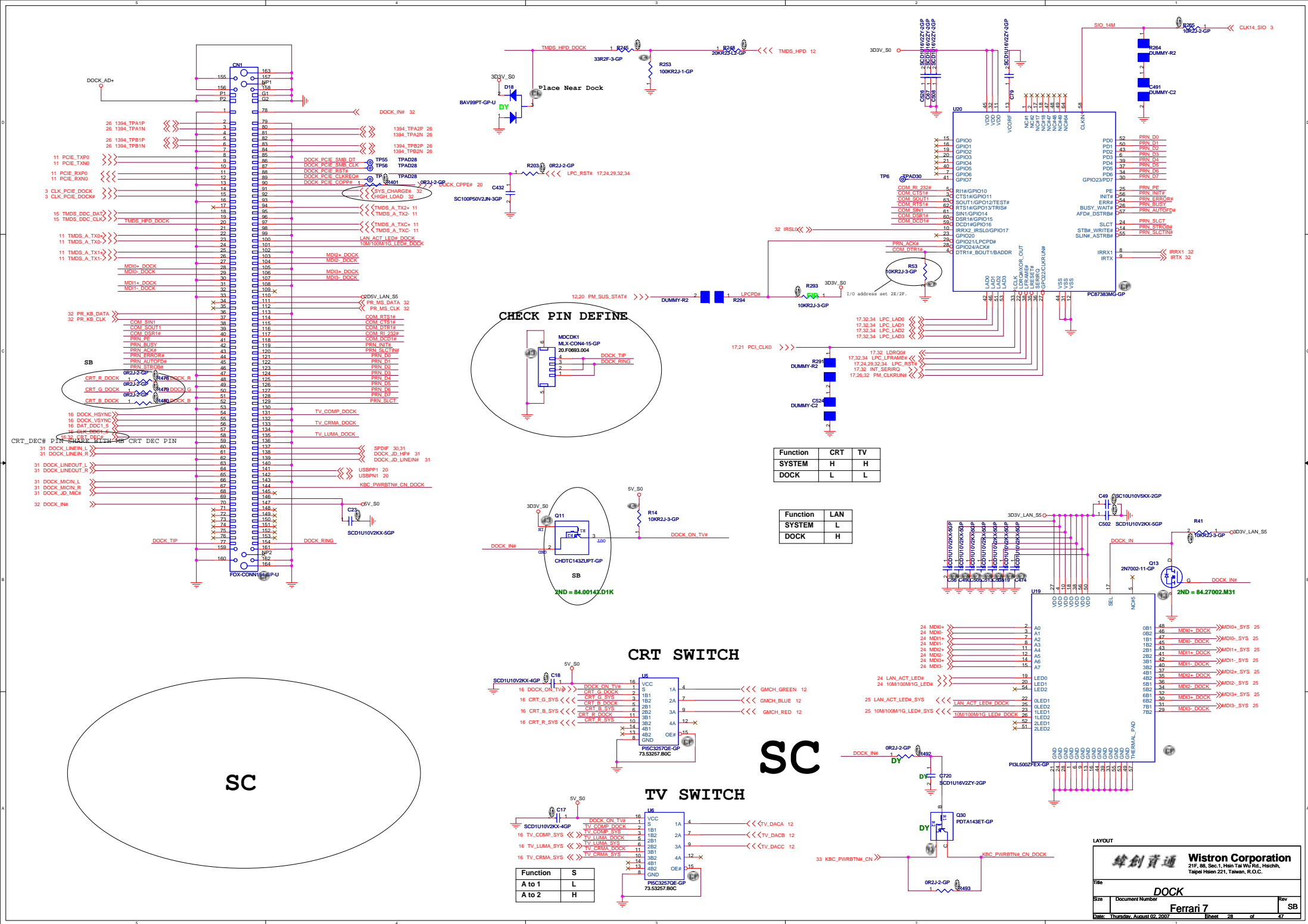
Title
LAN Connector
Size A3 Document Number
Ferrari 7
Date: Thursday, August 02, 2007 Sheet 25 of 47 Rev
SB

1394 Connector



LAYOUT

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsiehshih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
PCMCIA / 1394 / CARD READER			
Size	Document Number		Rev
	Ferrari 7		SB
Date:	Thursday, August 02, 2007		
	Sheet	27 of	47



SB

NEWCARD Connector

Reserve the symbol
for bottom side
connector

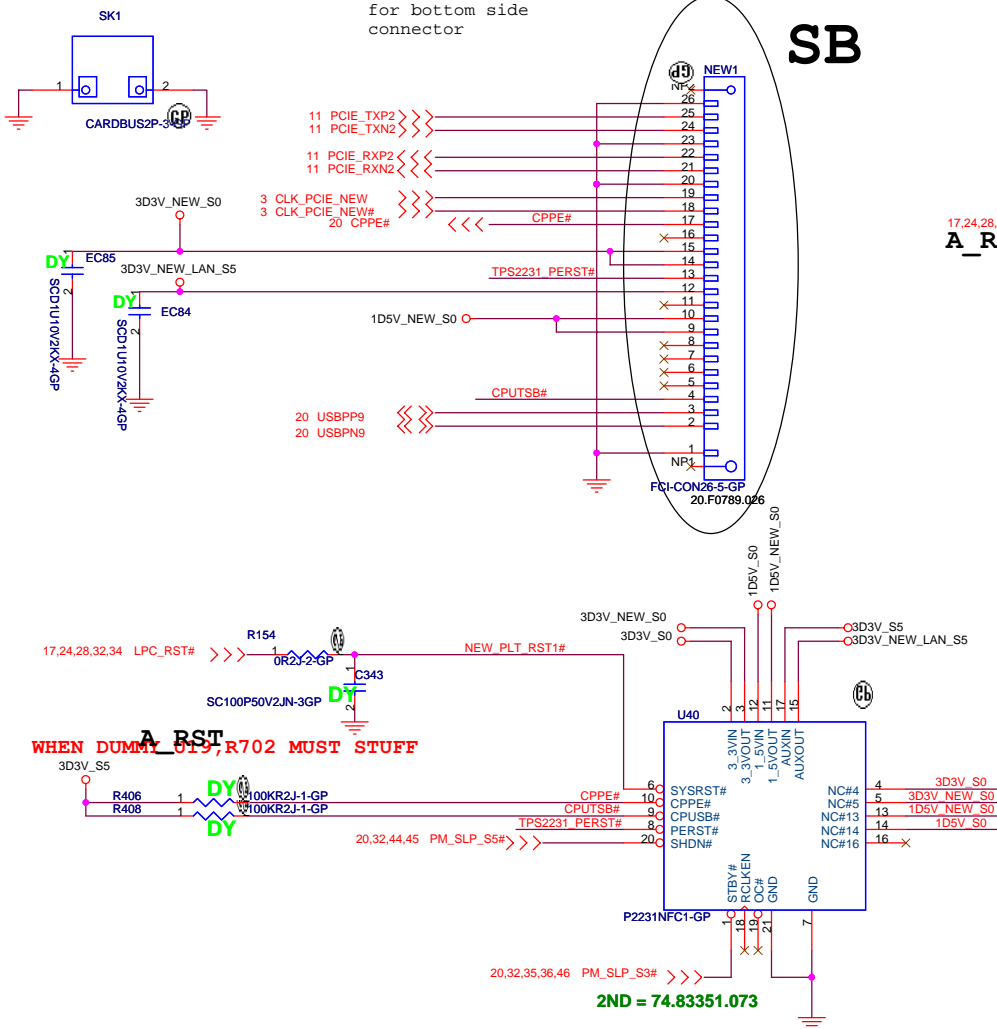
SB

Mini Card Connector

CHECK /POWER PIN

SB

SC

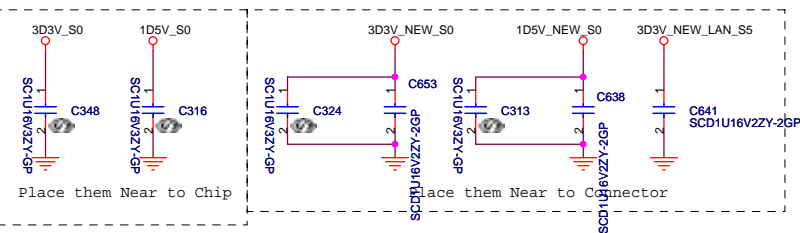


A_RST

WHEN DUMMY U19, R702 MUST STUFF

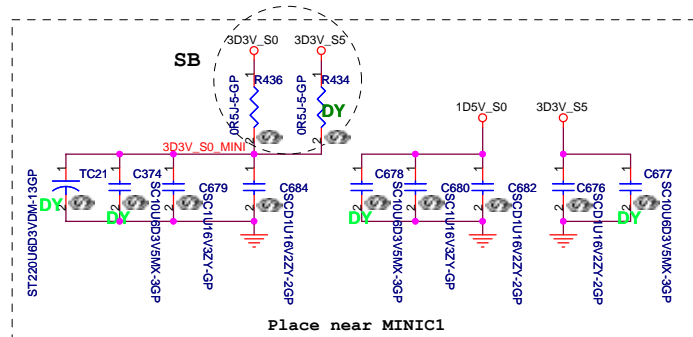
2ND = 74.83351.073

CHECK WITH COLUMBIA



Place them Near to Chip

Place them Near to Connector



Place near MINIC1

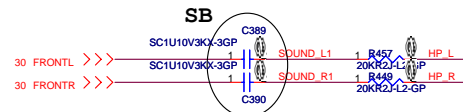
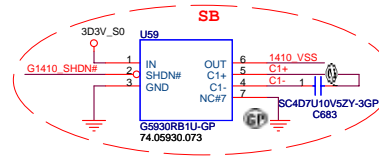
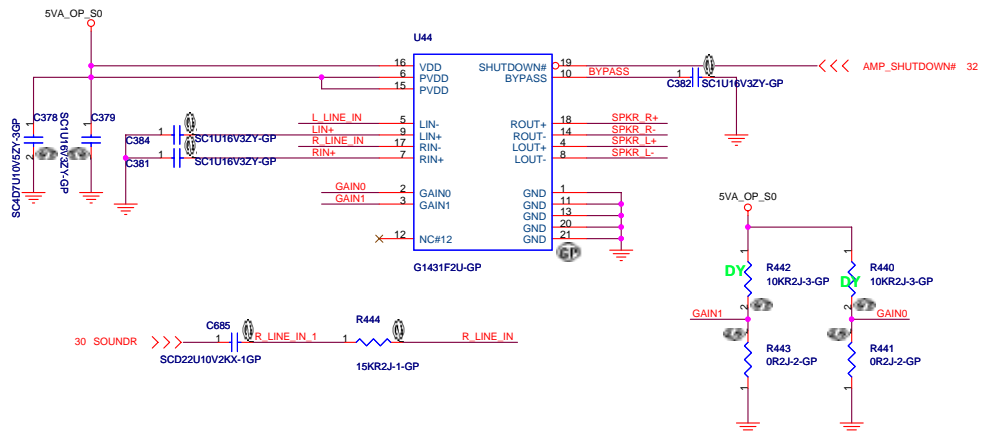
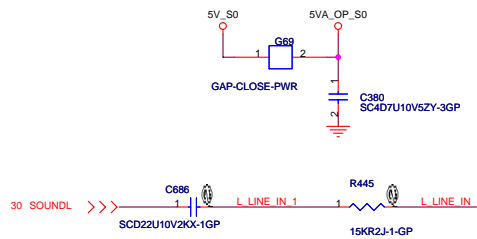
LAYOUT

緯創資通

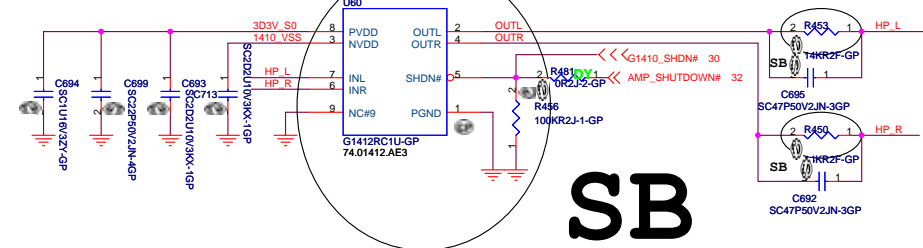
Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

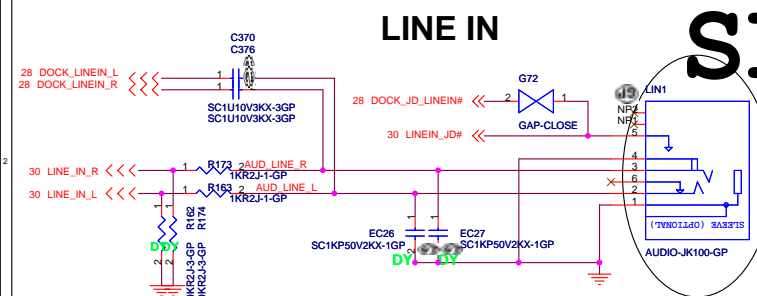
Title		
MINI CARD / NEW CARD		
Size	Document Number	Rev
Ferrari 7		SB
Date: Thursday, August 02, 2007	Sheet	29 of 47



-1_0624



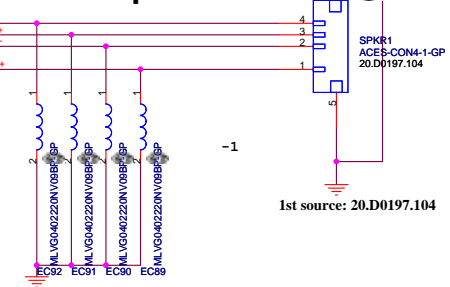
SB



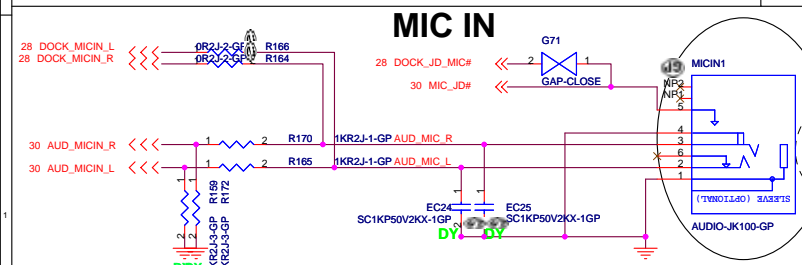
SB

SB

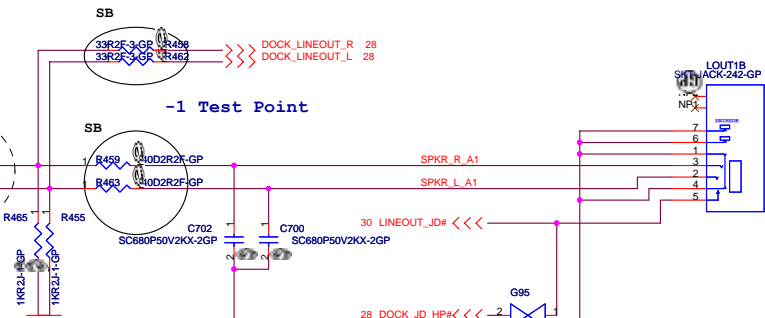
Internal Speaker



1st source: 20.D0197.104

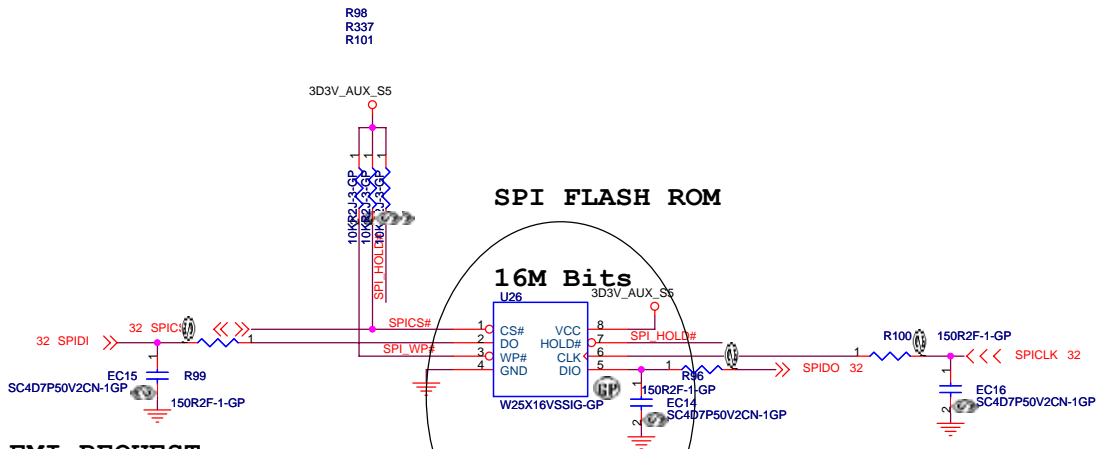


SB



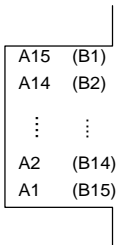
LINE OUT

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsin 221, Taiwan, R.O.C.			
Title AUDIO AMP AND JACK			
Size	Document Number	Rev	
Date: Thursday, August 02, 2007	Sheet 31	of	47

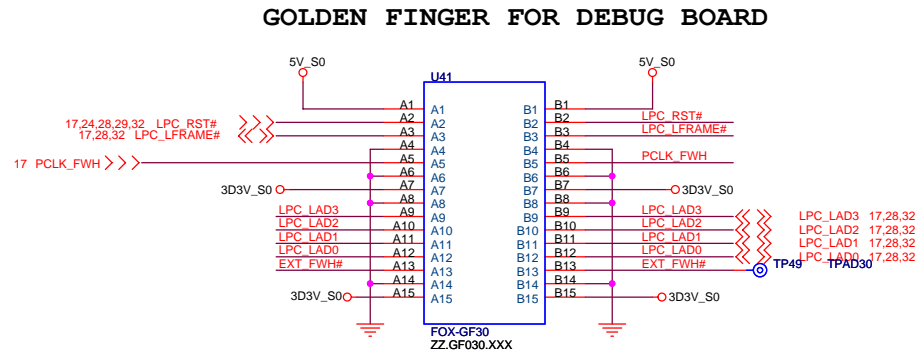


EMI REQUEST

TOP VIEW

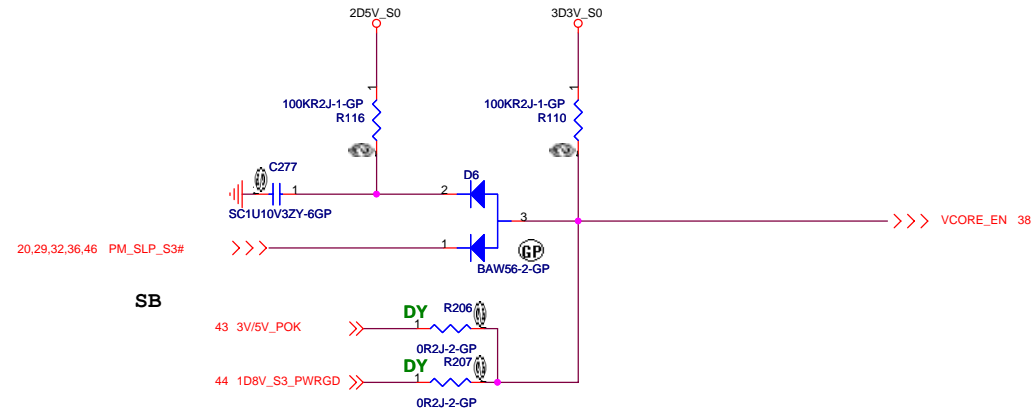


(BOTTOM VIEW)

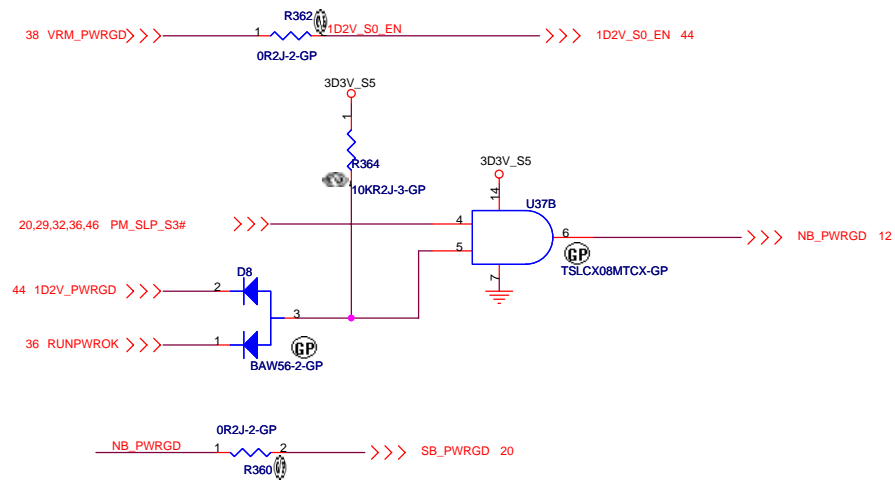


LAYOUT

緯創資通 Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title BIOS			
Size A3	Document Number Ferrari 7		Rev SB
Date: Thursday, August 02, 2007	Sheet 34	of	47



P/H @ 1D8V_S3 PAGE

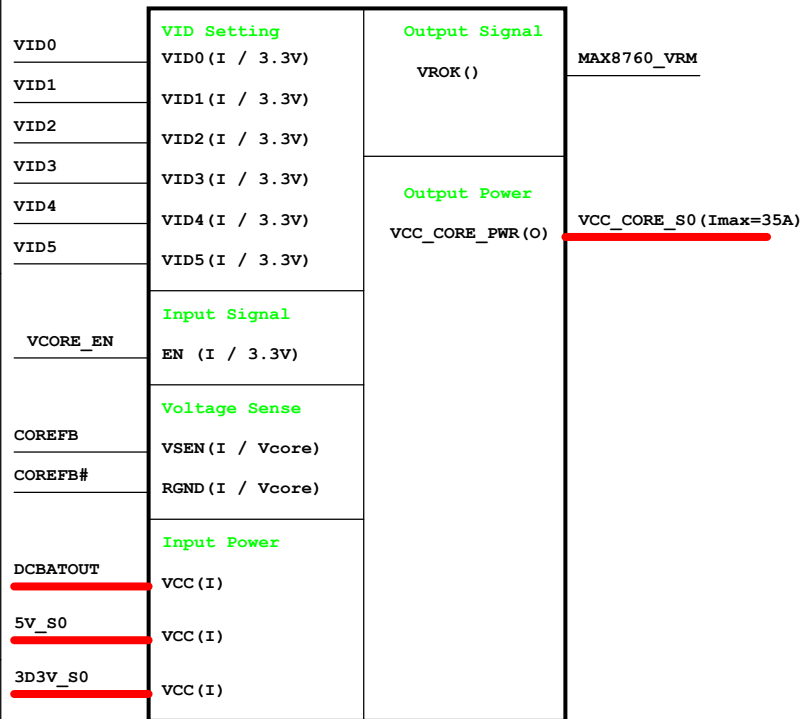


LAYOUT

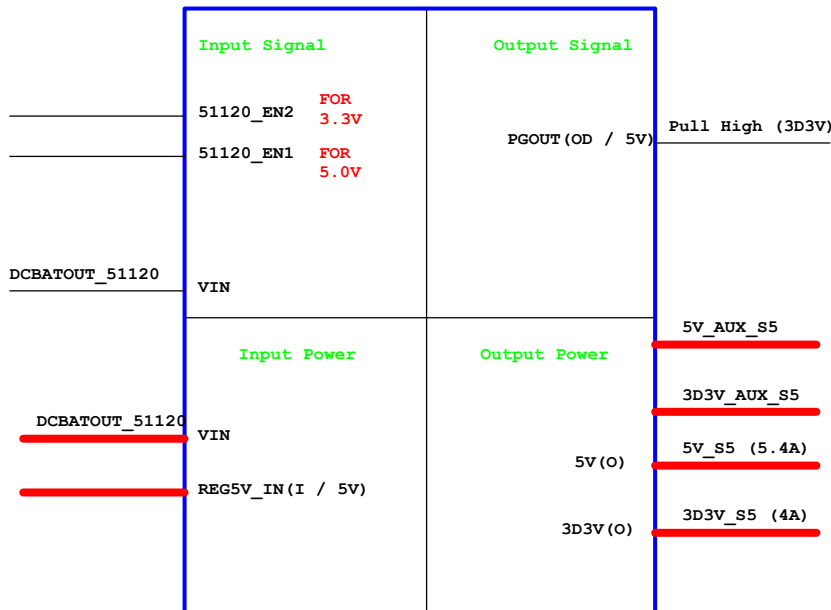
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title POWERGOOD&ENABLES(1/2)			
Size A3	Document Number	Rev SB	
Date: Thursday, August 02, 2007		Sheet 35	of 47

Title			
G792			
Size A3	Document Number		Rev
	Ferrari 7		SB
Date:	Thursday, August 02, 2007	Sheet 36 of 47	

CPU_CORE
ISL6264CRZ



TI TPS51120
3D3V/5V



2D5V_S0



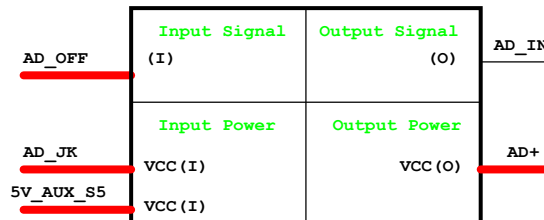
APL5913

1D8V_S5

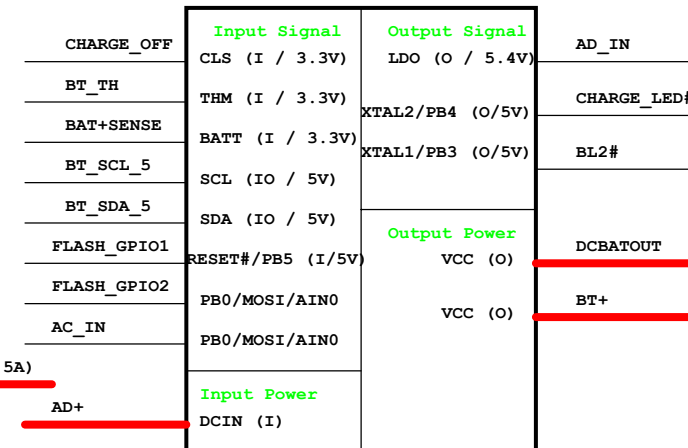


APL5332KAC-TRLGP

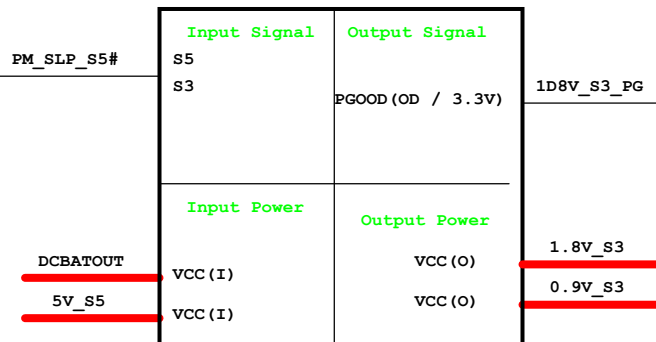
Adapter



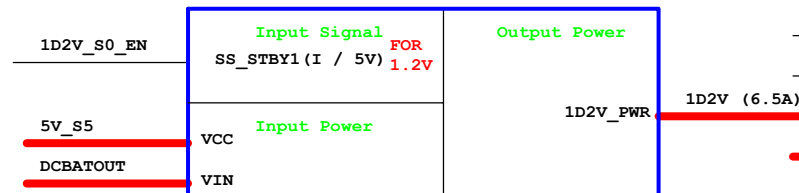
Charger_ISL6255



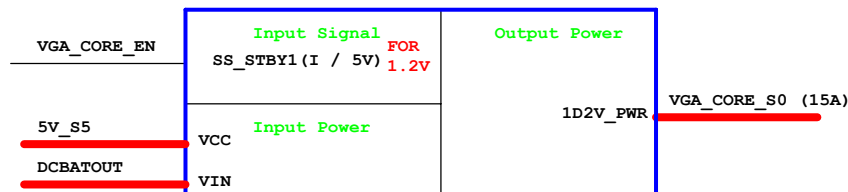
TI TPS51116
1.8V / 0.9V



ISL6268_1D2V



ISL6268_VGA_CORE



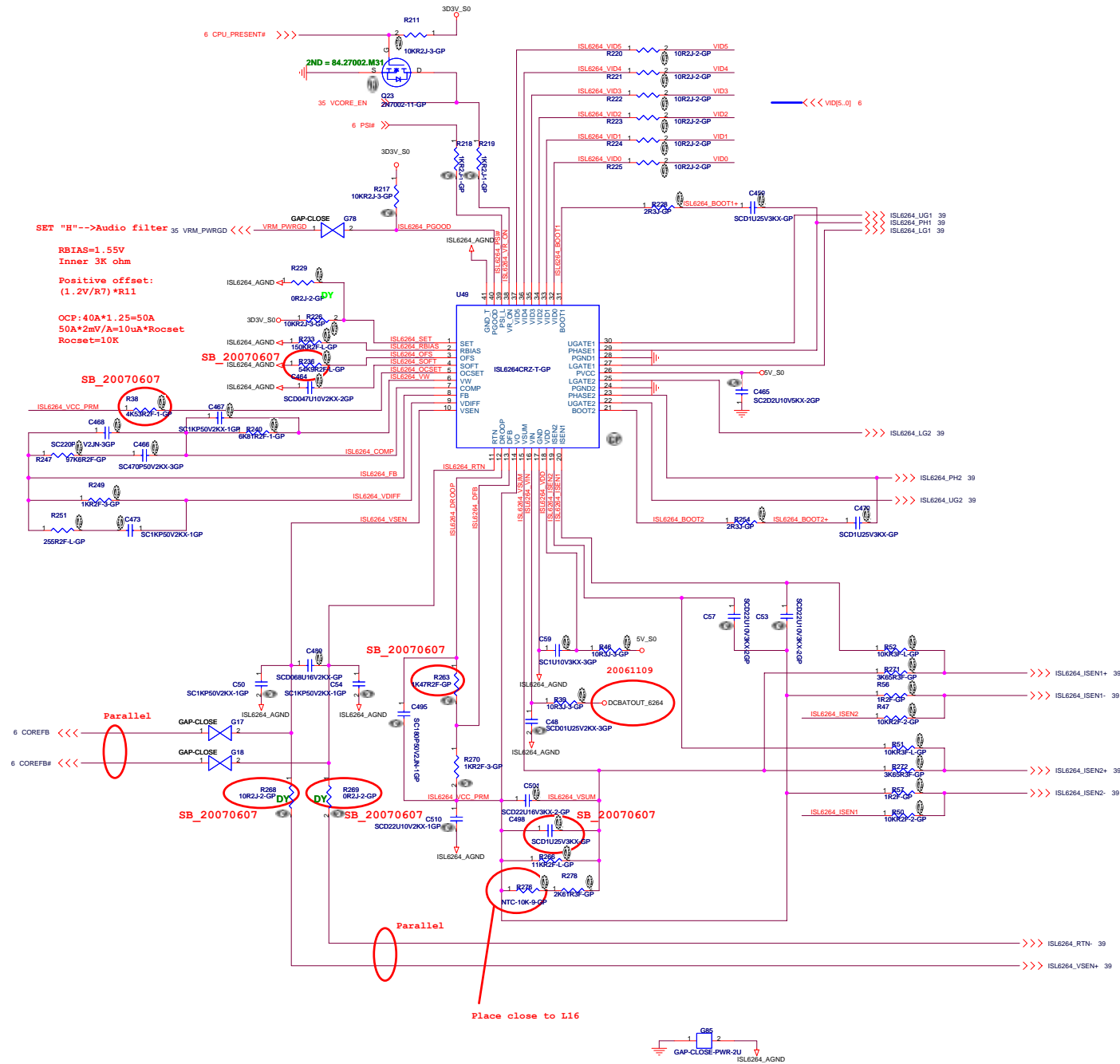
LAYOUT

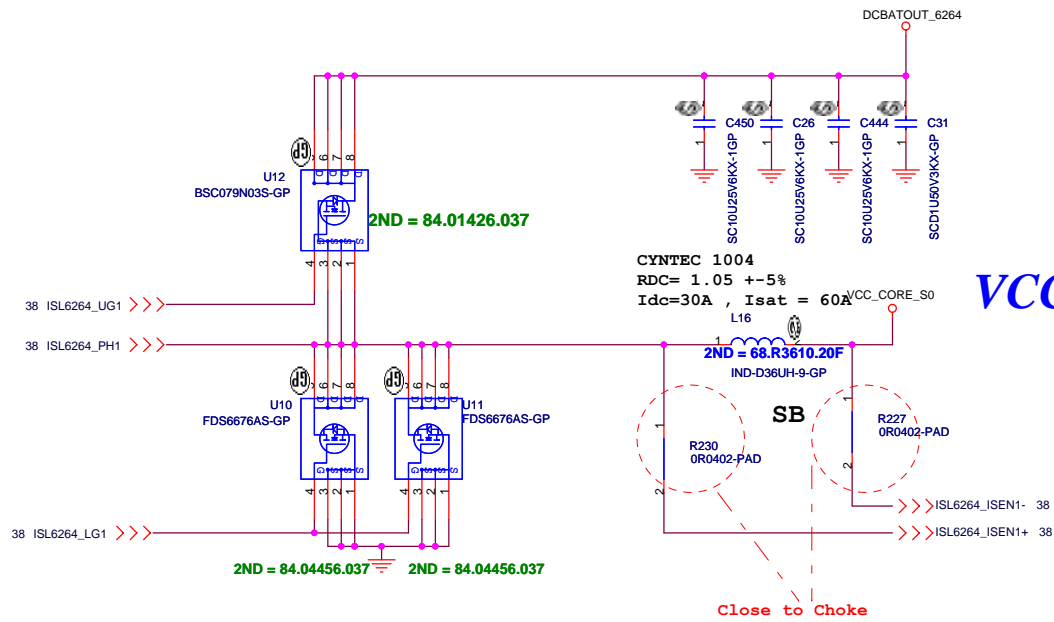
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Power Block Diagram	
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CPU_VCORE
VID=1.075V
Iomax=35A
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

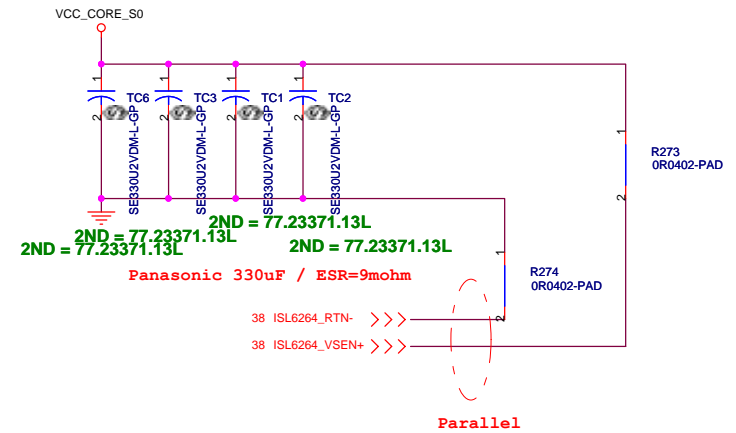
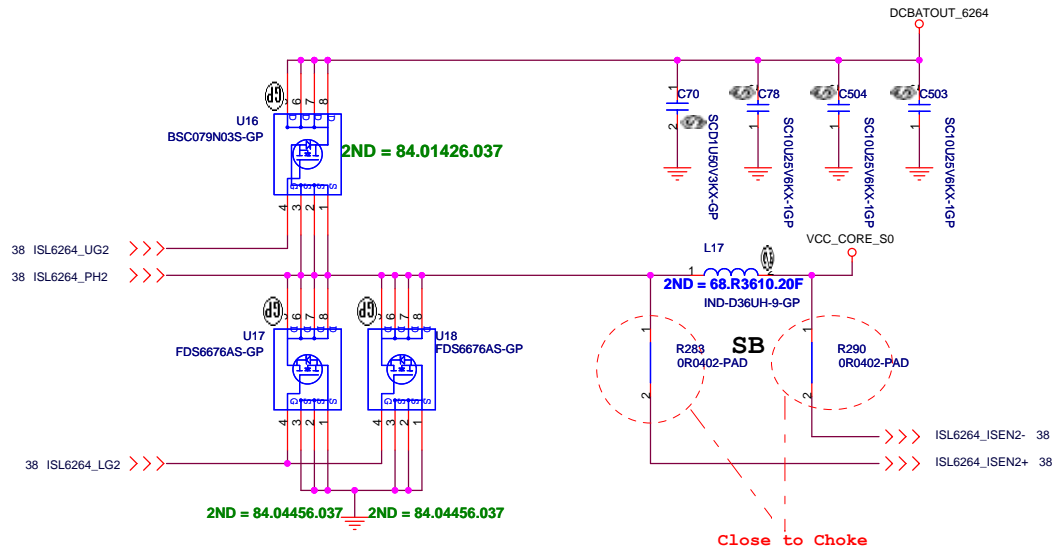
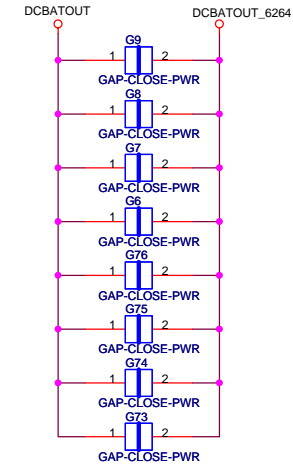
VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.500
0	0	0	0	0	1	1.525
0	0	0	0	0	1	1.500
0	0	0	0	1	1	1.475
0	0	0	0	1	0	1.450
0	0	0	0	1	0	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375





VCC_CORE_S0

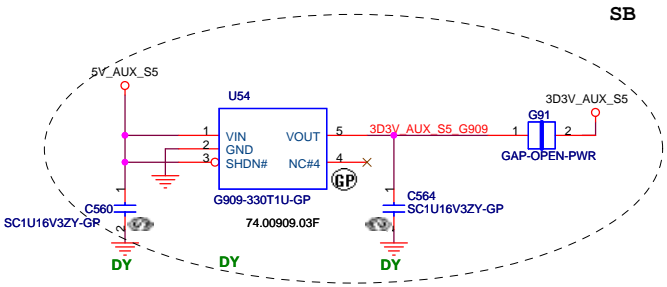
20061109



LAYOUT

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Aux Power 3D3V_AUX_S5



LAYOUT

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Title			
3D3V AUX			
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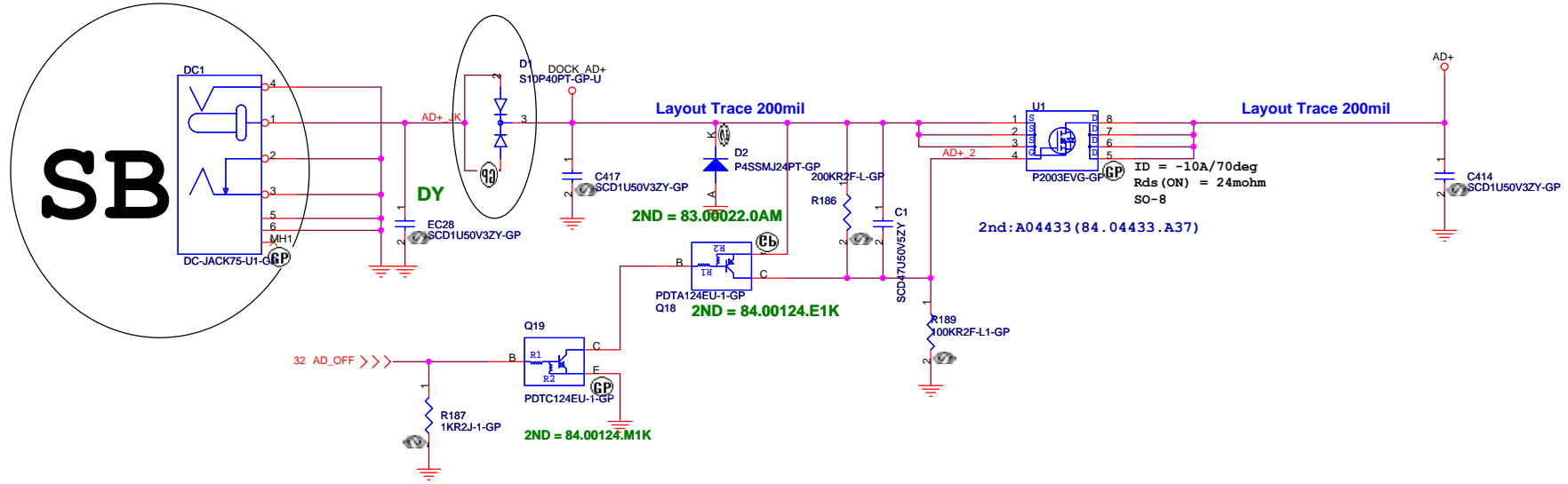


緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

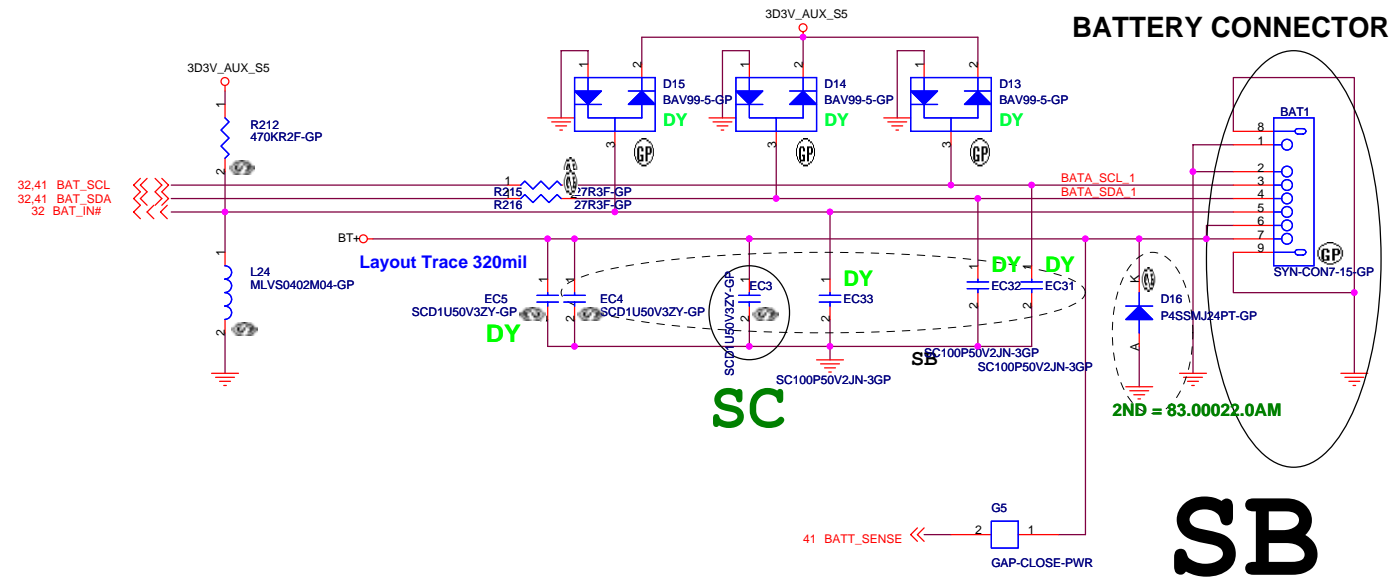
CHARGER MAX8731

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Adaptor in to generate DCBATOUT

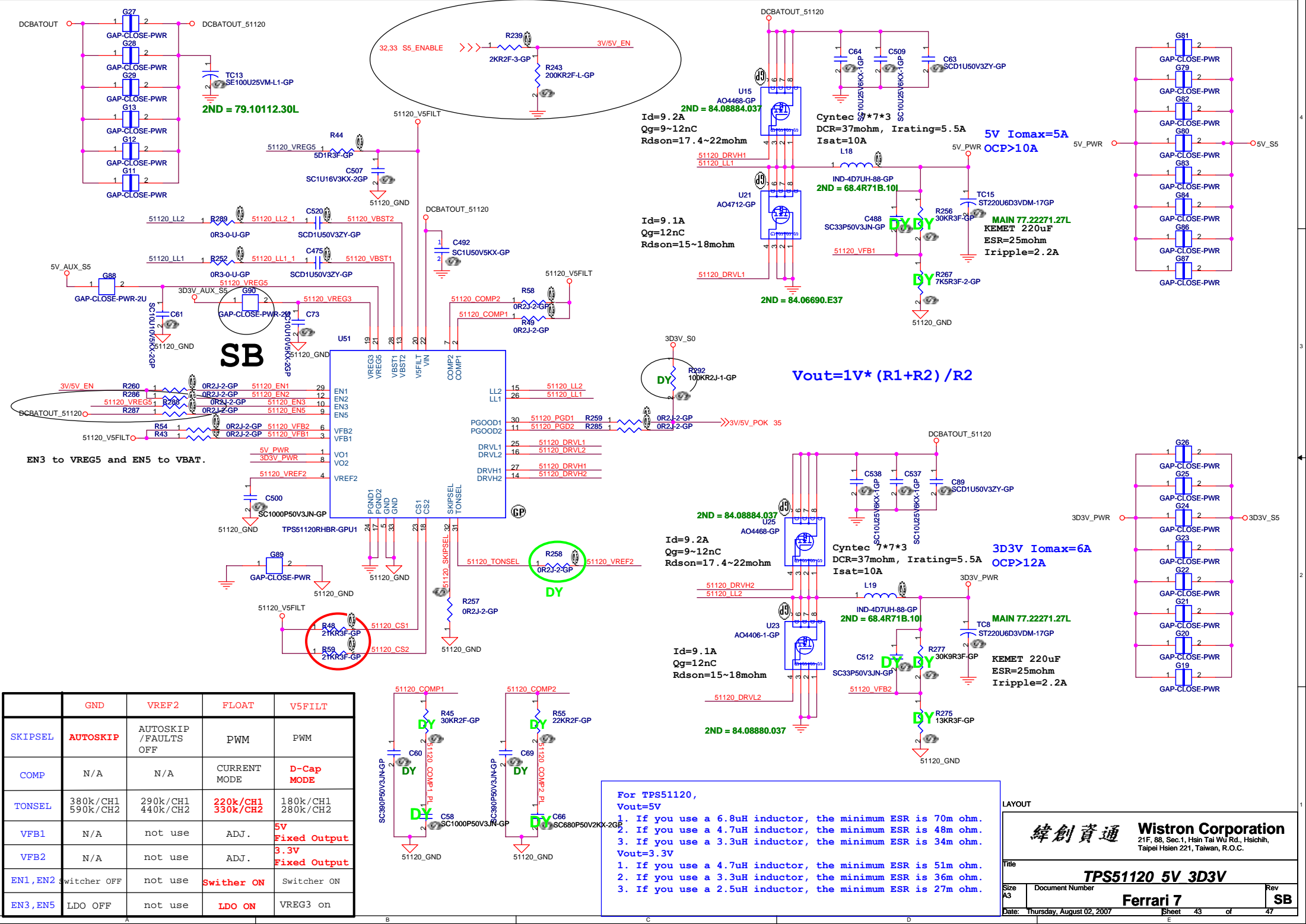


BATTERY CONNECTOR



LAYOUT

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	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	switcher OFF	not use	Switcher ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

For TPS51120,
Vout=5V

1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V

1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

LAYOUT

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Title

TPS51120 5V 3D3V

Size A3

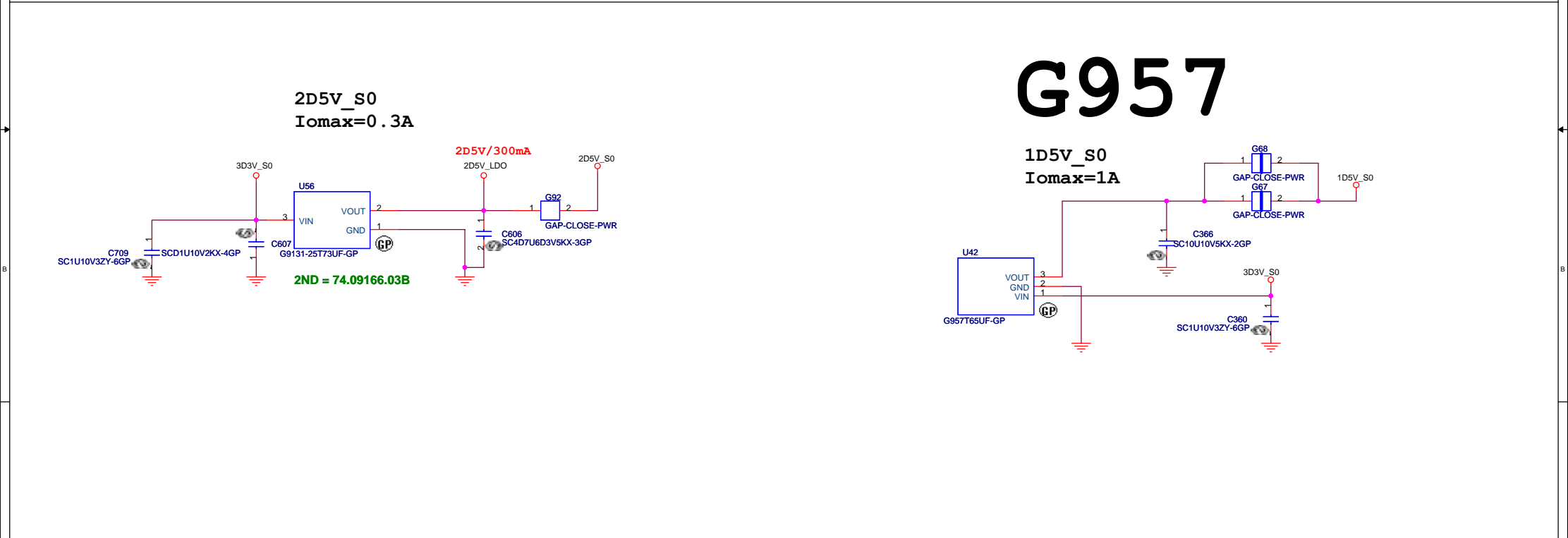
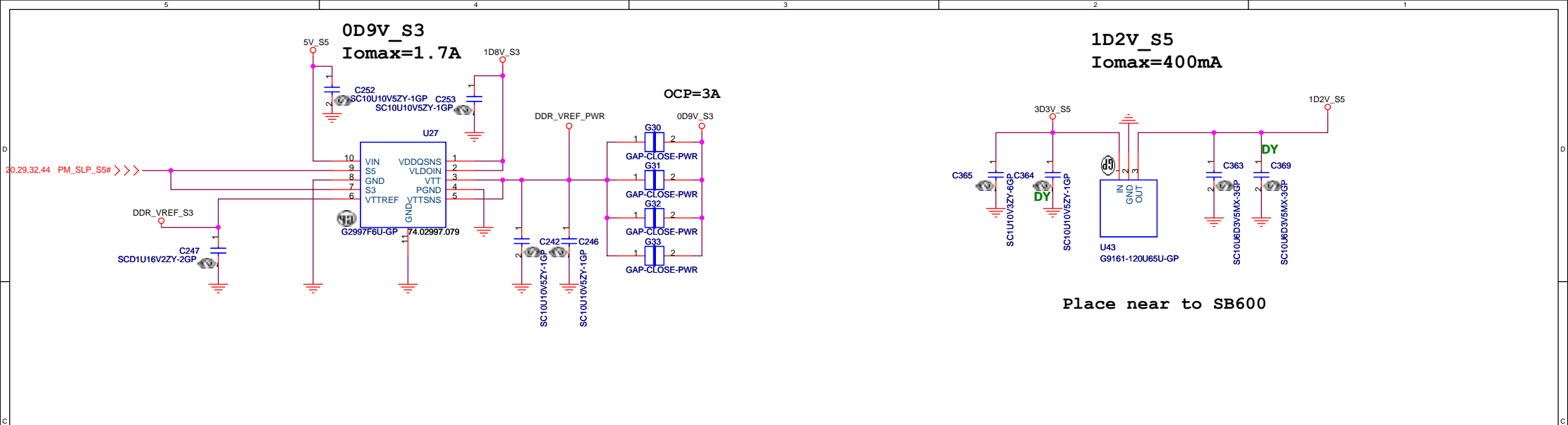
Document Number

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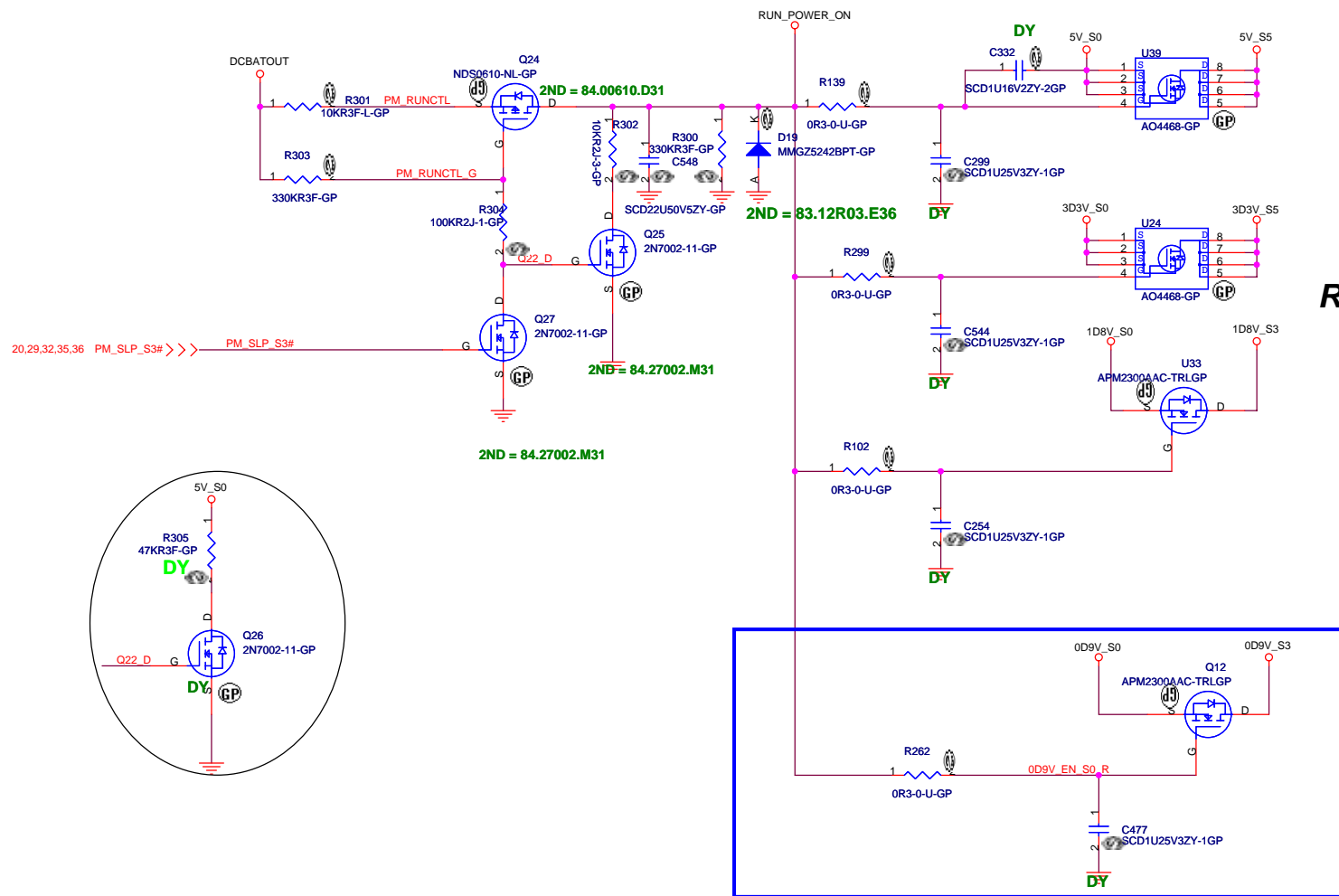
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