MODEL NAME : Maple
PCB NO : DA8000WL000 LA-B012PR01

Dell / Compal Confidential

Schematic Document

Intel Shark Bay ULT
Maple 14"/15" Value
UMA / DIS AMD 25W/S3+DDR3x4

2014-01-21 Rev: 1.0

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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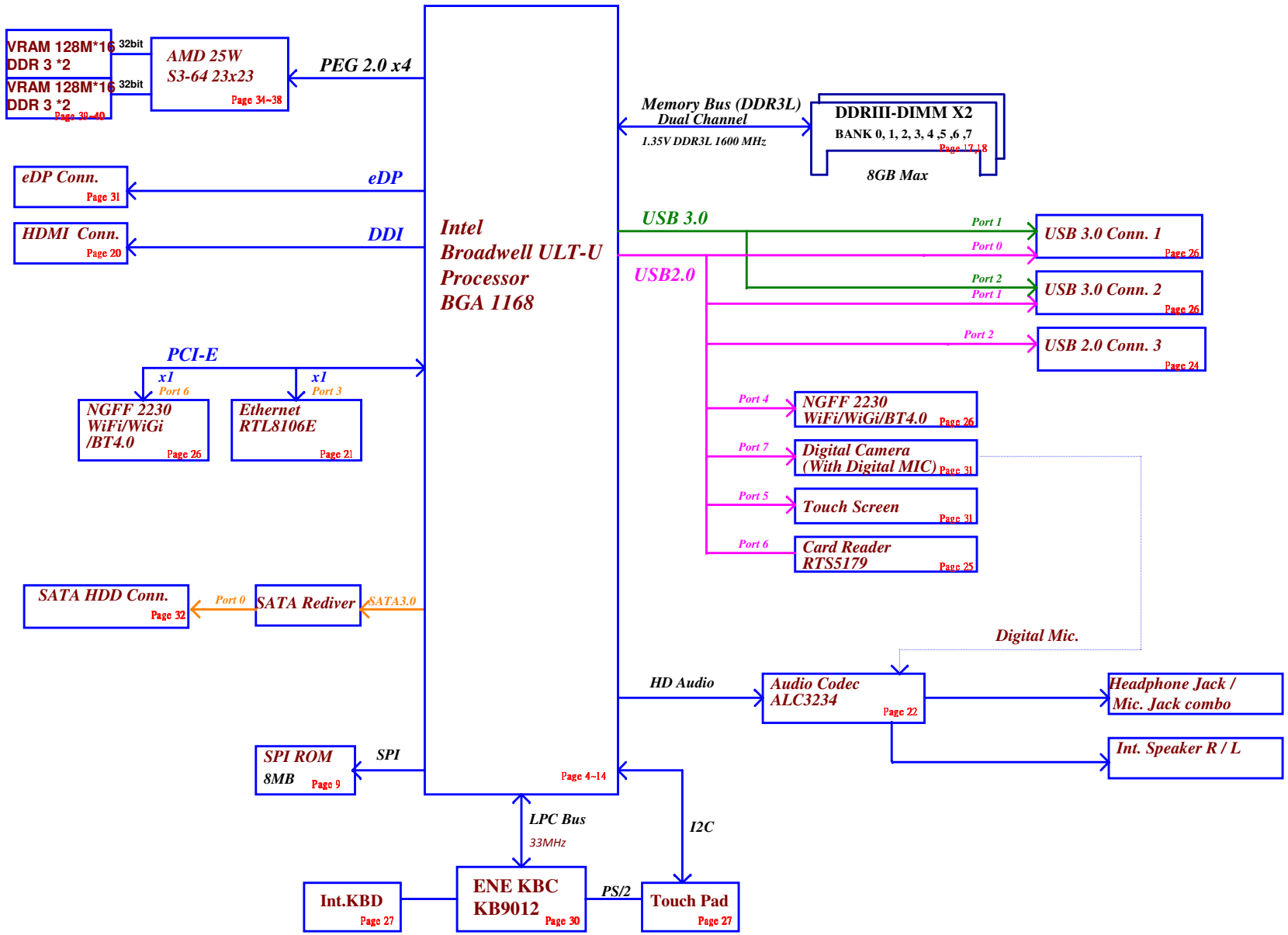
Compal Electronics, Inc.

Title: *MCP(1,2/19) eDP,XDP,MISC*

Size | Document Number: *LA-B012P* | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 1 of 55



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Issued Date	2014/01/20	Deciphered Date	2015/01/19	Title: MCP(1,2/19) eDP,XDP,MISC
				Size / Document Number: LA-B012P / Rev: 1.0
				Date: Tuesday, August 05, 2014 / Sheet 2 of 55

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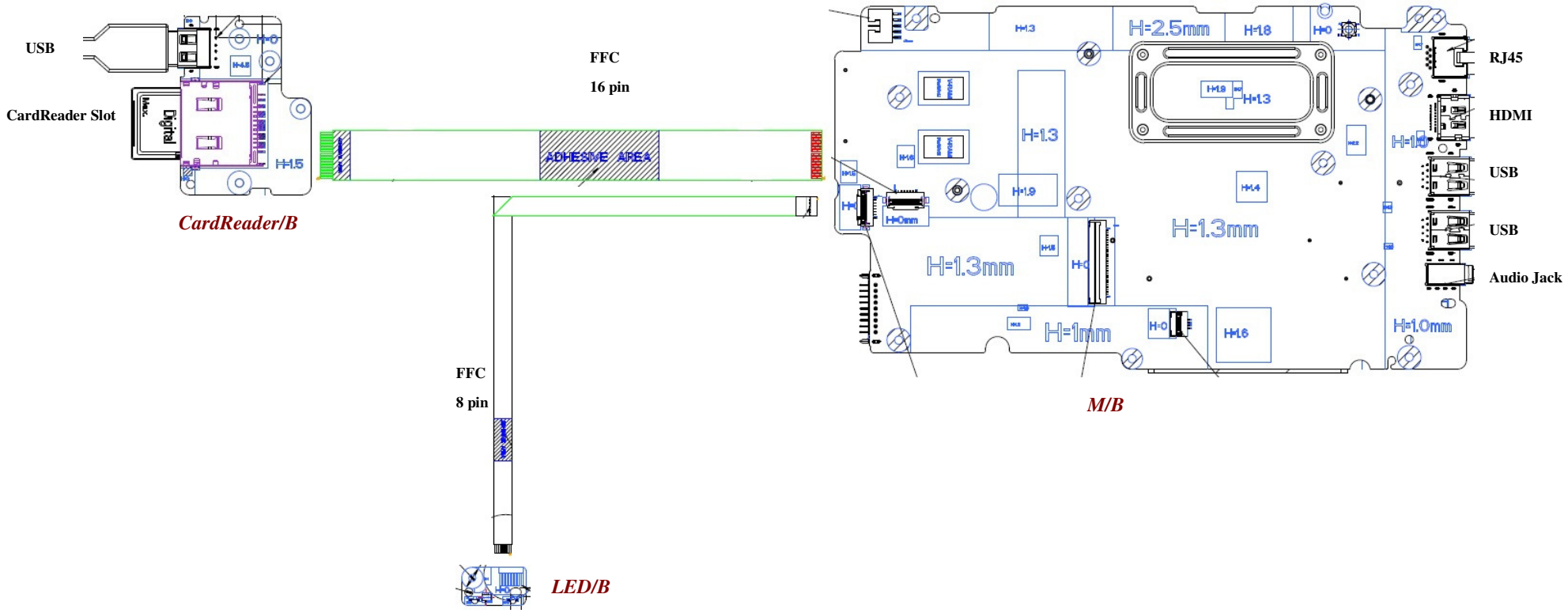

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Issued Date	2014/01/20	Deciphered Date 2015/01/19	Title MCP(1,2/19) eDP,XDP,MISC
			Size / Document Number LA-B012P / Rev 1.0
			Date: Tuesday, August 05, 2014 / Sheet 3 of 55

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Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

HSW BOARD ID Table

Board ID	UMA	DIS(JET)	DIS(Topaz)
0	SSI		
1		SSI	
2			SSI
3	PT		
4		PT	
5			PT
6	ST		
7		ST	
8			ST
9	1.0		
10		1.0	
11			1.0

BDW BOARD ID Table

Board ID	UMA	DIS(JET)	DIS(Topaz)
0	Pre-SSI		
1		Pre-SSI	
2			Pre-SSI
3	SSI		
4		SSI	
5			SSI
6	PT		
7		PT	
8			PT
9	ST		
10		ST	
11			ST
12	1.0		
13		1.0	
14			1.0

ULT	USB3.0	
	Port1	USB connector 1
	Port2	USB connector 2
	Port3	
	Port4	
	USB2.0	
	Port0	USB connector 1
	Port1	USB connector 2
	Port2	USB connector 3 (D/B)
	Port3	
	Port4	MINI Card (WLAN)
	Port5	Touch Screen Panel
	Port6	Card Reader
	Port7	Camera
	PCI EXPRESS	
	Lane 1	
	Lane 2	
	Lane 3	10/100 LAN
	Lane 4	MINI Card (WLAN)
	Lane 5	PEG (AMD JET/TOBAZ)
	Lane 6	
	SATA	
	SATA0	HDD
	SATA1	
	SATA2	
	SATA3	

SMBUS Control Table

	SOURCE	BATT	Charger	VGA	DIMM	XDP	Thermal Sensor	FFS
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V					
EC_SMB_CK2 EC_SMB_DA2	KB9012			V			V	
SMBCLK SMBDATA	ULT				V	V		V
SML0CLK SML0DATA	ULT							
SML1CLK SML1DATA	ULT							

Link

Symbol Note :

: means Digital Ground

: means Analog Ground

CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

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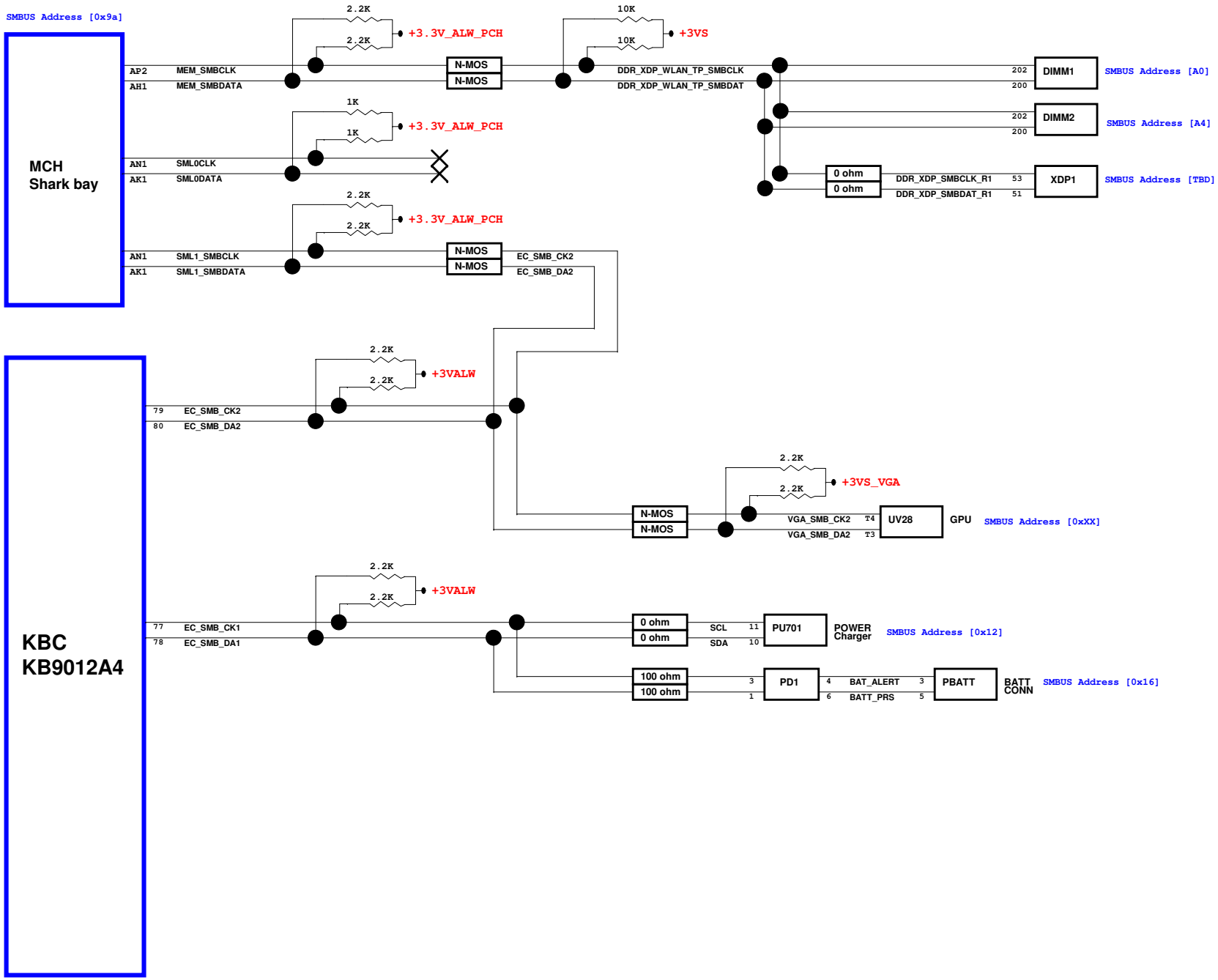

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Compal Electronics, Inc.

Title: MCP(1,2/19) eDP,XDP,MISC

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i3-4020U-15W-GT2-MP

UC1 I3R1@ CL8064701552800 QEZ5 D0 1.8G SA00007MG0L

UC2 I3R3@ CL8064701478202 SR16Q C1 1.7G A31! SA00006SX2L TBD

i5-4210U-15W-GT2-MP

UC4 I5R1@ CL8064701477802 QEAK D0 1.7G SA00007LO0L

UC5 I5R3@ CL8064701477702 SR170 C1 1.6G A31! SA00006SM3L TBD

i7-4510U-15W-GT2-MP

UC7 I7R1@ CL8064701477301 QEAF D0 2G BGA SA00007M70L

UC8 I7R3@ CL8064701477202 SR16Z C1 1.8G A31! SA00006SL2L TBD

Broadwell

UC6 QG21@ CL8065801674128 QG21 C0 1.2G SA00007OS0L

UC9 QFSY@ CL8064701614813 QFSY C0 1.6G SA00007AM0L

UC10 QG22@ CL8065801675027 QG22 C0 1.2G SA00007OT0L

UC3A HASWELL_MCP_E

DDI1_LANE_N0 C54 DDI1_TXN0
DDI1_LANE_P0 C55 DDI1_TXP0
DDI1_LANE_N1 B58 DDI1_TXN1
DDI1_LANE_P1 C58 DDI1_TXP1
DDI1_LANE_N2 B55 DDI1_TXN2
DDI1_LANE_P2 A55 DDI1_TXP2
DDI1_LANE_N3 A57 DDI1_TXN3
DDI1_LANE_P3 B57 DDI1_TXP3
DDI2_TXN0 C51
DDI2_TXP0 C53
DDI2_TXN1 B53
DDI2_TXP1 C49
DDI2_TXN2 B51
DDI2_TXP2 A51
DDI2_TXN3 B49
DDI2_TXP3

EDP_TXN0 C45 EDP_TX0# <31>
EDP_TXP0 B46 EDP_TX0 <31>
EDP_TXN1 A47 EDP_TX1# <31>
EDP_TXP1 B47 EDP_TX1 <31>
EDP_TXN2 C47
EDP_TXP2 C46
EDP_TXN3 B49
EDP_TXP3 B49
EDP_AUXN A45 EDP_AUX# <31>
EDP_AUXP B45 EDP_AUX <31>
EDP_RCOMP D20 EDP_COMP
EDP_DISP_UTIL A43 EDP_DISP_UTIL — RC1 0_0402_5% — EDP_BIA_PWM <10,31>

DDI EDP 1 OF 19 Rev1p2

COMPENSATION PU FOR eDP

+VCCIOA_OUT — RC2 24.9_0402_1%~D

CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.

+3VS — CC1 0.1U_0402_10V7K

UC11 @ 74CBTLV3126BQ_DHVQFN14_2P5X3

<8> PCH_JTAG_TDO	PCH_JTAG_TDO	RC3 0_0402_1%	TDO_XDP
<8> PCH_JTAG_TDI	TDI_XDP	RC4 0_0402_1% / RC5 0_0402_1%	TDI_XDP_R
<8> PCH_JTAG_TMS	TMS_XDP	RC6 0_0402_1%	
<30> RUNPWROK	RUNPWROK		
	TRST# XDP		

1A 1OE 2A 2OE 3A 3OE 4A 4OE VCC GND GND PAD — 1B XDP_TDO, 2B XDP_TDI, 3B XDP_TMS, 4B XDP_TRST#

RUNPWROK — CC5 ESD@ 0.1U_0402_10V7K

Place CC29 close to UC4

+1.05VS_PCH — CC2 XDP@ 0.1U_0402_10V7K — CC3 XDP@ 0.1U_0402_10V7K

Place near JXDP1

JXDP1 SAMTE_BSH-030-01-L-D-A CONN@

<10,30> PBTN_OUT#	H_CPUPWRGD	RC7 1K_0402_5%	H_VCCST_PWRGD_XDP
		RC9 0_0402_5%	CFD_PWRBTN# XDP
<13> CPU_PWR_DEBUG#	SYS_PWROK	RC11 0_0402_5%	CPU_PWR_DEBUG# R
<10,30> SYS_PWROK		RC12 0_0402_5%	SYS_PWROK_XDP
<17,18,32,9> DDR_XDP_WLAN_TP_SMBDAT		RP1 0_8P4R_5%	DDR_XDP_SMBDAT_R1
<17,18,32,9> DDR_XDP_WLAN_TP_SMBCLK			DDR_XDP_SMBCLK_R1
	PCH_JTAG_TCK		XDP_TCLK

CLK_XDP RC8 0_0402_5% — CLK_CPU_ITP <9>
CLK_XDP# RC10 0_0402_5% — CLK_CPU_ITP# <9>
XDP_RST# R — RC13 1K_0402_5% XDP@ — PLT_RST# <10,21,26,30,34>
XDP_DBRESET# — RC14 1K_0402_1% — +3VS
TDO_XDP — TRST# XDP — TDI_XDP — TMS_XDP — CFG3 R — RC15 1K_0402_5% XDP@ — CC6 0.1U_0402_10V7K

PLT_RST# — CC4 ESD@ 0.047U_0402_16V4Z

Place CC30 close to RC51.1

reference Shark Bay ULT Validation Customer Debug Port Implementation Requirement Rev 1.0

+1.05VS_PCH — RC16 @ 49.9_0402_1% H_CATERR# — RC18 62_0402_5% H_PROCHOT#

	PCH_JTAG_RST#	0_0402_1%	XDP_TRST# RC17
<8> PCH_JTAG_JTAGX		0_0402_1%	XDP_TCLK RC21
		0_0402_5% XDP@	TDO_XDP RC22
	PCH_JTAG_TDO	0_0402_5% XDP@	TDI_XDP_R RC23
<8> PCH_JTAG_TCK	PCH_JTAG_TCK	0_0402_5% XDP@	XDP_TCLK RC24

+3VALW_PCH — RC19 @ 1K_0402_5% — SYS_PWROK_XDP — CC7 ESD@ 0.1U_0402_10V7K

Place near JXDP1.47

XDP_DBRESET# — RC20 @ 0_0402_1% — SYS_RESET# — SYS_RESET# <10>

RC25 10K_0402_5% — CC8 100P_0402_50V8J @EMI@ — H_CPUPWRGD

ESD solution

CAD Note: Avoid stub in the PWRGD path while placing resistors RC115

UC3B HASWELL_MCP_E

<30> PECI_EC	H_CATERR#	D61 PROC_DETECT	MISC
	PECI_EC	K61 CATERR	
		N62 PECI	
<30,44> H_PROCHOT#	H_PROCHOT# R	RC26 56_0402_5%	K63 PROCHOT — THERMAL
	H_CPUPWRGD		C61 PROCPWRGD — PWR
	SM_RCOMP0		AU60 SM_RCOMP0 — DDR3
	SM_RCOMP1		AV60 SM_RCOMP1
	SM_RCOMP2		AU61 SM_RCOMP2
<17> DDR3_DRAMRST# CPU			AV15 SM_DRAMRST
<17> DDR_PG_CTRL			AV61 SM_PG_CNTL1

H_PROCHOT# — CC9 @EMI@ 22P_0402_50V8J

PRDY J62 XDP_PRDY#
PREQ K62 XDP_PREQ#
PROC_TCK E60 XDP_TCK
PROC_TMS E61 XDP_TMS
PROC_TRST# E59 XDP_TRST#
PROC_TDI F63 XDP_TDI
PROC_TDO F62 XDP_TDO — R1 @ 0_0402_5% — PCH_JTAG_RST# <8>

J60 XDP_OBS0_R — RC27 0_0402_1% — XDP_OBS1_R
BPM#0 H60 — T1
BPM#1 H61 — T2
BPM#2 H62 — T3
BPM#3 K59 — T4
BPM#4 H63 — T5
BPM#5 K60 — T6
BPM#6 J61
BPM#7

2 OF 19 Rev1p2

DDR3 COMPENSATION SIGNALS

200_0402_1%	RC28	SM_RCOMP0	
120_0402_1%	RC29	SM_RCOMP1	
100_0402_1%	RC30	SM_RCOMP2	

CAD Note: Trace width=12~15 mil, Spcing=20 mils Max trace length= 500 mil

DDR3_DRAMRST# CPU — CC10 @ESD@ 0.047U_0402_16V4Z

Place CC35 on BOT

PU/PD for JTAG signals

+1.05VS_PCH

XDP_TMS	XDP_TDI	XDP_PREQ#	TDO_XDP	RP2 @ 51_8P4R_5%
XDP_TDO	XDP_TCK	XDP_TRST#	RP3 51_8P4R_5%

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Compal Electronics, Inc.

Title: MCP(1,2/19) eDP,XDP,MISC

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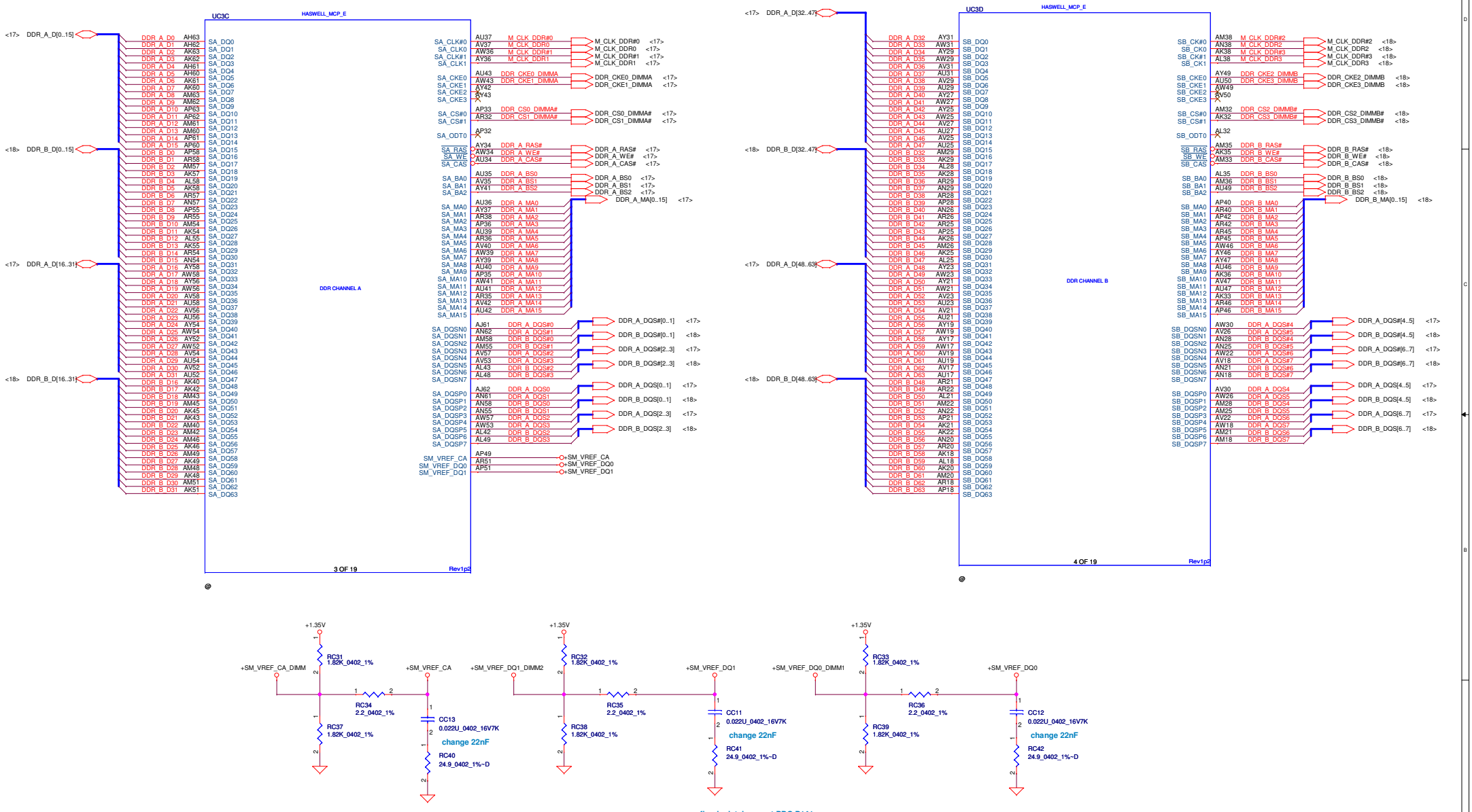
Interleaved Memory



confirm by intel request PDG P141

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Issued Date	2014/01/20	Deciphered Date	2015/01/19

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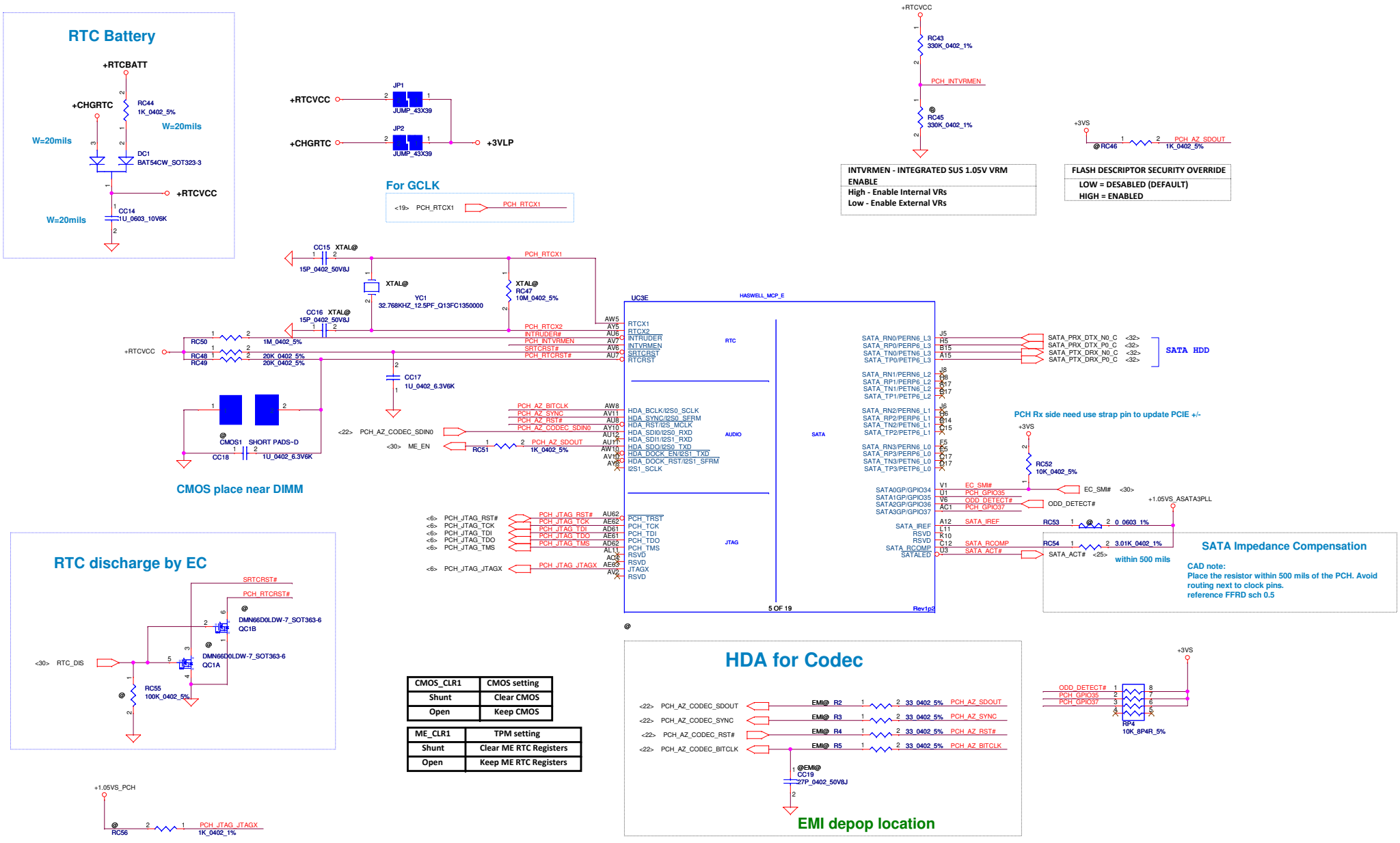
Compal Electronics, Inc.

Title: **MCP(3,4/19) DDR3**

Size | Document Number: **LA-B012P** | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 7 of 55



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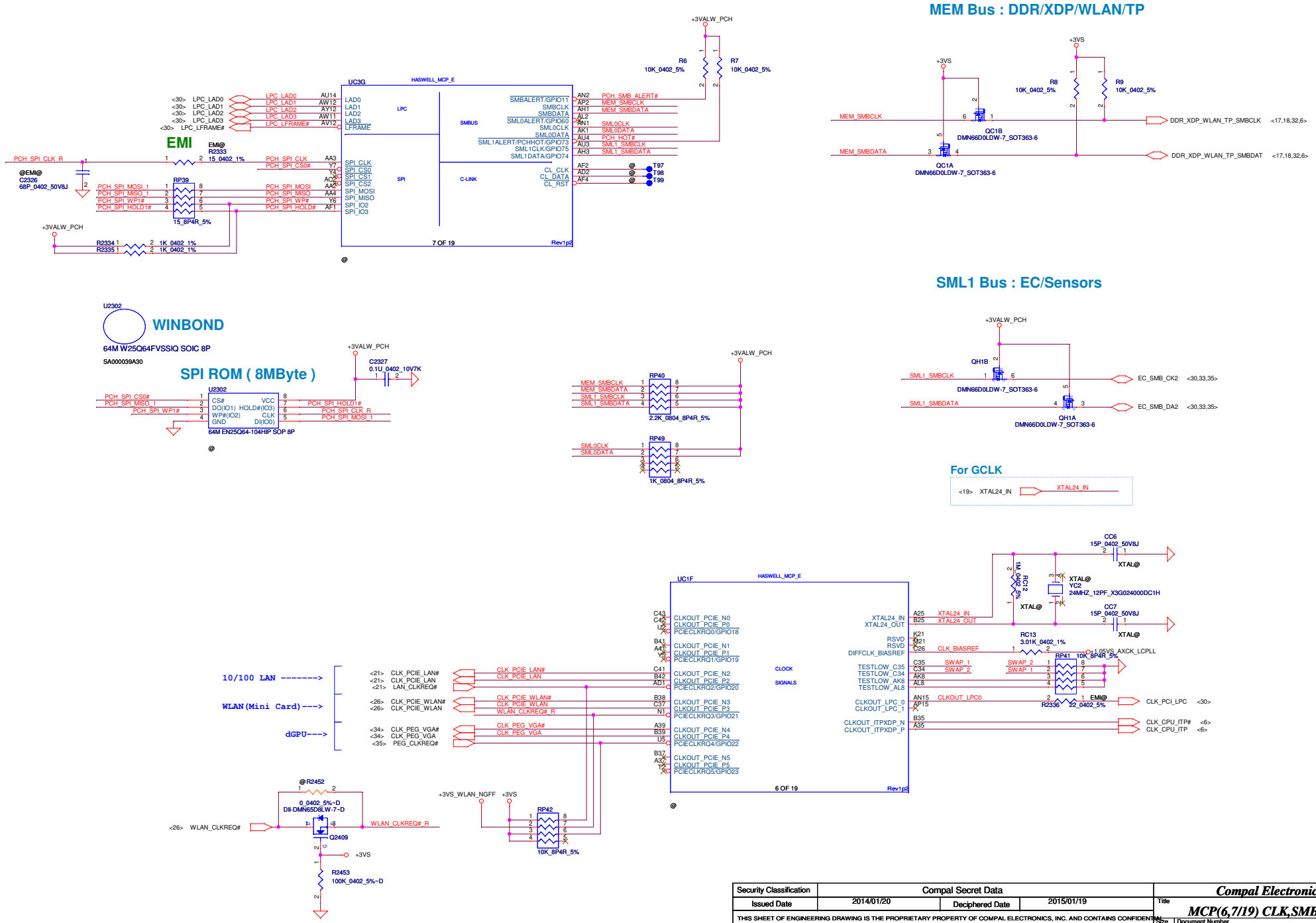
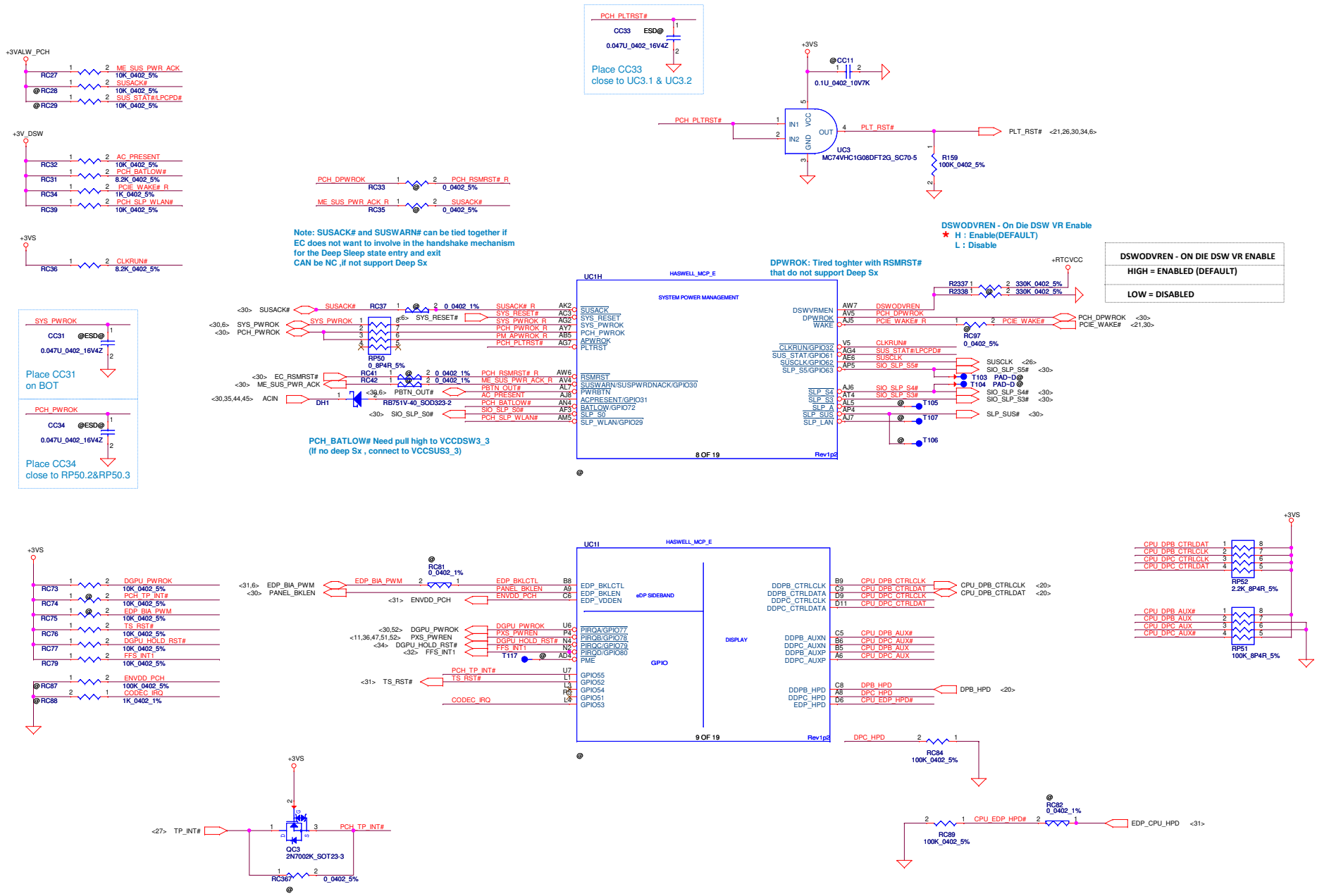
Compal Electronics, Inc.

Title: MCP(5/19) RTC,SATA,HDA,JTAG

Size | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 8 of 55


MEM Bus : DDR/XDP/WLAN/TP
SML1 Bus : EC/Sensors
EMI
WINBOND
64M W25Q64FVSSIQ SOIC 8P
SA000039A30
SPI ROM (8MByte)
64M EN25Q64-104HIP SOP 8P
UC3G
HASWELL_MCP_E
7 OF 19
Rev1p2
UC1F
6 OF 19
CLOCK
SIGNALS
For GCLK
10/100 LAN ------->
WLAN(Mini Card)--->
dGPU--->
Compal Secret Data
Issued Date
2014/01/20
Deciphered Date
2015/01/19
Compal Electronics, Inc.
MCP(6,7/19) CLK,SMB,SPI,LPC
LA-B012P
Rev 1.0
Date: Tuesday, August 05, 2014
Sheet 9 of 55



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Compal Electronics, Inc.

Title: **MCP(8,9/19) DDI,EDP,GPIO**

Size | Document Number: **LA-B012P** | Rev: 1.0

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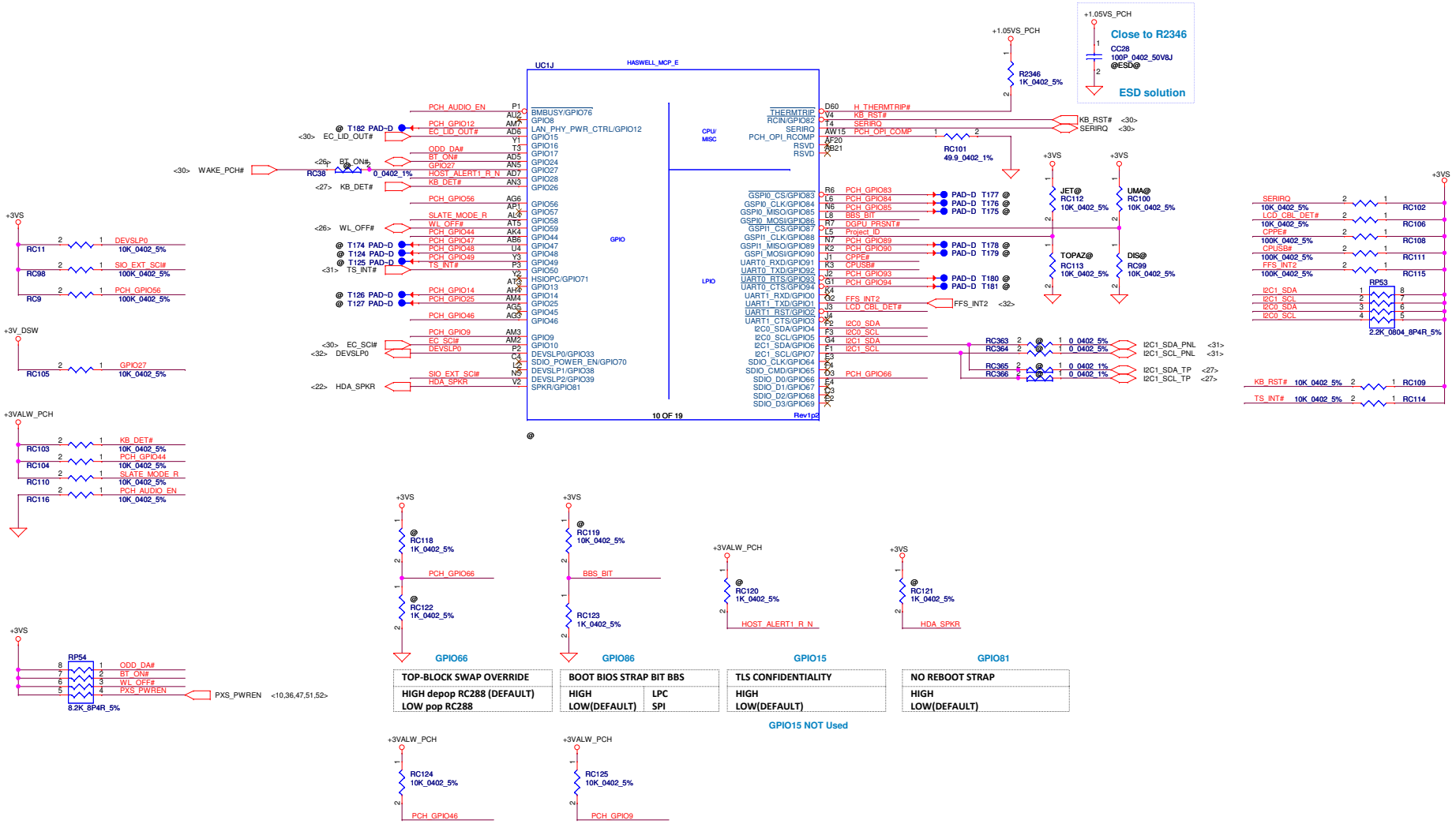

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Compal Electronics, Inc.

Title: **MCP(10/19) GPIO,LPIO,MISC**

Size | Document Number: **LA-B012P** | Rev: 1.0

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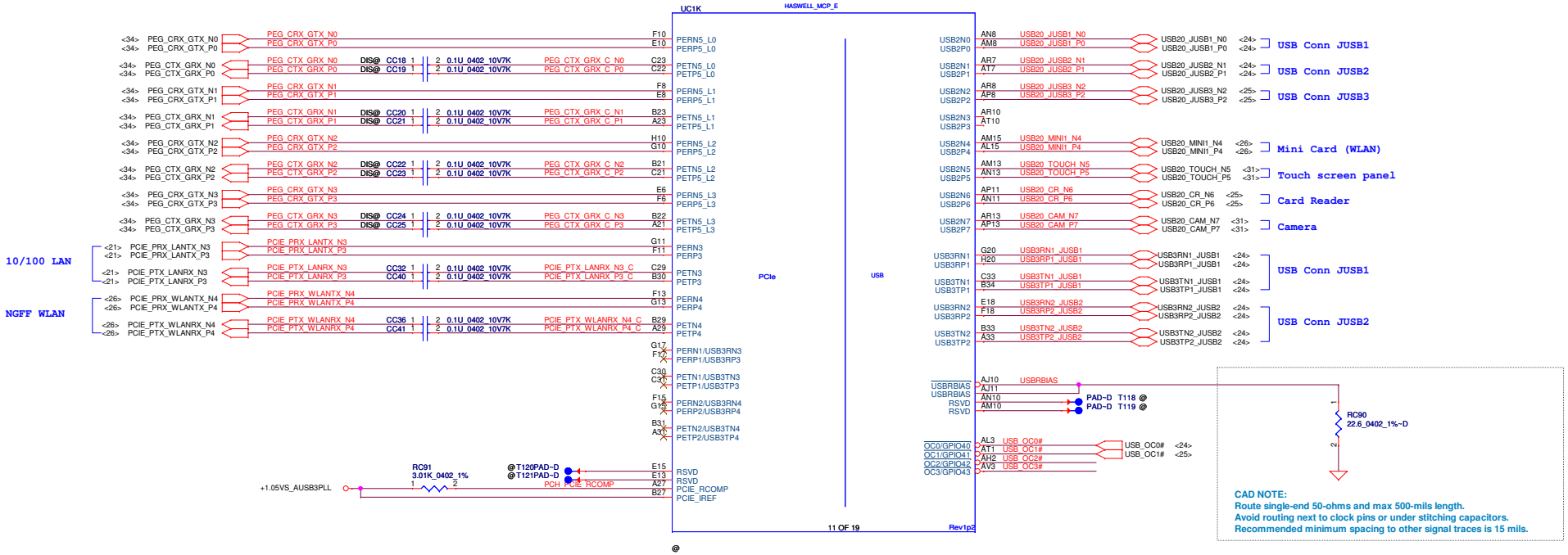

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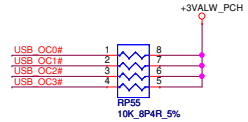

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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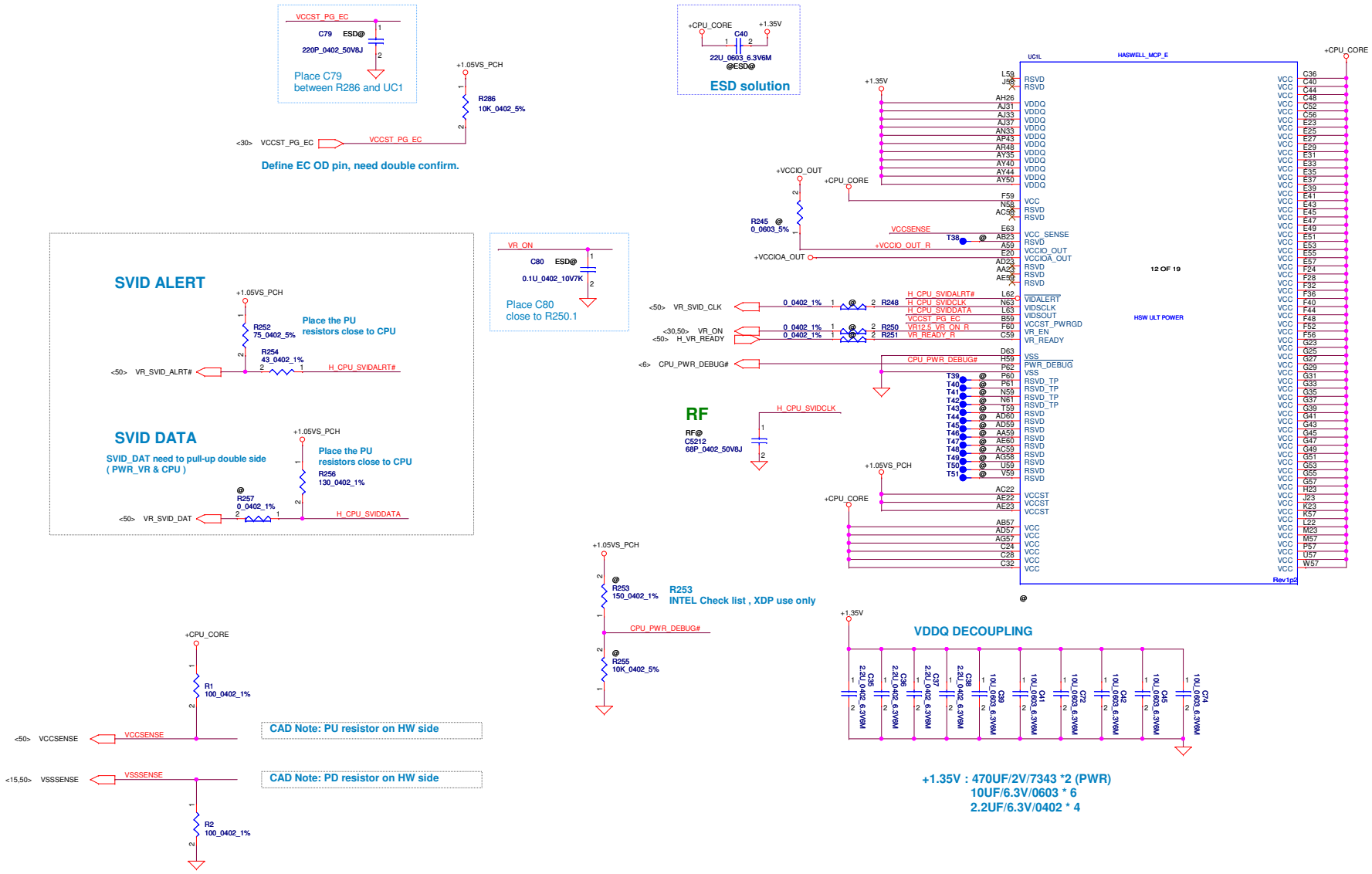
Compal Electronics, Inc.

Title: **MCP(11/19) PCIE,USB**

Size | Document Number: **LA-B012P** | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 12 of 55



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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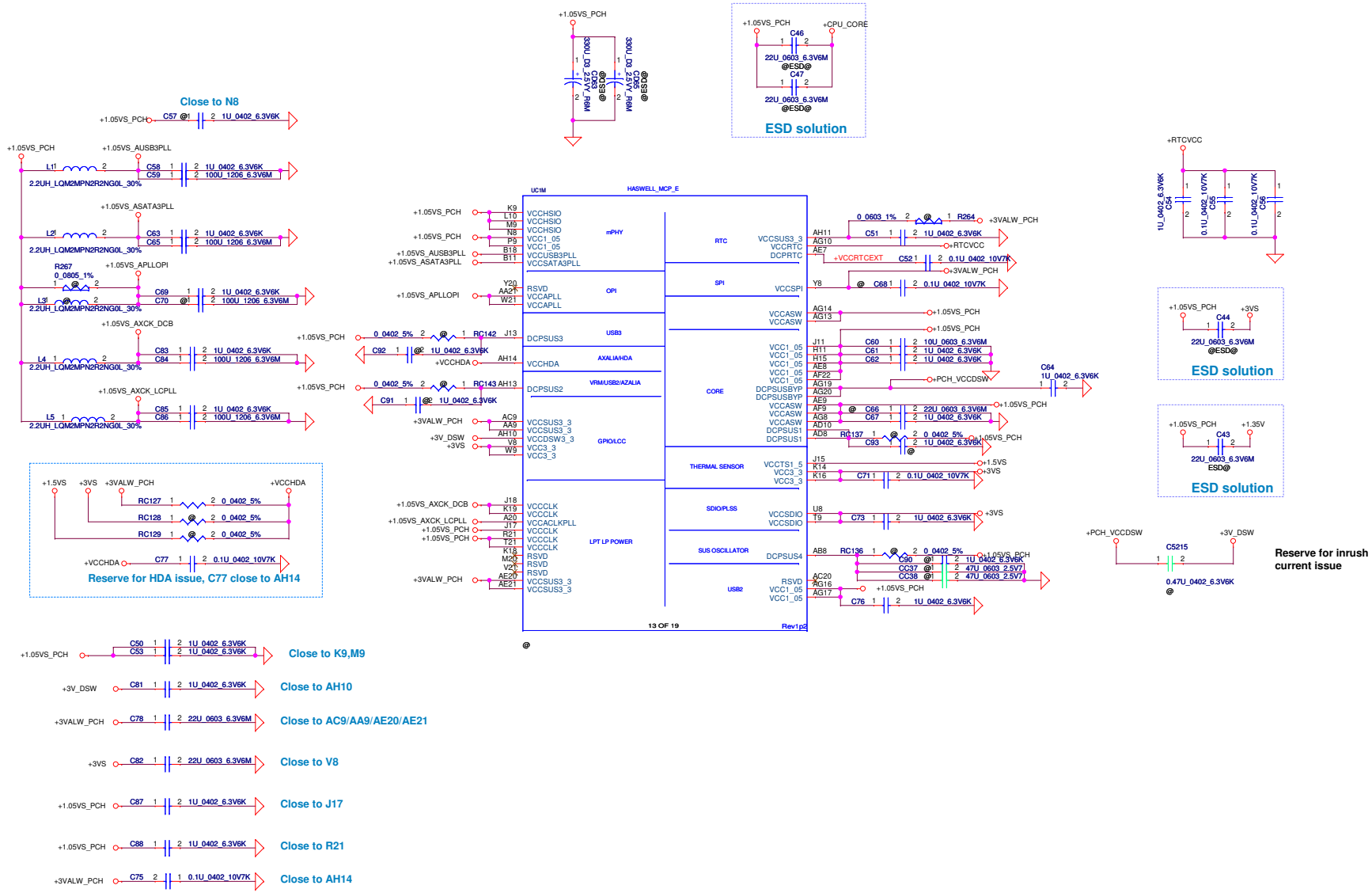
Compal Electronics, Inc.

Title: **MCP(12/19) Power**

Size | Document Number: **LA-B012P** | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 13 of 55



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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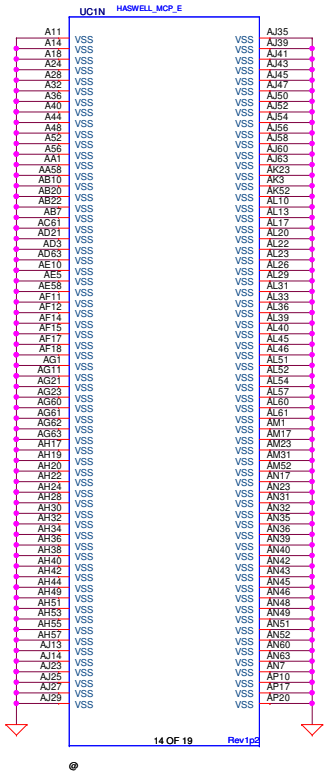
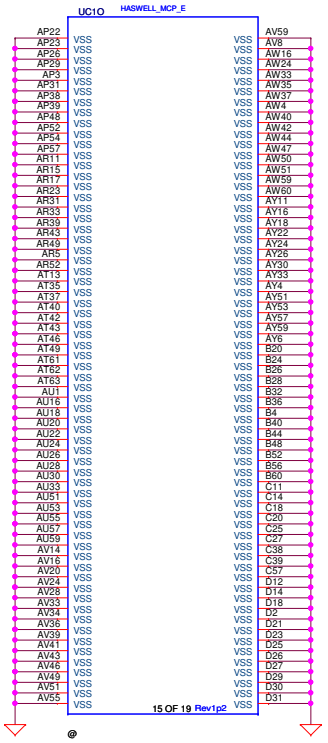
Compal Electronics, Inc.

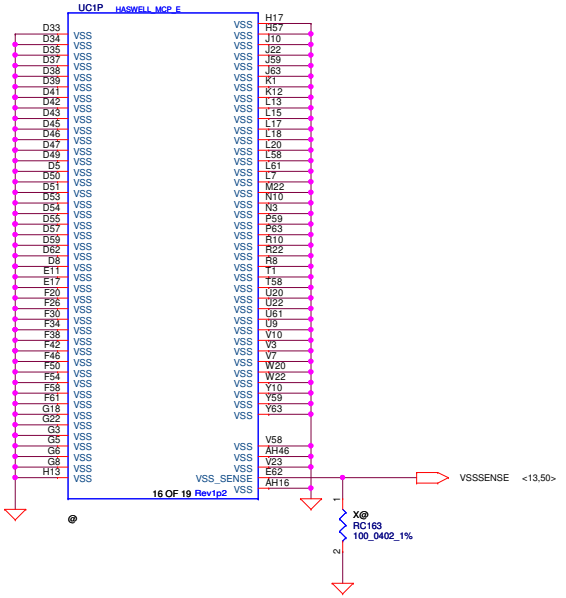
Title: **MCP(13/19) Power**

Size | Document Number: **LA-B012P** | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 14 of 55







CAD Note: RC163 SHOULD BE PLACED CLOSE TO CPU

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Issued Date	2014/01/20	Deciphered Date	2015/01/19

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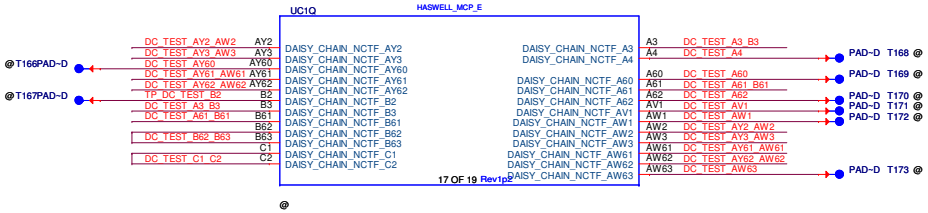
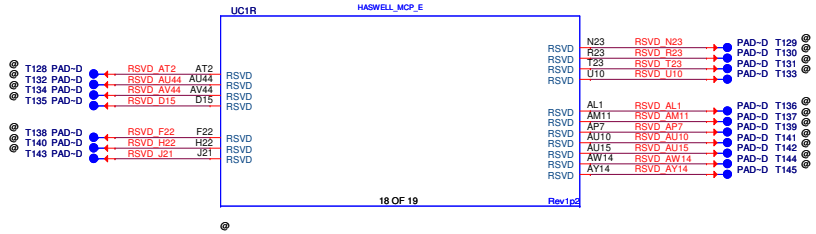
Compal Electronics, Inc.

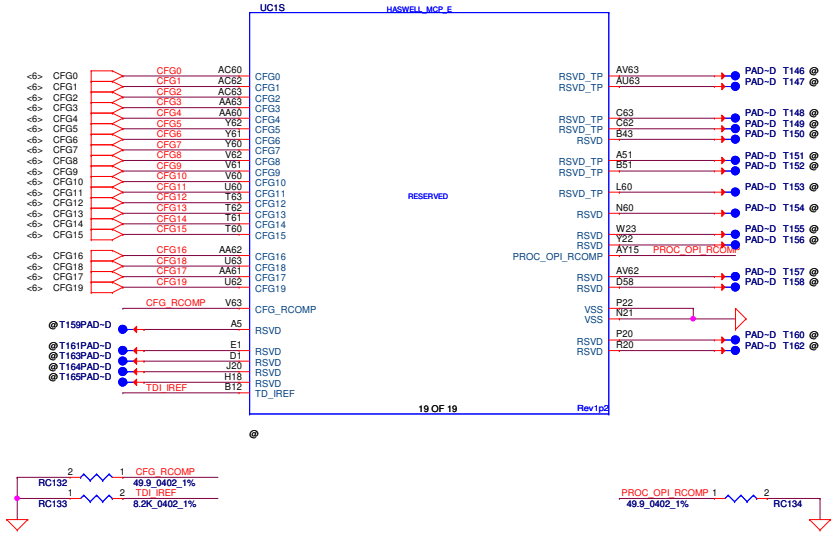
Title: **MCP(14,15,16/19) VSS**

Size | Document Number: **LA-B012P** | Rev: 1.0

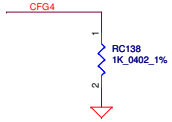
Date: Tuesday, August 05, 2014 | Sheet 15 of 55







CFG STRAPS for CPU



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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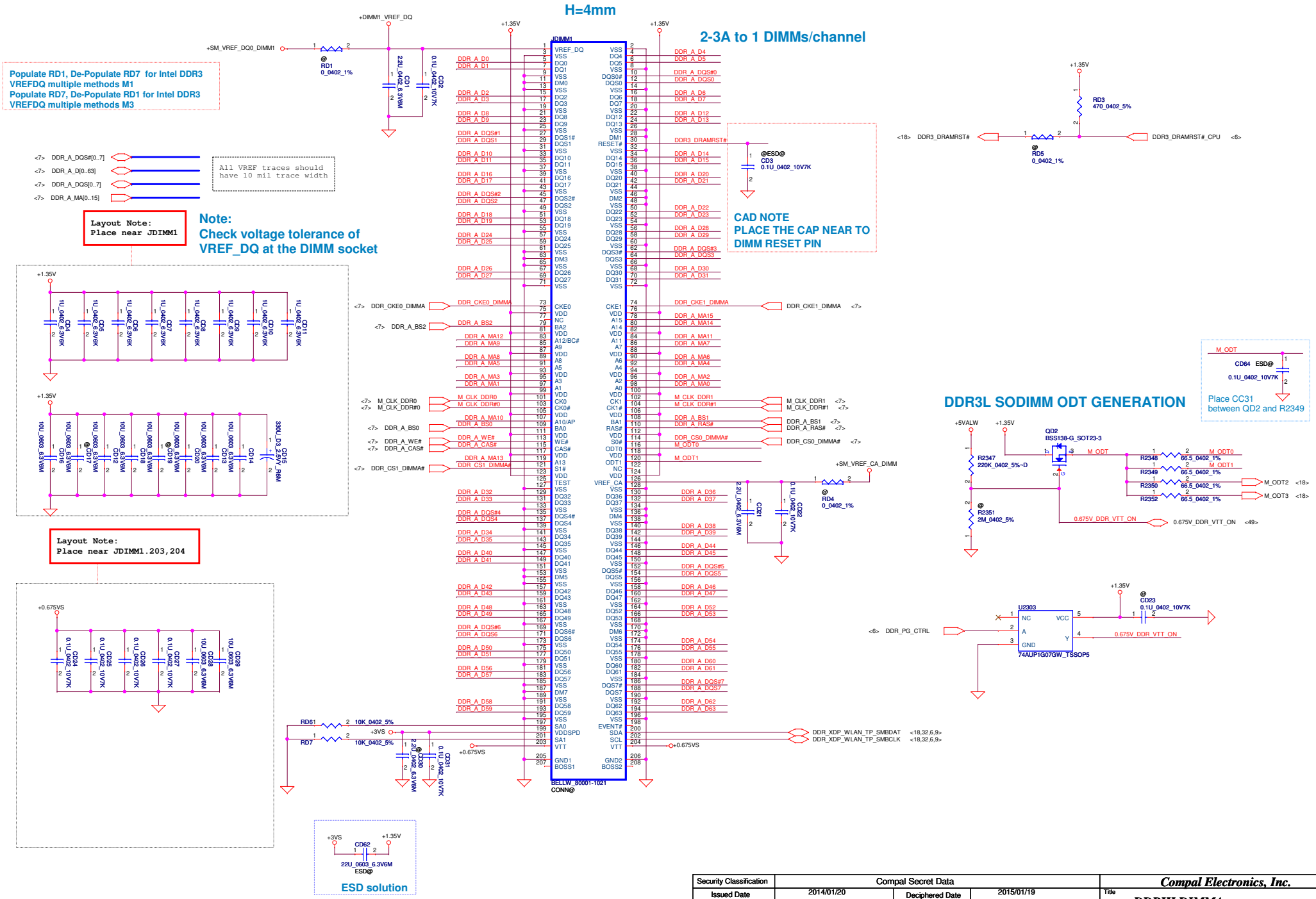
Compal Electronics, Inc.

Title: MCP(17,18,19/19) CFG,RSVD

Size | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 16 of 55



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Issued Date	2014/01/20	Deciphered Date	2015/01/19

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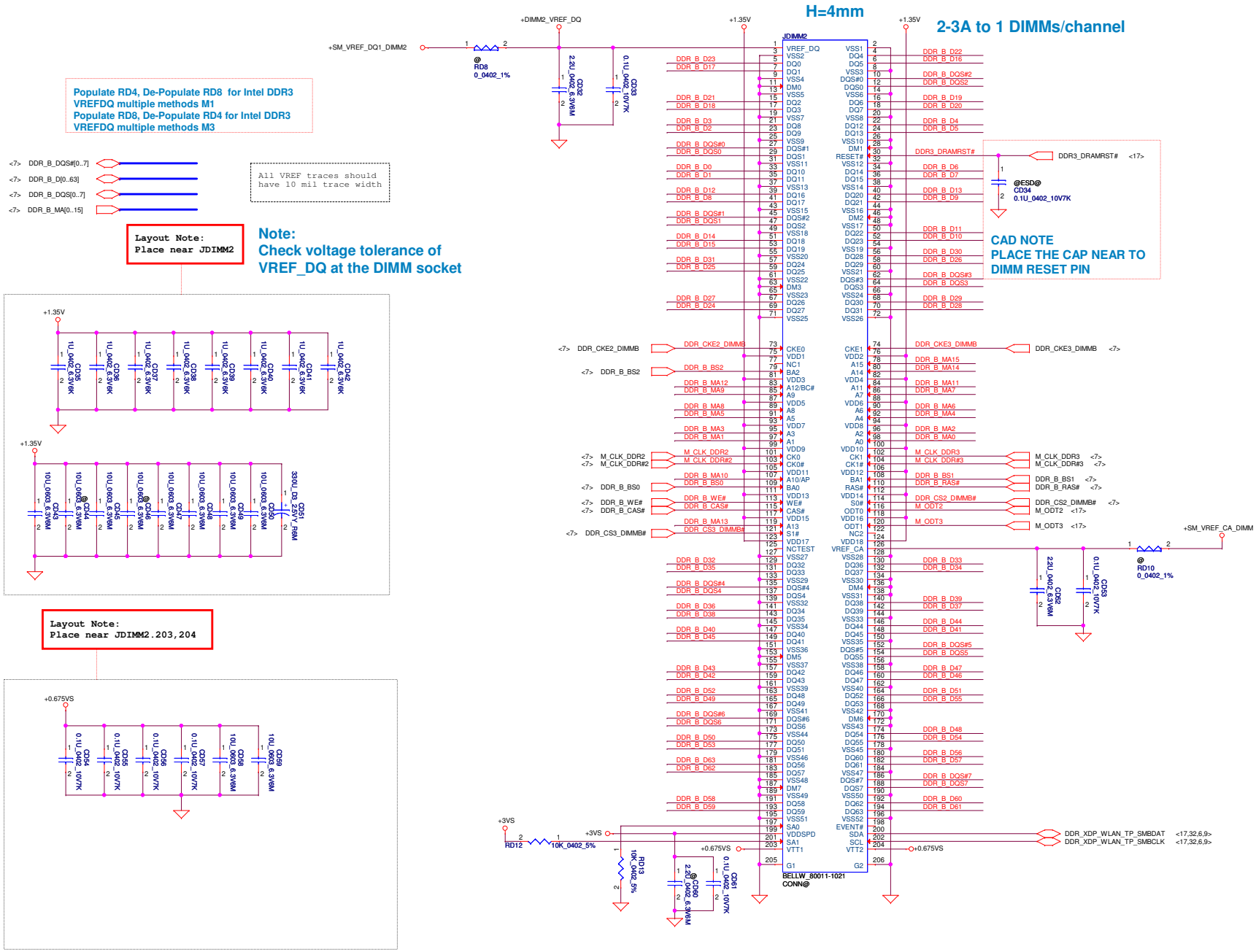
Compal Electronics, Inc.

Title: **DDRIII DIMMA**

Size: | Document Number: **LA-B012P** | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 17 of 55



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Issued Date	2014/01/20	Deciphered Date	2015/01/19

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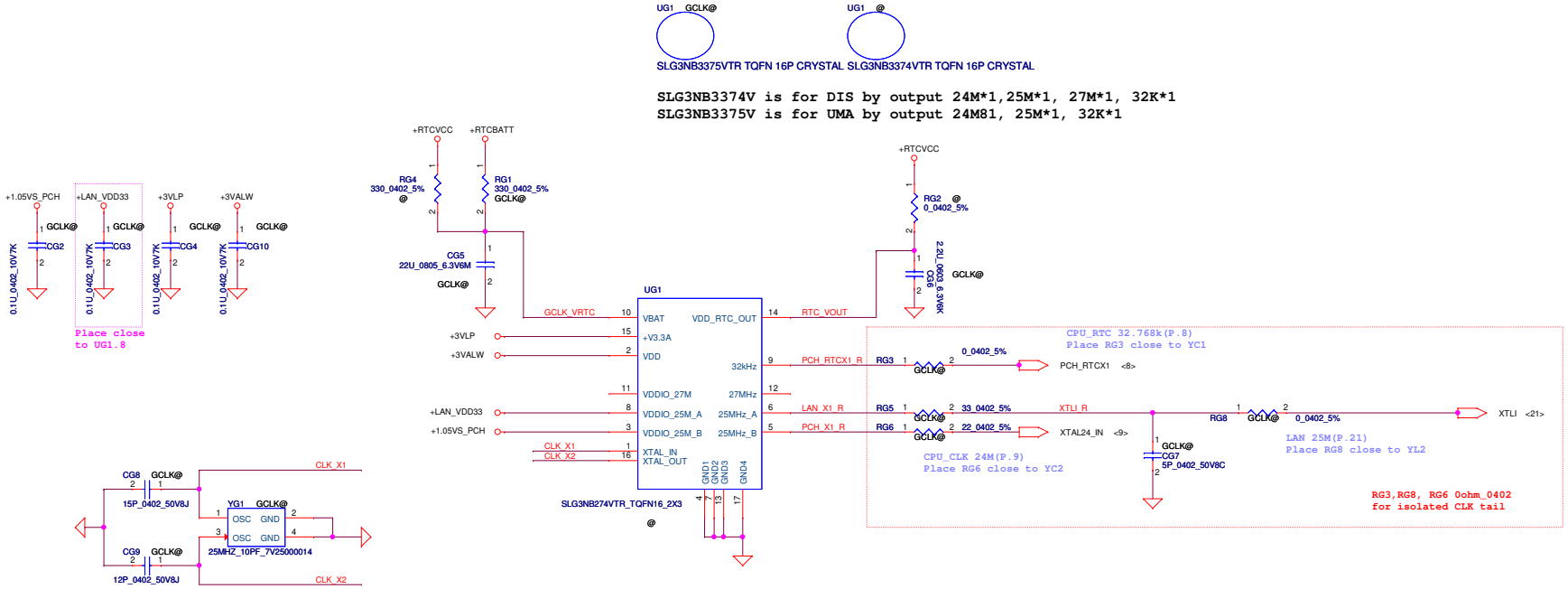
Compal Electronics, Inc.

Title: **DDRIII DIMMB**

Size: | Document Number: **LA-B012P** | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 18 of 55



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Issued Date	2014/01/20	Deciphered Date	2015/01/19

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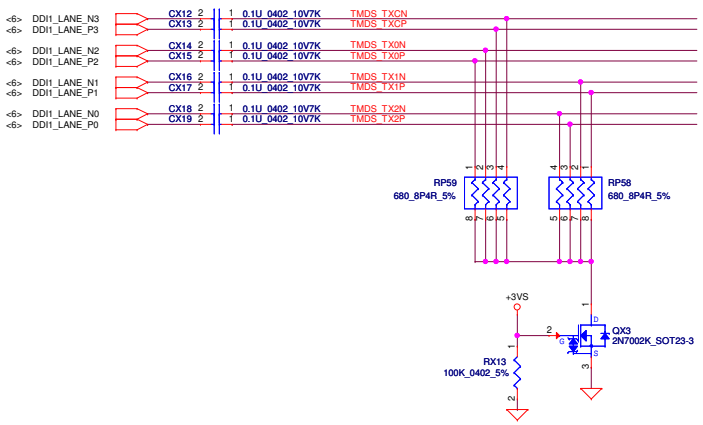
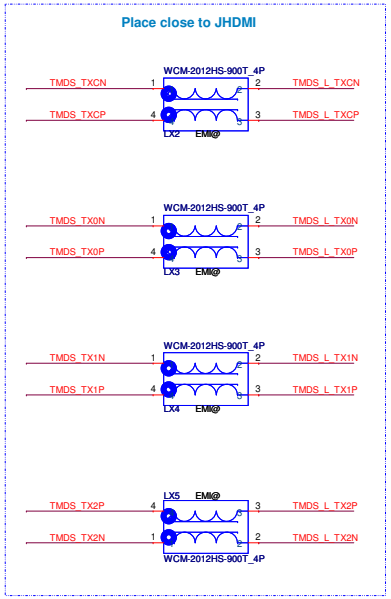
Compal Electronics, Inc.

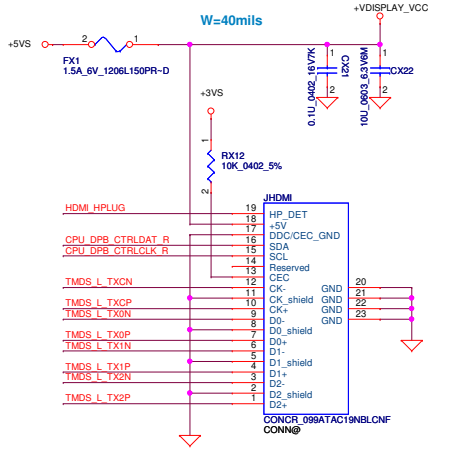
Title: **Green CLK**

Size | Document Number: **LA-B012P** | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 19 of 55

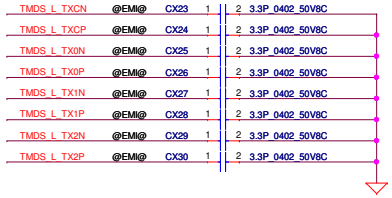


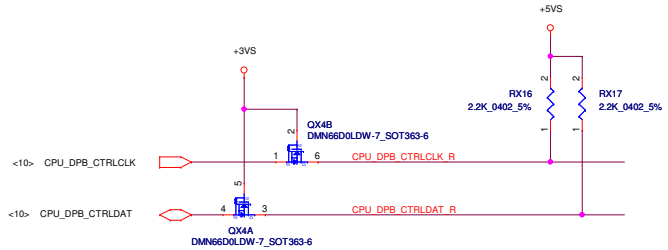


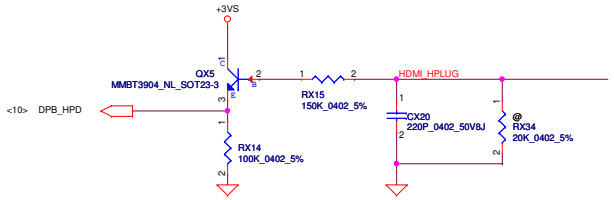


46@ ROYALTY HDMI W/LOGO

Part Number	Description
RO00000002HM	HDMI W/Logo:RO00000002HM







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Compal Electronics, Inc.

Title: HDMI

Size | Document Number: LA-B012P | Rev: 1.0

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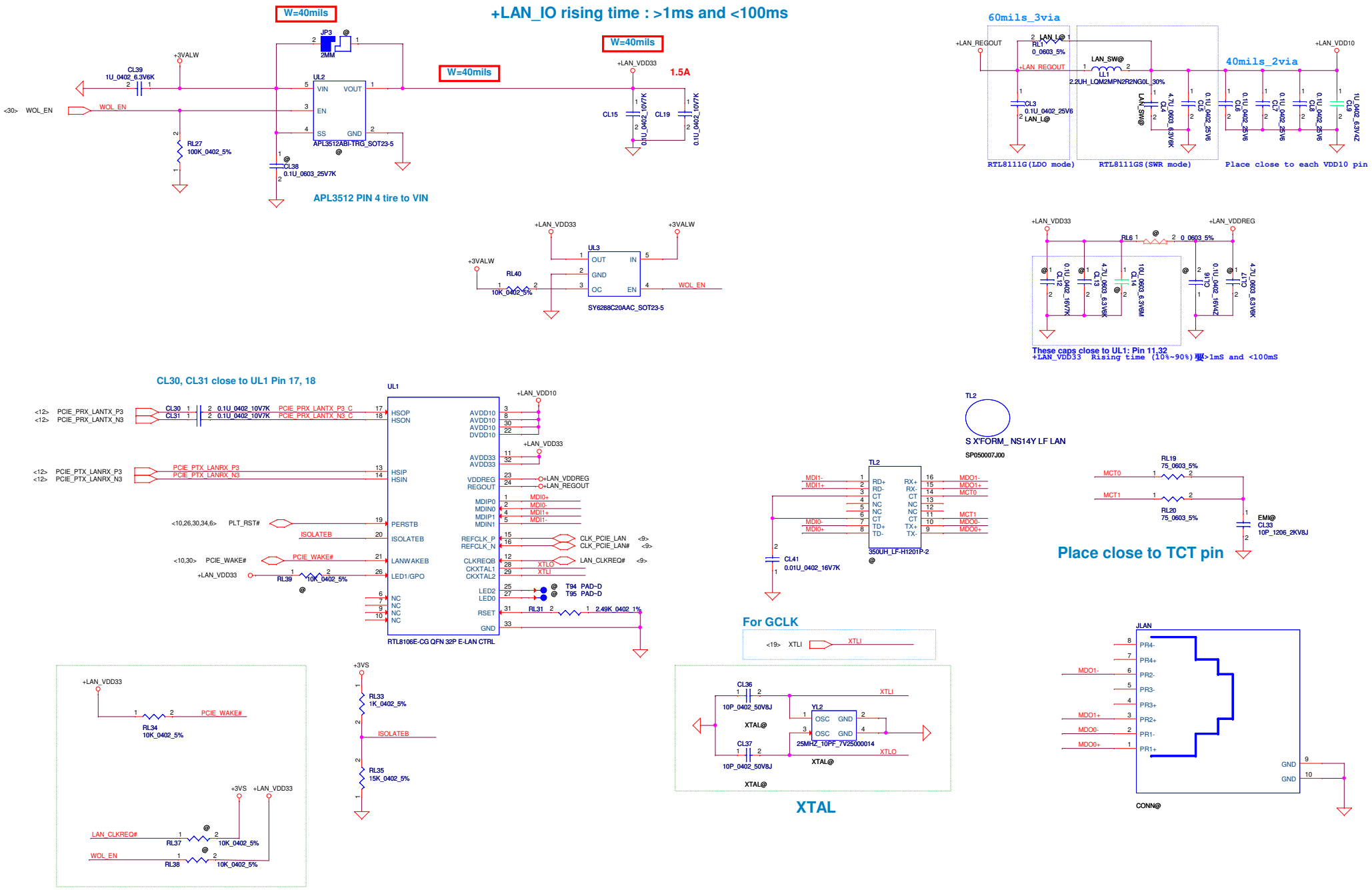

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Compal Electronics, Inc.

Title: **LAN RTL8106EUS**

Size: Custom | Document Number: **LA-B012P** | Rev: 1.0

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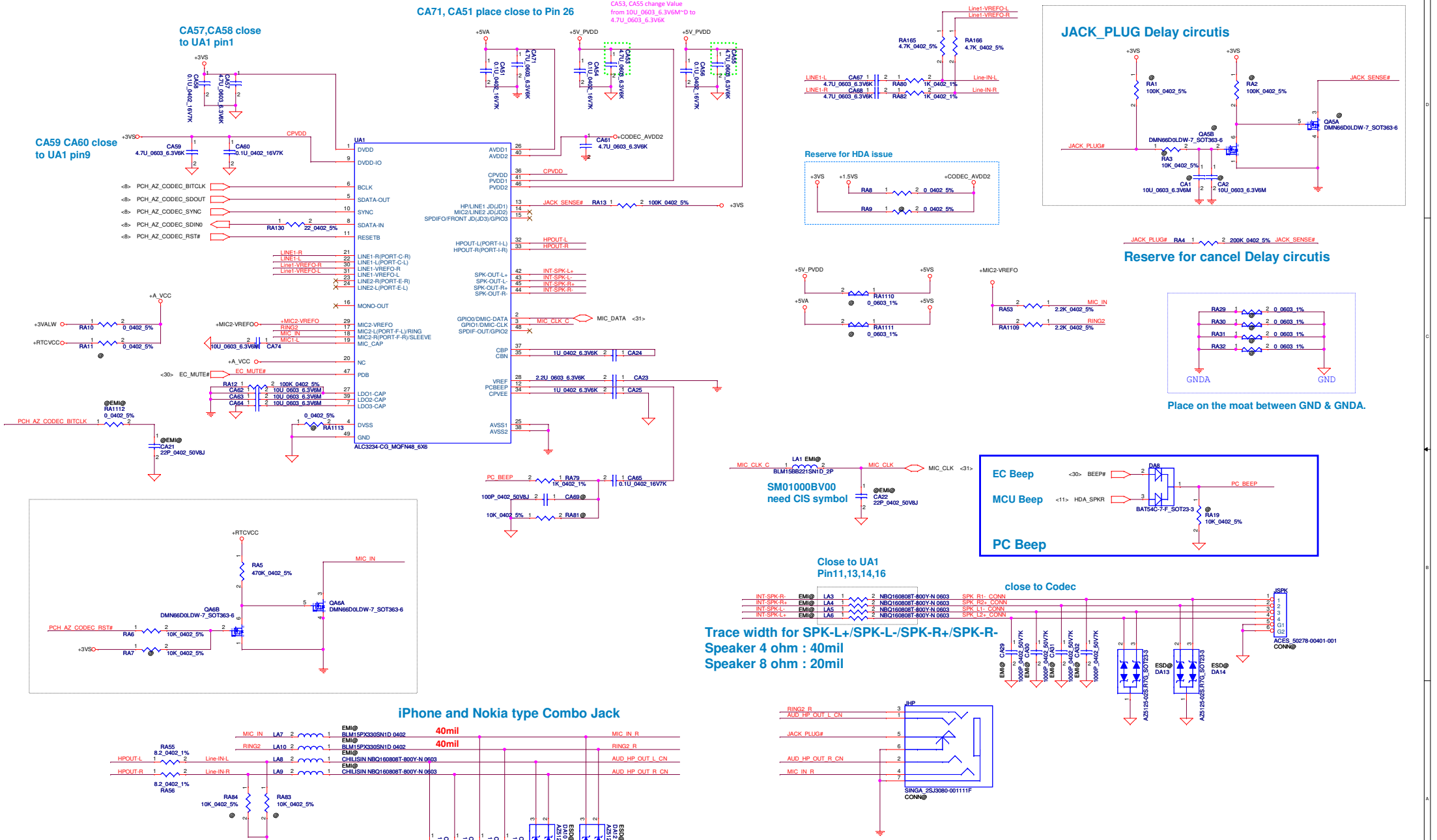

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Issued Date	2014/01/20	Deciphered Date	2015/01/19

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Compal Electronics, Inc.

Title: Audio Codec ALC3234

Document Number: LA-B012P

Rev: 1.0

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Compal Electronics, Inc.

Title: **Reserved Page**

Size | Document Number: **LA-B012P** | Rev: 1.0

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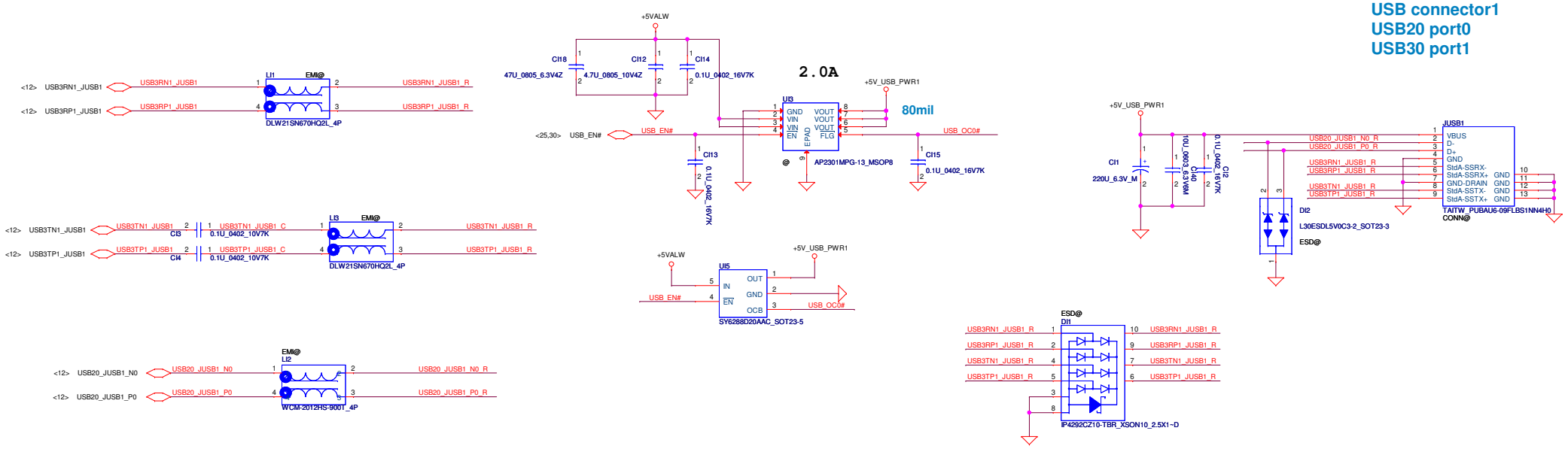
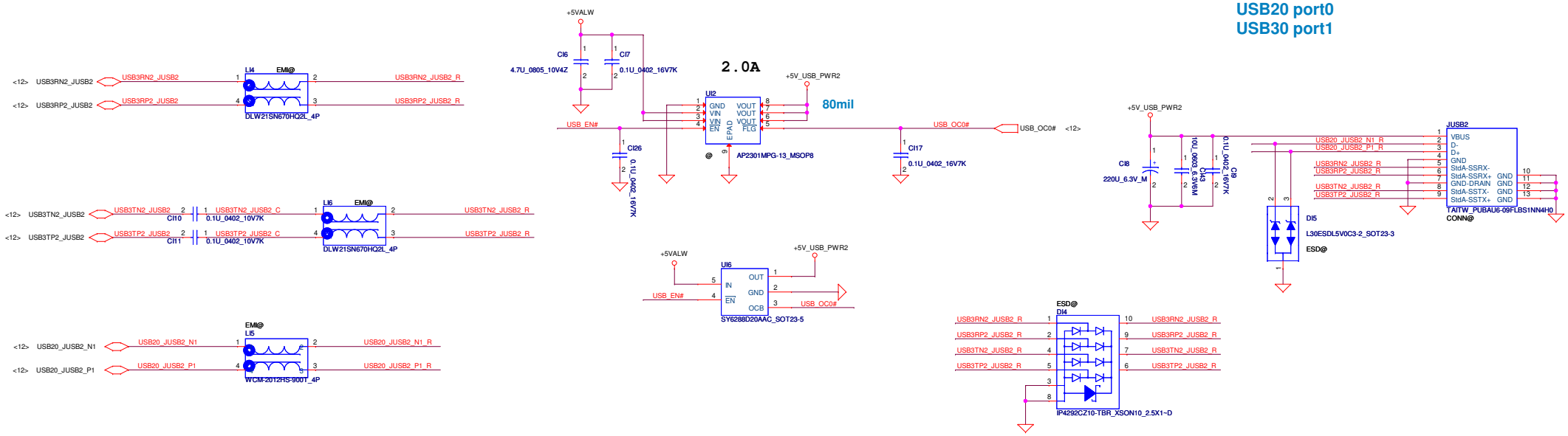
USB connector1
USB20 port0
USB30 port1



USB connector2
USB20 port0
USB30 port1



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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Compal Electronics, Inc.

Title: USB3.0

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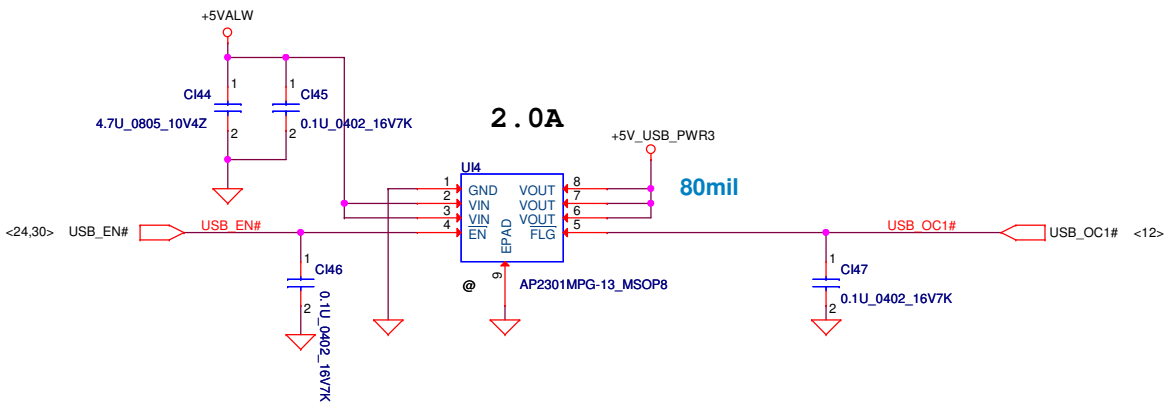
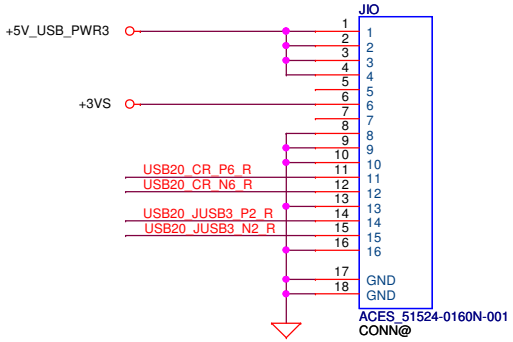
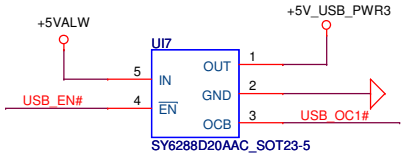
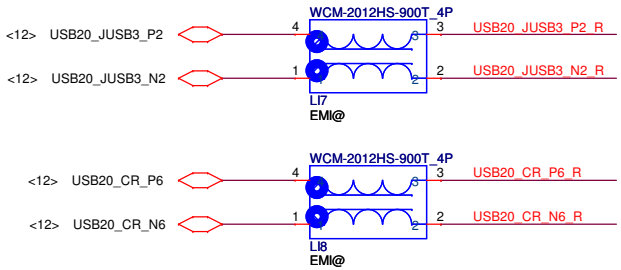
IO to MB CONN
Substitute:SP01001FS00

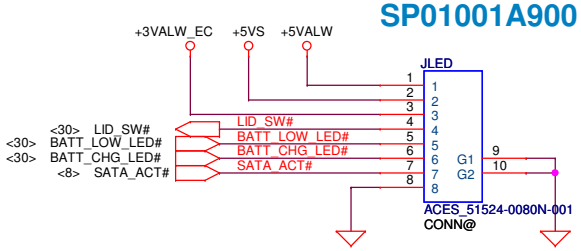






LED/B TO M/B
SP01001A900





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Title: *IO/B, LED/B*

Size: B | Document Number: *LA-B012P* | Rev: 1.0

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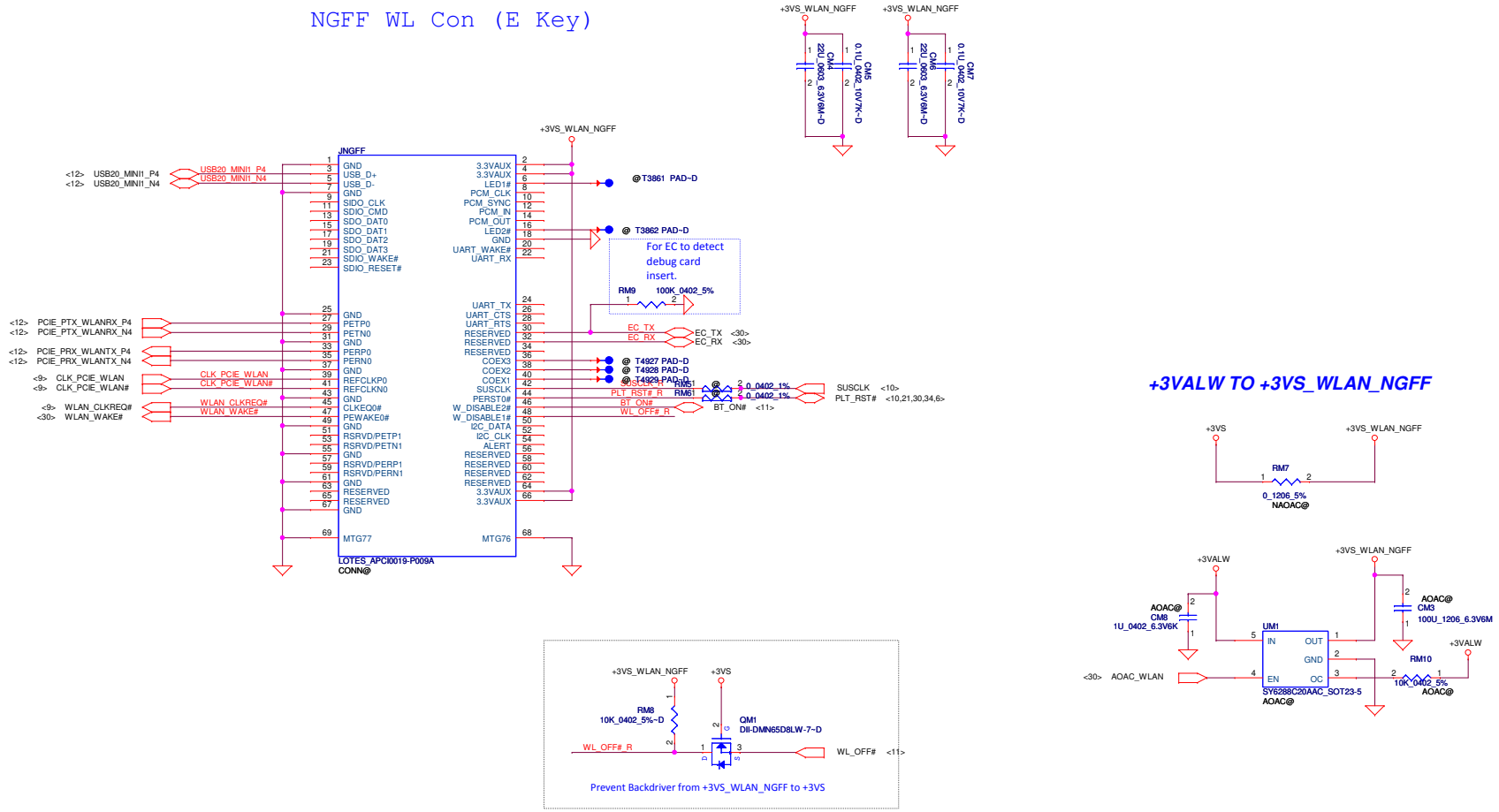
NGFF WL Con (E Key)

closed to pin 2, 4 closed to pin 64, 66



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Compal Electronics, Inc.

Title: **NGFF WLAN**

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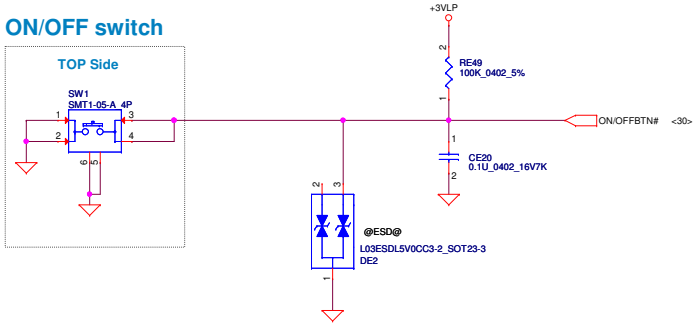
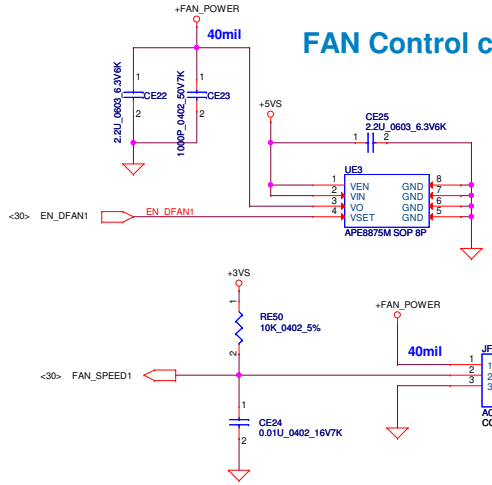
Power ON Circuit

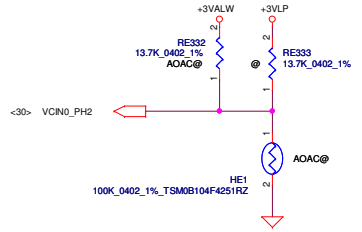
ON/OFF switch



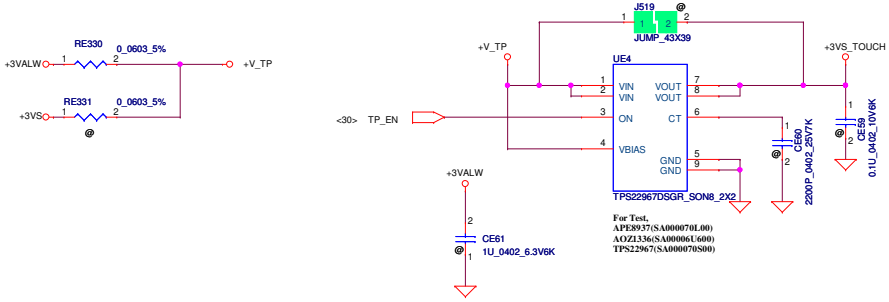
FAN Control circuit



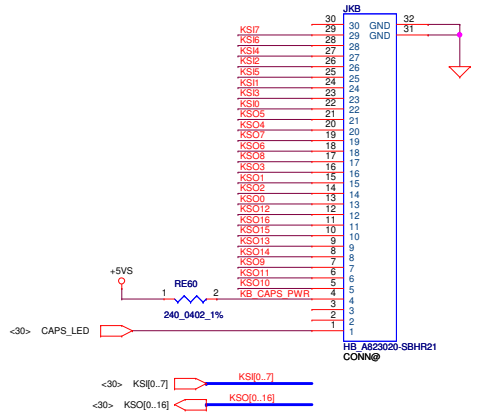
HE1 place around FAN area.

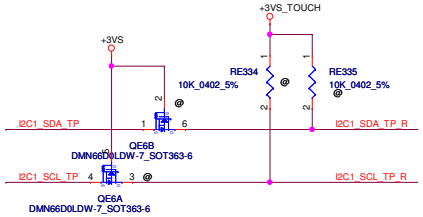


J519 short

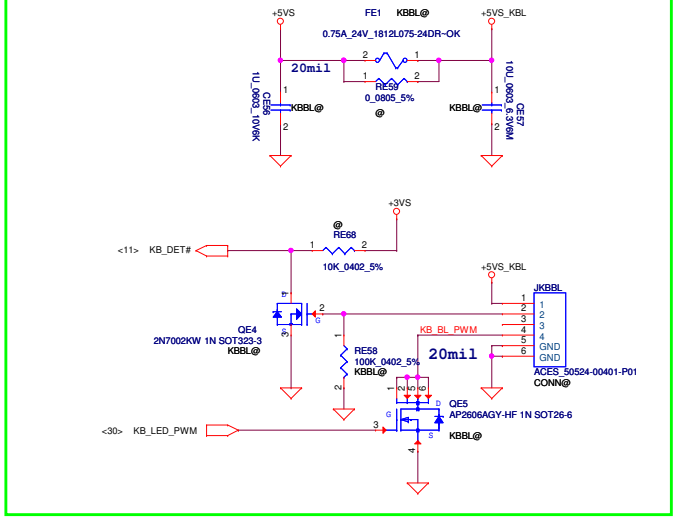


INT_KBD Connector

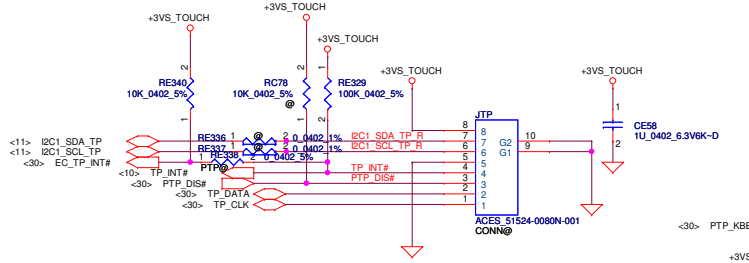




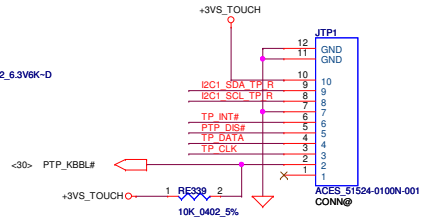
* Key Board Back Light



Touch pad



PTP



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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Compal Electronics, Inc.

Title: FAN / TP / PWR SW / KBBL

Size | Document Number: LA-B012P | Rev: 1.0

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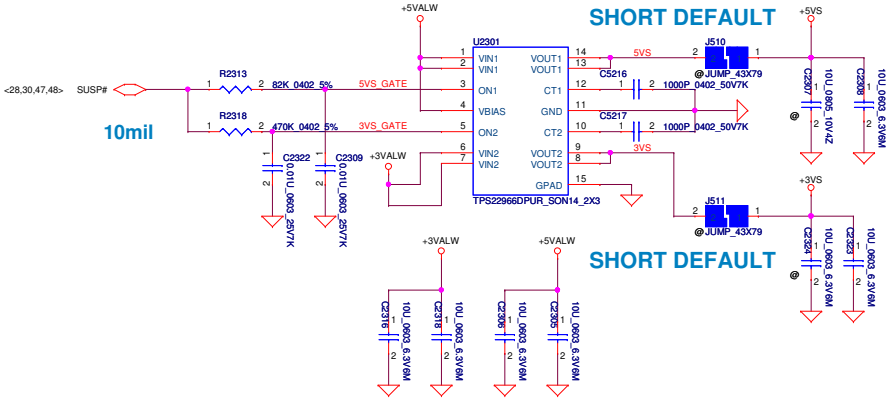
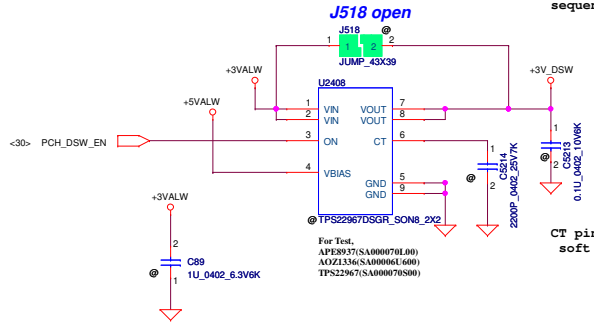
+5VS and +3VS switch



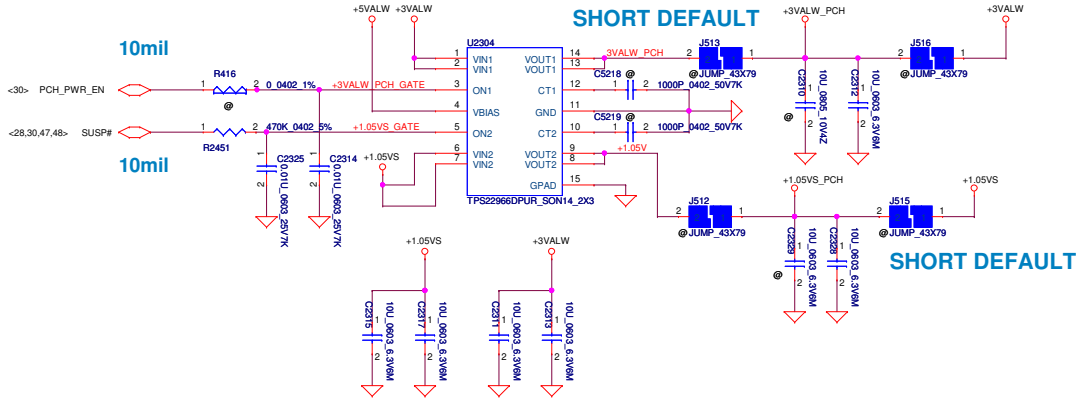
+3VALW TO +3V_DSW

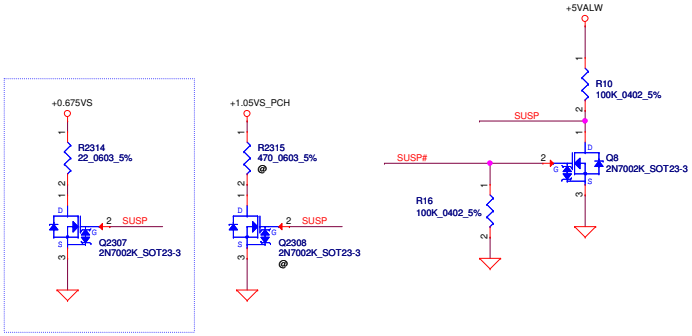


+3V_DSW have soft start sequence: +3V_DSW stable > +3VALW_PCH > 0ms

CT pin use 2200pf for soft start tuning

+3VALW_PCH switch





For Intel S3 Power Reduction

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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Compal Electronics, Inc.

Title: DC/DC Interface

Size | Document Number: LA-B012P | Rev: 1.0

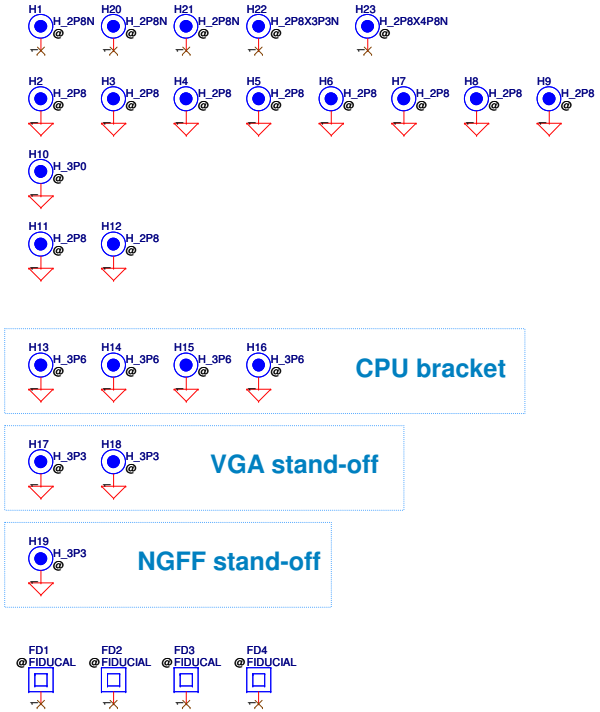
Date: Tuesday, August 05, 2014 | Sheet 28 of 55

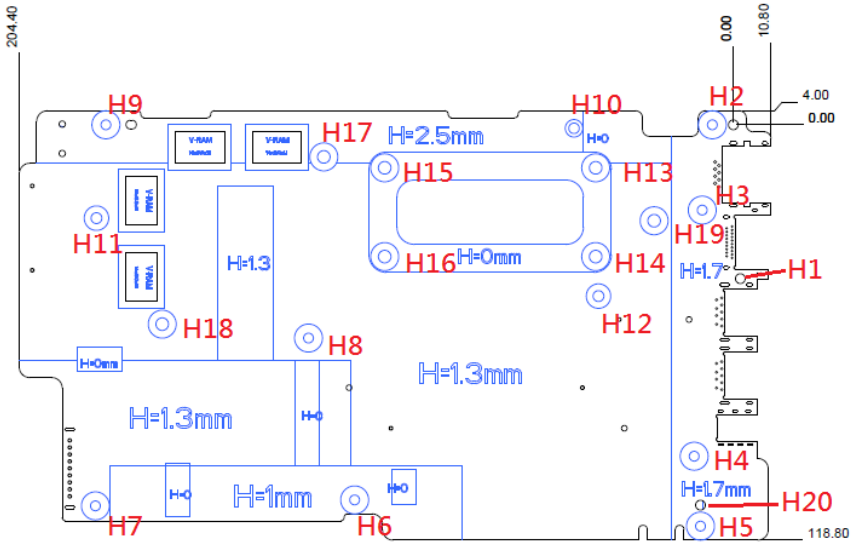
Screw Hole

ZZZ

PCB 13P LA-B011P REV0 M/B

DA60013U000





SCALE 1.000

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/01/20	Deciphered Date	2015/01/19	Title: Screw Hole
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				Date: Tuesday, August 05, 2014 / Sheet 29 of 55

SD034120280	12K_0402_1%
SD034270280	27K_0402_1%
SD034430280	43K_0402_1%
SD034560280	56K_0402_1%
SD034750280	75K_0402_1%
SD034100380	100K_0402_1%
SD034130380	130K_0402_1%
SD034160380	160K_0402_1%
SD034200380	200K_0402_1%
SD028430380	430K_0402_1%
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SD034330280	33K_0402_1%
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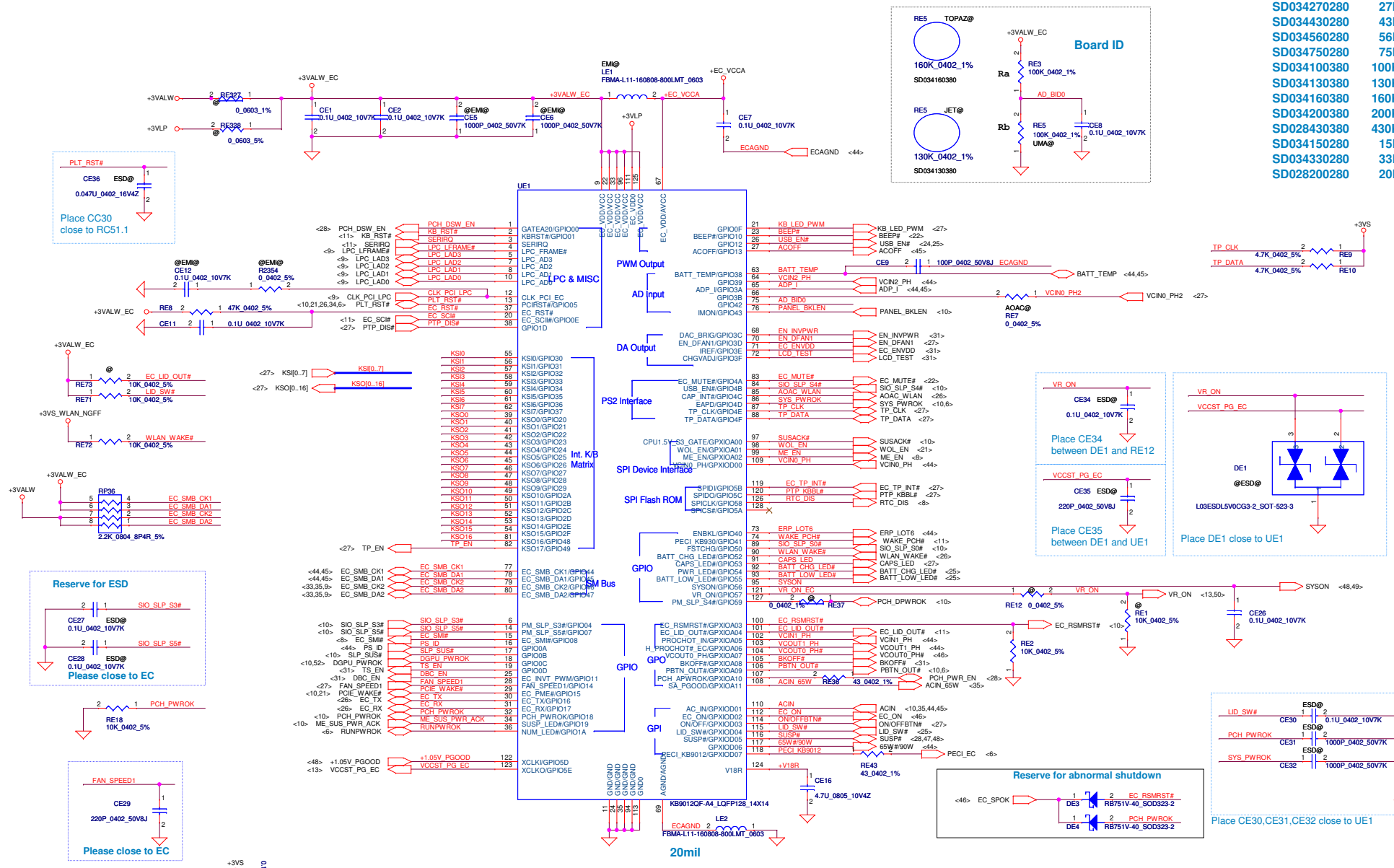

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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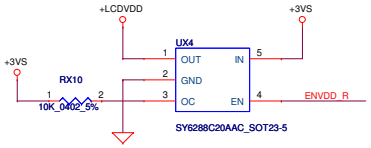
Compal Electronics, Inc.

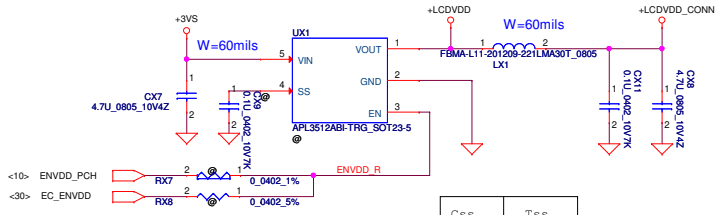
Title: EC ENE-KB9012

Size: | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 30 of 55

LCD PWR CTRL

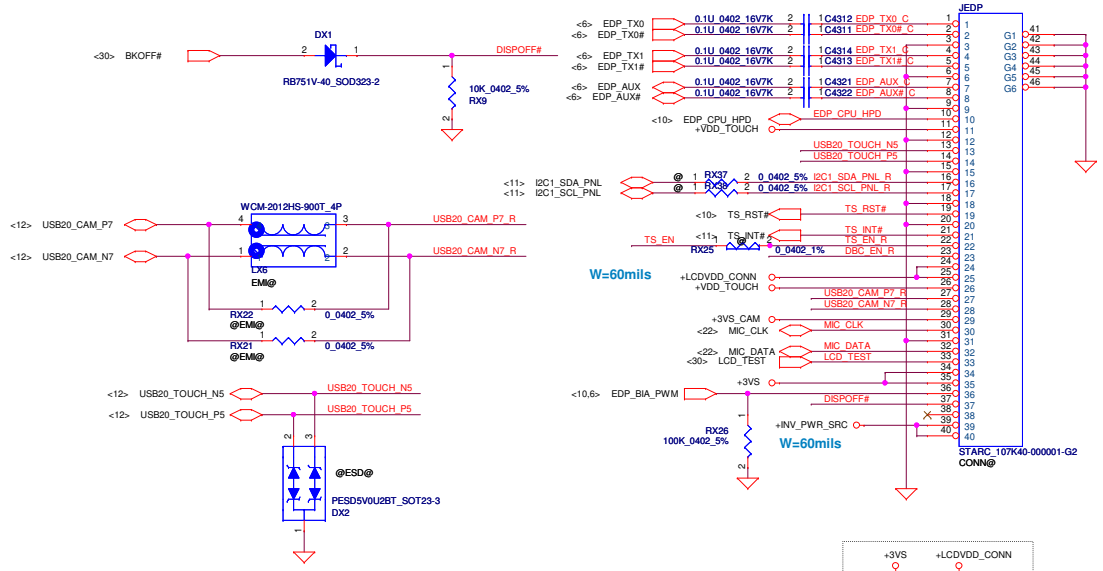




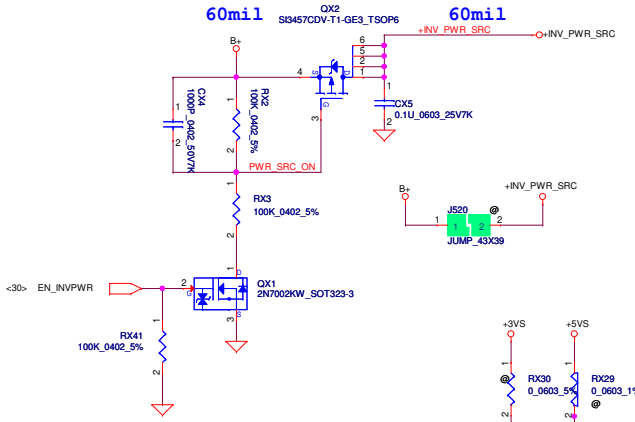
Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

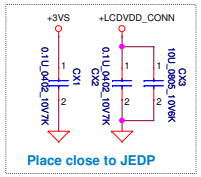
SS table

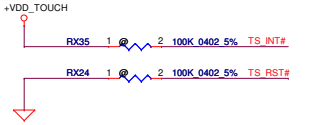
eDP Connector

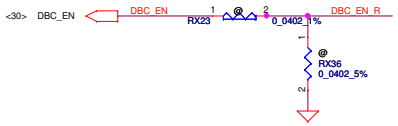


LCD backlight PWR CTRL

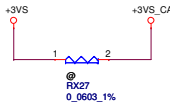




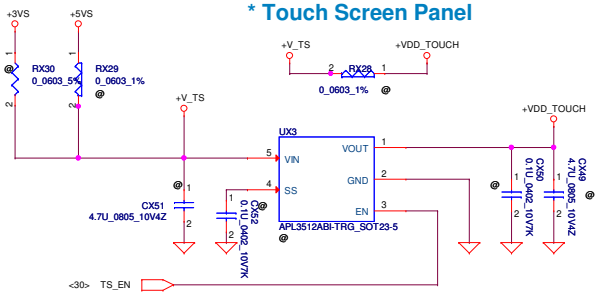


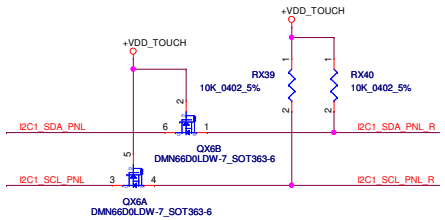


Webcam PWR CTRL



* Touch Screen Panel





Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

SS table

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/01/20	Deciphered Date	2015/01/19	Title: eDP / webcam / TouchScreen
				Size / Document Number: LA-B012P / Rev: 1.0
				Date: Tuesday, August 05, 2014 / Sheet 31 of 55

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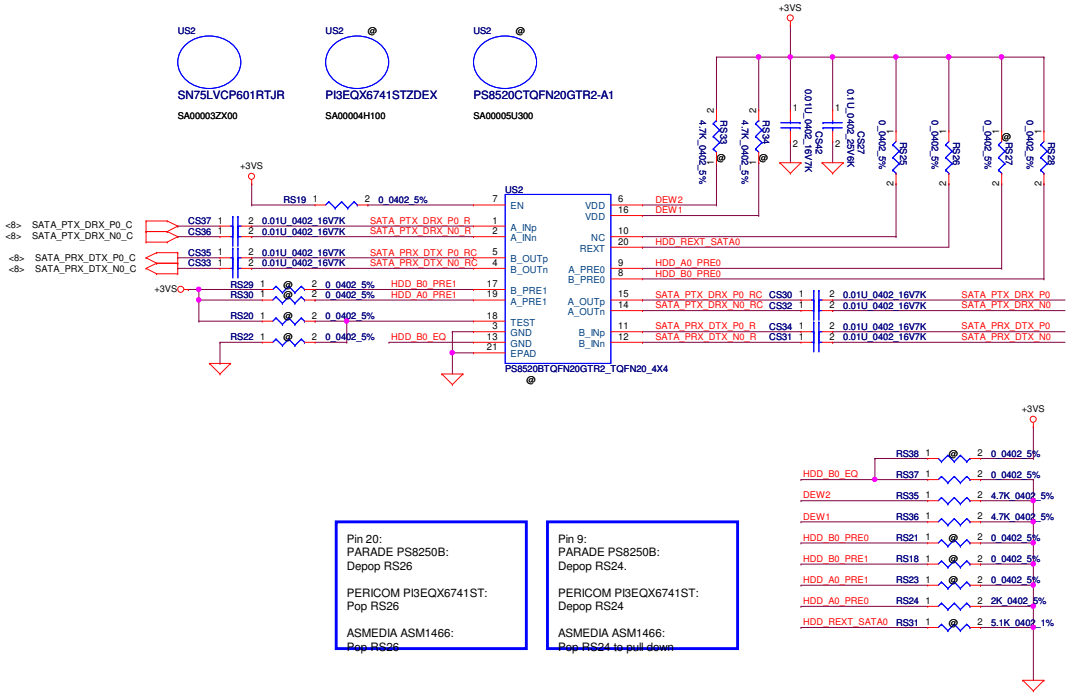
SATA HDD Connector



Pin 20:
PARADE PS8250B:
Depop RS26

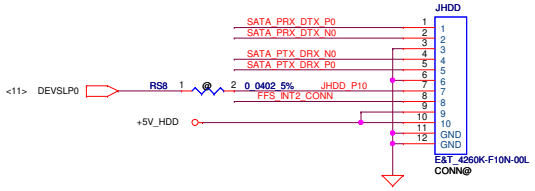
PERICOM PI3EQX6741ST:
Pop RS26

ASMEDIA ASM1466:
Pop RS26

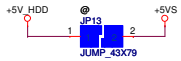
Pin 9:
PARADE PS8250B:
Depop RS24.

PERICOM PI3EQX6741ST:
Depop RS24

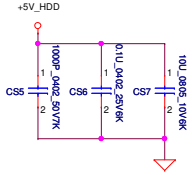
ASMEDIA ASM1466:
Pop RS24 to pull down



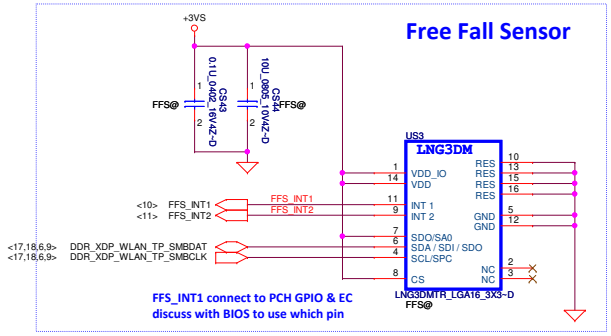
+5V_HDD Source

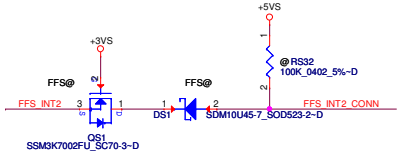


SHORT DEFAULT



Free Fall Sensor





Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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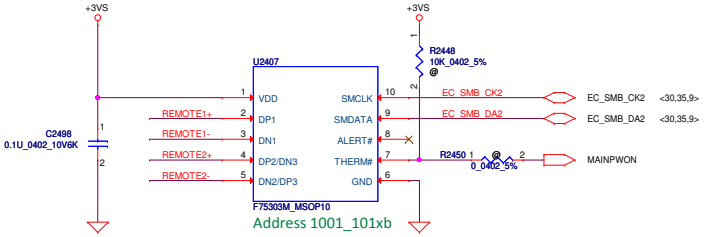
Compal Electronics, Inc.

Title: HDD

Size | Document Number: LA-B012P | Rev: 1.0

Date: Tuesday, August 05, 2014 | Sheet 32 of 55

Fintek thermal sensor
placed near by TOP DDR3



Address 1001_101xb

2nd source

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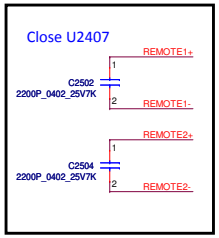

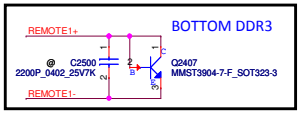

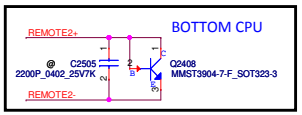

REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/01/20	Deciphered Date	2015/01/19	Title: Thermal Sensor
				Size / Document Number: LA-B012P / Rev: 1.0
				Date: Tuesday, August 05, 2014 / Sheet 33 of 55

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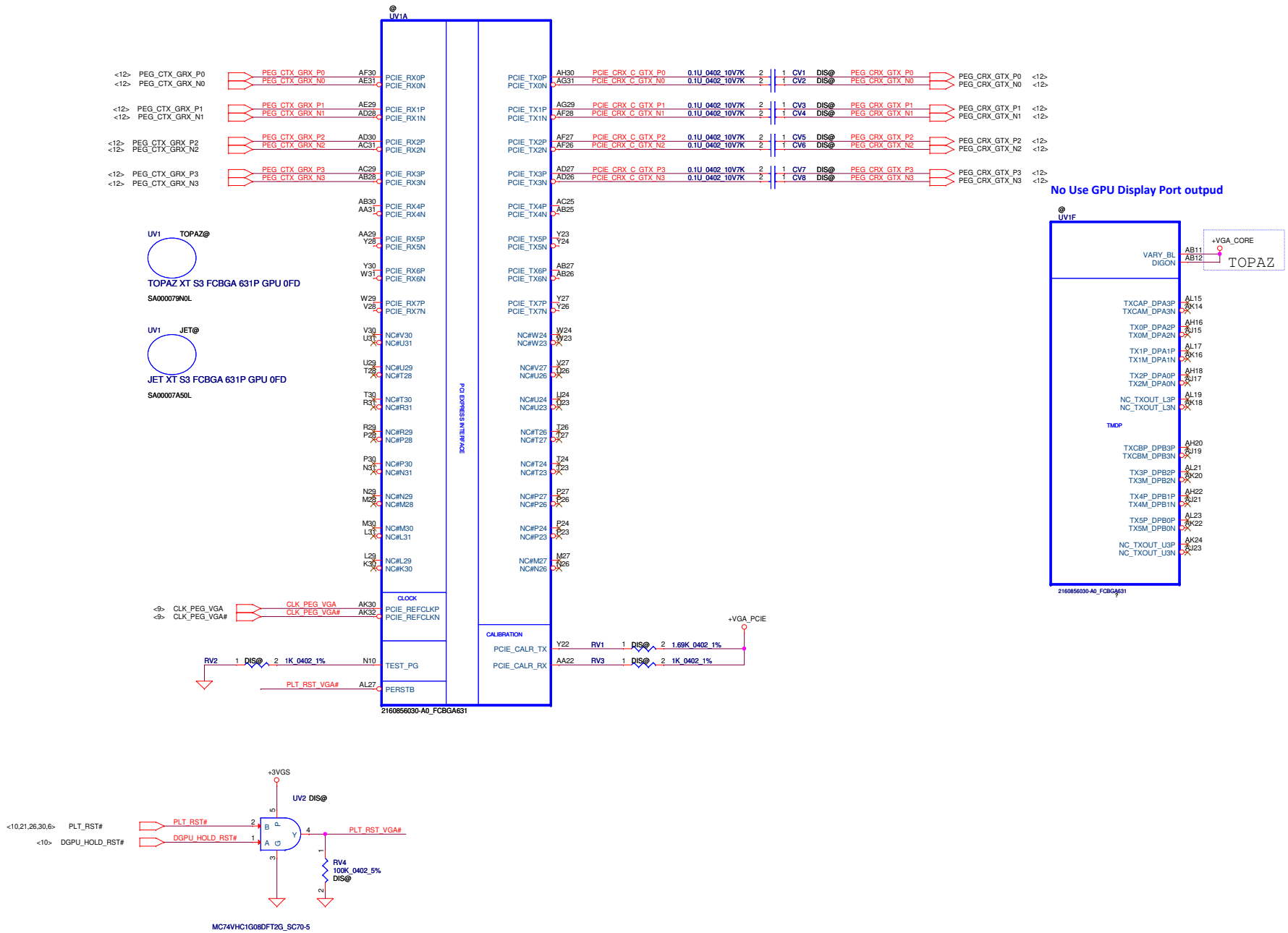

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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Compal Electronics, Inc.

Title: **TOPAZ_PCIE/DP**

Size: Custom | Document Number: **LA-B012P** | Rev: 1.0

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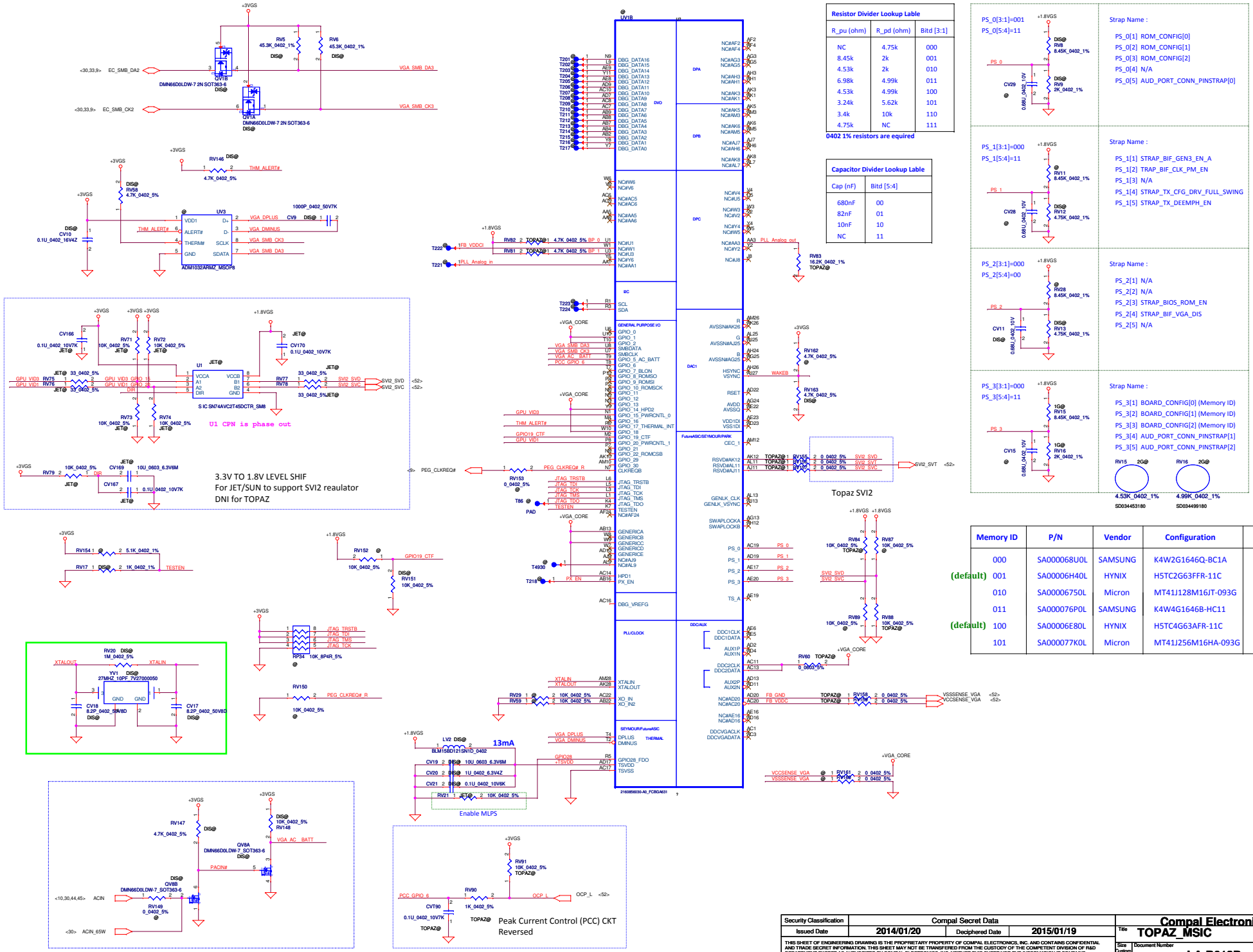

Resistor Divider Lookup Lable		
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are equired

Capacitor Divider Lookup Lable	
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	11
NC	11

PS_0[3:1]=001
PS_0[5:4]=11

Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]

PS_1[3:1]=000
PS_1[5:4]=11

Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN

PS_2[3:1]=000
PS_2[5:4]=00

Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A

PS_3[3:1]=000
PS_3[5:4]=11

Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

RV15 2G@ 4.53K_0402_1% SD034453180
RV16 2G@ 4.99K_0402_1% SD034499180

Memory ID	P/N	Vendor	Configuration	Size
000	SA000068U0L	SAMSUNG	K4W2G1646Q-BC1A	1GB
(default) 001	SA00006H40L	HYNIX	H5TC2G63FFR-11C	1GB
010	SA00006750L	Micron	MT41J128M16JT-093G	1GB
011	SA000076P0L	SAMSUNG	K4W4G1646B-HC11	2GB
(default) 100	SA00006E80L	HYNIX	H5TC4G63AFR-11C	2GB
101	SA000077K0L	Micron	MT41J256M16HA-093G	2GB

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: TOPAZ_MSIC

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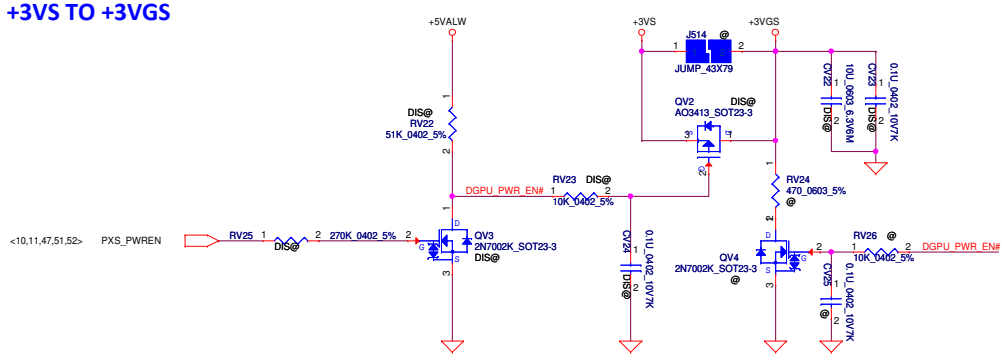
Date: Tuesday, August 05, 2014 | Sheet 35 of 55

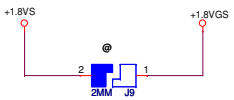
+3VS TO +3VGS



+1.35VS_VGA TO +1.35V_MEM_GFX

SHORT DEFAULT

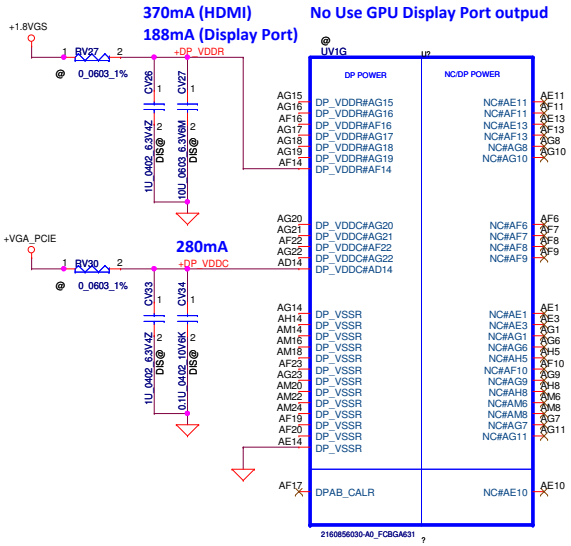
+1.8VS TO +1.8VGS

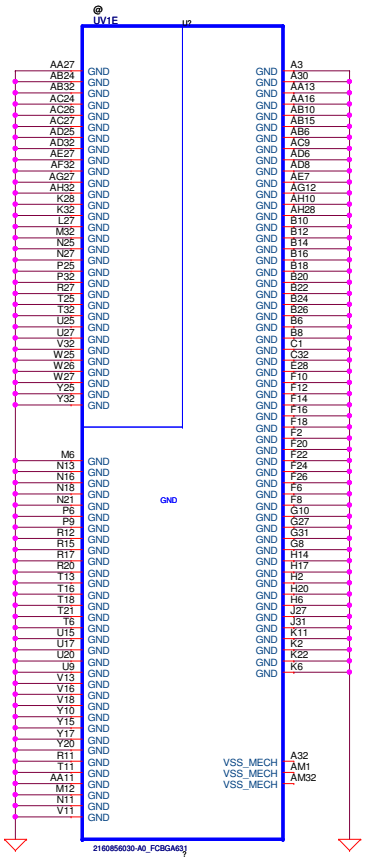


SHORT DEFAULT

370mA (HDMI)
188mA (Display Port)

No Use GPU Display Port outpud





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Compal Electronics, Inc.

Title: TOPAZ_Power/GND

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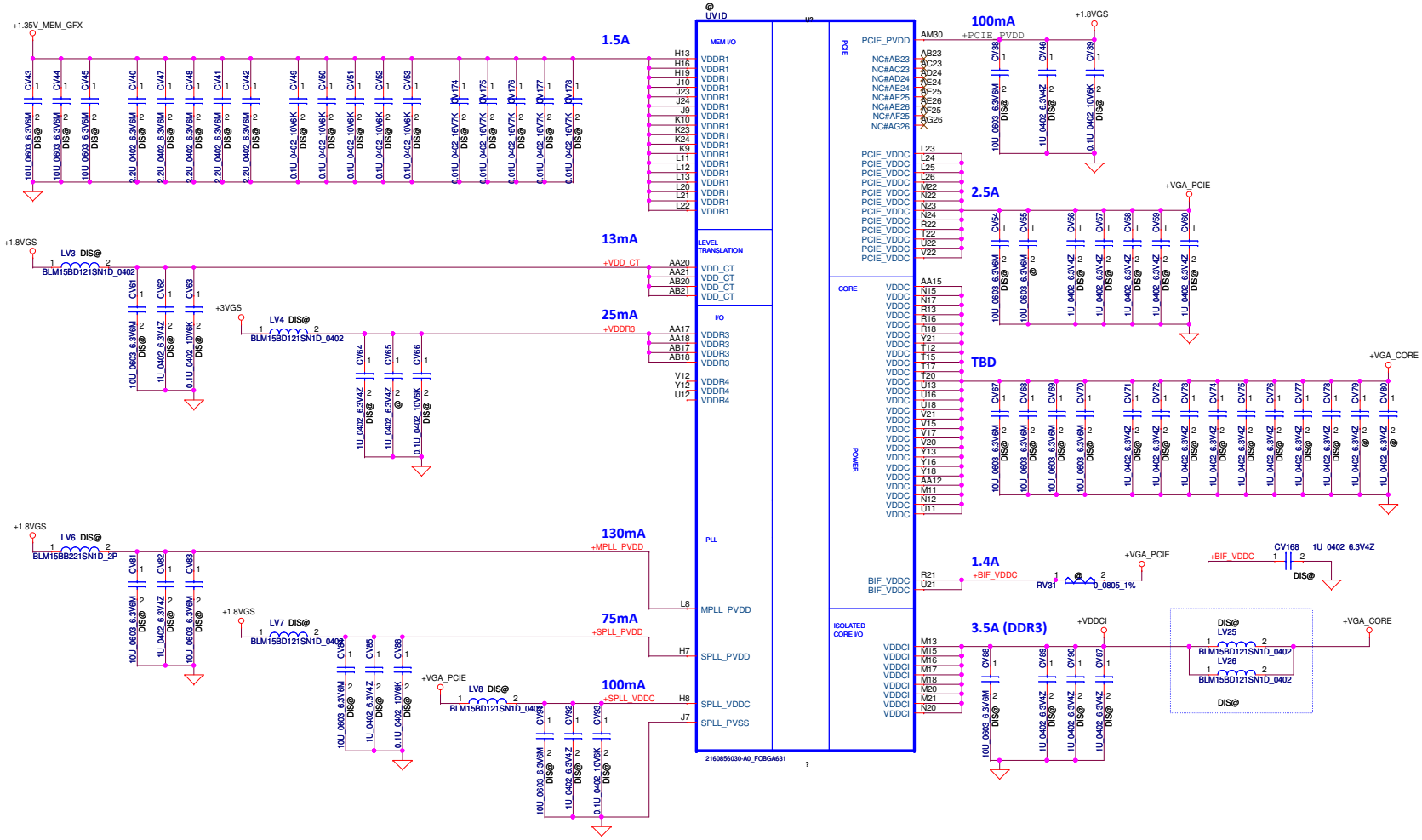
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+VGA_PCIE		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	1	0
SPLL_VDDC	100mA	1	1	1

+1.35V_MEM_GFX		10uF	2.2uF	0.1uF	0.01uF
VDDR1	1.5A	3	5	5	5

+1.8VGS		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VGS		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



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Compal Electronics, Inc.

Title: **TOPAZ_Power**

Size: Custom | Document Number: **LA-B012P** | Rev: 1.0

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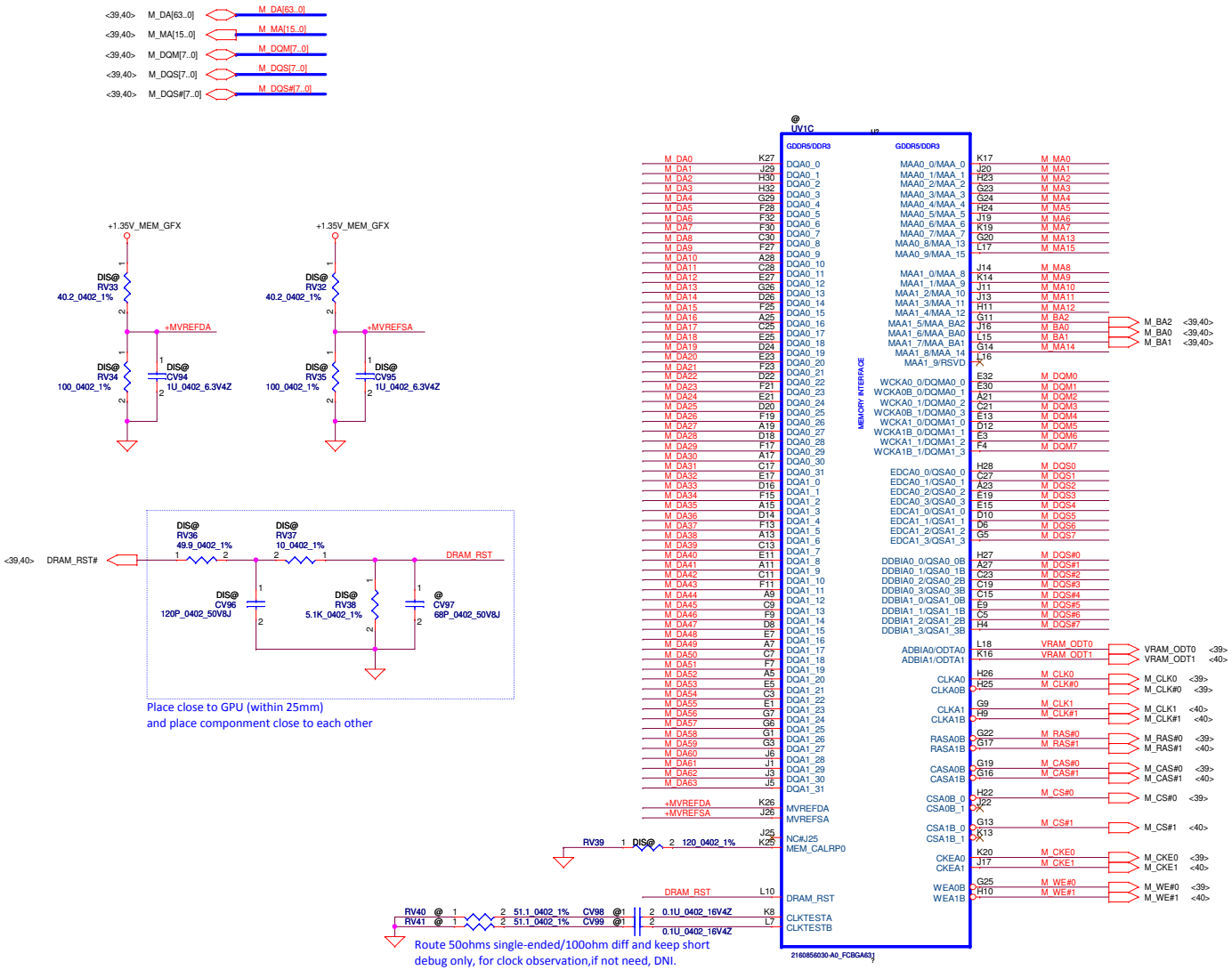

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Title: **TOPAZ_MEM**

Size: Custom | Document Number: **LA-B012P** | Rev: 1.0

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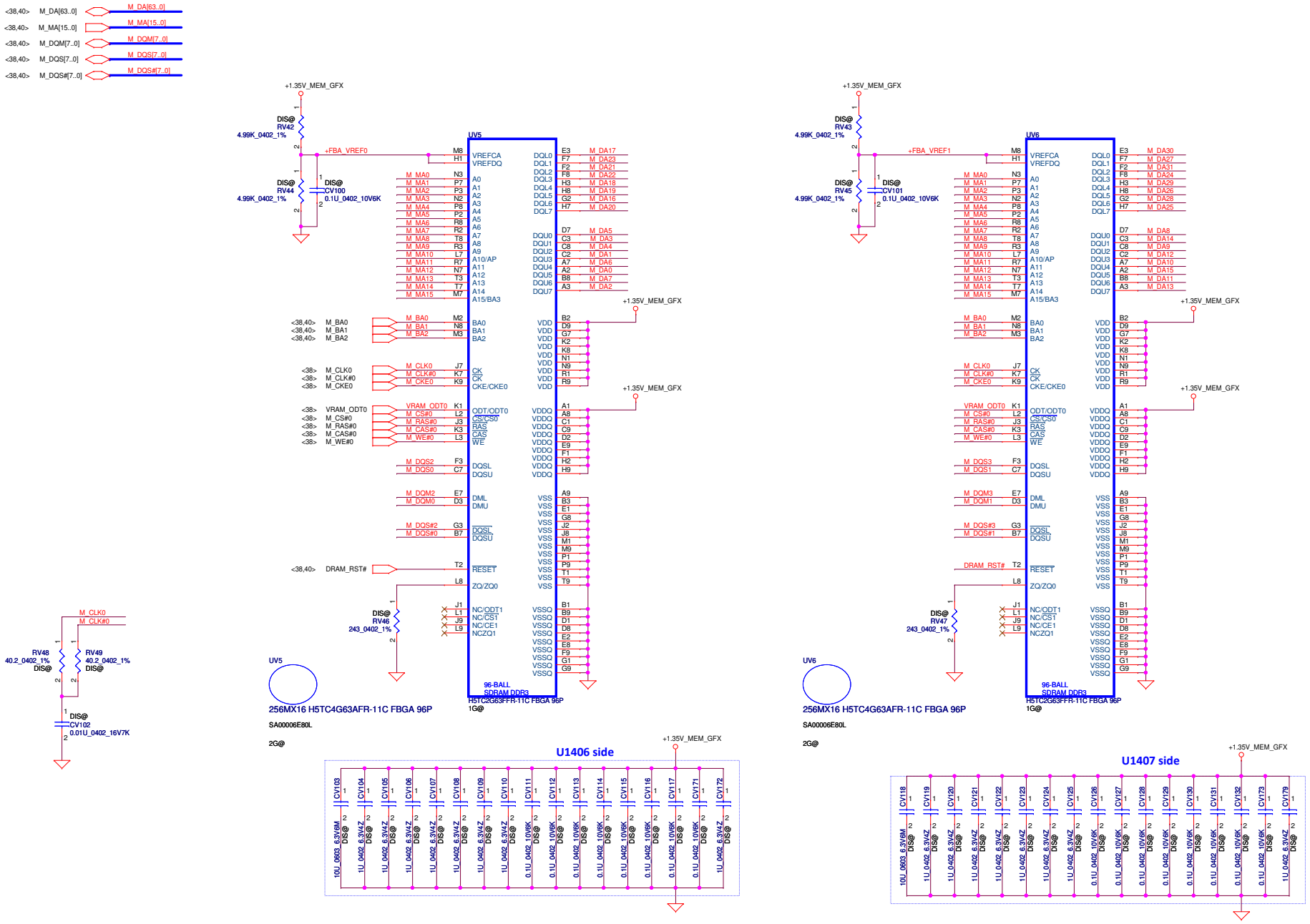
Memory Partition A - Lower 32 bits



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Compal Electronics, Inc.

Title: **TOPAZ_VRAM A Lower**

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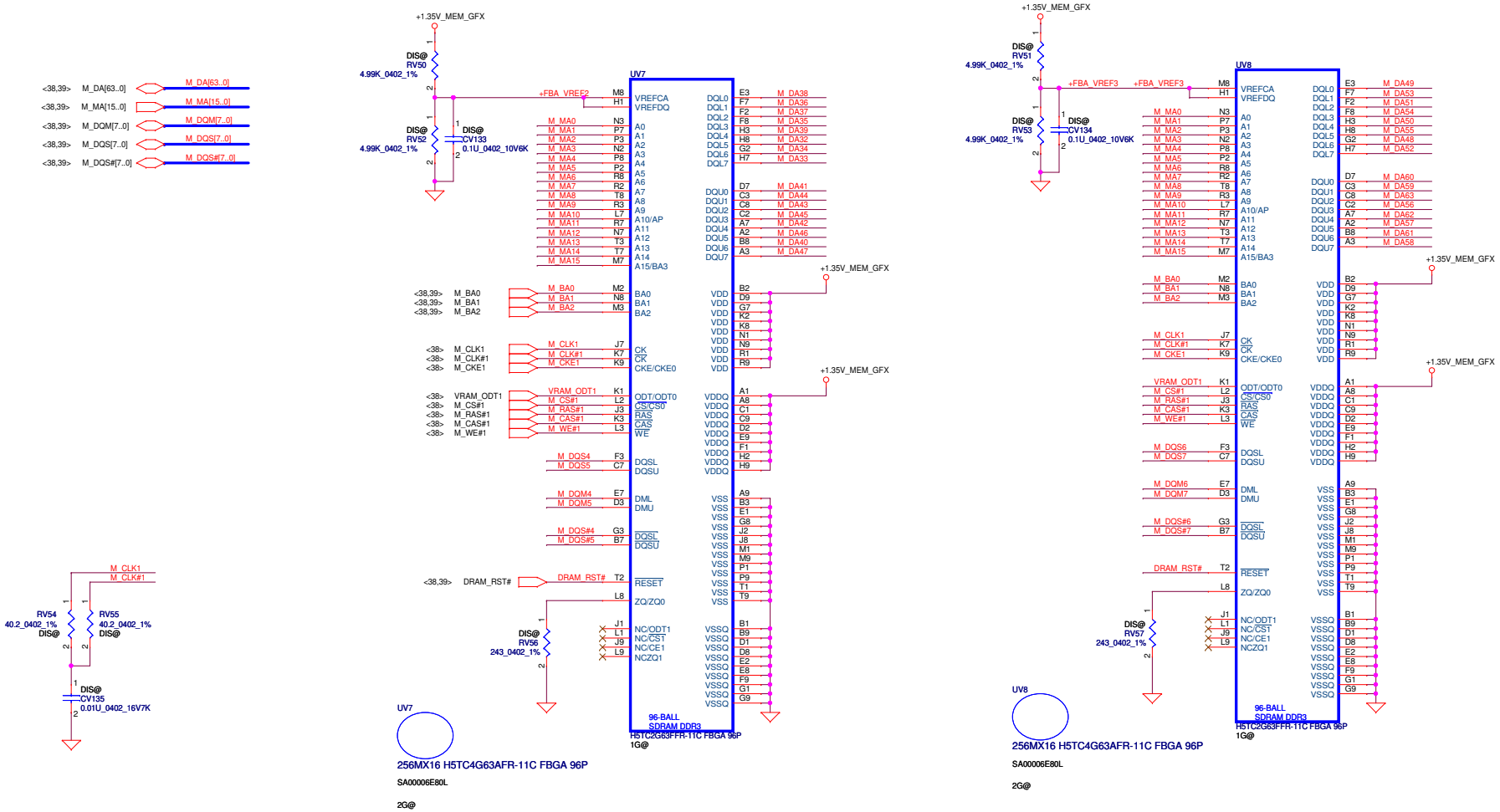
Memory Partition A - Upper 32 bits



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Issued Date	2014/01/20	Deciphered Date	2015/01/19

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Compal Electronics, Inc.

Title: **TOPAZ_VRAM A Upper**

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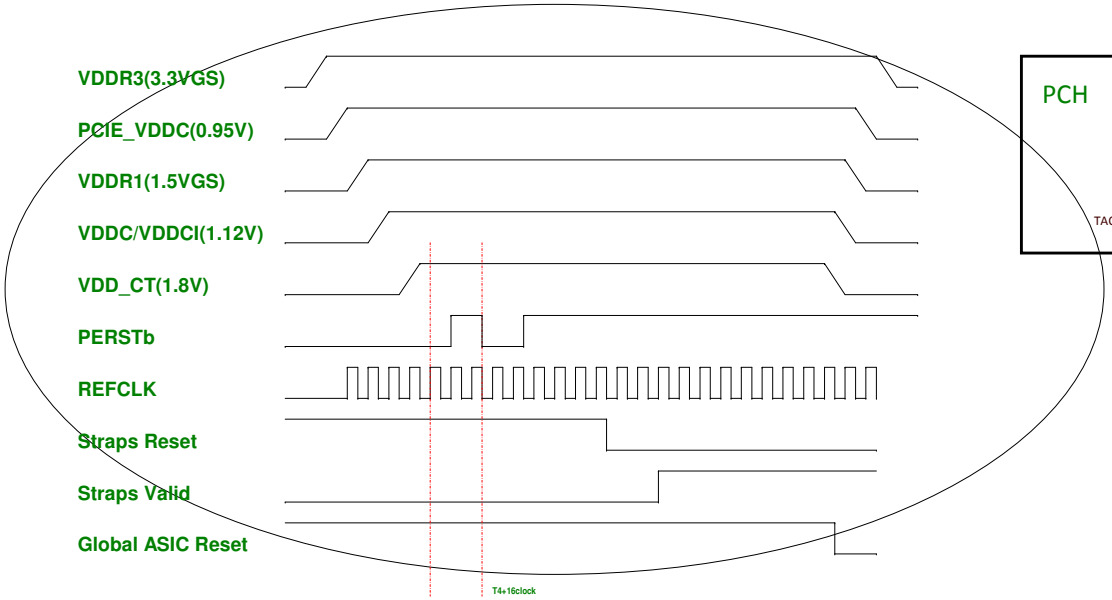
Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.

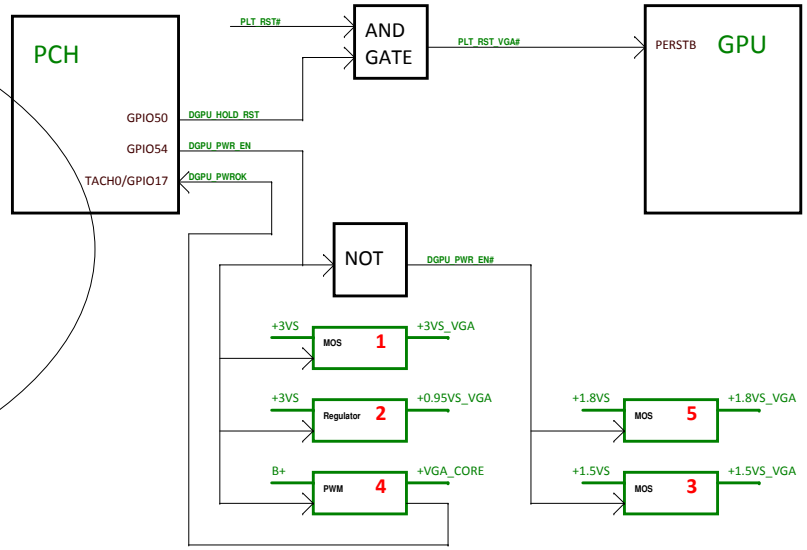
2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.

3. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).

4. For power down, reversing the ramp-up sequence is recommended.



CPU part



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Compal Electronics, Inc.

Title: **TOPAZ_NOTE**

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Title: **Reserved Page**

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Compal Electronics, Inc.

Title: **Reserved Page**

Size | Document Number: **LA-B012P** | Rev: 1.0

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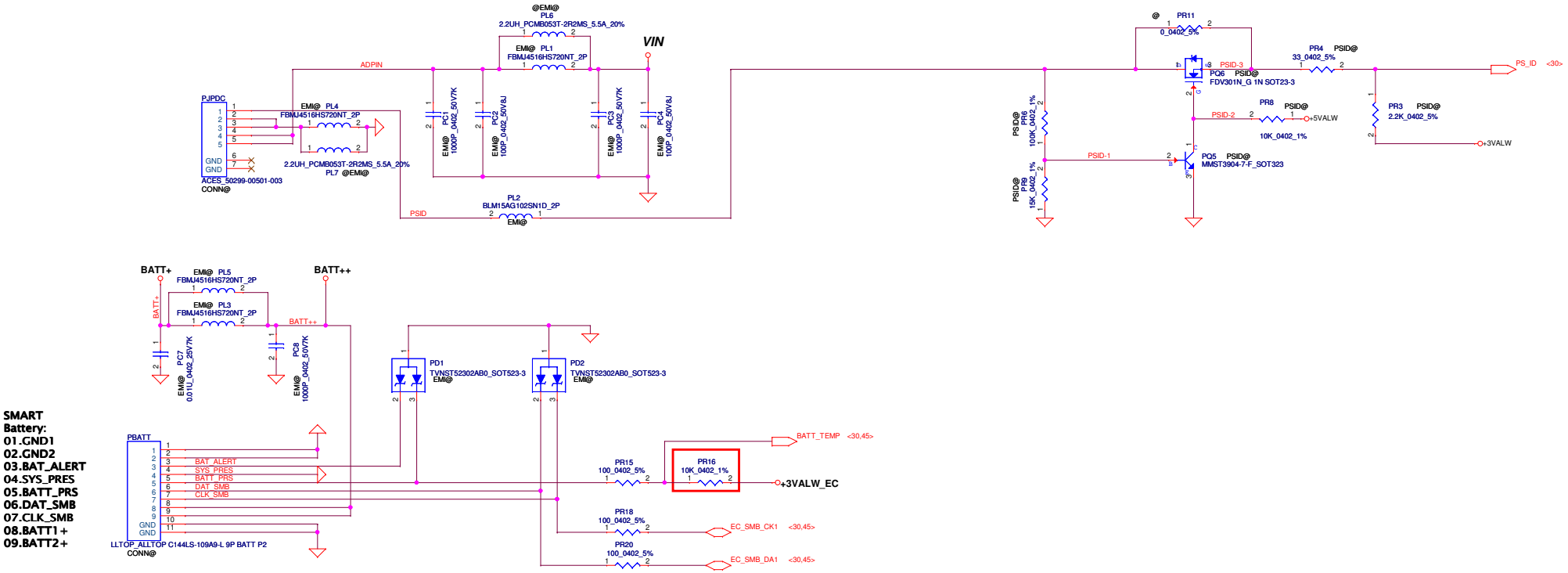
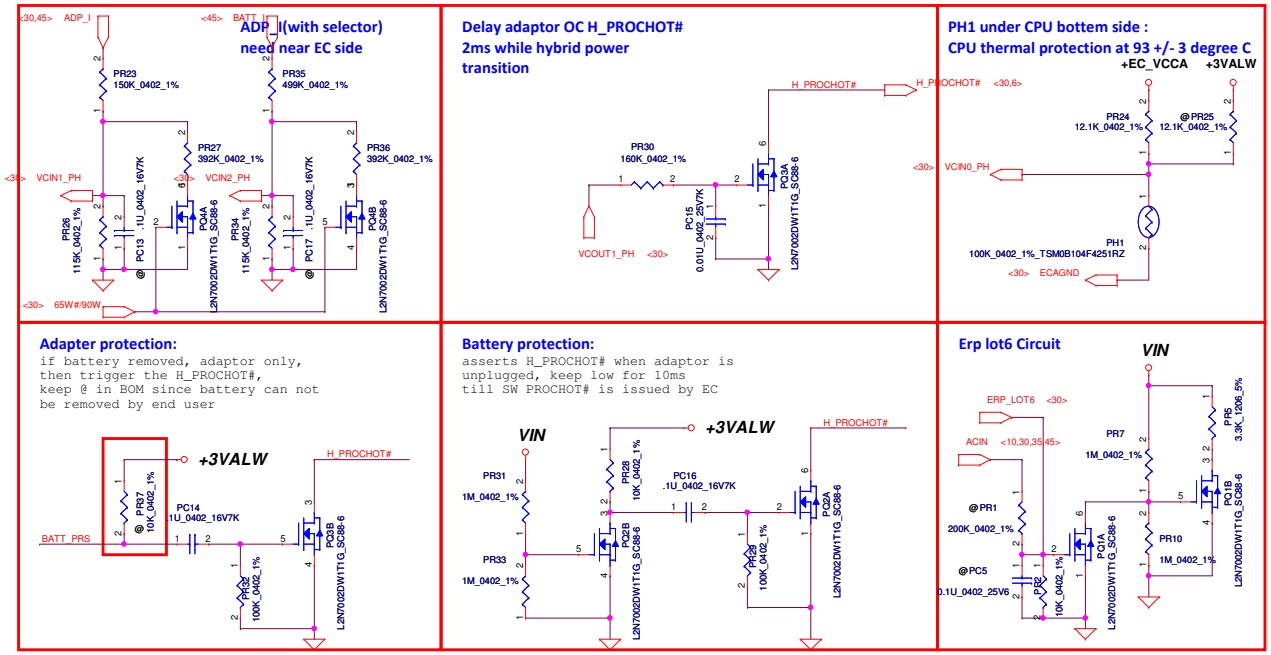
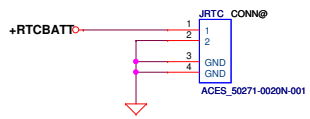


Other component (37.1)





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Compal Electronics, Inc.

Title: PWR_DCIN/BATT CONN/OTP

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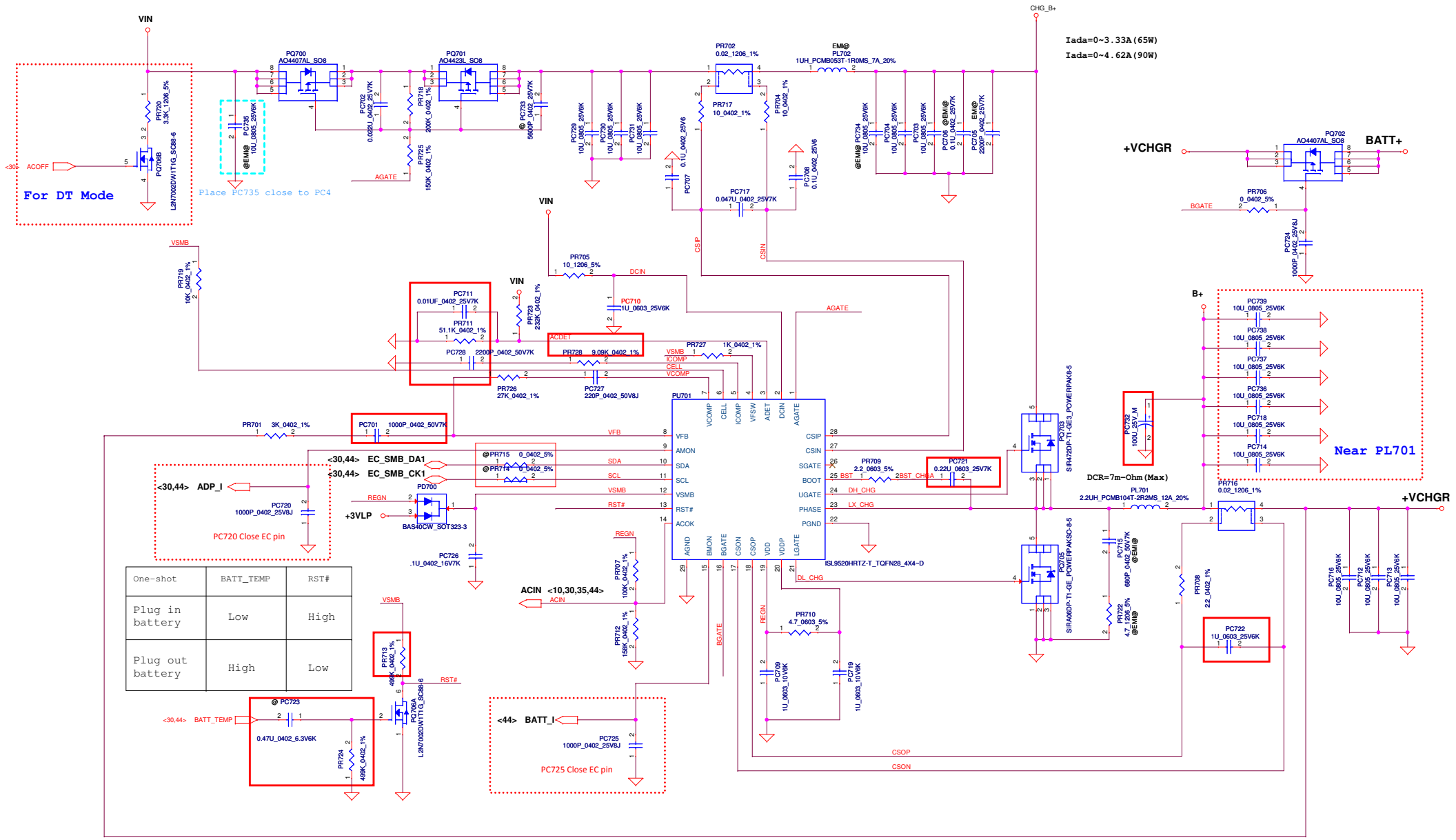

One-shot	BATT_TEMP	RST#
Plug in battery	Low	High
Plug out battery	High	Low

2S2P : CV = 8.4V CC = 3.9A
3S1P : CV = 12.6V CC = 2A

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Issued Date	2014/01/20	Deciphered Date	2015/01/19

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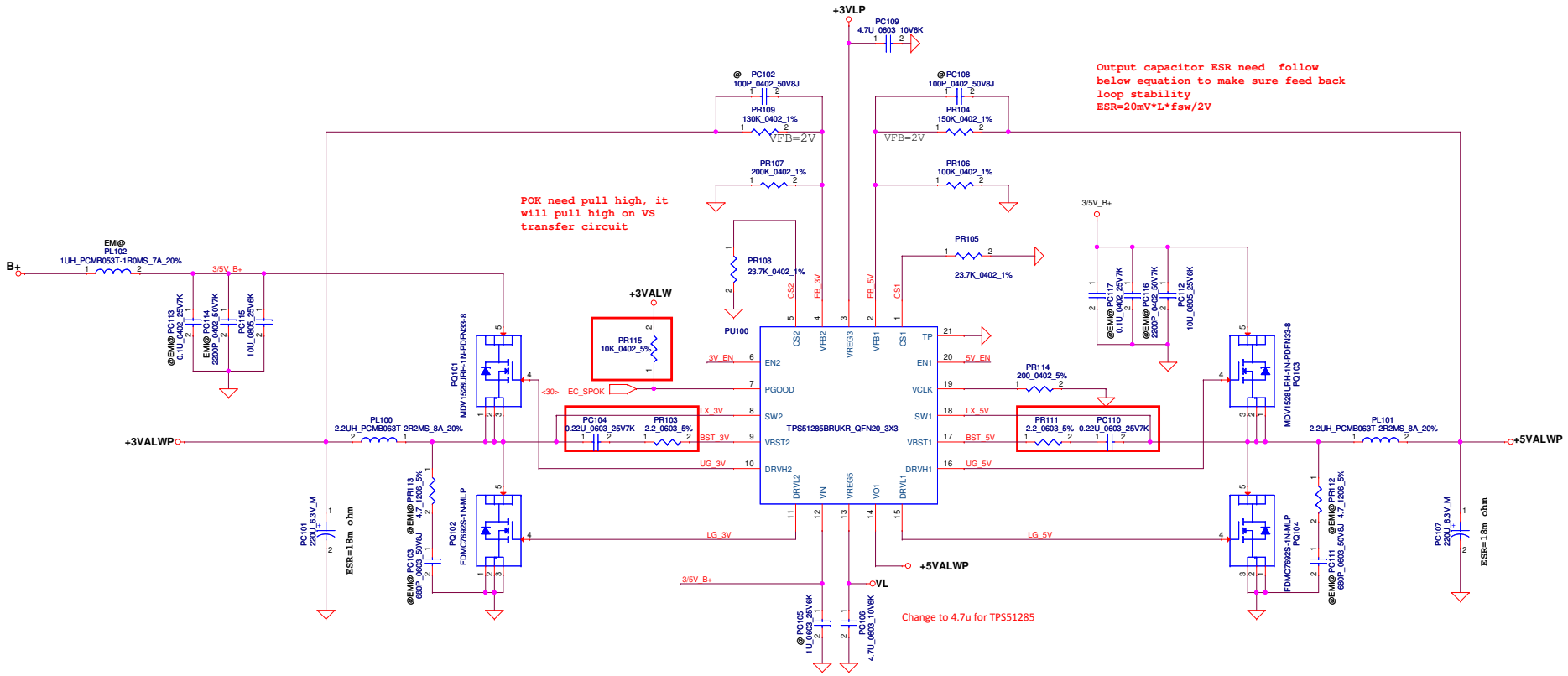
Compal Electronics, Inc.

Title: PWR_CHARGER

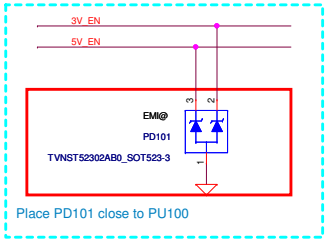
Size | Document Number: LA-B012P | Rev 1.0

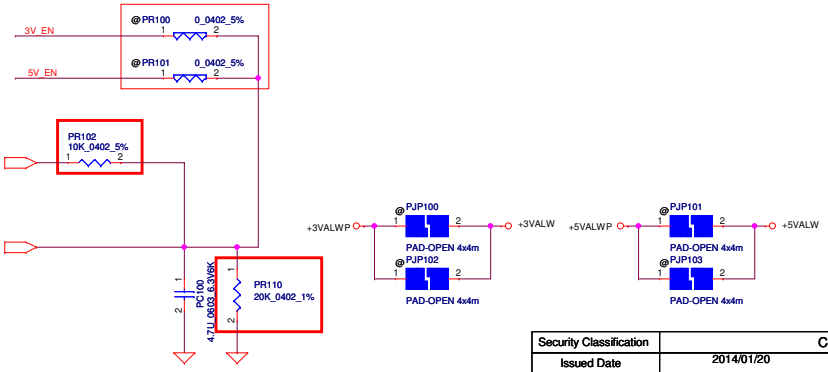
Date: Tuesday, August 05, 2014 | Sheet 45 of 55



3VALWP
TDC 5.95A
Peak Current 8.5A
OCP current 10.2A

	TYP	MAX
H/S Rds(on):	22mohm ,	30mohm
L/S Rds(on):	10.8mohm ,	13.6mohm





5VALWP
TDC 5.96A
Peak Current 8.51A
OCP current 10.2A

	TYP	MAX
H/S Rds(on):	22mohm ,	30mohm
L/S Rds(on):	10.8mohm ,	13.6mohm

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Issued Date	2014/01/20	Deciphered Date	2015/01/19

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Compal Electronics, Inc.

Title: PWR_3.3VALWP/5VALWP

Size | Document Number: LA-B012P | Rev: 1.0

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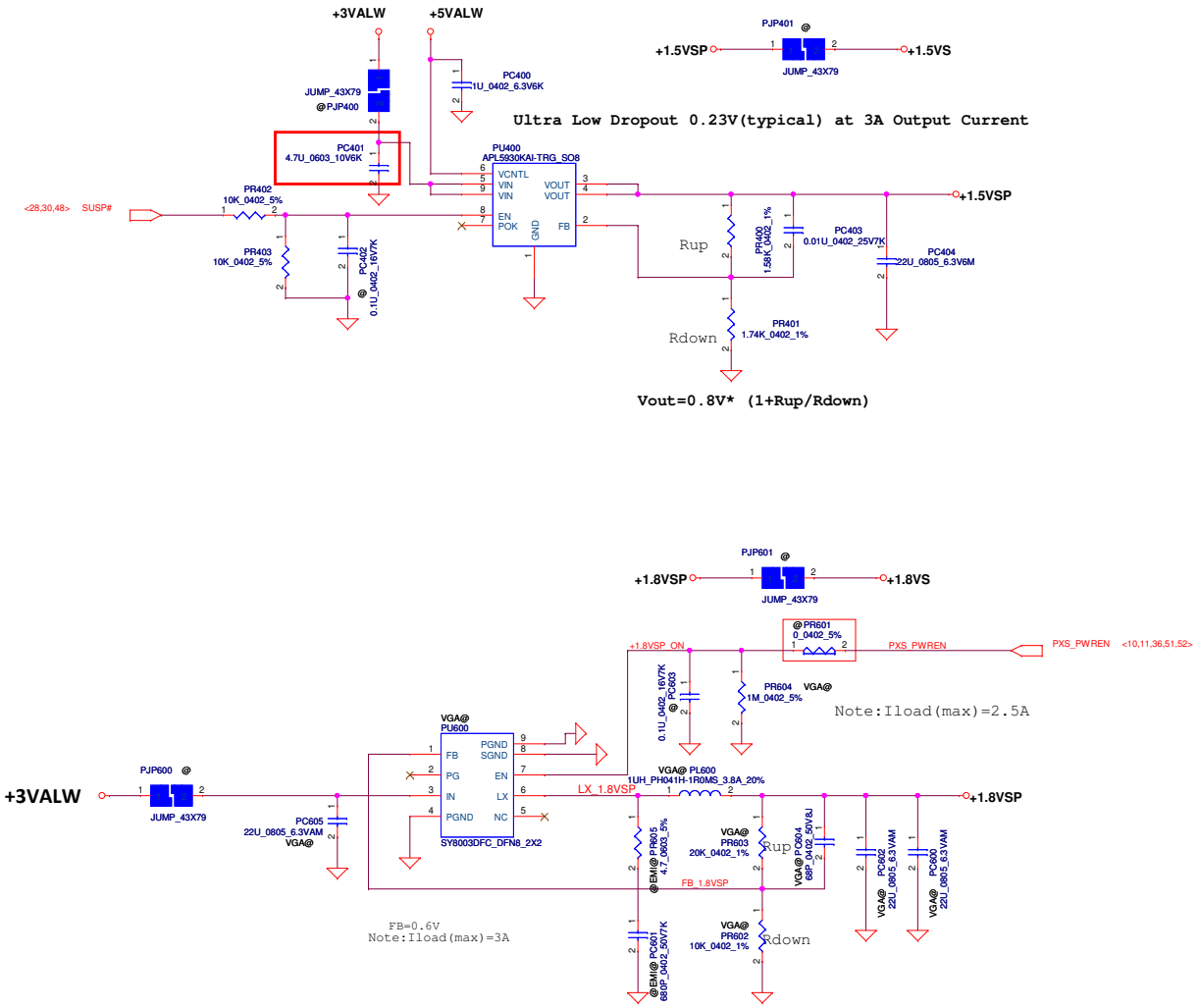

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Compal Electronics, Inc.

Title: **PWR_1.5VSP / 1.8VSP**

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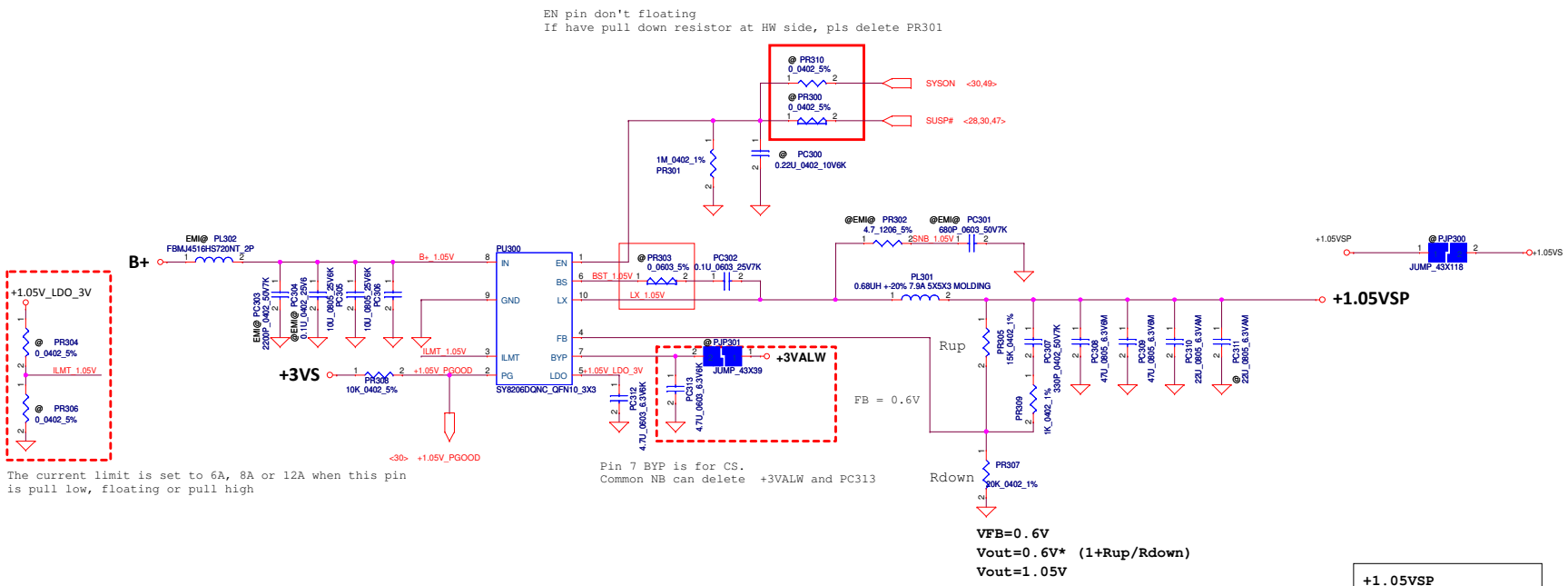

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Issued Date	2014/01/20	Deciphered Date	2015/01/19	Title: PWR_+VCCIO
				Size: C; Document Number: LA-B012P; Rev: 1.0
				Date: Tuesday, August 05, 2014; Sheet 48 of 55

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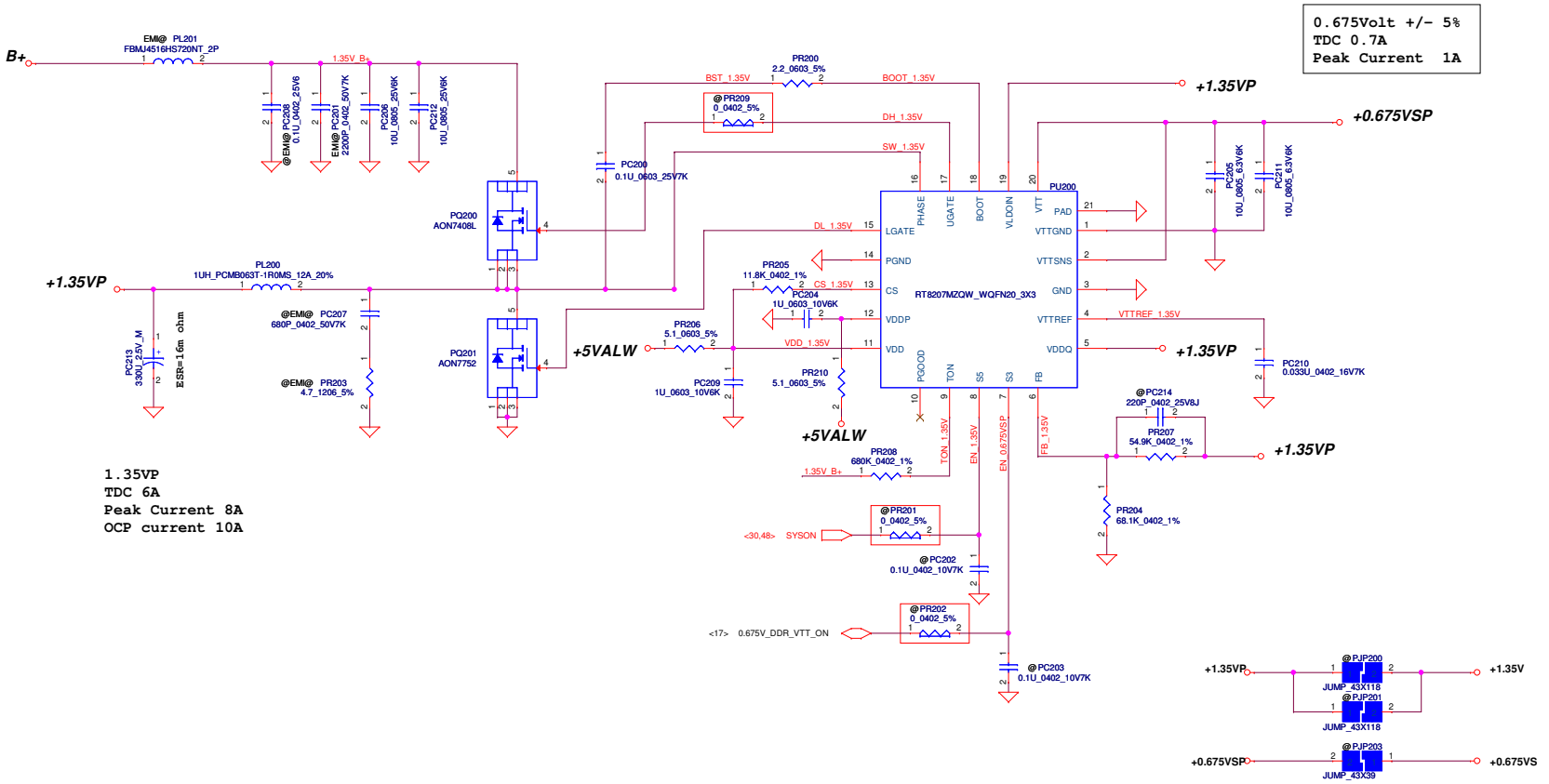

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Compal Electronics, Inc.

Title: **PWR_+1.35VP/0.675VSP**

Size | Document Number: **LA-B012P** | Rev: 1.0

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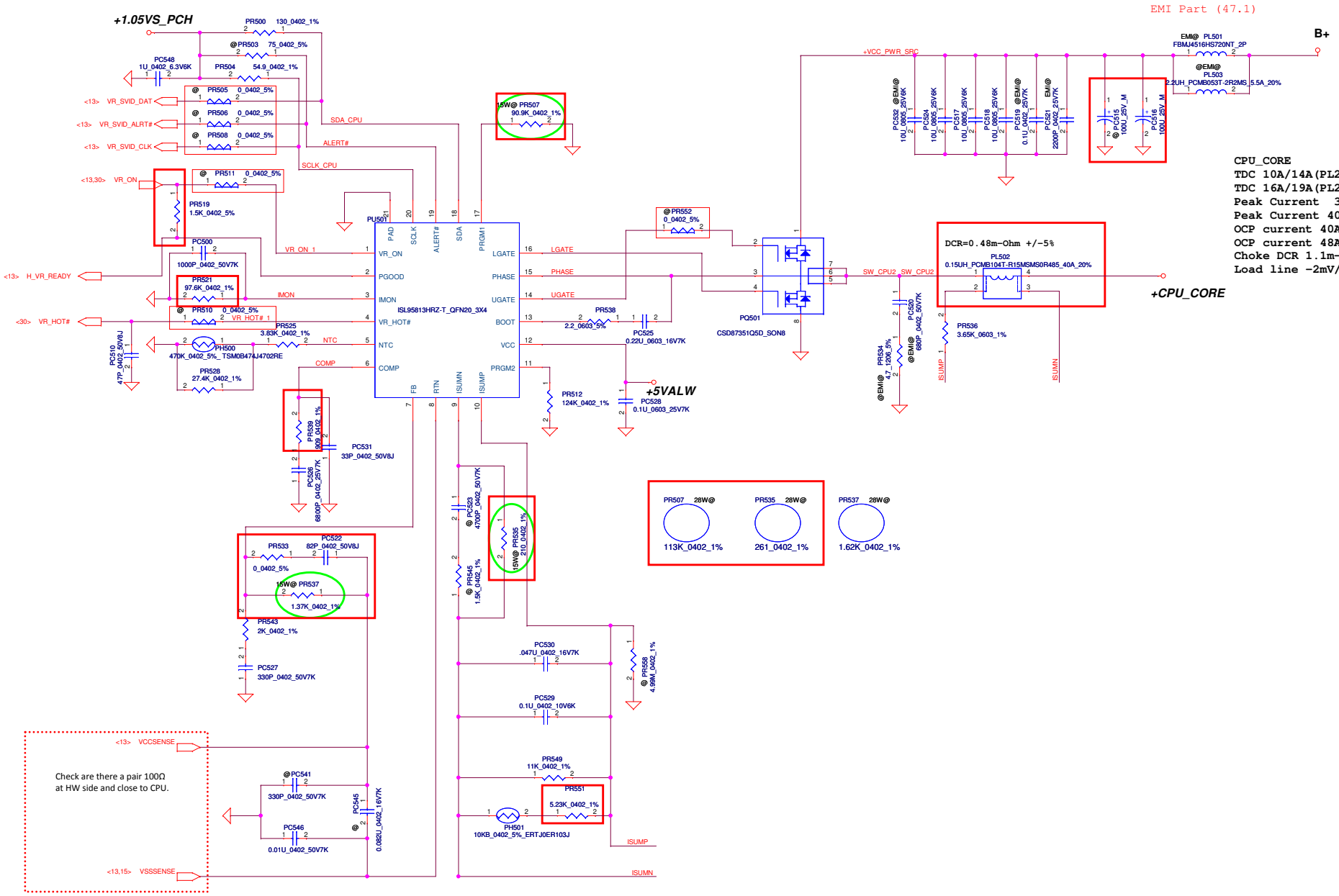

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Compal Electronics, Inc.

Title: **PWR_VCORE**

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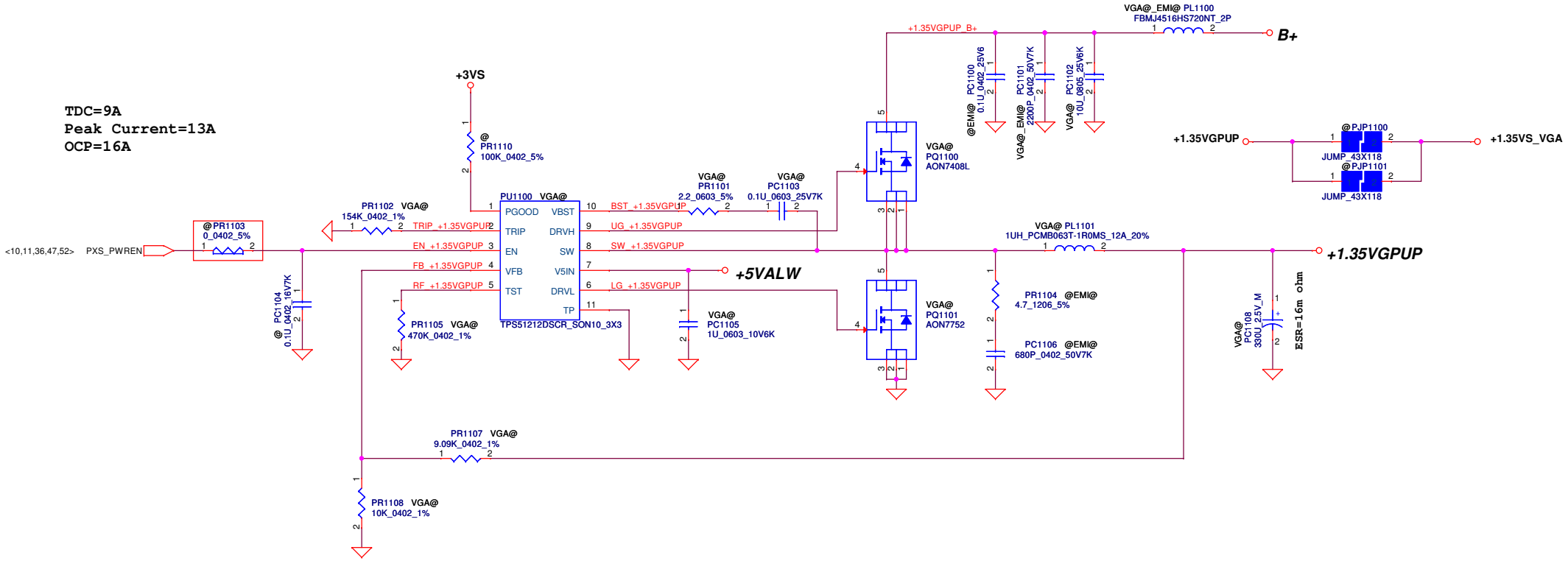

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Issued Date	2014/01/20	Deciphered Date	2015/01/19	Title: PWR_+1.35VGPU
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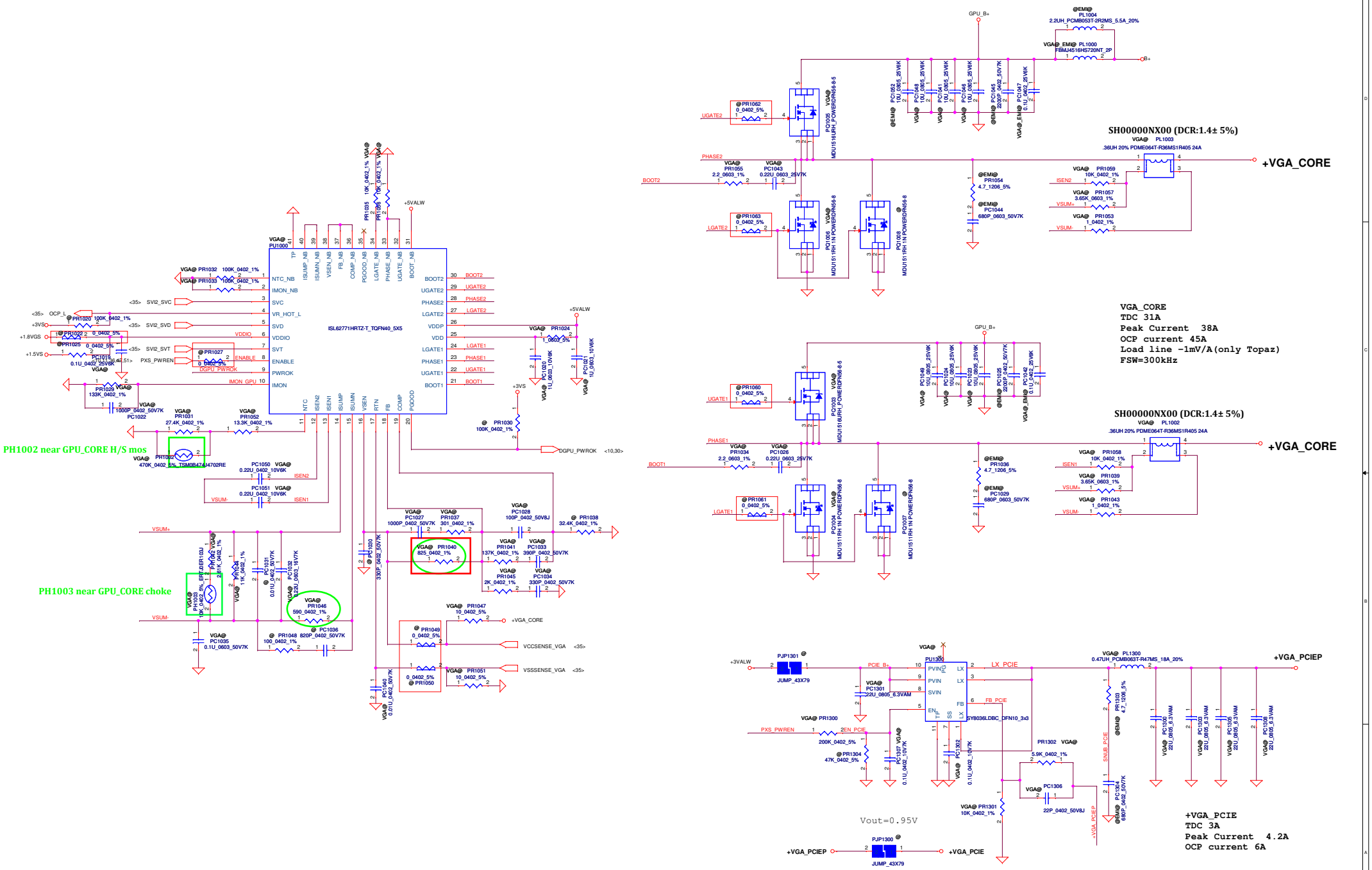

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Compal Electronics, Inc.

Title: *PWR_VGA_CORE/PCIE*

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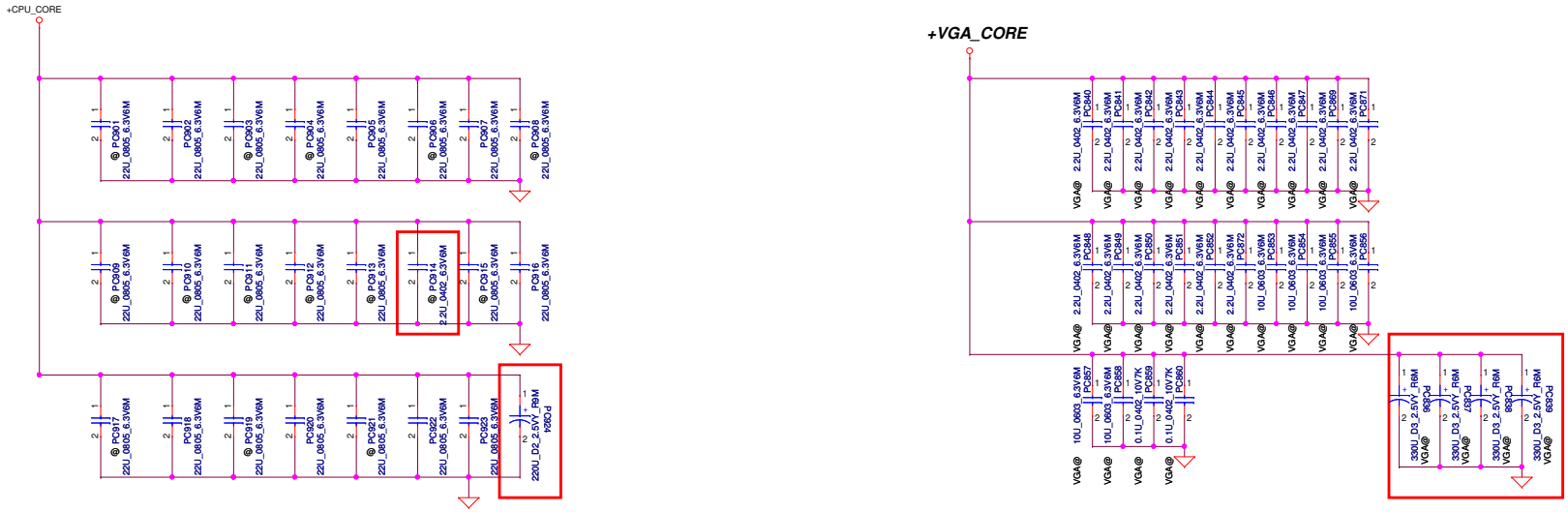

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Compal Electronics, Inc.

Title: **PWR_PROCESSOR DECOUPLING**

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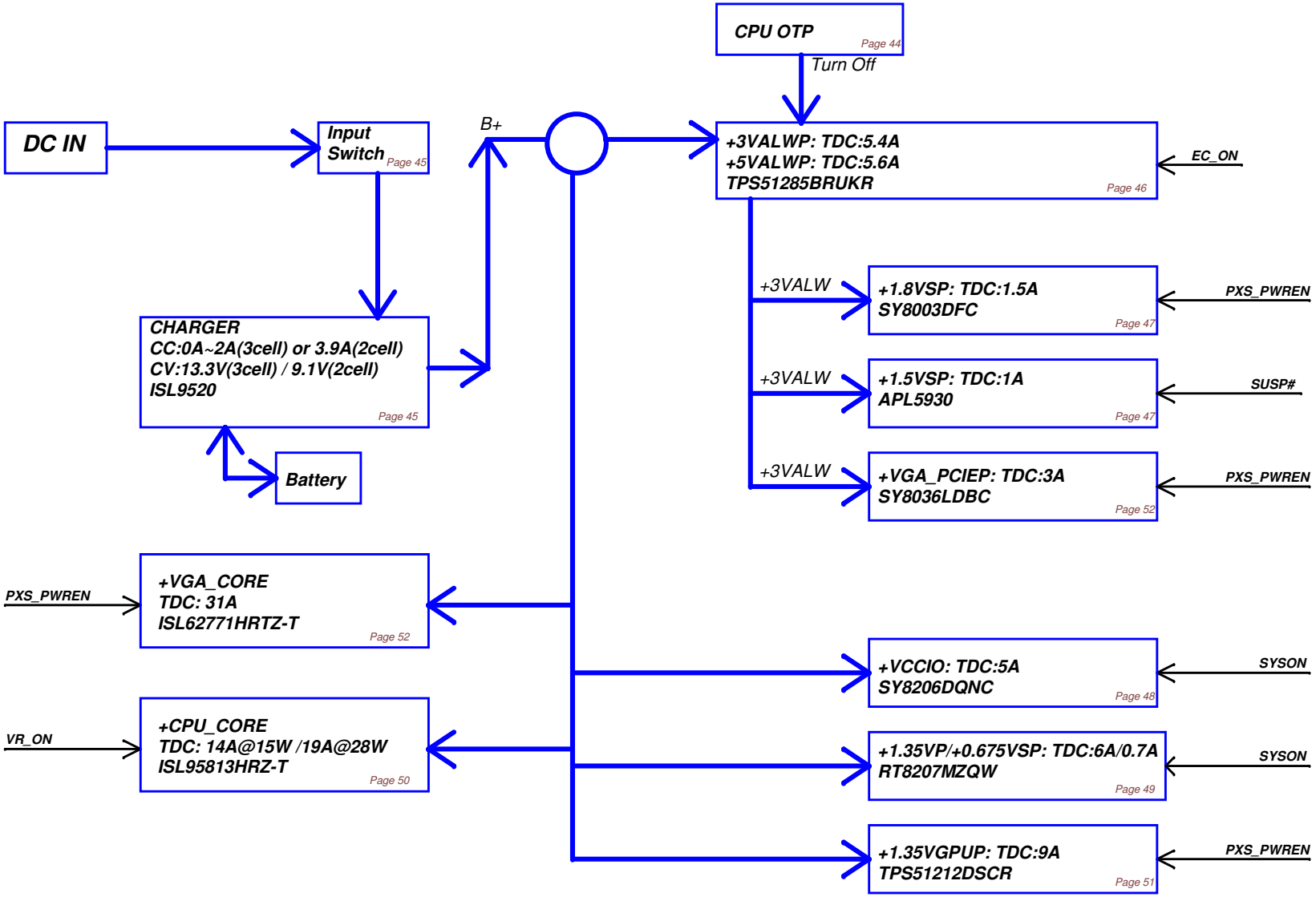
Power block



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Compal Electronics, Inc.

Title: PWR_POWER BLOCK DIAGRAM

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Version Change List (P. I. R. List) Page 1

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	44	DCIN/BATT CONN/OTP	13/10/24	Morris	design change	change PR16 from 100K to 10K add PR37 10K	0.2
2	45	CHARGER	13/10/24	Morris	design change	change PC711 from 1000pF to 0.01uF change PR711 from 49.9K to 51.1K change PR713 from 10K to 499K change PR724 from 100K to 499K change PC721 from 0.047u to 0.22u change PC722 from 0.1u to 1u add PC732 100u	0.2
3	46	3.3VALWP/5VALWP	13/10/24	Morris	design change for solve can't root issue	change PC104 from 0.1u to 0.22u change PC110 from 0.1u to 0.22u change PR102 from 2.2K to 10K add PR110 20K	0.2
4	50	VCORE	13/10/24	Morris	adjust CPU parameter	change PR507(15W@) from 90.9K to 169K change PR519 from 1.91K to 10K change PR521 from 95.3K to 97.6K change PR539 from 8.06K to 909 change PC515,PC516 from SF000005100 to SF000004M00 change PL502 from SH00000NM00 to SH00000PQ00 change PR535(15W@) from 340 to 210 change PR537 from 1.27K to 1.37K change PR535(28W@) from 432 to 261 change PR507(28W@) from 113K to 205K change PR551 from 2.61K to 5.23K add PC522 82pF add PR533 0-ohm	0.2
6	52	VGA_CORE/PCIE	13/10/24	Morris	design change from vendor change LL	change PR1040 from 1.24K to 825	0.2
7	53	PROCESSOR DECOUPLING	13/10/24	Morris	adjust CPU parameter	change PC924 from SGA20331E10 to SGA00009800 remove PC901,PC903,PC904,PC906,PC908,PC909,PC910,PC911,PC912,PC913,PC914,PC915,PC917,PC919,PC921	0.2
8	45	CHARGER	13/10/28	Morris	design change for plug out battery shut down issue	change PC723 from 0.01uF to 0.47uF change PR728 from 0 to 9.09K change PC728 from 4700pF to 2200pF change PC701 from 220pF to 1000pF	0.2
9	46	3.3VALWP/5VALWP	13/12/12	Morris	design change from EE request	add PR115 10K-ohm	0.3
10	50	VCORE	13/12/12	Morris	design change from Intel recommend	change PR519 from 10K to 1.5K	0.3
11	48	+VCCIO	13/12/13	Morris	design change from EE request	delete PR310 and add PR300 0-ohm	0.3
12	50	VCORE	14/01/20	Morris	adjust CPU parameter	change PR507(15W@) from 169K to 90.9K change PR507(28W@) from 205K to 113K	1.0
13	53	PROCESSOR DECOUPLING	14/02/13	Morris	design change from thermal request	change PC836 PC837 PC838 PC839 from SGA20331E10 to SGA00006A00	1.0

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