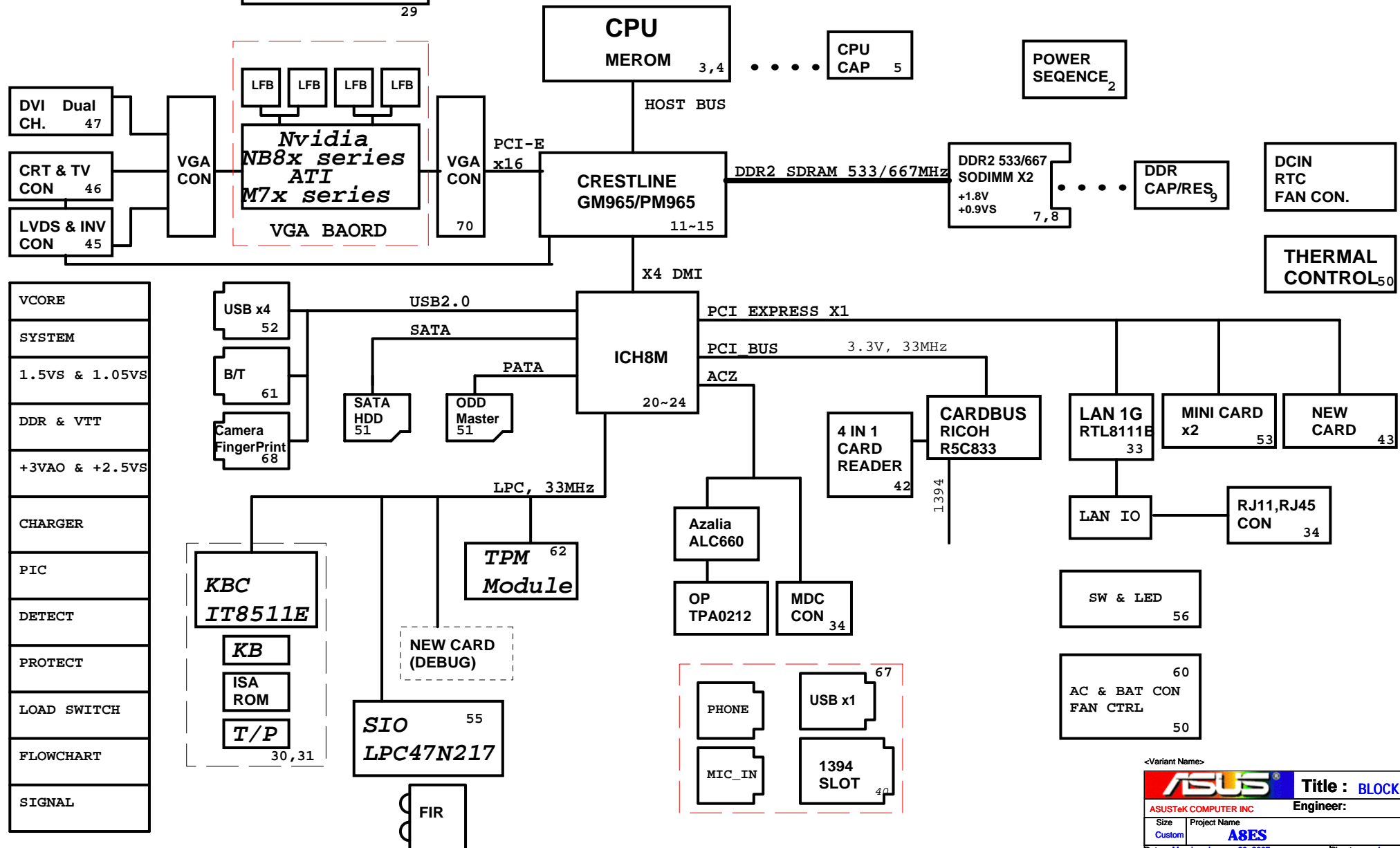
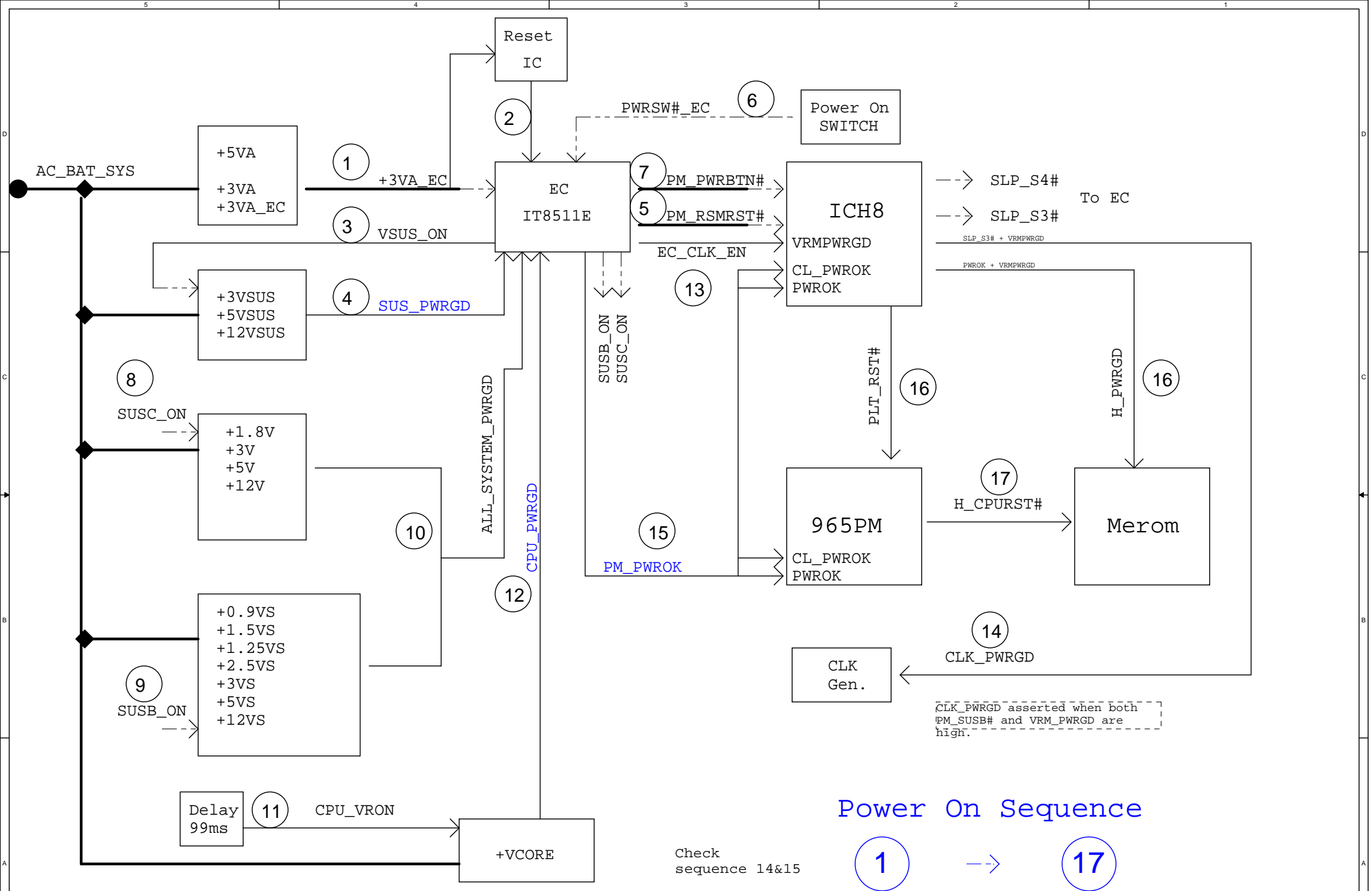
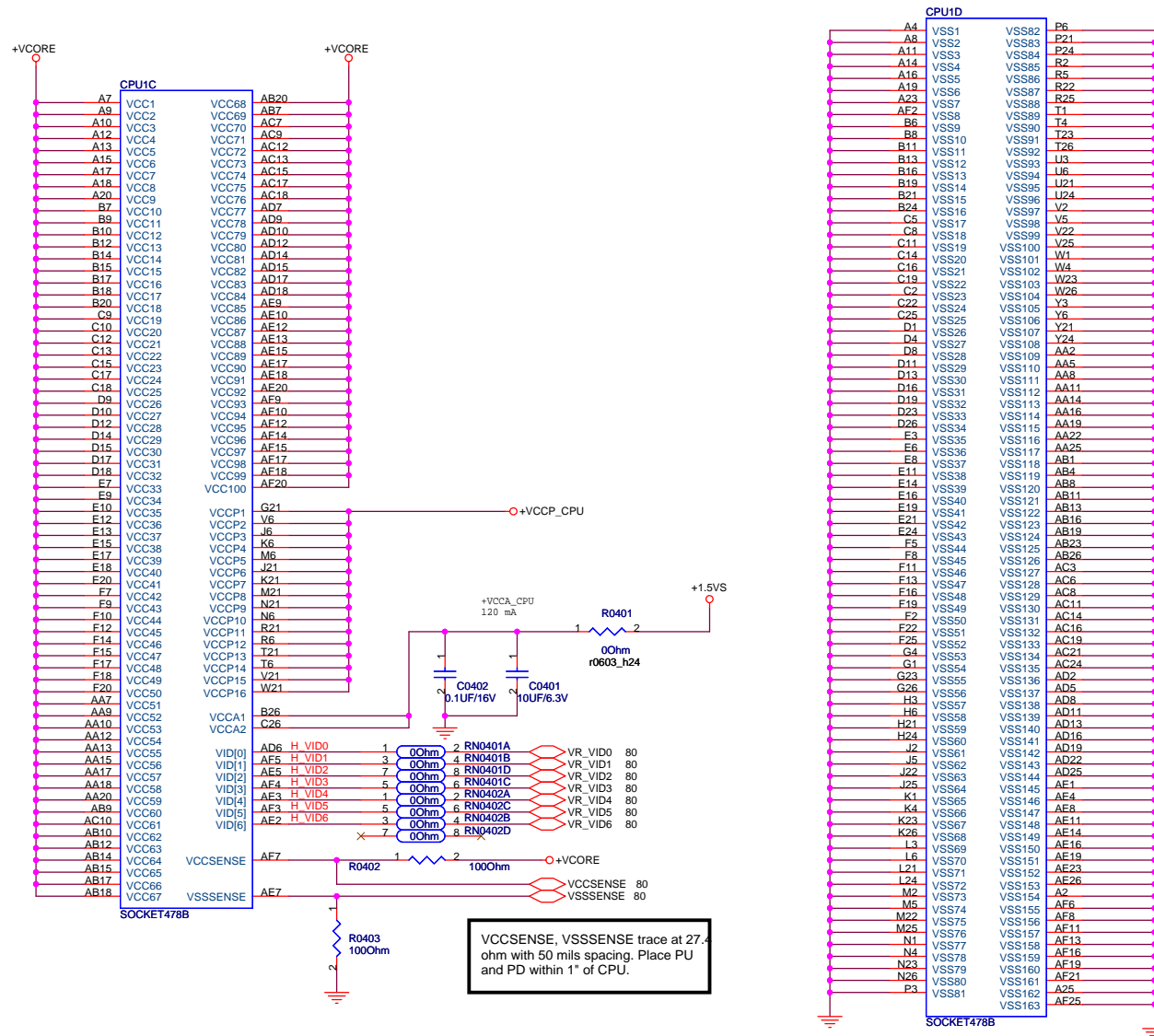
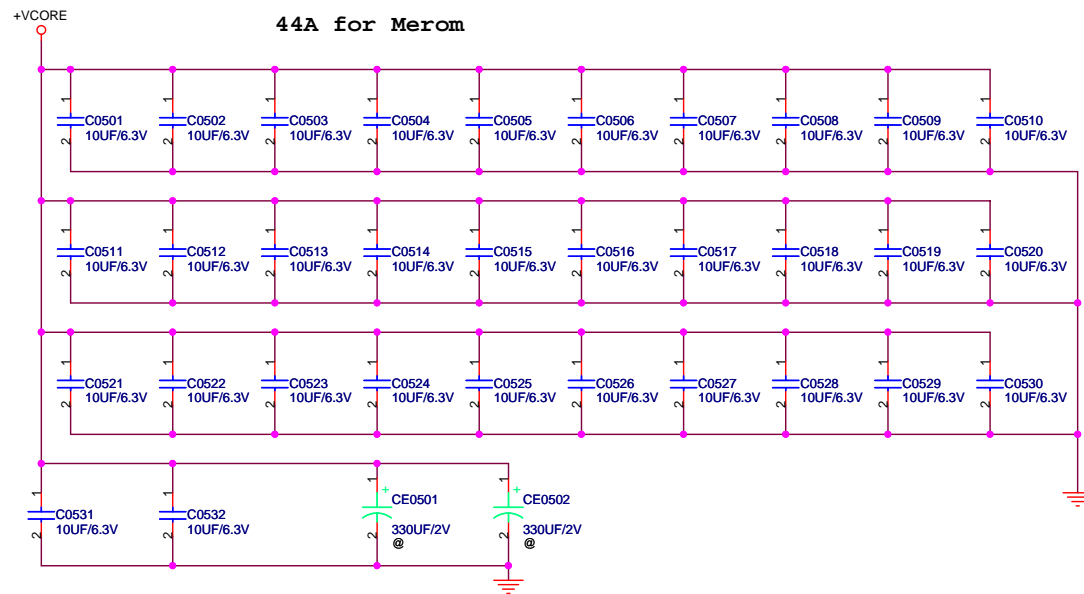


Sub block Diagram /
BOM option







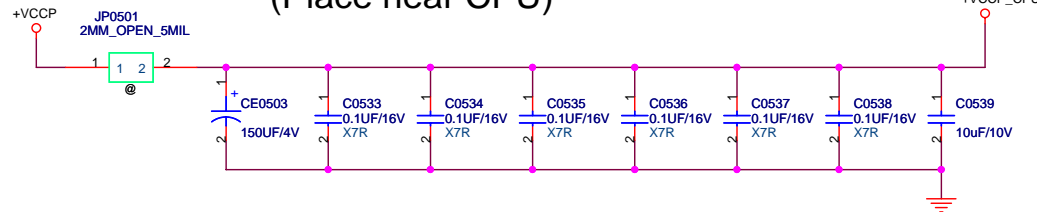


Decoupling guide from INTEL


VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

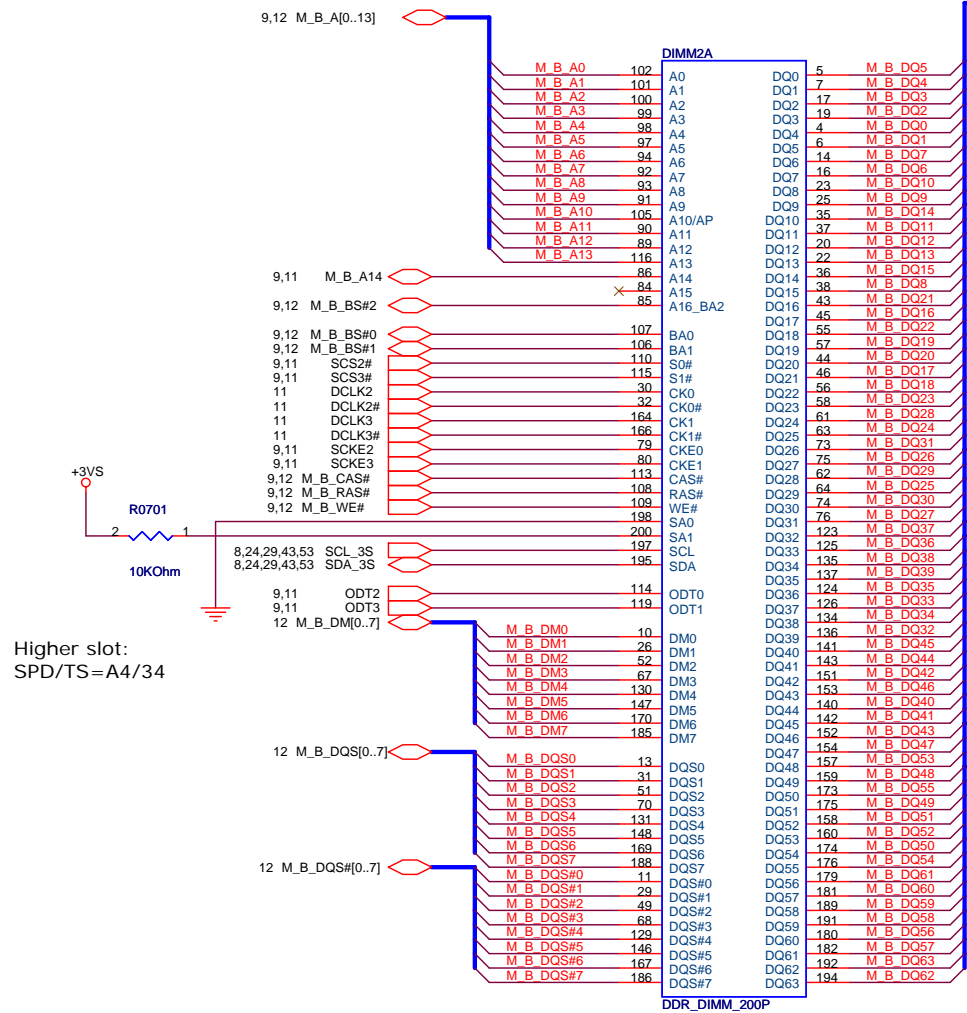
VCORE	10uF/10V	* 32pcs
	330uF/2V	* 0pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU
	10uF/10V	* 1pcs

**+VCCP Decoupling Capacitor
(Place near CPU)**

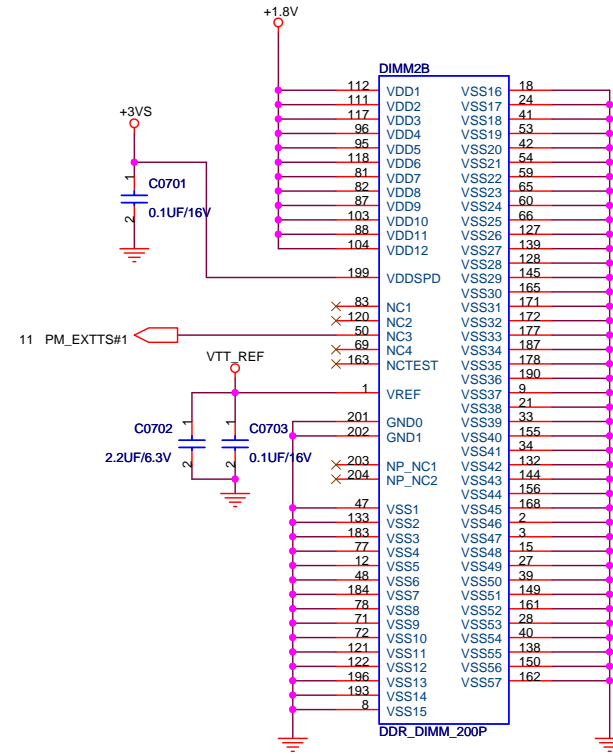


5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

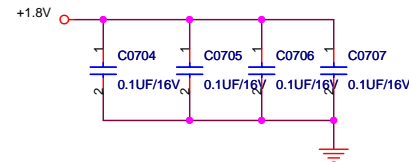
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ASUSTeK COMPUTER INC		Engineer:	
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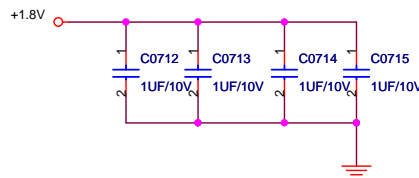
M_B_DQ[0..63] 12



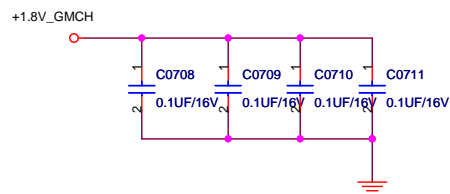
Layout Note: Place these Caps near SO DIMM 0



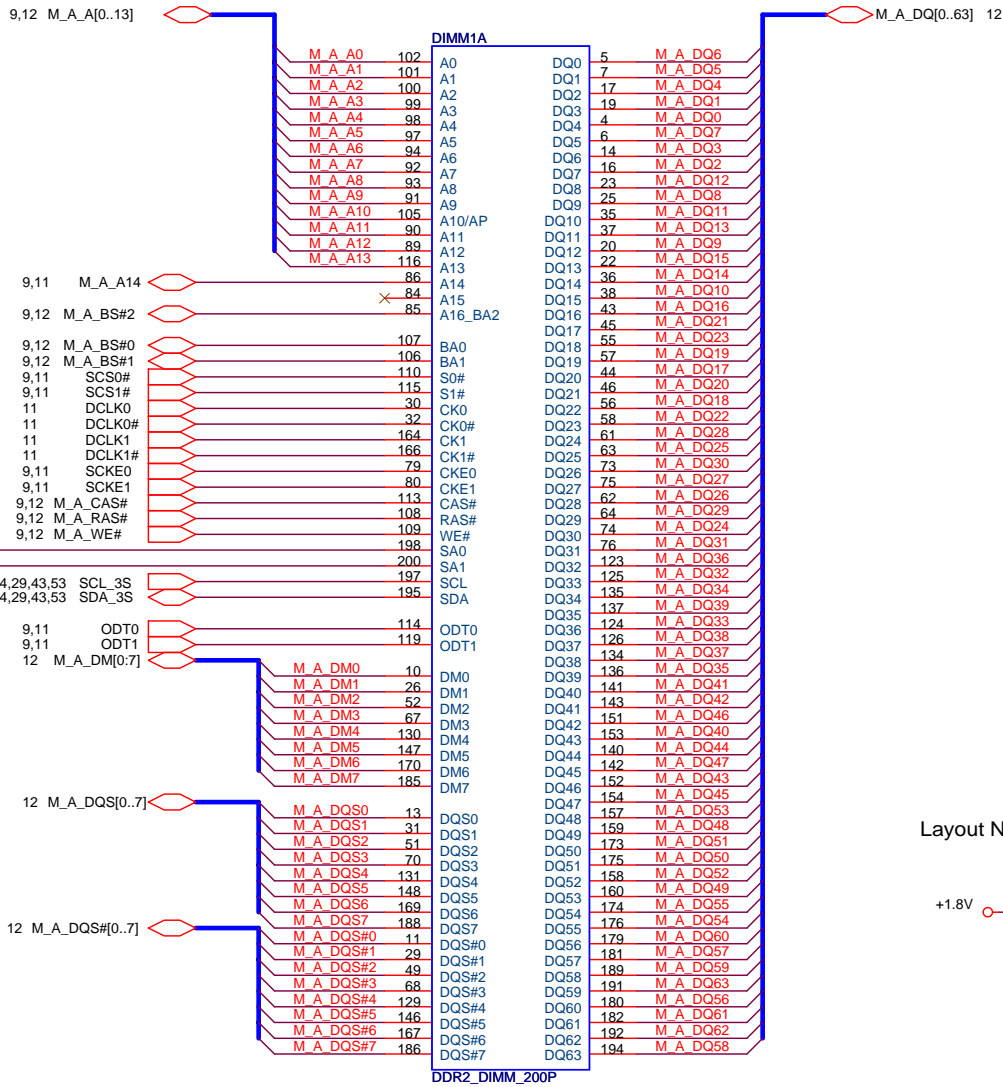
Layout Note: Place these Caps near SO DIMM 0



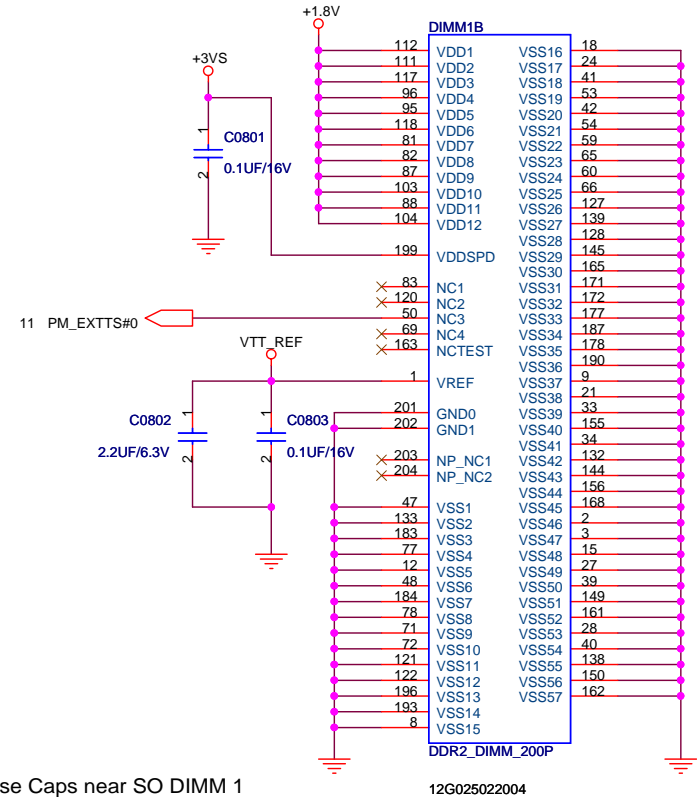
Layout Note: Place these High-Freq decoupling Caps near the GMCH



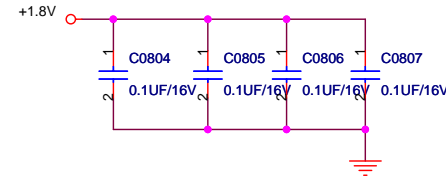
Upper:Channel B



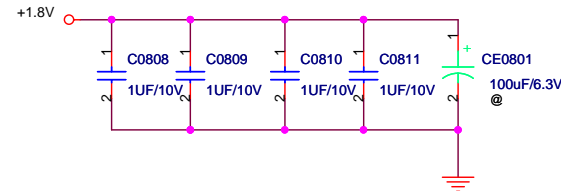
Lower slot:
SPD/TS=A0/30



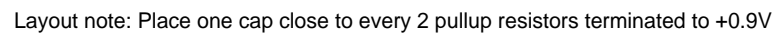
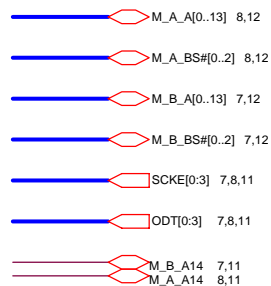
Layout Note: Place these Caps near SO DIMM 1

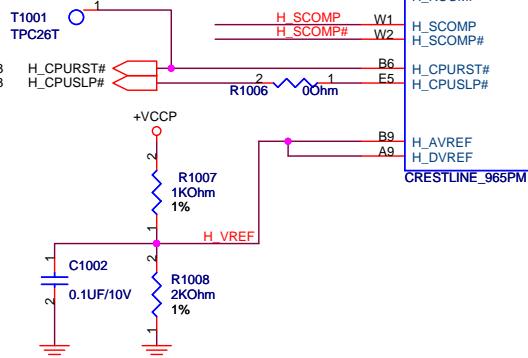
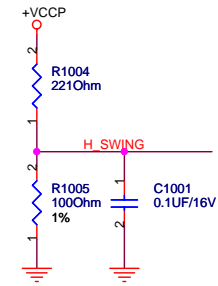
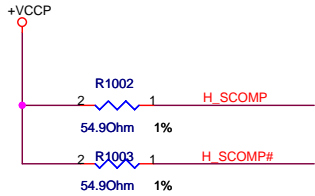
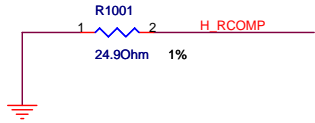


Layout Note: Place these Caps near SO DIMM 1



Lower:Channel A





H_D#0	E2	H_D#_0
H_D#1	G2	H_D#_1
H_D#2	G2	H_D#_2
H_D#3	M6	H_D#_3
H_D#4	H7	H_D#_4
H_D#5	H3	H_D#_5
H_D#6	G4	H_D#_6
H_D#7	F3	H_D#_7
H_D#8	N8	H_D#_8
H_D#9	H2	H_D#_9
H_D#10	M10	H_D#_10
H_D#11	N12	H_D#_11
H_D#12	N9	H_D#_12
H_D#13	H5	H_D#_13
H_D#14	P13	H_D#_14
H_D#15	K9	H_D#_15
H_D#16	M2	H_D#_16
H_D#17	W10	H_D#_17
H_D#18	Y8	H_D#_18
H_D#19	V4	H_D#_19
H_D#20	M3	H_D#_20
H_D#21	J1	H_D#_21
H_D#22	N5	H_D#_22
H_D#23	N3	H_D#_23
H_D#24	W6	H_D#_24
H_D#25	W9	H_D#_25
H_D#26	N2	H_D#_26
H_D#27	Y7	H_D#_27
H_D#28	Y9	H_D#_28
H_D#29	P4	H_D#_29
H_D#30	W3	H_D#_30
H_D#31	N1	H_D#_31
H_D#32	AD12	H_D#_32
H_D#33	AE3	H_D#_33
H_D#34	AD9	H_D#_34
H_D#35	AC9	H_D#_35
H_D#36	AC7	H_D#_36
H_D#37	AC14	H_D#_37
H_D#38	AD11	H_D#_38
H_D#39	AC11	H_D#_39
H_D#40	AB2	H_D#_40
H_D#41	AD7	H_D#_41
H_D#42	AB1	H_D#_42
H_D#43	Y3	H_D#_43
H_D#44	AC6	H_D#_44
H_D#45	AE2	H_D#_45
H_D#46	AC5	H_D#_46
H_D#47	AG3	H_D#_47
H_D#48	AJ9	H_D#_48
H_D#49	AH8	H_D#_49
H_D#50	AJ14	H_D#_50
H_D#51	AE9	H_D#_51
H_D#52	AE11	H_D#_52
H_D#53	AH12	H_D#_53
H_D#54	AJ5	H_D#_54
H_D#55	AH5	H_D#_55
H_D#56	AJ6	H_D#_56
H_D#57	AE7	H_D#_57
H_D#58	AJ7	H_D#_58
H_D#59	AJ2	H_D#_59
H_D#60	AE5	H_D#_60
H_D#61	AJ3	H_D#_61
H_D#62	AH2	H_D#_62
H_D#63	AH13	H_D#_63

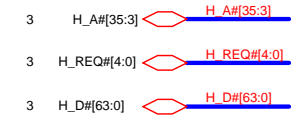
H_SWING	B3	H_SWING
H_RCOMP	C2	H_RCOMP
H_SCOMP	W1	H_SCOMP
H_SCOMP#	W2	H_SCOMP#
H_CPURST#	B6	H_CPURST#
H_CPUSLP#	E5	H_CPUSLP#

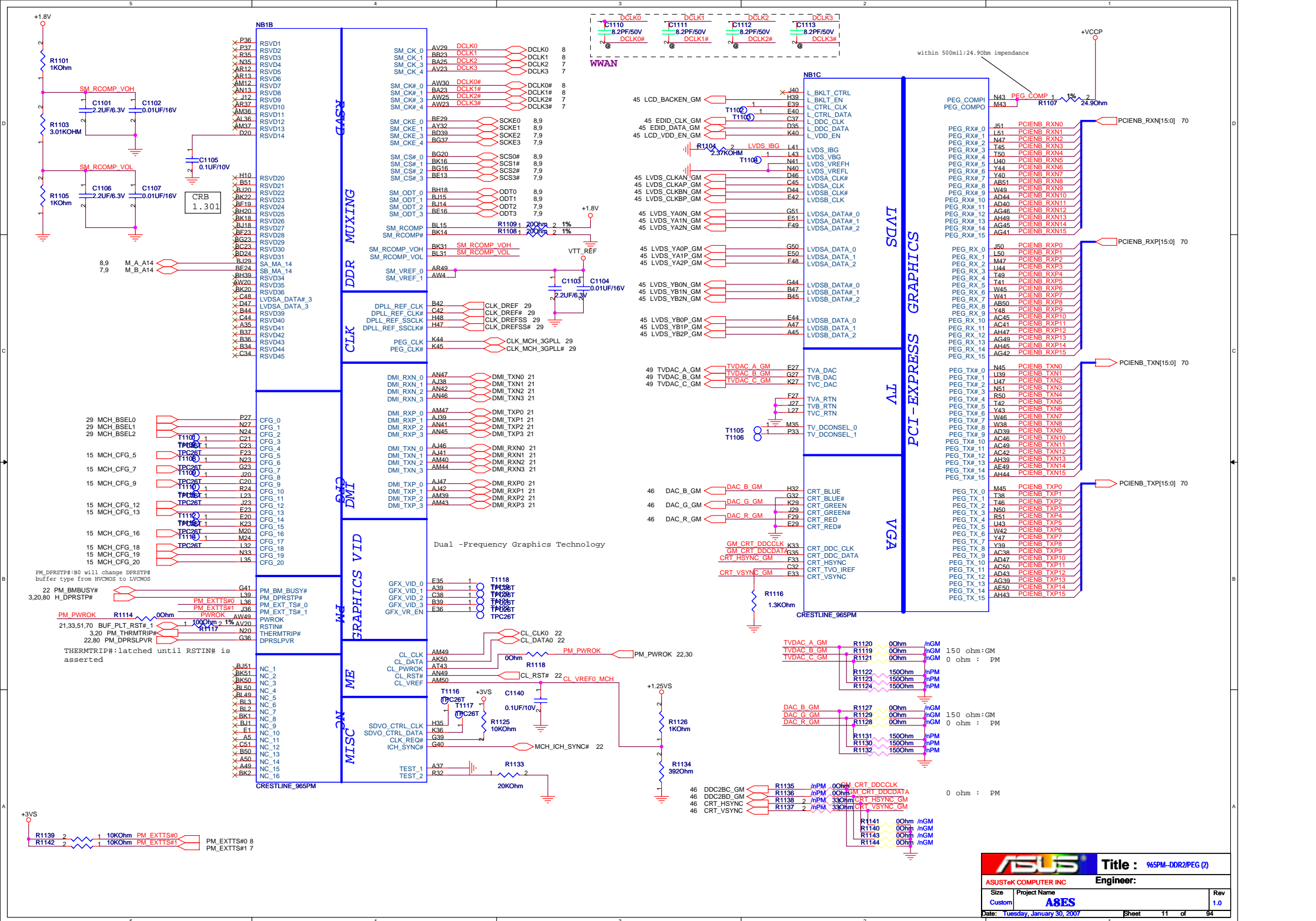
H_AVREF	B9	H_AVREF
H_DVREF	A9	H_DVREF

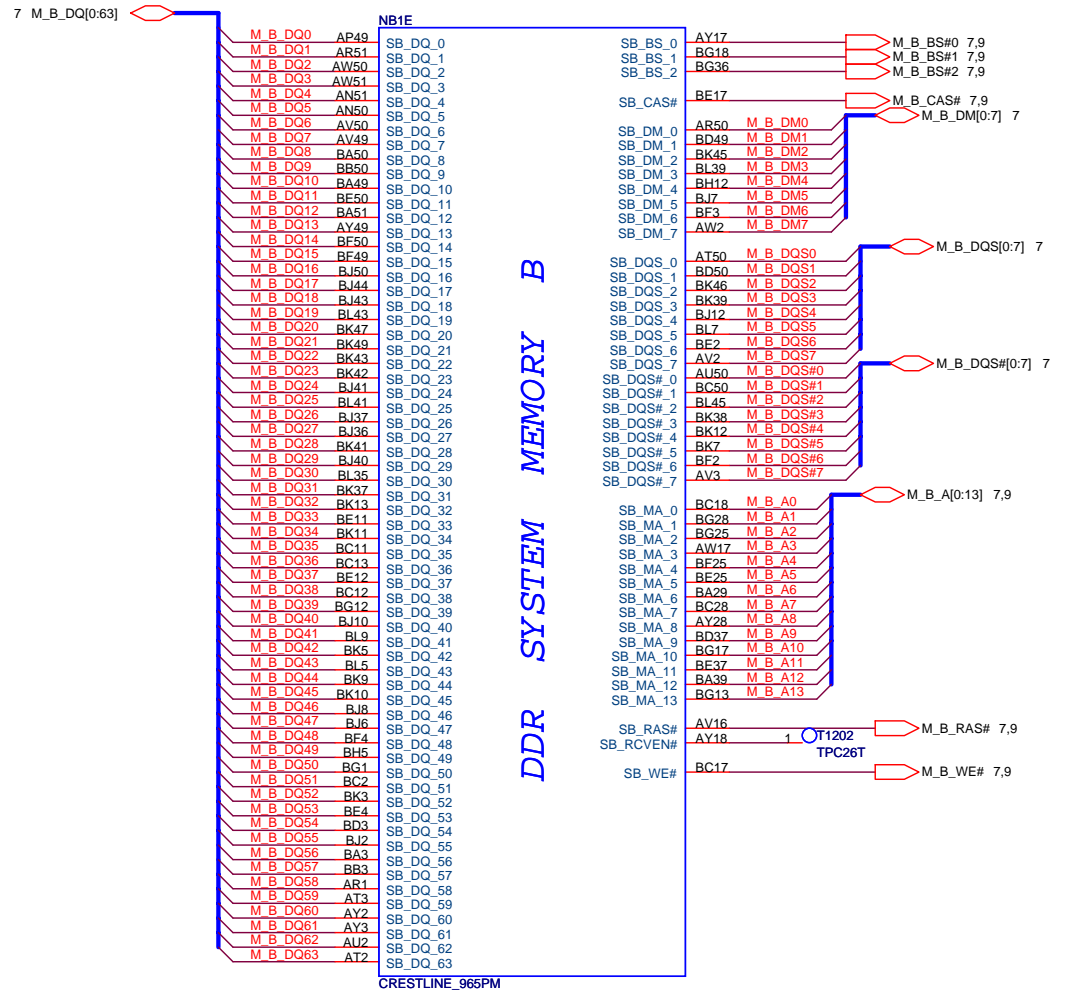
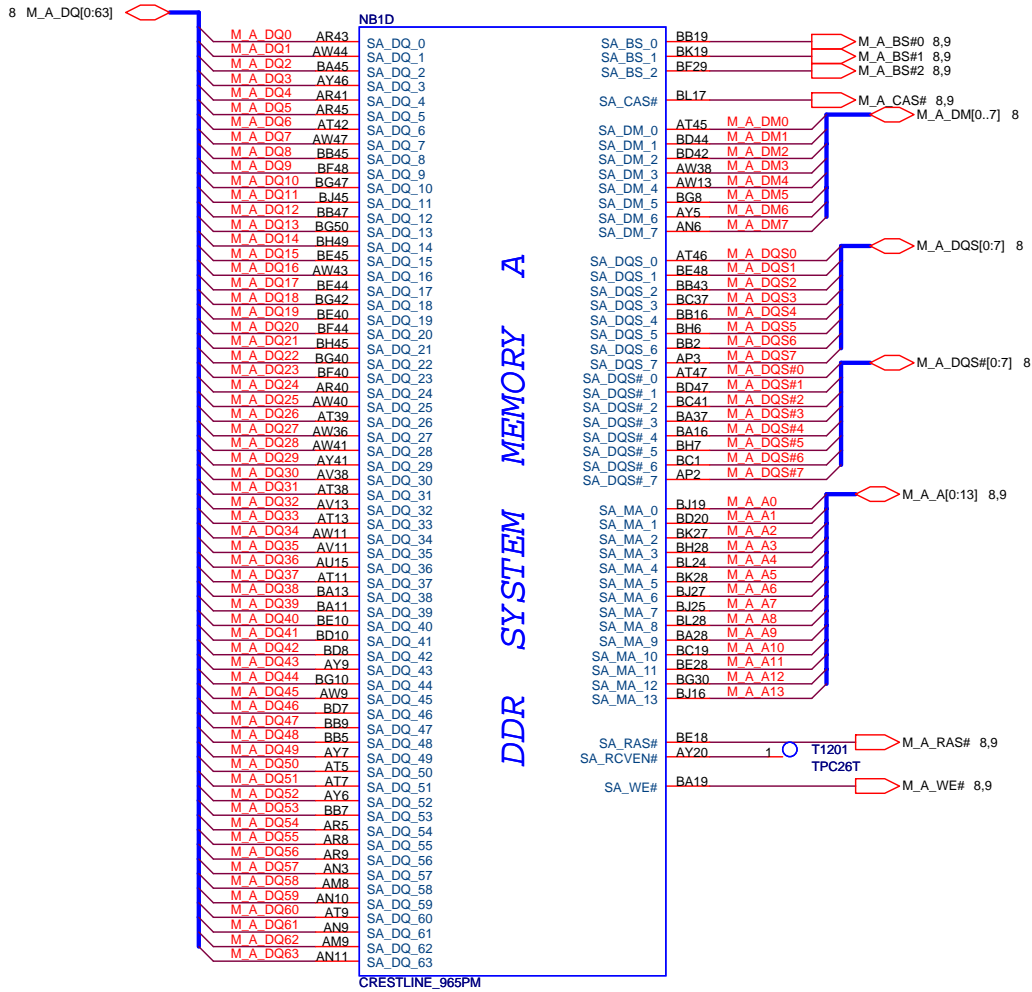
NB1A

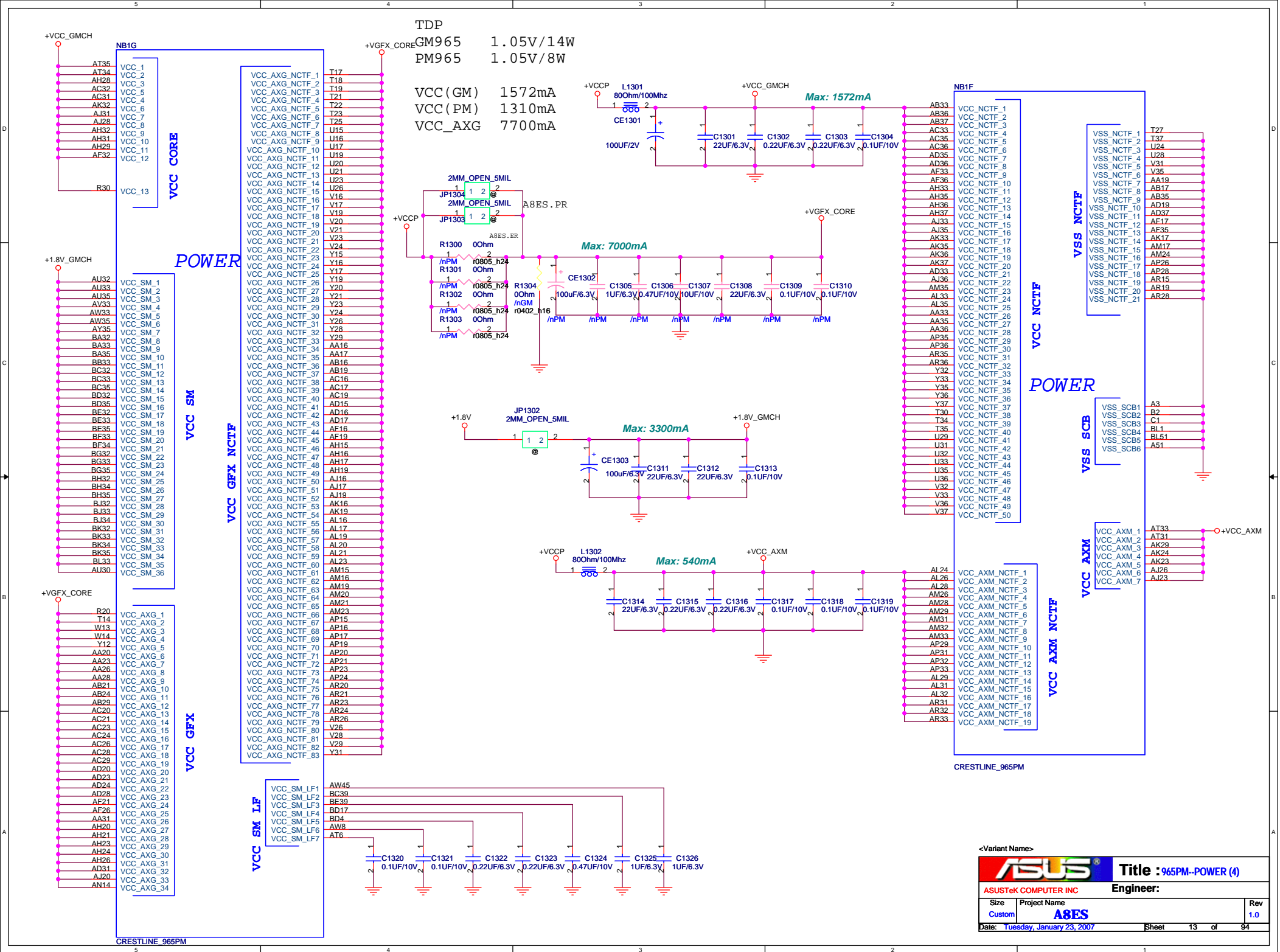
HOST

H_A#_3	J13	H_A#3
H_A#_4	B11	H_A#4
H_A#_5	C11	H_A#5
H_A#_6	M11	H_A#6
H_A#_7	C15	H_A#7
H_A#_8	F16	H_A#8
H_A#_9	L13	H_A#9
H_A#_10	G17	H_A#10
H_A#_11	C14	H_A#11
H_A#_12	K16	H_A#12
H_A#_13	B13	H_A#13
H_A#_14	L16	H_A#14
H_A#_15	J17	H_A#15
H_A#_16	B14	H_A#16
H_A#_17	K19	H_A#17
H_A#_18	P15	H_A#18
H_A#_19	R17	H_A#19
H_A#_20	B16	H_A#20
H_A#_21	H20	H_A#21
H_A#_22	L19	H_A#22
H_A#_23	D17	H_A#23
H_A#_24	M17	H_A#24
H_A#_25	N16	H_A#25
H_A#_26	J19	H_A#26
H_A#_27	B18	H_A#27
H_A#_28	E19	H_A#28
H_A#_29	B17	H_A#29
H_A#_30	B15	H_A#30
H_A#_31	E17	H_A#31
H_A#_32	C18	H_A#32
H_A#_33	A19	H_A#33
H_A#_34	B19	H_A#34
H_A#_35	N19	H_A#35
H_ADS#	G12	H_ADS#
H_ADSTB#_0	H17	H_ADSTB#0
H_ADSTB#_1	G20	H_ADSTB#1
H_BNR#	C8	H_BNR#
H_BPR#	E8	H_BPR#
H_BREQ#	F12	H_BREQ#
H_DEFER#	D6	H_DEFER#
H_DBSY#	C10	H_DBSY#
HPLL_CLK	AM5	CLK_MCH_BCLK# 29
HPLL_CLK#	AM7	CLK_MCH_BCLK# 29
H_DPWR#	H8	H_DPWR#
H_DRDY#	K7	H_DRDY#
H_HIT#	E4	H_HIT#
H_HITM#	C6	H_HITM#
H_LOCK#	G10	H_LOCK#
H_TRDY#	B7	H_TRDY#
H_DINV#_0	K5	H_DINV#0
H_DINV#_1	L2	H_DINV#1
H_DINV#_2	AD13	H_DINV#2
H_DINV#_3	AE13	H_DINV#3
H_DSTBN#_0	M7	H_DSTBN#0
H_DSTBN#_1	K3	H_DSTBN#1
H_DSTBN#_2	AD2	H_DSTBN#2
H_DSTBN#_3	AH11	H_DSTBN#3
H_DSTBP#_0	L7	H_DSTBP#0
H_DSTBP#_1	K2	H_DSTBP#1
H_DSTBP#_2	AC2	H_DSTBP#2
H_DSTBP#_3	AJ10	H_DSTBP#3
H_REQ#_0	M14	H_REQ#0
H_REQ#_1	E13	H_REQ#1
H_REQ#_2	A11	H_REQ#2
H_REQ#_3	H13	H_REQ#3
H_REQ#_4	B12	H_REQ#4
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H_RS#_1	D7	H_RS#1
H_RS#_2	D8	H_RS#2



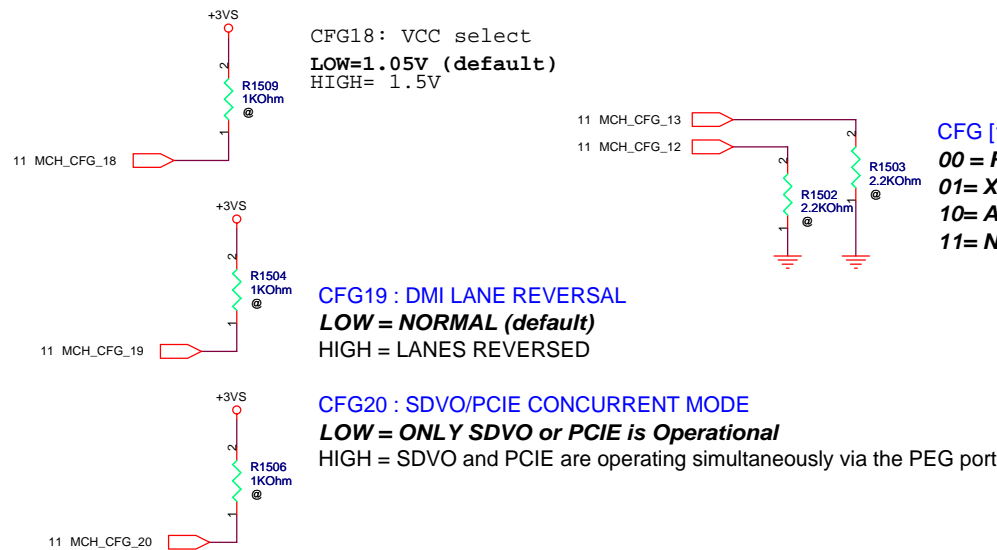
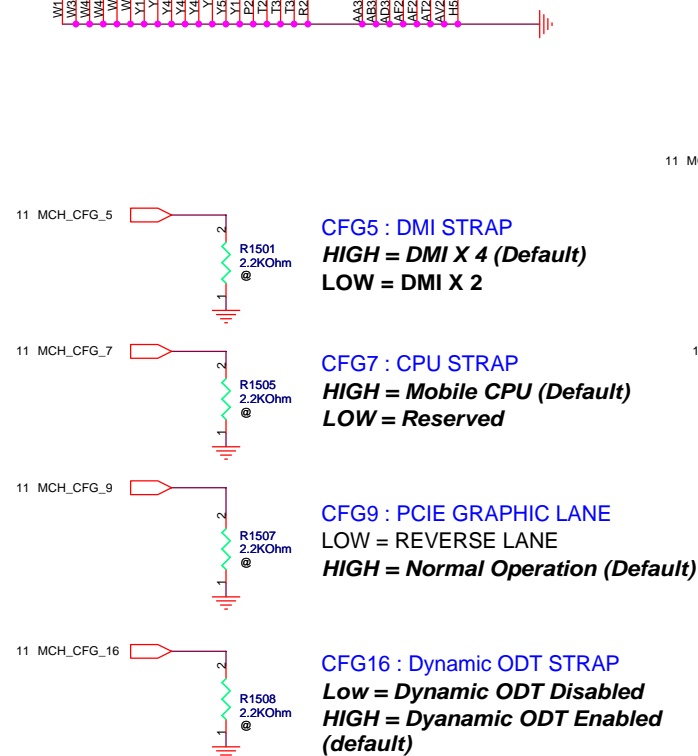






<Variant Name>

ASUS		Title : 965PM-POWER (4)	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
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Date: Tuesday, January 23, 2007	Sheet	13	of 94




CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)

5	4	3	2	1
D				D
C				C
B				B
A				A

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: Wednesday, October 11, 2006		Sheet 16 of 94	

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C				C
B				B
A				A

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ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	A8ES		0
Date: Wednesday, October 11, 2006		Sheet 17 of 94	

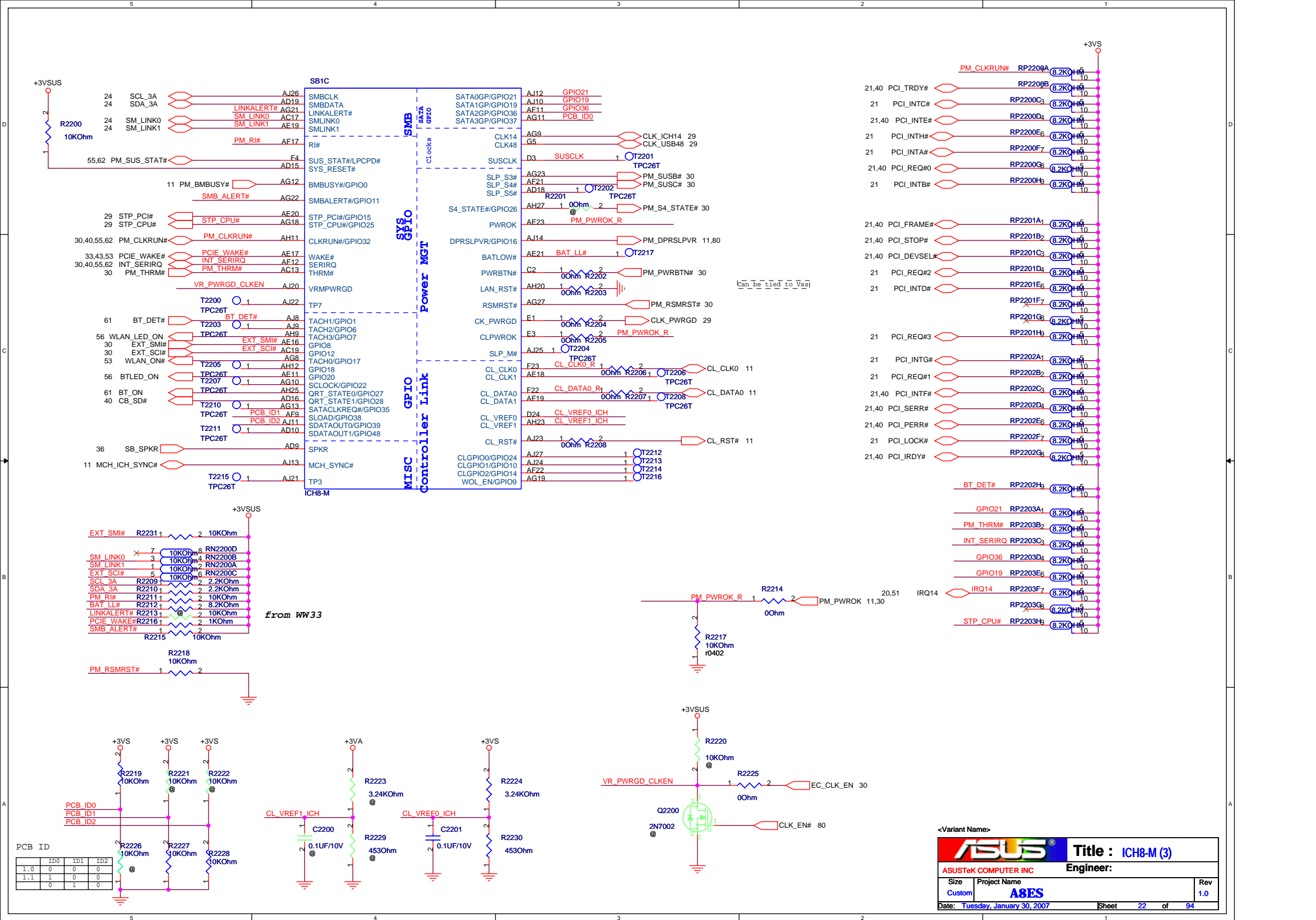
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A				A

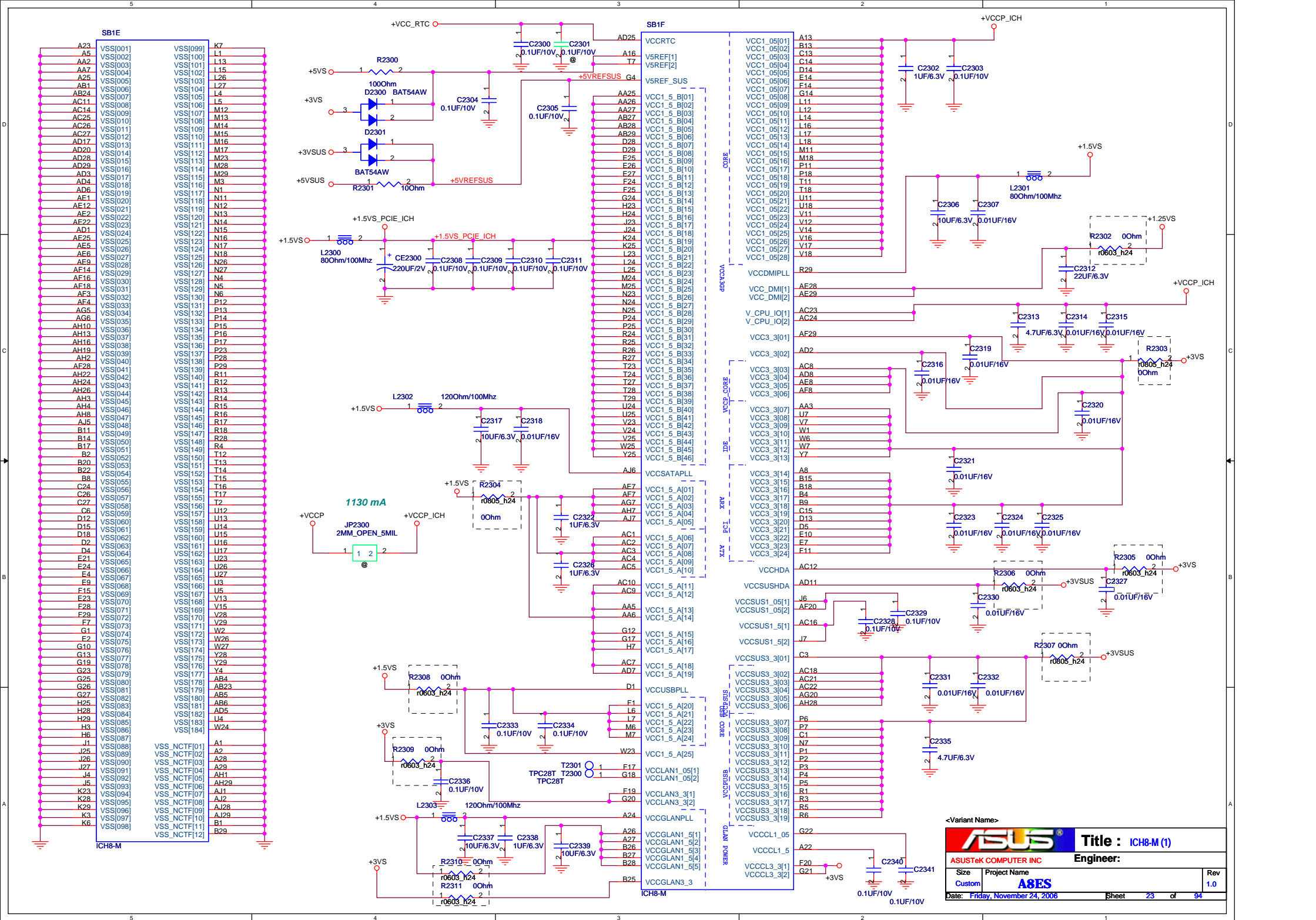
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Size	Project Name				Rev
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Date: Wednesday, October 11, 2006		Sheet 18 of 94			

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D				D
C				C
B				B
A				A
5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
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ICH8-M

22 SM_LINK0

22 SM_LINK1

Q2400B
UM6K1N
@

Q2400A
UM6K1N
@

Q2401B
UM6K1N

Q2401A
UM6K1N

R2400
4.7KOhm

R2401
4.7KOhm

ICH8-M

22 SCL_3A

22 SDA_3A

SCL_3S 7,8,29,43,53

SDA_3S 7,8,29,43,53

Check

Connect SMLINK and SMBUS
for SMBus 2.0 compliance.

<Variant Name>



Title : BLOCK DIAGRAM

ASUSTeK COMPUTER INC

Engineer:

Size
A

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1.0

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ICH8-M GPIO Assignment									
Name	H/W Pin Definition	Type	Tolerance	Power Well	Default	Mux	Native Name	Real Name	Note
GPIO0	PM_BMBUSY#	I/O	3.3V	Core	GPI	Yes	BMBUSY	PM_BMBUSY#	
GPIO1	BT_DET#	I/O	3.3V	Core	GPI	No			
GPIO2	PCI_INTE#	I/O	5V	Core	GPI	Yes	PIRQE#	PCI_INTE#	
GPIO3	PCI_INTF#	I/O	5V	Core	GPI	Yes	PIRQF#	PCI_INTF#	
GPIO4	PCI_INTG#	I/O	5V	Core	GPI	Yes	PIRQG#	PCI_INTG#	
GPIO5	PCI_INTH#	I/O	5V	Core	GPI	Yes	PIRQH#	PCI_INTH#	
GPIO6	BIOS_REC	I/O	3.3V	Core	GPI	No			
GPIO7	WLAN_LED_ON	I/O	3.3V	Core	GPI	No			
GPIO8	EXT_SM#	I/O	3.3V	Resume	GPI	No			
GPIO9	LAN_WOL_EN	I/O	3.3V	Resume	GPI	Yes	WOL_EN		
GPIO10	ME_ALERT#	I/O	3.3V	Resume	GPI	Yes	CLGPIO1		
GPIO11		I/O	3.3V	Resume	Native	Yes	SMBALERT#	pull high +3VSUS	
GPIO12	EXT_SC#	I/O	3.3V	Resume	GPI	No			
GPIO13	ODD_DET	I/O	3.3V	Resume	Native	Yes	GLAN_DOCK#		removing from EC
GPIO14	NETDETECT	I/O	3.3V	Resume	GPI	Yes	CLGPIO2		
GPIO15	STP_PC#	I/O	3.3V	Resume	Native	No	STP_PC#	STP_PC#	
GPIO16	PM DPRSLPVR	I/O	3.3V	Core	Native	Yes	DPRSLPVR	PM DPRSLPVR	
GPIO17	WLAN_ON#	I/O	3.3V	Core	GPI	No			
GPIO18		I/O	3.3V	Core	GPO	No			
GPIO19		I/O	3.3V	Core	GPI	Yes	SATA1GP		
GPIO20	BTLED_ON	I/O	3.3V	Core	GPO	No			
GPIO21		I/O	3.3V	Core	GPI	Yes	SATA0GP		
GPIO22		I/O	3.3V	Core	GPI	Yes	SCLOCK		
GPIO23		I/O	3.3V	Core	Native	Yes	LDRQ1#		
GPIO24	PS_CPPE#	I/O	3.3V	Resume	GPO	Yes	CLGPIO0		removing from EC; note by Alan
GPIO25	STP_CPU#	I/O	3.3V	Resume	Native	No	STP_CPU#	STP_CPU#	
GPIO26	PM_S4_STATE#	I/O	3.3V	Resume	Native	Yes	S4_STATE#		
GPIO27	BT_ON# BT_ON	I/O	3.3V	Resume	GPO	Yes	QRT_STATE0		
GPIO28	CB_SD#	I/O	3.3V	Resume	GPO	Yes	QRT_STATE1		Cardbus_Shutdown#
GPIO29	OC5#	I/O	3.3V	Resume	Native	Yes	OC5#		OC#
GPIO30	OC6#	I/O	3.3V	Resume	Native	Yes	OC6#		OC#
GPIO31	OC7#	I/O	3.3V	Resume	Native	Yes	OC7#		OC#
GPIO32	PM_CLKRUN#	I/O	3.3V	Core	Native	No	CLKRUN#	PM_CLKRUN#	
GPIO33		I/O	3.3V	Core	GPO	Yes	HDA_DOCK_EN#		
GPIO34		I/O	3.3V	Core	GPO	Yes	HDA_DOCK_RST#		
GPIO35	SATACLKREQ#	I/O	3.3V	Core	GPO	Yes	SATACLKREQ#		
GPIO36	EMAIL_LED#	I/O	3.3V	Core	GPI	Yes	SATA2GP		
GPIO37	PCB_ID0	I/O	3.3V	Core	GPI	Yes	SATA3GP		
GPIO38	PCB_ID1	I/O	3.3V	Core	GPI	Yes	SLOAD		
GPIO39	PCB_ID2	I/O	3.3V	Core	GPI	Yes	SDATAOUT0		
GPIO40	OC4#	I/O	3.3V	Resume	Native	Yes	OC4#		OC#
GPIO41	OC3#	I/O	3.3V	Resume	Native	Yes	OC3#		OC#
GPIO42	OC2#	I/O	3.3V	Resume	Native	Yes	OC2#		OC#
GPIO43	OC1#	I/O	3.3V	Resume	Native	Yes	OC1#		OC#
GPIO44		I/O	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO45		I/O	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO46		I/O	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO47		I/O	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO48		I/O	3.3V	Core	GPI	Yes	SDATAOUT1		
GPIO49	H_PWRGD	I/O	V_CPU_IO	V_CPU_IO	Native	Yes	CPUPWRGD	H_PWRGD	
GPIO50	PCI_REQ1#	I/O	5.5V	Core	Native	Yes	REQ1#		
GPIO51	PCI_GNT1#	I/O	3.3V	Core	Native	Yes	GNT1#		
GPIO52	PCI_REQ2#	I/O	5.5V	Core	Native	Yes	REQ2#		
GPIO53	PCI_GNT2#	I/O	3.3V	Core	Native	Yes	GNT2#		
GPIO54		I/O	5.5V	Core	Native	Yes	REQ3#		reserved for GPIO
GPIO55		I/O	3.3V	Core	Native	Yes	GNT3#		reserved for GPIO

Title : BLANK

Engineer:

ASUSTeK COMPUTER INC

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Title : BLANK

Engineer:

ASUSTek COMPUTER INC

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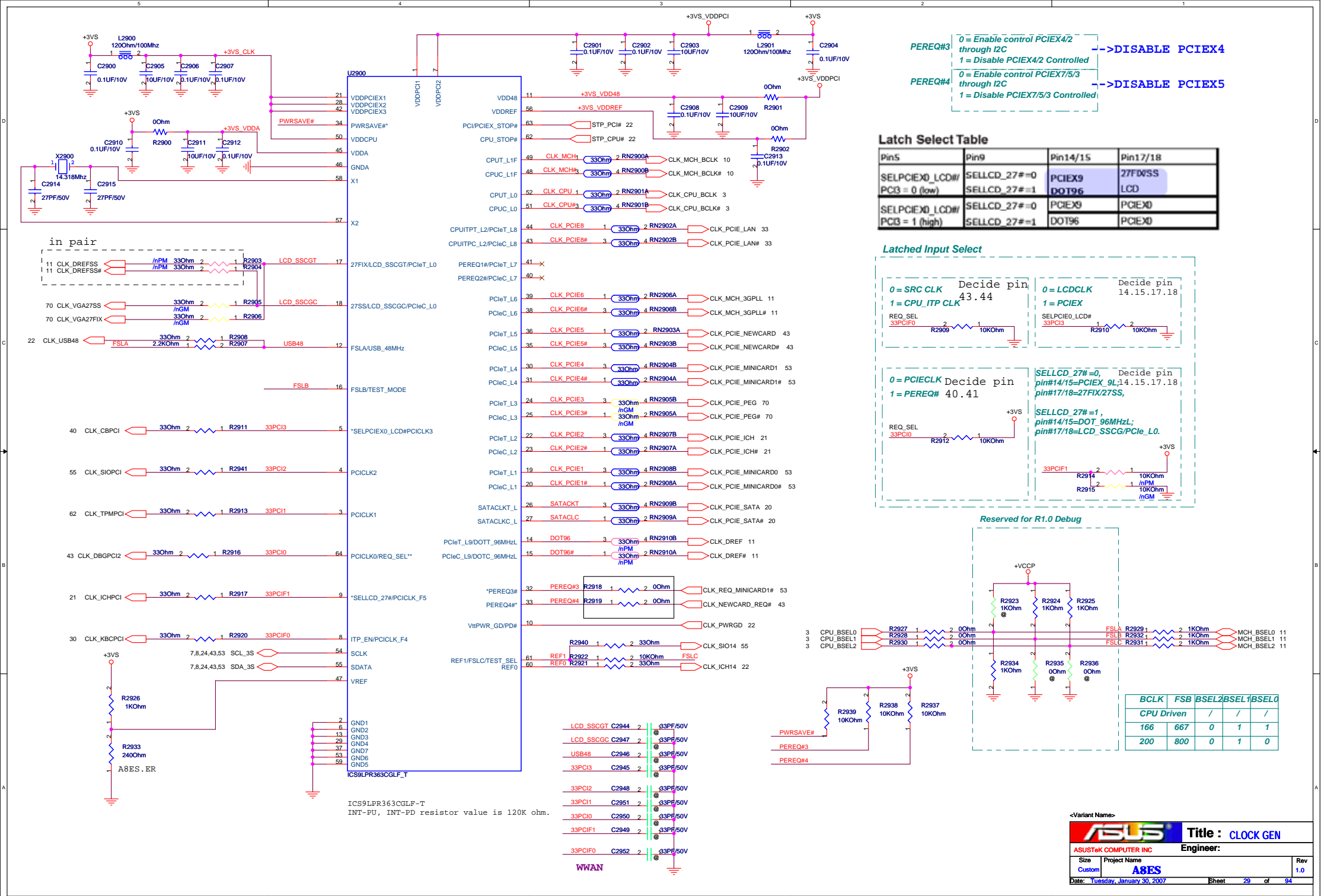
Wednesday, October 11, 2006

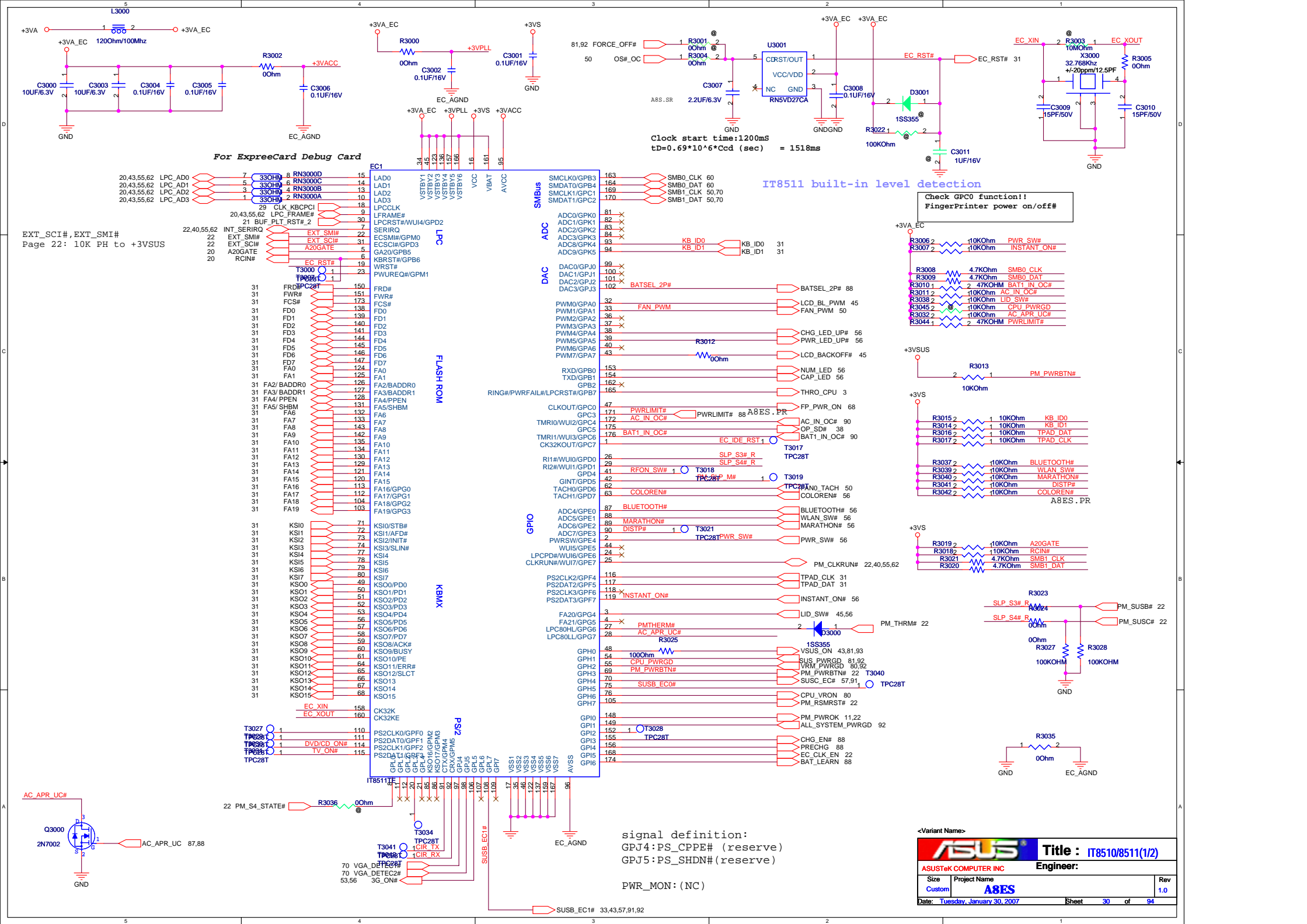
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ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	A8ES		0
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D				D
C				C
B				B
A				A

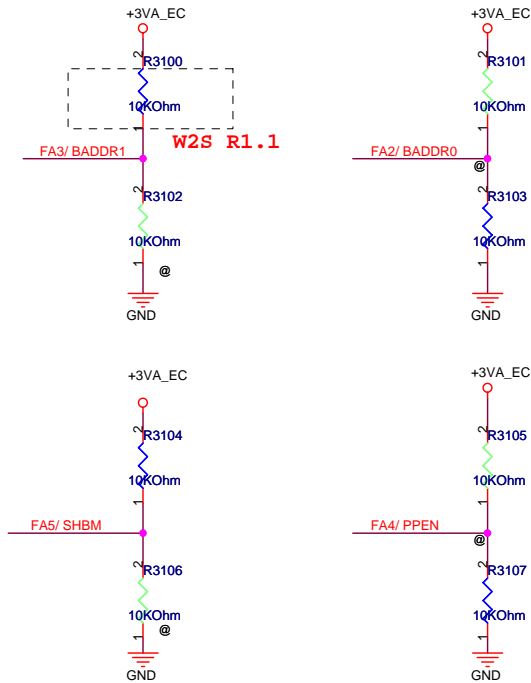
		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: Wednesday, October 11, 2006		Sheet 27 of 94	

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	A8ES		0
Date: Wednesday, October 11, 2006		Sheet 28 of 94	





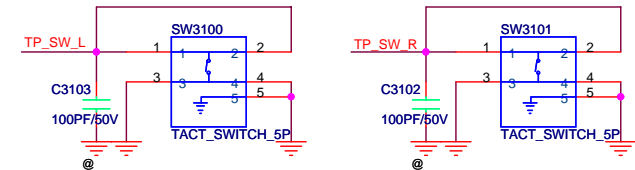
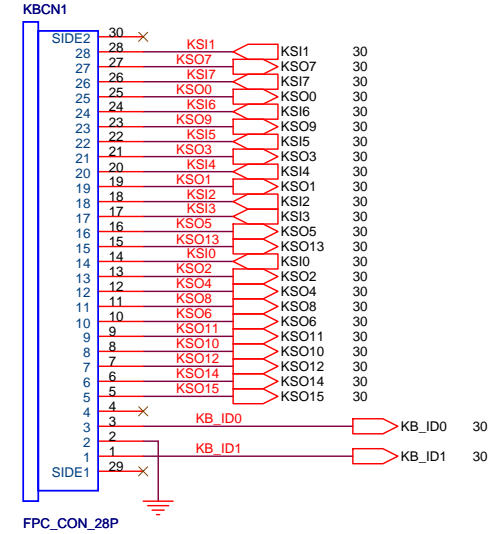
10:Determined by EC



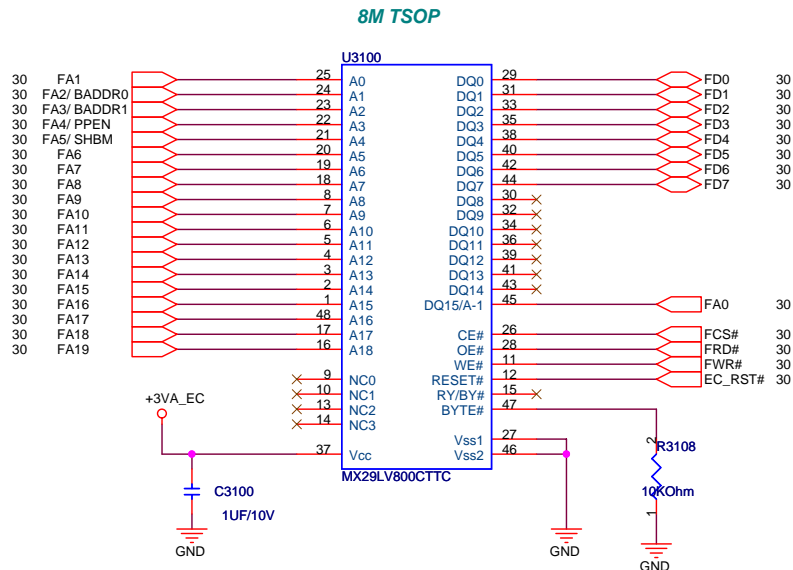
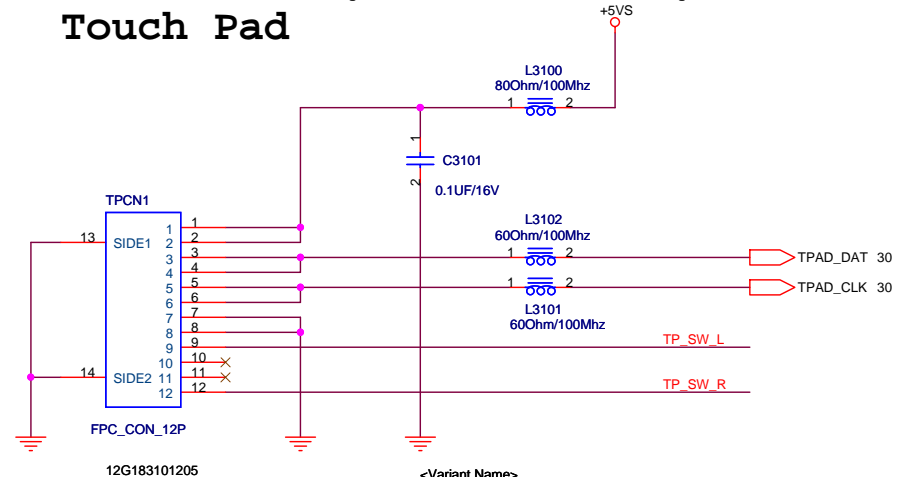
SHBM
No pull up:
disable shared memory with host BIOS
Ext 10K up:
enable shared memory with host BIOS

PPEN
No pull up:
Normal
Ext 10K up:
KBS interface pins are switched to parallel port interface for in-system programming.

KBDDT1	KBDDT0	Matrix
1	1	US
1	0	UK
0	1	JP




Touch Pad

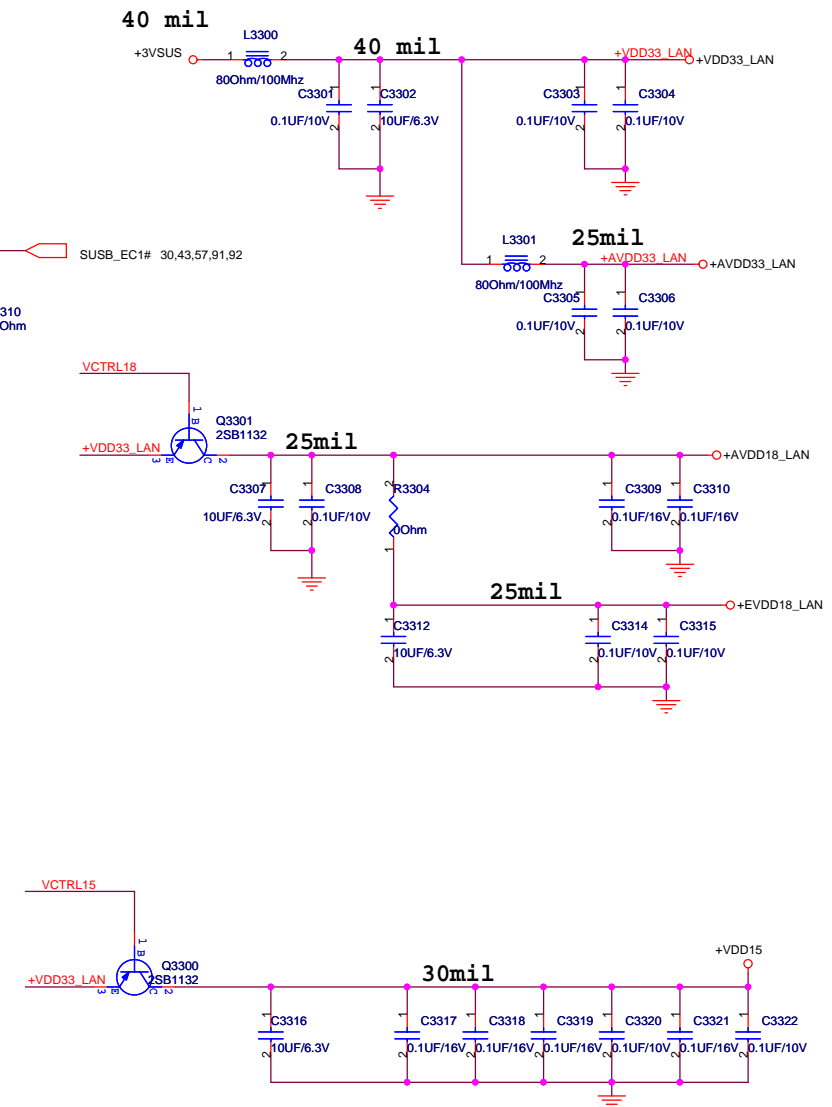


<Variant Name>

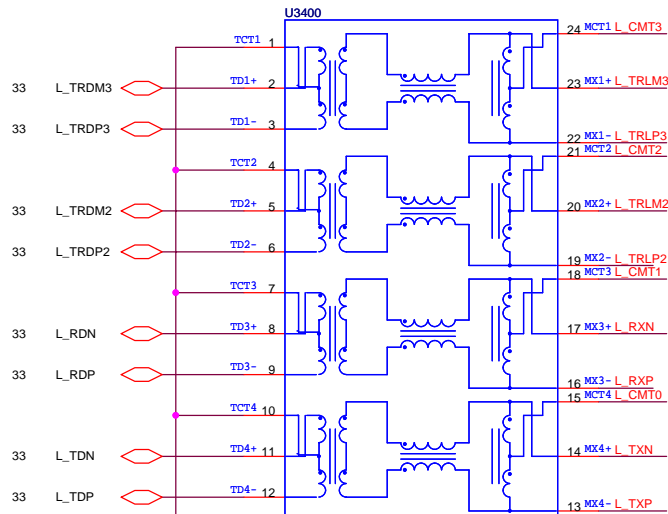
ASUS		Title : IT8510/8511(2/2)	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	1.0	
Date: Tuesday, January 30, 2007		Sheet 31 of 94	

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

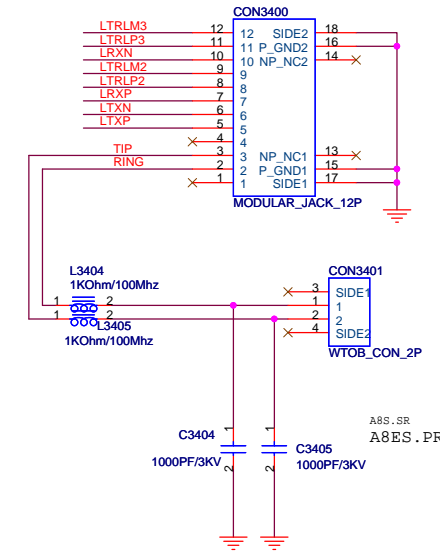
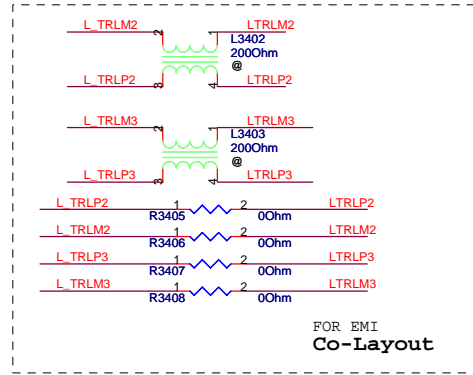
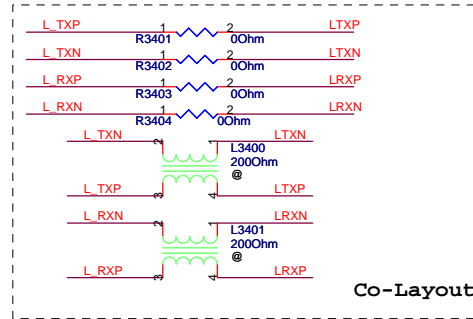
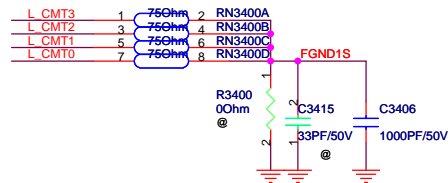
		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	A8ES		0
Date: Wednesday, October 11, 2006		Sheet	32 of 94



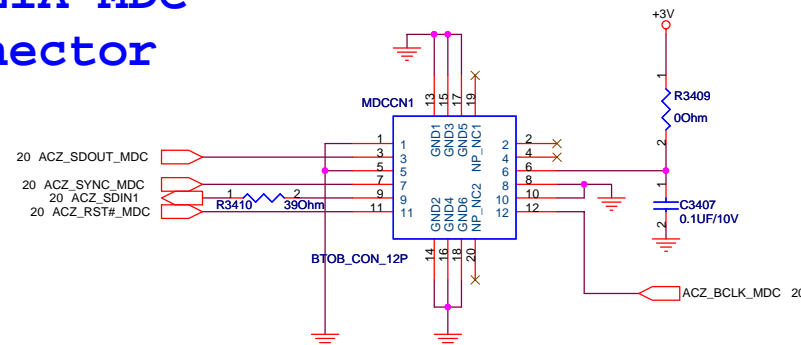
2402S have issue after IR reflow,
alternative part:LG-2410S-1



Transformer
close CON4




AZALIA MDC Connector

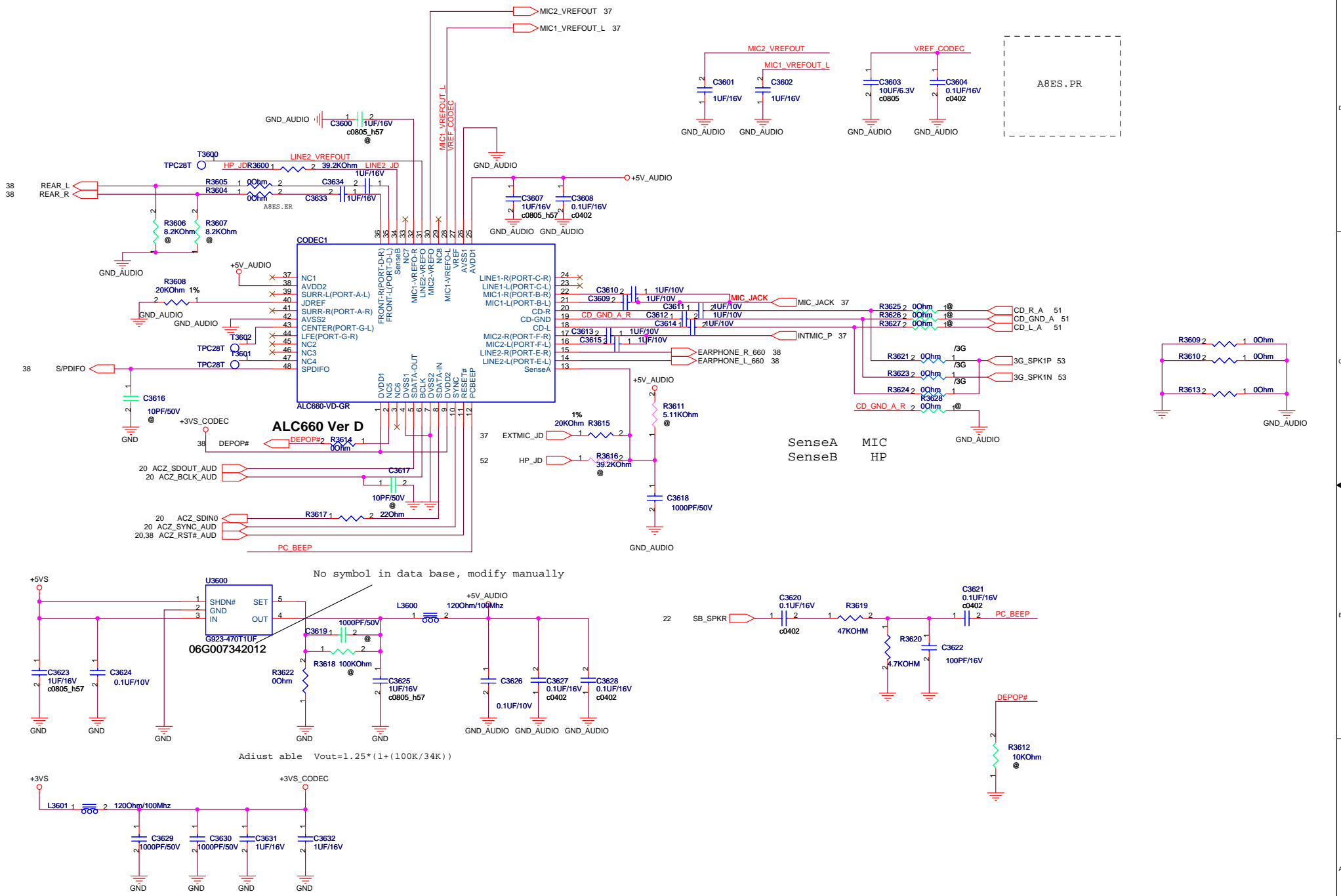


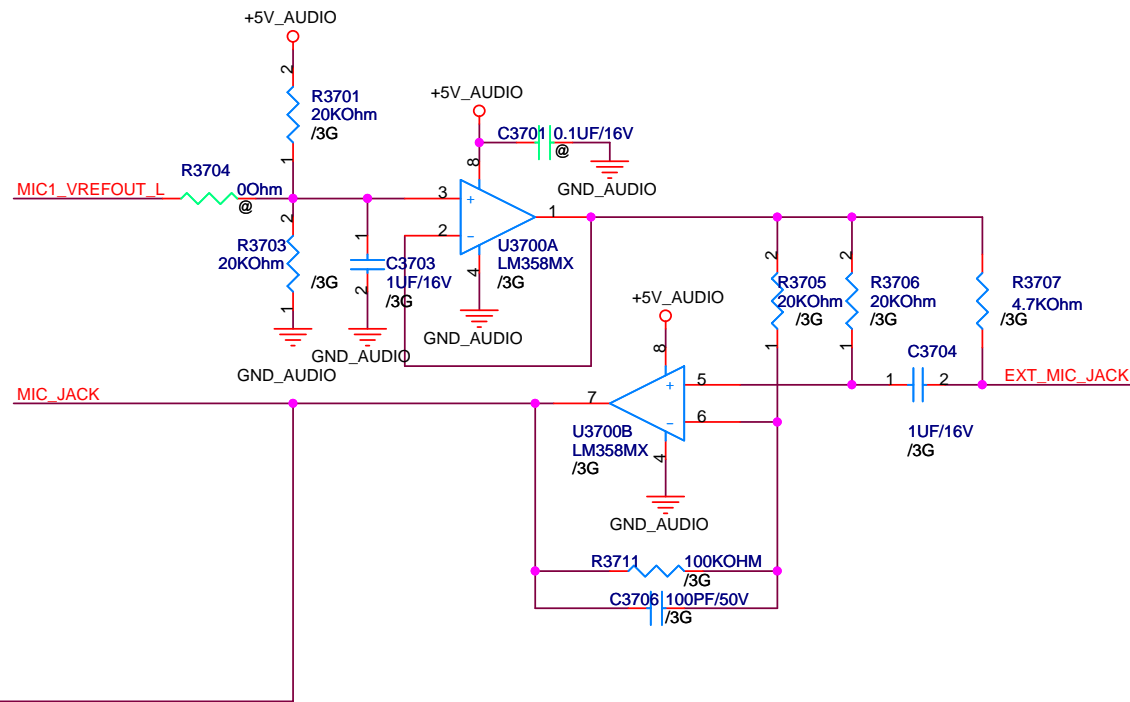
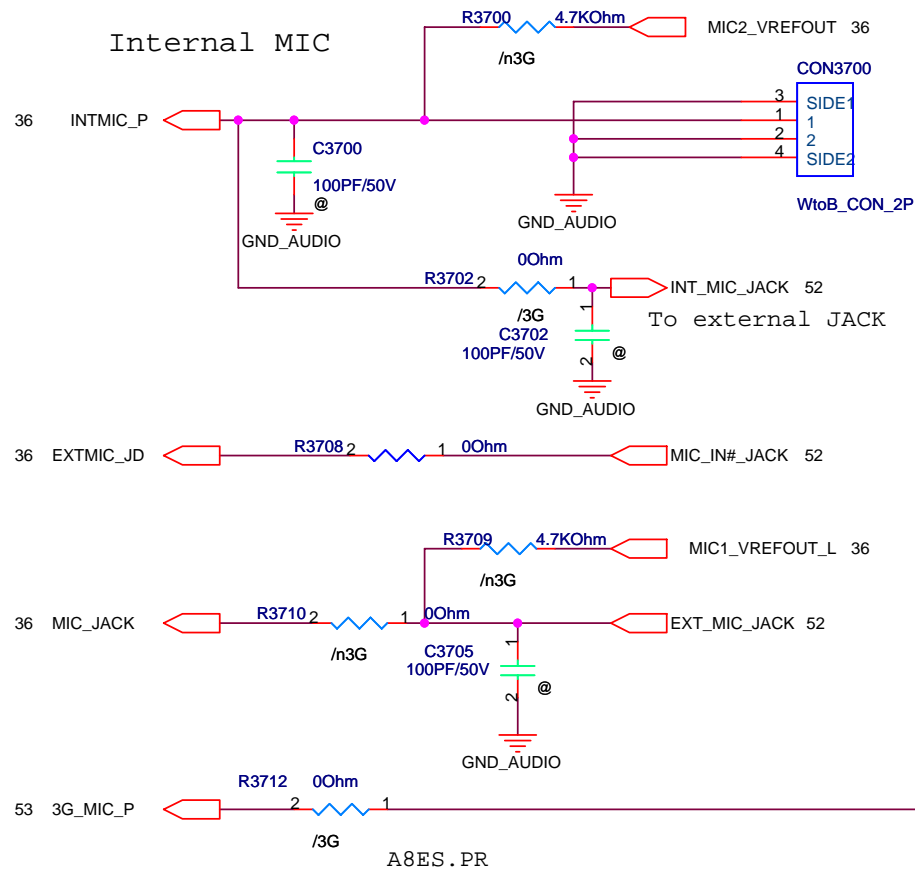
<Variant Name>

		Title : RJ11+45 , MDC	
ASUSTeK COMPUTER INC		Engineer:	
Size Custom	Project Name A8ES		Rev 1.0
Date: Tuesday, January 30, 2007		Sheet 34 of 94	

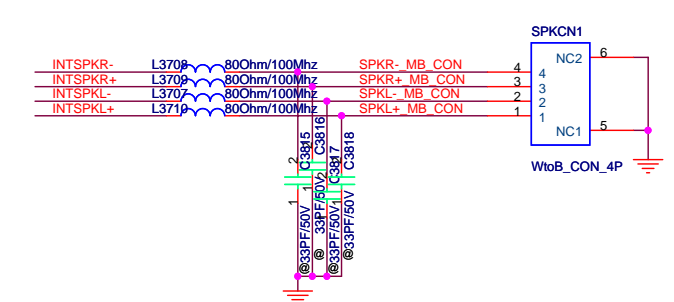
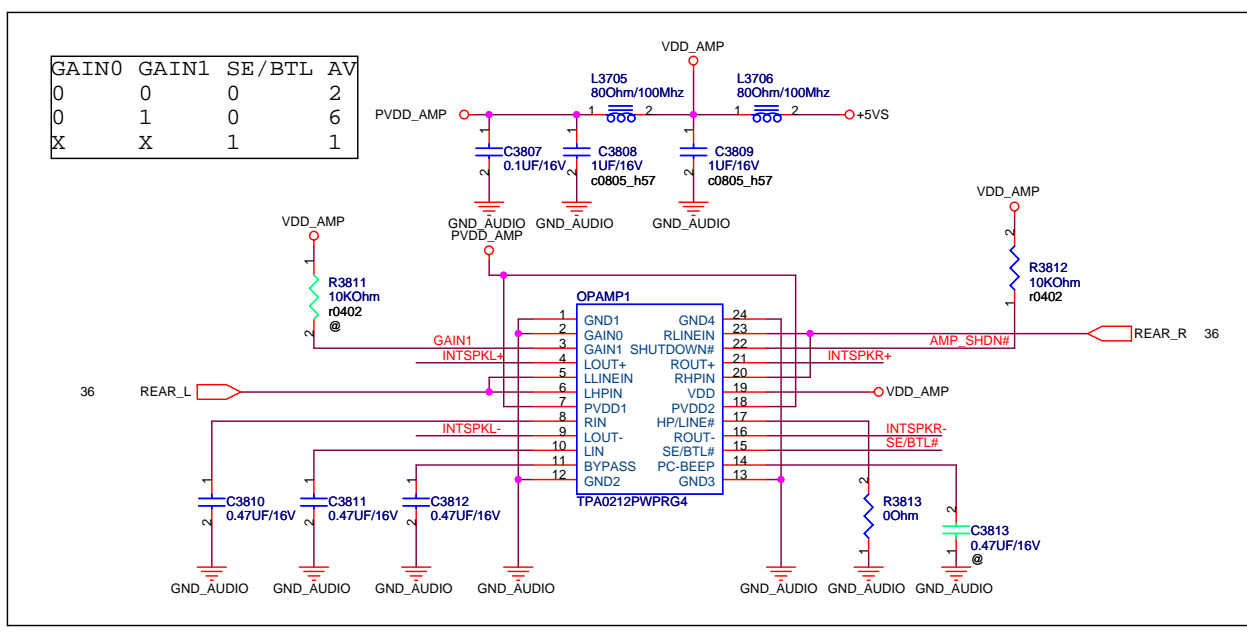
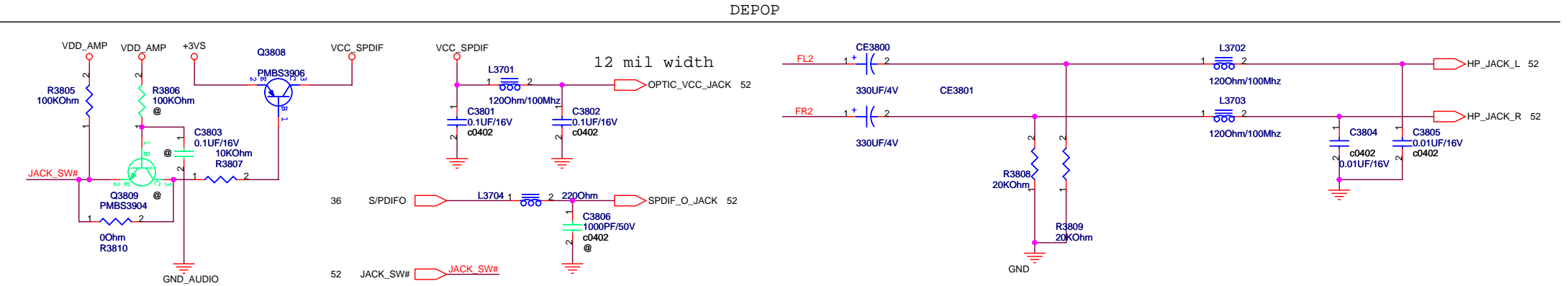
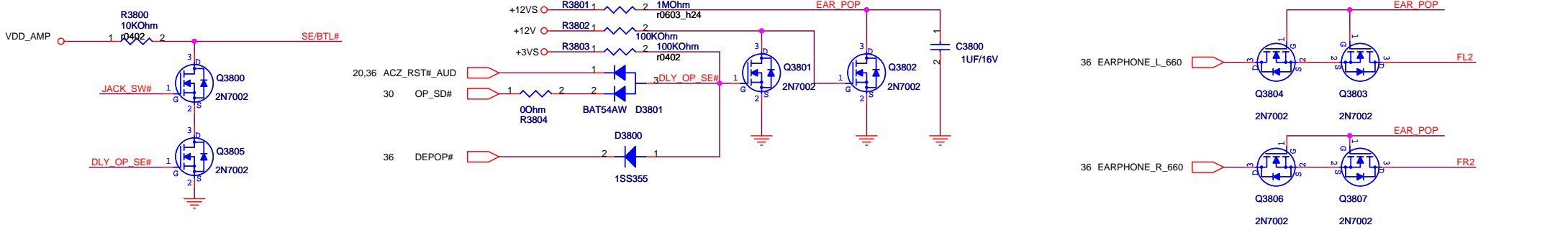
5	4	3	2	1
D				D
C				C
B				B
A				A

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: Wednesday, October 11, 2006		Sheet 35 of 94	





ASUS		Title : AUDIO-MIC	
ASUSTeK COMPUTER INC		Engineer:	
Size Custom	Project Name A8ES		Rev 1.0
Date: Tuesday, January 30, 2007		Sheet	37 of 94



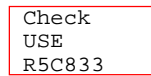
<Variant Name>

ASUS		Title : AUDIO-OP	
ASUSTeK COMPUTER INC		Engineer:	
Size B	Project Name A8ES		Rev 1.0
Date: Tuesday, January 30, 2007	Sheet	38	of 94

5	4	3	2	1
D				D
C				C
B				B
A				A

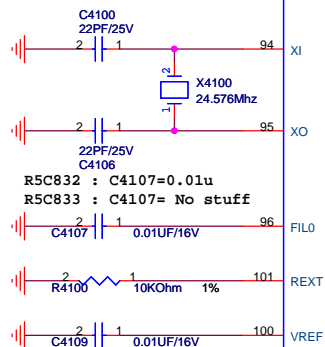
		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: Wednesday, October 11, 2006		Sheet 39 of 94	

Check
Circuit for R5C832 and R5C833



		Title : RICOH R5C832/PCI B	
ASUSTek COMPUTER INC		Engineer:	
Size Custom	Project Name A8ES		Rev 1.0
Date: Tuesday, January 30, 2007		Sheet 40 of 94	

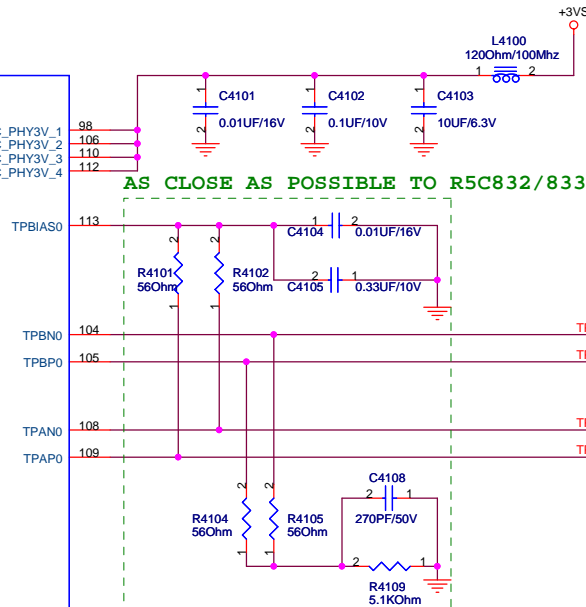
as close as possible to R5C832



IEEE1394/SD

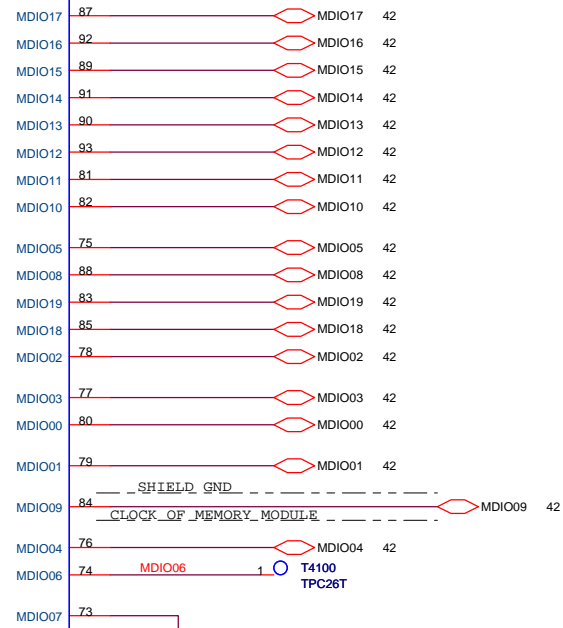
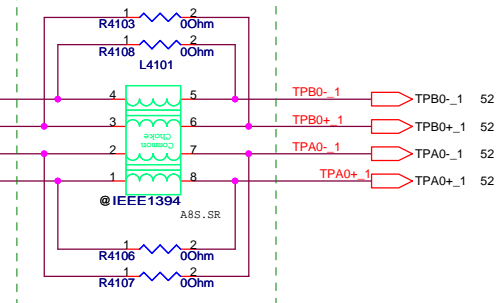
AVCC_PHY3V_1
AVCC_PHY3V_2
AVCC_PHY3V_3
AVCC_PHY3V_4

AS CLOSE AS POSSIBLE TO R5C832/833



Circuit area : As small as possible.

AS CLOSE AS POSSIBLE TO
1394 CONNECTOR.



MDIO02--> xDCE#

MDIO05--> SD Power Control 1 / xDWP

MDIO06--> xD/MS/SD LED Control

MDIO14--> xD Data

MDIO15--> xD Data

MDIO16--> xD Data

MDIO17--> xD Data

MDIO18--> xD CLE

MDIO19--> xD ALE

MDIO01--> MS Card Detect

MDIO03--> SD Write Protect

MDIO04--> SD Card Power0 Control/
MS Power Control

MDIO07--> SD External Clock/
MS External Clock

MDIO08--> SD Command/MS Bus State

MDIO09--> SD Clock/MS Clock

MDIO10--> SD Data 0/MS Data 0

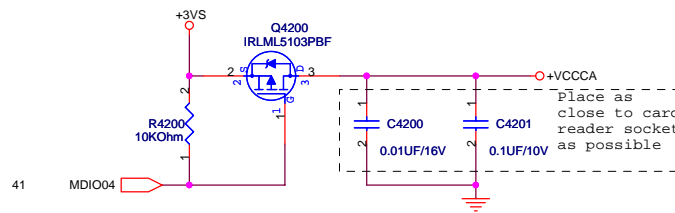
MDIO11--> SD Data 1/MS Data 1

MDIO12--> SD Data 2/MS Data 2

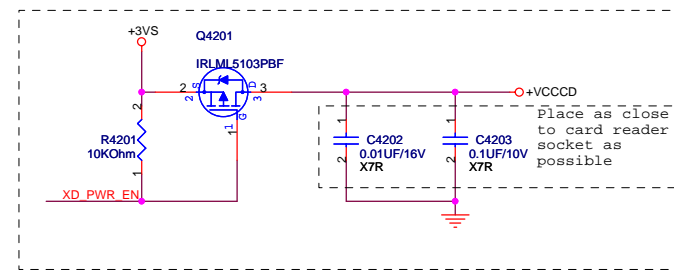
MDIO13--> SD Data 3/MS Data 3

<Variant Name>

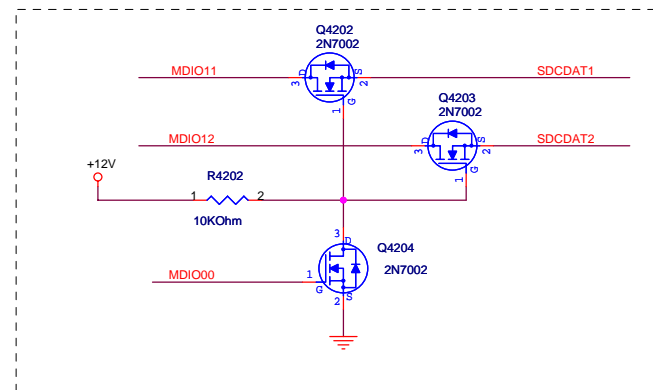
ASUS		Title : RICOH R5C832/PCL_A	
ASUSTeK COMPUTER INC		Engineer:	
Size Custom	Project Name A8ES	Rev 1.0	
Date: Tuesday, January 30, 2007		Sheet 41 of 94	



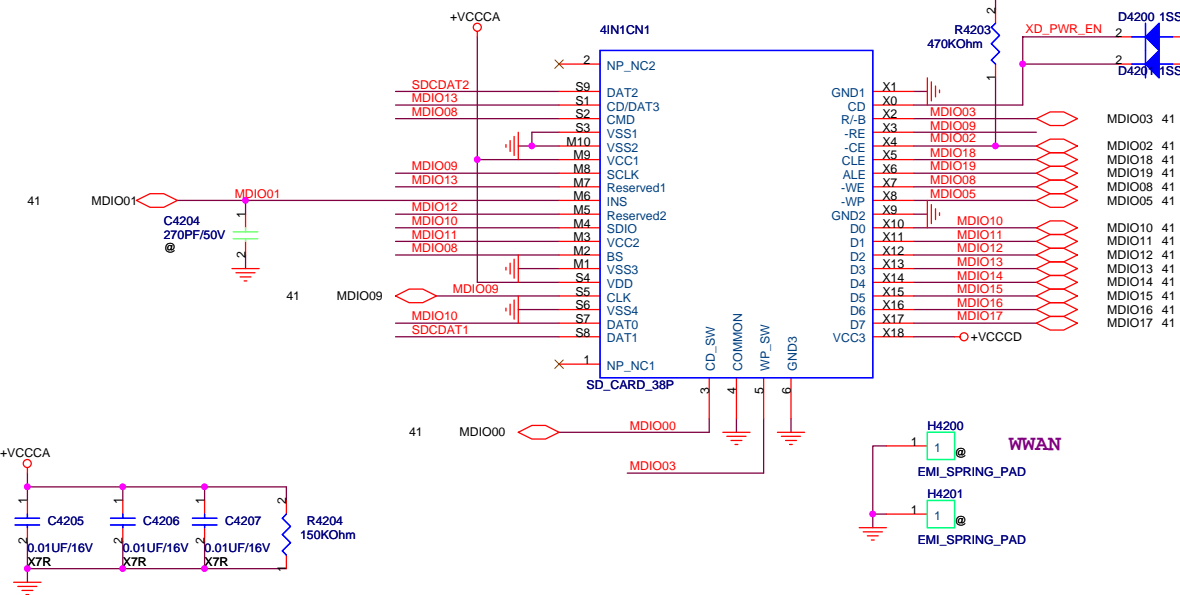
To correct the problem when MS Duo adaptor is in use.



Solve MS Duo Adaptor short issue.



Check
Change other p/n!!



- MDIO00--> SD Card Detect
- MDIO01--> MS Card Detect
- MDIO03--> SD Write Protect
- MDIO04--> SD Card Power0 Control/
MS Power Control
- MDIO08--> SD Command/MS Bus State
- MDIO09--> SD Clock/MS Clock
- MDIO10--> SD Data 0/MS Data 0
- MDIO11--> SD Data 1/MS Data 1
- MDIO12--> SD Data 2/MS Data 2
- MDIO13--> SD Data 3/MS Data 3

- MDIO02--> xDCE#
- MDIO05--> SD Power Control 1 / xDWP
- MDIO06--> xD/MS/SD LED Control
- MDIO14--> xD Data
- MDIO15--> xD Data
- MDIO16--> xD Data
- MDIO17--> xD Data
- MDIO18--> xD CLE
- MDIO19--> xD ALE

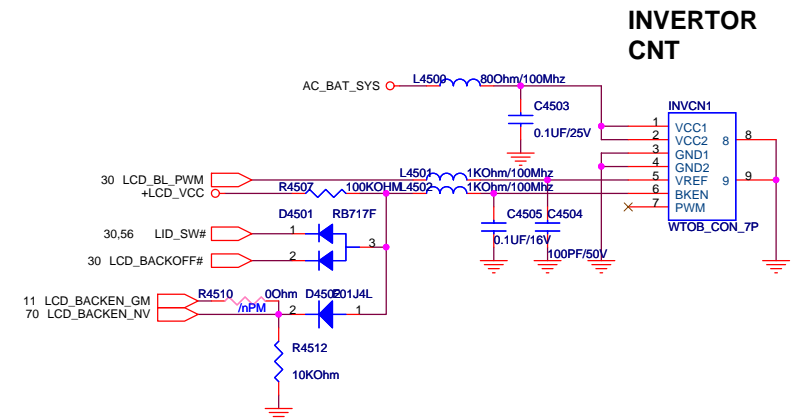
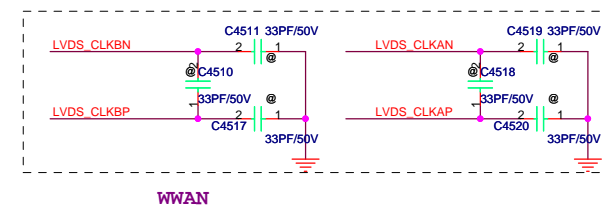
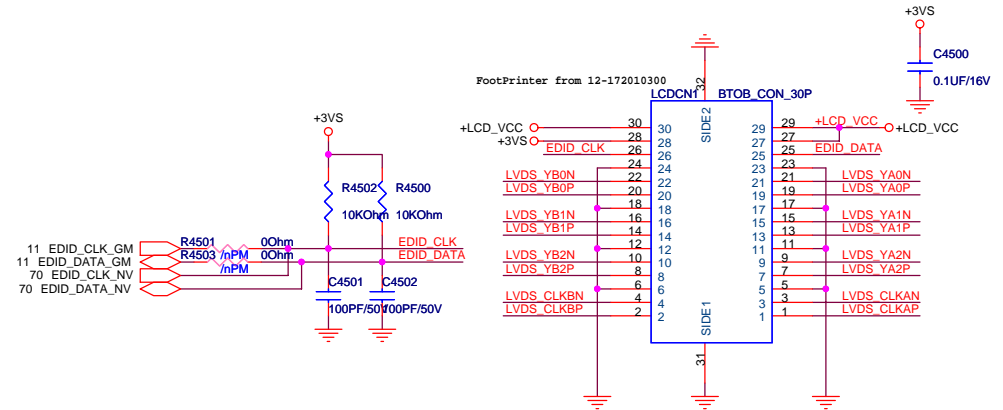
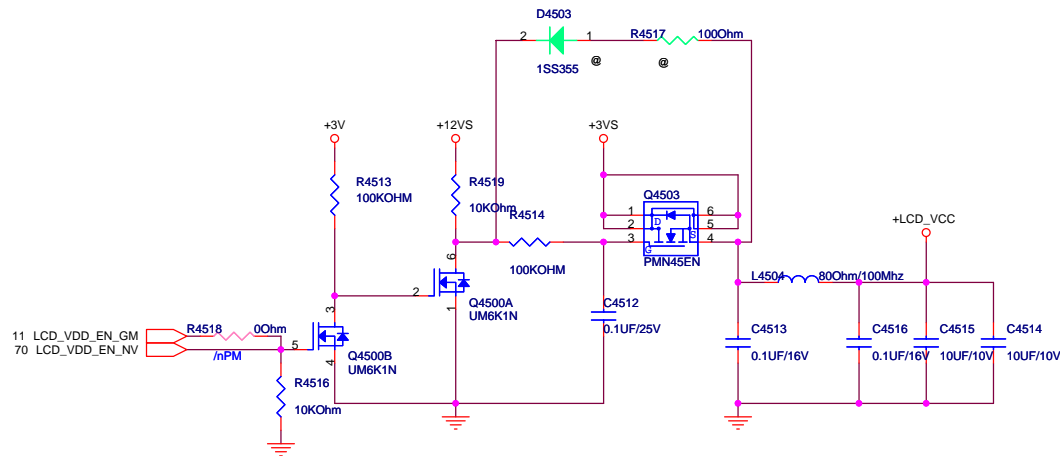
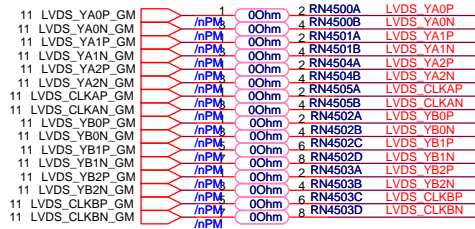
<Variant Name>

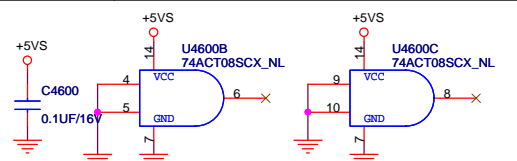
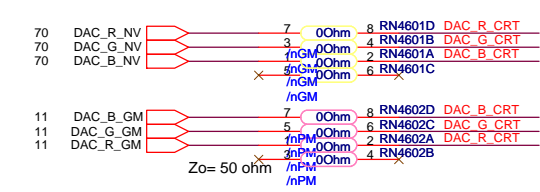
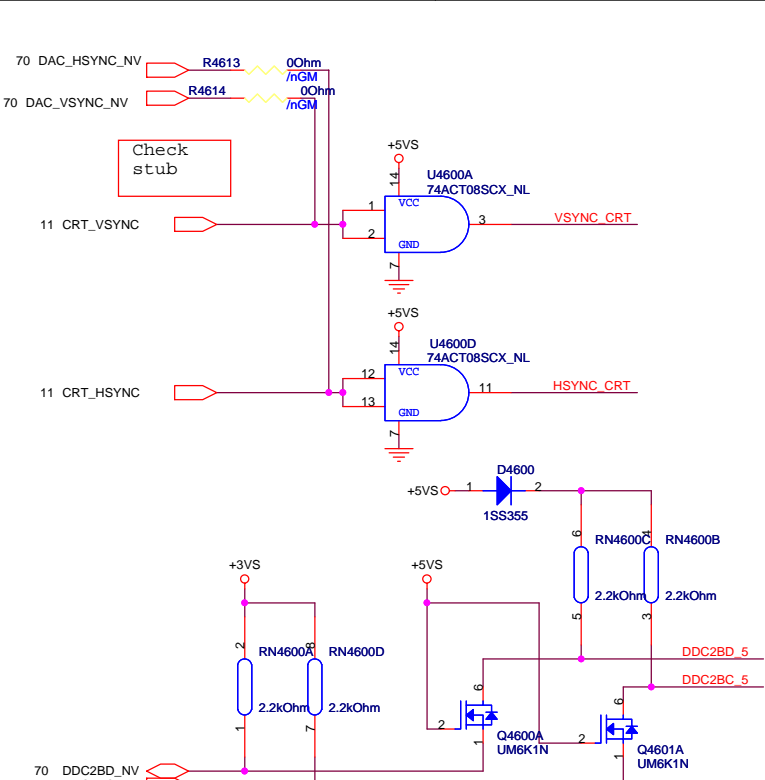
ASUS		Title : CardReader	
ASUSTek COMPUTER INC		Engineer:	
Size Custom	Project Name A8ES		Rev 1.0
Date: Thursday, January 25, 2007		Sheet 42 of 94	

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

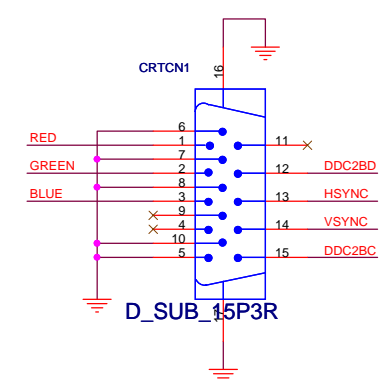
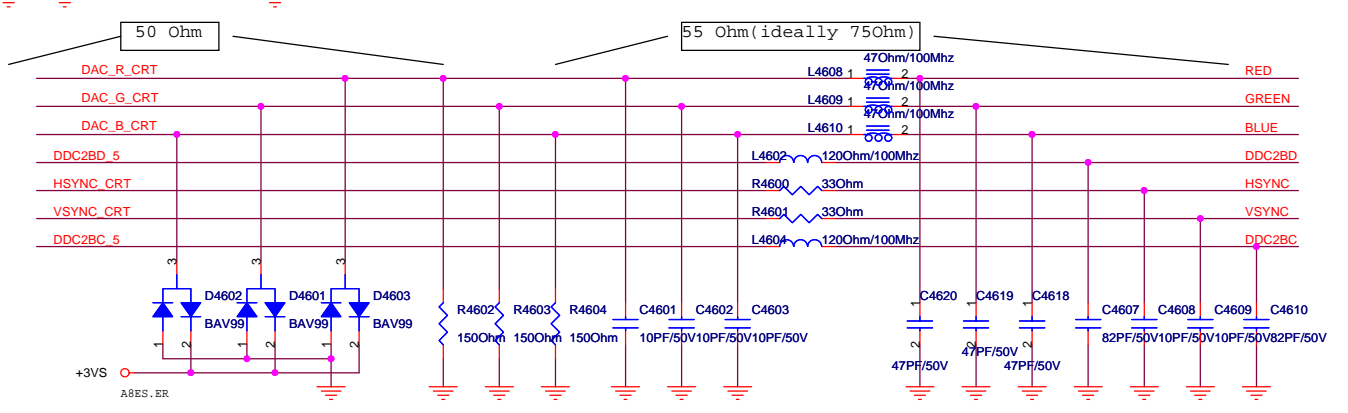
		Title : Blank	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 1.0
Date: Wednesday, October 11, 2006		Sheet	44 of 94

Check stub





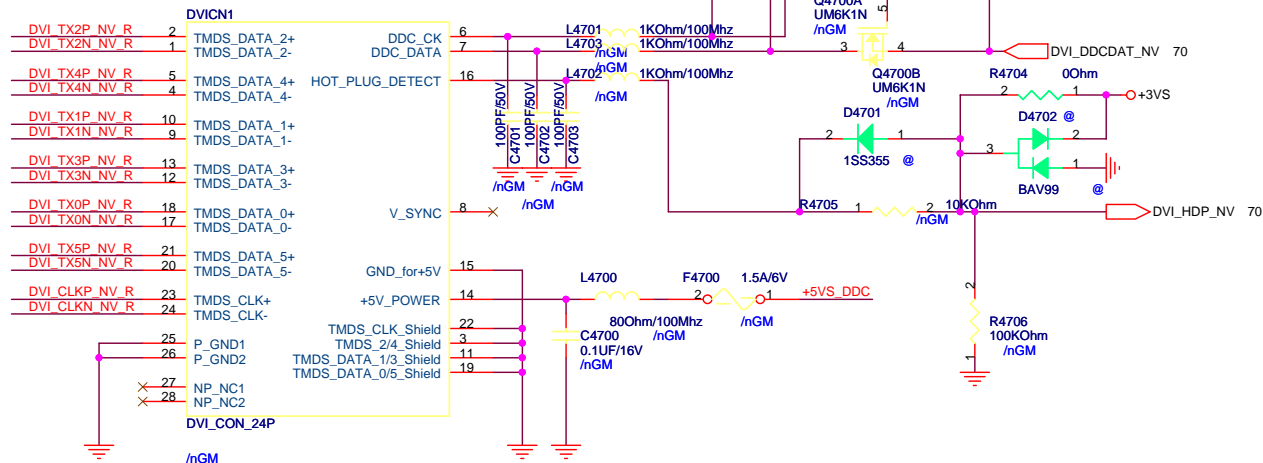
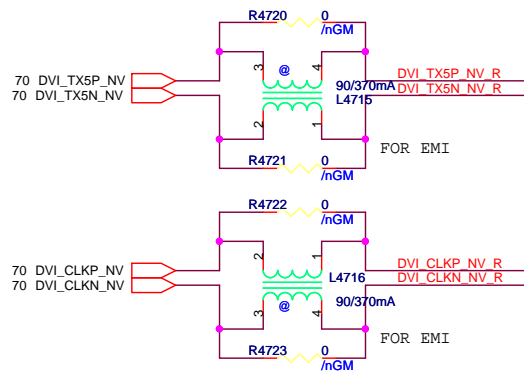
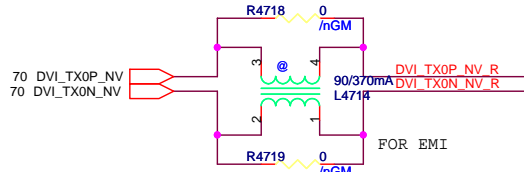
+2.5VS	+2.5VS	70,84
+3VS	+3VS	3,7,8,11,14,15,21,22,23,24,29,30,33,36,38,40,41,42,43,45,47,49,50,51,53,55,57,62,68,70,80
+5V	+5V	9,43,52,57,68,70,91
+5VS	+5VS	23,24,31,36,38,47,50,51,56,57,68,80,91



Blue:12G10110015L

<Variant Name>

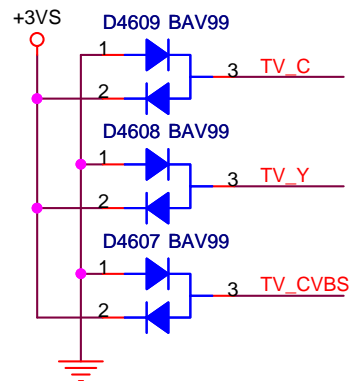
ASUS		Title : CRT & TV-Out	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	1.0	
Date: Tuesday, January 30, 2007		Sheet 46 of 94	



+5VS +5VS 23,24,31,36,38,46,50,51,56,57,68,80,91

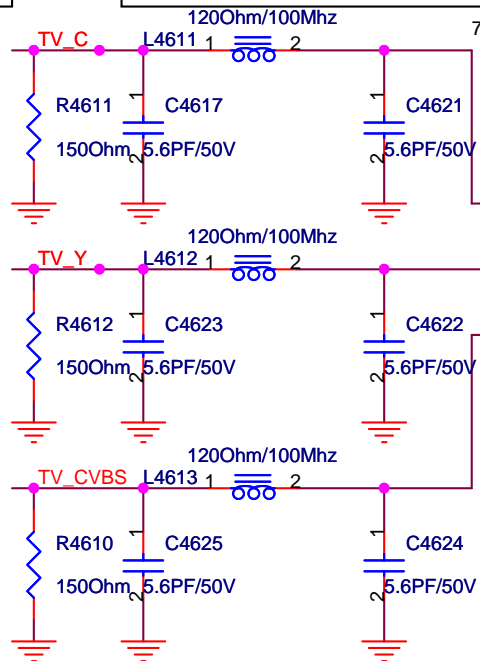
5	4	3	2	1
D				D
C				C
B				B
A				A

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: Wednesday, October 11, 2006		Sheet 48 of 94	



50 Ohm

55 Ohm(ideally 75Ohm)



HDTV_EN#

C CON

Y CON

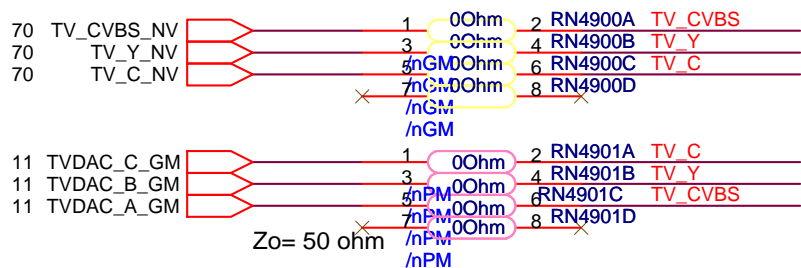
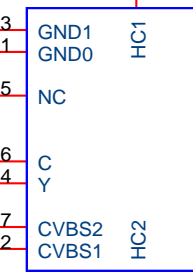
CVBS CON

12-141011072

TVSCN1

MINI_DIN_7P

12G141011077



Zo= 50 ohm



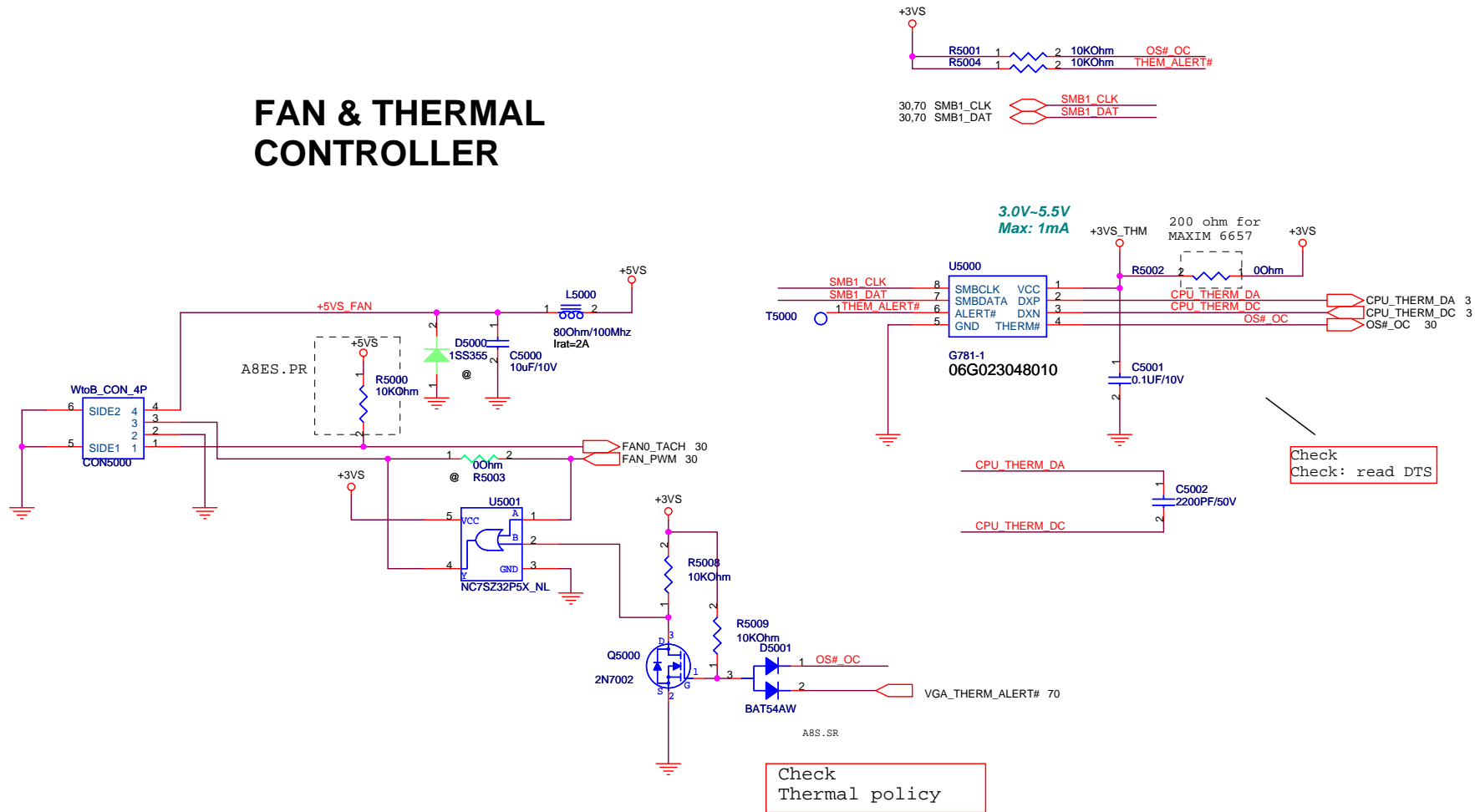
Title : TV

ASUSTeK COMPUTER INC

Engineer:

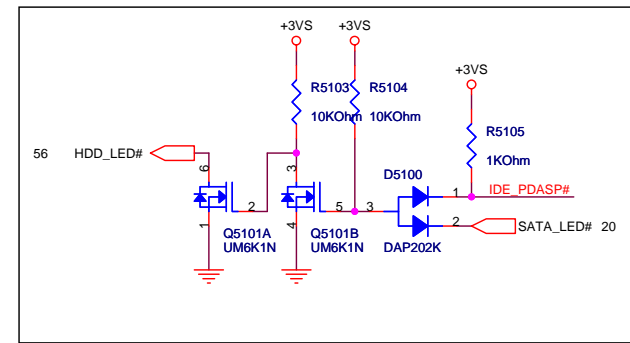
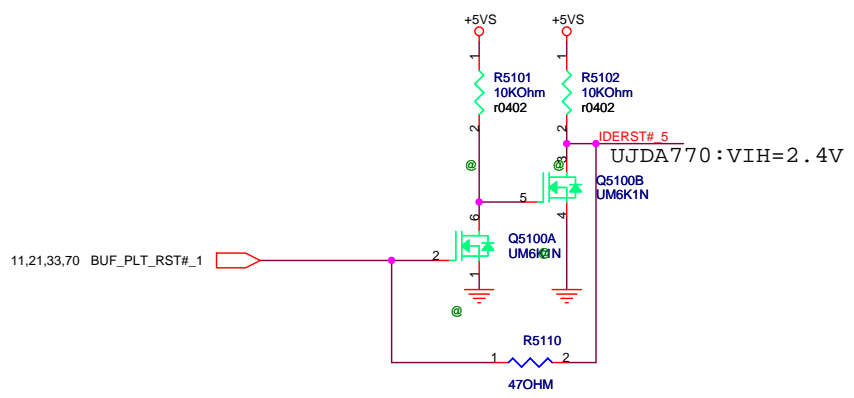
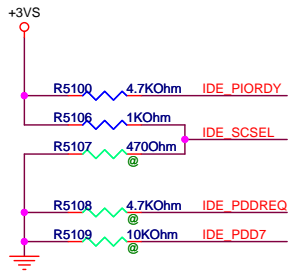
Size A	Project Name A8ES	Rev 1.0
Date: Tuesday, January 30, 2007	Sheet 49 of 94	

FAN & THERMAL CONTROLLER

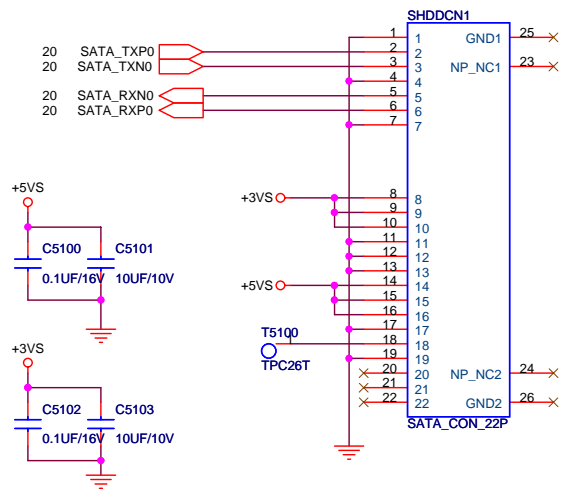


<Variant Name>

ASUS		Title : FAN & THERMAL	
ASUSTeK COMPUTER INC		Engineer:	
Size B	Project Name A8ES		Rev 1.0
Date: Tuesday, January 30, 2007		Sheet 50 of 94	

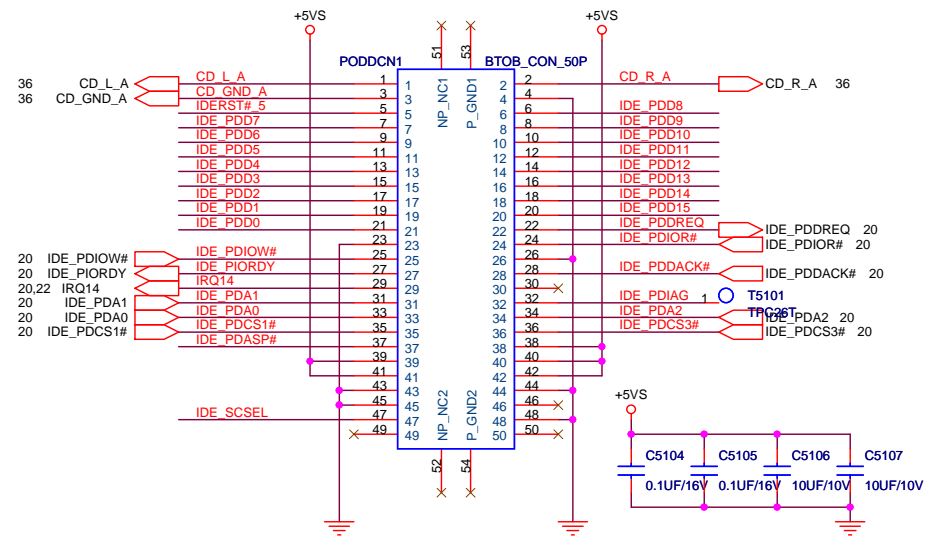


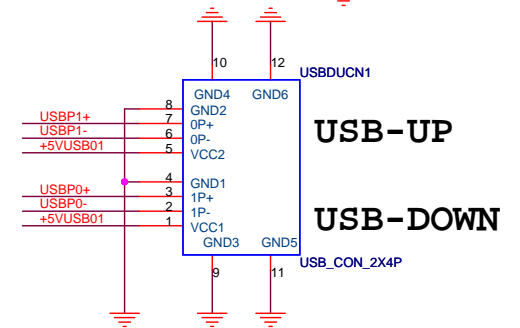
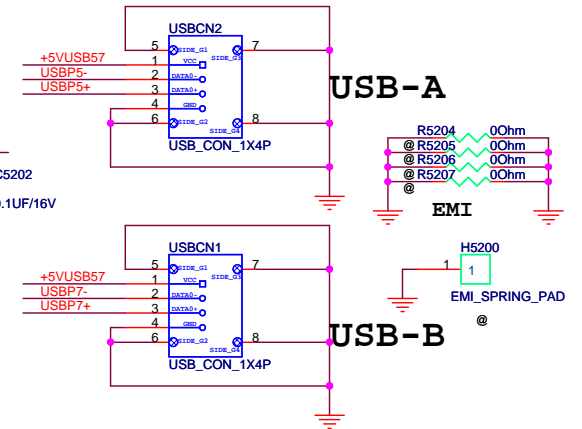
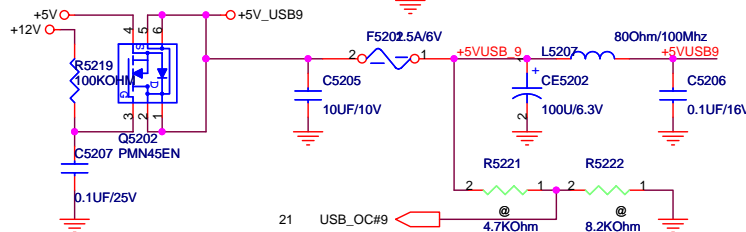
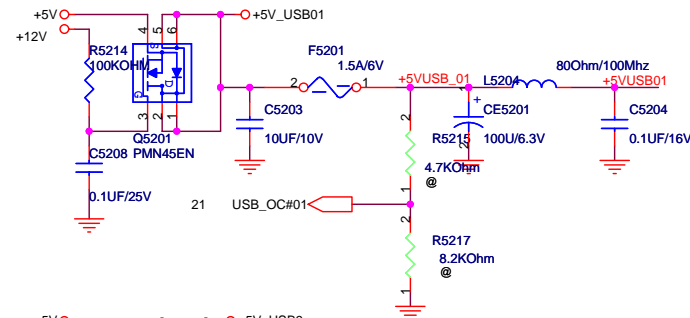
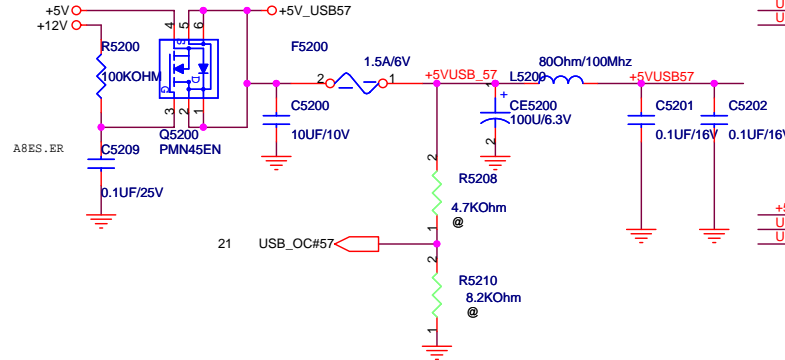
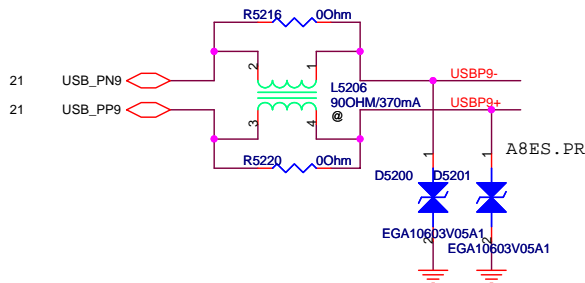
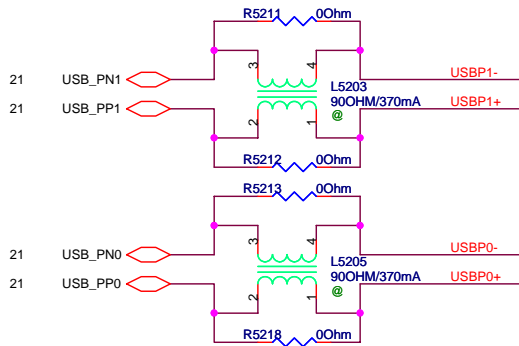
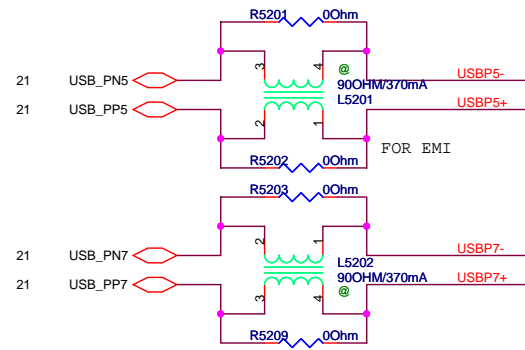
SATA HDD CON



+3VS → +3VS 3,7,8,11,14,15,21,22,23,24,29,30,33,36,38,40,41,42,43,45,46,47,49,50,53,55,57,62,68,70,80,91,92
 +5VS → +5VS 23,24,31,36,38,46,47,50,56,57,68,80,91
 +5V → +5V 9,43,52,57,68,70,91

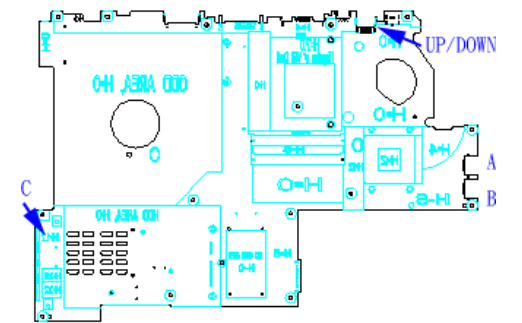
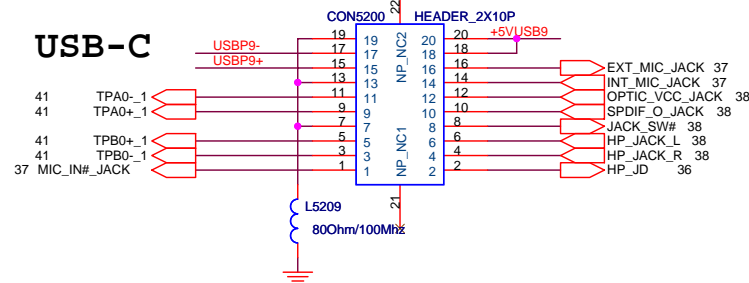
PATA CD-ROM CON





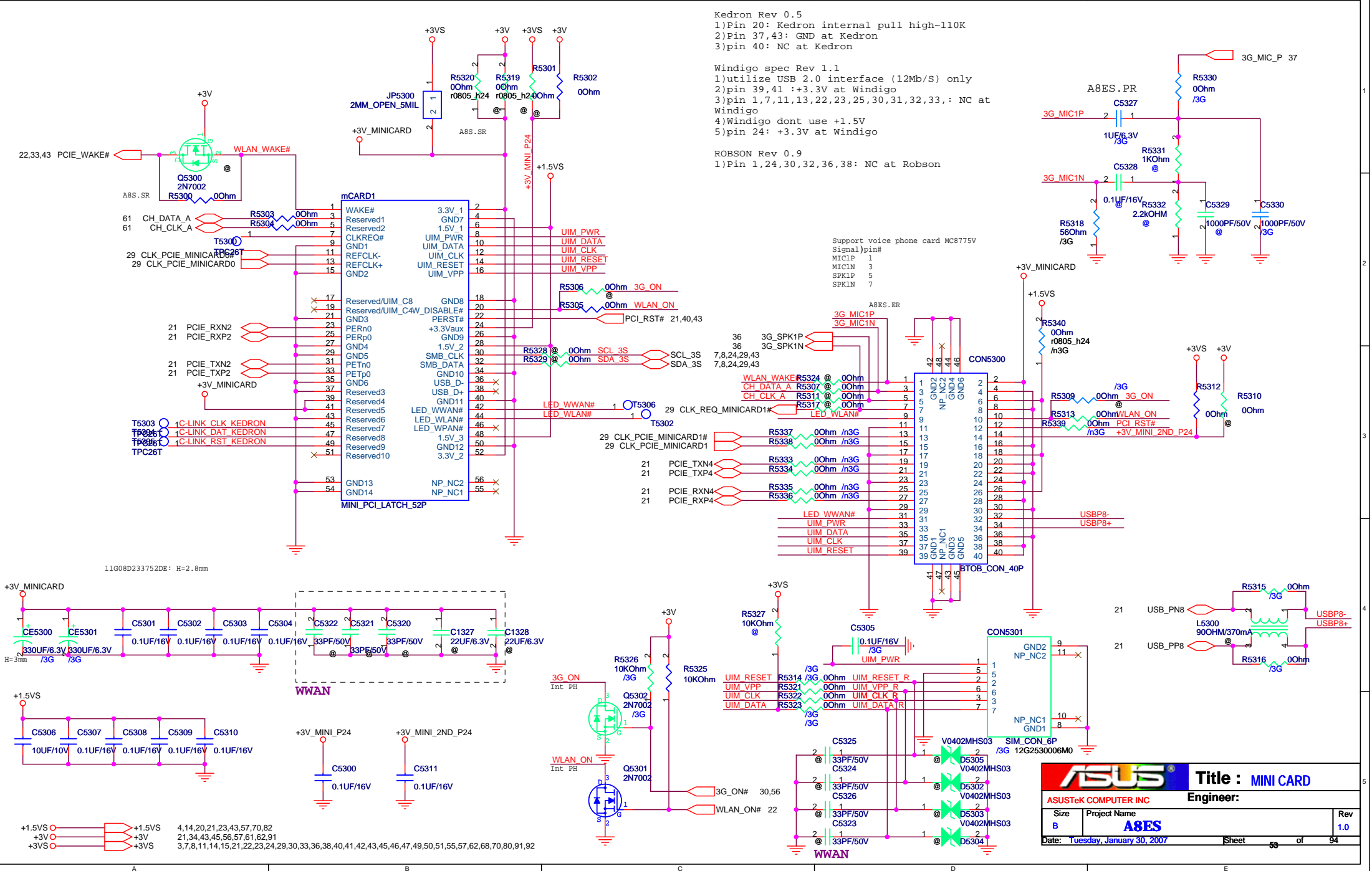
SUB-PCB: USB/1394/MIC/EARPHONE

USB-C



<Variant Name>

ASUS		Title : USB/SUB PCB	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	1.0	
Date: Tuesday, January 30, 2007	Sheet	52	of 94




Kedron Rev 0.5
1)Pin 20: Kedron internal pull high~110K
2)Pin 37,43: GND at Kedron
3)pin 40: NC at Kedron

Windigo spec Rev 1.1
1)utilize USB 2.0 interface (12Mb/S) only
2)pin 39,41 :+3.3V at Windigo
3)pin 1,7,11,13,22,23,25,30,31,32,33,: NC at Windigo
4)Windigo dont use +1.5V
5)pin 24: +3.3V at Windigo

ROBSON Rev 0.9
1)Pin 1,24,30,32,36,38: NC at Robson

Support voice phone card MC8775V
Signal)pin#
MIC1P 1
MIC1N 3
SPK1P 5
SPK1N 7



Title : MINI CARD

ASUSTeK COMPUTER INC

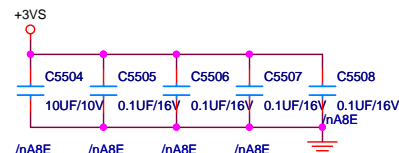
Engineer:

Size	Project Name	Rev
B	A8ES	1.0

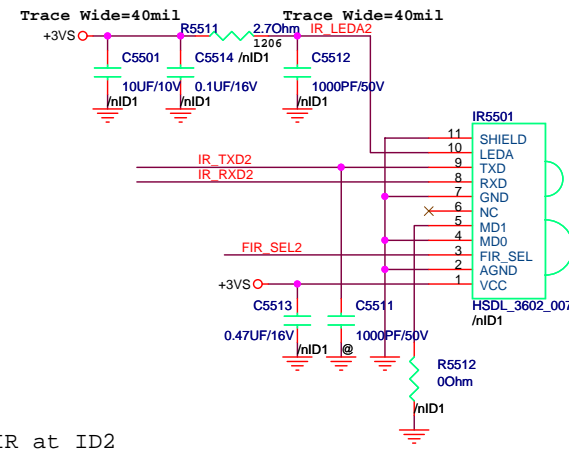
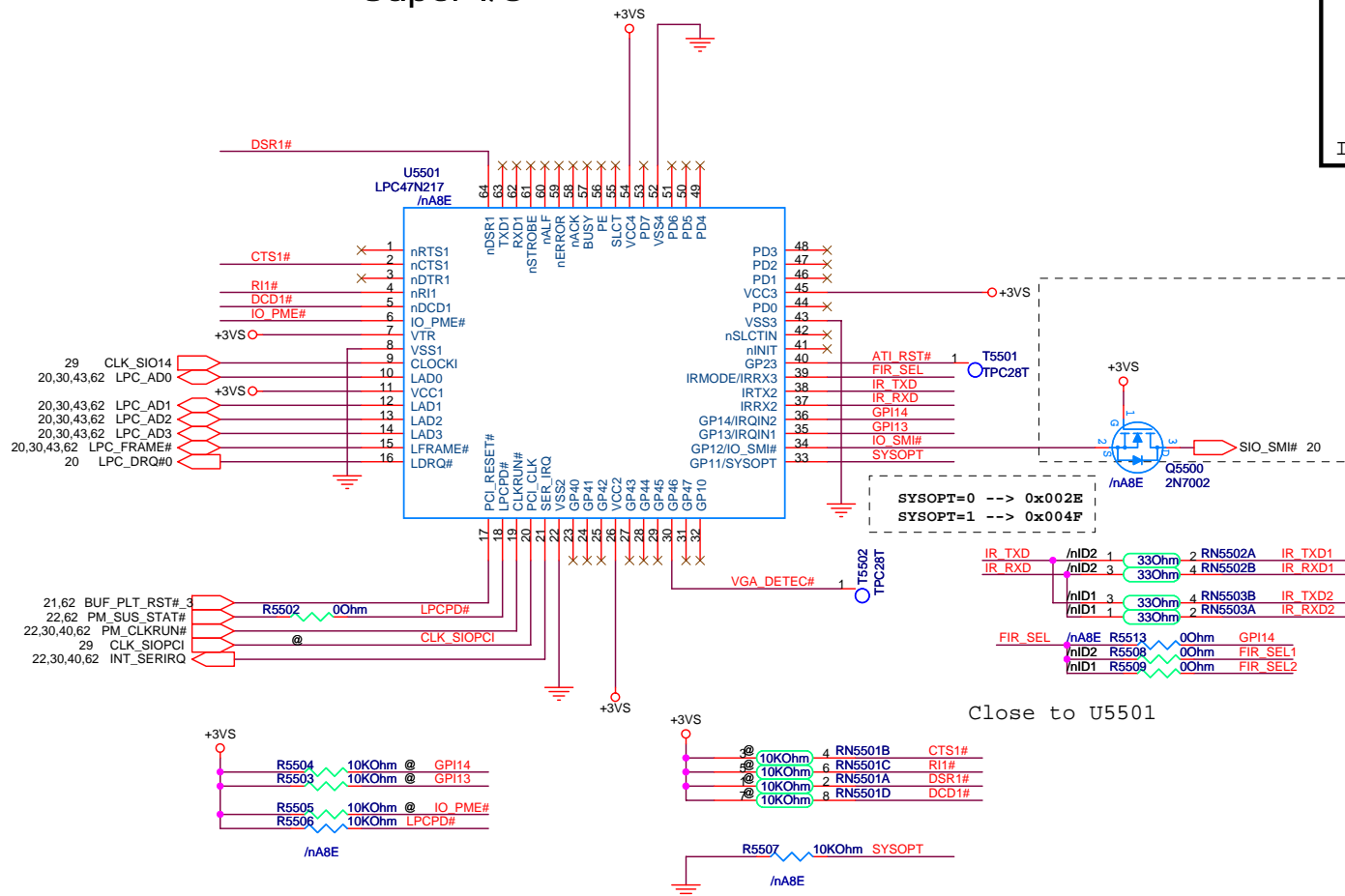
Date: Tuesday, January 30, 2007

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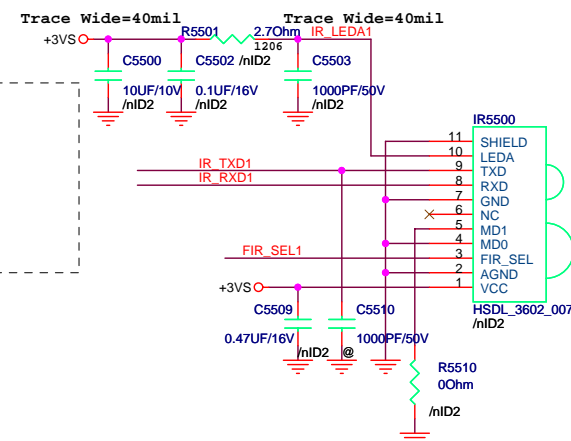
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ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	A8ES		0
Date: Wednesday, October 11, 2006		Sheet 54 of 94	



Super I/O



IR at ID2



Close to U5501

Transceiver Control Truth Table

Mode 0	Mode 1	FIR_SEL	RX Function	TX Function
1	0	X	Shutdown	Shutdown
0	0	0	SIR	Full Distance Power
0	1	0	SIR	2/3 Distance Power
1	1	0	SIR	1/3 Distance Power
0	0	1	MIR/FIR	Full Distance Power
0	1	1	MIR/FIR	2/3 Distance Power
1	1	1	MIR/FIR	1/3 Distance Power

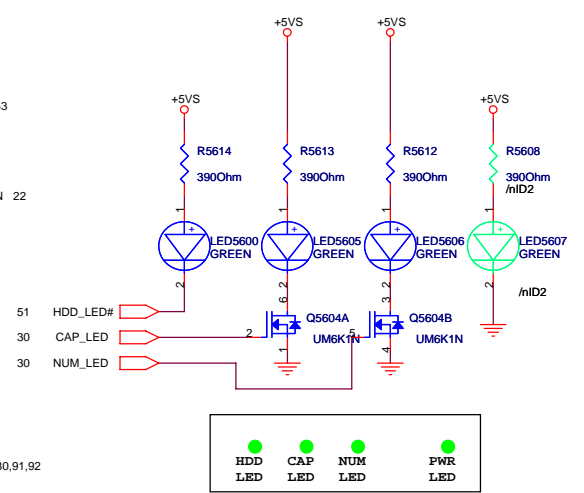
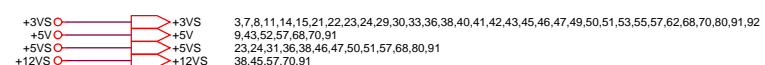
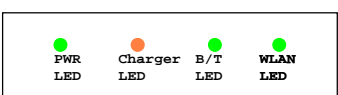
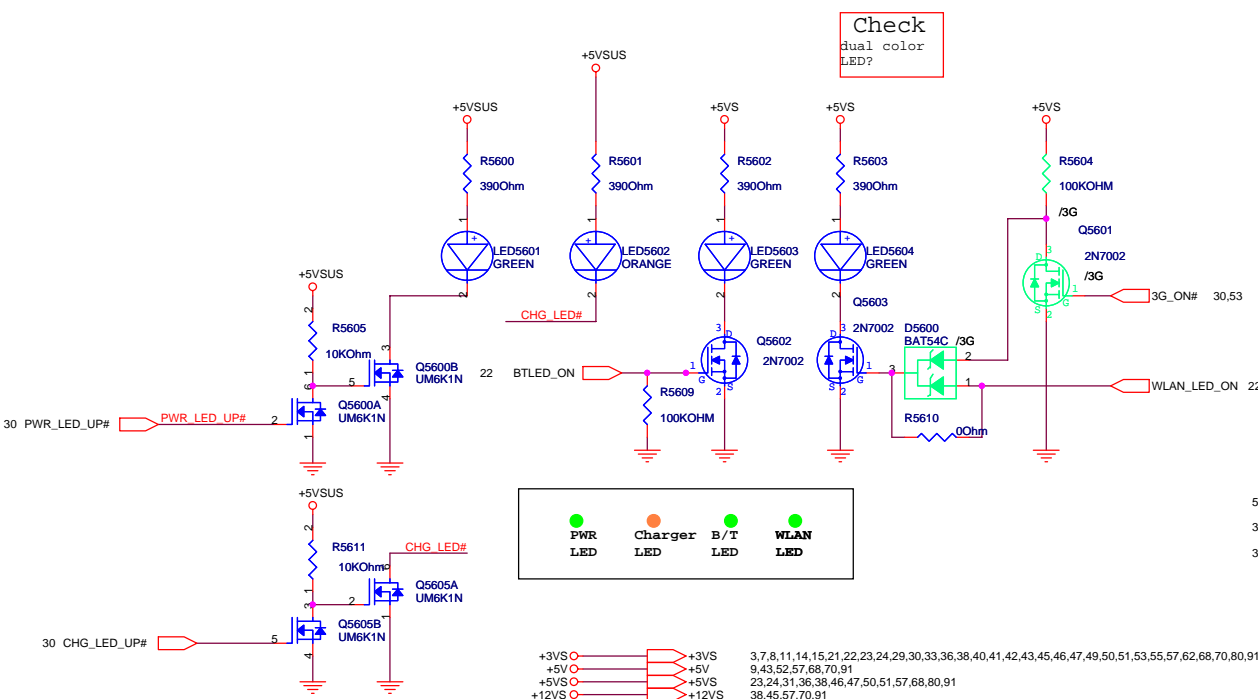
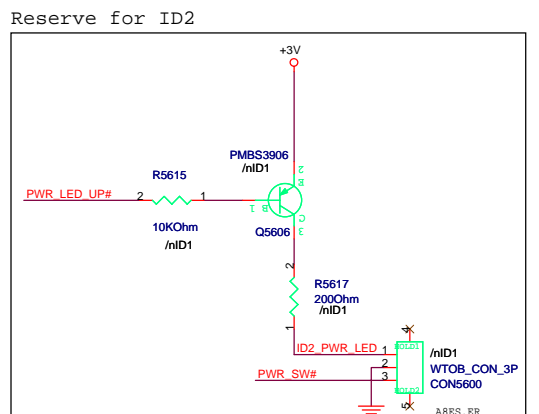
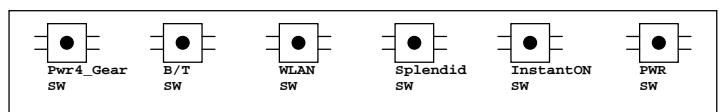
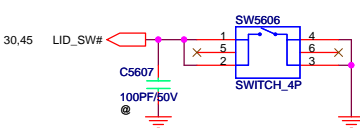
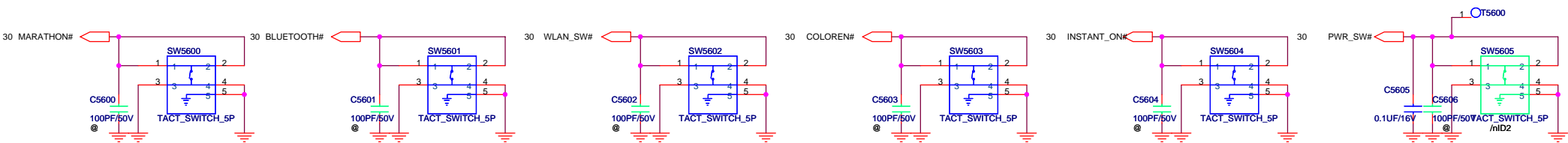


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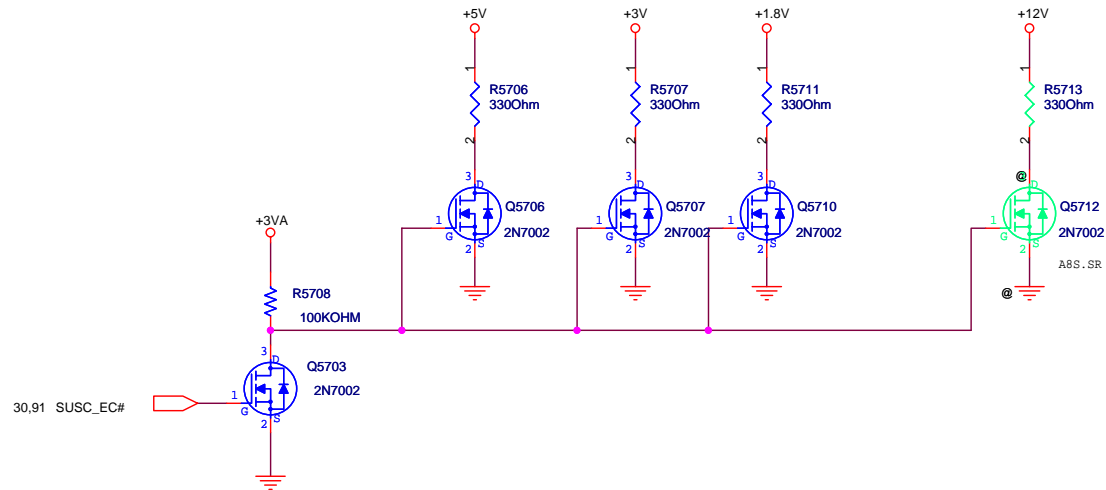
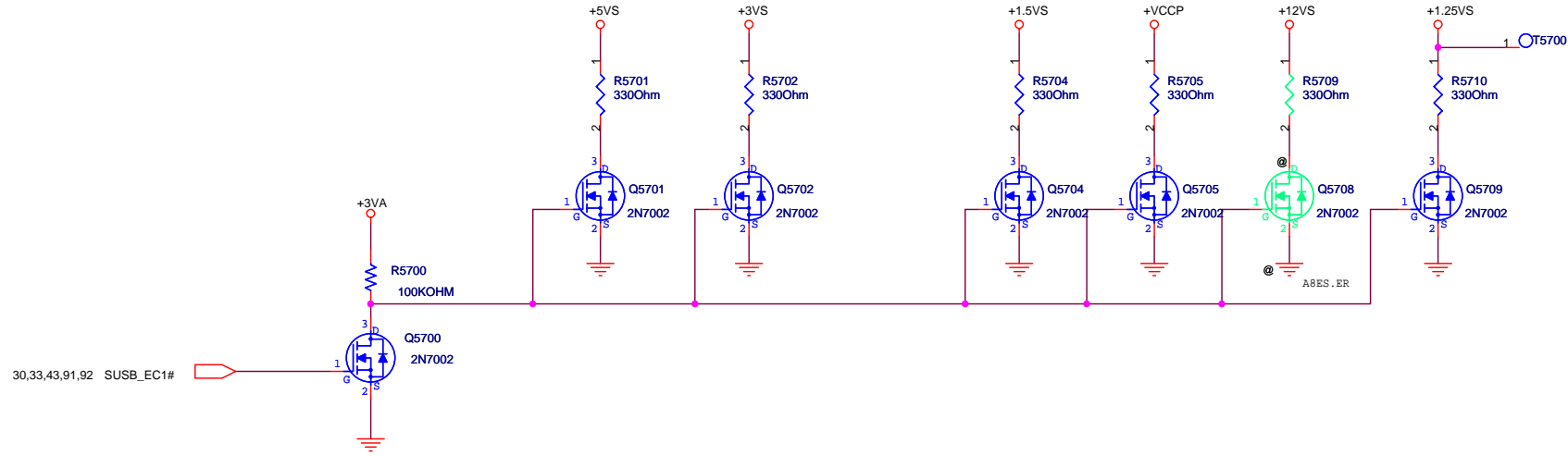
ASUSTeK COMPUTER INC.

Engineer:

Size B	Project Name A8ES	Rev 2.0
Date: Tuesday, January 30, 2007		Sheet 55 of 94



Discharge Circuit



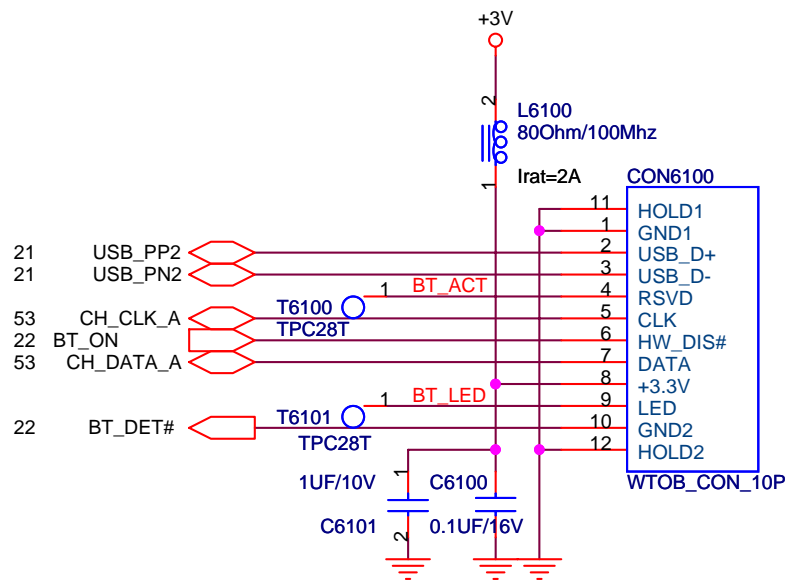
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ASUS		Title : Discharge	
ASUSTeK COMPUTER INC		Engineer:	
Size B	Project Name A8ES		Rev 1.0
Date: Tuesday, January 30, 2007		Sheet 57	of 94

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C				C
B				B
A				A

<Variant Name>

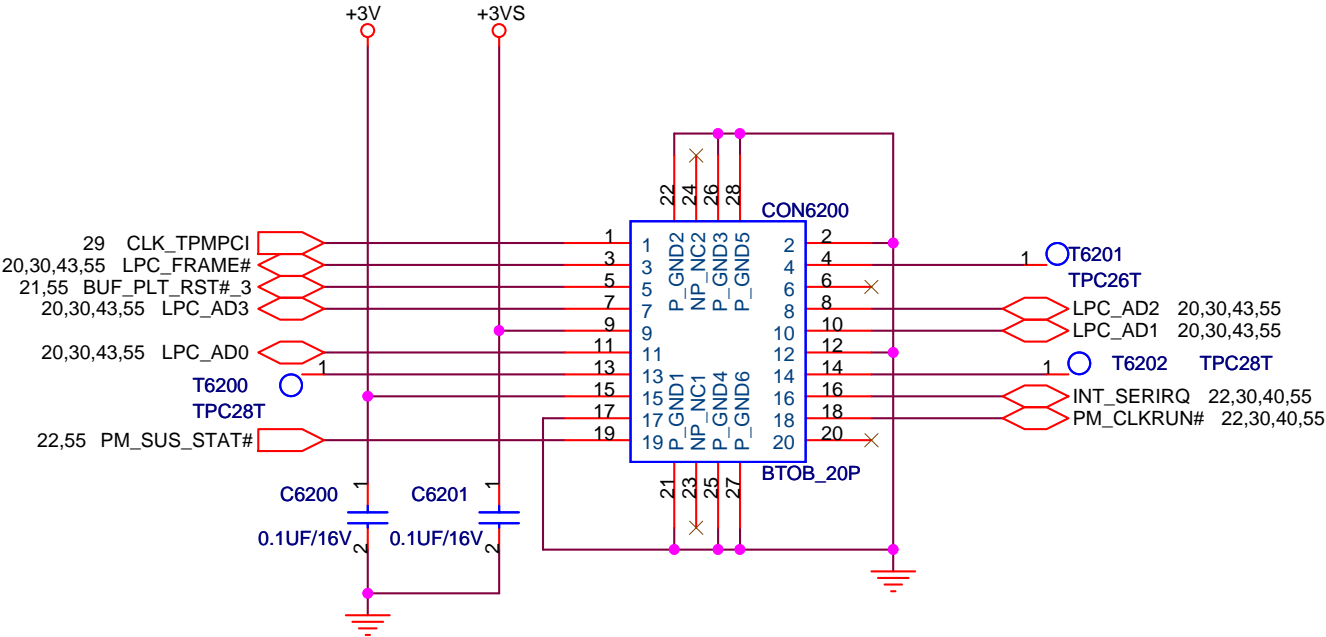
		Title :	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	A8ES		1.0
Date: Wednesday, October 11, 2006		Sheet	of 94




Bluetooth Module CON

ASUS		Title :BT/CAMERA	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 1.0
Date: Thursday, January 25, 2007		Sheet	61 of 94

TPM 1.2 Module



<Variant Name>

		Title :TPM	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 1.0
Date: Thursday, January 25, 2007		Sheet	62 of 94

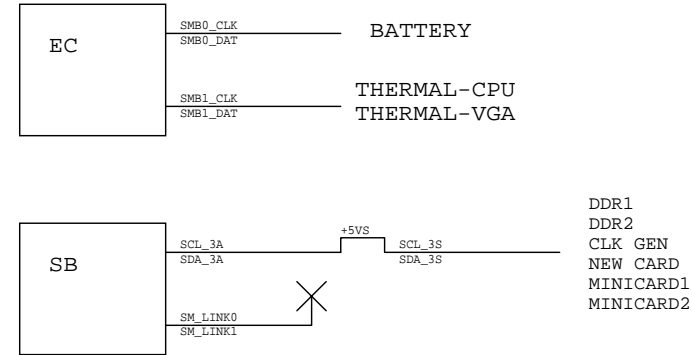
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C				C
B				B
A				A

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	A8ES		0
Date: Wednesday, October 11, 2006		Sheet 63 of 94	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 (Internal)		
CARDBUS	AD19	0	F,E

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0 (low)	
SPD/TS	A0/30
SO-DIMM 1(high)	
SPD/TS	A4/34
G781-1	9A
G781(VGA board)	98

Thermal Sensor (CPU)
SM-Bus Mapping 1001100



BOM option

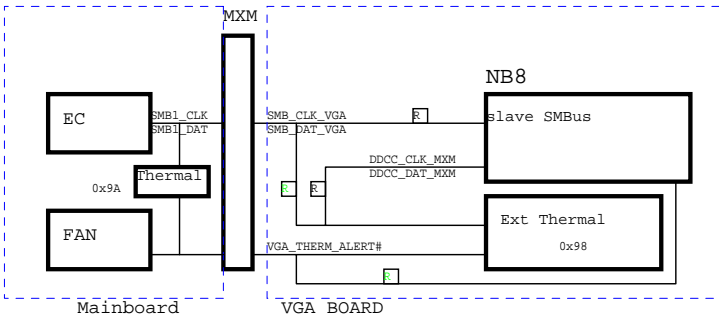
nGM:yellow
nPM:light red
=====

@ : no stuff for all
nGM :no stuff for A8E
nPM :no stuff for A8S
nGM1:no stuff for A8E, A8E/SR mount for debugging A8S in advance
3G :for Windigo, SR mount for debugging
SR :for SR debugging, should be removed or no stuff @ ER

Support ID2:

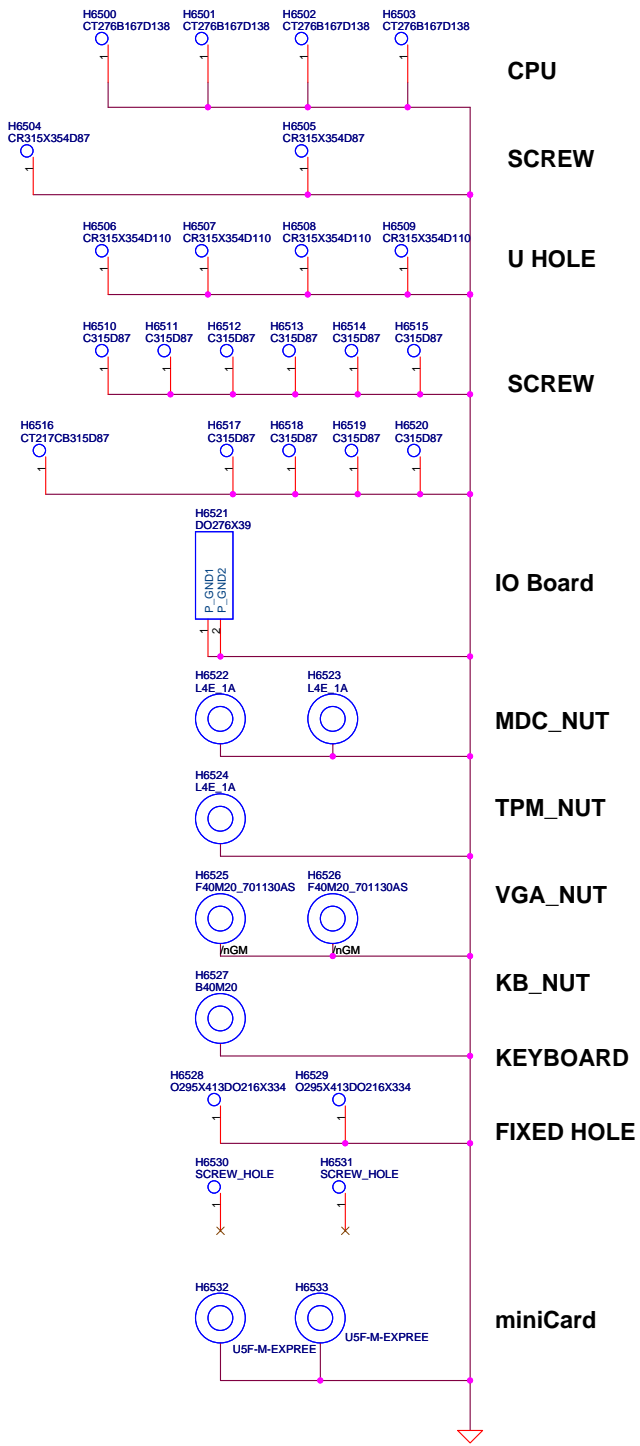
Support ID2:
page 68,Finger print
page 55,IR
Page 56,pwr switch and LED

Thermal block diagram




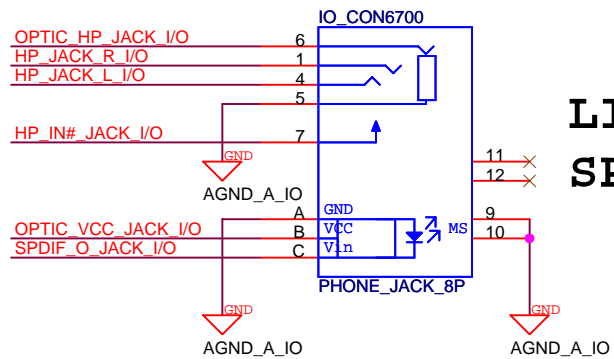
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ASUSTeK COMPUTER INC		Engineer:	
Size B	Project Name A8ES		Rev 1.0
Date: Monday, December 04, 2006		Sheet 64	of 94

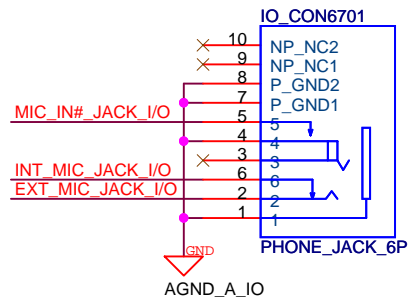


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Size	Document Number	Rev
CustomW2S		1.1
Date:	Tuesday, December 26, 2006	Sheet 65 of 94

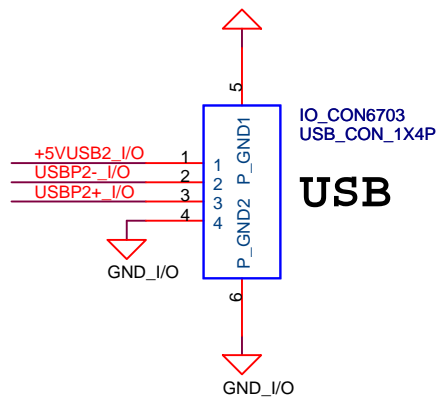
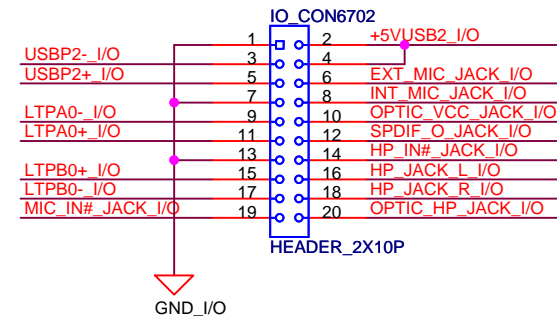
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Size	Project Name		Rev
B	A8ES		0
Date: Wednesday, October 11, 2006		Sheet 66 of 94	



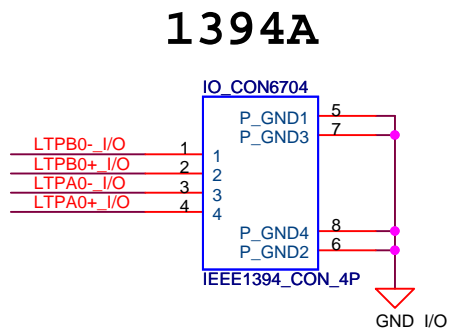
LINE_OUT SPDIF



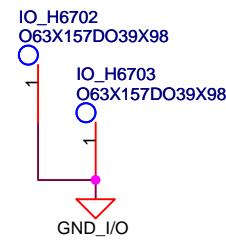
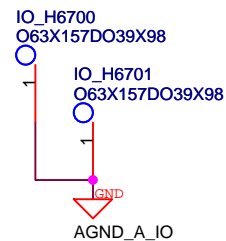
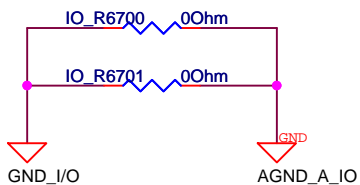
MIC



USB



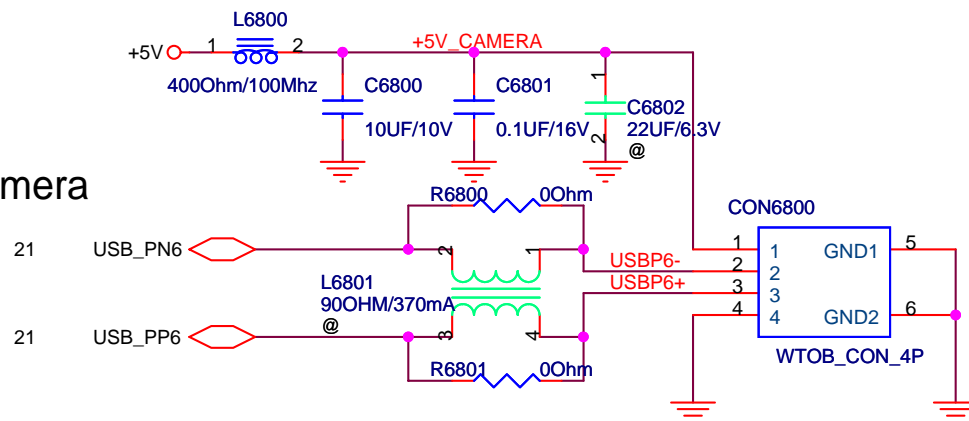
1394A



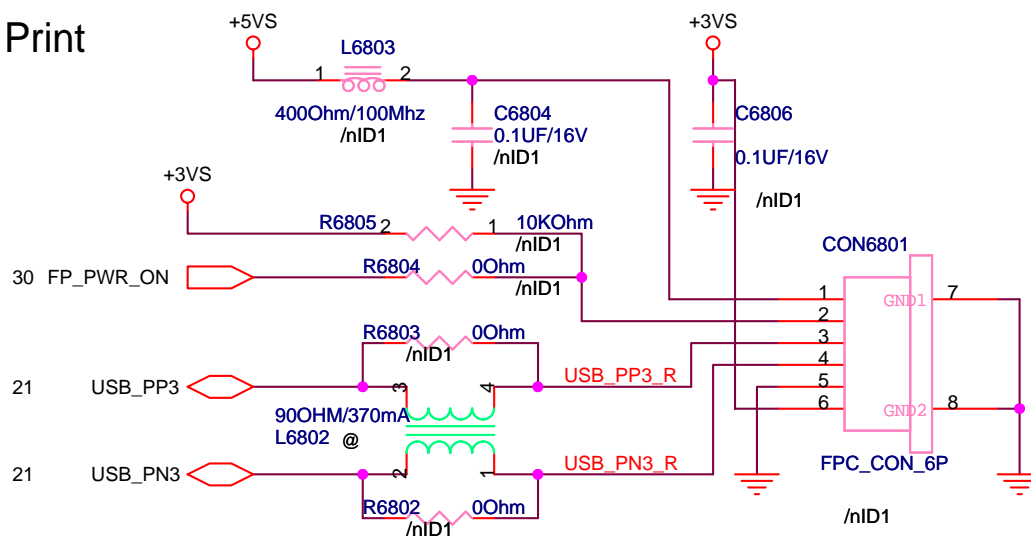
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ASUS		Title :SUB_PCB	
ASUSTeK COMPUTER INC		Engineer:	
Size A4	Project Name A8ES		Rev 1.0
Date: Tuesday, January 30, 2007		Sheet	67 of 94

Camera




Finger Print

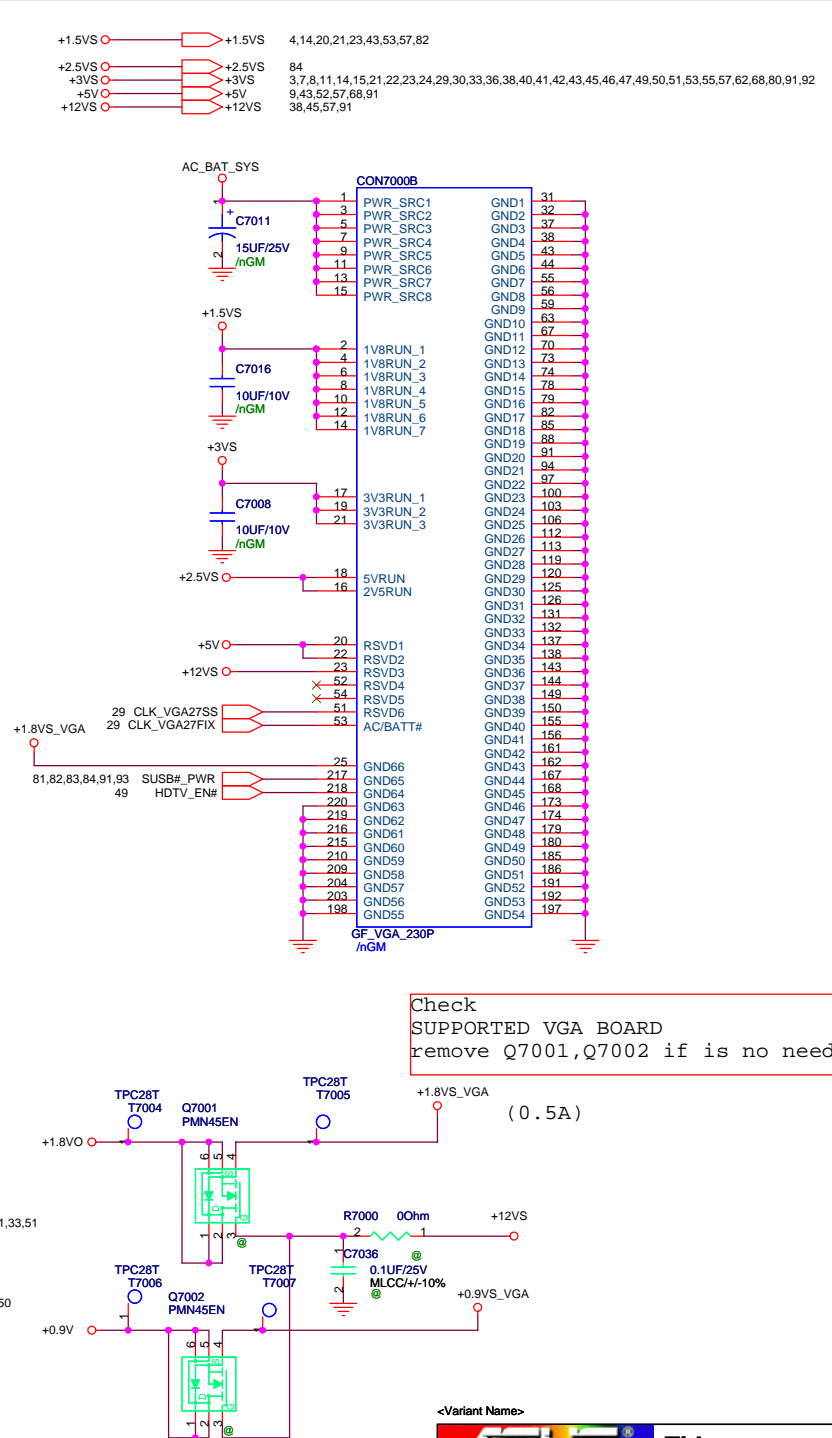
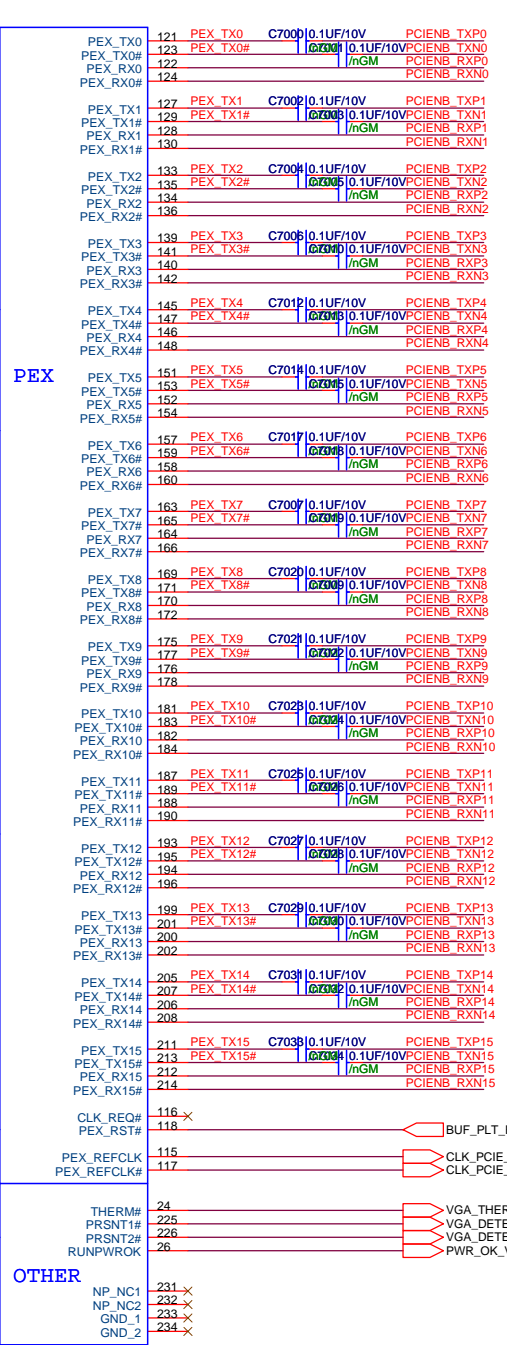
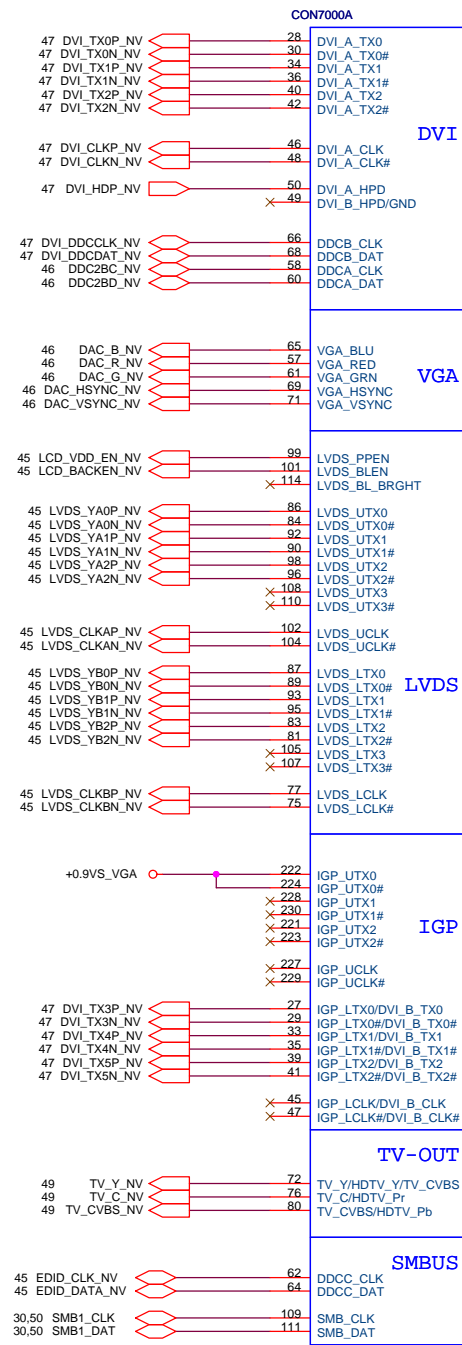


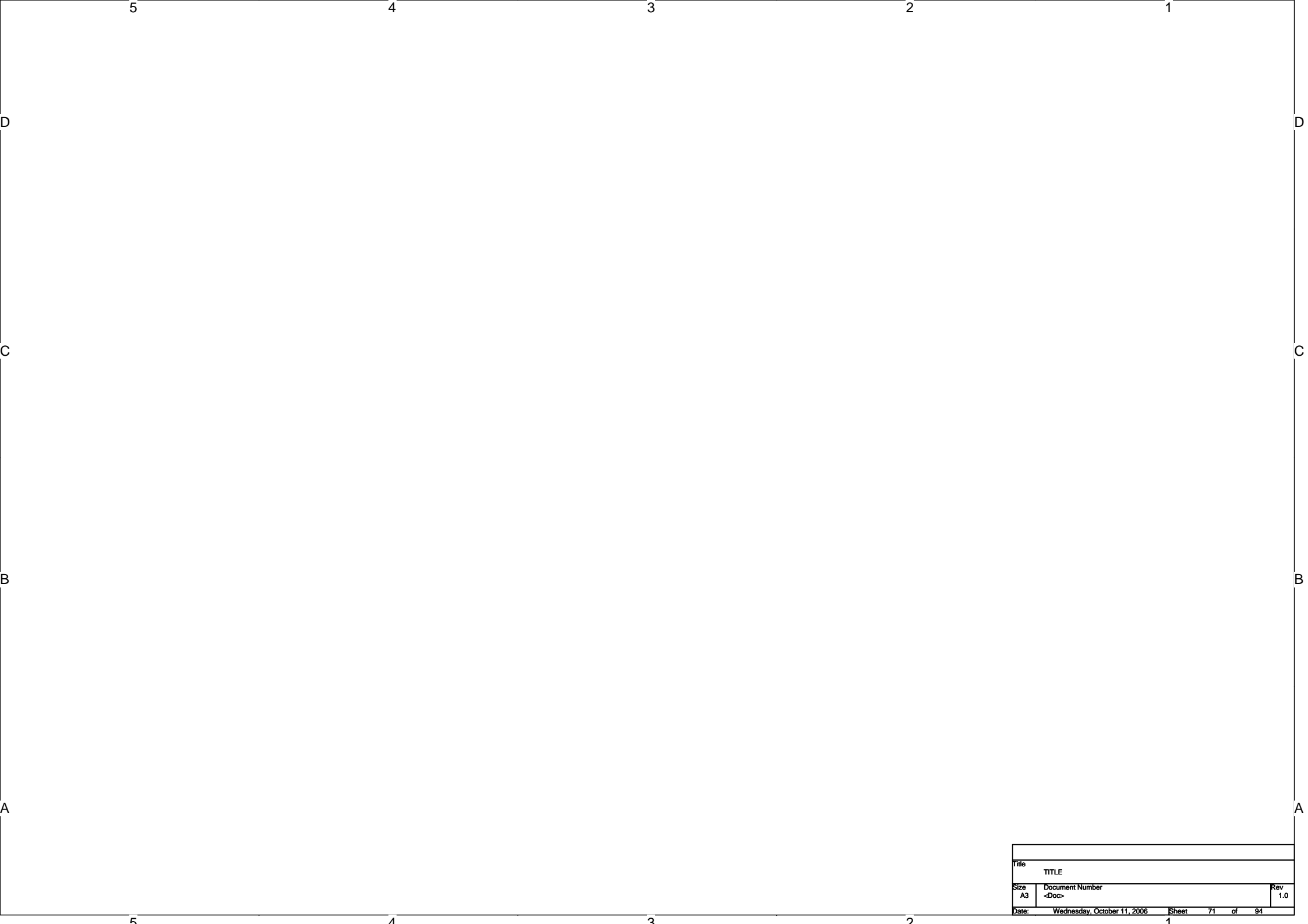
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ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 1.0
Date: Thursday, January 25, 2007		Sheet 68 of 94	

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C				C
B				B
A				A

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	A8ES		0
Date: Wednesday, October 11, 2006		Sheet 69 of 94	

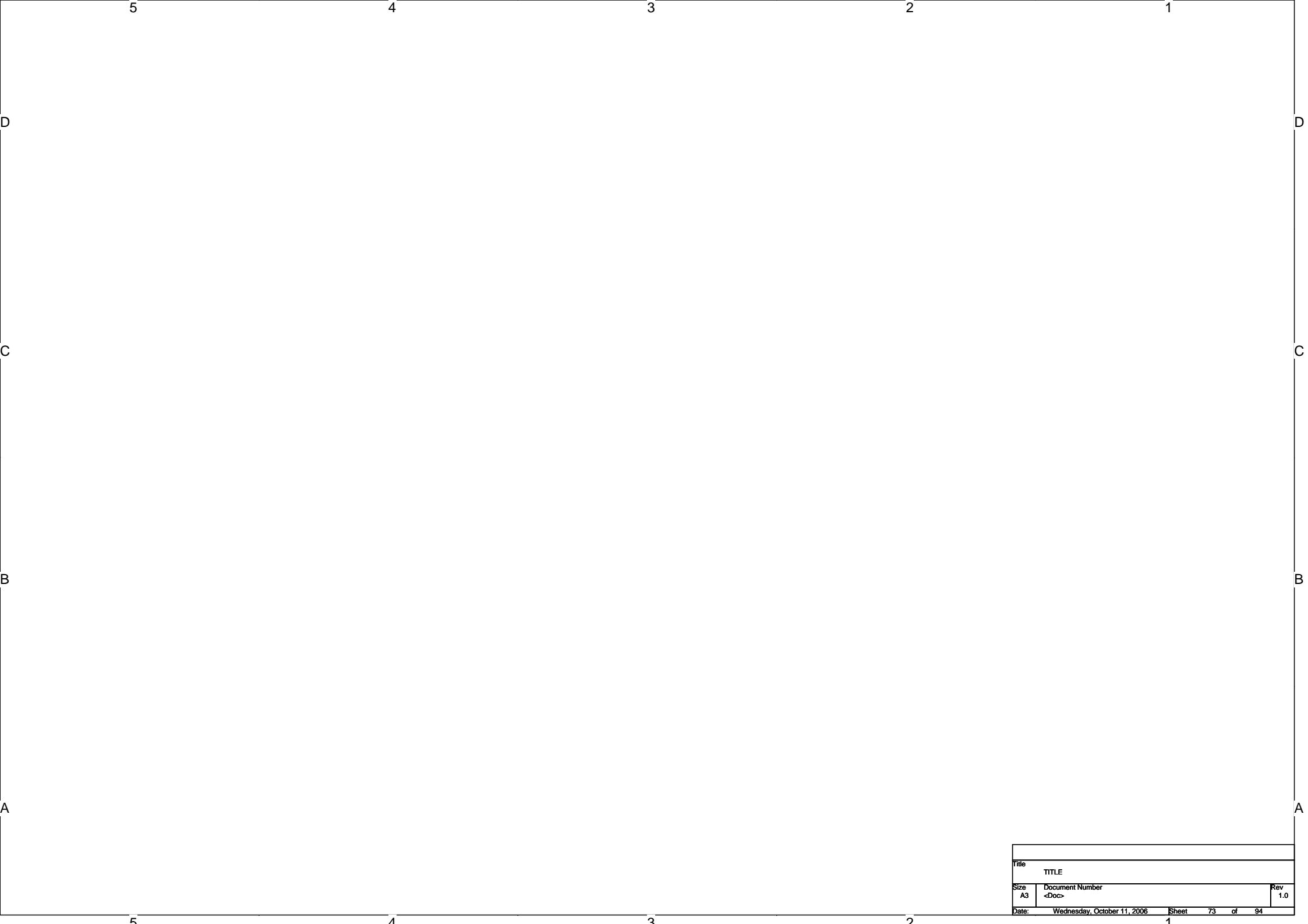




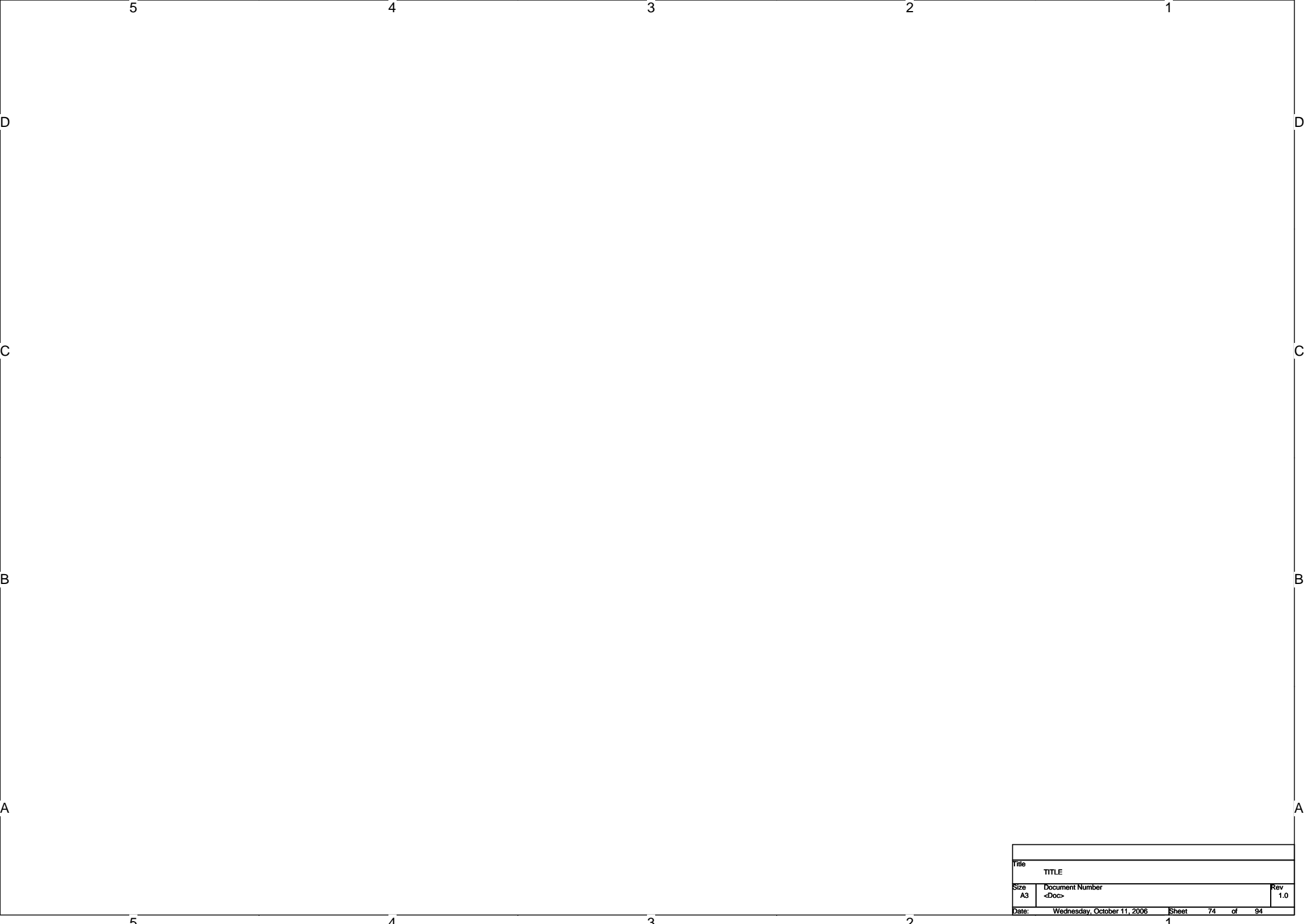
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Date:	Wednesday, October 11, 2006		Sheet 71 of 94



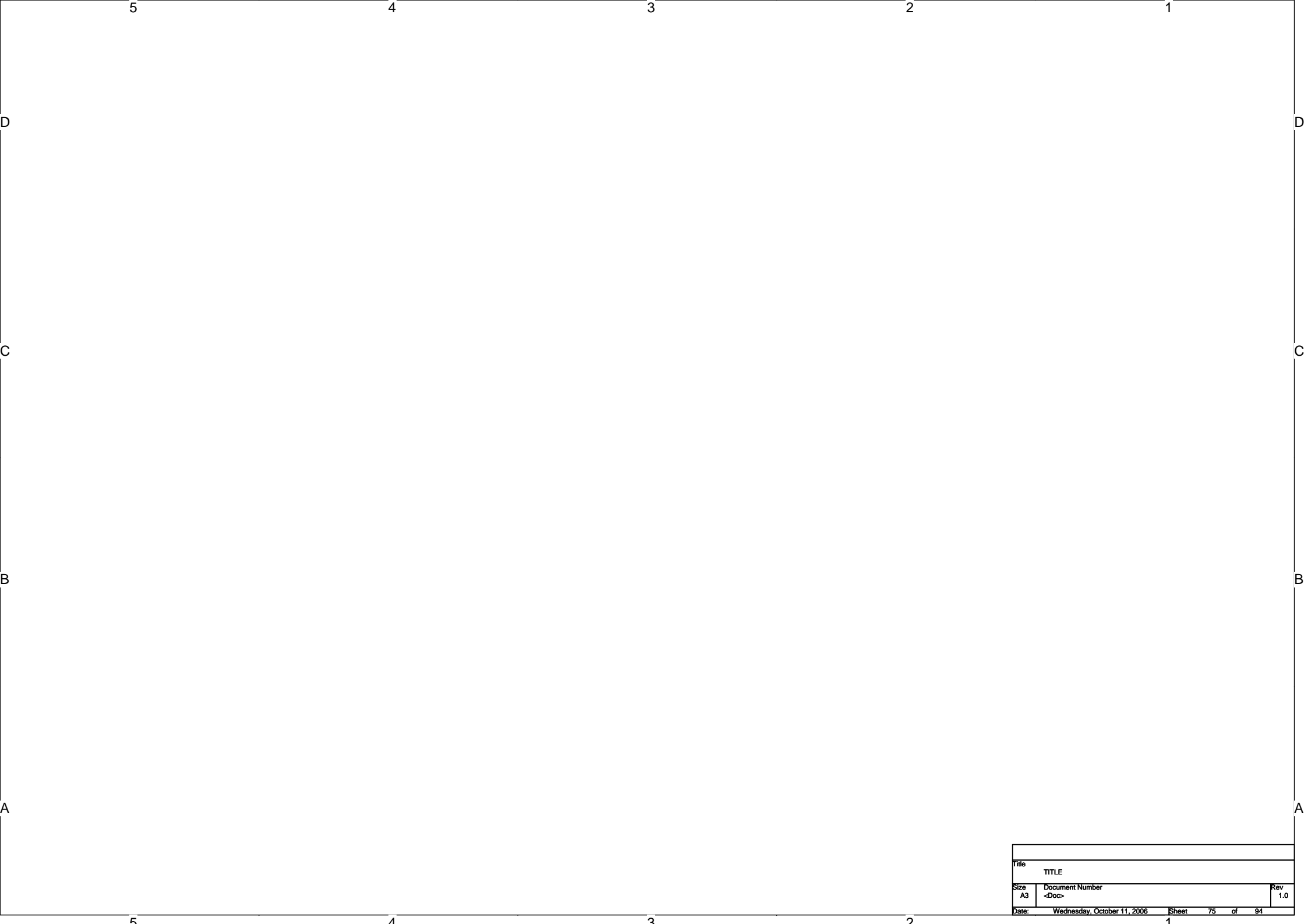
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Date:	Wednesday, October 11, 2006		Sheet 72 of 94



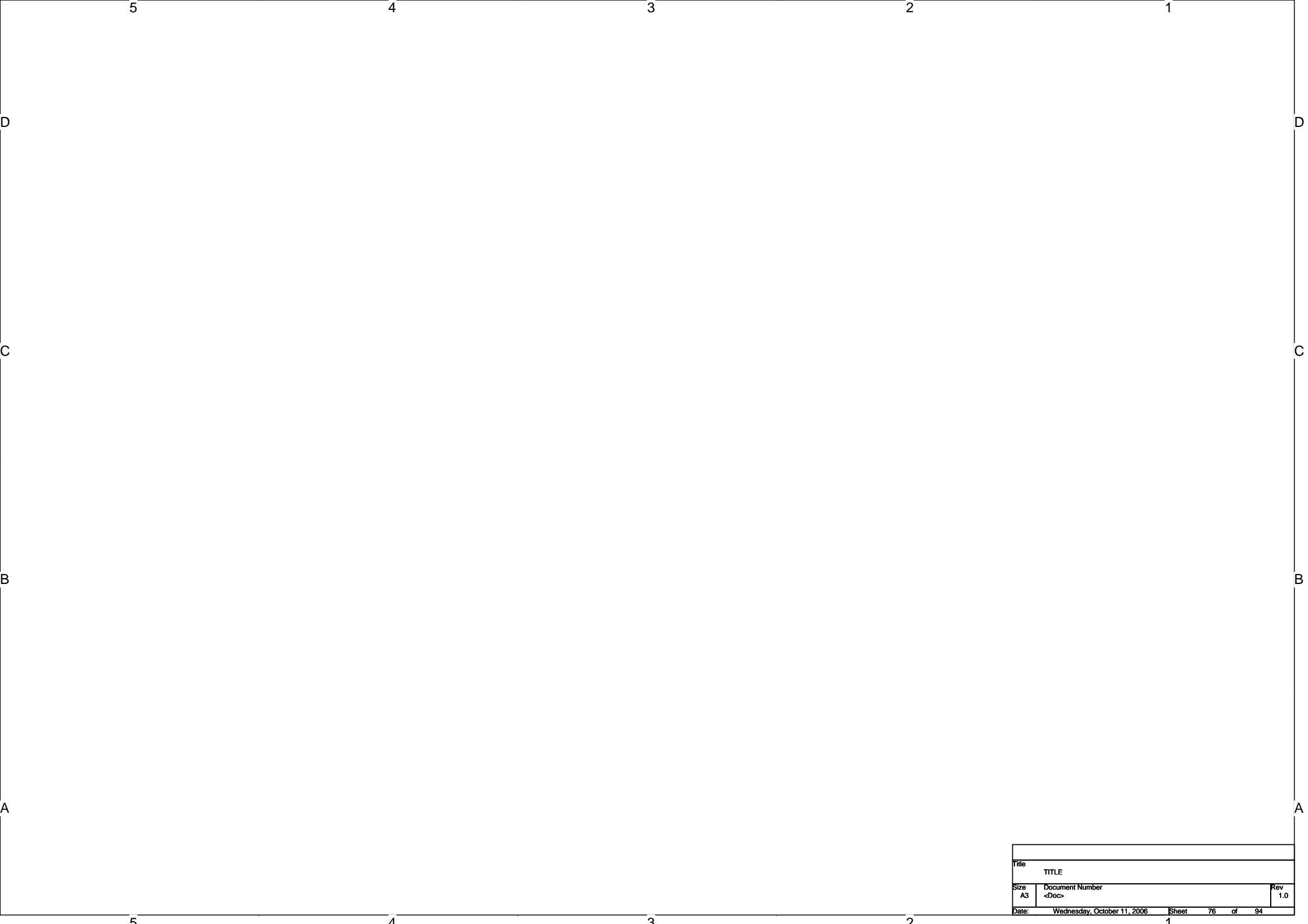
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Date:	Wednesday, October 11, 2006		Sheet 73 of 94



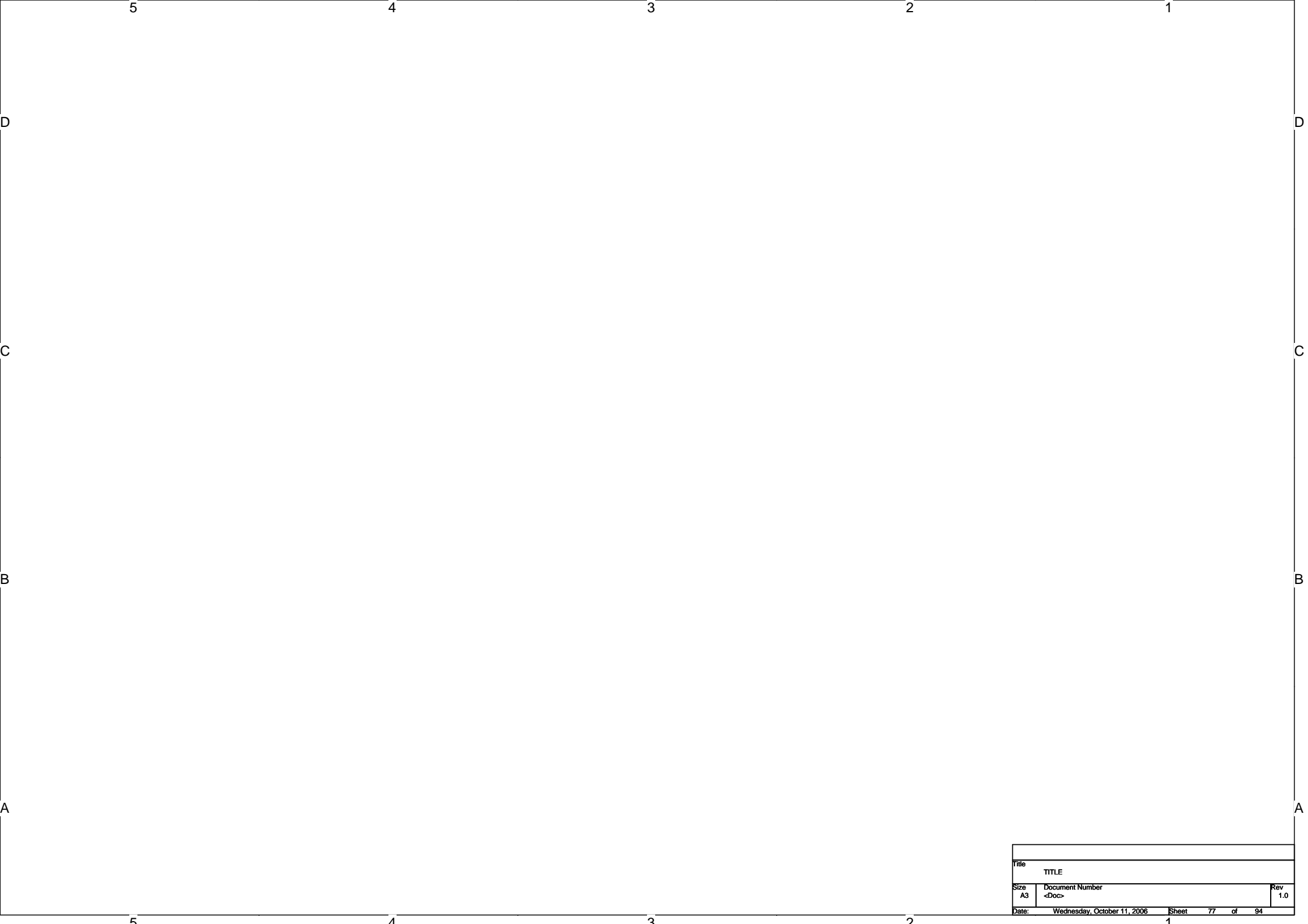
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Date:	Wednesday, October 11, 2006		Sheet 74 of 94




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A3	<Doc>		1.0
Date:	Wednesday, October 11, 2006		Sheet 75 of 94



Title			
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A3	<Doc>		1.0
Date:	Wednesday, October 11, 2006		Sheet 76 of 94



Title			
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A3	<Doc>		1.0
Date:	Wednesday, October 11, 2006		Sheet 77 of 94

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
B	A8ES		0
Date: Wednesday, October 11, 2006		Sheet	78 of 94

W2S

Change Note:
EE :

- 1. 965PM pin defined modification, C48/D47/BJ29/BE24 from RSVD pin to LVDSA_DATA#_3 / LVDSA_DATA_3 / SA_MA_14 / SB_MA_14
- 2. CE46 / CE25 --> 11G08D210791
- 3. Rst button circuit
- 4. BT_SW pull-high to different plane issue.
- 5. Remove RN3104
- 6. VTT_REF reserve in S3.
- 7. VTT stop in S3.
- 8. CIR PME# function.


Layout :

- 1. CPU side, per GND pin within per Via, don't share vias.
- 2. 0.9V_VTT_REF trace width.
- 3. single end trace width more than 3.5mil

SMT :

- 1. 開鋼板JP1, JP2

<Variant Name>



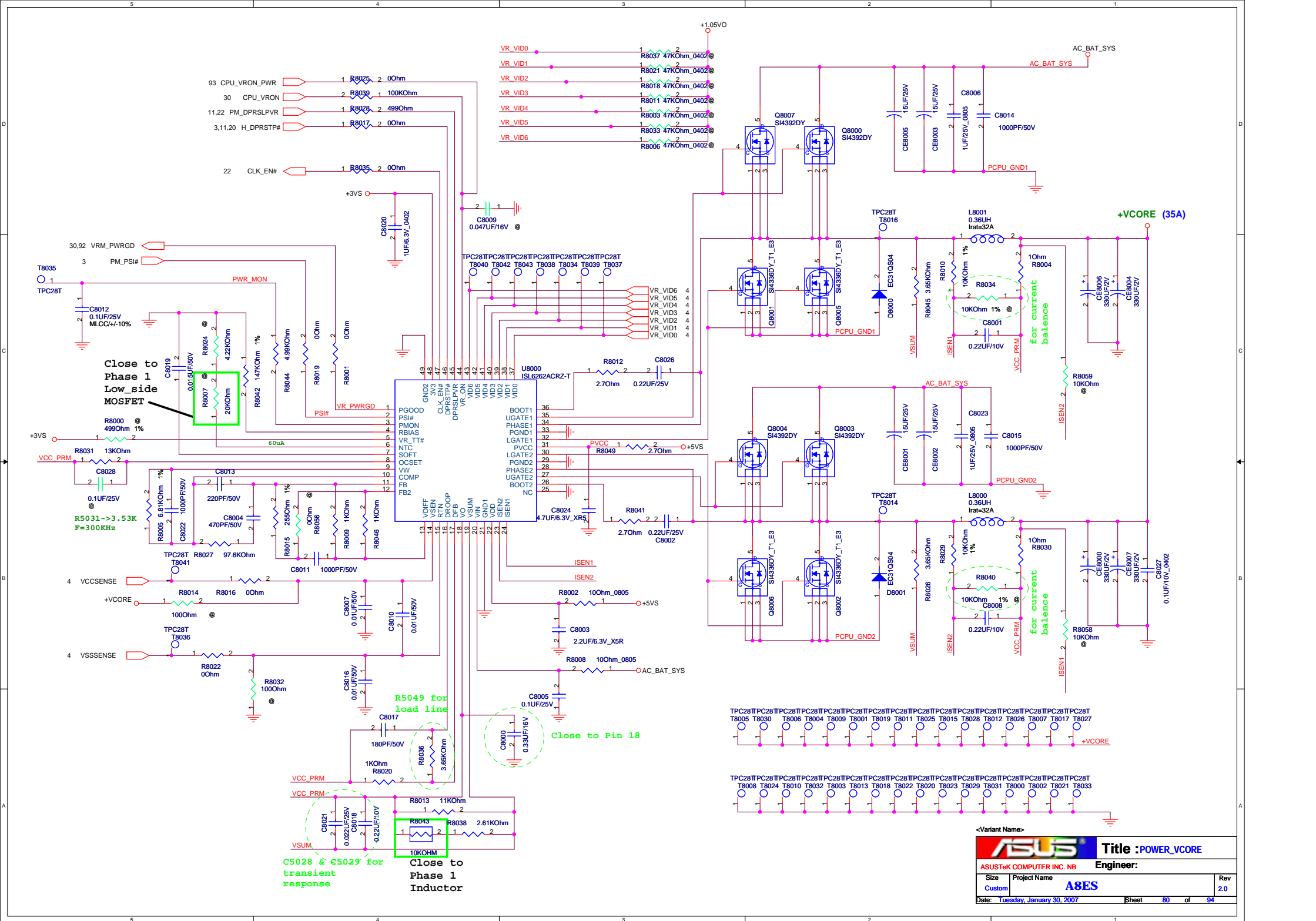
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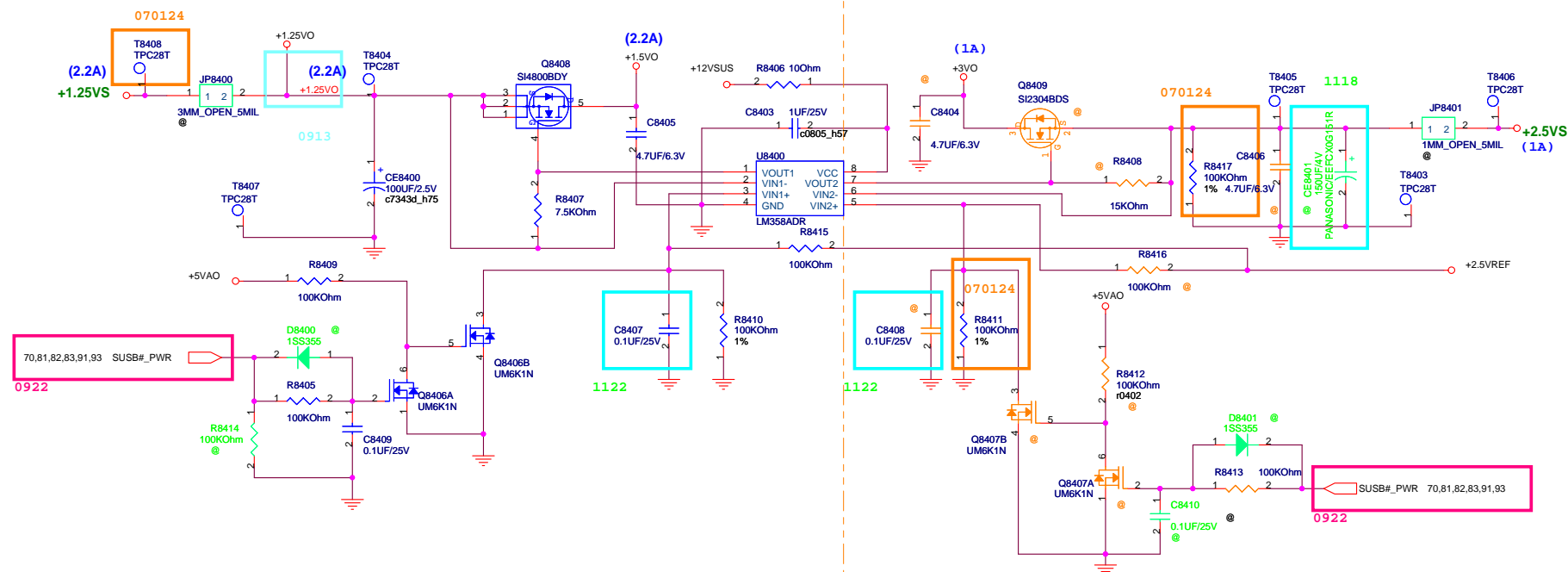
ASUSTeK COMPUTER INC

Engineer:

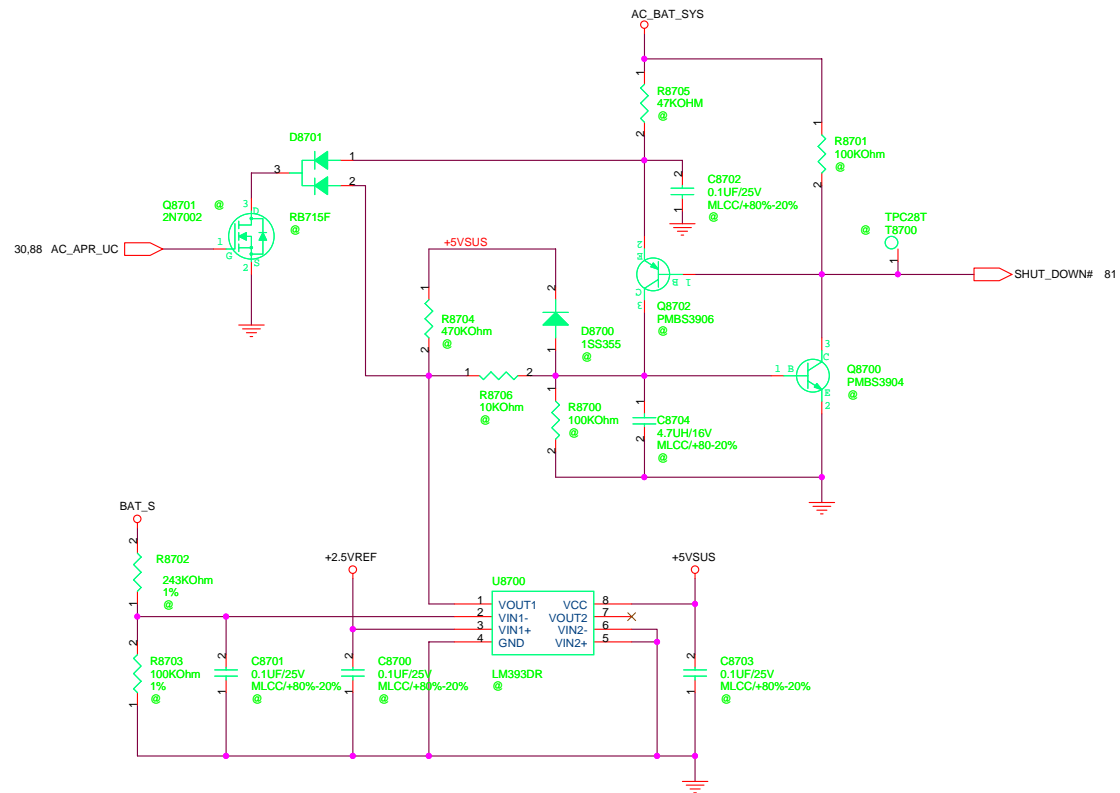
Size	Project Name	Rev
Custom	A8ES	1.0

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D				D
C				C
B				B
A				A
5	4	3	2	1



<Variant Name>

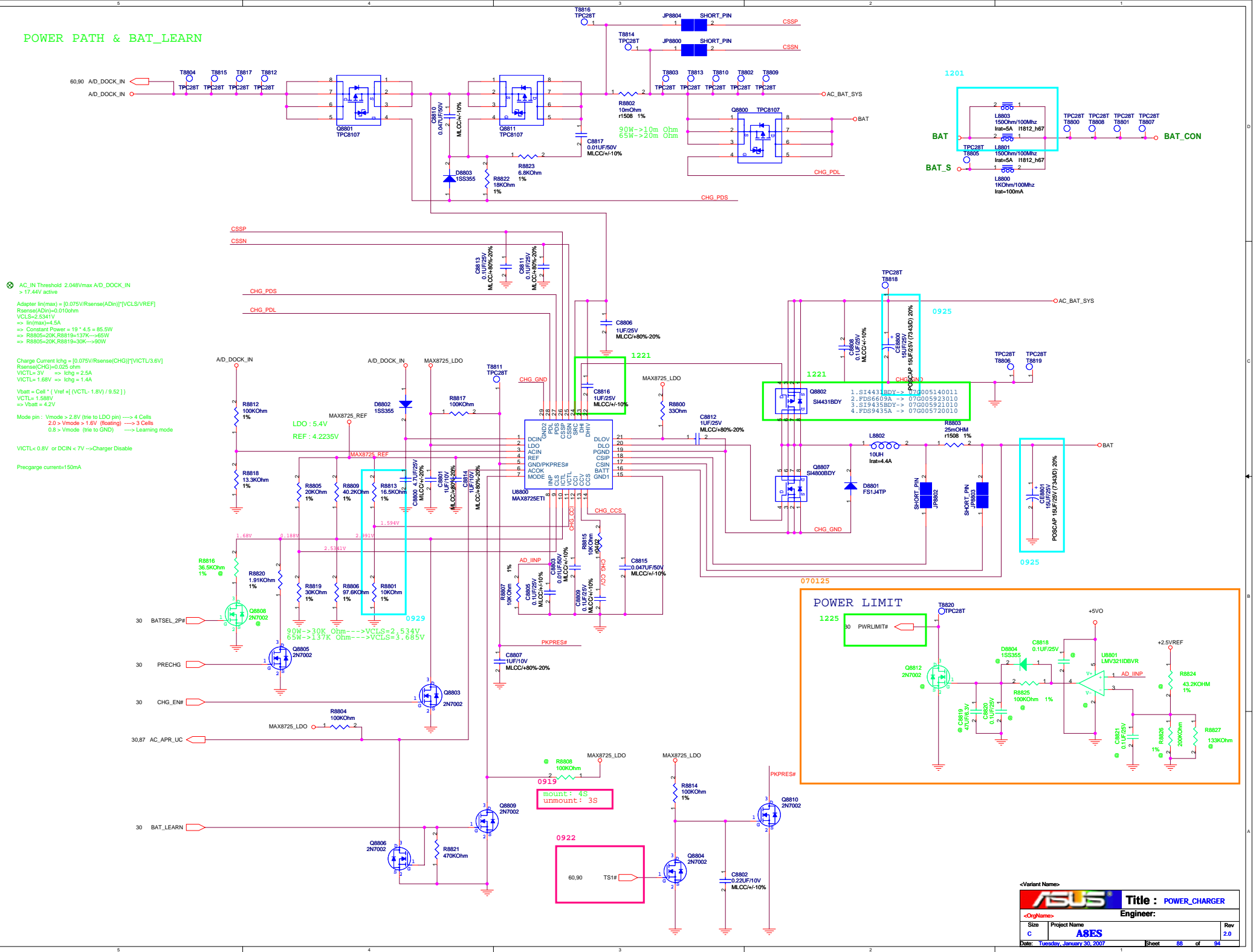


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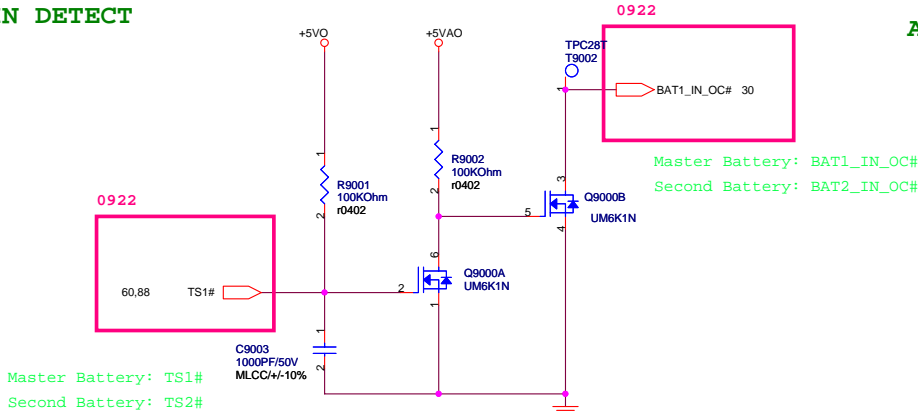
Engineer:

Size Custom	Project Name A8ES	Rev 2.0
Date: Tuesday, January 30, 2007		Sheet 87 of 94

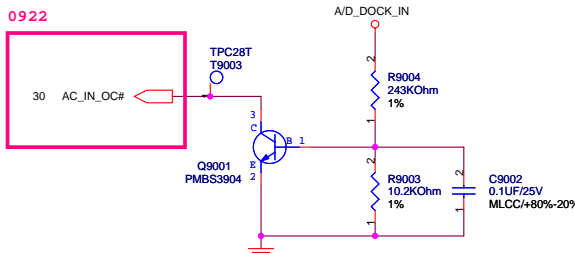
POWER PATH & BAT_LEARN



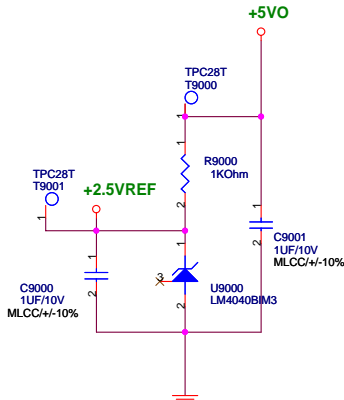
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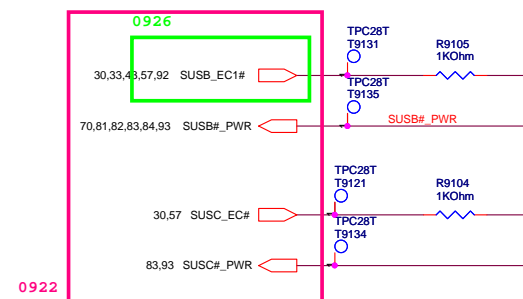
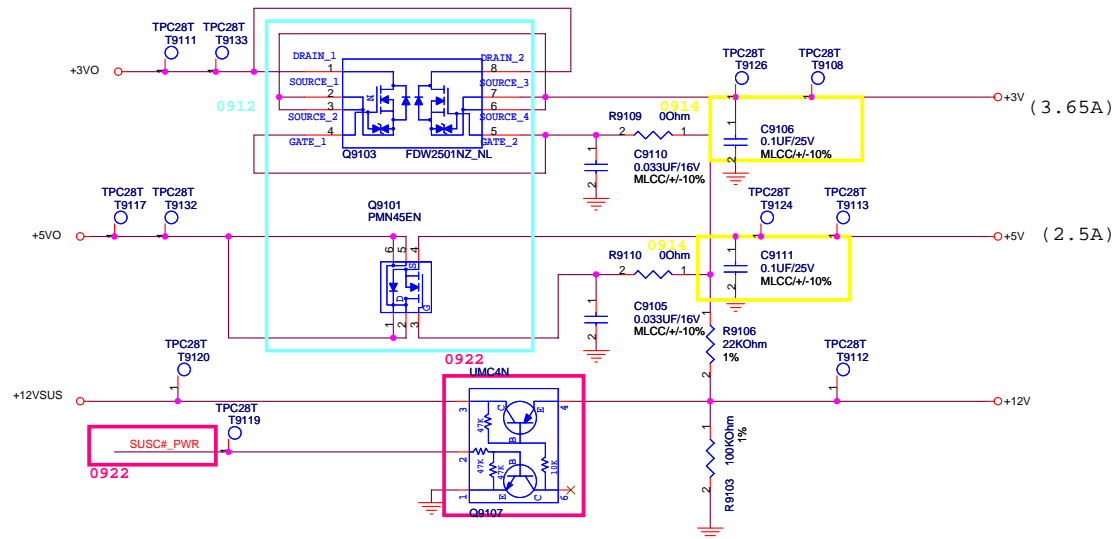
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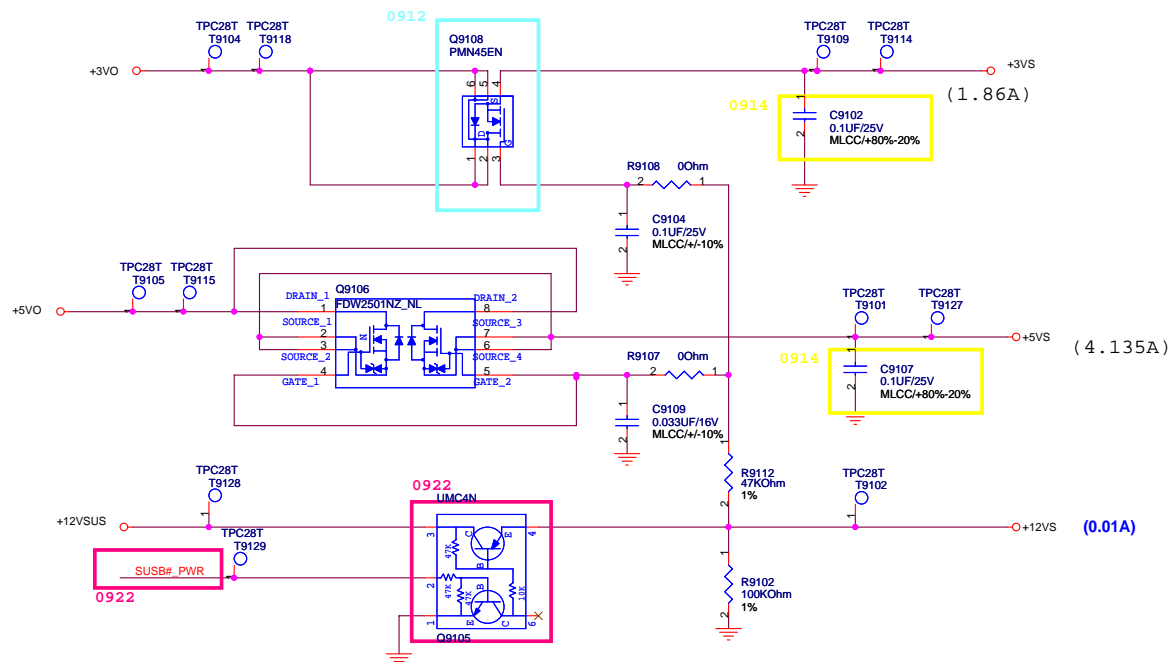
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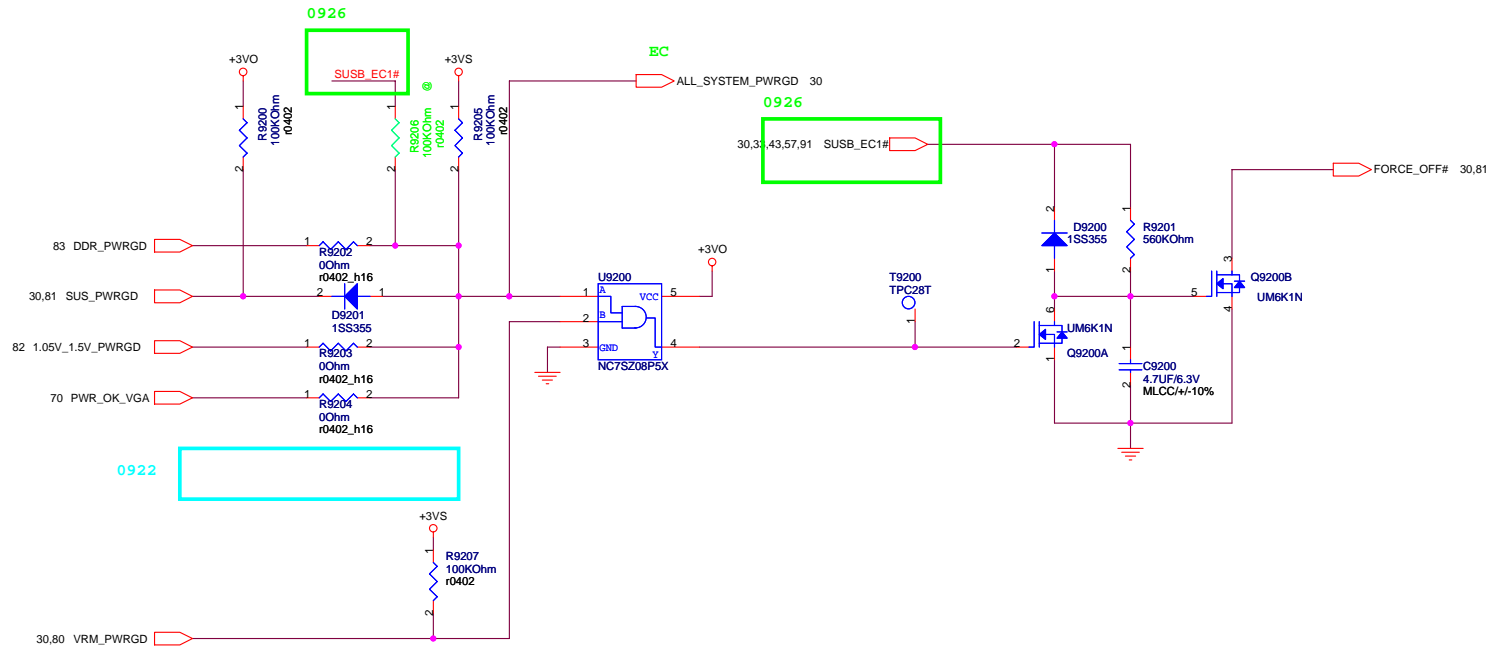
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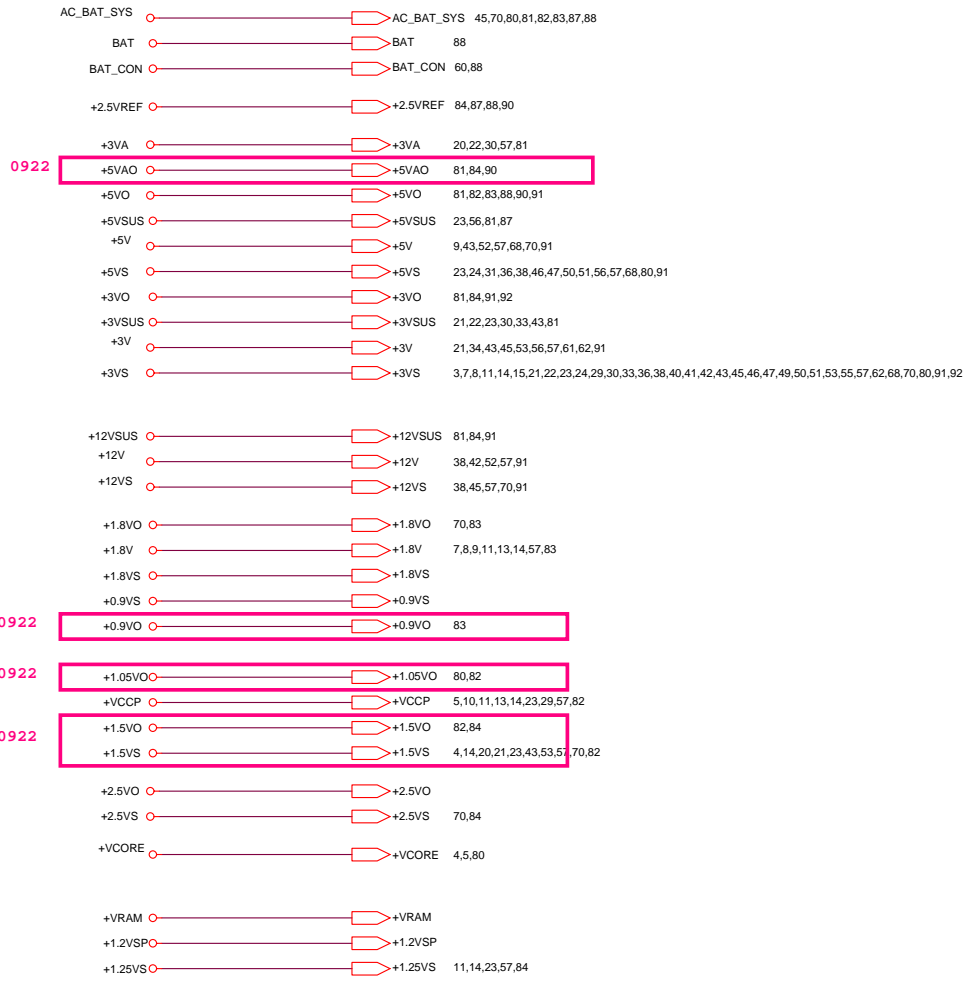


POWER GOOD DETECTOR



<Variant Name>

ASUS		Title : POWER_PROTECT	
<OrgName>		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	2.0	
Date: Thursday, January 25, 2007		Sheet	92 of 94



FOR POWER TEST

