

Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_PM+ICH9-M core logic

2009-02-13

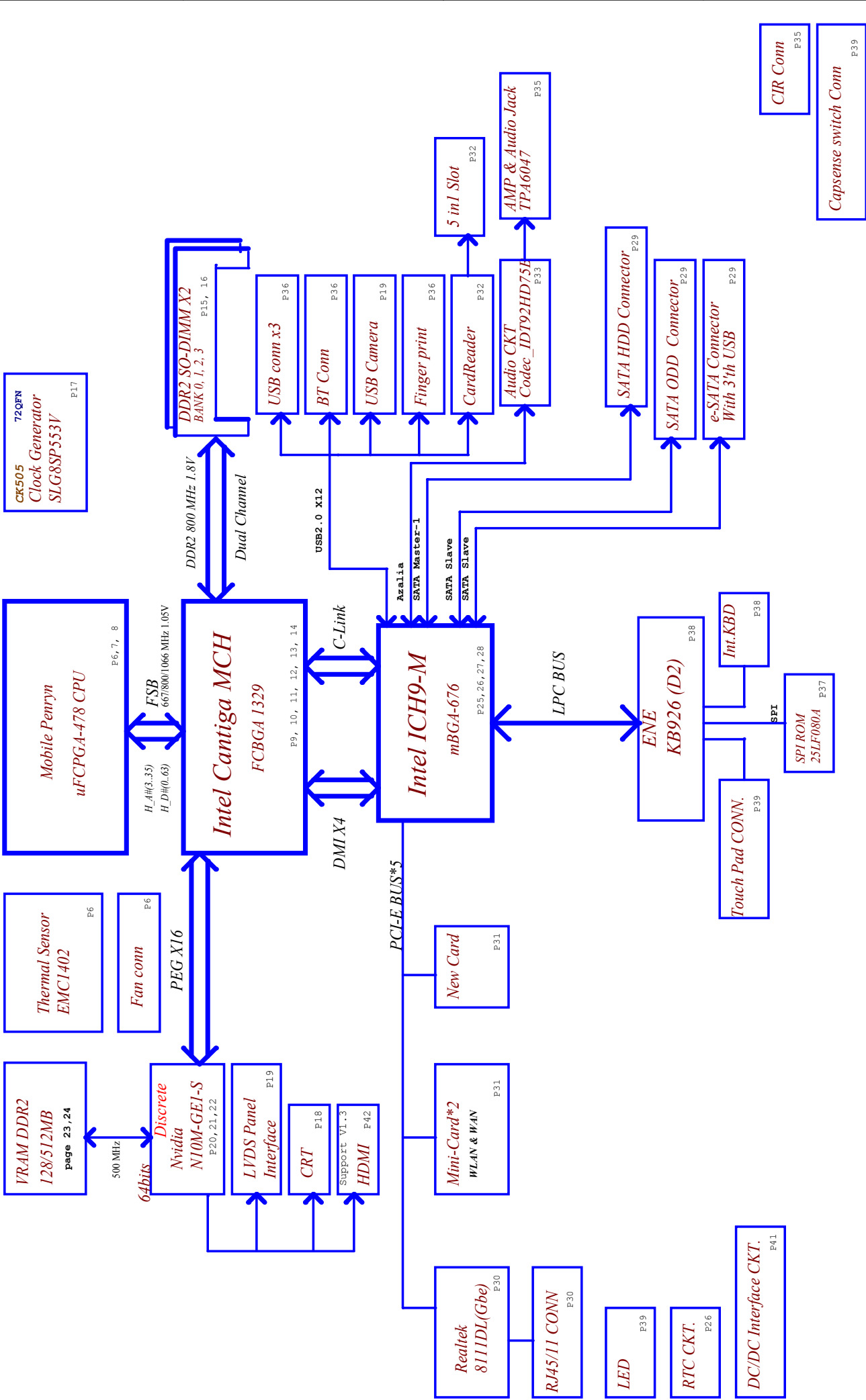
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	產出日期	
	解密日期	

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Cover Sheet



Voltage Rails

X MEANS
OFF

O MEANS ON

power plane	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS +NWDD +PCIE
State				
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM

FRU	R1	SA00002JJ80	NB
	R3	SA00002JJ80	NB
FRU	R1	SA00002JJH50	SB
	R3	SA00002JJH50	SB

Symbol Note :



: means Digital Ground



: means Analog Ground

USB assignment:

USB-0 Right side(with ESATA)

USB-1 Left side

USB-2 Left side

USB-3 Dock

USB-4 Camera

USB-5 WLAN

USB-6 Bluetooth

USB-7 Finger Printer

USB-8 MiniCard(WWAN/TX)

USB-9 Express card

USB-10 X

USB-11 X

PCIe assignment:

PCIe-1 TV tuner/WWAN/Robeson

PCIe-2 X

PCIe-3 WLAN

PCIe-4 GLAN (Marvell)

PCIe-6 New Card

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	Sensor board	N10M Thermal Sensor	N10M	G-sensor
/												
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	V	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	V	V	X
ICH_SMBCLK ICH_SMBDATA	IC9H	X	X	X	X	V	V	V	X	X	X	V

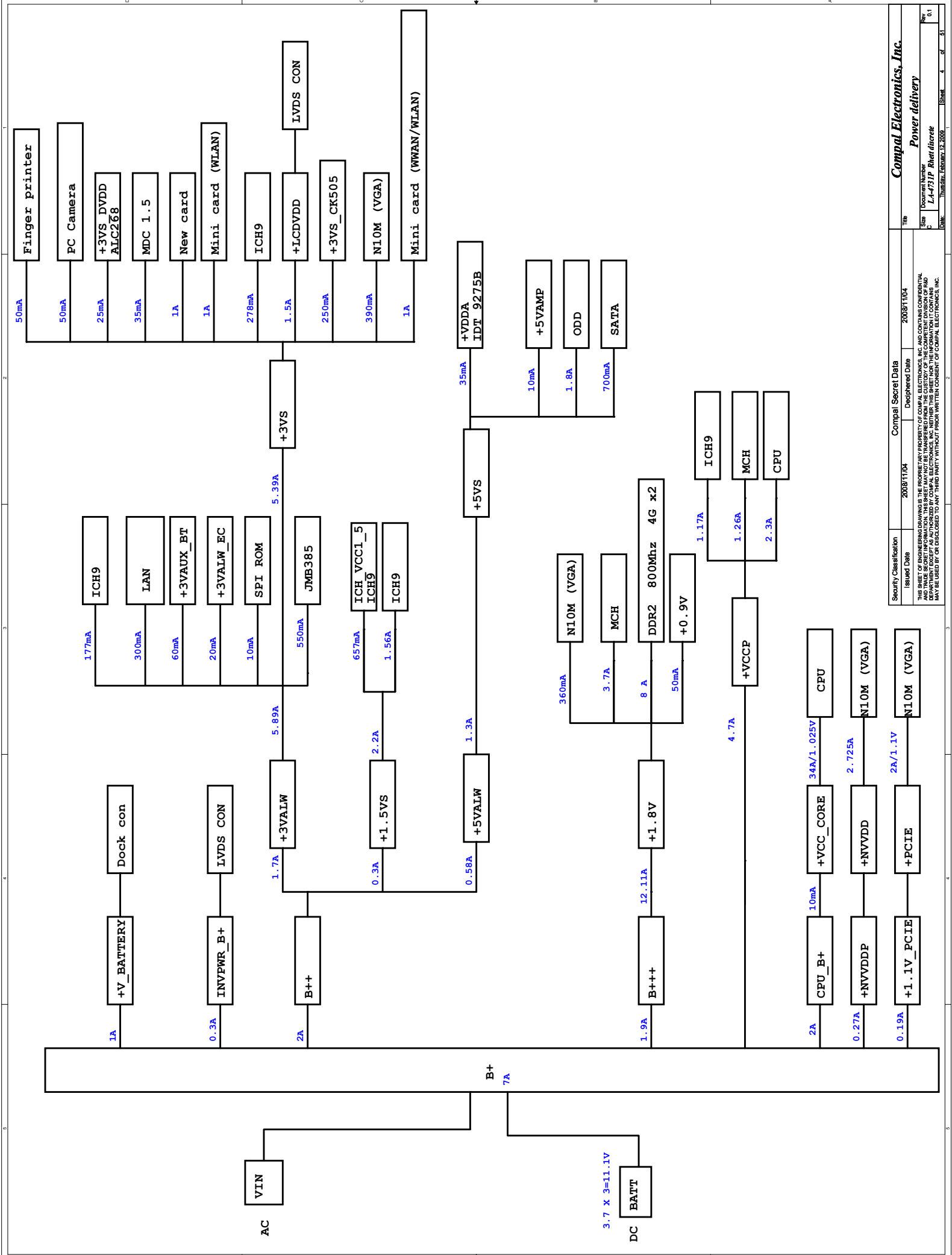
NB9M SMBUS Control Table

	SOURCE	LVDS	CRT	HDMI	HDCP
DOC2_DATA	N10M	V	X	X	X
DOC2_CLK	N10M	X	V	X	X
3VDDGDA	N10M	X			
3VDDCCL	N10M	X			
HDMIDAT_VGA	N10M	X	X	V	X
HDMICLK_VGA	N10M	X	X	X	X
HDCP_SDA	N10M	X	X	X	V
HDCP_SCL	N10M	X	X	X	V

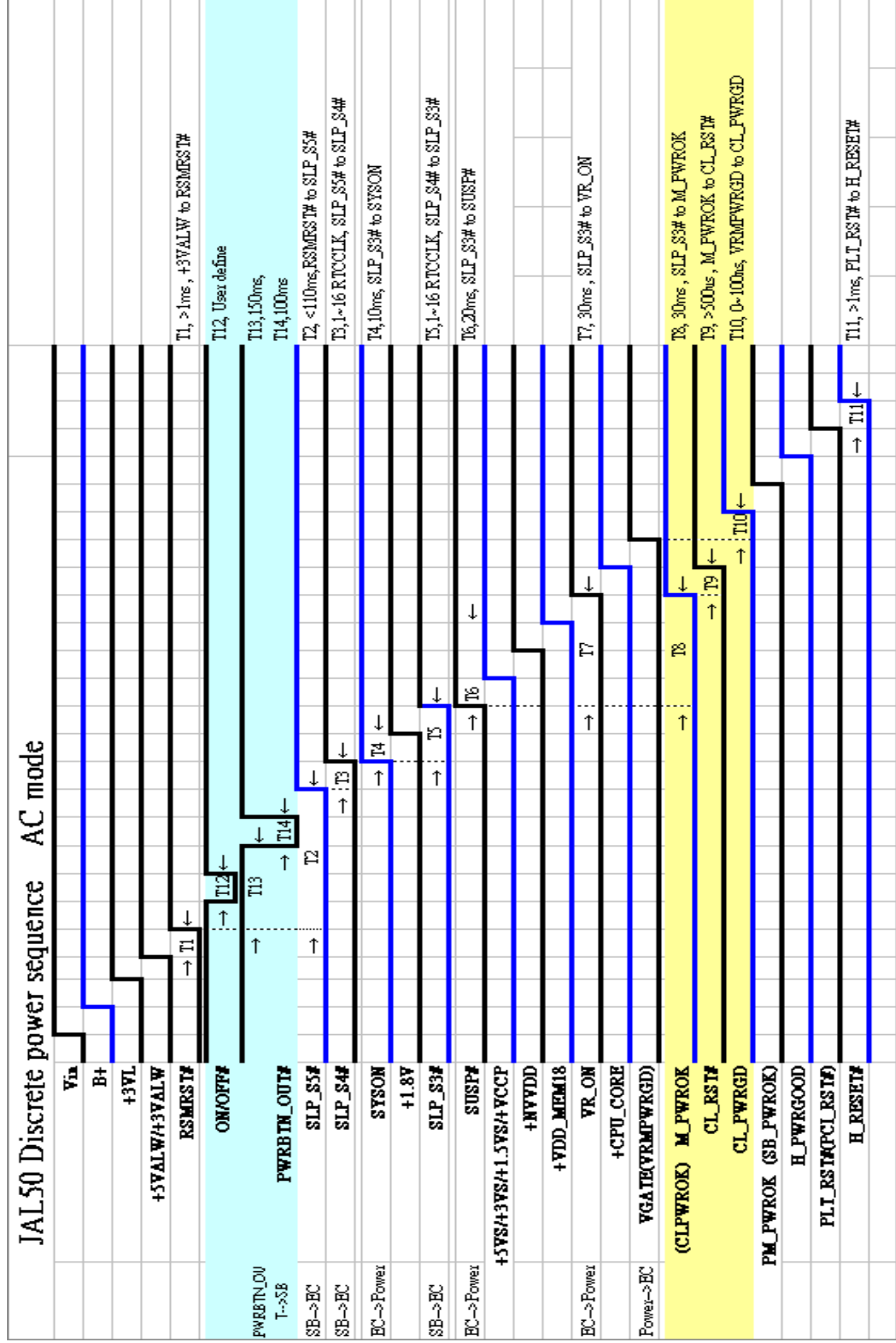
I2C / SMBUS ADDRESSING

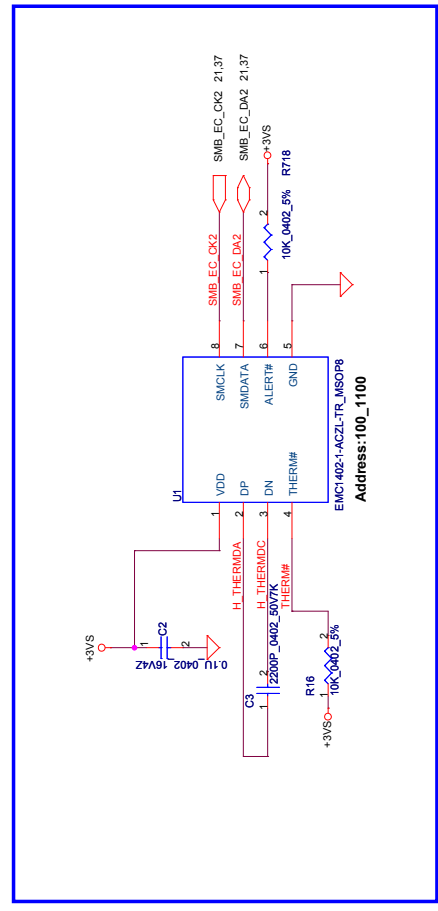
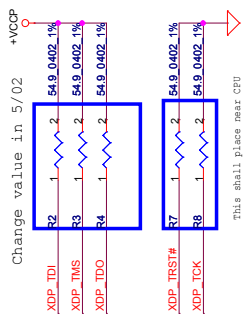
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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Custom		LA-731P Rhetri discrete		0.1				
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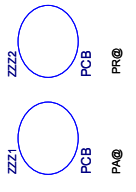
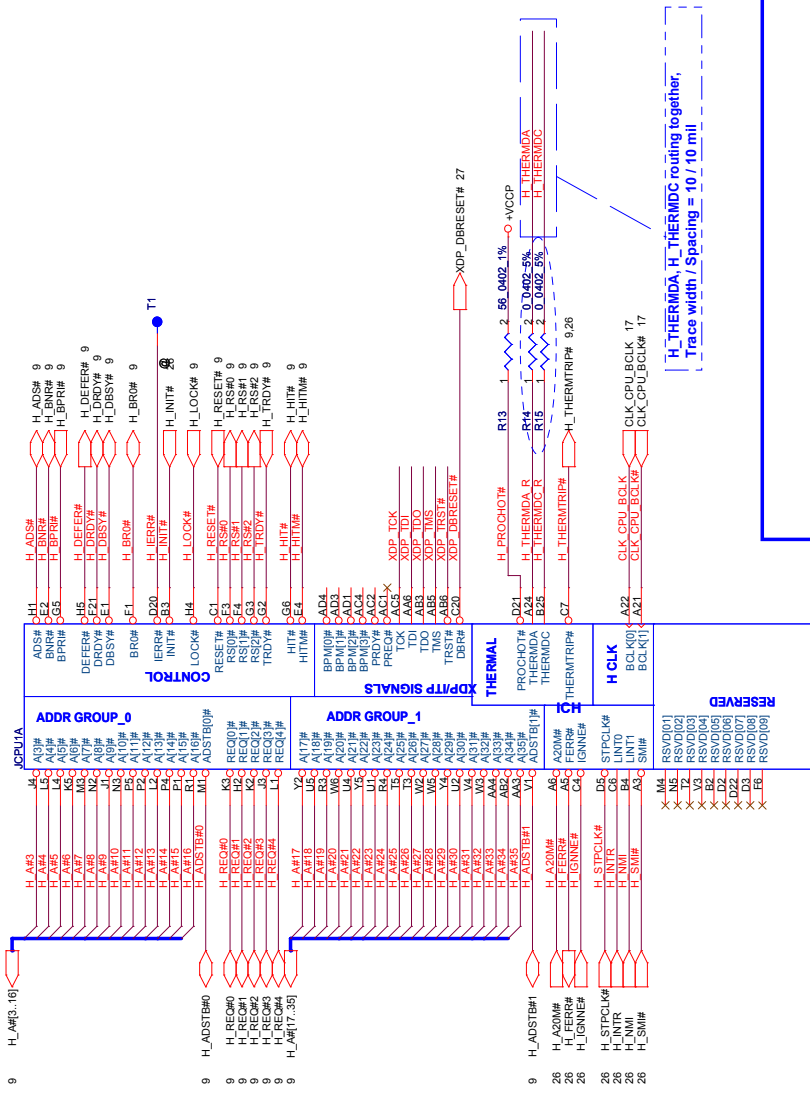
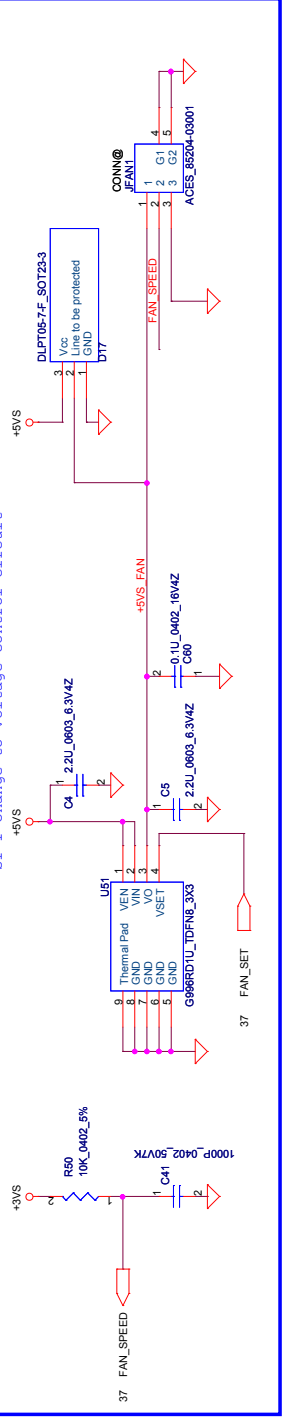
JAL50 Discrete power sequence AC mode





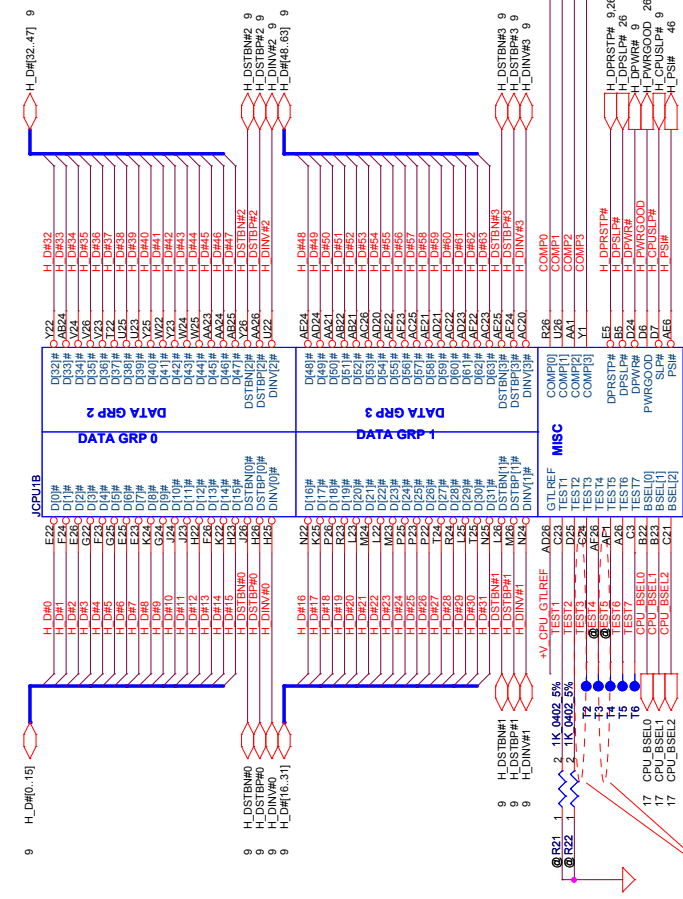
Fan Control circuit

SI-1 Change to voltage control circuit



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Date	2008/11/04	15/06/09	16/06/09	16/06/09	16/06/09	16/06/09	16/06/09	16/06/09
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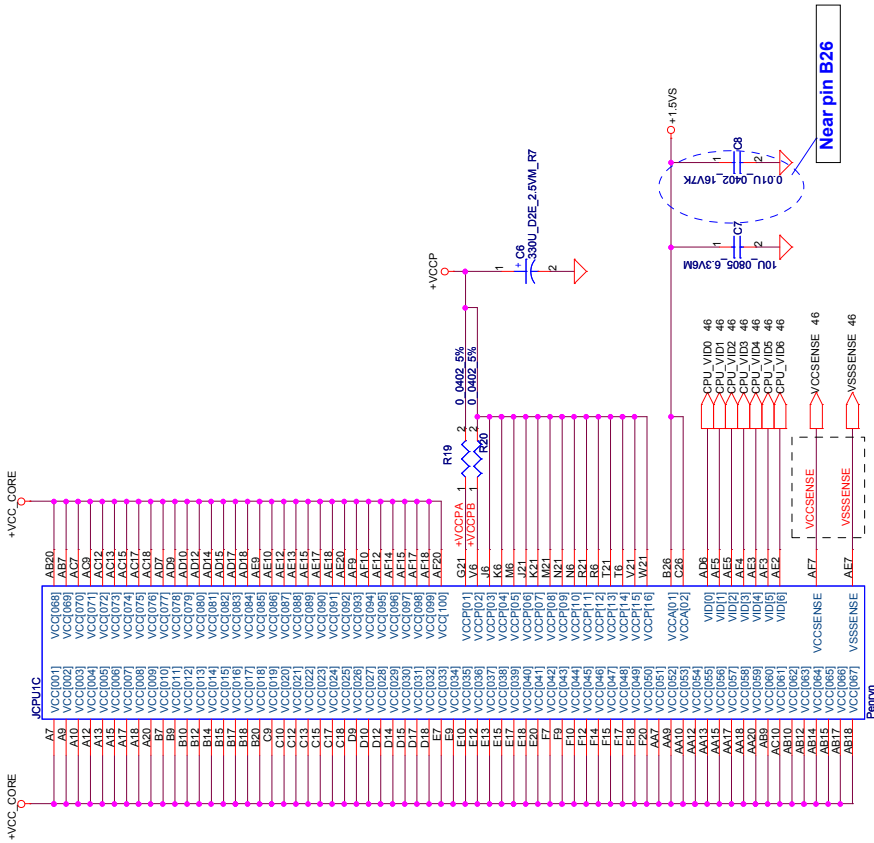
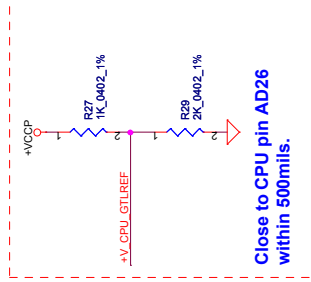
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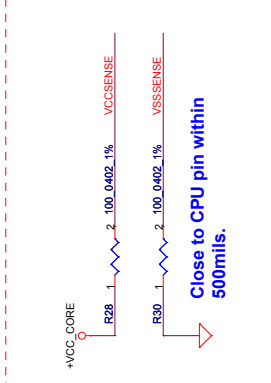
* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

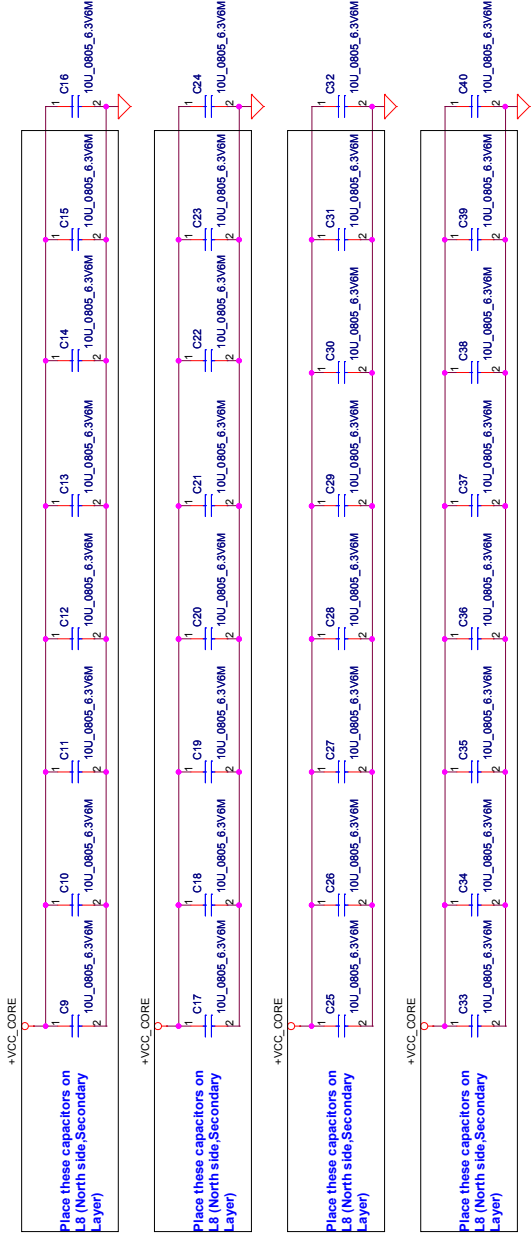
CPU_BSEL	CPU_BSEL0	CPU_BSEL1	CPU_BSEL2
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0.2] trace width is 18 mils. COMP[1.3] trace width is 4 mils.



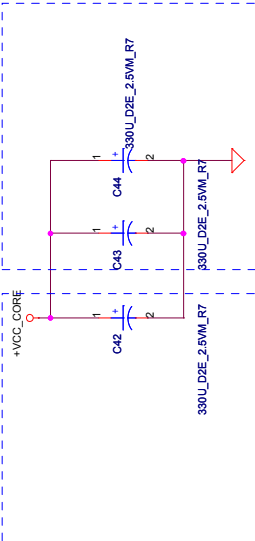
Length match within 25 mils. The trace width/spacing/other is 20/7/25.



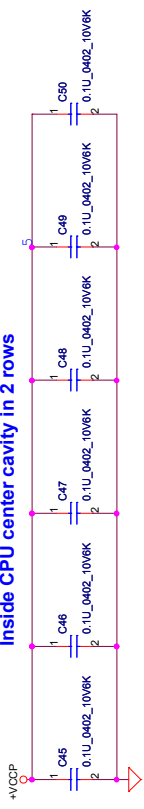


Mid Frequency Decoupling

ESR <= 1.5m ohm
Capacitor > 1980uF



Inside CPU center cavity in 2 rows



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Compal Electronics, Inc.

Penryn(3/3)-AGTL+ITP-XDP

Size

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Custom

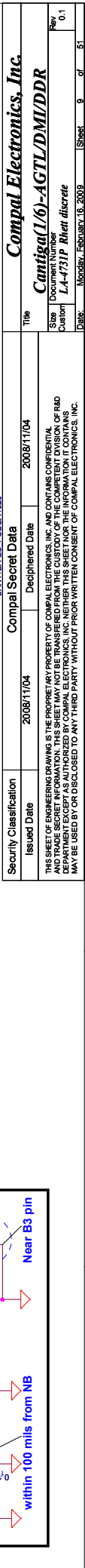
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15 DDR_A_D0[0..63]

U2D

16 DDR_B_D0[0..63]

U2E

17 DDR_C_D0[0..63]

18 DDR_D_D0[0..63]

19 DDR_E_D0[0..63]

20 DDR_F_D0[0..63]

U2D

21 DDR_G_D0[0..63]

U2E

22 DDR_H_D0[0..63]

23 DDR_I_D0[0..63]

24 DDR_J_D0[0..63]

25 DDR_K_D0[0..63]

U2D

26 DDR_L_D0[0..63]

U2E

27 DDR_M_D0[0..63]

28 DDR_N_D0[0..63]

29 DDR_O_D0[0..63]

30 DDR_P_D0[0..63]

U2D

31 DDR_Q_D0[0..63]

U2E

32 DDR_R_D0[0..63]

33 DDR_S_D0[0..63]

34 DDR_T_D0[0..63]

35 DDR_U_D0[0..63]

U2D

36 DDR_V_D0[0..63]

U2E

37 DDR_W_D0[0..63]

38 DDR_X_D0[0..63]

39 DDR_Y_D0[0..63]

40 DDR_Z_D0[0..63]

U2D

41 DDR_AA_D0[0..63]

U2E

42 DDR_AB_D0[0..63]

43 DDR_AC_D0[0..63]

44 DDR_AD_D0[0..63]

45 DDR_AE_D0[0..63]

U2D

46 DDR_AF_D0[0..63]

U2E

47 DDR_AG_D0[0..63]

48 DDR_AH_D0[0..63]

49 DDR_AI_D0[0..63]

50 DDR_AJ_D0[0..63]

U2D

51 DDR_AK_D0[0..63]

U2E

52 DDR_AL_D0[0..63]

53 DDR_AM_D0[0..63]

54 DDR_AN_D0[0..63]

55 DDR_AO_D0[0..63]

U2D

56 DDR_AP_D0[0..63]

U2E

57 DDR_AQ_D0[0..63]

58 DDR_AR_D0[0..63]

59 DDR_AS_D0[0..63]

60 DDR_AT_D0[0..63]

U2D

61 DDR_AU_D0[0..63]

U2E

62 DDR_AV_D0[0..63]

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65 DDR_AY_D0[0..63]

U2D

66 DDR_AZ_D0[0..63]

U2E

67 DDR_BA_D0[0..63]

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69 DDR_BC_D0[0..63]

70 DDR_BD_D0[0..63]

U2D

71 DDR_BE_D0[0..63]

U2E

72 DDR_BF_D0[0..63]

73 DDR_BG_D0[0..63]

74 DDR_BH_D0[0..63]

75 DDR_BI_D0[0..63]

U2D

76 DDR_BJ_D0[0..63]

U2E

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U2D

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U2E

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U2E

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U2E

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108 DDR_CP_D0[0..63]

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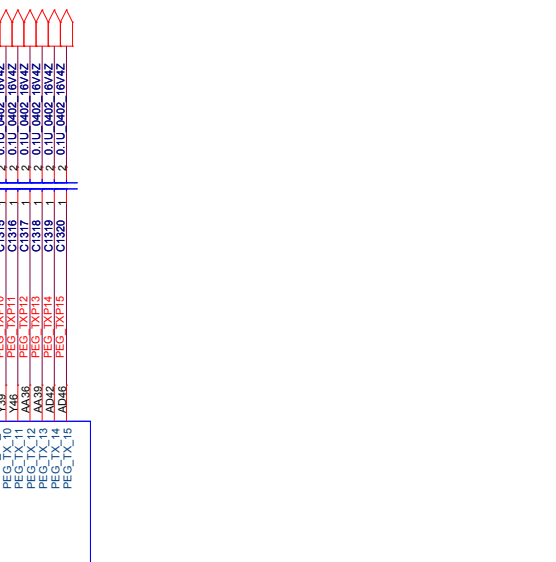
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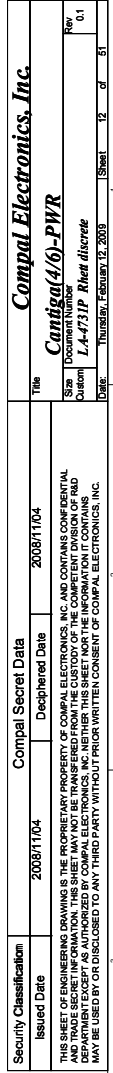
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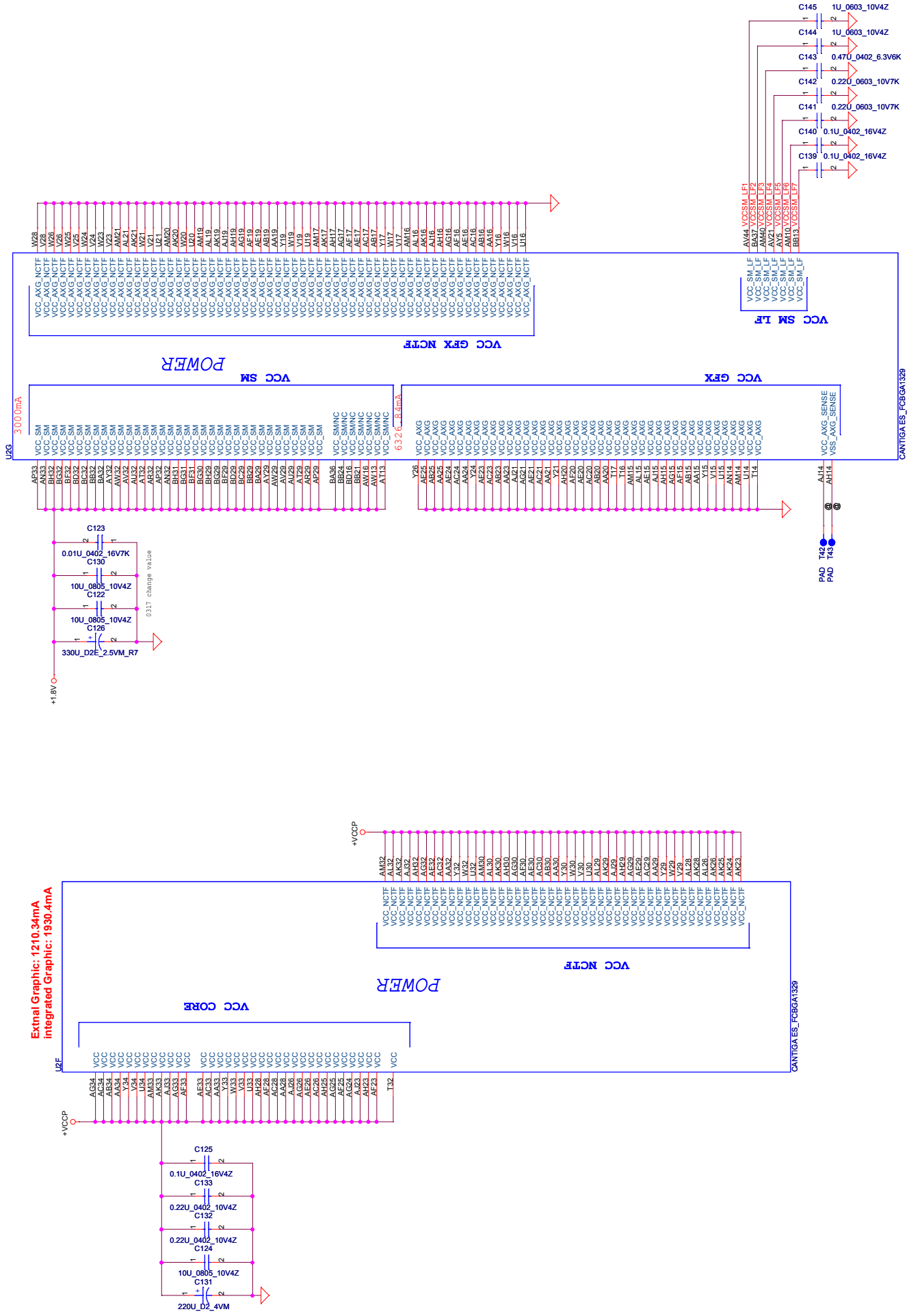
U2C

R57

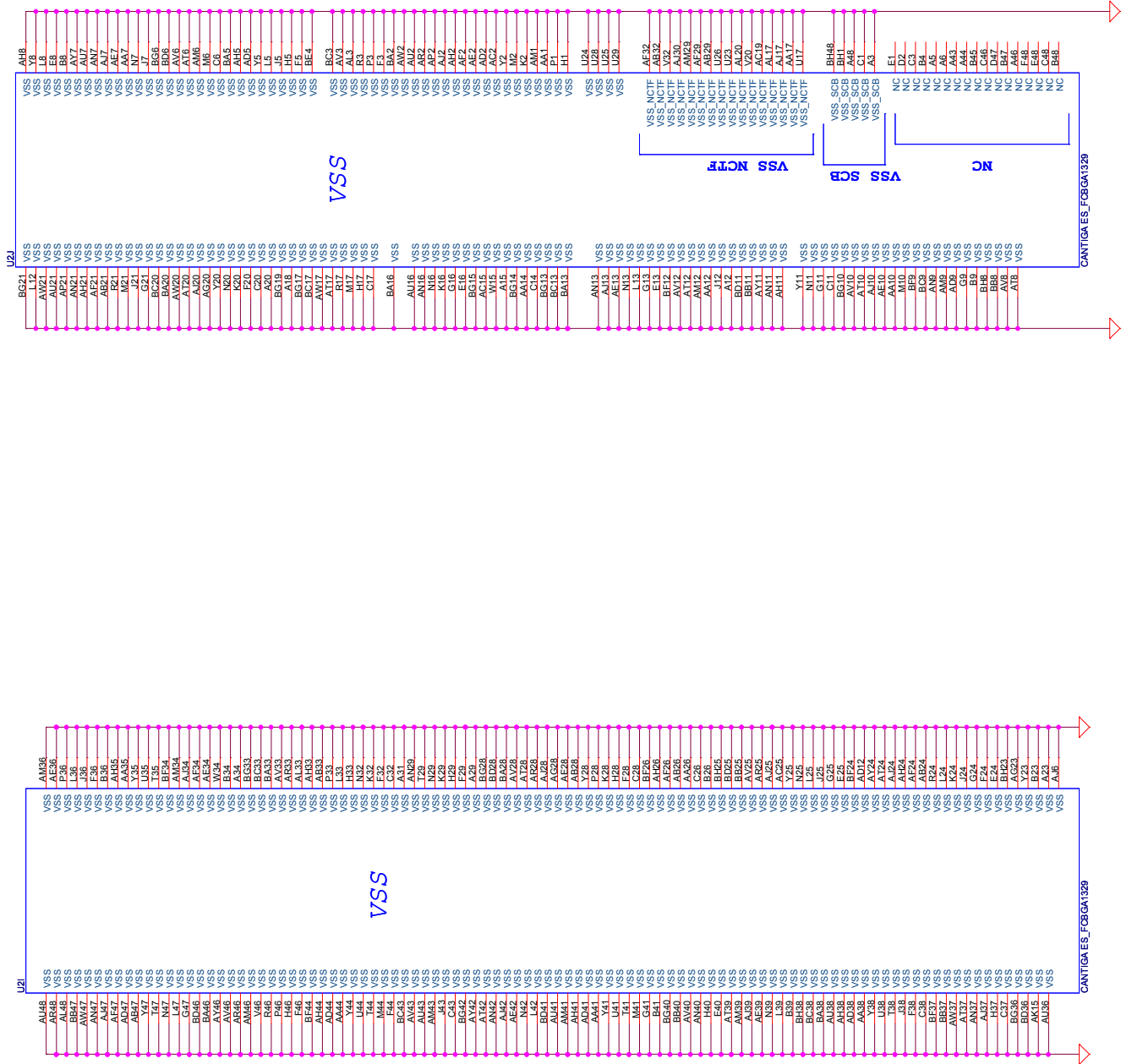
[illegible]



External Graphic: 1210.34mA
Integrated Graphic: 1930.4mA



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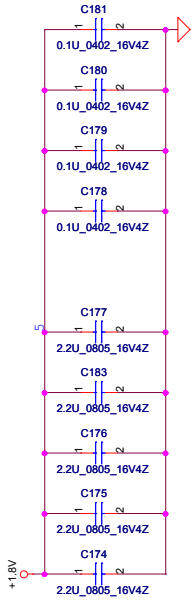


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<p align="center">Compal Electronics, Inc.</p> <p align="center">Canigua(66)-PWR/GND</p>				
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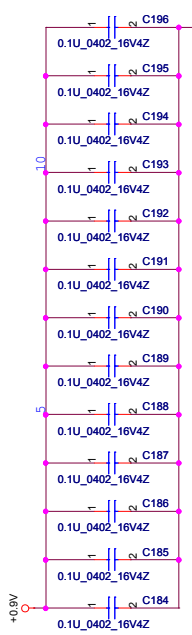


10 DDR_B_D0[0..7]
10 DDR_B_D0[8..15]
10 DDR_B_DM0[0..7]
10 DDR_B_DM0[8..15]
10 DDR_B_MA0[0..7]
10 DDR_B_MA0[8..15]

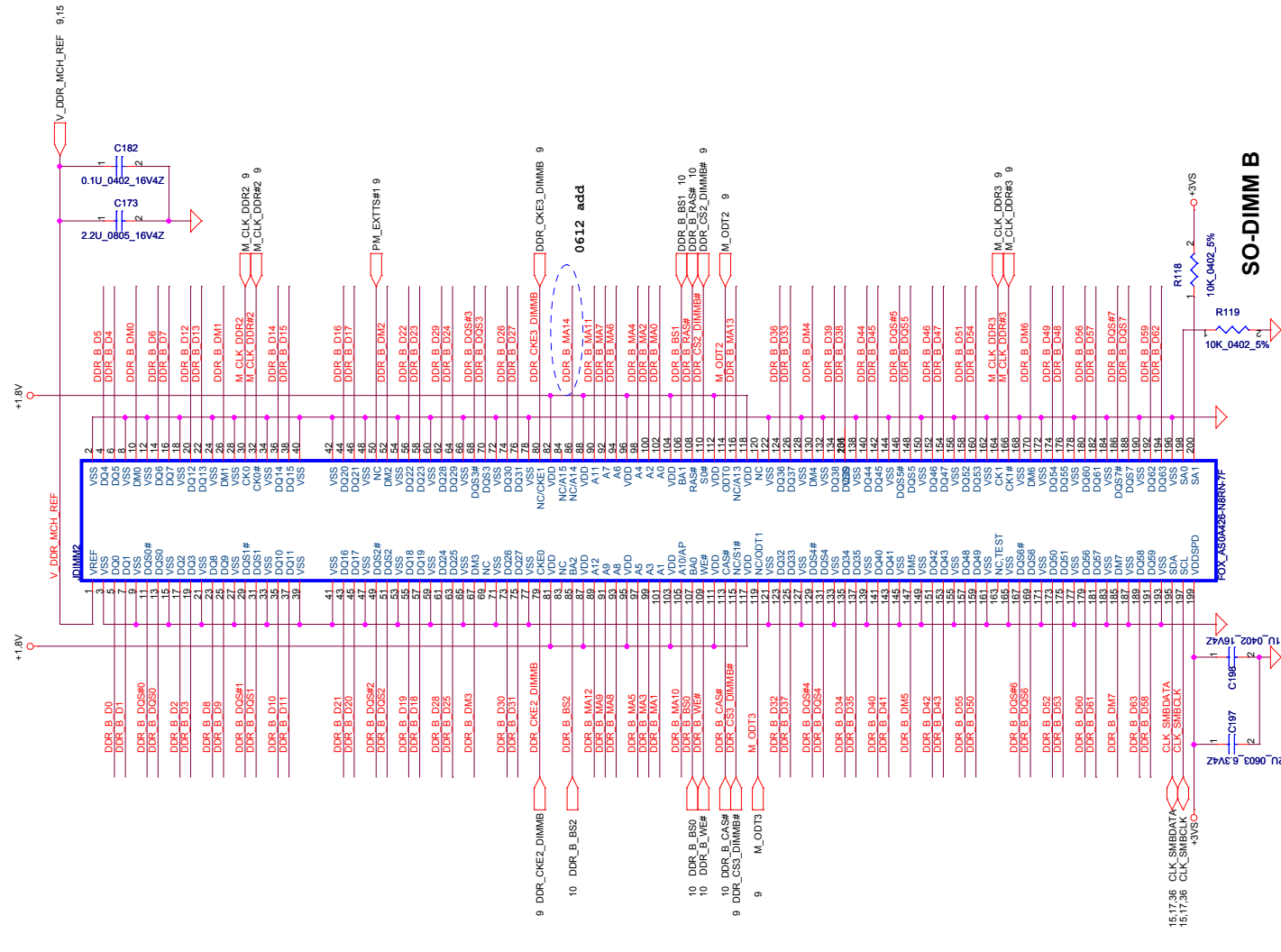
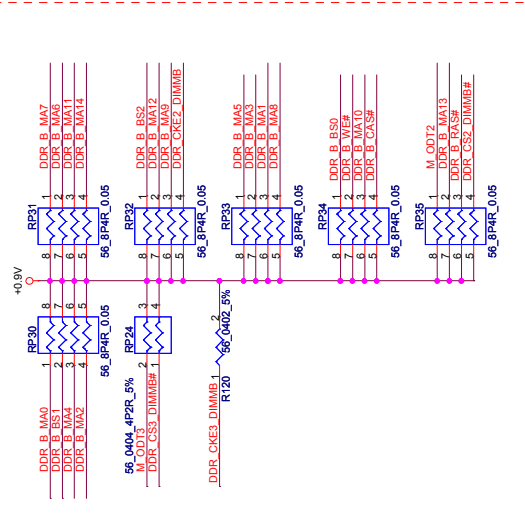
Layout Note:
Place near
JP10



Layout Note:
Place one cap close to every 2
pullup
resistors terminated to +0.9VS

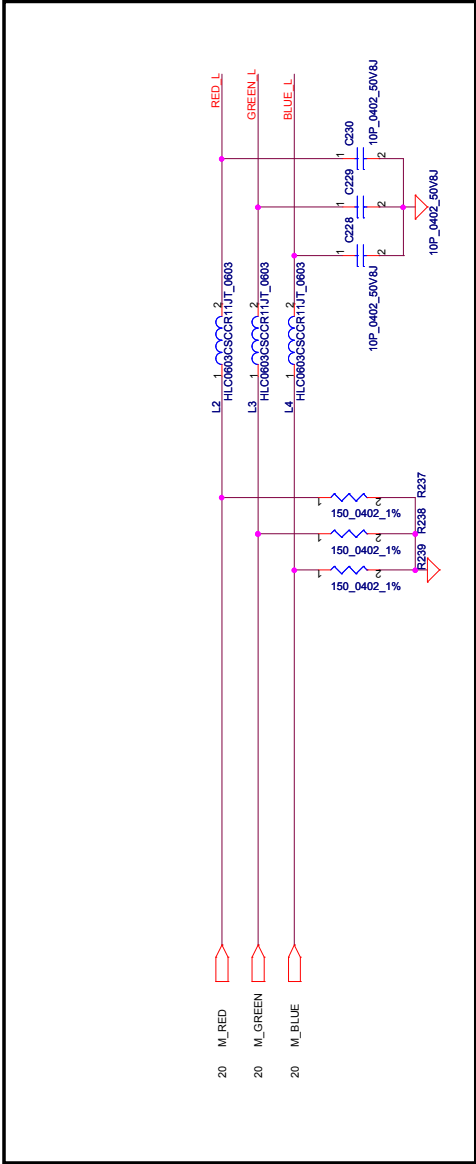
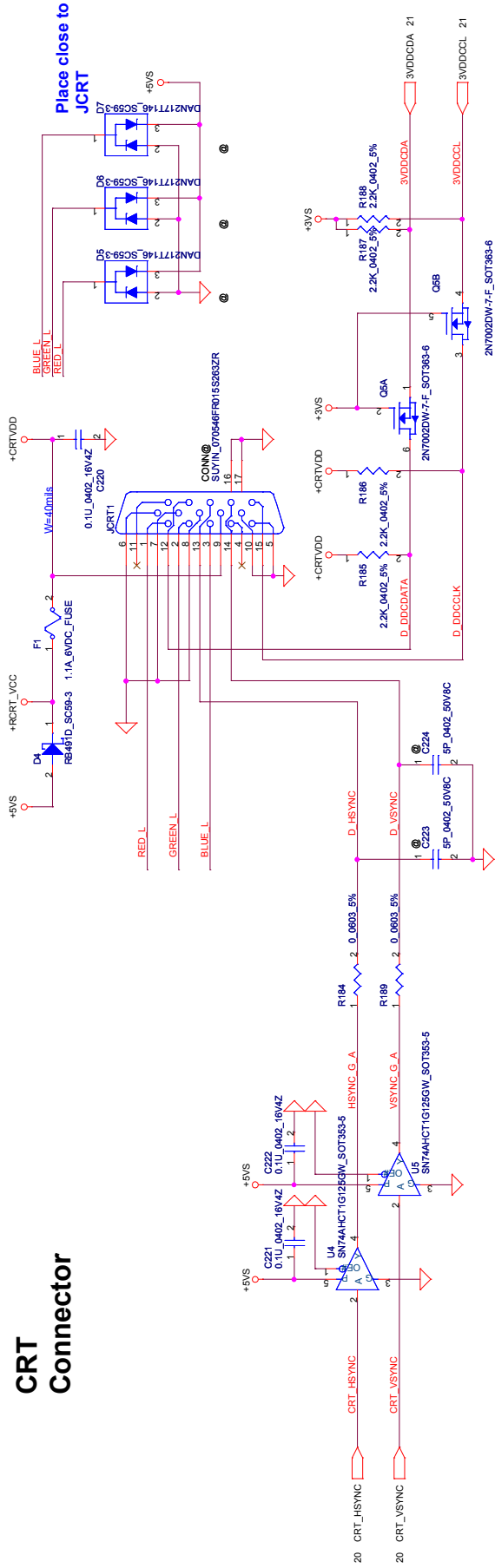


Layout Note:
Place these resistor
closely JP3,all
trace length Max=1.5"



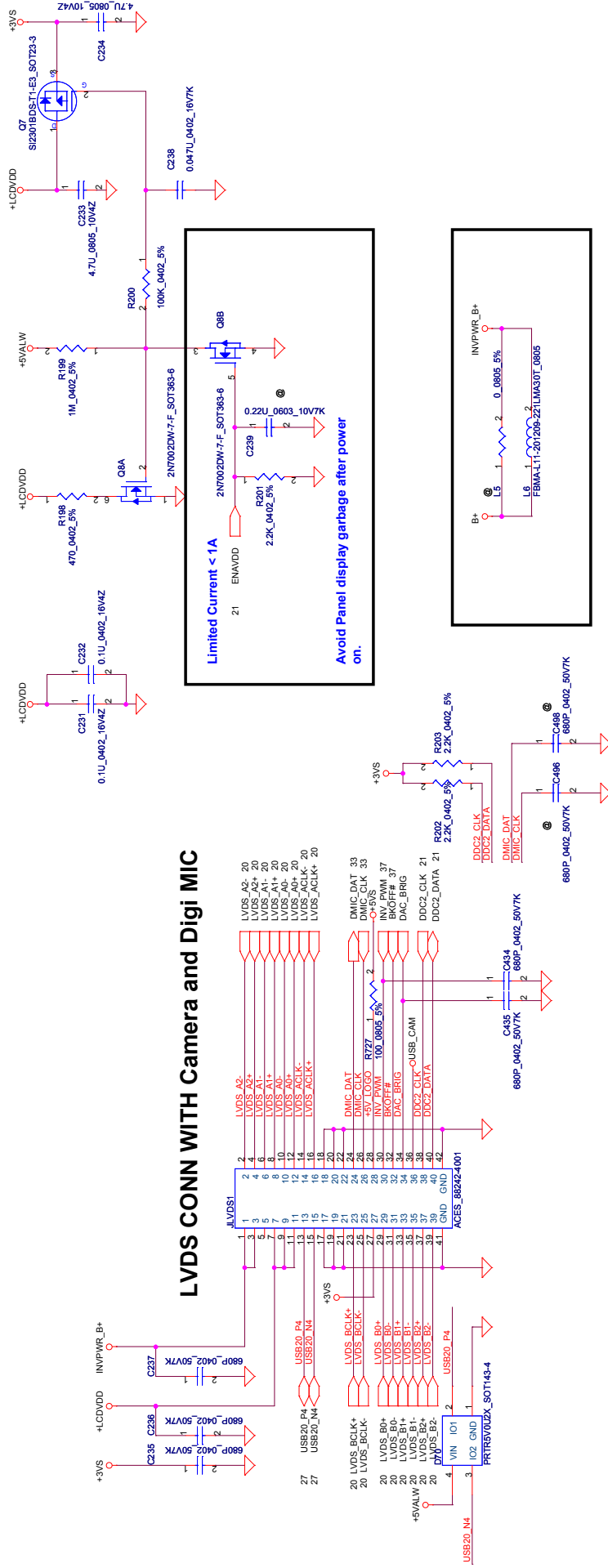
Compal Secret Data			
Security Classification	Issued Date	Deciphered Date	Title
	2008/1/10/4	2008/1/10/4	Compal Electronics, Inc.
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Size	Document Number	Rev	Page
16	LA-4731P Rhen discrete	0.1	51
16	Monday, February 16, 2009		Sheet

CRT Connector

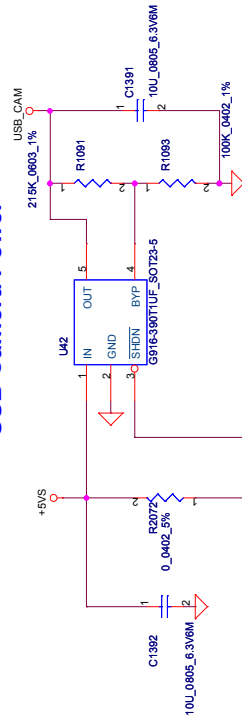


Compal Secret Data				Title	
Security Classification	2008/11/04	Deciphered Date	2008/11/04	CRT Connector	
Issued Date	2008/11/04	Deciphered Date	2008/11/04	Size	Document Number
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				Date	Monday, February 16, 2009
				Sheet	18 of 51

LVDS CONN WITH Camera and Digi MIC



USB Camera Power

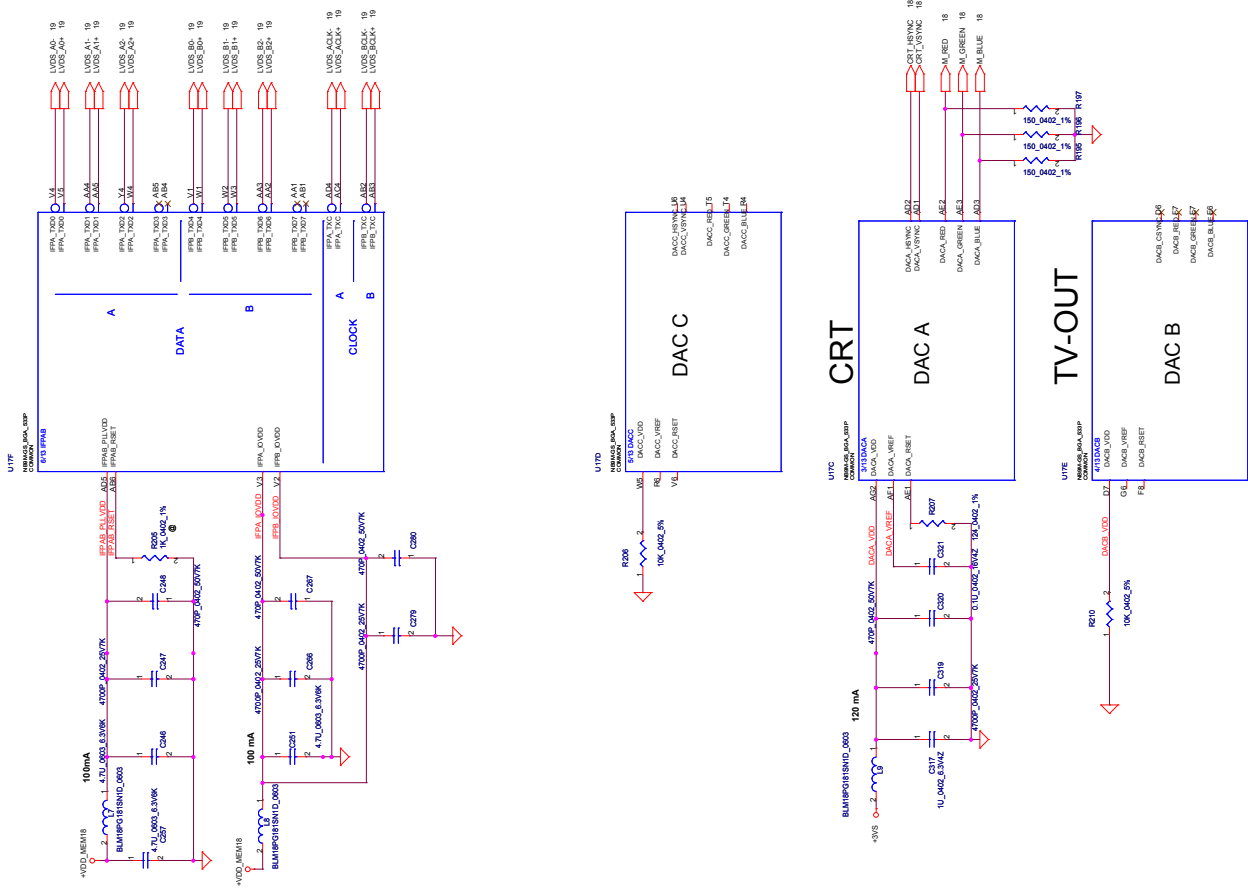


USB VCCA is +3.9V

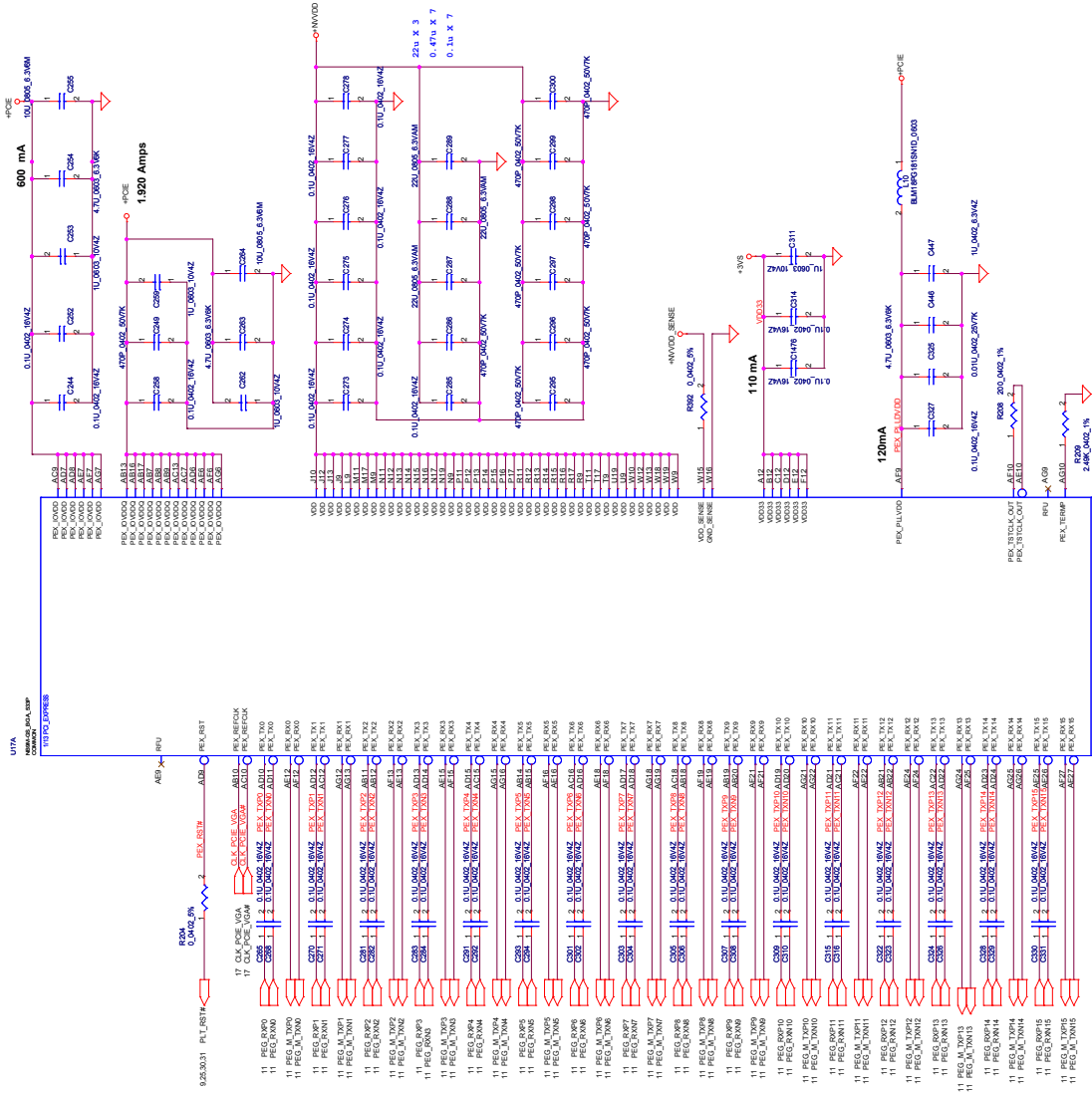
USB VCCA = 1.25X(1+R1091/R1093)

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<p>Compal Electronics, Inc.</p> <p>LCD CONN.</p>			<p>Size</p> <p>Document Number</p> <p>Rev</p> <p>L4-4731P Rhett discrete</p> <p>0.1</p>
Date:	Monday, February 18, 2008	Sheet	10 of 51

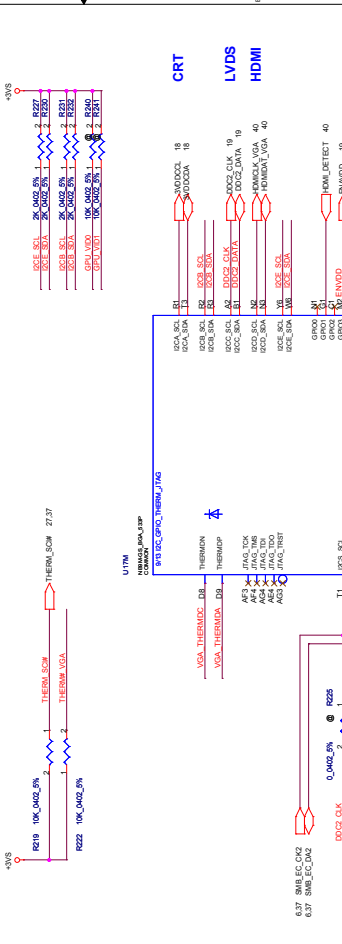
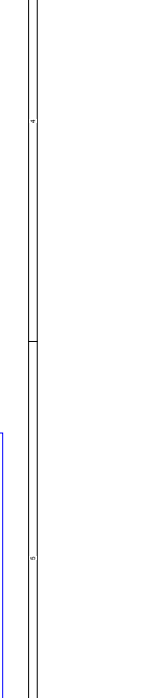
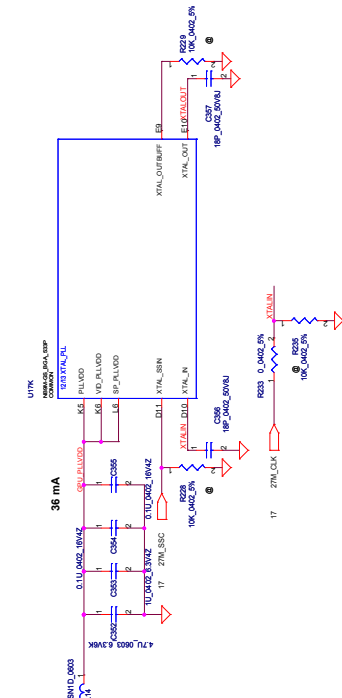
LVDS & DAC Interface



PEG Interface



Security Classification:	2008/11/04	Compal Secret Data	2008/11/04	Rev
Issued Date	2008/11/04	Dispersed Date	2008/11/04	01
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Compal Electronics, Inc.				
PEG & LVDS & DAC				
Rev 1.0				
L4-173 IP Rev 1.0				
10/2008				



The diagram shows a 10-bit DAC circuit. On the left, a 10-bit digital input is provided by a bus labeled '10bit_din'. This bus is connected to a 10-bit DAC core, which is represented by a block labeled '10bit_dac'. The output of the DAC core is a 10-bit digital signal labeled '10bit_dout'. This signal is then connected to a 10-bit DAC output, which is represented by a block labeled '10bit_dac_out'. The output of the DAC output block is a 10-bit analog signal labeled '10bit_dac_out_a'. The circuit is implemented using a 10-bit DAC core and a 10-bit DAC output block.

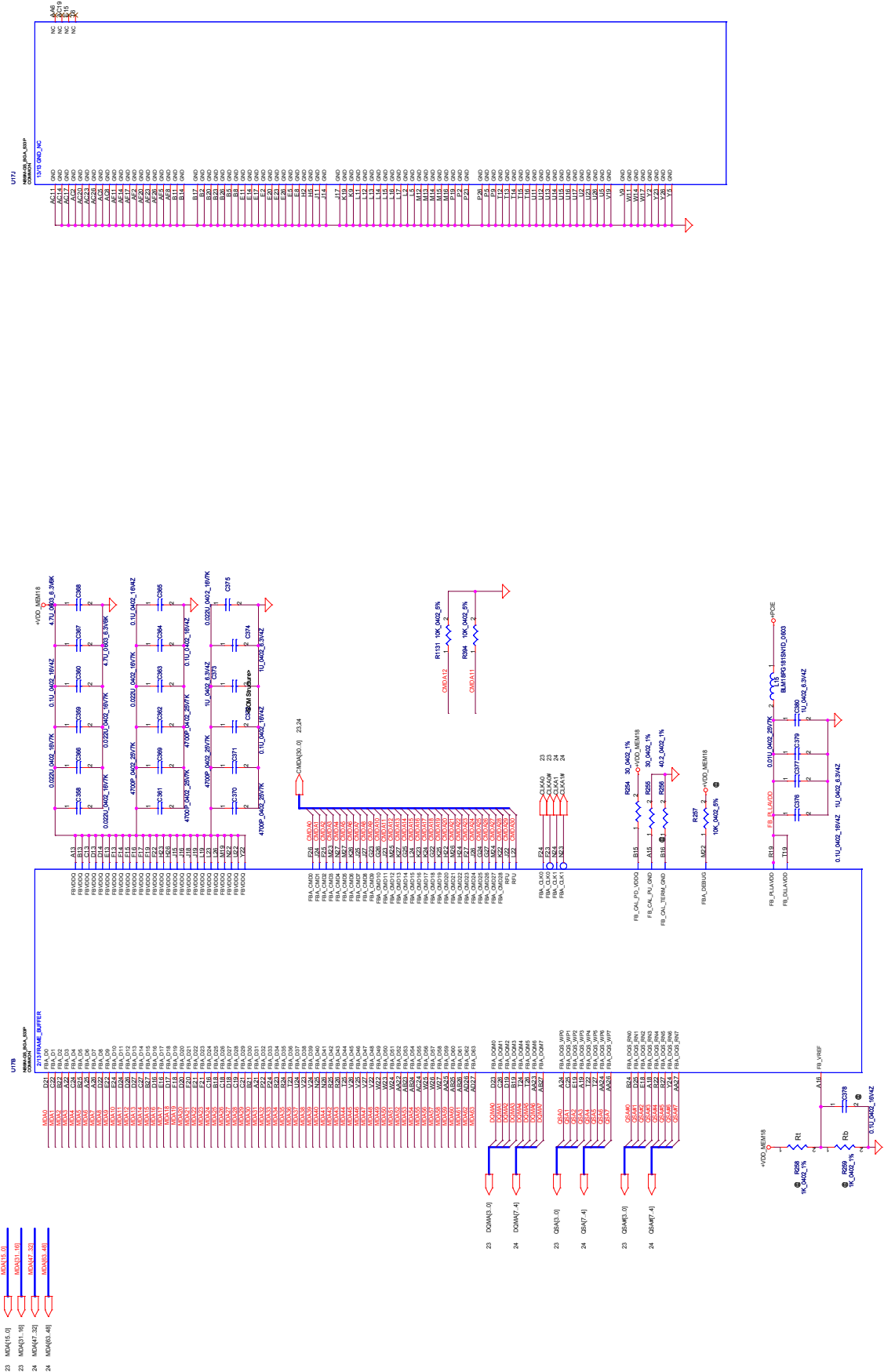
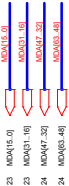
1.1.1.1	10.54
1.1.1.2	15.67mm
1.1.1.3	15.67mm
1.1.1.4	15.67mm

US & HDM

US	Sheet	21	of
76, February 18, 2009			

[illegible]

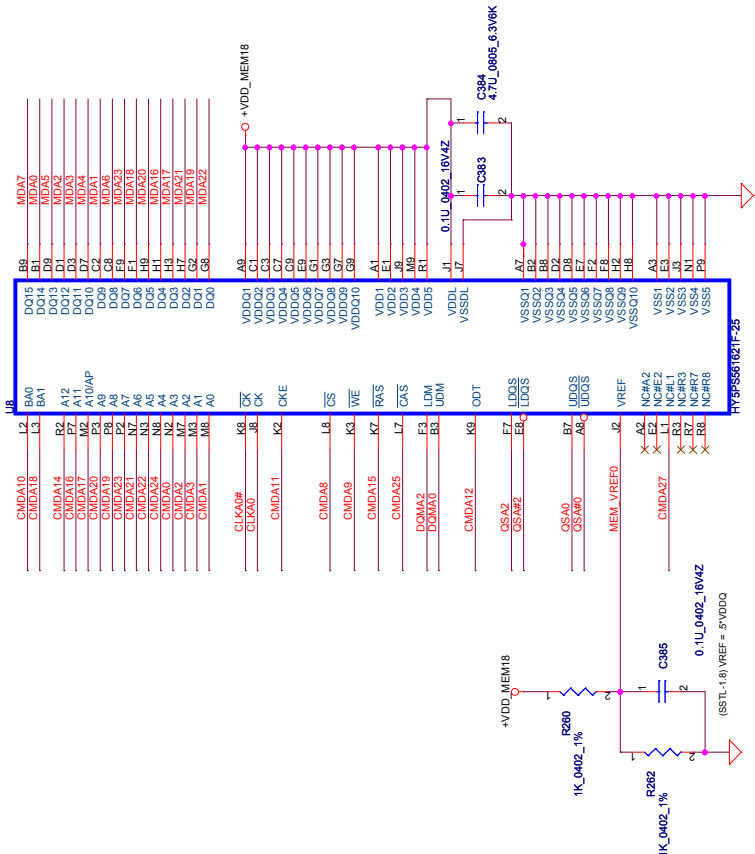
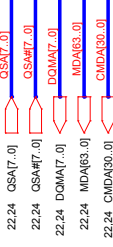
VRAM Interface



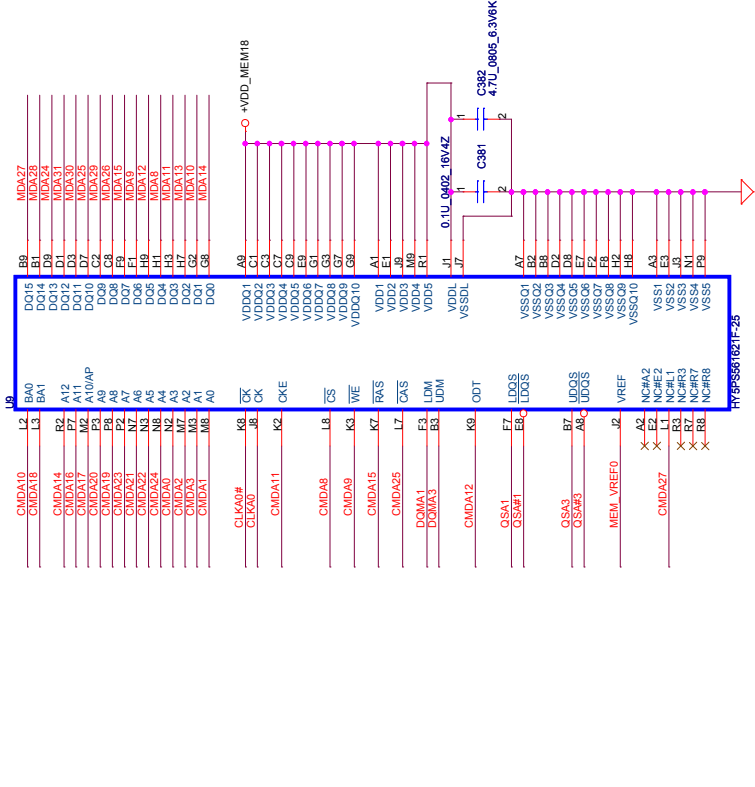
Security Classification		Compal Secret Data		16	
Issued Date	2008/11/04	Dispersed Date	2008/11/04		
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Compal Electronics, Inc.				VRAM / GND	
Rev. 1				Rev. 1	
Date: 11/04/08				Date: 11/04/08	
Drawn: 11/04/08				Drawn: 11/04/08	
Checked: 11/04/08				Checked: 11/04/08	
Approved: 11/04/08				Approved: 11/04/08	

VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB
64Mx16 DDR2 400MHz*4==>512MB

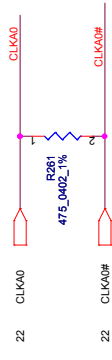


DDR2 BGA MEMORY



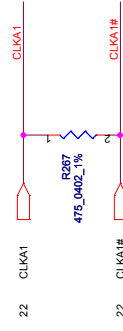
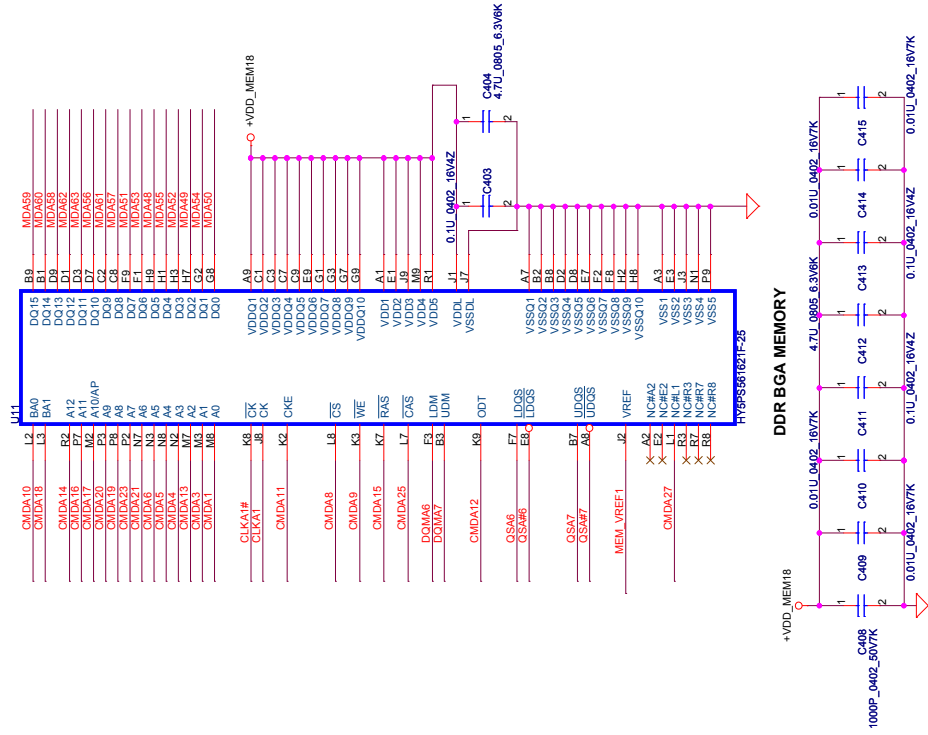
DDR BGA MEMORY

Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	A5
CMD23	A7	A7
CMD24	A4	A4
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

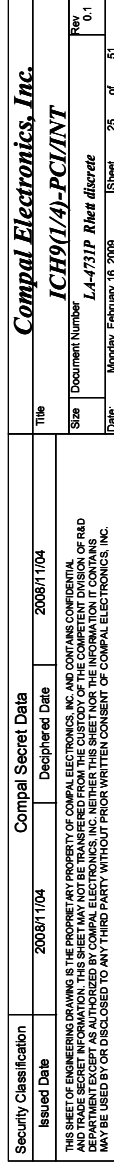
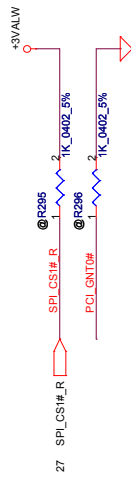
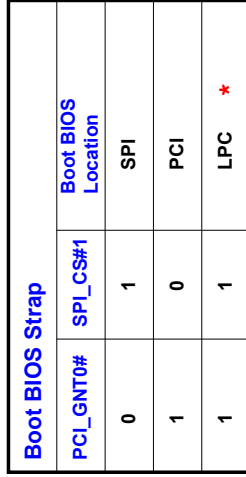


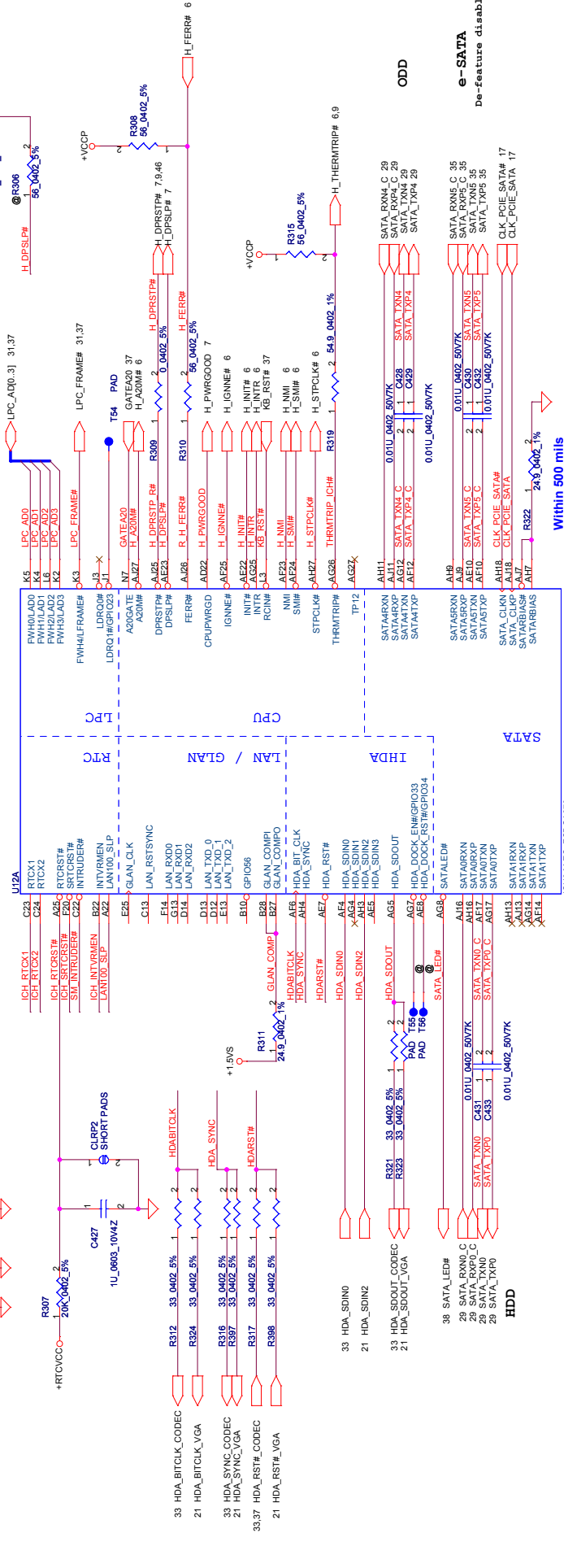
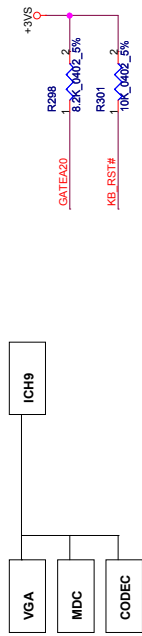
32Mx16 DDR2 400MHz *4==>256MB
64Mx16 DDR2 400MHz*4==>512MB

Address	DATA Bus	
	0...31	32...63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

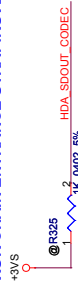


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Size			Document Number	Rev
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Date:			Issue Date	Sheet
Monday, February 18, 2009			8	of 16

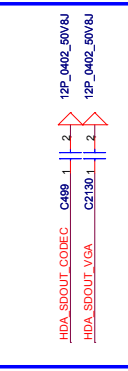




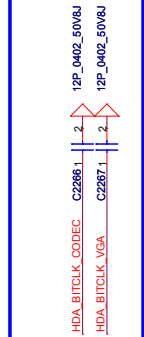
XOR CHAIN ENTRANCE STRAP:RSVD



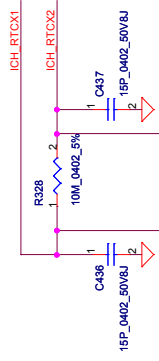
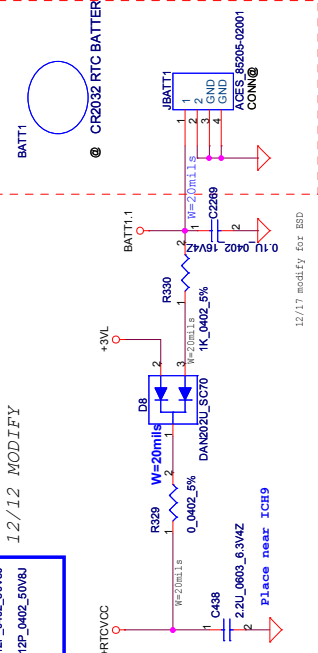
ICH_RSVD	HDA_SDOUT_CODEC
0	0
0	1
1	0
1	1



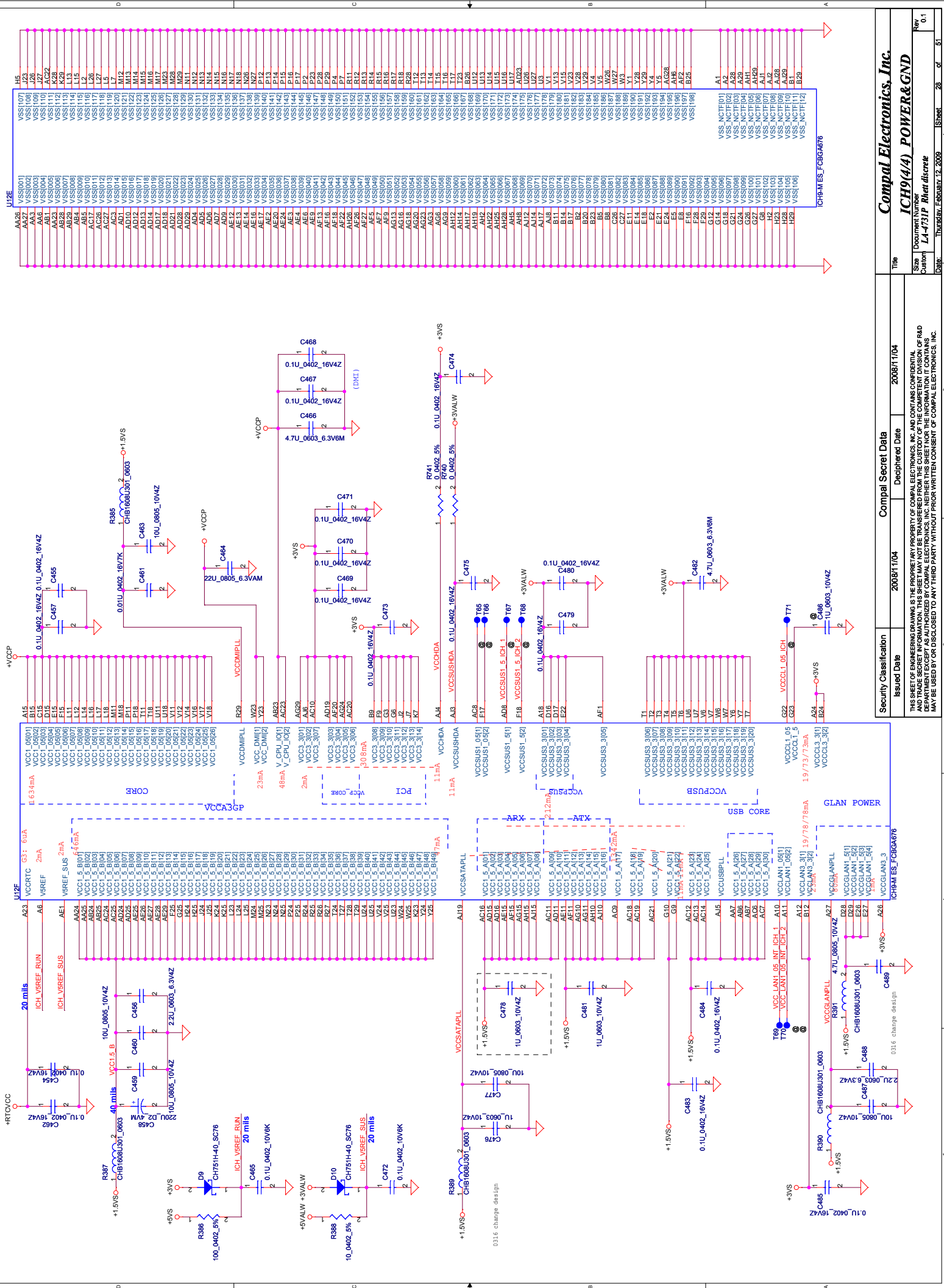
#PV reserve for WWAN noise



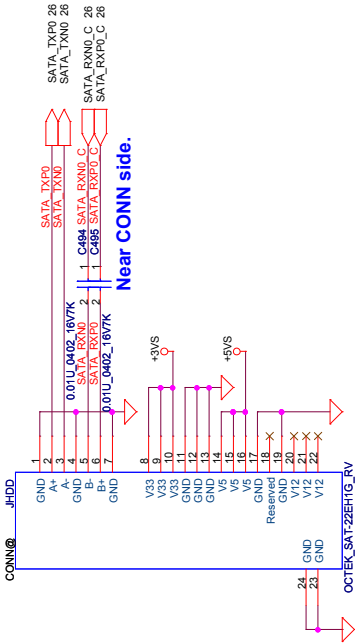
12/12 MODIFY



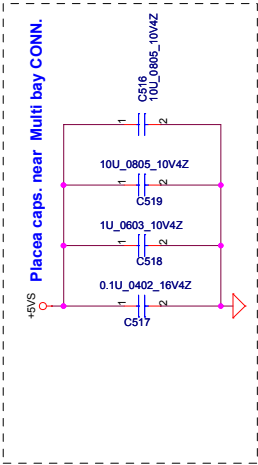
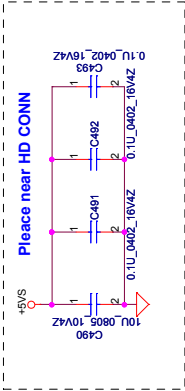
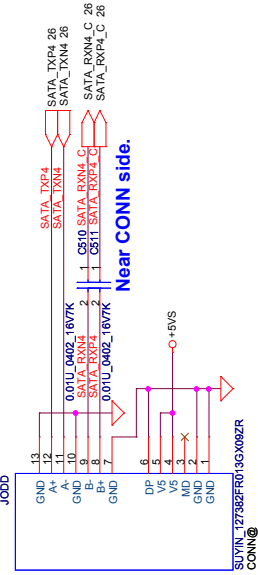
32.768KHz_12.5P_MC-146



HDD Connector

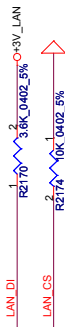


CD-ROM Connector

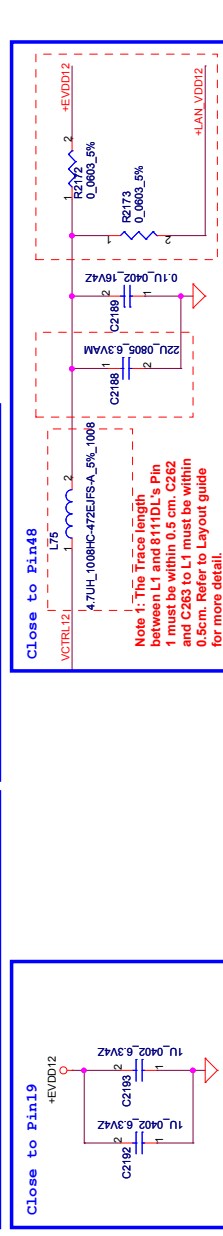
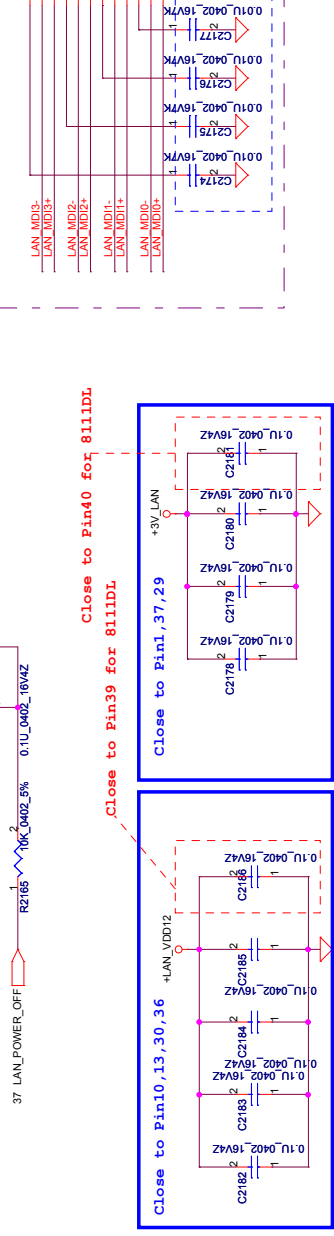
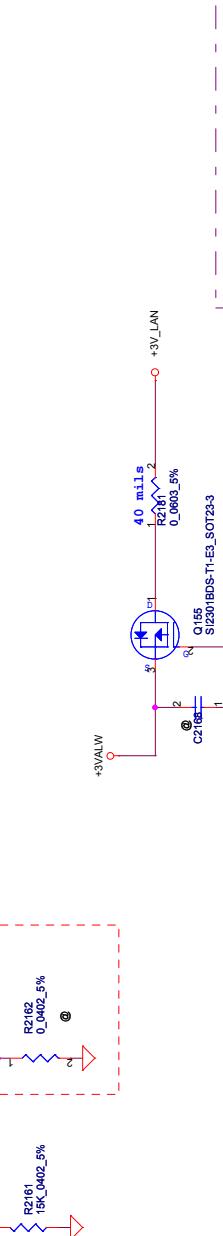
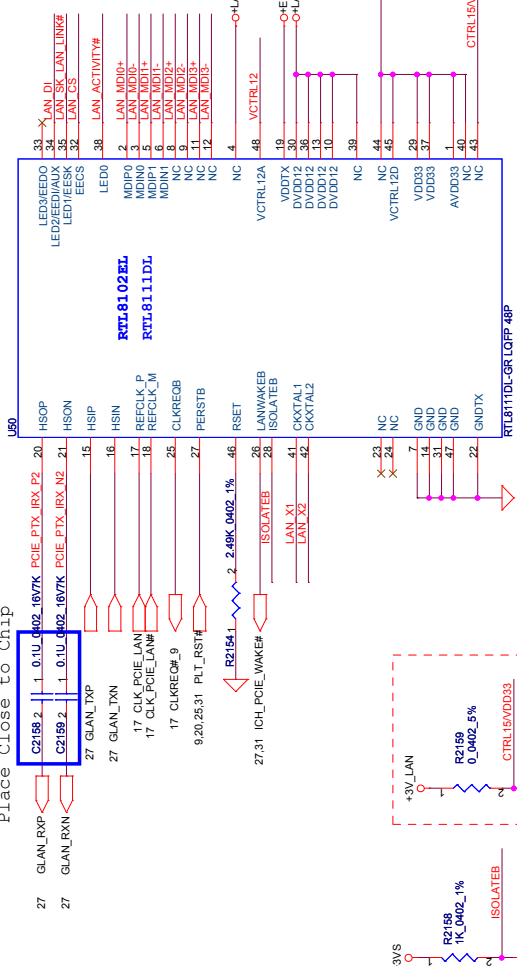


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Issued Date	2008/11/04	Deciphered Date	2008/11/04	HDD & CDROM
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				Custom L4-4731P Rev01
				Date Modified Frequency 16 2009 1 1 Sheet 28 of 51

LAN Conn.



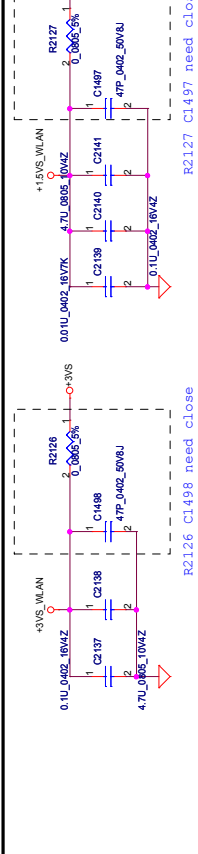
Place Close to Chip



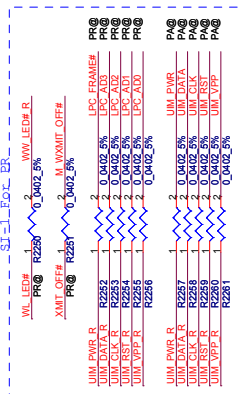
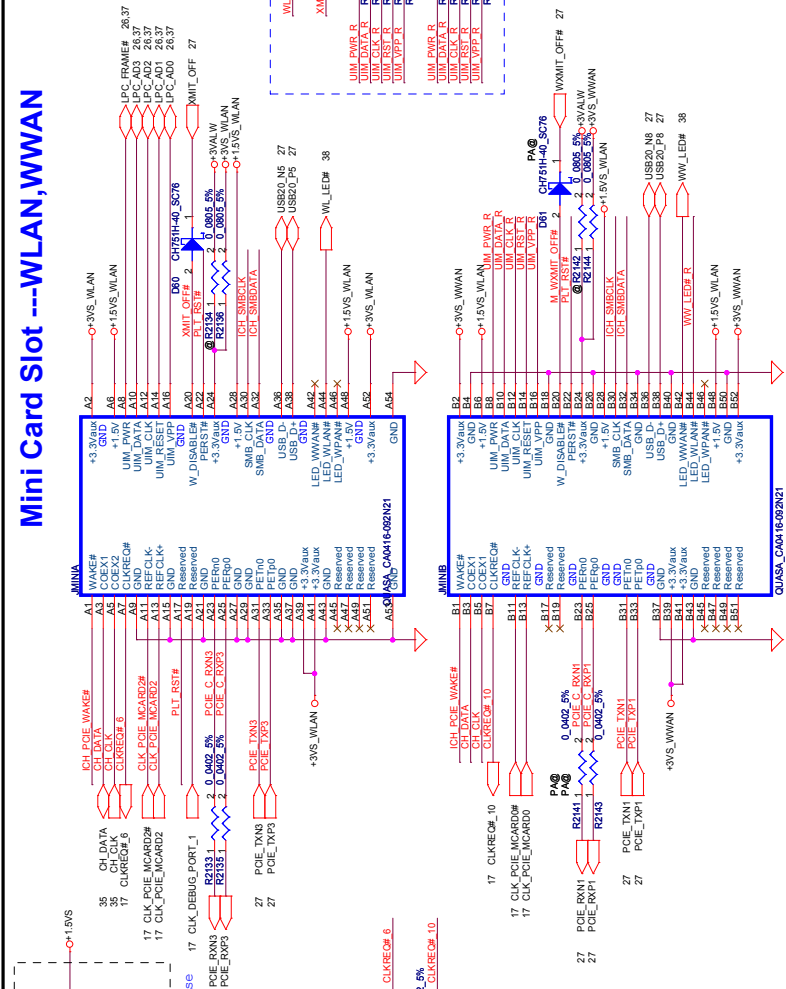
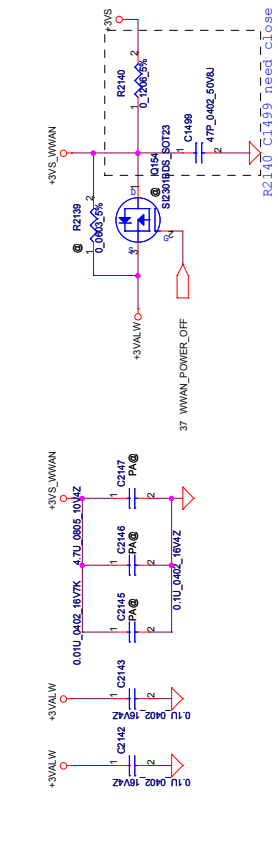
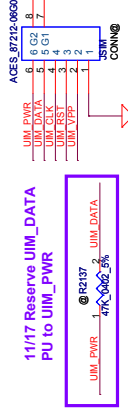
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								Document Number			
								LA-4731P			
								Rev			
								0.1			
								Date			
								Monday, February 18, 2009			
								Sheet			
								30			
								of			
								51			

Compal Electronics, Inc.

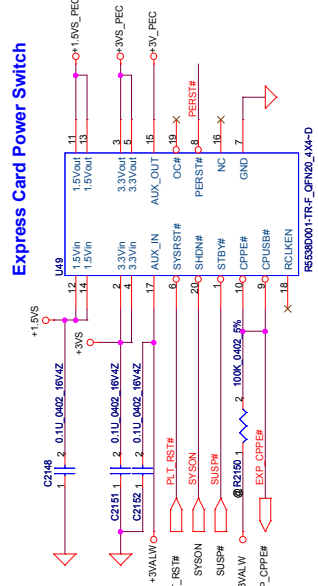
Mini Card Slot ---WLAN,WWAN



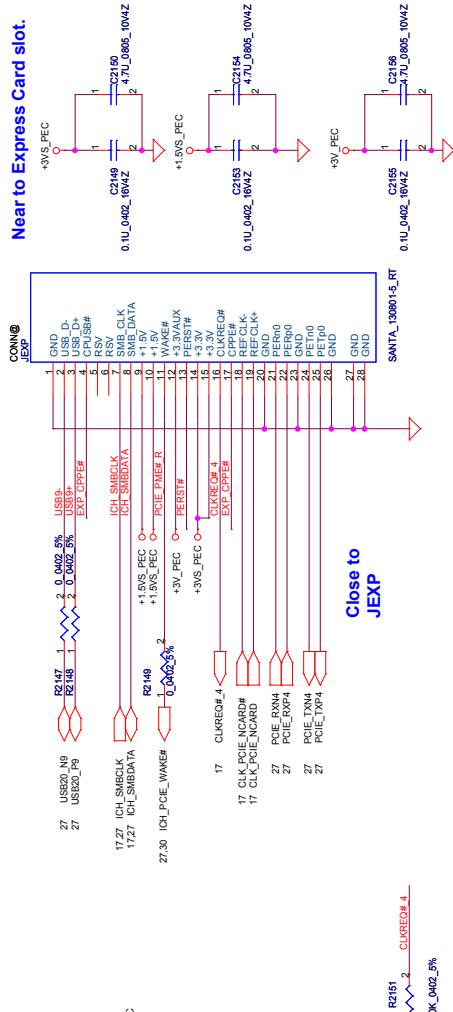
SIM card Connector



New Card

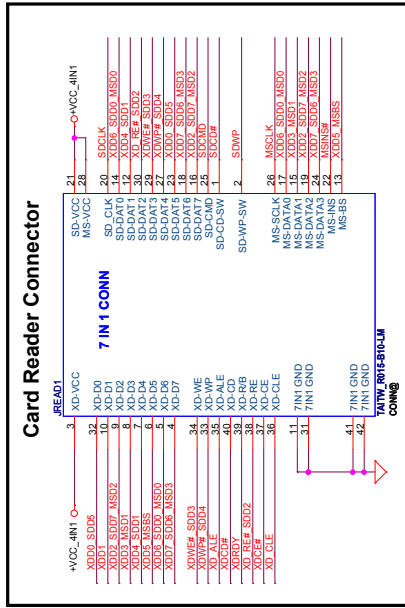
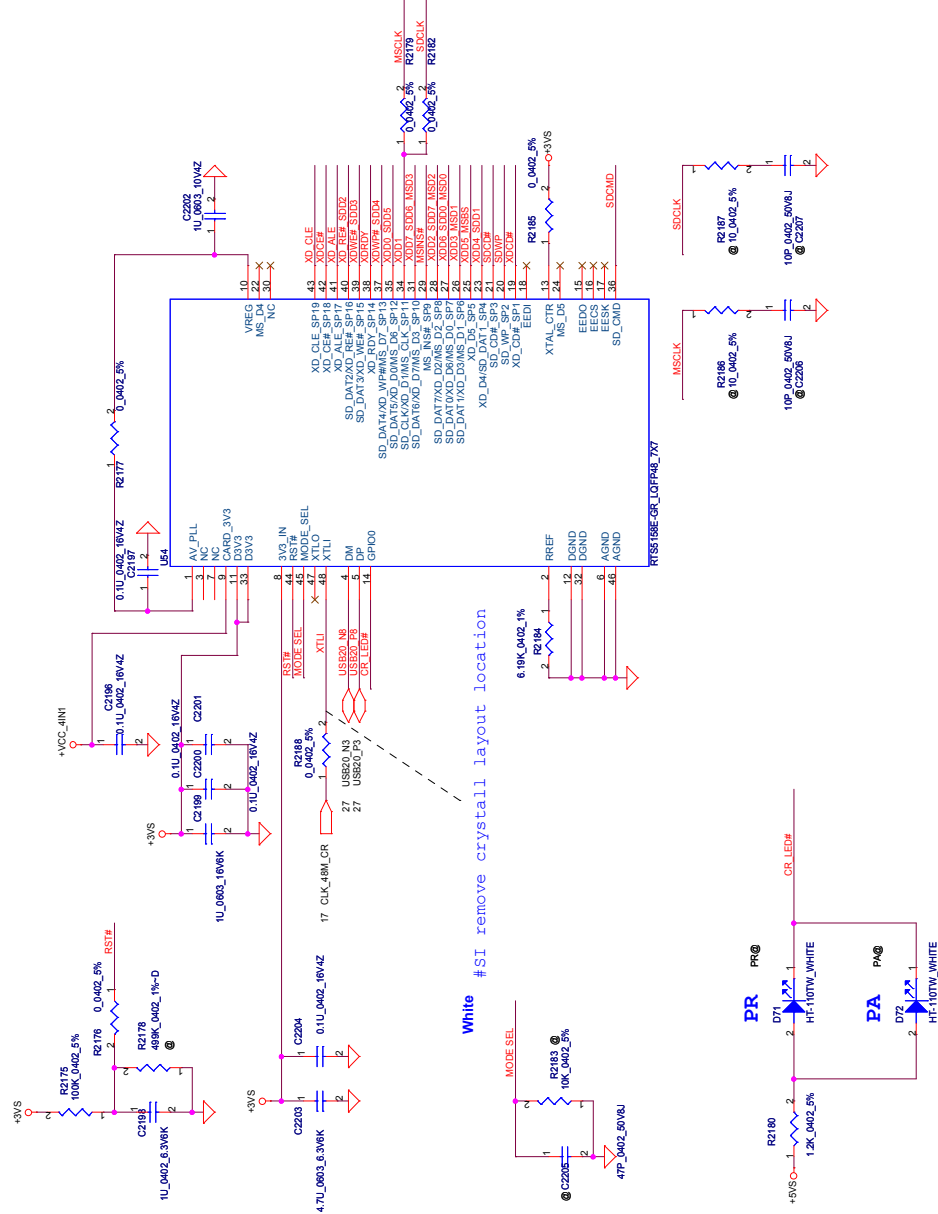


internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low

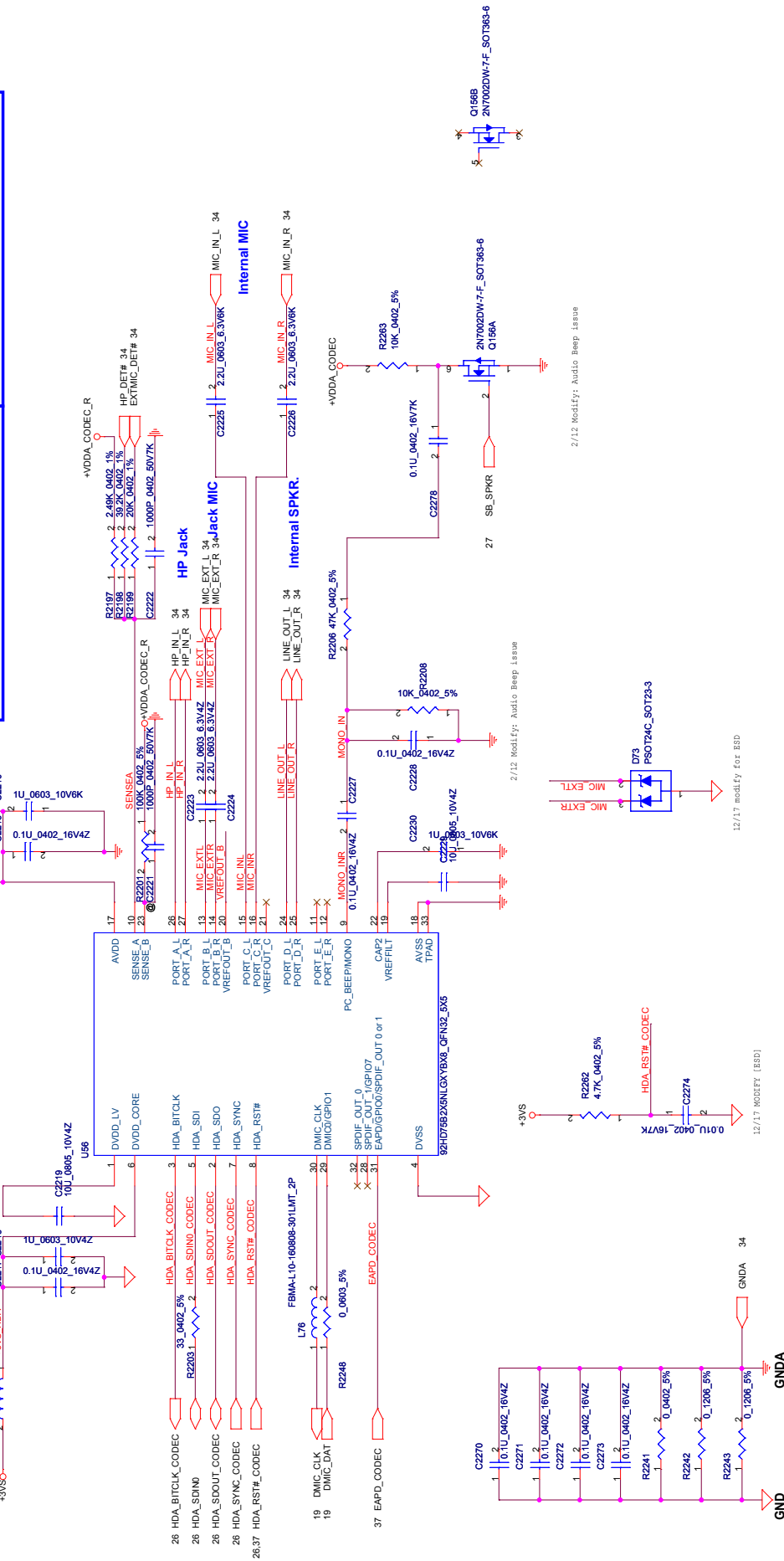
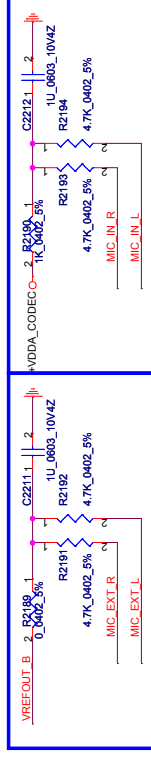
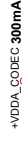


Near to Express Card slot

Security Classification	Compal Secret Data			Title	<i>Compal Electronics, Inc.</i> <i>WLAN, WWAN, New Card</i>		
Issued Date	2008/11/04	Deciphered Date	2008/11/04	Size	Document Number	Rev	0.1
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				L4-731P Rhet discrete			



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Issued Date			Deciphered Date			USB CardReader&CONN		
2008/11/04			2008/11/04			L4-4731P Rhett discrete		
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L4-4731P Rhett discrete			32			of		
Date:			Monday, February 16, 2009			Sheet		



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Issued Date	2008/11/04	Deciphered Date	2008/11/04
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Codec _IDT9278B			Size
LA-473 IP Rhett discrete			Document Number
Date:	Monday, February 16, 2010	Sheet	33 of 51
Page:			Rev 0.1

SPEAKER

9/20 SFO2000CN00

0V 100V 200V 300V

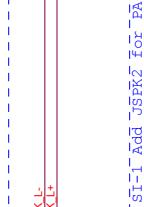
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C2221 C2231 C2232 C2233 C2234

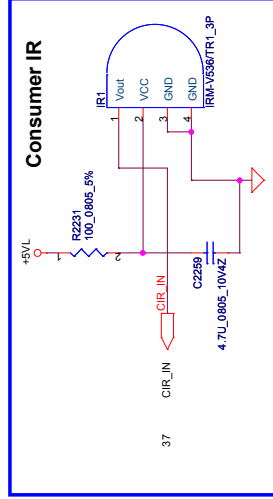
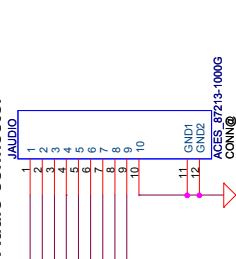
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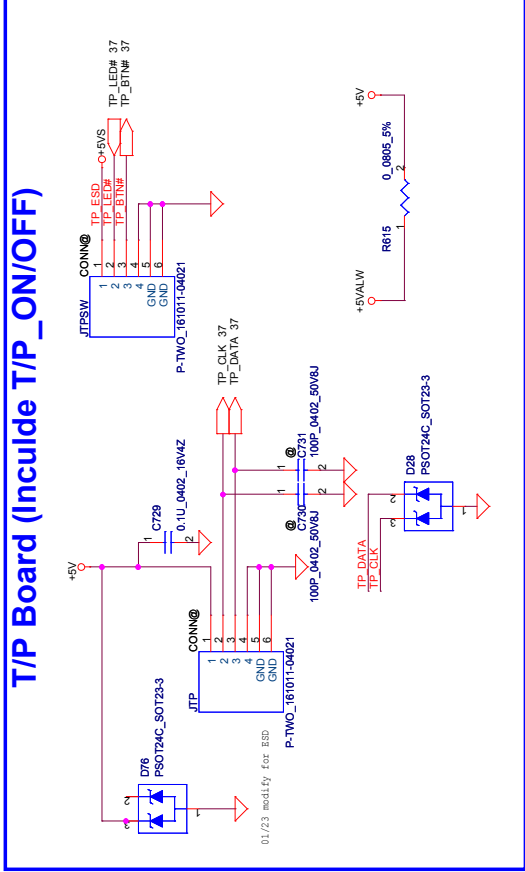
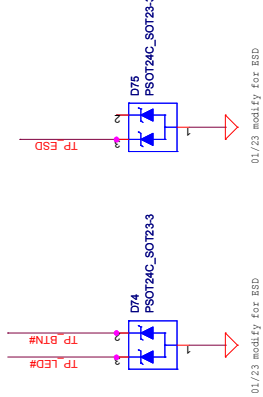
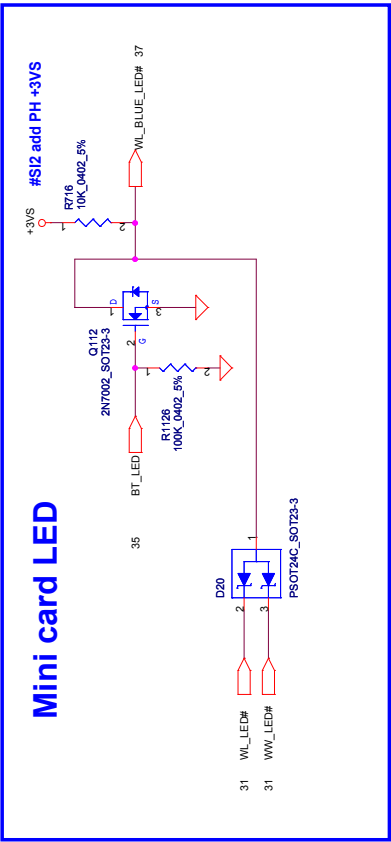
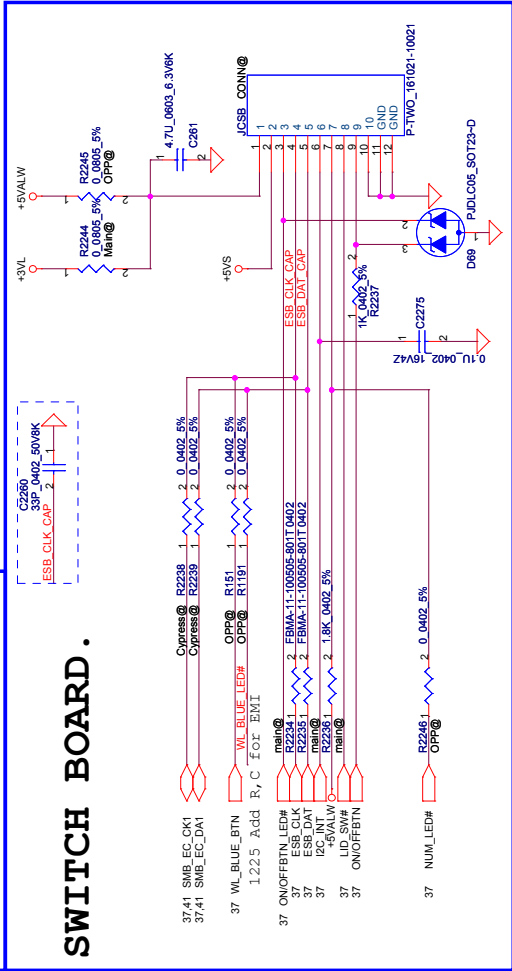
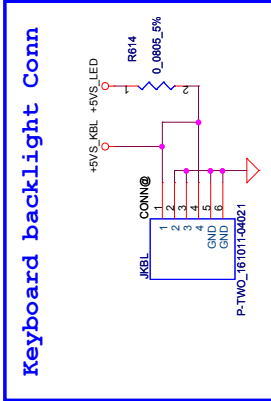
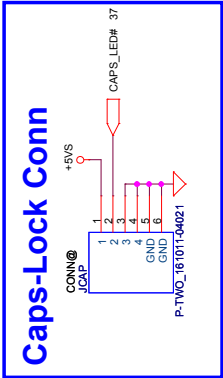
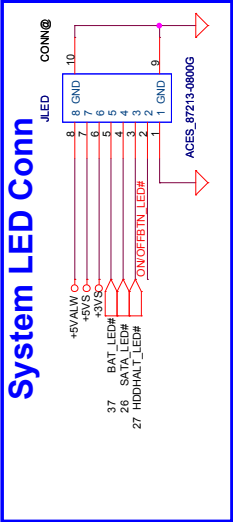
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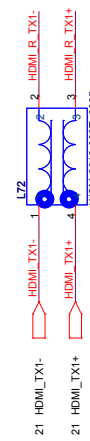
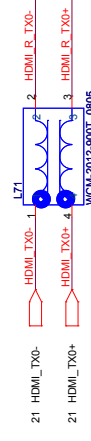
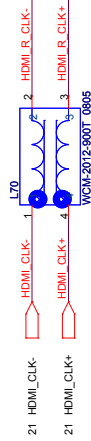
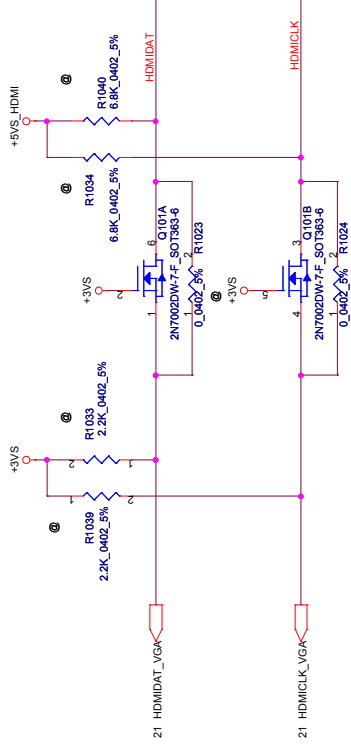
Audio connector



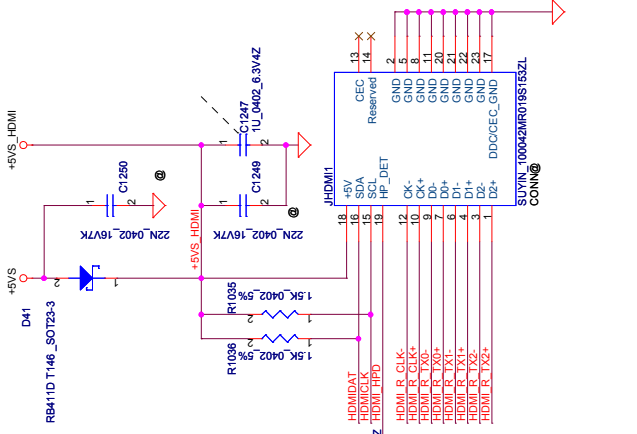
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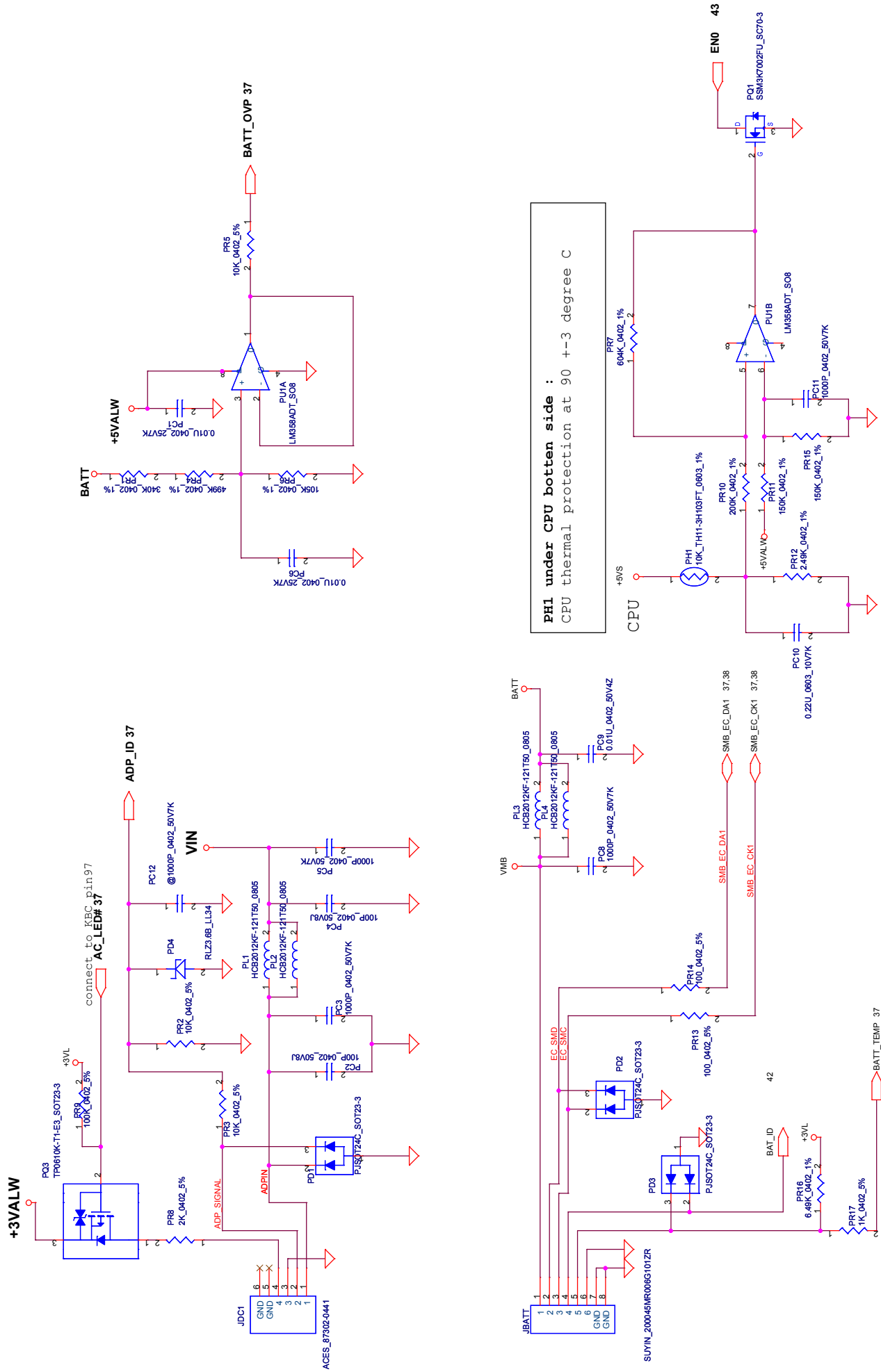


HDMI Connector



for HDMI certification

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Date:		Monday, February 16, 2009		Sheet	41 of 51

Compal Electronics, Inc.

DC Connector/CPU OTP

Montevina Consumer Discrete

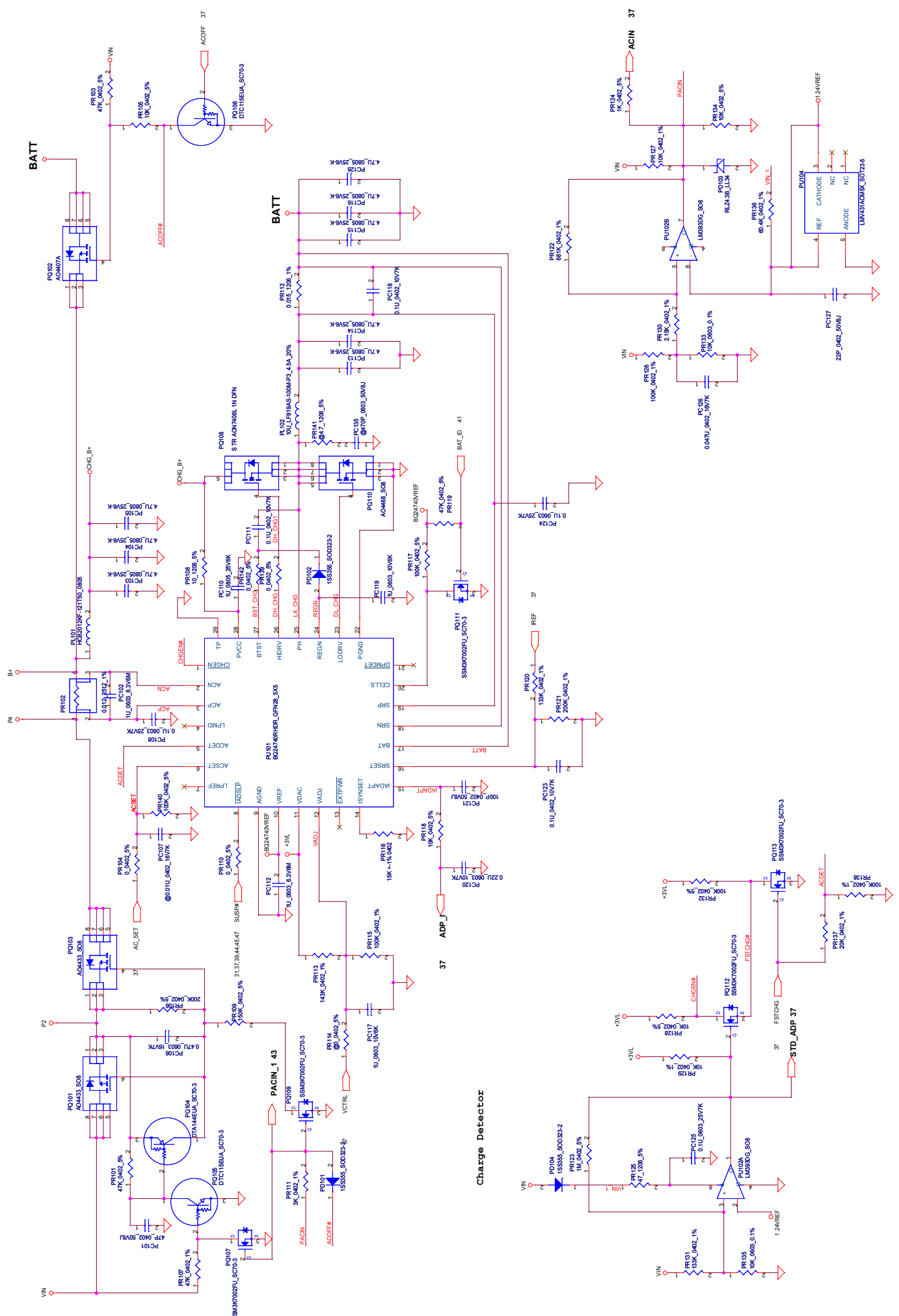
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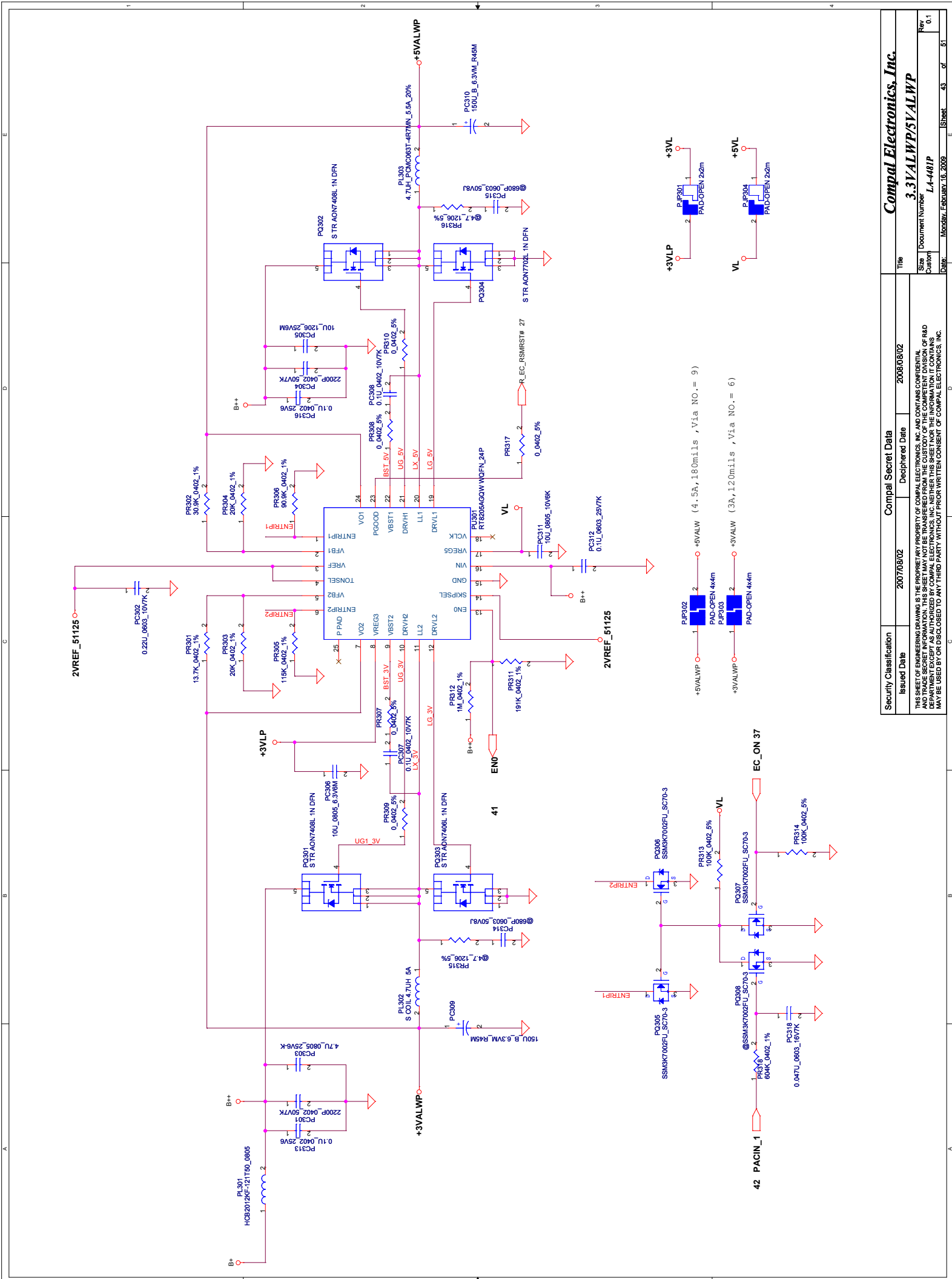
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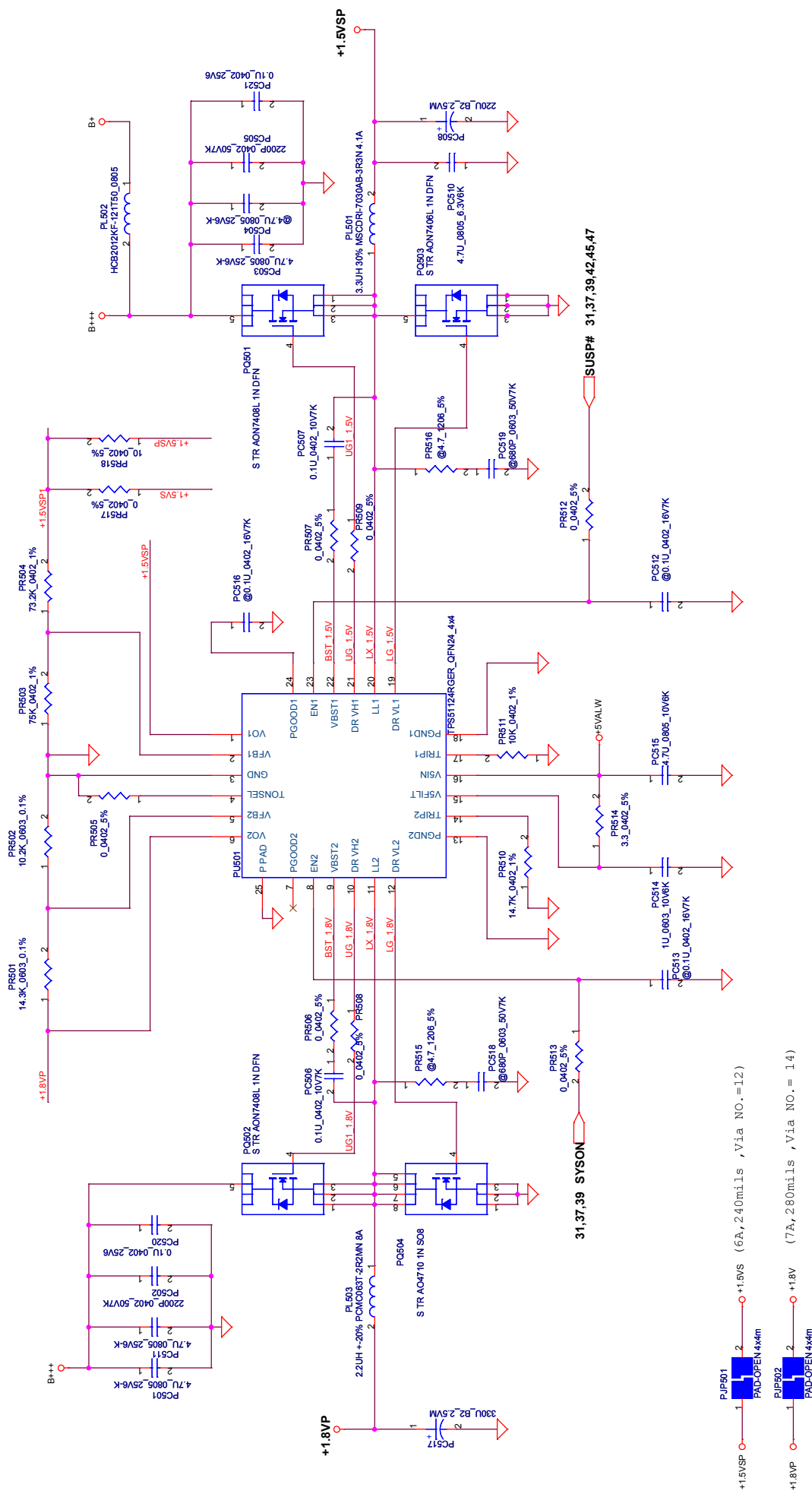
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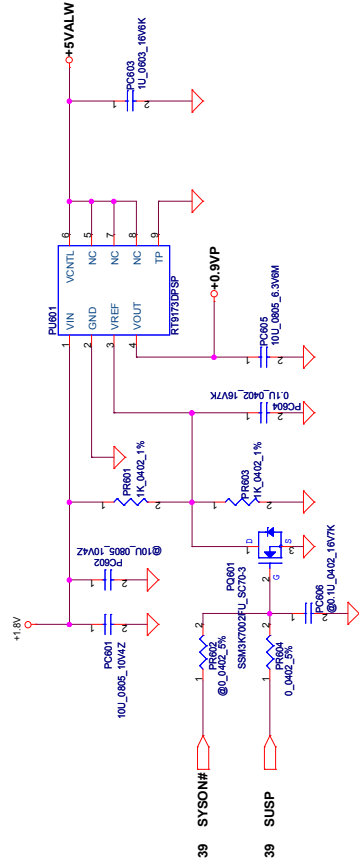
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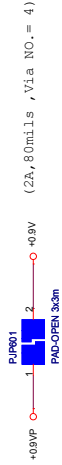


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39 SYSON#

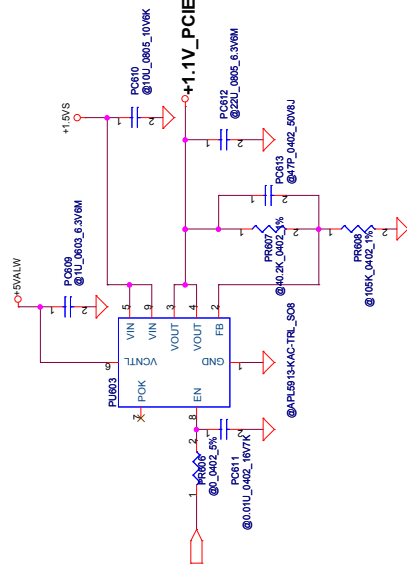
39 SUSP



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31,37,39,42,44,47 SUSP#

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0.9VP/1.1V_PCIE

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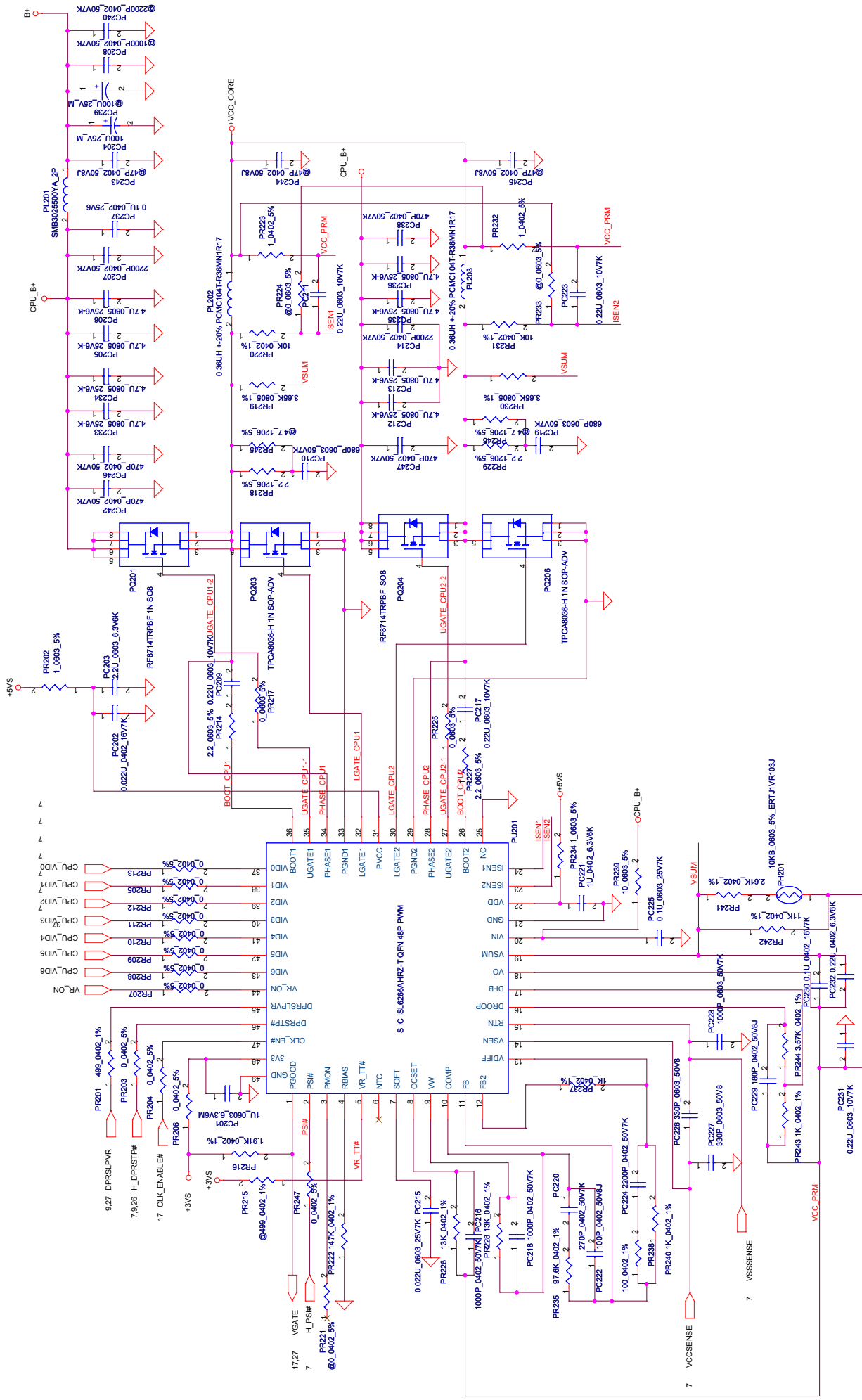
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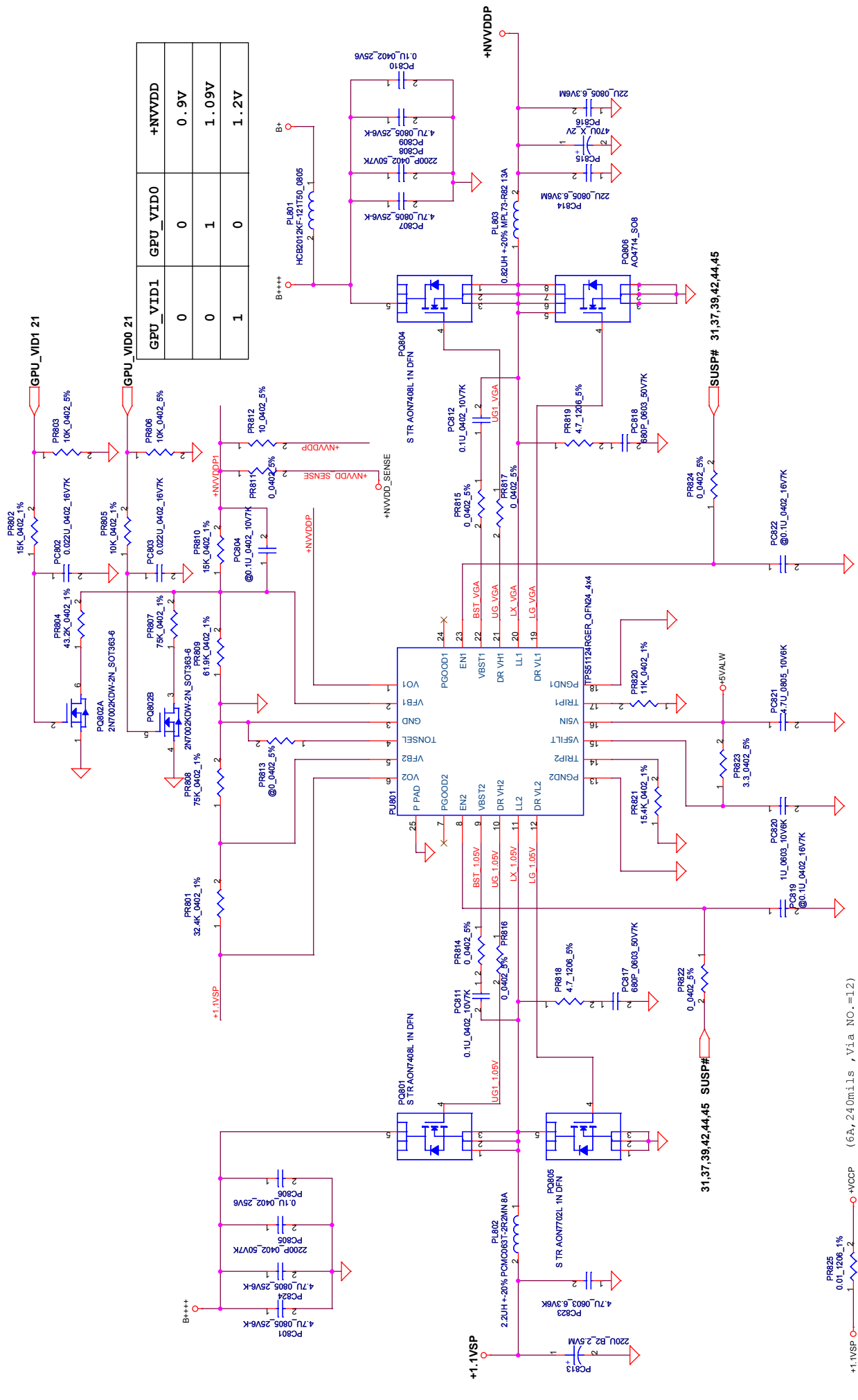


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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	CardReader clock issue	17	Using USB_0 for CLK_48M_CR	2008/10/08	SI-1
2	Debug Card issue	31	Connect PLT_RST# to JP7.A17	2008/10/08	SI-1
3	delete VGA external thermal sensor layout location for layout space limitation	29	Del U6,C348,C350	2008/10/08	SI-1
4	Add Audio board	34	Add AUDIO connector for audio board	2008/10/08	SI-1
5	delete VGA JTAG for layou space limitation	29	Delete T47,T48,T49,T50,T51	2008/10/08	SI-1
6	Cap board issue	38	Change Cap board power rail to +3VL	2008/10/08	SI-1
7	Change JFPR to 6 pin connector	35	change JFPR	2008/10/08	SI-1
8	Change FAN control circuit to voltage control	6	Add U51,D17,R50,C41	2008/10/08	SI-1
9	Delete HDA SSC	26	Remove U44 for layout spacing	2008/10/08	SI-1
10	For PR mini card connector	31	Add R2252 -- R2261	2008/10/08	SI-1
11	PA/PR CardReader LED	32	D72 for PA, D71 for PR	2008/10/08	SI-1
12	EMI request	33	Change R2205 to L76	2008/10/08	SI-1
13	change MIC to 2pin and add SPK connector	34		2008/10/08	SI-1
14	Speaker L & R reverse	34		2008/11/20	SI-2
15	JFPR change to 4 pin	40	Add U58,C2265	2008/11/20	SI-2
16	add buffer on detect pin for certification item 7-12	34		2008/11/20	SI-2
17	Bom Error [Bug: BT led fail]	38	Change D20's Part number to SCA00000G00	2008/12/10	PV
18	Realtek suggest us to change Cap value	30	Change C2193 value from 0.1uF to 1uF	2008/12/10	PV
19	Slove WVLAN Noise : Add Cap X4 [to GND]	26	C499 and C2130 default mount, Add C2266 and C2267 [12 PF]	2008/12/10	PV
20	Slove WVLAN Noise:Add Cap,change R191val	37	Add C2268 [22PF] on R191.2 to GND and R191 change to 47 ohm	2008/12/10	PV
21	Slove WVLAN Noise:C356,C357 default mou	21	C356 and C357 default mount	2008/12/10	PV
22	Slove SMT issue	37	Change U30 FOOTPRINT [fromKB926QFA1 LQFP128_14X14 change to ECE5028-NU VTQFP128_14X14]		PV
23	Slove SMT issue	37	Change JKB FOOTPRINT [from ACES_85202-24051_24P change to ACES_85202-24051_24P-S]	2008/12/10	PV
24	Slove ESD issue	26	ADD C2269 [0.1uF] on BAT1.1 trace (pin 1)	2008/12/17	PV
25	Slove ESD issue	33	Add one Diode [D73] on MIC_EXTR, MIC_EXTL (near chip side)	2008/12/17	PV
26	Slove ESD issue	33	Change cap value [C2270,C2271,C2272,C2273] to 0.1uF	2008/12/17	PV
27	Slove Audio issue	34	Change cap value to 2.2uF [C2239,C2240]	2008/12/17	PV
28	Slove non-RoHS Part	30	Change C2157,C2160,C2215 and C2217 Part number [from SE070104Z00 to SE070104Z80]	2008/12/17	PV

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
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