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N480 MB Schematics Document

Intel Ivy Bridge/Sandy Bridge Processor with PantherPoint HM76/HM70+ DDRIII

MotherBoard version：BM5238 Rev1.2

2012-04-09

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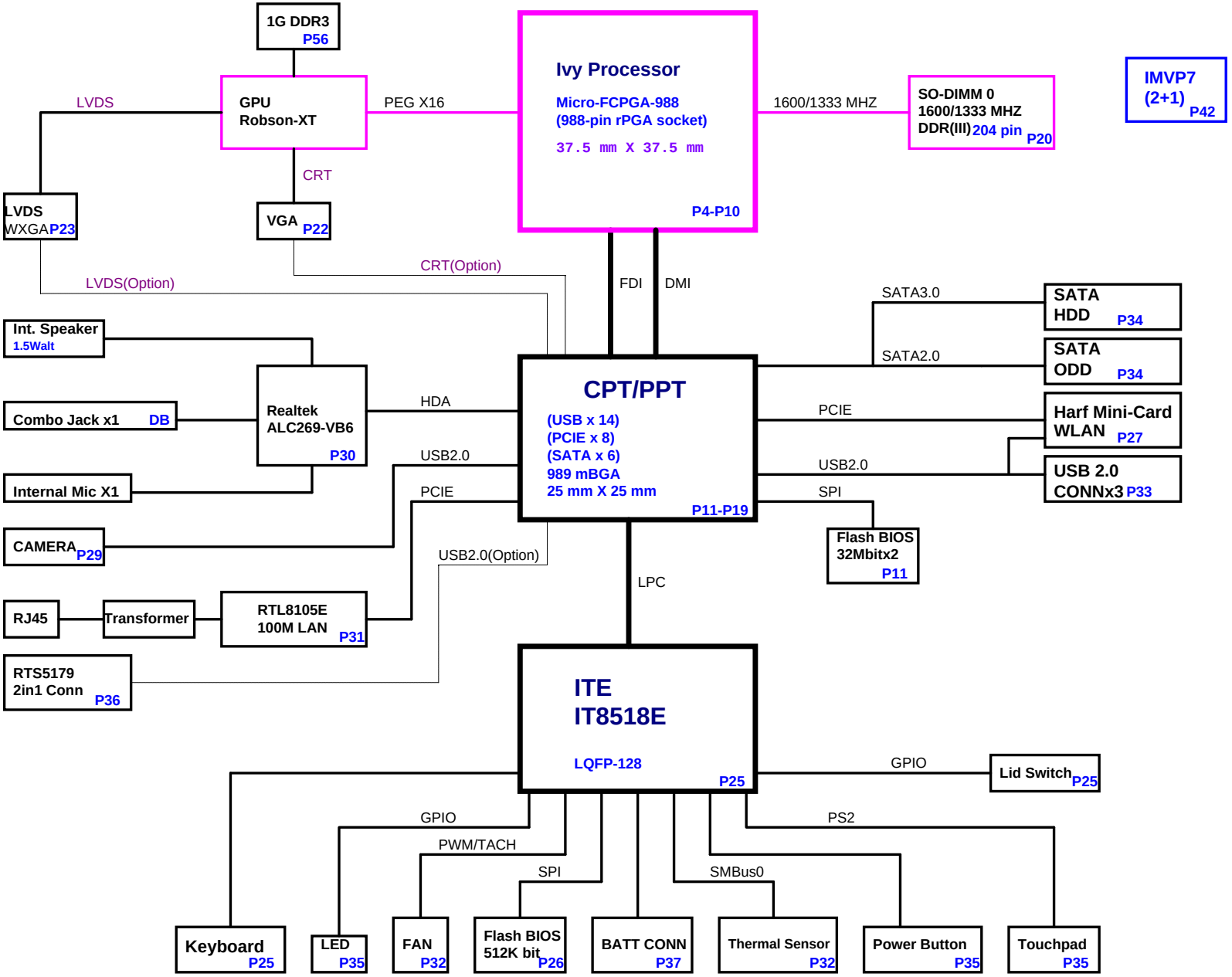

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Title	Block Diagram	
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Power Annotations

Power Plane	Description
AD+	Adapter power supply (19V)
DCBATOUT	AC or battery power rail for power circuit.
VHCORE	Core voltage for CPU
+0_75V	0_75VRUN LDO power rail for DDR terminator
+1_05VRUN	1.05V switched power rail
+1.0V_VCCP	VCCP switched power rail
+1_5VSUS	1.5V power rail for DDR
+1_5V_CPU	1.5V switched power rail
+1_8VRUN	1.8V power rail for system
+3VALW	3.3V always on power rail
+3VSUS	3.3V power rail for SB
+V3.3M_LAN	3.3V power rail for LAN
+3VRUN	3.3V switched power rail
+5VALW	5V always on power rail
+5VSUS	5V switched power rail
+5VRUN	5V switched power rail
+3VALW_LDO	3.3V power from TPS51125 LDO
+5VALW_LDO	5V power from TPS51125 LDO
+VCCSA	SA voltage for CPU
GFXCORE	GFXCORE voltage for CPU Graphic
+VDDC	CORE Power for discete GPU

Voltage Rails

State \ Power Plane	DCBATOUT +3VALW_LDO +5VALW_LDO	AD+ +3VALW +V3.3M_LAN +5VALW	+1_5VSUS +3VSUS +5VSUS	+0_75V +1_05VRUN +1.05V_VCCP +VCCSA VHCORE +1_5V_CPU +1_8VRUN +3VRUN +5VRUN GFXCORE +VDDC
S0	ON	ON	ON	ON
S3	ON	ON	ON	OFF
S4&S5 (AC)	ON	ON	OFF	OFF
S3&S4 (Battery only)	ON	OFF	OFF	OFF
S3&S4 (AC&Battery don't exist)	OFF	OFF	OFF	OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor for DDR&VR	1001 100X b

CPT/PPT SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM1	1001 010Xb
Debug Port	1100 1000 b

CPT/PPT SM Bus0 address

Device	Address

CPT/PPT SM Bus1 address

Device	Address
EC	

SMBUS Control Table

X V

	SOURCE	VGA	BATT	EC	DIMM	WLAN WWAN	Thermal Sensor	PCH	GPU	LAN
SMB_EC_CK0 SMB_EC_DA0	IT8105E +3VALW		V +ECVCC	X	X					
SMB_EC_CK1 SMB_EC_DA1	IT8105E +3VALW		X	X	X					
SMBCLK SMBDATA	PCH +3VALW		X	X	V +3VALW					
SML0CLK SML0DATA	PCH +3VALW		X	X	X					
SML1CLK SML1DATA	PCH +3VALW		X	V +3VALW	X					

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+V*SUS	+V*RUN	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

+ECVCC	3.3V 5%
R386	100K 5%

Board ID	R387	V min	V typ	V max	Phase
0	0	0V	0V	0V	REV1.0
1	8.2K 5%	0.216V	0.250V	0.289V	REV1.1
2	18K 5%	0.436V	0.503V	0.538V	REV1.2
3	33K 5%	0.712V	0.819V	0.875V	REV1.3

USB Port Table

	USB PORT	Function	OC pin
USB 2.0	PORT-0	Ext. Port(MB)	
	PORT-1	Ext. Port(MB)	OC#0
	PORT-2		OC#1
	PORT-3	Card reader	
	PORT-4		OC#2
	PORT-5		
	PORT-6		OC#3
	PORT-7		
	PORT-8		OC#4
	PORT-9	Ext. Port(DB)	
	PORT-10	BT	OC#5
	PORT-11	CAMERA	
	PORT-12		OC#6
	PORT-13		
USB 3.0	PORT-0		
	PORT-1		
	PORT-2		
	PORT-3		

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+1_05VRUN 5,7,11,13,17,18,26,40,42,44,48,49,51,52

CAD NOTE: PEG_ICOMPI and RCOMPO signals should be shorted and routed with
- max length = 500 mils
- typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with
- max length = 500 mils
- typical impedance = 14.5 mohms

add by lihong 0504

R7 2 1 1K_J R0402 GPU FDI_FSYNC0
R8 2 1 1K_J R0402 GPU FDI_FSYNC1
R40 2 1 1K_J R0402 GPU FDI_INT
R41 2 1 1K_J R0402 GPU FDI_LSYNC0
R42 2 1 1K_J R0402 GPU FDI_LSYNC1

CAD NOTE: DP_COMPIO and ICOMPO signals should be shorted near balls and routed with
- typical impedance < 25 mohms

+1_05VRUN
R2 24.9_F r0402
DP_COMP

+1_05VRUN

del R3 lihong 0504

U55A

13 DMI_TXN[3:0]
DMI_TXN0 B27 DMI_RX#[0]
DMI_TXN1 B25 DMI_RX#[1]
DMI_TXN2 A25 DMI_RX#[2]
DMI_TXN3 B24 DMI_RX#[3]

13 DMI_TXP[3:0]
DMI_TXP0 B28 DMI_RX[0]
DMI_TXP1 B26 DMI_RX[1]
DMI_TXP2 A24 DMI_RX[2]
DMI_TXP3 B23 DMI_RX[3]

13 DMI_RXN[3:0]
DMI_RXN0 G21 DMI_TX#[0]
DMI_RXN1 E22 DMI_TX#[1]
DMI_RXN2 F21 DMI_TX#[2]
DMI_RXN3 D21 DMI_TX#[3]

13 DMI_RXP[3:0]
DMI_RXP0 G22 DMI_TX[0]
DMI_RXP1 D22 DMI_TX[1]
DMI_RXP2 F20 DMI_TX[2]
DMI_RXP3 C21 DMI_TX[3]

DMI

13 FDI_TXN[7:0]
FDI_TXN0 A21 FDI0_TX#[0]
FDI_TXN1 H19 FDI0_TX#[1]
FDI_TXN2 E19 FDI0_TX#[2]
FDI_TXN3 F18 FDI0_TX#[3]
FDI_TXN4 B21 FDI1_TX#[0]
FDI_TXN5 C20 FDI1_TX#[1]
FDI_TXN6 D18 FDI1_TX#[2]
FDI_TXN7 E17 FDI1_TX#[3]

13 FDI_TXP[7:0]
FDI_TXP0 A22 FDI0_TX[0]
FDI_TXP1 G19 FDI0_TX[1]
FDI_TXP2 E20 FDI0_TX[2]
FDI_TXP3 G18 FDI0_TX[3]
FDI_TXP4 B20 FDI1_TX[0]
FDI_TXP5 C19 FDI1_TX[1]
FDI_TXP6 D19 FDI1_TX[2]
FDI_TXP7 F17 FDI1_TX[3]

Intel(R) FDI

13 FDI_FSYNC0 J18 FDI0_FSYNC
13 FDI_FSYNC1 J17 FDI1_FSYNC
13 FDI_INT H20 FDI_INT
13 FDI_LSYNC0 J19 FDI0_LSYNC
13 FDI_LSYNC1 H17 FDI1_LSYNC

A18 eDP_COMPIO
A17 eDP_ICOMPO
B16 eDP_HPD#
C15 eDP_AUX
D15 eDP_AUX#
C17 F16 C16 G15 eDP_TX[0:3]
C18 E16 D16 F15 eDP_TX#[0:3]

eDP

PCI EXPRESS* - GRAPHICS

PEG_ICOMPI J22
PEG_ICOMPO J21
PEG_RCOMPO H22

+1_05VRUN
PEG_COMP R1 1 2 24.9_F r0402

PEG_RX#[0] K33 GFX_RX0N_C 48
PEG_RX#[1] M35 GFX_RX1N_C 48
PEG_RX#[2] L34 GFX_RX2N_C 48
PEG_RX#[3] J35 GFX_RX3N_C 48
PEG_RX#[4] J32 GFX_RX4N_C 48
PEG_RX#[5] H34 GFX_RX5N_C 48
PEG_RX#[6] H31 GFX_RX6N_C 48
PEG_RX#[7] G33 GFX_RX7N_C 48
PEG_RX#[8] G30 GFX_RX8N_C 48
PEG_RX#[9] F35 GFX_RX9N_C 48
PEG_RX#[10] E34 GFX_RX10N_C 48
PEG_RX#[11] E32 GFX_RX11N_C 48
PEG_RX#[12] D33 GFX_RX12N_C 48
PEG_RX#[13] D31 GFX_RX13N_C 48
PEG_RX#[14] B33 GFX_RX14N_C 48
PEG_RX#[15] C32 GFX_RX15N_C 48

PEG_RX[0] J33 GFX_RX0P_C 48
PEG_RX[1] L35 GFX_RX1P_C 48
PEG_RX[2] K34 GFX_RX2P_C 48
PEG_RX[3] H35 GFX_RX3P_C 48
PEG_RX[4] H32 GFX_RX4P_C 48
PEG_RX[5] G34 GFX_RX5P_C 48
PEG_RX[6] G31 GFX_RX6P_C 48
PEG_RX[7] F33 GFX_RX7P_C 48
PEG_RX[8] F30 GFX_RX8P_C 48
PEG_RX[9] E35 GFX_RX9P_C 48
PEG_RX[10] E33 GFX_RX10P_C 48
PEG_RX[11] F32 GFX_RX11P_C 48
PEG_RX[12] D34 GFX_RX12P_C 48
PEG_RX[13] E31 GFX_RX13P_C 48
PEG_RX[14] C33 GFX_RX14P_C 48
PEG_RX[15] B32 GFX_RX15P_C 48

PEG_TX#[0] M29 C3510 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX0N_C 48
PEG_TX#[1] M32 C3511 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX1N_C 48
PEG_TX#[2] M31 C3512 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX2N_C 48
PEG_TX#[3] L32 C3513 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX3N_C 48
PEG_TX#[4] L29 C3514 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX4N_C 48
PEG_TX#[5] K31 C3515 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX5N_C 48
PEG_TX#[6] K28 C3516 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX6N_C 48
PEG_TX#[7] J30 C3517 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX7N_C 48
PEG_TX#[8] J28 C3502 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX8N_C 48
PEG_TX#[9] H29 C3503 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX9N_C 48
PEG_TX#[10] G27 C3504 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX10N_C 48
PEG_TX#[11] E29 C3505 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX11N_C 48
PEG_TX#[12] F27 C3506 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX12N_C 48
PEG_TX#[13] D28 C3507 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX13N_C 48
PEG_TX#[14] F26 C3508 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX14N_C 48
PEG_TX#[15] E25 C3509 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX15N_C 48

PEG_TX[0] M28 C3518 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX0P_C 48
PEG_TX[1] M33 C3519 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX1P_C 48
PEG_TX[2] M30 C3520 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX2P_C 48
PEG_TX[3] L31 C3521 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX3P_C 48
PEG_TX[4] L28 C3522 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX4P_C 48
PEG_TX[5] K30 C3523 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX5P_C 48
PEG_TX[6] K27 C3524 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX6P_C 48
PEG_TX[7] J29 C3525 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX7P_C 48
PEG_TX[8] J27 C3526 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX8P_C 48
PEG_TX[9] H28 C3527 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX9P_C 48
PEG_TX[10] G28 C3528 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX10P_C 48
PEG_TX[11] E28 C3529 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX11P_C 48
PEG_TX[12] F28 C3530 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX12P_C 48
PEG_TX[13] D27 C3531 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX13P_C 48
PEG_TX[14] E26 C3532 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX14P_C 48
PEG_TX[15] D25 C3533 1 2 0.1uF/10V,X5R c0402 GPU GFX_TX15P_C 48

0.22uF->0.1uF lihong 0626

In order to support Gen 3 PCI Express Graphic,
the value of the AC coupling capacitor should be 180 - 265 nF.
As for Gen2 PCI Express ,the value of the AC coupling capacitor should be 100 - 220 nF

MXM3.0 need put the CAP on the motherboard.
Close to the MXM Slot

Ivy_Bridge_rPGA_Rev0p7
mpga989_mcp_skt_37-5mm_sq_HR

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Title	CPU(DMI,DP,PEG,FDI)	
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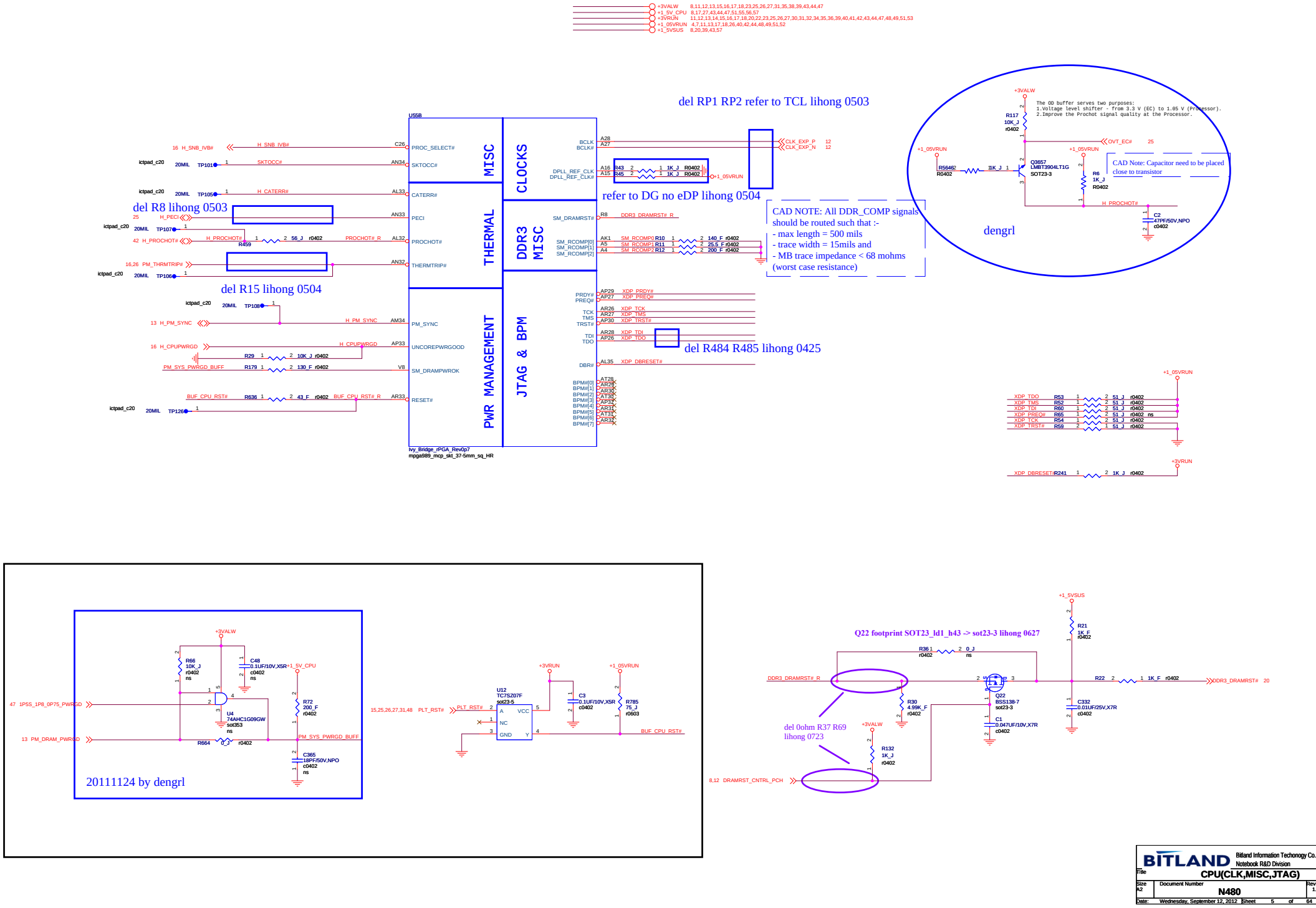

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Title	CPU(CLK,MISC,JTAG)	
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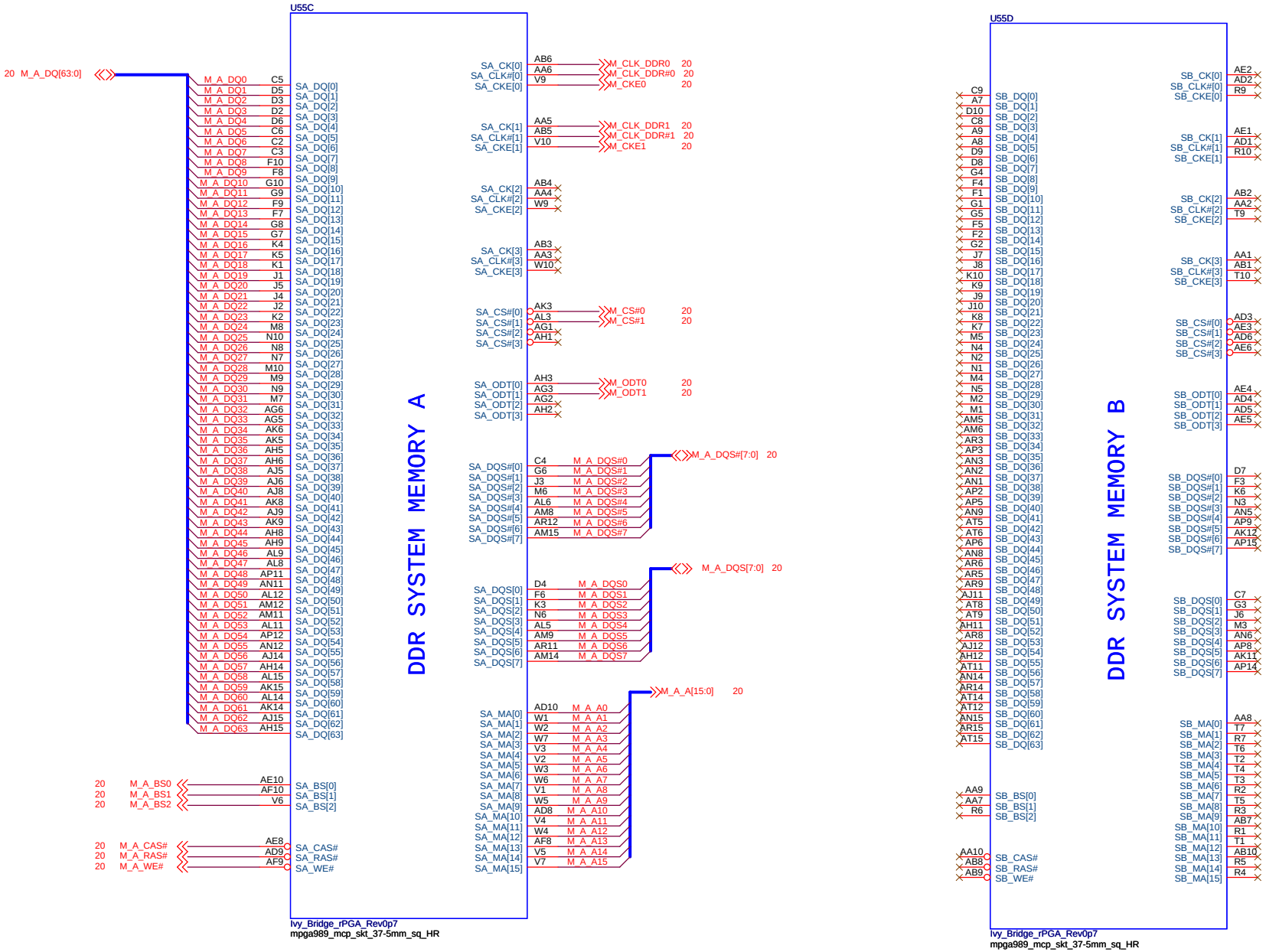

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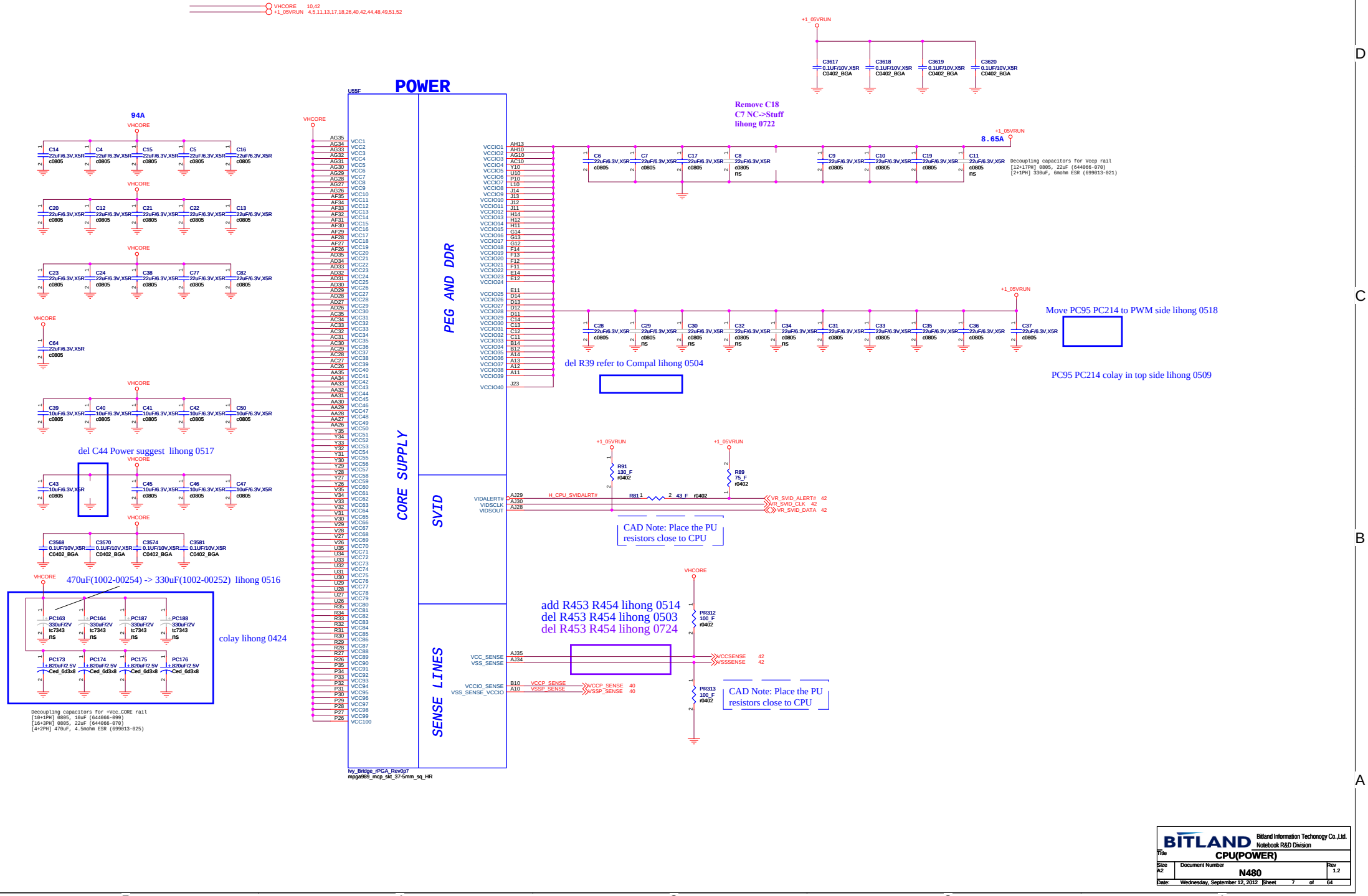
POWER



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POWER

add R532 R658 lihong 0514
del R532 R658 lihong 0503

del 0ohm R470
lihong 0723

CAD Note: All traces starting with +V_SM_VREF* and DDR_WR_VREF* should have 20:20mils wherever possible

dengrl

S3 circuit:- 1.5V input to IVB is gated & IVB Read Vref 0.75V is gated

38A

del reserved PC229 PC304

470uF(1002-00254) ->
330uF(1002-00252) lihong 0516

colay lihong 0424

max 5A

move C71 to Page39 lihong 0509

实测电流值(SNB)0.3857A lihong 0720

4.5A

C139 ns lihong 0423
C139 7343->3528 in top side lihong 0424

0.93A

del R7 lihong 0503

C91 C89 1uF/25V -> 1uF/6.3V
lihong 0502

Provides 1.0/1.05V selectable via VCCIO_SEL
refer EDS PR235 should NC for chief river lihong

Co_lay
C88 ns lihong 0423
PC90(7343) C88(3528)->3528 0805 lihong 0502
del PC90 C88 lihong 0509
add C196 C197 place near CPU lihong 0514

Function	xxVccSA_Select[1] [[CPU PIN# C24 VID0 of VR]]	xxVccSA_Select[0] [[CPU PIN# C22 VID1 of VR]]	VCCSA VR Vout
SNB HIGH	0	0	0.90V
IVB HIGH	0	1	0.725V
SNB LOW	1	0	0.80V
IVB LOW	1	1	0.675V

PROCESSOR DRIVEN Vref PATH WAS STUFFED BY DEFAULT:

Q41 footprint sot23_ld1_lp20 -> sot23-3 lihong 0620

CAD Note: Route with min. trace width of 10 mils 0.1uF capacitors need to be placed as close as possible to voltage divider

删除Q42及预留的R252 R5385 lihong 0516
no DDR_WR_VREF01

The FETs are needed in order to avoid potential leakage while system is in S3 state DRAMRST_CNTRL signal and FETs (with low Rdson) are required for S3 Power Reduction Circuitry. If the S3 Power Reduction Circuit isn't implemented than these FETs can be unstuffed and R251 and R252 would have to be stuffed

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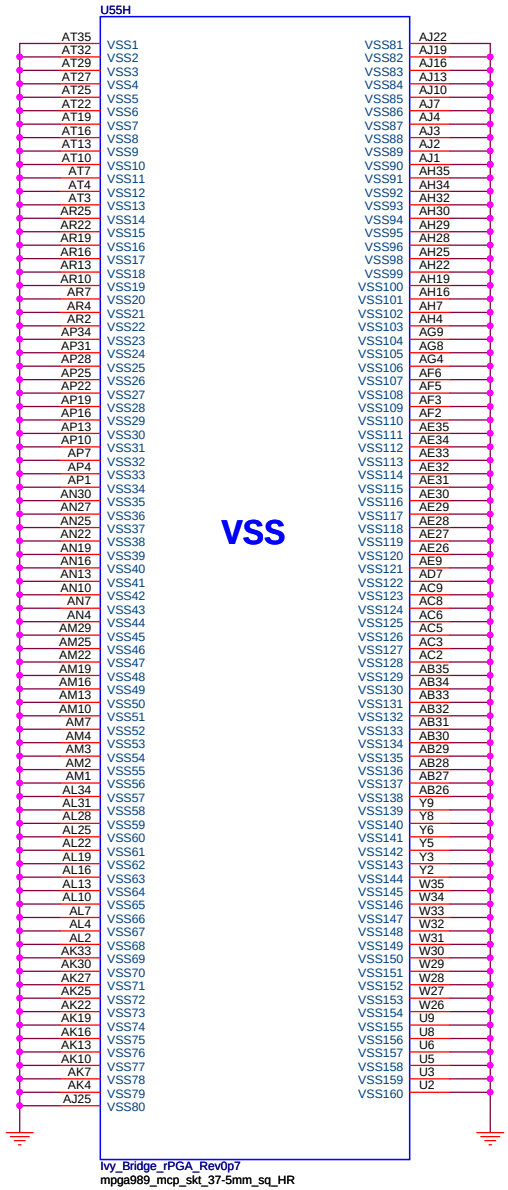

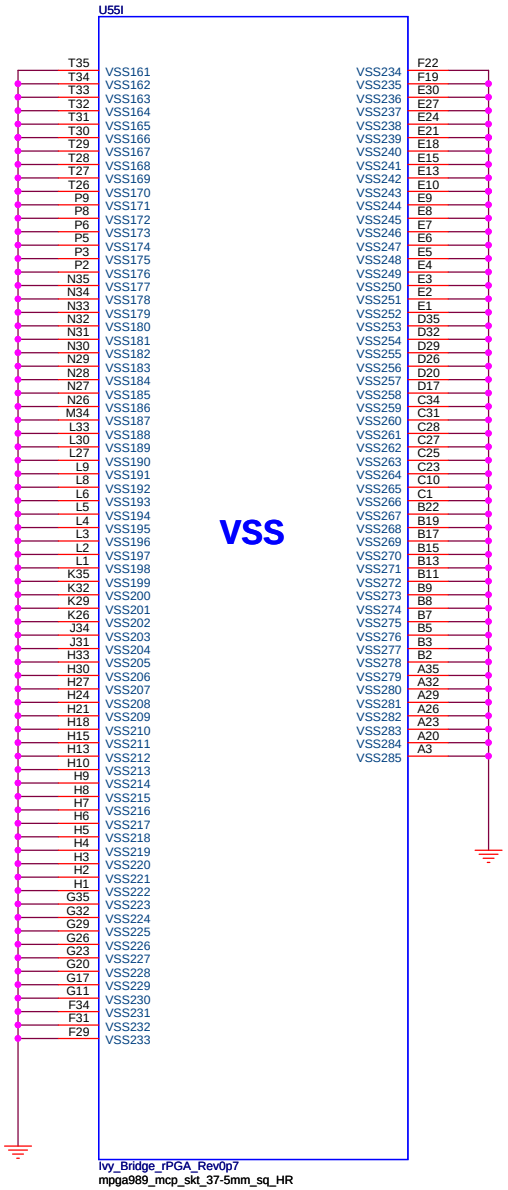

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Title: CPU(GND)			
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GFXCORE 8,42
VHCORE 7,42

GFXCORE
R200 49.9_F r0402 ns
R184 49.9_F r0402 ns
R198 49.9_F r0402 ns
VAXG_VAL_SENSE
VSSAXG_VAL_SENSE

CAD NOTE:Floating for probe use,

VHCORE
R191 49.9_F r0402 ns
R149 49.9_F r0402 ns
R174 49.9_F r0402 ns

CAD NOTE:Floating for probe use,

CFG2 1:(Default) Normal Operation; Lane # definition matches socket pin map definition
CFG2 0:Lane Reversed

CFG2
R55 1K_F r0402 ns

CGF[6: 5]
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG6
R57 1K_F r0402 ns
CFG5
R58 1K_F r0402 ns

CFG7 1: (Default) PEG Train immediately following xxRESETB de assertion
CFG7 0: PEG Wait for BIOS for training

CFG7
R62 1K_F r0402 ns

CFG4
R56 1K_J r0402 ns

CGF4 1:Disabled; No Physical Display Port attached to Embedded Display Port
CGF4 0:Enabled; An external Display Port device is connected to the Embedded Display Port

U55E

CFG0 AK28 CFG[0]
CFG1 AK29 CFG[1]
CFG2 AL26 CFG[2]
CFG3 AL27 CFG[3]
CFG4 AK26 CFG[4]
CFG5 AL29 CFG[5]
CFG6 AL30 CFG[6]
CFG7 AM31 CFG[7]
CFG8 AM32 CFG[8]
CFG9 AM30 CFG[9]
CFG10 AM28 CFG[10]
CFG11 AM26 CFG[11]
CFG12 AN28 CFG[12]
CFG13 AN31 CFG[13]
CFG14 AN26 CFG[14]
CFG15 AM27 CFG[15]
CFG16 AK31 CFG[16]
CFG17 AN29 CFG[17]
CFG

VAXG_VAL_SENSE AJ31 VAXG_VAL_SENSE
VSSAXG_VAL_SENSE AH31 VSSAXG_VAL_SENSE
TP_H_CPU_RSVD3 AJ33 VCC_VAL_SENSE
TP_H_CPU_RSVD4 AH33 VSS_VAL_SENSE

AJ26 RSVD5

F25 RSVD8
F24 RSVD9
F23 RSVD10
D24 RSVD11
G25 RSVD12
G24 RSVD13
E23 RSVD14
D23 RSVD15
C30 RSVD16
A31 RSVD17
B30 RSVD18
B29 RSVD19
D30 RSVD20
B31 RSVD21
A30 RSVD22
C29 RSVD23

J20 RSVD24
B18 RSVD25

J15 RSVD27

RESERVED

VCC_DIE_SENSE AH27 1 TP45 20MIL ictv20_10
VSS_DIE_SENSE AH26 1 TP133 20MIL ictv20_10

RSVD28 L7
RSVD29 AG7
RSVD30 AE7
RSVD31 AK2
RSVD32 W8
RSVD33 AT26
RSVD34 AM33
RSVD35 AJ27
RSVD37 T8
RSVD38 J16
RSVD39 H16
RSVD40 G16
RSVD_NCTF1 AR35
RSVD_NCTF2 AT34
RSVD_NCTF3 AT33
RSVD_NCTF4 AP35
RSVD_NCTF5 AR34
RSVD_NCTF6 B34
RSVD_NCTF7 A33
RSVD_NCTF8 A34
RSVD_NCTF9 B35
RSVD_NCTF10 C35
RSVD51 AJ32
RSVD52 AK32

BCLK_ITP AN35 CLK_XDP_ITP_P 1 TP40 20MIL ictv20_10
BCLK_ITP# AM35 CLK_XDP_ITP_N 1 TP41 20MIL ictv20_10

RSVD_NCTF11 AT2
RSVD_NCTF12 AT1
RSVD_NCTF13 AR1
KEY B1

Ivy_Bridge_rPGA_Rev0p7
mpga989_mcp_skt_37-5mm_sq_HR

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Title: CPU(RESERVED)

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A3	N480	1.2

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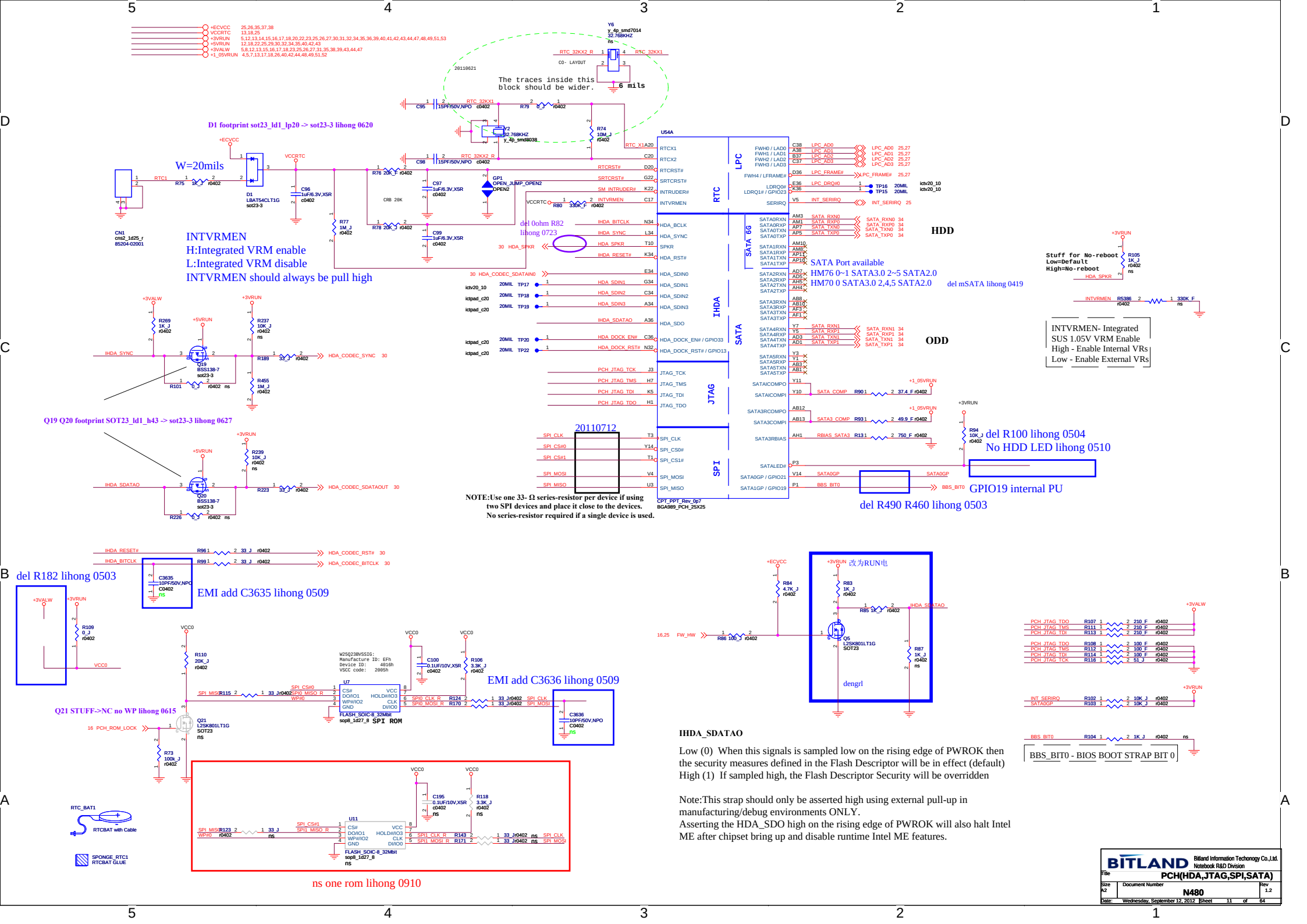
D1 footprint sot23_ld1_lp20 -> sot23-3 lihong 0620
W=20mils
INTVRMEN
H:Integrated VRM enable
L:Integrated VRM disable
INTVRMEN should always be pull high
del 0ohm R82
lihong 0723
The traces inside this block should be wider.
6 mils
CO- LAYOUT
20110621
SATA Port available
HM76 0~1 SATA3.0 2~5 SATA2.0
HM70 0 SATA3.0 2,4,5 SATA2.0
del mSATA lihong 0419
HDD
ODD
Stuff for No-reboot
Low=Default
High=No-reboot
INTVRMEN- Integrated
SUS 1.05V VRM Enable
High - Enable Internal VRs
Low - Enable External VRs
Q19 Q20 footprint SOT23_ld1_h43 -> sot23-3 lihong 0627
20110712
NOTE:Use one 33- Ω series-resistor per device if using two SPI devices and place it close to the devices. No series-resistor required if a single device is used.
del R490 R460 lihong 0503
del R100 lihong 0504
No HDD LED lihong 0510
GPIO19 internal PU
del R182 lihong 0503
EMI add C3635 lihong 0509
EMI add C3636 lihong 0509
Q21 STUFF->NC no WP lihong 0615
ns one rom lihong 0910
dengrl
IHDA_SDATAO
Low (0) When this signals is sampled low on the rising edge of PWROK then the security measures defined in the Flash Descriptor will be in effect (default)
High (1) If sampled high, the Flash Descriptor Security will be overridden
Note:This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
Asserting the HDA_SDO high on the rising edge of PWROK will also halt Intel ME after chipset bring up and disable runtime Intel ME features.
BBS_BIT0 - BIOS BOOT STRAP BIT 0
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Notebook R&D Division
PCH(HDA,JTAG,SPI,SATA)
N480
Wednesday, September 12, 2012

PCI-E Port Table

Port	Function
Port1	Un-used
Port2	WLAN
Port3	LAN
Port4	Un-used
Port5	Un-used
Port6	Un-used
Port7	Test point
Port8	Un-used

WIFI Port1->Port2 lihong 0615

Close to PCH

PCIE Port available
HM76 1~8
HM70 1~4

del 0ohm R47 R48 R20
lihong 0723

dengrl
N401 to GPU Thermal sensor
change port to SM1CLK

del 0ohm R266 R362
lihong 0723

refer to DG no eDP lihong 0504

R31 NC->Stuff lihong 0720

Configure Flex1 and Flex3 as 27MHZ 48MHZ lihong 0411

del 0ohm R155 R157
lihong 0723

DIMM0
DIMM1

EC
Thermal Sensor

CPT_PPT_Rev_0p7
BGA989_PCH_25X25

Title	PCH(PCI-E,SMBUS,CLK)		
Size A3	Document Number N480		Rev 1.2
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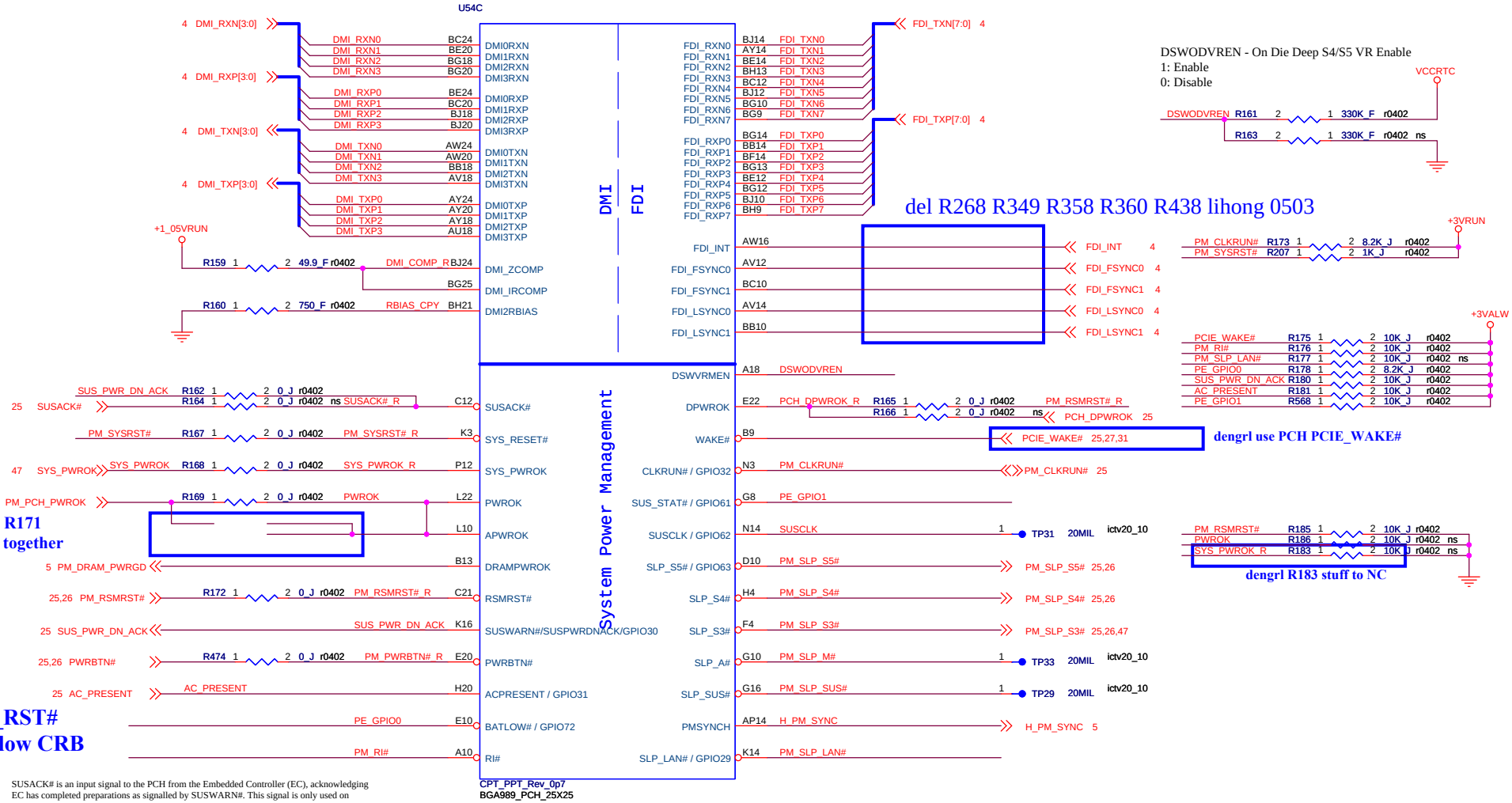
+3VRUN 5,11,12,14,15,16,17,18,20,22,23,25,26,27,30,31,32,34,35,36,39,40,41,42,43,44,47,48,49,51,53
+3VALW 5,8,11,12,15,16,17,18,23,25,26,27,31,35,38,39,43,44,47
VCCRTC 11,18,25
+1_05VRUN 4,5,7,11,17,18,26,40,42,44,48,49,51,52



SUSACK# is an input signal to the PCH from the Embedded Controller (EC), acknowledging EC has completed preparations as signalled by SUSWARN#. This signal is only used on platforms that support the Deep S4/S5 state.
SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep S4/S5 state entry and exit.

APWROK:For platforms not supporting Intel AMT it can be connected to PWROK

PWRBTN#:This signal is internally pulled-up in PCH to 3.3-V standby through a weak pull-up resistor (24-k nominal)

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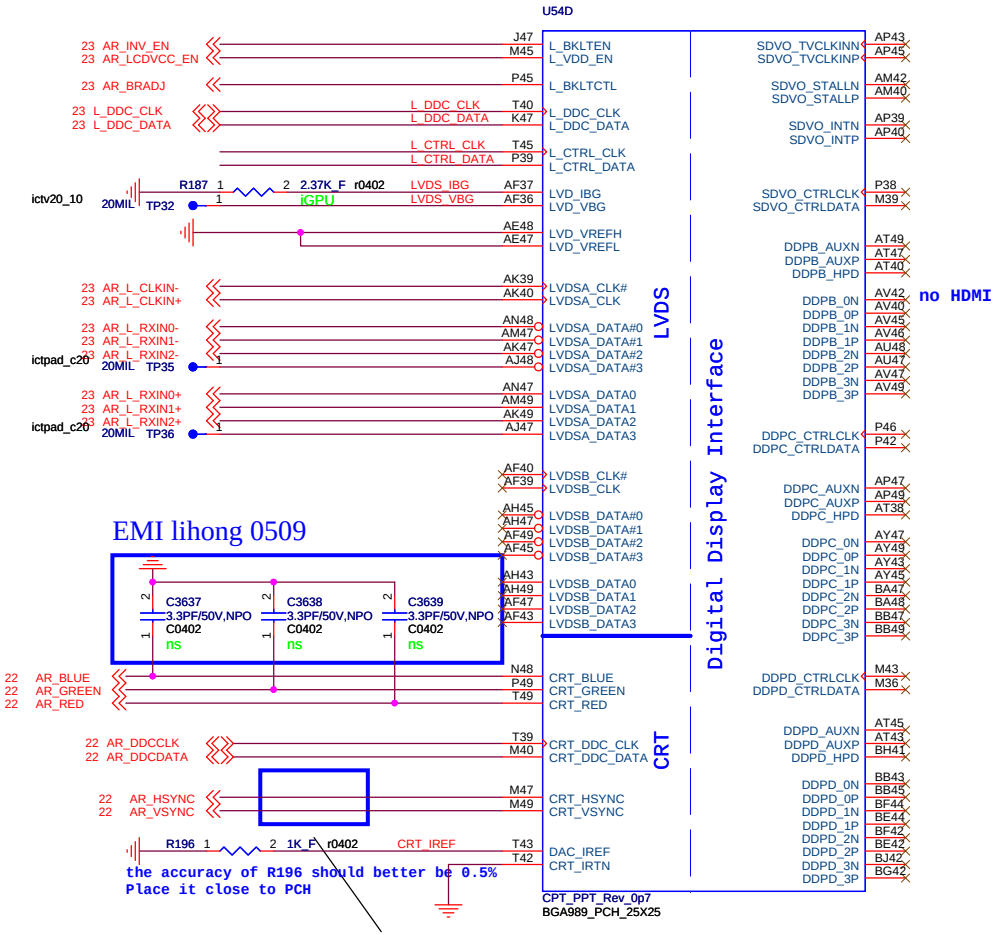
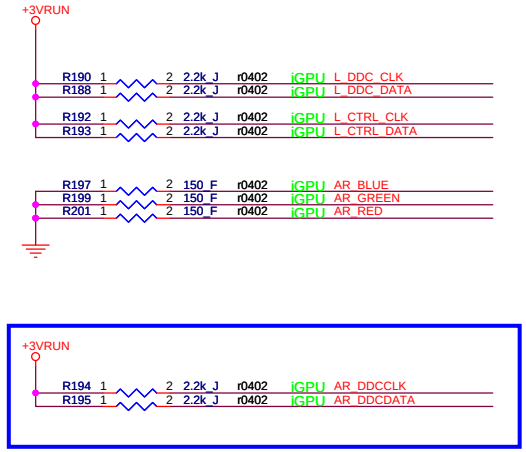
Title	PCH(DMI,FDI,GPIO)		
Size A3	Document Number N480		Rev 1.2
Date: Wednesday, September 12, 2012	Sheet 13	of 64	

+3VRUN 5,11,12,13,15,16,17,18,20,22,23,25,26,27,30,31,32,34,35,36,39,40,41,42,43,44,47,48,49,51,53



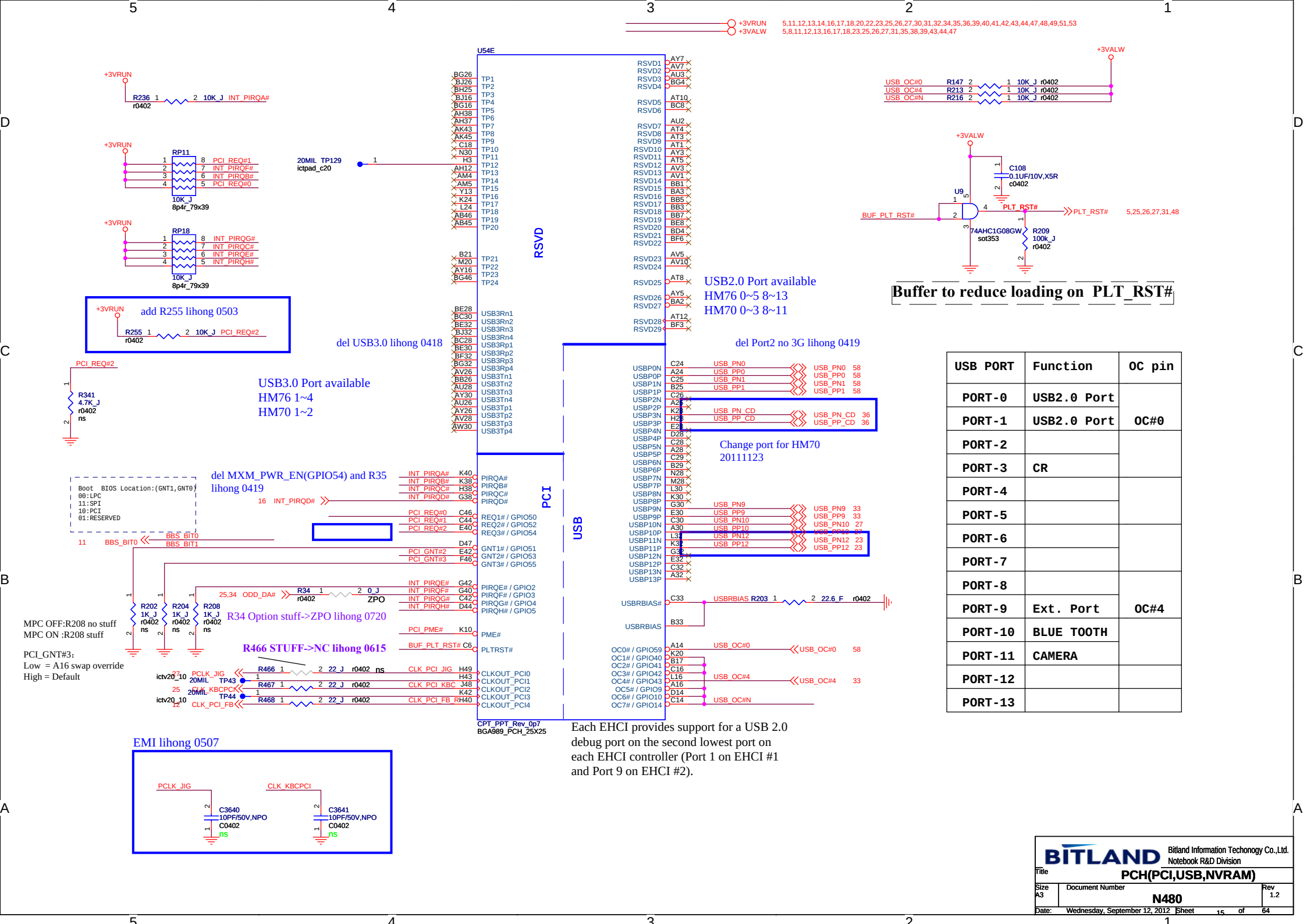
EMI lihong 0509

del R194 R195 lihong 0503



add R194 R195 lihong 0507

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	PCH(LVDS,DDI)	
Size A3	Document Number N480	Rev 1.2
Date: Wednesday, September 12, 2012	Sheet 14 of 64	



USB PORT	Function	OC pin
PORT-0	USB2.0 Port	
PORT-1	USB2.0 Port	OC#0
PORT-2		
PORT-3	CR	
PORT-4		
PORT-5		
PORT-6		
PORT-7		
PORT-8		
PORT-9	Ext. Port	OC#4
PORT-10	BLUE TOOTH	
PORT-11	CAMERA	
PORT-12		
PORT-13		

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Title: PCH(PCI,USB,NVRAM)

Size: A3 | Document Number: N480 | Rev: 1.2

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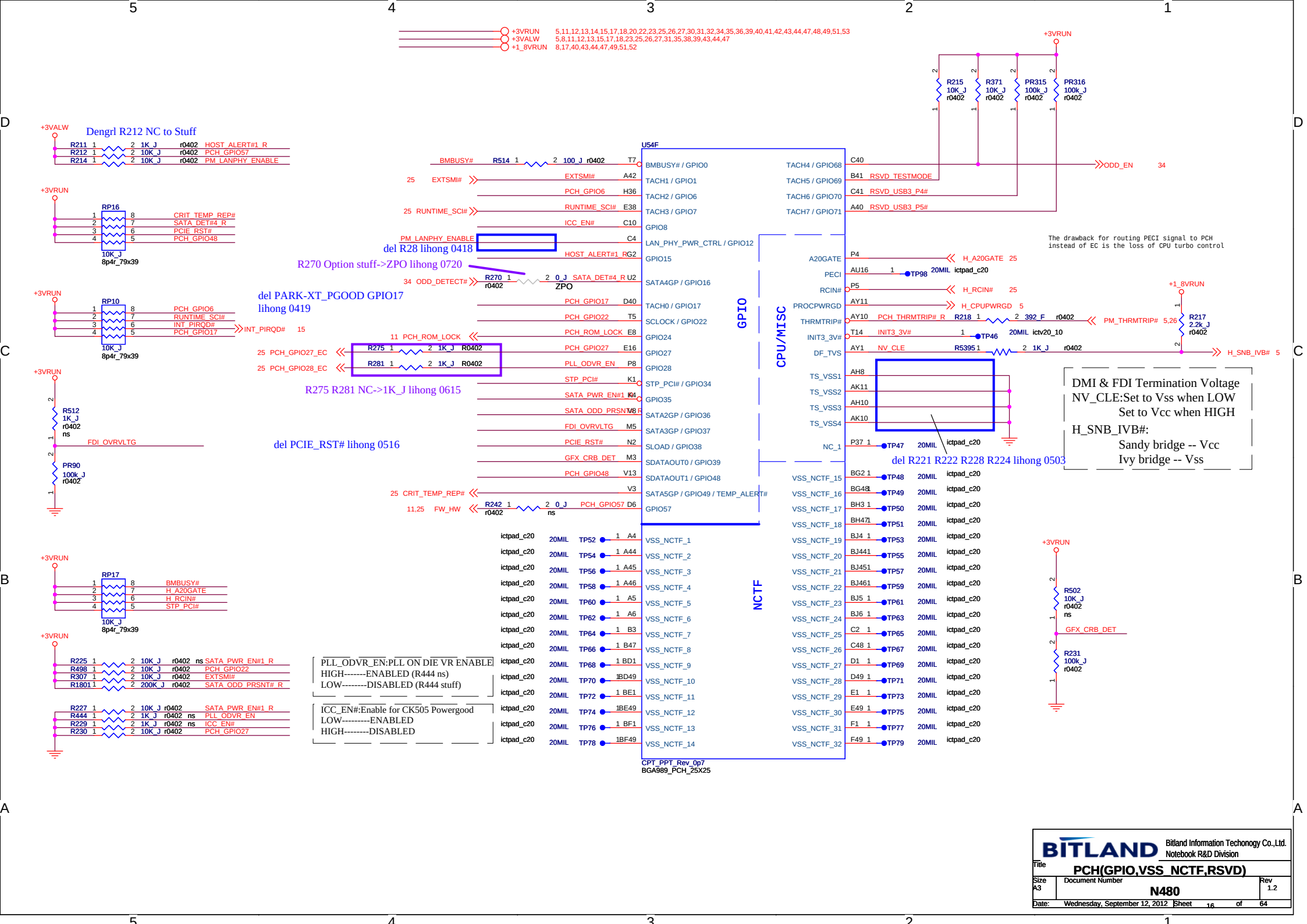
+3VRUN 5,11,12,13,14,15,17,18,20,22,23,25,26,27,30,31,32,34,35,36,39,40,41,42,43,44,47,48,49,51,53
+3VALW 5,8,11,12,13,15,17,18,23,25,26,27,31,35,38,39,43,44,47
+1_8VRUN 8,17,40,43,44,47,49,51,52
Dengrl R212 NC to Stuff
R211 1K_J r0402 HOST_ALERT#1_R
R212 10K_J r0402 PCH_GPIO57
R214 10K_J r0402 PM_LANPHY_ENABLE
RP16 CRIT_TEMP_REP# SATA_DET#4_R PCIE_RST# PCH_GPIO48 10K_J 8p4r_79x39
RP10 PCH_GPIO6 RUNTIME_SCI# INT_PIRQD# PCH_GPIO17 10K_J 8p4r_79x39
INT_PIRQD# 15
R512 1K_J r0402 ns FDI_OVRVLTG
PR90 100k_J r0402
RP17 BMBUSY# H_A20GATE H_RCIN# STP_PCI# 10K_J 8p4r_79x39
R225 10K_J r0402 ns SATA_PWR_EN#1_R
R498 10K_J r0402 PCH_GPIO22
R307 10K_J r0402 EXTSMI#
R1801 200K_J r0402 SATA_ODD_PRSNT#_R
R227 10K_J r0402 SATA_PWR_EN#1_R
R444 1K_J r0402 ns PLL_ODVR_EN
R229 1K_J r0402 ns ICC_EN#
R230 10K_J r0402 PCH_GPIO27
PLL_ODVR_EN:PLL ON DIE VR ENABLE
HIGH-------ENABLED (R444 ns)
LOW--------DISABLED (R444 stuff)
ICC_EN#:Enable for CK505 Powergood
LOW---------ENABLED
HIGH--------DISABLED
del R28 lihong 0418
R270 Option stuff->ZPO lihong 0720
R270 0_J SATA_DET#4_R r0402 ZPO
del PARK-XT_PGOOD GPIO17
lihong 0419
R275 R281 NC->1K_J lihong 0615
del PCIE_RST# lihong 0516
U54F
BMBUSY# / GPIO0
TACH1 / GPIO1
TACH2 / GPIO6
TACH3 / GPIO7
GPIO8
LAN_PHY_PWR_CTRL / GPIO12
GPIO15
SATA4GP / GPIO16
TACH0 / GPIO17
SCLOCK / GPIO22
GPIO24
GPIO27
GPIO28
STP_PCI# / GPIO34
GPIO35
SATA2GP / GPIO36
SATA3GP / GPIO37
SLOAD / GPIO38
SDATAOUT0 / GPIO39
SDATAOUT1 / GPIO48
SATA5GP / GPIO49 / TEMP_ALERT#
GPIO57
GPIO
TACH4 / GPIO68
TACH5 / GPIO69
TACH6 / GPIO70
TACH7 / GPIO71
A20GATE
PECI
RCIN#
PROCPWRGD
THRMTRIP#
INIT3_3V#
DF_TVS
CPU/MISC
TS_VSS1
TS_VSS2
TS_VSS3
TS_VSS4
NC_1
del R221 R222 R228 R224 lihong 0503
VSS_NCTF_1 ... VSS_NCTF_14
VSS_NCTF_15 ... VSS_NCTF_32
NCTF
CPT_PPT_Rev_0p7
BGA989_PCH_25X25
R215 10K_J r0402
R371 10K_J r0402
PR315 100k_J r0402
PR316 100k_J r0402
ODD_EN 34
RSVD_TESTMODE
RSVD_USB3_P4#
RSVD_USB3_P5#
The drawback for routing PECI signal to PCH instead of EC is the loss of CPU turbo control
H_A20GATE 25
H_RCIN# 25
H_CPUPWRGD 5
PCH_THRMTRIP# R
R218 392_F r0402
PM_THRMTRIP# 5,26
R217 2.2k_J r0402
INIT3_3V#
NV_CLE
R5395 1K_J r0402
H_SNB_IVB# 5
DMI & FDI Termination Voltage
NV_CLE:Set to Vss when LOW
Set to Vcc when HIGH
H_SNB_IVB#:
Sandy bridge -- Vcc
Ivy bridge -- Vss
R502 10K_J r0402 ns GFX_CRB_DET
R231 100k_J r0402
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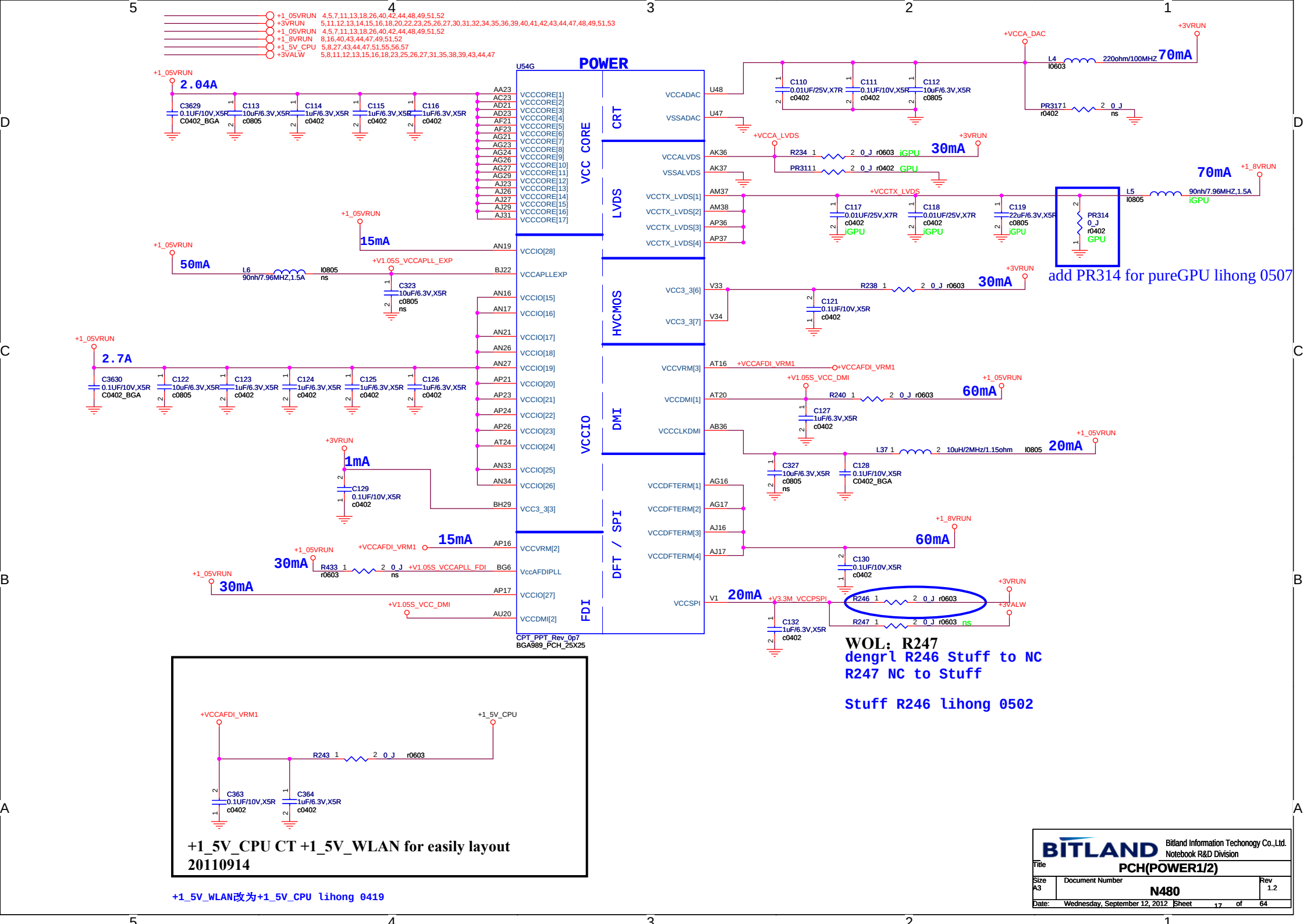
Notebook R&D Division
Title PCH(GPIO,VSS_NCTF,RSVD)
Size A3
Document Number N480
Rev 1.2
Date: Wednesday, September 12, 2012 Sheet 16 of 64


+1_05VRUN 4,5,7,11,13,18,26,40,42,44,48,49,51,52
+3VRUN 5,11,12,13,14,15,16,18,20,22,23,25,26,27,30,31,32,34,35,36,39,40,41,42,43,44,47,48,49,51,53
+1_05VRUN 4,5,7,11,13,18,26,40,42,44,48,49,51,52
+1_8VRUN 8,16,40,43,44,47,49,51,52
+1_5V_CPU 5,8,27,43,44,47,51,55,56,57
+3VALW 5,8,11,12,13,15,16,18,23,25,26,27,31,35,38,39,43,44,47
U54G
POWER
VCC CORE
CRT
LVDS
HVCMOS
VCCIO
DMI
DFT / SPI
FDI
VCCADAC
VSSADAC
VCCALVDS
VSSALVDS
VCCTX_LVDS[1]
VCCTX_LVDS[2]
VCCTX_LVDS[3]
VCCTX_LVDS[4]
VCC3_3[6]
VCC3_3[7]
VCCVRM[3]
VCCDMI[1]
VCCCLKDMI
VCCDFTERM[1]
VCCDFTERM[2]
VCCDFTERM[3]
VCCDFTERM[4]
VCCSPI
CPT_PPT_Rev_0p7
BGA989_PCH_25X25
2.04A
2.7A
15mA
50mA
1mA
30mA
60mA
20mA
70mA
add PR314 for pureGPU lihong 0507
WOL：R247
dengrl R246 Stuff to NC
R247 NC to Stuff
Stuff R246 lihong 0502
+1_5V_CPU CT +1_5V_WLAN for easily layout
20110914
+1_5V_WLAN改为+1_5V_CPU lihong 0419
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Notebook R&D Division
PCH(POWER1/2)
N480
Rev 1.2
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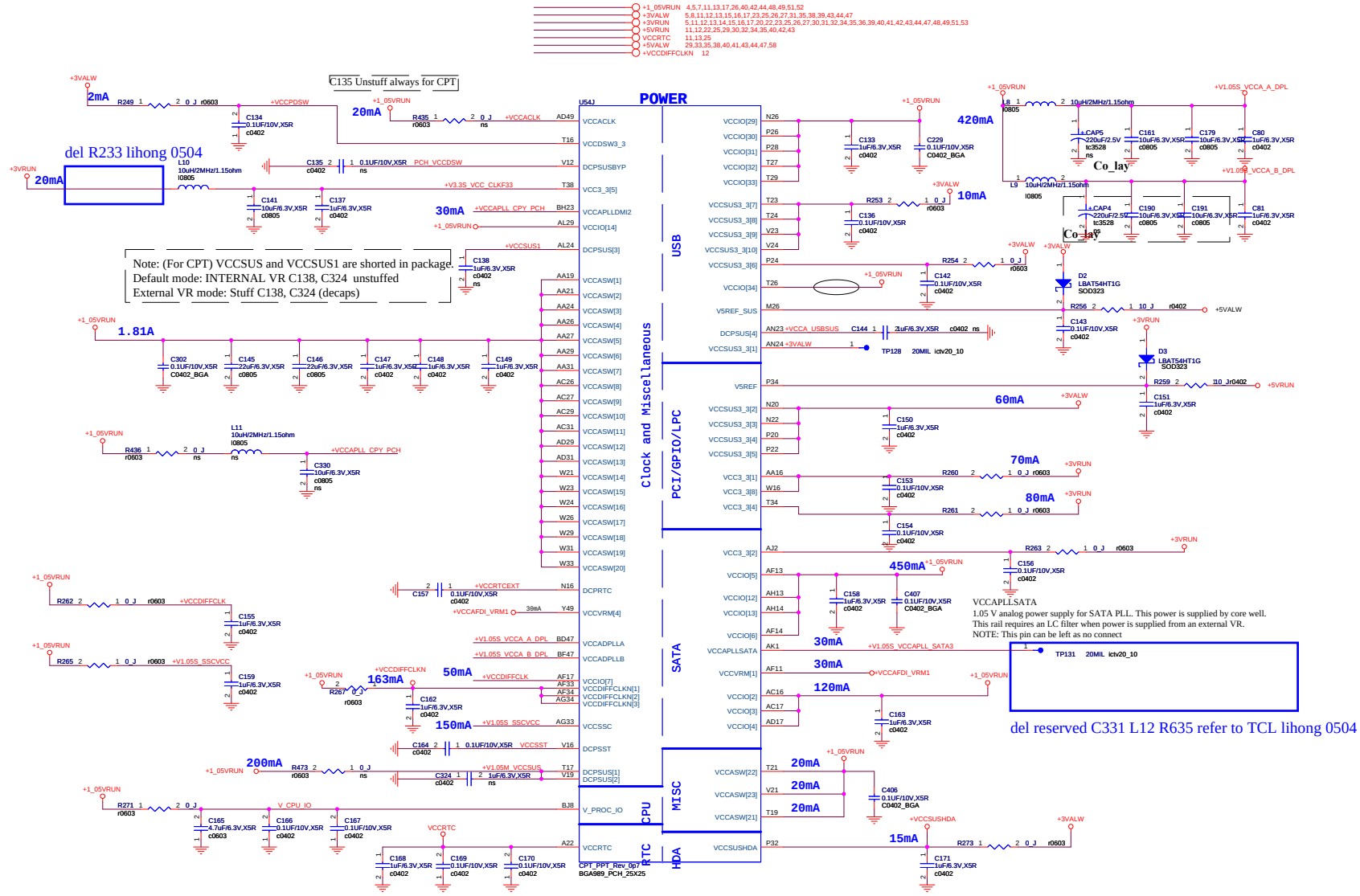

Title	PCH(POWER2/2)
Size	A2
Document Number	N480
Rev	1.2
Date:	Wednesday, September 12, 2012
Sheet	18 of 64

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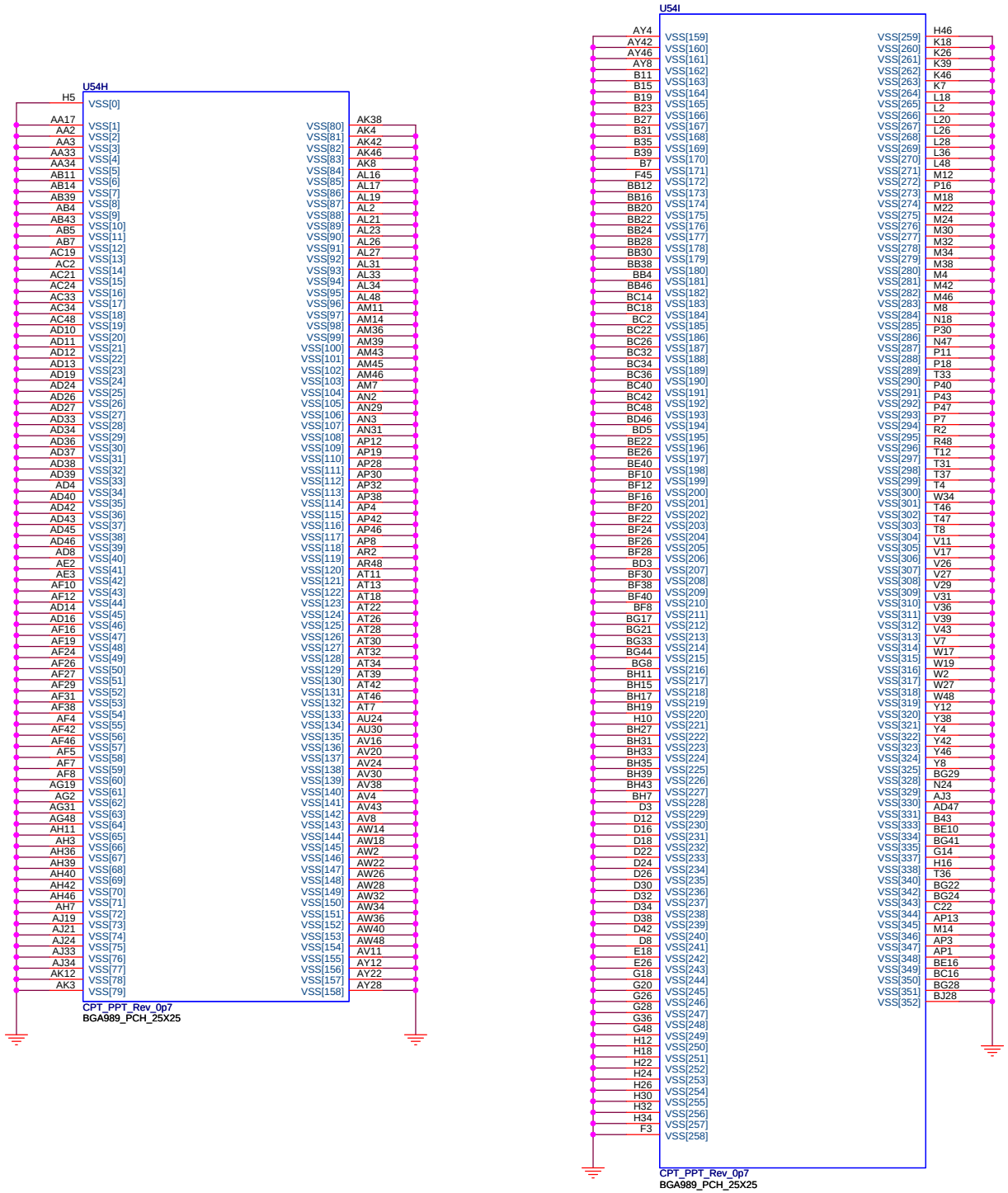
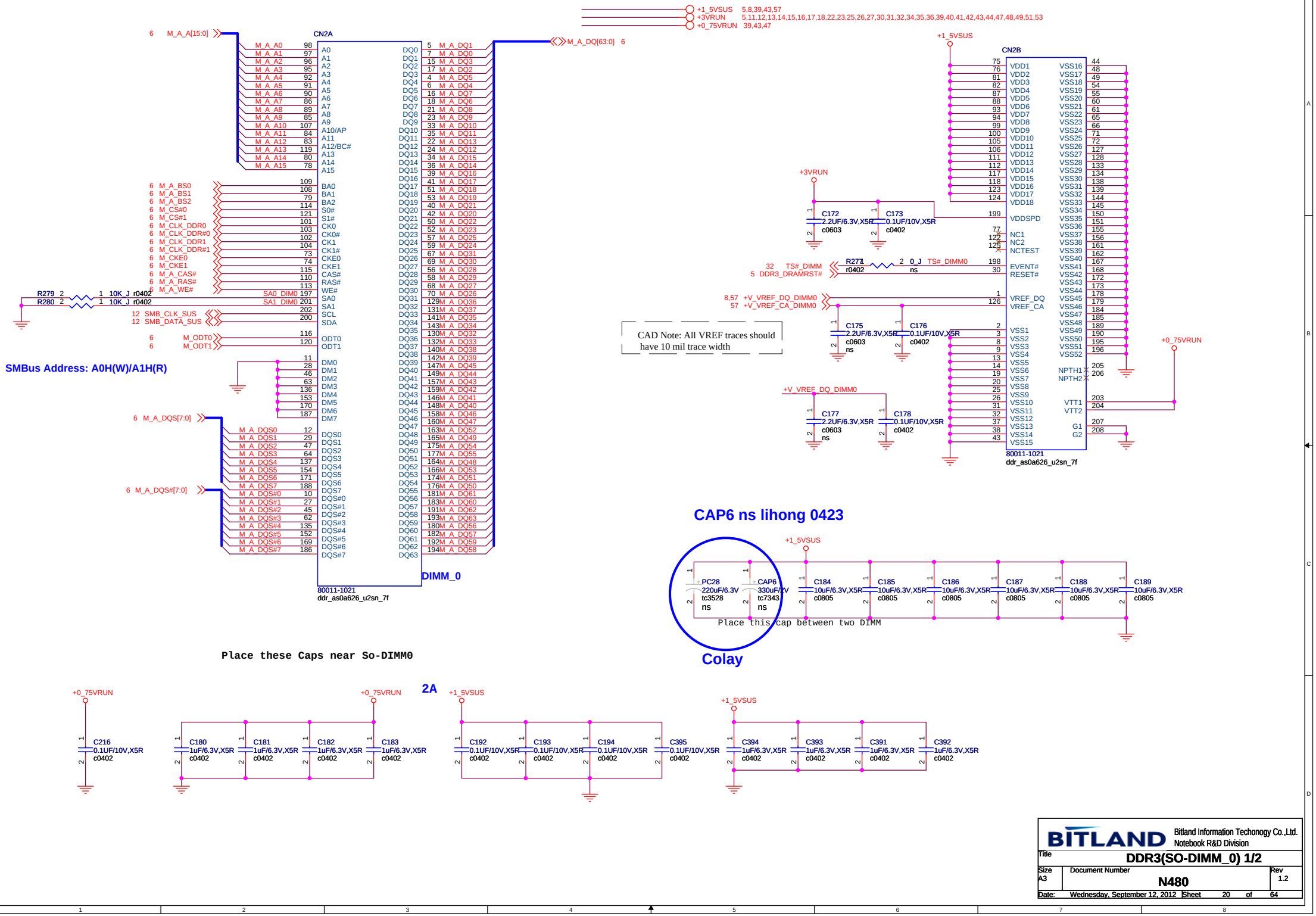
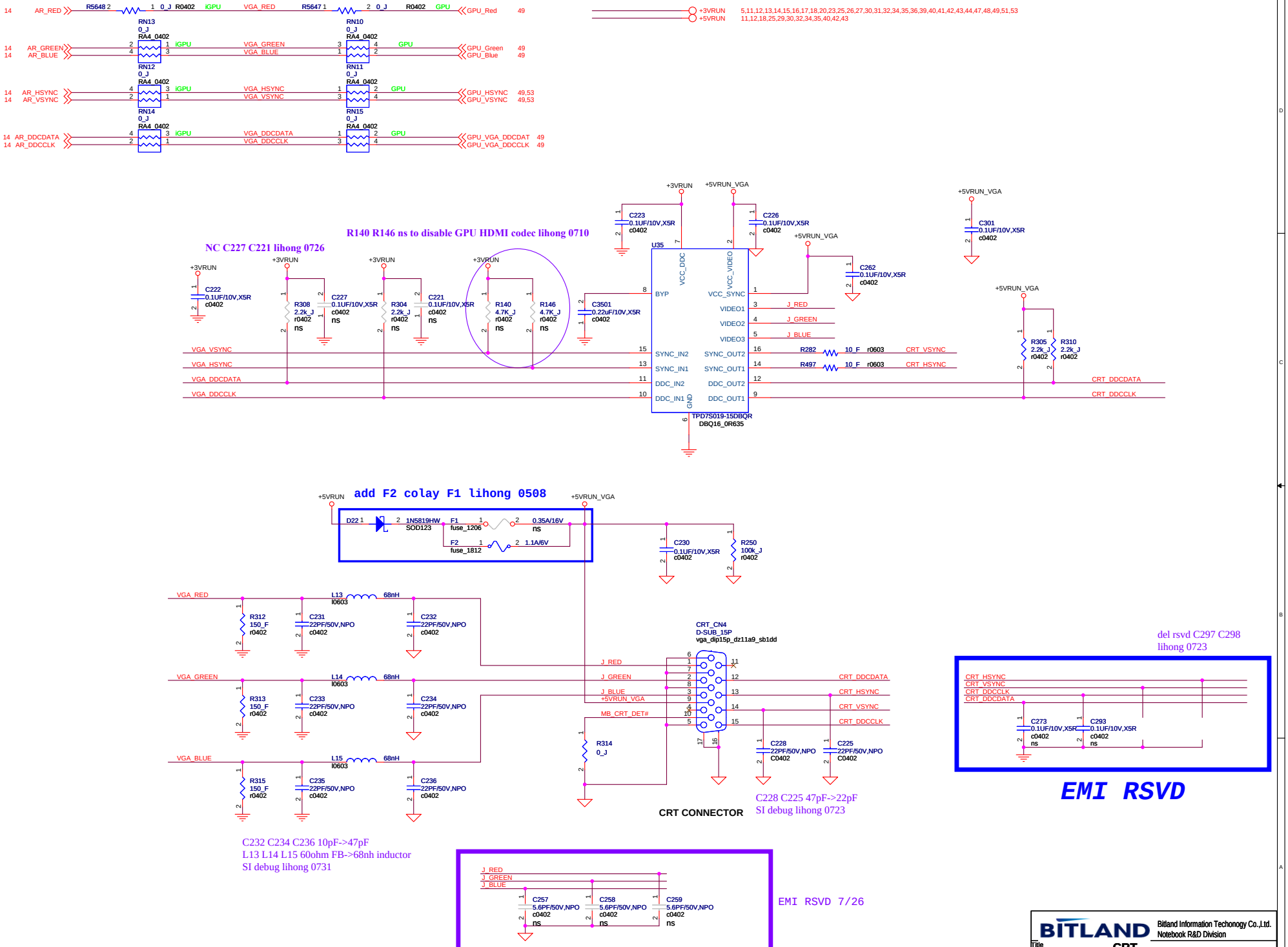


BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	PCH(GND)	
Size A3	Document Number N480	Rev 1.2
Date: Wednesday, September 12, 2012	Sheet 19 of 64	

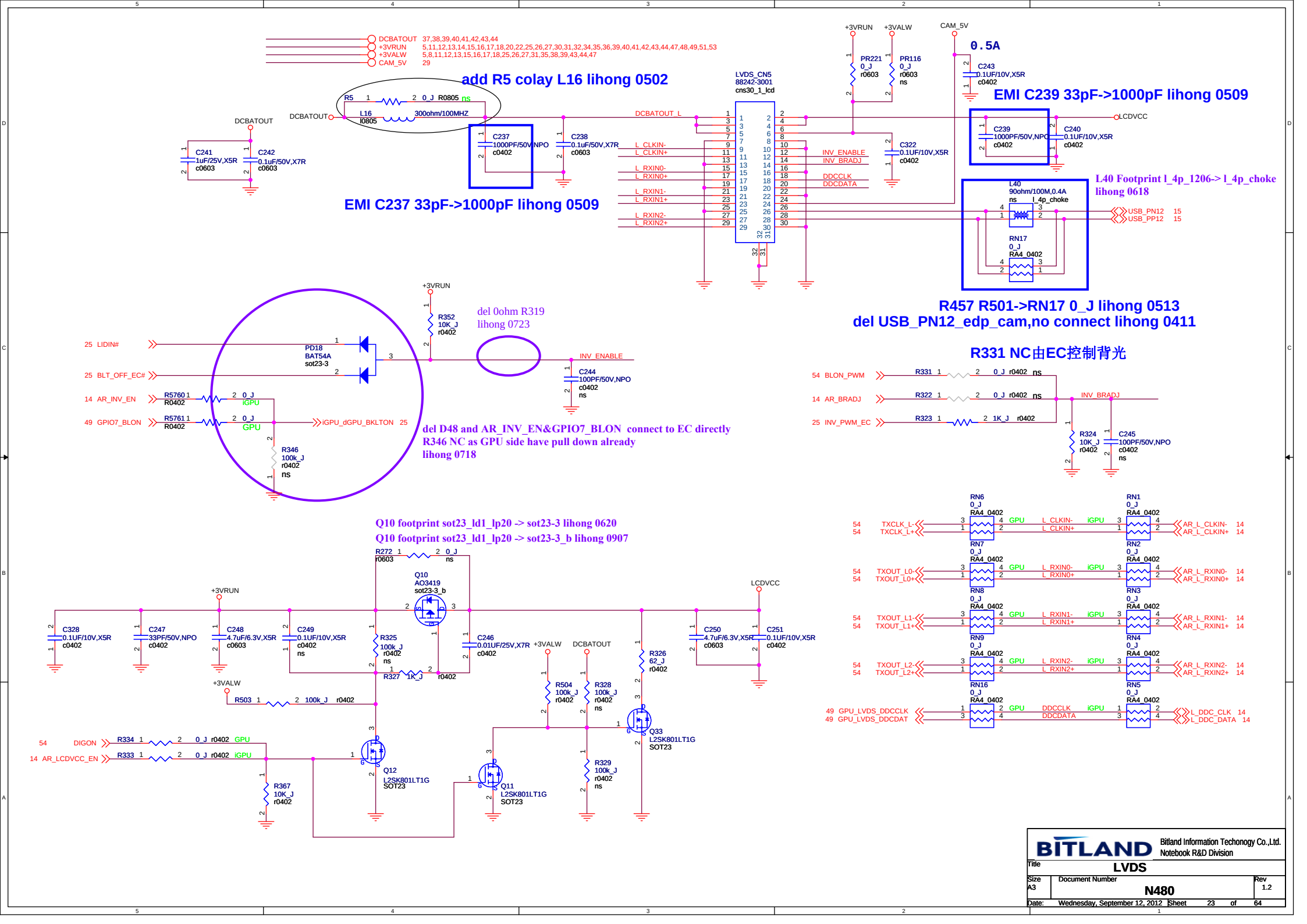


BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division
Title	DDR3(SO-DIMM_0) 1/2
Size A3	Document Number N480
Rev	1.2
Date: Wednesday, September 12, 2012	Sheet 20 of 64

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division
Title	DDR3(SO-DIMM_1) 2/2
Size: A3	Document Number: N480
Rev: 1.2	
Date: Wednesday, September 12, 2012	Sheet 21 of 64



BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division		
Title	CRT		
Size Custom	Document Number N480		Rev 1.2
Date: Wednesday, September 12, 2012	Sheet 22	of	64


DCBATOUT 37,38,39,40,41,42,43,44
+3VRUN 5,11,12,13,14,15,16,17,18,20,22,25,26,27,30,31,32,34,35,36,39,40,41,42,43,44,47,48,49,51,53
+3VALW 5,8,11,12,13,15,16,17,18,25,26,27,31,35,38,39,43,44,47
CAM_5V 29
add R5 colay L16 lihong 0502
R5 0_J R0805 ns
L16 300ohm/100MHZ l0805
DCBATOUT
C241 1uF/25V,X5R c0603
C242 0.1uF/50V,X7R c0603
C237 1000PF/50V,NPO c0402
C238 0.1uF/50V,X7R c0603
EMI C237 33pF->1000pF lihong 0509
LVDS_CN5
88242-3001
cns30_1_lcd
DCBATOUT_L
L_CLKIN-
L_CLKIN+
L_RXIN0-
L_RXIN0+
L_RXIN1-
L_RXIN1+
L_RXIN2-
L_RXIN2+
INV_ENABLE
INV_BRADJ
DDCCLK
DDCDATA
+3VRUN
+3VALW
CAM_5V
0.5A
PR221 0_J r0603
PR116 0_J r0603 ns
C243 0.1UF/10V,X5R c0402
C322 0.1UF/10V,X5R c0402
EMI C239 33pF->1000pF lihong 0509
C239 1000PF/50V,NPO c0402
C240 0.1UF/10V,X5R c0402
LCDVCC
L40 90ohm/100M,0.4A ns l_4p_choke
L40 Footprint l_4p_1206-> l_4p_choke lihong 0618
RN17 0_J RA4_0402
USB_PN12 15
USB_PP12 15
R457 R501->RN17 0_J lihong 0513
del USB_PN12_edp_cam,no connect lihong 0411
+3VRUN
R352 10K_J r0402
del 0ohm R319 lihong 0723
25 LIDIN#
25 BLT_OFF_EC#
PD18 BAT54A sot23-3
INV_ENABLE
C244 100PF/50V,NPO c0402 ns
14 AR_INV_EN
49 GPIO7_BLON
R5760 0_J iGPU
R5761 0_J GPU
iGPU_dGPU_BKLTON 25
R346 100k_J r0402 ns
del D48 and AR_INV_EN&GPIO7_BLON connect to EC directly
R346 NC as GPU side have pull down already
lihong 0718
R331 NC由EC控制背光
54 BLON_PWM
14 AR_BRADJ
25 INV_PWM_EC
R331 0_J r0402 ns
R322 0_J r0402 ns
R323 1K_J r0402
INV_BRADJ
R324 10K_J r0402
C245 100PF/50V,NPO c0402 ns
Q10 footprint sot23_ld1_lp20 -> sot23-3 lihong 0620
Q10 footprint sot23_ld1_lp20 -> sot23-3_b lihong 0907
R272 0_J r0603
Q10 AO3419 sot23-3_b
C328 0.1UF/10V,X5R c0402
C247 33PF/50V,NPO c0402
C248 4.7uF/6.3V,X5R c0603
C249 0.1UF/10V,X5R c0402 ns
R325 100k_J r0402 ns
R327 1K_J r0402
C246 0.01UF/25V,X7R c0402
C250 4.7uF/6.3V,X5R c0603
C251 0.1UF/10V,X5R c0402
R326 62_J r0402
R503 100k_J r0402
R504 100k_J r0402
R328 100k_J r0402 ns
R329 100k_J r0402 ns
54 DIGON
14 AR_LCDVCC_EN
R334 0_J r0402 GPU
R333 0_J r0402 iGPU
Q12 L2SK801LT1G SOT23
Q11 L2SK801LT1G SOT23
Q33 L2SK801LT1G SOT23
R367 10K_J r0402
RN6 RN1 RN7 RN2 RN8 RN3 RN9 RN4 RN16 RN5 0_J RA4_0402
54 TXCLK_L-
54 TXCLK_L+
54 TXOUT_L0-
54 TXOUT_L0+
54 TXOUT_L1-
54 TXOUT_L1+
54 TXOUT_L2-
54 TXOUT_L2+
49 GPU_LVDS_DDCCLK
49 GPU_LVDS_DDCDAT
GPU
iGPU
AR_L_CLKIN- 14
AR_L_CLKIN+ 14
AR_L_RXIN0- 14
AR_L_RXIN0+ 14
AR_L_RXIN1- 14
AR_L_RXIN1+ 14
AR_L_RXIN2- 14
AR_L_RXIN2+ 14
L_DDC_CLK 14
L_DDC_DATA 14
BITLAND
Bitland Information Techonogy Co.,Ltd.
Notebook R&D Division
Title
LVDS
Size A3
Document Number
N480
Rev 1.2
Date: Wednesday, September 12, 2012
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BITLAND Bitland Information Techonogy Co.,Ltd.
Notebook R&D Division

Title: HDMI

Size	Document Number	Rev
A2	N480	1.2

Date: Wednesday, September 12, 2012 Sheet 24 of 64

PLEASE DO NOT PLACE ANY PULL-UP RESISTOR ON
GPG0, GPG2 AND GPG6 (Reserved hardware strapping).(IT8518E)

U14 footprint sot23_ld1_h32 -> sot23-3 lihong 0620

LID Switch

del PCH_APWROK(GPE6) lihong 0516

Same as G470e

del 0ohm R158
lihong 0724

del RSVD crystal lihong 0412

EMI reserved close to EC lihong 0510

add CAPSLOCK_LED#(GPA6) lihong 0510
Move FAN1_PWM from GPJ3 to GPA7 lihong 0510

add novo_sw# lihong 0413

PCIE_WAKE# move from GPI6 to GPD1 lihong 0502
del PM_SLP_M#(GPD1) lihong 0502
del WWAN_EN(GPE5) no 3G lihong 0419
add novo_sw#(GPE5) lihong 0413
AR_INV_E(GPD0)-> iGPU_dGPU_BKLTON lihong 0414

add PCH_GPIO27_EC(GPA6) PCH_GPIO28_EC(GPH6) lihong 0512

del WWAN_LED#(GPH6) no 3G lihong 0419

BOARD ID move from GPA2 to GPI6 lihong 0502

add ACIN_EC_TO_GPU(GPJ4) lihong 0516

R386 NC->Stuff
R387 100K->8.2K
lihong 0724

add R481 lihong 0510
R478 stuff->NC lihong 0710

R399 Q50 R569 ns->Stuff lihong 0910

+ECVCC	3.3V 5%				
R386	100K 5%				
Board ID	R387	V min	V typ	V max	Phase
0	0	0V	0V	0V	REV1.0
1	8.2K 5%	0.216V	0.250V	0.289V	REV1.1
2	18K 5%	0.436V	0.503V	0.538V	REV1.2
3	33K 5%	0.712V	0.819V	0.875V	REV1.3

BITLAND Bitland Information Techonogy Co.,Ltd.
Notebook R&D Division

Title: EC (IT8518E)

Size: A2 | Document Number: N480 | Rev: 1.2

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+ECVCC 11,25,35,37,38
+3VALW 5,8,11,12,13,15,16,17,18,23,25,27,31,35,38,39,43,44,47
+3VRUN 5,11,12,13,14,15,16,17,18,20,22,23,25,27,30,31,32,34,35,36,39,40,41,42,43,44,47,48,49,51,53
+1_05VRUN 4,5,7,11,13,17,18,40,42,44,48,49,51,52

25 SPI_ROM_SDI
25 SPI_ROM_SDO
25 SPI_ROM_CLK
25 SPI_ROM_CS#

SPI_ROM_SDI
SPI_ROM_SDO
SPI_ROM_CLK
SPI_ROM_CS#

+ECVCC

U17
SPI_ROM_CS# 1 CS# VCC 8 +ECVCC
SPI_ROM_SDI_R 2 DO/IO1 HOLD#/IO3 7 HOLD#
SPI_ROM_WP# 3 WP#/IO2 CLK 6 SPI_ROM_CLK
4 GND DI/IO0 5 SPI_ROM_SDO
W25X8Mbit
sop8_1d27_8
ns

CO-LAY

+ECVCC
C280
0.1UF/10V,X5R
c0402

+ECVCC
R388
4.7K_J
r0402

+ECVCC
R389
1K_J
r0402

SPI_ROM_SDI R390 1 2 22_J r0402

U16
SPI_ROM_CS# 1 CS# VCC 8 +ECVCC
SPI_ROM_SDI_R 2 DO/IO1 HOLD#/IO3 7 HOLD#
SPI_ROM_WP# 3 WP#/IO2 CLK 6 SPI_ROM_CLK
4 GND DI/IO0 5 SPI_ROM_SDO
W25X512Kbit
sop8_1d27_6d0

R391
1K_J
r0402
ns

SPI ROM

+ECVCC
R392
100K_F
r0402

R393 1 2 0_J r0402
ECRST# ECRST# 25,32

C281
1uF/6.3V,X5R
c0402

PLT_RST# 1
Q23
L2SK801LT1G
SOT23

+1_05VRUN
R394 1 2 330_J r0402 1
Q24
LMBT3904LT1G
SOT23

5,16 PM_THRMTRIP# PM_THRMTRIP#

A0202

R394 Q24 NC->stuff
R394 2.2K->330 refer to E216CT
lihong 0718

+3VRUN
R395 2 1 10K_J r0402 ns
Q25
L2SK801LT1G
SOT23
ns

C282
0.1UF/10V,X5R
c0402
ns

32,53 SYS_SHDN# SYS_SHDN#

SYS_SHDN# not in use
R395 C282 Q25 NC
lihong 0718

+3VALW +3VALW +3VALW

GP61 OPEN_JUMP_OPEN2 OPEN2
GP63 OPEN_JUMP_OPEN2 OPEN2
GP86 OPEN_JUMP_OPEN2 OPEN2

25,38 ALW_ON
25,39,40,41,43,44 RUN_ON
25,42 IMVP_VR_ON
25,42,47 IMVP_OK
13,25 PM_SLP_S4#
5,15,25,27,31,48 PLT_RST#
13,25 PWRBTN#

tpc40b_75 TP_AN
tpc40b_75 TP_RN
tpc40b_75 TP_VN
tpc40b_75 TP89
tpc40b_75 TP_S4
tpc40b_75 TP93
tpc40b_75 TP_BTN

+3VALW +3VALW

GP62 OPEN_JUMP_OPEN2 OPEN2
GP64 OPEN_JUMP_OPEN2 OPEN2

TP_SN tpc40b_75
TP86 tpc40b_75
TP88 tpc40b_75
TP_S3 tpc40b_75

SUS_ON 25,39,43
PM_PCH_PWROK_L 25,47
ALL_SYS_PWRGD 25,42,47
PM_SLP_S3# 13,25,47

TP_S5 tpc40b_75
TP100 tpc40b_75

PM_SLP_S5# 13,25
PM_RSMRST# 13,25

these TP could near the MB outline.should be placed on one side of the PCB

del PM_SLP_M# TP94 lihong 0513

BITLAND Bitland Information Techonogy Co.,Ltd.
Notebook R&D Division

Title: Flash ROM/SPI

Size	Document Number	Rev
A3	N480	1.2

Date: Wednesday, September 12, 2012 Sheet 26 of 64

3.3V is available during the system's stand-by/suspend state to support wake event processing on the communications card.

+3VALW 5,8,11,12,13,15,16,17,18,23,25,26,31,35,38,39,43,44,47
+3VRUN 5,11,12,13,14,15,16,17,18,20,22,23,25,26,30,31,32,34,35,36,39,40,41,42,43,44,47,48,49,51,53
+1_5V_CPU 5,8,17,43,44,47,51,55,56,57
+1_5VSUS 5,8,20,39,43,57

add back lihong 0516

+3VALW
R46 1 2 0_J r0805
+3VRUN
R49 1 2 0_J r0805 ns

WLAN_+3_3V

place near Pin2 Pin52

C283 22uF/6.3V,X5R c0805 ns
C286 10uF/6.3V,X5R c0805
C284 0.1UF/10V,X5R c0402
C285 0.1UF/10V,X5R c0402

need double check placement

+1_5V_CPU
C437 0.1UF/10V,X5R c0402
C412 10uF/6.3V,X5R c0805
C292 0.1UF/10V,X5R c0402
C290 0.1UF/10V,X5R c0402

del 2pcs 10uF cap C291&C358 lihong 0718

reserve Q26 R9 lihong 0514

del reserved Q26 R9
R403 NC lihong 0719

使用WIDI时，请删除pin5的电阻

13,25,31 PCIE_WAKE# R397 2 1 0_J r0402 ns
25 BT_ON R403 2 1 2K_F r0402 ns
12 MINI_CARD_DET#

WIFI_CN7
80003-3021
minipcie_card_half

1	WAKE#	+3.3V_1	2
3	BT_DATA	GND7	4
5	BT_CLK	+1.5V_1	6
7	CLKREQ#	RSVD13	8
9	GND1	RSVD14	10
11	REFCLK-	RSVD15	12
13	REFCLK+	RSVD16	14
15	GND2	RSVD17	16
	KEY		
17	RSVD3	GND8	18
19	RSVD4	W_DISABLE#	20
21	GND3	PERST#	22
23	PER_N0	+3.3V_AUX	24
25	PER_P0	GND9	26
27	GND4	+1.5V_2	28
29	GND5	SMB_CLK	30
31	PET_N0	SMB_DATA	32
33	PET_P0	GND10	34
35	GND6	USB_D-	36
37	RSVD5	USB_D+	38
39	RSVD6	GND11	40
41	RSVD7	LED_WWAN#	42
43	RSVD8	LED_WLAN#	44
45	RSVD9	LED_WPAN#	46
47	RSVD10	+1.5V_3	48
49	RSVD11	GND12	50
51	RSVD12	+3.3V_2	52
53	GND13	NC1	54
55	GND14	NC2	56

12 CLK_PCIE_MINI#
12 CLK_PCIE_MINI

WLAN_+3_3V
+1_5V_CPU
+1_5V_CPU

LPC_FRAME# R R431 1 2 0_J r0402 LPC_FRAME#
R407 2 1 0_J r0402 E51TXD 25
R617 2 1 0_J r0402 E51RXD 25

WLAN_EN 25
PLT_RST# 5,15,25,26,31,48

12 MINI_RXN3
12 MINI_RXP3
12 MINI_TXN3
12 MINI_TXP3

USB_PN10 15
USB_PP10 15

+3VALW +3VALW +3VRUN
C287 0.1UF/10V,X5R c0402
C288 10uF/6.3V,X5R c0805

del 0ohm R44(stuff) R423(rsvd) lihong 0719

PIN39/41接INTEL WiFi时要接3.3V

+3VALW
R401 2 1 0_J r0402 ns
R402 2 1 0_J r0402 ns
R410 2 1 0_J r0402
15 PCLK_JIG
LPC_FRAME#
R411 2 1 0_J r0402 ns

11,25 LPC_AD0
11,25 LPC_AD1
11,25 LPC_AD2
11,25 LPC_AD3

RN18
0_J
ra8_0402

R406
0_J
r0402
ns

换为排阻 lihong 0516

Pin30,32,36,38 is Reserved in Kedron pin-out definition

WIFI_BOSS1
Hole+Dowel
hole4d06_2d24

删除此处0ohm lihong 0419

11,25 LPC_FRAME# LPC_FRAME#

删除+1_5VSUS转+1_5V_WLAN线路，直接使用+1_5V_CPU lihong 0419

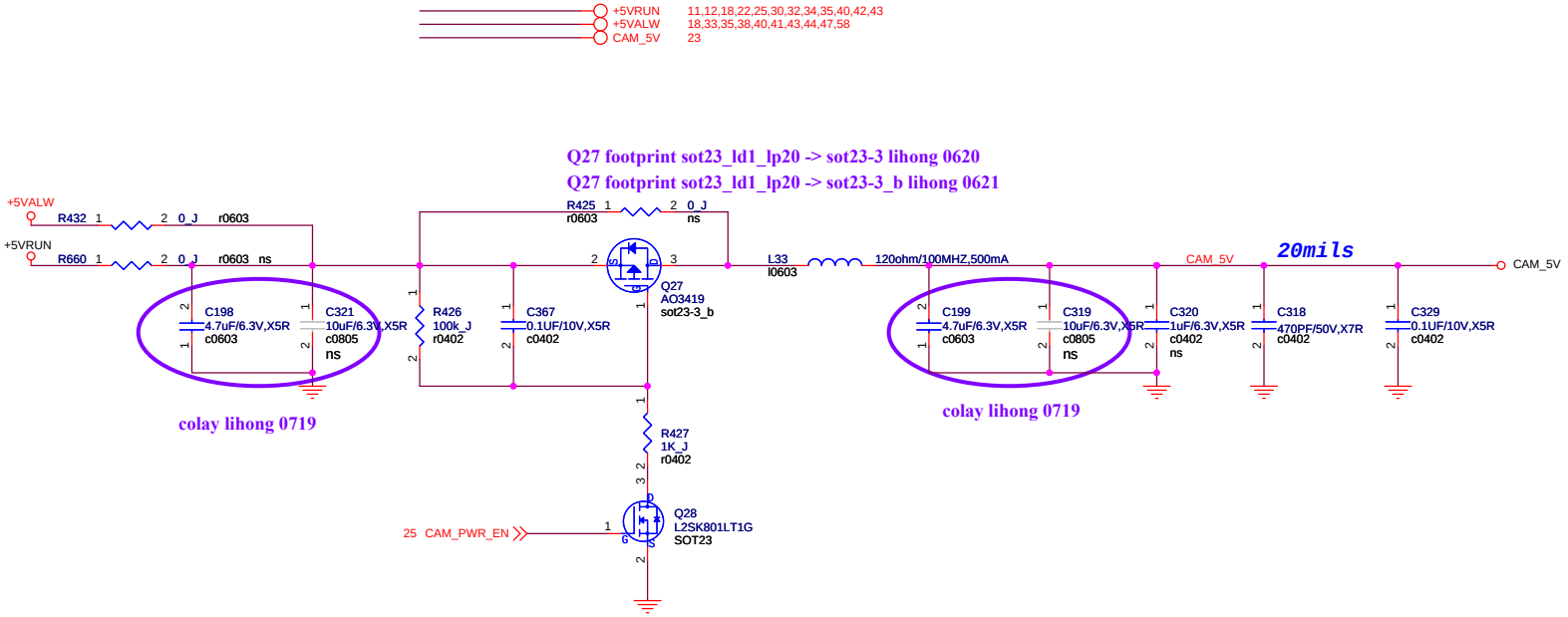
ADD for easily layout 20110908

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	WLAN Mini-PCIECard	
Size A3	Document Number N480	Rev 1.2
Date: Wednesday, September 12, 2012	Sheet 27 of 64	

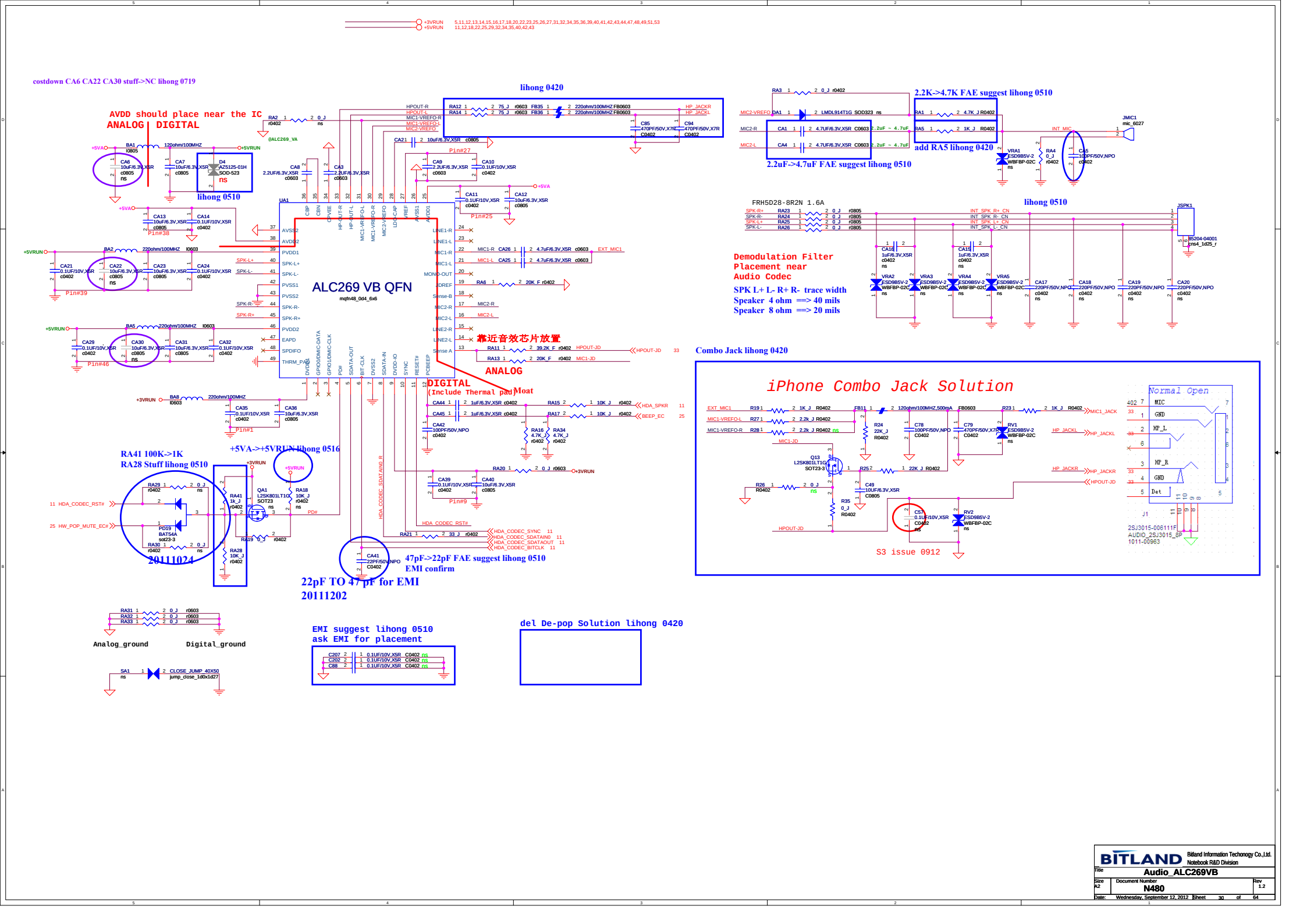
BITLAND

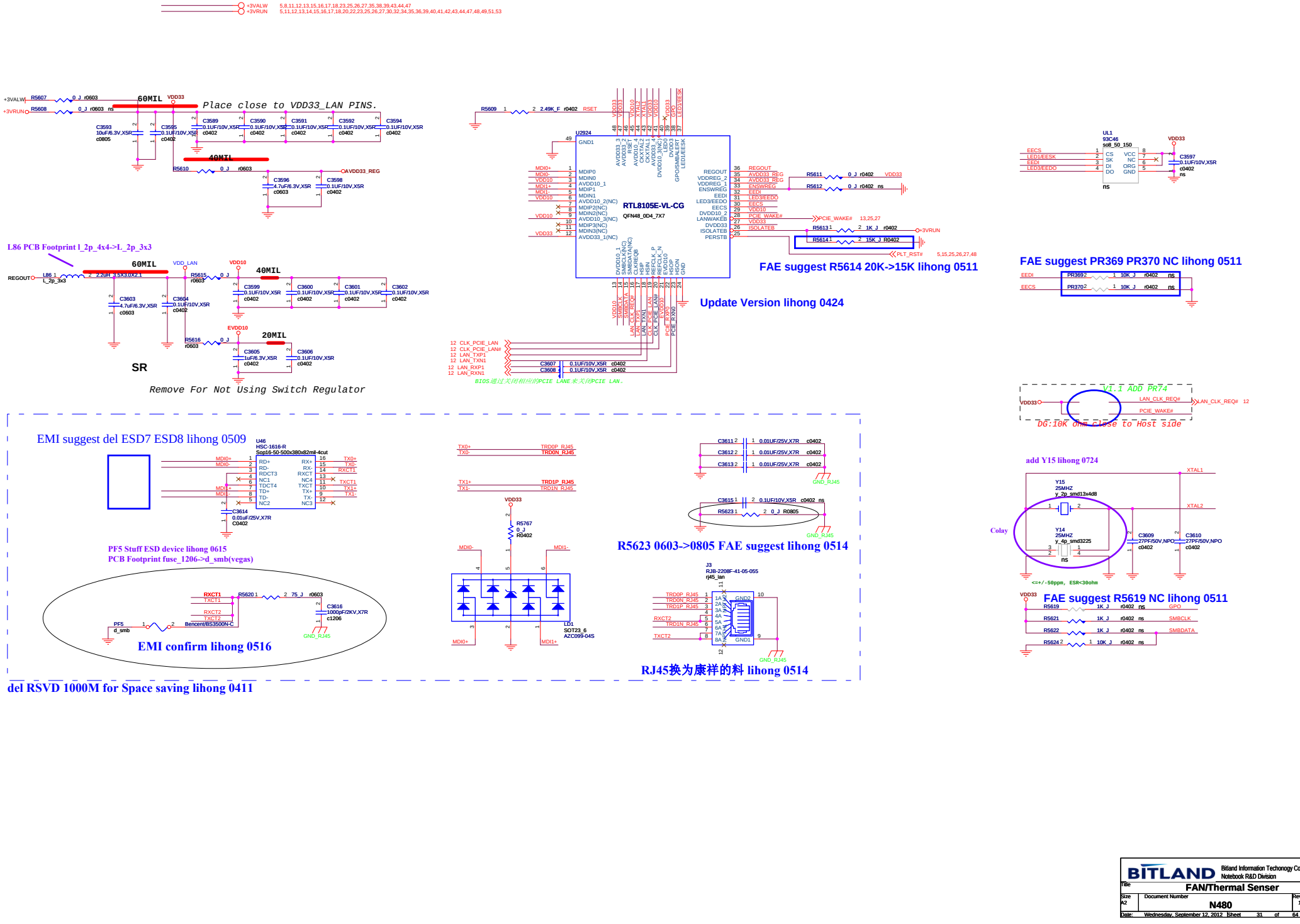
Bitland Information Techonogy Co.,Ltd.
Notebook R&D Division

Title	3G Mini-PCIE Card	
Size: A3	Document Number: N480	Rev: 1.2
Date: Wednesday, September 12, 2012	Sheet 28 of 64	



BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	BT & CAMERA &finger print	
Size A3	Document Number N480	Rev 1.2
Date: Wednesday, September 12, 2012	Sheet 29 of 64	


costdown CA6 CA22 CA30 stuff->NC lihong 0719
AVDD should place near the IC
ANALOG | DIGITAL
lihong 0420
2.2K->4.7K FAE suggest lihong 0510
add RA5 lihong 0420
2.2uF->4.7uF FAE suggest lihong 0510
lihong 0510
Demodulation Filter
Placement near
Audio Codec
SPK L+ L- R+ R- trace width
Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils
ALC269 VB QFN
mqfn48_0d4_6x6
靠近音效芯片放置
ANALOG
DIGITAL
(Include Thermal pad Moat
Combo Jack lihong 0420
iPhone Combo Jack Solution
Normal Open
RA41 100K->1K
RA28 Stuff lihong 0510
+5VA->+5VRUN lihong 0516
20111024
22pF TO 47pF for EMI
20111202
47pF->22pF FAE suggest lihong 0510
EMI confirm
EMI suggest lihong 0510
ask EMI for placement
del De-pop Solution lihong 0420
S3 issue 0912
Analog_ground
Digital_ground
BITLAND
Bitland Information Techonogy Co.,Ltd.
Notebook R&D Division
Audio_ALC269VB
N480
Wednesday, September 12, 2012

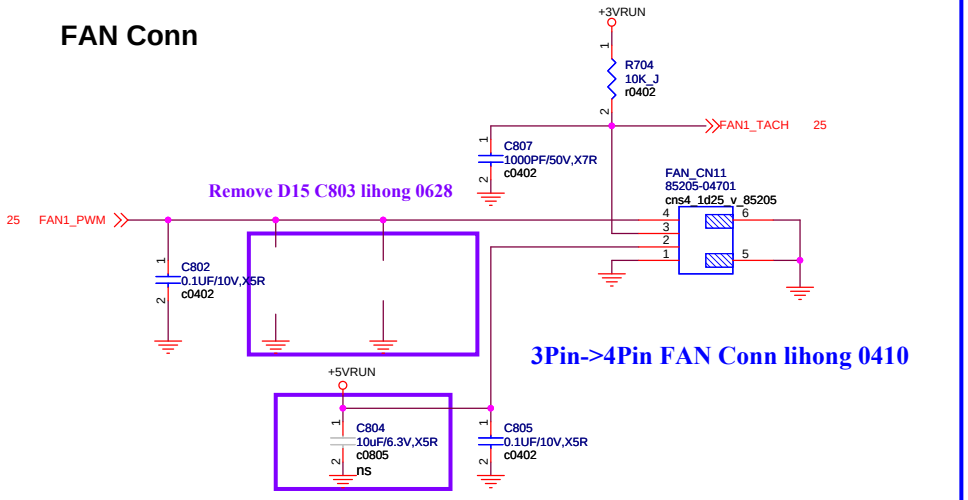


Title	FAN/Thermal Senser
Size	A2
Document Number	N480
Rev	1.2
Date:	Wednesday, September 12, 2012 Sheet 31 of 64

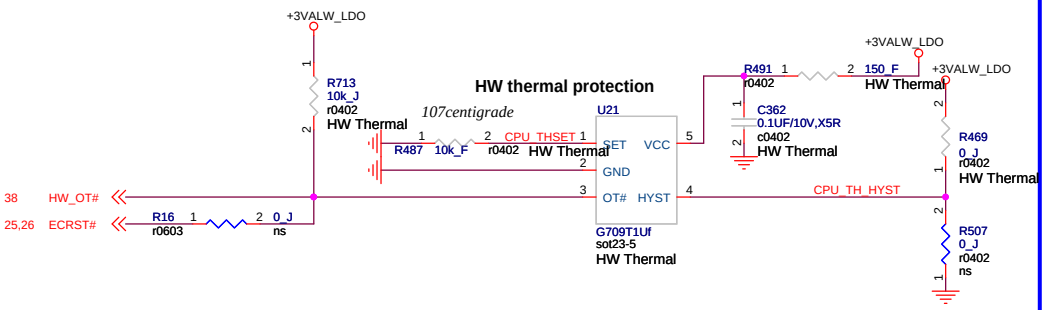
Bitland Information Technology Co.,Ltd.
Notebook R&D Division

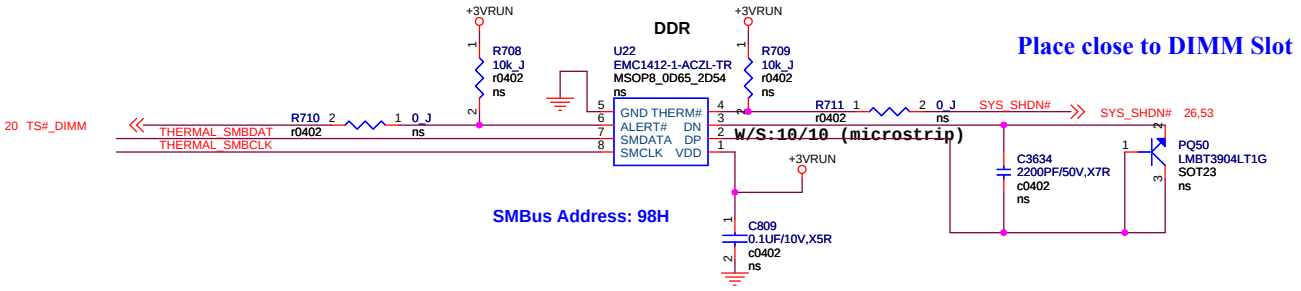
+3VALW_LDO 38
+3VRUN 5,11,12,13,14,15,16,17,18,20,22,23,25,26,27,30,31,34,35,36,39,40,41,42,43,44,47,48,49,51,53
+5VRUN 11,12,18,22,25,29,30,34,35,40,42,43

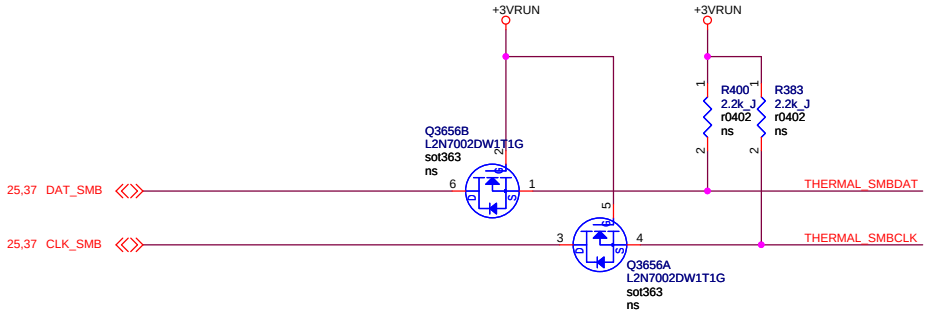
FAN Conn



check placement, place near hot components







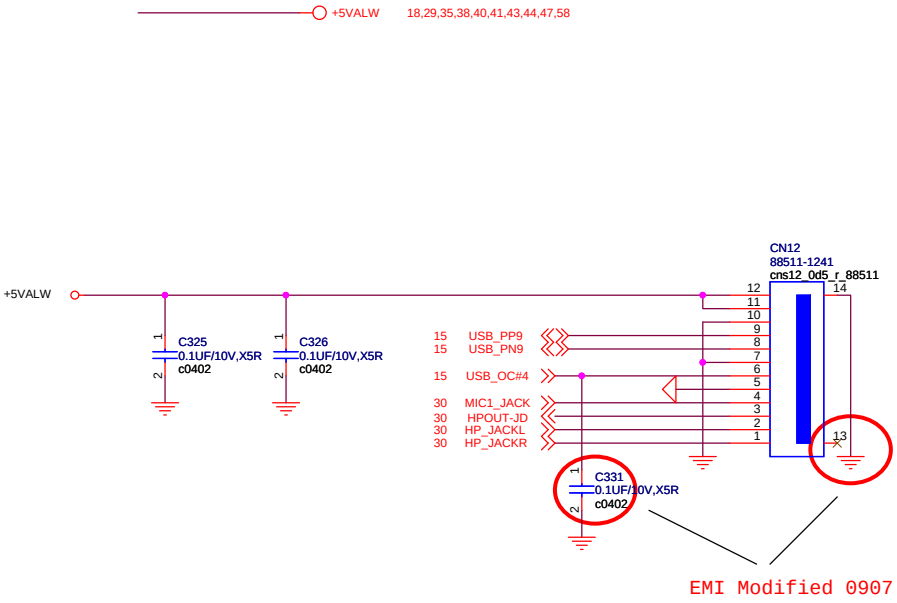
Reserve DDR thermal sensor lihong 0508

BITLAND Bitland Information Techonogy Co.,Ltd.
Notebook R&D Division

Title: FAN/Thermal Senser

Size	Document Number	Rev
A3	N480	1.2

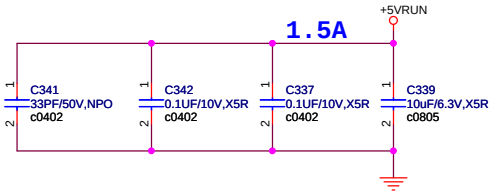
Date: Wednesday, September 12, 2012 Sheet 32 of 64



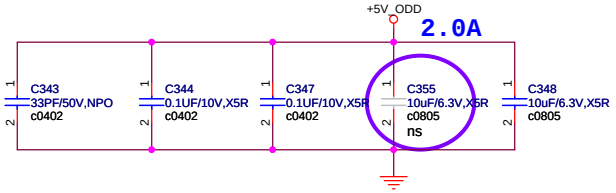
BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	USB2.0	
Size A3	Document Number N480	Rev 1.2
Date: Wednesday, September 12, 2012	Sheet 33 of 64	

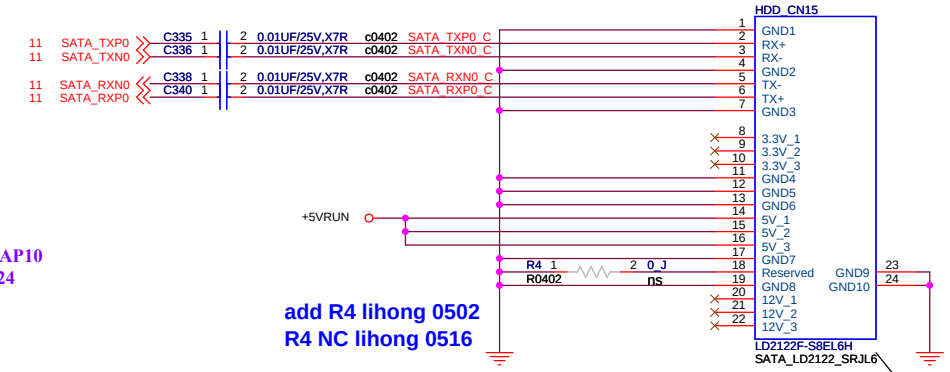
+3VRUN 5,11,12,13,14,15,16,17,18,20,22,23,25,26,27,30,31,32,35,36,39,40,41,42,43,44,47,48,49,51,53
+5VRUN 11,12,18,22,25,29,30,32,35,40,42,43

SATA HDD CONN



del RSVD 3528 47uF CAP10
reserve C355 lihong 0724





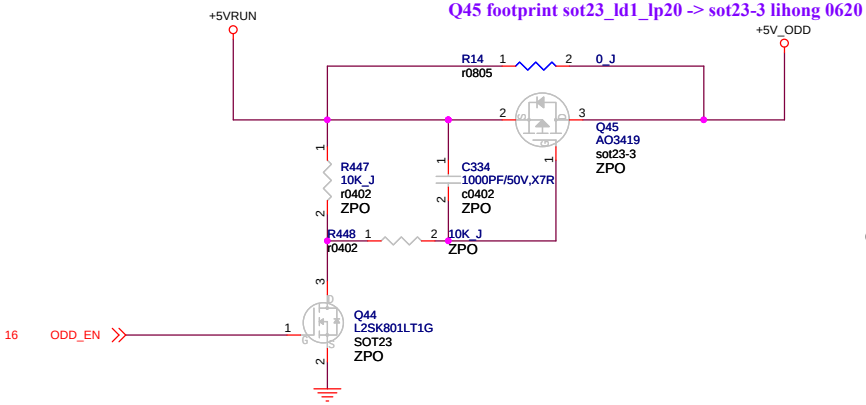
add R4 lihong 0502
R4 NC lihong 0516

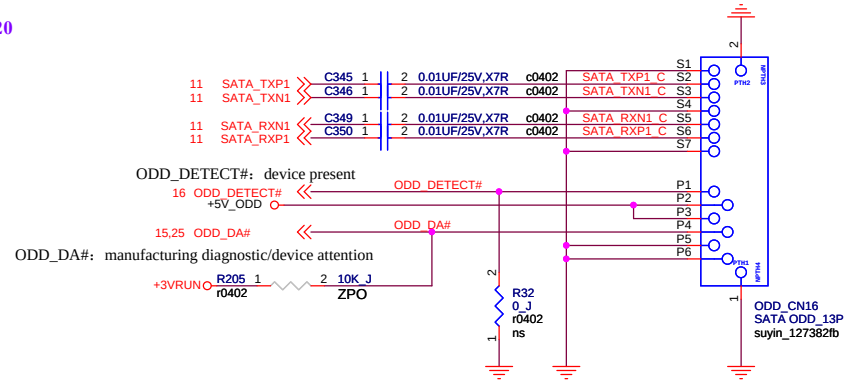
HDD换为康祥的料 lihong 0514

footprint sata_ld2122_s8el6h->
SATA_LD2122_SRJL6 lihong 0615

SATA ODD CONN

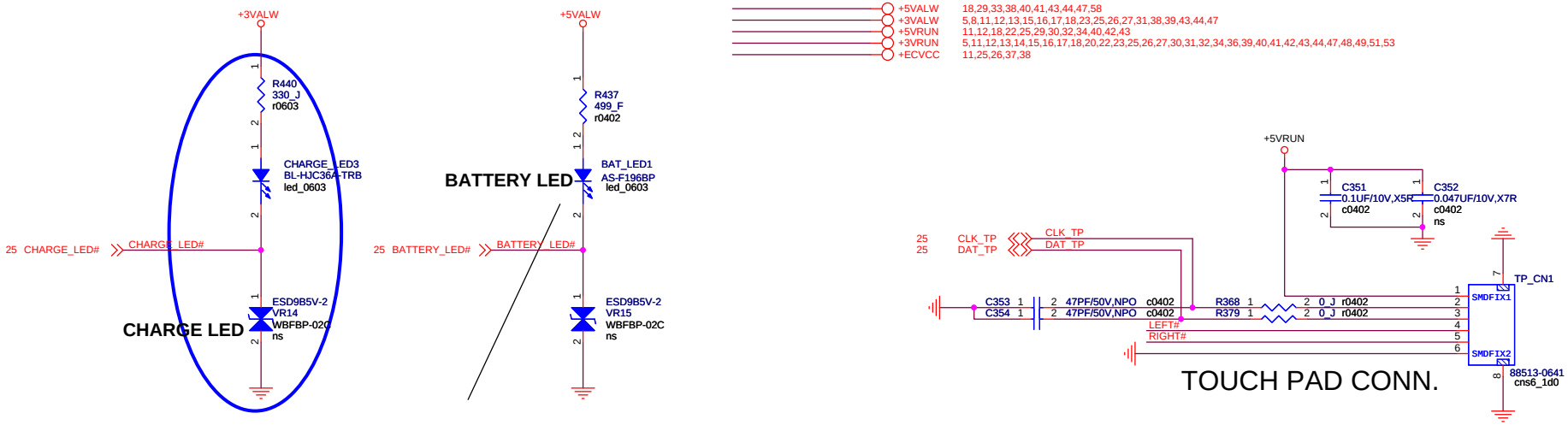
Q45 footprint sot23_ld1_lp20 -> sot23-3 lihong 0620



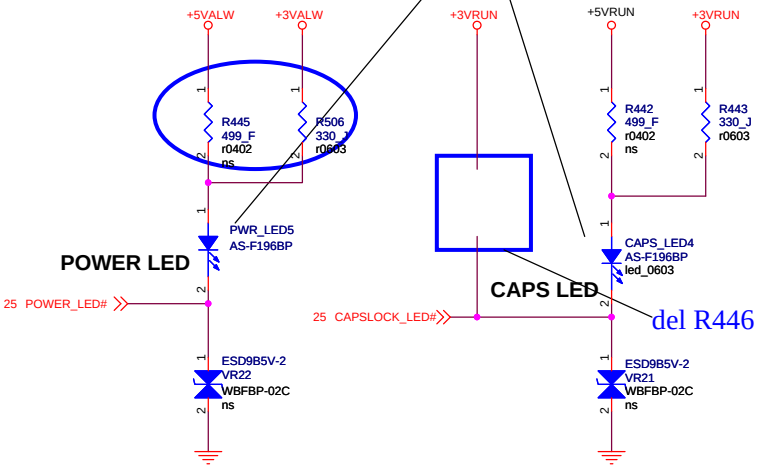


ODD换为康祥的料 lihong 0514

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	SATA HDD/ODD	
Size A3	Document Number N480	Rev 1.2
Date: Wednesday, September 12, 2012	Sheet 34 of 64	

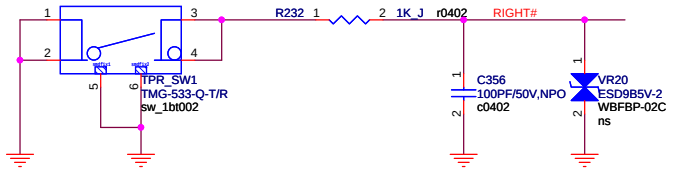


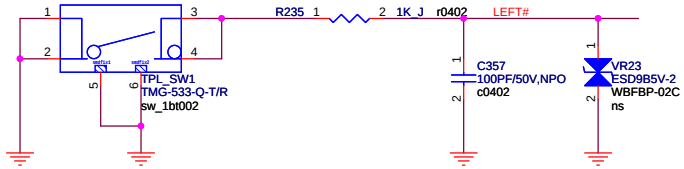
LED color Blue->White lihong 0521



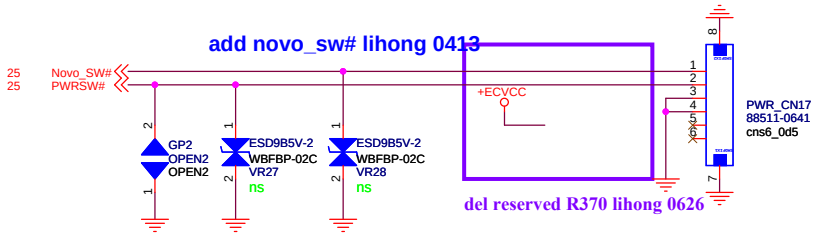
HDD LED-> Caps LED lihong 0510

del R446 already PU in chipset lihong 0503





add novo_sw# lihong 0413



del reserved R370 lihong 0626

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division		
Title	LED TP BTN		
Size A3	Document Number N480		Rev 1.2
Date: Wednesday, September 12, 2012	Sheet 35	of	64

+3VRUN 5,11,12,13,14,15,16,17,18,20,22,23,25,26,27,30,31,32,34,35,39,40,41,42,43,44,47,48,49,51,53

COLAY

+3VRUN — FB34 120ohm/100MHZ,500mA I0603 — 3V3_IN

R510 1 — 2 0_J R0603 ns

for Co-lay RTS5138 lihong 0411

12 Cardreader_48MHZ

C272 1 1uF/6.3V,X5R c0402 DV18

R98 6.2K_F r0402

Zdiff = 90 ohm

15 USB_PN_CD

15 USB_PP_CD

R511 1 0_J 2 r0402

R516 1 0_J 2 r0402

3V3_IN

400mA Card_3V3

C274 4.7uF/6.3V,X5R c0603

C86 0.1UF/10V,X5R c0402

C84 1uF/6.3V,X5R c0402

U13

RREF DM DP 3V3_IN CARD_3V3 SDREG GND

RTS5179

V18 XD_D7 SP14 SP13 SP12 SP11 XD_CD# SP1 SP2 SP3 SP4 SP5

SP10 GPIO0 SP9 SP8 SP7 SP6

RTS5179 QFN24_0D5_4X4

CARD_3V3

C87 0.1UF/10V,X5R c0402

C294 4.7uF/6.3V,X5R c0603

C92 0.1UF/10V,X5R c0402

Share Pin

SP1	SD_WP
SP3	SD_D1
SP4	SD_D0
SP6	SD_CD#
SP8	SD_CLK
SP10	SD_CMD
SP12	SD_D3
SP13	SD_D2

SD_CLK R971 2 0_J R0402 SD_CLK_R

Add for EMC

C368 22PF/50V,NPO c0402

CN28 CS1S-065 sd_card_cs1s-065

SD_D3 SD_CMD SD_CLK_R SD_D0 SD_D1 SD_D2 SD_CD# SD_WP

DAT3 CMD VSS1 VDD CLK VSS2 DAT0 DAT1 DAT2 CD WP GND1 GND2 GND3 GND4

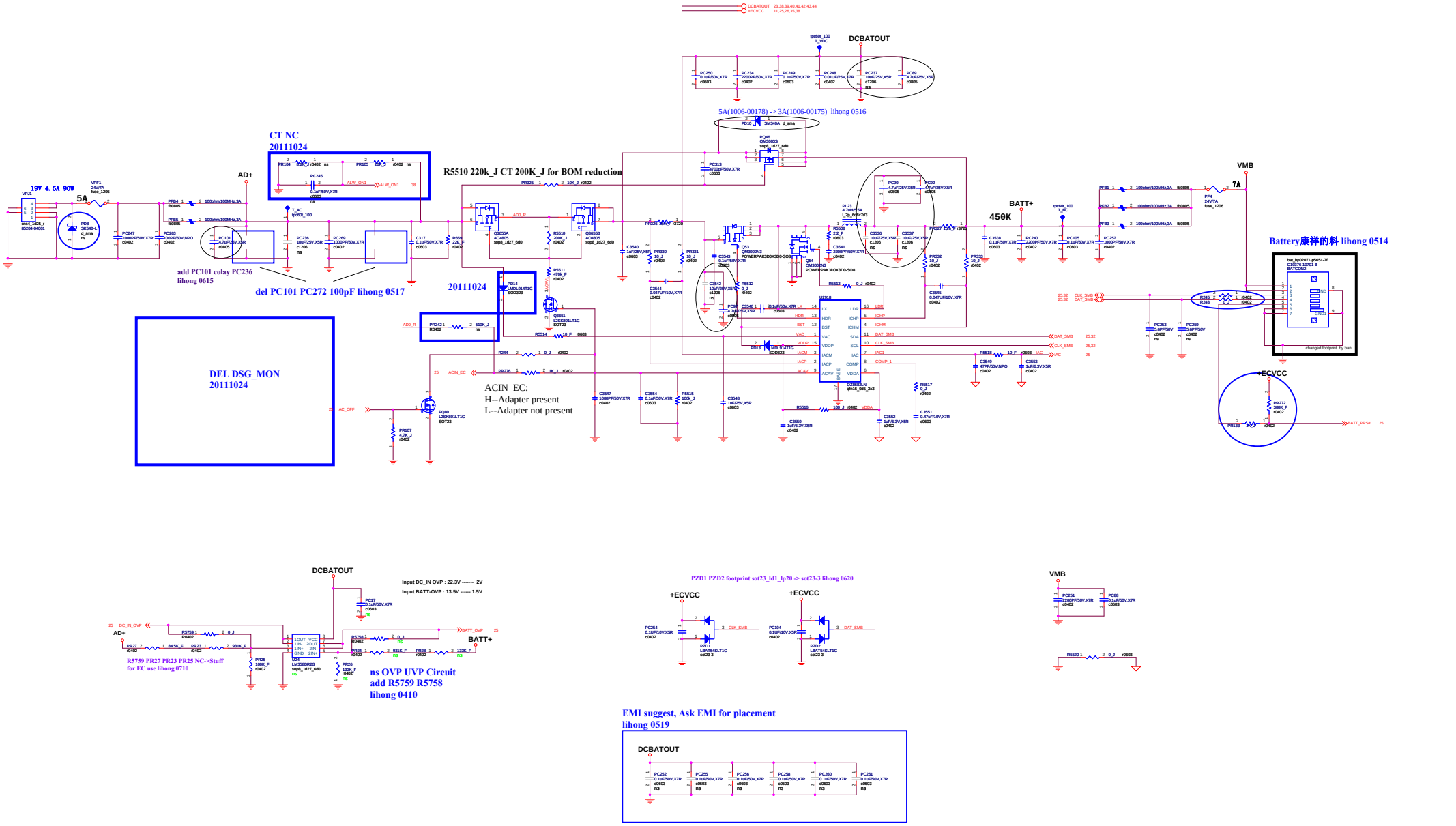
CARD_3V3

C388 1UF/6.3V,X5R c0402

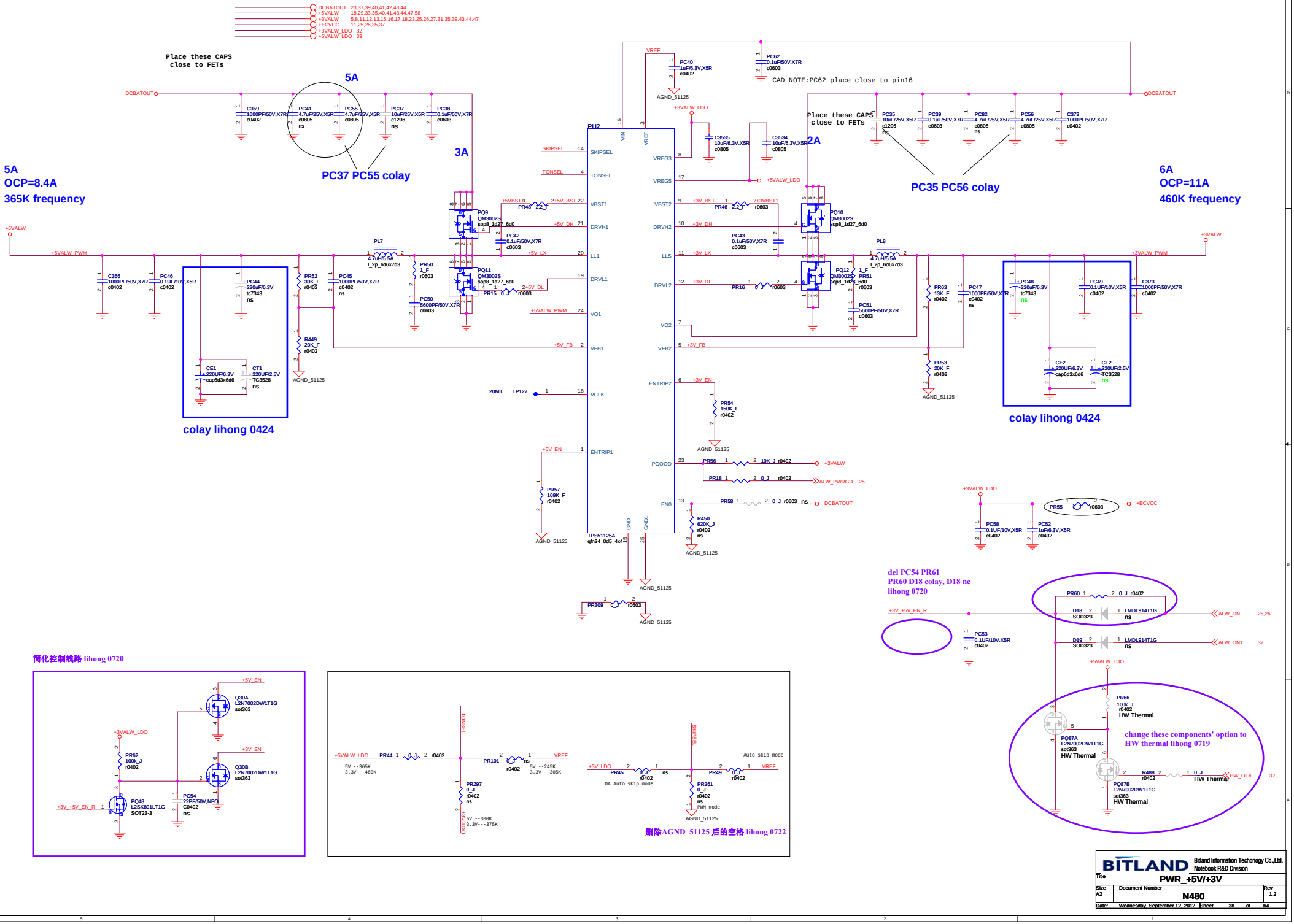
C93 0.1UF/10V,X5R c0402

BITLAND Bitland Information Techonogy Co.,Ltd. Notebook R&D Division

Title	Card Reader(RTS5179)	
Size A4	Document Number N480	Rev 1.2
Date: Wednesday, September 12, 2012	Sheet 36 of 64	



BITLAND	Bitland Information Technology Co.,Ltd. Notebook R&D Division		
Title	PWR_Charger-_AC_BATT_J		
Size A1	Document Number N480		Rev 1.2
Date: Wednesday, September 12, 2012	Sheet 37 of 64		


DCBATOUT 23,37,39,40,41,42,43,44
+5VALW 18,29,33,35,40,41,43,44,47,58
+3VALW 5,8,11,12,13,15,16,17,18,23,25,26,27,31,35,39,43,44,47
+ECVCC 11,25,26,35,37
+3VALW_LDO 32
+5VALW_LDO 39
Place these CAPS close to FETs
5A
3A
PC37 PC55 colay
5A
OCP=8.4A
365K frequency
colay lihong 0424
CAD NOTE:PC62 place close to pin16
Place these CAPS close to FETs
2A
PC35 PC56 colay
6A
OCP=11A
460K frequency
colay lihong 0424
PU2
TPS51125A
qfn24_0d5_4x4
del PC54 PR61
PR60 D18 colay, D18 nc
lihong 0720
change these components' option to HW thermal lihong 0719
简化控制线路 lihong 0720
删除AGND_51125 后的空格 lihong 0722
BITLAND
Bitland Information Techonogy Co.,Ltd.
Notebook R&D Division
PWR_+5V/+3V
N480
Wednesday, September 12, 2012
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+5VALW 18,29,33,35,38,40,41,43,44,47,58
DCBATOUT 23,37,38,40,41,42,43,44
+1_5VSUS 5,8,20,43,57
+3VRUN 5,11,12,13,14,15,16,17,18,20,22,23,25,26,27,30,31,32,34,35,36,40,41,42,43,44,47,48,49,51,53
+5VRUN 11,12,18,22,25,29,30,32,34,35,40,42,43
+3VALW 5,8,11,12,13,15,16,17,18,23,25,26,27,31,35,38,43,44,47
+0_75VRUN 20,43,47
+5VALW_LDO 38

3A

15A

OCP=21A

V1.1

RT8207

TCL与N401时序不同

Io=2A

colay

Colay

C71 colay CE4 in bottom side lihong 0509

+0_75VRUN should ramp down earlier than CPU VDDQ rail in S3-entry and ramp up after CPU VDDQ rail in S3-exit

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division		
Title	PWR_+1_5V/+0_75V		
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+5VALW 18,29,33,35,38,41,43,44,47,58
DCBATOUT 23,37,38,39,41,42,43,44
+1_05VRUN 4,5,7,11,13,17,18,26,42,44,48,49,51,52
+3VRUN 5,11,12,13,14,15,16,17,18,20,22,23,25,26,27,30,31,32,34,35,36,39,41,42,43,44,47,48,49,51,53
+5VRUN 11,12,18,22,25,29,30,32,34,35,42,43
+1_8VRUN 8,16,17,43,44,47,49,51,52

Move PC95 PC214 to PWM side lihong 0518
PC95 PC214 colay in top side lihong 0509

3A

PC95 330uF/2V tc7343 ns
PC214 330uF/2V tc3528 ns

DCBATOUT

PC75 0.1uF/50V,X7R c0603
PC78 10uF/25V,X5R c1206 ns
PC76 10uF/25V,X5R c1206 ns
C383 1000PF/50V,X7R c0402
PC61 4.7uF/25V,X5R c0805
PC63 4.7uF/25V,X5R c0805

Place these CAPS close to FETs

PR81 0603->0805 for thermal reason lihong 0615

290kHz
8.5A+ 7A

+1_05VRUN_F

PL10 1.0UH_11.5x10.4 !_2p_11d5x10

+1_05VRUN

PR382 220K_F R0402
PR383 110K_F R0402
PR381 22_J R0402
1.069V
PC357 470PF/50V,X7R C0402
PR386 140K_F R0402
PC358 0.1UF/10V,X5R C0402
PC359 0.1UF/10V,X5R C0402
PR387 270K_F R0402
PC356 1uF/6.3V,X5R C0402
R422 51K_J R0402
C26 0.01UF/25V,X7R C0402
GND8116_VTT

PU5 OZ8116 qfn16_0d4_2d5x2d5
VSET VREF TSET VDDA2 GNDA CSN CSP HDR GNDA1 ONOFF PGD BST LDR GNDP VDDP

VTT_CSN
VTT_CSP
VTT_DH
VTT_BST
VTT_DL
VTT_EN/PSV
VTT_PGOOD_PWM
+5VALW

PC77 1 2 0.1uF/50V,X7R c0603
PD16 LMDL914T1G sod323
PC84 1uF/6.3V,X5R c0402
PR22 0_J r0603

PQ15 QM3022M6 powerpak_so8
PQ16 QM3018M6 powerpak_so8

PR81 1_J r0805
PC86 4700pF/50V,X7R c0603

PR384 100K_J R0402
PR385 51_J R0402
PR388 100K_F r0402
PC360 6800PF/50V,X7R c0603
0402 to 0603

PC81 0.1UF/10V,X5R c0402
CE5 330UF/2.5V cap7d8x6d6
PC85 330uF/2V tc7343 ns
PR109 1 10_J r0402
PC91 330uF/2V tc7343 ns
CE6 330UF/2.5V cap7d8x6d6
C384 1000PF/50V,X7R c0402

PC85 colay CE5
PC91 colay CE6
in bottom side lihong 0509

VCCP_SENSE 7
VSSP_SENSE 7
PR33 2 1 10_J r0402

PC361 22PF/50V,NPO C0402
PR389 6.8K_J R0402 ns
PC362 0.01UF/25V,X7R C0402

+3VRUN
PR75 2 1 10K_J r0402
39,47 VCCP_PGOOD
PR77 1 2 0_J r0402
VTT_PGOOD_PWM
25,26,39,41,43,44 RUN_ON
PR78 1 2 100_J r0402
VTT_EN/PSV
PC80 0.1UF/10V,X5R c0402 ns

PR3901 2 0_J R0603

Signal Ground Power Ground

Single point ground connection

+5VRUN

PC106 22uF/6.3V,X5R c0805 ns
PC107 22uF/6.3V,X5R c0805
PC108 0.1UF/10V,X5R c0402

PU7 RT8055GQW DFN10_0D5_3X3
PVDD_2 PVDD_1 VDD FB COMP PGND LX_2 LX_1 GND SHDN/RT THRM GN9

PR111 2.2_F r0603
PC109 0.1UF/10V,X5R c0402 ns
PC113 c0402 2200PF/50V,X7R
PR112 30K_F r0402
PC114 0.1UF/10V,X5R ns c0402
PR113 330K_F
PC115 1000PF/50V,X7R c0402
PR114 240K_F r0402
PR115 300K_F r0402
PC115 c0402 0.1UF/10V,X5R ns

PL12 2_2p_6d6x7d3 2.2UH_6.86x6.47

3A
OCP=NA
1.2MHz

PC110 22uF/6.3V,X5R c0805
PC111 22uF/6.3V,X5R c0805
PC112 0.1UF/10V,X5R c0402

0.042A to PCH

+1_8VRUN

PR241 2.2_F r0603 ns

dengrl change R and C location

Vout=0.8V*(1+PR115/PR114)

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Title: PWR_1.05V_VCCP/1.8V/VCCIO

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R140	0	NA	100k	VCC
Fsw	300kHz	500kHz	600kHz	1M

		VID1	VID0
Vout1	0.675V	1	1
Vout2	0.725V	0	1
Vout3	0.8V	1	0
Vout4	0.9V	0	0

+5VALW 18,29,33,35,38,40,43,44,47,58
DCBATOUT 23,37,38,39,40,42,43,44
+VCCSA 8
+3VRUN 5,11,12,13,14,15,16,17,18,20,22,23,25,26,27,30,31,32,34,35,36,39,40,42,43,44,47,48,49,51,53

8 VCCSA_SELECT0 — PR240 10K_J r0402 — VCCSA_VID0
8 VCCSA_SELECT1 — PR295 10K_J r0402 — VCCSA_VID1
del 0ohm PR129 PR130
lihong 0723

+5VALW
PC119 1uF/6.3V,X5R c0402
PR1252 r0603 2.2_F
PC121 0.1uF/50V,X7R c0603
VCCSA_BST
VCCSA_DH_R
VCCSA_EN/PSV
VCCSA_VID0
VCCSA_VID1
VCCSA_PGOOD_PWM
EU10 RT8241 qfn12_0d4_2x2
EN VCC BOOT UG PH LG GND FB CS GNDL AGNDL
PR141 0.6K_F r0402
OCP=PR141/16*0.001A
+VCCSA_F

PQ19 QM3002N3 POWERPAK3D0X3D0-SO8
PQ20 QM3014N3 powerpak3d0x3d0-so8
VCCSA_DL — PR121 0_J r0603 — VCCSA_LGATE_R
PR127 1_F r0603
PC126 4700pF/50V,X7R c0603
PL13 2.2UH_6.86x6.47 I_2p_6d6x7d3

DCBATOUT
PC116 0.1uF/50V,X7R c0603
PC117 10uF/25V,X5R c1206 ns
PC118 10uF/25V,X5R c1206 ns
C386 1000PF/50V,X7R c0402
PC64 4.7uF/25V,X5R c0805
PC66 4.7uF/25V,X5R c0805
2A

6A
6A
OCP=10.5A
300kHz

PC128 220uF/6.3V tc7343 ns
PC124 4.7uF/6.3V,X5R c0603
PC123 0.1UF/10V,X5R C0402
C387 1000PF/50V,X7R c0402
CE7 220UF/6.3V cap6d3x6d6
+VCCSA_F
+VCCSA

PC128 colay CE7
in bottom side lihong 0509

+3VRUN — PR1221 100k_J r0402 ns
25,26,39,40,43,44 RUN_ON — PR1231 100_J r0402 — VCCSA_EN/PSV
PC122 0.1UF/10V,X5R c0402 ns

25,47 RUN_PWRGD — PR1241 0_J r0402 — VCCSA_PGOOD_PWM
+3VRUN — PR1262 10k_F r0402 ns
PC125 100PF/50V,NPO c0402 ns

+VCCSA_F — PR131 0_J r0402 — VCCSA_SENSE 8

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Notebook R&D Division
Title: PWR_VCCSA
Size: A3 | Document Number: N480 | Rev: 1.2
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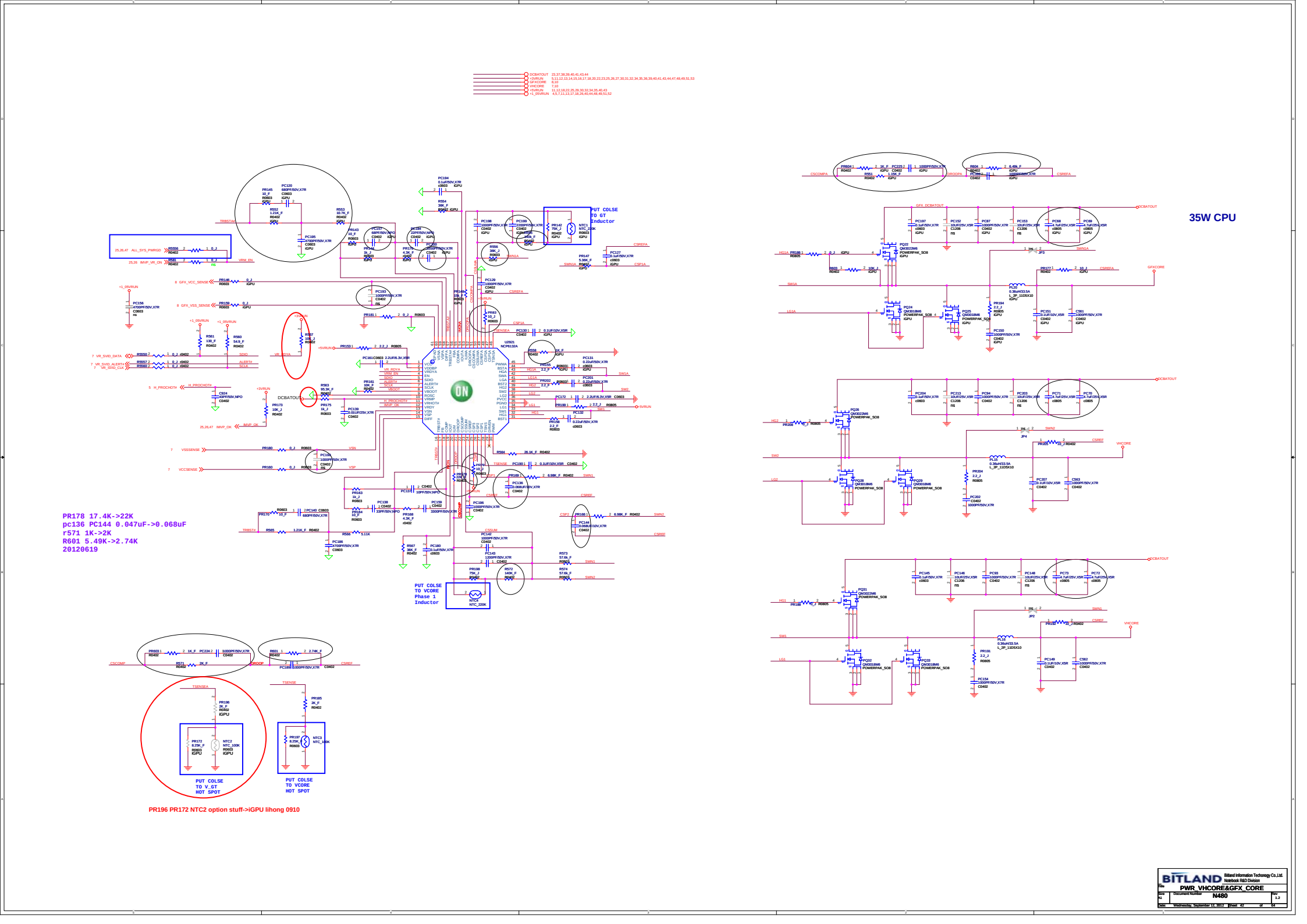
35W CPU
PUT COLSE TO GT Enductor
PUT COLSE TO VCORE Phase 1 Inductor
PUT COLSE TO V_GT HOT SPOT
PUT COLSE TO VCORE HOT SPOT
PR178 17.4K->22K
pc136 PC144 0.047uF->0.068uF
r571 1K->2K
R601 5.49K->2.74K
20120619
PR196 PR172 NTC2 option stuff->iGPU lihong 0910
PWR_VHCORE&GFX_CORE
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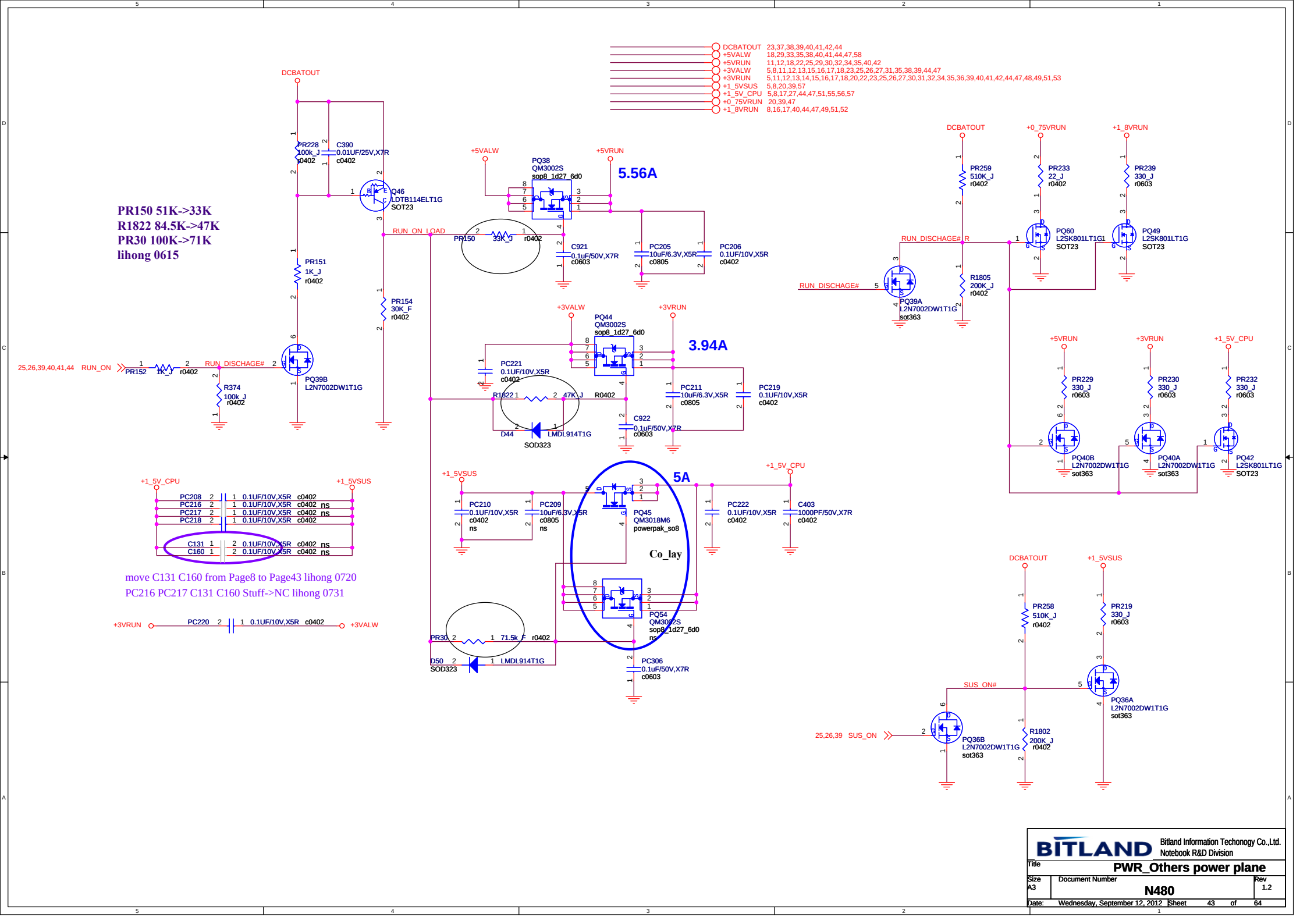
Notebook R&D Division
N480
Wednesday, September 12, 2012


DCBATOUT 23,37,38,39,40,41,42,44
+5VALW 18,29,33,35,38,40,41,44,47,58
+5VRUN 11,12,18,22,25,29,30,32,34,35,40,42
+3VALW 5,8,11,12,13,15,16,17,18,23,25,26,27,31,35,38,39,44,47
+3VRUN 5,11,12,13,14,15,16,17,18,20,22,23,25,26,27,30,31,32,34,35,36,39,40,41,42,44,47,48,49,51,53
+1_5VSUS 5,8,20,39,57
+1_5V_CPU 5,8,17,27,44,47,51,55,56,57
+0_75VRUN 20,39,47
+1_8VRUN 8,16,17,40,44,47,49,51,52
PR150 51K->33K
R1822 84.5K->47K
PR30 100K->71K
lihong 0615
5.56A
3.94A
5A
Co_lay
move C131 C160 from Page8 to Page43 lihong 0720
PC216 PC217 C131 C160 Stuff->NC lihong 0731
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Notebook R&D Division
PWR_Others power plane
N480
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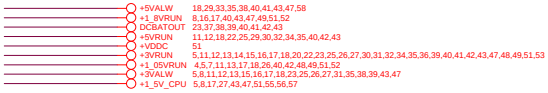
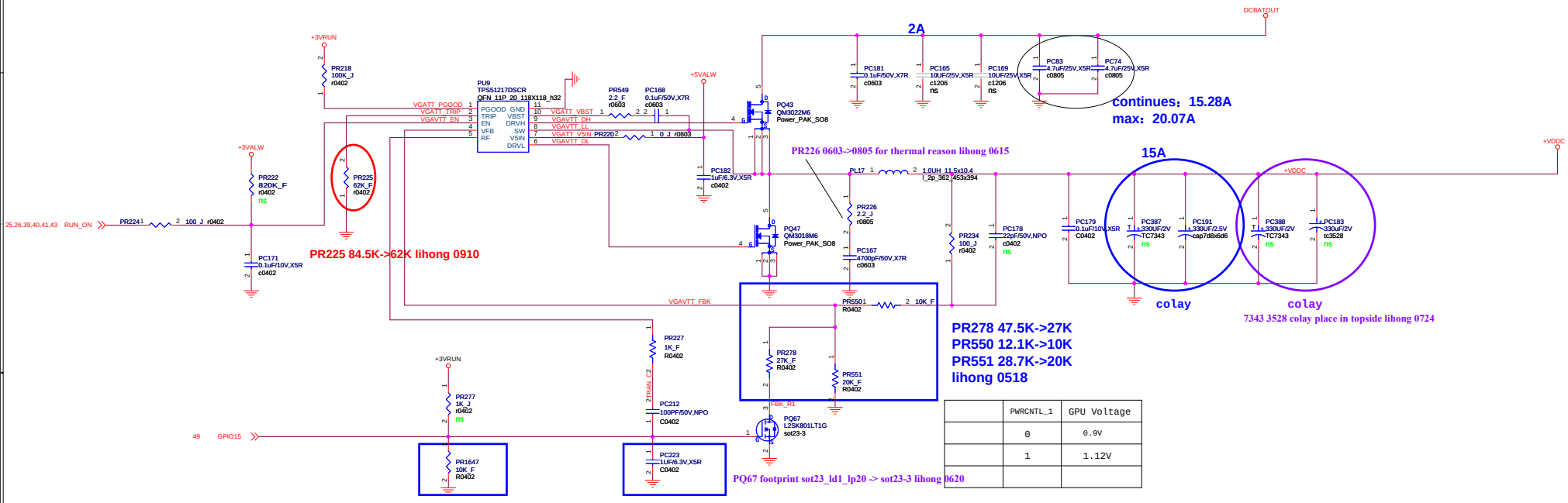
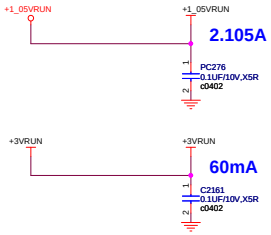


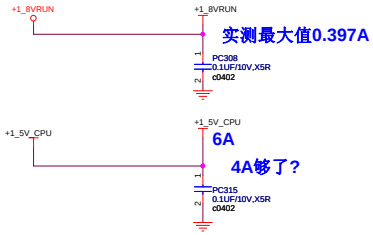


	PWRCNTL_1	GPU Voltage
	0	0.9V
	1	1.12V

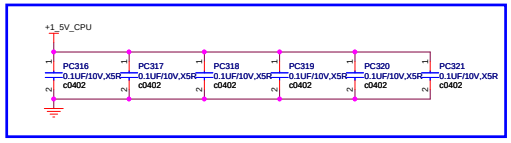
显卡其他供电net

VDDC should reach 90% before VDD_CT
starts to ramp up (or vice versa)





EMI suggest lihong 0516



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Title	PWR_GFX	
Size A2	Document Number N480	Rev 1.2
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BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division
Title	Debug
Size: A4	Document Number: N480
Rev: 1.2	
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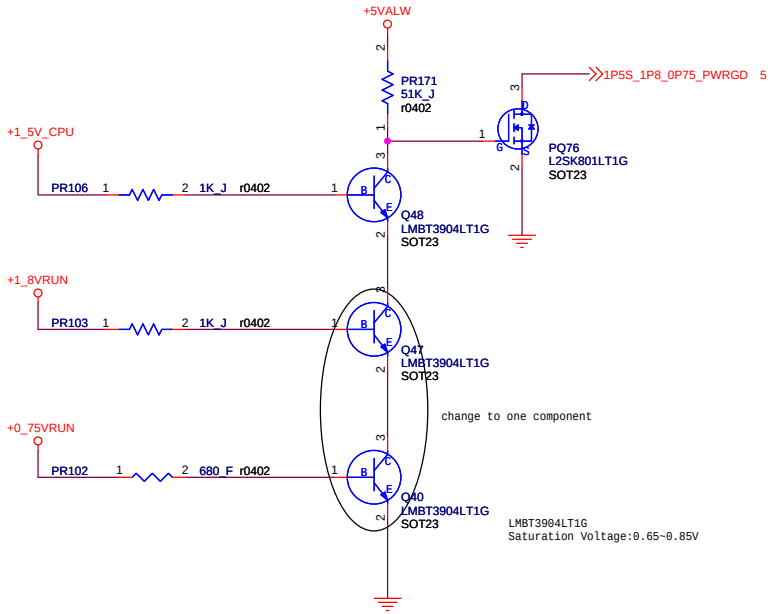
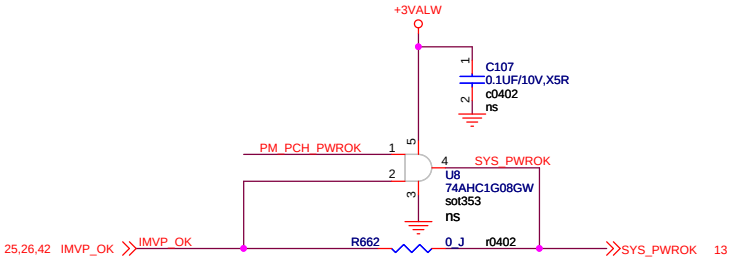
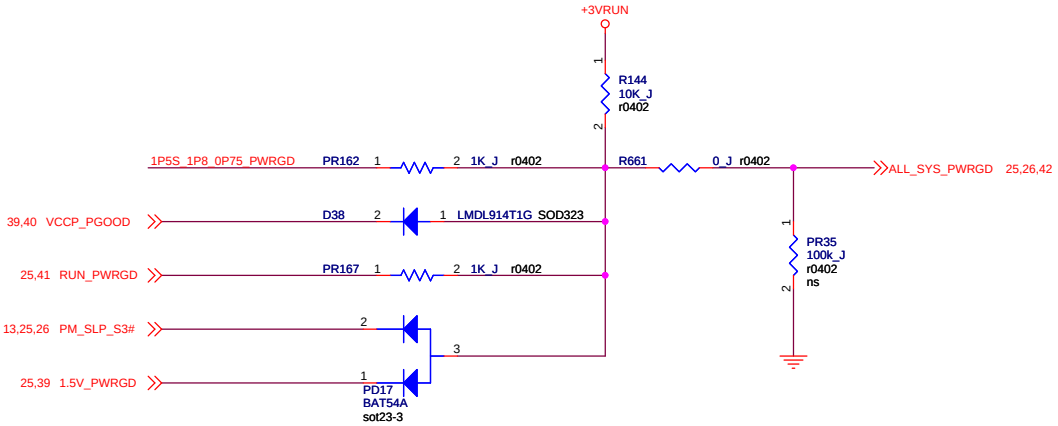
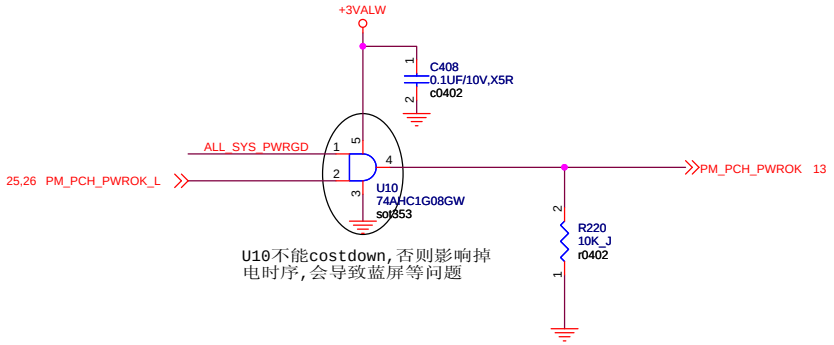
BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division
Title	eDP
Size: A4	Document Number: N480
Rev: 1.2	
Date: Wednesday, September 12, 2012	Sheet 46 of 64

+1_5V_CPU 5,8,17,27,43,44,51,55,56,57
+1_8VRUN 8,16,17,40,43,44,49,51,52
+0_75VRUN 20,39,43
+3VALW 5,8,11,12,13,15,16,17,18,23,25,26,27,31,35,38,39,43,44
+5VALW 18,29,33,35,38,40,41,43,44,58
+3VRUN 5,11,12,13,14,15,16,17,18,20,22,23,25,26,27,30,31,32,34,35,36,39,40,41,42,43,44,48,49,51,53









U10不能costdown,否则影响掉电时序,会导致蓝屏等问题

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Title	Power Sequence	
Size A3	Document Number N480	Rev 1.2
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+3VRUN 5,11,12,13,14,15,16,17,18,20,22,23,25,26,27,30,31,32,34,35,36,39,40,41,42,43,44,47,49,51,53
+1_05VRUN 4,5,7,11,13,17,18,26,40,42,44,49,51,52

COMPONENTS SHOWN ARE EXAMPLES ONLY AND NOT NECESSARILY QUALIFIED

0.22uF->0.1uF lihong 0626

U2910A

PCI EXPRESS INTERFACE

4 GFX_TX0P_C	AF30	PCIE_RX0P	PCIE_TX0P	AH30	PCIE_TXP0	C3244 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX0P_C 4
4 GFX_TX0N_C	AE31	PCIE_RX0N	PCIE_TX0N	AG31	PCIE_TXN0	C3245 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX0N_C 4
4 GFX_TX1P_C	AE29	PCIE_RX1P	PCIE_TX1P	AG29	PCIE_TXP1	C3246 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX1P_C 4
4 GFX_TX1N_C	AD28	PCIE_RX1N	PCIE_TX1N	AF28	PCIE_TXN1	C3247 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX1N_C 4
4 GFX_TX2P_C	AD30	PCIE_RX2P	PCIE_TX2P	AF27	PCIE_TXP2	C3248 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX2P_C 4
4 GFX_TX2N_C	AC31	PCIE_RX2N	PCIE_TX2N	AF26	PCIE_TXN2	C3249 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX2N_C 4
4 GFX_TX3P_C	AC29	PCIE_RX3P	PCIE_TX3P	AD27	PCIE_TXP3	C3250 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX3P_C 4
4 GFX_TX3N_C	AB28	PCIE_RX3N	PCIE_TX3N	AD26	PCIE_TXN3	C3251 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX3N_C 4
4 GFX_TX4P_C	AB30	PCIE_RX4P	PCIE_TX4P	AC25	PCIE_TXP4	C3252 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX4P_C 4
4 GFX_TX4N_C	AA31	PCIE_RX4N	PCIE_TX4N	AB25	PCIE_TXN4	C3253 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX4N_C 4
4 GFX_TX5P_C	AA29	PCIE_RX5P	PCIE_TX5P	Y23	PCIE_TXP5	C3254 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX5P_C 4
4 GFX_TX5N_C	Y28	PCIE_RX5N	PCIE_TX5N	Y24	PCIE_TXN5	C3255 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX5N_C 4
4 GFX_TX6P_C	Y30	PCIE_RX6P	PCIE_TX6P	AB27	PCIE_TXP6	C3256 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX6P_C 4
4 GFX_TX6N_C	W31	PCIE_RX6N	PCIE_TX6N	AB26	PCIE_TXN6	C3257 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX6N_C 4
4 GFX_TX7P_C	W29	PCIE_RX7P	PCIE_TX7P	Y27	PCIE_TXP7	C3258 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX7P_C 4
4 GFX_TX7N_C	V28	PCIE_RX7N	PCIE_TX7N	Y26	PCIE_TXN7	C3259 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX7N_C 4
4 GFX_TX8P_C	V30	PCIE_RX8P	PCIE_TX8P	W24	PCIE_TXP8	C3260 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX8P_C 4
4 GFX_TX8N_C	U31	PCIE_RX8N	PCIE_TX8N	W23	PCIE_TXN8	C3261 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX8N_C 4
4 GFX_TX9P_C	U29	PCIE_RX9P	PCIE_TX9P	V27	PCIE_TXP9	C3262 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX9P_C 4
4 GFX_TX9N_C	T28	PCIE_RX9N	PCIE_TX9N	U26	PCIE_TXN9	C3263 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX9N_C 4
4 GFX_TX10P_C	T30	PCIE_RX10P	PCIE_TX10P	U24	PCIE_TXP10	C3264 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX10P_C 4
4 GFX_TX10N_C	R31	PCIE_RX10N	PCIE_TX10N	U23	PCIE_TXN10	C3265 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX10N_C 4
4 GFX_TX11P_C	R29	PCIE_RX11P	PCIE_TX11P	T26	PCIE_TXP11	C3266 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX11P_C 4
4 GFX_TX11N_C	P28	PCIE_RX11N	PCIE_TX11N	T27	PCIE_TXN11	C3267 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX11N_C 4
4 GFX_TX12P_C	P30	PCIE_RX12P	PCIE_TX12P	T24	PCIE_TXP12	C3268 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX12P_C 4
4 GFX_TX12N_C	N31	PCIE_RX12N	PCIE_TX12N	T23	PCIE_TXN12	C3269 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX12N_C 4
4 GFX_TX13P_C	N29	PCIE_RX13P	PCIE_TX13P	P27	PCIE_TXP13	C3270 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX13P_C 4
4 GFX_TX13N_C	M28	PCIE_RX13N	PCIE_TX13N	P26	PCIE_TXN13	C3271 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX13N_C 4
4 GFX_TX14P_C	M30	PCIE_RX14P	PCIE_TX14P	P24	PCIE_TXP14	C3272 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX14P_C 4
4 GFX_TX14N_C	L31	PCIE_RX14N	PCIE_TX14N	P23	PCIE_TXN14	C3273 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX14N_C 4
4 GFX_TX15P_C	L29	PCIE_RX15P	PCIE_TX15P	M27	PCIE_TXP15	C3274 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX15P_C 4
4 GFX_TX15N_C	K30	PCIE_RX15N	PCIE_TX15N	N26	PCIE_TXN15	C3275 1 2 0.1uF/10V_X5R c0402 GPU	GFX_RX15N_C 4

CLOCK

12 PCIE_REFCLKP → PCIE_REFCLKP AK30
12 PCIE_REFCLKN → PCIE_REFCLKN AK32

CALIBRATION

PCIE_CALRP Y22 — R5399 1.27k_F r0402 — +1_05VRUN
PCIE_CALRN AA22 — R5400 2k_F r0402

For Park-S3: the PWRGOOD pin must need to pull down to GND

For M9X-S2/S3: This PWRGOOD pin is not connected

N10 PWRGOOD

R5401 10K_J r0402

+3VRUN

R5402 10K_J r0402 ns

PERST# buf AL27 PERSTB

5,15,25,26,27,31 PLT_RST# — R5403 0_J r0402

Thames PRO S3
bga631_0d8x1d0_23x23

COMPONENTS SHOWN ARE EXAMPLES ONLY AND NOT NECESSARILY QUALIFIED

GPU_BOSS1 GPU_BOSS2
1101-00117->1101-00118
lihong 0627

GPU_BOSS1 — Hole+Dowel hole4d06_2d24 GPU

GPU_BOSS2 — Hole+Dowel hole4d06_2d24 GPU

del PCIE_RST# and PCI_REQ#0 for pure GPU lihong 0411

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Title: Robson_XT(PCI-E)

Size: A2 | Document Number: N480 | Rev: 1.2

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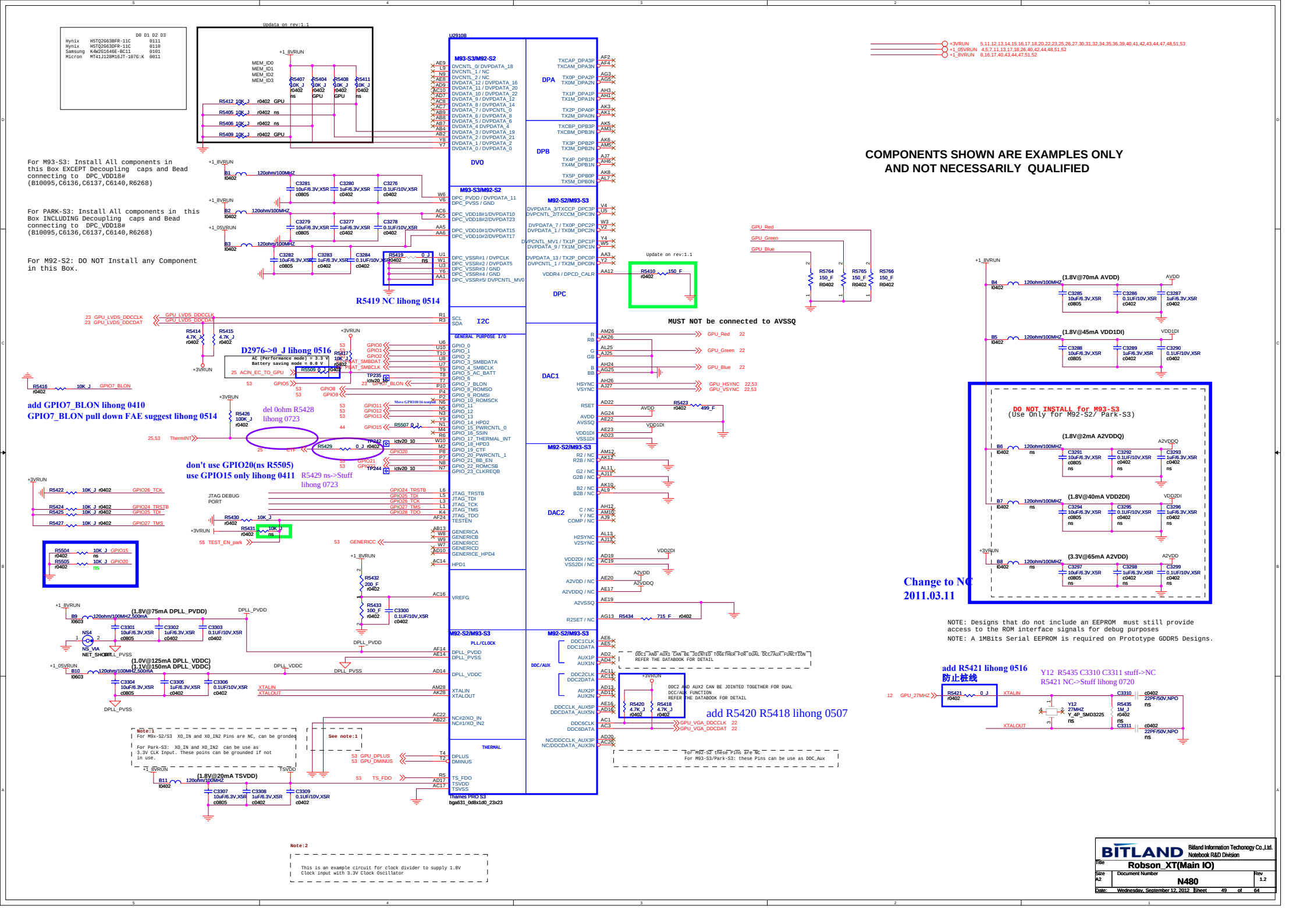
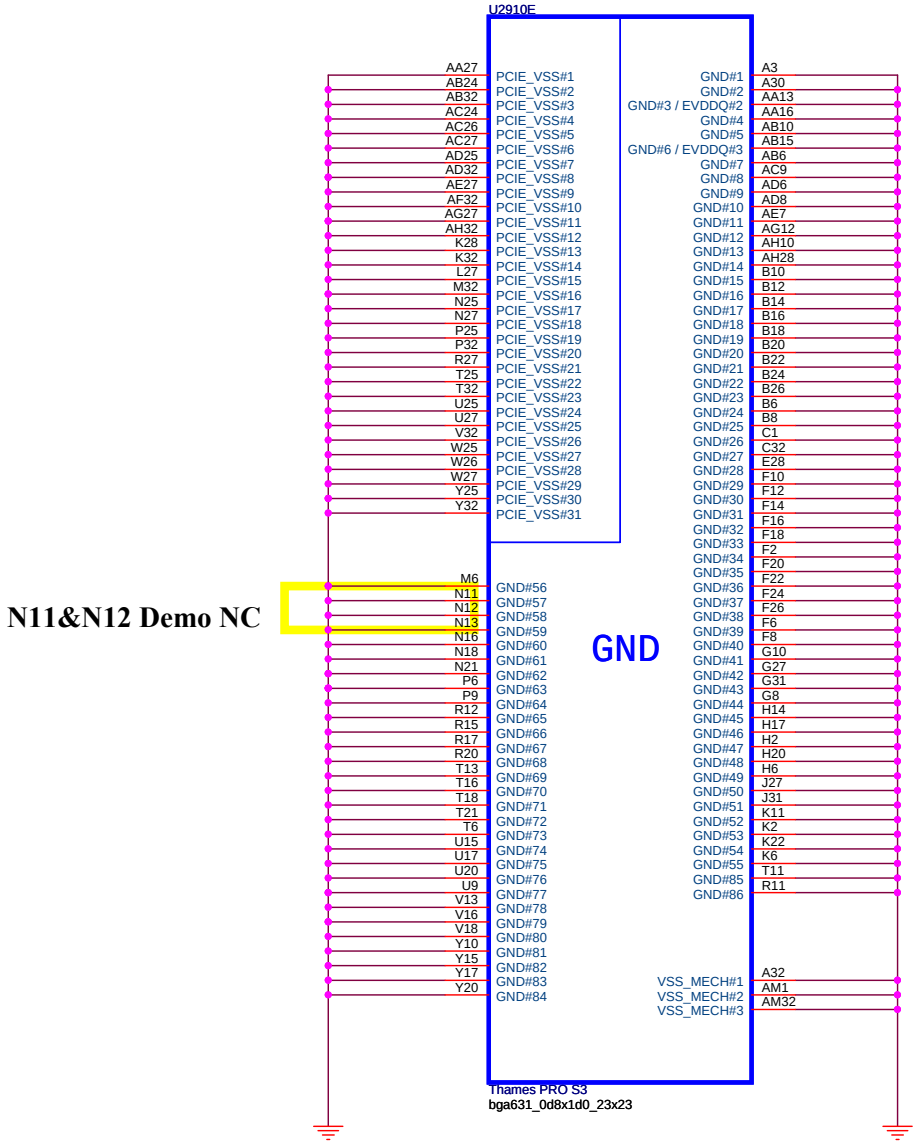

D0 D1 D2 D3
Hynix H5TQ2G63BFR-11C 0111
Hynix H5TQ2G63DFR-11C 0110
Samsung K4W2G1646E-BC11 0101
Micron MT41J128M16JT-107G:K 0011
Updata on rev:1.1
U2910B
M93-S3/M92-S2
DPA
DPB
DVO
DPC
I2C
GENERAL PURPOSE I/O
DAC1
DAC2
JTAG DEBUG PORT
THERMAL
Thames PRO S3
bga631_0d8x1d0_23x23
For M93-S3: Install All components in this Box EXCEPT Decoupling caps and Bead connecting to DPC_VDD18# (B10095,C6136,C6137,C6140,R6268)
For PARK-S3: Install All components in this Box INCLUDING Decoupling caps and Bead connecting to DPC_VDD18# (B10095,C6136,C6137,C6140,R6268)
For M92-S2: DO NOT Install any Component in this Box.
R5419 NC lihong 0514
D2976->0 J lihong 0516
add GPIO7_BLON lihong 0410
GPIO7_BLON pull down FAE suggest lihong 0514
del 0ohm R5428 lihong 0723
don't use GPIO20(ns R5505)
use GPIO15 only lihong 0411
R5429 ns->Stuff lihong 0723
COMPONENTS SHOWN ARE EXAMPLES ONLY AND NOT NECESSARILY QUALIFIED
MUST NOT be connected to AVSSQ
DO NOT INSTALL for M93-S3
(Use Only for M92-S2/ Park-S3)
Change to NC 2011.03.11
add R5420 R5418 lihong 0507
add R5421 lihong 0516
防止桩线
Y12 R5435 C3310 C3311 stuff->NC
R5421 NC->Stuff lihong 0720
NOTE: Designs that do not include an EEPROM must still provide access to the ROM interface signals for debug purposes
NOTE: A 1MBits Serial EEPROM is required on Prototype GDDR5 Designs.
BITLAND
Bitland Information Techonogy Co.,Ltd.
Notebook R&D Division
Robson_XT(Main IO)
N480
Wednesday, September 12, 2012



N11&N12 Demo NC

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division		
Title	Robson_XT(Core_GND)		
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CRB MVDDQ:
1uF*5
4.7uF*3 or 10uF*3

+1_5V_CPU 5,8,17,27,43,44,47,55,56,57
+1_05VRUN 4,5,7,11,13,17,18,26,40,42,44,48,49,52
+1_8VRUN 8,16,17,40,43,44,47,49,52
+3VRUN 5,11,12,13,14,15,16,17,18,20,22,23,25,26,27,30,31,32,34,35,36,39,40,41,42,43,44,47,48,49,53
+VDDC 44

+1_5V_CPU

(for DDR2 and GDDR3: 1.8V@2.2A VDDR1) (For DDR3, MVDDQ = 1.5V@2.0A)

C3312 1UF/6.3V,X5R C0402_BGA
C3313 1UF/6.3V,X5R C0402_BGA
C3315 1UF/6.3V,X5R C0402_BGA
C3314 1UF/6.3V,X5R C0402_BGA
C3335 1uF/6.3V,X5R c0402
C3345 10uF/6.3V,X5R c0603
C3346 10uF/6.3V,X5R c0603
C3347 10uF/6.3V,X5R c0603
C3348 10uF/6.3V,X5R c0603

VDDR1 del 1uF C3327 C3328 C3329 C3330 C3331 C3332 C3333 C3334
0.1uF C3316 C3317 C3318
10uF C3344
lihong 0719

U2910D

MEM I/O
H13 VDDR1#1
H16 VDDR1#2
H19 VDDR1#3
J10 VDDR1#4
J23 VDDR1#5
J24 VDDR1#6
J9 VDDR1#7
K10 VDDR1#8
K23 VDDR1#9
K24 VDDR1#10
K9 VDDR1#11
L11 VDDR1#12
L12 VDDR1#13
L13 VDDR1#14
L20 VDDR1#15
L21 VDDR1#16
L22 VDDR1#17

LEVEL TRANSLATION
VDD_CT#1
VDD_CT#2
VDD_CT#3
VDD_CT#4

M93-S3/M92-S2 I/O
AA17 VDDR3#1
AA18 VDDR3#2
AB17 VDDR3#3
AB18 VDDR3#4
V12 VDDR4#1 / VDDR5
Y12 VDDR4#2
U12 VDDR4#3 / VDDR5
AA11 NC#1 / VDDR4
Y11 DVCLK / VDDR4
V11 NC#3 / VDDR5
U11 NC / VDDR5

MEM CLK
L17 VDDRHA
L16 VSSRHA

PLL
AM30 PCIE_PVDD
L8 MPV18
H7 SPV18
H8 SPV10
J7 SPVSS

BACK BIAS
M11 BBP#1
M12 BBP#2

PCIE
AB23 PCIE_VDDR#1
AC23 PCIE_VDDR#2
AD23 PCIE_VDDR#3
AE24 PCIE_VDDR#4
AE25 PCIE_VDDR#5
AE26 PCIE_VDDR#6
AF25 PCIE_VDDR#7
AG26 PCIE_VDDR#8
L23 PCIE_VDDC#1
L24 PCIE_VDDC#2
L25 PCIE_VDDC#3
L26 PCIE_VDDC#4
M22 PCIE_VDDC#5
N22 PCIE_VDDC#6
N23 PCIE_VDDC#7
N24 PCIE_VDDC#8
R22 PCIE_VDDC#9
T22 PCIE_VDDC#10
U22 PCIE_VDDC#11
V22 PCIE_VDDC#12

CORE POWER
AA15 VDDC#1
N15 VDDC#2
N17 VDDC#3
R13 VDDC#4
R16 VDDC#5
R18 VDDC#6
Y21 VDDC#7
T12 VDDC#8
T15 VDDC#9
T17 VDDC#10
T20 VDDC#11
U13 VDDC#12
U16 VDDC#13
U18 VDDC#14
V21 VDDC#15
V15 VDDC#16
V17 VDDC#17
V20 VDDC#18
Y13 VDDC#20
Y16 VDDC#21
Y18 VDDC#22
R21 VDDC#23 /BIF_VDDC
U21 VDDC#19/BIF_VDDC

ISOLATED CORE I/O
M13 VDDCI#1
M15 VDDCI#2
M16 VDDCI#3
M17 VDDCI#4
M18 VDDCI#5
M20 VDDCI#6
M21 VDDCI#7
N20 VDDCI#8

Thames PRO S3

PCIE_VDDR_PARK
del 1uF C3324 C3325
lihong 0719

PCIE_VDDR_PARK
(1.8V@500mA PCIE_VDDR)
+1_8VRUN
L85 100ohm/100MHz,3A i0805
C3319 0.1UF/10V,X5R C0402_BGA
C3320 0.1UF/10V,X5R C0402_BGA
C3321 1UF/6.3V,X5R C0402_BGA
C3322 1UF/6.3V,X5R C0402_BGA
C3323 1UF/6.3V,X5R C0402_BGA
C3326 10uF/6.3V,X5R c0603

CRB MVDDQ:
1uF*3
0.1uF*2
10uF*1

(1.1V@2A PCIE_VDDC)
+1_05VRUN
C3336 1UF/6.3V,X5R C0402_BGA
C3337 1UF/6.3V,X5R C0402_BGA
C3338 1UF/6.3V,X5R C0402_BGA
C3339 1UF/6.3V,X5R C0402_BGA
C3340 1UF/6.3V,X5R C0402_BGA
C3341 1UF/6.3V,X5R C0402_BGA
C3342 1UF/6.3V,X5R C0402_BGA
C3343 10uF/6.3V,X5R c0603
C3565 0.1UF/10V,X5R C0402_BGA
C3555 0.1UF/10V,X5R C0402_BGA

CRB MVDDQ:
1uF*7
10uF*1

SEE DATABOOK FOR REQUIRED EDP

+VDDC
C3349 1UF/6.3V,X5R C0402_BGA
C3350 1UF/6.3V,X5R C0402_BGA
C3351 1UF/6.3V,X5R C0402_BGA
C3352 1UF/6.3V,X5R C0402_BGA
C3353 1UF/6.3V,X5R C0402_BGA
C3354 1UF/6.3V,X5R C0402_BGA
C3355 1UF/6.3V,X5R C0402_BGA
C3356 1UF/6.3V,X5R C0402_BGA
C3363 1UF/6.3V,X5R C0402_BGA
C3364 1UF/6.3V,X5R C0402_BGA
C3365 1UF/6.3V,X5R C0402_BGA
C3366 1UF/6.3V,X5R C0402_BGA
C3367 1UF/6.3V,X5R C0402_BGA
C3368 1UF/6.3V,X5R C0402_BGA
C3369 1UF/6.3V,X5R C0402_BGA
C3370 1UF/6.3V,X5R C0402_BGA
C3377 1UF/6.3V,X5R C0402_BGA ns
C3378 1UF/6.3V,X5R C0402_BGA ns
C3379 1UF/6.3V,X5R C0402_BGA ns
C3380 0.1UF/10V,X5R C0402_BGA
C3381 0.1UF/10V,X5R C0402_BGA
C3382 0.1UF/10V,X5R C0402_BGA
C3386 10uF/6.3V,X5R c0805
C3387 10uF/6.3V,X5R c0805
C3388 10uF/6.3V,X5R c0805
C3389 10uF/6.3V,X5R c0805
C3390 10uF/6.3V,X5R c0805
C3391 10uF/6.3V,X5R c0805

CRB MVDDQ:
1uF*16
4.7uF*4 or 10uF*4

+VDDC
del 1uF C3357 C3371 C3372
NC 1uF C3377 C3378 C3379
lihong 0719

del B16 FAE suggest lihong 0517

(0.95V-1.1V@(2-??)A VDDCI)
VDDCI
C3398 10uF/6.3V,X5R c0805 ns
C3399 10uF/6.3V,X5R c0805 ns
C3400 1UF/6.3V,X5R C0402_BGA
C3401 1UF/6.3V,X5R C0402_BGA
C3402 0.1UF/10V,X5R C0402_BGA
C3403 10uF/6.3V,X5R c0805 ns

0.9-1.1V @2A (DDR3) ??(GDDR5)
Warning:Select the correct Bead to support expected VDDCI current. See databook for details.

CRB MVDDQ:
1uF*2
0.1uF*3
4.7uF*1 or 10uF*1

+VDDC
NC 10uF C3398 C3399 C3403
目前擺放位置不起作用，拿掉实测3D OK lihong 0722

+1_8VRUN
(1.8V@17mA VDD_CT)
VDDC_CT
B12 120ohm/100MHZ i0402
C3358 10uF/6.3V,X5R c0603
C3359 1UF/6.3V,X5R C0402_BGA
C3360 1UF/6.3V,X5R C0402_BGA
C3361 0.1UF/10V,X5R C0402_BGA
C3362 1UF/6.3V,X5R C0402_BGA

+3VRUN
C3373 10uF/6.3V,X5R c0603
C3374 1UF/6.3V,X5R C0402_BGA
C3375 1UF/6.3V,X5R C0402_BGA
C3376 0.1UF/10V,X5R C0402_BGA

VDDR4 VDDR5

VDDR4 del 10uF C3383
lihong 0719

B13 120ohm/100MHZ i0402
C3384 1UF/6.3V,X5R C0402_BGA
C3385 0.1UF/10V,X5R C0402_BGA

For M9X-S3/ Park-S3: REMOVE R6274, R6402,R6284 and INSTALL R8210

B14 120ohm/100MHZ i0402
C3392 10uF/6.3V,X5R c0603
C3393 1UF/6.3V,X5R C0402_BGA
C3394 0.1UF/10V,X5R C0402_BGA

(1.8V@40mA PCIE_PVDD)
B15 120ohm/100MHZ i0402
C3395 10uF/6.3V,X5R c0603
C3396 1UF/6.3V,X5R C0402_BGA
C3397 0.1UF/10V,X5R C0402_BGA

SPV10
C3404 10uF/6.3V,X5R c0603
C3405 1UF/6.3V,X5R C0402_BGA
C3406 0.1UF/10V,X5R C0402_BGA

+1_05VRUN B17 120ohm/100MHZ i0402 SPV10
1.0V @100mA

NS5 NS_VIA NET_SHORT SPVSS

For Park-S3: Connect 1.1V_1.0V_PWR to SPV10 ONLY
For M9X-S2/S3: Connect VDDC to SPV18 ONLY

+VDDC R5436 0 J r0402 +BBP
C3407 1UF/6.3V,X5R C0402_BGA
C3408 0.1UF/10V,X5R C0402_BGA

For PARK-S3:BAckBias(BBP#1 and #2) is not supported, Connect to VDDC Rail

(DNI For M9X-S2/S3)
(For PARK-S3)

(1.8V@90mA SPV18)
B18 120ohm/100MHZ i0402
C3409 1UF/6.3V,X5R C0402_BGA
C3410 0.1UF/10V,X5R C0402_BGA
SPV18

(1.8V@75mA MPV18)
B19 120ohm/100MHZ,500mA i0603
C3411 1UF/6.3V,X5R C0402_BGA
C3412 0.1UF/10V,X5R C0402_BGA
MPV18

BIF_VDDC: separate core power for PCIe bus logic
In BACO mode, BIF_VDDC =PCIE_VDDC (1.0V).
Designs that do not support the BACO option must connect the BIF_VDDC to VDDC.
2011.03.04

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Notebook R&D Division

Title	Robson_XT(Power_and_NC)	
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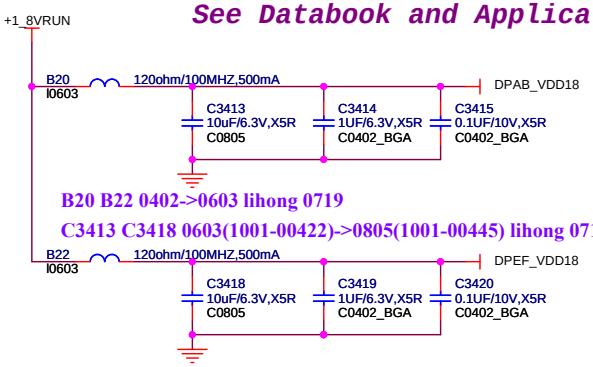
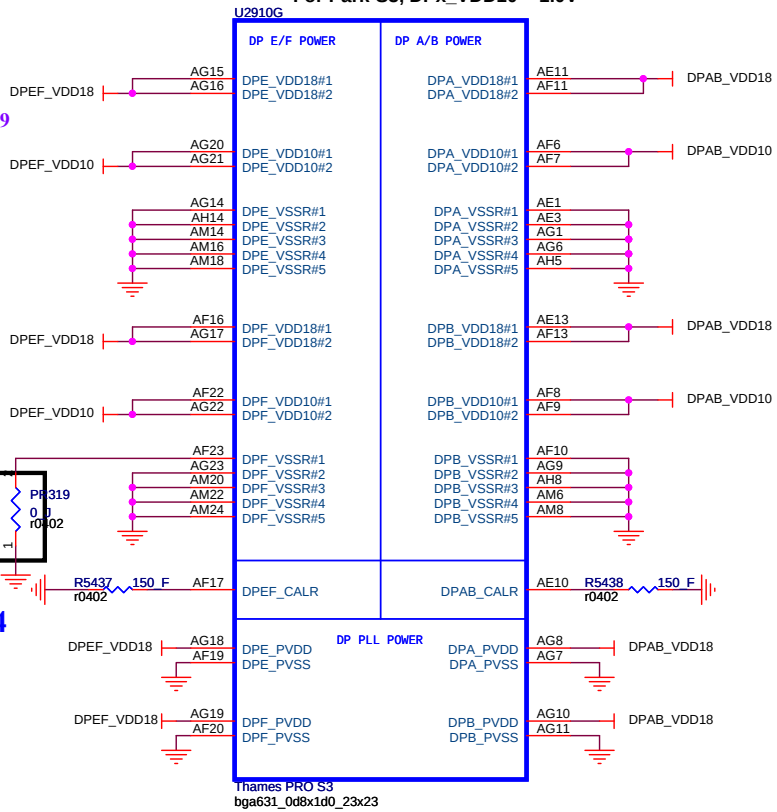
+1_05VRUN 4,5,7,11,13,17,18,26,40,42,44,48,49,51
+1_8VRUN 8,16,17,40,43,44,47,49,51

See Databook and Application note table for Voltage and Current requirements for each individual rail.



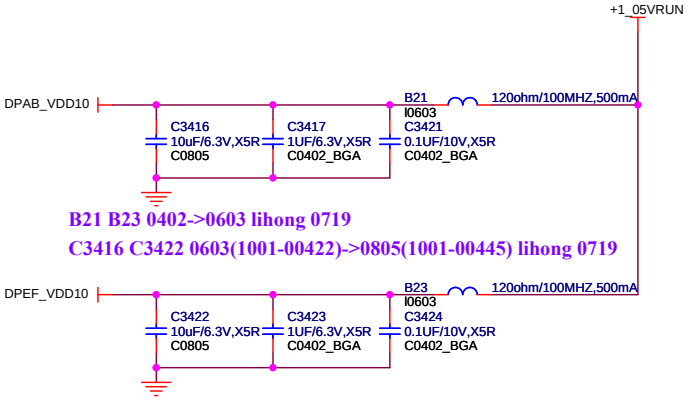
For M9X-S2/S3 , DPx_VDD10 = 1.1V
For Park-S3, DPx_VDD10 = 1.0V

COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED



Add these BOM Options for solder down Motherboard design to support Future GPU Multi Level Pin Straps feature

2011.03.14



del 0603 FB B25 B28
0402 FB B27 B29
10uF C3428 C3434 C3437 C3440
1uF C3429 C3435 C3438 C3441
0.1uF C3430 C3436 C3439 C3442
lihong 0719

del 0402 FB B24 B26
10uF C3425 C3431
1uF C3426 C3432
0.1uF C3427 C3433
lihong 0719

NOTE:1: DPx_VDD18 and DPx_PVDD Rails can be join together and remove Decoupling Capacitors and BEAD for DPx_PVDD if signal integrity for DP lanes are OK.

NOTE:2: DPA_VDD10 / DPB_VDD10 and DPE_VDD10 / DPF_VDD10 Rails can be join together and remove Decoupling Capacitors and BEAD for one rail of each pair if signal integrity for DP lanes are OK. We also need to Change BEAD to minimum 400mA rating.

NOTE:3: DPx_VDD18 Rails can be join together as shown in schematic for Dual -Link DVI or LVDS setting and remove Decoupling Capacitors and BEAD of any one rail of the pair if signal integrity for DP lanes are OK. We need atleast 500mA Bead to support join rails.

NOTE:4: Do not Install for M9X-S2/S3. INSTALL ONLY for PARK-S3. Other Notes can be apply as well.

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	Robson_XT(DP Power)	
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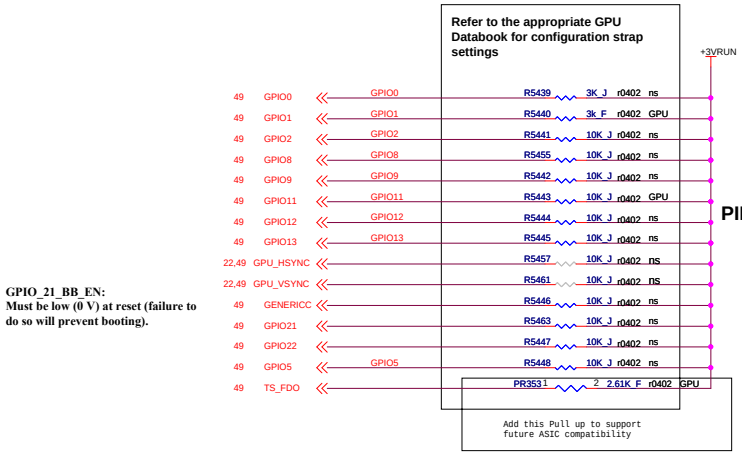
+3VRUN 5,11,12,13,14,15,16,17,18,20,22,23,25,26,27,30,31,32,34,35,36,39,40,41,42,43,44,47,48,49,51



PIN STRAPS

GPIO_21_BB_EN:
Must be low (0 V) at reset (failure to do so will prevent booting).

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

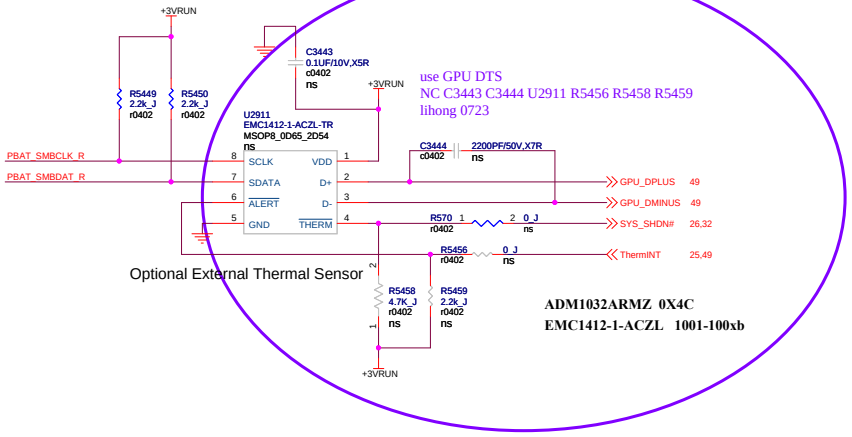
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD	GPIO8		0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD	H2SYNC		
RSVD	GENERICC		0
AUD[1]	HSYNC	AUD[1] AUD[0]	0
AUD[0]	VSYNC	0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	X X
RSVD	GENERICC		0

AMD RESERVED CONFIGURATION STRAPS

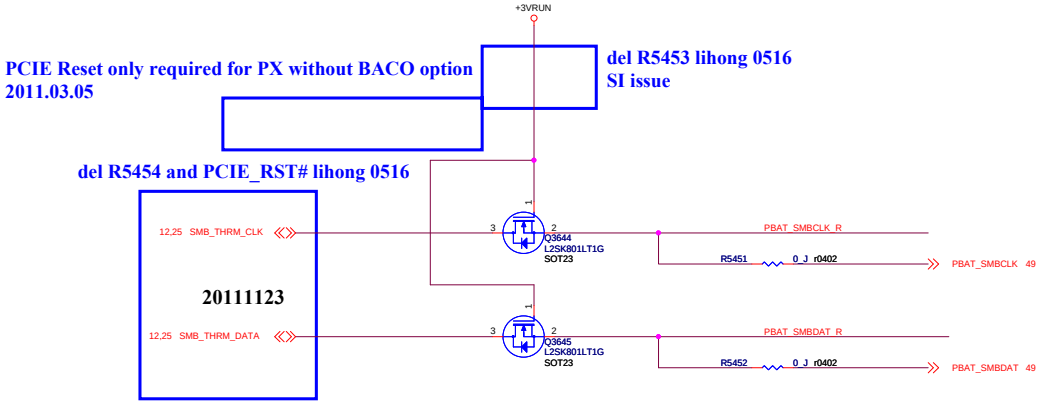
Provide pull-up pads for these straps - but do not populate. GPIOs functions on these signals must not conflict with the pin strap at Reset

H2SYNC	GENERICC	GPIO21	GPIO2	GPIO8



Optional External Thermal Sensor

ADM1032ARMZ 0X4C
EMC1412-1-ACZL 1001-100xb



BITLAND Bitland Information Technology Co.,Ltd.
Notebook R&D Division

Title: Robson_XT(Straps & Thermal)

Size	Document Number	Rev
C	N480	1.2

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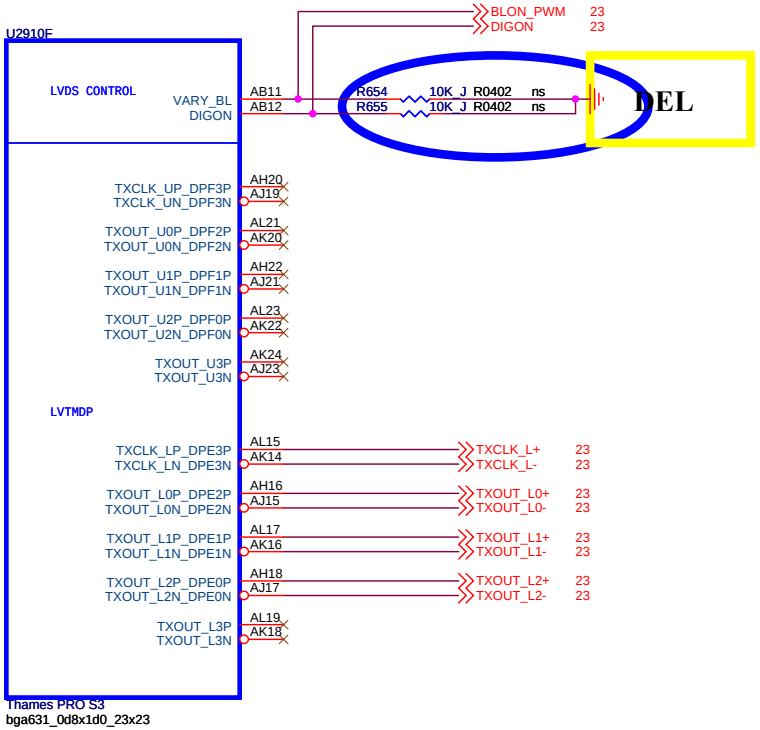
LVDS Interface



BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	Robson_XT(DPEF_ LVDS)	
Size B	Document Number N480	Rev 1.2
Date: Wednesday, September 12, 2012	Sheet 54 of 64	

DDR3 Memory Interface

MVDDQ = 1.5V FOR DDR3 Memory

PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

For M9X-S2/S3

DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Ra)	100R	40.2R
MVREF TO GND (Rb)	100R	100R

For Park-S3

DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R

follow FAE suggest lihong 0514

Note 1 : Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.
Note 2 :For M9X-S2/S3,J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
For Park-S3,J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR
Note 3 :For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected.
For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24

route 50ohms single-ended/100ohms diff and keep short

Use this option ONLY for Park-S3

Differential for testing and DNI component for normal operation.

PX_EN: PowerXpress Enable
3.3V turn the regulators to the dGPU core OFF (enter BACO mode).
0V turn the regulators ON.
PX_EN outputs low (0V) by default.
If this signal is unused, it should be left not connected on the PCB.
2011.03.04

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Title	Robson_XT(MEM Interface)	
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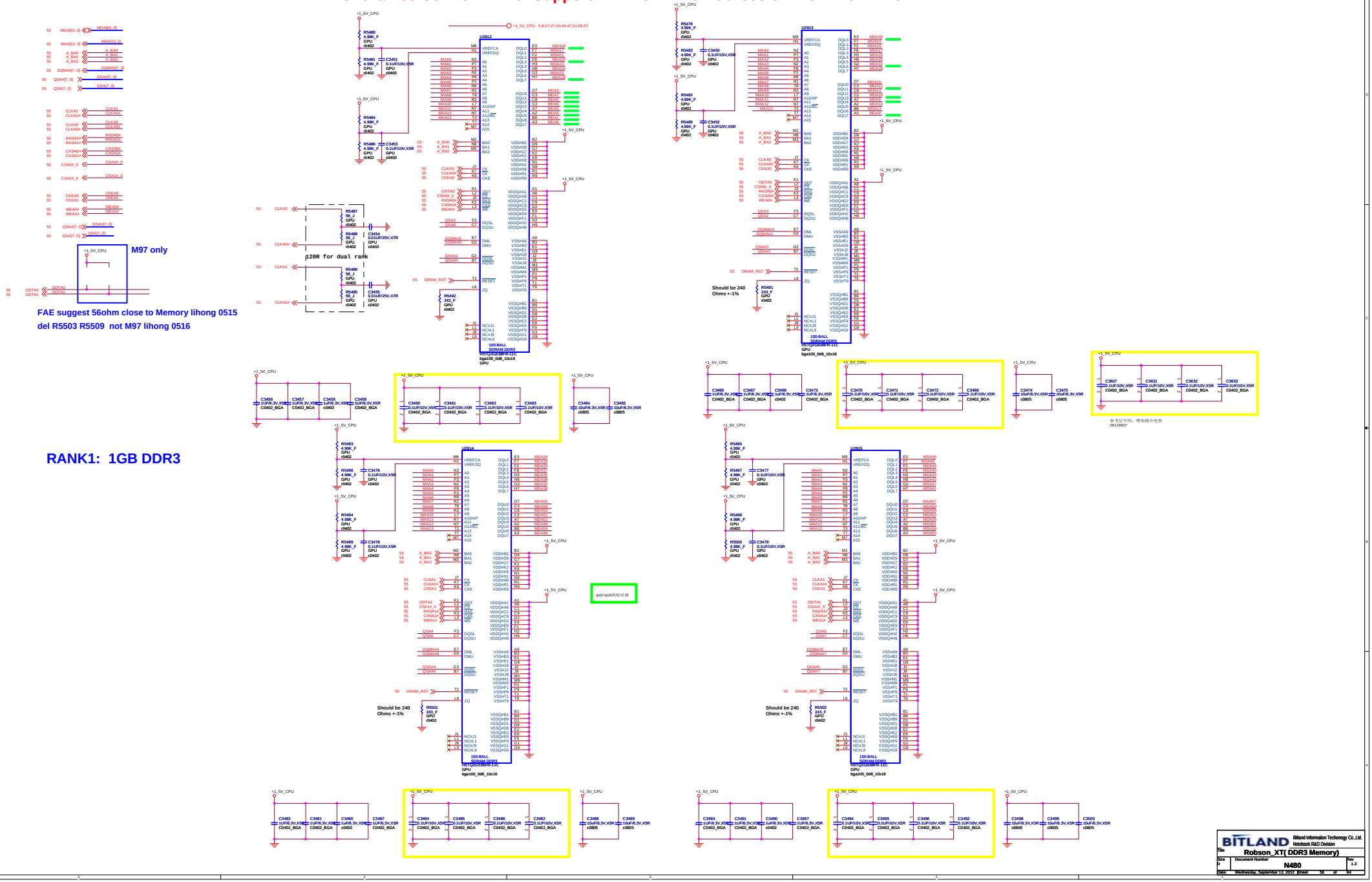
For thames-S3 with DDR3: Support MAA13-MAA0 Address or 128KX16 DDR3.



COMPONENTS SHOWN ARE EXAMPLES ONLY - AND NOT NECESSARILY QUALIFIED.

For M9X-S2/S3 with DDR3: Support MAA12-MAA0 Address or 64KX16 DDR3. MAA13 is NC

BITLAND	Bitland Information Technogy Co.,Ltd. Notebook R&D Division		
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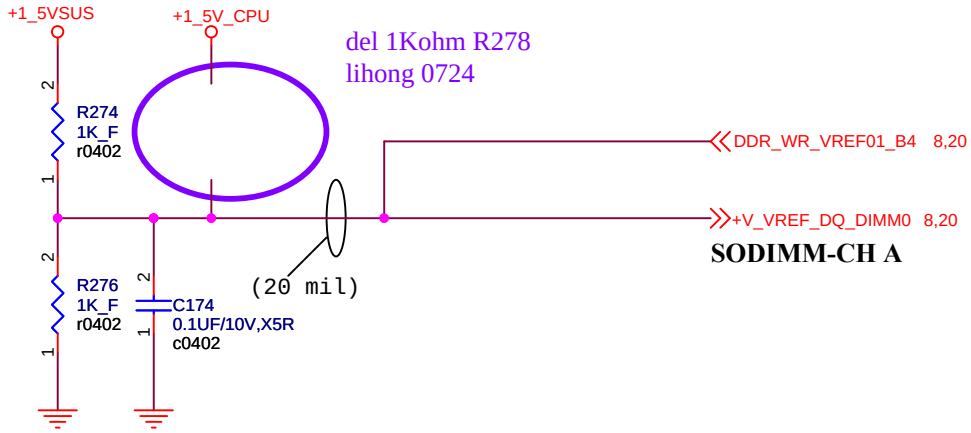
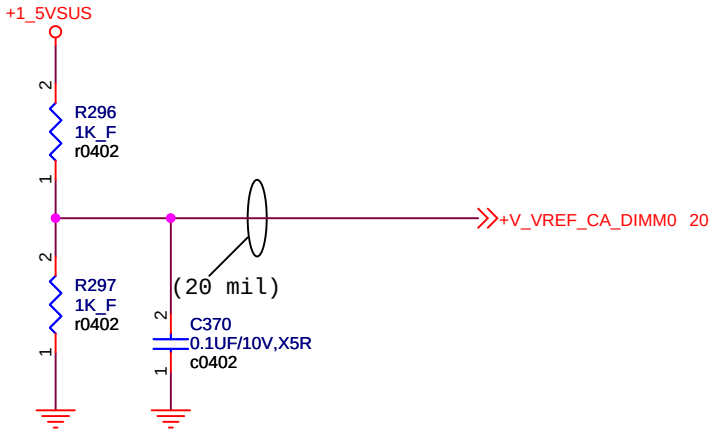
VREF circuitry - M1 (Voltage Divider Network) & M3 (Driven By Processor) implementation

M3+M1: Default Recommendation
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off state
M3: VREF_DQ driven by Processor

+1_5V_CPU 5,8,17,27,43,44,47,51,55,56
+1_5VSUS 5,8,20,39,43





SODIMM-CH B

删除R289 R291及预留的R287 lihong 0516
no DDR_WR_VREF01_D1

CAD NOTE:All VREF traces should be at least 20 mils wide and 20 mils spacing to other signals/planes

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	VREF circuitry - M1&M3	
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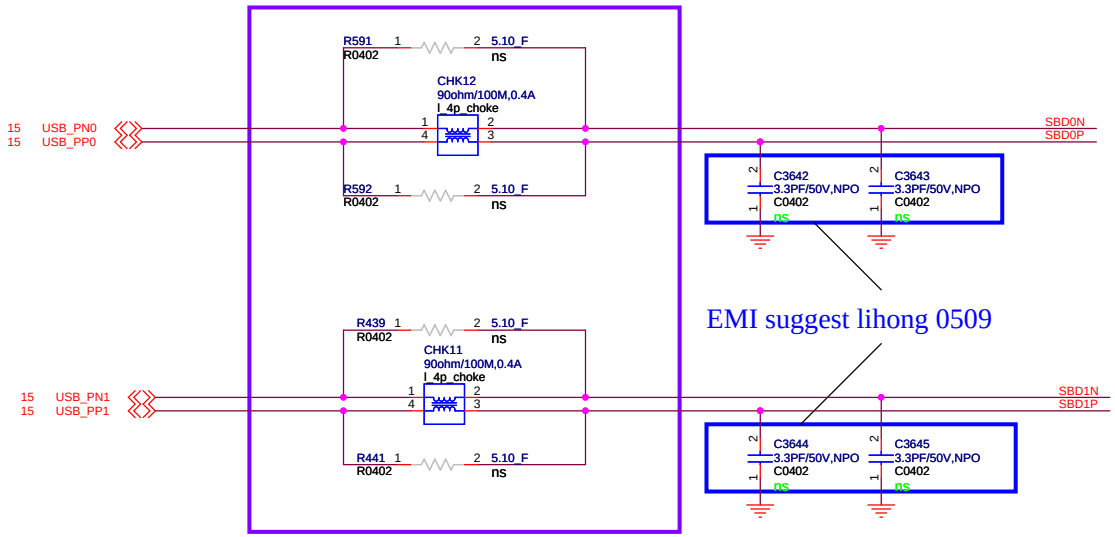
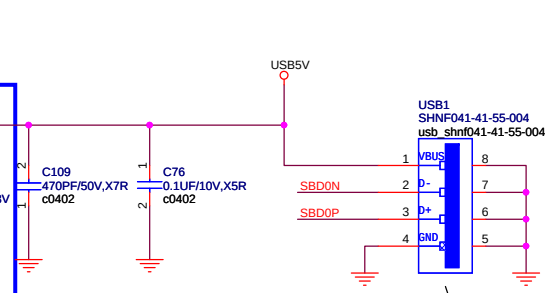
R591 R592 R439 R441 Stuff->NC
CHK12 CHK11 NC->Stuff lihong 0618

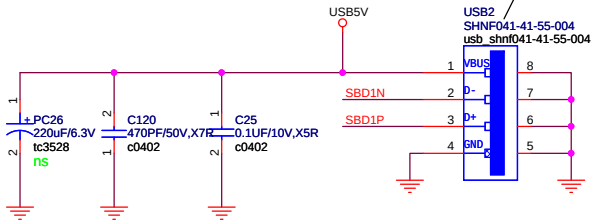


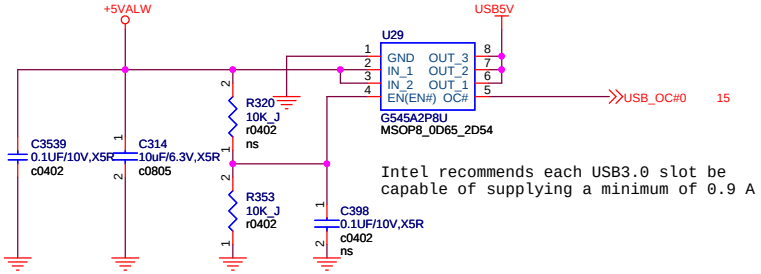
EMI suggest lihong 0509



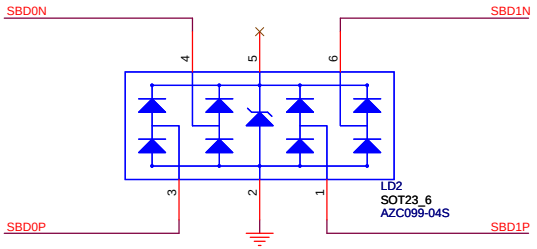
colay in bottom side and place between USB1 and USB2 lihong 0509

USB2.0换为康祥的料 lihong 0514





Intel recommends each USB3.0 slot be capable of supplying a minimum of 0.9 A



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Title	USB2.0	
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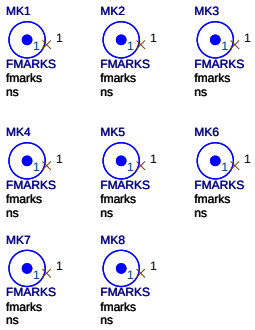

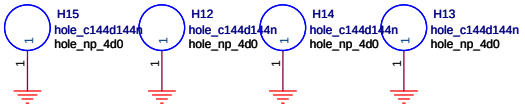

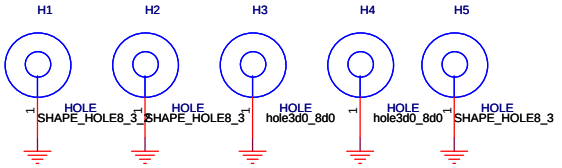

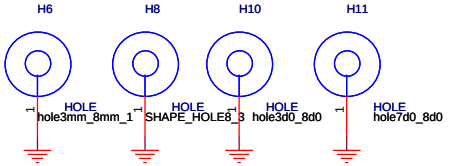

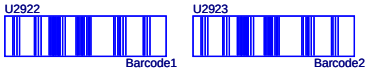

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Title	HOLE&BOSS	
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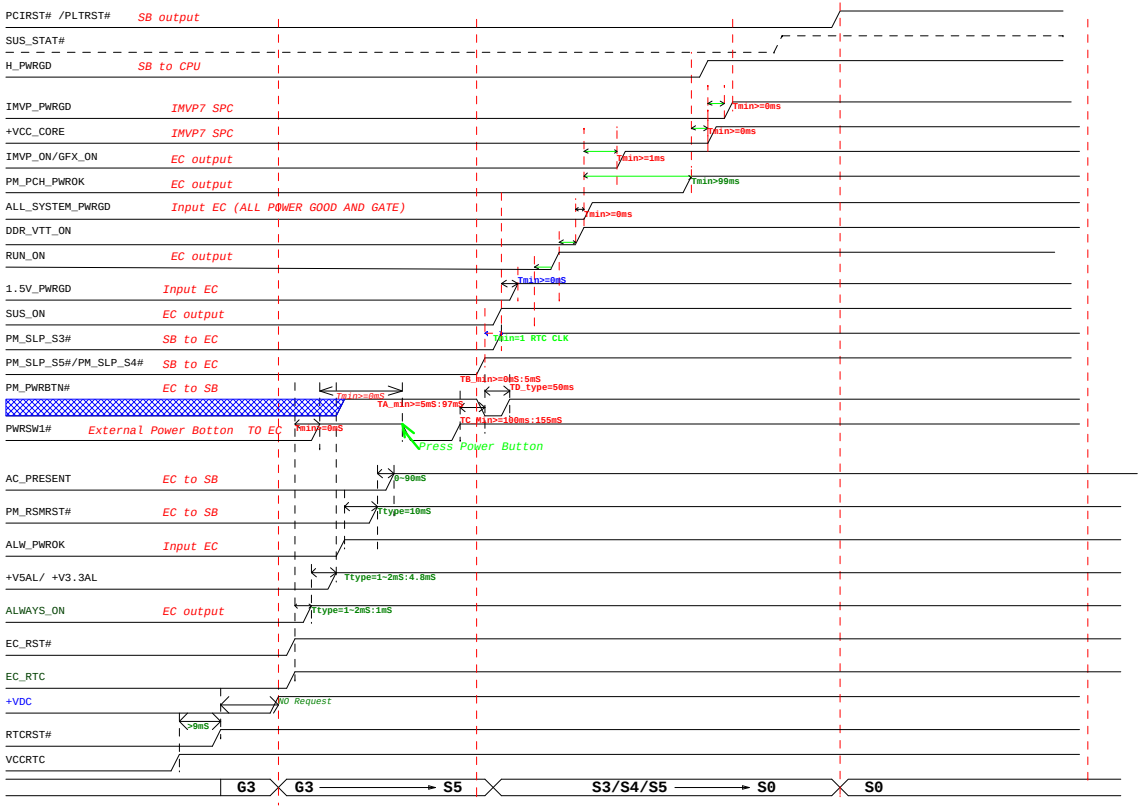
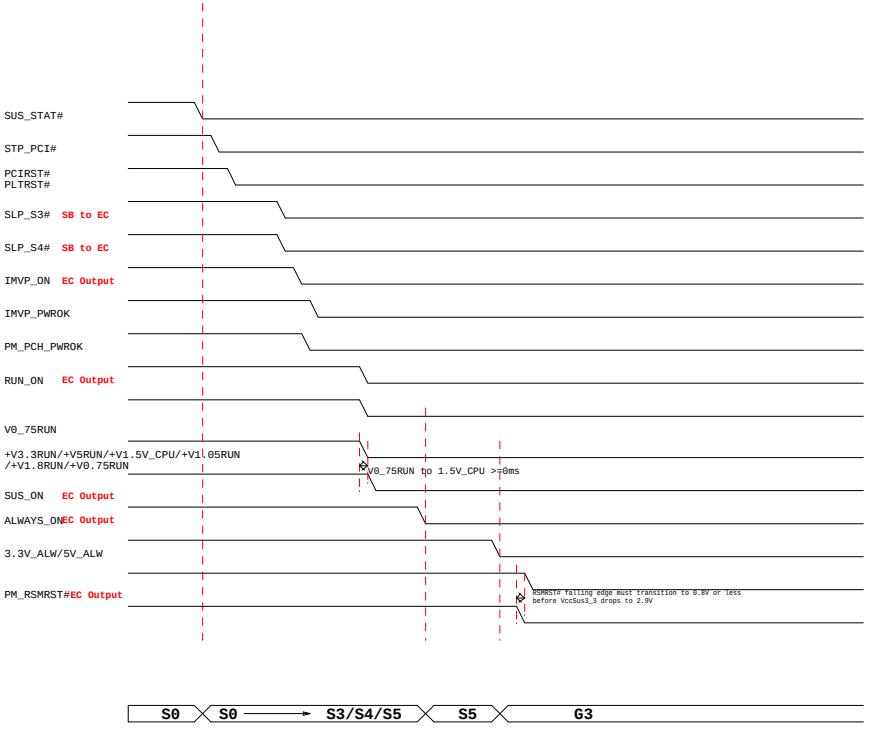
BM5238 Power On/Off Sequence Specification(Adapter Mode) G3-S5-S4-S3-S0





条纹填充区域表示在这段时间任意一个时间点达到要求电平都OK

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division		
Title	PowerOn/Off Seq. AC		
Size: Custom	Document Number: N480		Rev: 1.2
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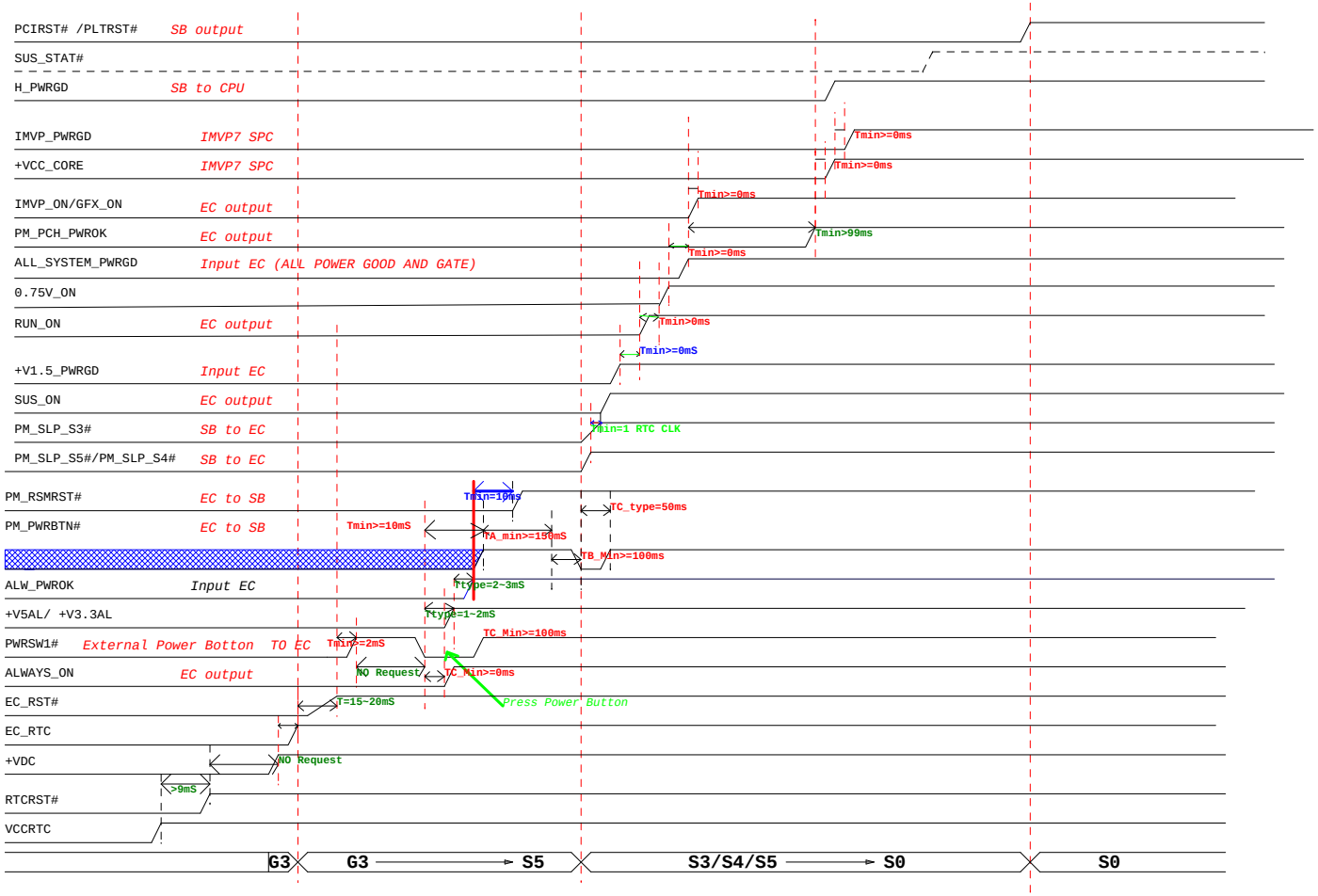
BM5238 Power On/Off Sequence Specification(Battery Mode) G3-S5-S4-S3-S0



条纹填充区域表示在这段时间任意一个时间点达到要求电平都OK

BITLAND Bitland Information Techonogy Co.,Ltd. Notebook R&D Division		
Title: PowerOn/Off Seq. DC		
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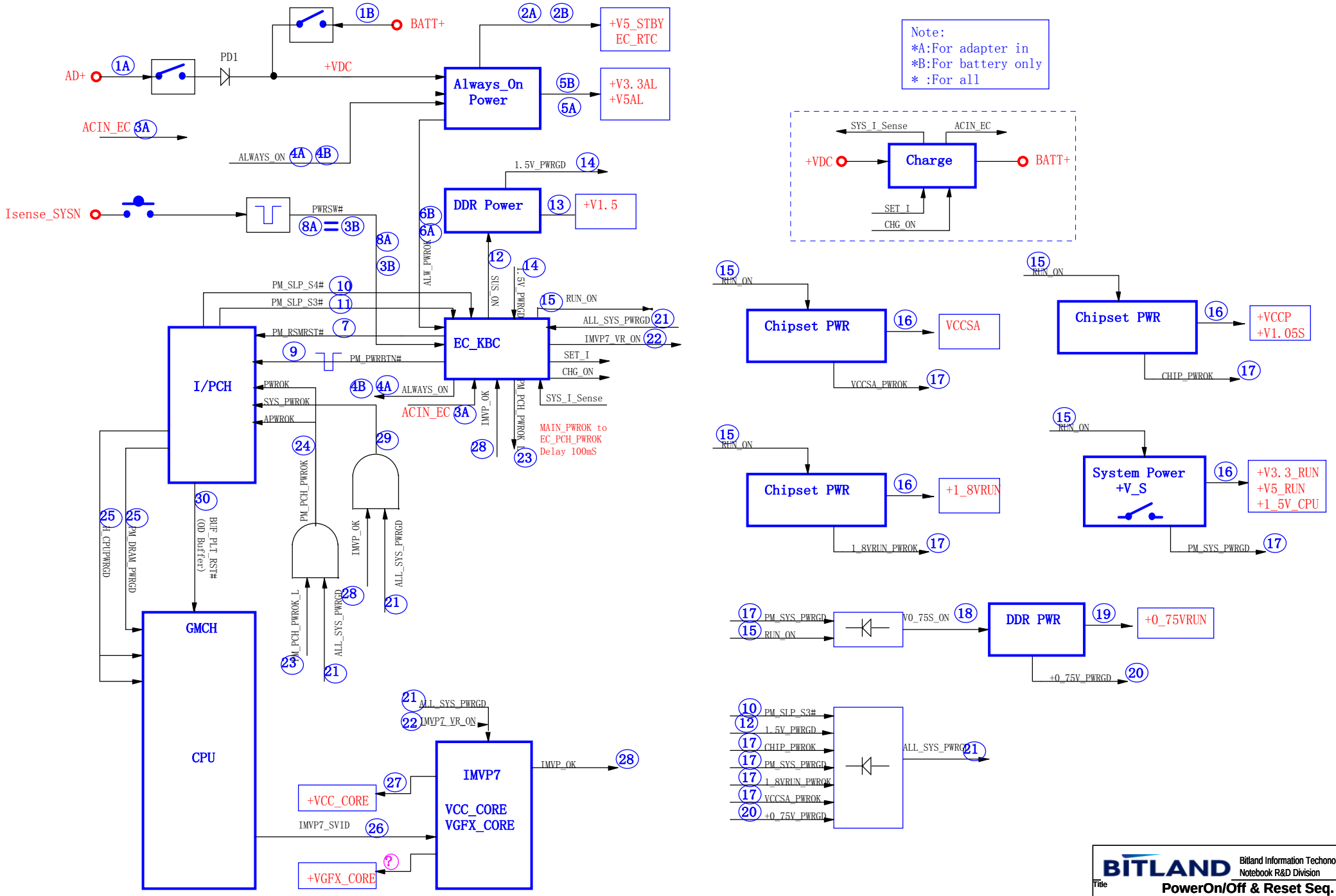
DS4/5 Disable



Title	PowerOn/Off & Reset Seq.	
Size A3	Document Number N480	Rev 1.2
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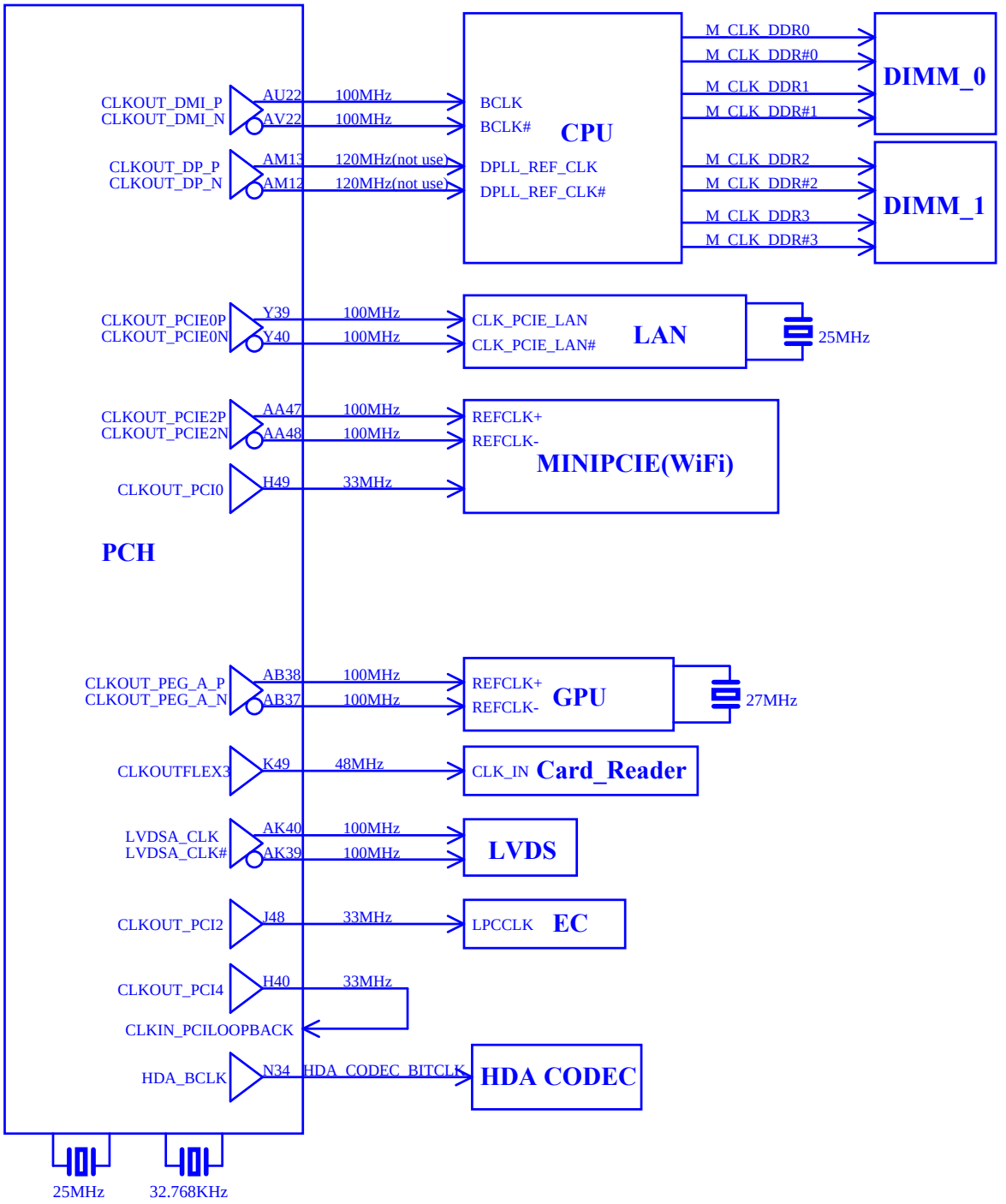

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Title: Clock diagram

Size	Document Number	Rev
A2	N480	1.2

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History

Version	History	Date
V1.0	Initial release	20120519
V1.1	1) WIFI change from PCIE Port1 to Port2 2) VCORE improve PR178 17.4K->22K pc136 PC144 0.047uF->0.068uF r571 1K->2K R601 5.49K->2.74K 3) Modify power sequence PR150 51K->33K R1822 84.5K->47K PR30 100K->71K 4) change some components footprint 5) PEG capacitor 0.22uF->0.1uF, 0.1uF/25V,X5R->0.1uF/50V,X7R	
V1.2	1) Remove Jumpers 2) add C331，left Pin13 of CN12 no connect 3) add GPU CTF function	

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Title: History		
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