

PCB STACK UP

LAYER 1 : TOP
 LAYER 2 : GND
 LAYER 3 : IN1
 LAYER 4 : GND
 LAYER 5 : SVCC
 LAYER 6 : IN2
 LAYER 7 : GND
 LAYER 8 : BOT

BLOCK DIAGRAM

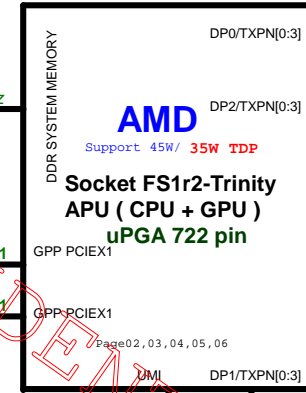
FAN /THERMAL
 EMC2103-2
 Page32

Note :DP means Display Port Interface

Note :DDR3-1.35V support 1066-1333 MHz
 DDR3-1.5V support 1066-1600 MHz

DDR III
 SO-DIMM 0
 SO-DIMM 1
 Memory size MAX is 16GB per channel
 Page12, 13

Dual Channel
 1333/1600 MHz



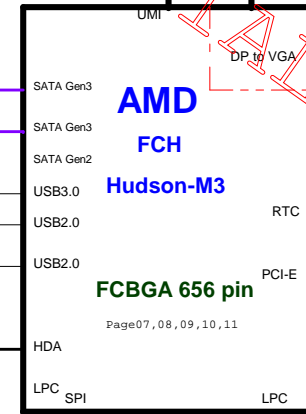
ANX3111
 Page25
 DP to LVDS

LVDS
 Page26

HDMI
 Page23

Seymour XT
 Page14~Page22

VGA
 Page24



HDD (SATA)
 Page29
 SATA0 6Gbit/s

ODD (SATA)
 Page29
 SATA1 6Gbit/s

USB3.0/USB2.0 COMBO
 Page31
 USB 3.0
 USB 2.0

USB 2.0 X2
 Page31, 34
 USB 2.0

Bluetooth
 Page33
 USB 2.0

CCD
 Page33
 USB 2.0

Card Reader
 RTS5131-GR
 Page34
 USB 2.0

Audio CODEC
 ALC269Q-VC2-GR
 Page28
 Azalia (HDA bus)

SPI ROM
 8M
 Page09

(IT8518 HX)
 Page35
 X'TAL 32.768KHz

HP Jack

MIC Jack

SPK
 Page28

DMIC
 Page28

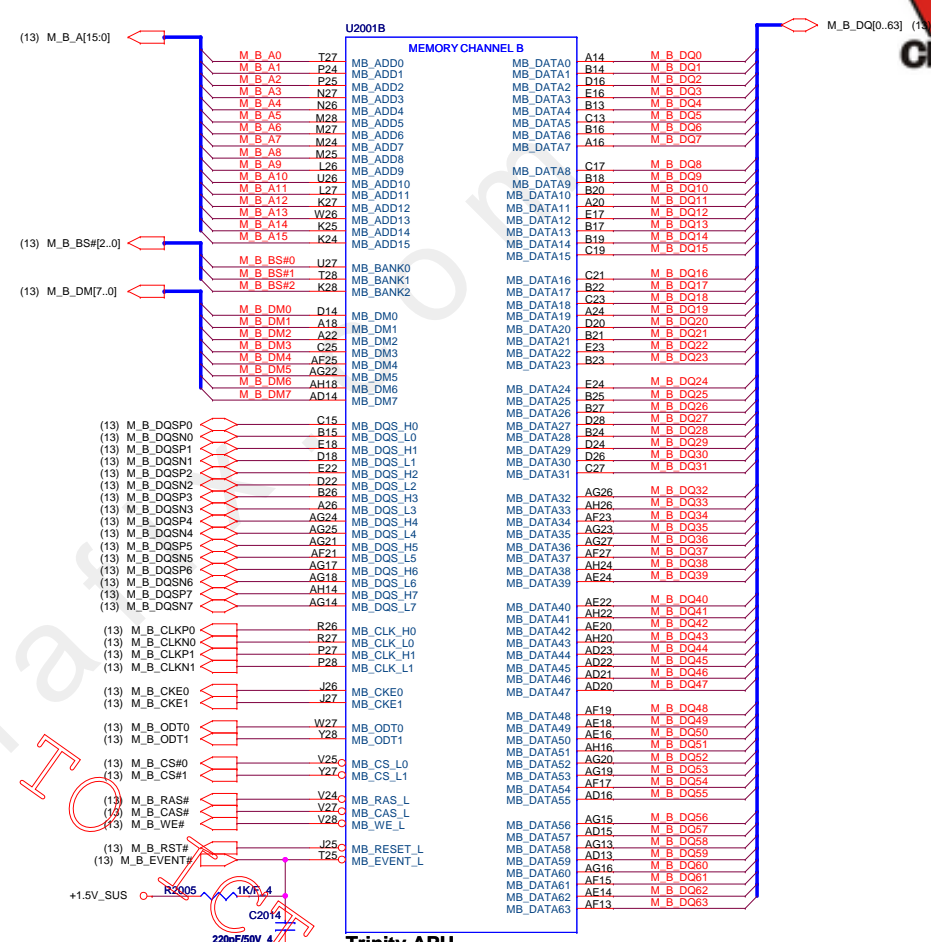
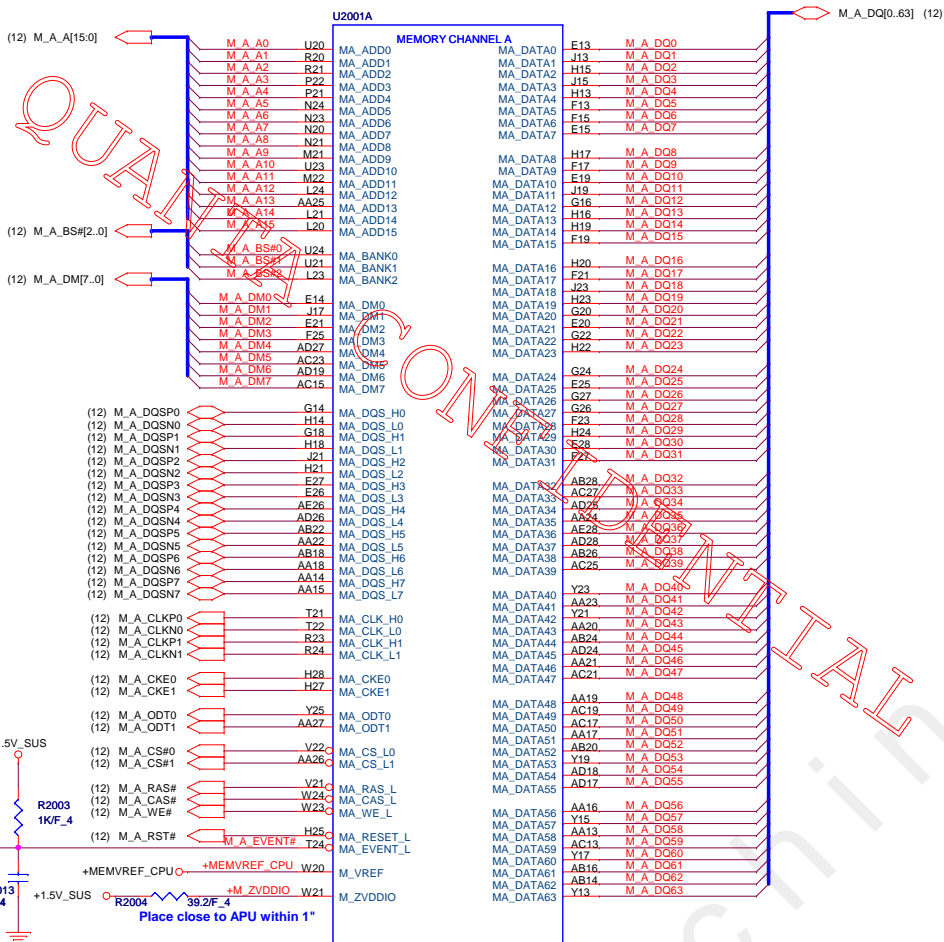
SPI ROM
 Page35

Touch Pad
 Page34

Keyboard
 Page34

Discharge	Page37
Charge (BQ24737)	Page38
DDR3/0.75V (TP581216)	Page40
3V/5V (TP581123AARGER)	Page39
+1.1V_DUAL & 1.1V (TP5811211)	Page41
+1.2V_VDDPR/+2.5 (ISL6277HRT2-T)	Page42
VDD+VDDNB_CORE (ISL6277HRT2-T)	Page43
DGPU (ISL6277HRT2-T)	Page44
1.8V	Page45
GPU	Page46





Trinity APU

Trinity APU

Display port power 1.5V min 1.2v max : 1.65v

U2001C

ANALOG/DISPLAY/MISC

DP0 output to eDP to LVDS converter

DP1 output to Hudson-M3 for VGA translator interface

note --HDMI P&N can not swap
DP1 output to HDMI connector

Note: CLK_APU_HCLKP/N is 100MHZ SSC

Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

EC-A-04

EC-A-03

Trinity APU

Thermal

ThermTRIP# shutdown temperature 125°C

APU_PROCHOT# 可以当 input or output

当Low时CPU会降 P - STATE

to EC reserve only

220pF/50V_4

APU_PROCHOT#_VDDIO

Display port power 1.5V min 1.2v max : 1.65v

LVDS

VGA

HDMI

EC-A-03

EC-A-03

EC-A-03

EC-A-03

FS1R1 signals is for detect CPU TYPE and protect it.
FS1R1 CPU this pin is N.C
FS1R2 CPU this pin is LOW
can remove it at MP

DMAACTIVE_L controls entry and exit from the sleep and power states

SI

EC-A-05

+1.2V_VDDPR

EC-B-03

PROJECT : LZ2C

Quanta Computer Inc.

Size Document Number Rev 2A
Date: Monday, January 08, 2012 Sheet 4 of 51

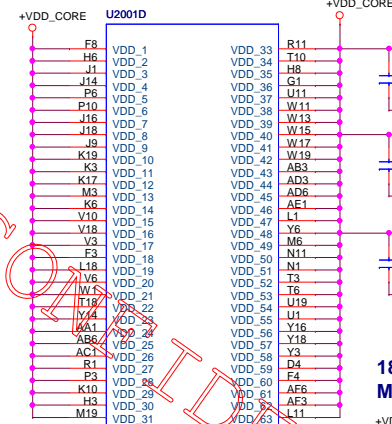
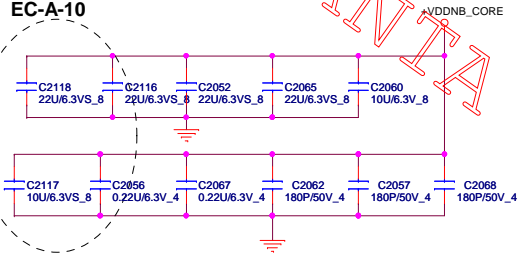
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



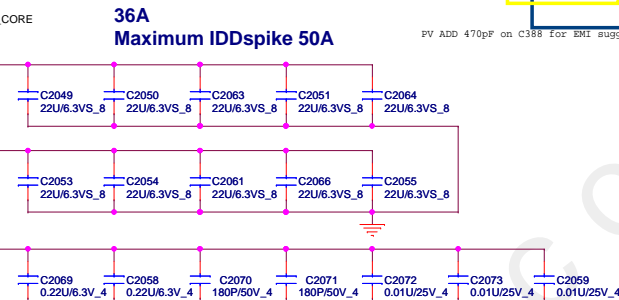
SI EMI



EC-A-10

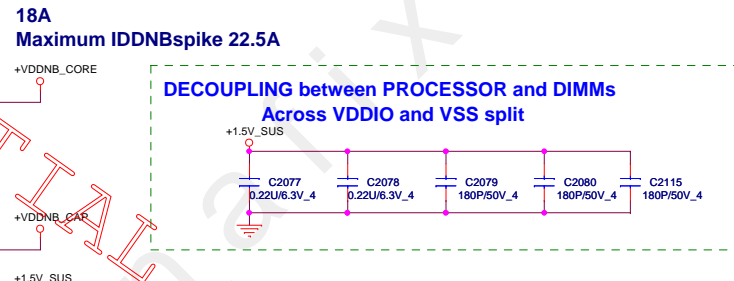


36A
Maximum IDDspike 50A

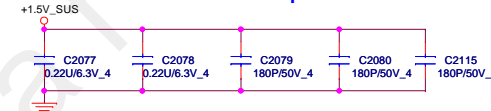


PV ADD 470pF on C388 for EMI suggestion

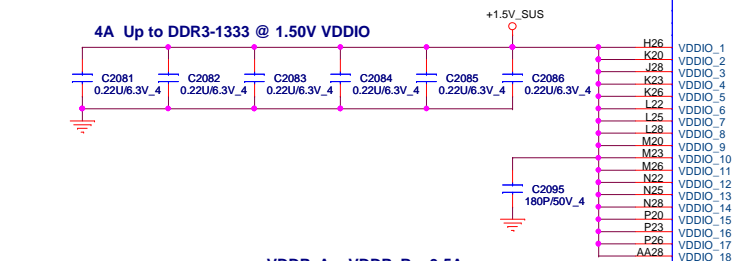
18A
Maximum IDDNBspike 22.5A



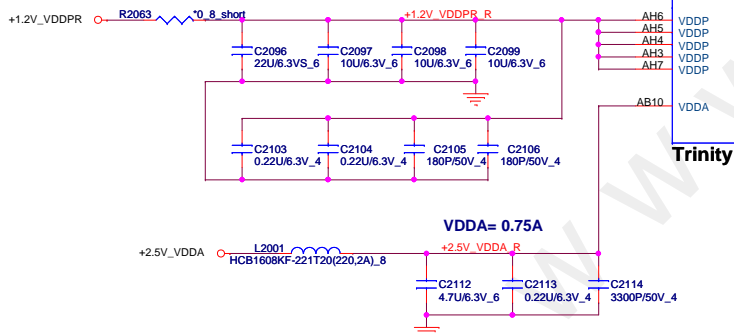
DECOUPLING between PROCESSOR and DIMMs Across VDDIO and VSS split



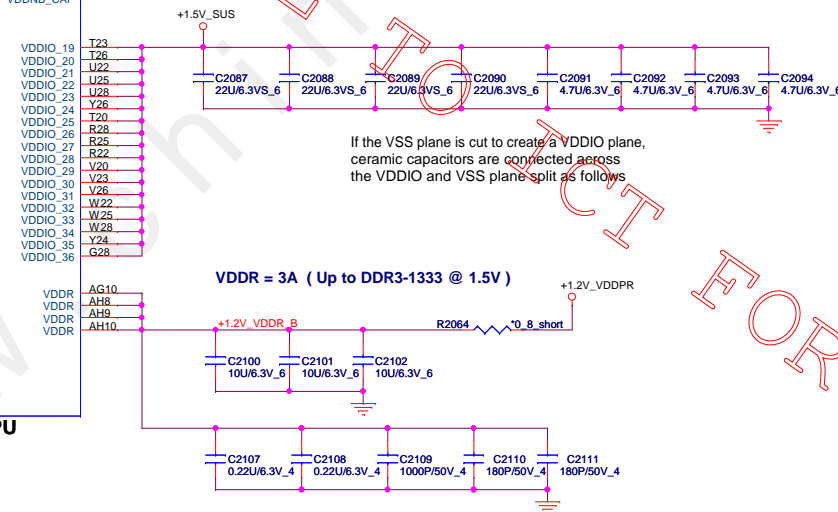
4A Up to DDR3-1333 @ 1.50V VDDIO



VDDP_A + VDDP_B = 3.5A

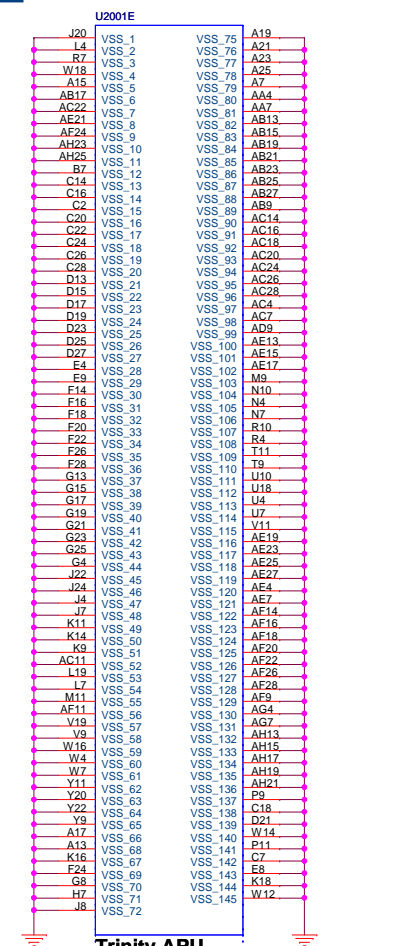
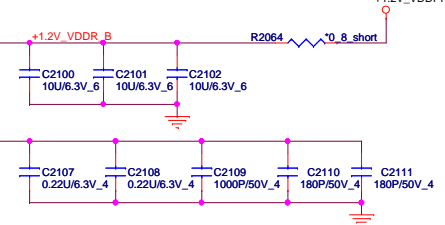


Trinity APU

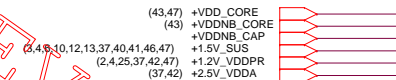


If the VSS plane is cut to create a VDDIO plane ceramic capacitors are connected across the VDDIO and VSS plane split as follows.

VDDR = 3A (Up to DDR3-1333 @ 1.5V)



Trinity APU



PROJECT : LZ2C
Quanta Computer Inc.

Size	Document Number APU 4/5(POWER/GND)	Rev 2A
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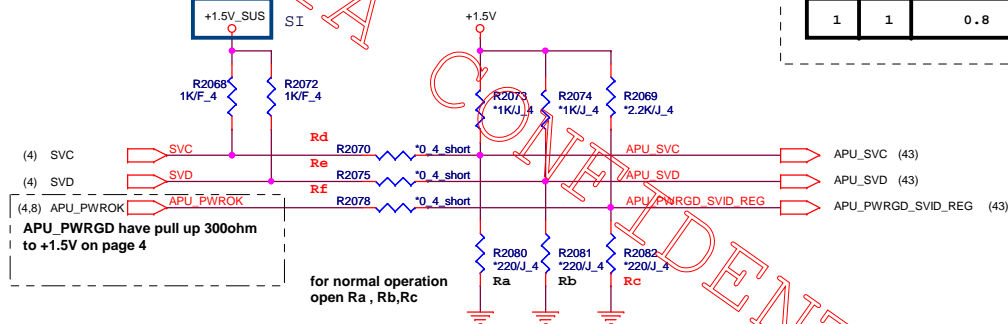
VID Override Circuit

(4,25,30,41,43) +1.5V
(3,4,5,10,12,13,37,40,41,46,47) +1.5V_SUS

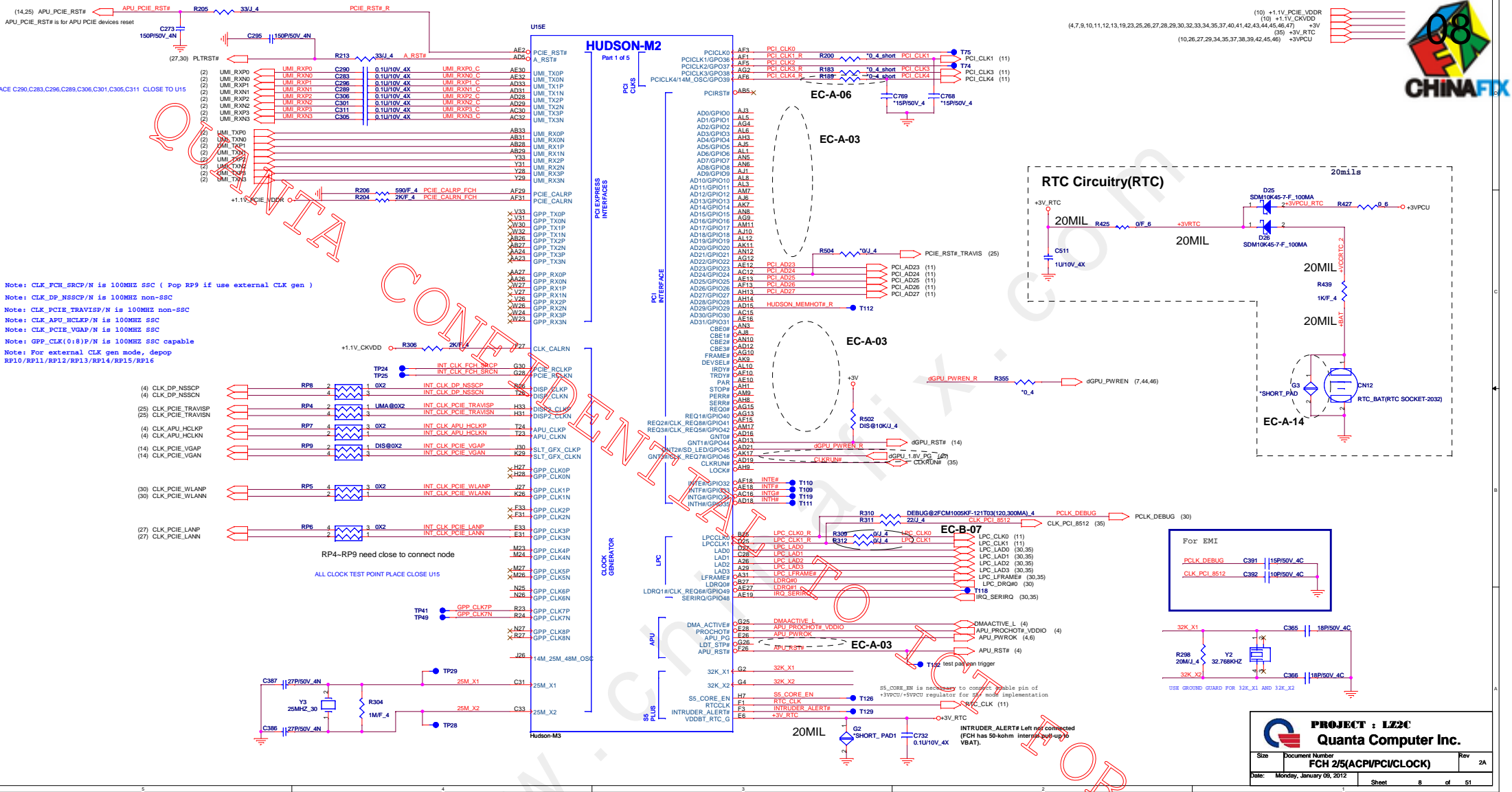
06



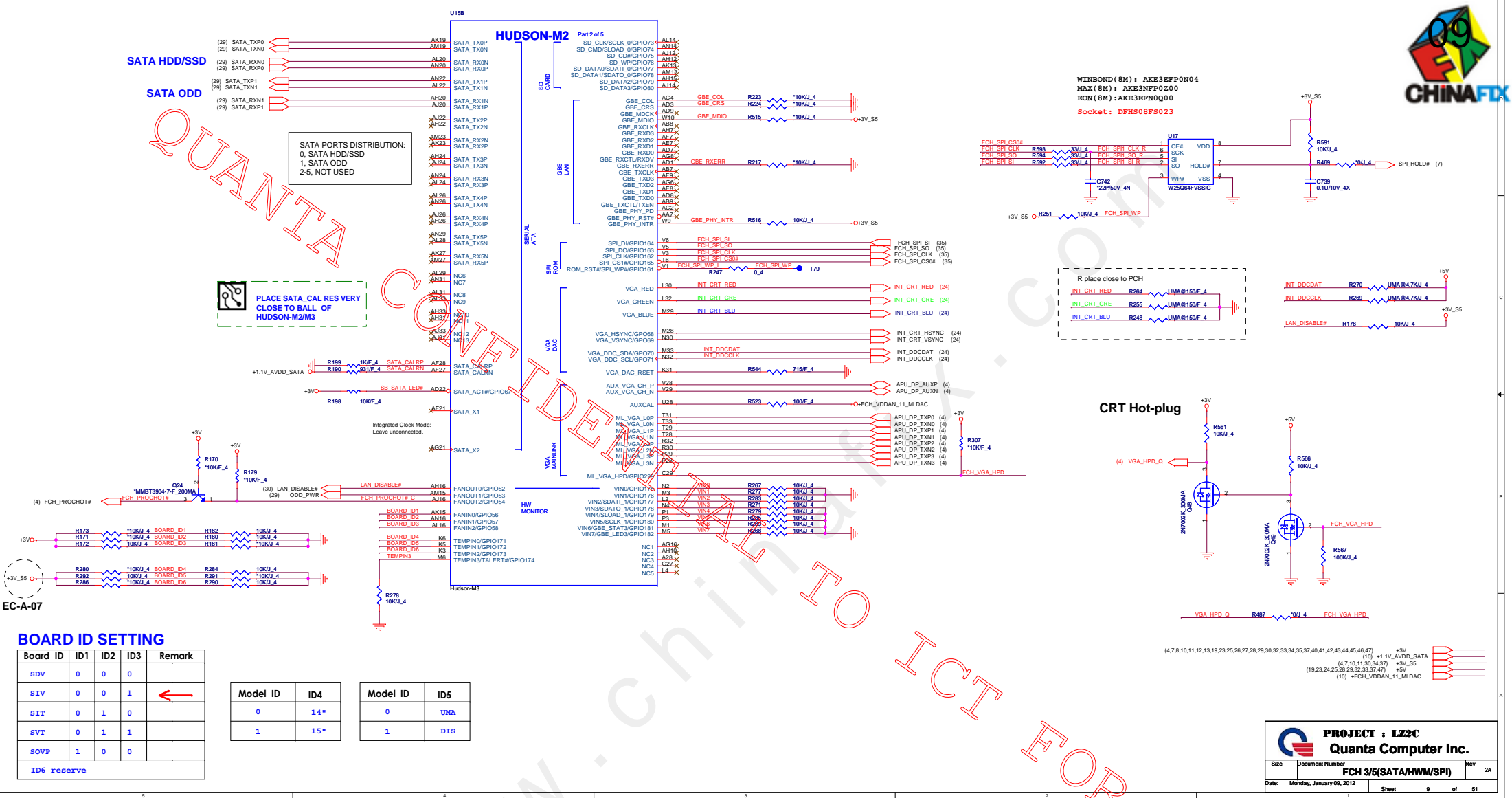
Note:
To override VID, Remove Rd, Re, Rf, install Rc
set VID via SVC & SVD option RES.



BOOT VOLTAGE			
SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8



REVIEW



EC-A-07

BOARD ID SETTING

Board ID	ID1	ID2	ID3	Remark
SDV	0	0	0	
SIV	0	0	1	←
SIT	0	1	0	
SVT	0	1	1	
SOVP	1	0	0	
ID6 reserve				

Model ID	ID4
0	14"
1	15"

Model ID	ID5
0	UMA
1	DIS

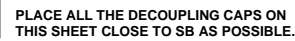
PROJECT : LZ2C

Quanta Computer Inc.

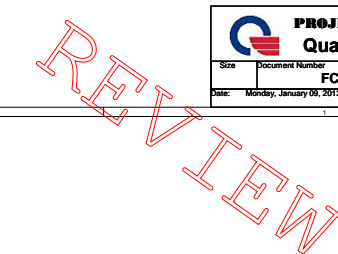
Size	Document Number	Rev
	FCH 3/5(SATA/HWM/SPI)	2A

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REVIEW



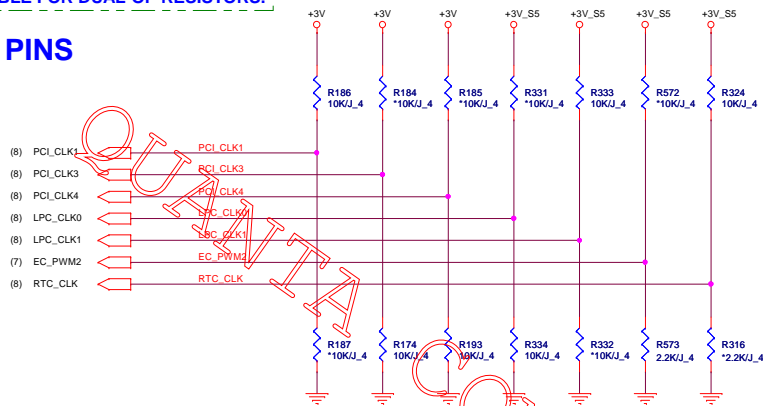
(4,7,8,9,11,12,13,19,23,25,26,27,28,30,32,33,34,35,37,40,41,42,43,44,45,46,47) +3V
(3,4,5,6,12,13,37,40,41,46,47) +1.5V_SUS
(9) +FCH_VDDAN_11_MILDAC
(4,7,9,11,30,34,37) +3V_SS
(37,41) +1.1V_DUAL
(7) +FCH_VDD_11_SSUSBS_S
(41) +1.1V
(8,26,27,29,34,35,37,38,39,42,45,46) +3VPCU





OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS

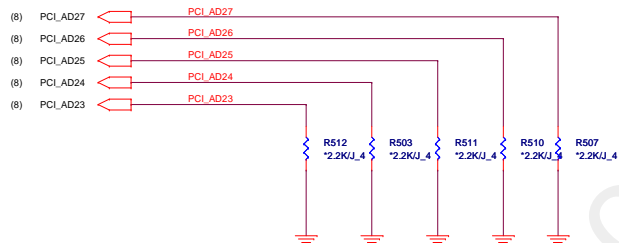


REQUIRED STRAPS

	-----	PCI_CLK1	-----	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	-----	ALLOW PCIE Gen2 DEFAULT	-----	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

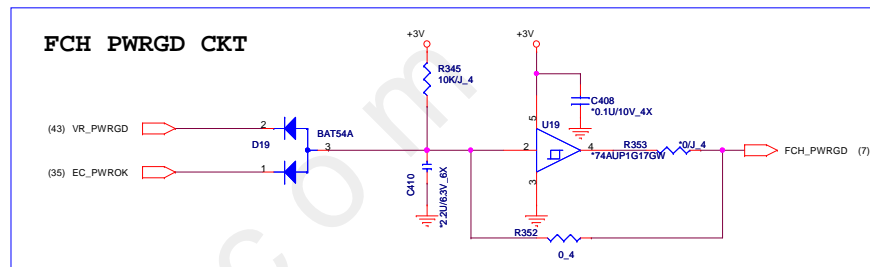
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

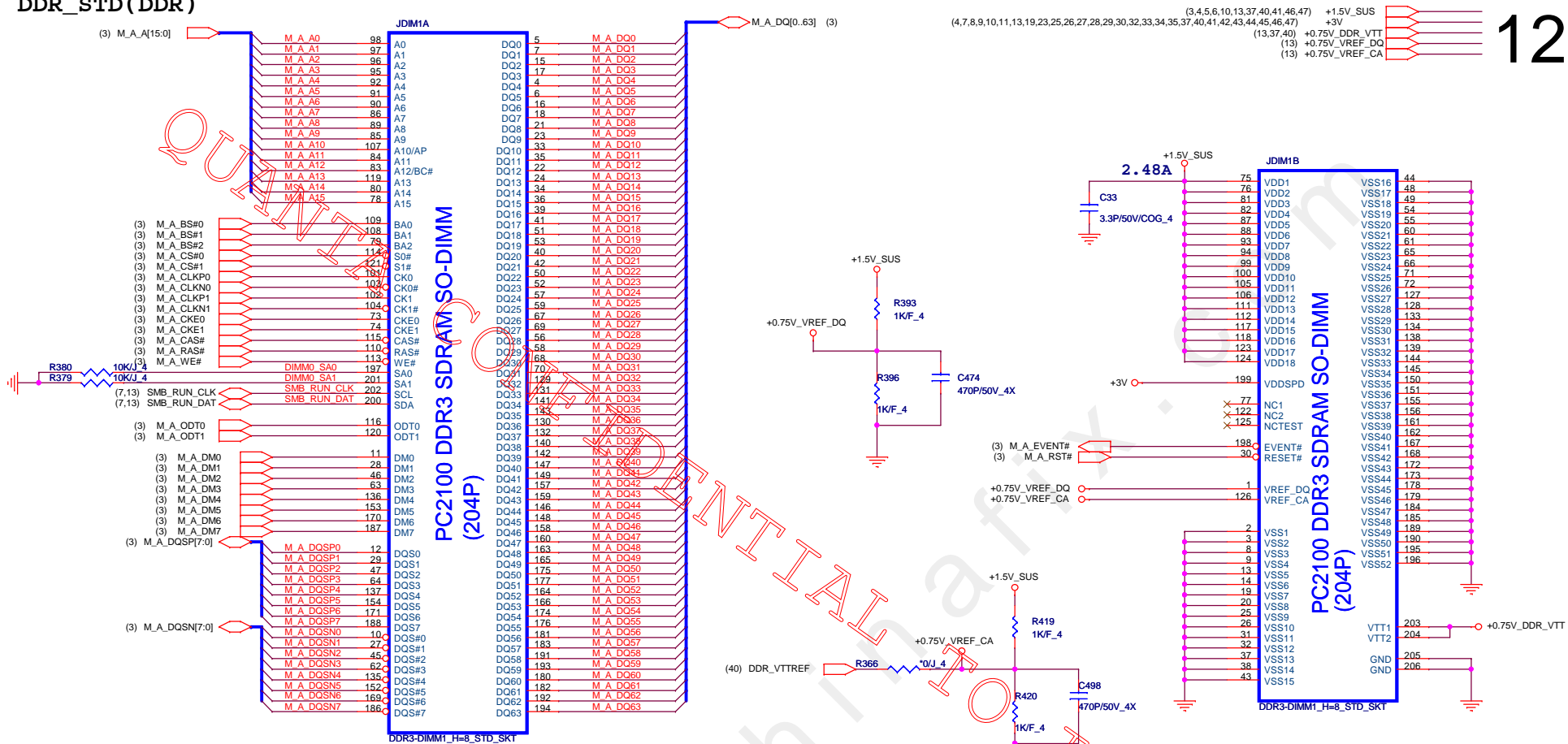


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

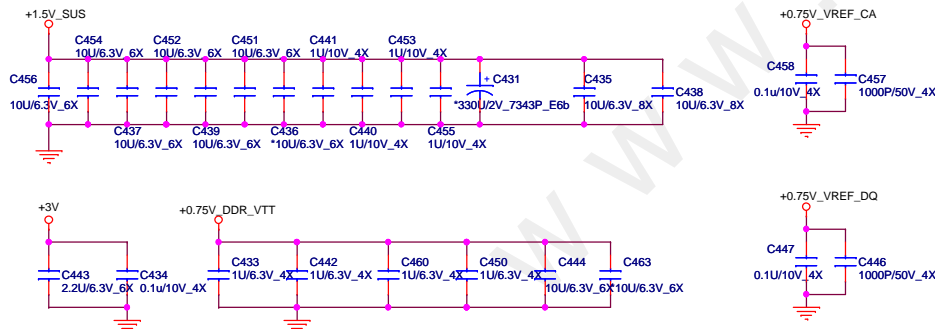
FCH PWRGD CKT



DDR STD (DDR)

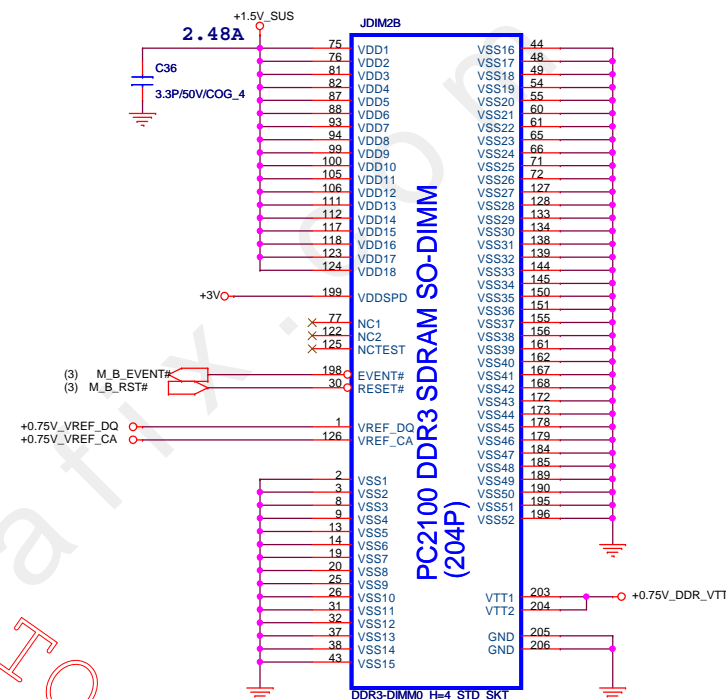
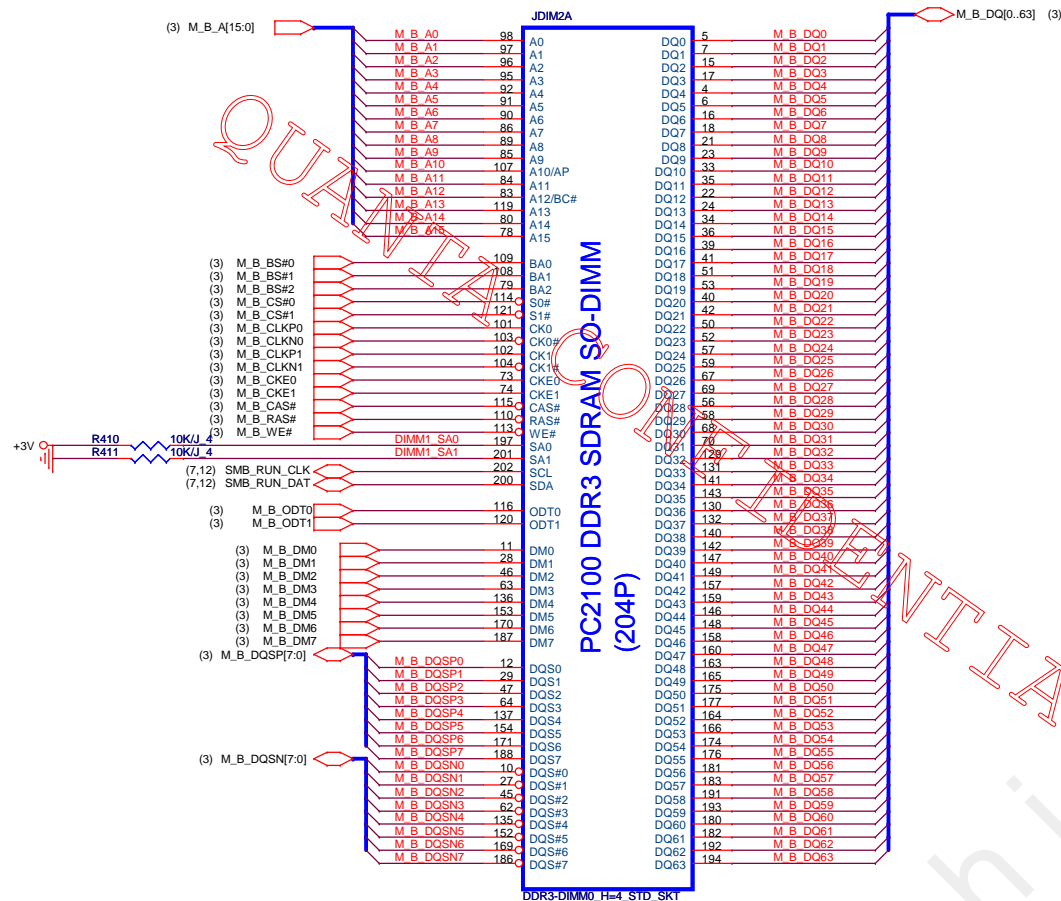


Place these Caps near So-Dimm0.

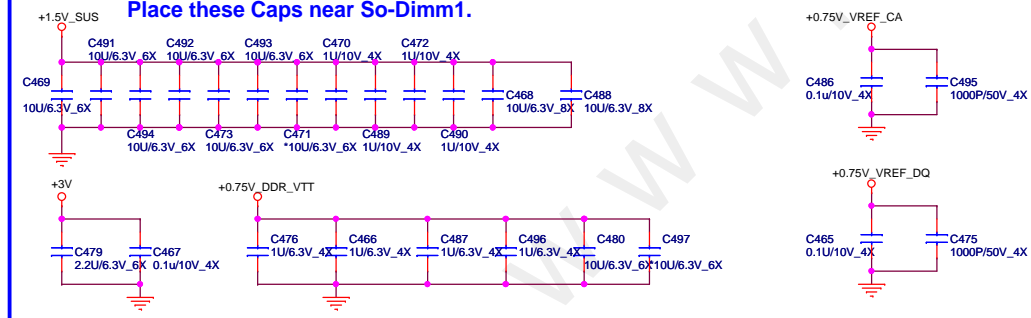


PROJECT : LZ2C
Quanta Computer Inc.

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	DDR3 SO-DIMM-0	2A
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Place these Caps near So-Dimm1.



PROJECT : LZ2C

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	DDR3 SO-DIMM-1	2A
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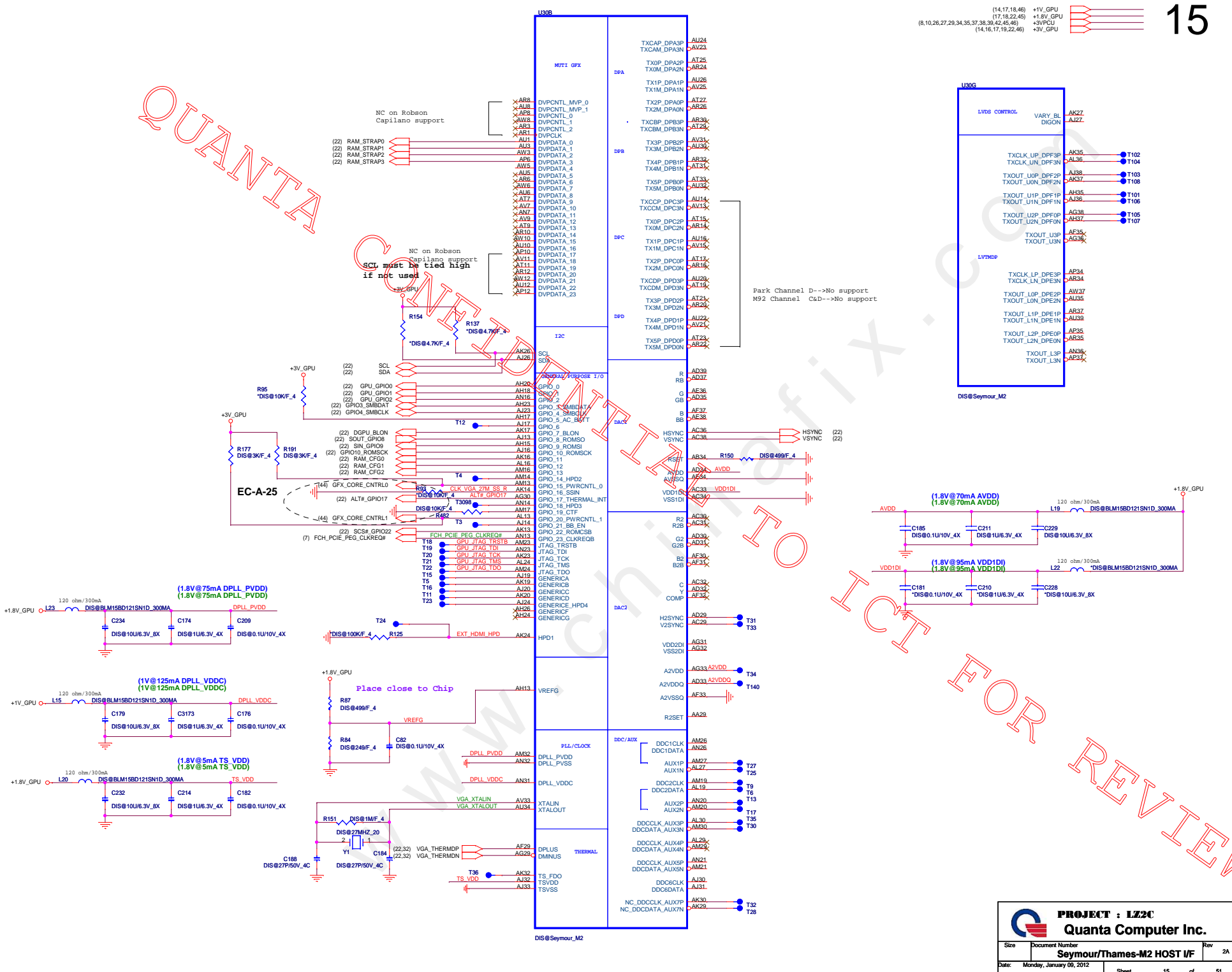
CALIBRATION



Size	Document Number	Rev
	Seymour/Thames-M2 PCIE I/F	2/
Date:	Monday, January 09, 2012	
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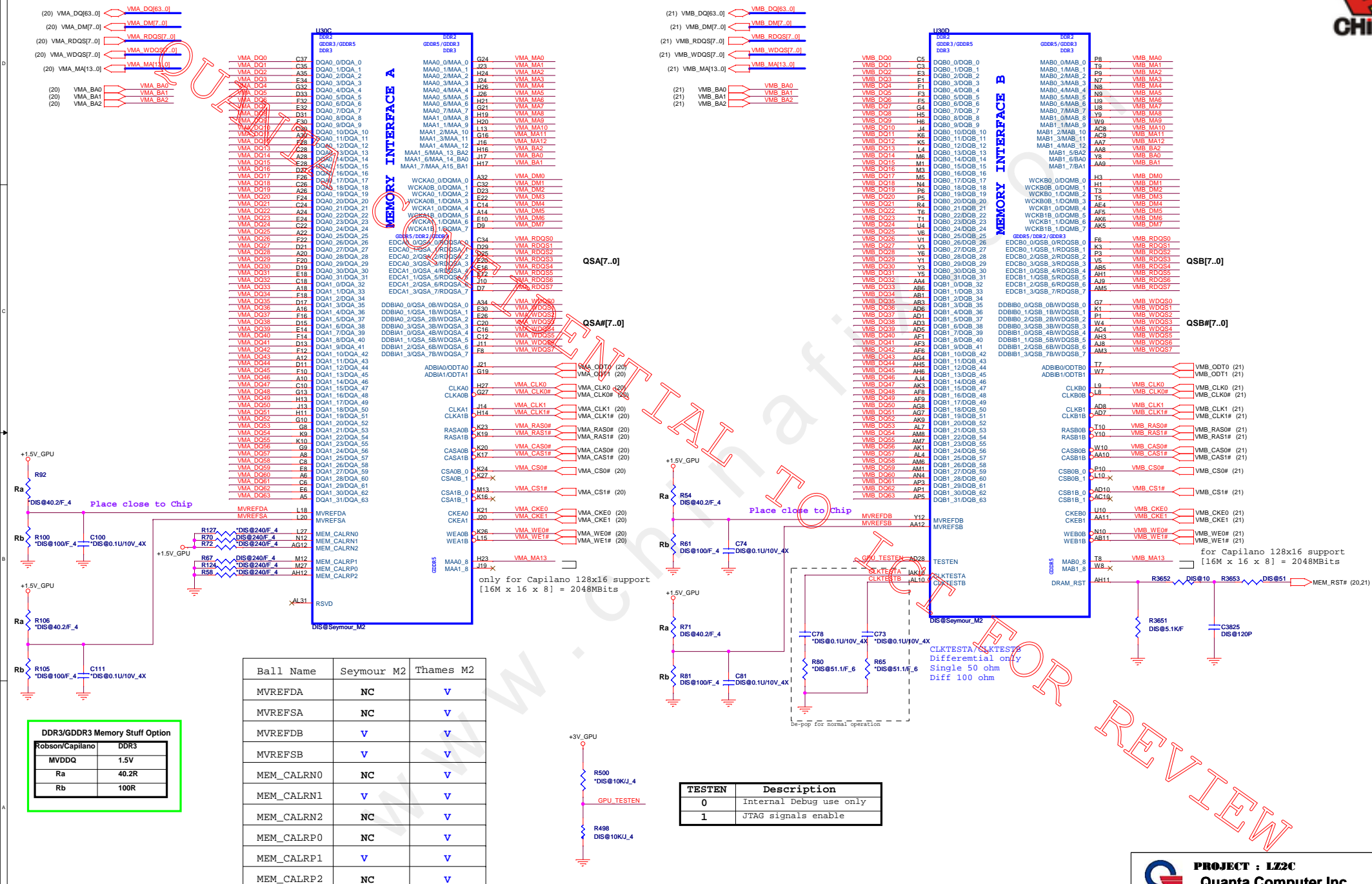
QUANTA

(14,17,18,46) +1V_GPU
(17,18,22,45) +1.8V_GPU
(8,10,26,27,29,34,35,37,38,39,42,45,46) +3VPCU
(14,16,17,19,22,46) +3V_GPU



FOR REVIEW

(14,15,17,19,22,46) +3V_{GPU}
(17,20,21,46,47) +1.5V_{GPU}

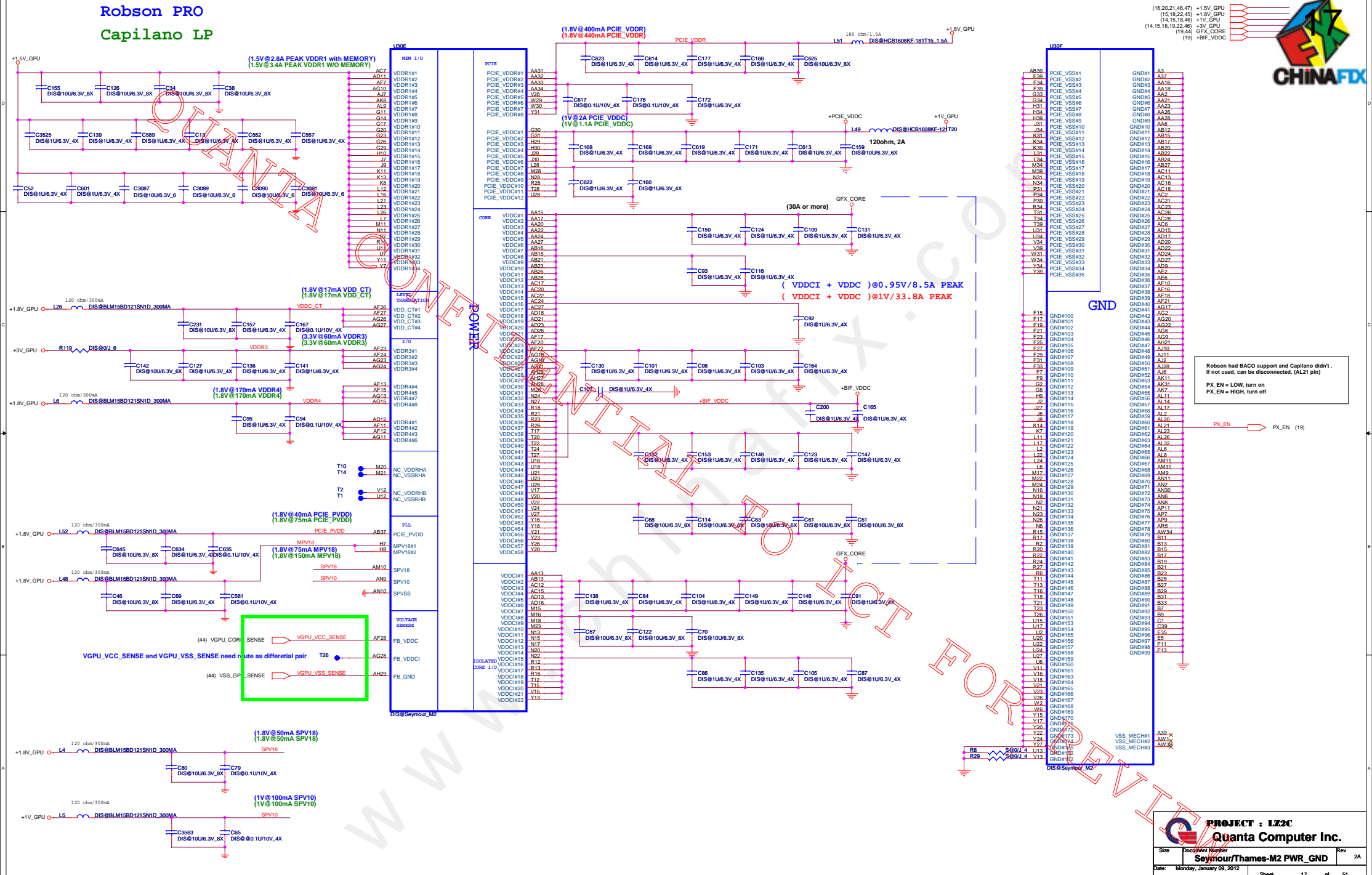


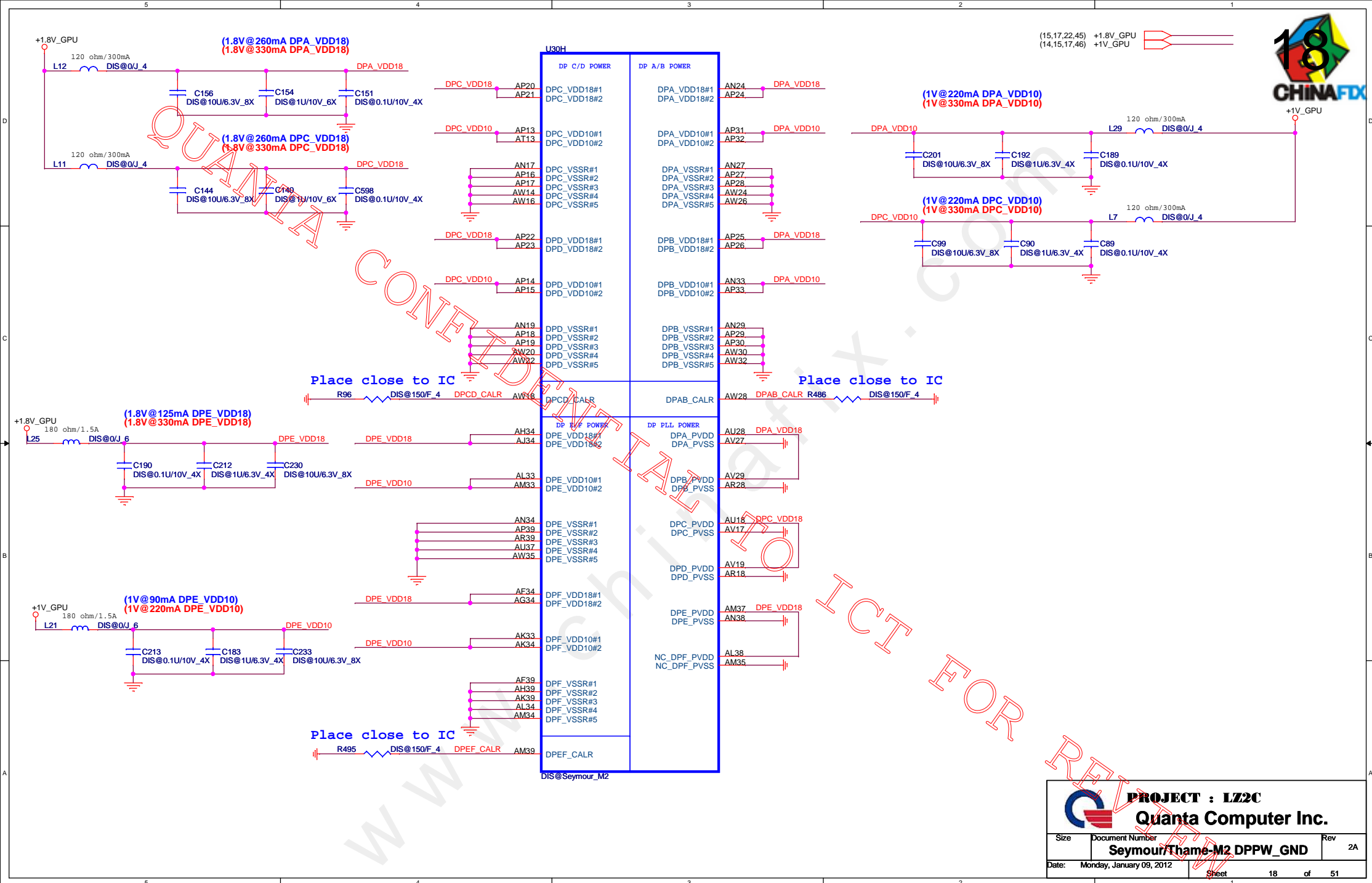
Robson/Capilano	DDR3
MVDDQ	1.5V
Ra	40.2R
Rb	100R

Ball Name	Seymour M2	Thames M2
MVREFDA	NC	V
MVREFSA	NC	V
MVREFDB	V	V
MVREFSB	V	V
MEM_CALRN0	NC	V
MEM_CALRN1	V	V
MEM_CALRN2	NC	V
MEM_CALRP0	NC	V
MEM_CALRP1	V	V
MEM_CALRP2	NC	V

TESTEN	Description
0	Internal Debug use only
1	JTAG signals enable

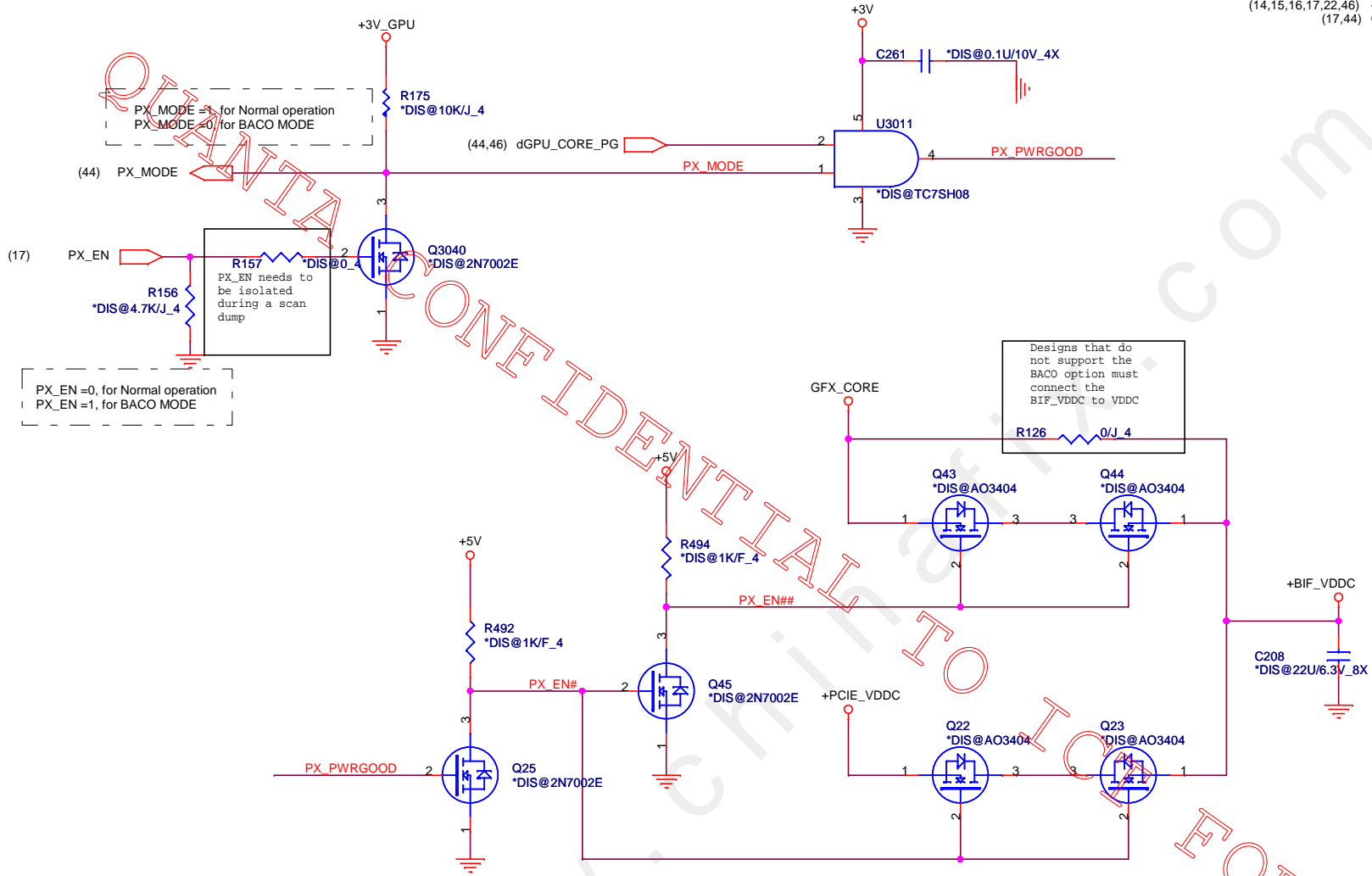
Robson PRO
Capilano LP



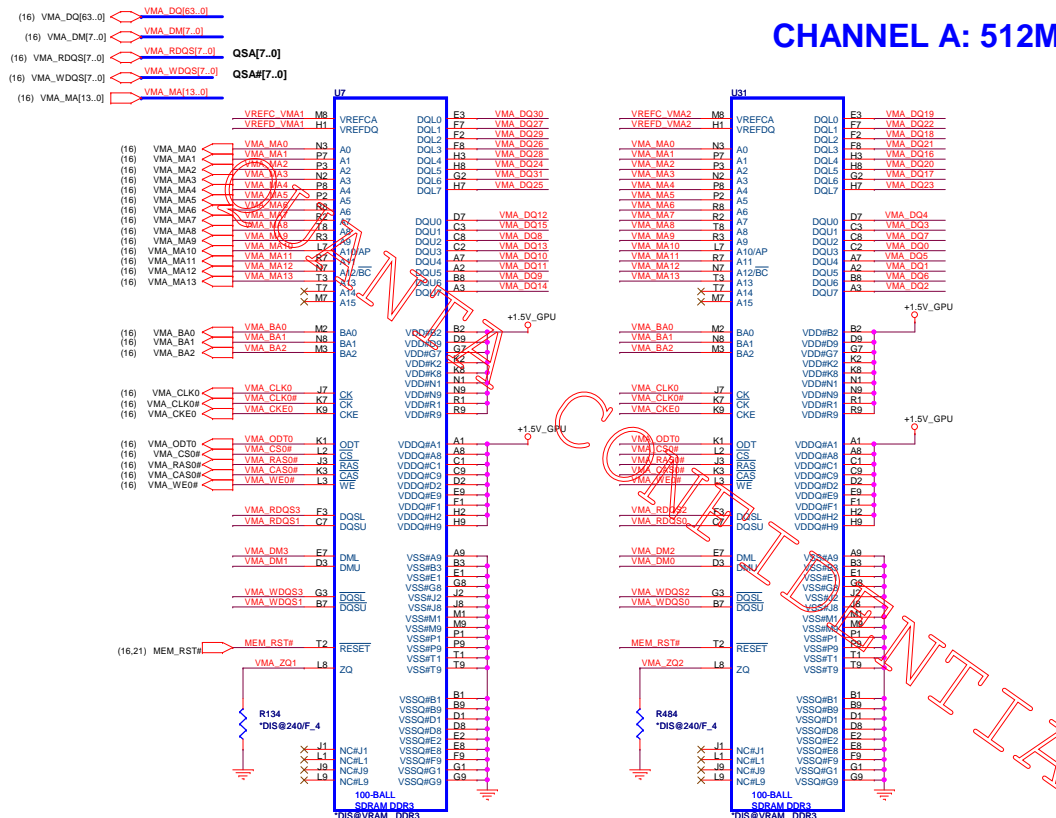


EC-B-08

(4,7,8,9,10,11,12,13,23,25,26,27,28,29,30,32,33,34,35,37,40,41,42,43,44,45,46,47) +3V
 (9,23,24,25,28,29,32,33,37,47) +5V
 (17) +PCIE_VDDC
 (14,15,16,17,22,46) +3V_GPU
 (17,44) GFX_CORE

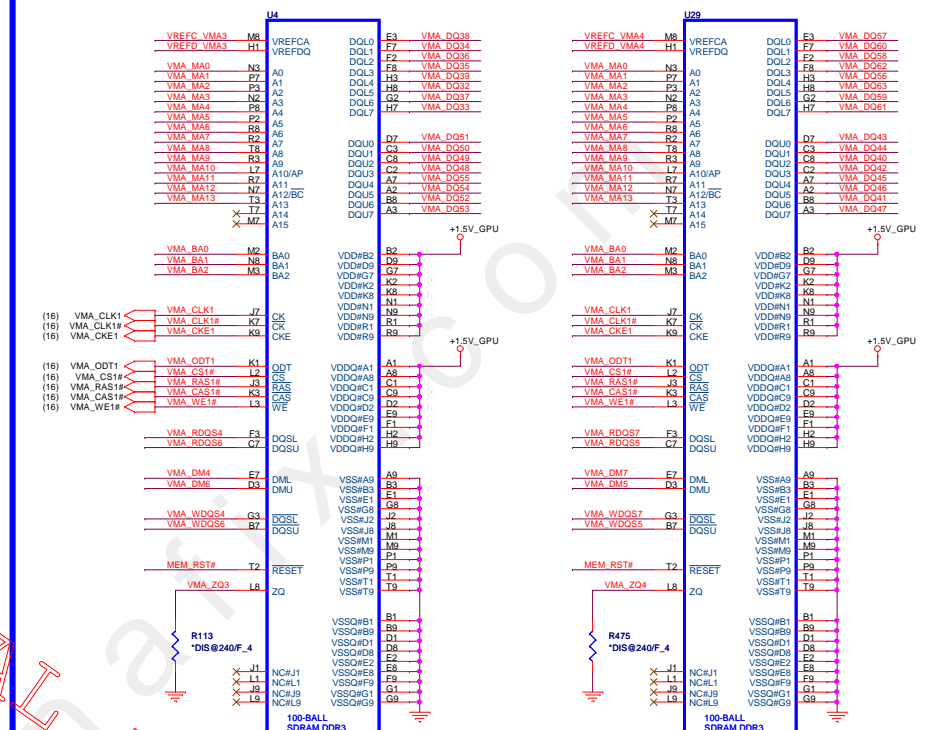


PROJECT : LZ2C Quanta Computer Inc.			
Size	Document Number	Rev	
	Seymour -M2 BACO	2A	
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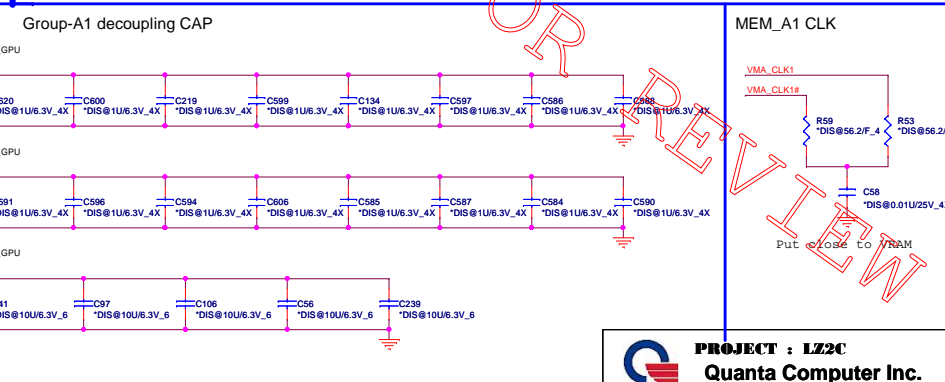
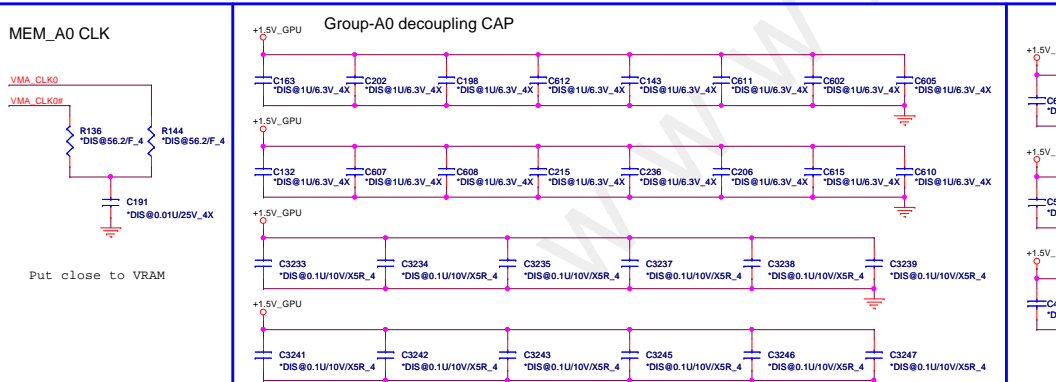
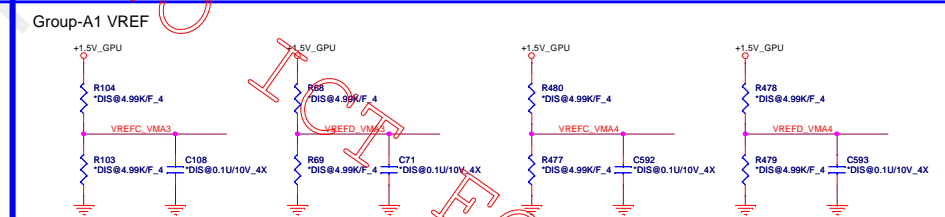
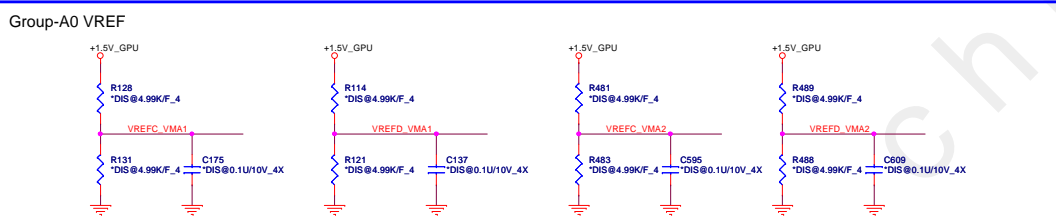
TOP Left

BOT Left



BOT Right

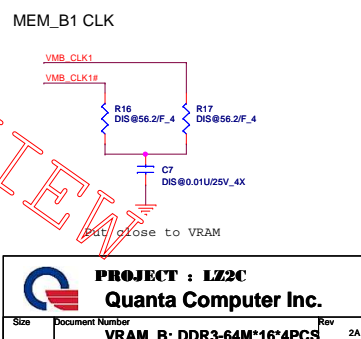
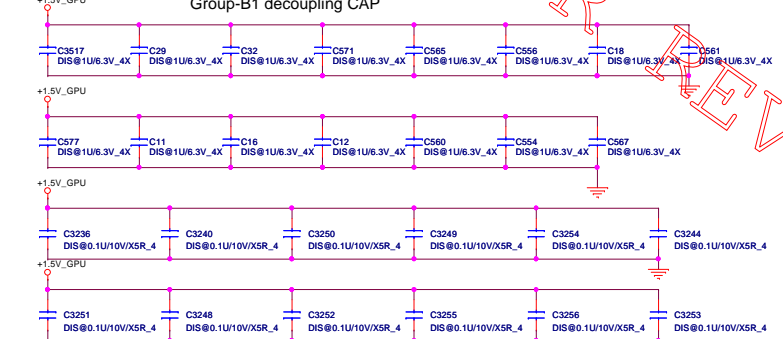
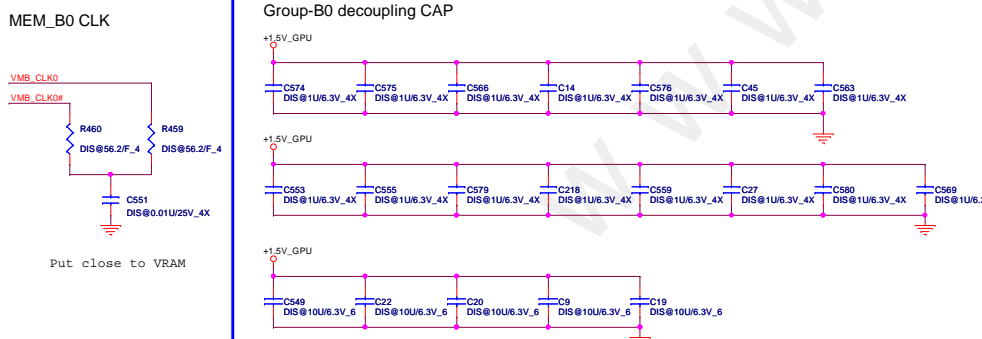
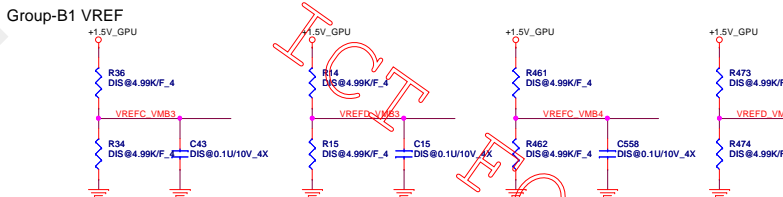
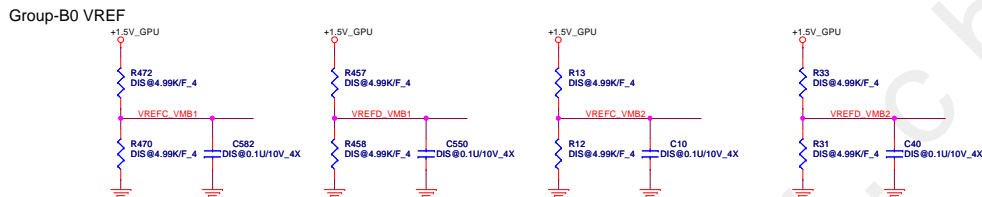
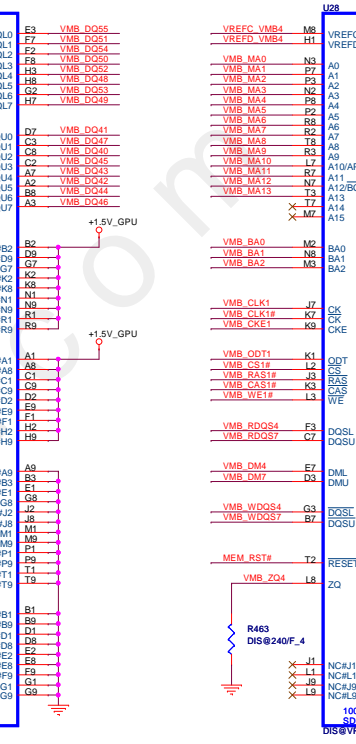
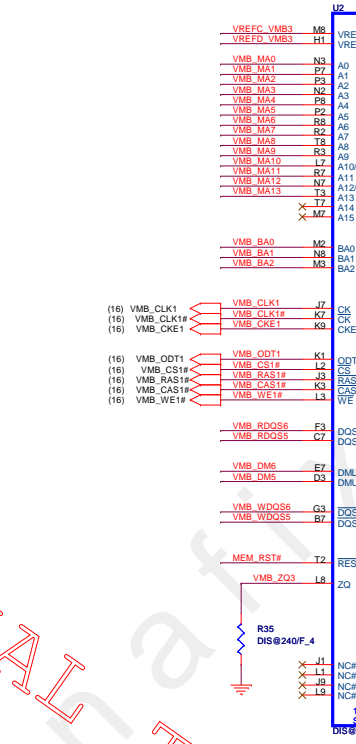
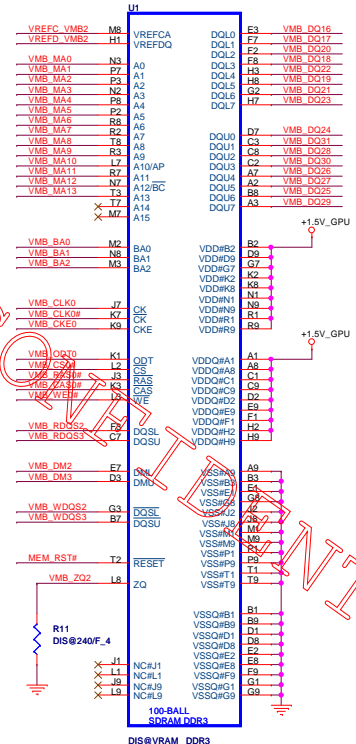
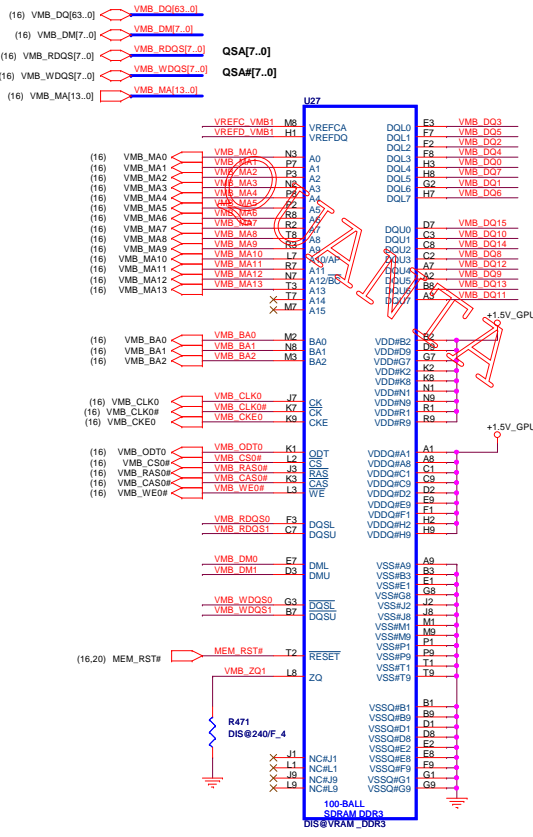
TOP Right

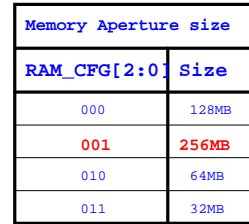


CHANNEL B: 512MB DDR3 (64M*16*4pcs)

Seymour choose channel B

(16,17,20,46,47) +1.5V_GPU



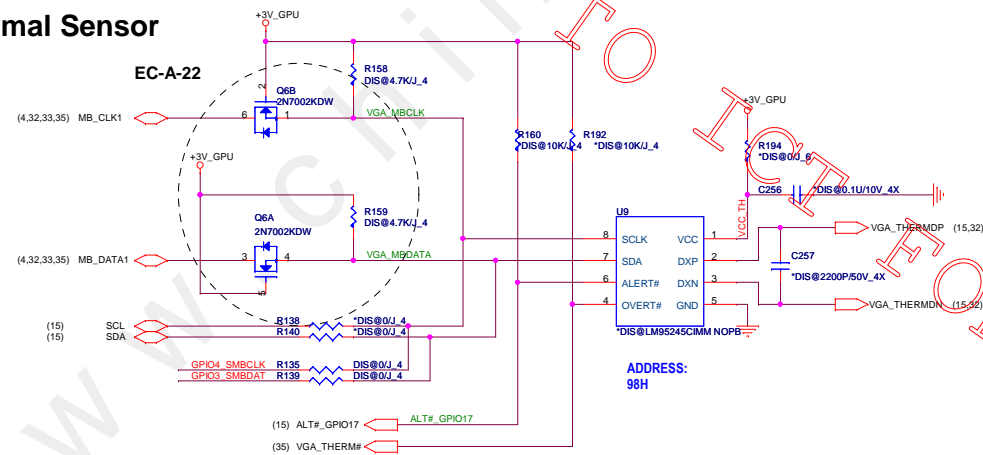


ROM Table		
HSYNC	VSYNC	Discription
0	0	No Audio
0	1	Any one by detect
1	0	DP only
1	1	Both DP & HDMI

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63DFFR-11C	AKD5LZW7W02 (64M*16-1Gb)	1GB	0	0	1	0
	H5TQ2G63BFR-11C	AKD5MGWTW00 (128M*16-1Gb)	2GB	0	0	0	0
	H5TQ2G63DFFR-11C	AKD5MGWTW16 (128M*16-1Gb)	2GB	0	1	0	0
Samsung	K4W1G1646G-BC11	AKD5EGGT500 (64M*16-1Gb)	1GB	0	0	1	1
	K4W2G1646C-HC11	AKD5MGWT500 (128M*16-1Gb)	2GB	0	0	0	1

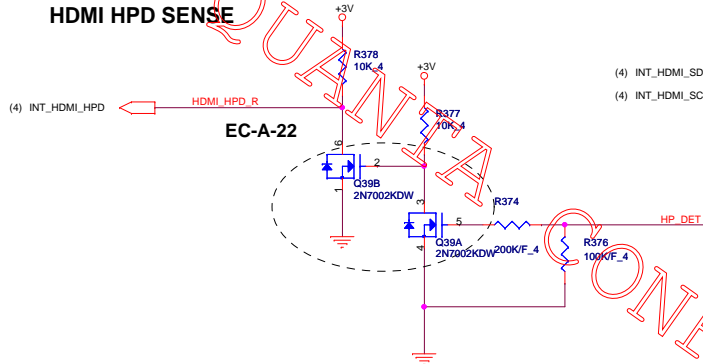
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM (Only for GDDR5) 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONXX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIe DEVICE AS 2.5GT/S CAPABLE 1 = PCIe DEVICE AS 5GT/S CAPABLE	1	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1]	HSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED.	11	See Audio table
AUD[0]	VSYN	10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI		
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIF_DEVICE_STRAP_ENA VIP:-Video Capture Port Interface	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

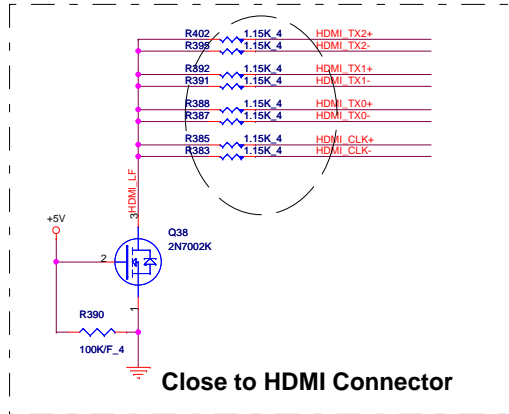


EC-A-08

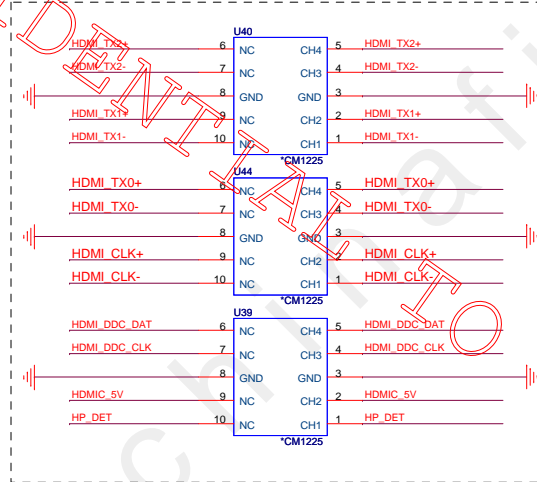
HDMI HPD SENSE



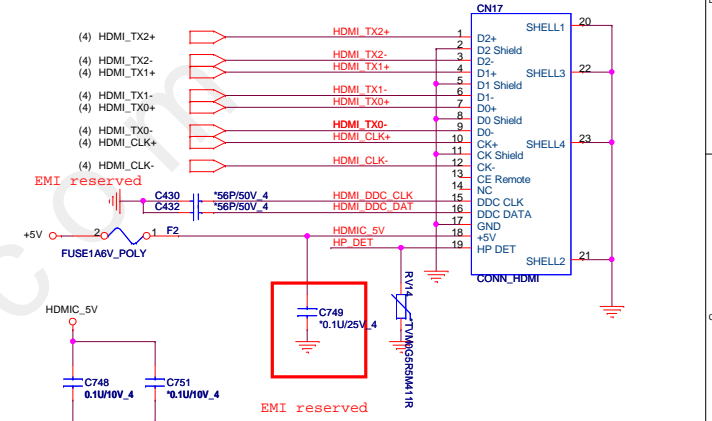
EC-B-04



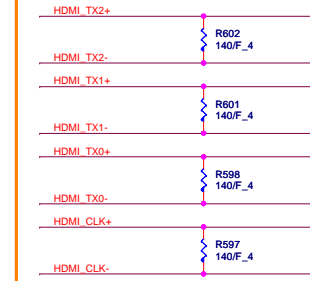
For ESD



(4,6,25,30,41,43) +1.5V
(9,19,24,25,28,29,32,33,37,47) +5V
(4,7,8,9,10,11,12,13,19,25,26,27,28,29,30,32,33,34,35,37,40,41,42,43,44,45,46,47) +3V



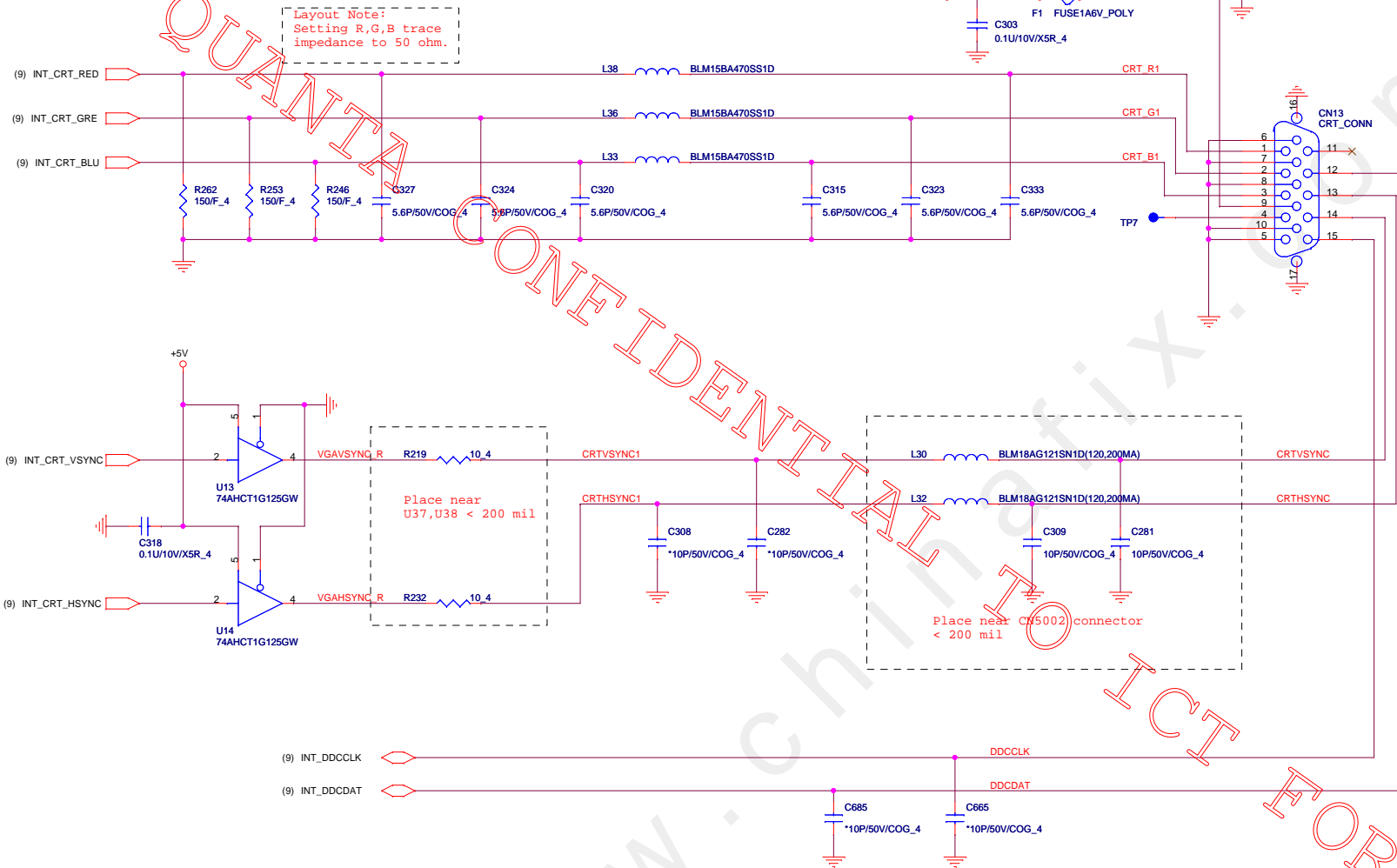
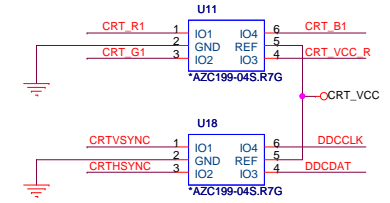
EMI reserve for HDMI



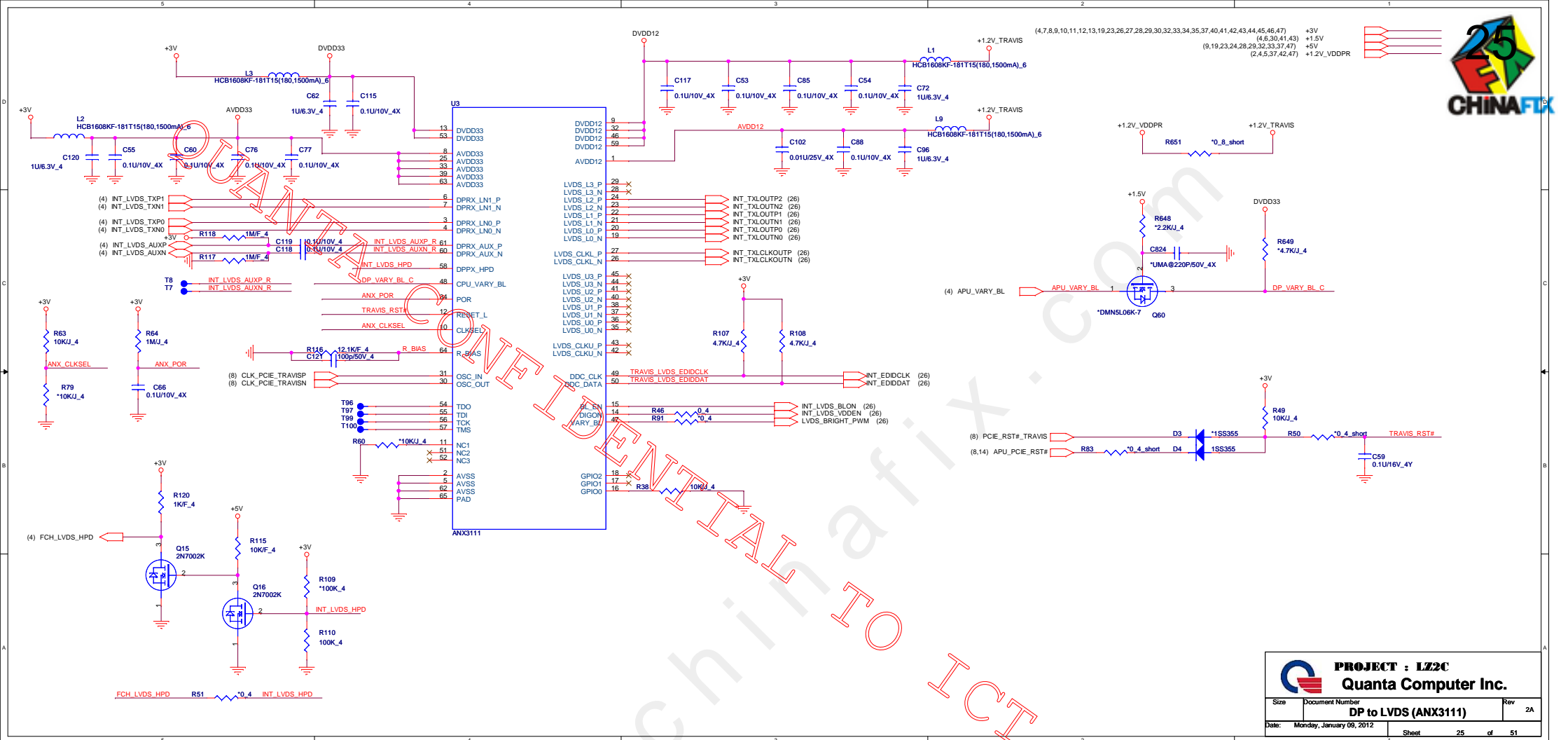
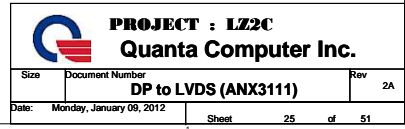
PROJECT : LZ2C		Quanta Computer Inc.	
Size	Document Number	HDMI CONN	Rev
Custom			2A
Date	Monday, January 09, 2012	Sheet	23 of 51

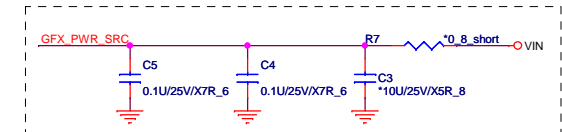


ESD PROTECTION



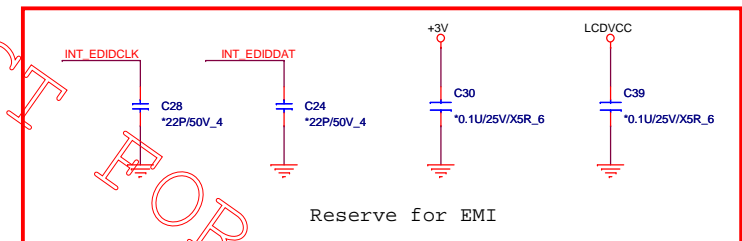
PROJECT : LZ2C Quanta Computer Inc.			
Size Custom	Document Number CRT_CONN	Rev	2A
Date: Monday, January 09, 2012	Sheet 24	of	51





The schematic diagram illustrates the power and control circuitry for the EC-A35. Key components and connections include:

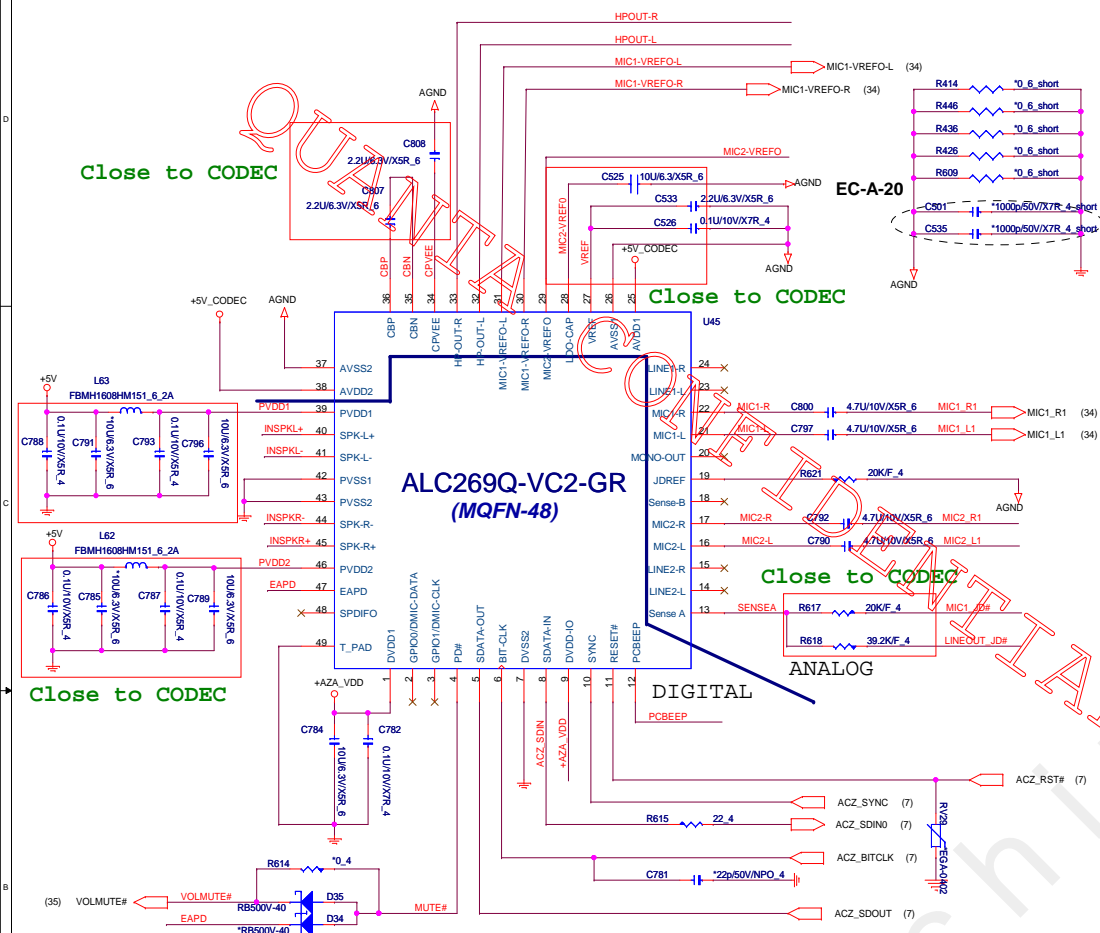
- Power Supply:** A +3VPCU source is connected to the circuit. A +3V source is also shown.
- Resistors:** R5 (10K_4), R20 (*4.7K_4), R4 (100K_4), R2 (*0.4_short), R6 (2.2K_4), R1 (*0/J_4), and R3 (10K_4) are distributed throughout the circuit.
- Capacitors:** C2 (220P/50V/X7R_4) is highlighted in a dashed circle. C1 (*47P/50V/NPO_4) and C21 (*1U/6.3V/X5R_4) are also present.
- Diodes:** D2 and D1 are Schottky diodes (RB500V-40) used for signal conditioning.
- Control IC:** Q1 (LTC044EUBFS8TL) is a precision centration and level shifter.
- Inputs:** LID551# (34,35), INT_LVDS_BLOK (25), and APU_BLEN (4) are external inputs.
- Outputs:** DISPON and LCD_BK_OFF# (7) are control signals.



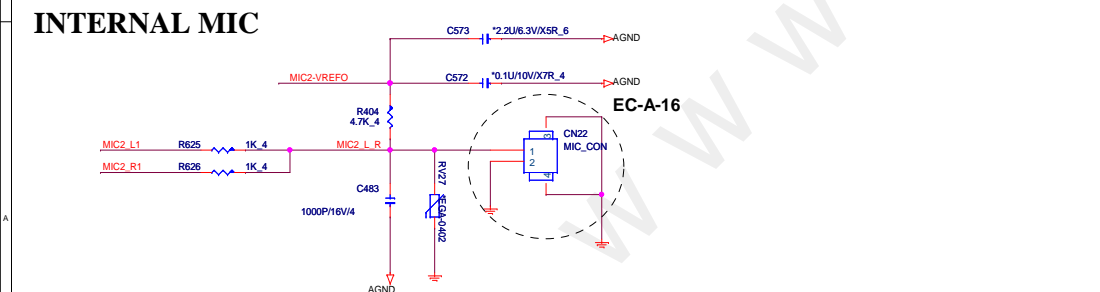


10/100 non-stuff

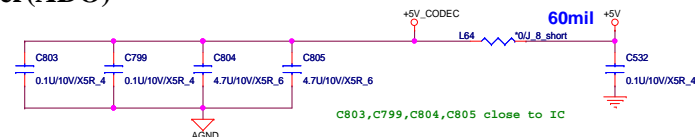
CODEC(ADO)



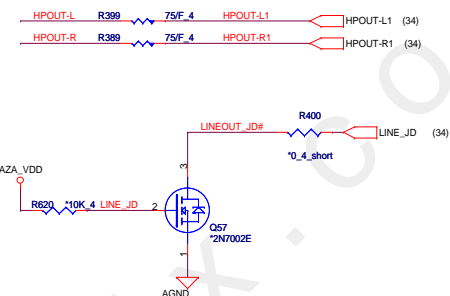
INTERNAL MIC



Codec Power(ADO)

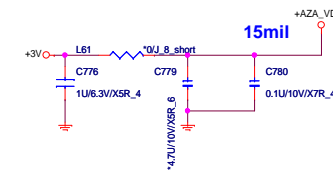


Earphone(AMP)



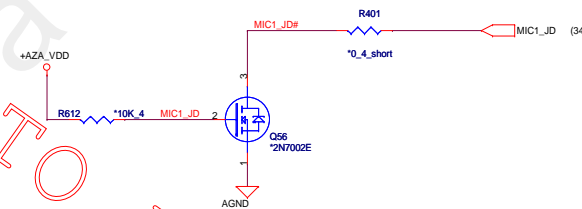
HDA Power(ADO)

*Intel HDA Either +1.5V_S5 or +3V_S5

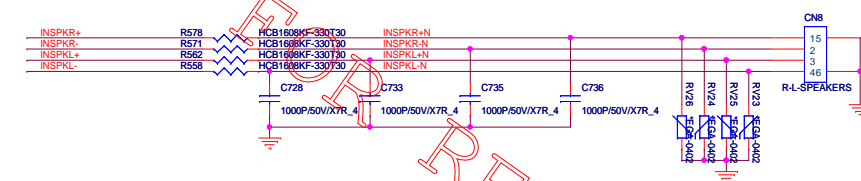


System MIC(AMP)

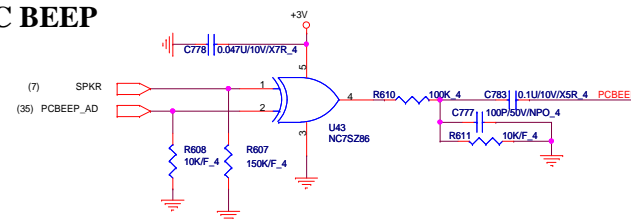
(4,7,8,9,10,11,12,13,19,23,25,26,27,29,30,32,33,34,35,37,40,41,42,43,44,45,46,47) (9,19,23,24,25,29,32,33,37,47) +5V +3V



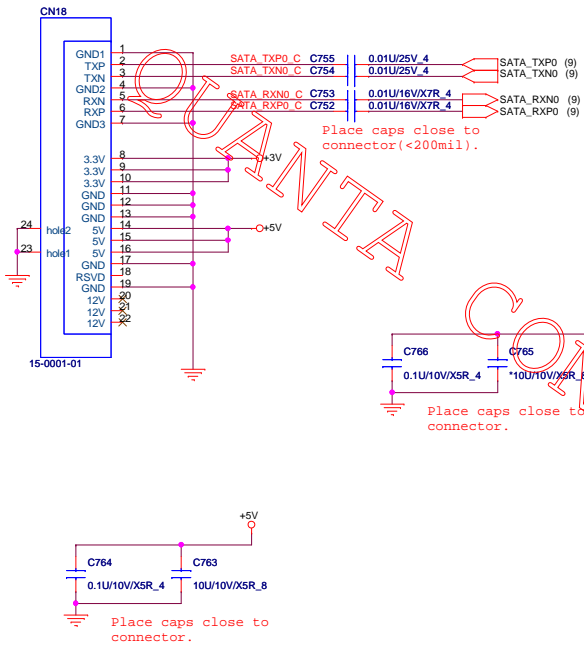
Speaker(AMP)



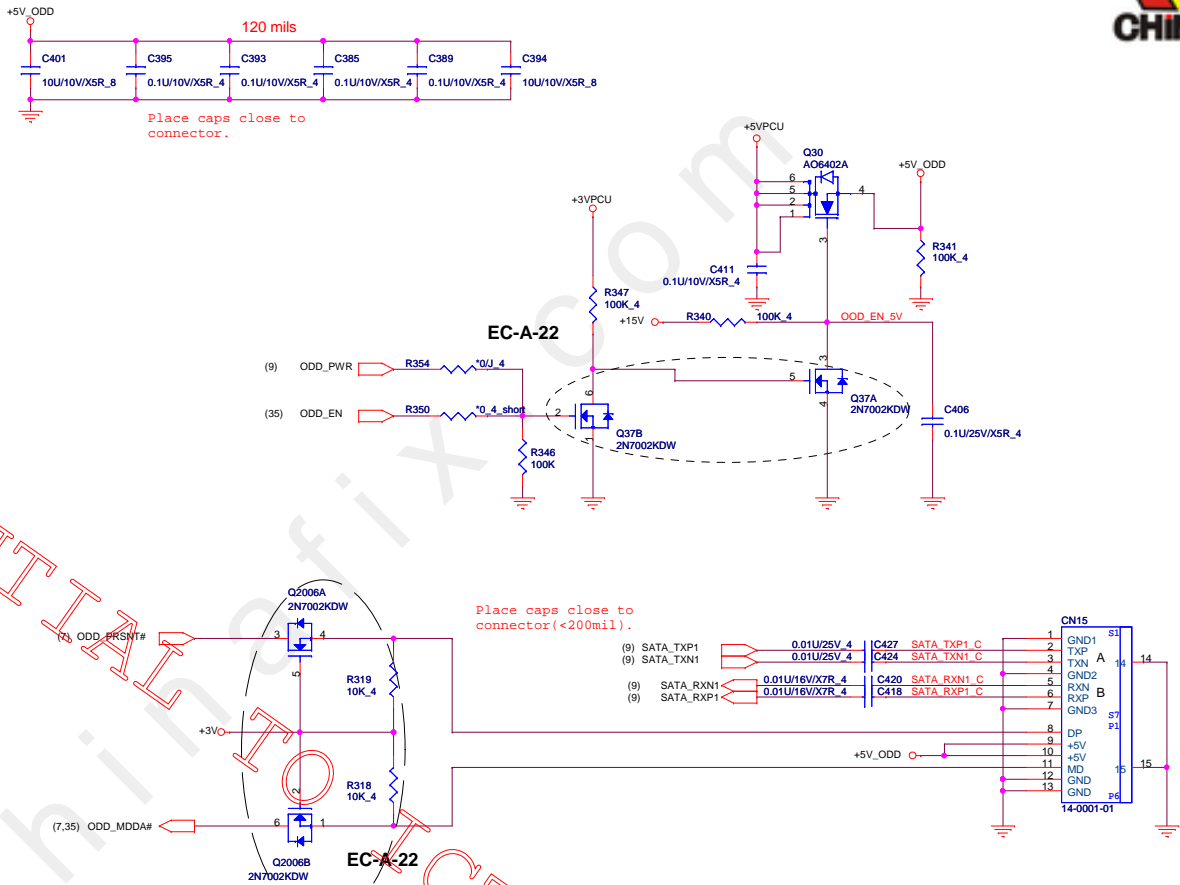
PC BEEP




SATA HDD Connector.

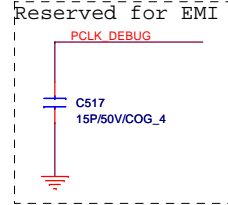


SATA ODD Connector.



			PROJECT : LZ2C	
			Quanta Computer Inc.	
Size Custom	Document Number SATA HDD/CD-ROM			Rev 2A
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MiniCard WLAN connector



PCI-Express TX and RX
direct to Connector

EC-B-09

EC-A-01

EC-C-01

ACS-88911-5204

EC-A-24

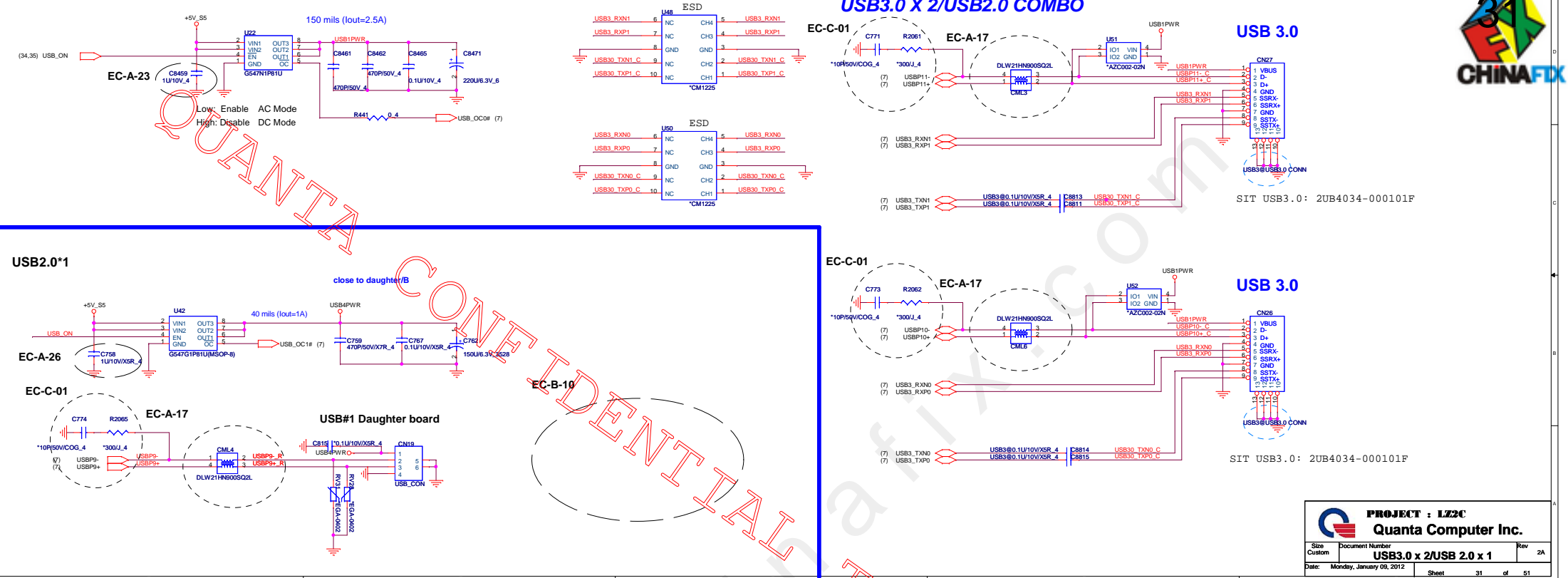
EC-A-20

For RF

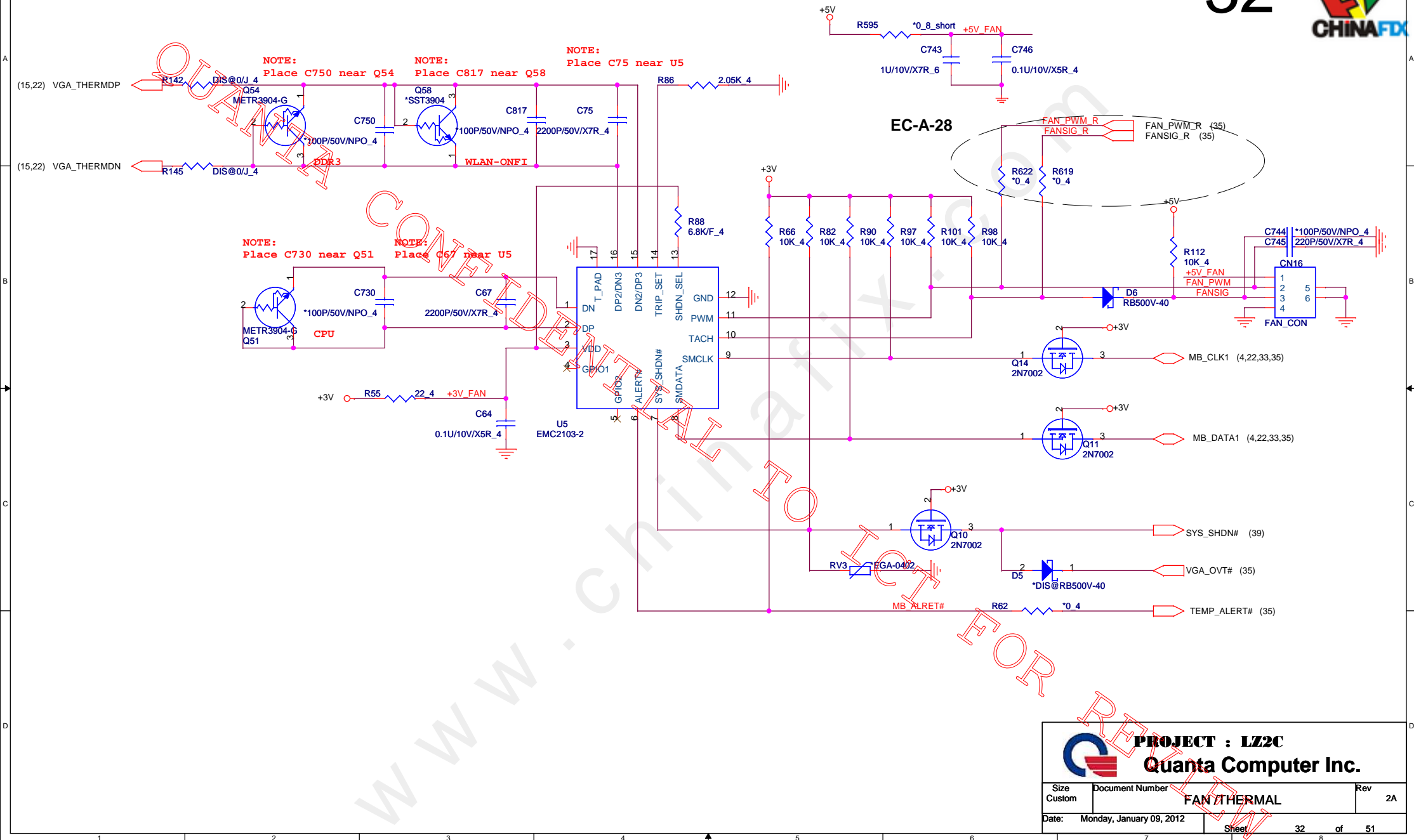
Place caps close to
connector.

Place caps close to
connector.

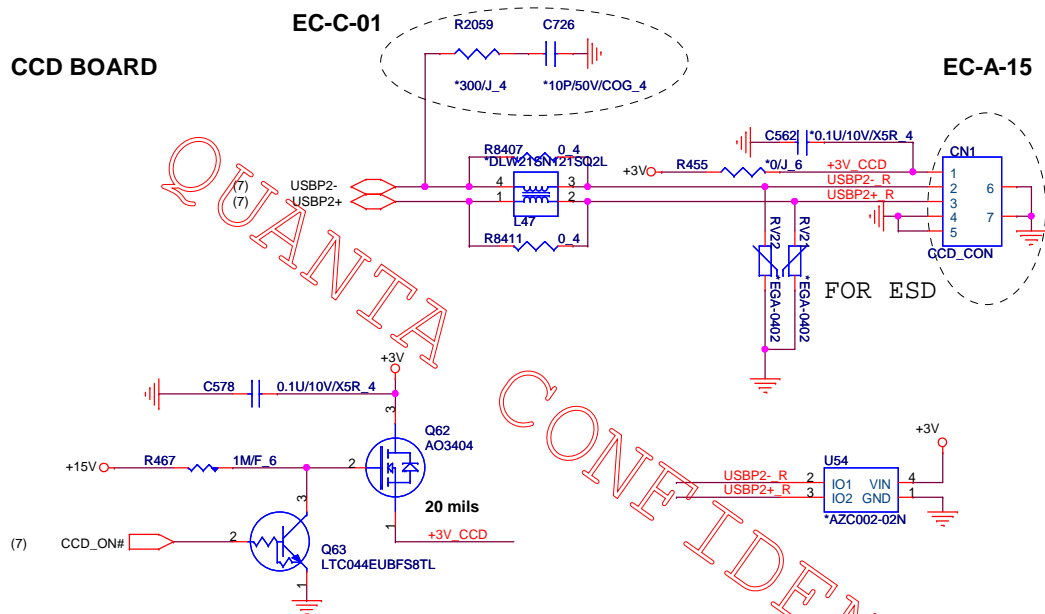
PROJECT : LZ2C		Quanta Computer Inc.	
Site Custom	Document Number MINI-Card WLAN	Rev	2A
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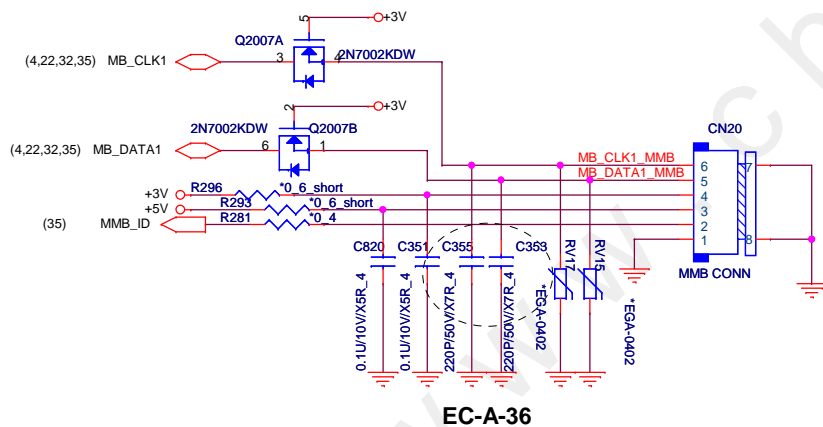
(4,7,8,9,10,11,12,13,19,23,25,26,27,28,29,30,33,34,35,37,40,41,42,43,44,45,46,47) +3V
(9,19,23,24,25,28,29,33,37,47) +5V



CCD BOARD



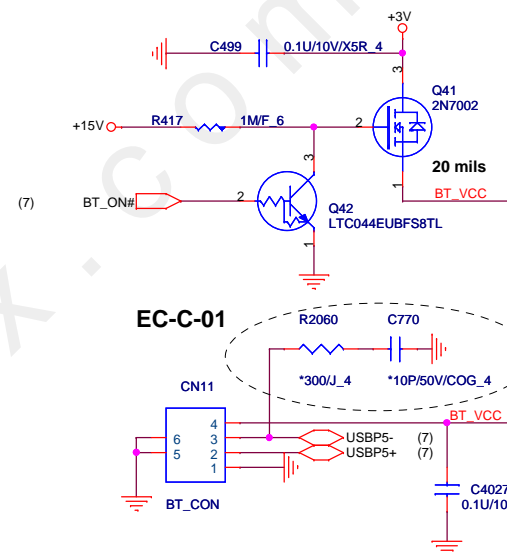
MMB



(4,7,8,9,10,11,12,13,19,23,25,26,27,28,29,30,32,34,35,37,40,41,42,43,44,45,46,47) +3V
(10,26,29,37,39,41,46) +15V
(9,19,23,24,25,28,29,32,37,47) +5V



BLUETOOTH



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Size	Document Number	Rev	2A
		BT/USB2.0*2	
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KEYBOARD

EC-A-18

EC-B-11

POWER BOARD

EC-A-32

Touch pad

LED

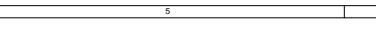
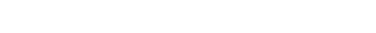
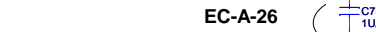
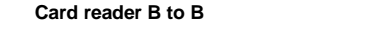
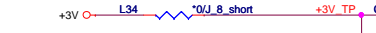
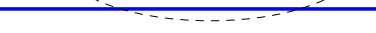
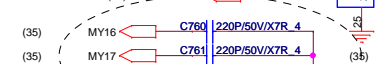
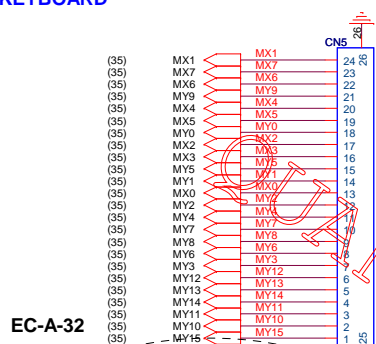
Card reader B to B

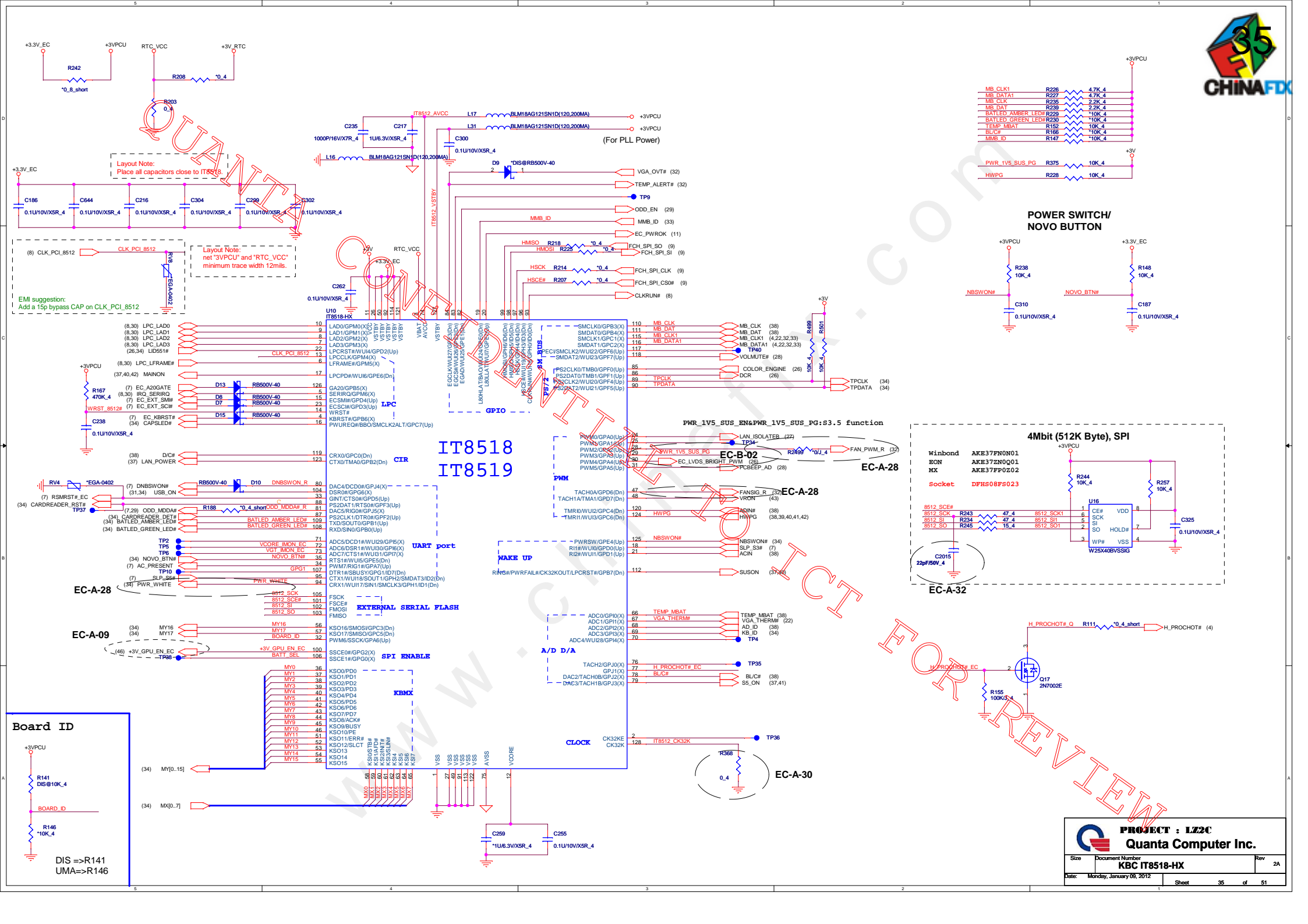
EC-A-34

Power/suspend LED

CAPS LED

EC-A-19





Screw for ME



VGA

HOLE18

HOLE20

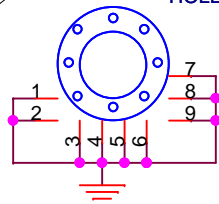
DIS@H-TC5_5BC4I3D3P2 DIS@H-TC5_5BC4I3D3P2



SMT NUT H=4 / 7mm

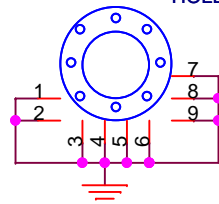
EC-A-26

HOLE17



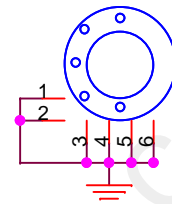
*HG-TC276BC315D106P2

HOLE4



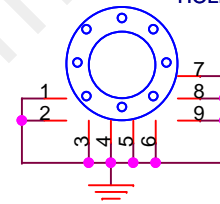
*HG-TC276BC315D106P2

HOLE7



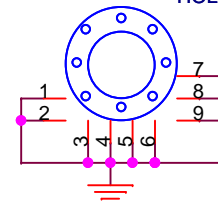
*HG-TC6_5IC3_7BC8D2_7P2-4

HOLE13



*HG-TC276BC315D106P2

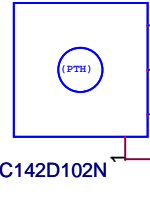
HOLE16



*HG-TC276BC315D106P2

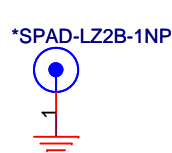
CPU BKT

HOLE9



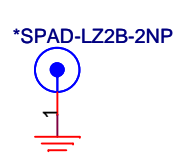
*C142D102N

HOLE11



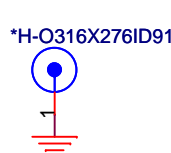
*SPAD-LZ2B-1NP

HOLE5



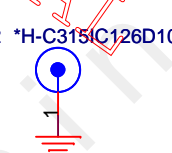
*SPAD-LZ2B-2NP

HOLE1



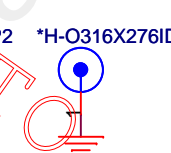
*H-O316X276ID91P2

HOLE2



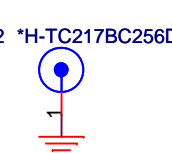
*H-C315IC126D106P2

HOLE3



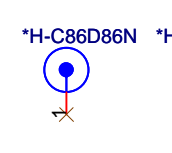
*H-O316X276ID91P2

HOLE6



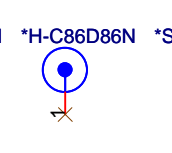
*H-TC217BC256D118P2

HOLE8



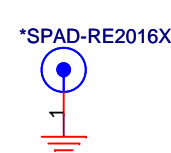
*H-C86D86N

HOLE10



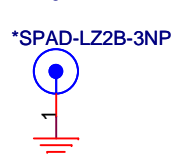
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HOLE12



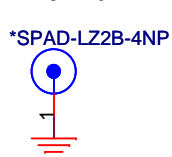
*SPAD-RE2016X60NP

HOLE14



*SPAD-LZ2B-3NP

HOLE15



*SPAD-LZ2B-4NP



PROJECT : LZ2C

Quanta Computer Inc.

Size Custom

Document Number

HOLD & SKEW

Rev

2A

Date: Monday, January 09, 2012

Sheet

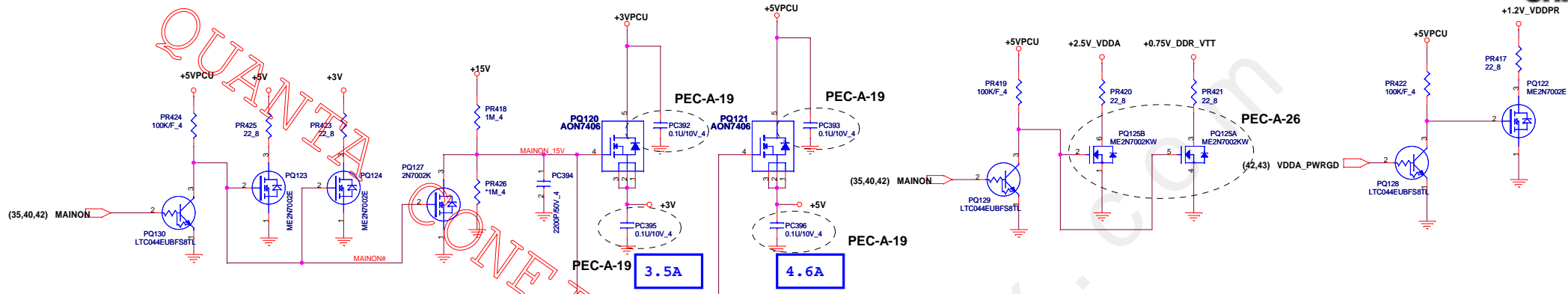
36

of

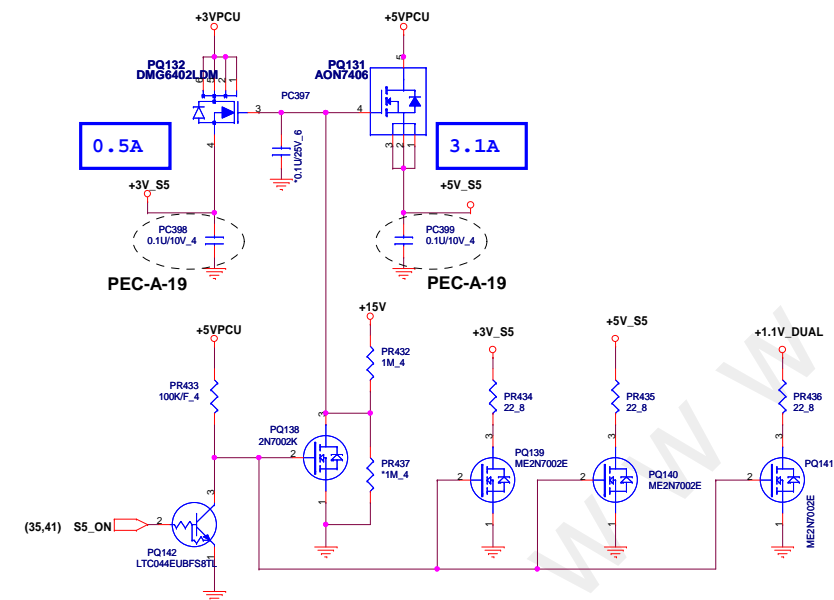
51

DISCHARGE

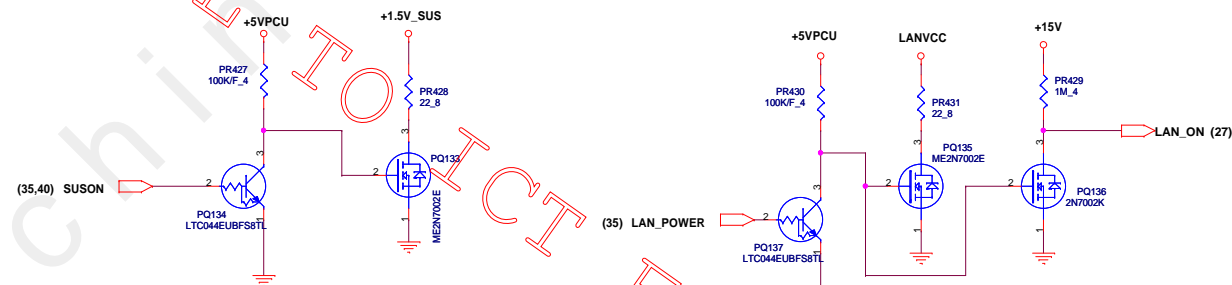
+3V, +5V

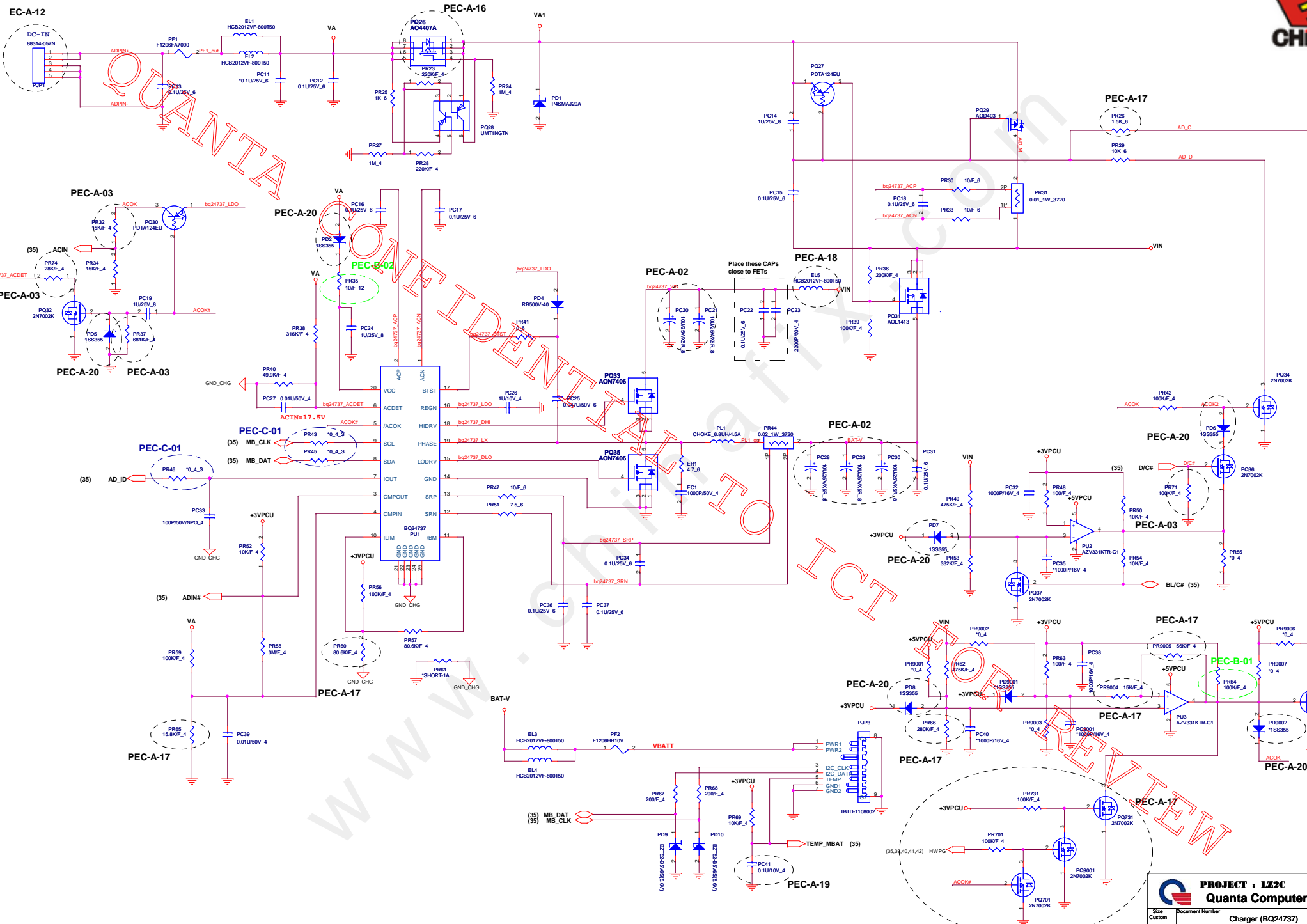


3V_S5, 5V_S5



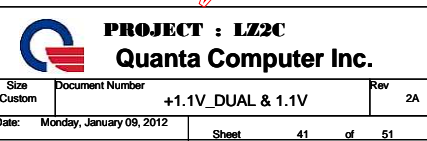
LANVCC

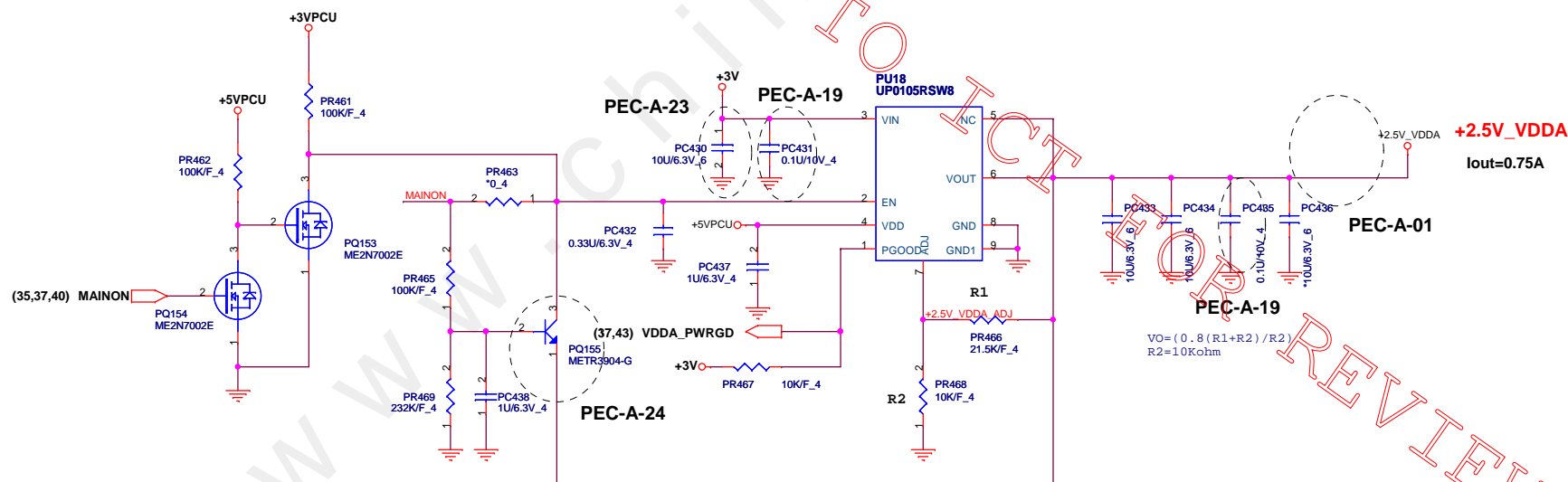
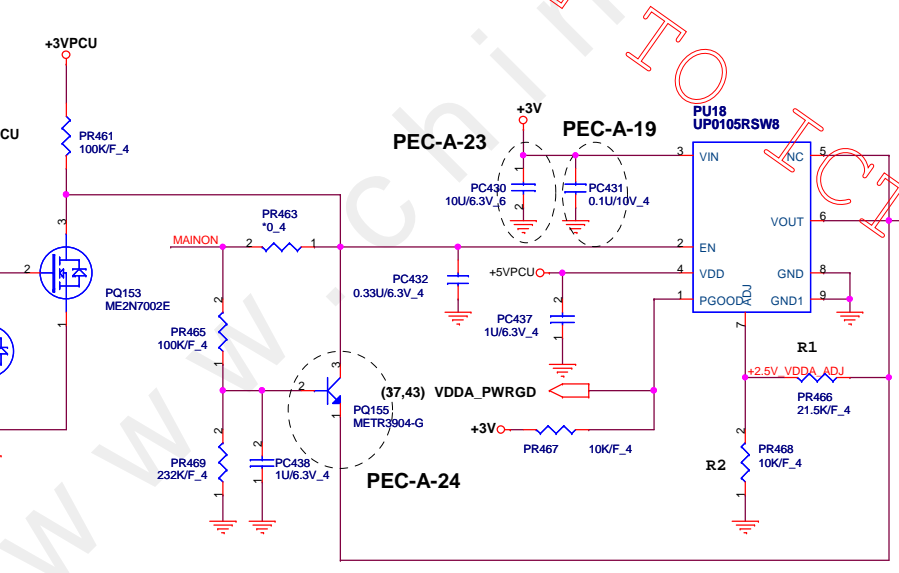


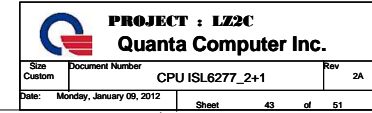


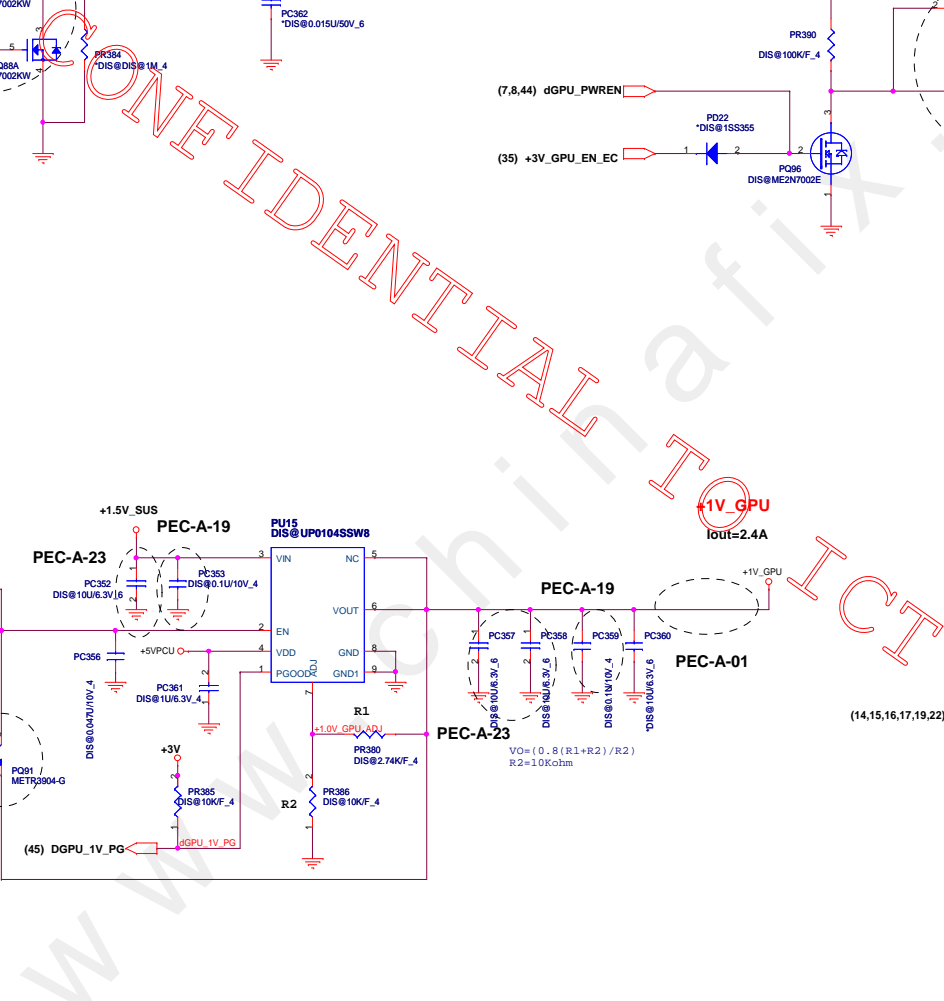




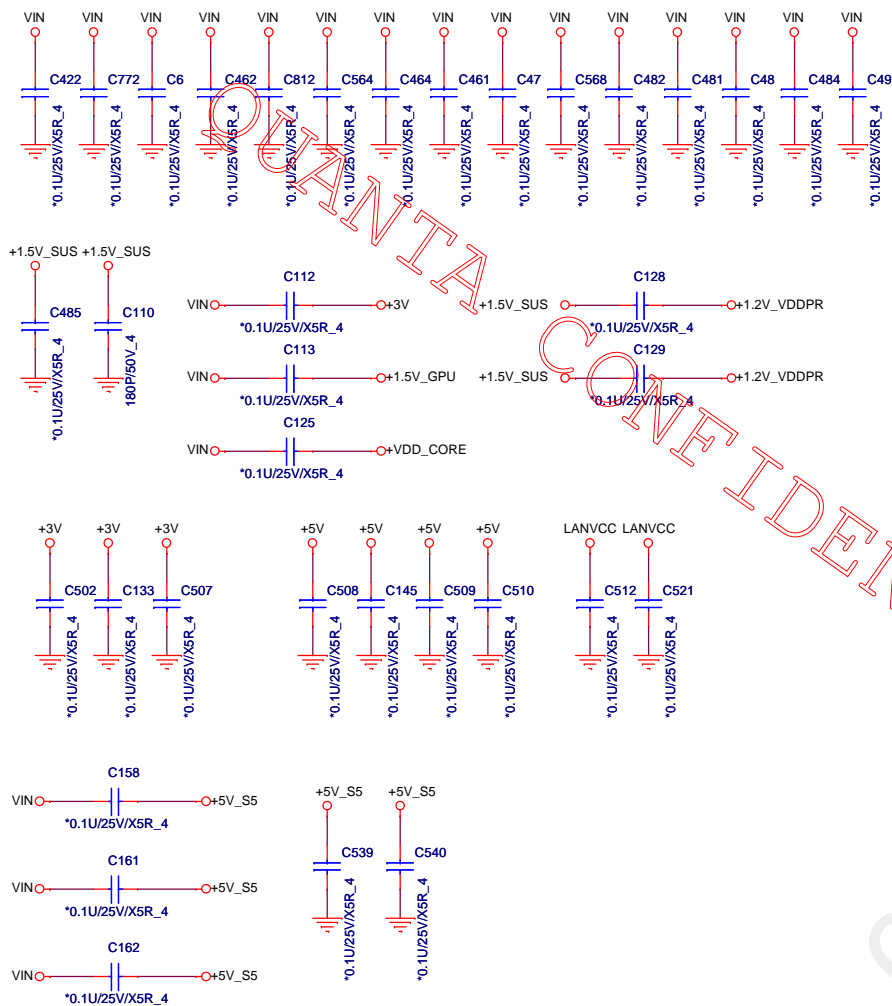




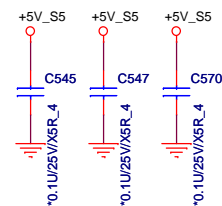






ESD suggestion



EMI suggestion



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		Quanta Computer Inc.	
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2011	SDV~SIV	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION							
		EC-A-01	30	08/23	CN21	Change connection form pin19 to pin 5 due to module choose as below #5: Liteon #53: Cyber TAN POP R628 & R629							
		EC-A-02	26	08/23	C23	C23 change from 0603 to 0402							
		EC-A-03	4,8	08/23	U2001,U15	DELETE SOME TPS							
		EC-A-04	4	08/24	U2001	add pull high resistor R2053~R2057 for JTAG signals.							
		EC-A-05	4	08/24	R2033	reserve R2033 for Test35							
		EC-A-06	8	08/25	R189	change R189 to 0 ohm							
		EC-A-07	9	08/25	R280,R286,R292	pull up resistor from +3V to +3V_S5							
		EC-A-08	23	09/02	U49	U49.1 need connect to +3V to meet D.G.							
		EC-A-09	35	09/06	U35	move net +3V_GPU_EN_EC to pin 100							
		EC-A-10	5	09/06	U2001	add C2117 & C2116 & C2118 to improve +VDDNB_CORE ripple							
		EC-A-11	7	09/06	U15	change port 0 and port 8 setting							
		EC-A-12	38	09/06	PJP1	change pin define for PJP1							
		EC-A-13	34	09/06	R28	Pop R28 for K/B ID setting							
		EC-A-14	8	09/07	G3	Add short pad for RTC							
		EC-A-15	33	09/26	CN1	add pin5 for CN1							
		EC-A-16	34	09/26	CN9	change CN9 footprint							
		EC-A-17	31	10/05	CML3/CML4/CML6/R8406 R8410/R8405/R8409/R8198 R8200	add CML4(CX21SQ2L000) and delete R8406/R8410 for EMI request and CML3/4/6 change footprint to choke-dlw21s-4p add CML3&CML6(CX21SQ2L000) and delete R8405/R8409/R8198/R8200 for EMI request							
		EC-A-18	34	10/05	CA1~CA6	POP for EMI request							
		EC-A-19	34	10/05	C2119,C2120	add C2119 for CARDREADER_DET# and C2120 for CARDREADER_RST# from EMI request							
		EC-A-20	28 30	10/05	C501,C535 C530	change footprint to short pad from EMI request							
<div><div></div><div>PROJECT : LZ2C Quanta Computer Inc.</div></div> <table><tr><td>Size B</td><td>Document Number</td><td>EC list1</td><td>Rev 2A</td></tr><tr><td colspan="2">Date: Monday, January 09, 2012</td><td>Sheet 48</td><td>of 51</td></tr></table>						Size B	Document Number	EC list1	Rev 2A	Date: Monday, January 09, 2012		Sheet 48	of 51
Size B	Document Number	EC list1	Rev 2A										
Date: Monday, January 09, 2012		Sheet 48	of 51										

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-A-21	26	10/05	R10/R27	Not support DCR & COLOR_ENGINE from customer request
EC-A-22	26	10/05	Q19,Q20,Q6	change to dual mosfet Q6
	23		Q34,Q35,Q39	change to dual mosfet Q39
	29		Q31,Q36,Q37	change to dual mosfet Q37
	29		Q27,Q28,Q2006	change to dual mosfet Q2006
EC-A-23	31	10/05	C8459	C8459 change to 1uF/10V/0402
EC-A-24	27	10/05	C513,C519	change to 4.7uF/6.3V/0603
	30		C528	
EC-A-25	15	10/05	U30	change GFX_CORE_CNTRL0/GFX_CORE_CNTRL1 for VBIOS setting
EC-A-26	31	10/05	C758	change to 1U/10V/X5R_4
	34		C757	
EC-A-27	36	10/06	hloe17	add hole 17
EC-A-28	32/35	10/06	R2498/R2499/R619/R622	reserve R2498/R2499/R619/R622 for EC control FAN
EC-A-29	8	10/06	U15	change dGPU_1.8V_PG to GPIO46
EC-A-30	35	10/06	R368	reserve for GPIO pin
EC-A-31				
EC-A-31				
EC-A-32	34	10/07	C760,C761	POP for EMI request
EC-A-32	35	10/7	C2015	Change from 220p to 22p, POP for EMI request
EC-A-33	27	10/14	C515,C516	Change from 27p to 33p, vendor test result.
EC-A-34	34	10/14	C197,C199,C203	Change from 1000p to 220p, POP for EMI request
EC-A-35	26	10/18	C2	Change from 0.1U to 220p, POP for EMI request
EC-A-36	33	10/14	C353,C355	Change from 10p to 220p, POP for EMI request
EC-B-01	10	11/04	R343	change R343 to power rail from Vin to +15V
EC-B-02	35	11/14	U10	reserve PWR_1V5_SUS_EN&PWR_1V5_SUS_PG:S3.5 function
EC-B-03	04	11/18	R2496,R2497	pop for EC can read graphic temp.
EC-B-04	23	11/18	R383,R385	tune resistor to meet AMD spec.
			R387,R388	
			R391,R392	
			R395,R402	

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-B-06	26	11/18	Q3,Q4,Q65,R23	Delete Q3,Q4 add Q65 and R23 change to 47 ohm
EC-B-07	8	11/18	R309,R312	change to 0 ohm due to non pci device.
EC-B-08	19	11/18		R126 pop & depop C208,C261,Q22,Q23,Q25,Q43,Q44,Q45,Q3040,R156,R157,R175,R492,R494,U3011 for PX5 implement
EC-B-09	30	12/06	D28	reserve to prevent leakage
EC-B-10	31	12/06	U53	remove
EC-B-11	34	12/06	CA3/CA4/C204/C205 C220/C221/C222 C223/C224/C225	CA3,CA4 change to 0402*8(C204,C205,C220,C221,C222,C223,C224,C225)
EC-B-12	7	12/06	R527	reserve for dgpu_pwr_en
EC-B-13	27	12/06		Reserve for Surge Line to GND Gas Tube Discharge
EC-C-01	30	01/03	R2066,C775	Add resistor(300ohm) and CAP(10PF) to meet AMD spec.
	31		R2065,C774	
	33		R2061,C771	
	34		R2062,C773	
			R2059,C726	
			R2060,C770	
			R2042,C708	
			R2058,C710	

2011	SDV~SIV	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
		PEC-A-01	38,39,40,41,42	09/21	PJP4,PJP5,PJP6,PJP7,PJP8,PJP9,PJP32,PJP33,PJP34,PJP35,PJP36,PJP26,PJP29,PJP16,PJP17,PJP31	Change open pad to short pad.
		PEC-A-02	38,39,40,41,43,44	09/22	PC30,PC21,PC28,PC29,PC30,PC42,PC43,PC44,PC45,PC68,PC70,PC403,PC404,PC420,PC421,PC503,PC504,PC514,PC532,PC533,PC547,PC548,PC514,PC519,PC335,PC336	Change MLCC 10UF size from 1206 to 0805.
		PEC-A-03	38	09/22	PR32,PR37,PR71,PR78,PR74	Adjust AC plug-in detect function.
		PEC-A-04	39	09/22	PR81,PR82	PR81,PR82 change from 140K to 121K for 3V/5V OCP.
		PEC-A-05	40	09/22	PR100	PR100 change from 124K to 82.5K for 1.5VSUS OCP.
		PEC-A-06	41	09/22	PR440,PR444,PL20	PR440 change from 100K to 75K for 1.1V_DUAL OCP. PR440 change from 0.2ohm to 2.2 ohm for improve ringing voltage. PL20 change from 100K to 2.2K for improve ripple.
		PEC-A-07	42	09/22	PR455,PR458,PL21,PC440	PR455 change from 100K to 75K for 1.1V_DUAL OCP. PR455 change from 0.2ohm to 2.2 ohm for improve ringing voltage. PL21 change from 100K to 2.2K for improve ripple. add PC440 220UF and for improve 1.6V output ripple.
		PEC-A-08	43	09/22	PU501	Change PU501 driver IC size from 2*2 to 2*2.
		PEC-A-09	43	09/22	PR508,PR525,PR533,PR534,PR551,PR550,PR566,PR558,PC509	Adjust VDDNB core load line(OCP/OTF) function.
		PEC-A-10	44	09/22	PR347,PC330,PC327,PR350	Adjust GFX core OCP function.
		PEC-A-11	44	09/22		Change GFX core power budget for ATI Seymour XT(15w).
		PEC-A-12	45	09/08	PU9	Change from MAINON to DGPU_1V_PG
		PEC-A-13	45	09/22	PR471	add pull high resistor PR471 for DGPU_1.8V_PG.
		PEC-A-14	44	09/26	PC341	Reduce 1pcs GFX core 7343 size output Cap for ATI Seymour XT(15w).
		PEC-A-15	43	09/26	PL502,PL503	Change VDD core choke footprint for SMT request.
		PEC-A-16	38	09/26	PQ26	Delete AQ4427 MOSFET from BOM source.
		PEC-A-17	38	09/29	PQ101,PR701,PQ251,PR65,PR60,PR26,PR66,PR3004,PR9005,	Adjust Battery discharge function.
		PEC-A-18	38	09/29	EL5	add charger input bead for EMI.
		PEC-A-19	37,38,39,40,41,42,45,46,	10/04	PC429,PC408,PC399,PC393,PC51,PC431,PC435,PC392,PC396,PC40,PC41,PC398,PC399,PC395,PC58,PC78,PC58,PC359,PC393,PC128,PC123	Change P/N from CH4104R9B03 to CH41002KB93.
		PEC-A-20	38	10/04	PD6,PD8,PD2,PD6,PD7,PD8002	Change P/N from BC1SS355Z07 to BC1SS355Z21.
		PEC-A-21	39	10/04	PC46	Change P/N from CH61001ME96 to CH6102K9A01.
		PEC-A-22	39	10/04	PC56,PC59	Change P/N from CH5472K9A02 to CH5472M9901.
		PEC-A-23	40,41,42,45,46	10/04	PC74,PC72,PC127,PC122,PC126,PC121,PC412,PC351,PC430,PC348,PC350,PC365,PC358,PC349,PC357,PC352,PC366	Change P/N from CH61001ME96 to CH6101M9905.
		PEC-A-24	42,45,46	10/04	PQ155,PQ91,PQ157	Change P/N from BA039040019 to BA039040040.
		PEC-A-25	44	10/04	PR360	Change P/N from CS37682FB00 to CS37672FB15.
		PEC-A-26	37,44,45,46	10/17	PQ123,PQ124,PQ125,PQ126,PQ139,PQ140,PQ82,PQ102,PQ101,PQ85,PQ116,PQ119,PQ88,PQ26,PQ87,PQ89,PQ84,PQ55	change to dual mosfet.
		PEC-A-27	44	10/20	PC327	POP for power request.
		PEC-B-01	38	11/18	PR64	Adjust Battery discharge function.
		PEC-B-02	38	11/22	PR35	Change footprint from RC0603 to RC1206.



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