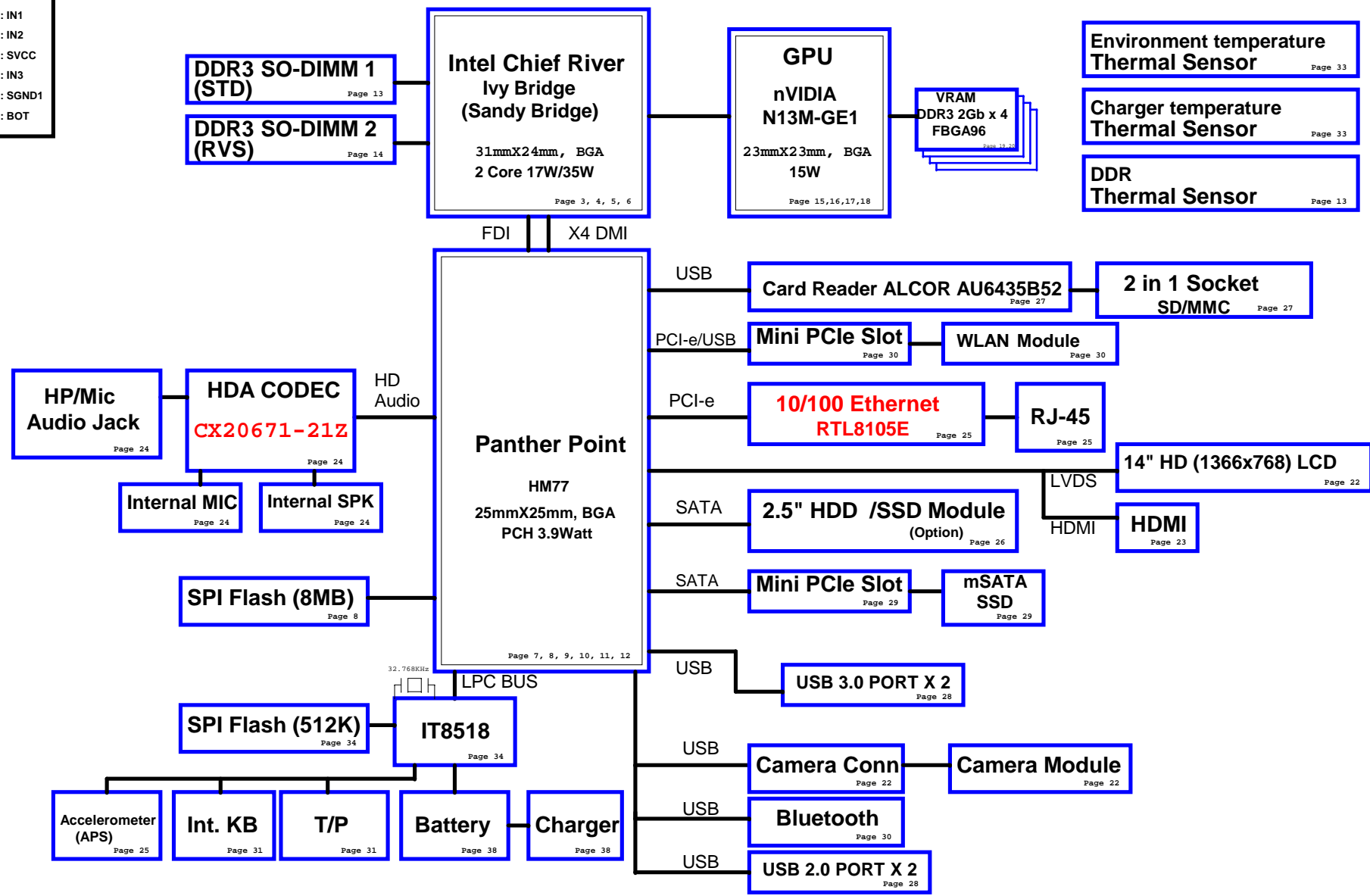


- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : SVCC
- LAYER 6 : IN3
- LAYER 7 : SGND1
- LAYER 8 : BOT

LZ8 14" Block Diagram -- Intel Chief River ULV



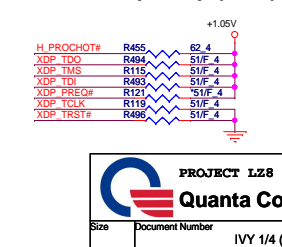
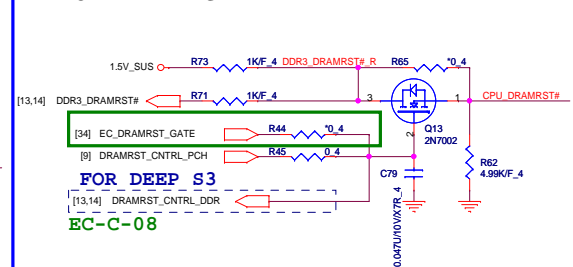
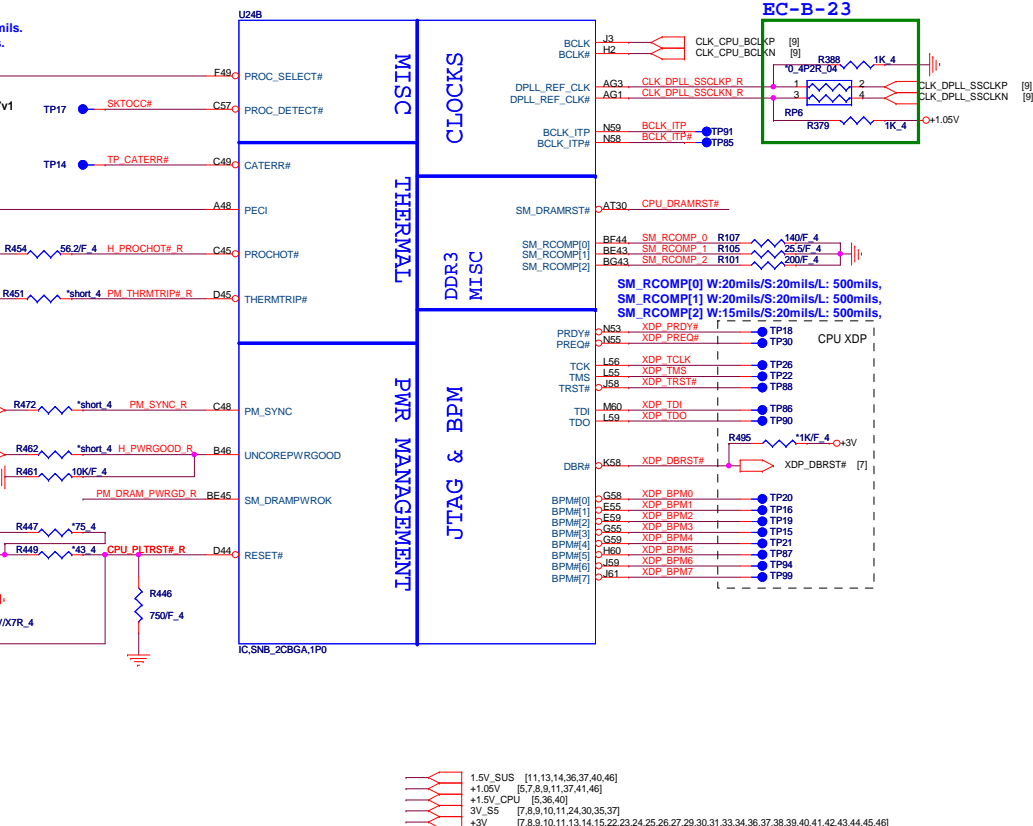
POWER	
DC/DC	3V_PCU, 5V_PCU, +15V Page 39
REGULATOR (DDR3)	1.5V_SUS, 0.75V_DDR_VTT Page 40
REGULATOR	1.05V Page 41
REGULATOR	VCCSA Page 42
CPU Core	Page 44
Charger	Page 38
RUN POWER SW/Discharge	5V_SUS, 3V_S5, 5V_S5 +3V, +5V Page 37
REGULATOR	1.8V Page 43
dGPU Core	Page 45,46

Table of Contents

PAGE	DESCRIPTION
01	BLOCK DIAGRAM
02	FRONT PAGE
03-06	IVY/Sandy Bridge
07-12	Panther/Cougar Point-PCH
13-14	DDR3 SO-DIMM
15-18	N13M
19-20	N13M VRAM
21	PS8622 LVDS converter
22	LCD/CAMERA
23	HDMI CONN
24	Audio Codec CX20672
25	LAN[RTL8105E]
26	SATA
27	Card Reader-AU6435B52-GDL
28	USB2.0 X2/USB3.0 X2
29	MINI Card (SSD)
30	WLAN/BT
31	KB/TP/LID
32	USB2.0--Audio Jack conn
33	FAN/Thermal
34	KBC IT8518
35	SW/LED
36	Screw Hole/EMI/ESD
37	Discharge
38	CHARGER (bq24725A)
39	3V/5V (TPS51123ARGER)
40	DDR3/0.75V (TPS51216)
41	1.05V_PCH(RT8240B)
42	VCCSA (RT8241A)
43	1.8V(TPS54318)
44	CPU(ISL95831)IMVP2+1
45	DGPU CORE(TPS51728)
46	GPU
47	
48	
49	
50	
51	

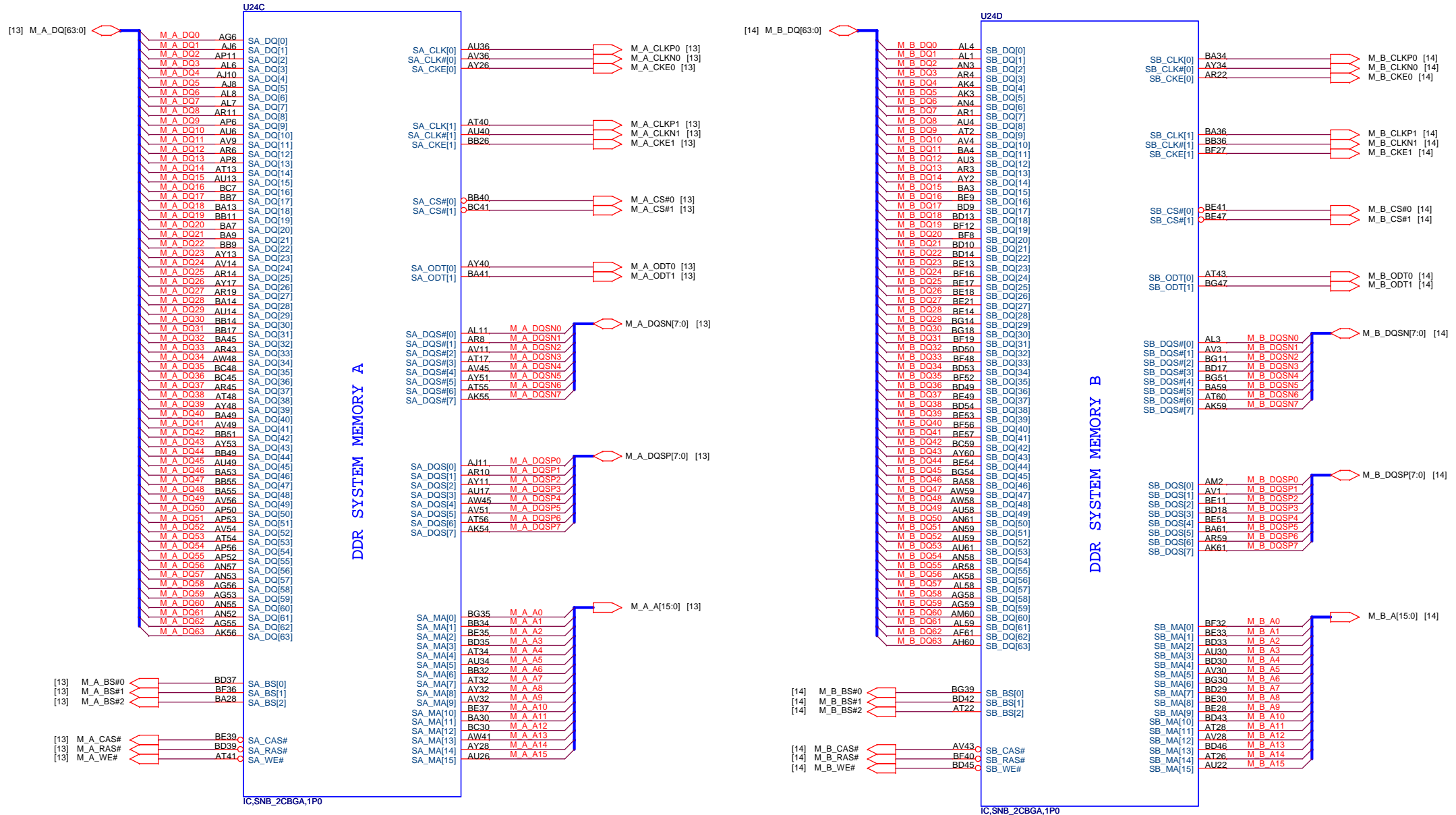
Power States

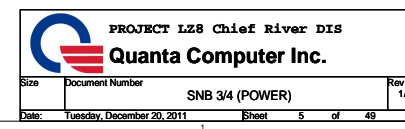
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	22,36,38,39,40,41,42,44,45	MAIN POWER		S0~S5
+3V_RTC	+3.0V~+3.3V	7,8,11,34	RTC		S0~S5
3VPCU	+3.3V	7,8,22,23,25,30,31,34,35,36,37,38,39,43,45	IT8518/19 POWER	3V5V_EN	S0~S5
5VPCU	+5V	22,36,37,39,40,41,42,43,44,45,46	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
15V	+15V	22,37,39,40,46	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	25,37	LAN POWER	LAN_ON	
5V_S5	+5V	11,24,28,32,37	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	3,7,8,9,10,11,30,35,37,45	Sys Management,PCH Resume Well, USB,WLAN,WiMAX POWER	S5_ON	S0~S3
1.5V_SUS	+1.5V	3,11,13,14,36,37,40,46	DDR3 SODIMM POWER	SUSON	S0~S3
+0.75V_DDR_VTT	+0.75V	13,14,37,40	DDR3 SODIMM REFERENCE POWER	MAINON	S0
+5V	+5V	7,8,11,22,23,24,26,31,33,36,37,38	SLP_S3# CTRLD POWER	MAINON	S0
+3V	+3.3V	3,7,8,9,10,11,13,14,15,21,22,23,24,25,26,27,29,30,31,33,34,35,36,37,38,39,40,41,42,43,44,45,46	SLP_S3# CTRLD POWER	MAINON	S0
VCC_GFX		5,36,44	VGA CORE POWER	MAINON	S0
VCCSA	+0.8V~+0.9V	5,37,42	Sandy Bridge Power	MAINON	S0
+1.8V	+1.8V	5,8,11,37,43	LVDS,NVM POWER	MAINON	S0
+1.05V	+1.05V	3,5,7,8,9,11,21,36,37,41,46	Sandy Bridge VTT POWER/PCH CORE POWER	MAINON	S0
VCC_CORE		5,6,36,44	CPU CORE POWER	VRON	S0
+LCDVCC	+3.3V	22	LCD Power	ENVDD	S0
+3V_HDD	+3V	26	ODD Power	ODD_5V_ON	S0
+5V_HDD	+5V	26	HDD Power	MAINON#	S0
BAT-V	+10V~+17V	38	MAIN BATTERY	CHG_PBATT	S0~S5
+1.5V_CPU	+1.5V	3,5,36	DDR3 1.5V Rails	PS_S3CNTRL	S0



Ivy/Sandy Bridge Processor (DDR3)

04

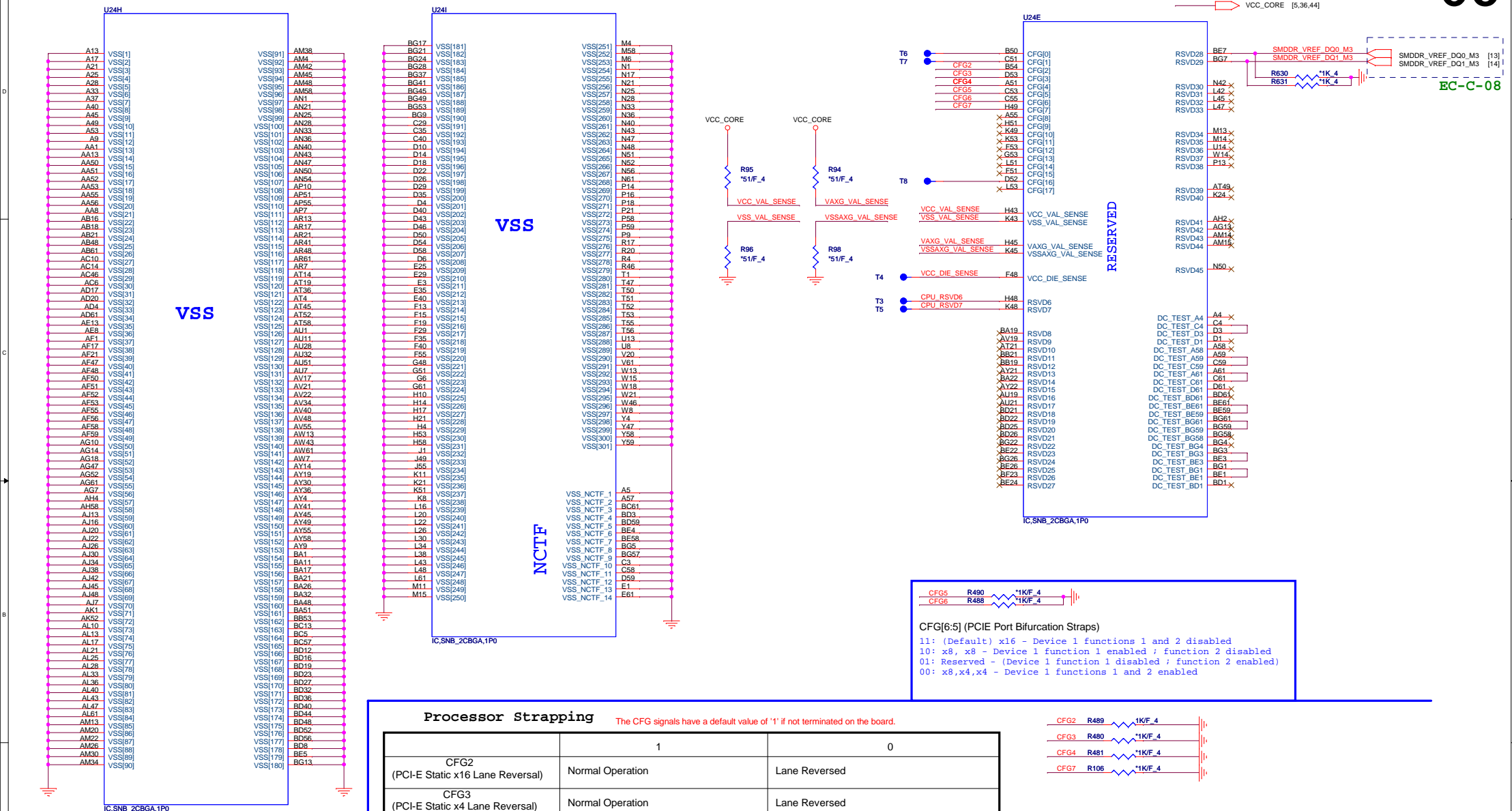




Sandy Bridge Processor (GND)

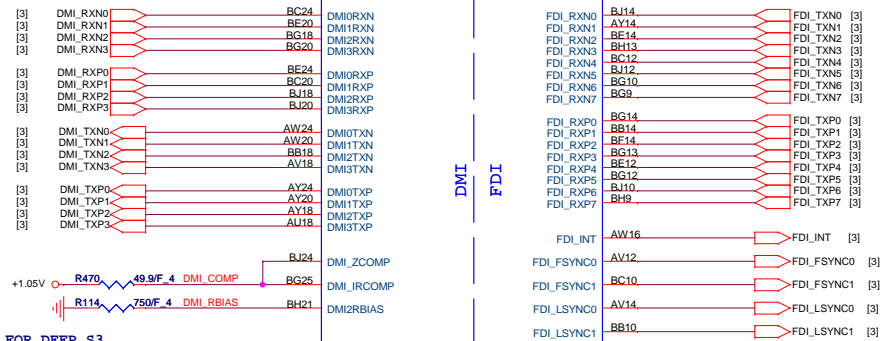
Sandy Bridge Processor (RESERVED, CFG)

06



Panther/Cougar Point (DMI,FDI,PM)

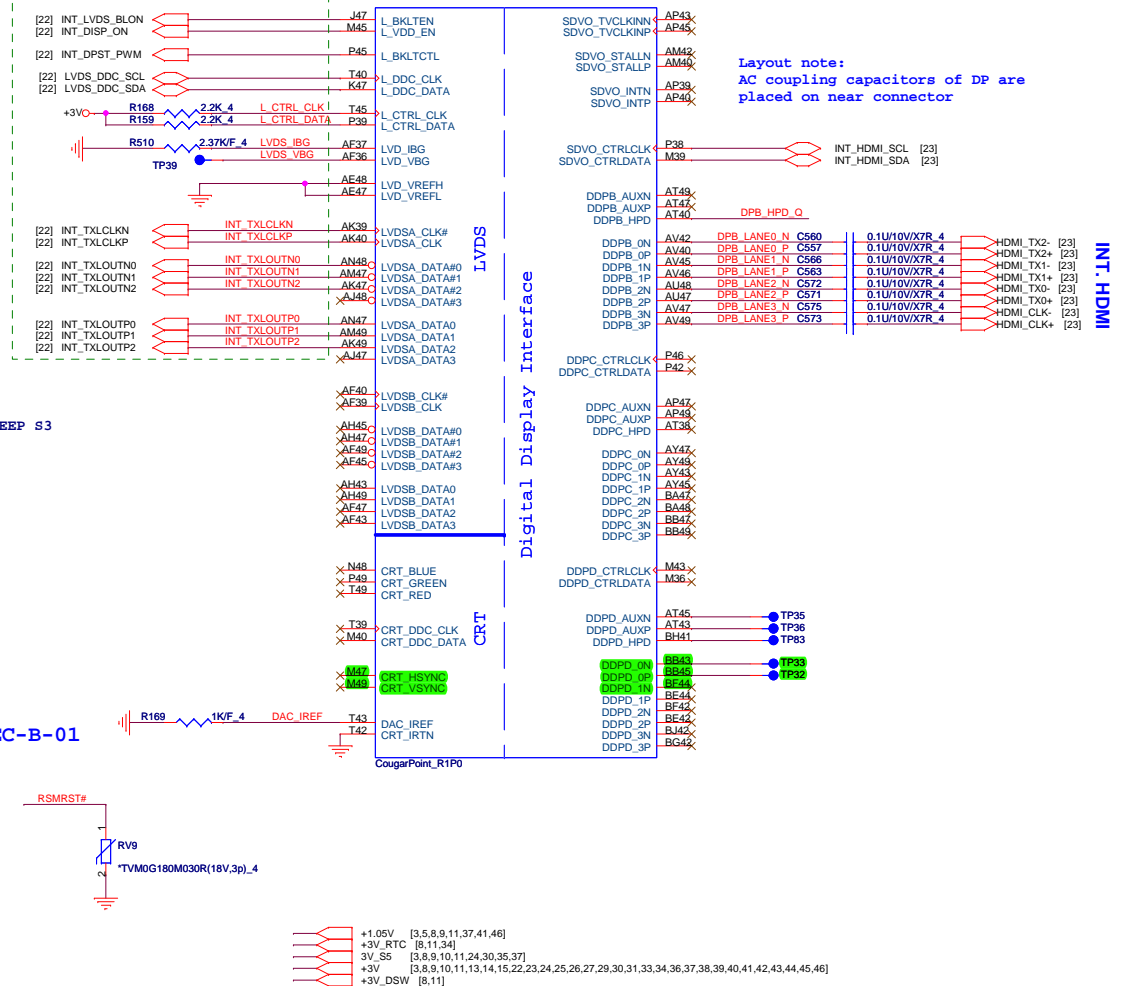
U32C



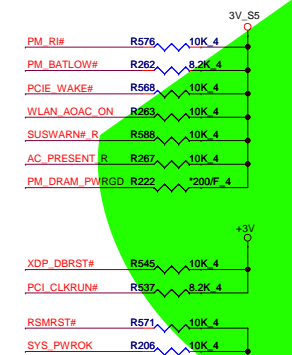
EC-B-23

Panther/Cougar Point (LVDS,DDI)

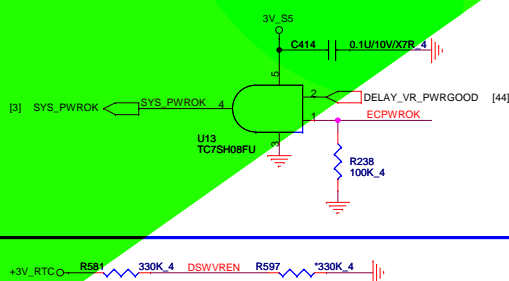
U32D



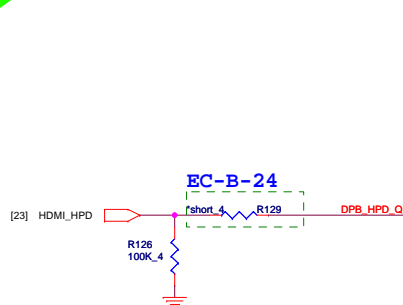
PCH Pull-high/low(CLG)



System PWR_OK(CLG)



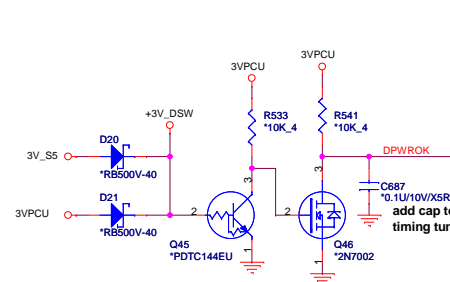
INT HDMI DETECT



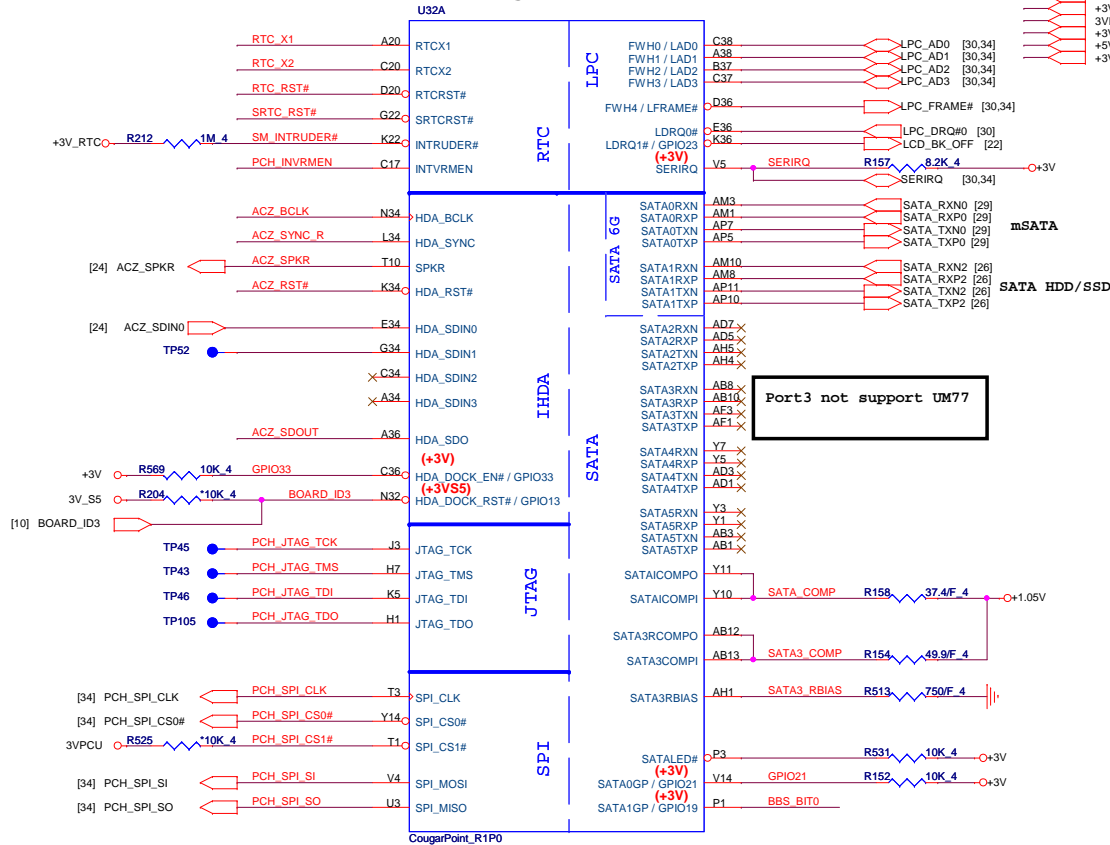
LVDS for HM76



DPWROK FOR DSW (DEEP S3)



Panther/Cougar Point (HDA,JTAG,SATA)



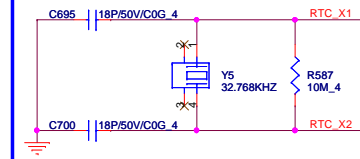
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR <div>Different from Calpella</div>	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
HDA_SDO	Flash Descriptor Security Only for Interposer	PWROK	0 = effective(Default: weak pull down) 1 = Override										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>0</td><td>SPI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table>	GNT1#	GNT0#	Boot Location	1	0	SPI	0	0	LPC	[Need external pull-down for LPC BIOS]
GNT1#	GNT0#	Boot Location											
1	0	SPI											
0	0	LPC											
GPIO19 <div>Different from Calpella</div>	Boot BIOS Selection 0 [bit-0]	PWROK											
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
DF_TVS	DMI Termination voltage	PWROK	weak pull-down 20kohm										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite		Low = Disable (Default) High = Enable										
GPIO28 <div>Different from Calpella</div>	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
DSWVREN	0: disable 1: enable												

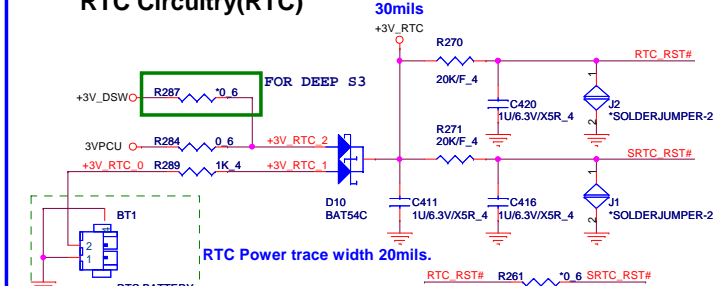
if default boot destination is SPI,
no external pull-up/-down resistors on the board are necessary

RTC Clock 32.768KHz

08



RTC Circuitry(RTC)

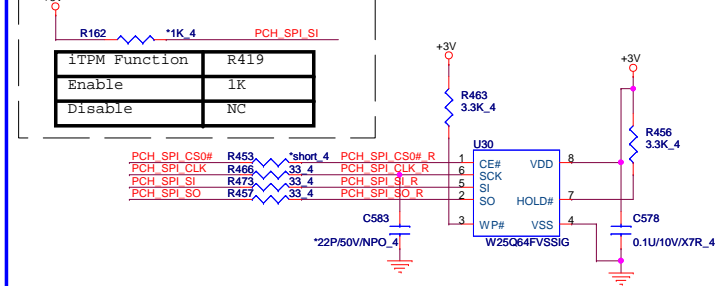


W25Q64CVSSIG: AKE3EFP0N04
MX25L6406EM2I-12G: AKE3NFP0Z00
EN25Q64-104HIP: AKE3EFN0Q00

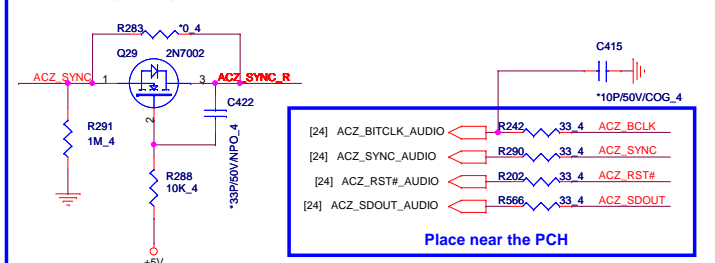
PCH Dual SPL

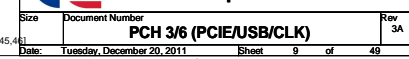
64Mbit (8M Byte), SPI

iTPM ENABLE/DISABLE

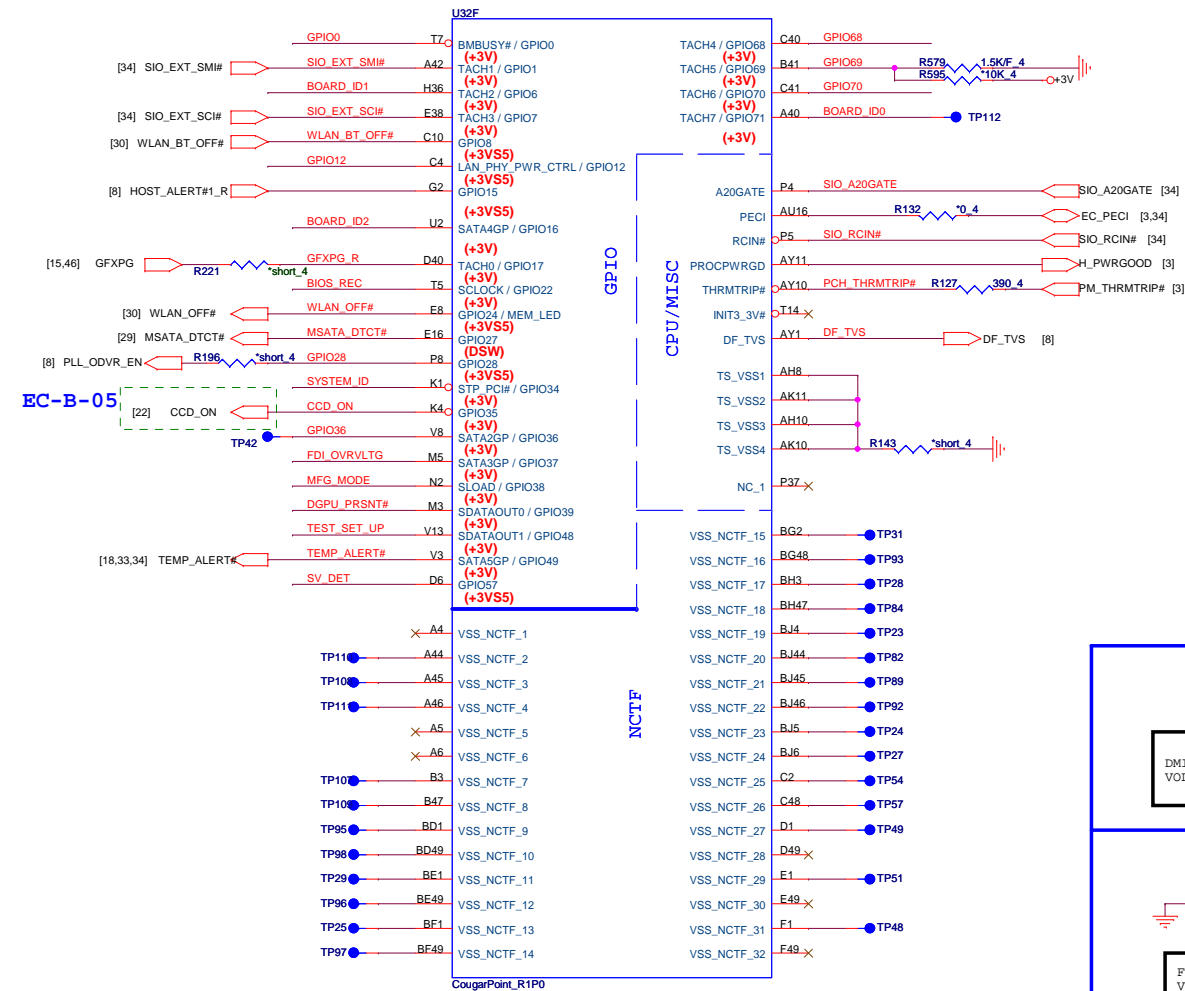


HDA Bus(CLG)





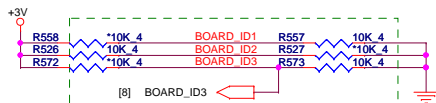
Panther/Cougar Point (GPIO,VSS_NCTF,RSVD)



BOARD ID SETTING

Board ID For Function	ID1 GPIO6	ID2 GPIO16	ID3 GPIO13
SDV	0	0	0
SIV	0	0	1
SIT	0	1	0
SVT			
SOVP			

	SYSTEM_ID
L27	0
L28	1

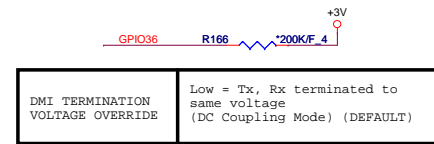
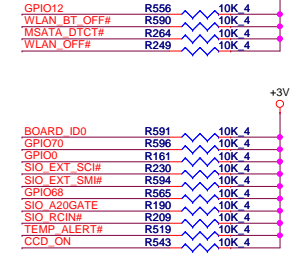


EC-B-04
EC-C-02

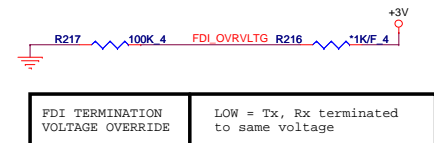
3V_S5 +3V [3,7,8,9,11,24,30,35,37]
[3,7,8,9,11,13,14,15,22,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]

10

GPIO Pull-up/Pull-down(CLG)



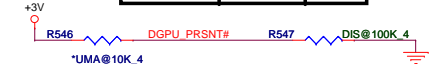
SV_SET_UP
High = Strong (Default)



MFG-TEST



	Optimus	UMA
Stuff	R547	R546
No Stuff	R546	R547

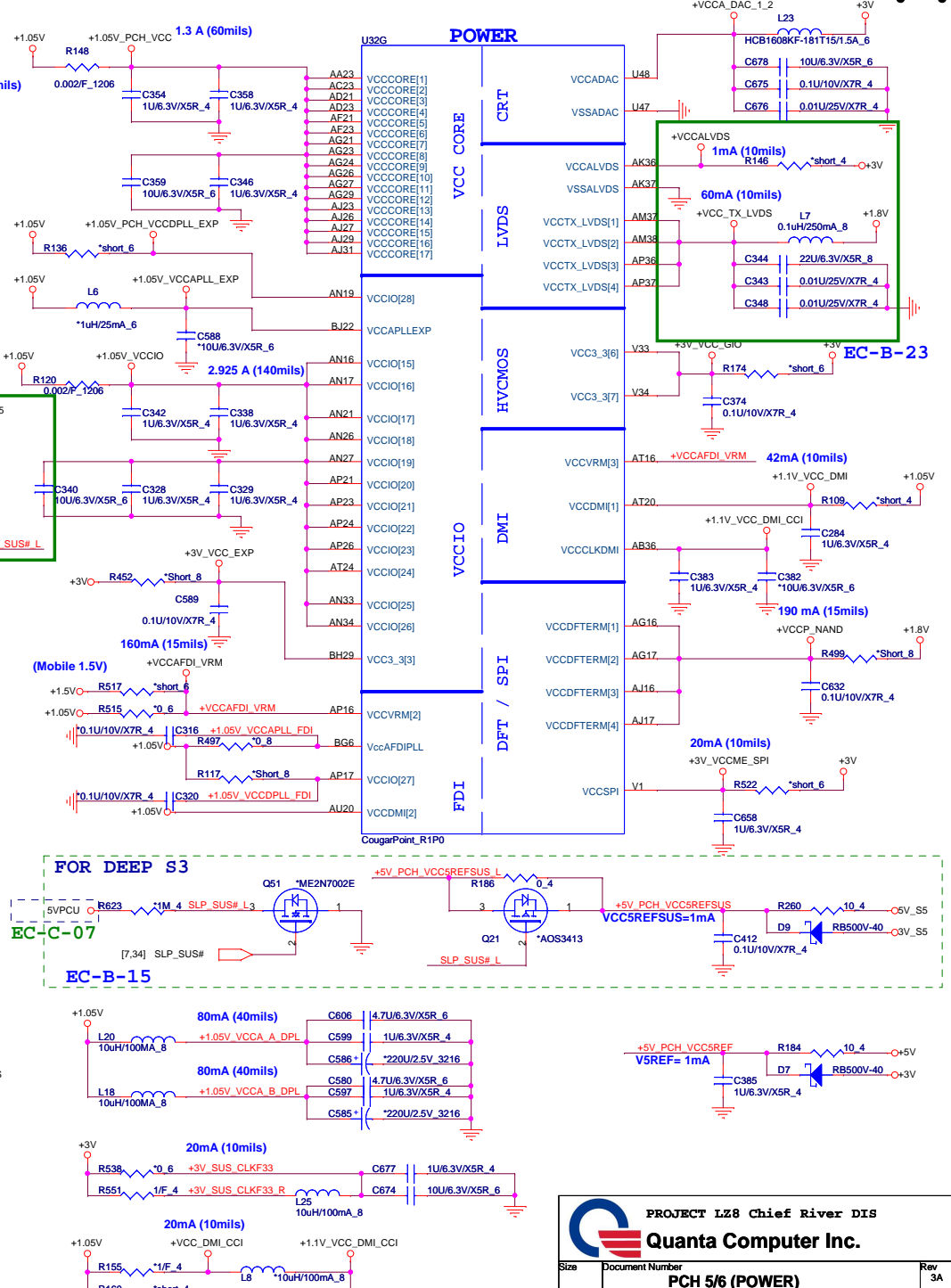


BIOS RECOVERY
High = Disable (Default)
Low = Enable

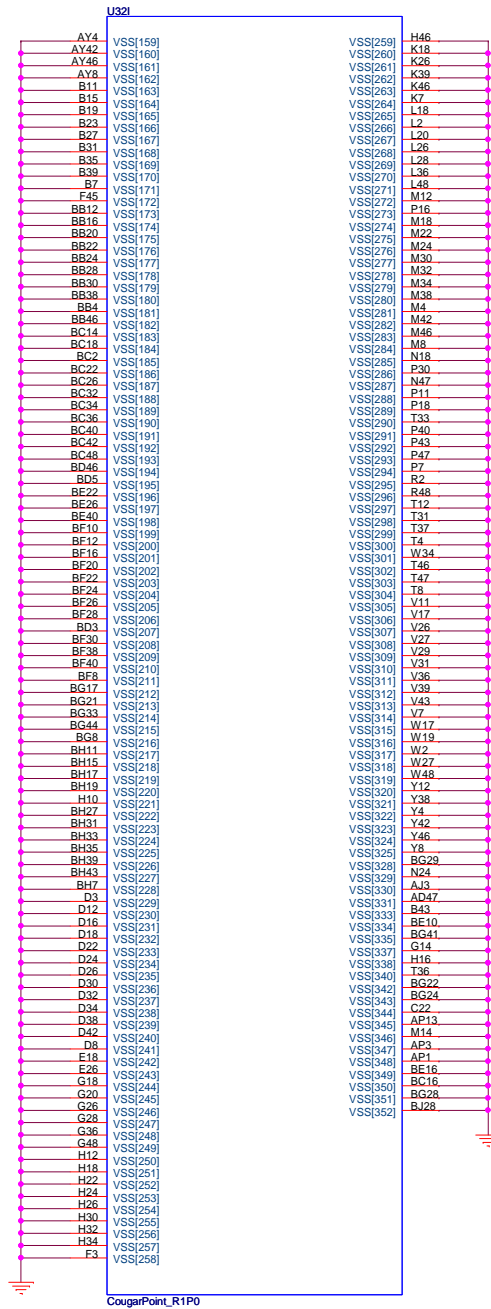
PROJECT L28 Chief River DIS
Quanta Computer Inc.

Panther/COUGAR POINT (POWER)

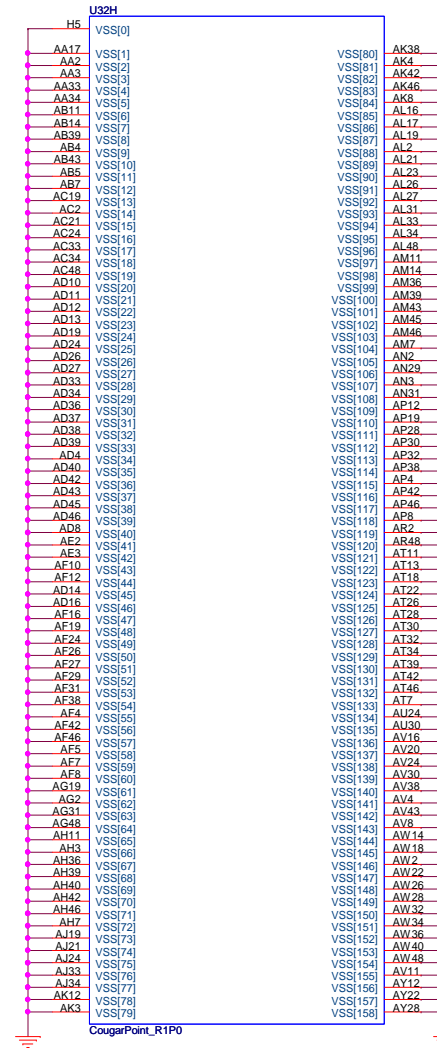
11

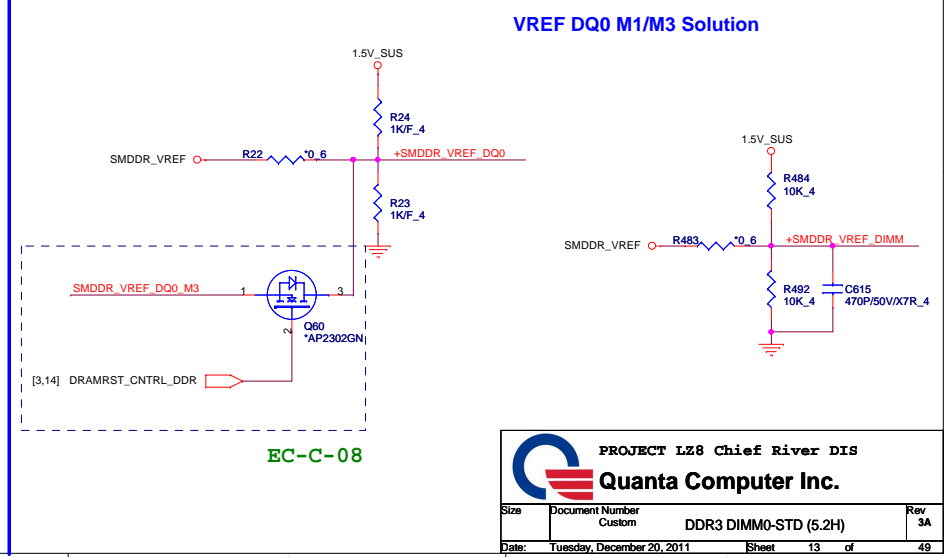
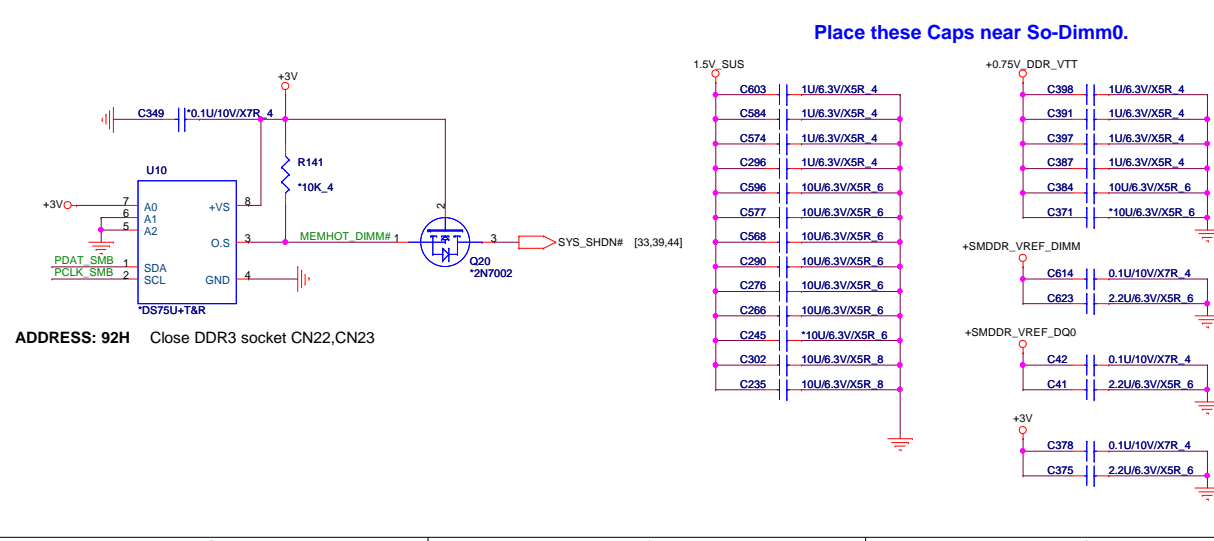
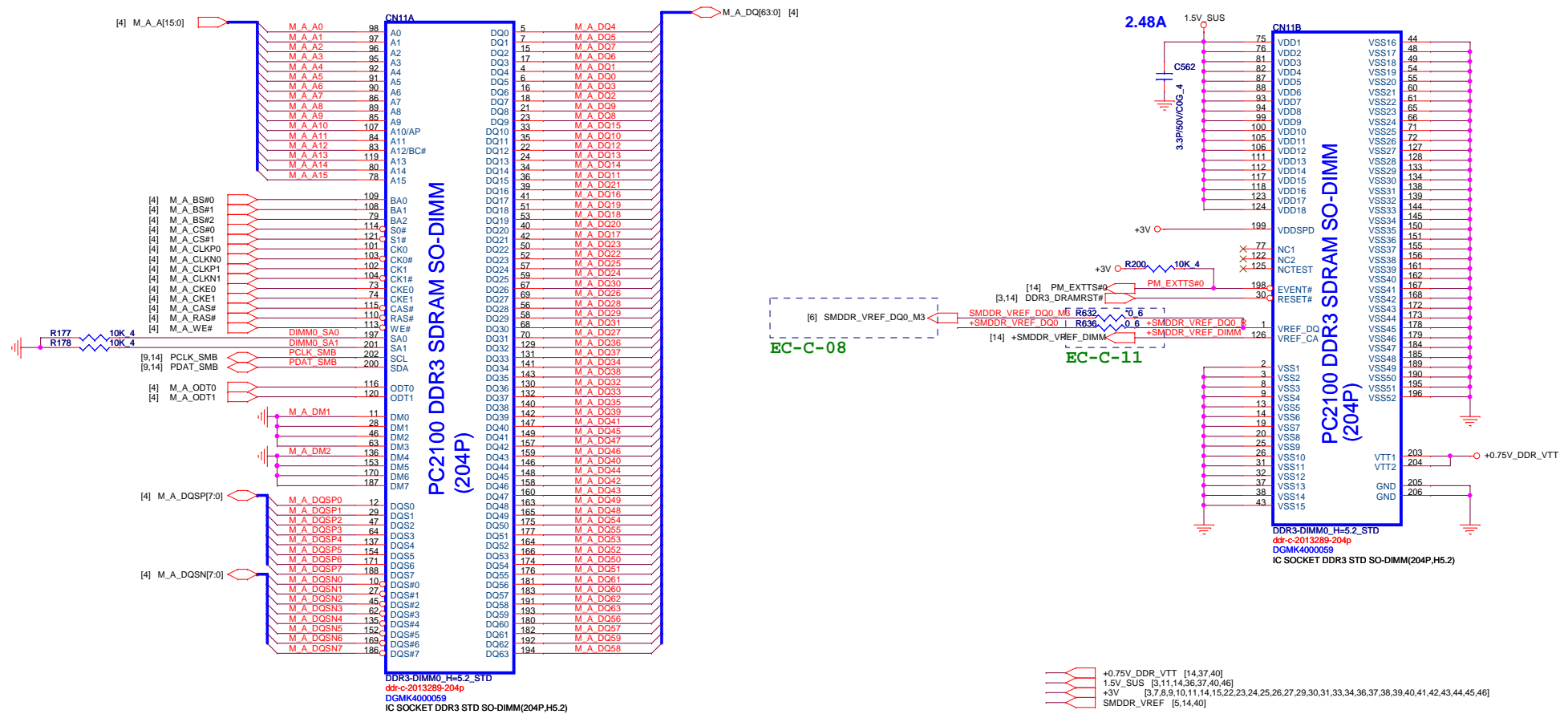


Panther/Cougar Point-M (GND)




Panther/Cougar Point-M (GND)





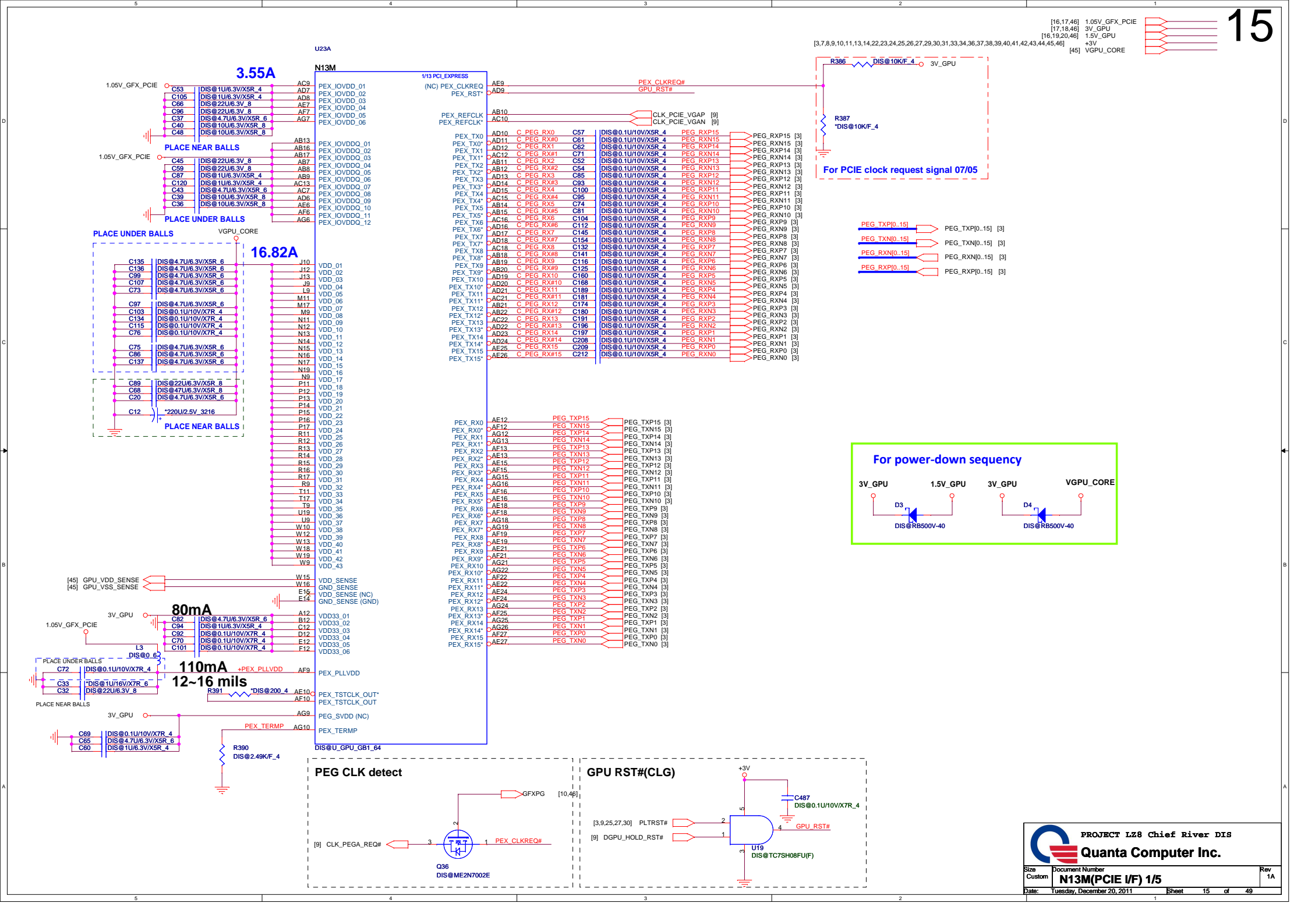


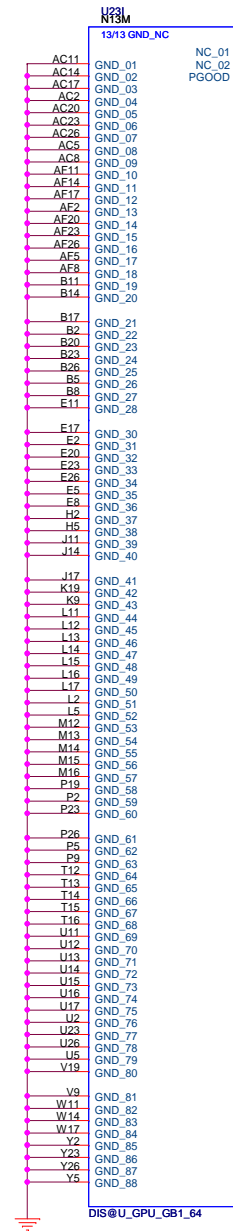

PROJECT LZ8 Chief River DIS
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Size	Document Number	Rev
	Custom	3



DDR3 DIMM1-RVS (4.0H)



Date:	Tuesday, December 20, 2011	Sheet	14	of	49
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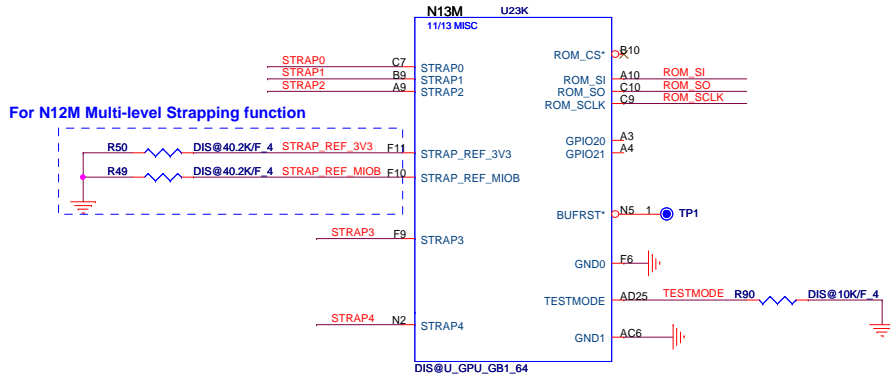
[19,20] VMA_DQ[63..0]  

[19,20] VMA_DM[7..0]  

[19,20] VMA_WDQS[7..0]  

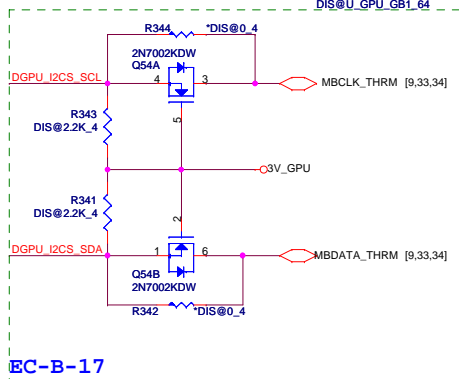
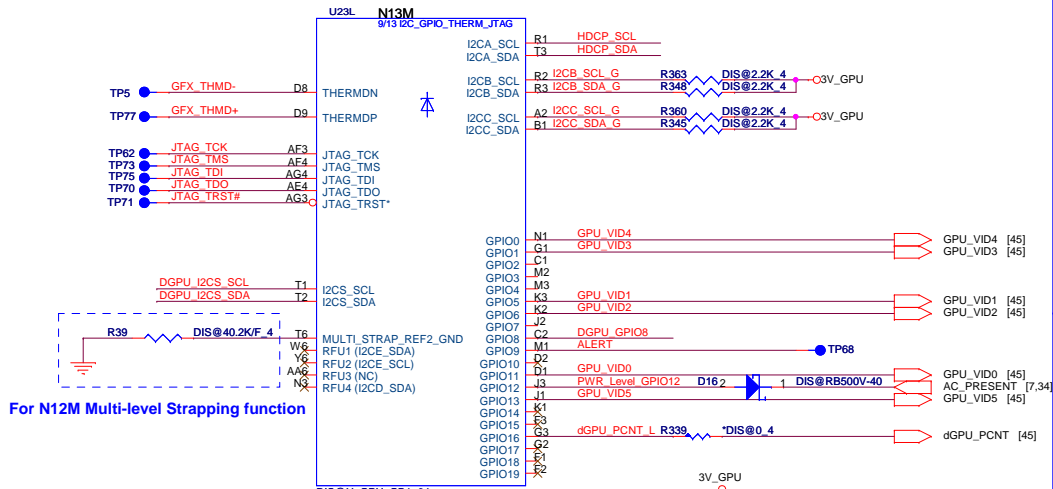
[19,20] VMA_RDQS[7..0]  

[19,20] FBA_CMD[30..0]  



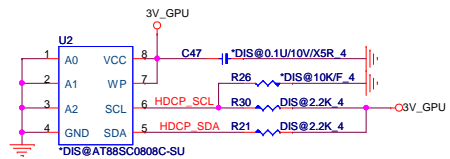
9.5 Unused I2C Pins

For unused dedicated (non-AUX) I2C pins, pull-up both the I2C_SCL, I2C_SDA, to 3.3 V using 2.2 kΩ resistors routing.



EC-B-17

HDCP ROM



DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

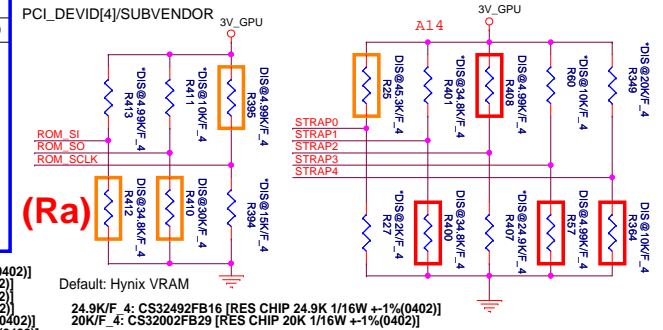
nV FAE suggest that the device ID for N13M-GE1 is 0x1058

N13M-GE1

Logical Strap Bit Mapping

Rv	PU-VDD	PD-GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

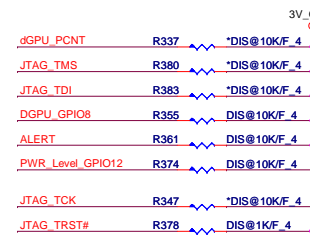
4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1% (0402)]
10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30K/F 4: CS33002FB13 [RES CHIP 30K 1/16W +1% (0402)]
34.8K/F 4: CS33482FB22 [RES CHIP 34.8K 1/16W +1% (0402)]
45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1% (0402)]



	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO N13M-GE1	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	0101
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V	0001

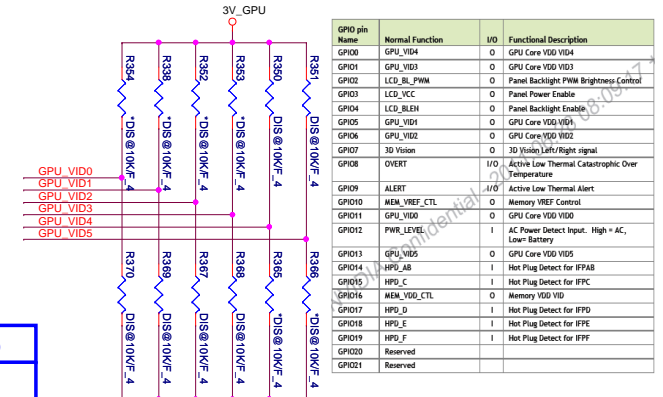
VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000	Reserved	Reserved	Reserved	Reserved
0001	Reserved	Reserved	Reserved	Reserved
0010	Reserved	Reserved	Reserved	Reserved
0011	Reserved	Reserved	Reserved	Reserved
0100	Reserved	Reserved	Reserved	Reserved
0101	Reserved	Reserved	Reserved	Reserved
0110	Reserved	Reserved	Reserved	Reserved
0111	DDR3 128Mx16x4, 64bit, 1GB, 900MHz DDR3 128Mx16x4, 64bit, 1GB, 900MHz	Hynix Samsung	H5TQ2G63BFR-11C K4W2G1646C-HC11	PD 34.8K/F PD 45.3K/F



NVDD Table

N13M-GE1 (GF119)	NVDD (0.875V)
GPU_VID0	0 (R370)
GPU_VID1	0 (R369)
GPU_VID2	0 (R367)
GPU_VID3	0 (R368)
GPU_VID4	1 (R350)
GPU_VID5	1 (R351)



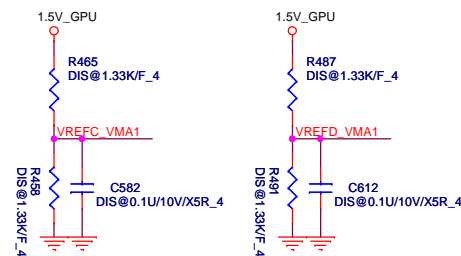
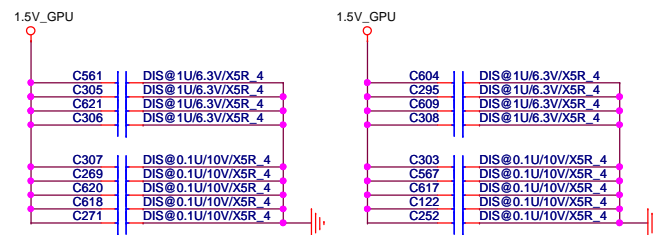
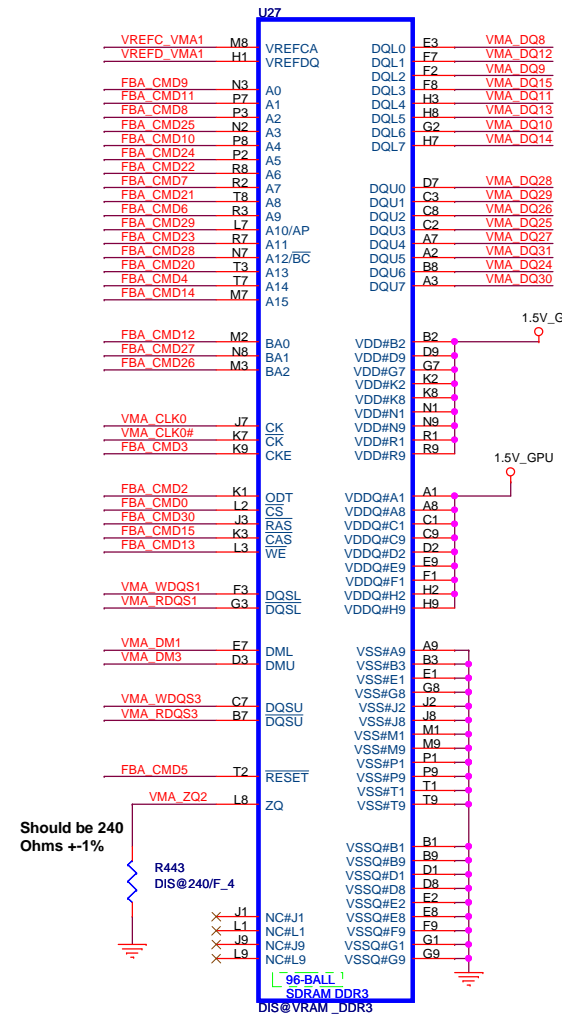
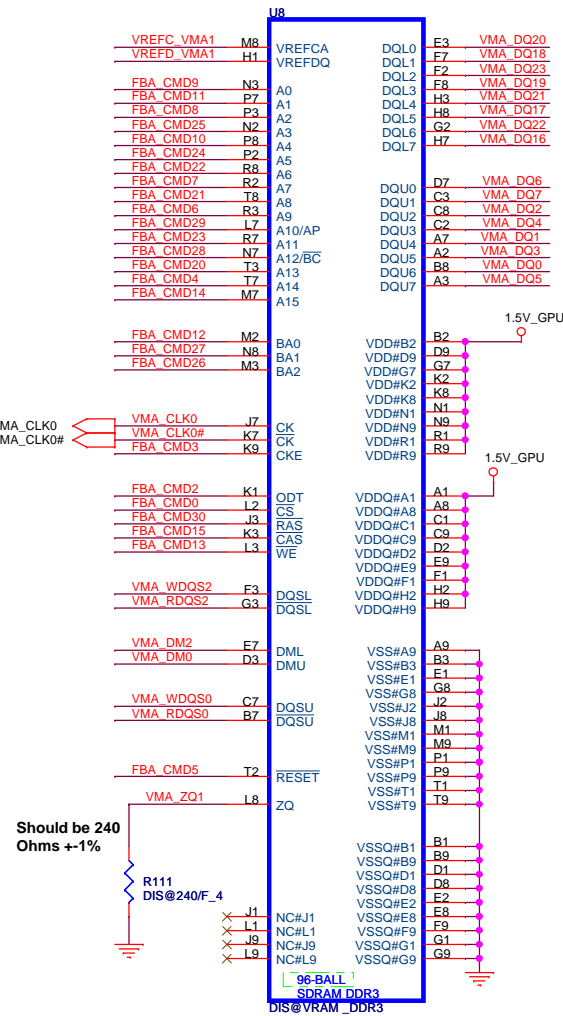
GPIO pin Name	Normal Function	I/O	Functional Description
GPIO0	GPU_VID4	O	GPU Core VDD VDD4
GPIO1	GPU_VID3	O	GPU Core VDD VDD3
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control
GPIO3	LCD_VCC	O	Panel Power Enable
GPIO4	LCD_BL_EN	O	Panel Backlight Enable
GPIO5	GPU_VID0	O	GPU Core VDD VDD0
GPIO6	GPU_VID2	O	GPU Core VDD VDD2
GPIO7	3D Vision Left/Right signal	O	3D Vision Left/Right signal
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VID5	O	GPU Core VDD VDD5
GPIO12	PWR_LEVEL	I	AC Power Detect Input. High = AC, Low = Battery
GPIO13	GPU_VID5	O	GPU Core VDD VDD5
GPIO14	HPO_AB	I	Hot Plug Detect for HPAB
GPIO15	HPO_C	I	Hot Plug Detect for HPC
GPIO16	MEM_VDD_CTL	O	Memory VDD VDD
GPIO17	HPO_D	I	Hot Plug Detect for HPD
GPIO18	HPO_E	I	Hot Plug Detect for HPE
GPIO19	HPO_F	I	Hot Plug Detect for HFF
GPIO20	Reserved		
GPIO21	Reserved		

PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

CHANNEL A: 1024MB DDR3

[15,16,20,46] 1.5V_GPU

19

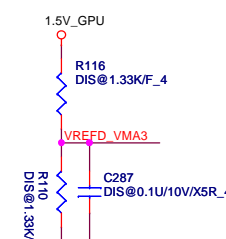
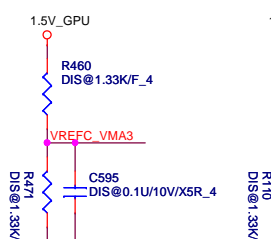
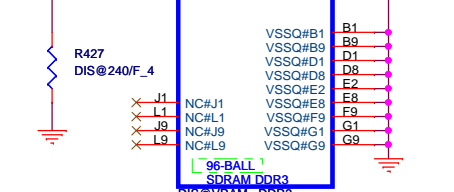
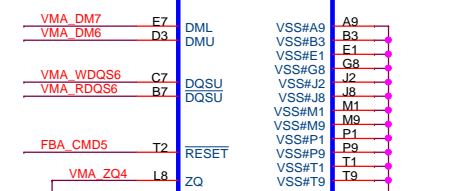
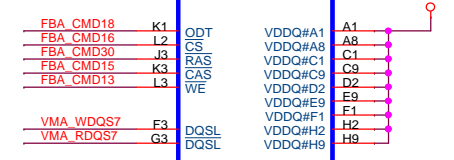
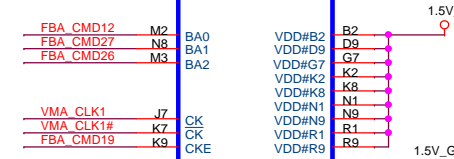
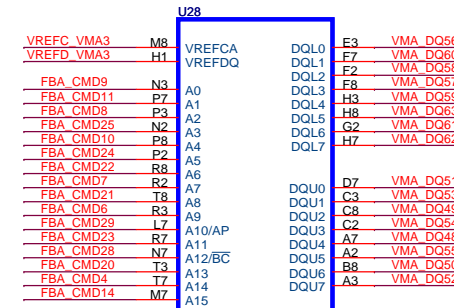
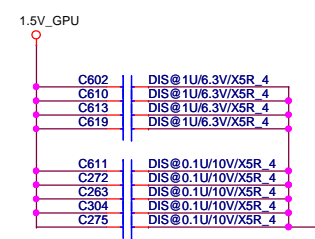
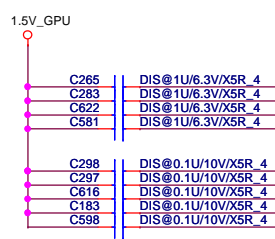
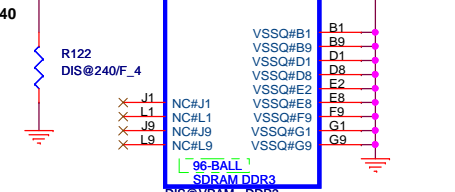
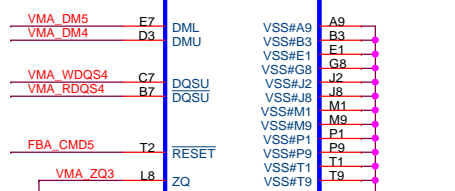
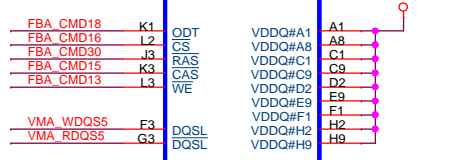
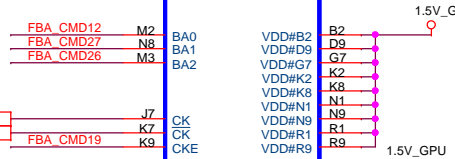
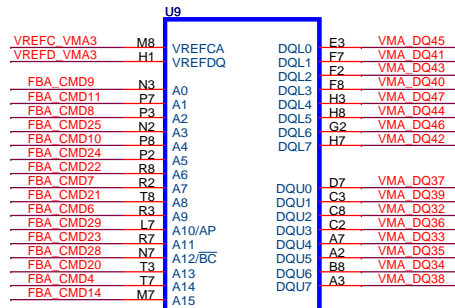


CHANNEL A: 1024MB DDR3

[15,16,19,46] 1.5V_GPU

20

[16,19] VMA_DQ[63..0]
[16,19] VMA_DM[7..0]
[16,19] FBA_CMD[30..0]
[16,19] VMA_RDQS[7..0]



D

D

C

C

B

B

A

A



PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size

Custom

Document Number

Blank

Rev

1A

Date:

Friday, November 11, 2011

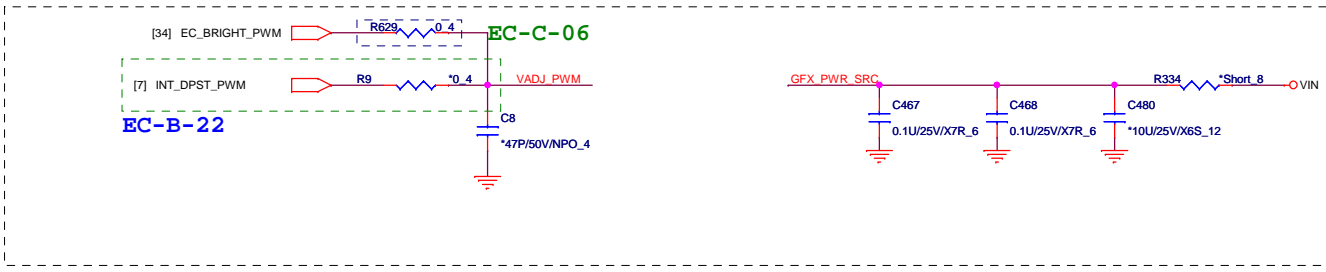
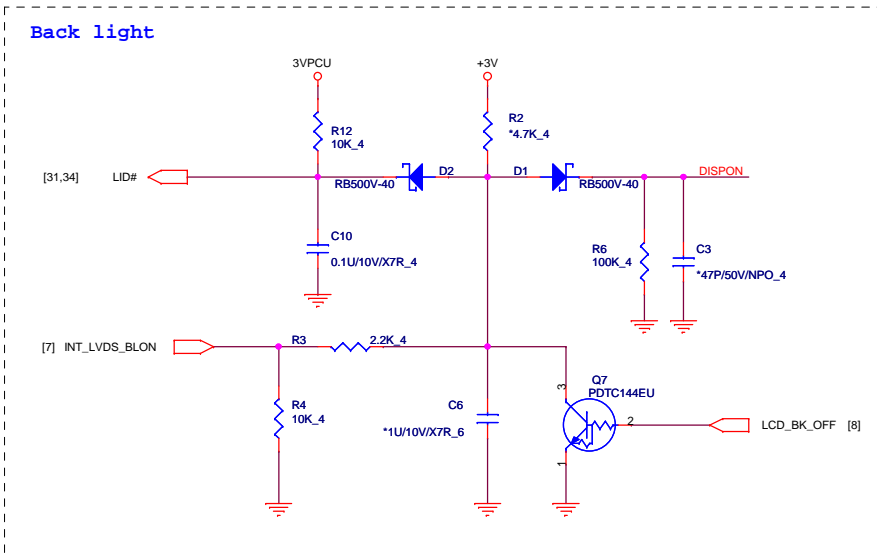
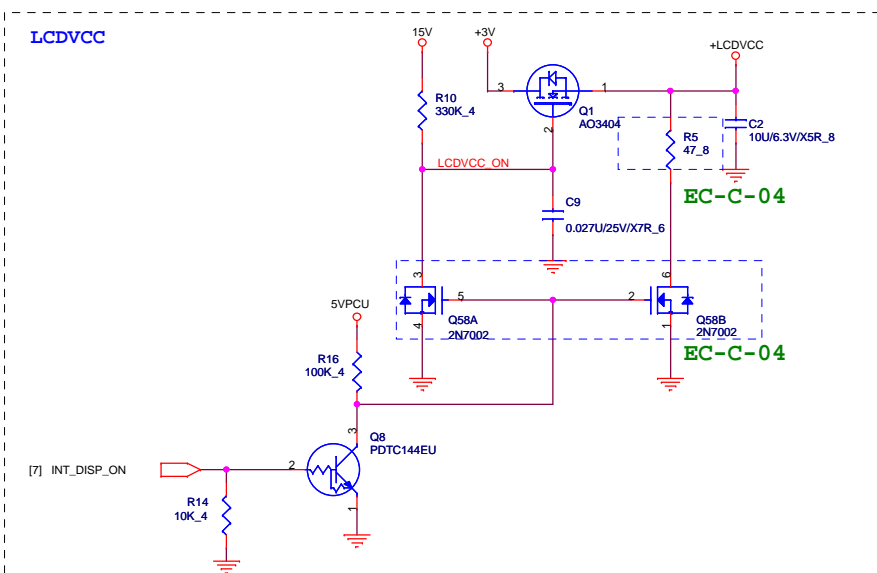
Sheet

21

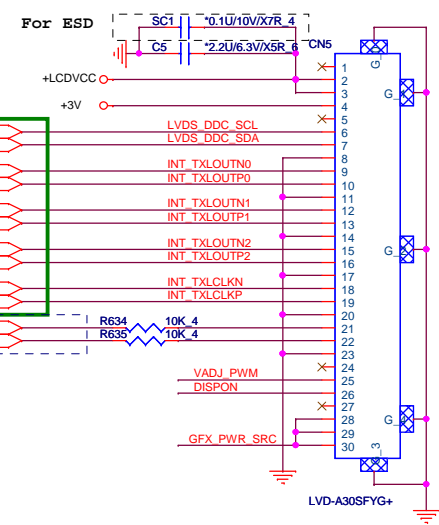
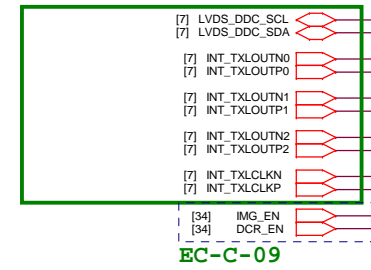
of

49

+3V	[3,7,8,9,10,11,13,14,15,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]
3VPCU	[7,8,25,30,31,34,35,36,37,38,39,43,45]
15V	[37,39,40,46]
VIN	[36,38,39,40,41,42,44,45]
5VPCU	[11,36,37,39,40,41,42,43,44,45,46]

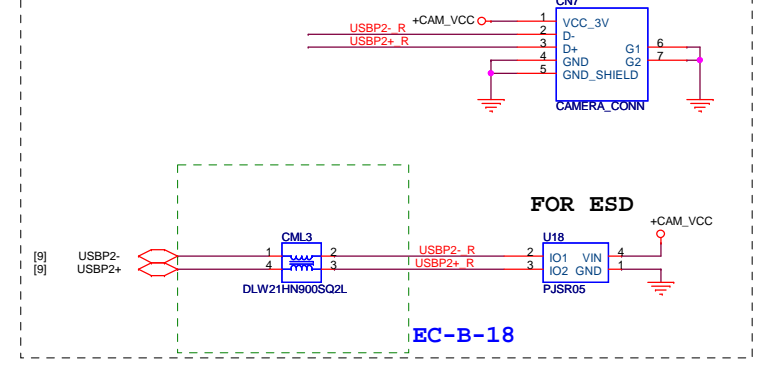


EC-B-22

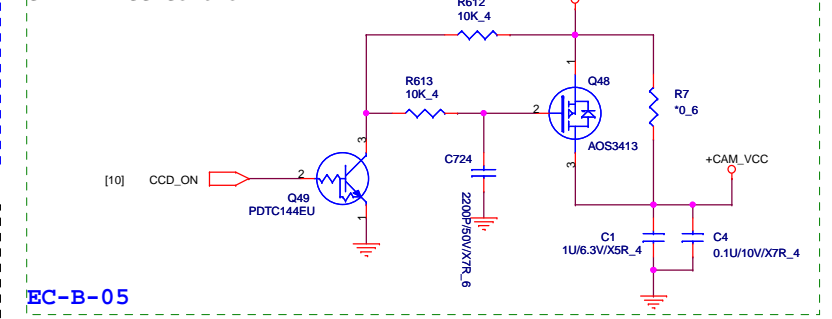


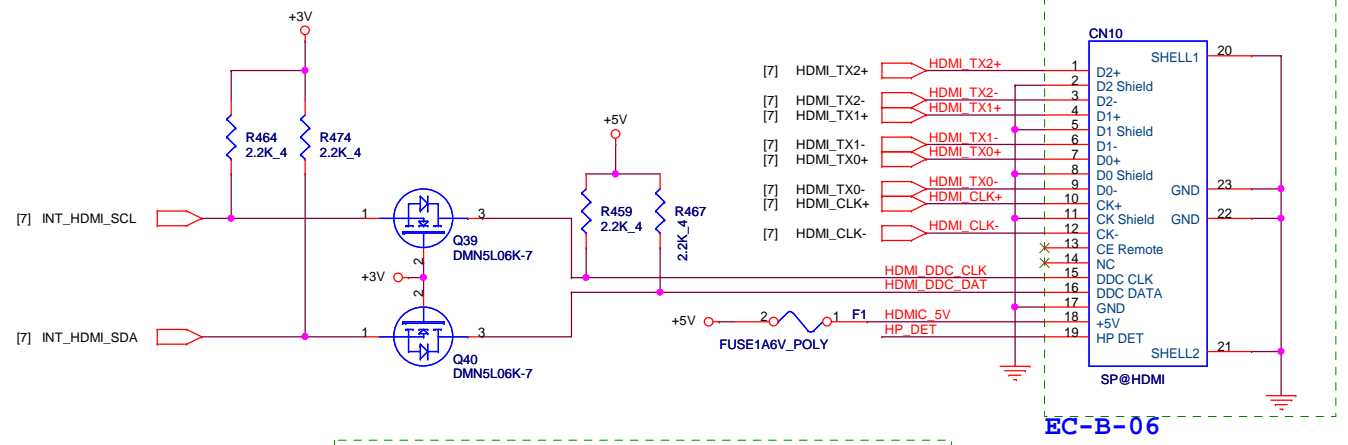
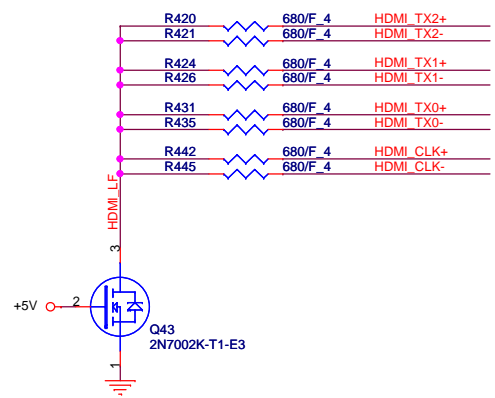
LVDS (14")
(1024x600,
1366x768)

CAMERA CONN

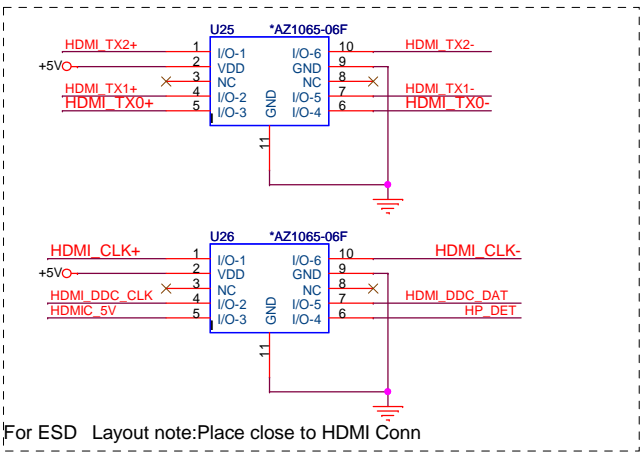


CAMERA VCC Control

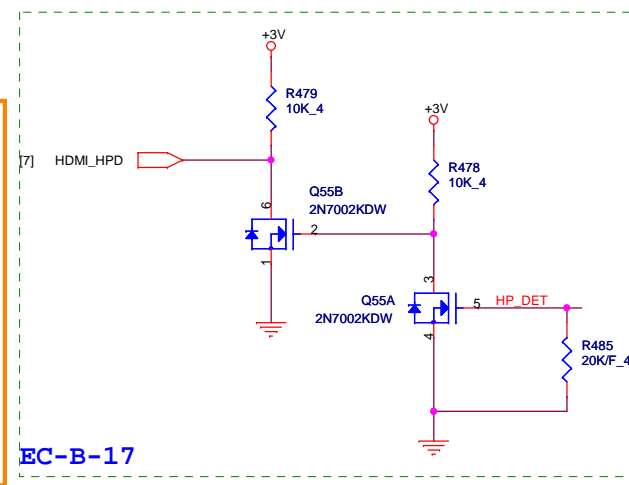
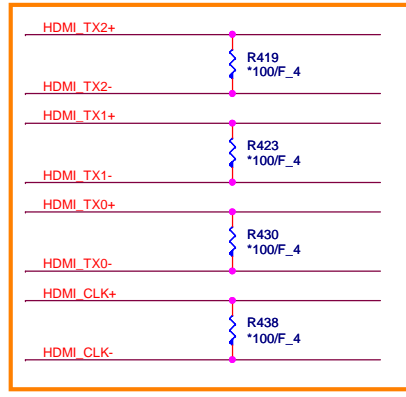




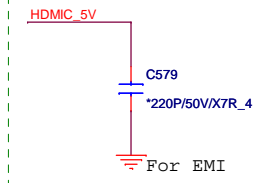
EC-B-06



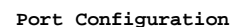
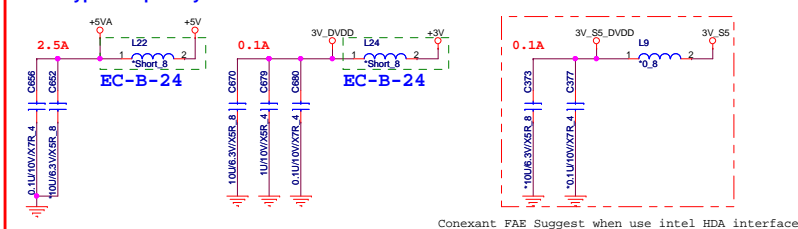
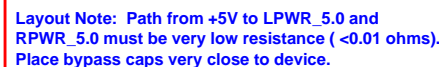
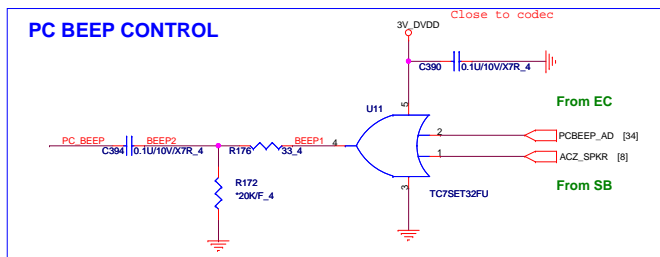
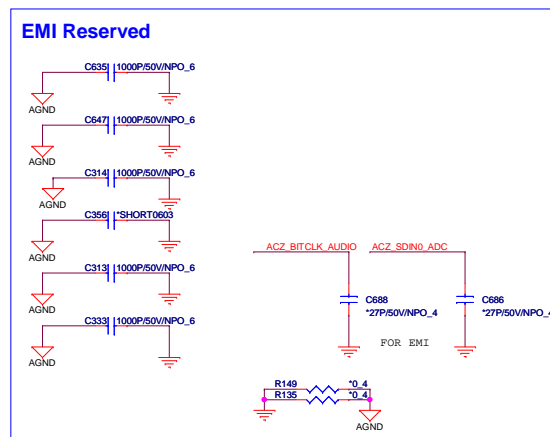
EMI reserve for HDMI

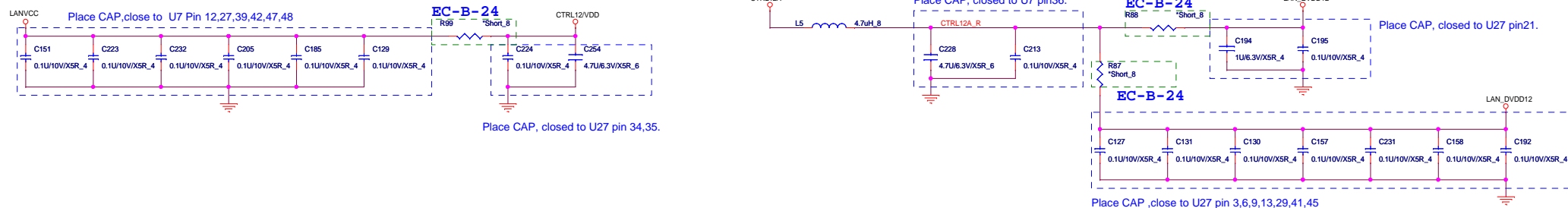
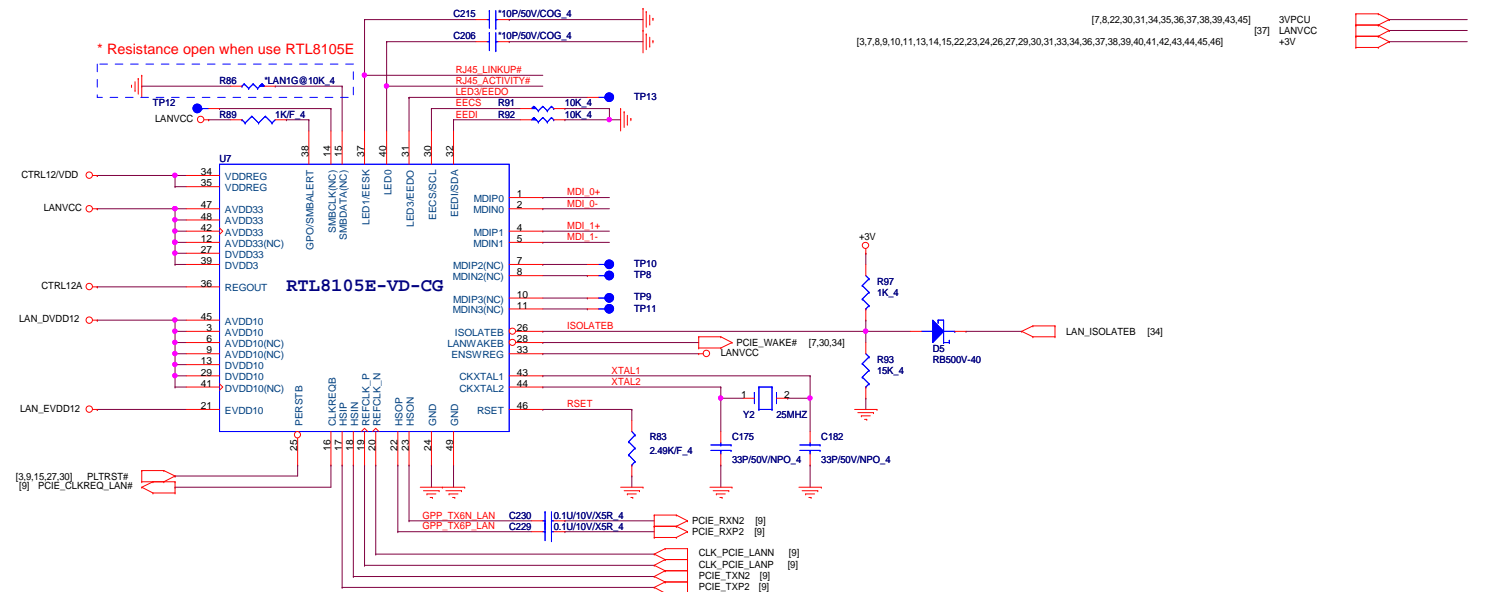


EC-B-17



AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

[illegible]



Transformer

MDI 0- R59 1/F.4
MDI 0+ R67 1/F.4

MDI 1- R53 1/F.4
MDI 1+ R55 1/F.4

Layout:
All termination signal
should have 20 mil trace

EC-C-05

close to transformer(U5)

MDI 1- C80 *5P10V/XSR_4
MDI 0+ C106 *5P10V/XSR_4
MDI 0- C98 *5P10V/XSR_4
MDI 1+ C91 *5P10V/XSR_4

Reserve for GO-TO Rural
Line to Line TVS

U4
UCLAMP2512T.TCT

U5
NS0013LF

TX- 9 LAN_MX0-
TD+ 10 LAN_MX0+
CT 11 LAN_MCT0
NC 12
NC 13
NC 14
CT 15 LAN_MX1-
RD+ 16 LAN_MX1+
RX- 17

R415 75/F.8 LANCT3
R409 75/F.8

Layout:
All termination signal
should have 20 mil trace

Reserve for GO-TO Rural
Surge Suppressor

R416 1M.8
C820 10P5KV/XTR_1008
R418 1/F.8
D18 SS3500N-C

The diagram illustrates the internal circuitry of an RJ45 connector, showing the connection between the external LAN pins and the internal ICs (U21 and U22).

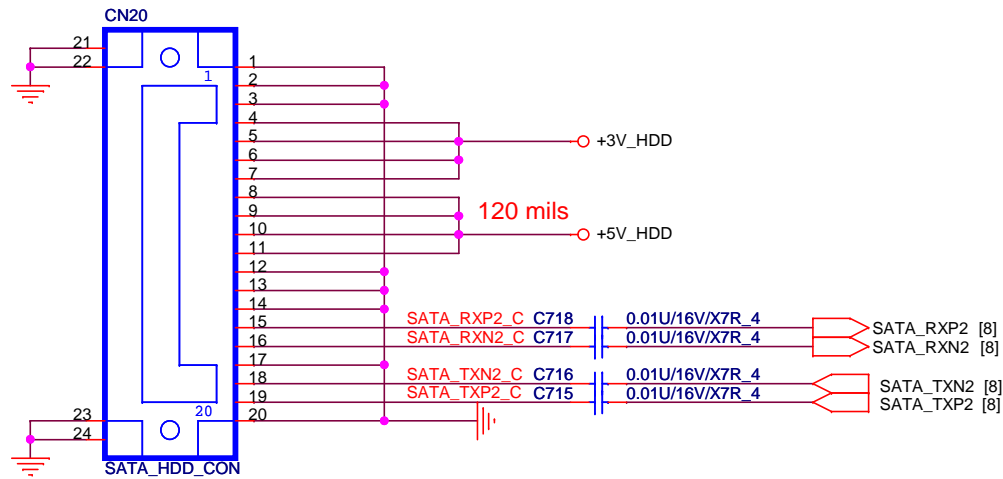
For ESD: The top section shows the ESD protection circuit. It includes two diodes (RV2, RV7) connected to the LAN pins (1, 2, 3, 4) and a network of resistors (R396, R625, R626, R627) and capacitors (C517, C509) for ESD protection. The text "EMI:close RJ45" is present.

For EMI: The bottom section shows the EMI filtering circuit. It includes two diodes (RV1, RV6) connected to the LAN pins (1, 2, 3, 4) and a network of resistors (R393, R625, R626, R627) and capacitors (C517, C509) for EMI filtering. The text "EMI:close RJ45" is present.

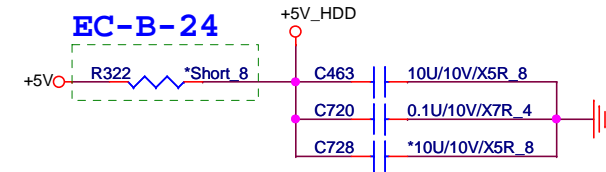
ICs: The diagram features two ICs: U21 (TP4220C26) and U22 (JM36113-N4525-7F). U21 is connected to the LAN pins (1, 2, 3, 4) and the LANVCC pin. U22 is connected to the LAN pins (1, 2, 3, 4) and the LANVCC pin.

LEDs: The diagram includes two LEDs: GREEN LED (RJ45_LINKUP#) and ORANGE LED (RJ45_ACTIVITY#). The GREEN LED is connected to the LAN pins (1, 2, 3, 4) and the LANVCC pin. The ORANGE LED is connected to the LAN pins (1, 2, 3, 4) and the LANVCC pin.

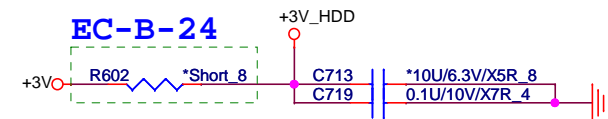
Labels: The diagram is labeled with "RJ45 Connector" at the top left, "For ESD" at the top center, "For EMI" at the bottom center, and "RJ45 Connector" at the bottom right.

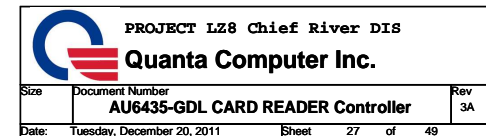


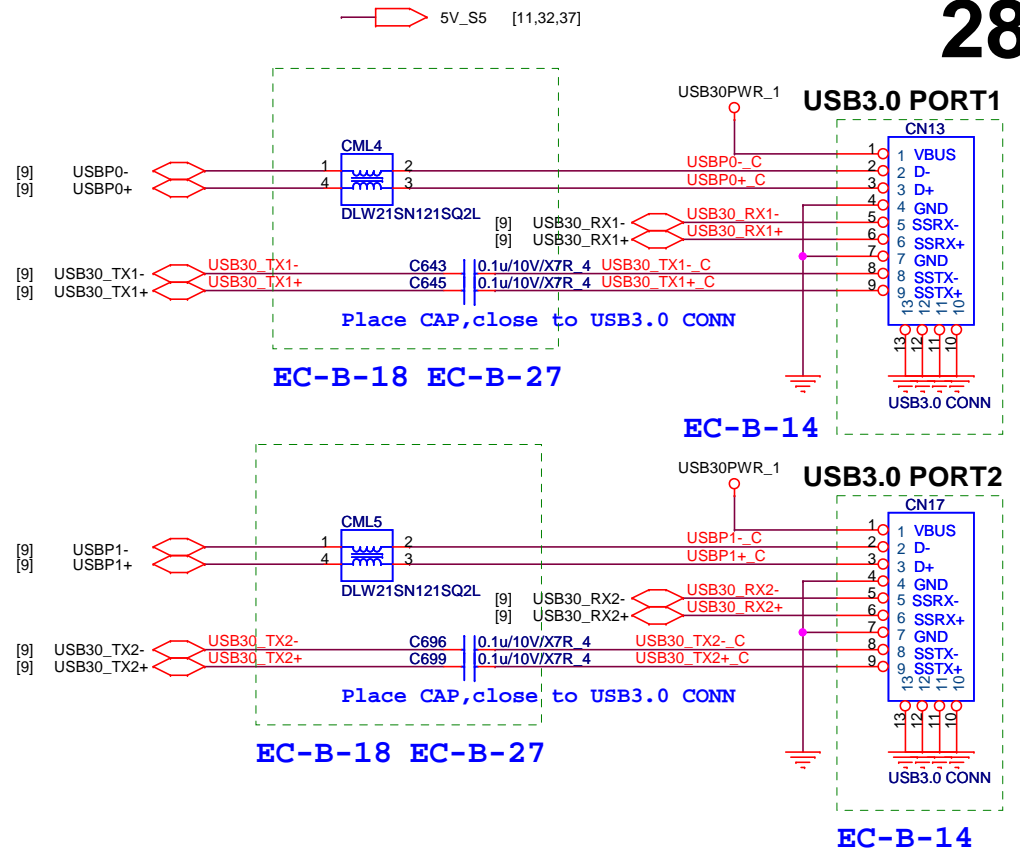
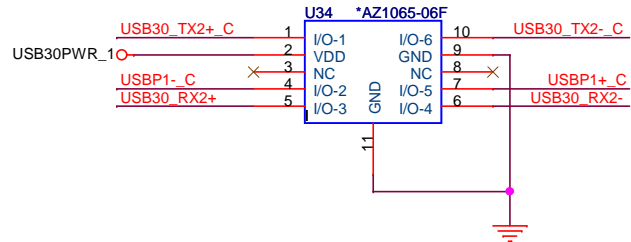
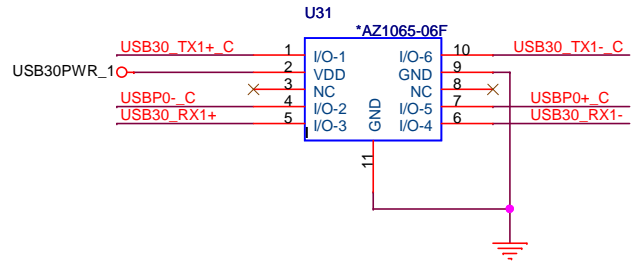
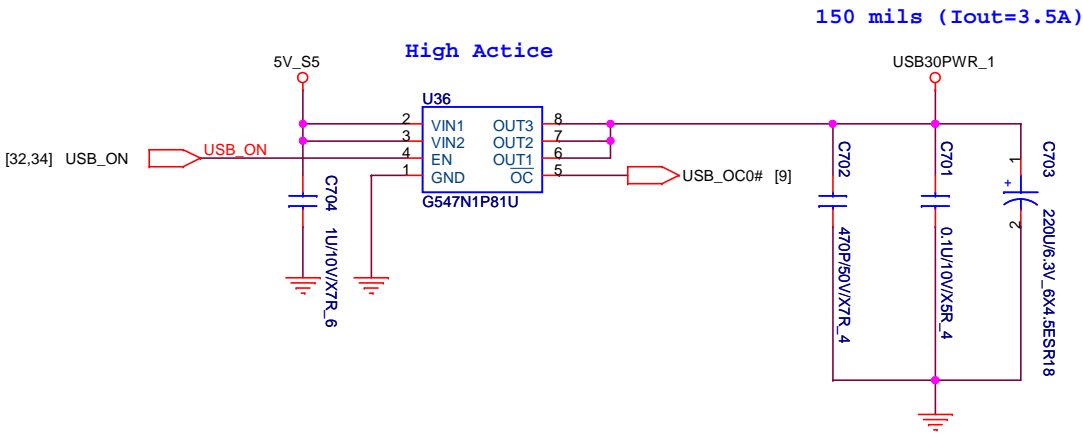
DC Current rating: 2 A (MAX)

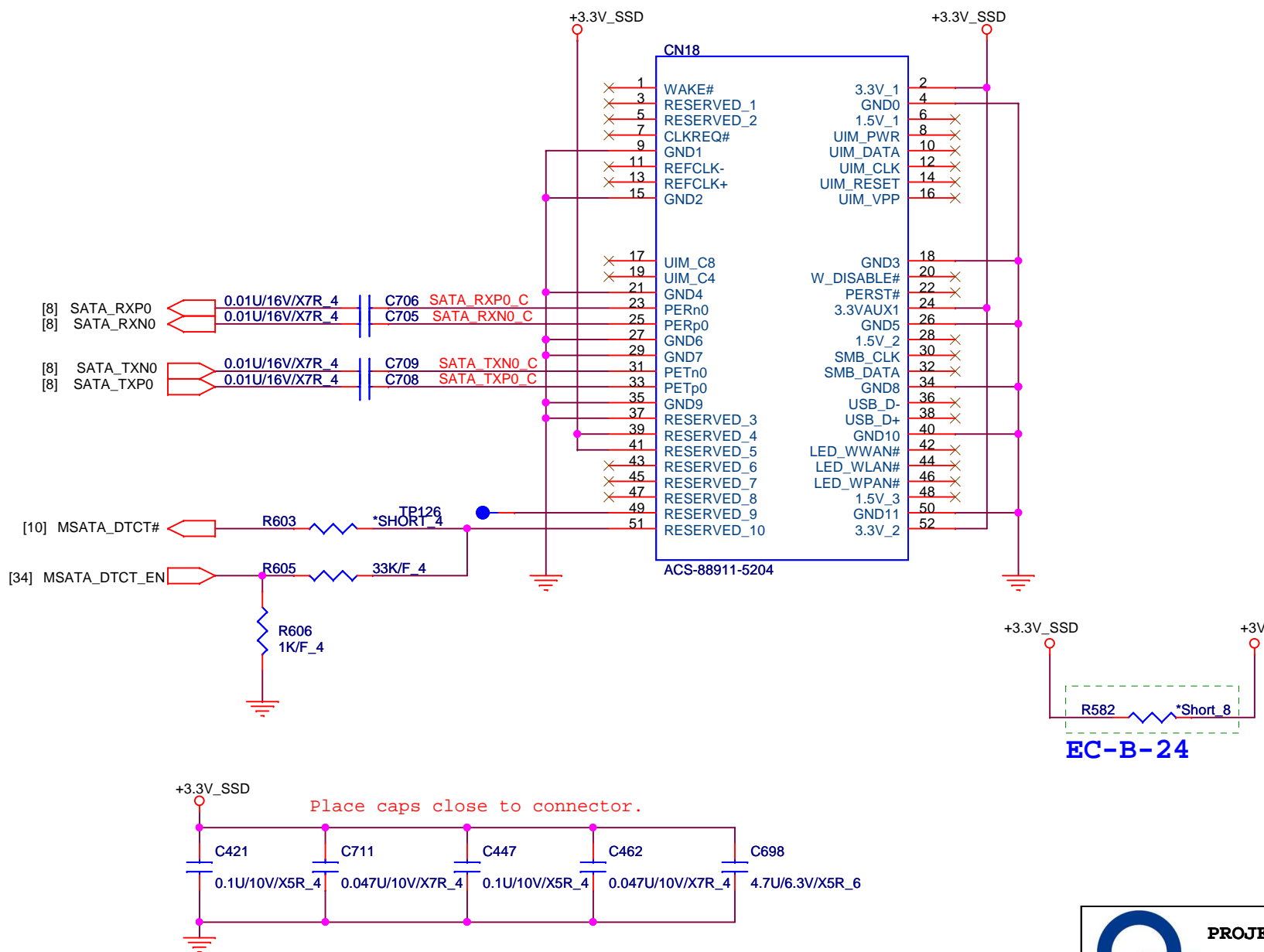


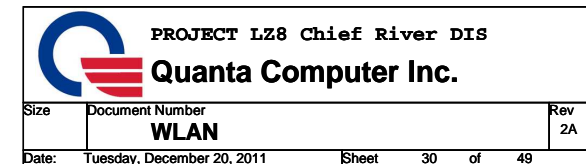
DC Current rating: 3 A (MAX)

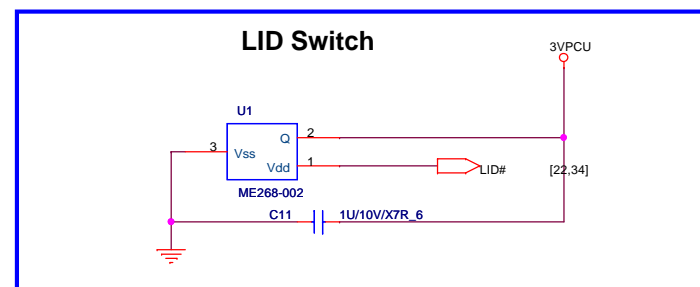
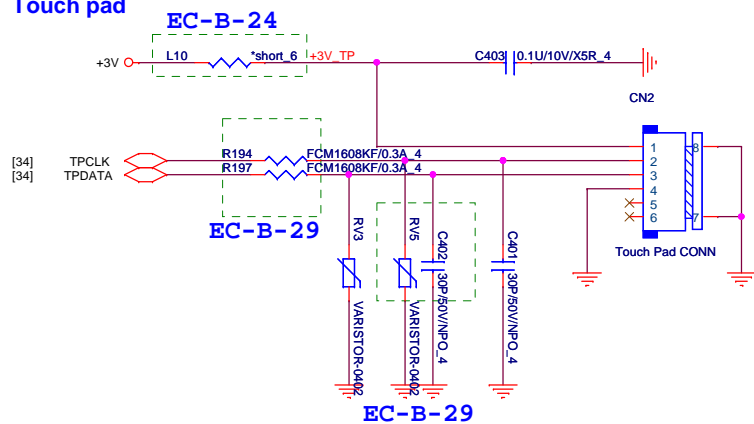




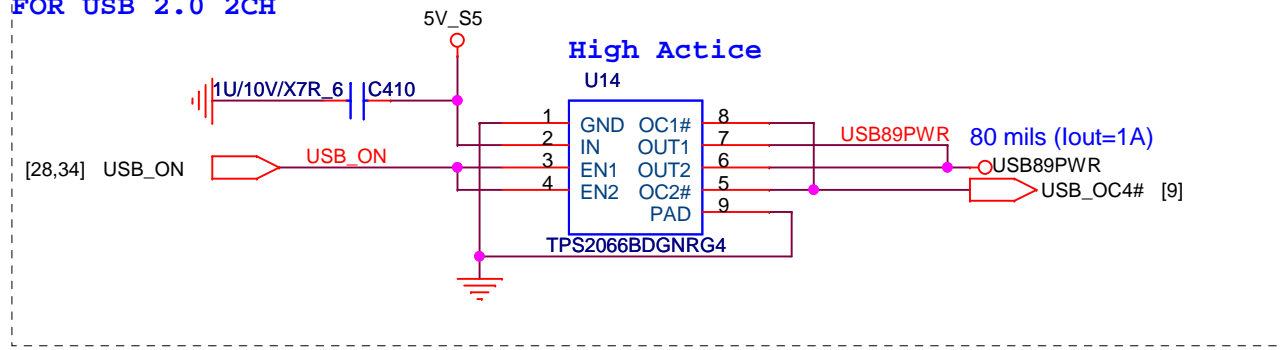




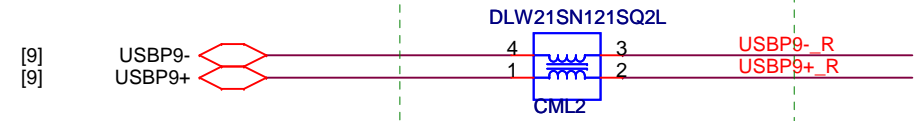
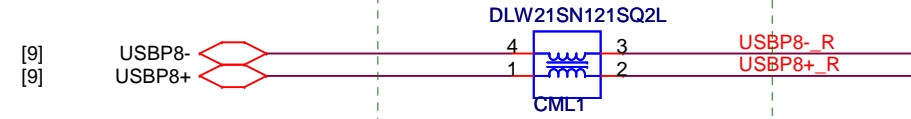
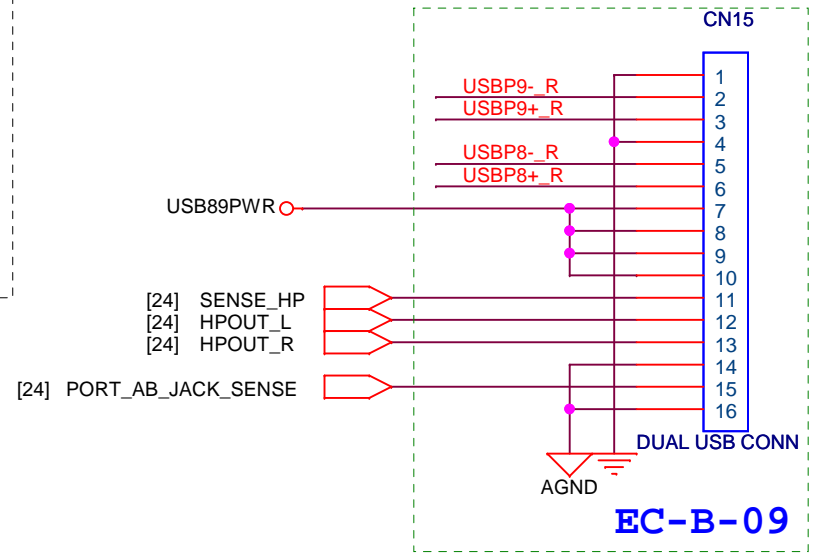




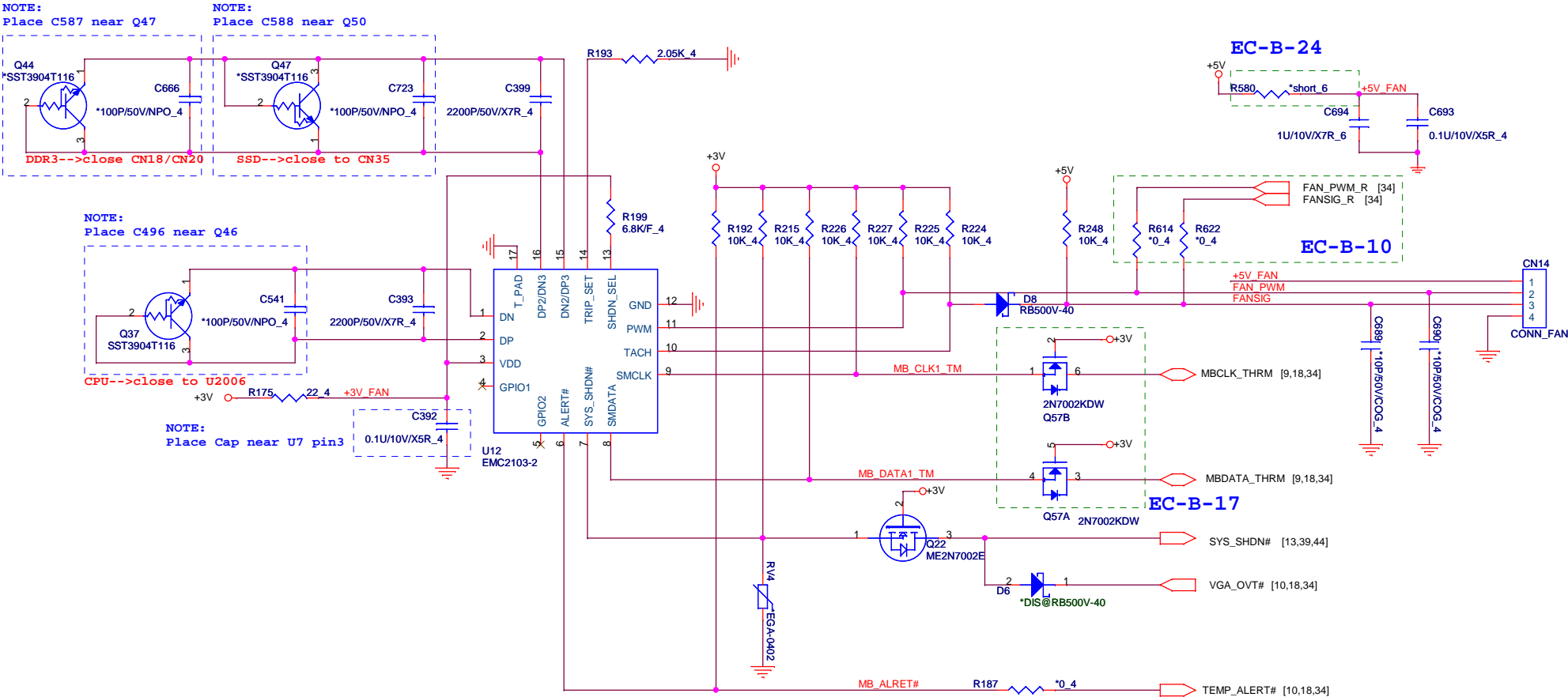
FOR USB 2.0 2CH

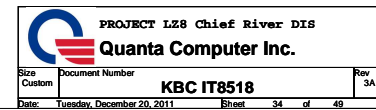


5V_S5 [11,28,37]



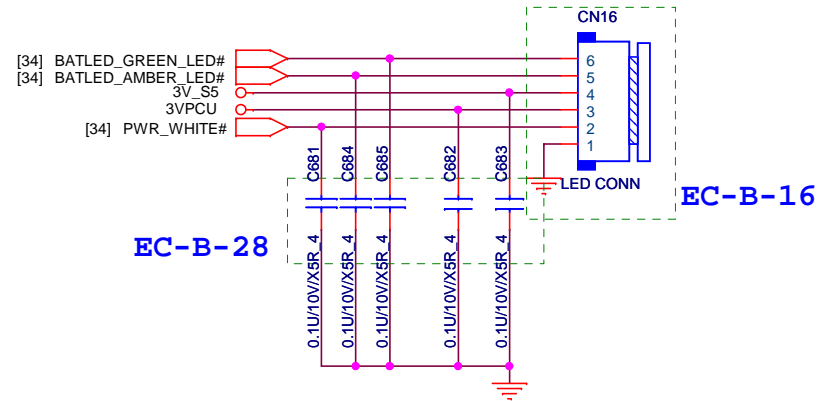
EC-B-18
EC-B-27





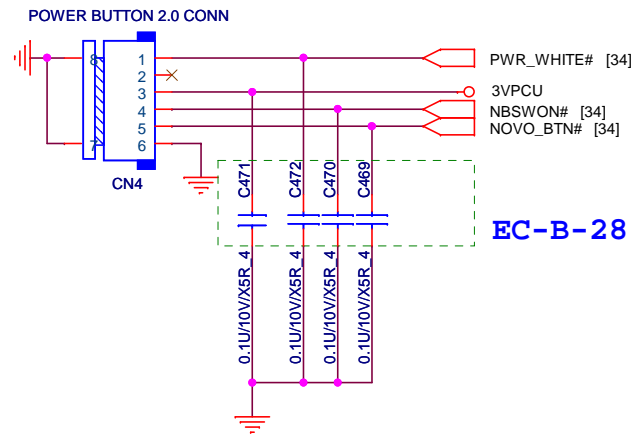
3VPCU [7,8,22,25,30,31,34,36,37,38,39,43,45]
3V_S5 [3,7,8,9,10,11,24,30,37]

LED Conn



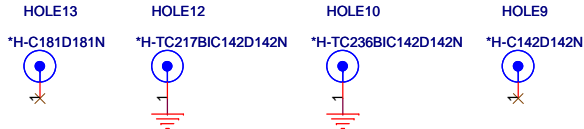
EC-B-28

POWER BUTTON/NOVO Button

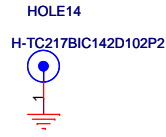


EC-B-28

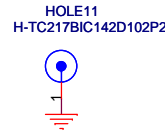
Hole for CPU support



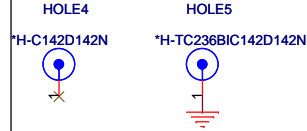
MiniCard WWAN



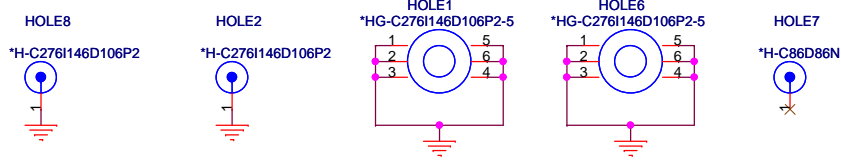
MiniCard WLAN



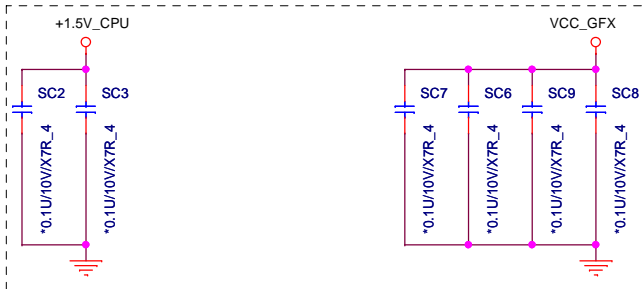
Hole for GPU support



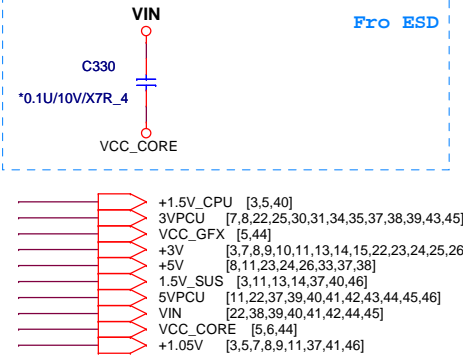
Boundary Hole



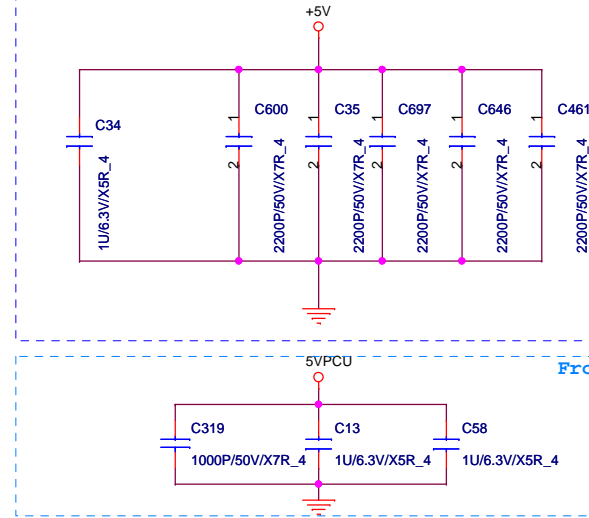
Fro ESD



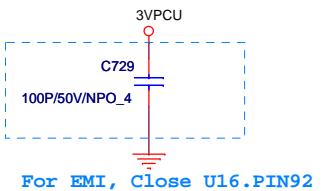
Fro ESD



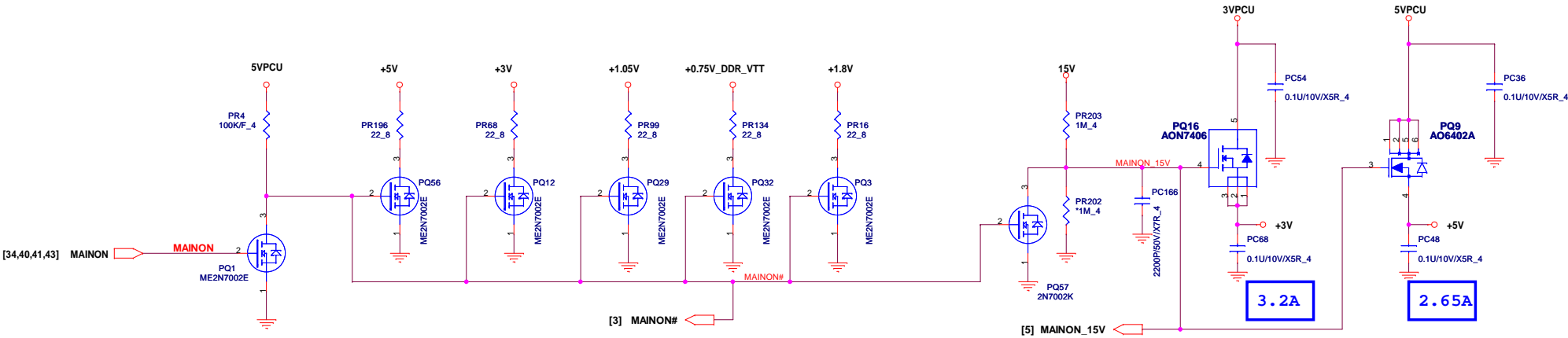
Fro EMI



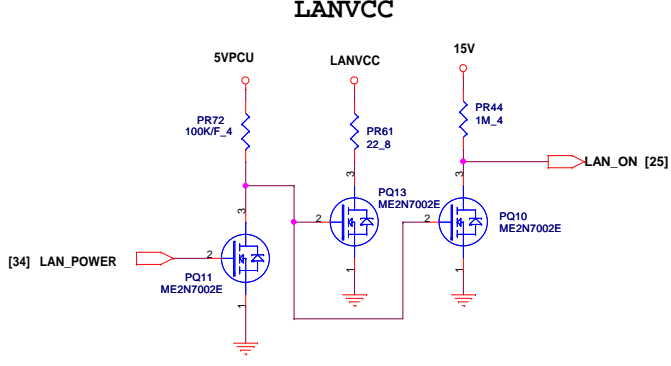
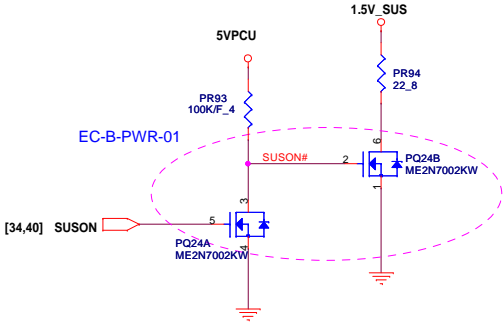
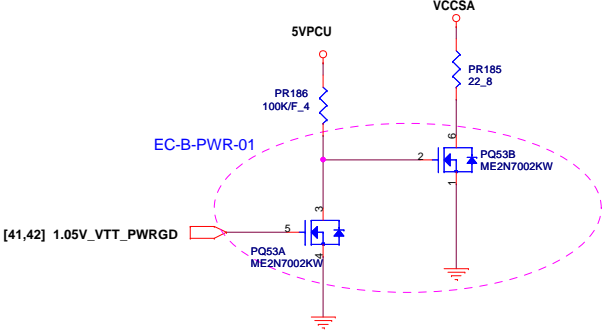
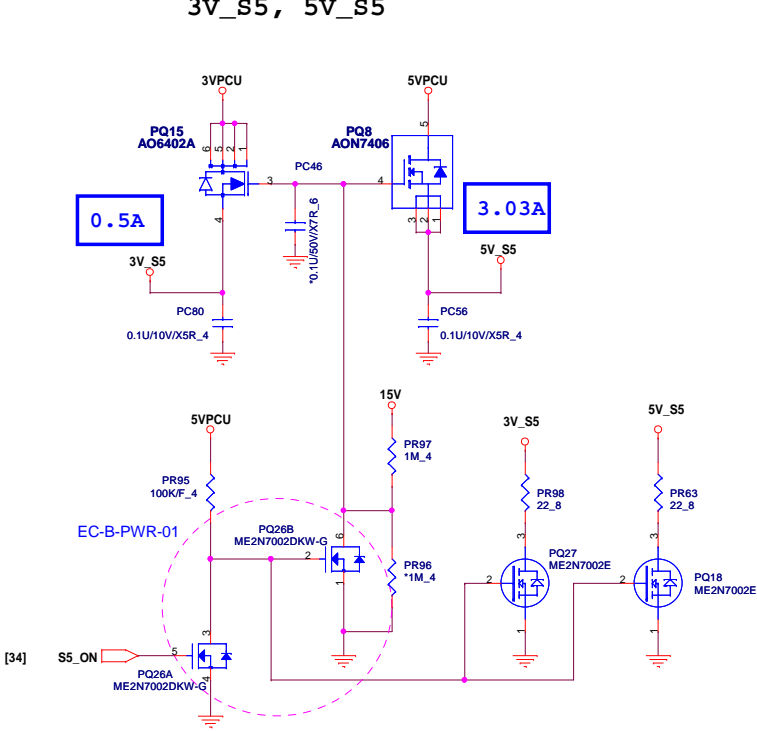
EC-B-22

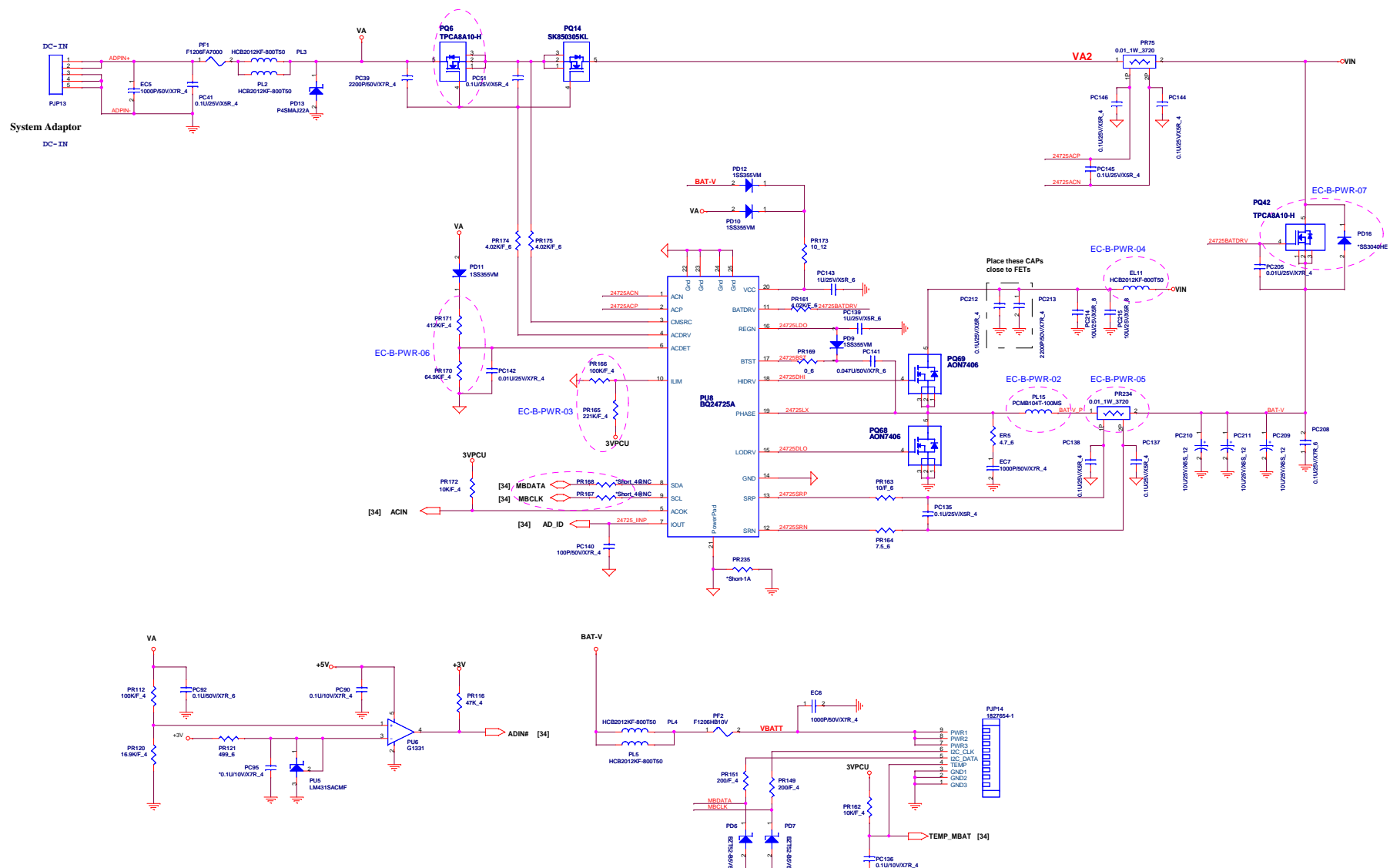


For EMI, Close U16.PIN92



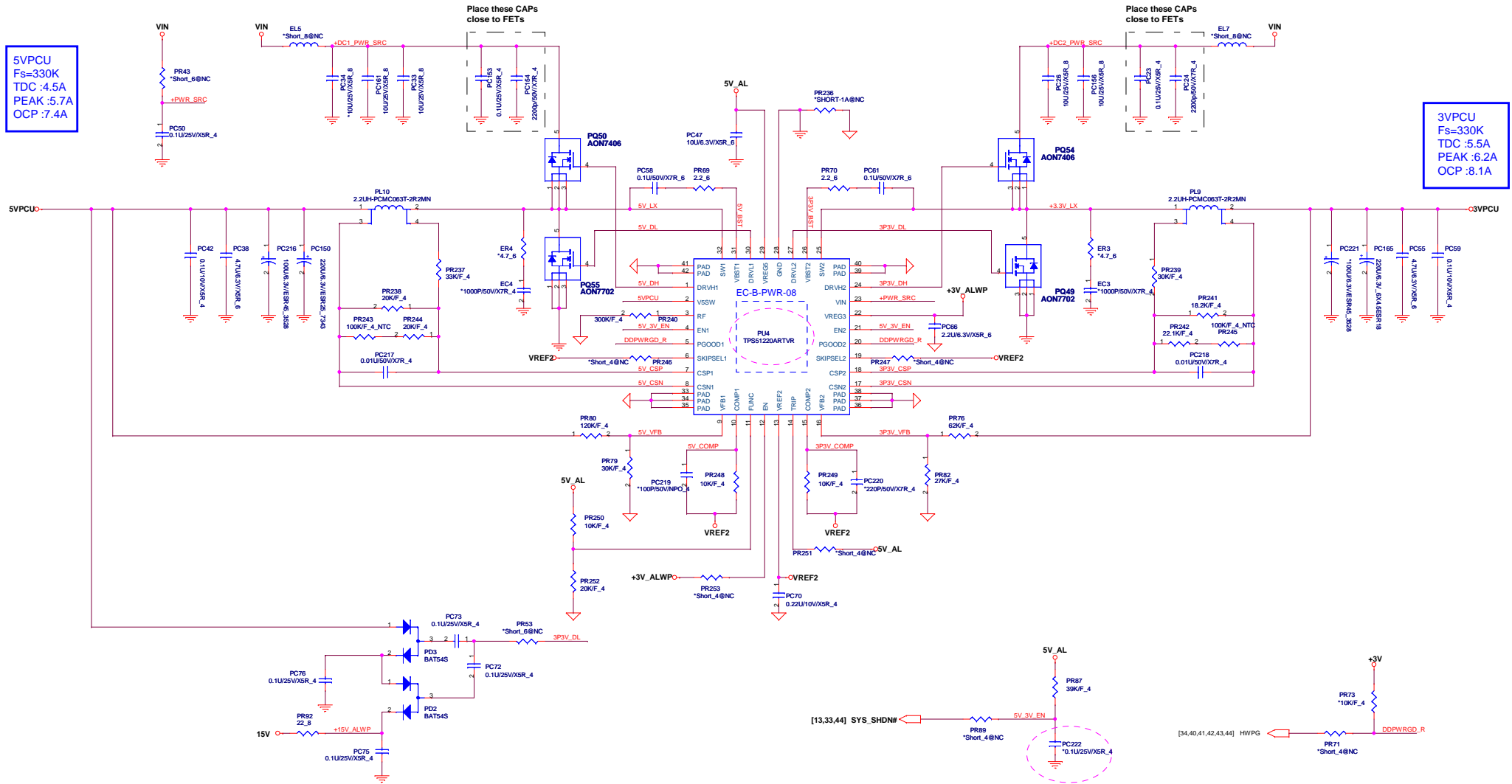
3V_S5, 5V_S5

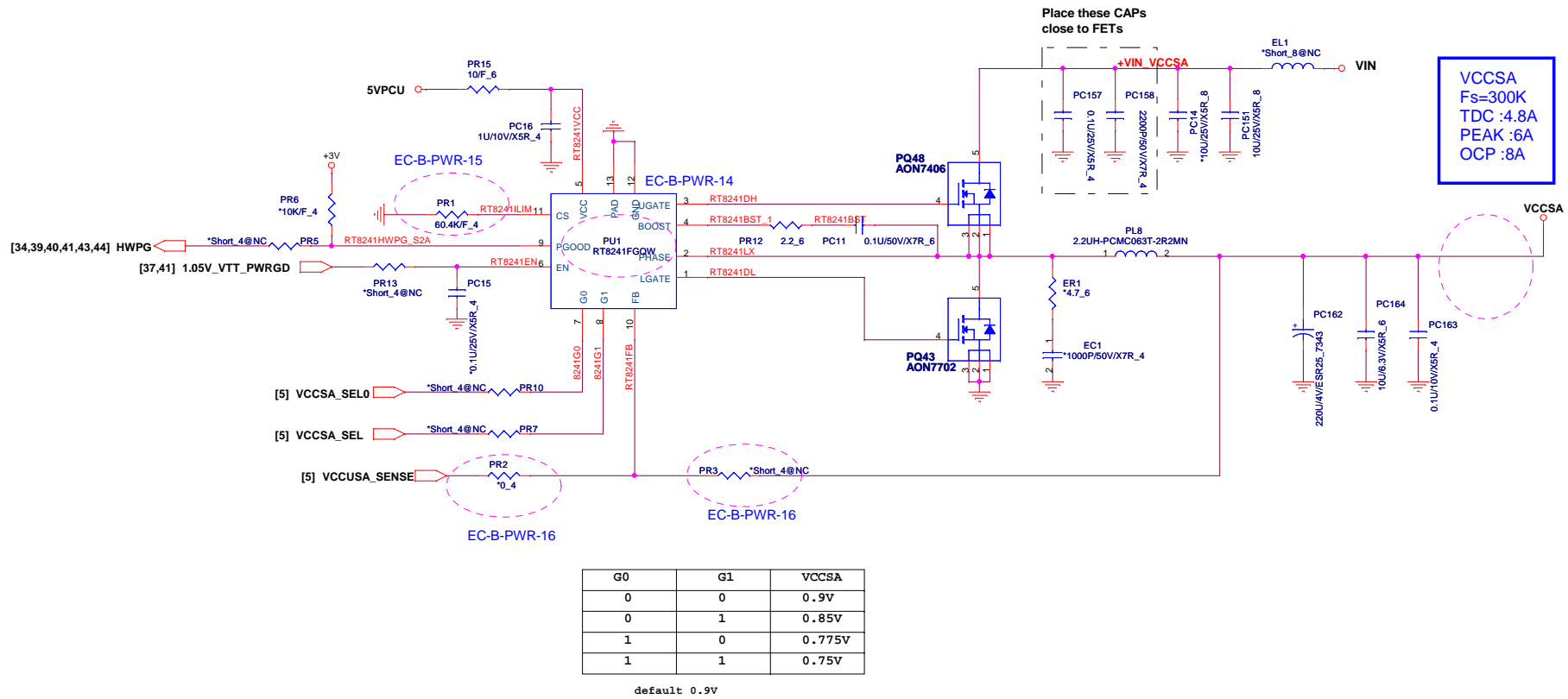


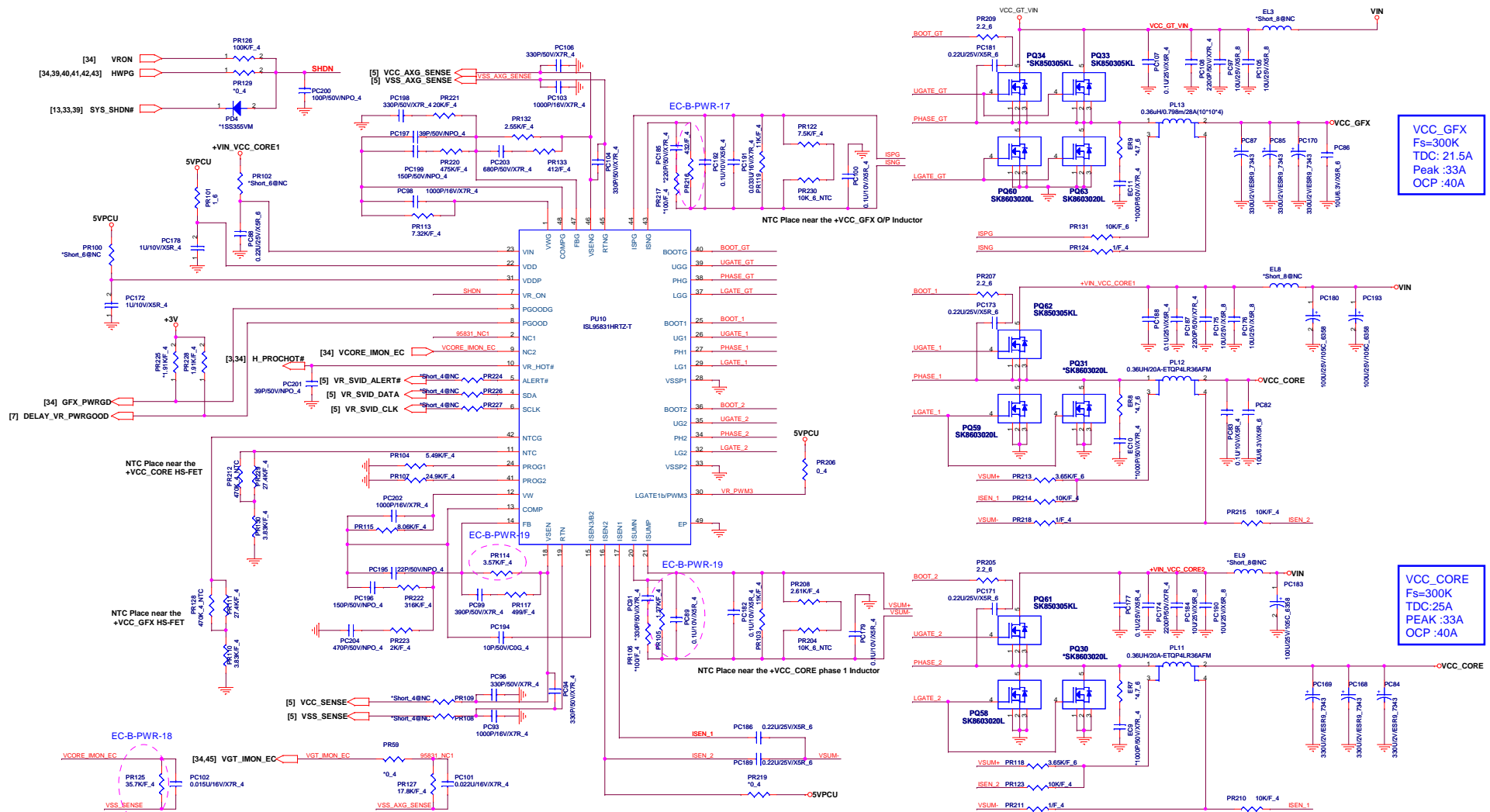


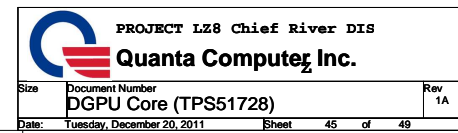
5VPCU
Fs=330K
TDC :4.5A
PEAK :5.7A
OCP :7.4A

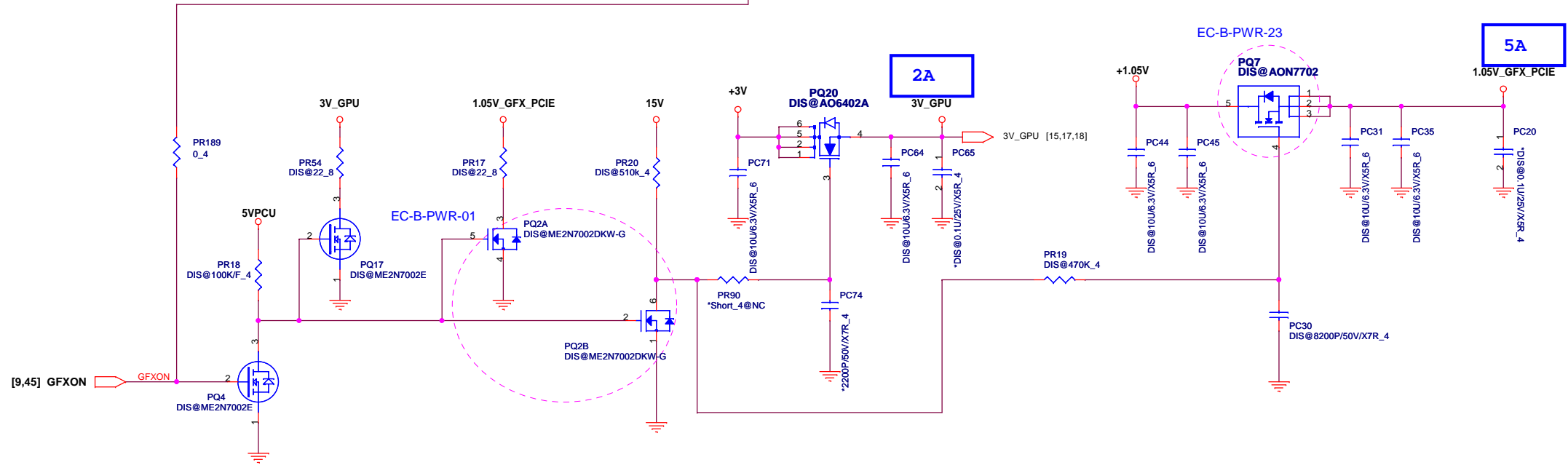
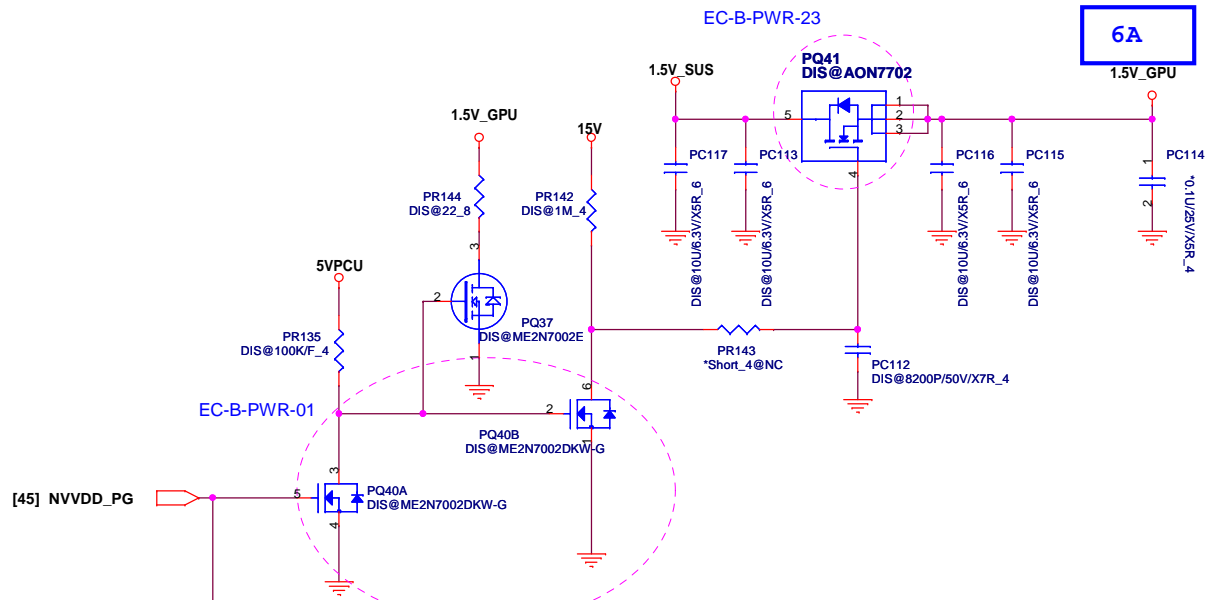
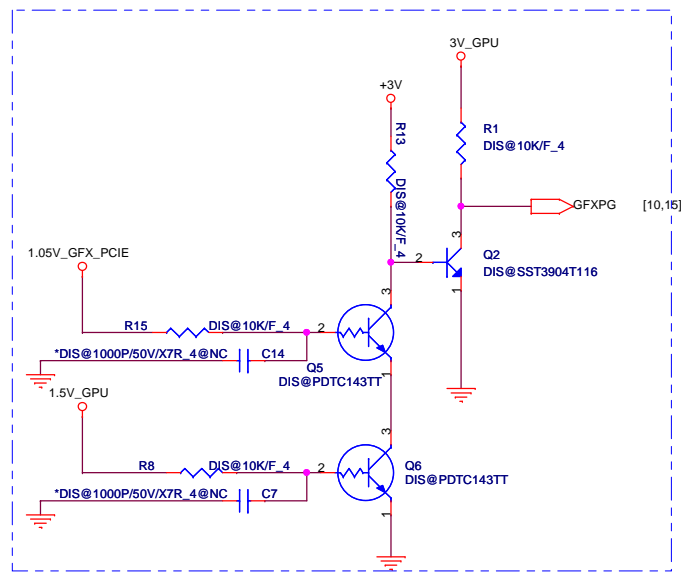
3VPCU
Fs=330K
TDC :5.5A
PEAK :6.2A
OCP :8.1A











E C N D	P G	D A r/mm/dd	P A R T	D E S C R I P T I O N
EC-B-01	7,11,34	11/10/13	Add R607,R608,R621 and no ASM	Add DEEP S3 function
EC-B-02	7	11/10/13	R210	R210 change to short pad
EC-B-03	9	11/10/13	R610 no ASM,R611 ASM, R	For DGPU power enable sequence
EC-B-04	10	11/10/13	R573 no ASM,R572 ASM	Change Board ID for SIV stage
EC-B-05	10,22	11/10/13	R49,R613,C724,R612,Q48 add and ASM	Change CCD control by PCH GPIO35
EC-B-06	23	11/10/13	CN10	Change CN10 to correct footprint
EC-B-07	24	11/10/13	R	Change Audio detect schematic
EC-B-08	25	11/10/13	CN8	Change CN8 to correct footprint
EC-B-09	32	11/10/13	CN15	Change CN25 Pin define
EC-B-10	33	11/10/13	Add R614,R622 no ASM	Add EC detect Fan speed schematic
EC-B-11	34	11/10/13	DEL R321	Change EC pin define,PIN94 connect to PWR_WHITE,PIN28 connect to FAN_PWM_R,PIN47 connect to FANSIG_R
EC-B-12	34	11/10/13	R298 no ASM	EC can output CLOCK by itself
EC-B-13	30	11/10/13	R35 no ASM,Q11ASM	input AOAC function
EC-B-14	28	11/10/13	CN13,CN17	Change CN13,CN17 to correct footprint
EC-B-15	28	11/10/13	add Q51,R623 no ASM	Add DEEP S3 function
EC-B-16	35	11/10/13	CN16	Change CN16 footprint for ME request
EC-B-17	9,18,22 23,33	11/10/14	Q30,Q31,Q26,Q27,Q34,Q35,Q3,Q4, Q41,Q42,Q23,Q24 DEL Add Q52,Q53,Q54,Q55,Q56,Q57 and ASM	Change MOS to Dual MOS
EC-B-18	21	11/10/19	Add Q58	For PS8622 flash ROM by EC ROM
EC-B-19	05	11/10/19	Add C727	Add a 10UF CAP for INTEL suggestion
EC-B-20	21	11/10/19	L14,L15,L16	Change footprint to 0603
EC-B-21	27	11/10/20	CN3	Change footprint for ME request
EC-B-22	36	11/10/24	Add C729,C730,C731	For EMI request
EC-B-23	3,7,11	11/10/24		Change LVDS signal by PCH provide
EC-B-24	7,24,25 26,27,29 30,31,33	11/10/24	R602,R322,R274,R305,R582,R580, L10,R129,R88,R87,R99,R79,R78, L22,L24	Change to short PAD
EC-B-25	8	11/10/24	BT1	Change BT1 footprint
EC-B-26	25	11/10/24	CN8	CN8 PIN4,5,7,8 connect to GND
EC-B-27	11,15	11/10/24	CML1,CML2,CML4,CML5 ASM R505,R502,R560,R563,R232,R233 R234,R235,C486,C488,C490,C497	for EMI request
EC-B-28	35	11/10/25	C472, C471, C470,C469,C681, C682 C683, C684,C685 ASM 0.1U	for EMI request
EC-B-29	35	11/10/25	RV5,C402 ASM 30P R194,R197 change to Bead	for EMI request
EC-B-30	35	11/10/26	C460 ASM 22P	for EMI request

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