HAINAN3_EXT

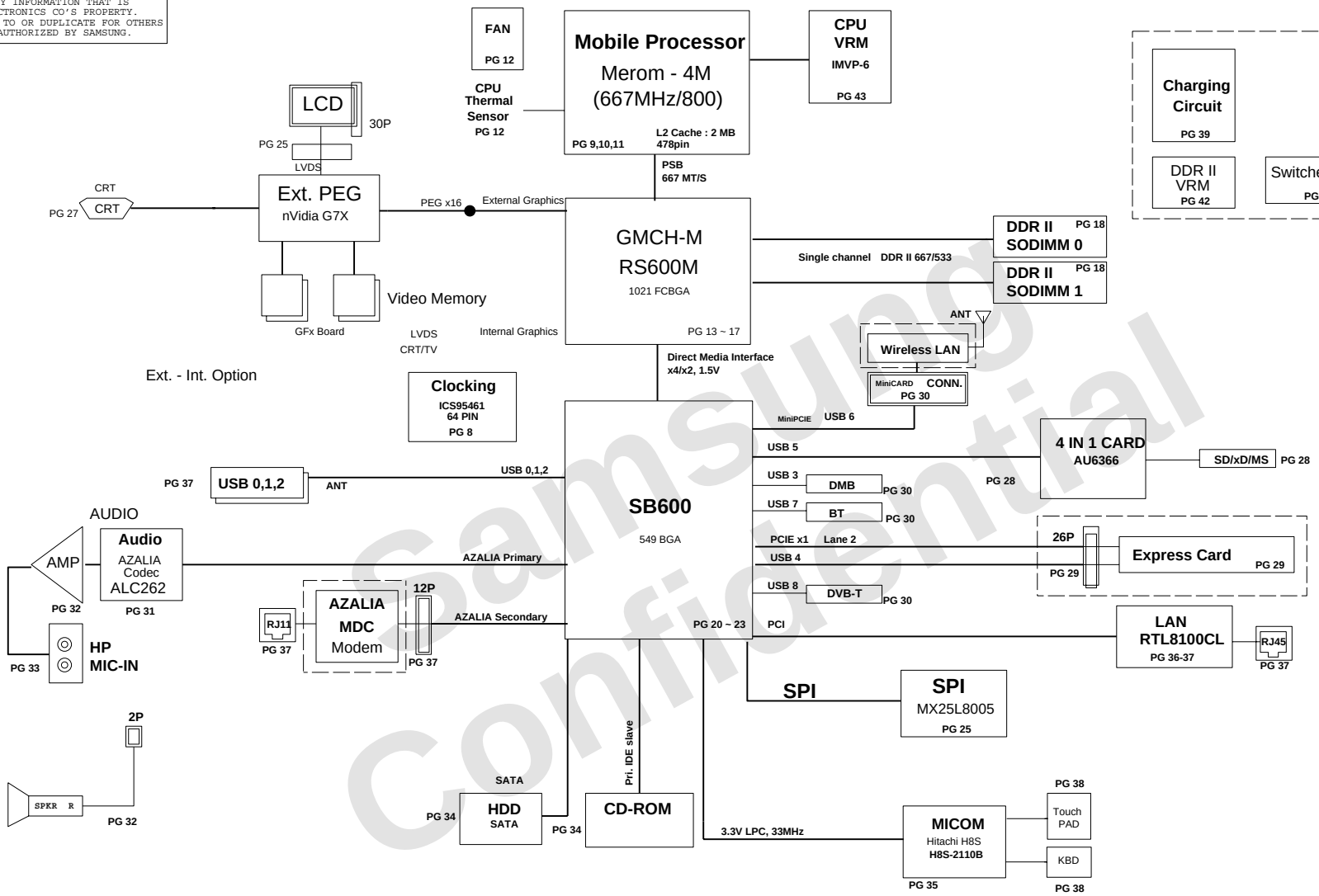
CPU : Intel Santarosa Merom
Chip Set : RS600&SB600&M64S
Remarks : Mobility Platform

Model Name : HAINAN3_EXT
PBA Name : MAIN
PCB Code : BA41-00809A GCE
BA41-00810A NANYA
Dev. Step : SR
Revision : 1.0
T.R. Date : 2007.06.16

DRAW	CHECK	APPROVAL
ELLEN ZHANG	ROKY ZHENG	KEVIN LEE

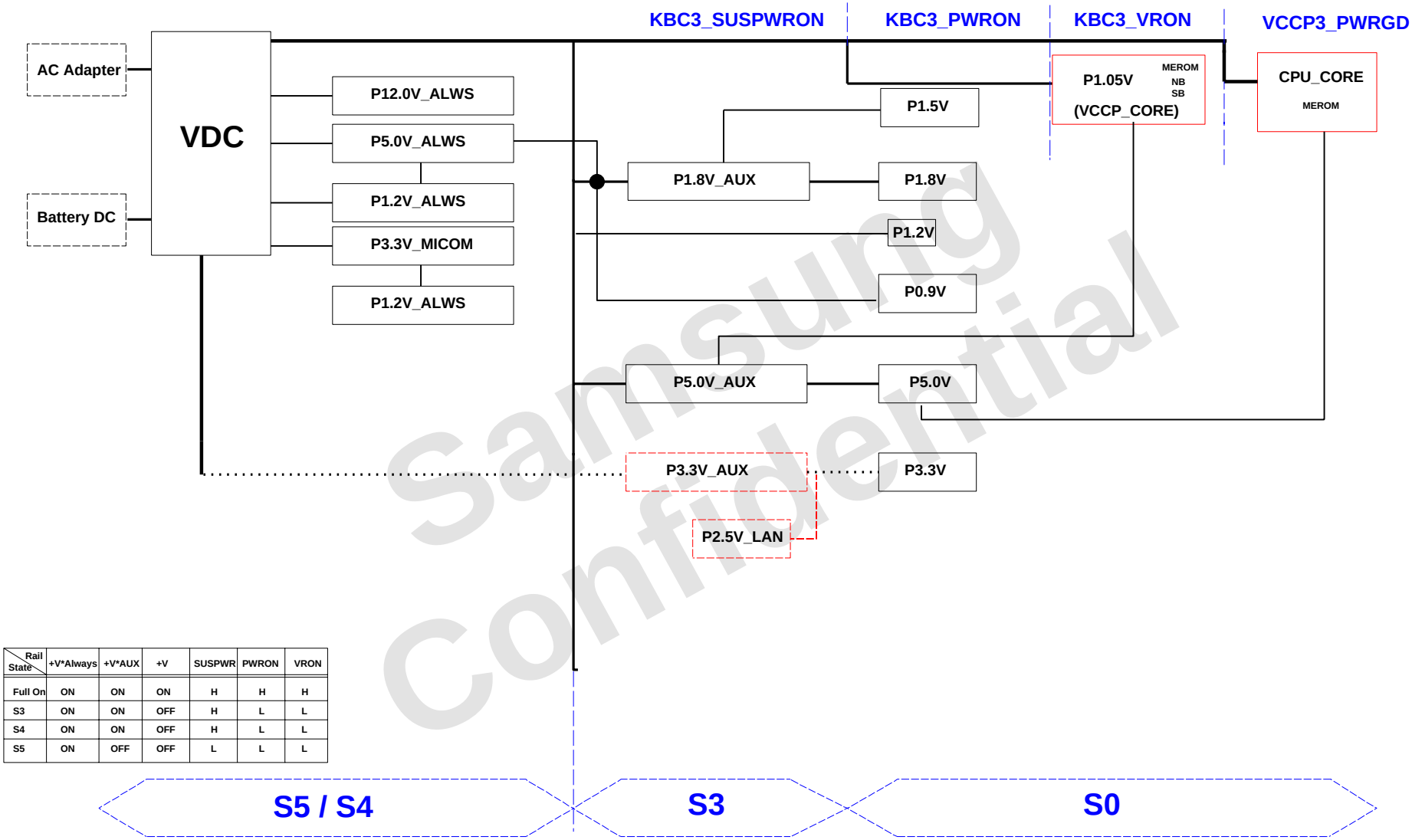
Table of Contents

DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	COVER	PART NO.: BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM	PAGE 1 OF 53	



DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	DIAGRAM	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM	PAGE 2 OF 53	

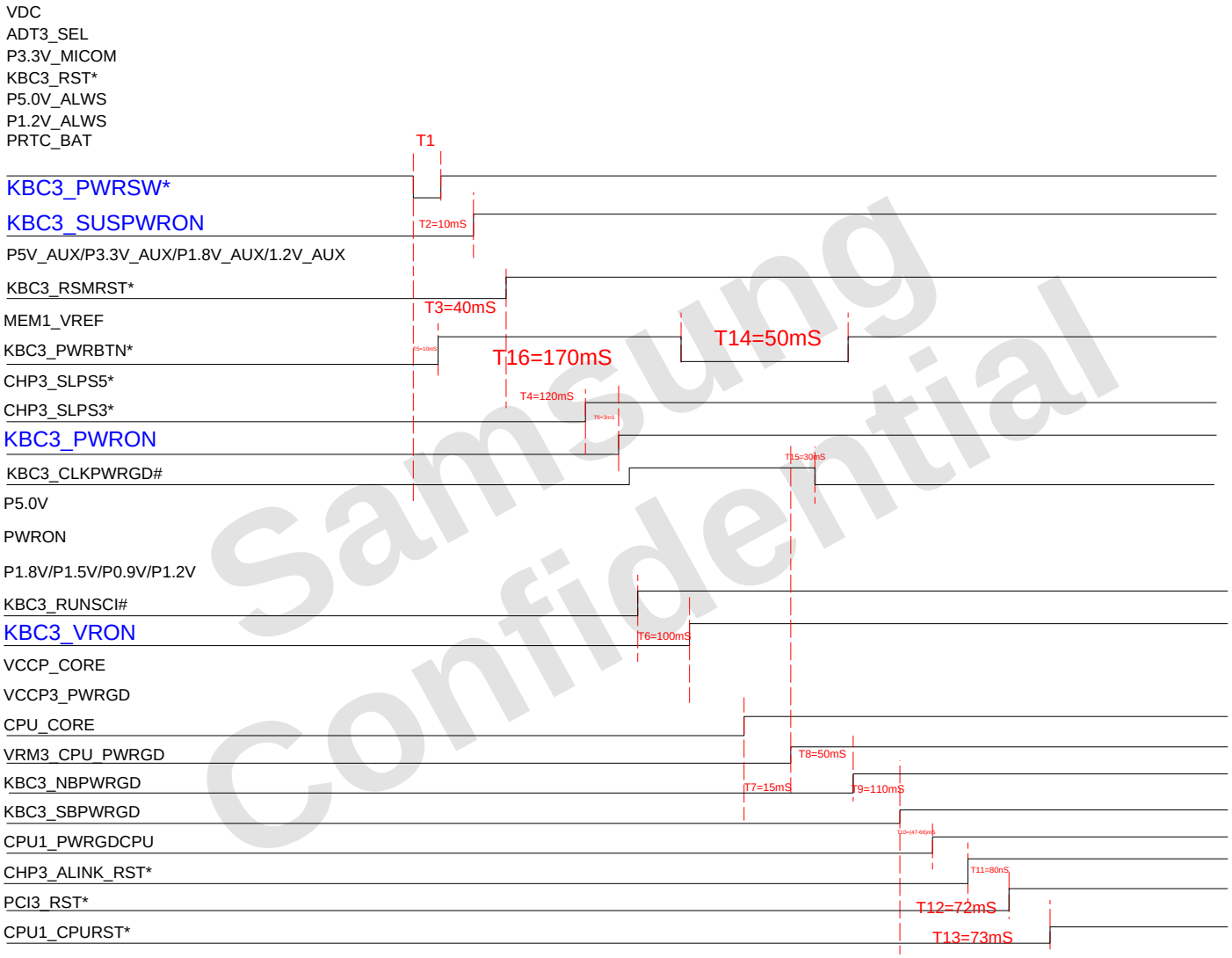
Power Diagram



Rail / State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	ON	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L

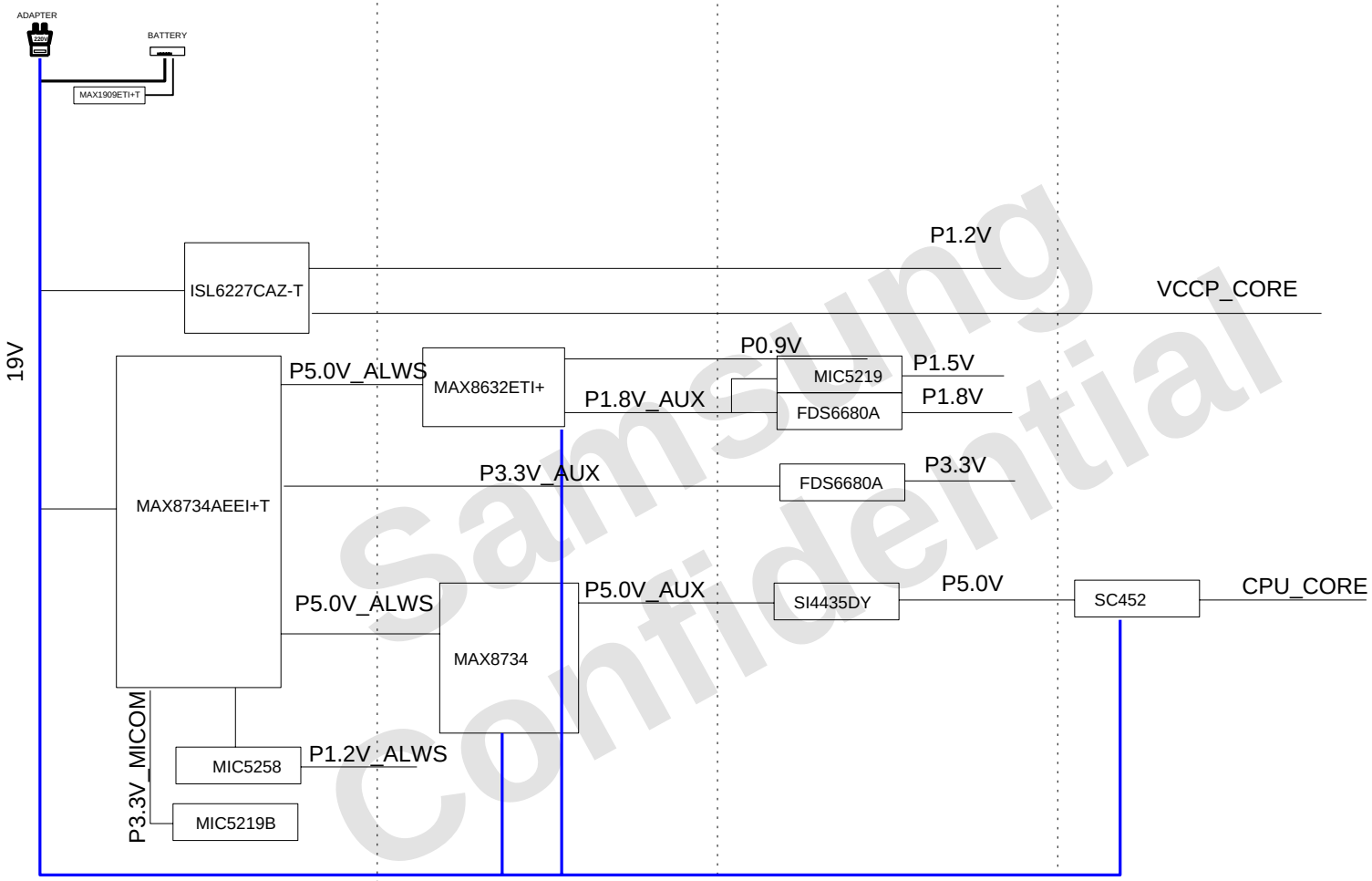
DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	POWER DIAGRAM	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 3 OF 53

POWER SEQUENCE

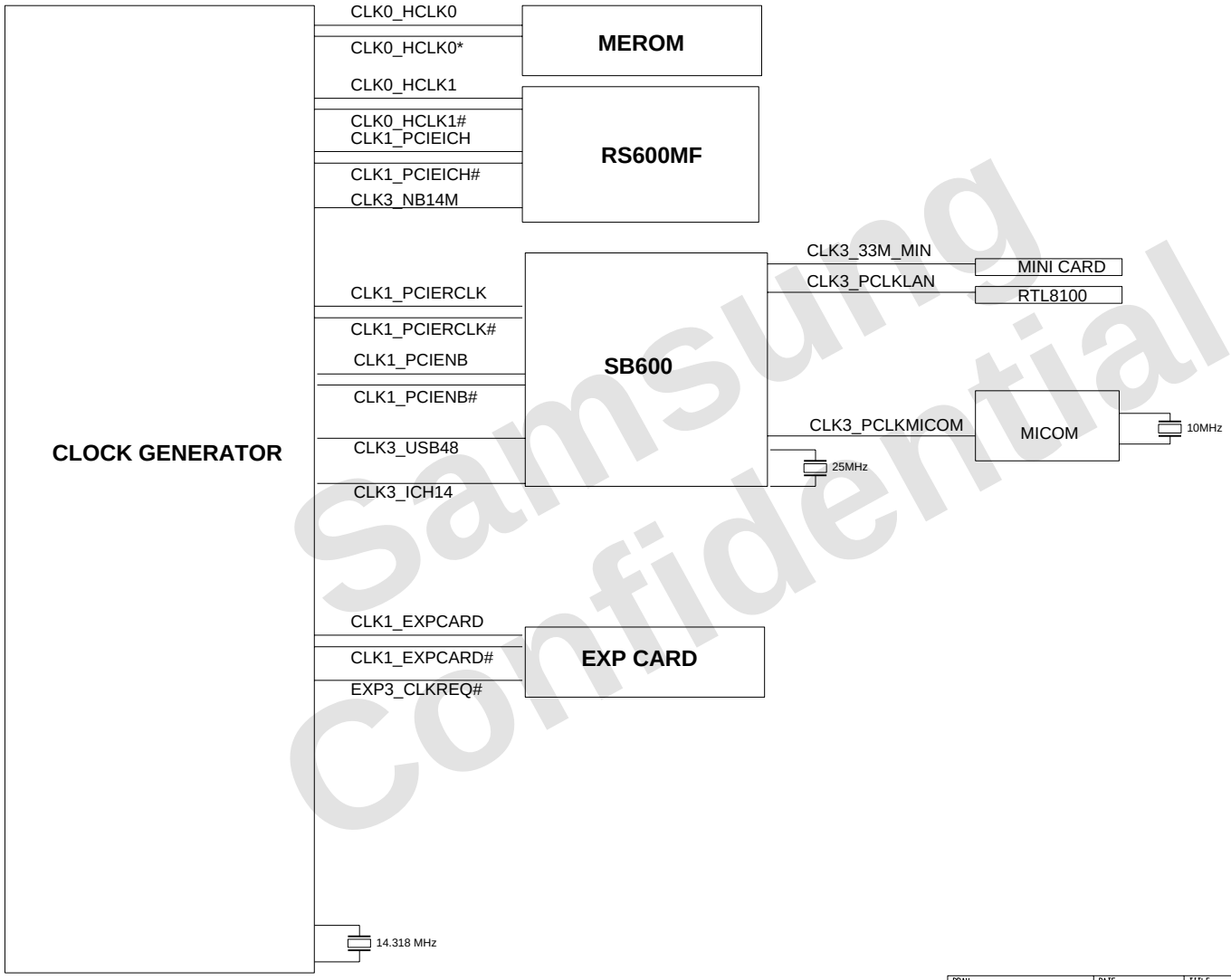


DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	POWER SEQUENCE	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 4 OF 53

POWER RAILS ANALYSIS



DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	POWER BLOCK	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 5 OF 53



DRAW ELLEN ZHANG	DATE 6/16/2007	TITLE HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK ROKY ZHENG	DEV. STEP SR		
APPROVAL KEVIN LEE	REV 1.0	CLOCK DIAGRAM	PART NO. BA41-00809/810A
MODULE CODE undefined	LAST EDIT March 23, 2007 11:06:39 AM		PAGE 6 OF 53

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
LAN	AD21	1	G
USB	AD30(internal)	-	- - -
Hub to PCI	AD31(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	-
Internal MAC	AD31(internal)	-	-
AC Link	-	-	-

Voltage Rails

CPU_CORE	CPU
VCCP_CORE	CPU RS600 SB600
P1.2V	RS600 SB600
P1.5V	CPU EXPCARD
P1.8V	RS600
P0.9V	DDR2
P5.0V	FAN THERMAL CRT SB600 AU6366 MINIPCI ALC262 HDD ODD MICOM USB TOUCH-PAD CPU_CORE
P3.3V	SYSTEM POWER
P2.5V_LAN	RTL8100
P1.8V_AUX	DDR2 P1.8V RS600
P5.0V_AUX	THERMAL LCD P1.2V P5.0V
P3.3V_AUX	MDC MICOM MINIPCI EXP-CARD SB600 THERMAL
P12.0V_ALWS	P1.5V P3.3V P1,8V
P5.0V_ALWS	P3.3V DDR2-PWR
P3.3V_MICOM	THERMAL SB600 MICOM LED P1.8V_ALWS
P1.2V_ALWS	SB600,P1.2V
VDC	Primary DC system power supply (7 to 21V)

I 2 C / SMB Address

Devices	Address	Hex	Bus
SB600	Master	-	SMBUS Master
EMC6N300(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
ICS95411 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1,2	SYSTEM PORT B
3	DMB
4	EXPRESS CARD
5	4 IN 1 CARD
6,8	MINI PCIE
7	BT

System Power States

CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped.
The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other criticial subsystems.
Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.

CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits.
Memory is retained, and refreshes continue. All clocks stop except RTC clock.

CHP3_SLP4S* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
Externally appears same as S5, but may have different wake events.

CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB600	Real Time Clock
Crystal	10MHz	MICOM	HD64F2110B
Crystal	14.318MHz	CLOCK-Generator	ICS95461
Crystal	12MHz	AU6366	4 IN 1 CARD
Crystal	25MHz	LAN	LOM

CPU Core Voltage Table

IMVP-6

Active Mode VID(6:0)	Voltage	Active/Deeper Sleep Dual Mode Region VID(6:0)	Voltage	Deeper Sleep/Extended Deeper Sleep Dual Mode Region VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 1 0 0 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

Active

DPRSLPVR	0
DPRSTP*	1
PSI2*	0 or 1

Deeper Slp

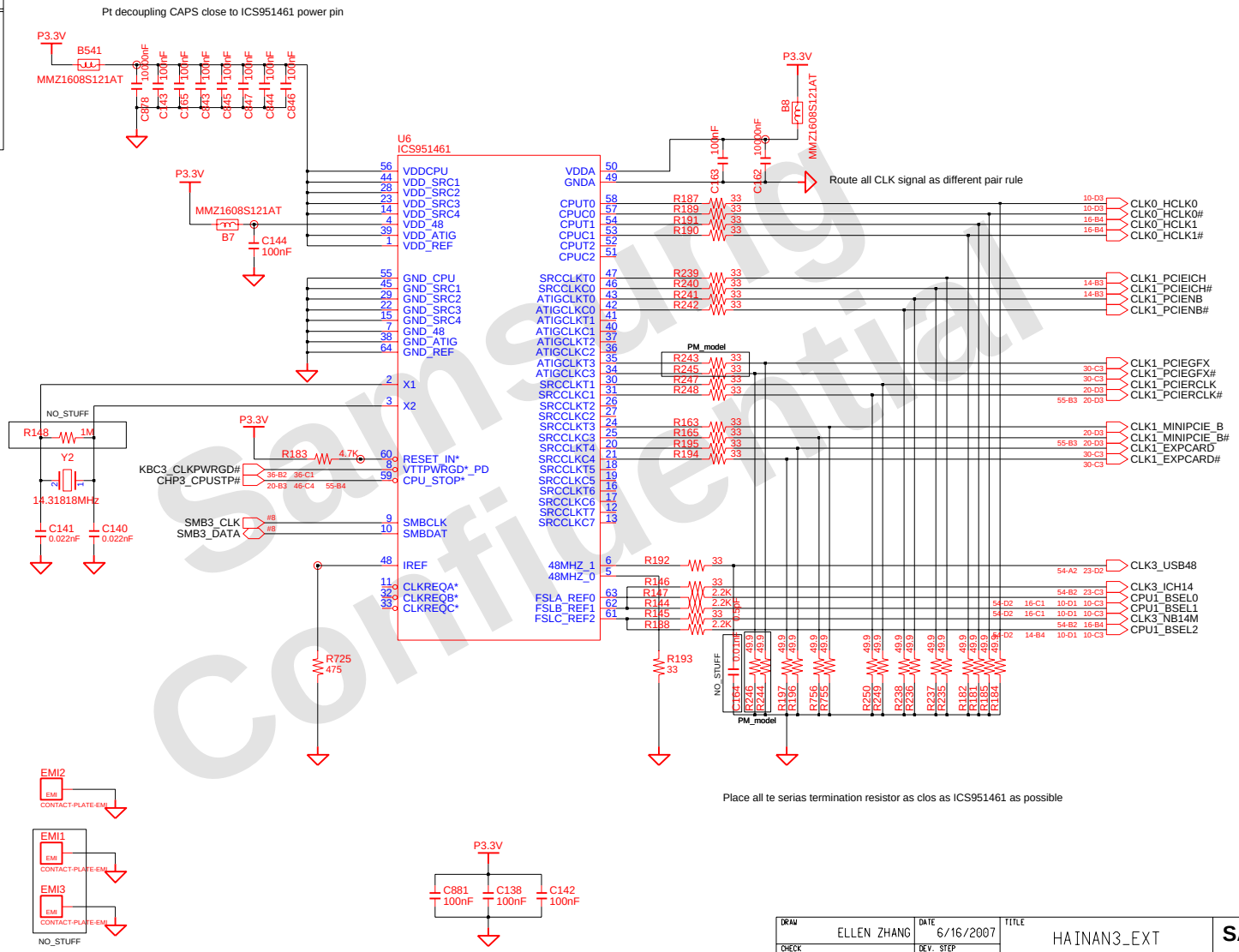
DPRSLPVR	1
DPRSTP*	0
PSI2*	0 or 1

*"1111111" : 0V power good asserted.

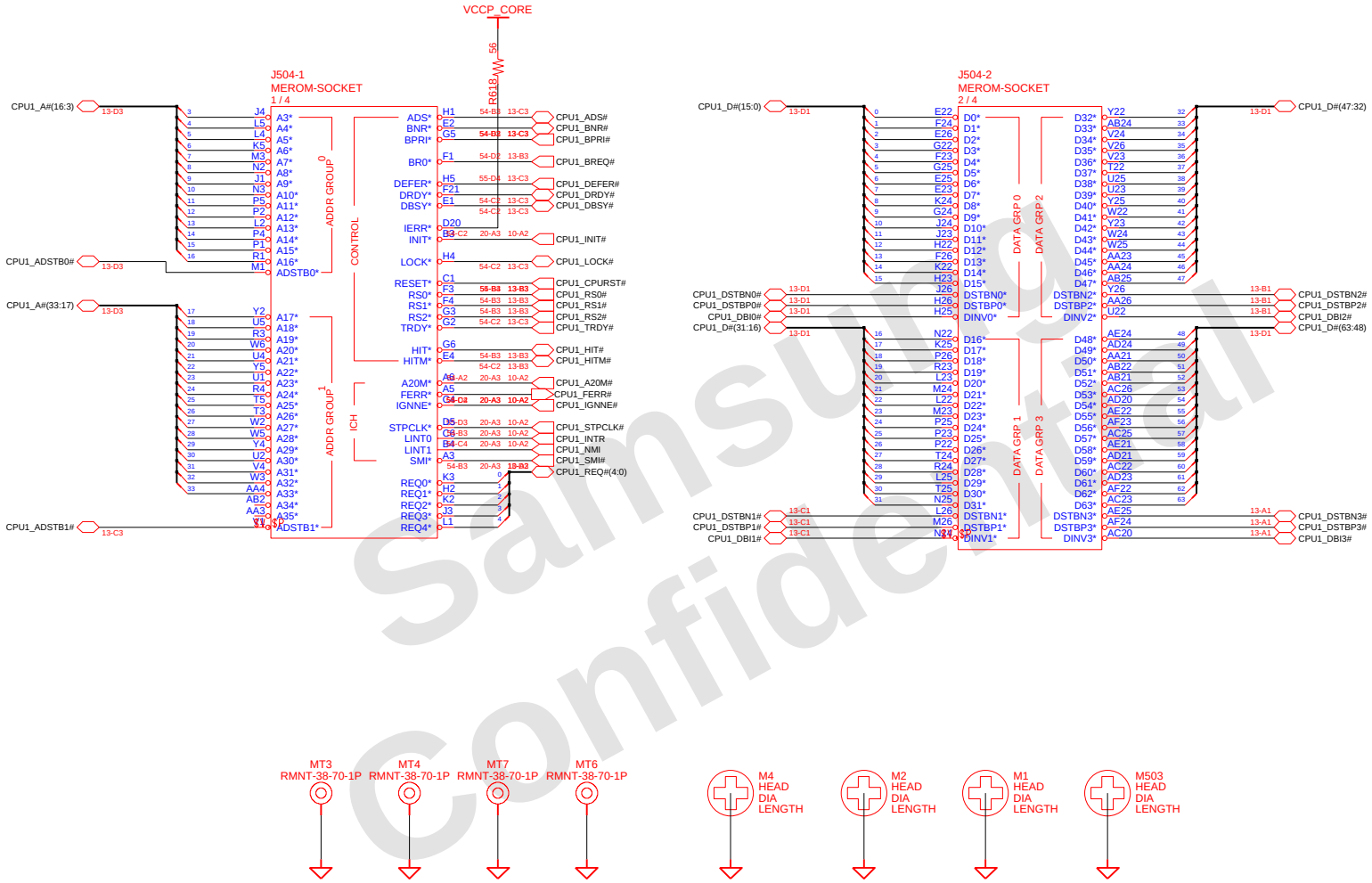
*Yonah Processor (2.33 GHz / 800 MHz : TBD)

DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT ANNOTATIONS	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 7 OF 53

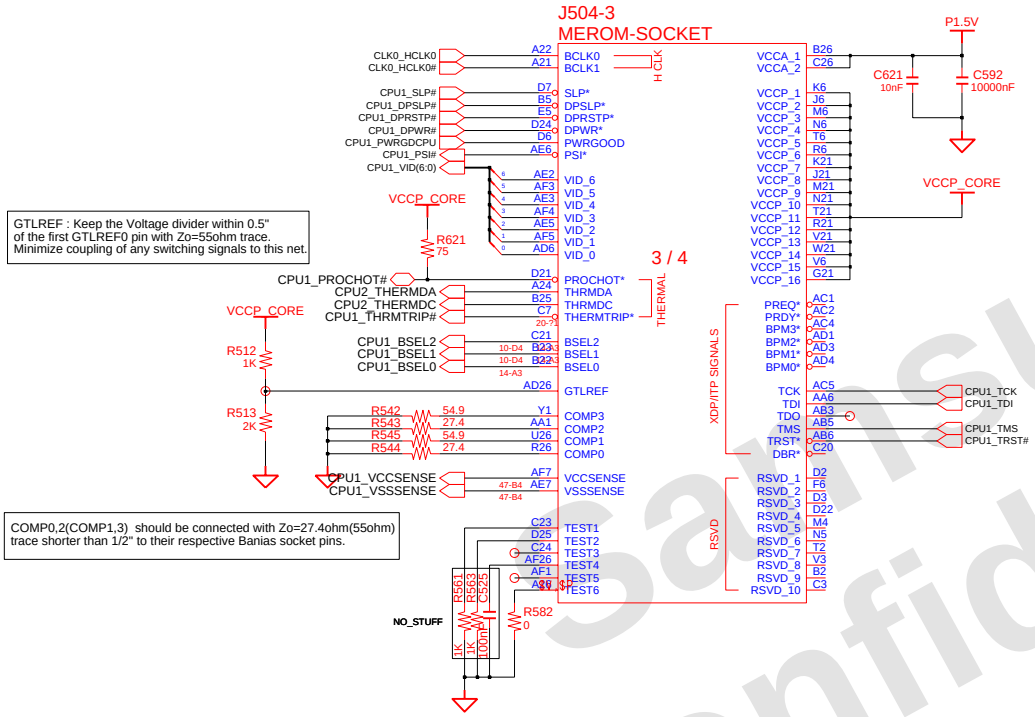
CPU	FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
	0	0	0	266 MHz
	0	0	1	333 MHz
	0	1	0	200 MHz
	0	1	1	400 MHz
	1	0	0	133 MHz
	1	0	1	100 MHz
	1	1	0	166 MHz
	1	1	1	RSVD



DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT CLOCK	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 8 OF 53



DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	MEROM(1/3)	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 9 OF 53



GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

CPU Core Voltage Table

IMVP-6

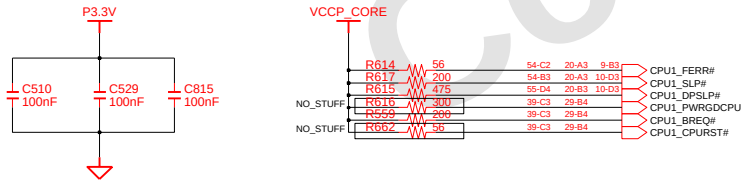
Active Mode VID(6:0)	Voltage	Active/Deeper Sleep Dual Mode Region VID(6:0)	Voltage	Deeper Sleep/Extended Deeper Sleep Dual Mode Region VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 1 0 0 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

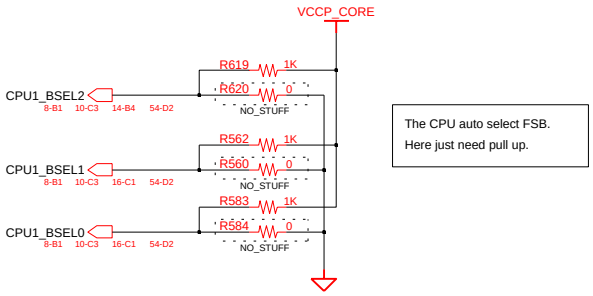
Active	
DPRSLPVR	0
DPRSTP*	1
PSI2*	0 or 1

Deeper Slp	
DPRSLPVR	1
DPRSTP*	0
PSI2*	0 or 1

*"1111111" : 0V power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)



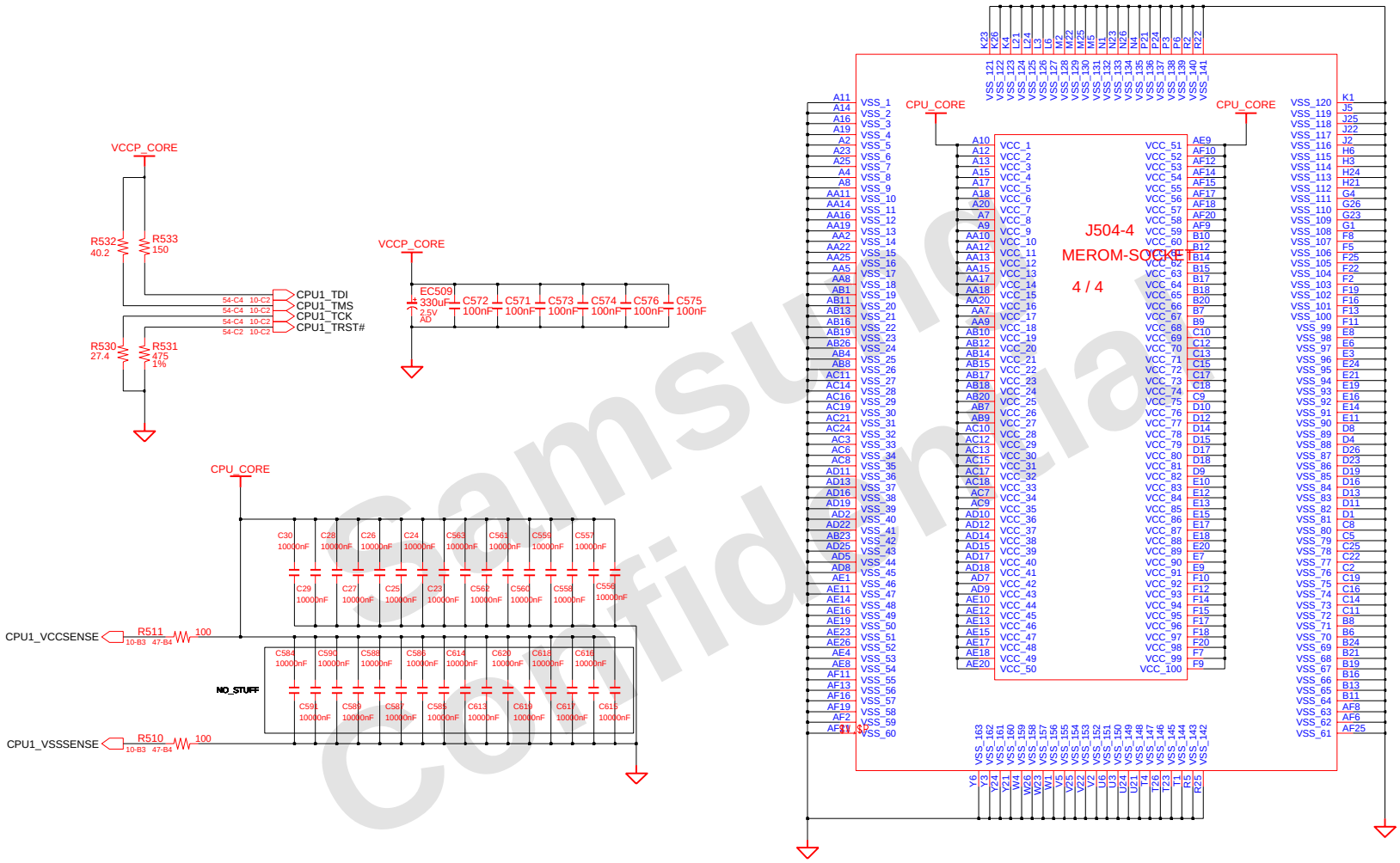


The CPU auto select FSB.
Here just need pull up.

DRAW	ELLEN ZHANG	DATE	6/16/2007	TITLE	HAINAN3_EXT
CHECK	ROKY ZHENG	DEV. STEP	SR		
APPROVAL	KEVIN LEE	REV	1.0		MEROM(2/3)
MODULE CODE	undefined	LAST EDIT	March 23, 2007 11:06:39 AM		

SAMSUNG ELECTRONICS

PART NO. BA41-00809/810A

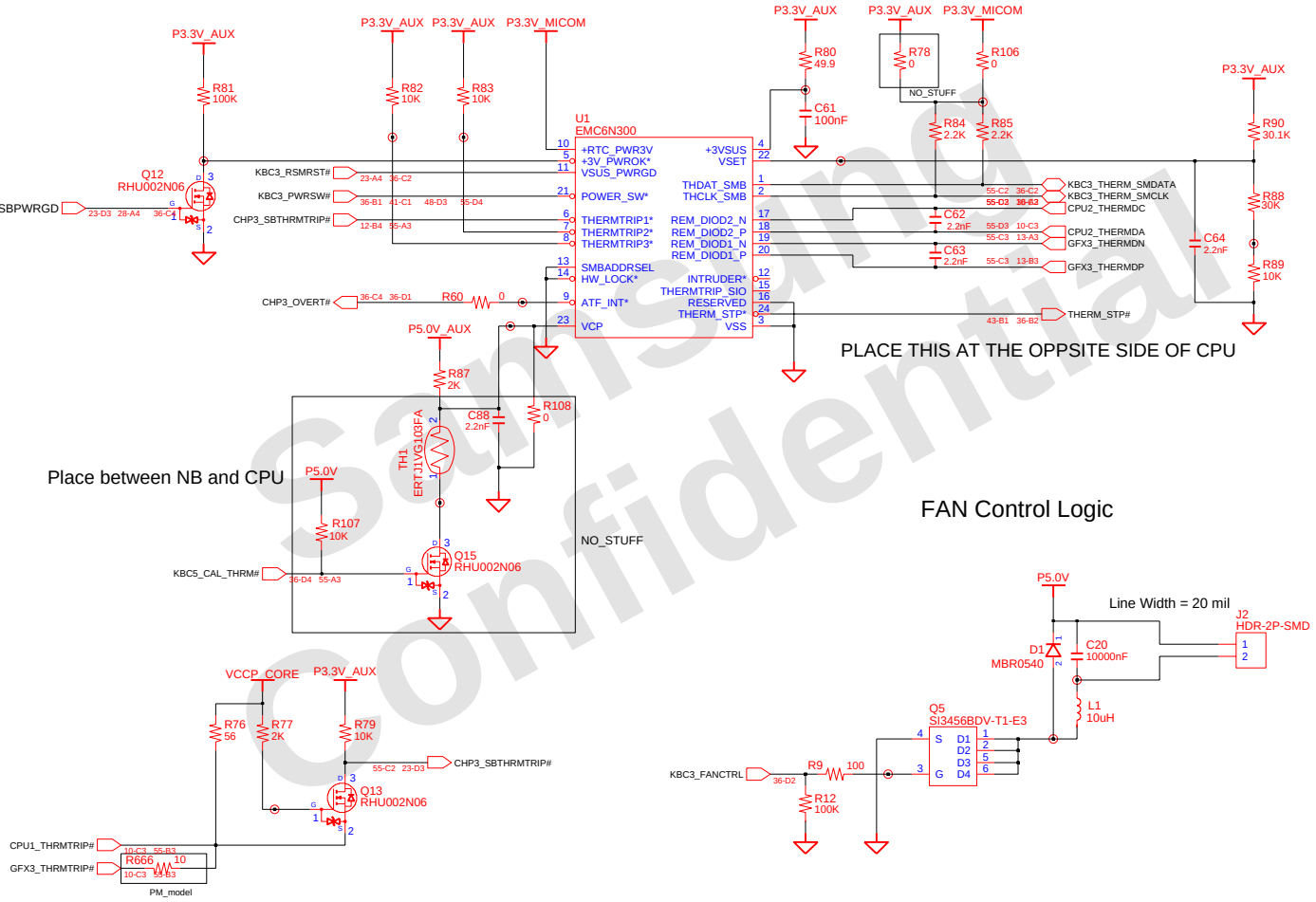


DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	MEROM(3/3)	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM	PAGE 11 OF 53	

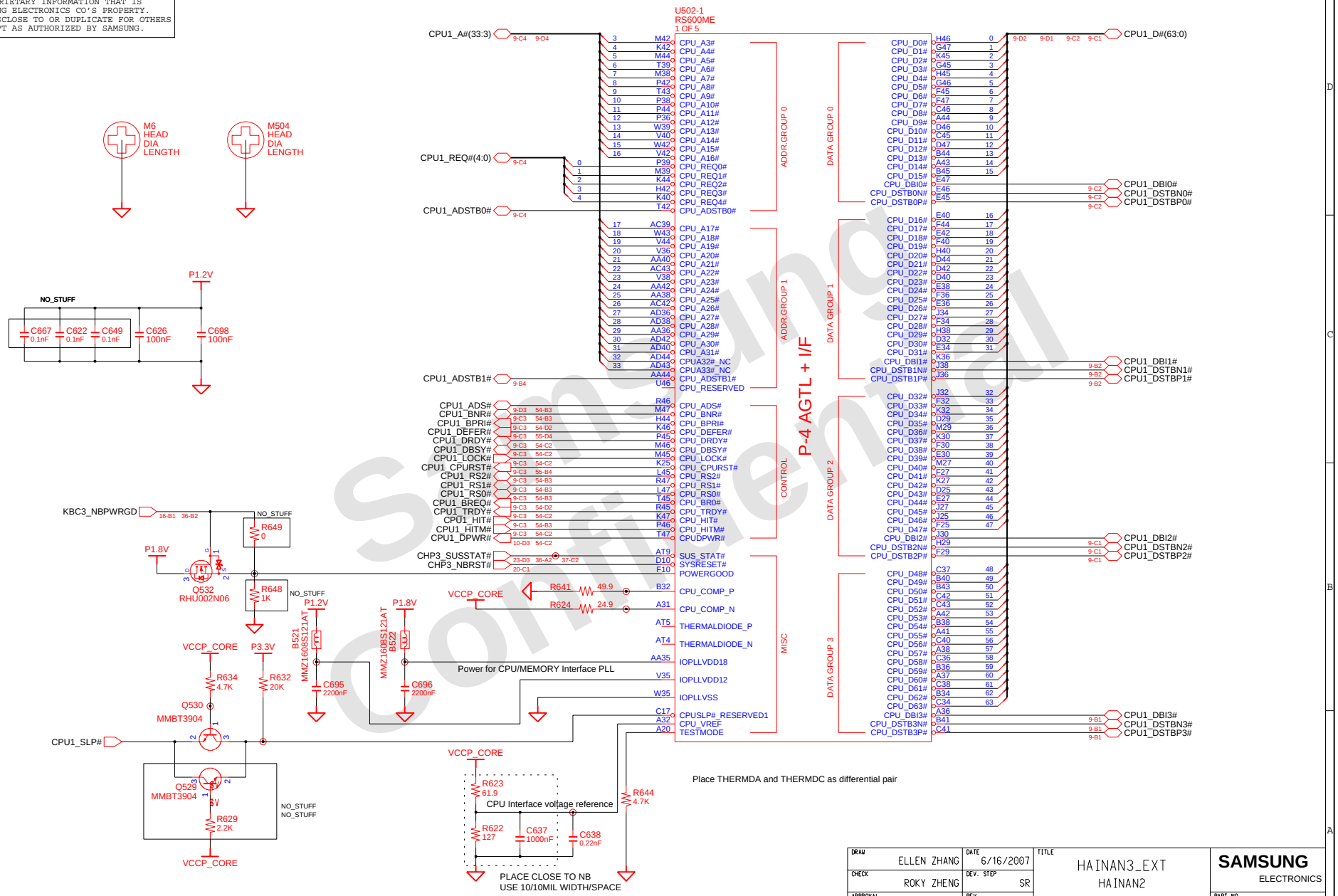
CPU / RS600 Thermal Sensor

Refer To Thermal Sensor Layout Guidelines.

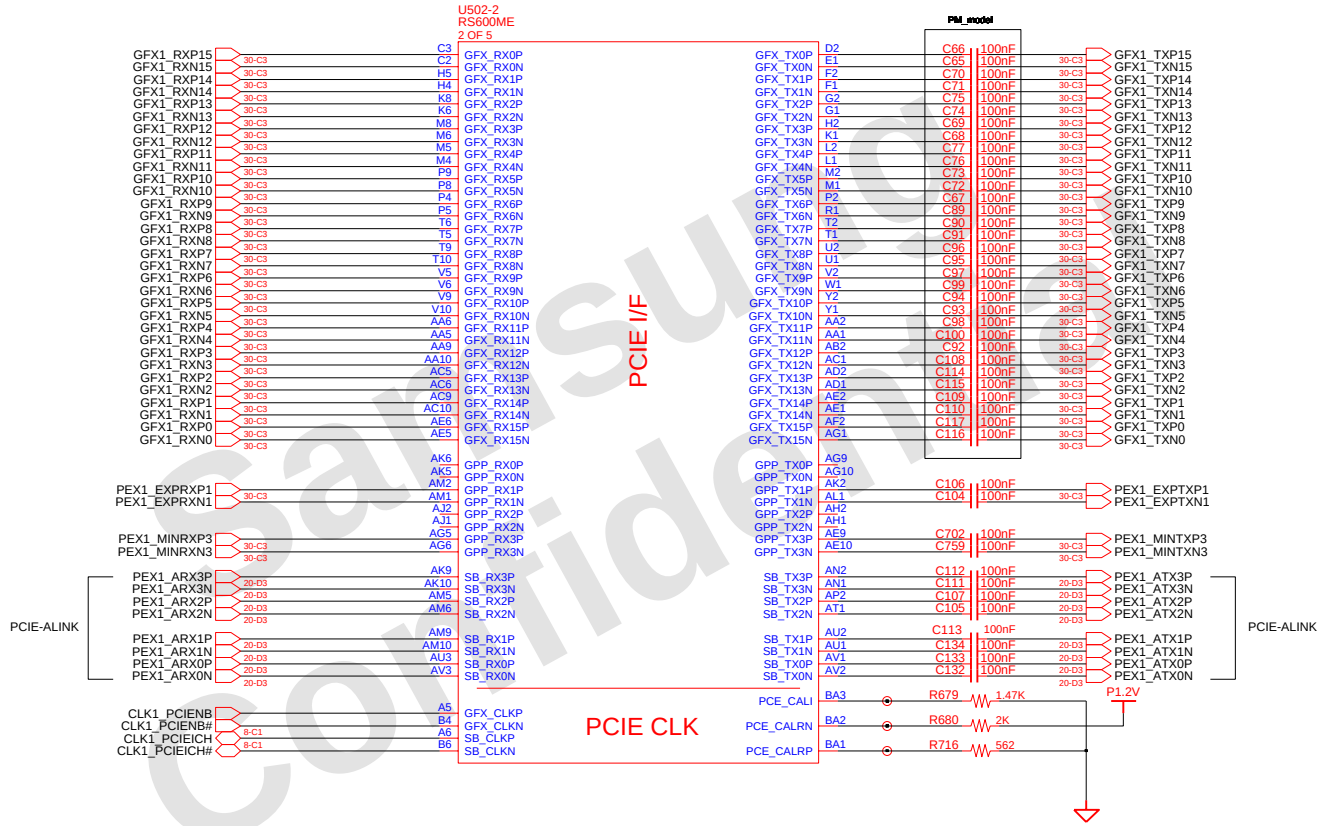
- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND



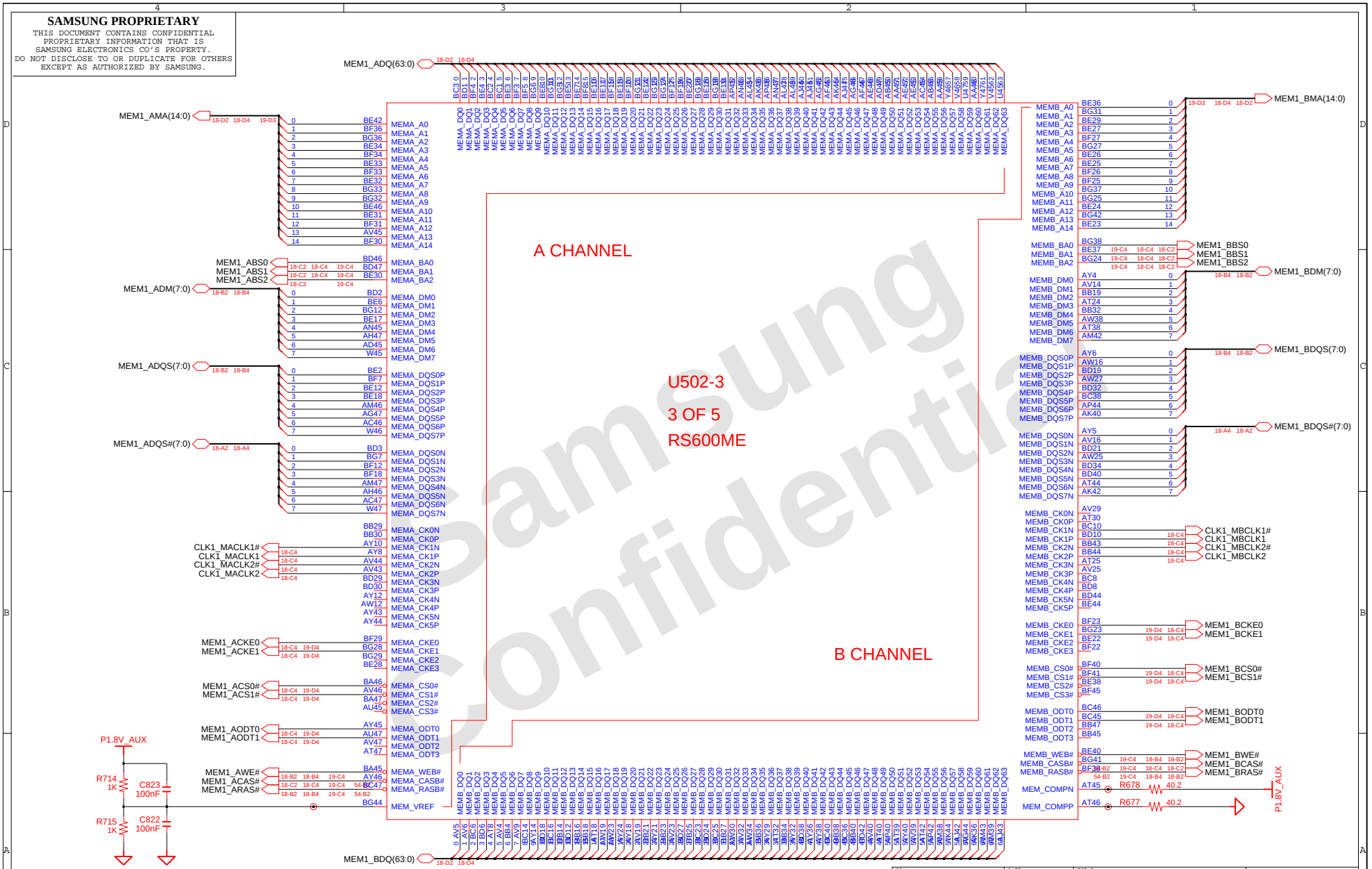
DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	THERMAL & FAN	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 12 OF 53



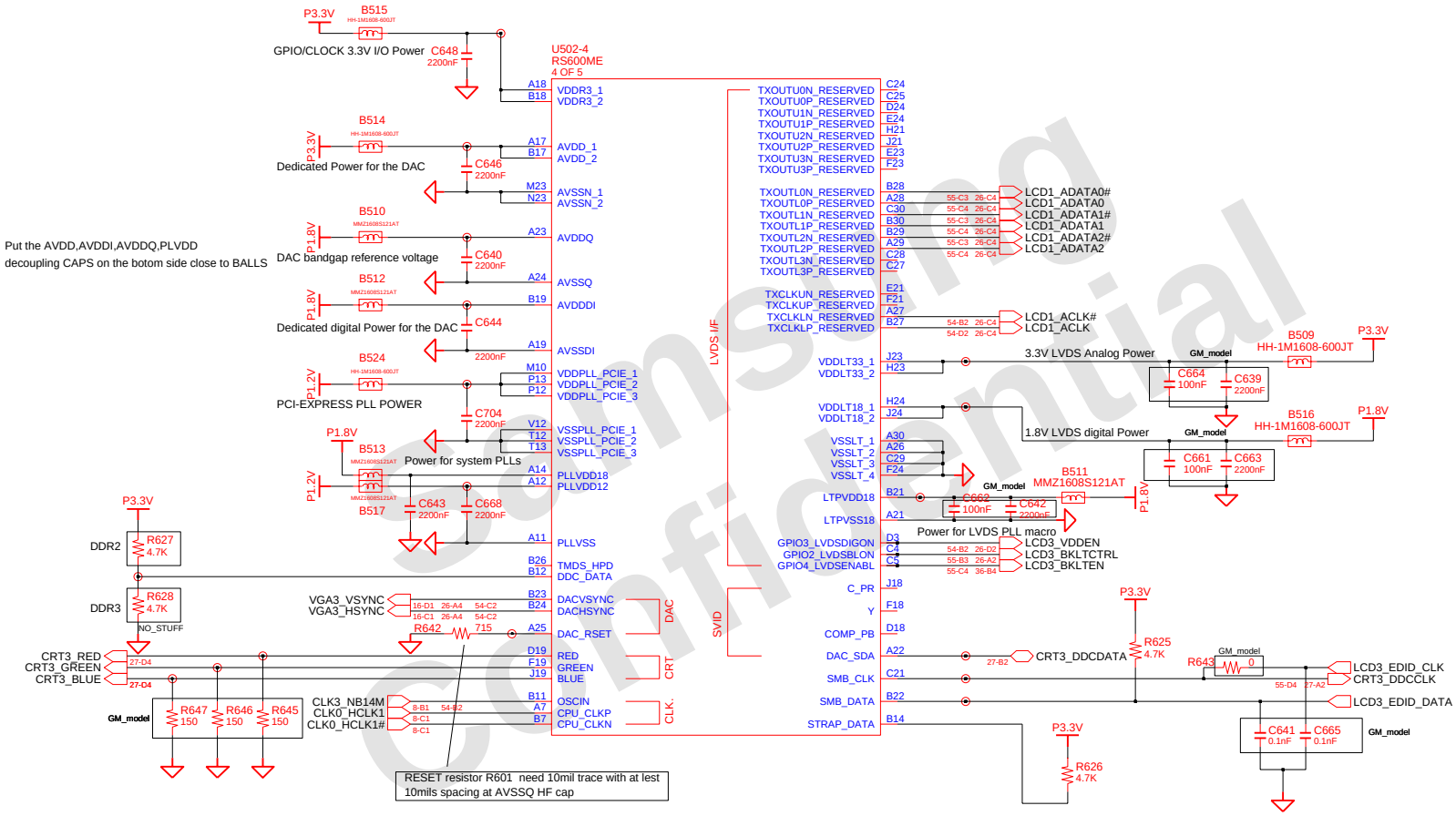
DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT HAINAN2 RS600 (1/5)	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		PART NO. BA41-00809/810A
APPROVAL: KEVIN LEE	REV: 1.0		
MODULE CODE	LAST EDIT: March 23, 2007 11:06:39 AM	PAGE 13 OF 53	



DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT HAINAN2 RS600 (2/5)	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO. BA41-00809/810A
MODULE CODE	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 14 OF 53

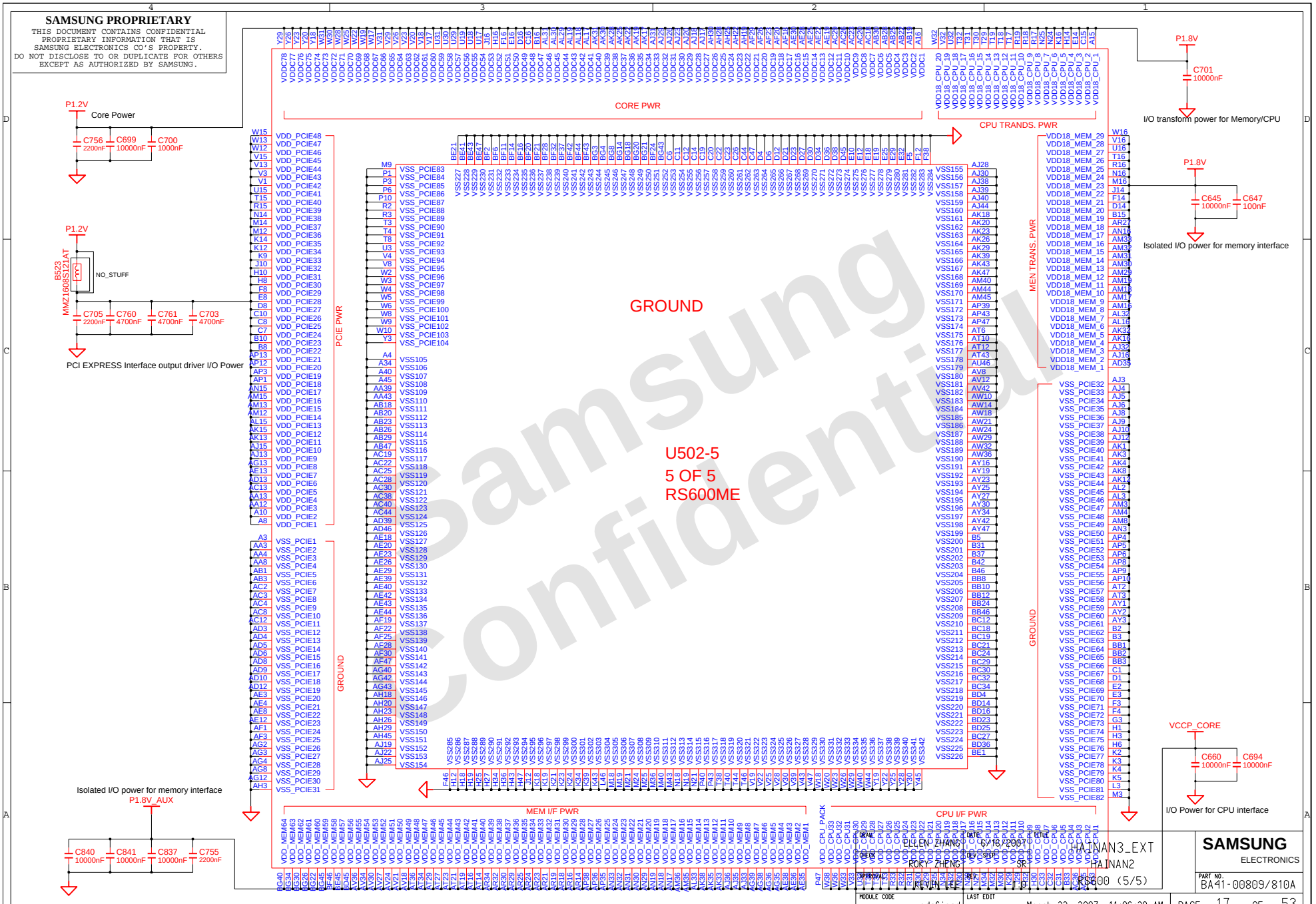


DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT HAINAN2 RS600 (3/5)	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		PART NO. BA41-00809/810A
APPROVAL: KEVIN LEE	REV: 1.0		
MODULE CODE	LAST EDIT: March 23, 2007 11:06:39 AM	PAGE 15 OF 53	



RESET resistor R601 need 10mil trace with at lest
10mils spacing at AVSSQ HF cap

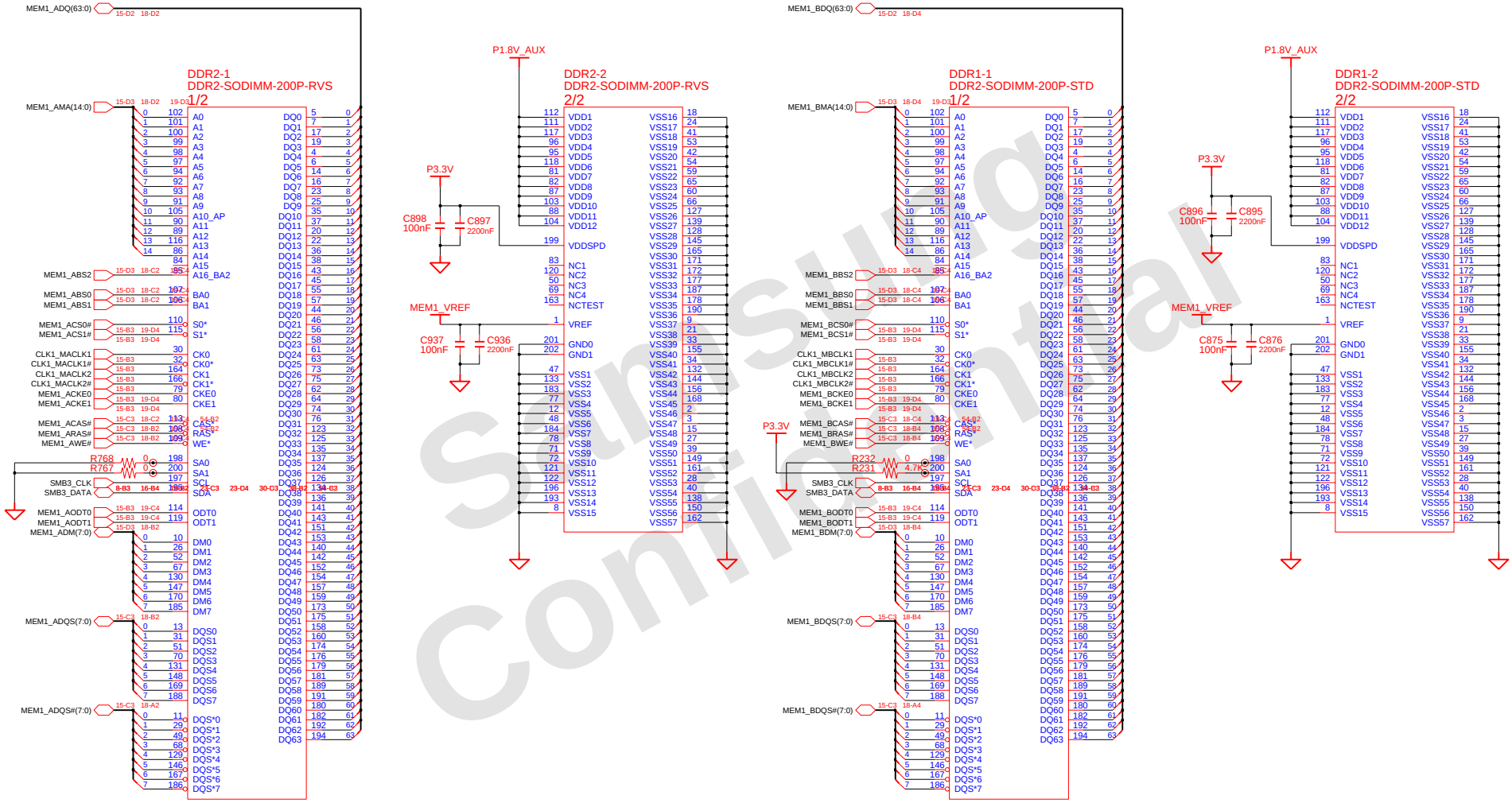
DRAW ELLEN ZHANG	DATE 6/16/2007	TITLE HAINAN3_EXT HAINAN2 RS600 (4/5)	SAMSUNG ELECTRONICS
CHECK ROKY ZHENG	DEV. STEP SR		
APPROVAL KEVIN LEE	REV 1.0		PART NO. BA41-00809/810A
MODULE CODE	LAST EDIT March 23, 2007 11:06:39 AM		PAGE 16 OF 53



DRAWN	ELLEN ZHANG	5/16/2007	HAINAN3_EXT
CHECK	RORY ZHENG		HAINAN2
APPROVAL			RS600 (5/5)
MODULE CODE	undefined	LAST EDIT	March 23, 2007 11:06:39 AM

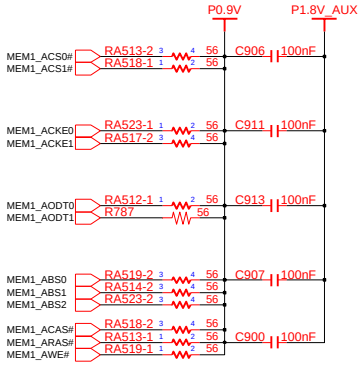
SAMSUNG ELECTRONICS

PART NO. BA41-00809/810A

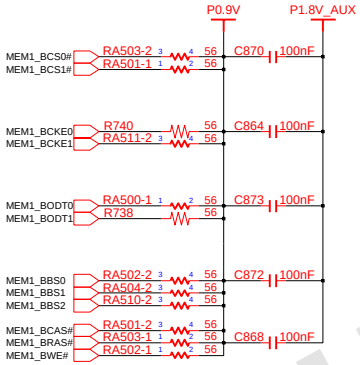


DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	MEMORY SODIMM	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM	PAGE 18 OF 53	

Channel 1

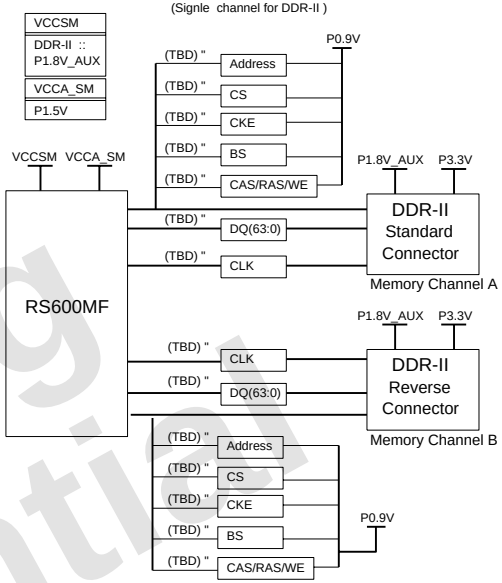


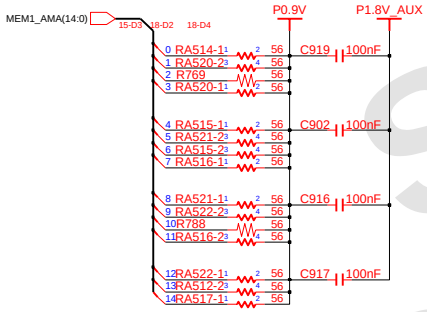
Channel 2

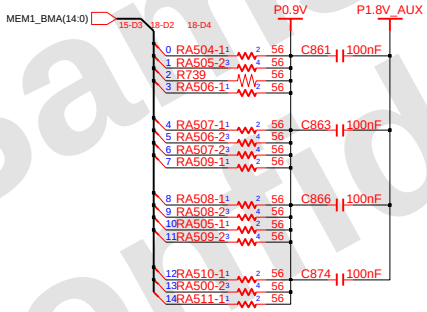


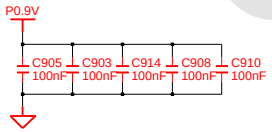
Memory Topology

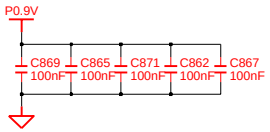
(Signle channel for DDR-II)

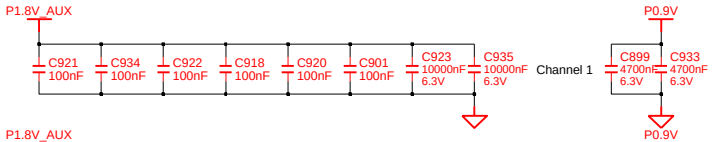


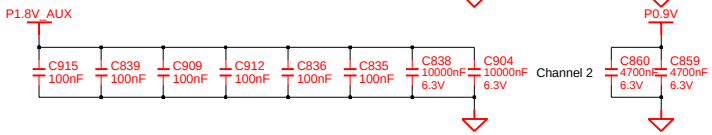




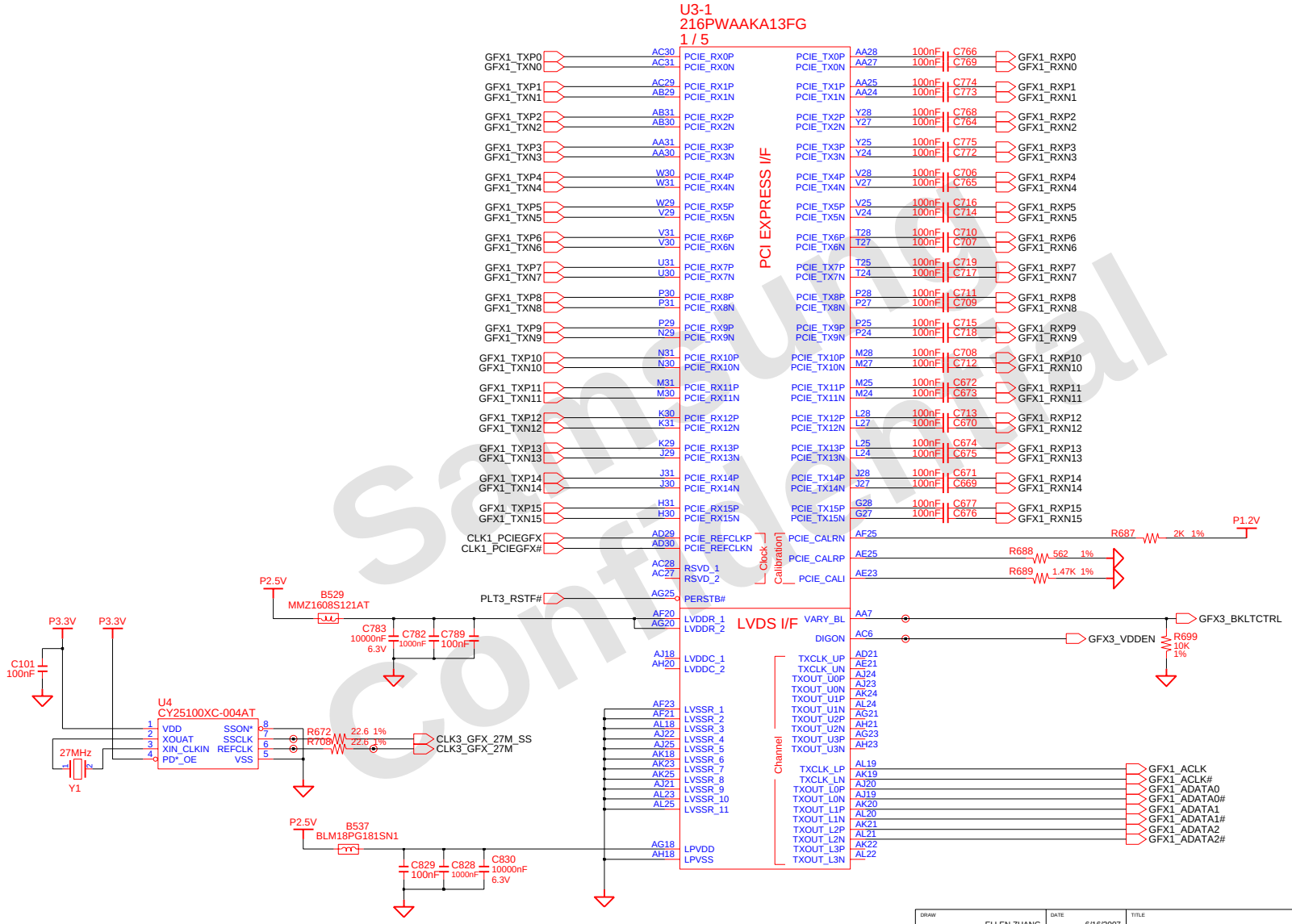




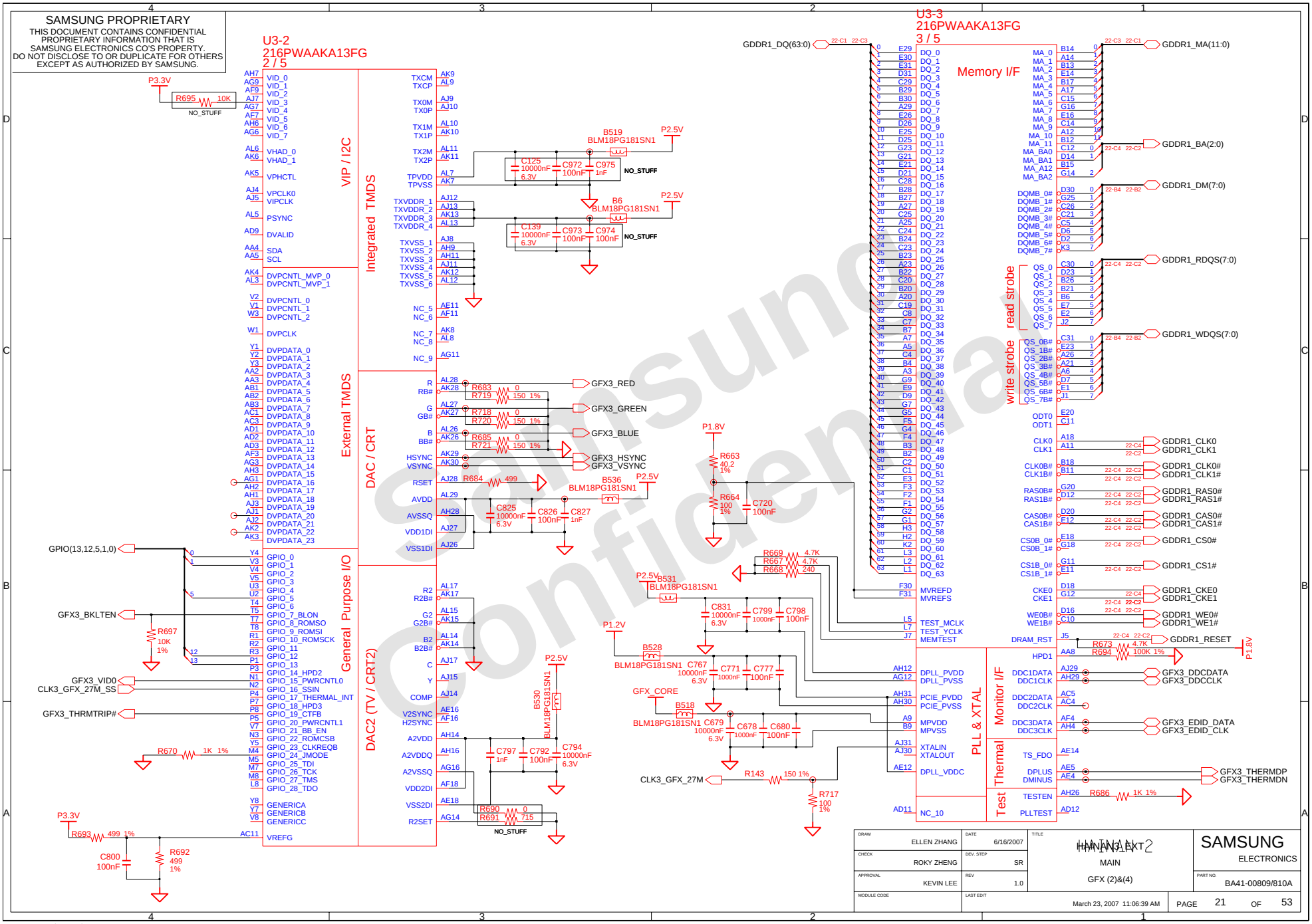


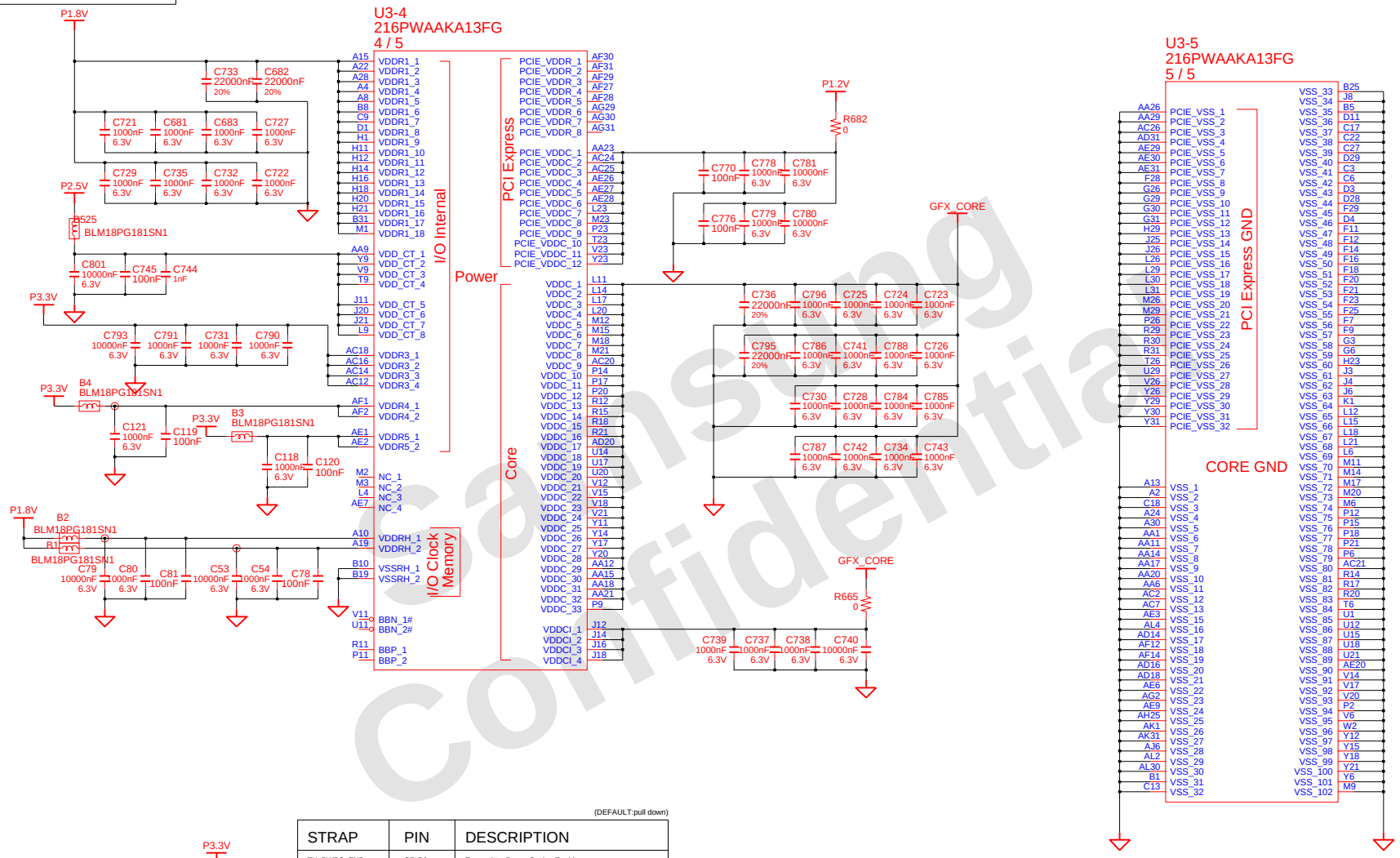


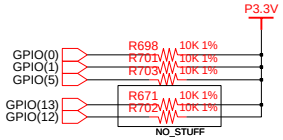
DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	DDR2 TERMINATION	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 19 OF 53



DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT MAIN GFX (1)	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO.: BA41-00809/810A
MODULE CODE	LAST EDIT: March 23, 2007 11:06:39 AM	PAGE 20 OF 53	



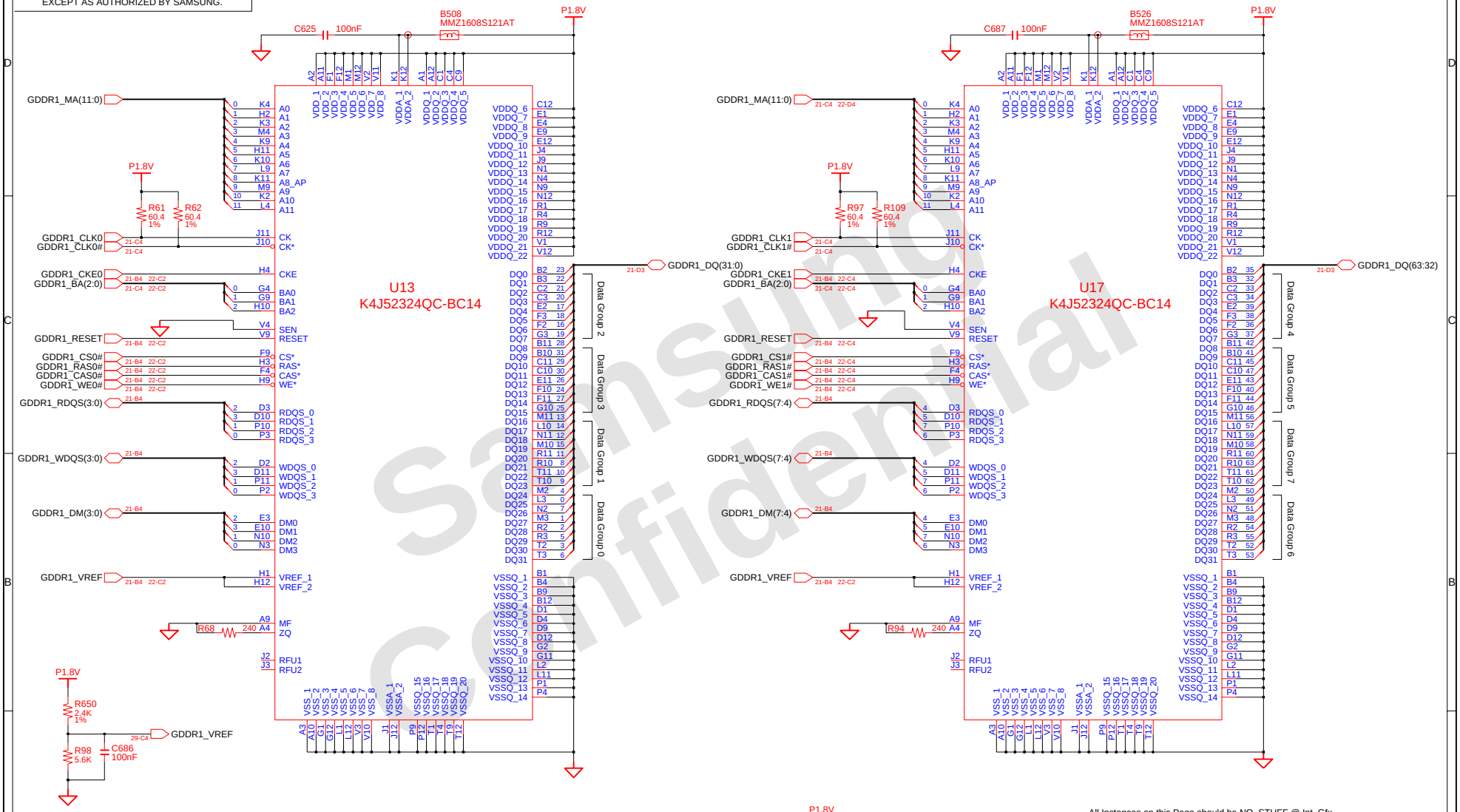




(DEFAULT:pull down)

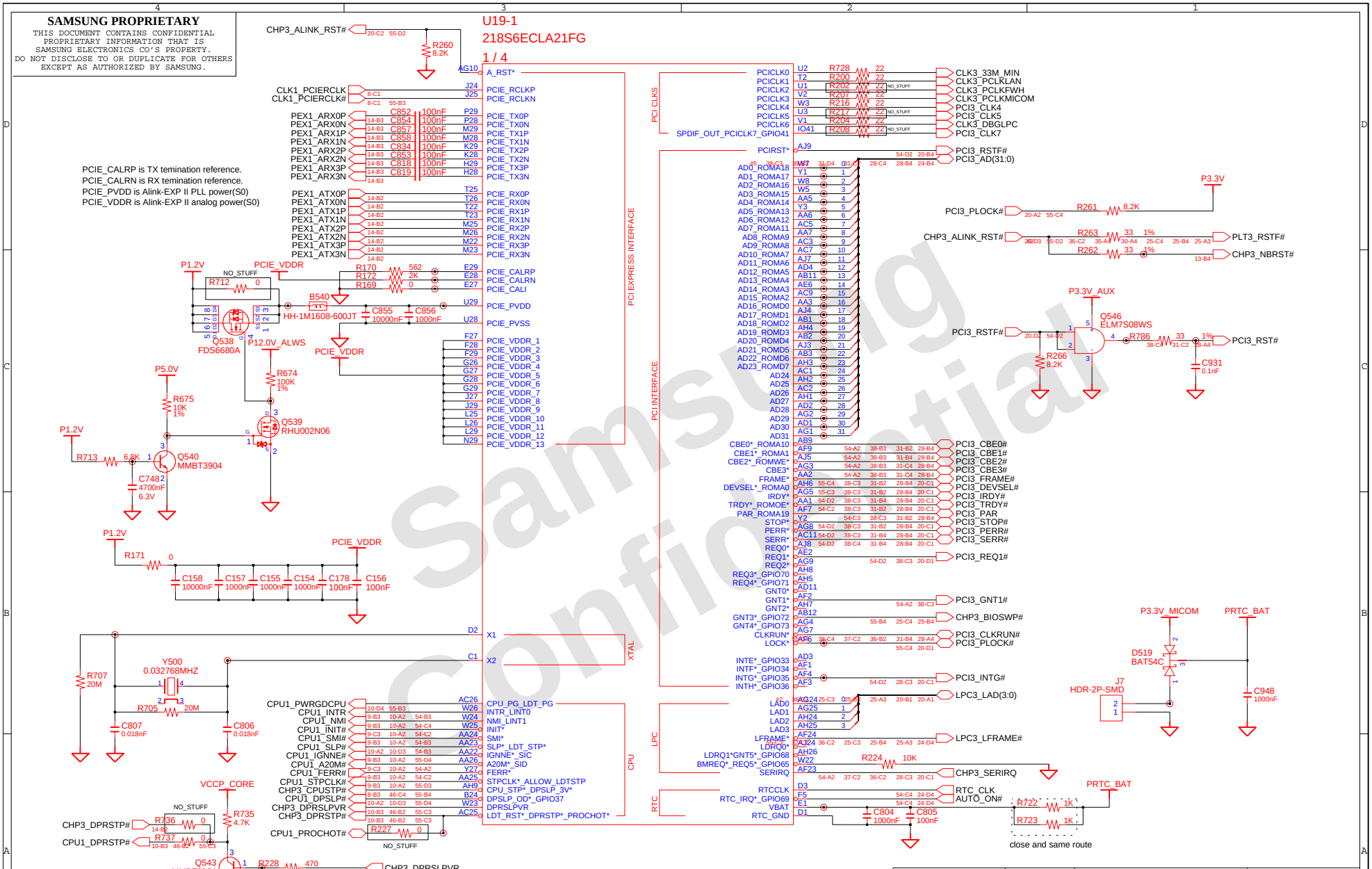
STRAP	PIN	DESCRIPTION
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0:50% Tx output swing 1:full Tx output swing
TX_DEEMPH_EN	GPIO1	Transmitter De_emphasis Enable 0:Tx De_emphasis disable 1:TX De_emphasis enable
PLL_IBIAS_RD	GPIO[6:5]	Bias Current for the PCI Express PHY PLL GPIO5=1 GPIO6=0
Memory aperture size	GPIO[13:12]	GPIO[13:12]=00 128M GPIO[13:12]=01 256M GPIO[13;12]=10 64M GPIO[13:12]=11 RESERVED

DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT MAIN GFX (3)	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		PART NO.: BA41-00809/810A
APPROVAL: KEVIN LEE	REV: 1.0		
MODULE CODE	LAST EDIT: March 23, 2007 11:06:39 AM	PAGE 22 OF 53	

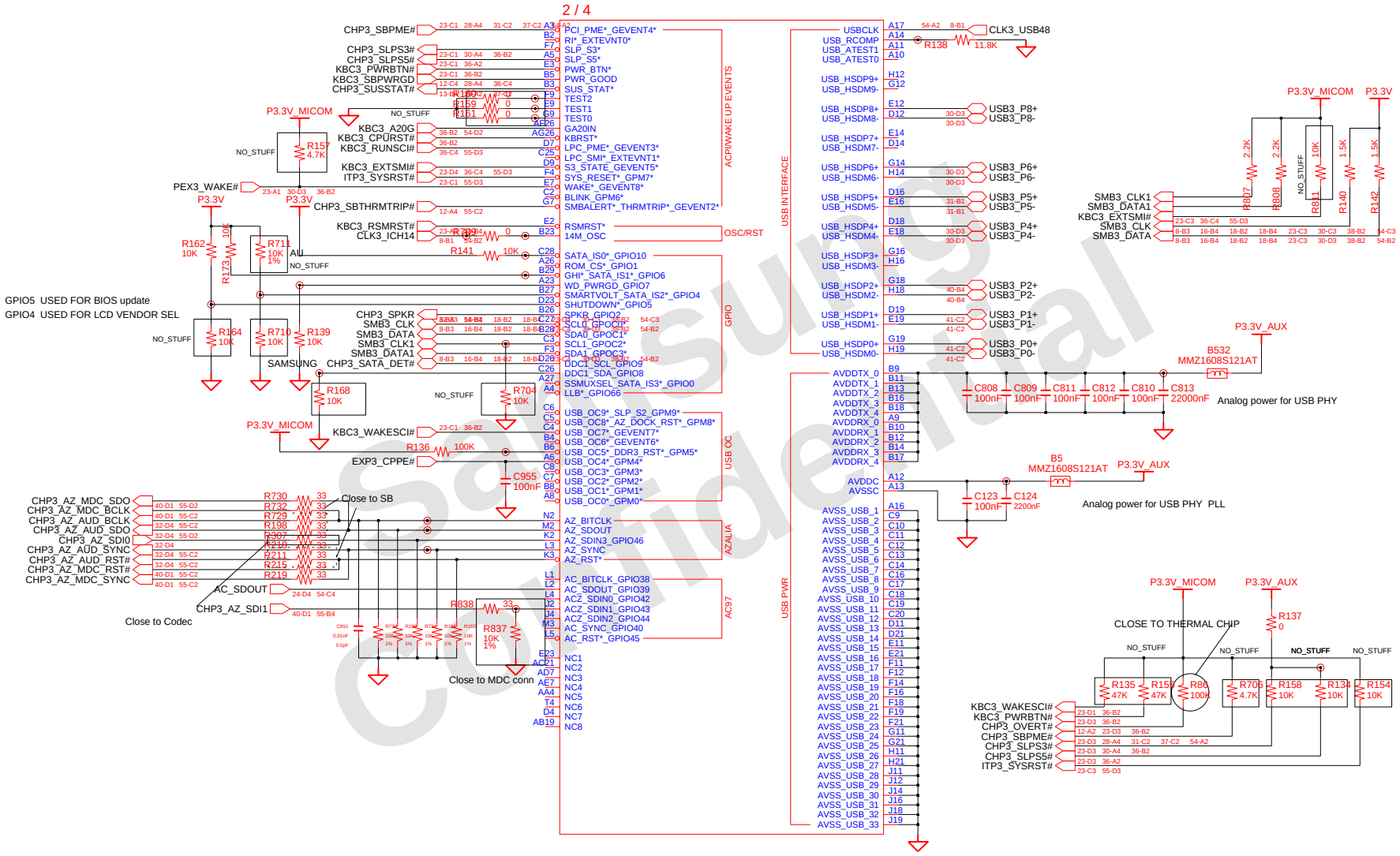


All Instances on this Page should be NO_STUFF @ Int. Gfx.

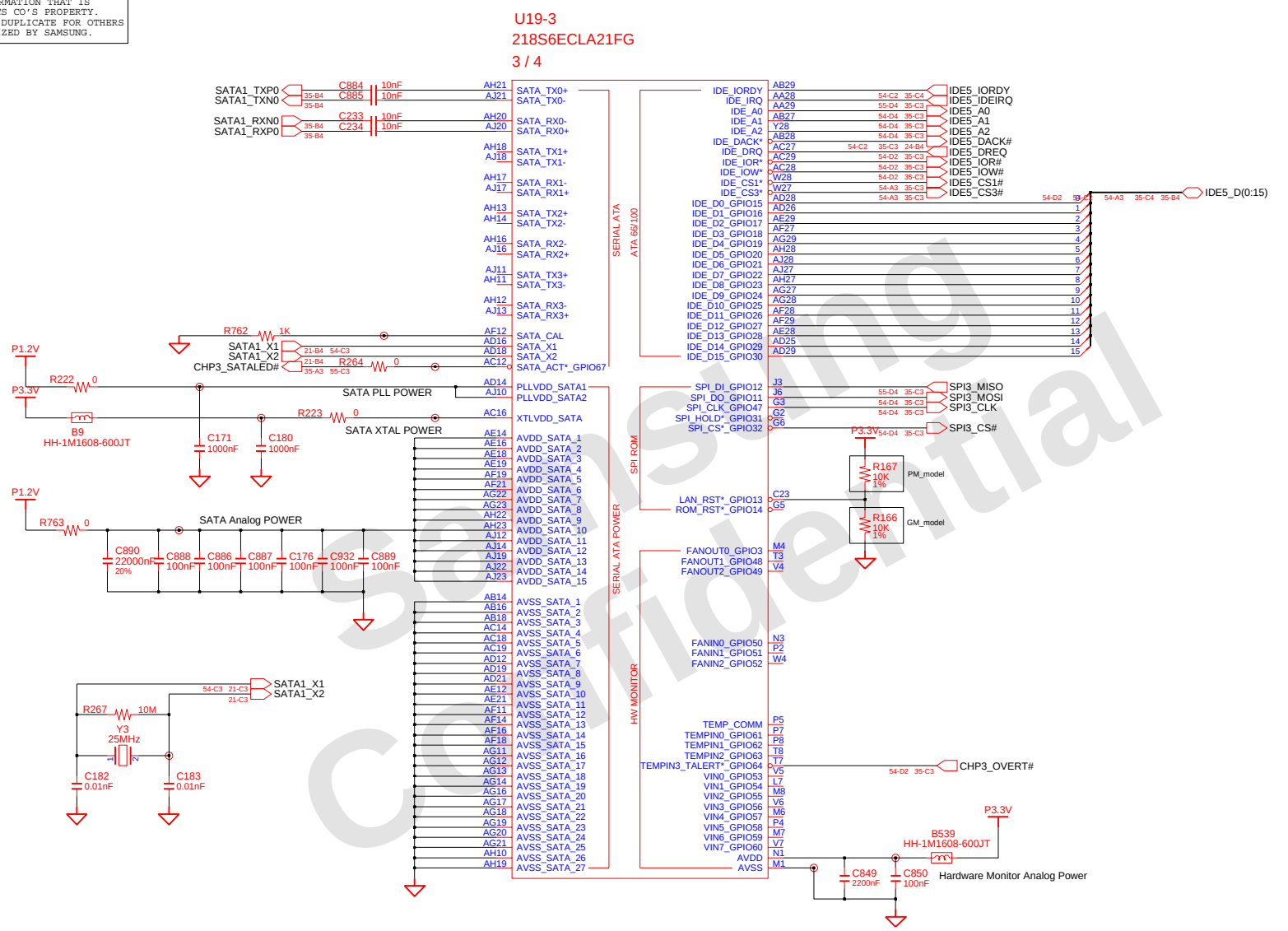
DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT MAIN GFX MEMORY	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO. BA41-00809/810A
MODULE CODE	LAST EDIT: March 23, 2007 11:06:39 AM	PAGE 23 OF 53	



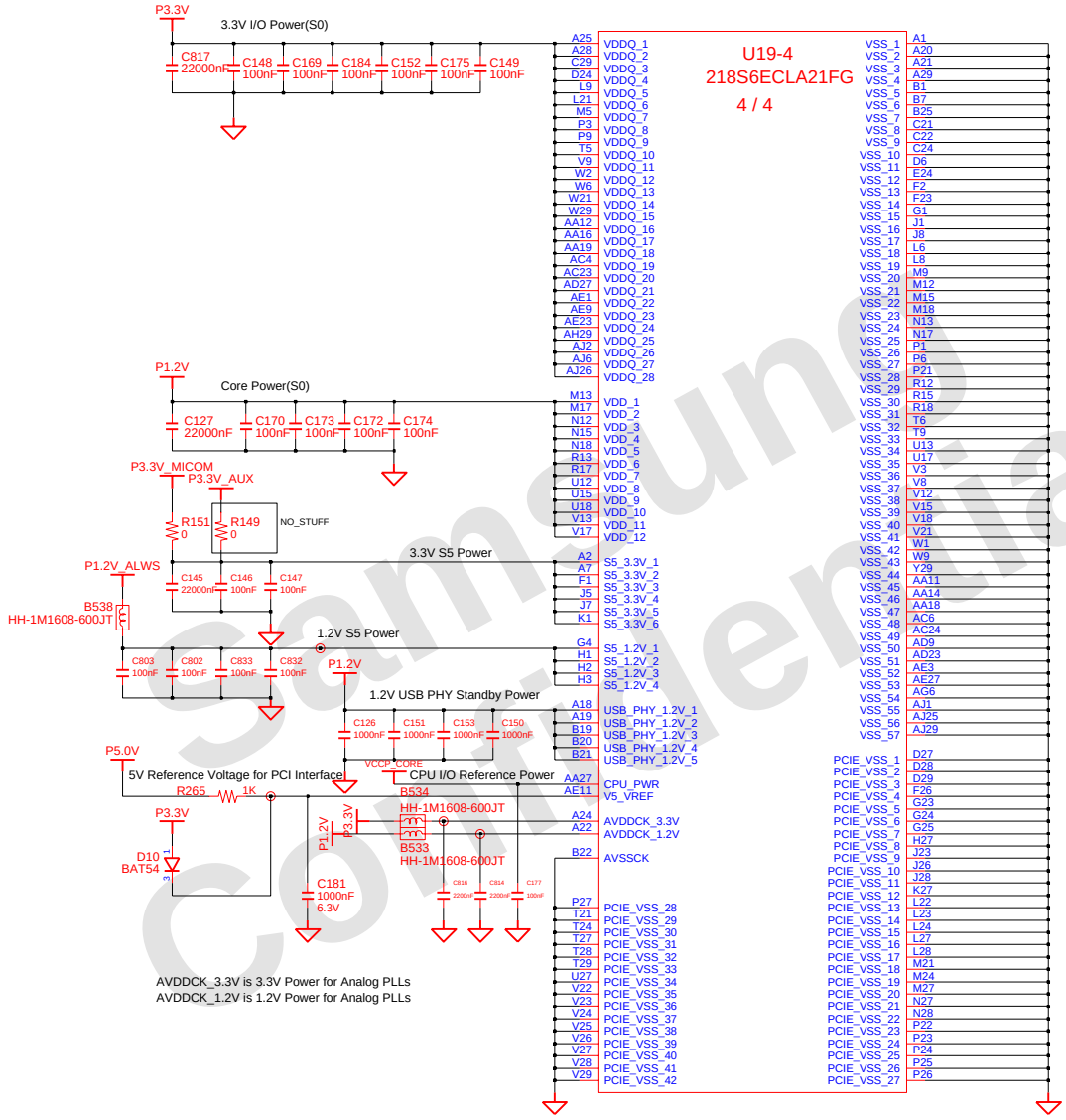
DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR	SB600(1/4)	
APPROVAL: KEVIN LEE	REV: 1.0		PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 24 OF 53



DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	SB600(2/4)	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM	PAGE 25 OF 53	

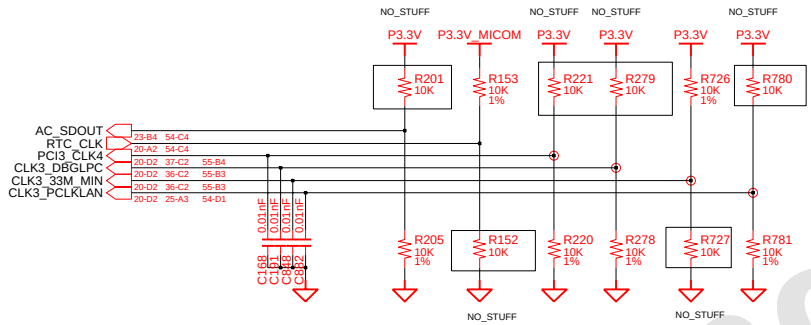


DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	SB600(3/4)	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM	PAGE 26 OF 53	



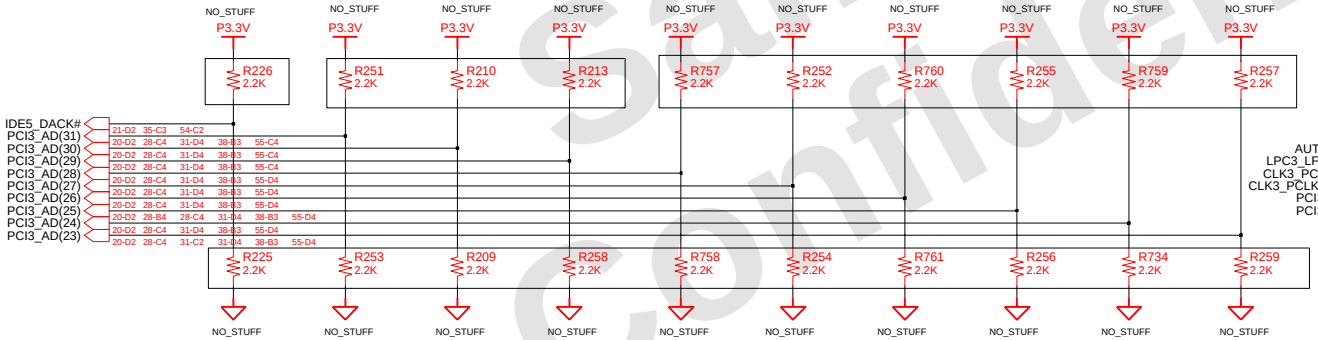
DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	SB600(4/4)	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM	PAGE 27 OF 53	

REQUIRED SYSTEM STRAPS



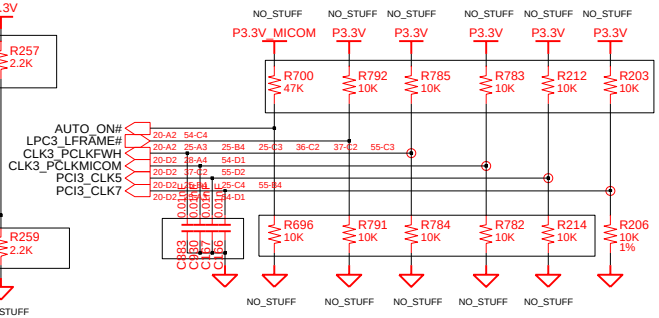
	AC_SDOUT	RTC_CLK	PCI3_CLK4	CLK3_DBGLPC	CLK3_33M_MIN,CLK3_PCLKLAN
STRAP HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT PLL 48	CPU I/F = K8	ROM TYPE H,H = PCI ROM H,L = SPI ROM L,H = LPC ROM L,L = FWH ROM
STRAP LOW	IGNORE DEBUG STRAPS DEFAULT	EXRERNAL RTC	USE EXT 48MHZ DEFAULT	CPU I/F = P4 DEFAULT	

DEBUG STRAPS

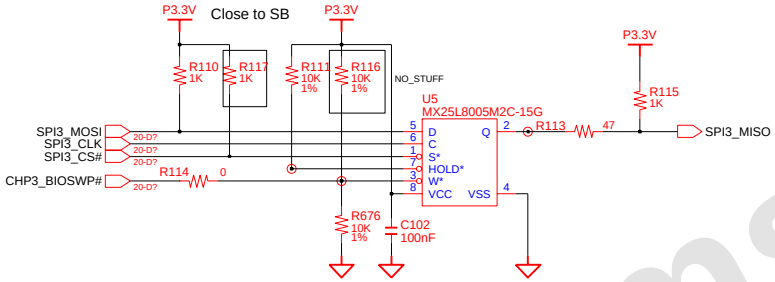


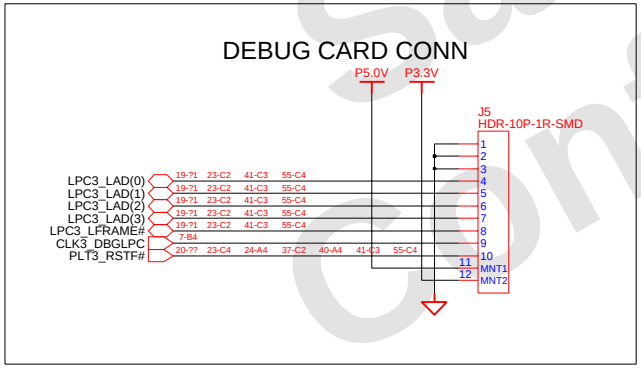
	IDE5_DACK*	PCI3_AD(31)	PCI3_AD(30)	PCI3_AD(29)	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	RESERVED	RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTF ALL TIMER DISABLED DEFAULT
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	BYPASS EEPROM PCIE STRAPS	BOOTF ALL TIMER ENABLED

RESERVED PORT DEBUG



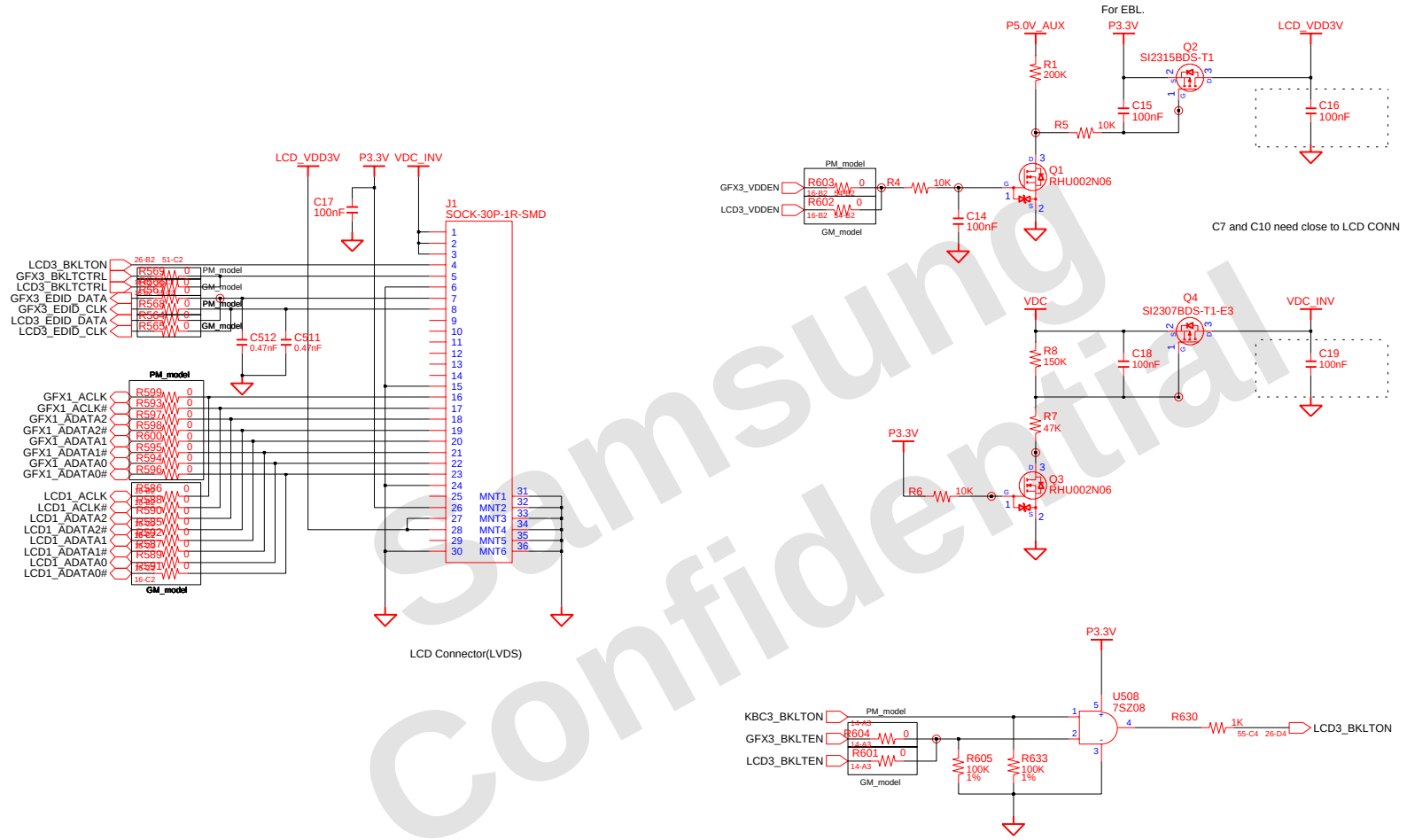
DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR	SB600 STRAPS	
APPROVAL: KEVIN LEE	REV: 1.0		PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 28 OF 53





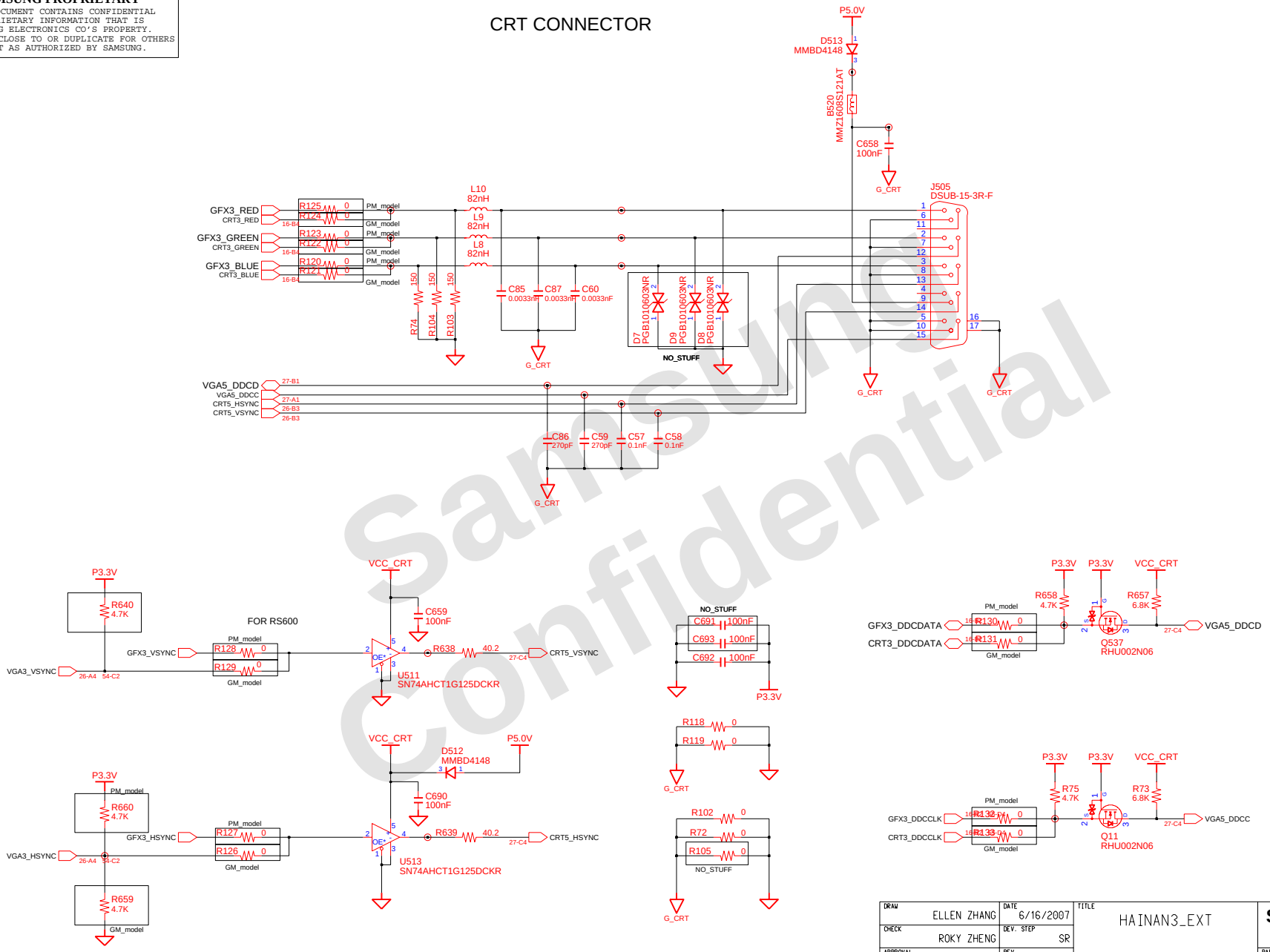
02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD EERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
OE	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET WITH INITIAL POST VALUE	86	RE-INIT. ON-BOARD I/O PORT
		88	INIT. BIOS DATA ROM
14	INIT. KEYBOARD CONTROLLER	8A	INIT.EXTENDED BIOS DATA AREA
16	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
18	8254 TIMER INIT.	9A	SHADOW OPTION ROMS
1A	8237 DMA CONTROLLER INIT.	9C	SETUP POWER MANAGEMENT
1C	RESET INTERRUP CONTROLLER	9E	ENABLE H/W INTERRUPT
20	TEST DRAM REFRESH	A0	SET TIME OF DAY
22	TEST 8742 KEYBOARD CONTROLLER	A4	INIT. TYPEMATIC RATE
24	SET ES SEGMENT REG. TO 4GB	A8	ERASE F2 PROMPT
26	ENABLE A20	AA	SCAN FOR F2 KEY STROKE
28	AUTO SIZING DRAM	AC	ENTER SETUP
32	COMPUTE THE CPU SPEED	AE	CLEAR IN POST FLAG
34	TESET CMOS RAM	B0	CHECK FOR ERRORS
38	SHADOW SYSTEM BIOS ROM	B2	POST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B4	ONE BEEP
3C	CONFIGURE ADVANCED CHIPSET REG.	B6	CHECK PASSWORD (OPTION)
3D	LOAD ALTER REG. WITH CMOS VALUE	B7	ACPI INIT
42	INIT. INTERRUPT VECTOR	BA	DMI INIT
44	INIT. BIOS INTERRUPT	BE	CLEAR SCREEN
46	CHECK ROM COPYRIGHT NOTICE	C0	TRY BOOT WITH INT19
47	INIT. I20 SUPPORT IF INSTALLED	D0	INTERRUPT HANDLER ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D2	UNKNOWN INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D4	PENDING INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D6	SHUTDOWN 5
4C	SHADOW VIDEO BIOS ROM	D8	SHUTDOWN ERROR
50	DISPLAY CPU TYPE AND SPEED	DA	EXTENDED BLOCK MOVE
52	TEST KEYBOARD	DC	SHUTDOWN 10
54	SET KEYCLICK IF ENABLED	89	ENABLE NMI
56	ENABLE KEYBOARD	90	INIT. HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	91	INIT. LOCAL BUS HDD CONTROLLER
5A	DISPLAY " PRESS ..... SETUP"	92	JUMP TO USER PATCH 2
5C	TEST RAM GETWEEN 512K AND 640K	94	DISABLE A20 ADDRESS LINE
60	TEST EXTENDED MEMORY	96	CLEAR HUGE ES SEGMENT REG.
62	TEST EXTENDED MEMORY ADDRESS LINE	98	SEARCH FOR OPTION ROMS
64	JUMP TO USER PATCH 1		

DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	FWH	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 29 OF 53



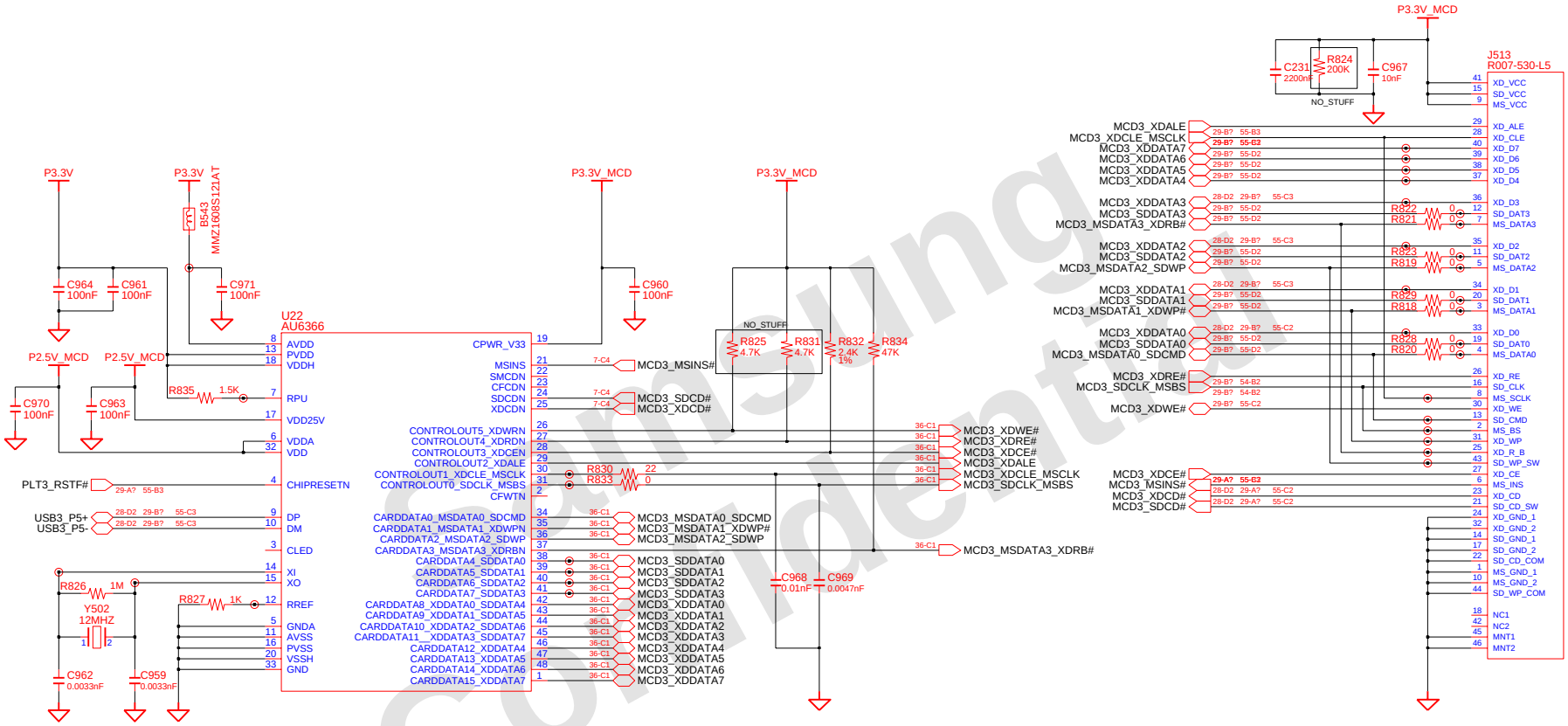
DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	LCD	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 30 OF 53

CRT CONNECTOR



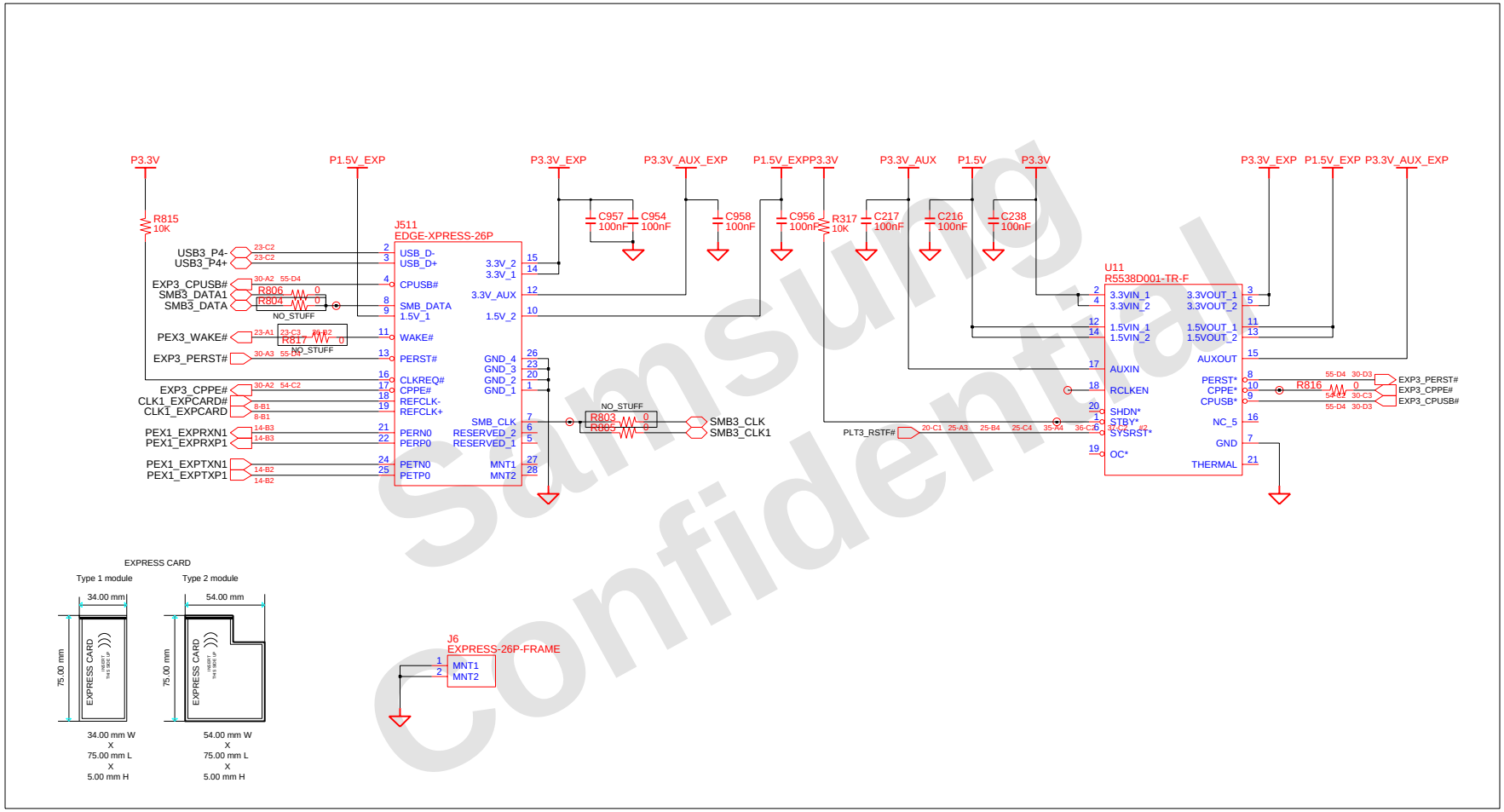
DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	CRT	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM	PAGE 31 OF 53	

4 IN 1 CARD



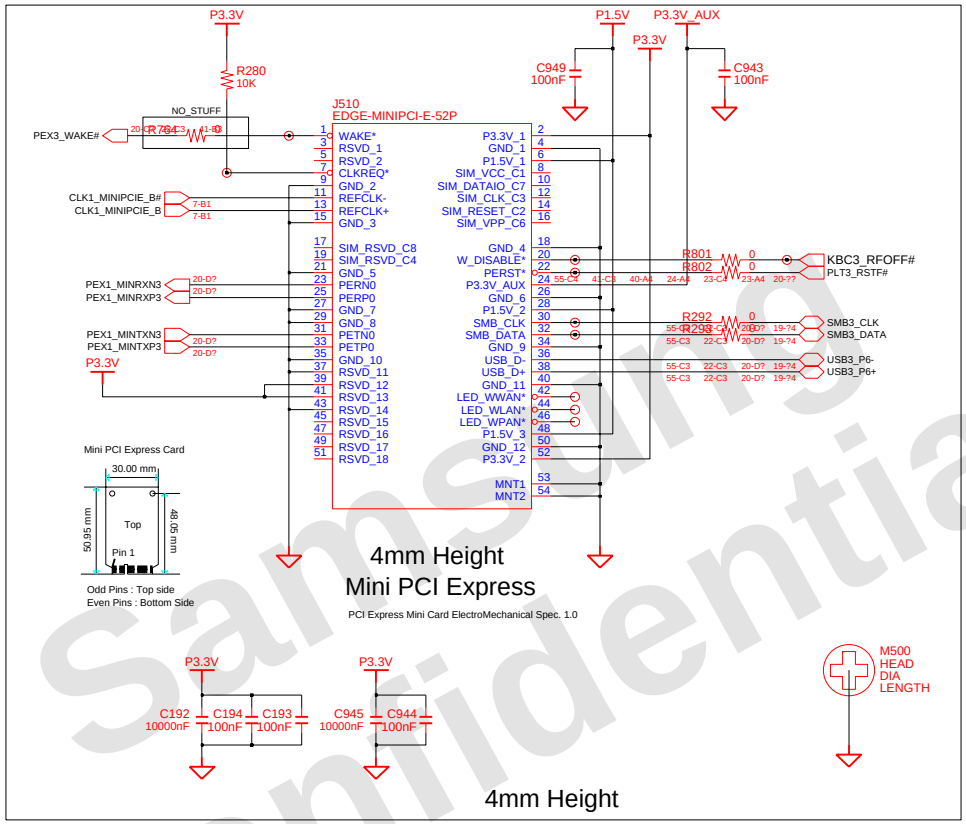
DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	4 IN 1 CARD	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 32 OF 53

EXPCARD

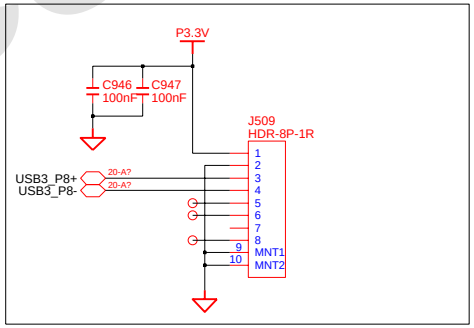


DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	EXPRESS CARD	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 33 OF 53

MINI CARD



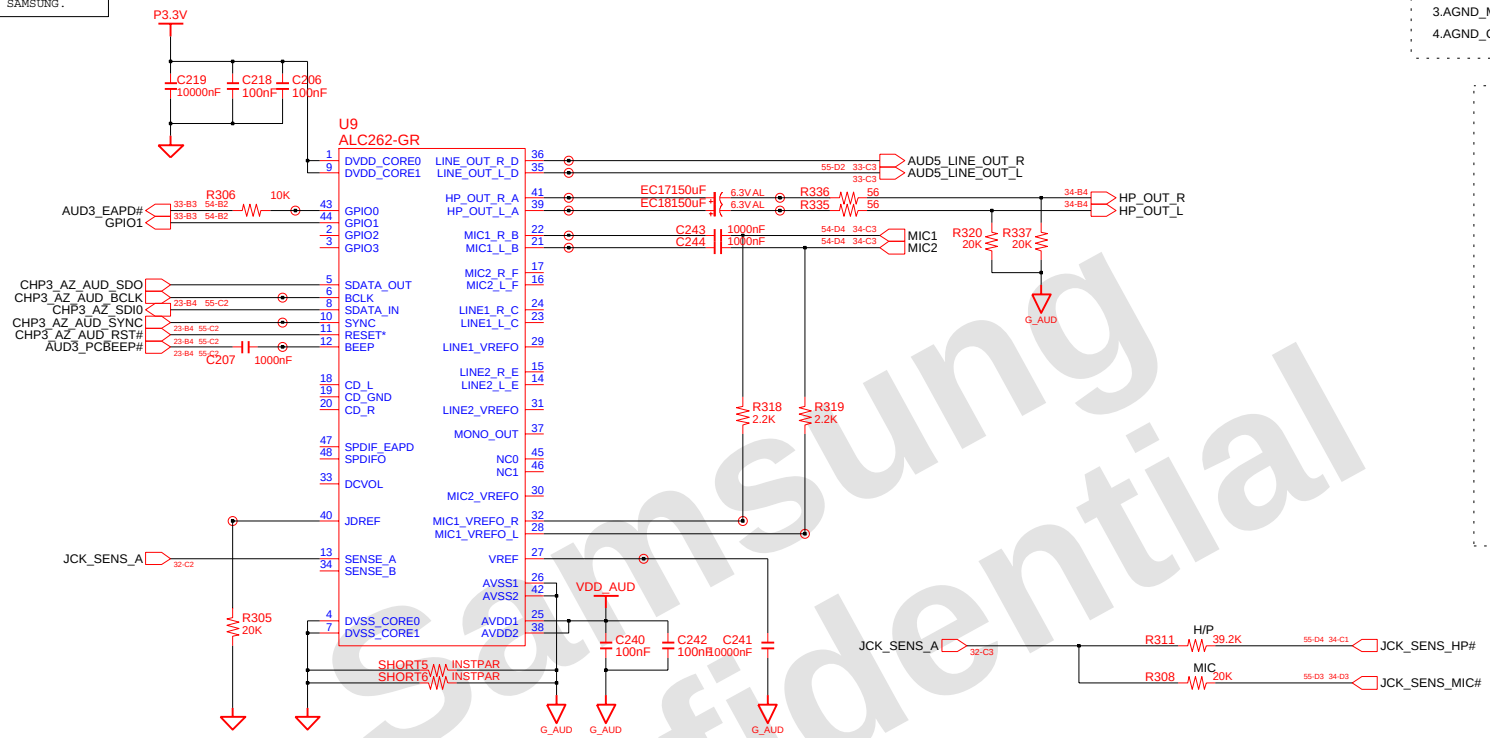
Bluetooth Interface

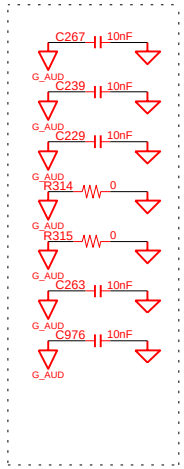


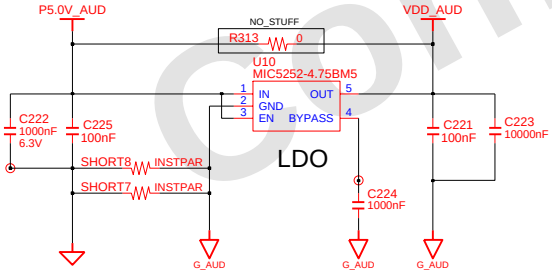
DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT HAINAN2 MINI CARD	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 34 OF 53

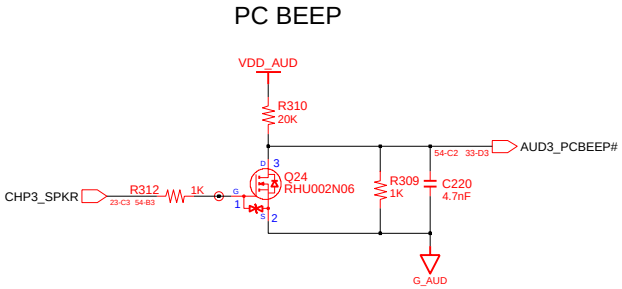
1.AGND_AUD IS AUDIO GROUND
2. GND IS DIGITAL GROUND
3.AGND_MIC IS MIC GROUND
4.AGND_CHS IS CHASS GROUND

ALL TYPE IS 1608

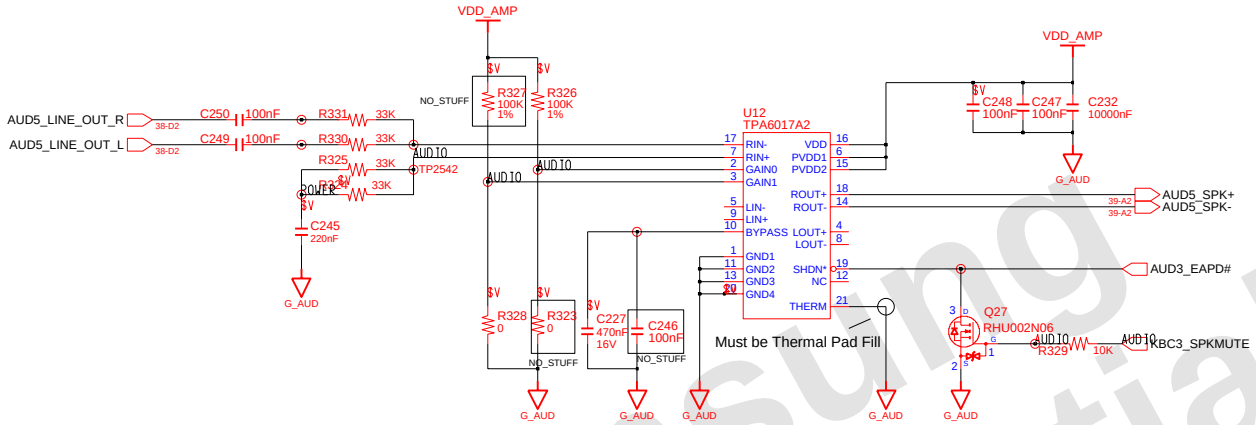


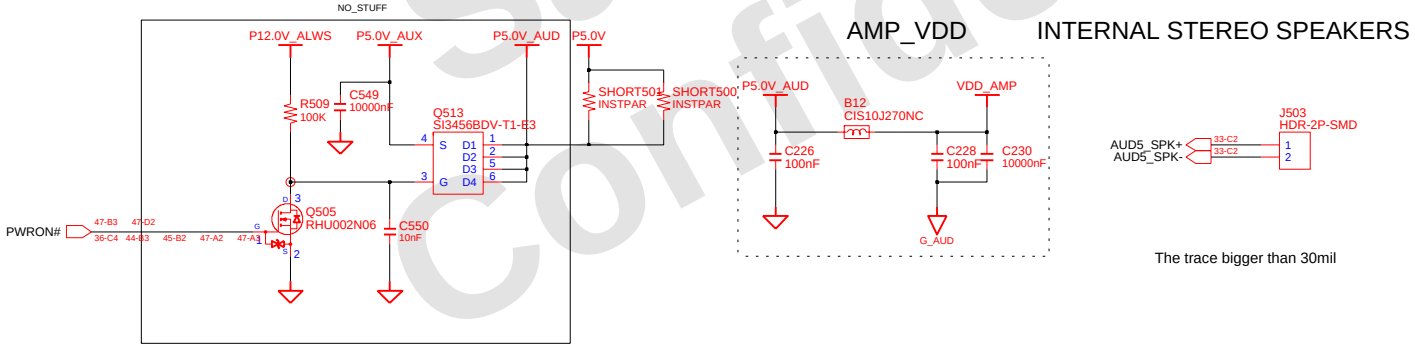






DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	AUDIO(1/3)	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 35 OF 53

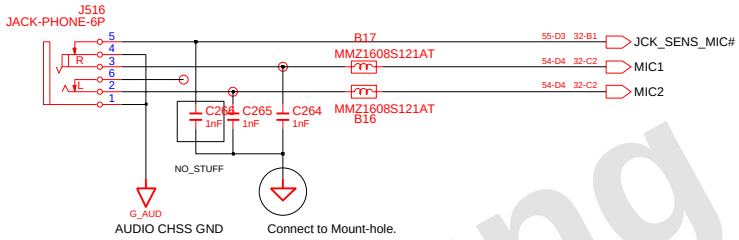




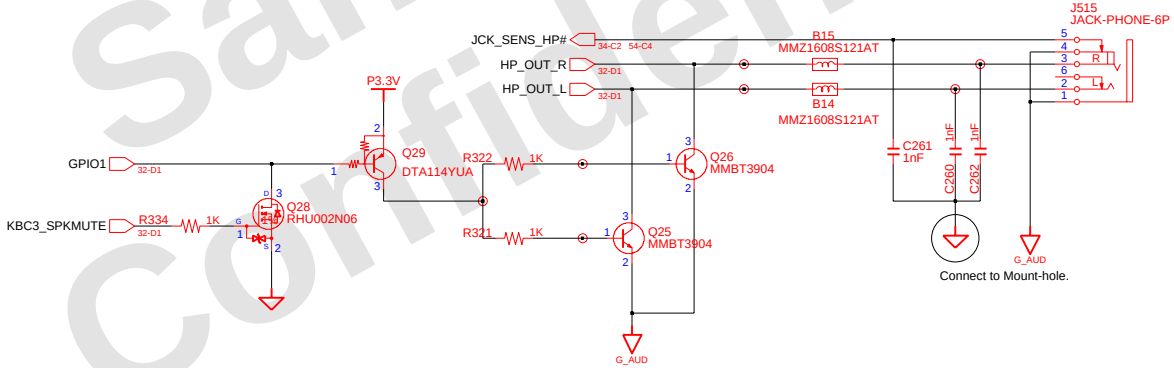
The trace bigger than 30mil

DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	AUDIO(2/3)	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM	PAGE 36 OF 53	

MIC JACK



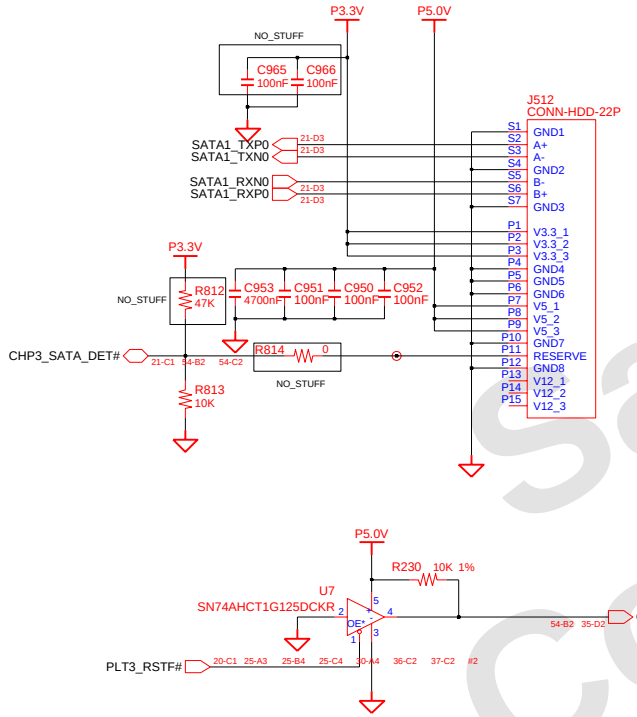
HEADPHONE



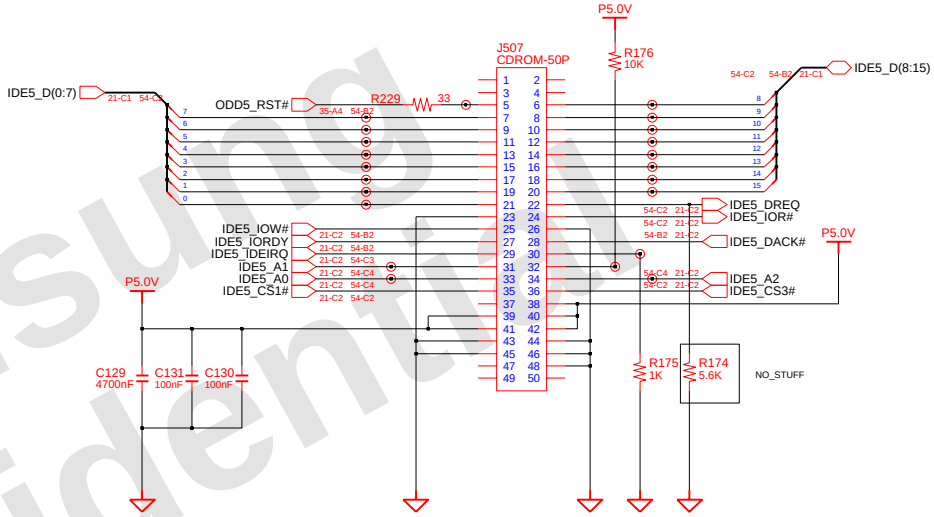
The traces led to Audio Jacks have the width over 10mil

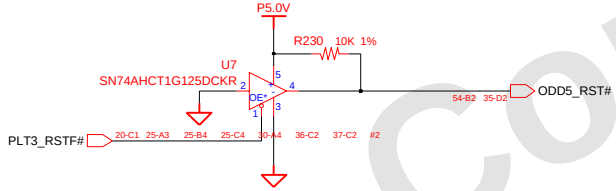
DRAW ELLEN ZHANG	DATE 6/16/2007	TITLE HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK ROKY ZHENG	DEV. STEP SR		
APPROVAL KEVIN LEE	REV 1.0	AUDIO(3/3)	PART NO. BA41-00809/810A
MODULE CODE undefined	LAST EDIT March 23, 2007 11:06:39 AM		PAGE 37 OF 53

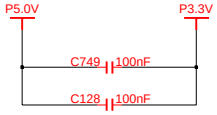
Main to HDD



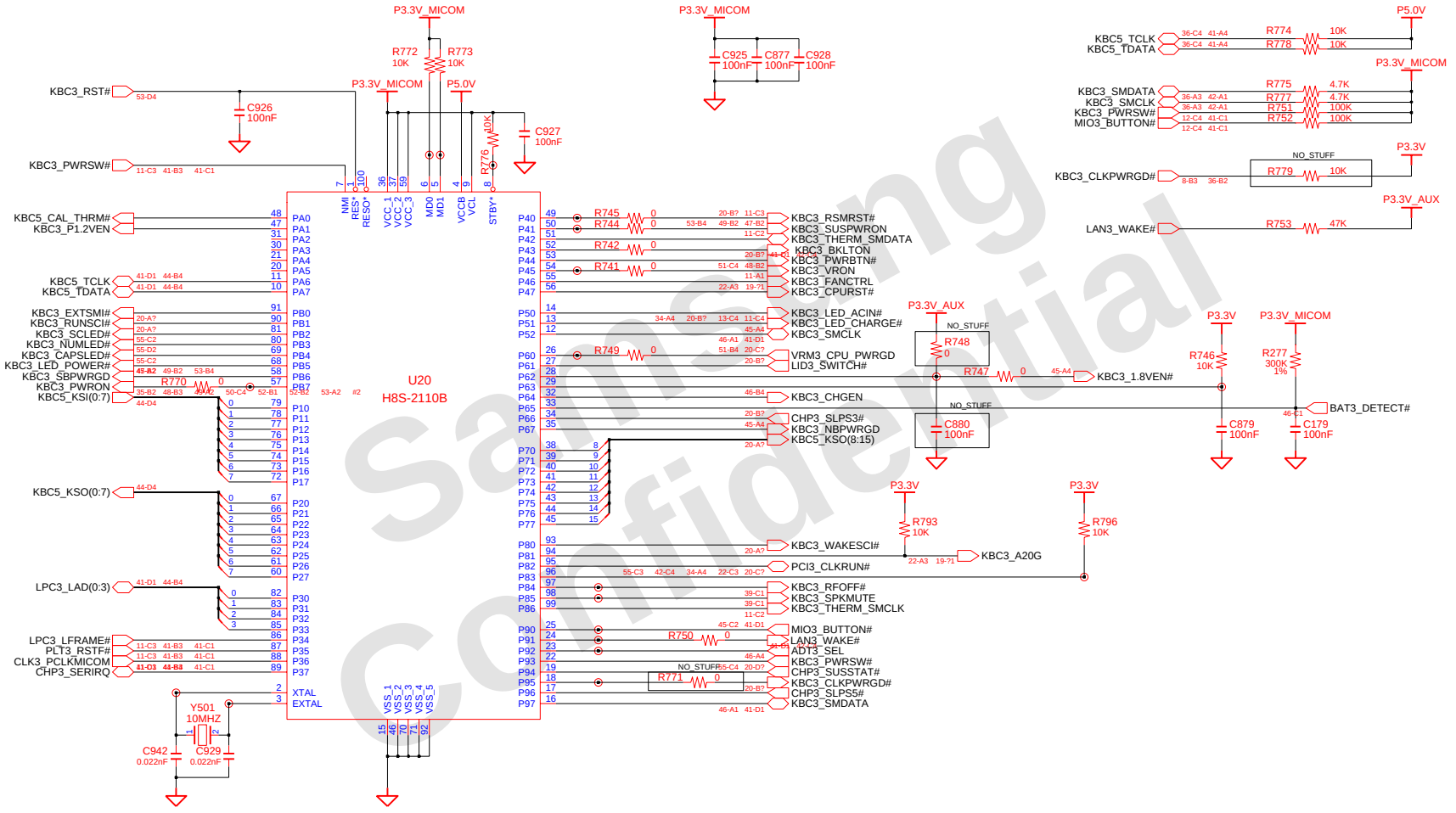
Main to ODD







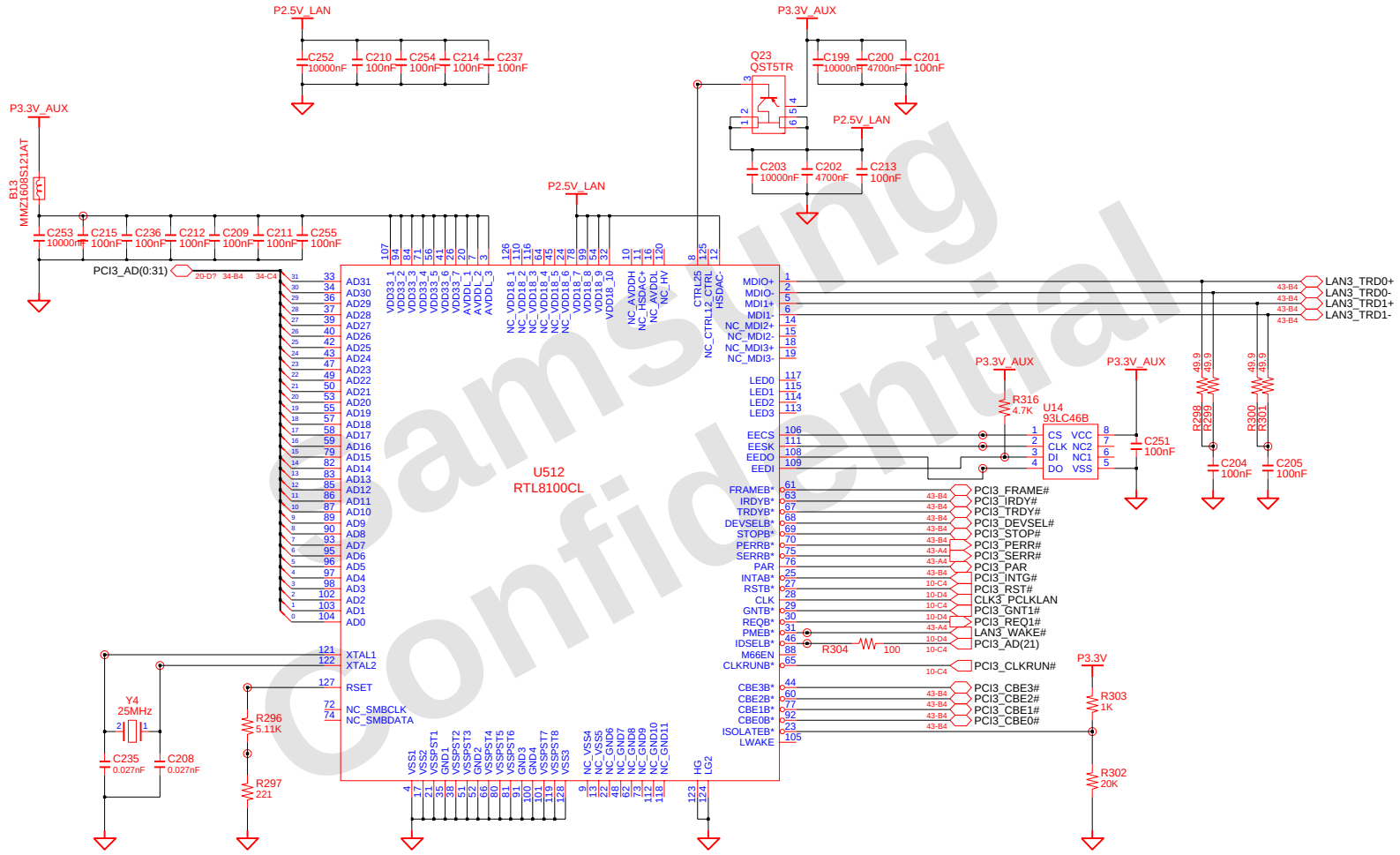
DRAW ELLEN ZHANG	DATE 6/16/2007	TITLE HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK ROKY ZHENG	DEV. STEP SR		
APPROVAL KEVIN LEE	REV 1.0	HDD & ODD	PART NO. BA41-00809/810A
MODULE CODE undefined	LAST EDIT March 23, 2007 11:06:39 AM	PAGE 38 OF 53	



TP FOR UPDATE MICOM:
P84=>TXD;P85=>RXD
MD0 and MD1 =>GND
P90,P91,P92=>VCC

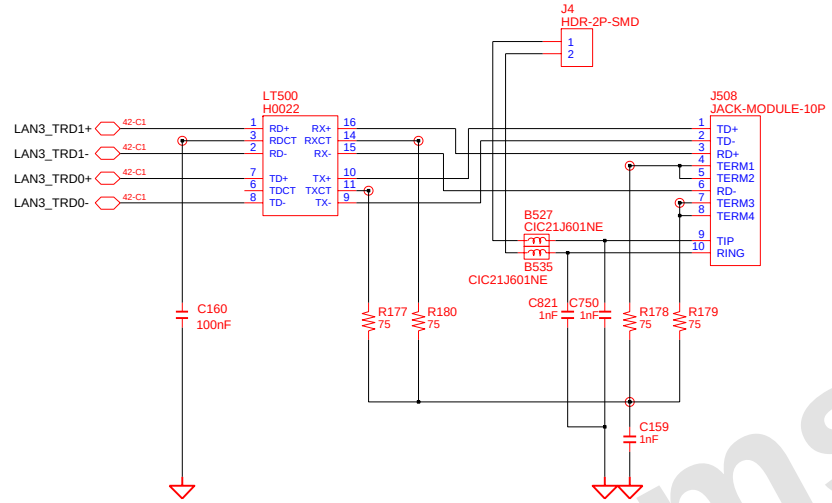
DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT MICOM	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0		PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 39 OF 53

LAN Controller (Only 10/100M)

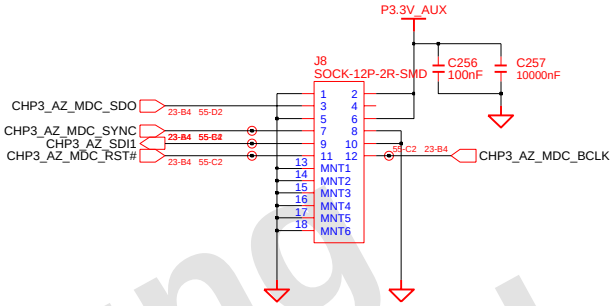


DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	LAN	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 40 OF 53

LAN Connector

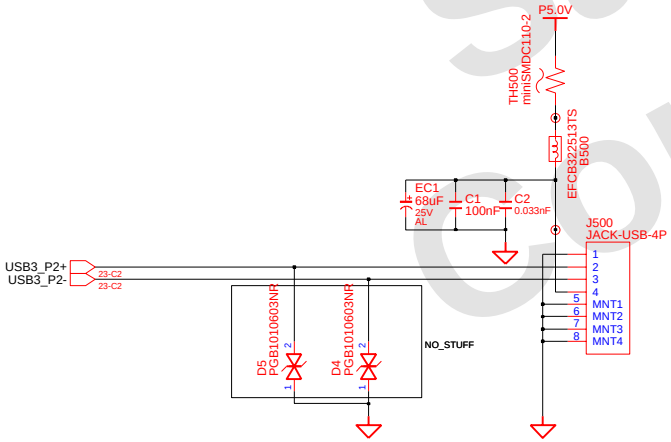


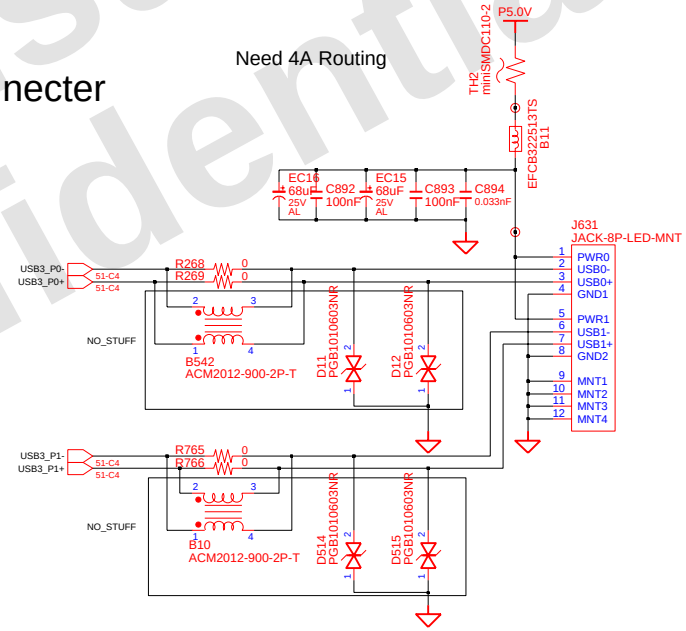
MDC Connecter



Need 4A Routing

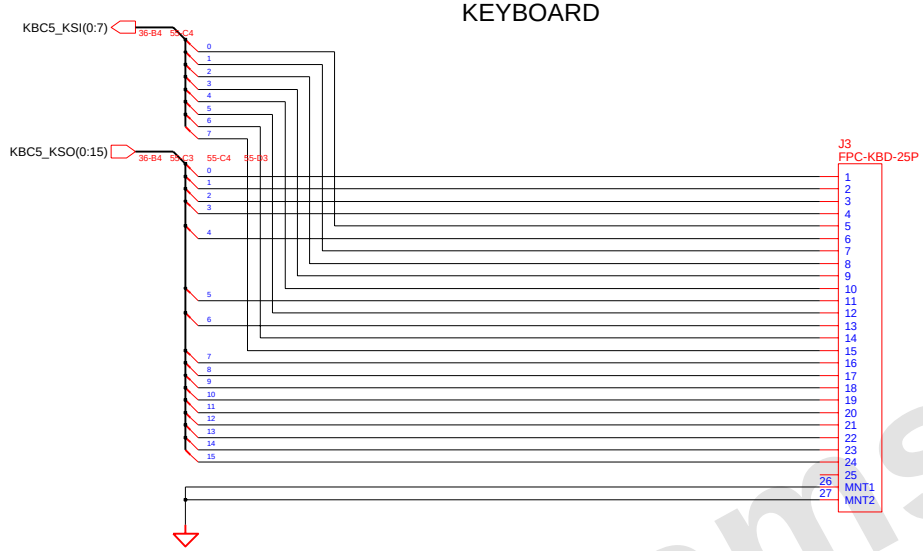
USB Connecter



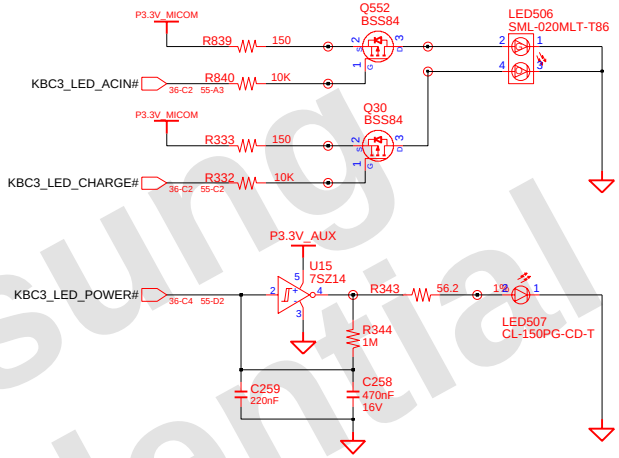


DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	LAN & MDC CONN	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 41 OF 53

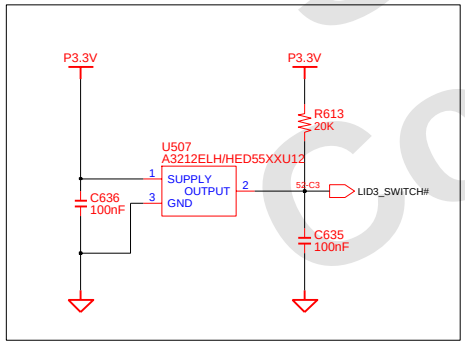
KEYBOARD



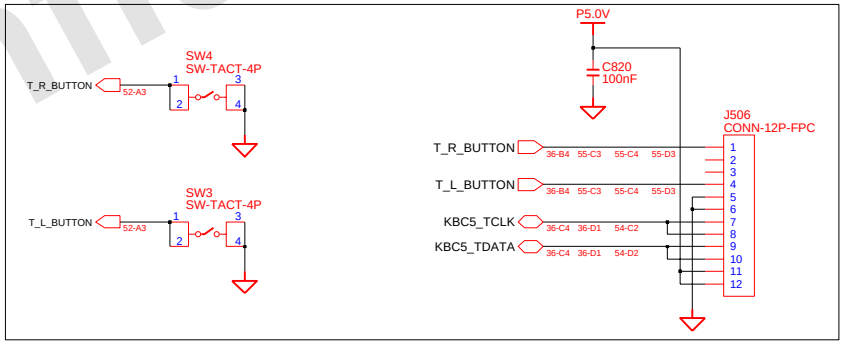
ADAPTERIN/CHARGING LED



LID SWITCH

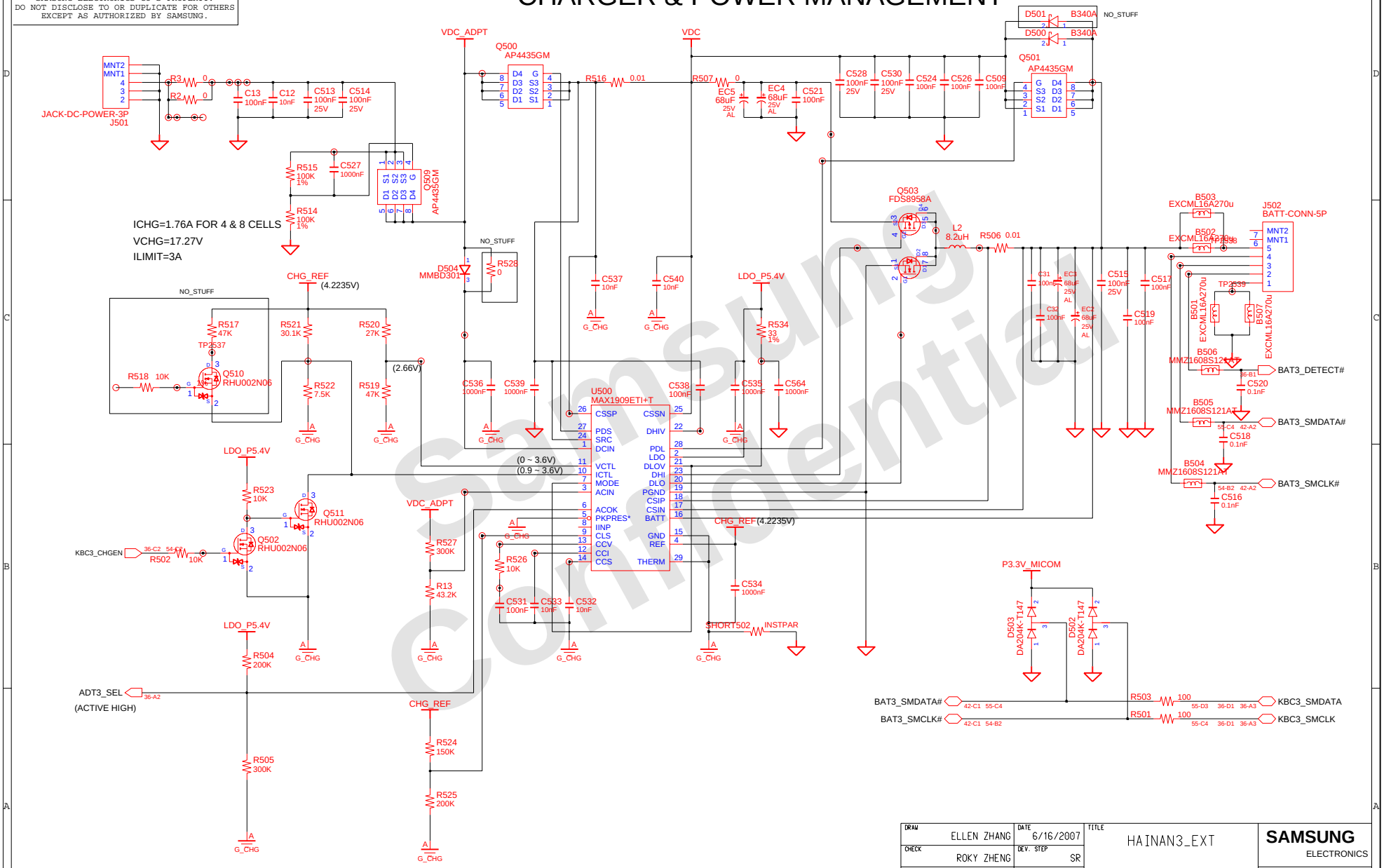


TOUCHPAD



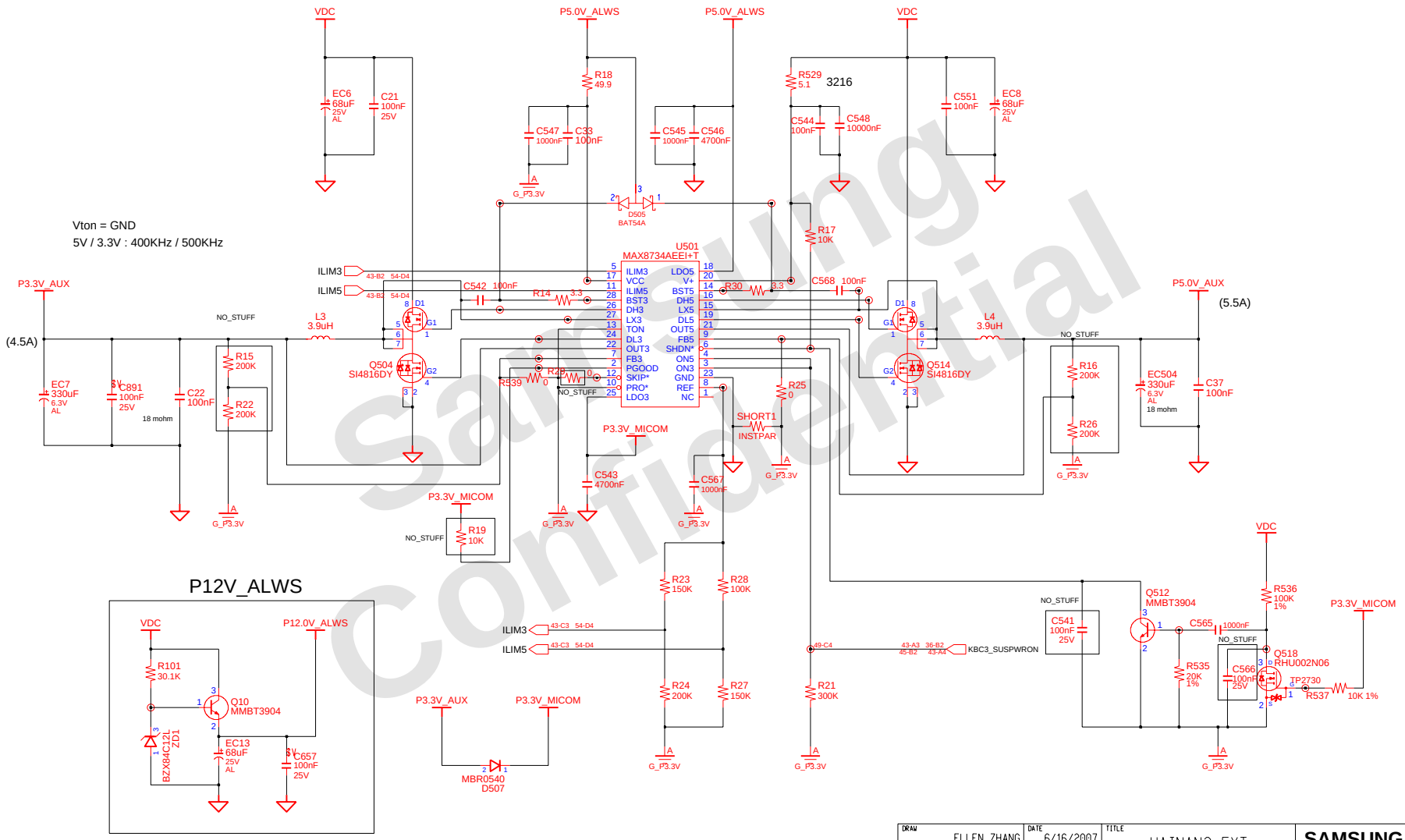
DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	BOARD CONN	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 42 OF 53

CHARGER & POWER MANAGEMENT



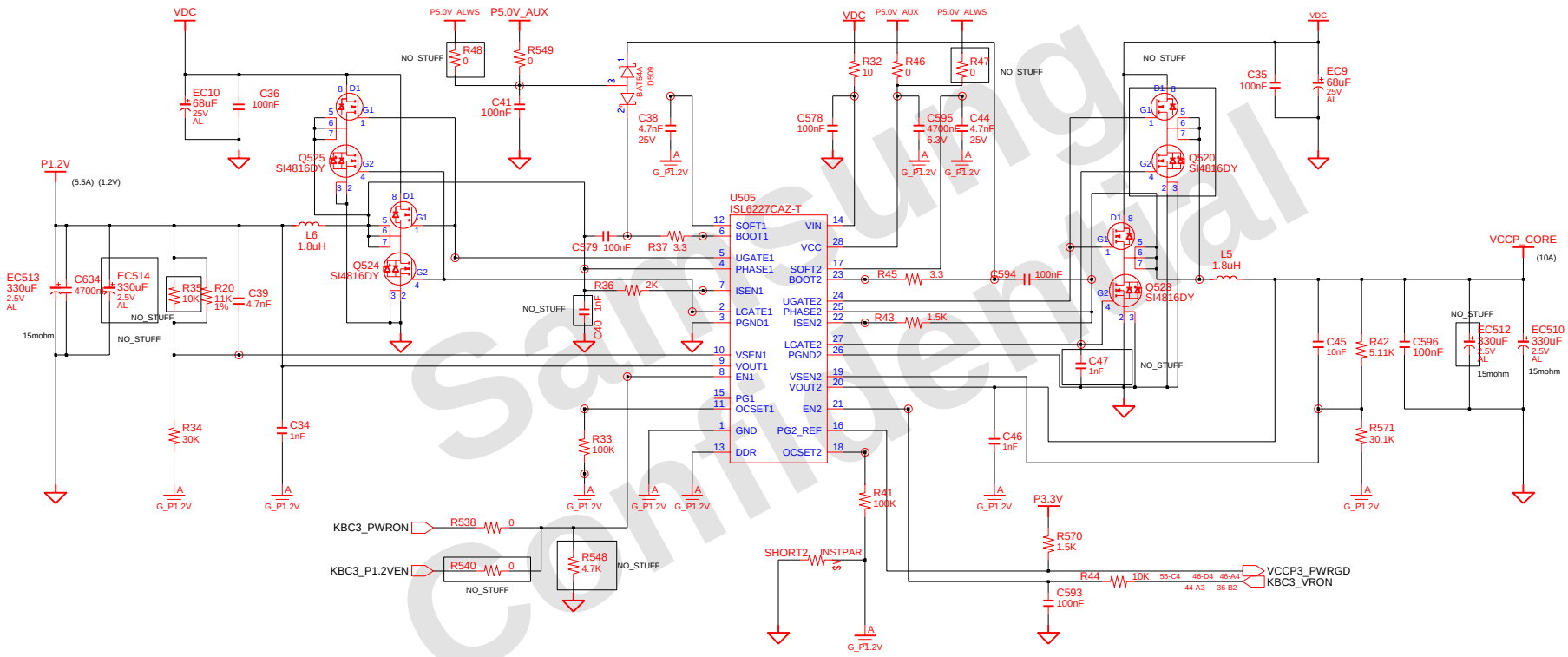
DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR	CHARGE	
APPROVAL: KEVIN LEE	REV: 1.0		PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 43 OF 53

P3.3V_AUX & P5V_AUX



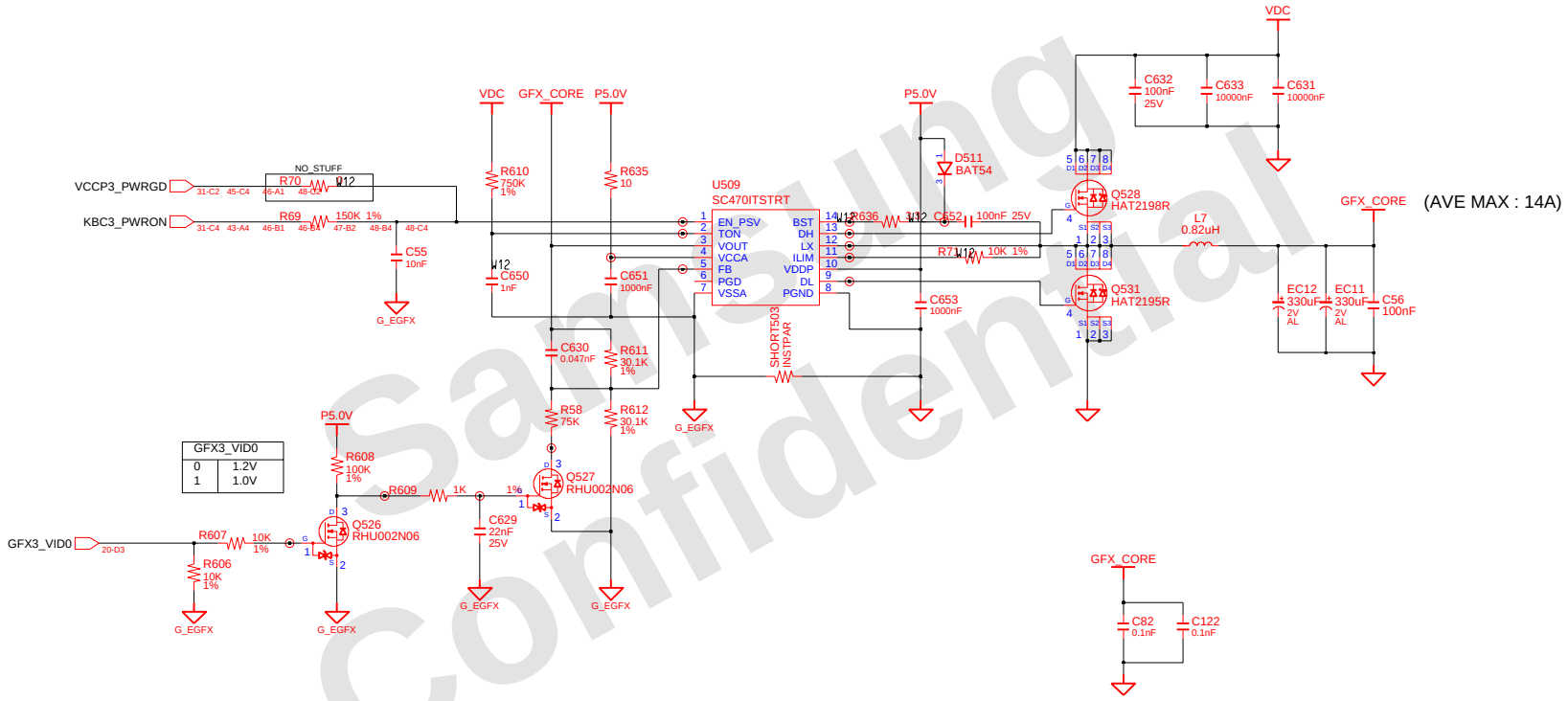
DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR	P3.3V_AUX & P5V_AUX	
APPROVAL: KEVIN LEE	REV: 1.0		PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 44 OF 53

P1.2V & VCCP _CORE(1.05V)



DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	P1.2V & VCCP	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 45 OF 53

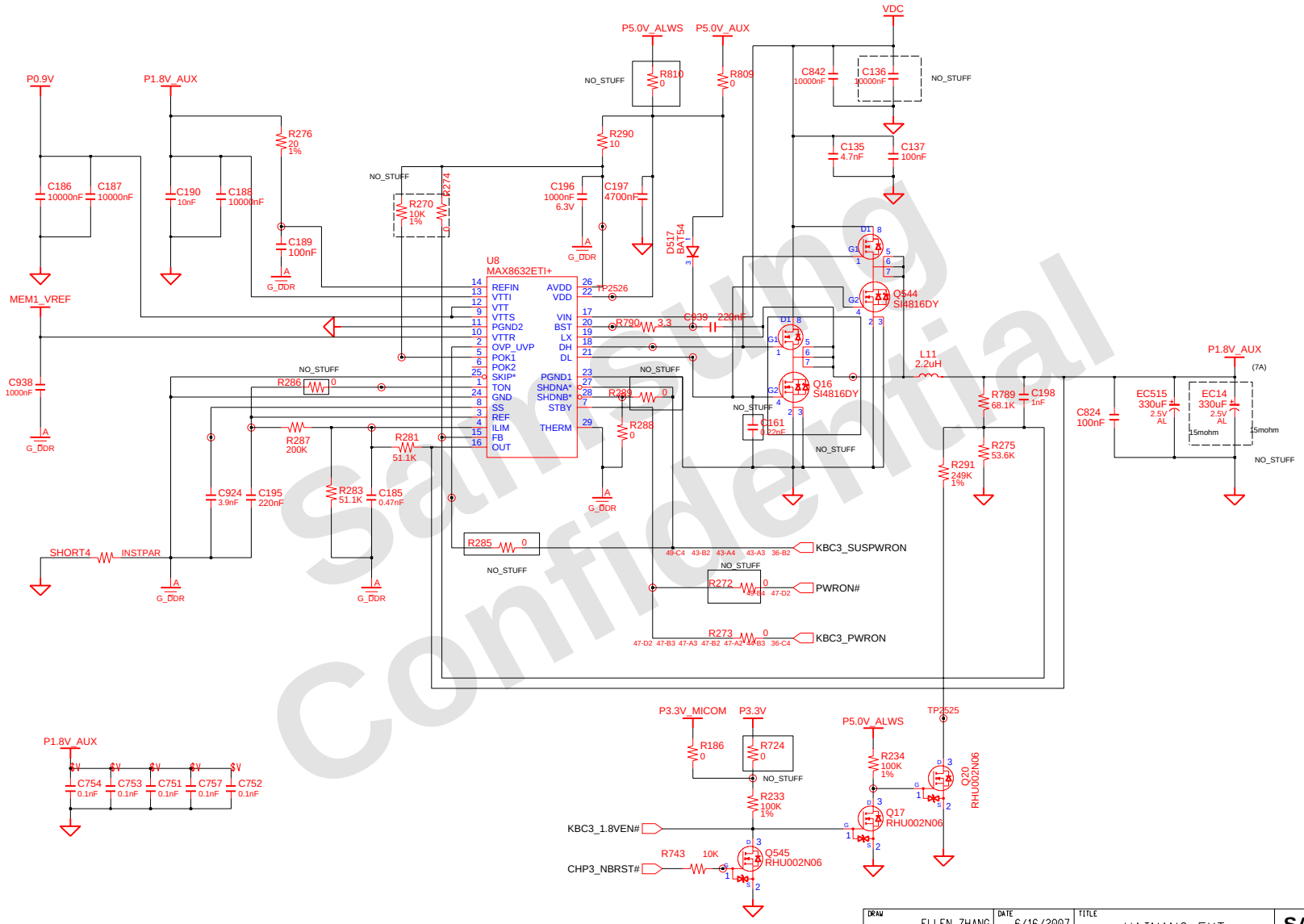
Graphic Core Power



GFX3_VID0	
0	1.2V
1	1.0V

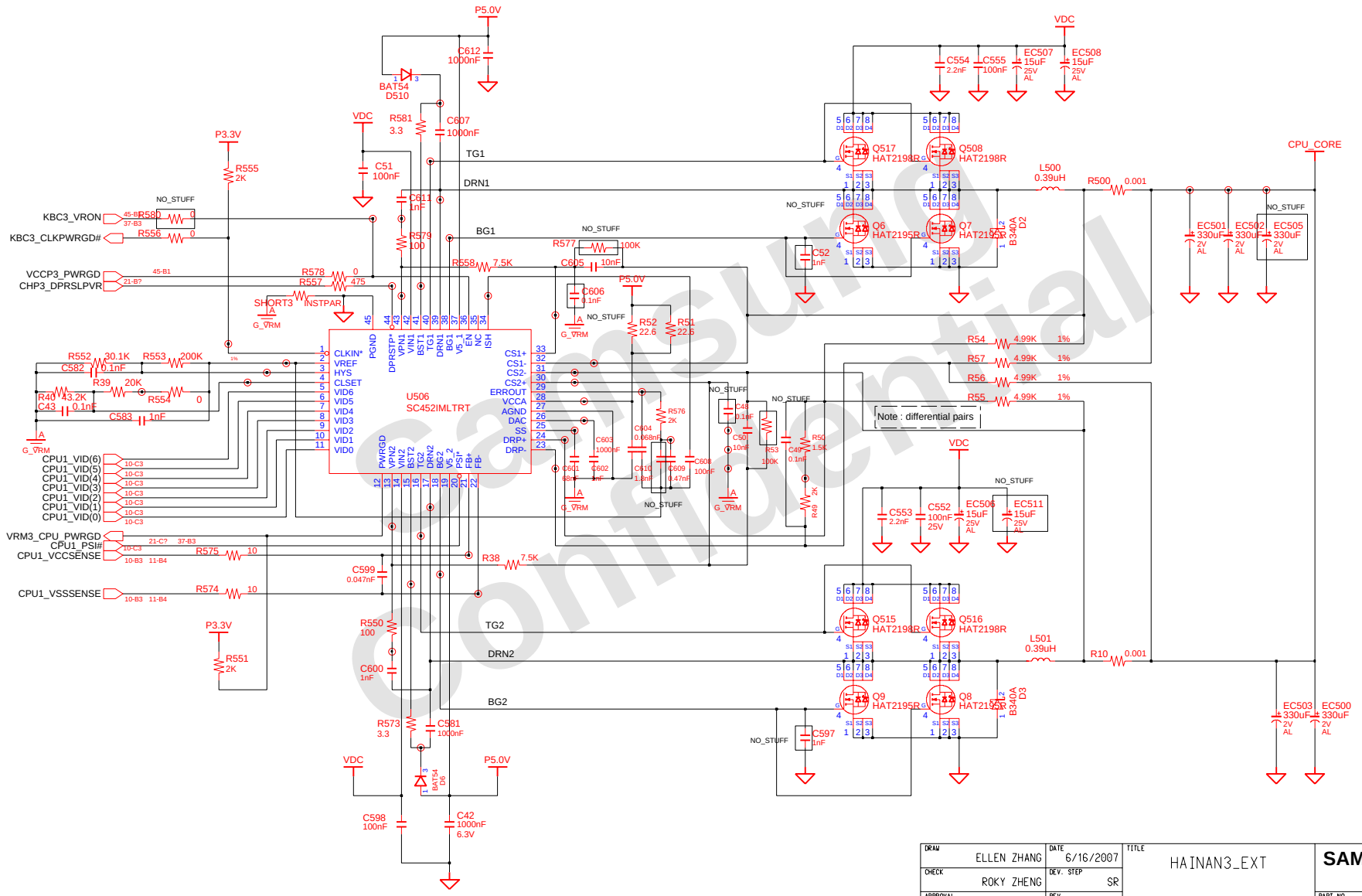
DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT MAIN GFX_CORE & P1.5V	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		PART NO.: BA41-00809/810A
APPROVAL: KEVIN LEE	REV: 1.0		
MODULE CODE	LAST EDIT: March 23, 2007 11:06:39 AM	PAGE 46 OF 53	

DDR2 Power



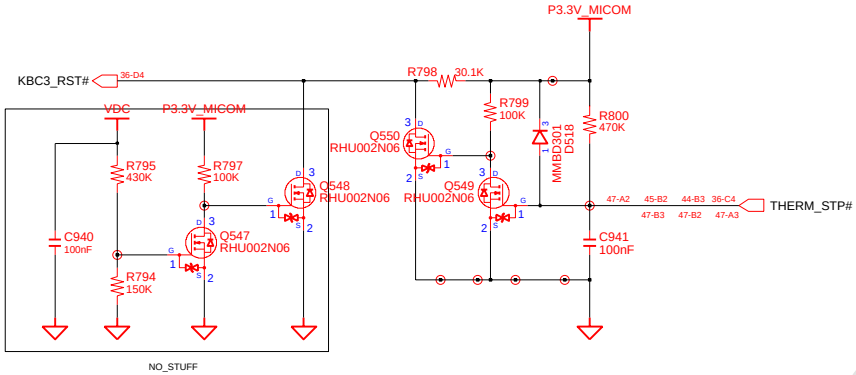
DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	DDR2 POWER	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 47 OF 53

CPU VRM [SEMTECH]



DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR	CPU VRM	
APPROVAL: KEVIN LEE	REV: 1.0		PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 48 OF 53

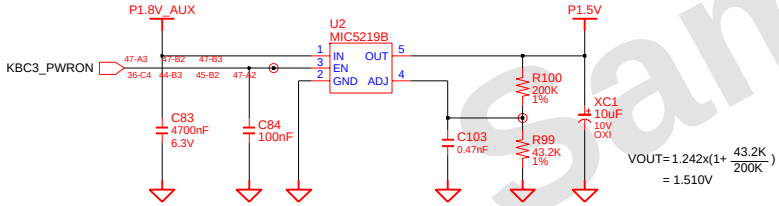
MICOM RESET



P1.5V POWER

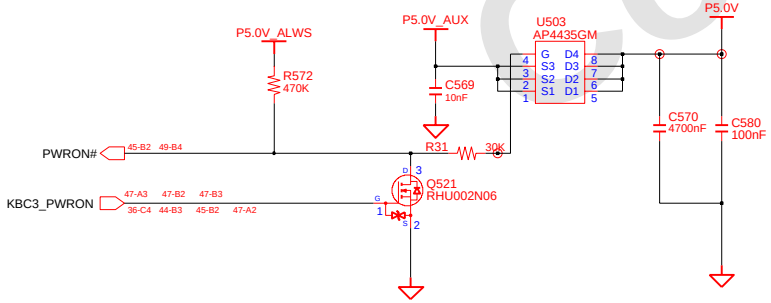
(EBL)

(AVE MAX : 2A)

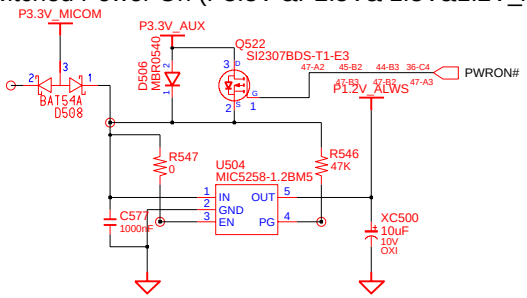


$$VOUT = 1.242x(1+\frac{43.2K}{200K}) = 1.510V$$

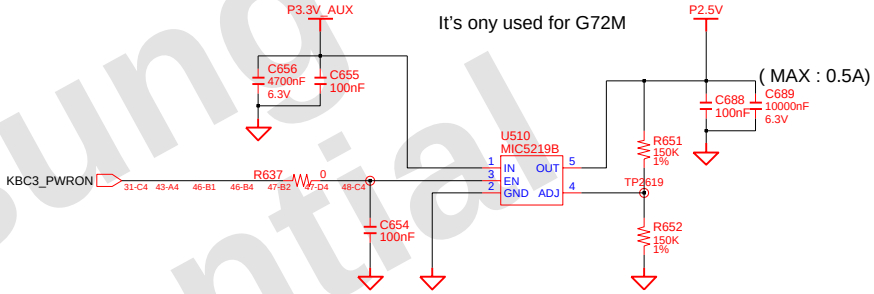
Switched Power On (P5V)

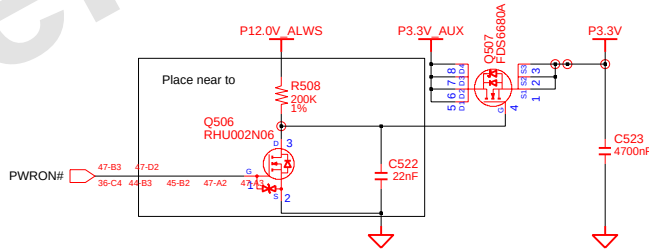


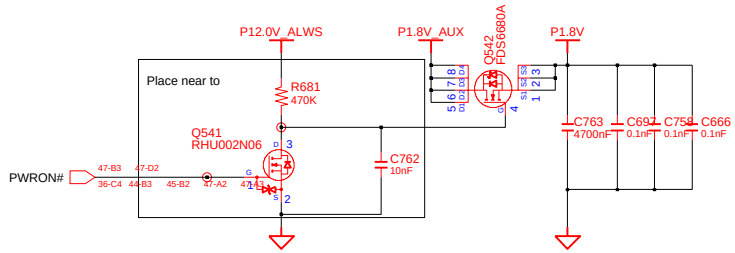
Switched Power On (P3.3V &P2.5V& 1.8V&1.2V_ALWS)



It's ony used for G72M

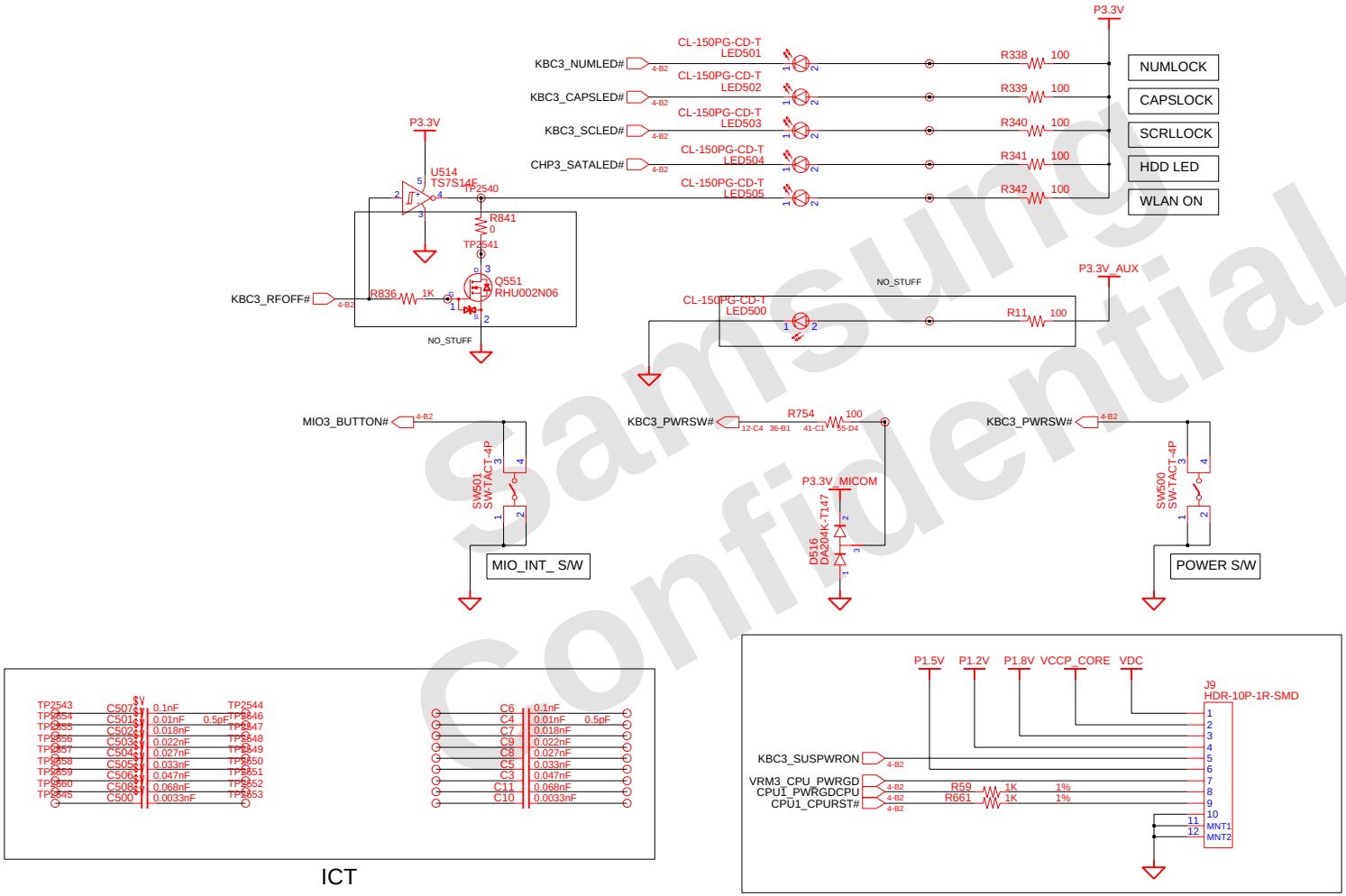






DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	SWITCH POWER	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 49 OF 53

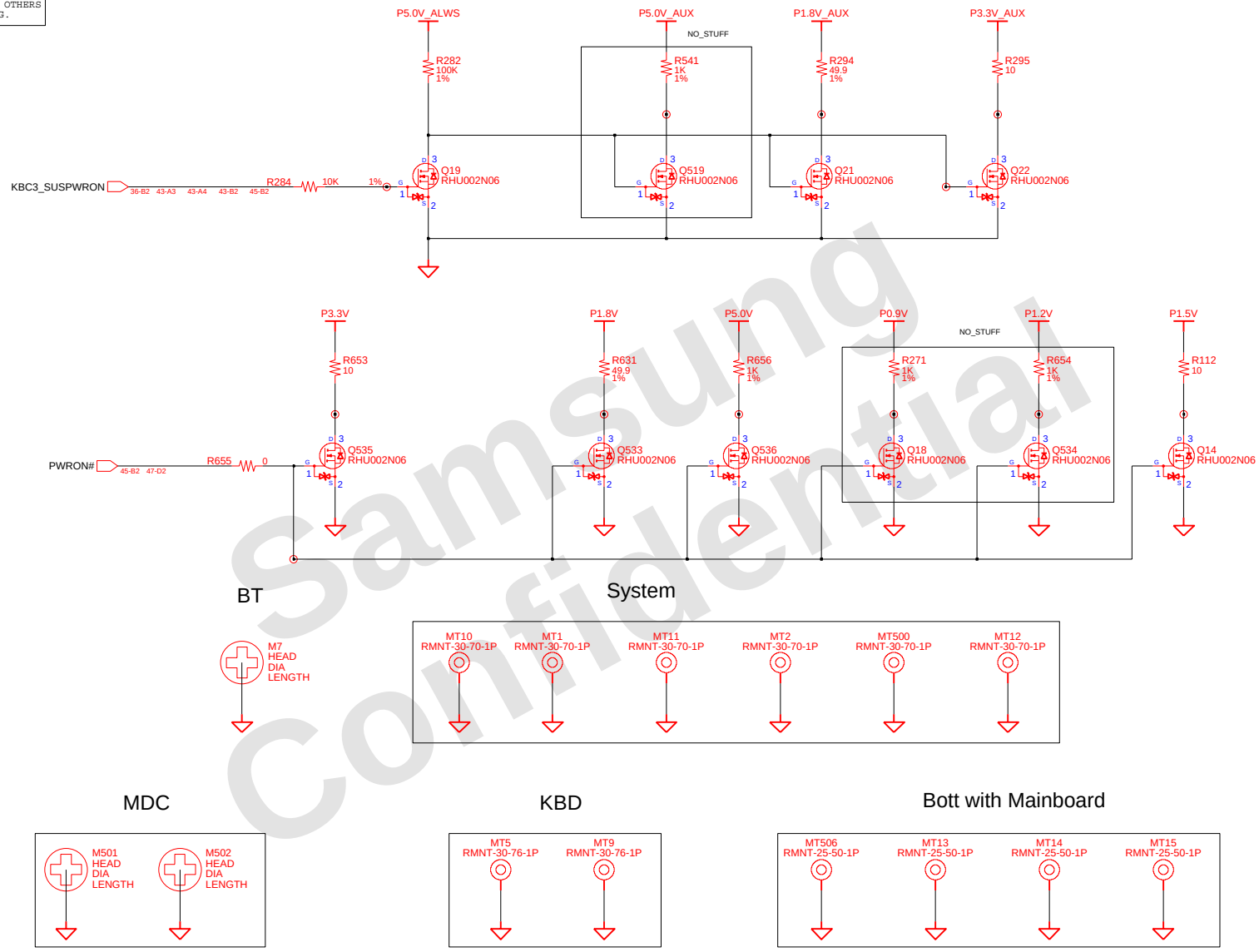
LED
0801-002195



ICT

ICT/JIG

DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	POWER SWITCH	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 50 OF 53



DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	POWER STRAPS	PART NO. BA41-00809/810A
MODULE CODE: undefined	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 51 OF 53

TP2027 MIC1
TP2028 MIC2
TP2029 GPIO1
TP2030 ILIM3
TP2031 ILIM5

TP2637 SMB3_DATA1

TP2638 VGA3_HSYNC
TP2639 VGA3_VSYNC
TP2640 GFX_CORE
TP2641 GFX_CORE
TP2642 GFX_CORE
TP2643 GFX_CORE
TP2644 CG_EGFX
TP2645 CG_EGFX
TP2646 CG_EGFX
TP2647 CG_EGFX
TP2648 P2.5V
TP2649 P2.5V
TP2650 P2.5V
TP2651 P2.5V

TP2020 CPU1_TDI
TP2021 CPU1_TMS
TP2022 PCI3_PAR
TP2023 SATA1_X1
TP2024 SMB3_CLK
TP2025 SPI3_CLK
TP2026 SPI3_CS#

TP2002 CHP3_SPKR

TP2006 CPU1_INTR
TP2007 CPU1_PSI#

TP2011 CPU1_SLP#
TP2012 CPU1_SMI#
TP2013 IDE5_CS1#
TP2014 IDE5_CS3#

TP2621 MEM1_BRAS#
TP2622 MEM1_BWE#

TP2633 LCD3_BKLTCTRL
TP2634 LCD3_BKLTEN
TP2635 LCD3_EDID_CLK
TP2636 LCD3_VDDEN

TP2623 GFX3_BKLTEN
TP2624 GFX3_THRMTRIP#
TP2625 GFX3_VID0

TP2629 GPIO(13)
TP2630 GPIO(5)
TP2631 KBC3_BKLTON
TP2632 KBC3_P1.2VEN

TP2015 RTC_CLK
TP2016 AC_SDOUT
TP2017 AUTO_ON#
TP2018 CPU1_NMI
TP2019 CPU1_TCK

TP1968 CPU1_A20M#

TP1971 CPU1_BSEL0
TP1972 CPU1_BSEL1
TP1973 CPU1_BSEL2

TP1977 CPU1_FERR#

TP1979 CPU1_INIT#

TP1950 CPU1_TRST#
TP1951 EXP3_CPPE#

TP1952 IDE5_DACK#
TP1953 IDE5_IORDY
TP1954 JCK_SENS_A
TP1955 KBC3_CHGEN
TP1956 KBC3_SMCLK
TP1957 KBC5_TDATA

TP1980 IDE5_DREQ
TP1981 IDE5_IOR#
TP1982 IDE5_IOW#
TP1983 KBC3_A20G
TP1984 KBC3_RST#
TP1985 KBC3_VRON
TP1986 KBC5_TCLK

TP1959 MCD3_SDCD#
TP1960 MCD3_XDALE
TP1961 MCD3_XDCD#
TP1962 MCD3_XDCE#
TP1963 MCD3_XDRE#
TP1964 MCD3_XDWE#

TP1996 ODD5_RST#

TP1997 SMB3_DATA
TP1998 SPI3_MISO
TP1999 SPI3_MOSI
TP2000 AUD3_EAPD#

TP2001 CLK3_NB14M

TP1939 PCI3_CBE0#
TP1940 PCI3_CBE1#
TP1941 PCI3_CBE2#
TP1942 PCI3_CBE3#
TP1943 PCI3_GNT1#

TP1945 PCI3_IRDY#
TP1946 PCI3_PERR#
TP1947 PCI3_REQ1#
TP1914 PCI3_RSTF#
TP1915 PCI3_SERR#
TP1916 PCI3_STOP#
TP1917 PCI3_TRDY#

TP1918 PEX3_WAKE#
TP1919 PLT3_RSTF#

TP1920 T_L_BUTTON
TP1921 T_R_BUTTON

TP1924 BAT3_SMCLK#
TP1925 CHP3_OVERT#
TP1910 CHP3_SBPME#
TP1911 CHP3_SERIRQ
TP1912 CHP3_SLPS3#
TP1913 CHP3_SLPS5#

TP1902 CPU1_DPSLP#
TP1903 CPU1_IGNNE#
TP1904 CPU1_VID(0)
TP1905 CPU1_VID(1)
TP1906 CPU1_VID(2)
TP1907 CPU1_VID(3)
TP1908 CPU1_VID(4)
TP1909 CPU1_VID(5)
TP1872 CPU1_VID(6)
TP1873 EXP3_CPUSB#
TP1874 EXP3_PERST#
TP1875 IDE5_IDEIRQ
TP1876 KBC3_1.8VEN#
TP1877 KBC3_PWRSW#
TP1878 KBC3_SCLED#
TP1879 KBC3_SMDATA
TP1880 KBC5_KSI(0)
TP1881 KBC5_KSI(1)
TP1882 KBC5_KSI(2)
TP1883 KBC5_KSI(3)
TP1884 KBC5_KSI(4)
TP1885 KBC5_KSI(5)
TP1886 KBC5_KSI(6)
TP1887 KBC5_KSI(7)

TP1888 KBC5_KSO(0)
TP1889 KBC5_KSO(1)
TP1890 KBC5_KSO(2)
TP1891 KBC5_KSO(3)
TP1892 KBC5_KSO(4)
TP1893 KBC5_KSO(5)
TP1894 KBC5_KSO(6)
TP1895 KBC5_KSO(7)
TP1896 KBC5_KSO(8)
TP1897 KBC5_KSO(9)

TP1898 LCD3_BKLTON
TP1899 LPC3_LAD(0)
TP1900 LPC3_LAD(1)
TP1869 LPC3_LAD(2)
TP1870 LPC3_LAD(3)
TP1871 MCD3_MSINS#

DRAW: ELLEN ZHANG	DATE: 6/16/2007	TITLE: HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK: ROKY ZHENG	DEV. STEP: SR		
APPROVAL: KEVIN LEE	REV: 1.0	TP	PART NO. BA41-00809/810A
MODULE CODE	LAST EDIT: March 23, 2007 11:06:39 AM		PAGE 52 OF 53

TP2233 PCI3_FRAME#

TP2235 VCCP3_PWRGD
TP2236 AUD3_PCBEEP#
TP2237 BAT3_DETECT#
TP2238 BAT3_SMDATA#
TP2239 CHP3_AZ_SDI0
TP2240 CHP3_BIOSWP#
TP2241 CHP3_CPUSTP#

TP2223 CPU1_STPCLK#

TP2225 ITP3_SYSRST#
TP2226 JCK_SENS_HP#
TP2227 KBC3_CPURST#
TP2228 KBC3_EXTSMI#
TP2229 KBC3_FANCTRL
TP2230 KBC3_NBPWRGD
TP2231 KBC3_NUMLED#
TP2232 KBC3_PWRBTN#
TP2207 KBC3_RSMRST#
TP2208 KBC3_RUNSCI#
TP2209 KBC3_SBPWRGD
TP2210 KBC5_KSO(10)
TP2211 KBC5_KSO(11)
TP2212 KBC5_KSO(12)
TP2213 KBC5_KSO(13)
TP2214 KBC5_KSO(14)
TP2215 KBC5_KSO(15)

TP2216 LID3_SWITCH#
TP2217 LPC3_LFRAME#

TP2193 PCI3_CLKRUN#
TP2194 PCI3_DEVSEL#

TP2195 CHP3_DPRSLPVR
TP2196 CHP3_SATALED#

TP2197 CPU1_PROCHOT#
TP2198 CPU1_PWRGDCPU
TP2199 CPU1_VCCSENSE
TP2200 CPU1_VSSSENSE
TP2201 JCK_SENS_MIC#
TP2202 KBC3_CAPSLED#
TP2203 KBC3_WAKESCI#

TP2180 CHP3_SATA_DET#

TP2181 CPU1_THRMTRIP#
TP2182 KBC3_CLKPWRGD#
TP2183 KBC3_LED_ACIN#
TP2184 KBC5_CAL_THRM#

TP2186 VRM3_CPU_PWRGD

TP2187 CHP3_ALINK_RST#
TP2188 CHP3_AZ_AUD_SDO
TP2189 CHP3_AZ_MDC_SDO

TP2192 KBC3_LED_POWER#

TP2158 CHP3_AZ_AUD_RST#

TP2159 CHP3_SBTHRMTRIP#

TP2162 KBC3_LED_CHARGE#
TP2163 KBC3_THERM_SMCLK

TP2164 KBC3_THERM_SMDATA

TP2169 CHG_REF
TP2170 G_AUD
TP2171 G_AUD
TP2172 G_AUD
TP2173 G_AUD
TP2174 G_CHG
TP2175 G_CHG
TP2176 G_CHG
TP2177 G_CHG
TP2178 G_CRT
TP2179 G_CRT

TP2126 G_CRT
TP2127 G_CRT
TP2128 G_DDR
TP2129 G_DDR
TP2130 G_DDR
TP2131 G_DDR
TP2132 G_P3.3V
TP2133 G_P3.3V
TP2134 G_P3.3V
TP2135 G_P3.3V
TP2136 LCD_VDD3V
TP2137 LCD_VDD3V

TP2142 LDO_P5.4V
TP2143 LDO_P5.4V

TP2146 MEM1_VREF
TP2147 MEM1_VREF
TP2148 P0.9V
TP2149 P0.9V
TP2150 P0.9V
TP2151 P0.9V
TP2152 P1.2V
TP2153 P1.2V
TP2154 P1.2V
TP2155 P1.2V
TP2156 P1.5V
TP2157 P1.5V
TP2094 P1.5V
TP2095 P1.5V
TP2096 P1.8V
TP2097 P1.8V
TP2098 P1.8V
TP2099 P1.8V

TP2103 PRTC_BAT

TP2109 P1.5V_EXP
TP2110 P1.5V_EXP
TP2111 P1.5V_EXP
TP2112 P1.8V_AUX
TP2113 P1.8V_AUX
TP2114 P1.8V_AUX
TP2115 P1.8V_AUX
TP2116 P2.5V_LAN
TP2117 P2.5V_LAN
TP2118 P2.5V_LAN
TP2119 P2.5V_LAN

TP2123 P2.5V_MCD
TP2124 P3.3V_AUX
TP2125 P3.3V_AUX
TP2062 P3.3V_AUX
TP2063 P3.3V_AUX

TP2065 P3.3V_EXP
TP2066 P3.3V_EXP

TP2068 P3.3V_MCD
TP2069 P3.3V_MCD
TP2070 P3.3V_MCD
TP2071 P3.3V_MCD
TP2072 P5.0V_AUD
TP2073 P5.0V_AUD
TP2074 P5.0V_AUD
TP2075 P5.0V_AUD
TP2076 P5.0V_AUX
TP2077 P5.0V_AUX

TP2078 P5.0V_AUX
TP2079 P5.0V_AUX
TP2080 PCIE_VDDR

TP2085 P1.2V_ALWS
TP2086 P1.2V_ALWS

TP2088 P5.0V_ALWS
TP2089 P5.0V_ALWS
TP2090 P5.0V_ALWS
TP2091 P5.0V_ALWS
TP2092 P12.0V_ALWS
TP2093 P12.0V_ALWS
TP2032 P12.0V_ALWS
TP2033 P12.0V_ALWS

TP2035 P3.3V_AUX_EXP

TP2037 P3.3V_AUX_EXP
TP2038 VDC
TP2039 VDC
TP2040 VDC
TP2041 VDC

TP2045 VCC_CRT
TP2046 VDC_INV
TP2047 VDC_INV

TP2050 VDD_AMP
TP2051 VDD_AMP
TP2052 VDD_AMP
TP2053 VDD_AMP
TP2054 VDD_AUD
TP2055 VDD_AUD
TP2056 VDD_AUD
TP2057 VDD_AUD
TP2058 VCCP_CORE
TP2059 VCCP_CORE
TP2060 VCCP_CORE
TP2061 VCCP_CORE

TP2656 GPIO(1)

TP2660 KBC3_BKLTON
TP2661 KBC3_P1.2VEN

TP2663 GFX_CORE
TP2664 GFX_CORE
TP2665 GFX_CORE
TP2666 GFX_CORE
TP2667 G_EGFX
TP2668 G_EGFX
TP2669 G_EGFX
TP2670 G_EGFX
TP2671 P2.5V
TP2672 P2.5V
TP2673 P2.5V
TP2674 P2.5V

REV500

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(YY/MM/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW ELLEN ZHANG	DATE 6/16/2007	TITLE HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK ROKY ZHENG	DEV. STEP SR		
APPROVAL KEVIN LEE	REV 1.0	TP	PART NO. BA41-00809/810A
MODULE CODE	LAST EDIT March 23, 2007 11:06:39 AM		PAGE 53 OF 53