

KL3 Intel Calpella Platform with UMA GFX



01

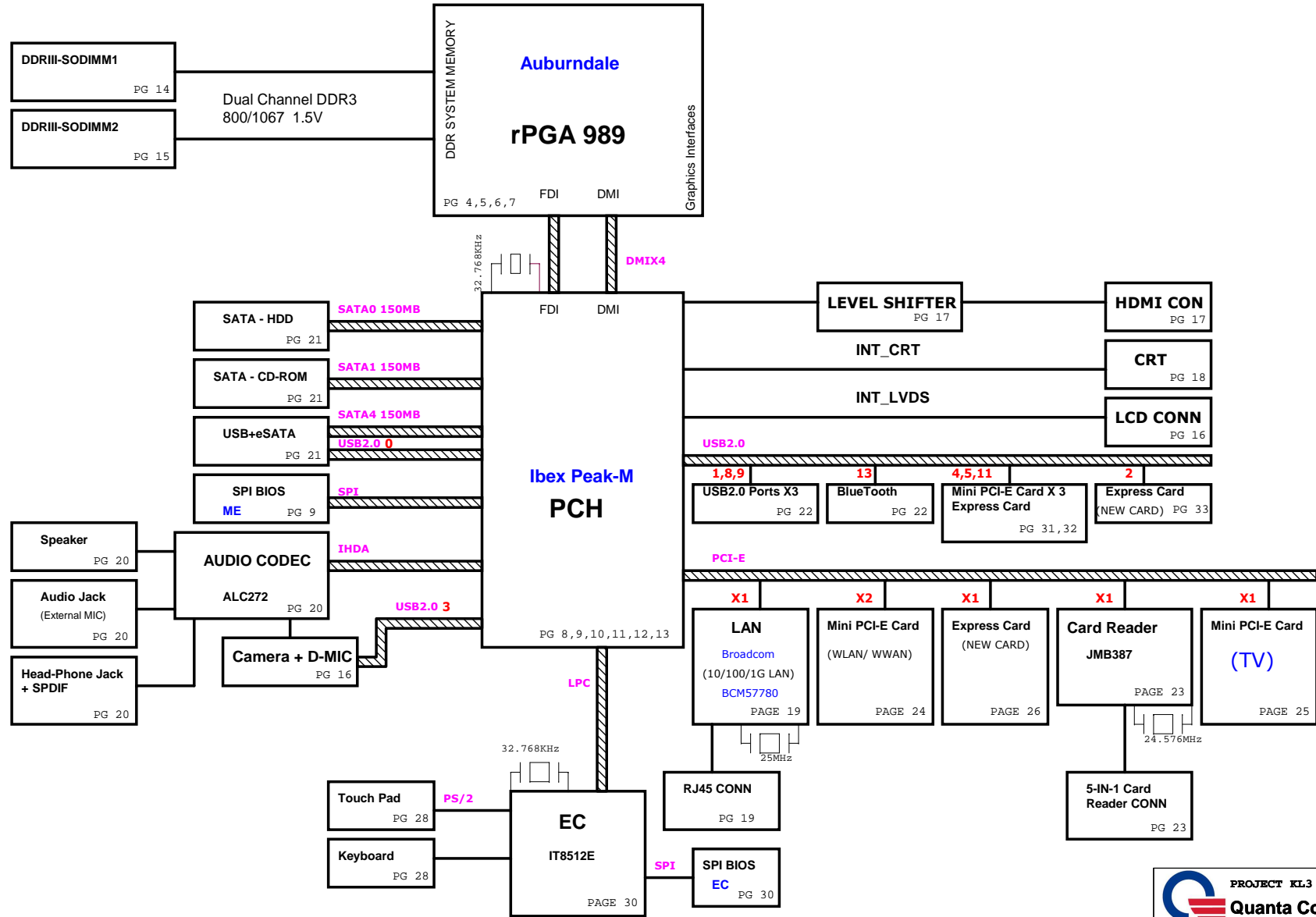
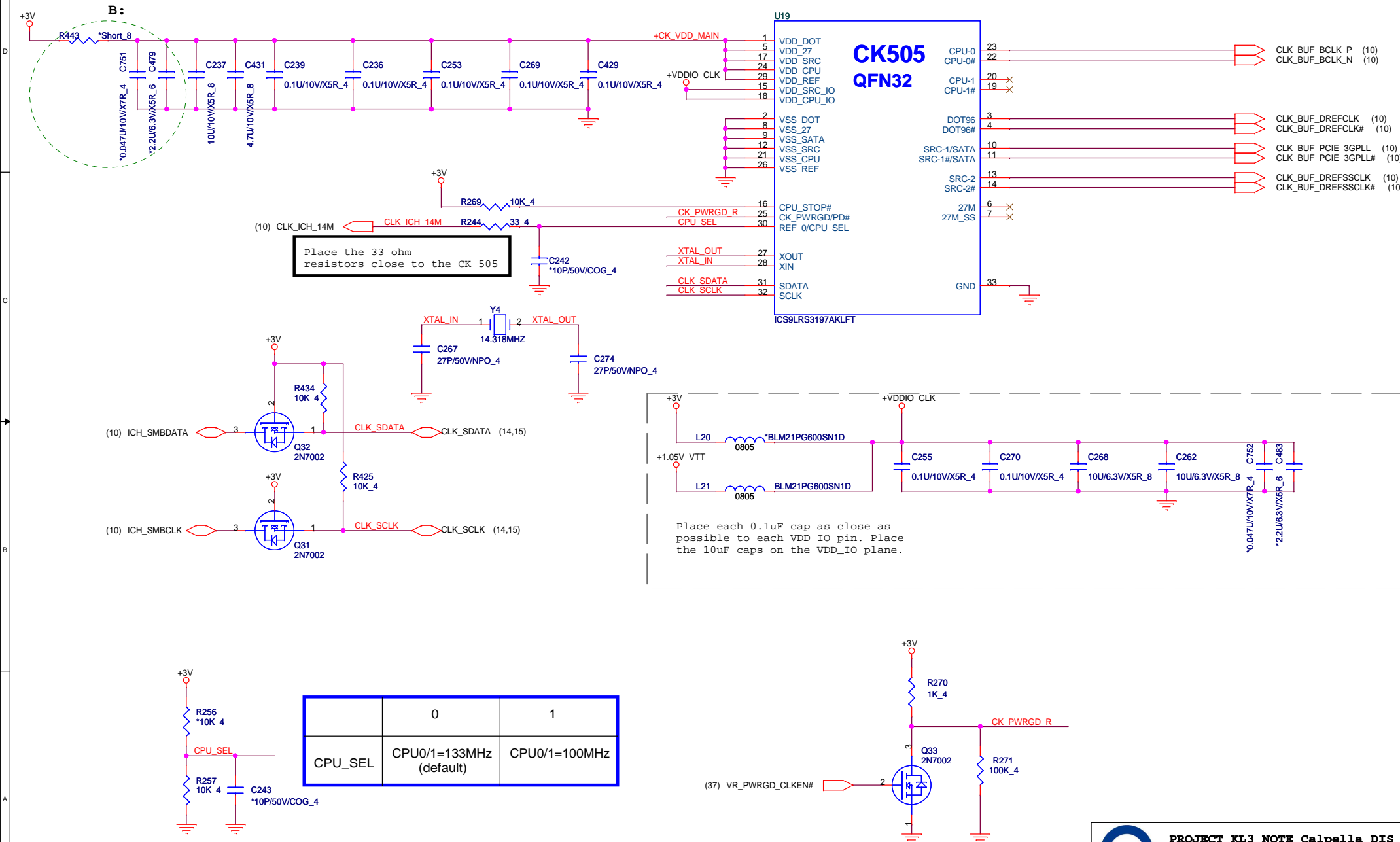


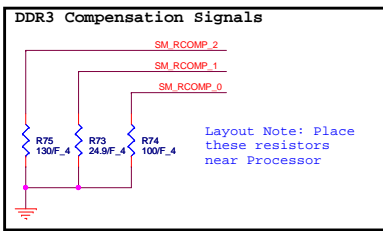
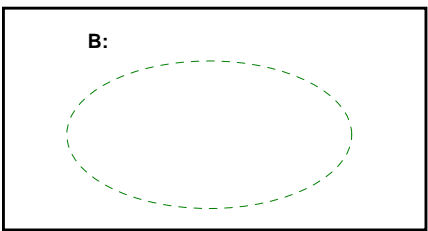
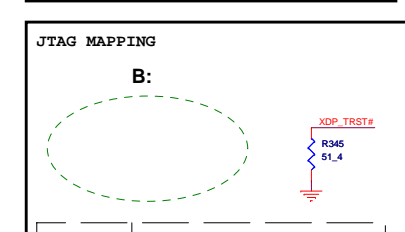
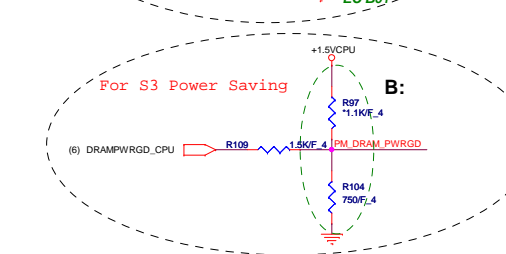
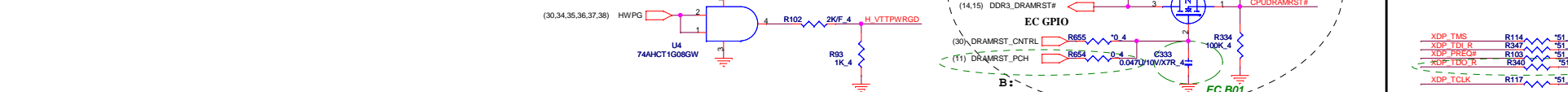
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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	23,32,43,44,45,46,47,48,49,50	MAIN POWER		S0~S5
+3VRTC	+3.0V~+3.3V	9,12,41	RTC		S0~S5
3VPCU	+3.3V	9,23,27,30,32,35,39,41,43,44,47	ITE8052 POWER	3V5V_EN	S0~S5
5VPCU	+5V	14,43,44,45,46,47,49,50	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
+15V	+15V	23,38,43,45,46,47	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	27,43	LAN POWER	LAN_ON	
5V_S5	+5V	12,29,30,43	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	8,9,10,11,12,43,52	Sys Management,PCH Resume Well, Intel HD Audio,USB,WLAN WiMAX POWER	S5_ON	S0~S3
5VSUS	+5V	23,39,43,48	SLP_S4# CTRLD POWER	SUSON	S0~S3
3VSUS	+3.3V	14,15,30,34,41,43,49	SLP_S4# CTRLD POWER	SUSON	S0~S3
1.5VSUS	+1.5V	4,6,14,15,43,45,46,49,50	SODIMM POWER	SUSON	S0~S3
0.75VSMDDR_VTERM	+0.75V	14,15,43,45	DDR3 SODIMM REFERENCE POWER	MAIN_ON	S0
+5V	+5V	12,18,23,24,25,26,28,35,37,41,43,44	SLP_S3# CTRLD POWER	MAIN_ON	S0
+3V	+3.3V	3,4,8,9,10,11,12,14,15,17,23,25,26,27,28,29,30,31,32,33,34,36,37,38,39,40,41,43,44,45,46,47,48,50,52	SLP_S3# CTRLD POWER	MAIN_ON	S0
+1.8V	+1.8V	6,12,17,18,21,22,33,43,50	LVDS,NVM POWER	MAIN_ON	S0
+1.5V	+1.5V	12,18,19,20,31,32,34,45,46	Mini PCIe,Express Card POWER	MAIN_ON	S0
+1.05V_VTT	+1.05V	4,6,11,12,43,46,48,52	AuBurndale VTT POWER	MAIN_ON	S0
+1.05V_PCH	+1.05V	3,10,12,43,46,52	PCH CORE POWER	1.05V_RUN_ON	S0
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,43,49	VGA CORE POWER	GFXVR_EN	S0
VCC_CORE		6,43,48	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	23	LCD Power	ENVDD	S0
+5V_ODD	+5V	28	ODD Power	MAIN_ON	S0
+5V_HDD	+5V	28	HDD Power	MAIN_ON	S0
BAT-V	+10V~+17V	44	MAIN BATTERY	CHG_PBATT	S0~S5

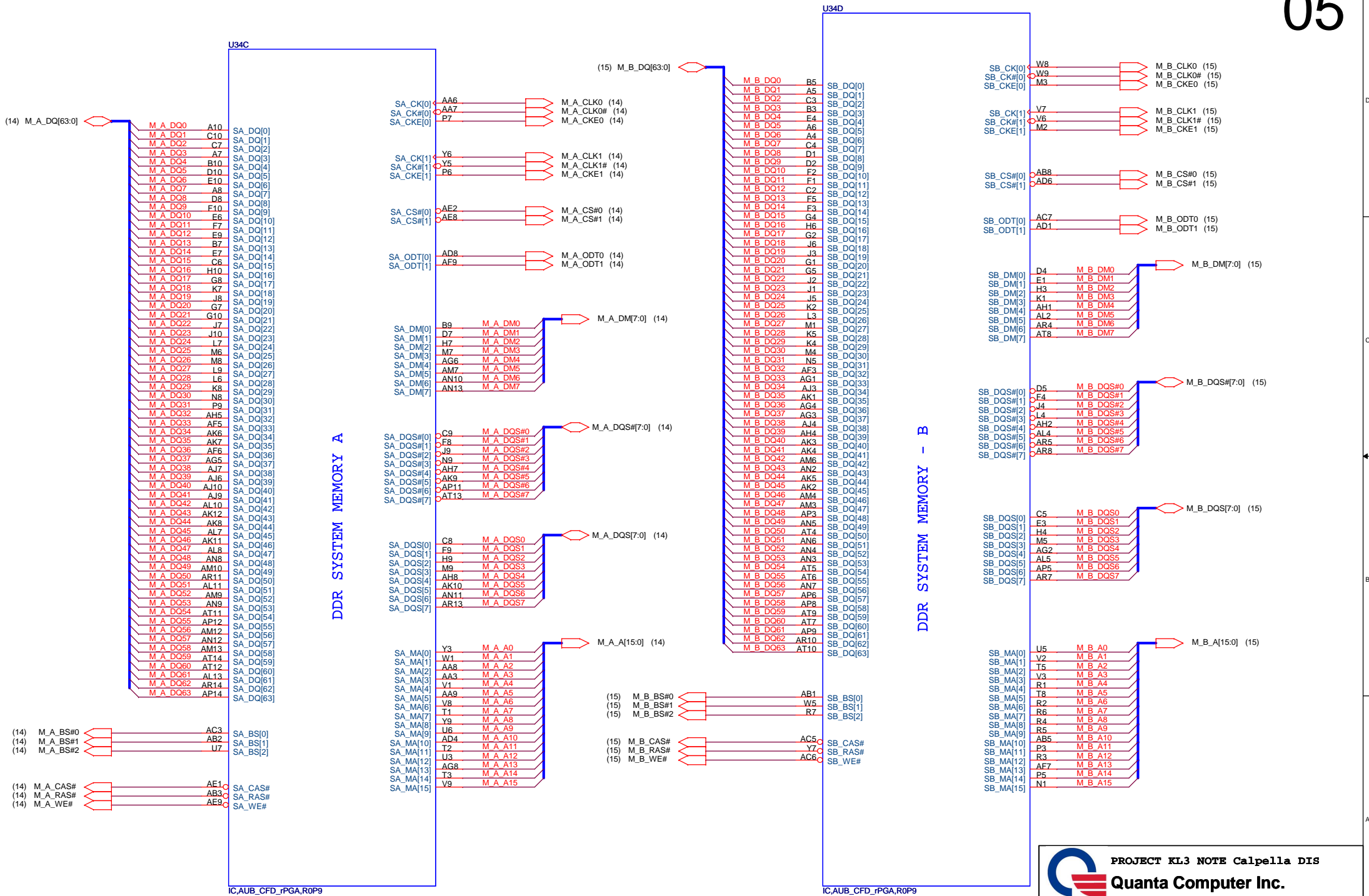


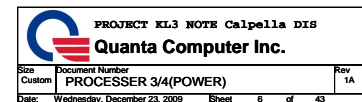


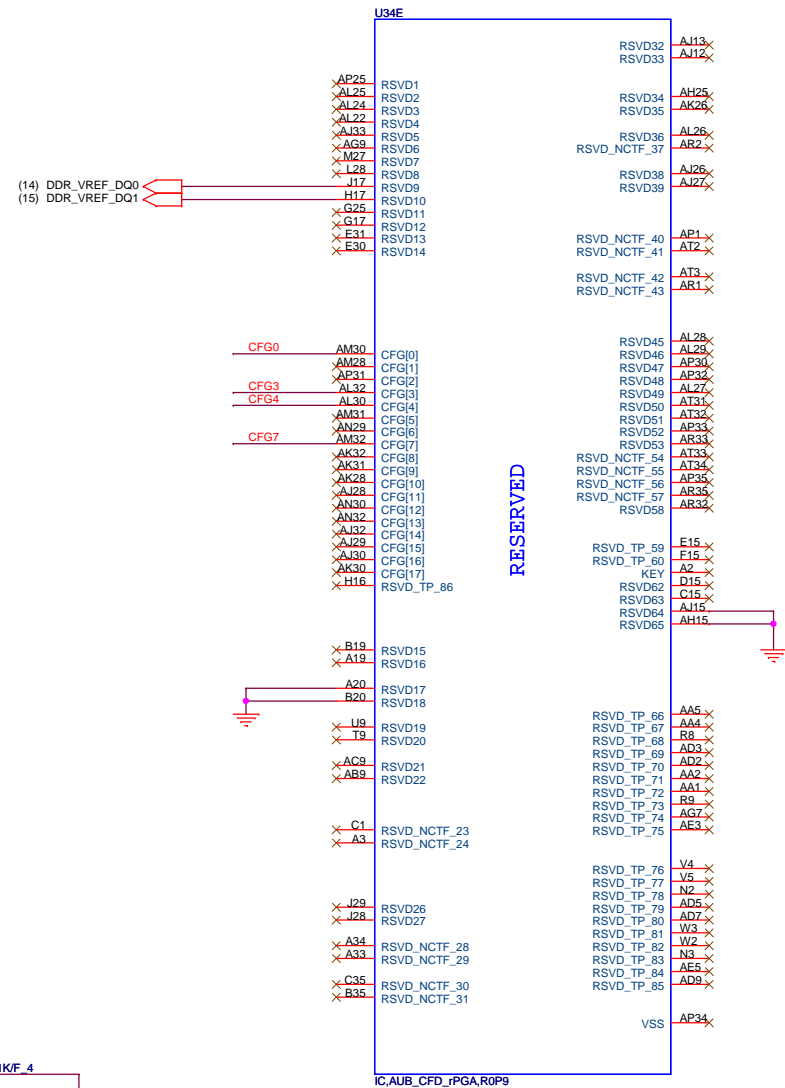
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Date:	Wednesday, December 23, 2009 <table border="1" data-bbox="2027 1533 2085 1538"> <tr> <td>Sheet</td> <td>4</td> </tr> </table>	Sheet	4
Sheet	4		

AUBURNDALE PROCESSOR (DDR3)

05








CFG4 R122 *3.01K/F 4

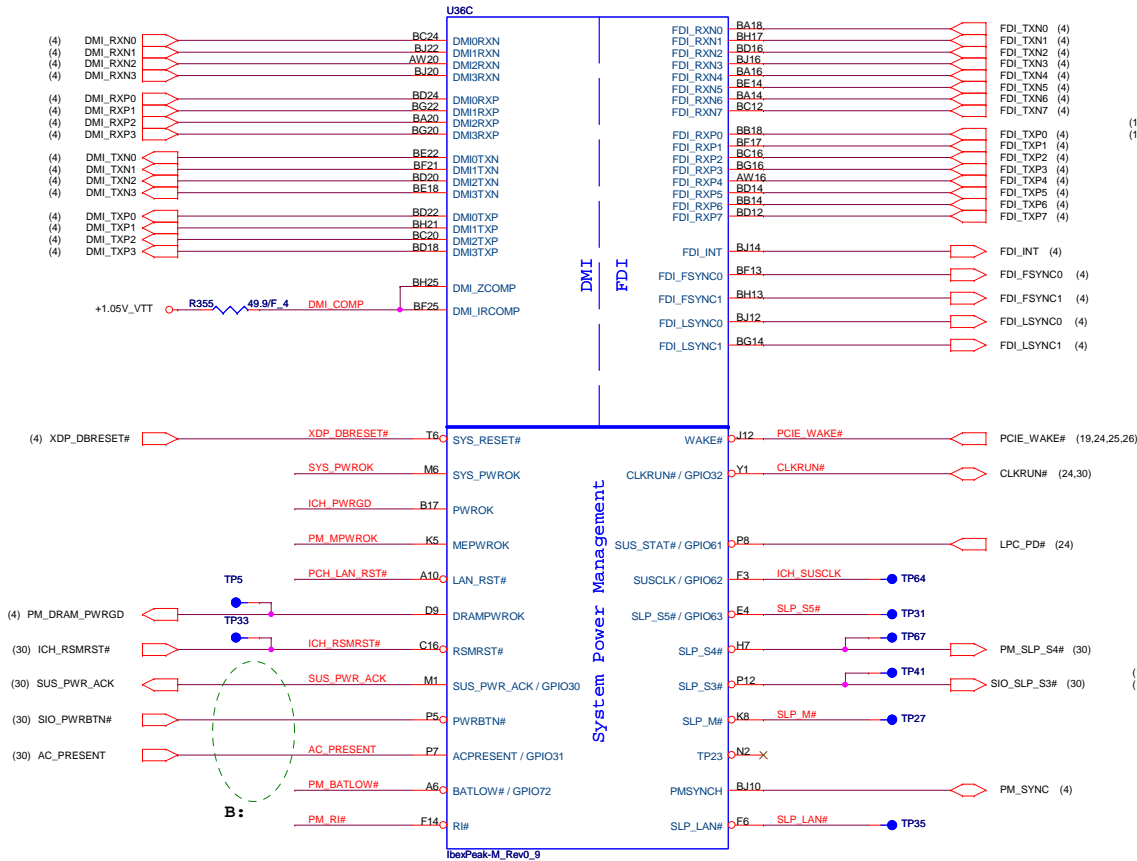
CFG0 R123 *3.01K/F 4

CFG3 R121 3.01K/F 4

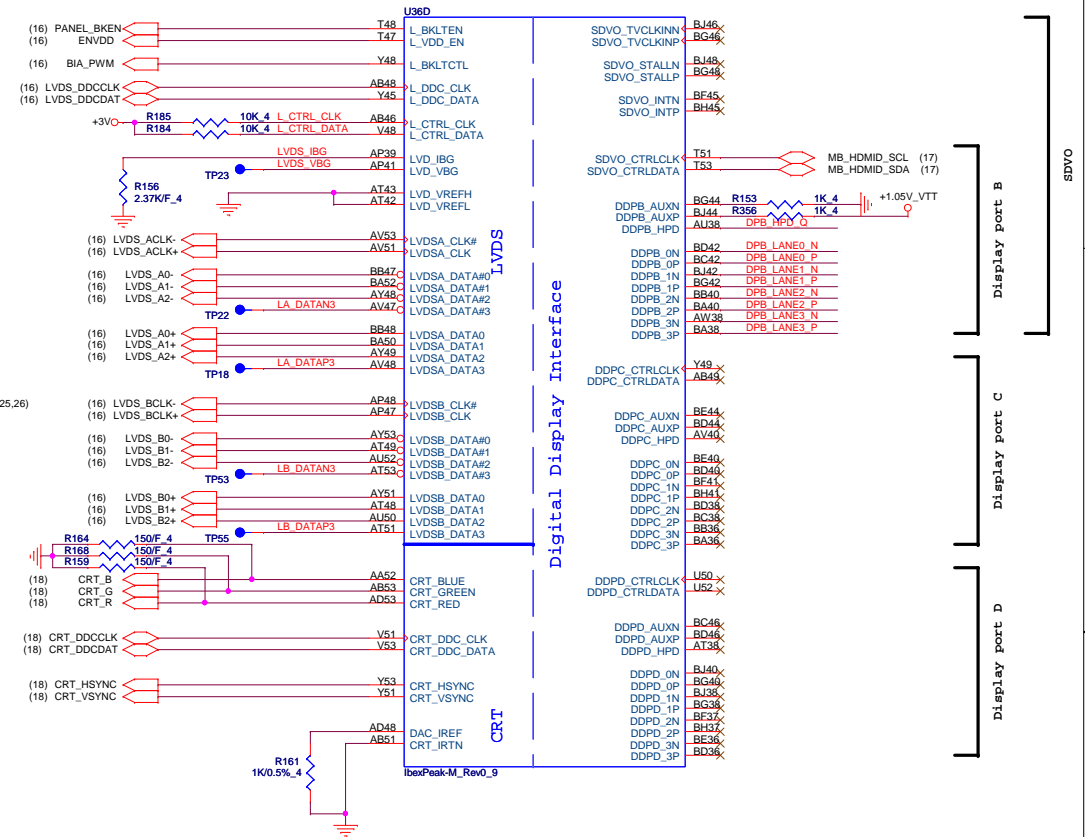
CFG7 R45 *3.01K/F 4

	PROJECT KL3 NOTE Calpella DIS	
	Quanta Computer Inc.	
Size Custom	Document Number PROCESSOR 4/4(GND)	Rev 1A
Date:	Wednesday, December 23, 2009	Sheet 7 of 43

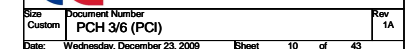
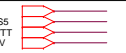
IBEX PEAK-M (DMI, FDI, GPIO)



IBEX PEAK-M (LVDS, DDI)



TPM Function	R9386
Enable	Stuff
Disable	NC (Default)



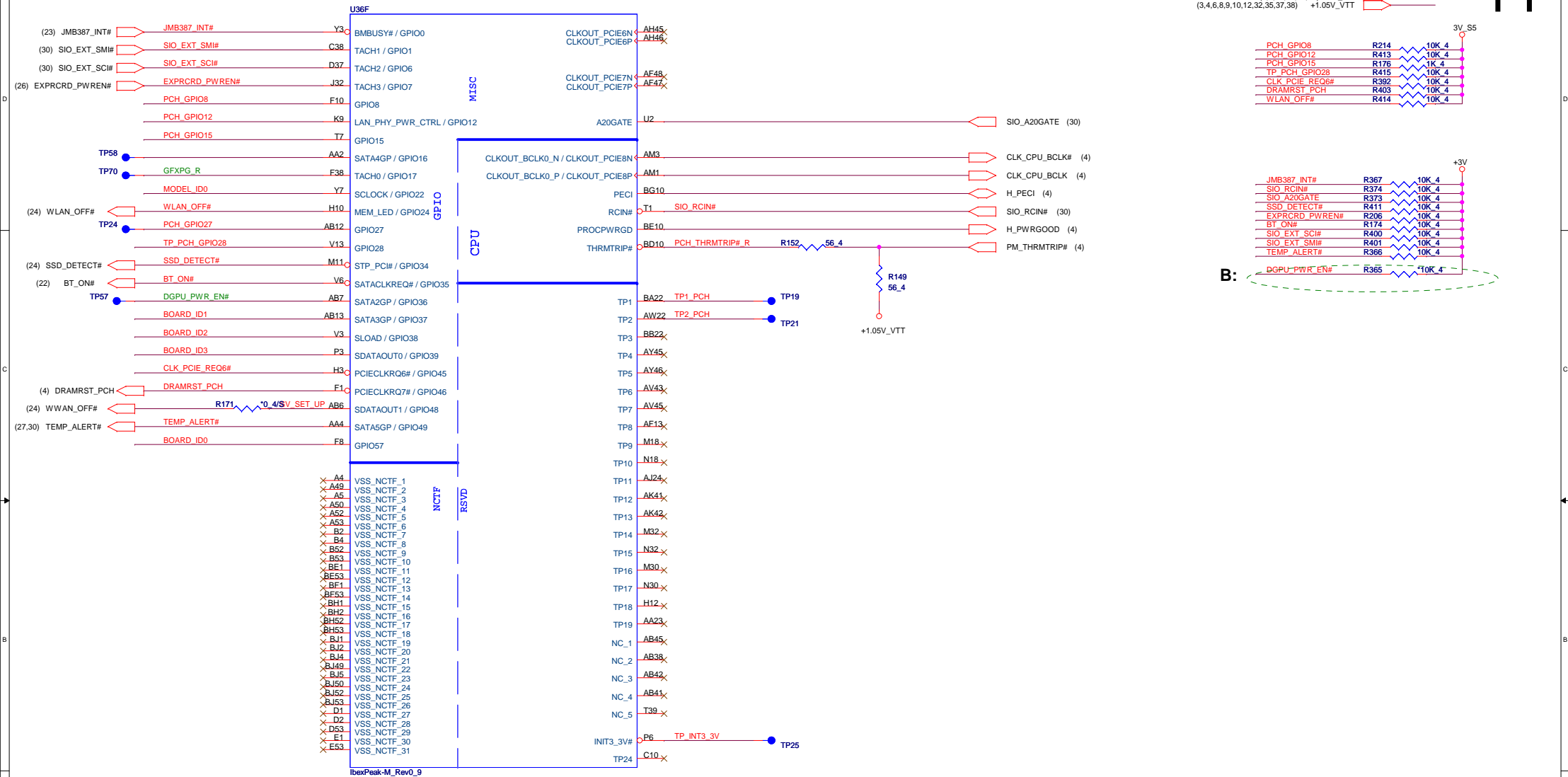
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

(3,4,8,9,10,12,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,32,33,37)

+3V

(8,9,10,12,24,32) 3V_S5
(3,4,6,8,9,10,12,32,35,37,38) +1.05V_VTT

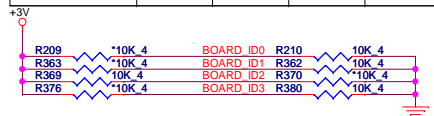
11



B:

Board ID

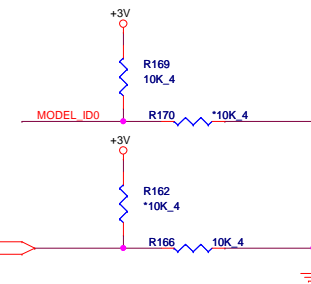
Board ID For Function	ID3 GPIO39	ID2 GPIO38	ID1 GPIO37	ID0 GPIO57
SDV	0	0	0	0
SIV	0	0	0	1
SIT	0	0	1	0
SVT	0	1	0	0
SOVP	1	0	0	0



Model ID

Model ID	MODEL_ID0	MODEL_ID1
14"	0	1
15"	1	0
Default	1	1

(9) MODEL_ID1



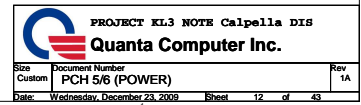
SV_SET_UP 1-X High = Strong (Default)

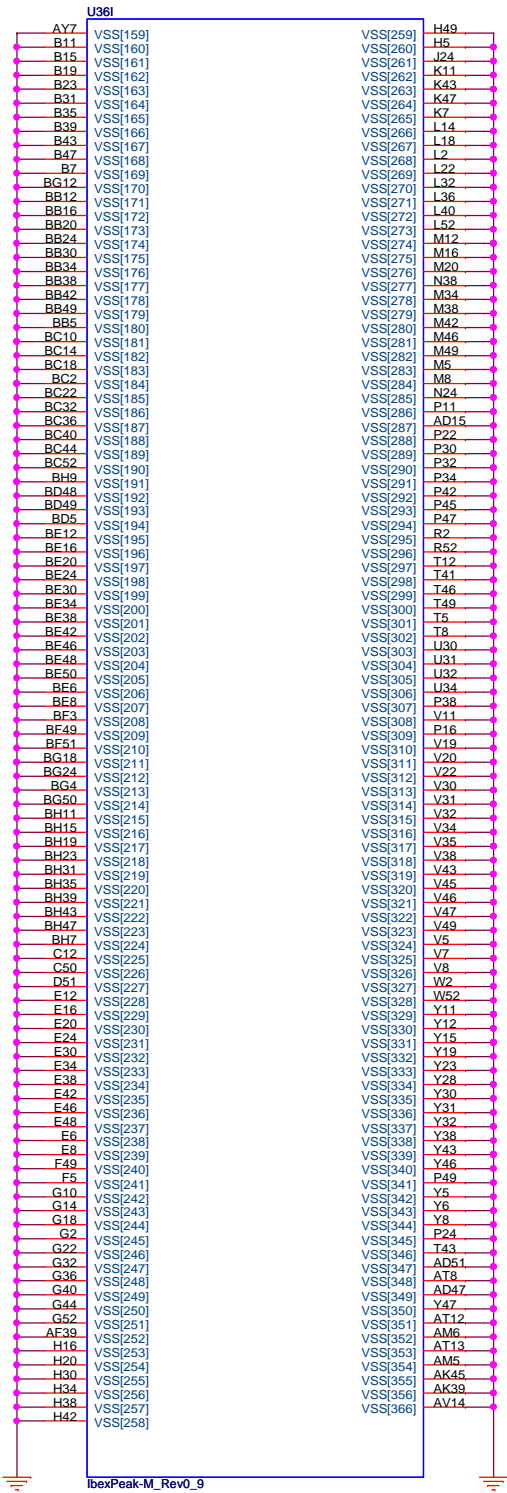
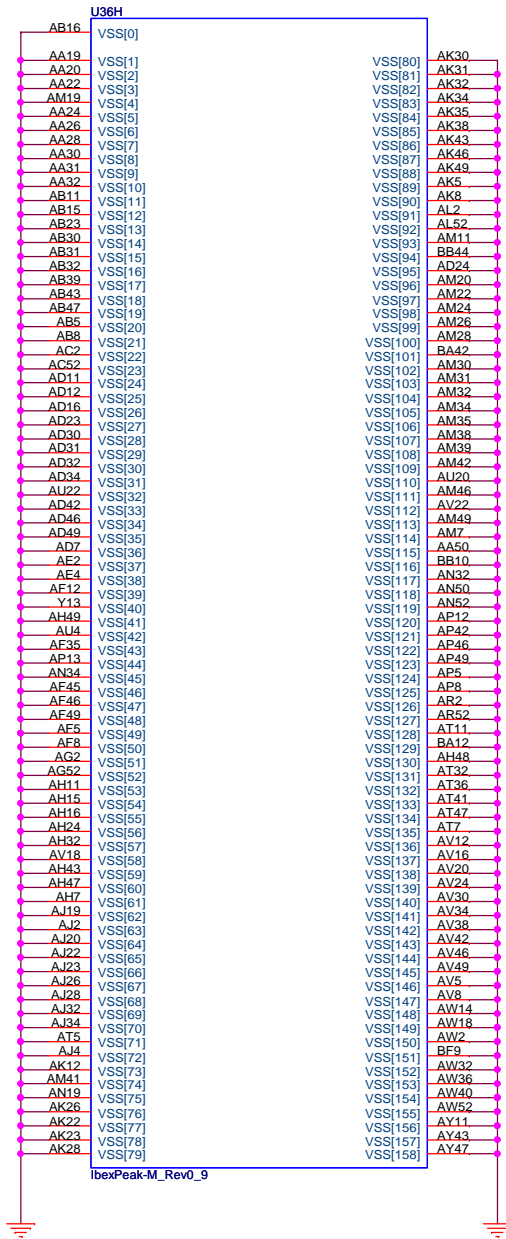
PROJECT KL3 NOTE Calpella DIS

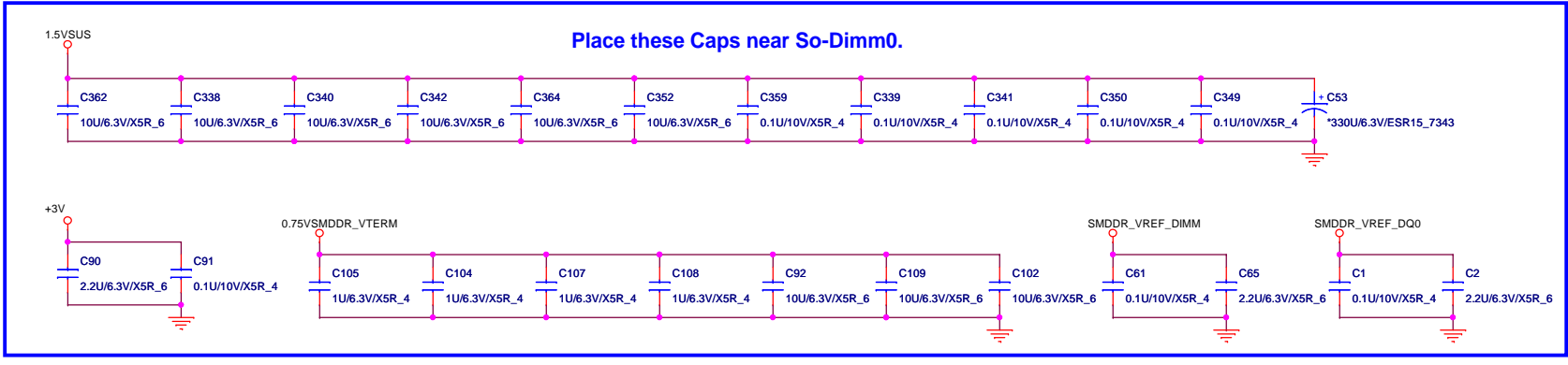
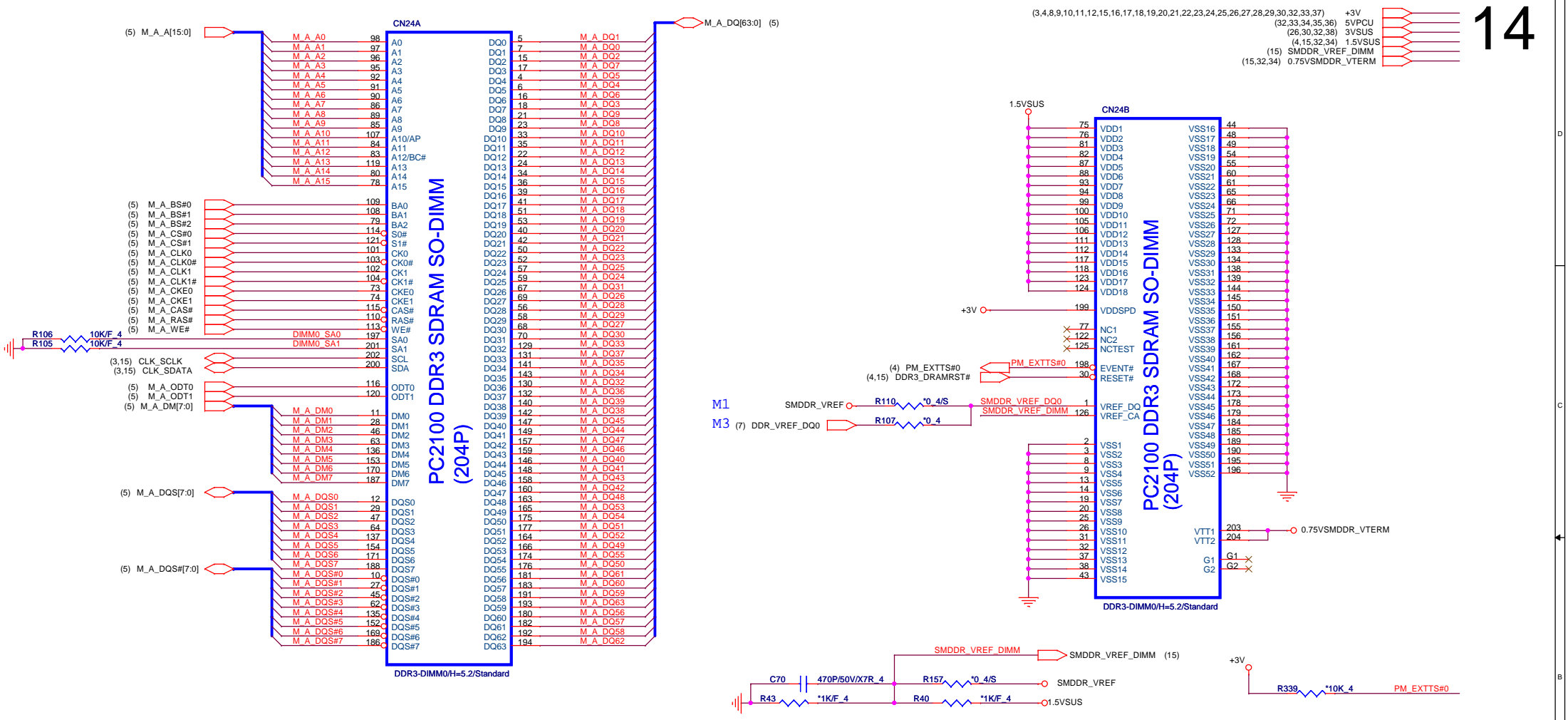
Quanta Computer Inc.

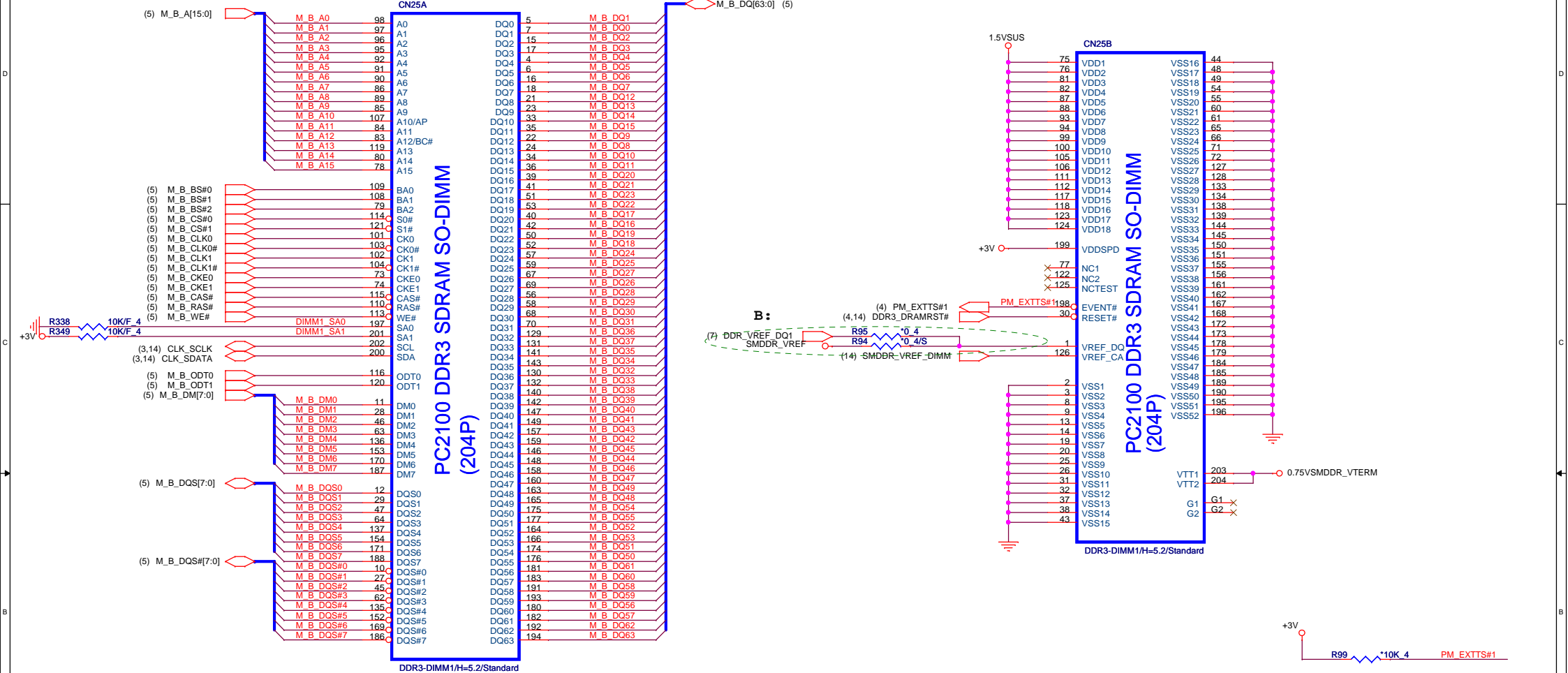
Size Custom Document Number PCH 4/6 (GPIO) Rev 1A

Date: Wednesday, December 23, 2009 Sheet 11 of 43

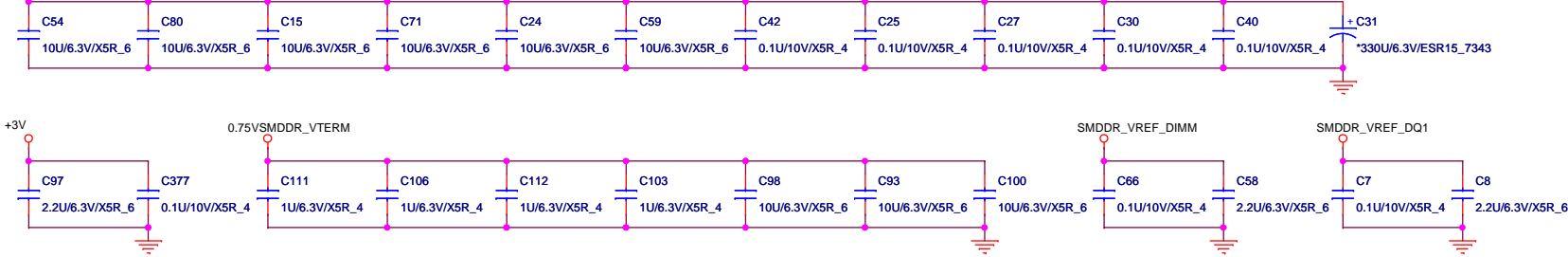




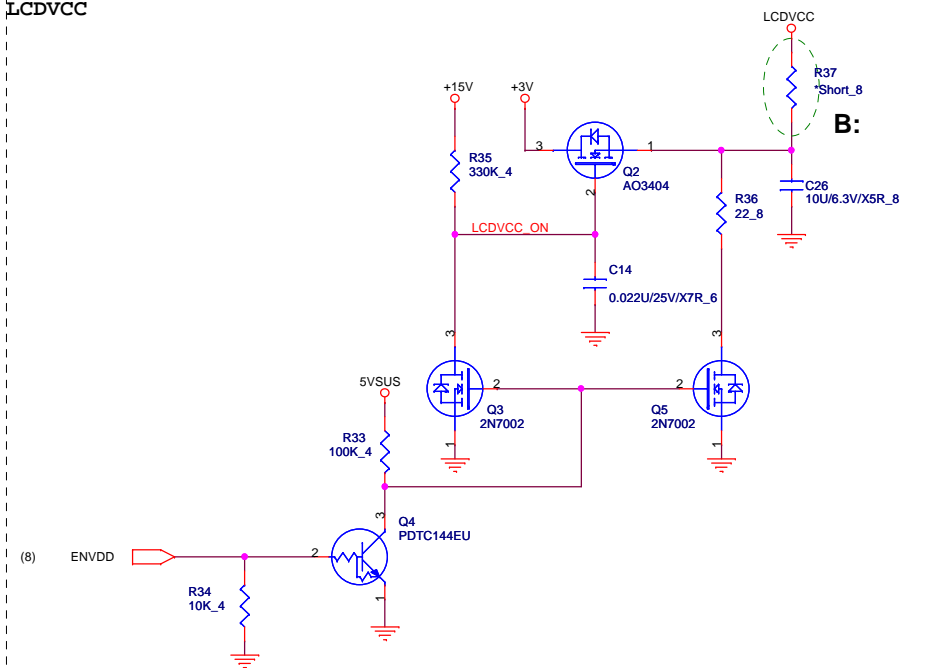




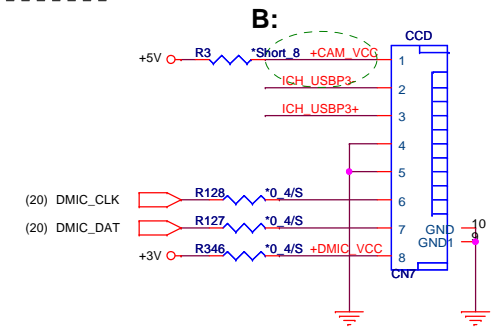
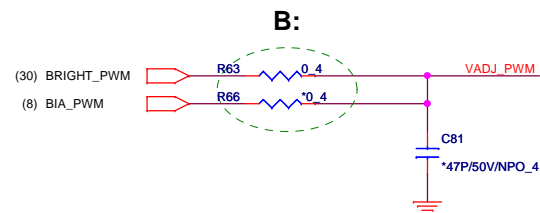
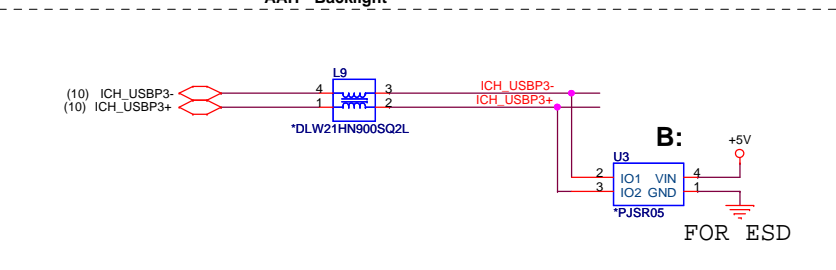
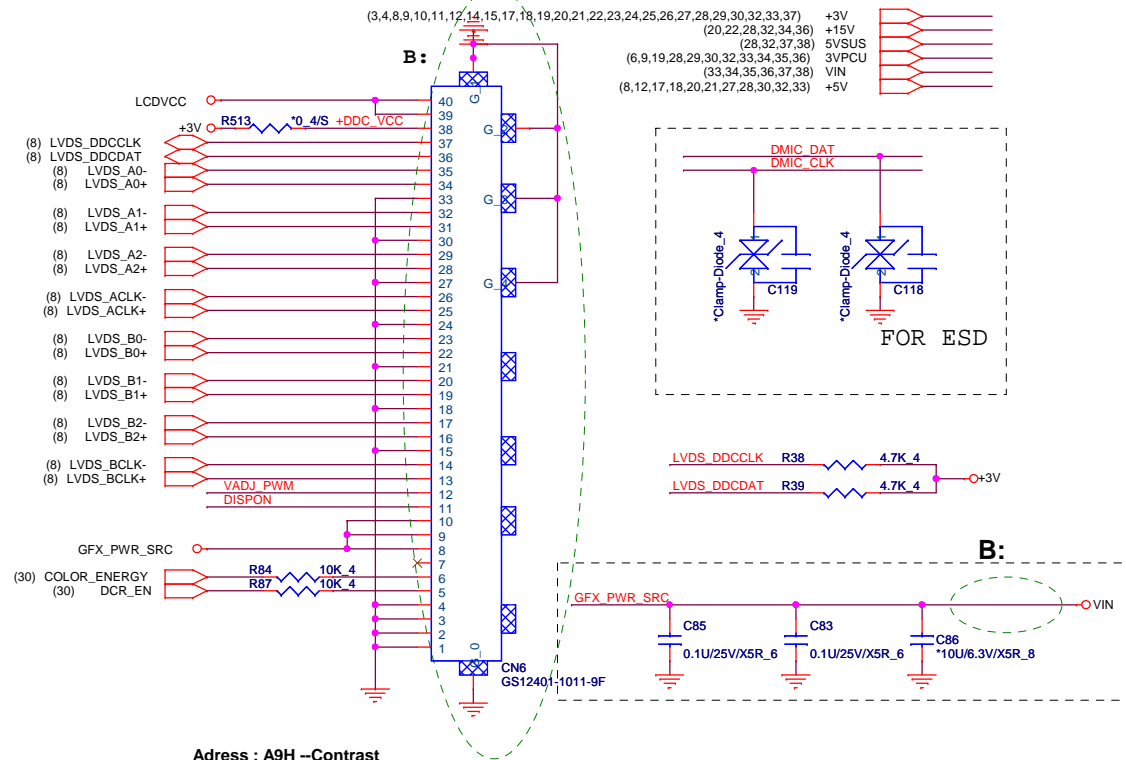
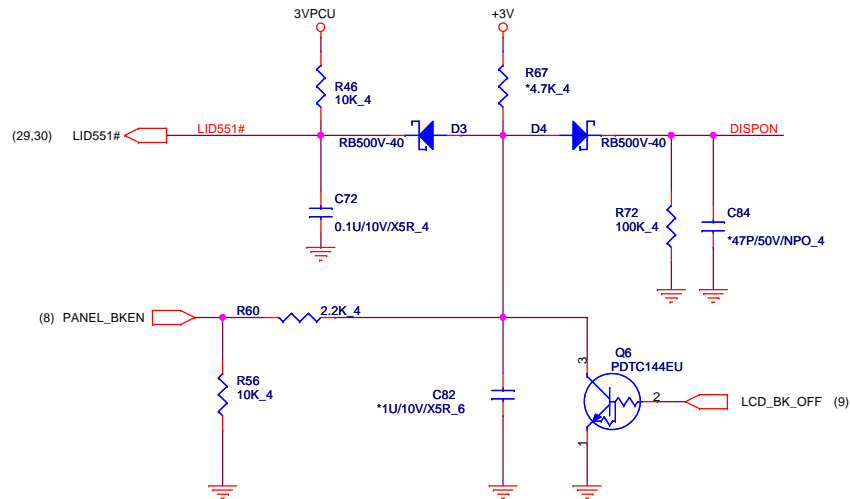
Place these Caps near So-Dimm1.

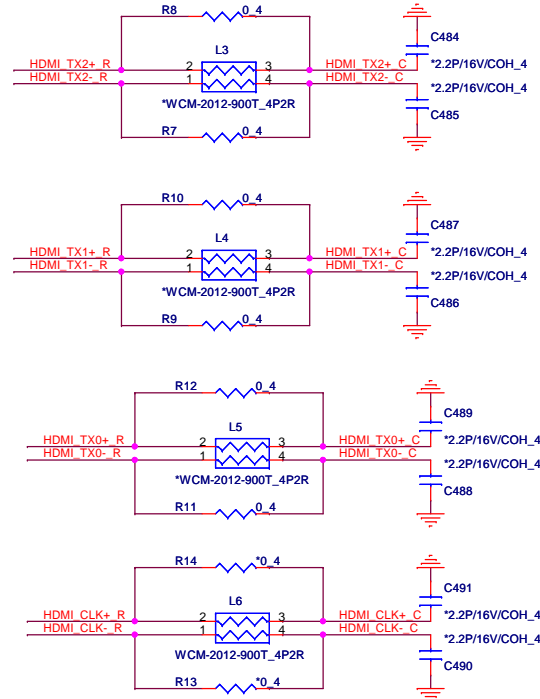
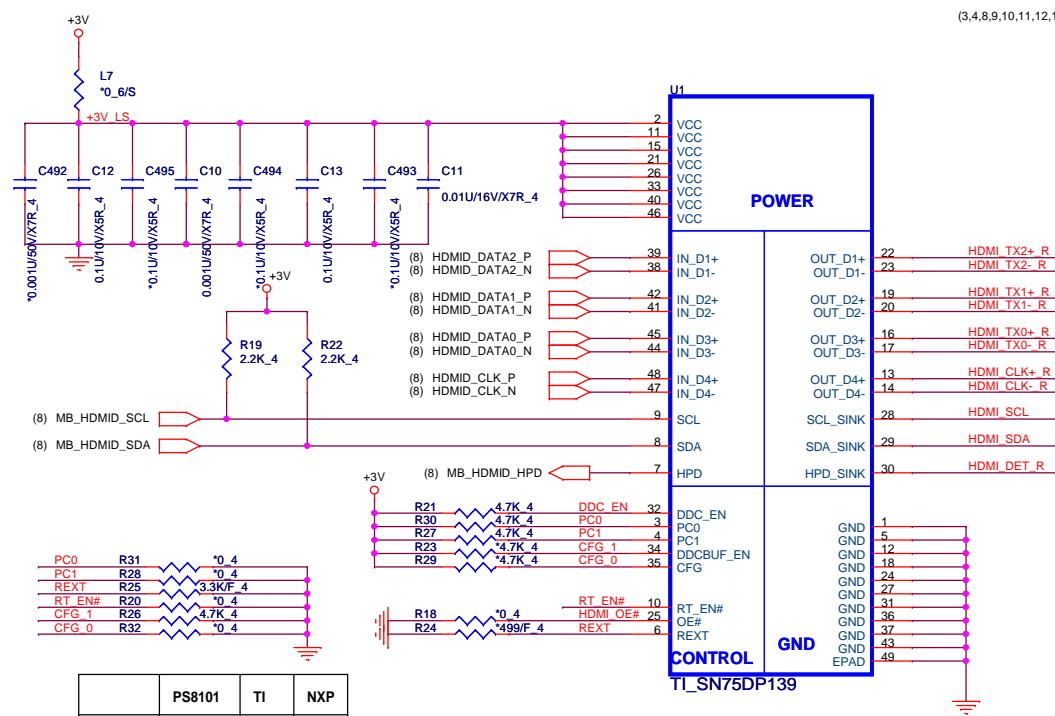


LCDVCC



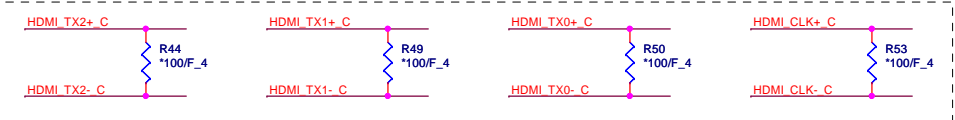
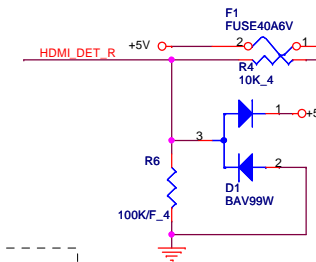
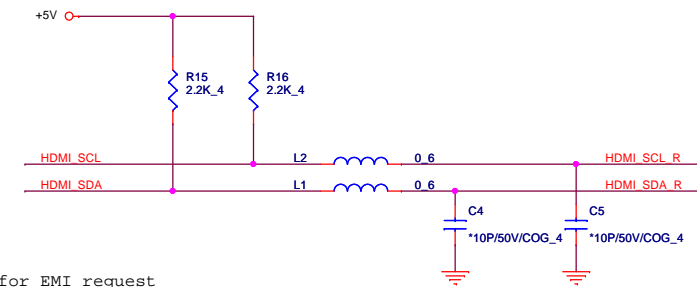
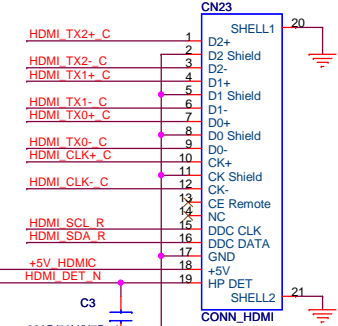
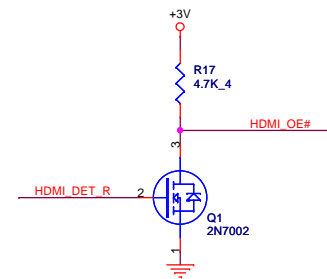
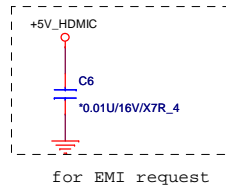
back light

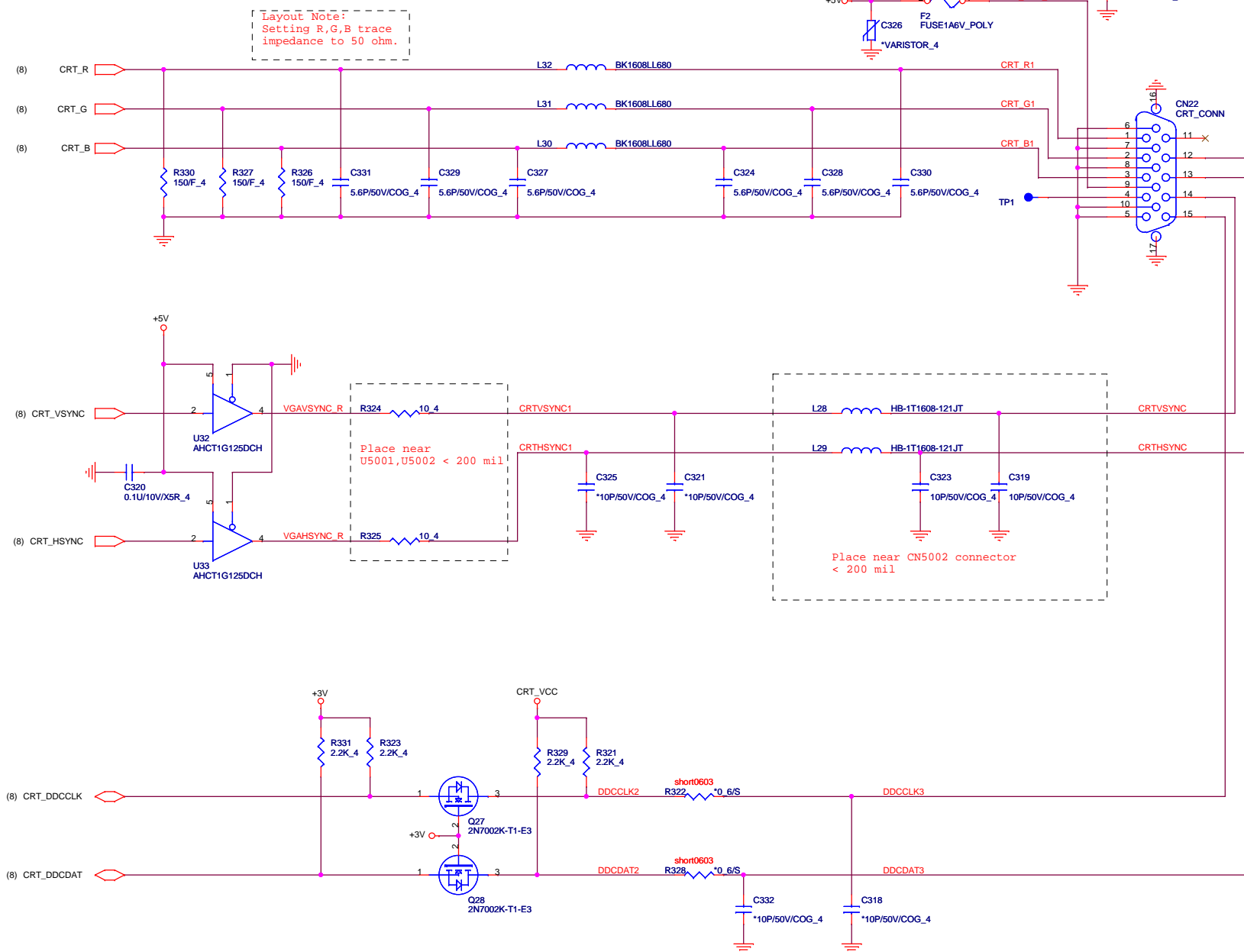


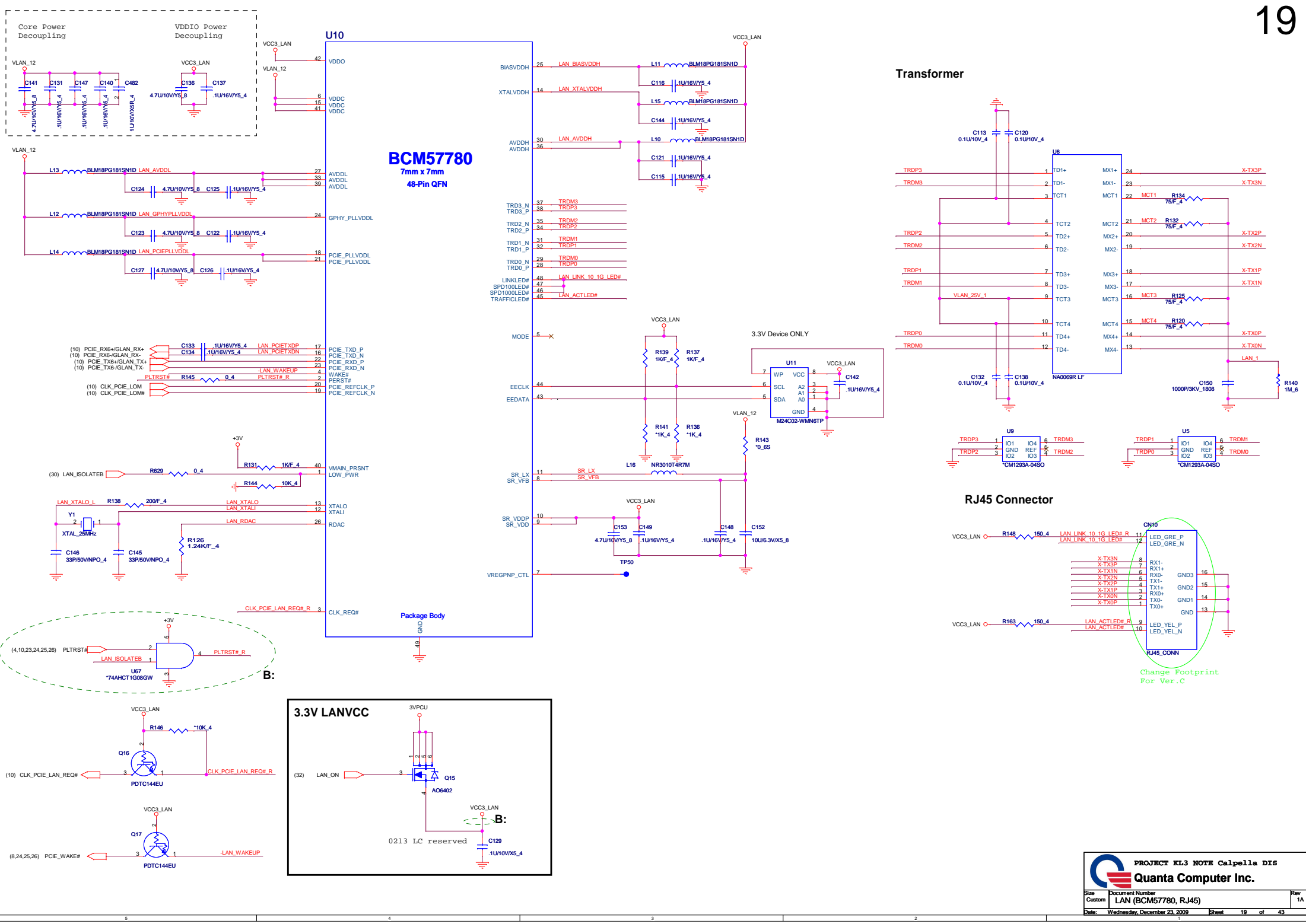


EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommended
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

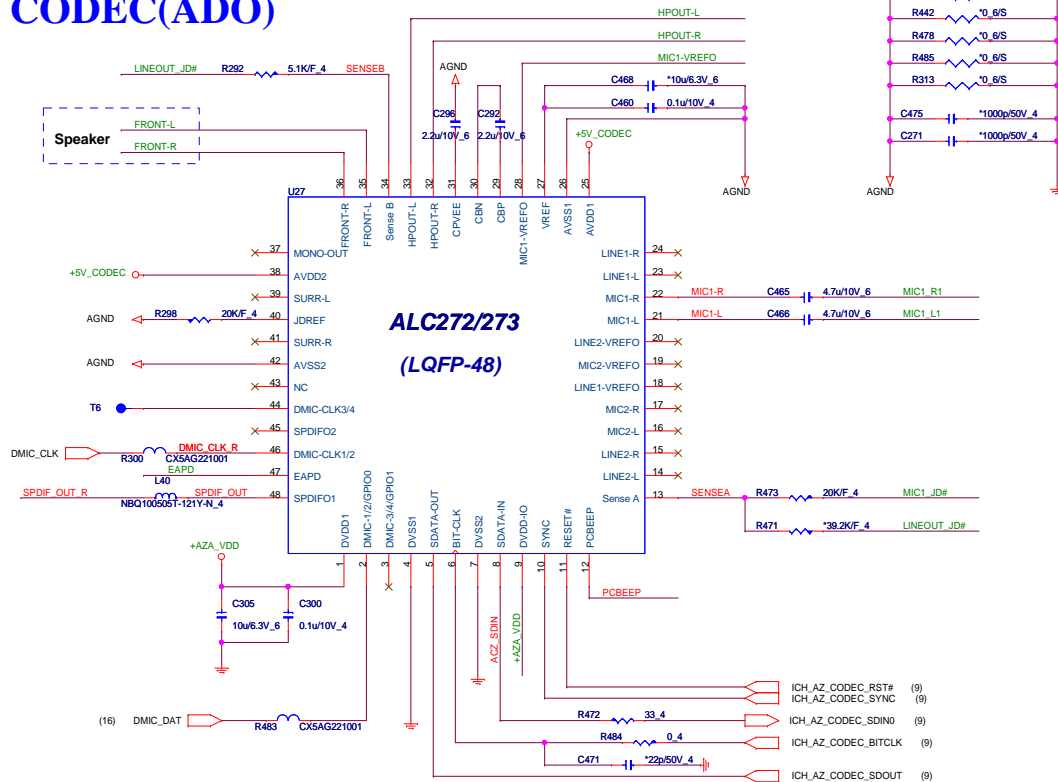
PS8101 Pin34/35 is NC
SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CFG1:CFG0=0:1 VIL:<0.36V VOL:0.55V
CFG1:CFG0=1:0 VIL:<0.44V VOL:0.65V
CFG1:CFG0=1:1 VIL:<0.36V VOL:0.6V



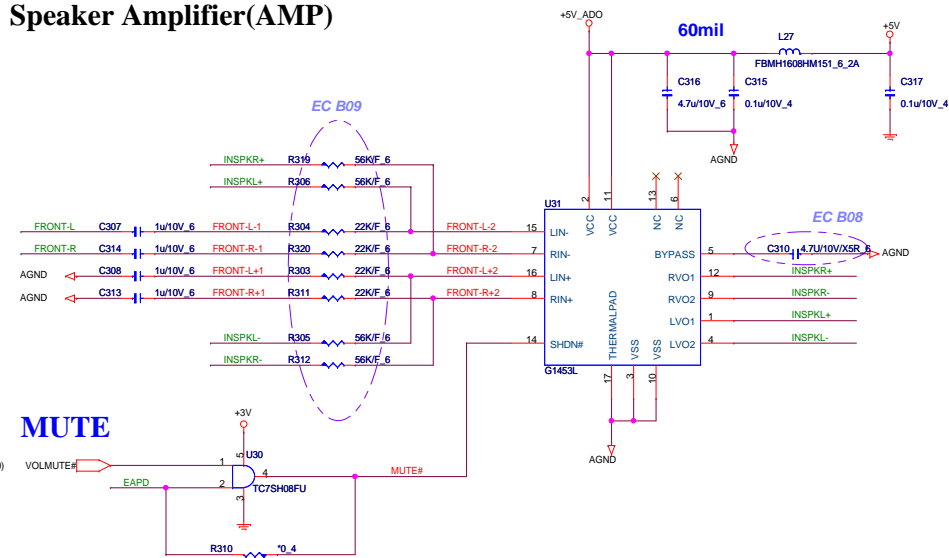




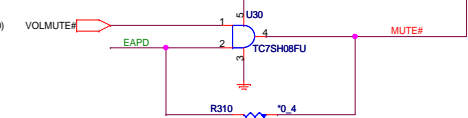
CODEC(ADO)



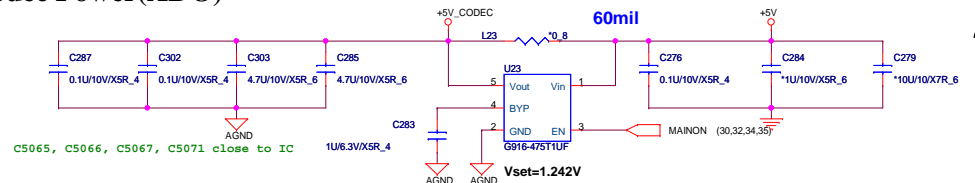
Speaker Amplifier(AMP)



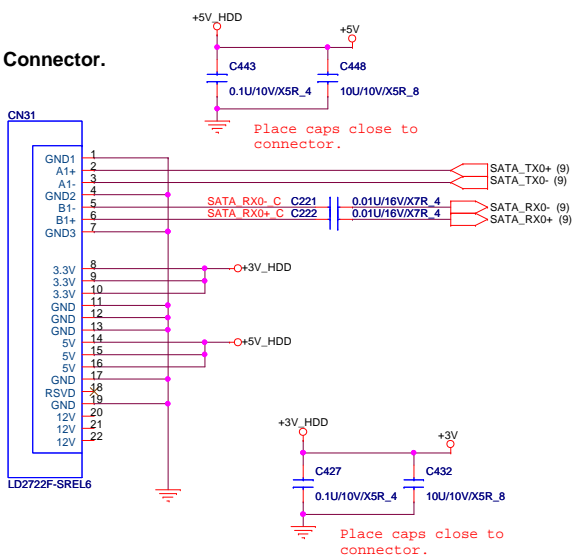
MUTE



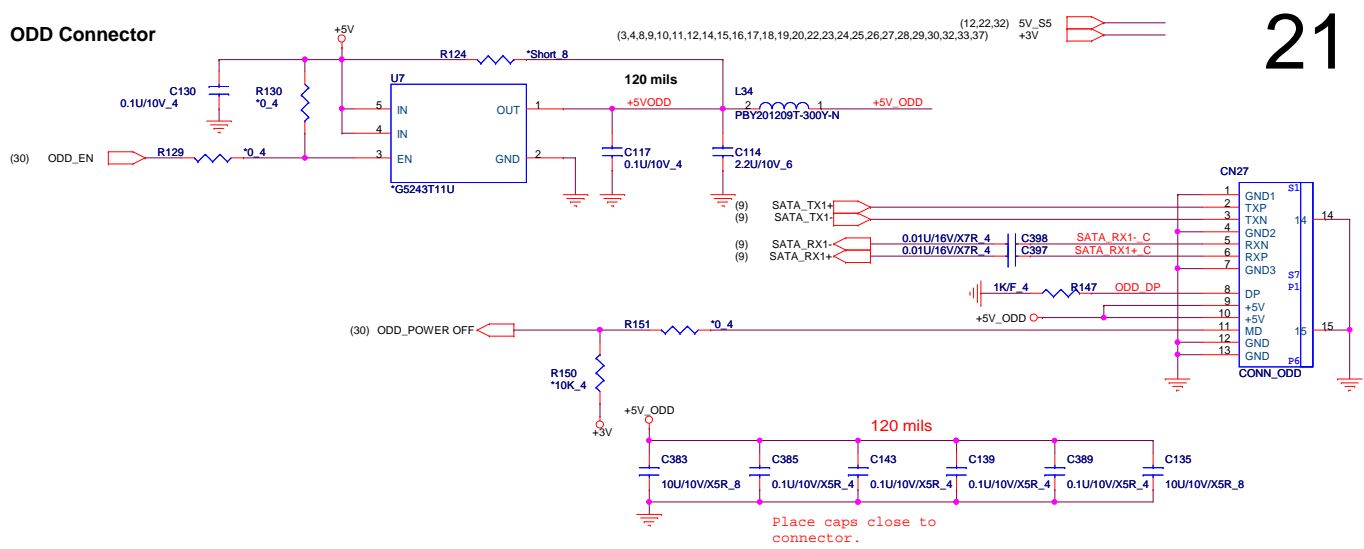
Codec Power(ADO)



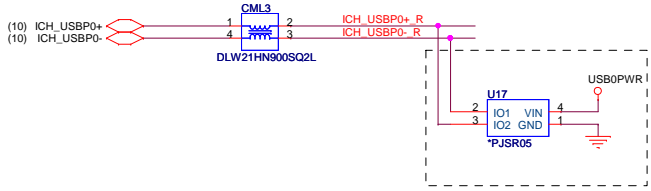
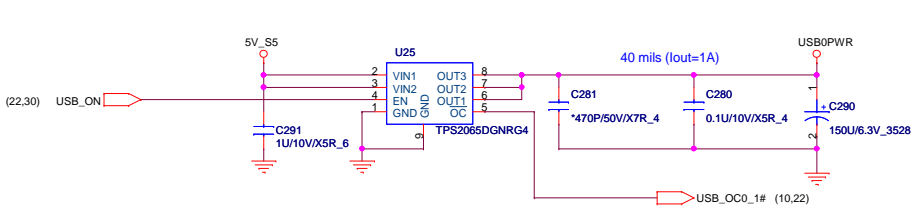
SATA Connector.



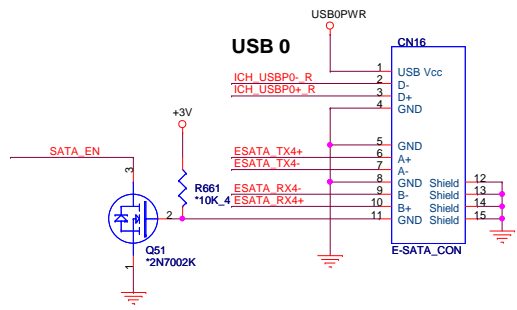
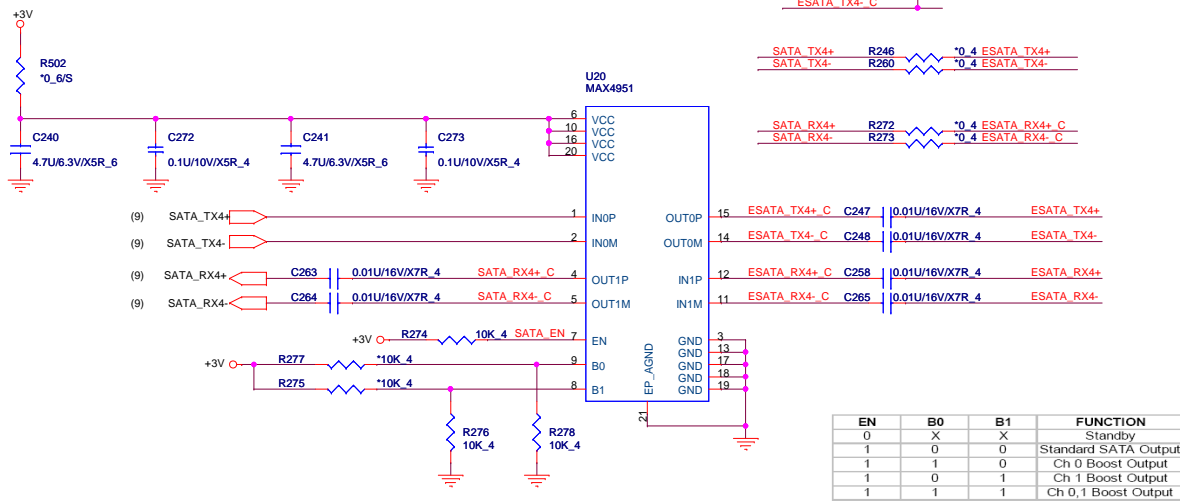
ODD Connector



USB + E-SATA

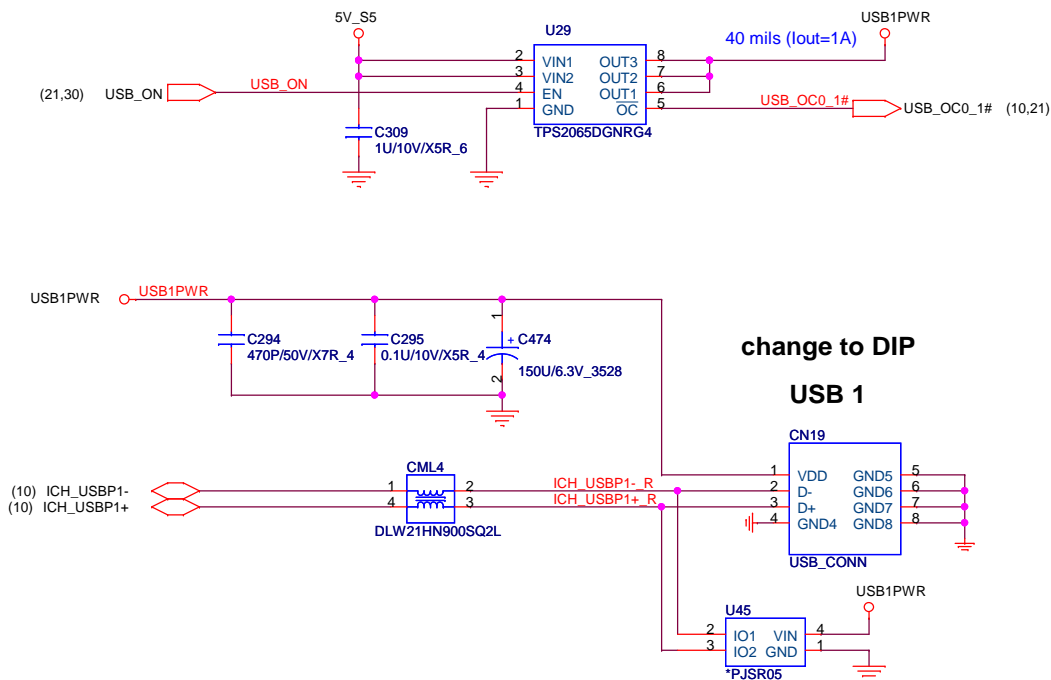


E-SATA RE-DRIVER

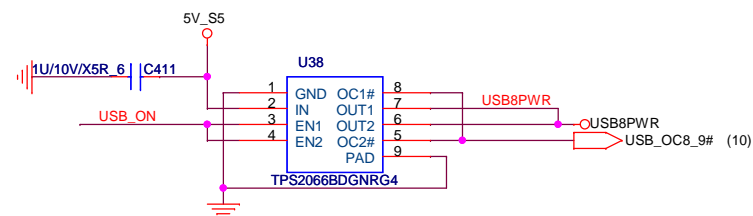
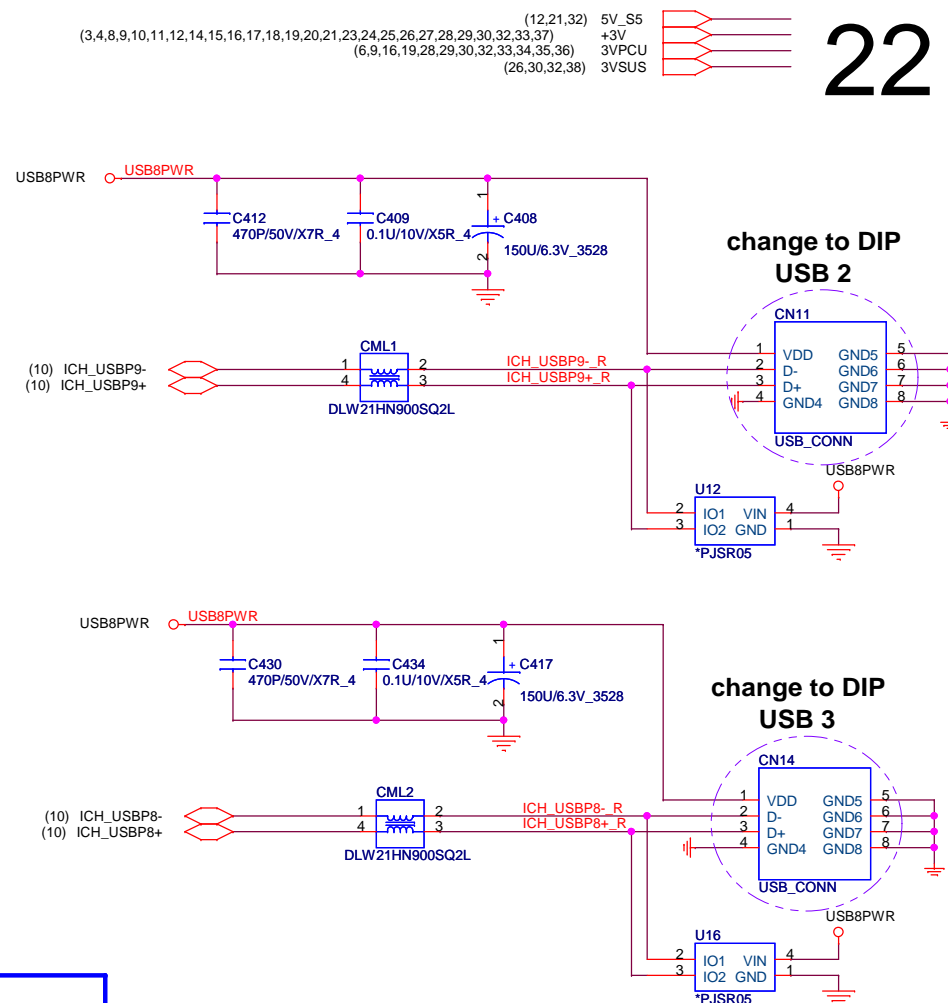
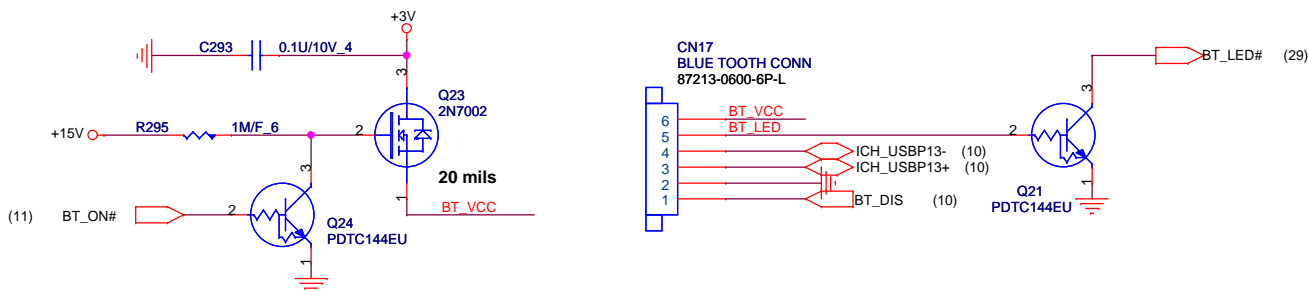


EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

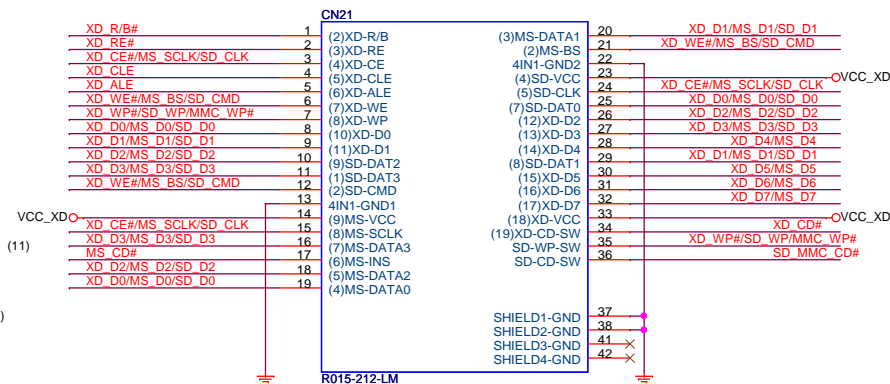
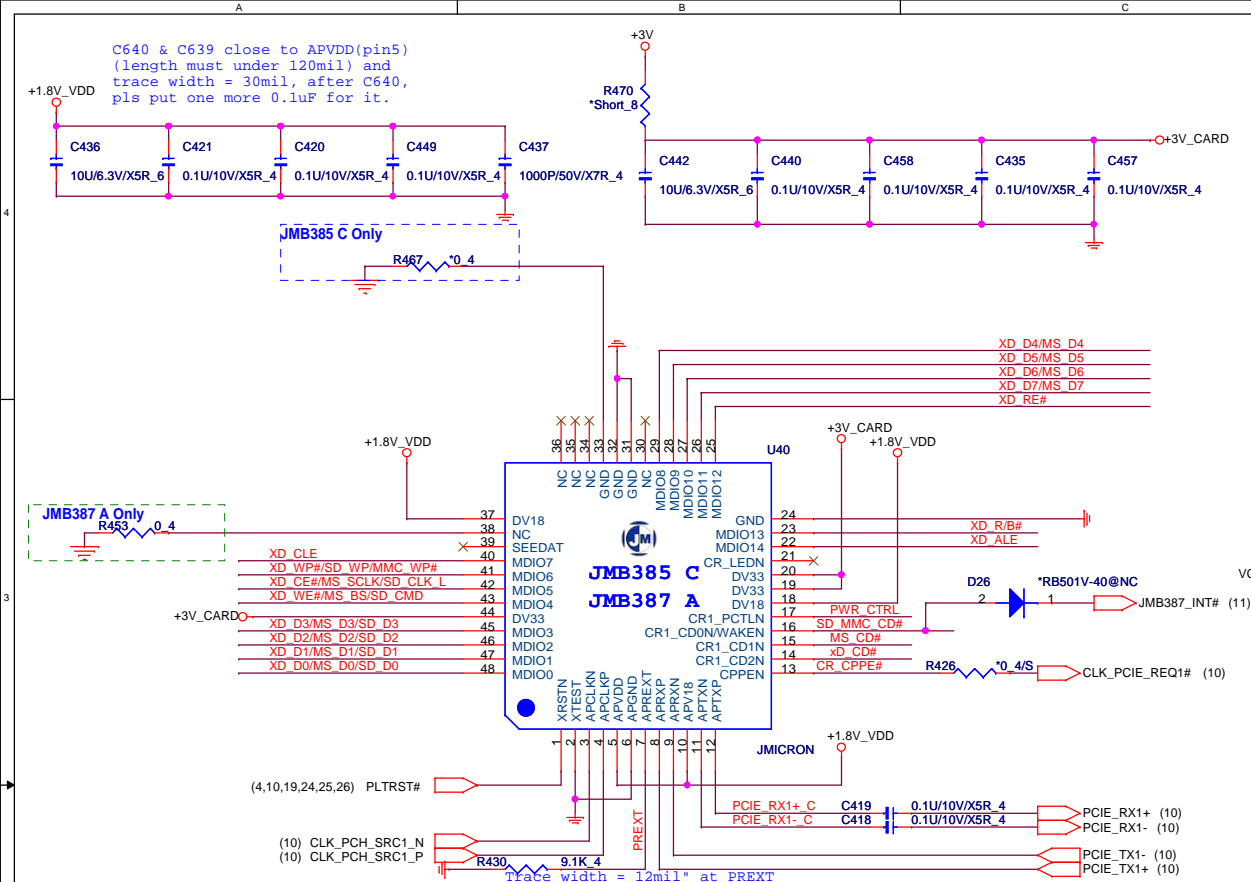
USBX3



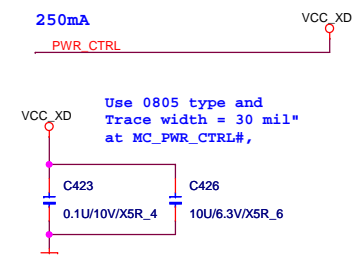
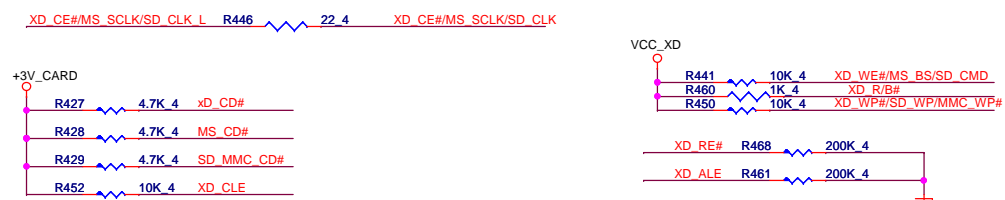
BLUETOOTH



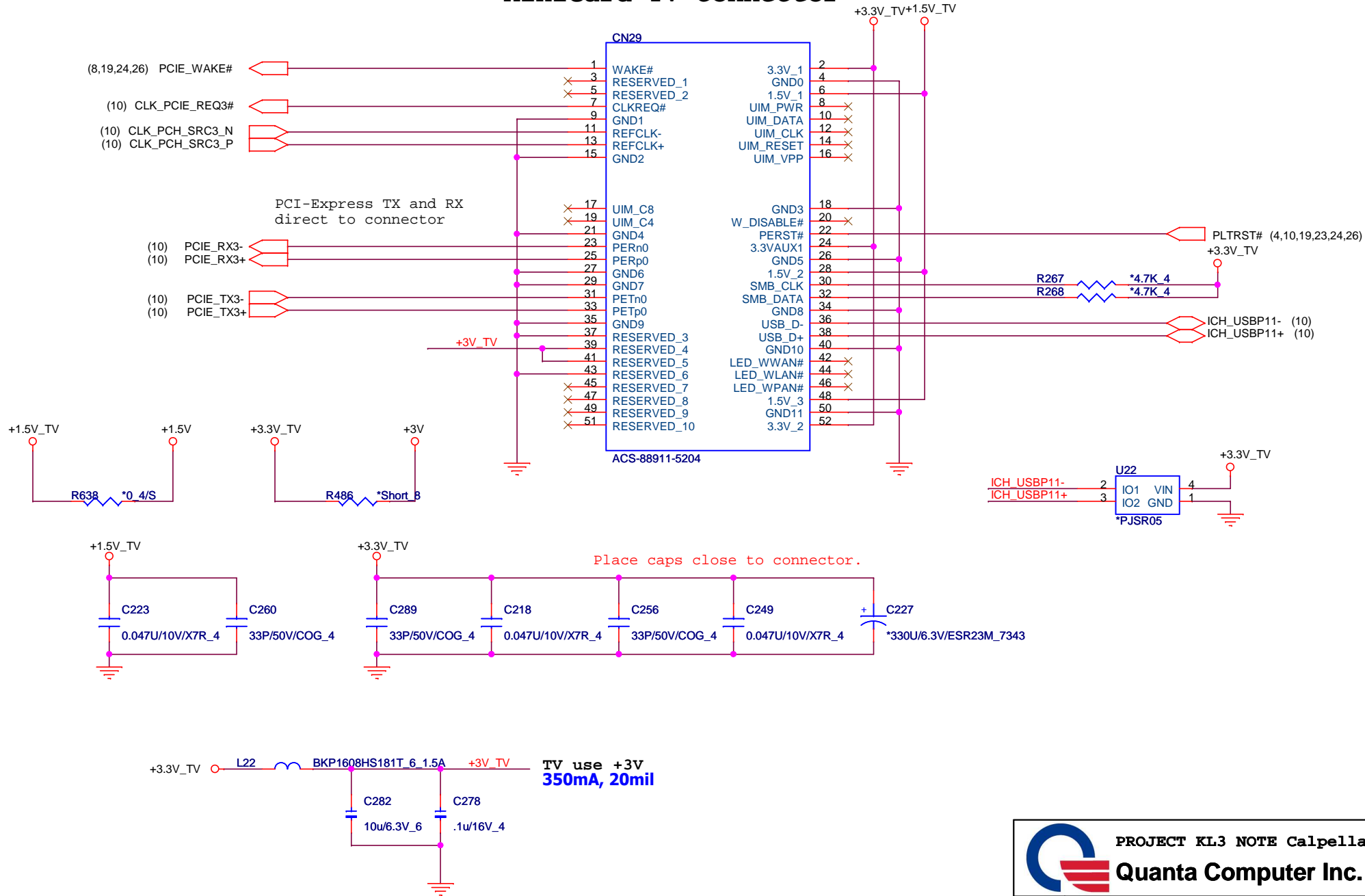
5 IN 1 CARD READER



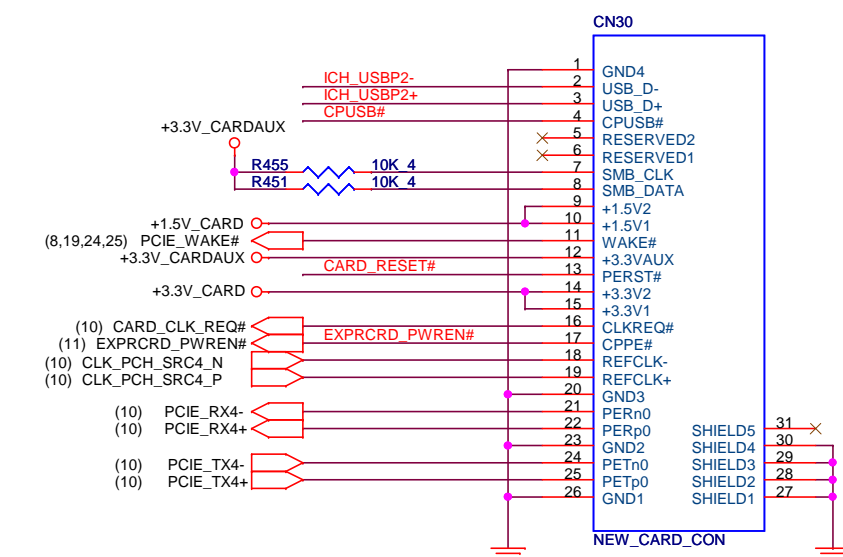
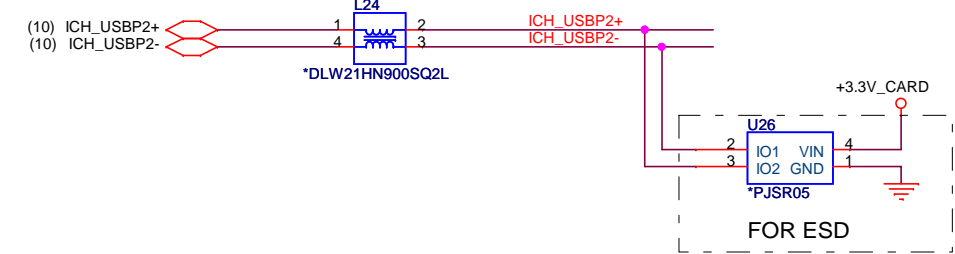
Memory Card Power Supply



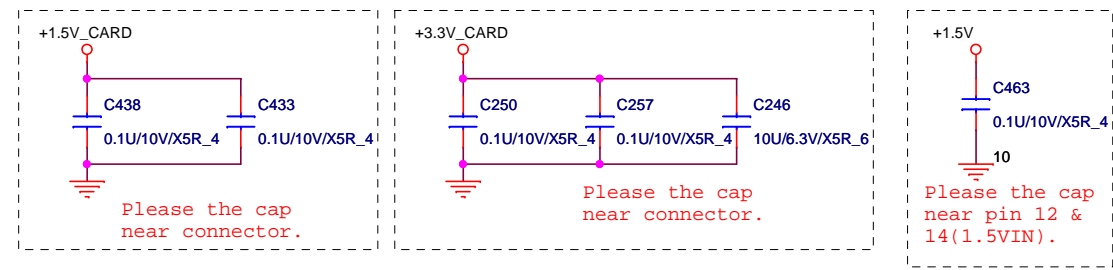
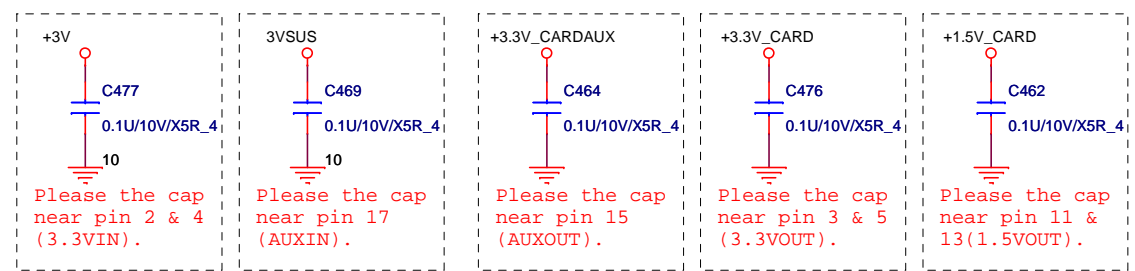
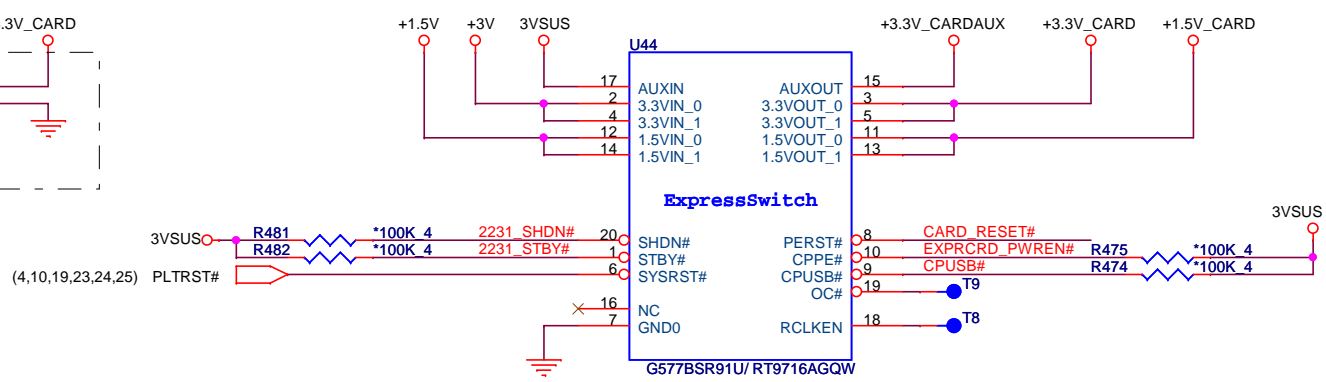
MiniCard TV connector



Express Card

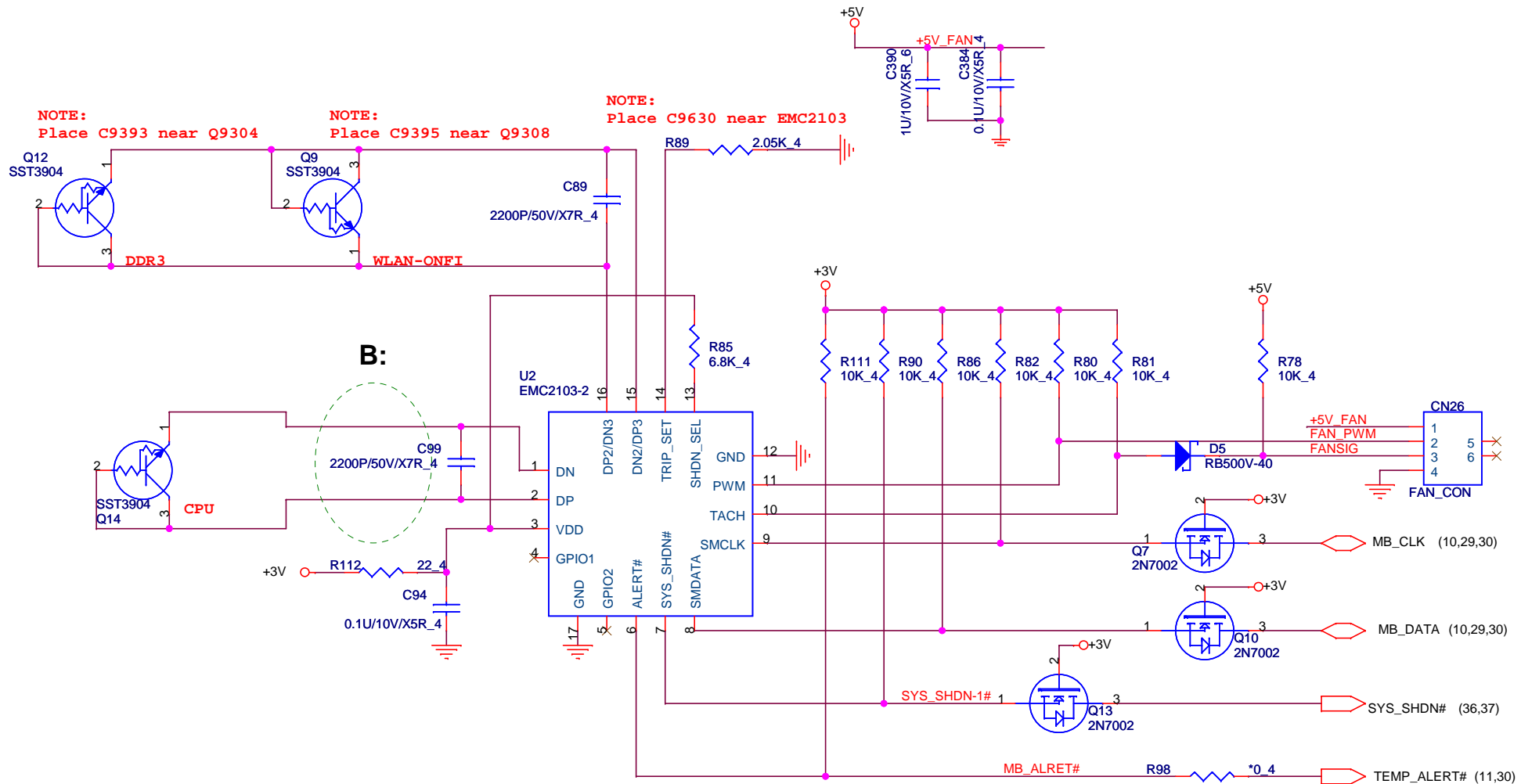


JAE PX10FS16PH-26P

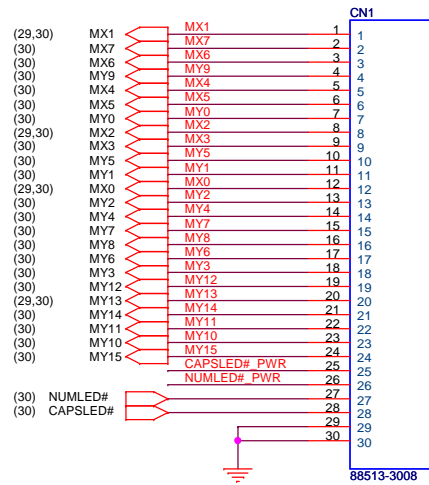


FAN CONTROL

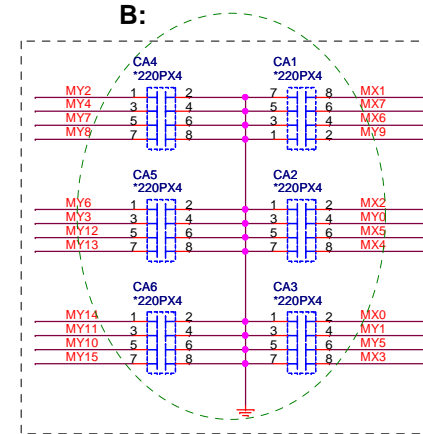
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KEYBOARD



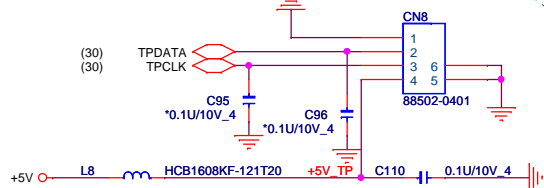
(8,12,16,17,18,20,21,27,30,32,33) +5V
(6,9,16,19,29,30,32,33,34,35,36) 3VPCU



For EMI request

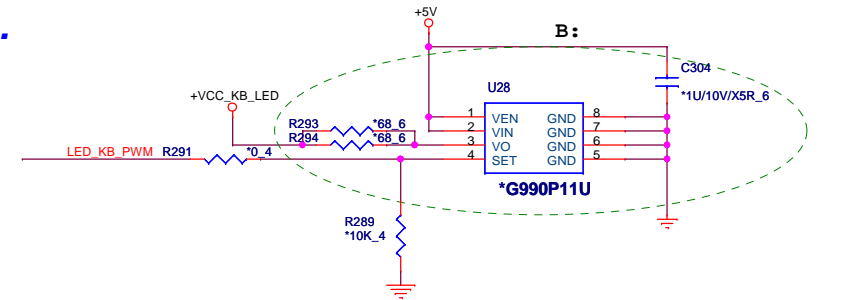
Touch pad

B:

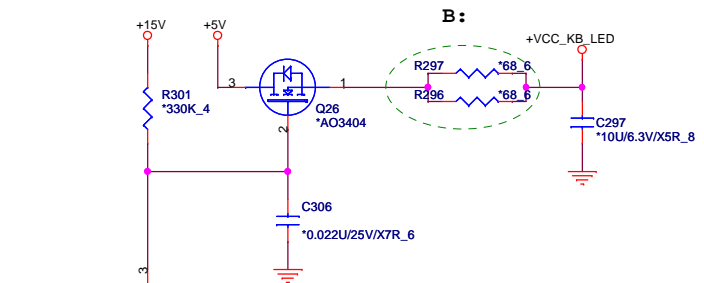


Backlight Keyboard Con.

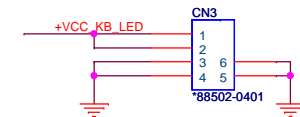
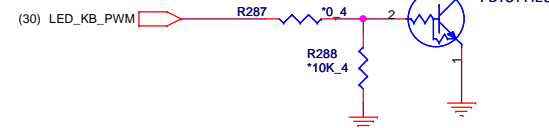
B:



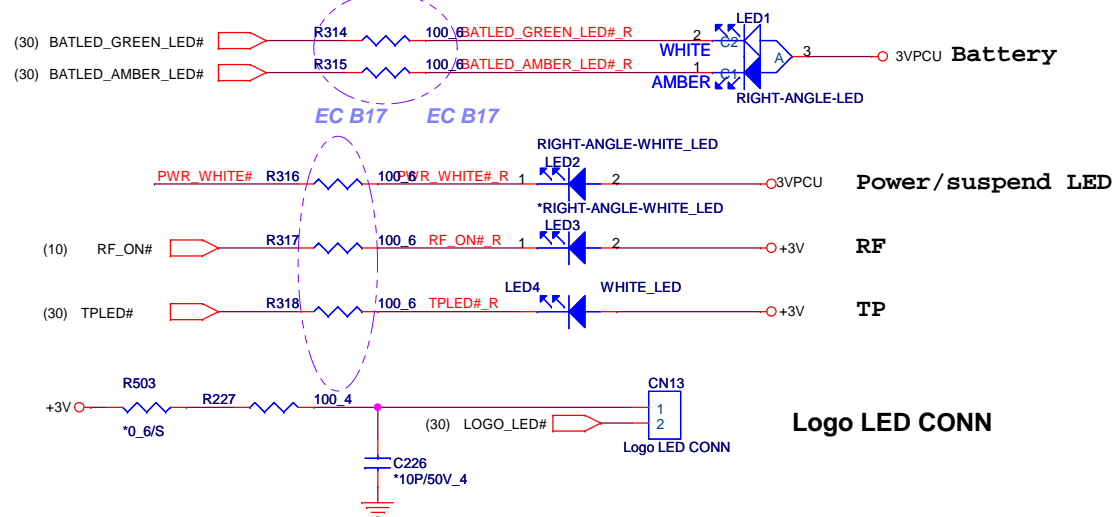
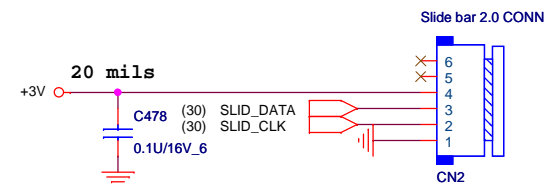
B:



EC PWM Pin

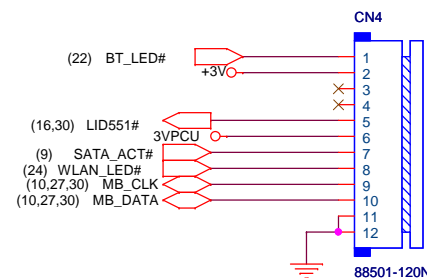


(6,9,16,19,28,30,32,33,34,35,36) 3VPCU
 (3,4,8,9,10,11,12,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,30,32,33,37) +3V

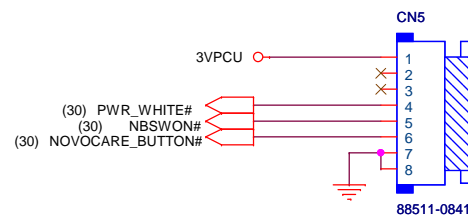


UP LED BOARD

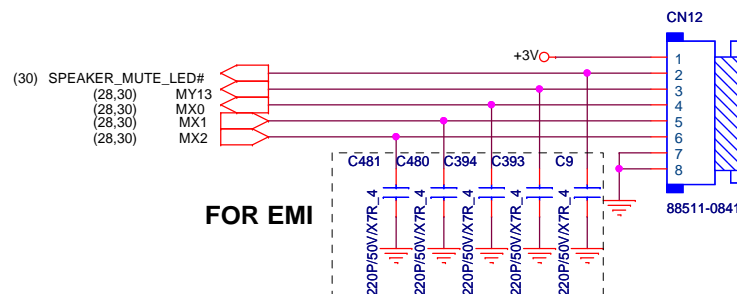
BT
 LID SWITCH
 HDD
 WLAN
 LIGHT SENSOR

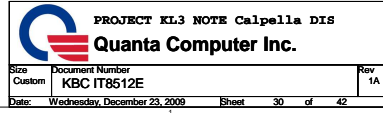


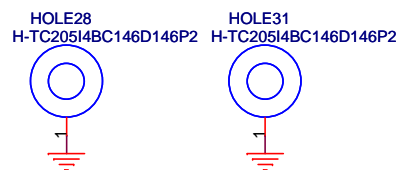
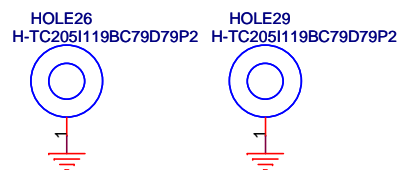
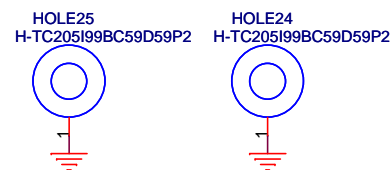
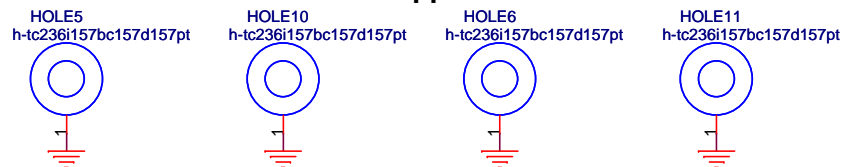
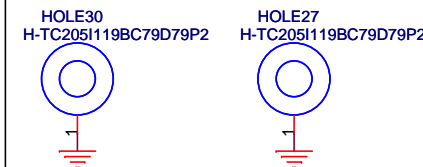
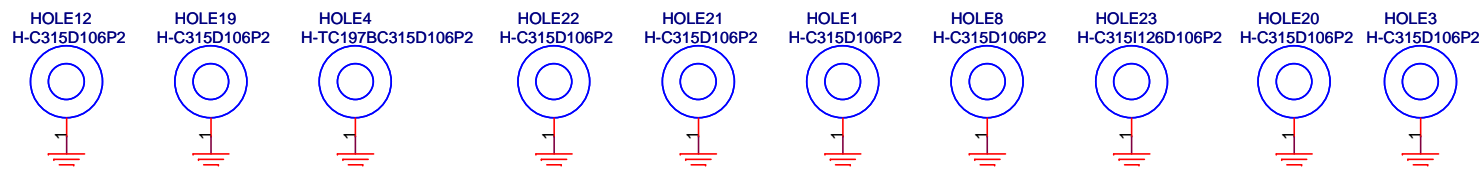
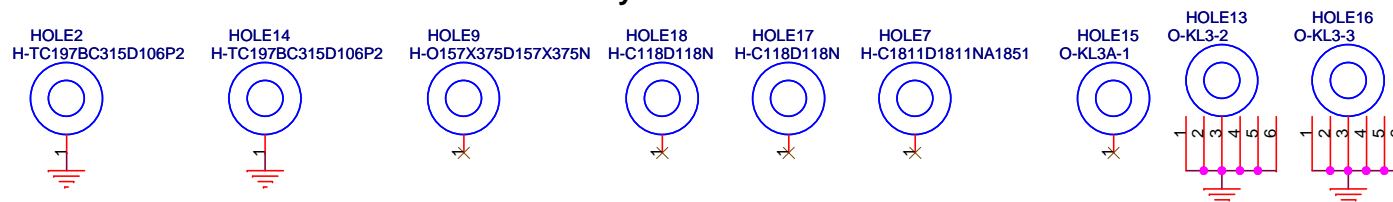
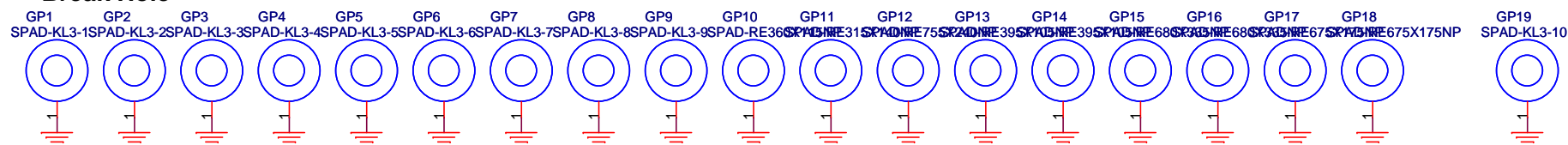
LEFT POWER BOARD



RIGHT VOLUME BOARD





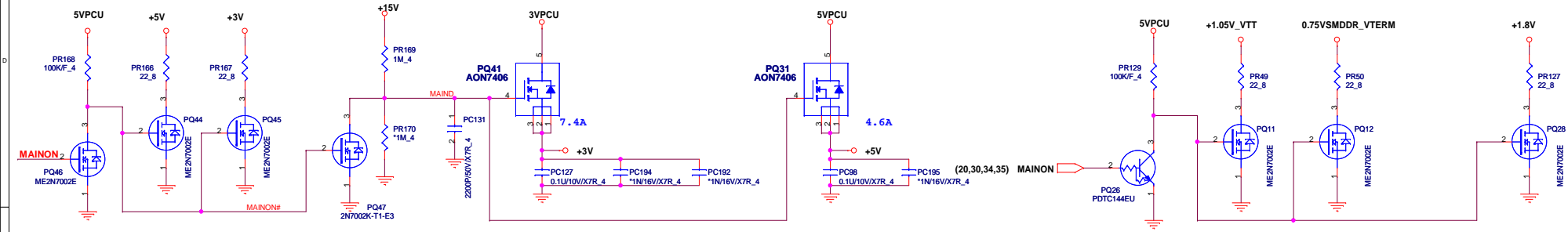
MiniCard WLAN**MiniCard WWAN****Hole for PCH support****Drink Hole****ESD for ESATA****Hole for CPU support****VGA nut****MiniCard TV****Boundary Hole****Boundary Hole****Card reader board nut****Break Hole**

PROJECT KL3 NOTE Calpella DIS

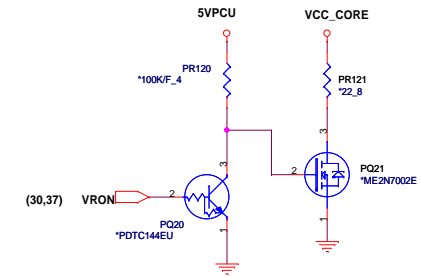
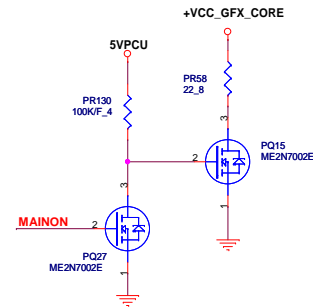
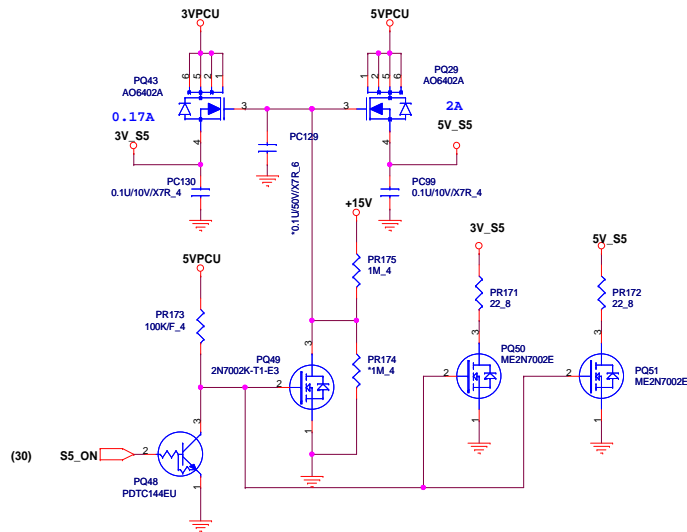
Quanta Computer Inc.Size
CustomDocument Number
HOLD & SKEWRev
1A

Date: Wednesday, December 23, 2009 Sheet 31 of 42

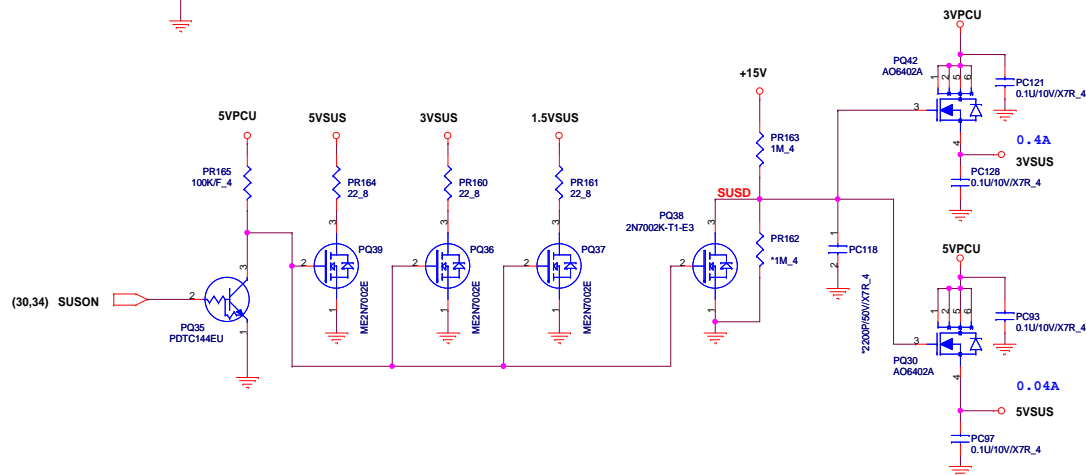
+3V, +5V



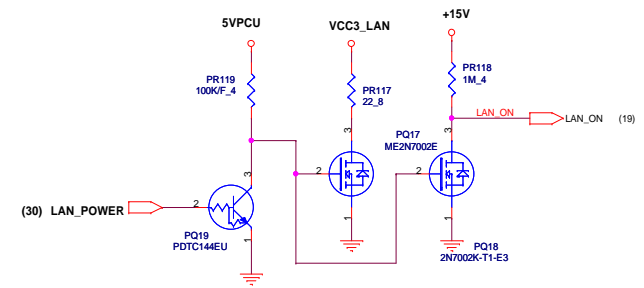
3V_S5, 5V_S5



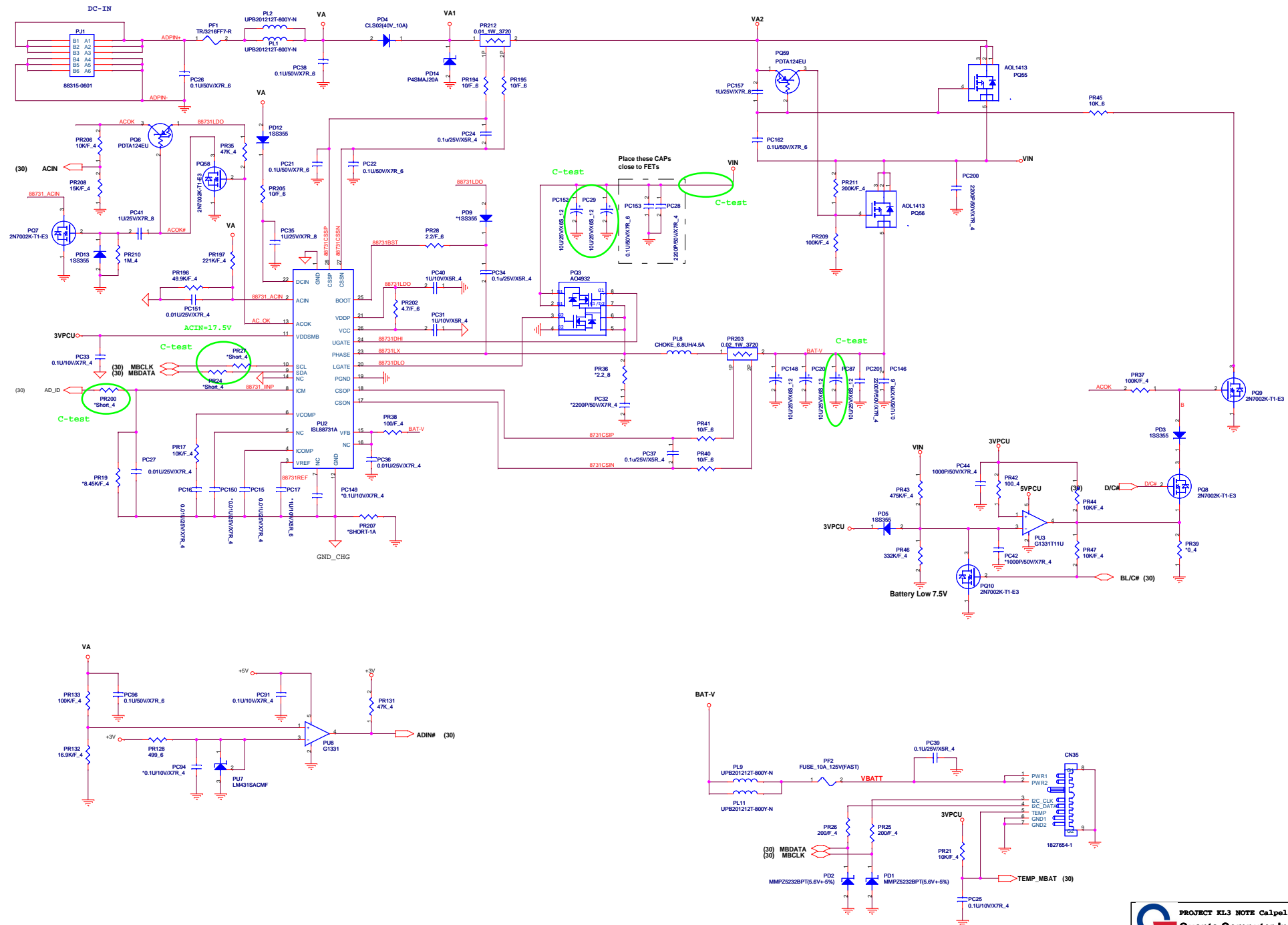
3VSUS, 5VSUS

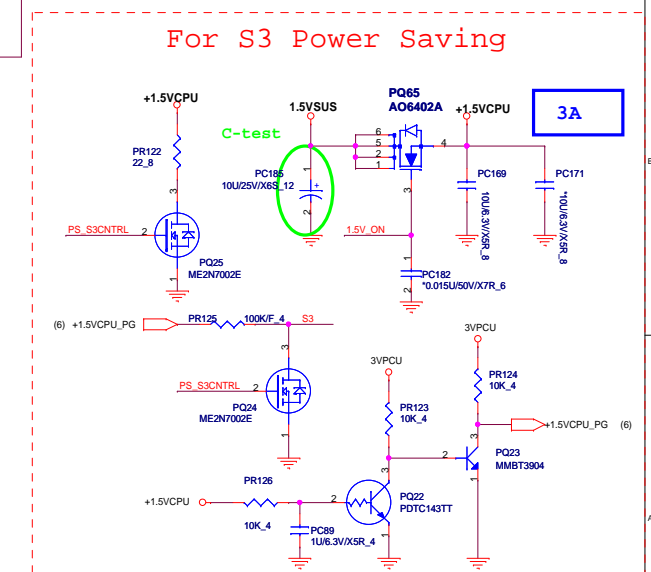


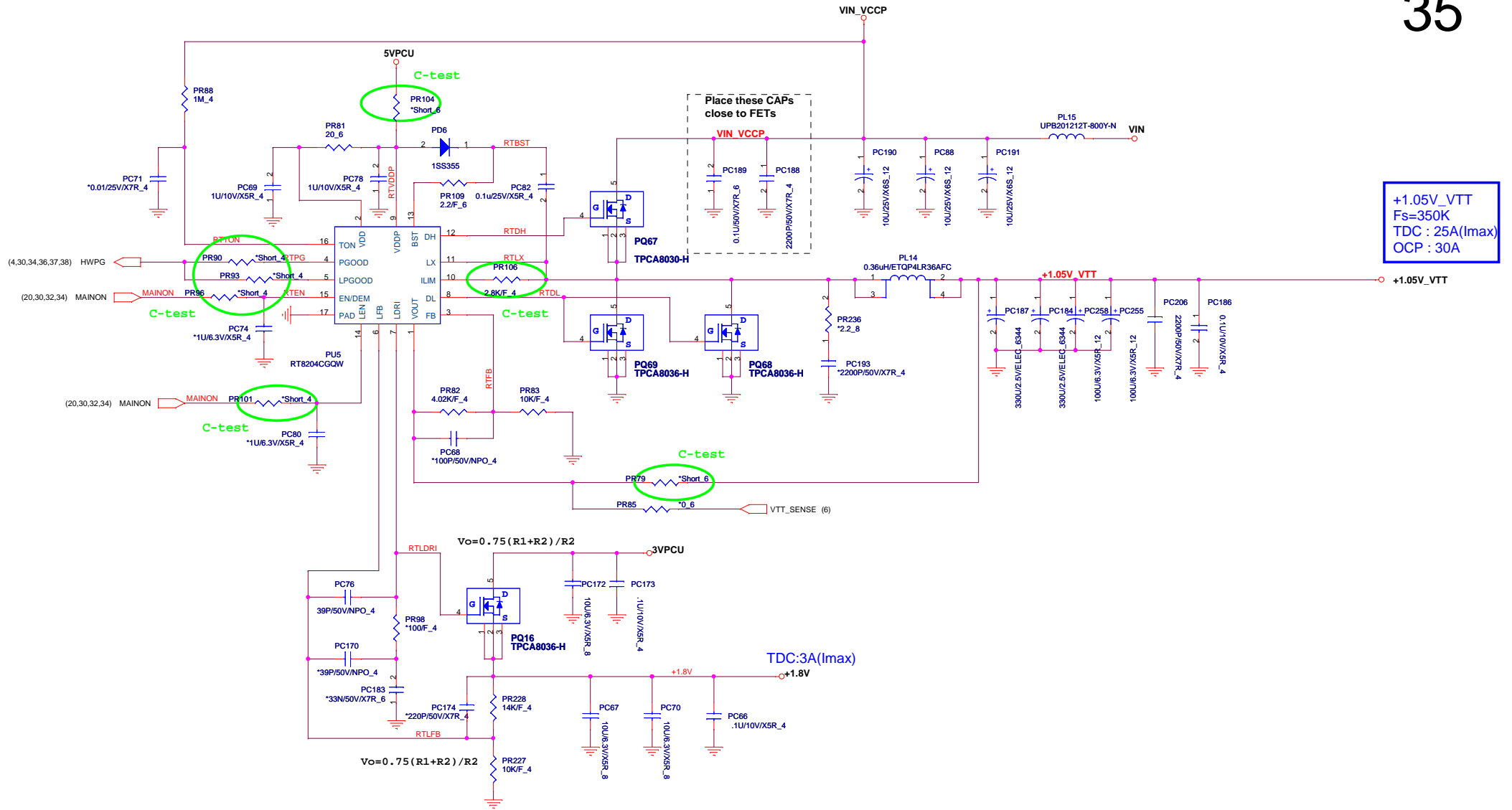
LANVCC

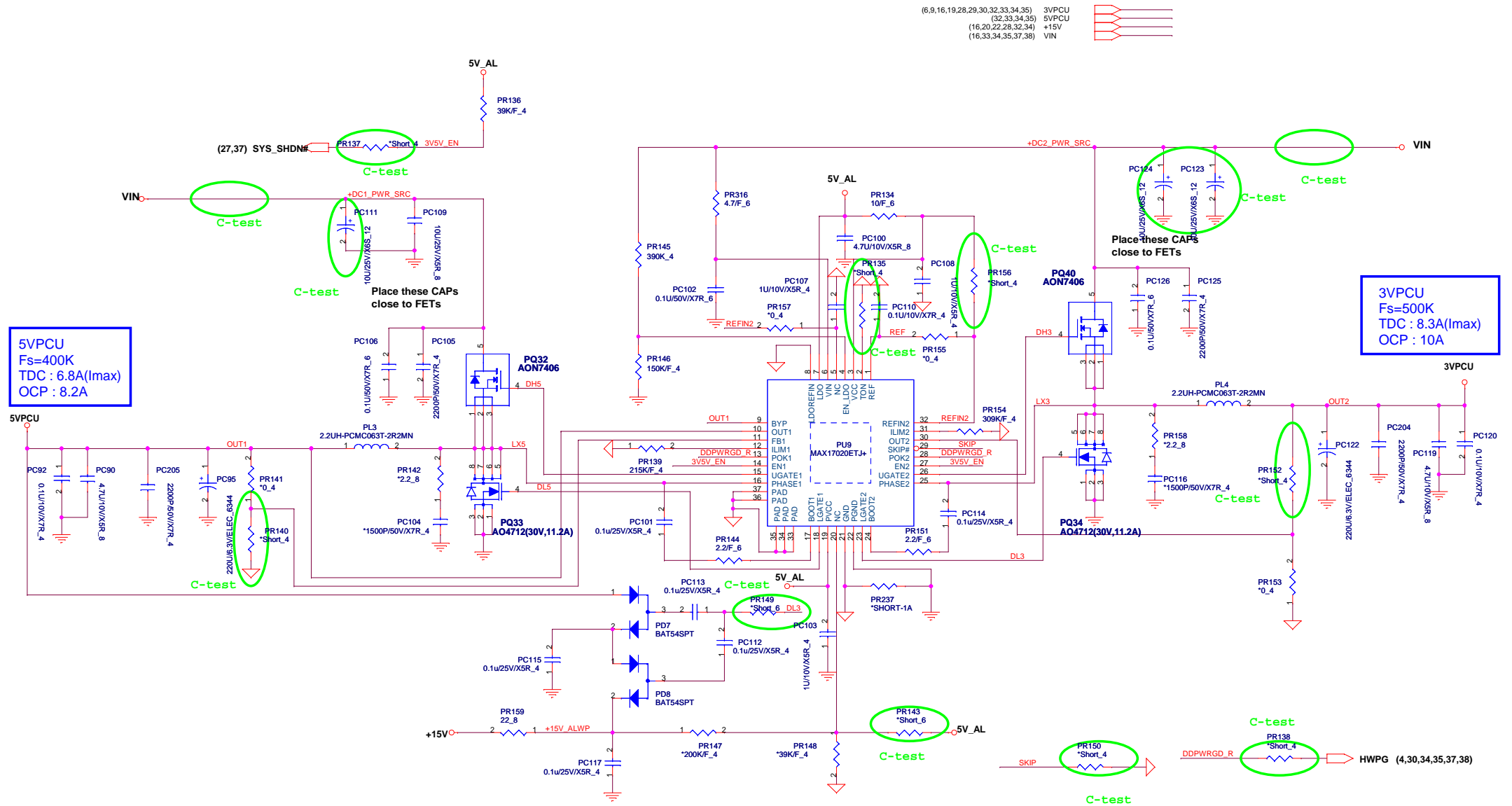


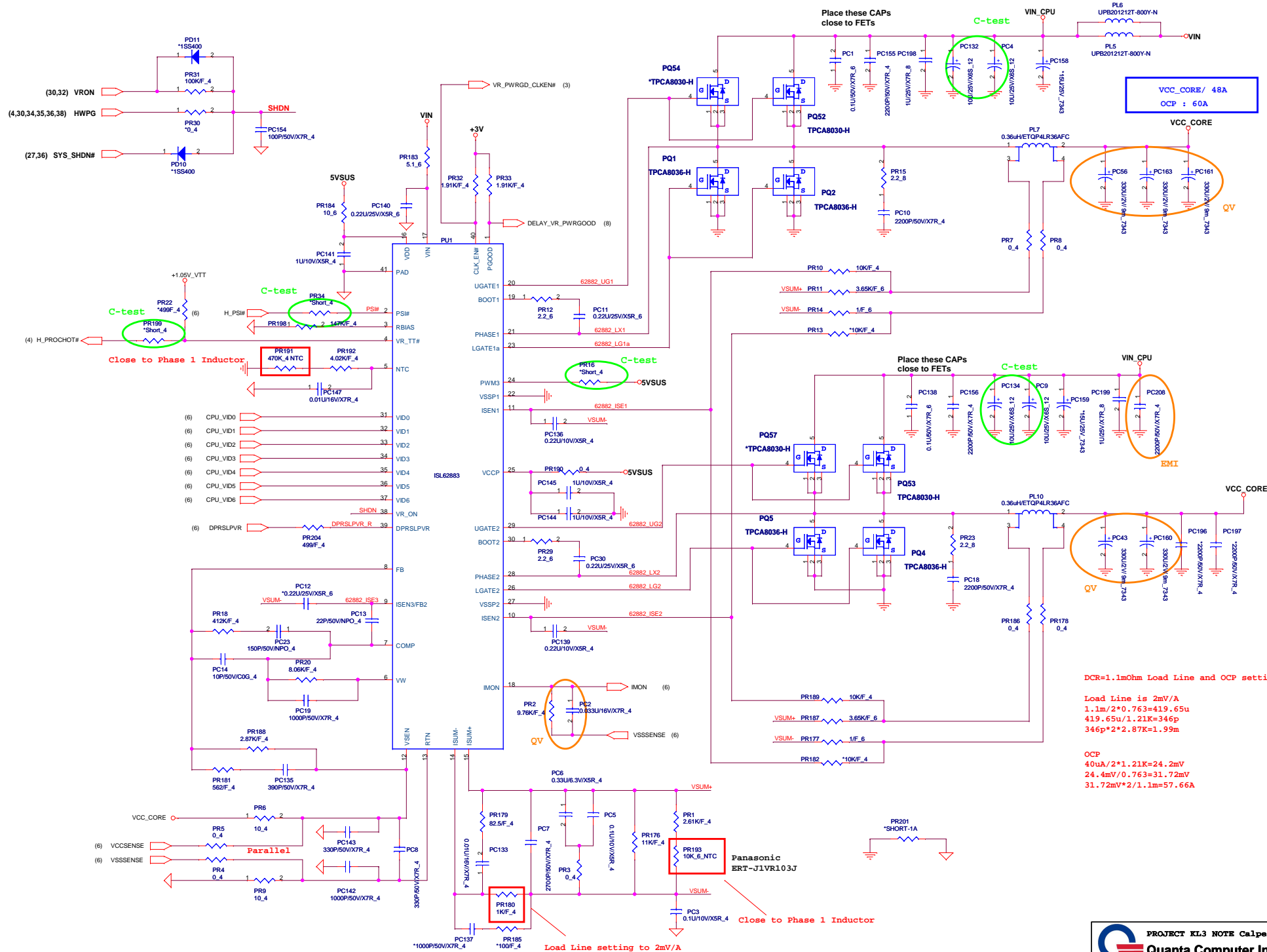
R138=0.02m ohm for 65W adapter-->current limit is 3A;

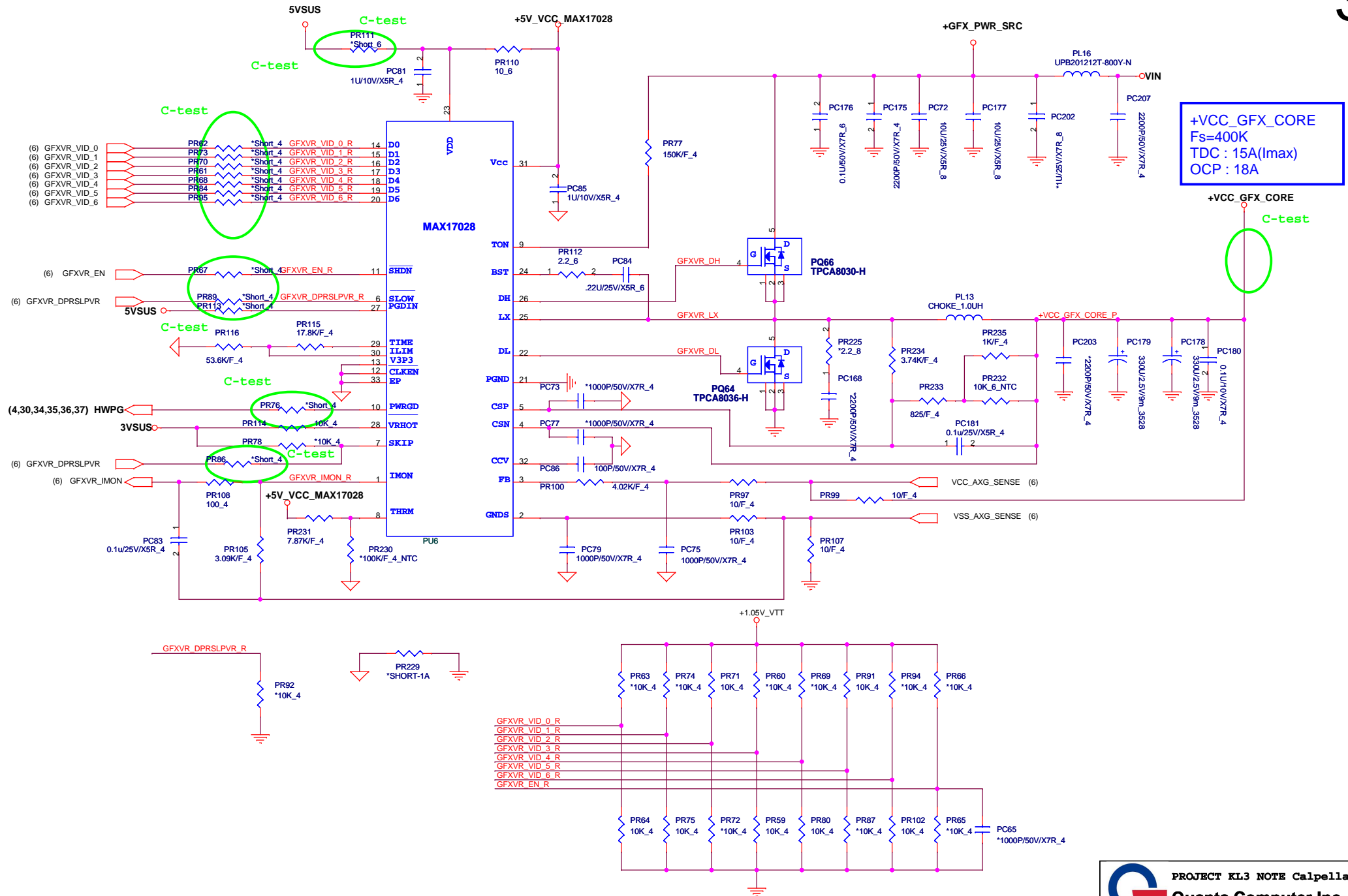












Revision History

Revision	Date	Phase	Change List	Release Schematic Date	Release Gerber File Date
1A		DV	Initial release		

Schematic Value Explanation Description :

RESISTOR

Value	F	4	6	8	12	1210	*	Description
*1K/F_4	1%	0402 (1005)					DE POP	1K ohm 1% SMD 0402 package and DE POP
1K_6	5%		0603 (1608)				POP	1K ohm 5% SMD 0603 package and POP
1K_8	5%			0805 (2125)			POP	1K ohm 5% SMD 0805 package and POP
1K_12	5%				1206 (3216)		POP	1K ohm 5% SMD 1206 package and POP
1K_1210	5%					1210 (3225)	POP	1K ohm 5% SMD 1210 package and POP

CAPACITOR

Value	Voltage	Material	6				*	Description
*0.1U/10V/X5R_4	10V	X5R	0402 (1005)				DE POP	0.1UF 10V X5R SMD 0402 package DE POP
1U/25V/X7R_6	25V	X7R	0603 (1608)				POP	0.1UF 25V X7R SMD 0603 package POP

[illegible]

G NOTE SKU TABLE

[illegible]

D

D

C


C

B

B

A

A

		PROJECT KL3 NOTE Calpella DIS	
		Quanta Computer Inc.	
Size Custom	Document Number POWER BLOCK		Rev 1A
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EC #	Page	Description	Part Affected
EC-A-01	12	0 ohm change to DEL for reduce 1.05V drop	R261
EC-A-02	35	Change footprint and schematic for design request	CN5
EC-A-03	35	DEL R126 and connect CN5.25 to GND directly	R126
EC-A-04	38	Add 10 ohm for reduce noise	R577
EC-A-05	39	DEL CN2 for combine with GC4/GC5	CN2
EC-A-06	10	25MHz X'tal ICG support removed from POR	Y6,R478,C671,C670
EC-A-07	12	Based on Intel DG V1.5 page320, remove external LC filter for VCCAClk, VccapIEXP, VCCFDIPLL, VCCSATAPLL.	L45,C692,L46,C697,L47,C712, C715,L21,C329,C331
EC-A-08	14	Based on Intel DG V1.5 page100 ,remove DDR3 Vref control circuit M2 option.	U1 etc...
EC-A-09	15	Based on Intel DG V1.5 page100 ,remove DDR3 Vref control circuit M2 option.	U46 etc...
EC-A-10	23	Change from 0 ohm to bead for EMI request	R150
EC-A-11	26	Change from 0 ohm to bead for EMI request	R237,R238,R239,R240
EC-A-12	43	Del +1.05V_PCH discharge	PR219,PQ11
EC-A-13	43	Add charger PTC	PR263
EC-A-14	43	Change Footprint	PQ66
EC-A-15	43	Modify OTP circuit	PD34
EC-A-16	44	Del NO ASM circuit	PU16 etc...
EC-A-17	46	Del +1.05V_PCH circuit	PQ133 etc...
EC-A-18	46	Reduce +1.05V power rail impedance	PJP13,PJP4
EC-A-19	46	Reserve for current derating	PL23
EC-A-20	46	Reduce transient regulation	PL20
EC-A-21	47	Reduce ripple voltage	PC216
EC-A-22	49	Add to separate enable from protect circuit	PR264
EC-A-23	49	Reserve for sequence	PR265
EC-A-24	29	ESD suggestion because ESATA don't CDE test so we DEL U7,U8 and add a GND shielding in board file	U7,U8