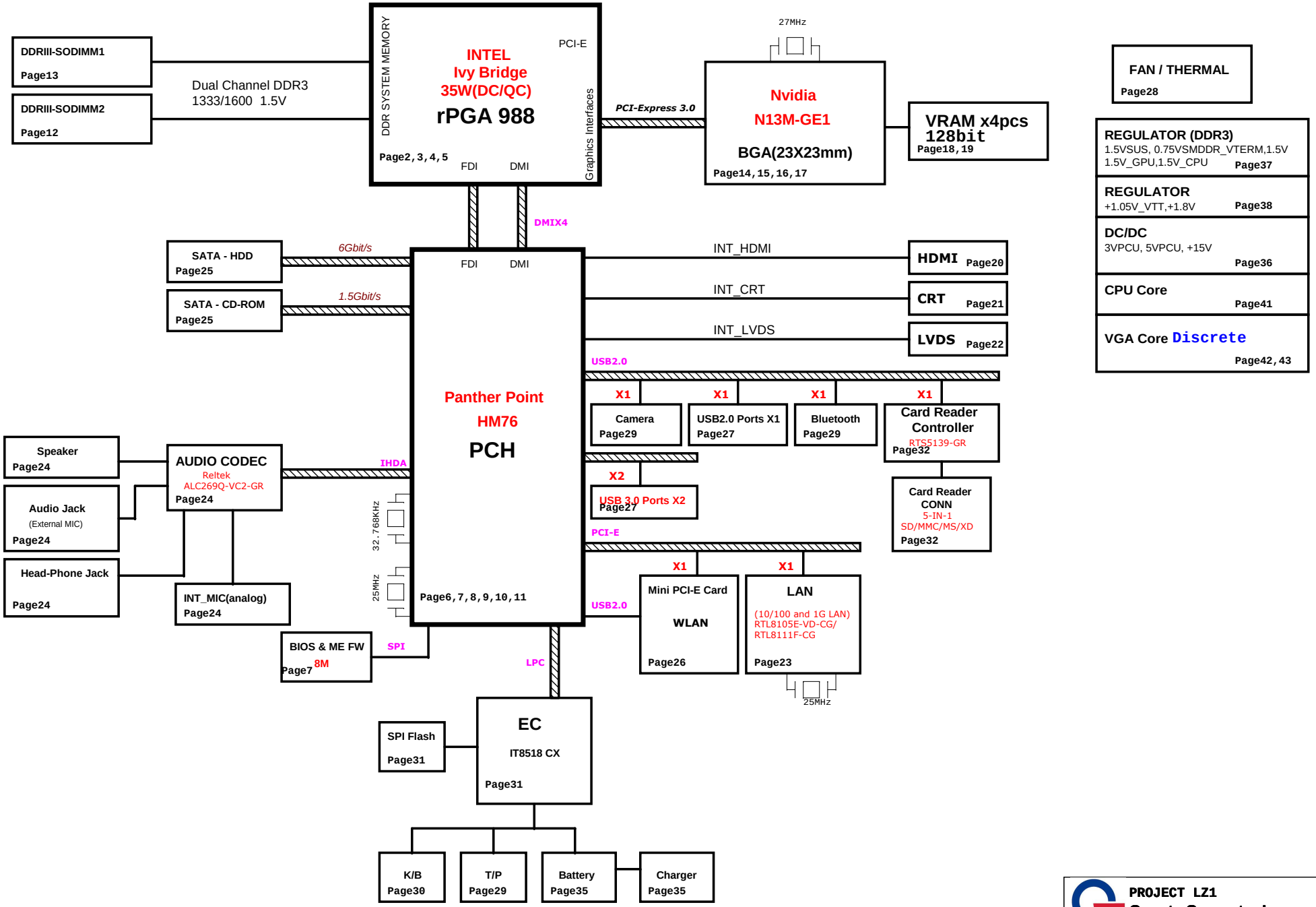
# LZ1/LZ1A(Z380) Intel Chief River Platform (Optimus) Block Diagram

01




PROJECT LZ1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | BLOCK DIAGRAM | 1B |

Date: Monday, January 09, 2012 Sheet 1 of 46

# Ivy Bridge Processor (DMI,PEG,FDI)

# Ivy Bridge Processor (CLK,MISC,JTAG)

02

[4,6,7,8,10,33,34,38,43] +1.05V_PCH
[4,10,12,13,33,34,37,43] +1.5V_SUS
[6,7,8,9,10,26,30,34] +3V_S5
[4] +1.5V_CPU

PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

U34A

DMI
[6] DMI_TXN0 B27 DMI_RX#[0]
[6] DMI_TXN1 B25 DMI_RX#[1]
[6] DMI_TXN2 A25 DMI_RX#[2]
[6] DMI_TXN3 B24 DMI_RX#[3]
[6] DMI_TXP0 B28 DMI_RX[0]
[6] DMI_TXP1 B26 DMI_RX[1]
[6] DMI_TXP2 A24 DMI_RX[2]
[6] DMI_TXP3 B23 DMI_RX[3]
[6] DMI_RXN0 G21 DMI_TX#[0]
[6] DMI_RXN1 E22 DMI_TX#[1]
[6] DMI_RXN2 F21 DMI_TX#[2]
[6] DMI_RXN3 D21 DMI_TX#[3]
[6] DMI_RXP0 G22 DMI_TX[0]
[6] DMI_RXP1 D22 DMI_TX[1]
[6] DMI_RXP2 F20 DMI_TX[2]
[6] DMI_RXP3 C21 DMI_TX[3]

Intel(R) FDI
[6] FDI_TXN0 A21 FDI0_TX#[0]
[6] FDI_TXN1 H19 FDI0_TX#[1]
[6] FDI_TXN2 E19 FDI0_TX#[2]
[6] FDI_TXN3 F18 FDI0_TX#[3]
[6] FDI_TXN4 B21 FDI1_TX#[0]
[6] FDI_TXN5 C20 FDI1_TX#[1]
[6] FDI_TXN6 D18 FDI1_TX#[2]
[6] FDI_TXN7 E17 FDI1_TX#[3]
[6] FDI_TXP0 A22 FDI0_TX[0]
[6] FDI_TXP1 G19 FDI0_TX[1]
[6] FDI_TXP2 E20 FDI0_TX[2]
[6] FDI_TXP3 G18 FDI0_TX[3]
[6] FDI_TXP4 B20 FDI1_TX[0]
[6] FDI_TXP5 C19 FDI1_TX[1]
[6] FDI_TXP6 D19 FDI1_TX[2]
[6] FDI_TXP7 F17 FDI1_TX[3]
[6] FDI_FSYNC0 J18 FDI0_FSYNC
[6] FDI_FSYNC1 J17 FDI1_FSYNC
[6] FDI_INT H20 FDI_INT
[6] FDI_LSYNC0 J19 FDI0_LSYNC
[6] FDI_LSYNC1 H17 FDI1_LSYNC

eDP
eDP_COMP A18 eDP_COMPIO
INT_eDP_HPD_Q A17 eDP_ICOMPO
B16 eDP_HPD
C15 eDP_AUX
D15 eDP_AUX#
C17 eDP_TX[0]
E16 eDP_TX[1]
C16 eDP_TX[2]
G15 eDP_TX[3]
C18 eDP_TX#[0]
E16 eDP_TX#[1]
D16 eDP_TX#[2]
E15 eDP_TX#[3]

eDP_COMP connect to PIN A18 W: 4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W: 12mils/S:15mils/L: 500mils.

PCI EXPRESS* - GRAPHICS
PEG_ICOMPI J22 PEG_COMP
PEG_ICOMPO J21
PEG_RCOMPO H22
PEG_RX#[0] K33 PEG_RXN0
PEG_RX#[1] M35 PEG_RXN1
PEG_RX#[2] L34 PEG_RXN2
PEG_RX#[3] J35 PEG_RXN3
PEG_RX#[4] J32 PEG_RXN4
PEG_RX#[5] H34 PEG_RXN5
PEG_RX#[6] H31 PEG_RXN6
PEG_RX#[7] G33 PEG_RXN7
PEG_RX#[8] G30 PEG_RXN8
PEG_RX#[9] E35 PEG_RXN9
PEG_RX#[10] E34 PEG_RXN10
PEG_RX#[11] E32 PEG_RXN11
PEG_RX#[12] D33 PEG_RXN12
PEG_RX#[13] D31 PEG_RXN13
PEG_RX#[14] B33 PEG_RXN14
PEG_RX#[15] C32 PEG_RXN15
PEG_RXN[0..15] [14]
PEG_RX[0] J33 PEG_RXP0
PEG_RX[1] L35 PEG_RXP1
PEG_RX[2] K34 PEG_RXP2
PEG_RX[3] H35 PEG_RXP3
PEG_RX[4] H32 PEG_RXP4
PEG_RX[5] G34 PEG_RXP5
PEG_RX[6] G31 PEG_RXP6
PEG_RX[7] F33 PEG_RXP7
PEG_RX[8] F30 PEG_RXP8
PEG_RX[9] E35 PEG_RXP9
PEG_RX[10] E33 PEG_RXP10
PEG_RX[11] F32 PEG_RXP11
PEG_RX[12] D34 PEG_RXP12
PEG_RX[13] E31 PEG_RXP13
PEG_RX[14] C33 PEG_RXP14
PEG_RX[15] B32 PEG_RXP15
PEG_RXP[0..15] [14]
PEG_TX#[0] M29 PEG_TXN0_C
PEG_TX#[1] M32 PEG_TXN1_C
PEG_TX#[2] M31 PEG_TXN2_C
PEG_TX#[3] L32 PEG_TXN3_C
PEG_TX#[4] L29 PEG_TXN4_C
PEG_TX#[5] K31 PEG_TXN5_C
PEG_TX#[6] K28 PEG_TXN6_C
PEG_TX#[7] J30 PEG_TXN7_C
PEG_TX#[8] J28 PEG_TXN8_C
PEG_TX#[9] H29 PEG_TXN9_C
PEG_TX#[10] G27 PEG_TXN10_C
PEG_TX#[11] E29 PEG_TXN11_C
PEG_TX#[12] F27 PEG_TXN12_C
PEG_TX#[13] D28 PEG_TXN13_C
PEG_TX#[14] F26 PEG_TXN14_C
PEG_TX#[15] E25 PEG_TXN15_C
PEG_TX[0] M28 PEG_TXP0_C
PEG_TX[1] M33 PEG_TXP1_C
PEG_TX[2] M30 PEG_TXP2_C
PEG_TX[3] L31 PEG_TXP3_C
PEG_TX[4] L28 PEG_TXP4_C
PEG_TX[5] K30 PEG_TXP5_C
PEG_TX[6] K27 PEG_TXP6_C
PEG_TX[7] J29 PEG_TXP7_C
PEG_TX[8] J27 PEG_TXP8_C
PEG_TX[9] H28 PEG_TXP9_C
PEG_TX[10] G28 PEG_TXP10_C
PEG_TX[11] E28 PEG_TXP11_C
PEG_TX[12] F28 PEG_TXP12_C
PEG_TX[13] D27 PEG_TXP13_C
PEG_TX[14] E26 PEG_TXP14_C
PEG_TX[15] D25 PEG_TXP15_C

Ivy Bridge_rPGA_2DPC_Rev0p61

U34B

MISC
[7] H_SNB_IVB# C26 PROC_SELECT#
TP53 SKTOCC# AN34 SKTOCC#

THERMAL
TP30 TP_CATERR# AL33 CATERR#
[31] EC_PECI AN33 PECI
[31,41] H_PROCHOT# R189 56_4 H_PROCHOT#_R AL32 PROCHOT#
[9] PM_THRMTRIP# AN32 THERMTRIP#

PWR MANAGEMENT
[6] PM_SYNC R415 *0_4_S PM_SYNC_R AM34 PM_SYNC
C442 *0.1U/10V_4
[9] H_PWRGOOD R417 *0_4_S H_PWRGOOD_R AP33 UNCOREPWRGOOD
R416 10K_4
PM_DRAM_PWRGD_R V8 SM_DRAMPWROK
+1.05V_PCH R418 *75_4
CPU_PLTRST# R401 *43_4 CPU_PLTRST#_R AR33 RESET#
R400 750/F_4
RV29 *EGA-0402
For ESD

Ivy Bridge_rPGA_2DPC_Rev0p61

CLOCKS
BCLK A28 CLK_CPU_BCLKP [8]
BCLK# A27 CLK_CPU_BCLKN [8]
DPLL_REF_CLK A16 DPLL_SSCLKP_R R535 *0_4 CLK_DPLL_SSCLKP [8]
DPLL_REF_CLK# A15 DPLL_SSCLKN_R R537 *0_4 CLK_DPLL_SSCLKN [8]
R536 1K/F_4
R538 1K/F_4 +1.05V_PCH

DDR3 MISC
SM_DRAMRST# R8 CPU_DRAMRST#
SM_RCOMP[0] AK1 SM_RCOMP_0 R549 140/F_4
SM_RCOMP[1] A5 SM_RCOMP_1 R278 25.5/F_4
SM_RCOMP[2] A4 SM_RCOMP_2 R277 200/F_4
SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

JTAG & BPM
PRDY# AP29 XDP_PRDY# TP33
PREQ# AP27 XDP_PREQ# TP36
TCK AR26 XDP_TCLK TP69
TMS AR27 XDP_TMS TP60
TRST# AP30 XDP_TRST# TP57
TDI AR28 XDP_TDI_R TP58
TDO AP26 XDP_TDO TP63
DBR# AL35 XDP_DBRST# XDP_DBRST# [6]
BPM#[0] AT28
BPM#[1] AP29
BPM#[2] AR30
BPM#[3] AT30
BPM#[4] AP32
BPM#[5] AR31
BPM#[6] AT31
BPM#[7] AR32

## DDR3 DRAM RESET

+1.5V_SUS
R290 1K/F_4
R271 *0_4
[12,13] DDR3_DRAMRST# R293 1K/F_4 CPU_DRAMRST#_R
EC-B-06
Q23 ME2N7002E
CPU_DRAMRST#
[8] DRAMRST_CNTRL_PCH R607 *0_4
[31] EC_DRAMRST_GATE R606 0_4
C260 0.047U/10V_4
R284 4.99K/F_4
FOR DEEP S3
EC-C-01
[12,13] DRAMRST_CNTRL_DDR

CPU_PLTRST#_R
+3V_S5
R399 1.5K/F_4
C406 *0.1U/10V_4
U33 *74LVC1G07GW
[8,14,23,26] PLTRST#
CPU_PLTRST#

## SM_DRAMPWROK Processor Input.

+3V_S5 +1.5V_CPU
C262 *0.1U/10V_4
R287 200/F_4
[6] SYS_PWROK
[6] PM_DRAM_PWRGD
R273 *0_4
U21 *74AHC1G09GW
PM_DRAM_PWRGD_Q R281 130/F_4 PM_DRAM_PWRGD_R
R282 *0_4_S
R288 39_4
Q25 ME2N7002E
PM_DRAM_PWRGD_Q R272 *3K/F_4
MAINON# [4,34]

## PEG x16 (UMA Non-stuff)

PEG_TXP[0..15] [14]

| | | | |
|---|---|---|---|
| PEG_TXP0_C | | | PEG_TXP0 |
| PEG_TXP1_C | C439 | DIS@0.1U/10V_4 | PEG_TXP1 |
| PEG_TXP2_C | C437 | DIS@0.1U/10V_4 | PEG_TXP2 |
| PEG_TXP3_C | C435 | DIS@0.1U/10V_4 | PEG_TXP3 |
| PEG_TXP4_C | C434 | DIS@0.1U/10V_4 | PEG_TXP4 |
| PEG_TXP5_C | C432 | DIS@0.1U/10V_4 | PEG_TXP5 |
| PEG_TXP6_C | C429 | DIS@0.1U/10V_4 | PEG_TXP6 |
| PEG_TXP7_C | C427 | DIS@0.1U/10V_4 | PEG_TXP7 |
| PEG_TXP8_C | C416 | DIS@0.1U/10V_4 | PEG_TXP8 |
| PEG_TXP9_C | C425 | DIS@0.1U/10V_4 | PEG_TXP9 |
| PEG_TXP10_C | C415 | DIS@0.1U/10V_4 | PEG_TXP10 |
| PEG_TXP11_C | C423 | DIS@0.1U/10V_4 | PEG_TXP11 |
| PEG_TXP12_C | C412 | DIS@0.1U/10V_4 | PEG_TXP12 |
| PEG_TXP13_C | C422 | DIS@0.1U/10V_4 | PEG_TXP13 |
| PEG_TXP14_C | C410 | DIS@0.1U/10V_4 | PEG_TXP14 |
| PEG_TXP15_C | C408 | DIS@0.1U/10V_4 | PEG_TXP15 |
| | C419 | DIS@0.1U/10V_4 | |

0.1uF AC Coupling Caps for PCIE GEN2

PEG_TXN[0..15] [14]

| | | | |
|---|---|---|---|
| PEG_TXN0_C | | | PEG_TXN0 |
| PEG_TXN1_C | C440 | DIS@0.1U/10V_4 | PEG_TXN1 |
| PEG_TXN2_C | C438 | DIS@0.1U/10V_4 | PEG_TXN2 |
| PEG_TXN3_C | C436 | DIS@0.1U/10V_4 | PEG_TXN3 |
| PEG_TXN4_C | C433 | DIS@0.1U/10V_4 | PEG_TXN4 |
| PEG_TXN5_C | C431 | DIS@0.1U/10V_4 | PEG_TXN5 |
| PEG_TXN6_C | C430 | DIS@0.1U/10V_4 | PEG_TXN6 |
| PEG_TXN7_C | C428 | DIS@0.1U/10V_4 | PEG_TXN7 |
| PEG_TXN8_C | C417 | DIS@0.1U/10V_4 | PEG_TXN8 |
| PEG_TXN9_C | C426 | DIS@0.1U/10V_4 | PEG_TXN9 |
| PEG_TXN10_C | C414 | DIS@0.1U/10V_4 | PEG_TXN10 |
| PEG_TXN11_C | C424 | DIS@0.1U/10V_4 | PEG_TXN11 |
| PEG_TXN12_C | C413 | DIS@0.1U/10V_4 | PEG_TXN12 |
| PEG_TXN13_C | C421 | DIS@0.1U/10V_4 | PEG_TXN13 |
| PEG_TXN14_C | C411 | DIS@0.1U/10V_4 | PEG_TXN14 |
| PEG_TXN15_C | C409 | DIS@0.1U/10V_4 | PEG_TXN15 |
| | C420 | DIS@0.1U/10V_4 | |

0.1uF AC Coupling Caps for PCIE GEN2

## DP & PEG Compensation

+1.05V_PCH R531 24.9/F_4 PEG_COMP

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils
typical impedance = 14.5 mohms

+1.05V_PCH R533 *10K_4 INT_eDP_HPD_Q
+1.05V_PCH R532 24.9/F_4 eDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

## Processor pull-up(CPU)

+1.05V_PCH

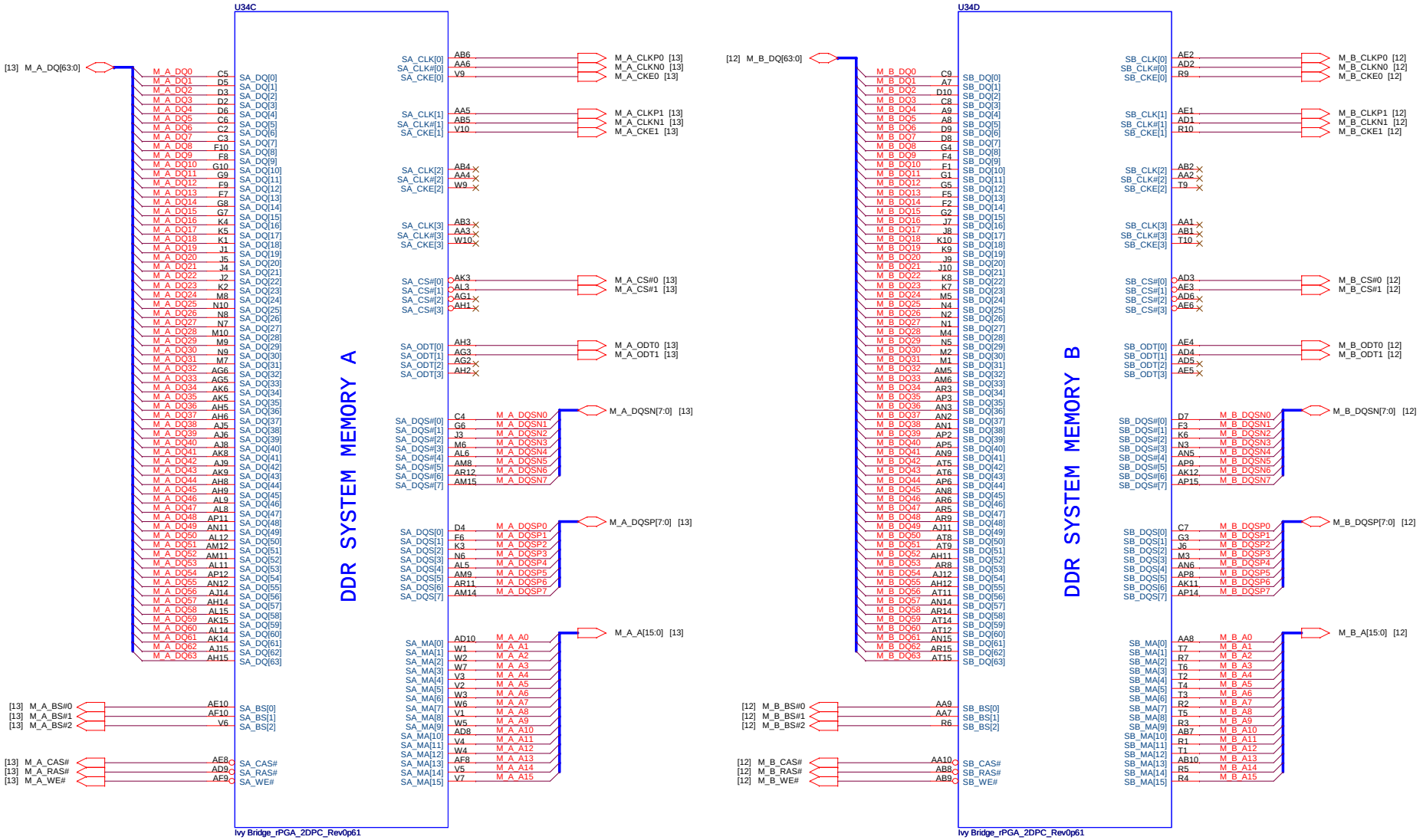
| | | |
|---|---|---|
| H_PROCHOT# | R190 | 62/F_4 |
| XDP_TDO | R468 | 51_4 |
| XDP_TMS | R459 | 51_4 |
| XDP_TDI_R | R449 | 51_4 |
| XDP_PREQ# | R192 | *51_4 |
| XDP_TCLK | R474 | 51_4 |
| XDP_TRST# | R429 | 51_4 |

PROJECT LZ1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | IVY Bridge 1/4 | 1B |

Date: Monday, January 09, 2012 Sheet 2 of 46

# Ivy Bridge Processor (DDR3)




PROJECT LZ1

Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | IVY Bridge 2/4 | 1B |

Date: Monday, January 09, 2012 Sheet 3 of 46

[33,41] +VCC_CORE
[2,6,7,8,10,33,34,38,43] +1.05V_PCH
[34] MAINON_15V
[2,10,12,13,33,34,37,43] +1.5V_SUS
[2] +1.5V_CPU
[10,26] +1.5V
[7,10,34,40] +1.8V
[34,39] +0.85V
[33,41] +VCC_GFX

# Ivy Bridge Processor (GRAPHIC POWER)

## POWER

U34F

### CORE SUPPLY

+VCC_CORE
SNB: 55A
IVY: 55A

C191 22U/6.3V_8, C190 22U/6.3V_8, C189 22U/6.3V_8, C193 22U/6.3V_8
C170 22U/6.3V_8, C192 22U/6.3V_8, C139 22U/6.3V_8, C142 22U/6.3V_8
C151 22U/6.3V_8, C171 22U/6.3V_8, C143 22U/6.3V_8, C172 22U/6.3V_8
C194 22U/6.3V_8, C201 22U/6.3V_8, C161 22U/6.3V_8, C195 22U/6.3V_8
C482 10U/6.3V_8, C481 10U/6.3V_8, C480 10U/6.3V_8, C505 10U/6.3V_8
C479 10U/6.3V_8, C494 10U/6.3V_8, C495 10U/6.3V_8, C496 10U/6.3V_8
C478 10U/6.3V_8, C504 10U/6.3V_8

+VCC_CORE:
22uF_8 x8 TOP Socket cavity
22uF_8 x8 TOP Socket edge
10uF_8 x10 BOT Socket cavity

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

Ivy Bridge_rPGA_2DPC_Rev0p61

### PEG AND DDR

+1.05V_PCH
SNB: 8.5A
IVY: 8.5A

C221 22U/6.3V_8, C215 22U/6.3V_8, C216 22U/6.3V_8, C217 22U/6.3V_8, C218 22U/6.3V_8, C219 22U/6.3V_8
C220 22U/6.3V_8, C512 22U/6.3V_8, C511 22U/6.3V_8, C510 22U/6.3V_8, C509 22U/6.3V_8, C508 22U/6.3V_8

22uF_8 x7 TOP Socket cavity
22uF_8 x5 BOT Socket cavity

C224 *22U/6.3V_8, C229 *22U/6.3V_8, C222 *22U/6.3V_8, C513 *22U/6.3V_8
C227 *22U/6.3V_8, C228 *22U/6.3V_8, C514 *22U/6.3V_8

22uF (Reserved)

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

J23 +1.05V_PCH 40 R525 *0_4_S +1.05V_PCH

### SVID

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

### SENSE LINES

VCC_SENSE AJ35 R420 100_4 +VCC_CORE
VSS_SENSE AJ34 R419 100_4
VCC_SENSE [41]
VSS_SENSE [41]

VCCIO_SENSE B10 VTT_SENSE
VSS_SENSE_VCCIO A10 VSSP_SENSE
VTT_SENSE [38]
VSSP_SENSE [38]

Trace Route to Power IC area.

+1.05V_PCH
VTT_SENSE R276 10/F_4
VSSP_SENSE R275 10/F_4

## POWER

U34G

### GRAPHICS

+VCC_GFX
SNB: 21.5A
IVY: 33A

C491 22U/6.3V_8, C468 22U/6.3V_8, C469 22U/6.3V_8, C502 22U/6.3V_8
C213 22U/6.3V_8, C212 22U/6.3V_8, C211 22U/6.3V_8, C214 22U/6.3V_8
C507 22U/6.3V_8, C506 22U/6.3V_8, C207 22U/6.3V_8, C208 22U/6.3V_8

+VCC_GFX:
22uF_8 x2 TOP Socket cavity
22uF_8 x4 TOP Socket edge
22uF_8 x2 BOT Socket cavity
22uF_8 x4 BOT Socket edge

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

### 1.8V RAIL

+1.8V
SNB:1.5A
IVY:1.5A

C524 10U/6.3V_6, C522 1U/6.3V_4, C523 1U/6.3V_4, C527 *330U/2.5V_7343

330uF/7mohm x 1
10uF x 1
1uF x 2

VCCPLL1 VCCPLL2 VCCPLL3

Ivy Bridge_rPGA_2DPC_Rev0p61

### SENSE LINES

VAXG_SENSE AK35 R414 100/F_4 +VCC_GFX
VSSAXG_SENSE AK34 R406 100/F_4
TP50 TP51
VCC_AXG_SENSE [41]
VSS_AXG_SENSE [41]

### VREF

SM_VREF AL1 +VDDR_REF_CPU
CAD Note: +VDDR_REF_CPU should have 10 mil trace width

SA_DIMM_VREFDQ B4 SMDDR_VREF_DQ0_M3
SB_DIMM_VREFDQ D1 SMDDR_VREF_DQ1_M3
R280 *1K_4
R279 *1K_4
SMDDR_VREF_DQ0_M3 [13]
SMDDR_VREF_DQ1_M3 [12]

### DDR3 -1.5V RAILS

SNB: 5A
IVY: 5A

VDDQ1 AF7 VDDQ2 AF4 VDDQ3 AF1 VDDQ4 AC7 VDDQ5 AC4 VDDQ6 AC1 VDDQ7 Y7 VDDQ8 Y4 VDDQ9 Y1 VDDQ10 U7 VDDQ11 U4 VDDQ12 U1 VDDQ13 P7 VDDQ14 P4 VDDQ15 P1

+1.5V_CPU

C254 10U/6.3V_6, C259 10U/6.3V_6, C253 10U/6.3V_6, C255 10U/6.3V_6

330uF x1, 10uF_8 x6 Socket BOT edge.

C252 10U/6.3V_6, C258 10U/6.3V_6, C256 220U/2.5V/ESR15_7343

### SA RAIL

SNB: 6A
IVY: 6A

VCCSA1 M27 VCCSA2 M26 VCCSA3 L26 VCCSA4 J26 VCCSA5 J25 VCCSA6 J24 VCCSA7 H26 VCCSA8 H25

+0.85V

C202 10U/6.3V_6, C203 10U/6.3V_6, C475 10U/6.3V_6

330uF x1, 10uF_8 x1 Socket BOT edge,
10uF_8 x2 Socket BOT cavity.

### MISC

VCCSA_SENSE H23 R225 *0_4_S
VCCUSA_SENSE [39]
VCCSA_SEL0 [39]

VCCSA_VID[0] C22 VCCSA_SEL0 R210 1K_4
VCCSA_VID[1] C24 VCCSA_SEL R200 1K_4
VCCSA_SEL [39]

VCCIO_SEL A19 R526 *0_4
H_VTTVID1 [38]

Layout note:
need routing together and ALERT need between CLK and DATA

### SVID CLK

+1.05V_PCH
C598 0.1U/10V_4
Close to VR
R457 54.9/F_4
H_CPU_SVIDCLK R216 *0_4_S VR_SVID_CLK [41]

### SVID DATA

+1.05V_PCH
C599 0.1U/10V_4
Close to CPU
R206 130/F_4

+1.05V_PCH
C601 0.1U/10V_4
R483 130/F_4
Close to VR

H_CPU_SVIDDAT R203 *0_4_S VR_SVID_DATA [41]

### SVID ALERT

+1.05V_PCH
C597 0.1U/10V_4
Close to CPU
R214 75_4
H_CPU_SVIDALRT# R221 43_4 VR_SVID_ALERT_L# R207 *0_4_S VR_SVID_ALERT# [41]

+1.5V_CPU +1.5V
R295 *0_8_S
40mile routing

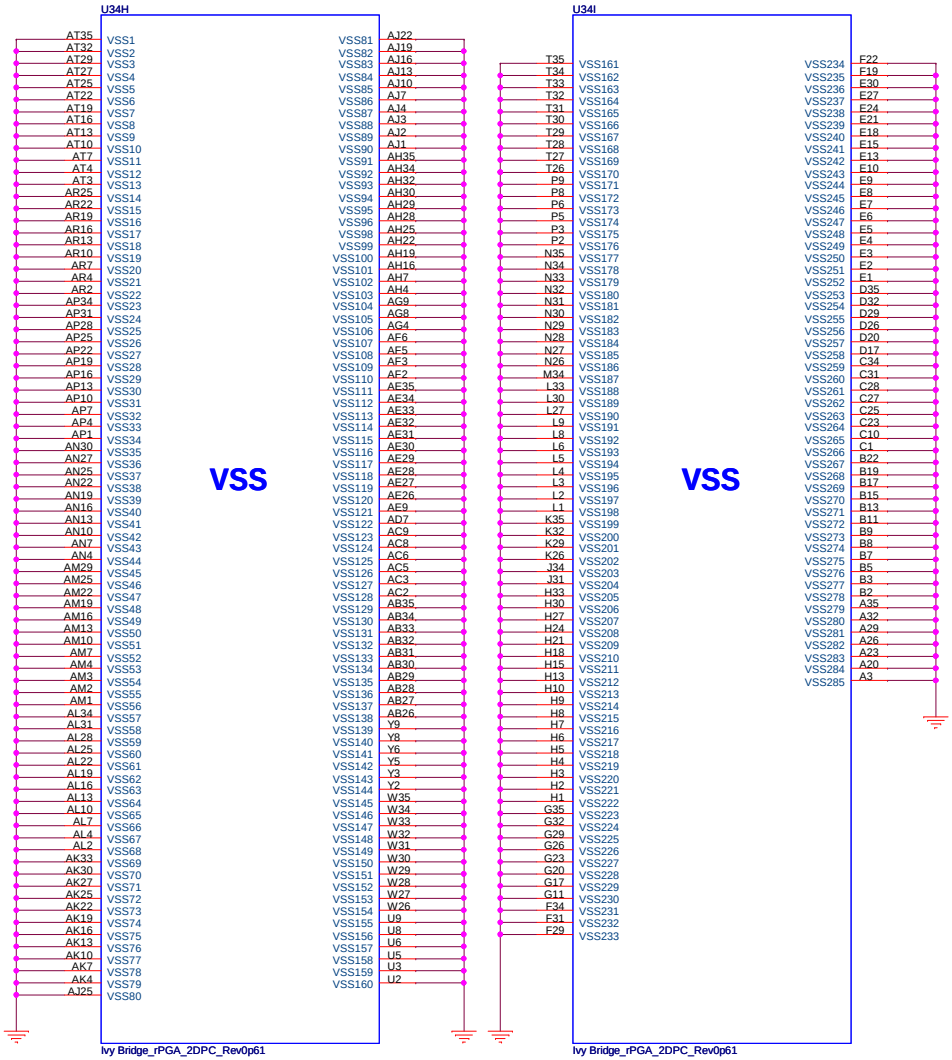
+1.5V_SUS 5A +1.5V_CPU +1.5V_SUS
Q26 AON7406
C267 0.1U/10V_4
C268 0.1U/10V_4
C263 0.1U/10V_4
C264 0.1U/10V_4
Placement close to CPU.
[34] MAINON_15V
C261 *470P/50V_4
R292 220_8
[2,34] MAINON#
Q28 2N7002K

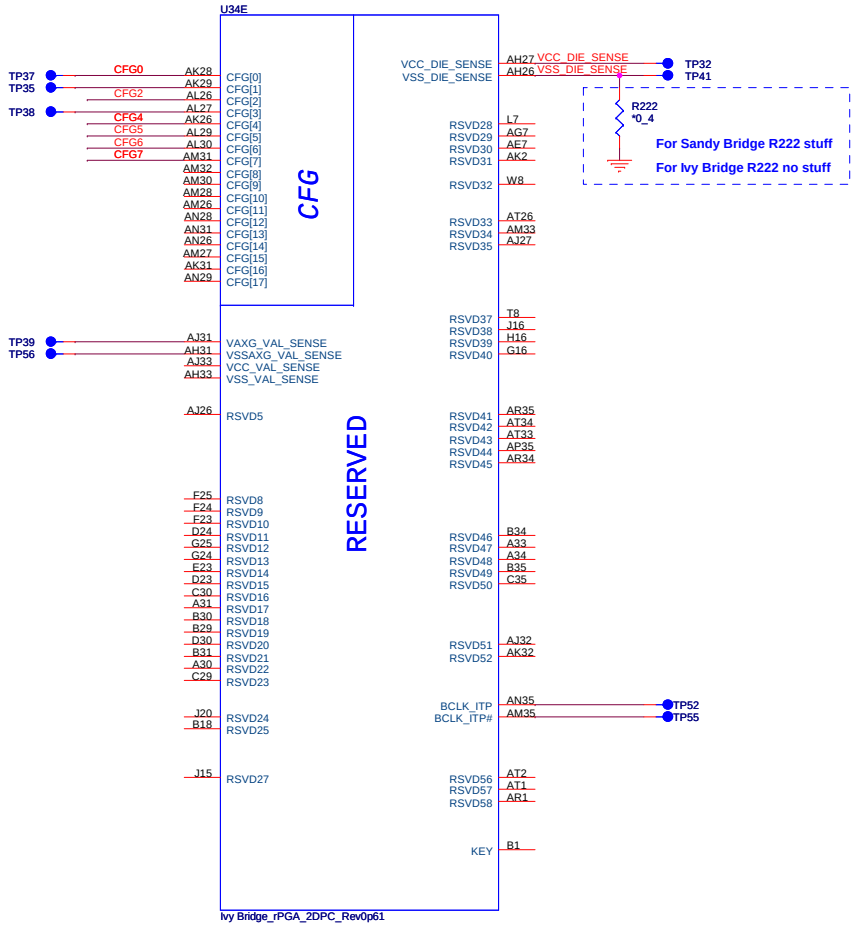
[12,13,37] SMDDR_VREF R553 *0_8 +VDDR_REF_CPU
Q48 ME2N7002E
MAINON_15V
R552 100K_4

PROJECT LZ1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | IVY Bridge 3/4 | 1B |

Date: Monday, January 09, 2012 Sheet 4 of 46

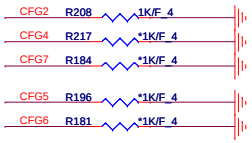



## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

| | 1 | 0 |
|---|---|---|
| CFG2<br>(PEG Static Lane Reversal) | Normal Operation | Lane Reversed |
| CFG4<br>(DP Presence Strap) | Disable; No physical DP attached to eDP | Enable; An ext DP device is connected to eDP |
| CFG7<br>(PEG Defer Training) | PEG train immediately following xxRESETB de assertion | PEG wait for BIOS training |




**CFG[6:5] (PCIE Port Bifurcation Straps)**

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

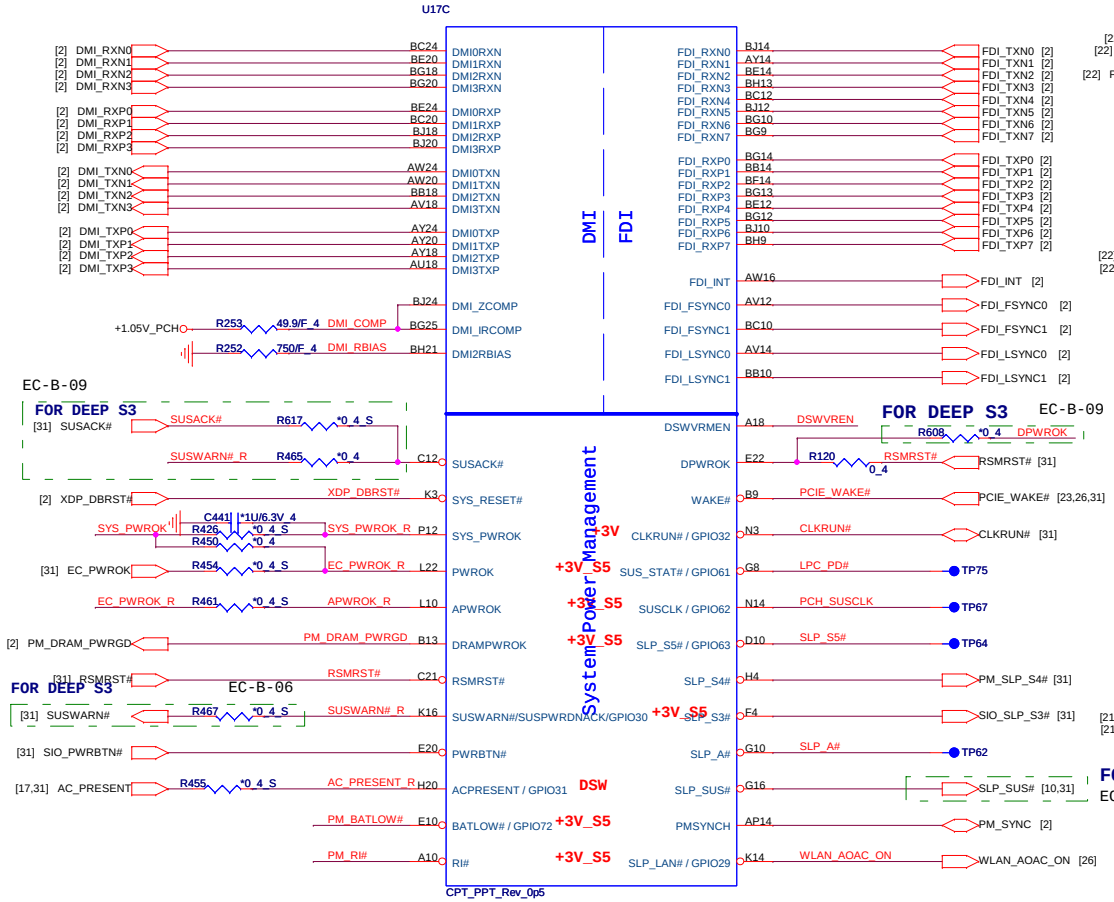
PROJECT LZ1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | IVY Bridge 4/4 | 1B |

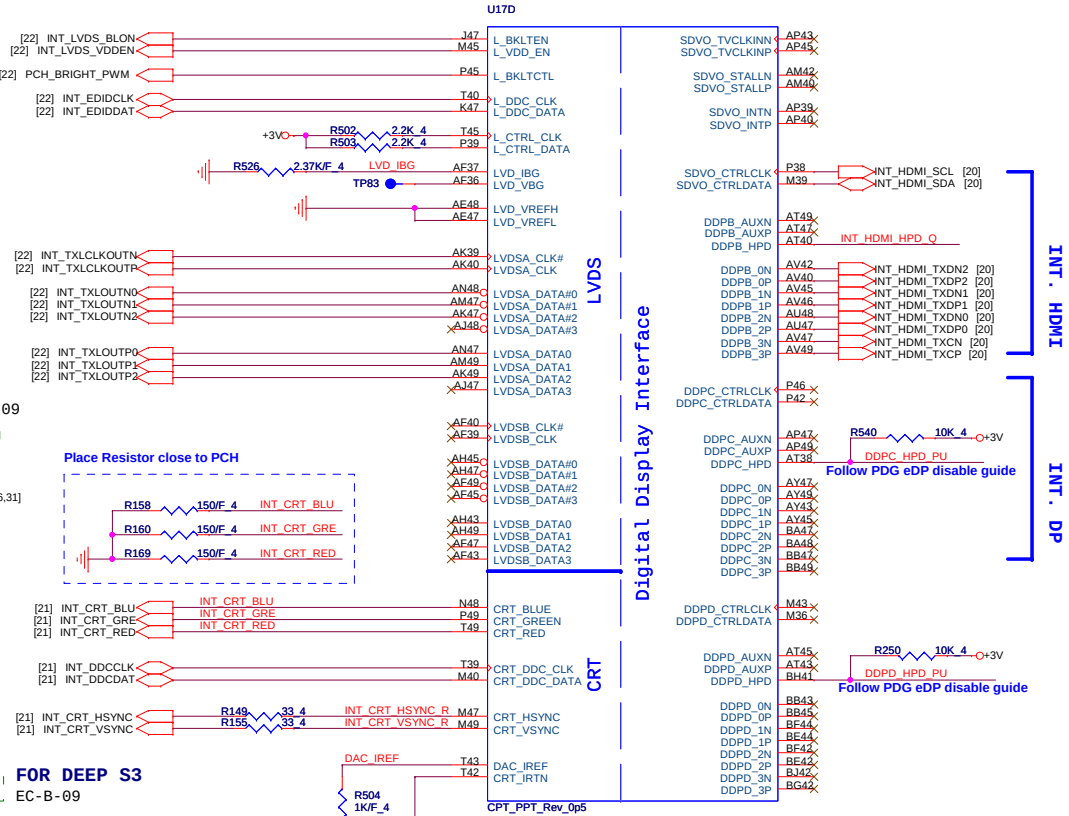
Date: Monday, January 09, 2012 Sheet 5 of 46

[2,4,7,8,10,33,34,38,43] +1.05V_PCH
[7,8,9,10,12,13,14,20,21,22,23,24,25,26,28,29,30,31,32,33,34,37,38,41,42,43] +3V
[2,7,8,9,10,26,30,34] +3V_S5
[7,10,31] +3V_RTC
[7,22,23,25,26,30,31,34,35,36,40] +3VPCU
[10] +3V_DSW

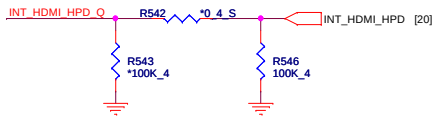
# Cougar Point/Panther Point (DMI,FDI,PM)




# Cougar Point/Panther Point (LVDS,DDI)

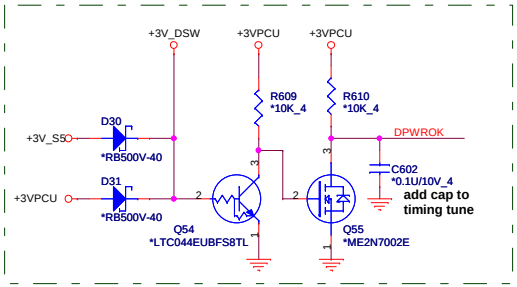



## INT HDMI Detect Function

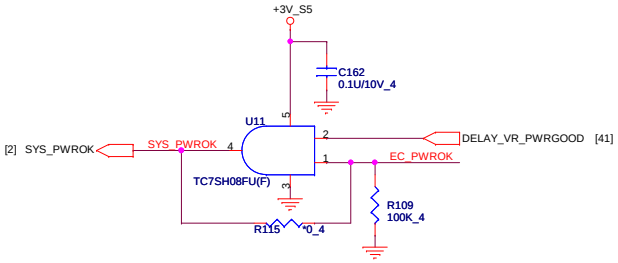


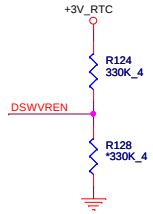

## DPWROK FOR DSW

FOR DEEP S3 EC-B-09



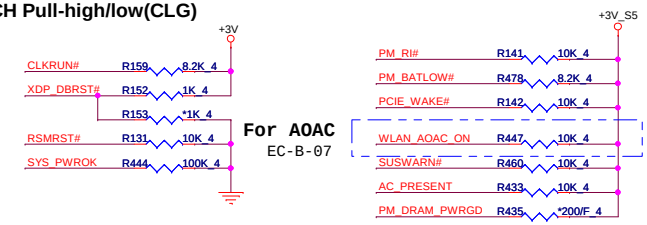

## System PWR_OK(CLG)




| On Die DSW VR Enable |
|---|
| High = Enable (Default) |
| Low = Disable |

## PCH Pull-high/low(CLG)

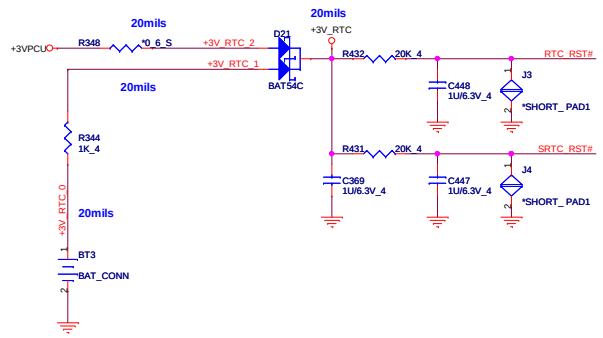



PROJECT LZ1
Quanta Computer Inc.

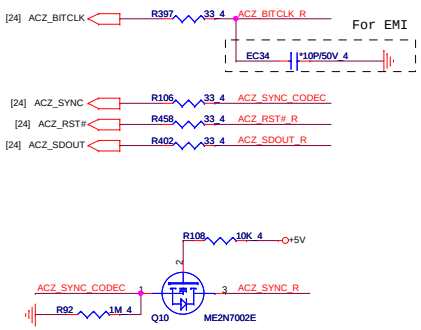
| Size | Document Number | Rev |
|---|---|---|
| Custom | Cougar Point 1/6 | 1B |

Date: Monday, January 09, 2012 Sheet 6 of 46

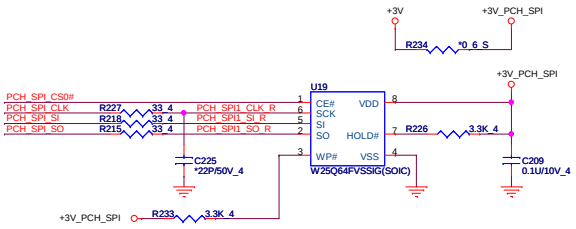
## RTC Circuitry(RTC)




## HDA Bus(CLG)

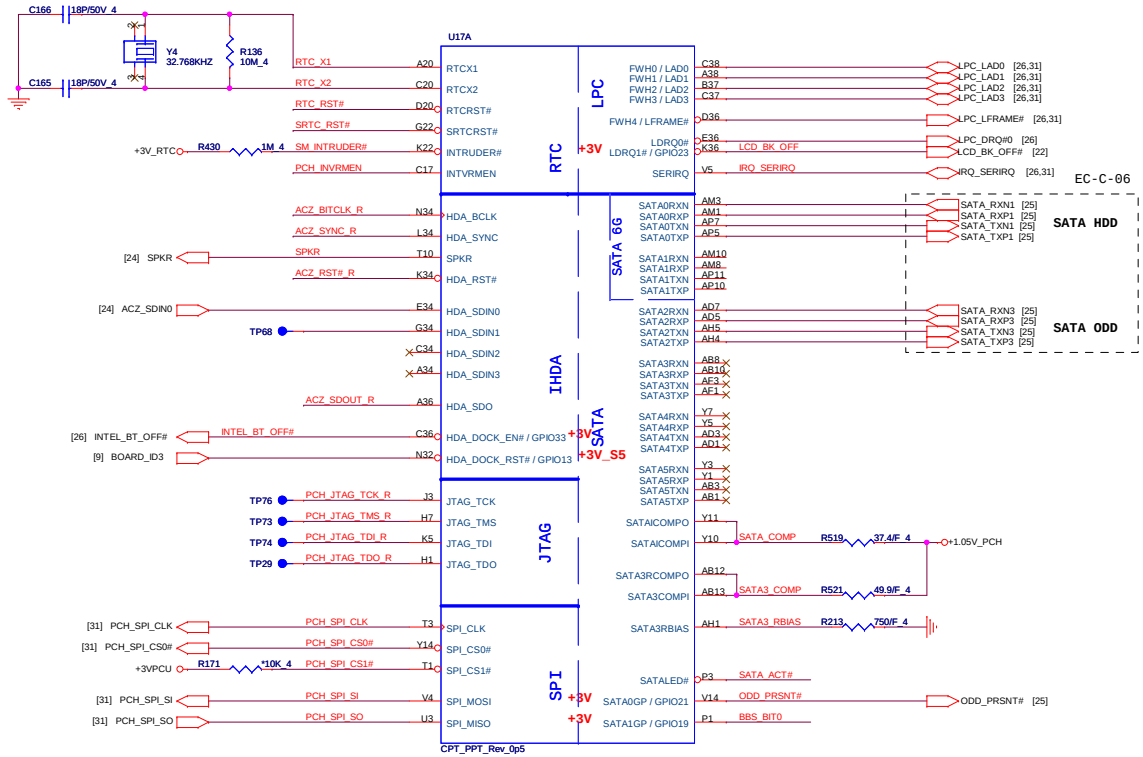


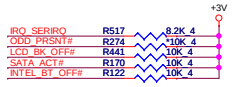

## PCH Dual SPI (CLG)




## 32Mbit (8M Byte), SPI

## PCH2(CLG)




## PCH Strap Table

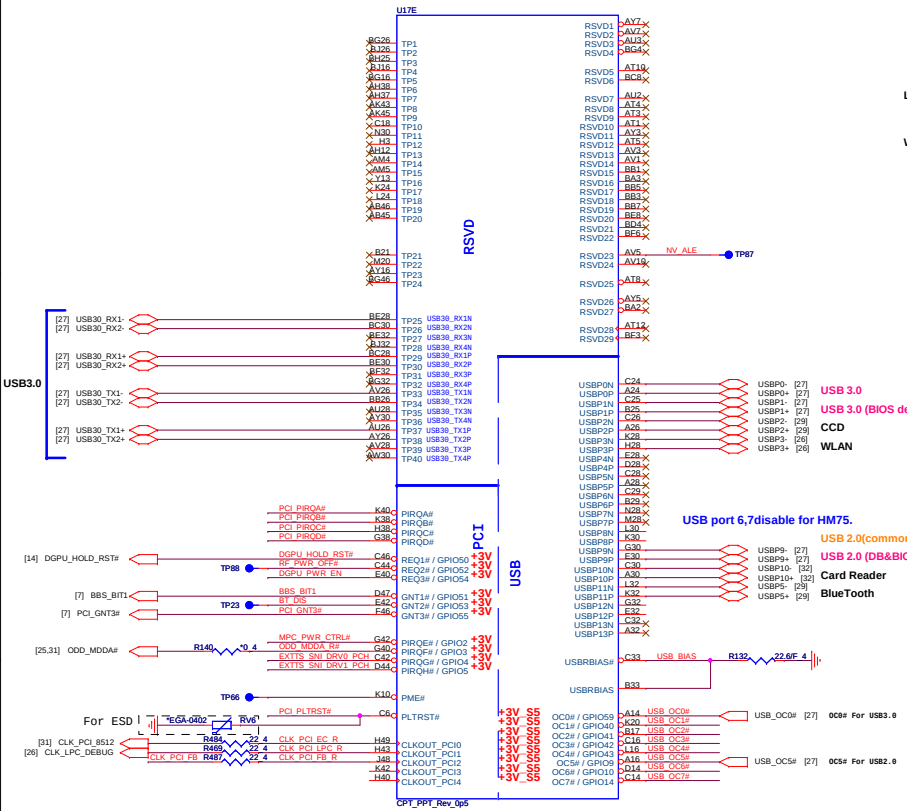
| Pin Name | Strap description | Sampled | Configuration | |
|---|---|---|---|---|
| SPKR | No reboot mode setting | PWROK | 0 = Default (weak pull-down 20K)<br>1 = Setting to No-Reboot mode | +3V R515 *1K_4 SPKR |
| GNT3# / GPIO55 | Top-Block Swap Override | PWROK | 0 = "top-block swap" mode<br>1 = Default (weak pull-up 20K) | R486 *1K_4 PCI_GNT3# [8] |
| INTVRMEN | Integrated 1.05V VRM enable | ALWAYS | Should be always pull-up | +3V_RTC R129 330K_4 PCH_INVRMEN |
| GNT1# / GPIO51 | Boot BIOS Selection 1 [bit-1] | PWROK | GNT1# / GNT0# / Boot Location<br>1 / 1 / SPI *<br>0 / 0 / LPC | Default weak pull-up on GNT0/1#<br>[Need external pull-down for LPC BIOS] |
| GPIO19 | Boot BIOS Selection 0 [bit-0] | PWROK | | R479 *1K_4 BBS_BIT1 [8]<br>R167 *1K_4 BBS_BIT0 |
| HDA_SDO | Flash Descriptor Security | RSMRST | 0 = Override<br>1 = Default (weak pull-up 20K) | +3V_S5 R413 *1K_4 ACZ_SDOUT_R |
| DF_TVS | DMI/FDI Termination voltage | PWROK | 0 = Set to Vss<br>1 = Set to Vcc (weak pull-down 20K) | R251 2.2K_4 +1.8V<br>R258 1K_4 DF_TVS [9]<br>H_SNB_IVB# [2] |
| GPIO28 | On-die PLL Voltage Regulator | RSMRST# | 0 = Disable<br>1 = Enable (Default) | R496 *1K_4 PLL_ODVR_EN [9] |
| HDA_SYNC | On-Die PLL VR Voltage Select | RSMRST | 0 = Support by 1.8V (weak pull-down)<br>1 = Support by 1.5V | +3V_S5 R90 1K_4 ACZ_SYNC_R |
| GPIO8 | Integrated Clock Chip Enable | RSMRST# | Should be pull-down<br>(weak pull-up 20K) | |
| SPI_MOSI | iTPM function Disable | APWROK | 0 = Default (weak pull-down 20K)<br>1 = Enable | +3V R209 *1K_4 PCH_SPI_SI |
| NV_ALE | Intel Anti-Theft HDD protection | PWROK | 0 = Disable (Internal pull-down 20kohm) | |

PROJECT LZ1
Quanta Computer Inc.

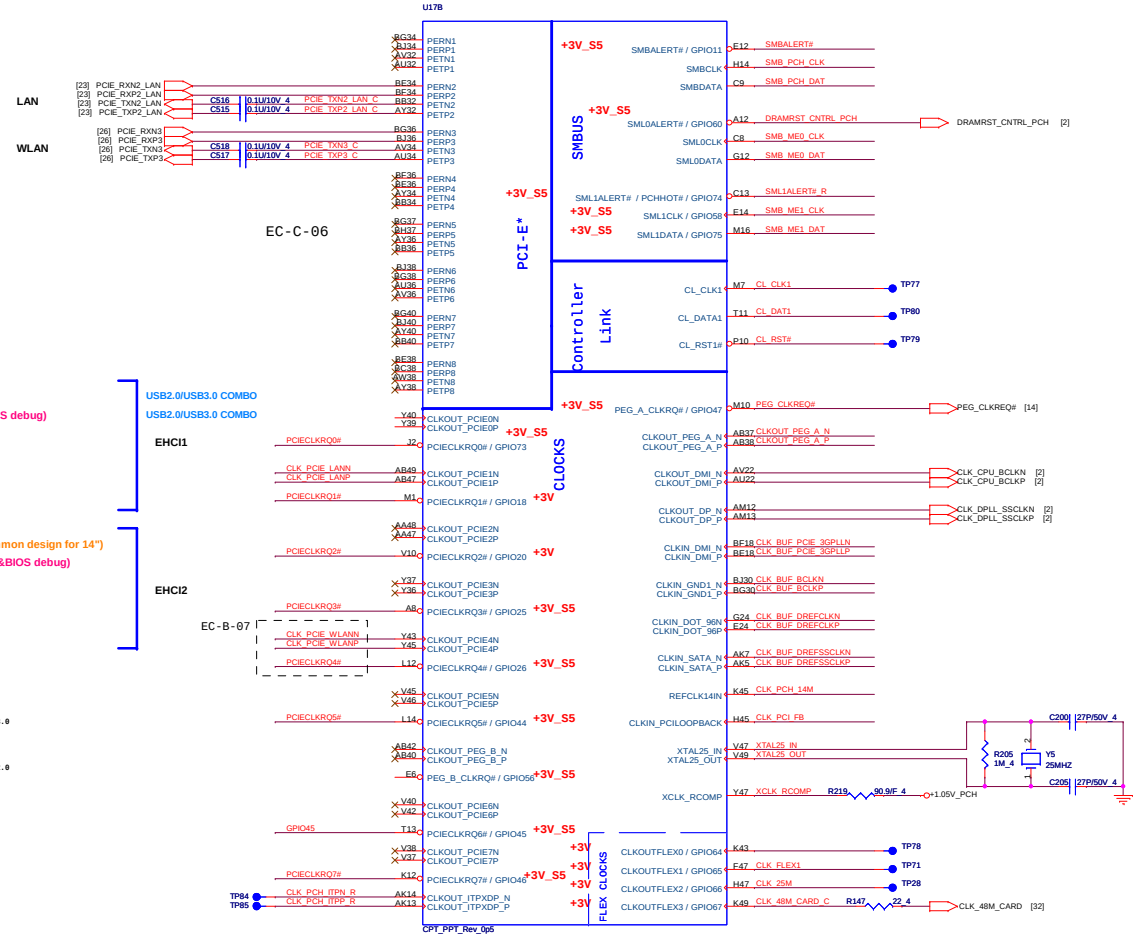
| Size | Document Number | Rev |
|---|---|---|
| Custom | Cougar Point 2/6 | 1B |

Date: Monday, January 09, 2012 Sheet 7 of 46

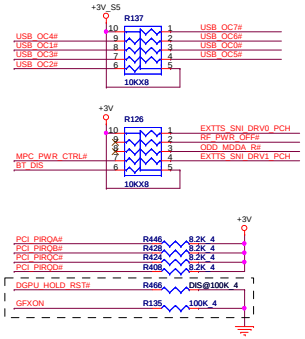
# Cougar Point-M/Panther Point (PCI,USB,NVRAM)



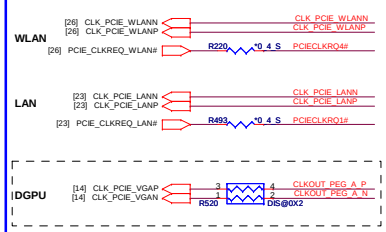

# Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)




## PCI/USBOC# Pull-up(CLG)

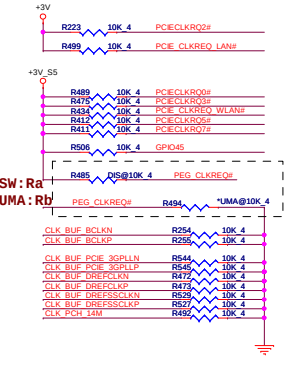


## PCIE CLOCK

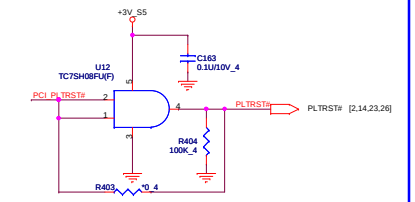



| MPC Switch Control | |
|---|---|
| MPC_PWR_CTRL# | Low = MPC ON<br>High = MPC OFF (Default) |

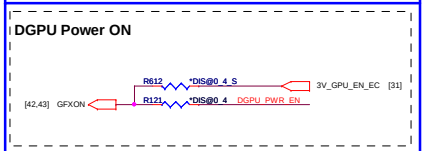
## CLK_REQ/Strap Pin(CLG)



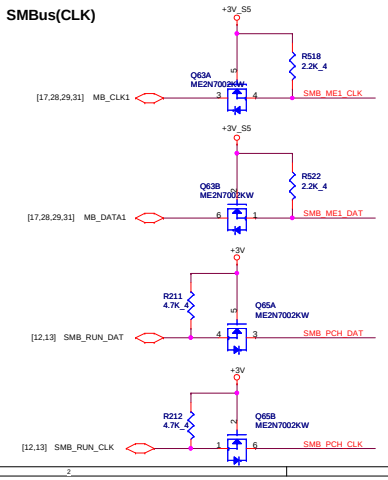

## PLTRST#(CLG)



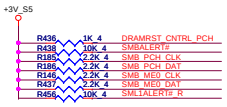
## DGPU Power ON



## SMBus(CLK)



## SMBus/Pull-up(CLG)

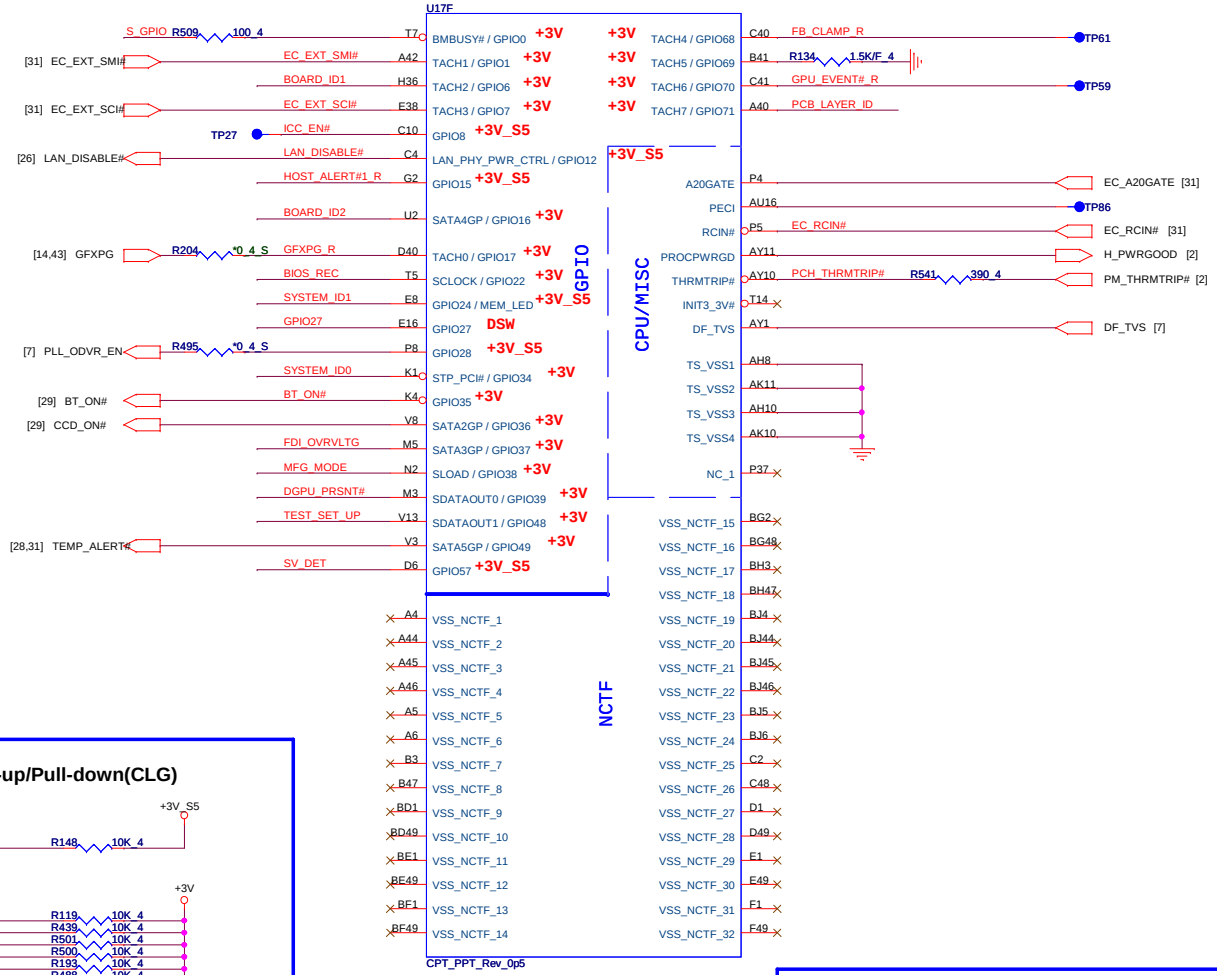


PROJECT LZ1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Cougar Point 3/6 | 1B |

Date: Monday, January 09, 2012 Sheet 8 of 46

# Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)




## Board ID

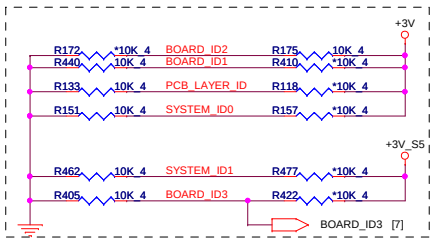
| Board ID For Function | ID1 GPIO6 | ID2 GPIO16 | ID3 GPIO13 |
|---|---|---|---|
| SDV | 0 | 0 | 0 |
| SIV | 0 | 0 | 1 |
| SIT | 0 | 1 | 0 |
| SVT | | | |
| SOVP | | | |

**Board ID:**
BOARD_ID1
BOARD_ID2
BOARD_ID3

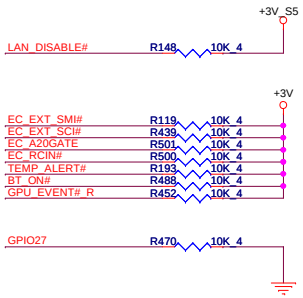
**PCB LAYER ID:**
6 layer-->0
8 layer-->1

**System ID[0.1]:**
-->LZ1 [0.0]
-->LZ2 [0.1]
-->LZ3 [1.0]

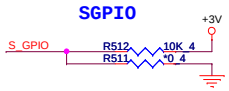
EC-B-02
EC-C-02



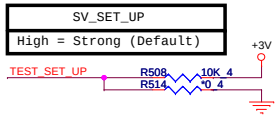

## GPIO Pull-up/Pull-down(CLG)




## SGPIO




| SV_SET_UP |
|---|
| High = Strong (Default) |

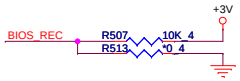




| | | | |
|---|---|---|---|
| SATA2GP/GPIO36 | Reserved | Rising edge of PWROK | This signal has a weak internal pull-down.<br>NOTES:<br>1. The internal pull-down is disabled after PLTRST# deasserts.<br>2. This signal should not be pulled high when strap is sampled. |


| DMI TERMINATION VOLTAGE OVERRIDE | Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT) |
|---|---|

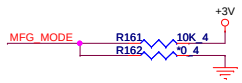

| FDI TERMINATION VOLTAGE OVERRIDE | LOW = Tx, Rx terminated to same voltage |
|---|---|



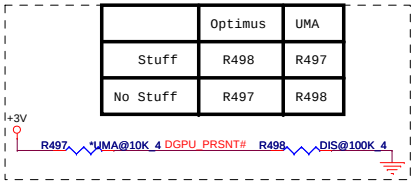

| BIOS RECOVERY | High = Disable (Default)<br>Low = Enable |
|---|---|


| Intel ME Crypto Transport Layer Security (TLS) cipher suite |
|---|
| Low = Disable (Default) |
| High = Enable |

## MFG-TEST



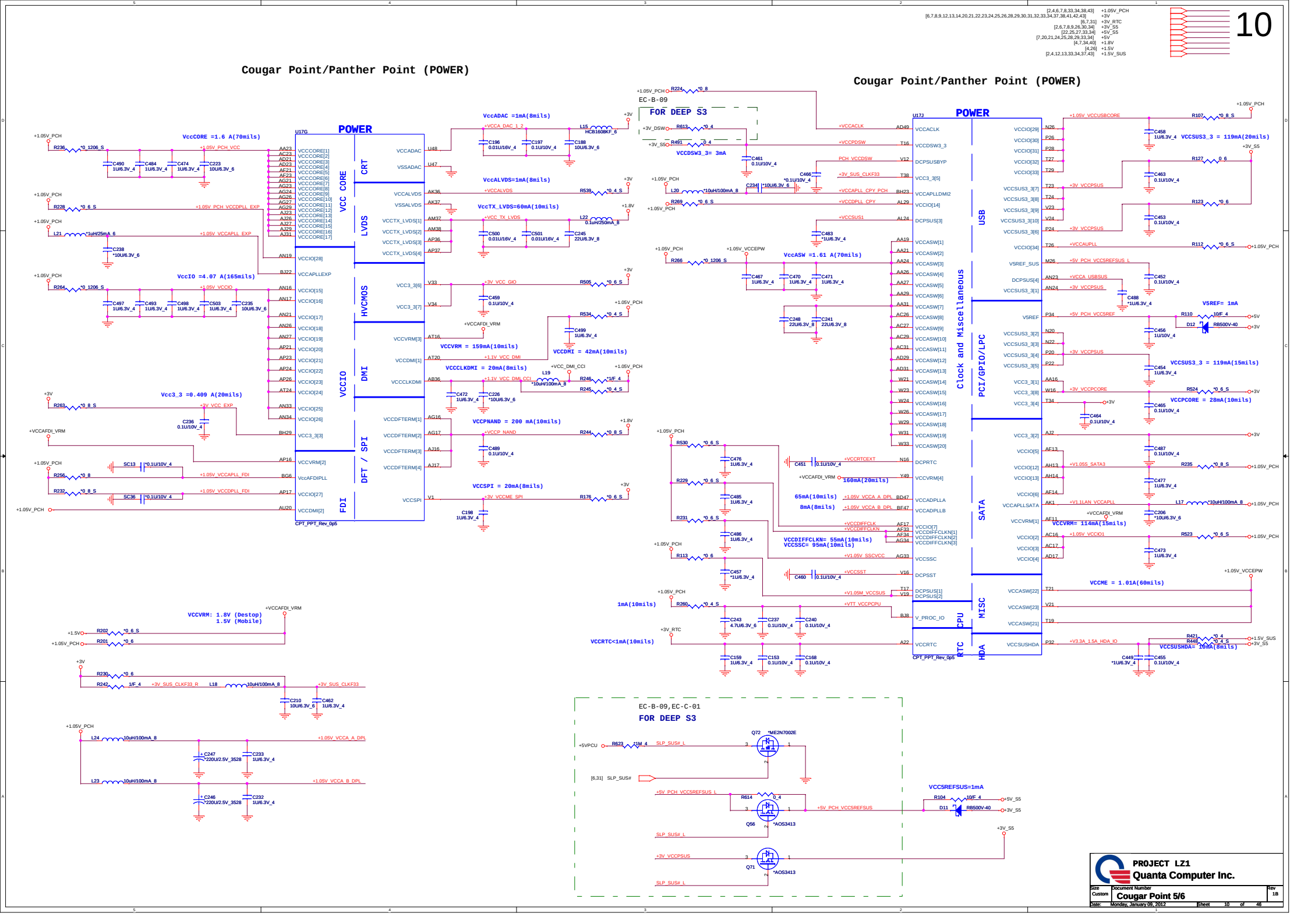

| | Optimus | UMA |
|---|---|---|
| Stuff | R498 | R497 |
| No Stuff | R497 | R498 |




PROJECT LZ1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Cougar Point 4/6 | 1B |

Date: Monday, January 09, 2012 Sheet 9 of 46

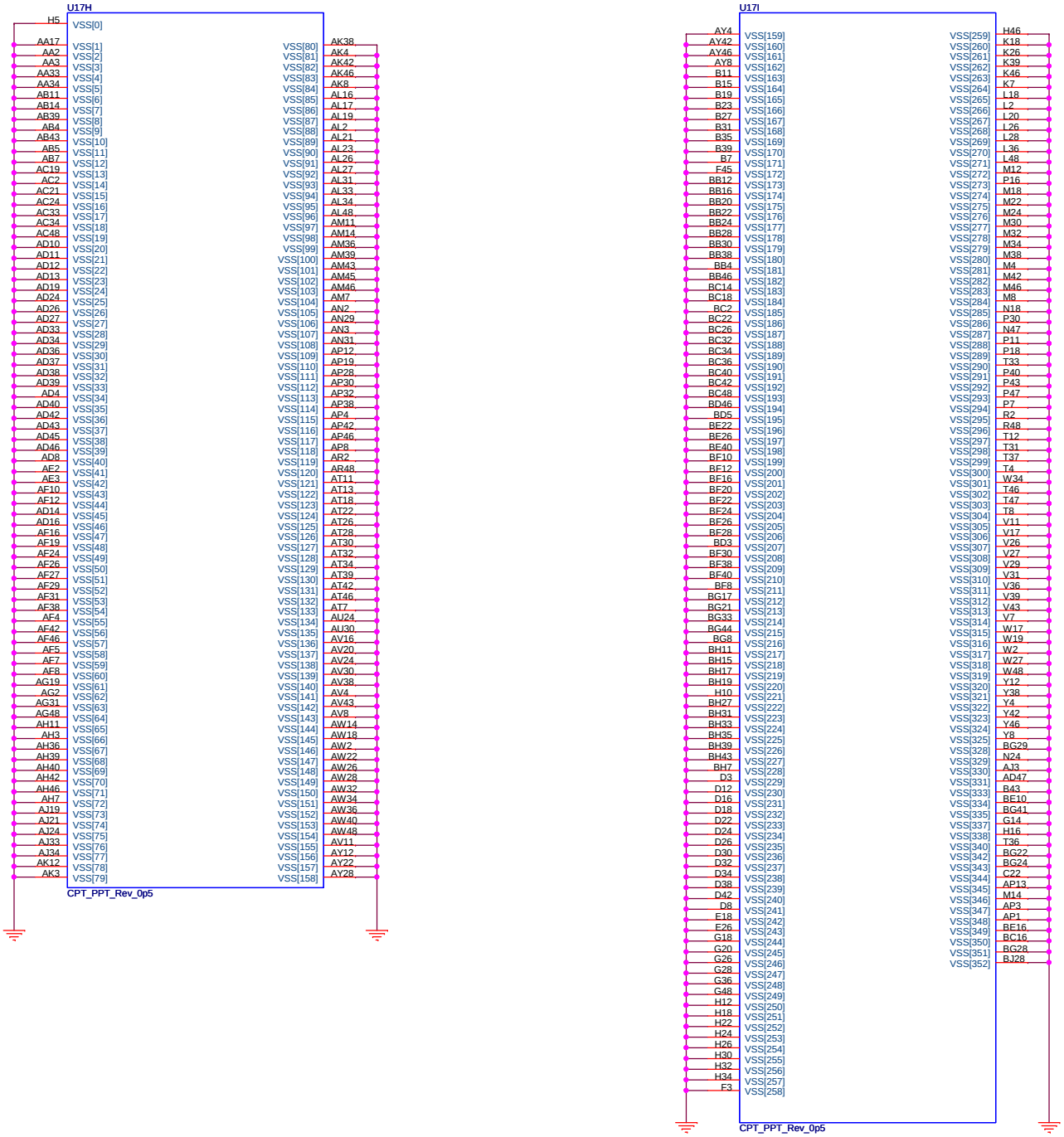



PROJECT LZ1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Cougar Point 5/6 | 1B |

Date: Monday, January 09, 2012 Sheet 10 of 46

# Cougar Point/Panther Point (GND)




**PROJECT LZ1**

**Quanta Computer Inc.**

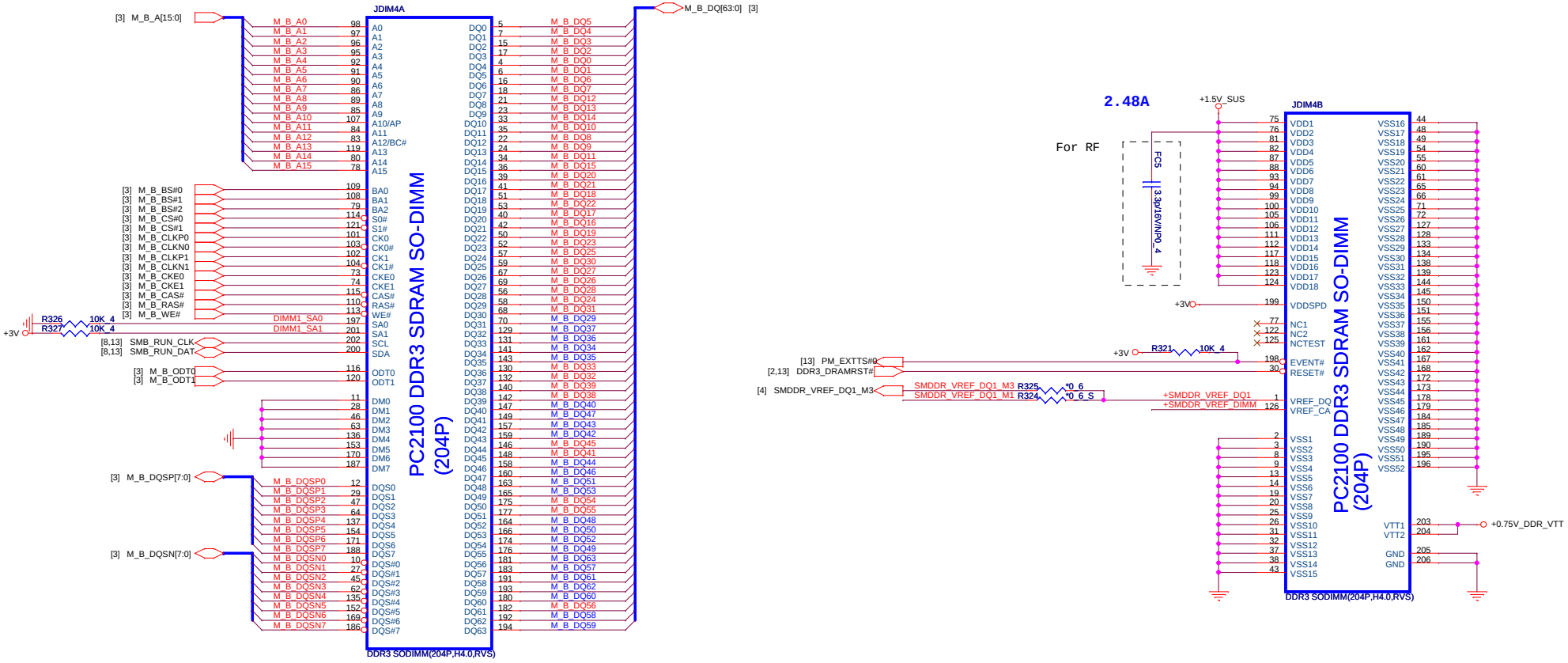
| Size | Document Number | Rev |
|---|---|---|
| Custom | Cougar Point 6/6 | 1B |

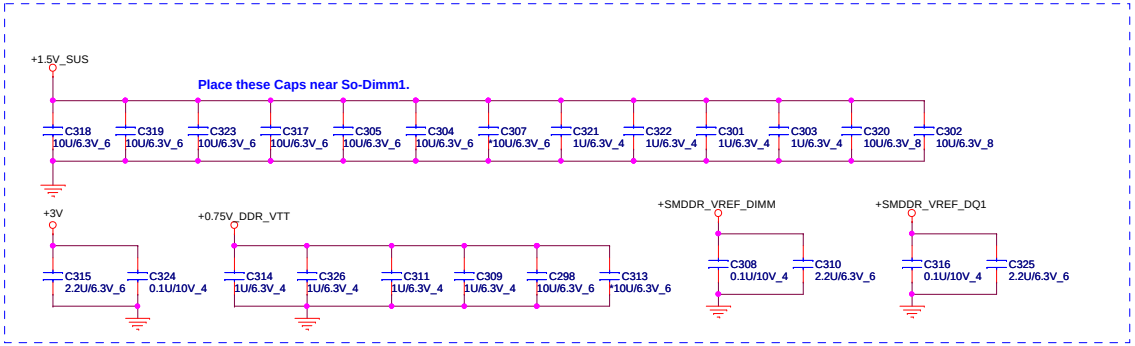
Date: Monday, January 09, 2012 Sheet 11 of 46

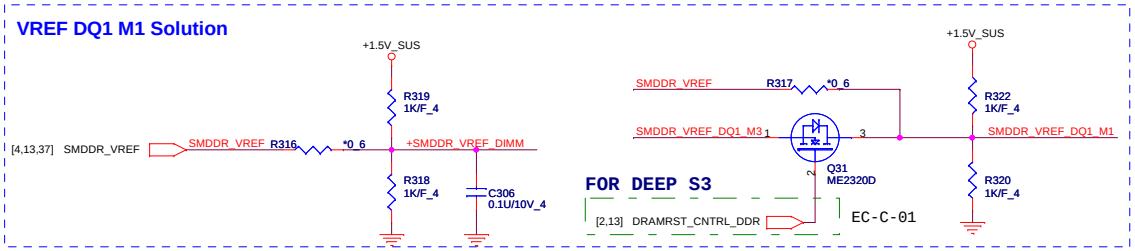
# DDR_RVS(DDR)



[6,7,8,9,10,13,14,20,21,22,23,24,25,26,28,29,30,31,32,33,34,37,38,41,42,43] +3V
[2,4,10,13,33,34,37,43] +1.5V_SUS
[13,34,37] +0.75V_DDR_VTT
[13] +SMDDR_VREF_DIMM



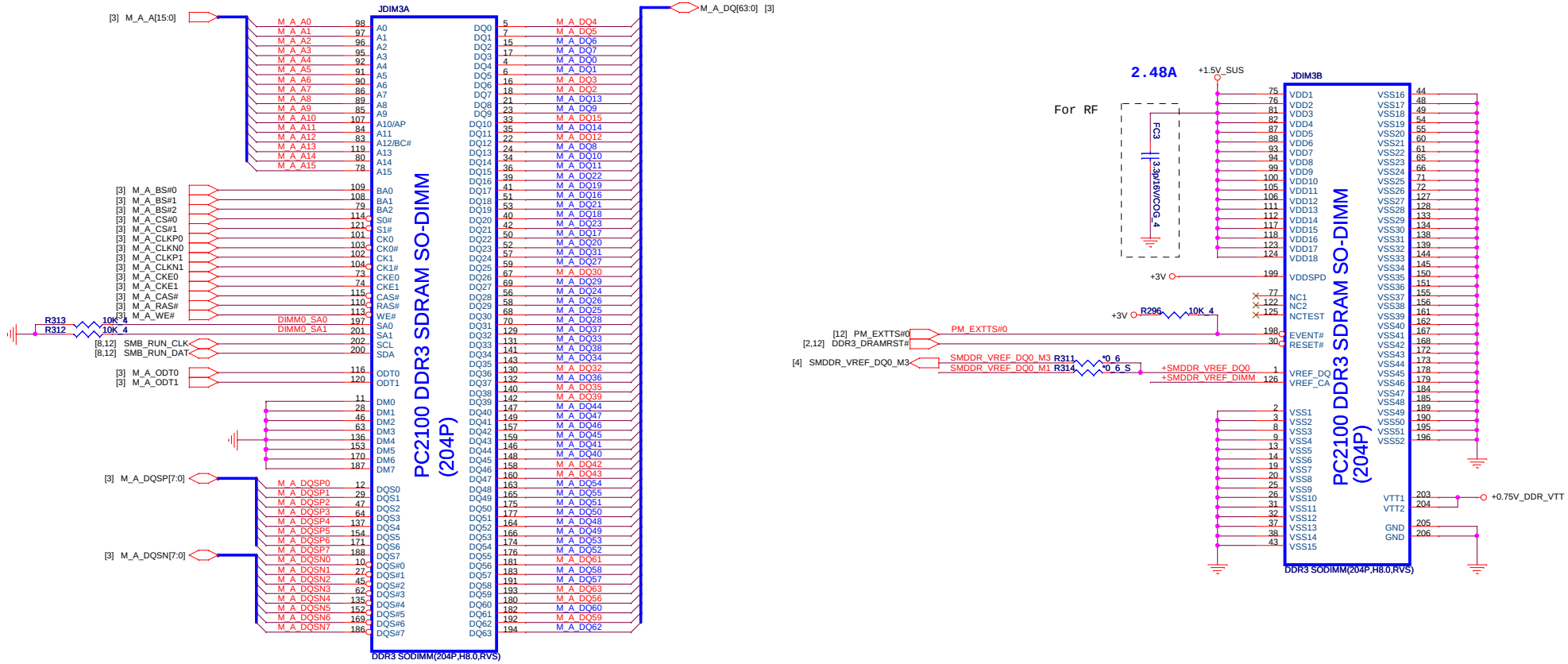



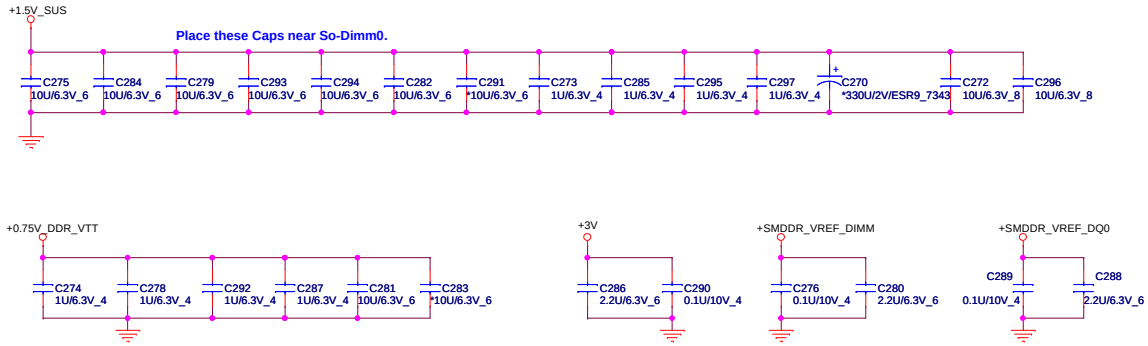

| | | |
|---|---|---|
| PROJECT LZ1 | | |
| Quanta Computer Inc. | | |
| Size: Custom | Document Number: DDRIII SO-DIMM-0 | Rev: 1B |
| Date: Monday, January 09, 2012 | Sheet 12 of 46 | |

# DDR_RVS(DDR)

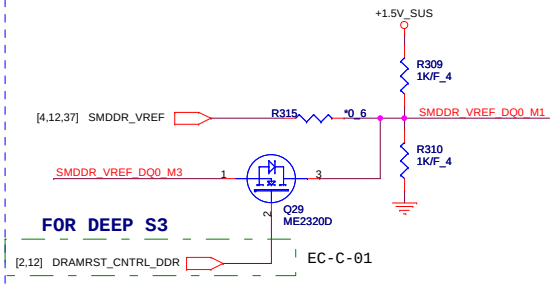


[6,7,8,9,10,12,14,20,21,22,23,24,25,26,28,29,30,31,32,33,34,37,38,41,42,43] +3V
[2,4,10,12,33,34,37,43] +1.5V_SUS
[12,34,37] +0.75V_DDR_VTT
[12] +SMDDR_VREF_DIMM




## VREF DQ0 M1 Solution




PROJECT LZ1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | DDRIII SO-DIMM-1 | 1B |

Date: Monday, January 09, 2012 Sheet 13 of 46

[15,16,43] +1.05V_GFX_PCIE
[16,17,43] +3V_GPU
[15,18,19,43] +1.5V_GPU
[6,7,8,9,10,12,13,20,21,22,23,24,25,26,28,29,30,31,32,33,34,37,38,41,42,43] +3V
[42] GFX_CORE


## power up sequence

All GPU power rails must ramp up after VDD33. The following conditions must be met:

- tNVVDD > 0
- tFBVDDQ > 0
- tPEX_VDD > 0
- tIFPx_IOVDD ≥ 0
- tIFPy_IOVDD ≥ 0
- The ramp time for any rail must be more than 40 us.



Figure 18. Recommended Power Off Sequencing Order




Figure 17. Recommended Power On Sequencing Order




Figure 18. Recommended Power Off Sequencing Order

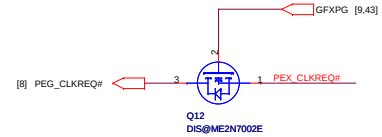
### For power-down sequency



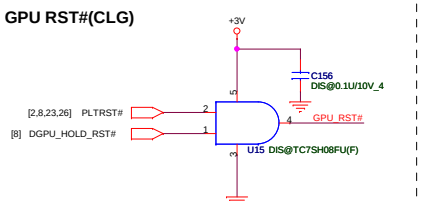

The following voltage constraints must be satisfied at all times including power down after VDD33 has ramped up:

- NVVDD <= VDD33+0.5 V
- FBVDDQ <= VDD33+0.5 V

### PEG CLK detect




### GPU RST#(CLG)

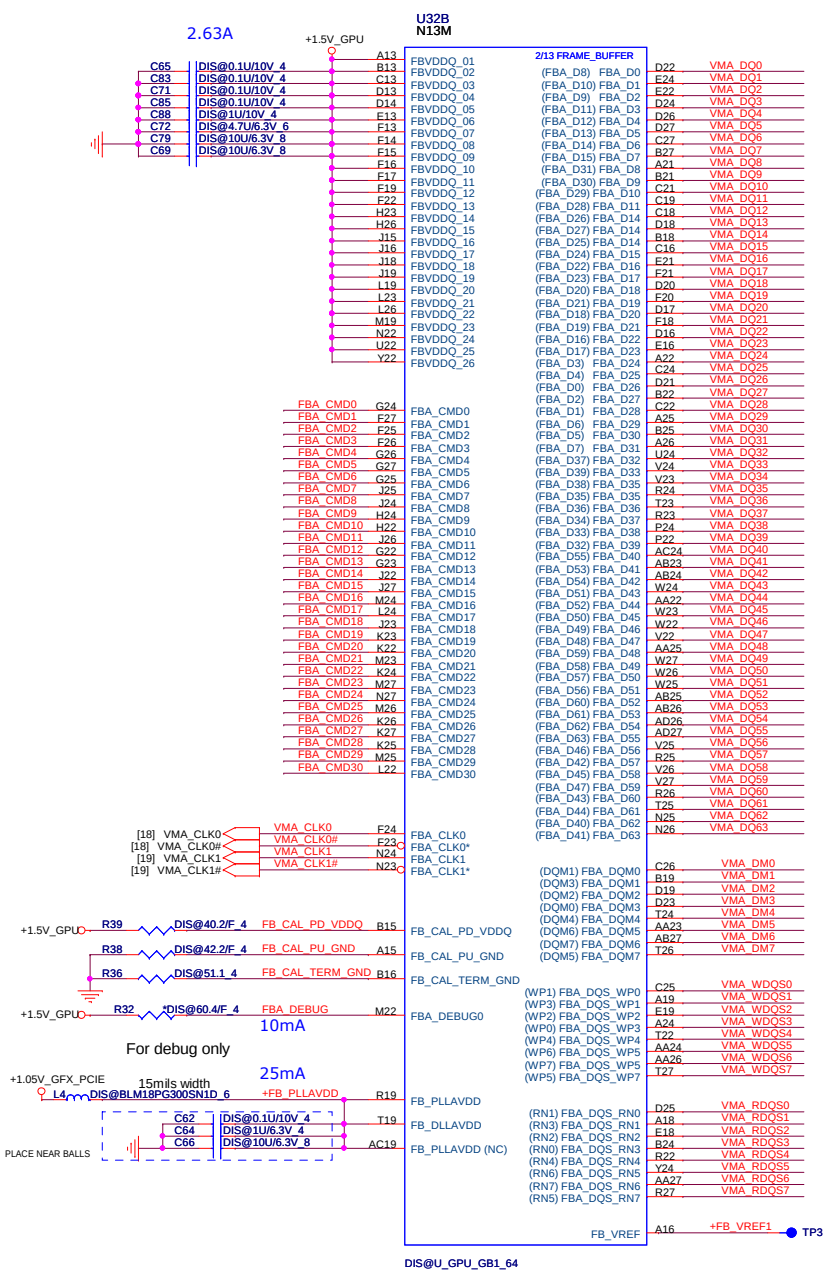


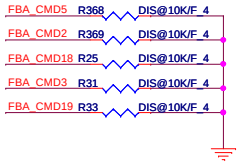


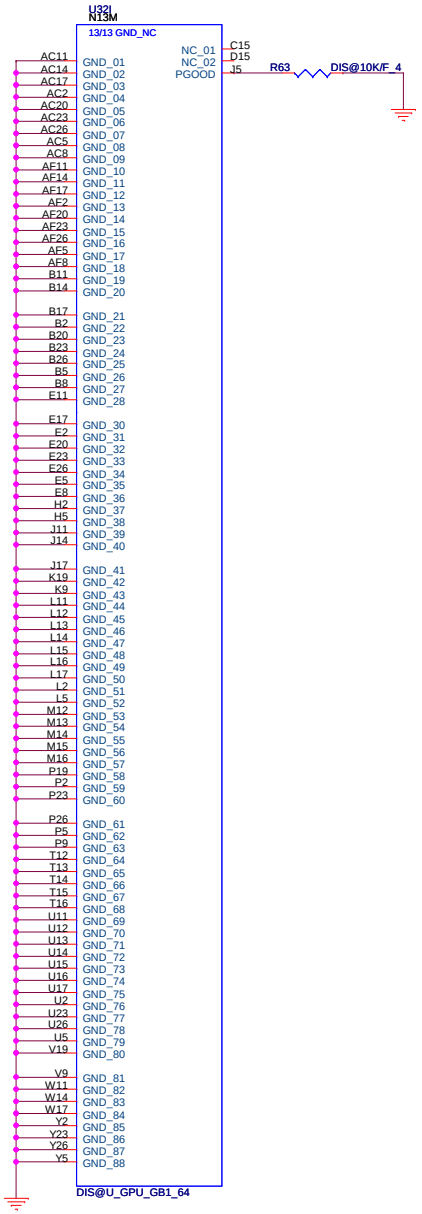

| | |
|---|---|
| PROJECT | LZ1 |
| Quanta Computer Inc. | |
| Size: Custom | Document Number: N13M(PCIE I/F) 1/5 |
| Rev | 1B |
| Date: Monday, January 09, 2012 | Sheet 14 of 46 |

[14,16,43] +1.05V_GFX_PCIE
[14,18,19,43] +1.5V_GPU

[18,19] VMA_DQ[63..0]
[18,19] VMA_DM[7..0]
[18,19] VMA_WDQS[7..0]
[18,19] VMA_RDQS[7..0]
[18,19] FBA_CMD[30..0]



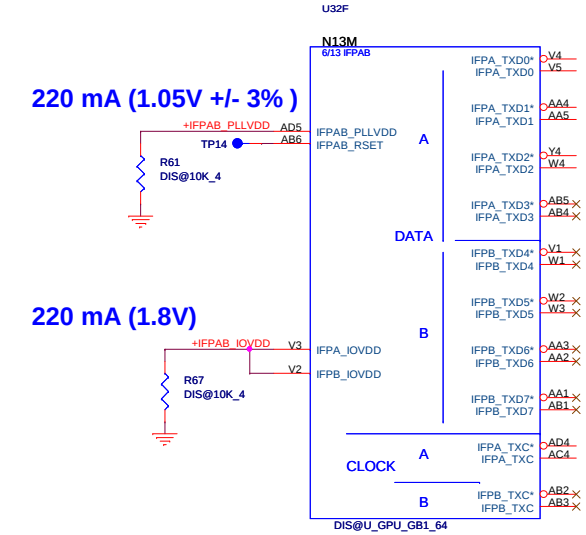



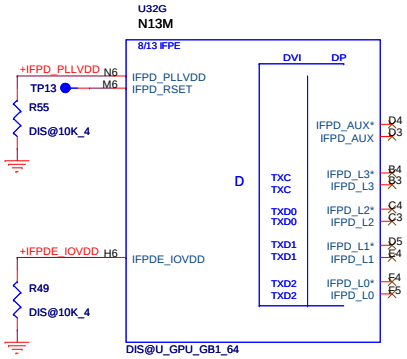




**PROJECT LZ1**
**Quanta Computer Inc.**

| Size | Document Number | Rev |
|---|---|---|
| Custom | N13M(MEMORY I/F & GND) 2/5 | 1B |

Date: Monday, January 09, 2012 Sheet 15 of 46




The following guidelines only apply to a fully unused IFP macro:

- Pull down IFPxy_IOVDD with 10 kΩ resistor
- Pull down IFPxy_PLLVDD with 10 kΩ resistor
- The other IO pins can be NC
- It is also recommended that footprints for both a 10 kΩ resistor to ground and a 10 kΩ resistor to power be implemented as stuffing options to allow for flexibility in design options

The circuit shown in Figure 6.12 shows the connection for an unused IFP macro.

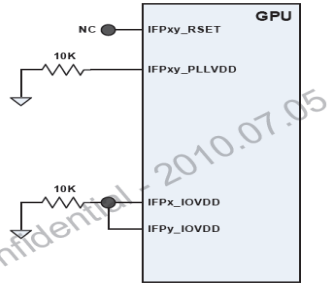
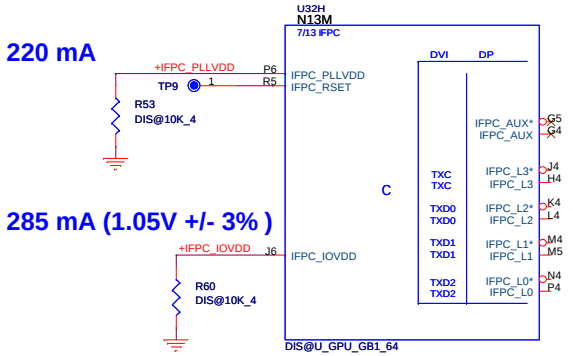
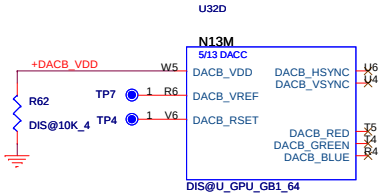



Figure 6.12 Unused IFP Interface



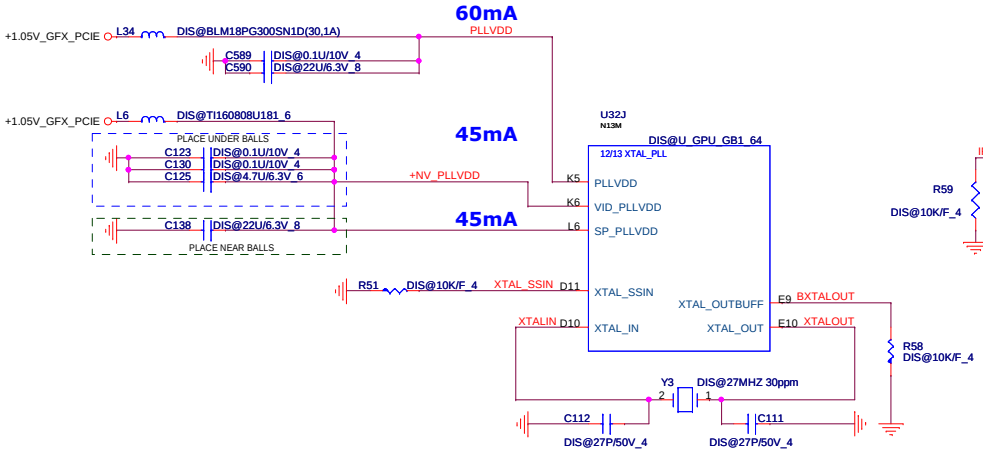



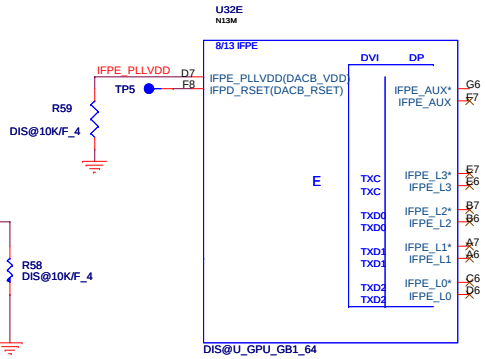

## 7.4 Unused DAC Interface

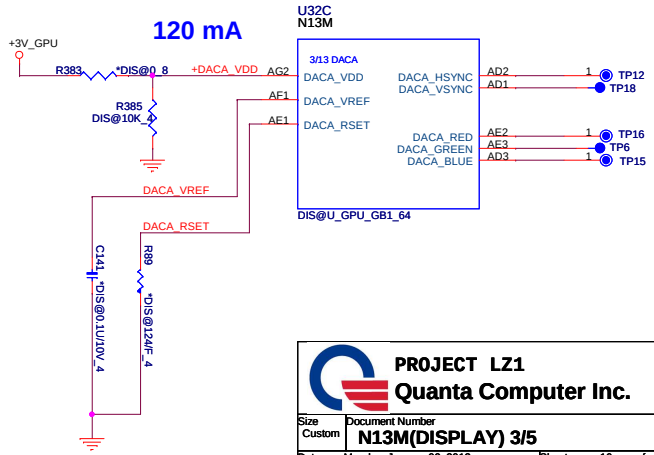
To disable a DAC interface:

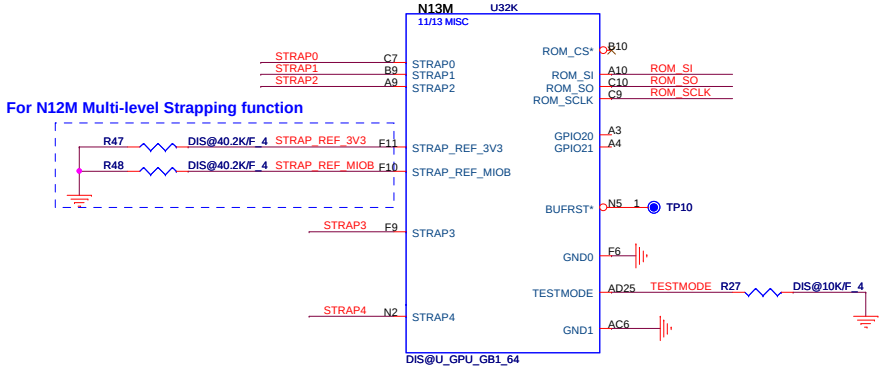
- Pull down the DACx_VDD with a 10 kΩ resistor
- The other DAC IO pins (including DACx_VREF, DACx_RSET) can be NC





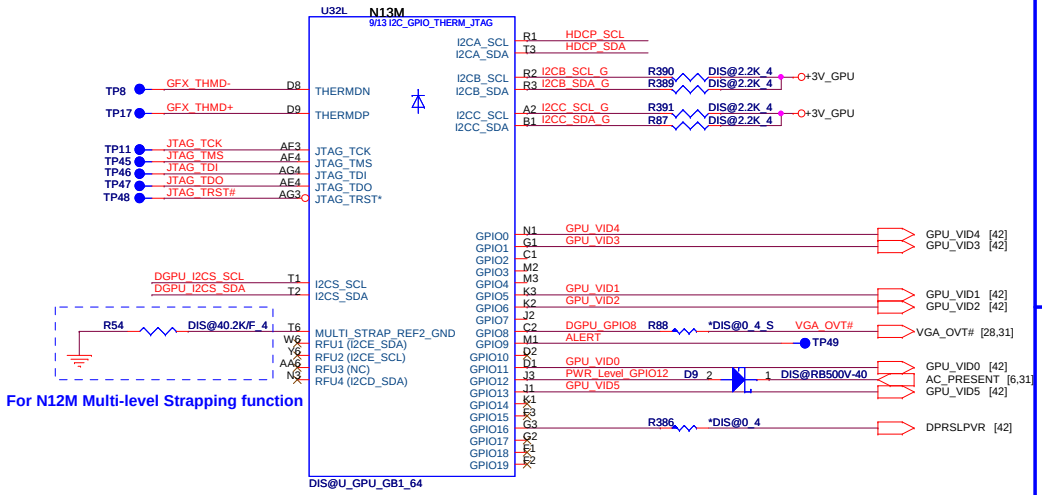



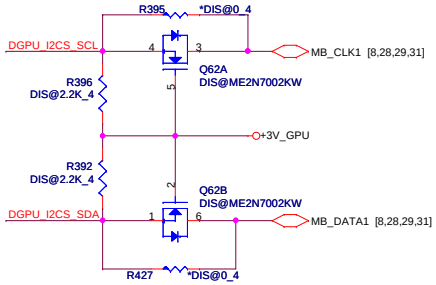





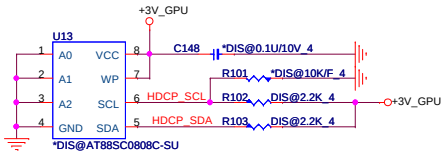

## 9.5 Unused I2C Pins

For unused dedicated (non-AUX) I2C pins, pull-up both the I2Cx_SCL, I2Cx_SDA, to 3.3 V using 2.2 kΩ resistors.routing.




## HDCP ROM




| DHCP ROM | |
|---|---|
| HDCP_SCL | Low: Crypto ROM<br>Hi: I2C ROM |

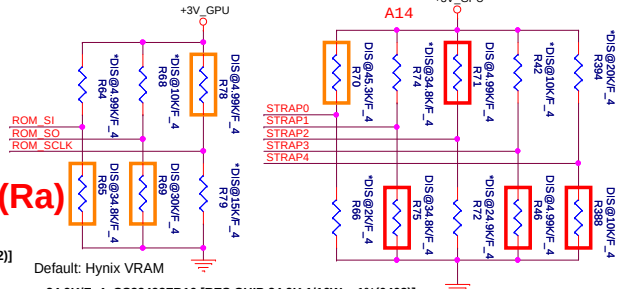
nV FAE suggest that the device ID for N13M-GE1 is 0x1058

[14,16,43] +3V_GPU

| Logical Strap Bit Mapping | | |
|---|---|---|
| Rv | PU-VDD | PD-GND |
| 5K | 1000 | 0000 |
| 10K | 1001 | 0001 |
| 15K | 1010 | 0010 |
| 20K | 1011 | 0011 |
| 25K | 1100 | 0100 |
| 30K | 1101 | 0101 |
| 35K | 1110 | 0110 |
| 45K | 1111 | 0111 |

N13M-GE1

PCI_DEVID[4]/SUBVENDOR




Default: Hynix VRAM

4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30K/F_4: CS33002FB13 [RES CHIP 30K 1/16W +-1%(0402)]
34.8K/F_4: CS33482FB22 [RES CHIP 34.8K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

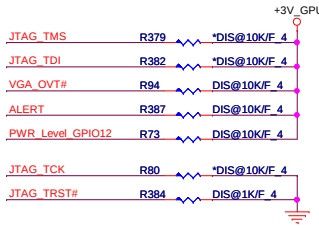
24.9K/F_4: CS32492FB16 [RES CHIP 24.9K 1/16W +-1%(0402)]
20K/F_4: CS32002FB29 [RES CHIP 20K 1/16W +-1%(0402)]

| | Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 | |
|---|---|---|---|---|---|
| ROM_SO N13M-GE1 | FB[1] | FB[0] | SMB_ALT_ADDR | VGA_DEVICE | 0101 |
| ROM_SCLK | PCI_DEVIDE[4] | SUB_VENDOR | PCI_DEVID[5] | PEX_PLL_EN_TERM | 1010 |
| ROM_SI | RAMCFG[3] | RAMCFG[2] | RAMCFG[1] | RAMCFG[0] | 0110 |
| STRAP0 | USER[3] | USER[2] | USER[1] | USER[0] | 1111 |
| STRAP1 | 3GIO_PADCFG[3] | 3GIO_PADCFG[2] | 3GIO_PADCFG[1] | 3GIO_PADCFG[0] | 0110 |
| STRAP2 | PCI_DEVID[3] | PCI_DEVID[2] | PCI_DEVID[1] | PCI_DEVID[0] | 1000 |
| STRAP3 | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED | 0000 |
| STRAP4 | RESERVED | RESERVED | PCIE_MAX_SPEED | DP_PLL_VDD33V | 0001 |

VRAM Configuration Table

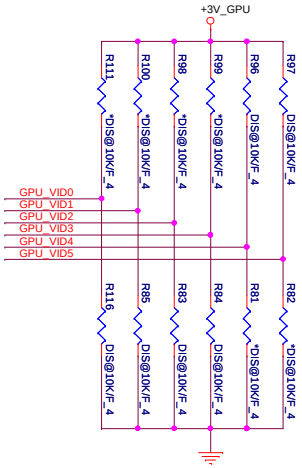
(Ra)

| | RAMCFG [3:0] | DESCRIPTION | Vendor | Vendor P/N | ROM_SI |
|---|---|---|---|---|---|
| | 0000 | | Reserved | | |
| | 0001 | | Reserved | | |
| | 0010 | | Reserved | | |
| | 0011 | | Reserved | | |
| | 0101 | | Reserved | | |
| | 0110 | | Reserved | | |
| AKD5MGWTW00 | 0110 | DDR3 128Mx16x4, 64bit, 1GB,900MHz | Hynix | H5TQ2G63BFR-11C | PD 34.8K/F |
| AKD5MGWT500 | 0111 | DDR3 128Mx16x4, 64bit, 1GB,900MHz | Samsung | K4W2G1646C-HC11 | PD 45.3K/F |




## NVVDD Table

| N13M-GE1 (GF119) | NVVDD (0.9V) |
|---|---|
| GPU_VID0 | 0 (R116) |
| GPU_VID1 | 0 (R85) |
| GPU_VID2 | 0 (R83) |
| GPU_VID3 | 0 (R84) |
| GPU_VID4 | 1 (R96) |
| GPU_VID5 | 1 (R97) |




| GPIO pin Name | Normal Function | I/O | Functional Description |
|---|---|---|---|
| GPI00 | GPU_VID4 | O | GPU Core VDD VID4 |
| GPI01 | GPU_VID3 | O | GPU Core VDD VID3 |
| GPI02 | LCD_BL_PWM | O | Panel Backlight PWM Brightness Control |
| GPI03 | LCD_VCC | O | Panel Power Enable |
| GPI04 | LCD_BLEN | O | Panel Backlight Enable |
| GPI05 | GPU_VID1 | O | GPU Core VDD VID1 |
| GPI06 | GPU_VID2 | O | GPU Core VDD VID2 |
| GPI07 | 3D Vision | O | 3D Vision Left/Right signal |
| GPI08 | OVERT | I/O | Active Low Thermal Catastrophic Over Temperature |
| GPI09 | ALERT | I/O | Active Low Thermal Alert |
| GPI010 | MEM_VREF_CTL | O | Memory VREF Control |
| GPI011 | GPU_VID0 | O | GPU Core VDD VID0 |
| GPI012 | PWR_LEVEL | I | AC Power Detect Input. High = AC, Low= Battery |
| GPI013 | GPU_VID5 | O | GPU Core VDD VID5 |
| GPI014 | HPD_AB | I | Hot Plug Detect for IFPAB |
| GPI015 | HPD_C | I | Hot Plug Detect for IFPC |
| GPI016 | MEM_VDD_CTL | O | Memory VDD VID |
| GPI017 | HPD_D | I | Hot Plug Detect for IFPD |
| GPI018 | HPD_E | I | Hot Plug Detect for IFPE |
| GPI019 | HPD_F | I | Hot Plug Detect for IFPF |
| GPI020 | Reserved | | |
| GPI021 | Reserved | | |

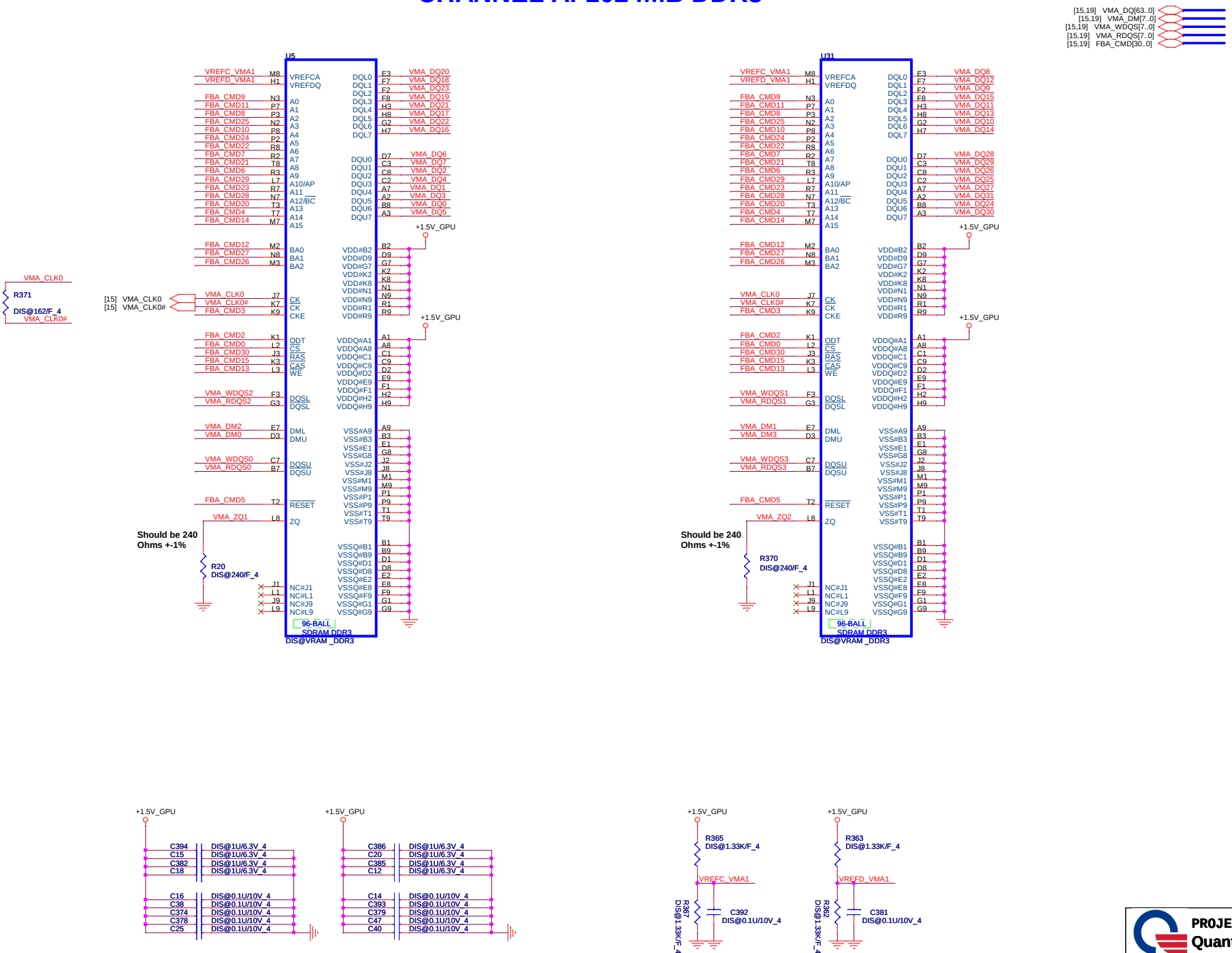


PROJECT LZ1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | N13M(GPIO & STRRAPS) 4/5 | 1B |

Date: Monday, January 09, 2012 Sheet 17 of 46

# CHANNEL A: 1024MB DDR3

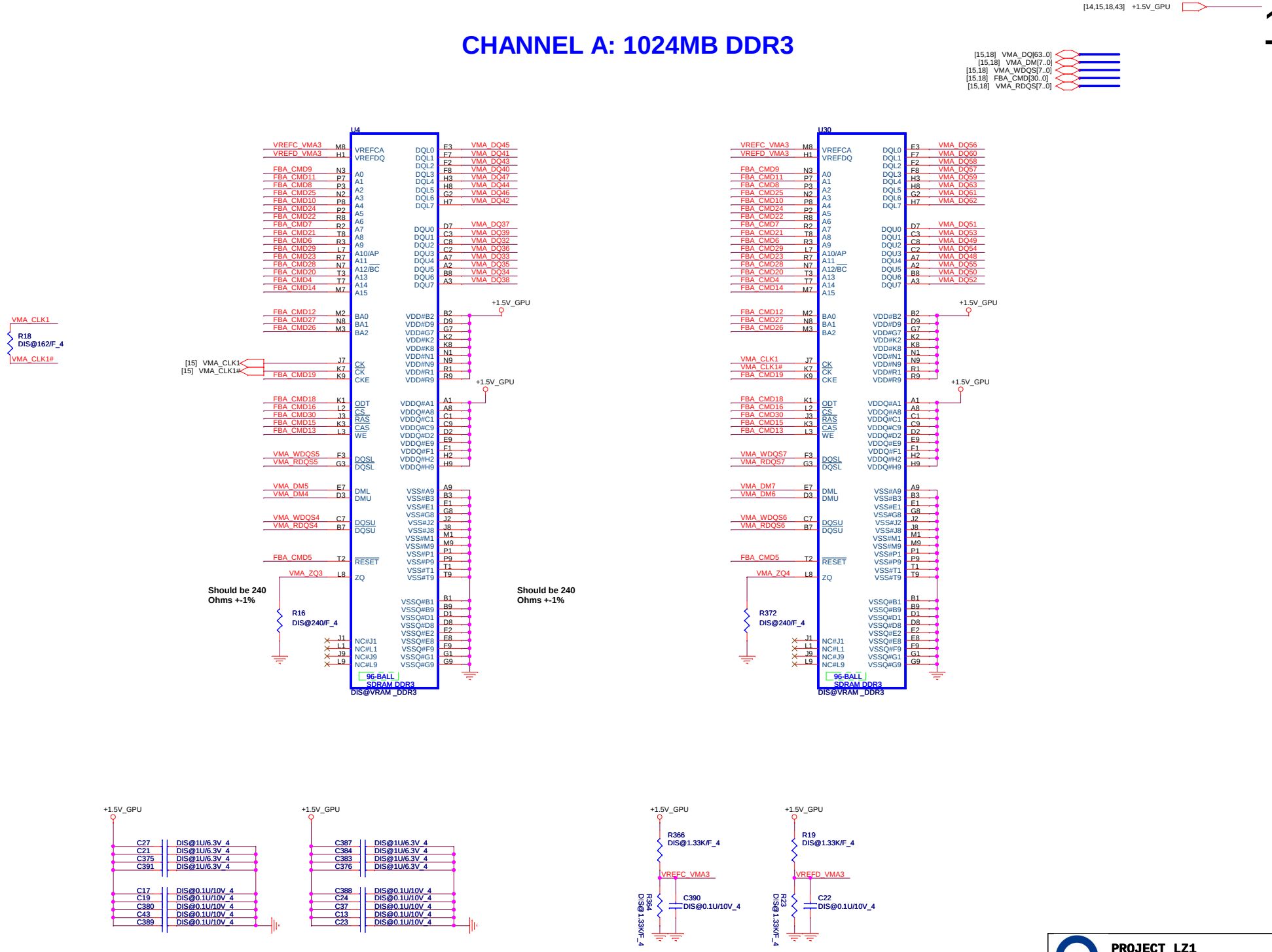



**PROJECT LZ1**
**Quanta Computer Inc.**

| Size | Document Number | Rev |
|---|---|---|
| Custom | N13M (DDR3) 5/5 | 1B |

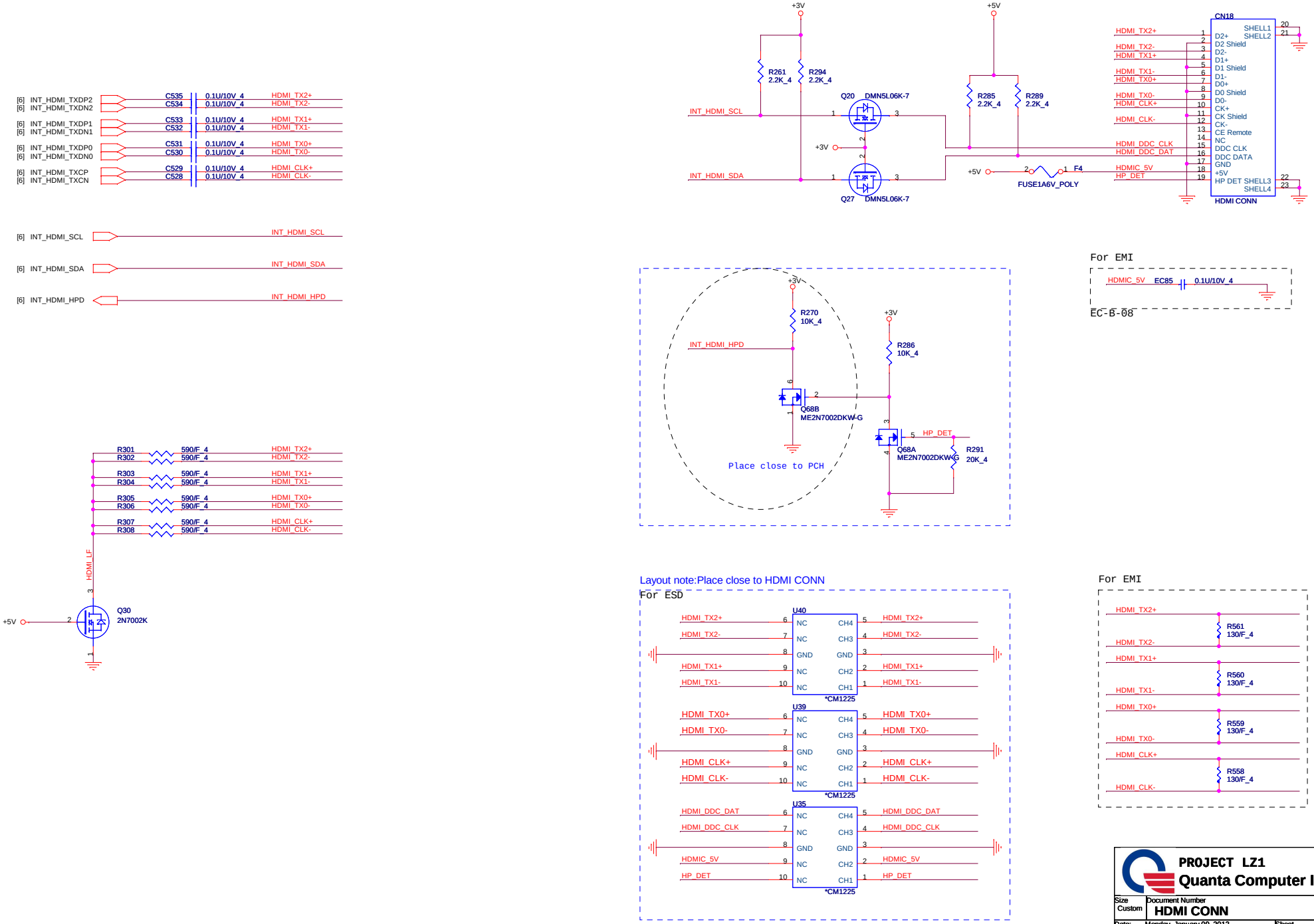
Date: Monday, January 09, 2012 Sheet 18 of 46

# CHANNEL A: 1024MB DDR3



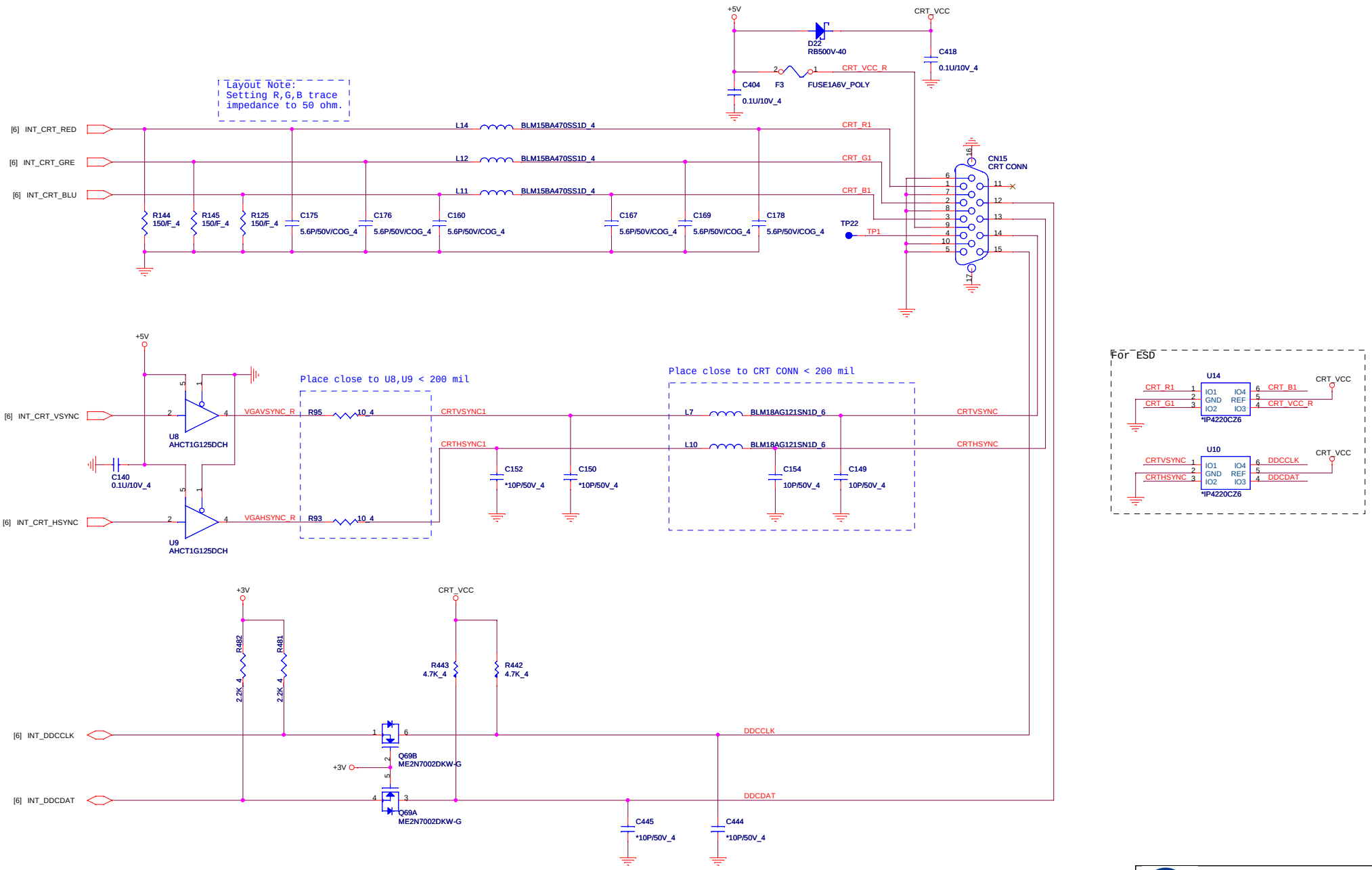

| | | |
|---|---|---|
| PROJECT LZ1 | | |
| Quanta Computer Inc. | | |
| Size: Custom | Document Number: N13M (DDR3) 6/6 | Rev: 1B |
| Date: Monday, January 09, 2012 | Sheet 19 of 46 | |

[6,7,8,9,10,12,13,14,21,22,23,24,25,26,28,29,30,31,32,33,34,37,38,41,42,43] +3V
[7,10,21,24,25,28,29,33,34] +5V




| | | | |
|---|---|---|---|
| PROJECT LZ1 Quanta Computer Inc. | | | |
| Size Custom | Document Number HDMI CONN | | Rev 1B |
| Date: Monday, January 09, 2012 | Sheet 20 of 46 | | |

[7,10,20,24,25,28,29,33,34] +5V
[6,7,8,9,10,12,13,14,20,22,23,24,25,26,28,29,30,31,32,33,34,37,38,41,42,43] +3V



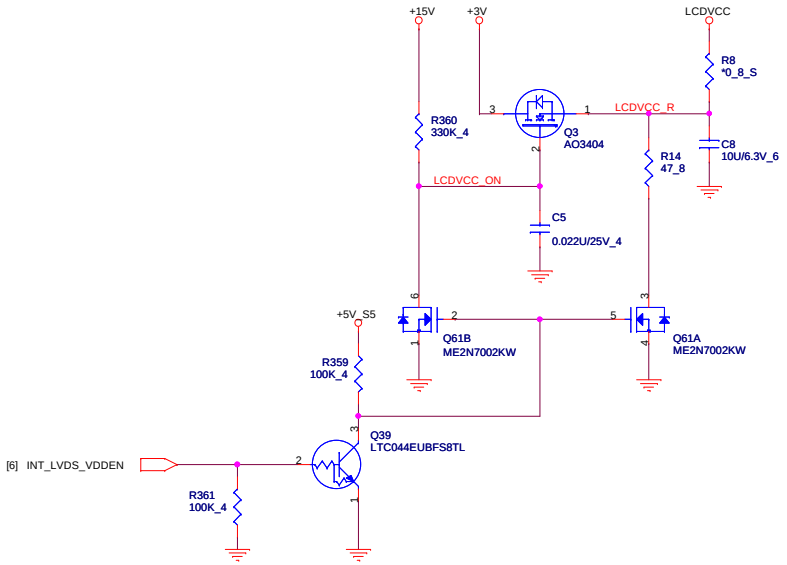

**PROJECT LZ1**
**Quanta Computer Inc.**

| Size | Document Number | Rev |
|---|---|---|
| Custom | CRT CONN | 1B |

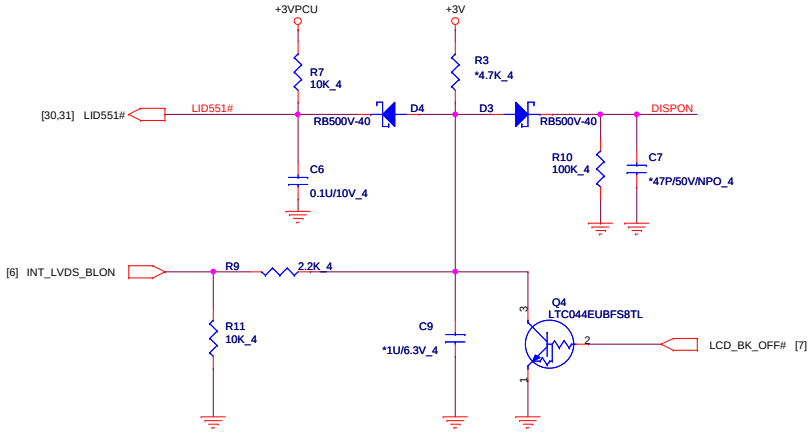
Date: Monday, January 09, 2012 Sheet 21 of 46

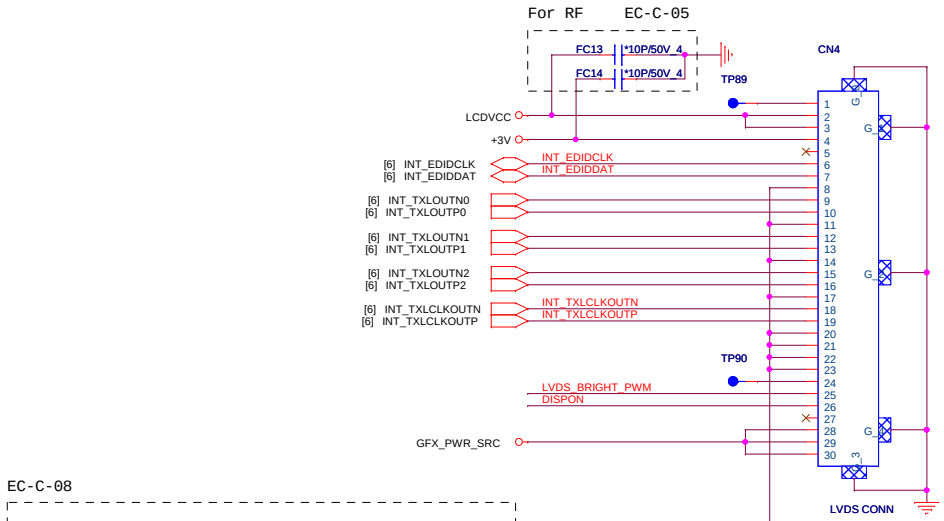
[25,29,34,36,43] +15V
[6,7,8,9,10,12,13,14,20,21,23,24,25,26,28,29,30,31,32,33,34,37,38,41,42,43] +3V
[10,25,27,33,34] +5V_S5
[6,7,23,25,26,30,31,34,35,36,40] +3VPCU
[33,35,36,37,38,39,41,42] VIN

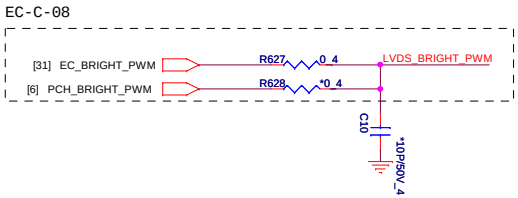
## LCDVCC

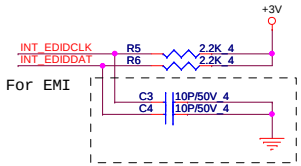


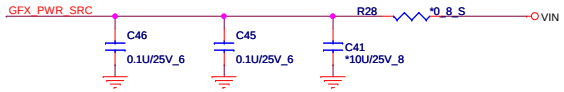

## Back light

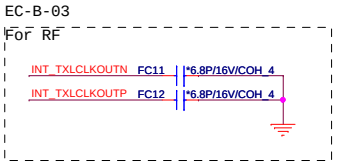


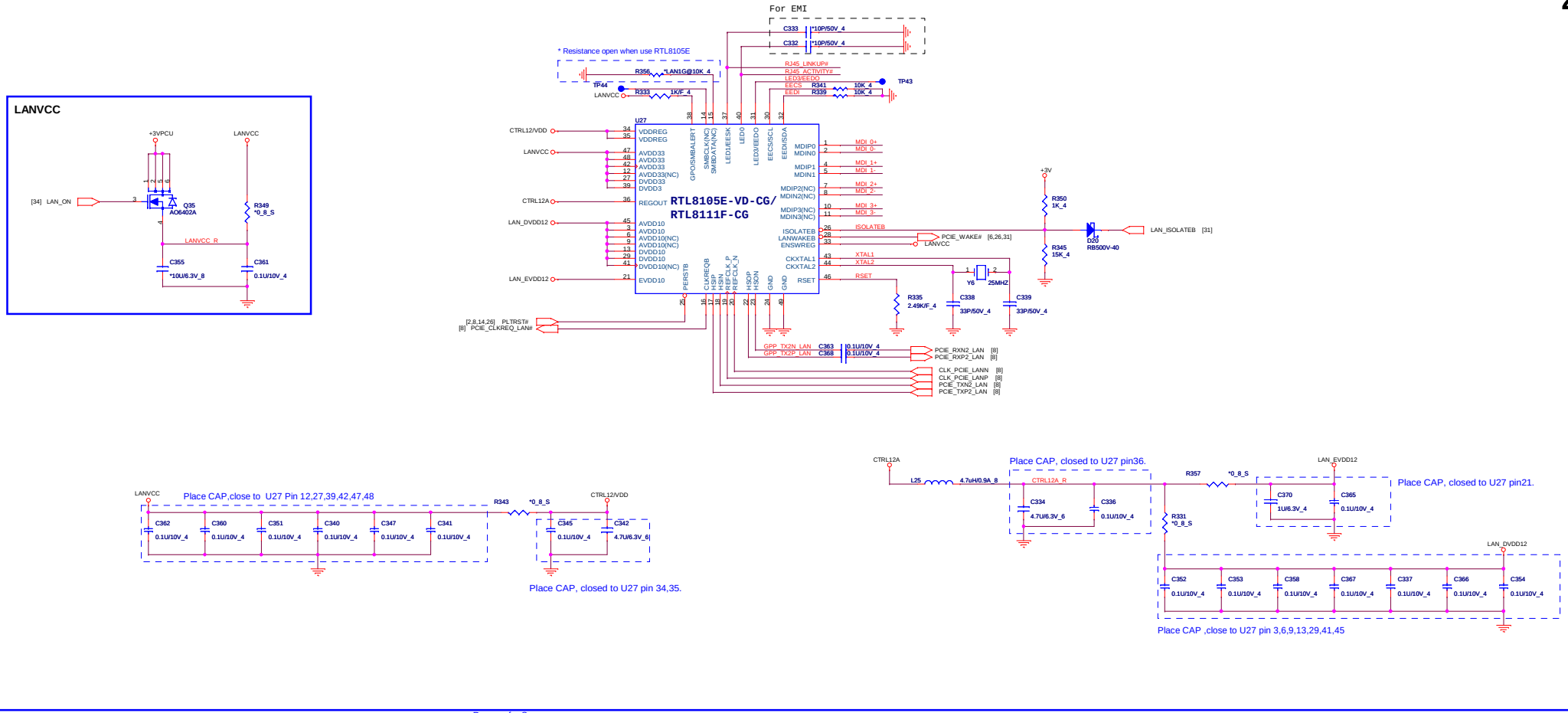



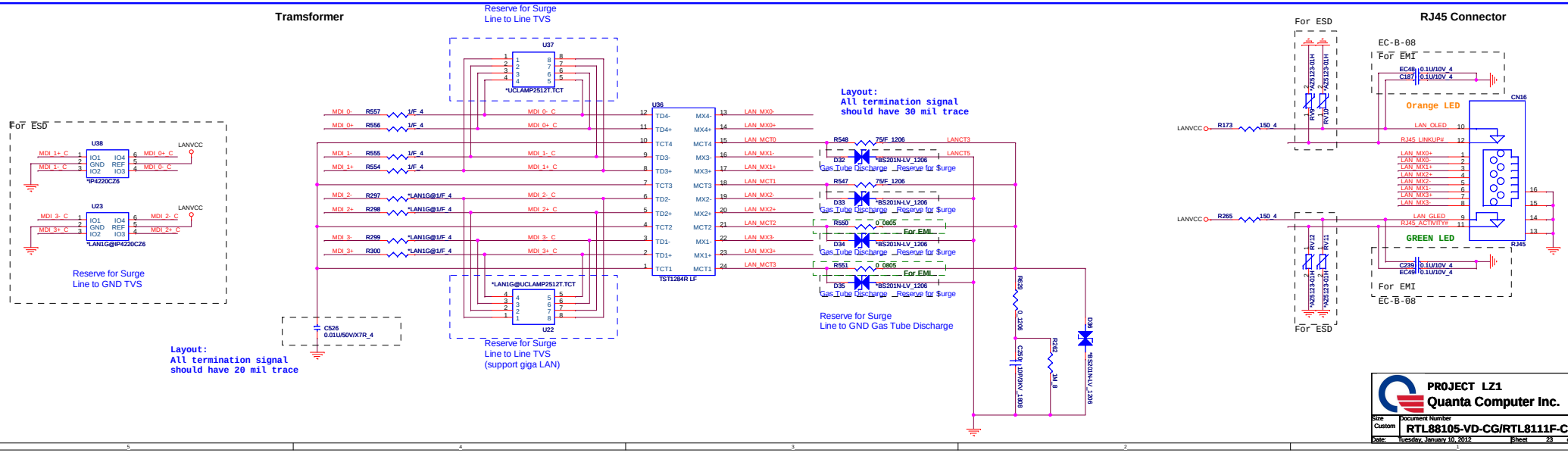




| | | |
|---|---|---|
| PROJECT LZ1 Quanta Computer Inc. | | |
| Size Custom | Document Number LCD CONN | Rev 1B |
| Date: Monday, January 09, 2012 | Sheet 22 of 46 | |

[6,7,22,25,26,30,31,34,35,36,40] +3VPCU
[34] LANVCC
[6,7,8,9,10,12,13,14,20,21,22,24,25,26,28,29,30,31,32,33,34,37,38,41,42,43] +3V



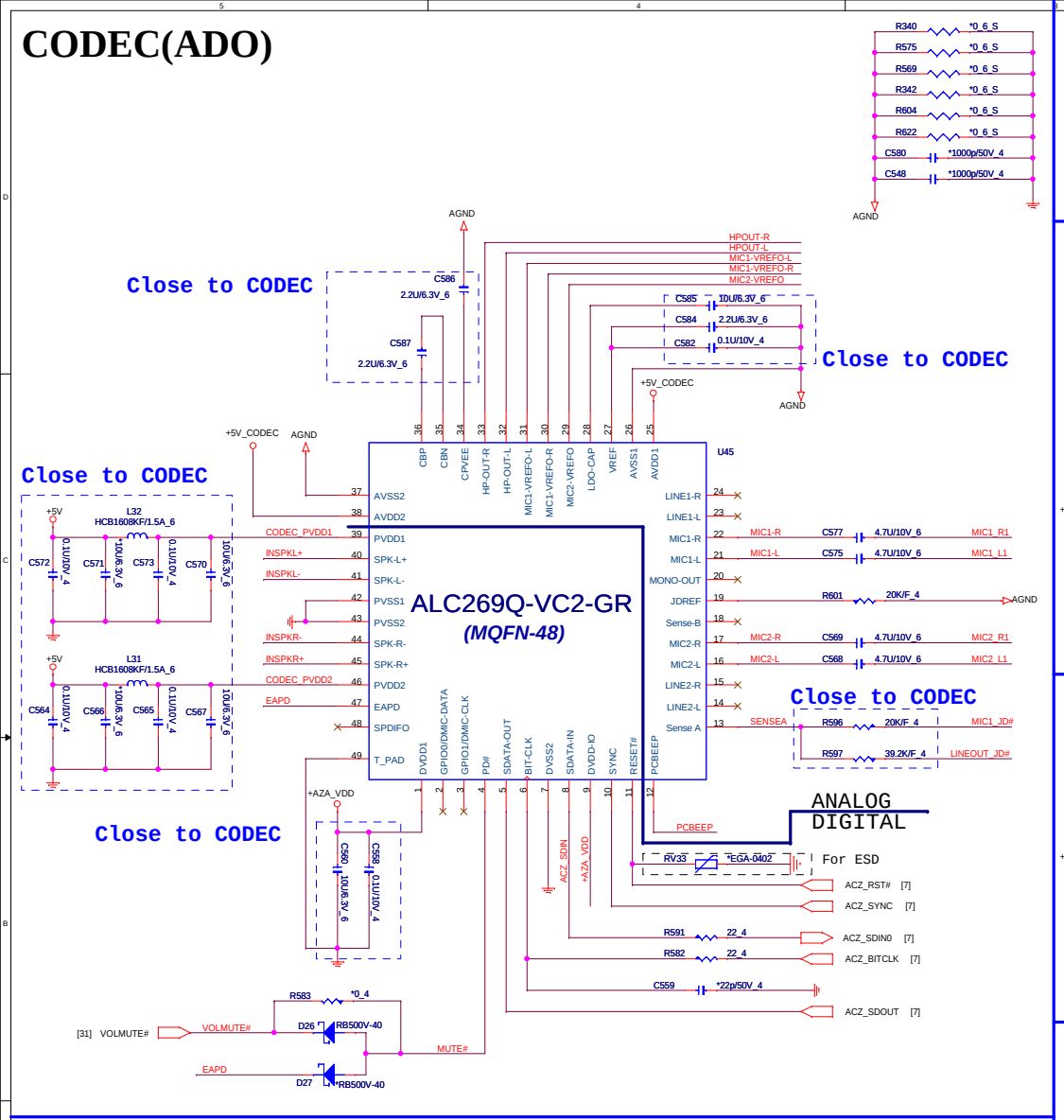




PROJECT LZ1
Quanta Computer Inc.

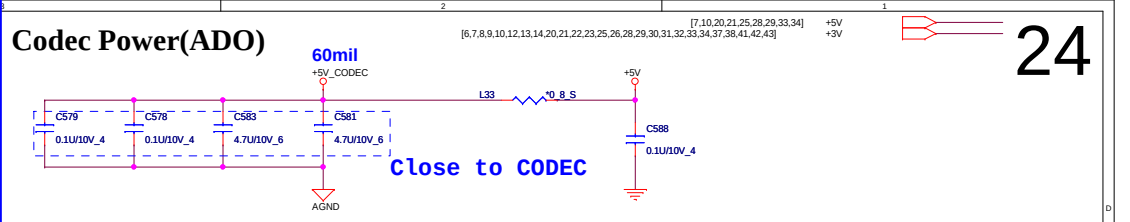
| Size | Document Number | Rev |
|---|---|---|
| Custom | RTL88105-VD-CG/RTL8111F-CG | 1B |

Date: Tuesday, January 10, 2012 Sheet 23 of 46

# CODEC(ADO)

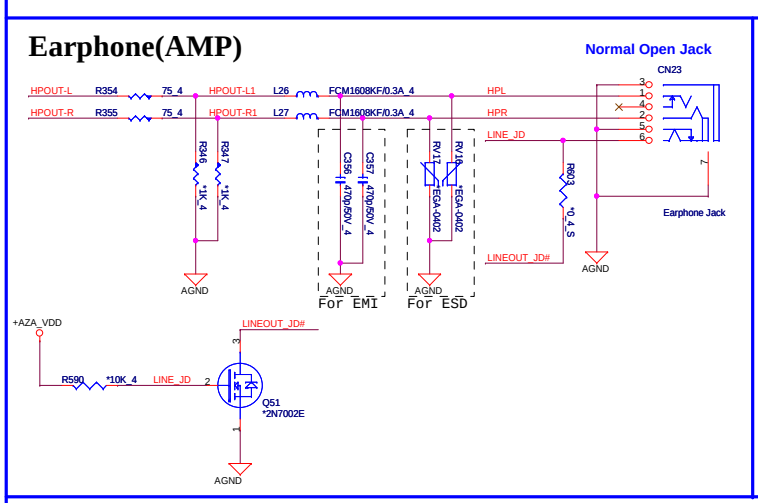



# Codec Power(ADO)



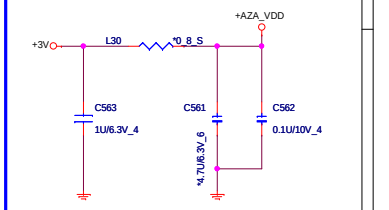

24

# Earphone(AMP)

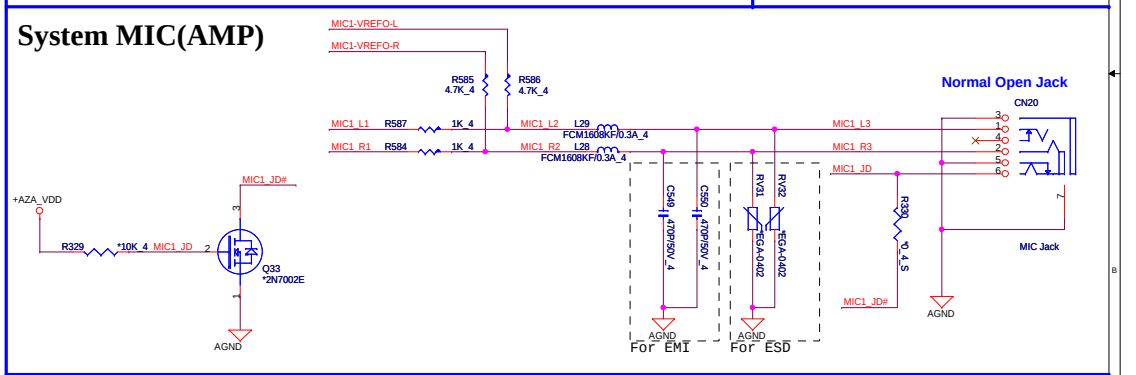



# HDA Power(ADO)

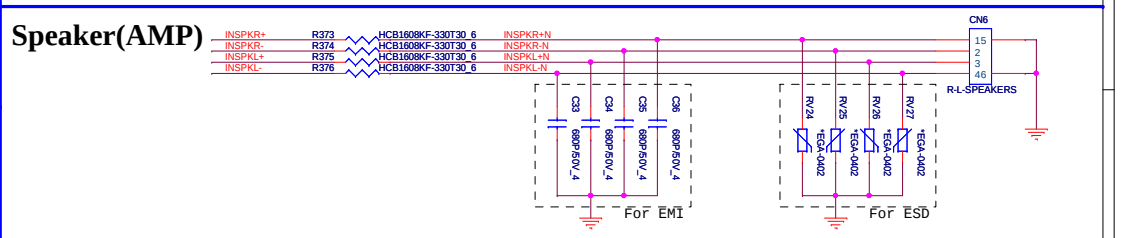
*Intel HDA Either +1.5V_S5 or +3V_S5



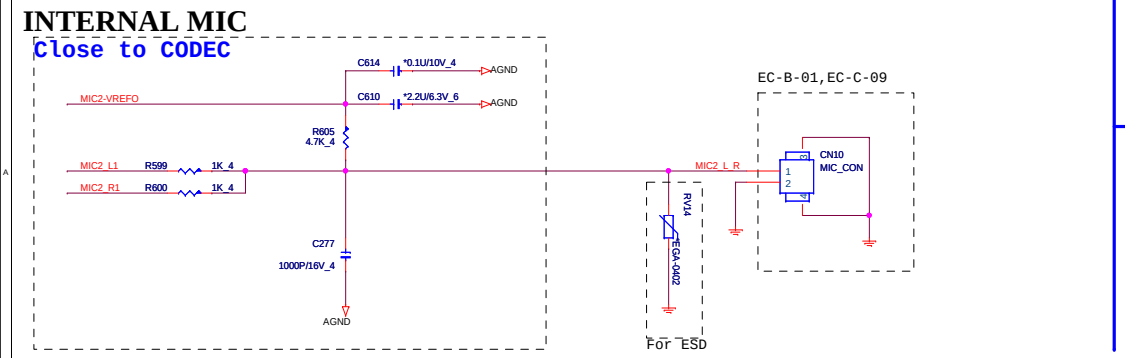

# System MIC(AMP)



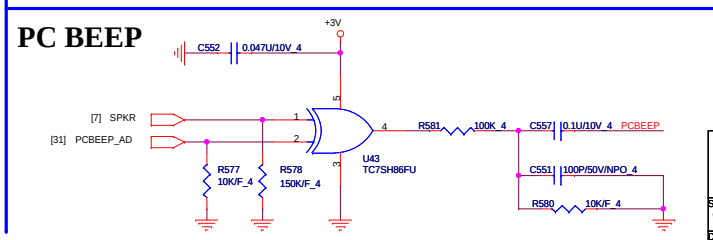

# Speaker(AMP)




# INTERNAL MIC




# PC BEEP



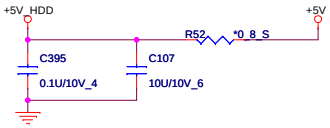

PROJECT LZ1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | ALC269/MIC/Line out | 1B |

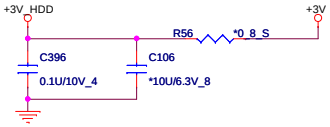
Date: Monday, January 09, 2012 Sheet 24 of 46

# SATA HDD

**HDD-->1A**
**HDD-->1.5A(burning)**

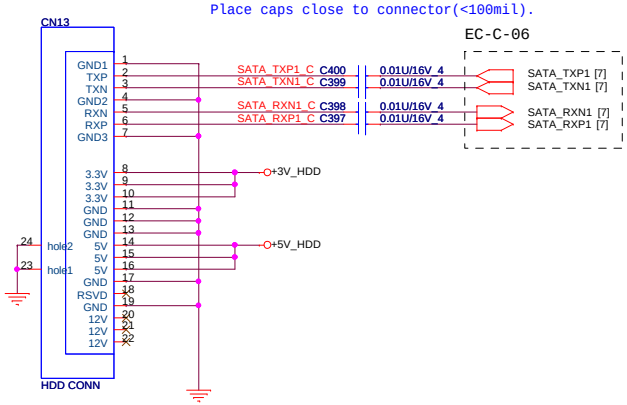



Place caps close to connector.



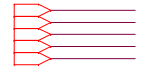

Place caps close to connector.

Place caps close to connector(<100mil).

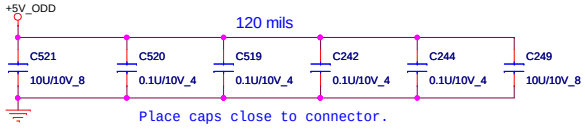



# SATA ODD

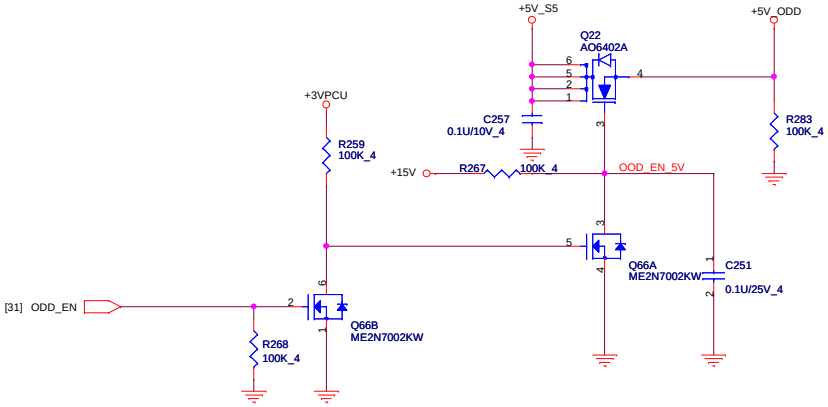
[7,10,20,21,24,28,29,33,34] +5V
[6,7,8,9,10,12,13,14,20,21,22,23,24,26,28,29,30,31,32,33,34,37,38,41,42,43] +3V
[10,22,27,33,34] +5V_S5
[6,7,22,23,26,30,31,34,35,36,40] +3VPCU
[22,29,34,36,43] +15V

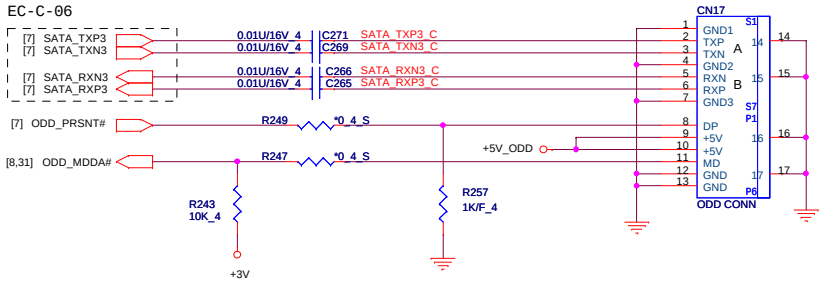






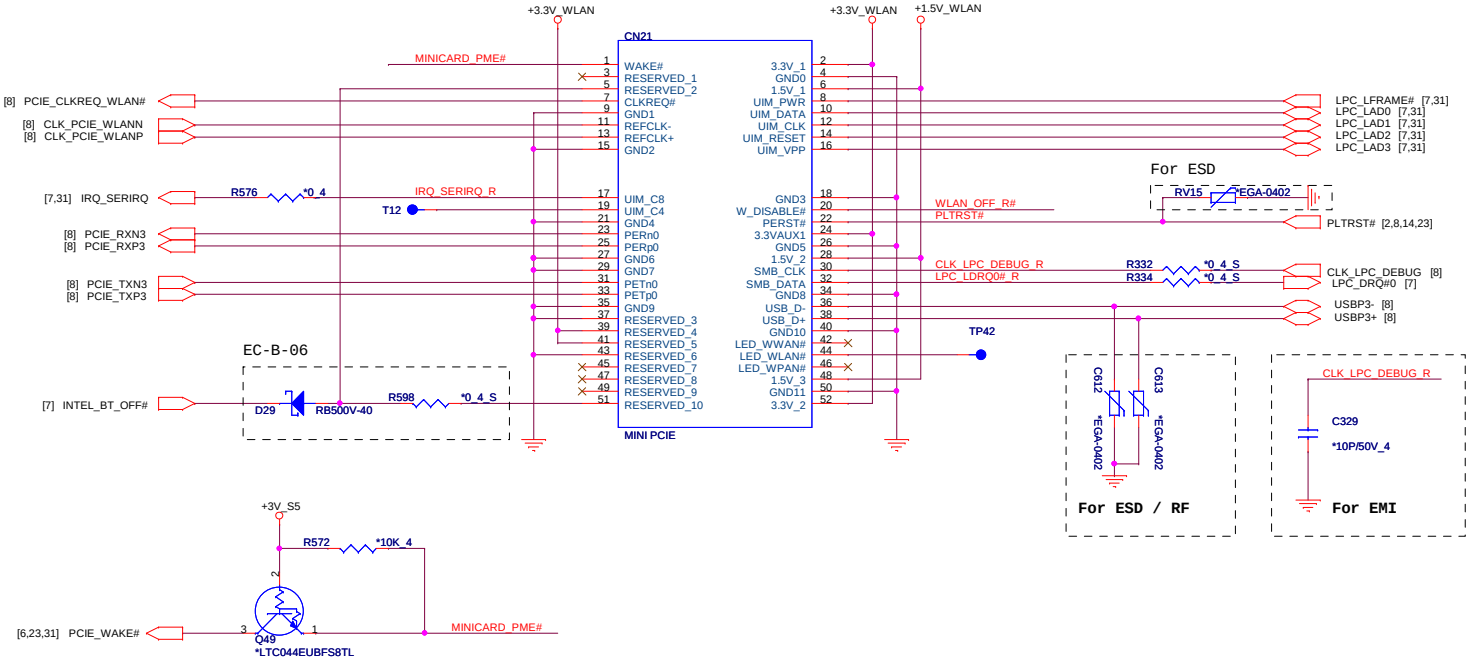

Place caps close to connector.



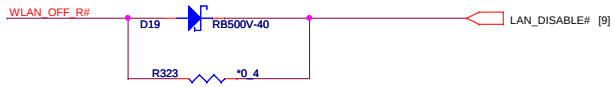

| | | |
|---|---|---|
| PROJECT LZ1 Quanta Computer Inc. | | |
| Size Custom | Document Number SATA HDD/CD-ROM | Rev 1B |
| Date: Monday, January 09, 2012 | Sheet 25 of 46 | |

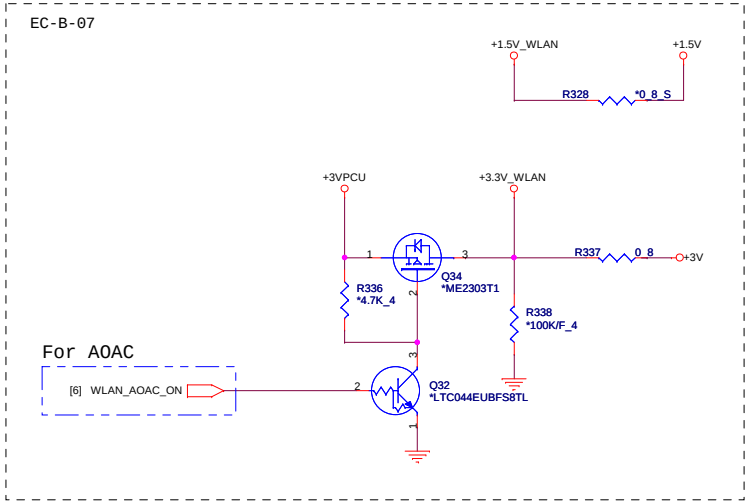
[2,6,7,8,9,10,30,34] +3V_S5
[4,10] +1.5V
[6,7,8,9,10,12,13,14,20,21,22,23,24,25,28,29,30,31,32,33,34,37,38,41,42,43] +3V

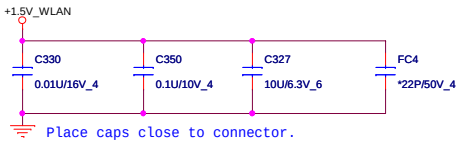


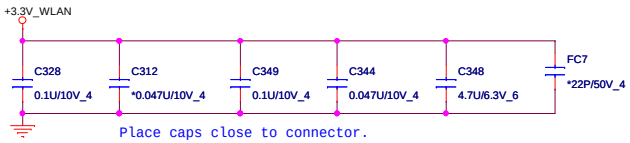






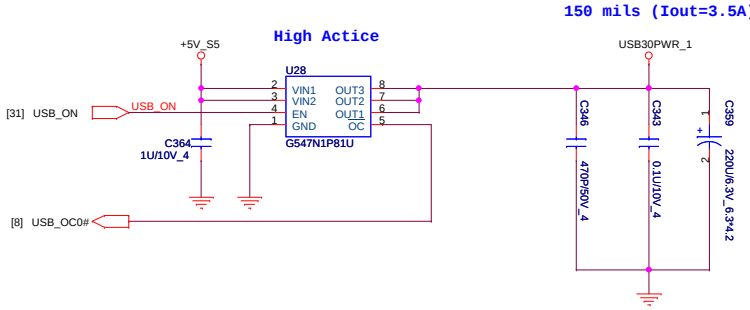

**PROJECT LZ1**
**Quanta Computer Inc.**

| Size | Document Number | Rev |
|---|---|---|
| Custom | WLAN | 1B |

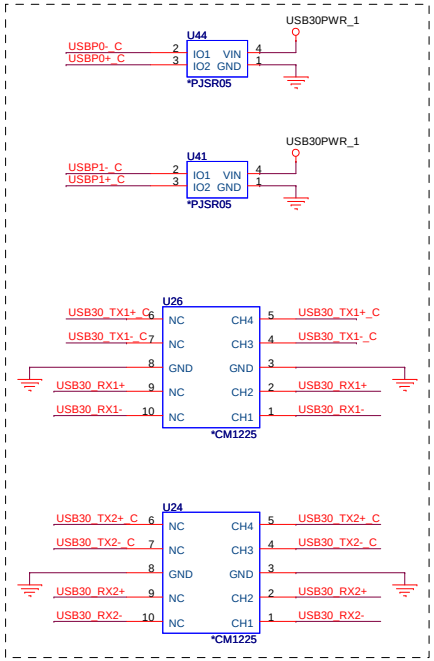
Date: Monday, January 09, 2012 Sheet 26 of 46

# USB3.0

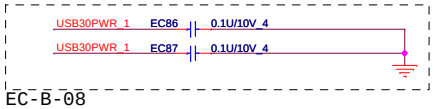
[10,22,25,33,34] +5V_S5



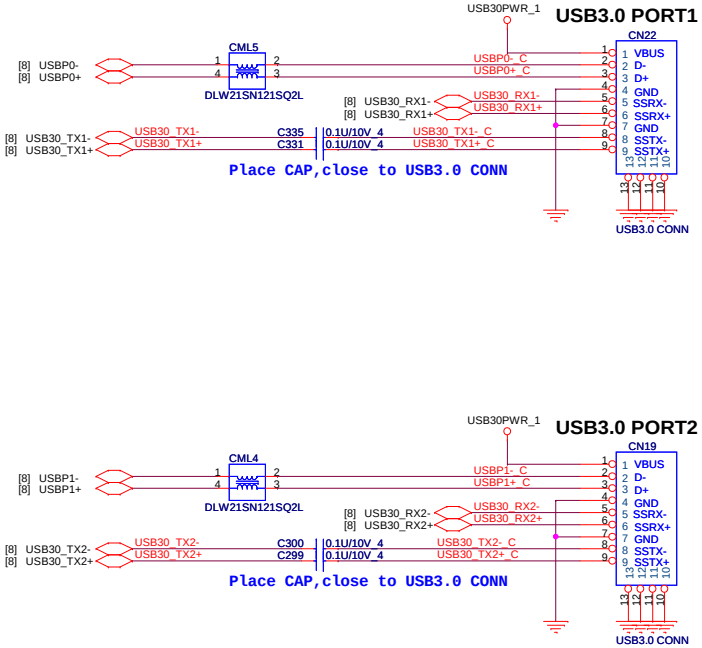

For ESD



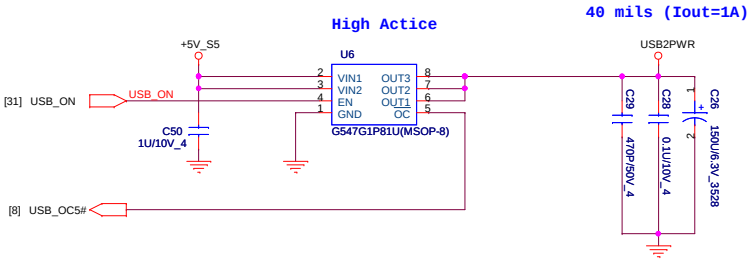

For EMI



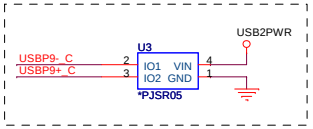

EC-B-08

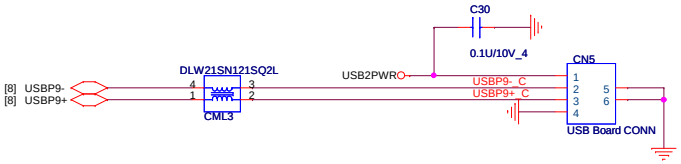



# USB 2.0 BOARD UP Right




For ESD



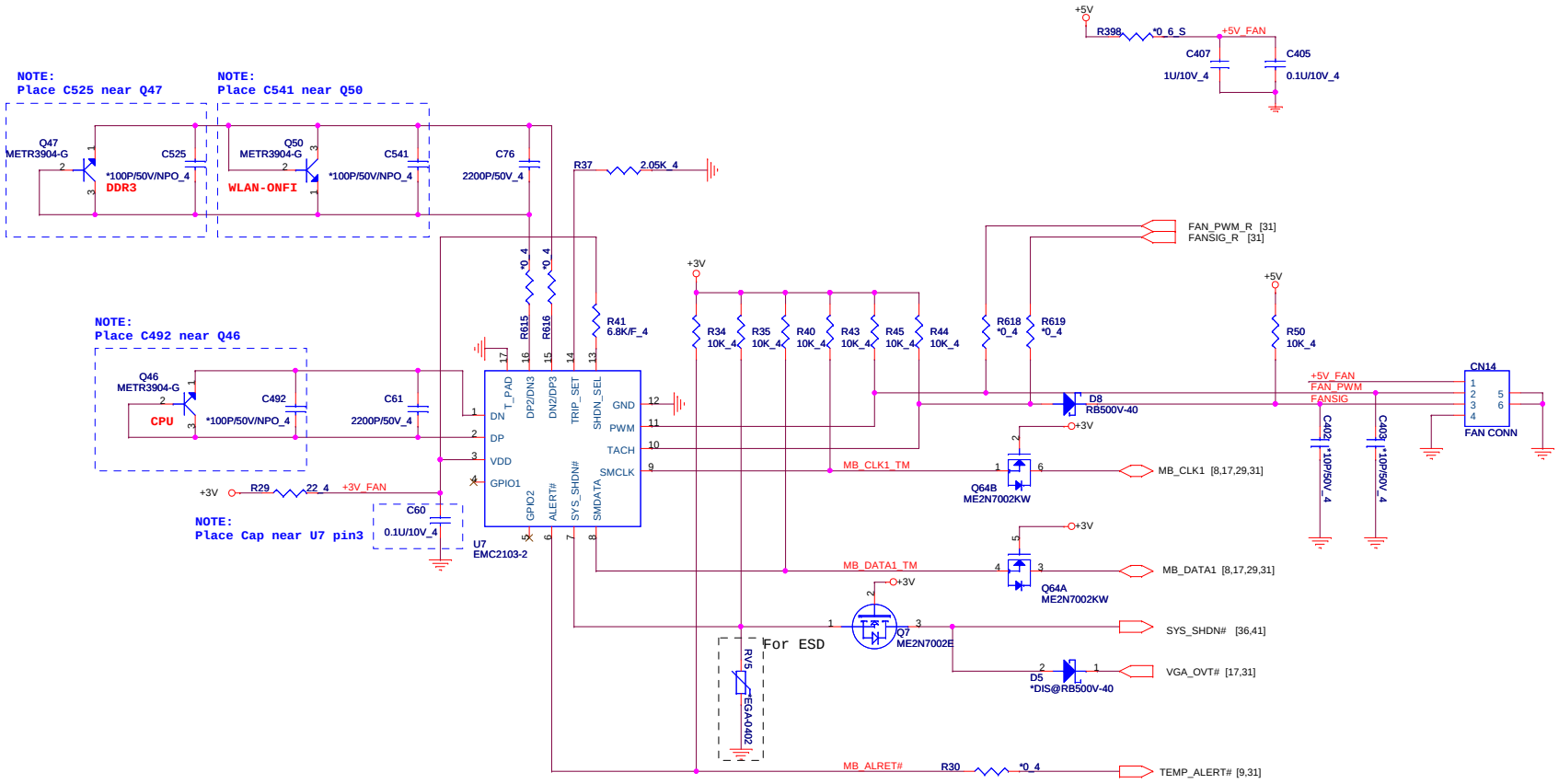




PROJECT LZ1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | USB3.0 *1/USB2.0*1 | 1B |

Date: Monday, January 09, 2012 Sheet 27 of 46

[6,7,8,9,10,12,13,14,20,21,22,23,24,25,26,29,30,31,32,33,34,37,38,41,42,43] +3V
[7,10,20,21,24,25,29,33,34] +5V

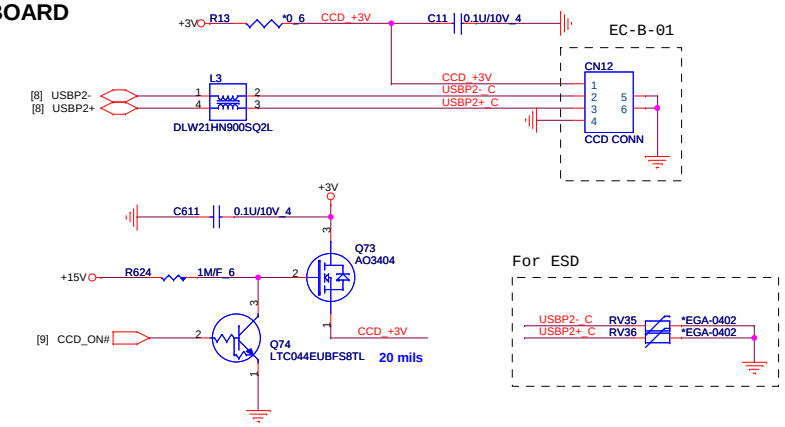



PROJECT LZ1
Quanta Computer Inc.

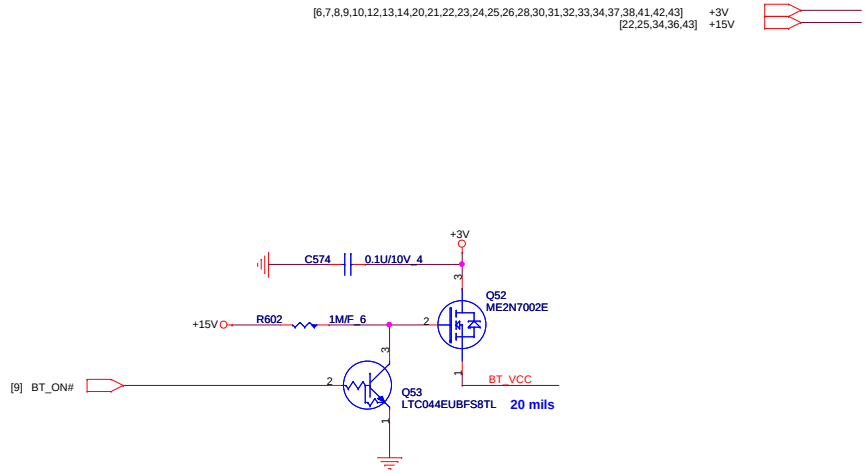
| Size | Document Number | Rev |
|---|---|---|
| Custom | FAN / THERMAL | 1B |

Date: Monday, January 09, 2012 Sheet 28 of 46

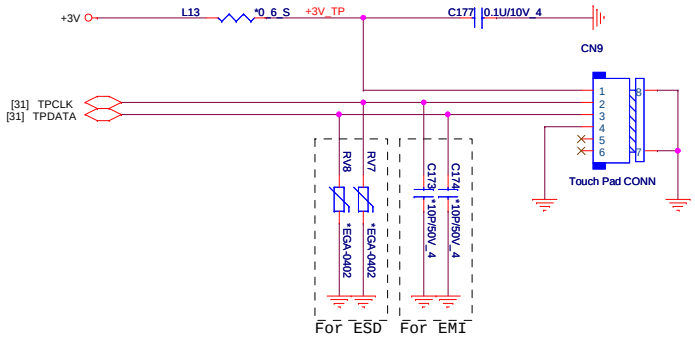
## CCD BOARD



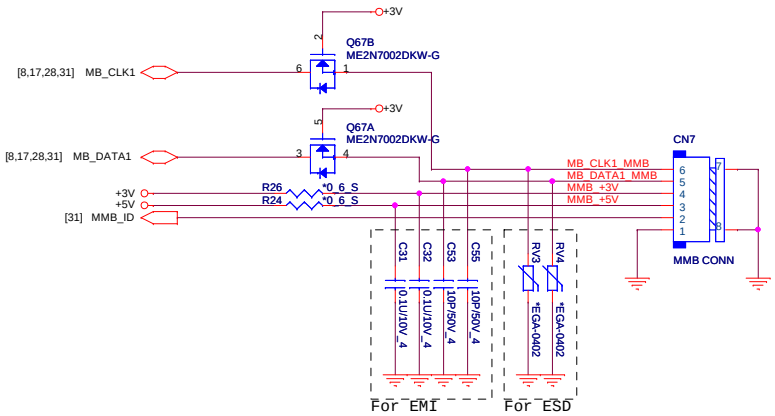

## BLUETOOTH




## Touch pad




## MMB

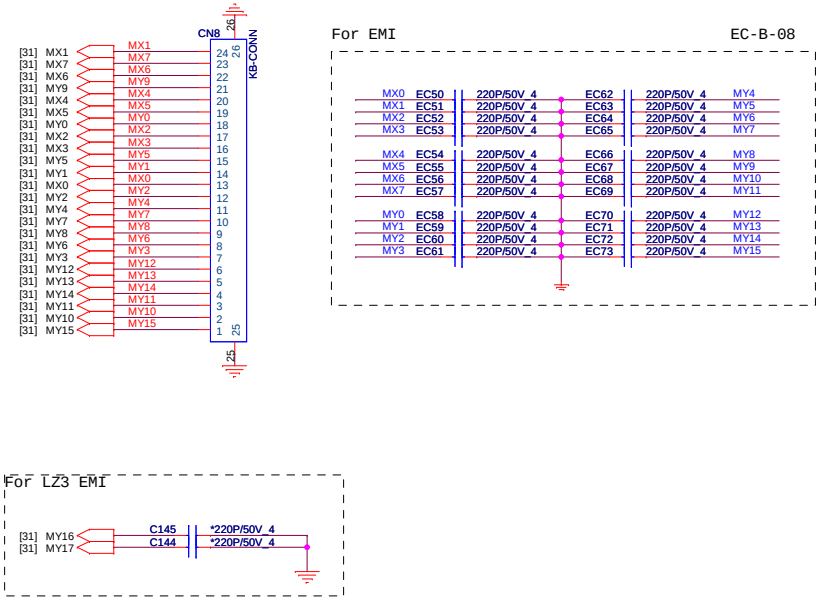



PROJECT LZ1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | CCD/TP/BT/MMB | 1B |

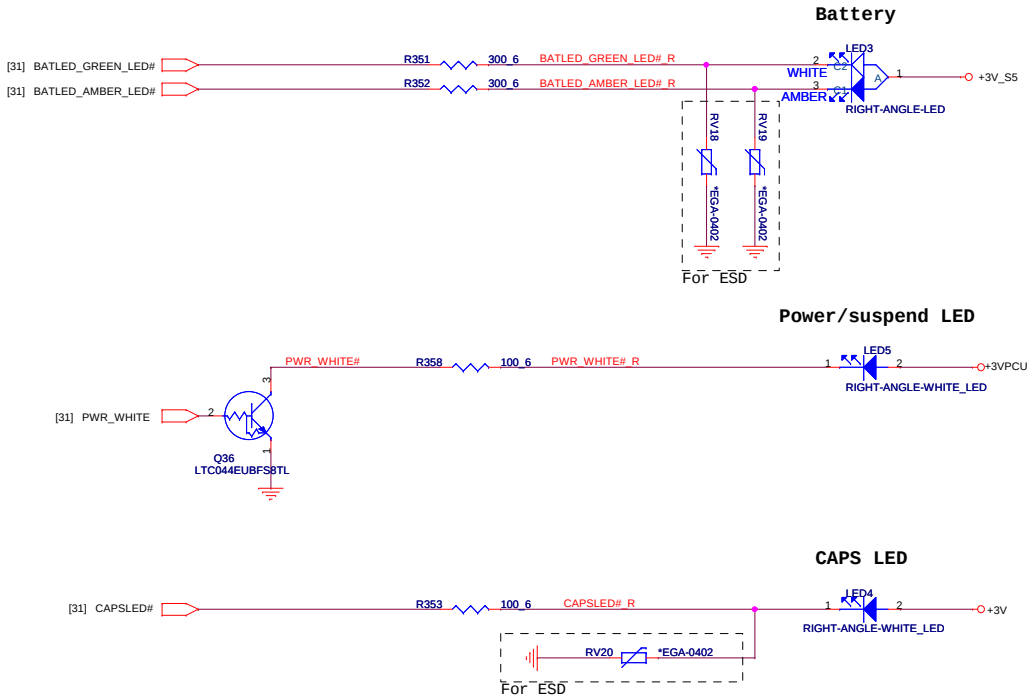
Date: Monday, January 09, 2012 Sheet 29 of 46

## KEYBOARD

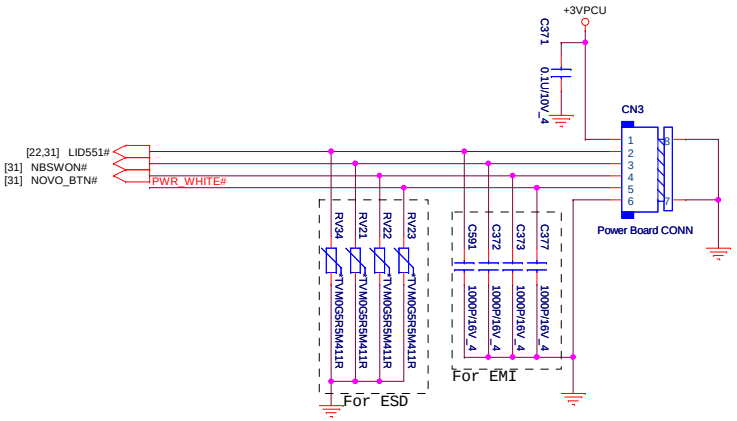



## LEDs

[6,7,22,23,25,26,31,34,35,36,40] +3VPCU
[6,7,8,9,10,12,13,14,20,21,22,23,24,25,26,28,29,31,32,33,34,37,38,41,42,43] +3V
[2,6,7,8,9,10,26,34] +3V_S5



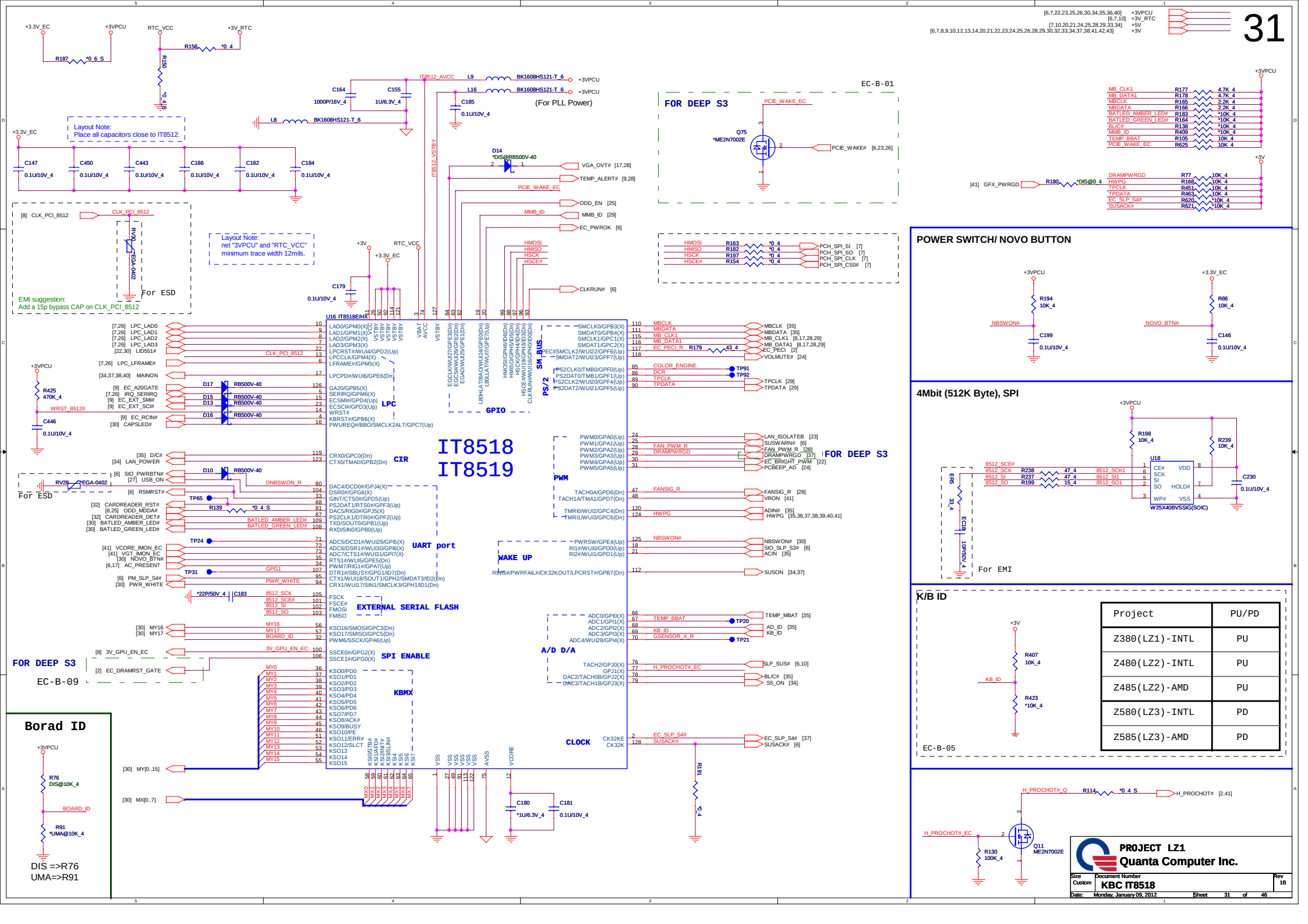

## POWER BOARD



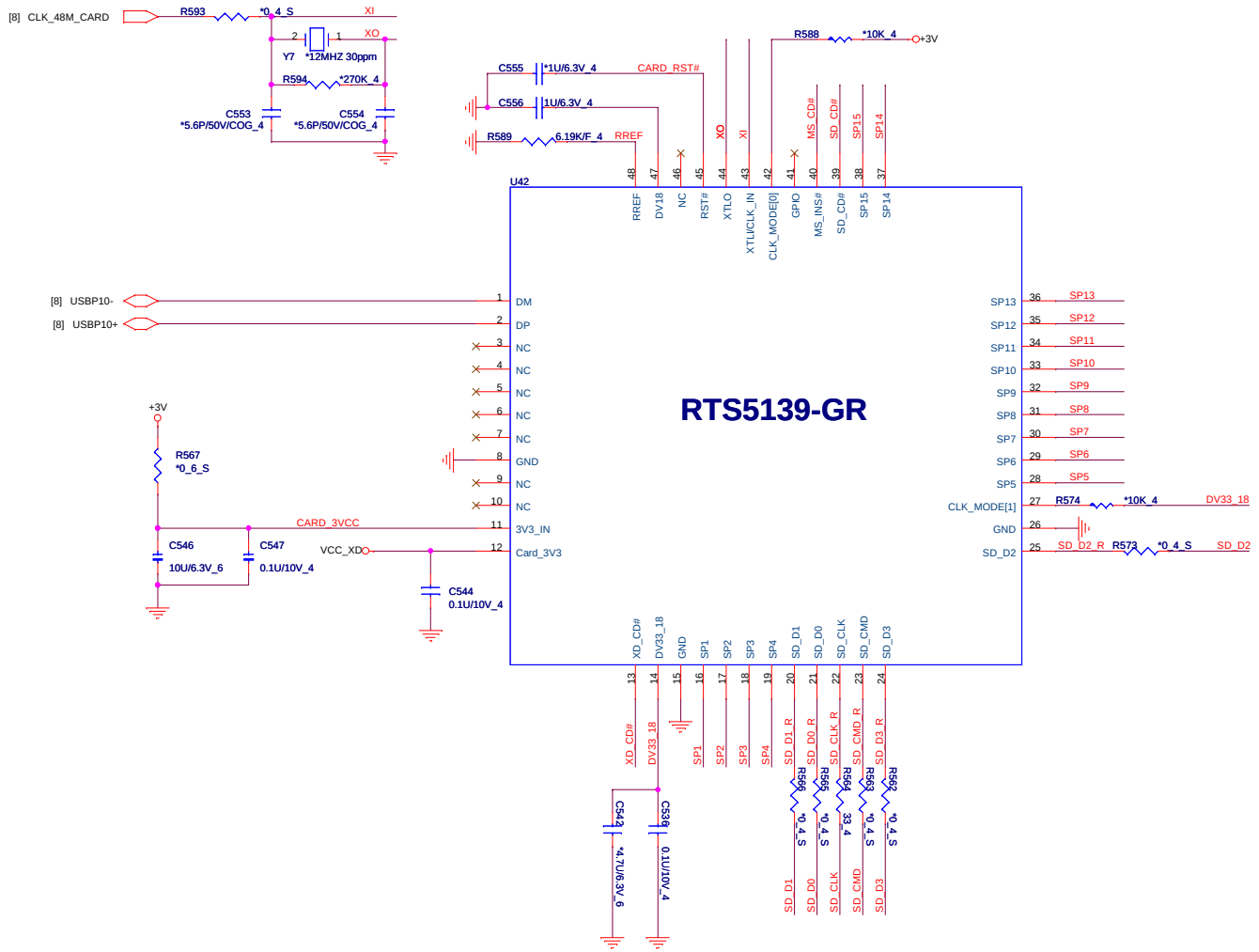

**PROJECT LZ1**
**Quanta Computer Inc.**

| Size | Document Number | Rev |
|---|---|---|
| Custom | KB/PB/LED/CRB | 1B |

Date: Monday, January 09, 2012 Sheet 30 of 46

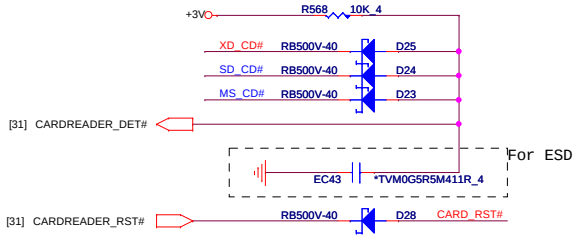



| Project | PU/PD |
|---|---|
| Z380(LZ1)-INTL | PU |
| Z480(LZ2)-INTL | PU |
| Z485(LZ2)-AMD | PU |
| Z580(LZ3)-INTL | PD |
| Z585(LZ3)-AMD | PD |

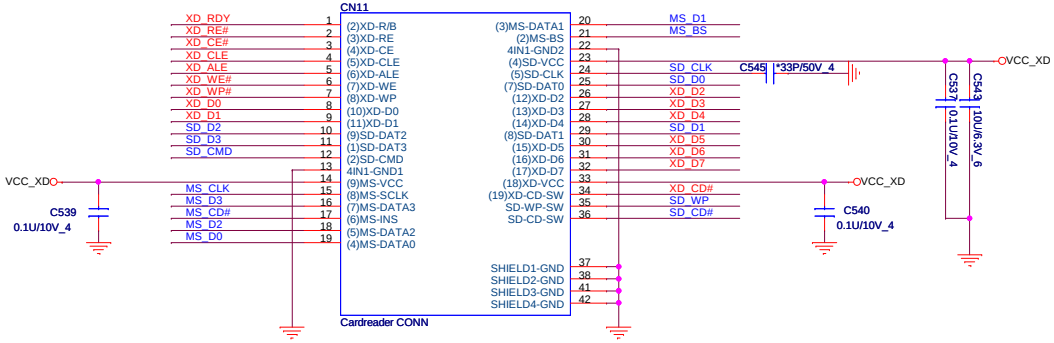



## Note:

| SD/MMC | MS | XD |
|---|---|---|
| SP1 SD_D7 | | XD_RDY |
| SP2 SD_D6 | | XD_RE# |
| SP3 SD_D5 | | XD_CE# |
| SP4 SD_D4 | | XD_WE# |
| SP5 | MS_BS | XD_CLE |
| SP6 | MS_D5 | XD_ALE |
| SP7 | MS_D1 | XD_WP# |
| SP8 | MS_D4 | XD_D0 |
| SP9 | MS_D0 | XD_D1 |
| SP10 | MS_D2 | XD_D2 |
| SP11 | MS_D6 | XD_D3 |
| SP12 | MS_D3 | XD_D4 |
| SP13 | MS_D7 | XD_D5 |
| SP14 | MS_CLK | XD_D6 |
| SP15 SD_WP | | XD_D7 |




## 7 IN1 CARD CONN
## XD,MMC/SD,MS/MSP

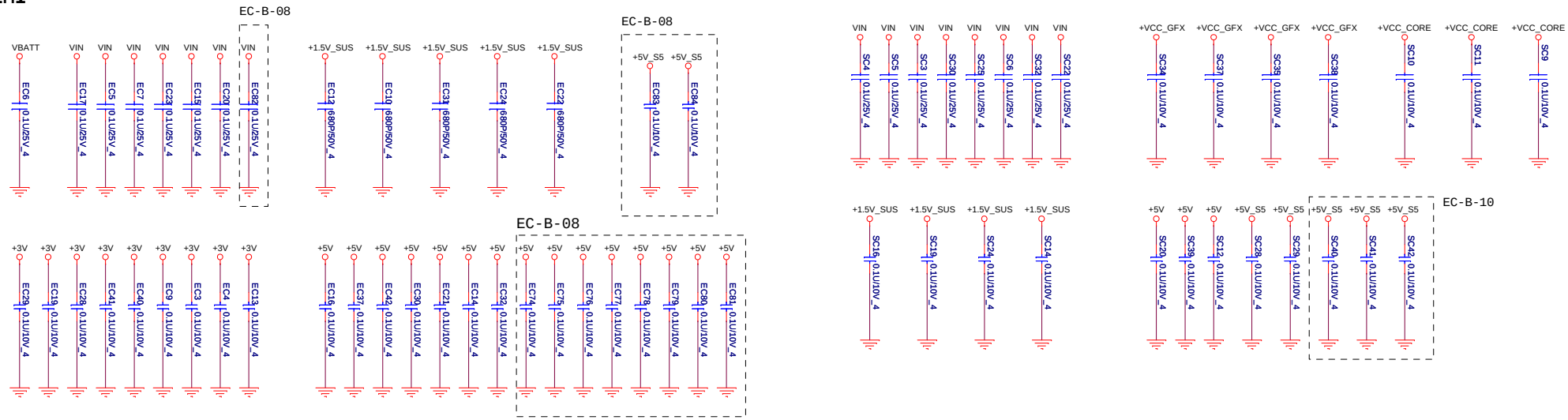



**PROJECT LZ1**
**Quanta Computer Inc.**

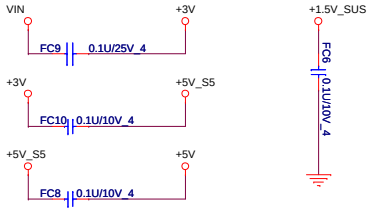
| Size | Document Number | Rev |
|---|---|---|
| Custom | Card Reader (RTS5139-GR) | 1B |

Date: Monday, January 09, 2012 Sheet 32 of 46

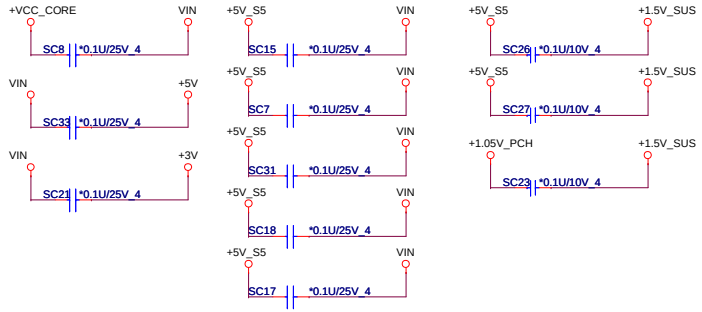
# EMI




# RF



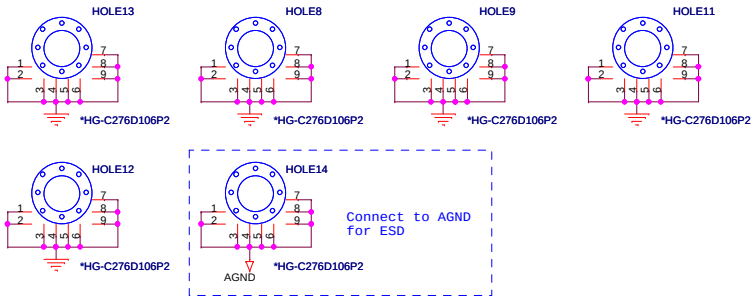

# ESD



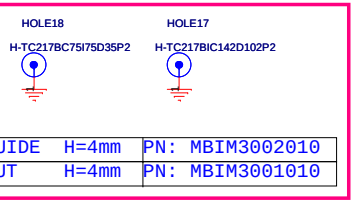

# Screw For ME

## ME-other holes

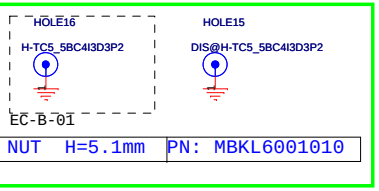
**Round screw hole(8 guard hole)*7 for ESD**

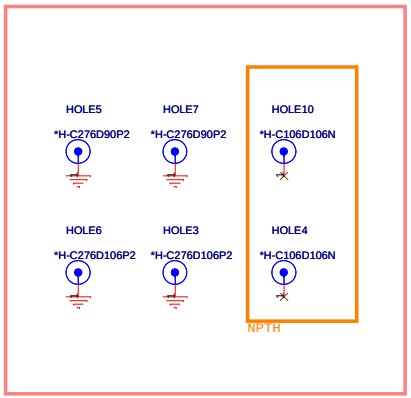



## WLAN

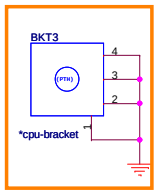



## VGA




## CPU BKT



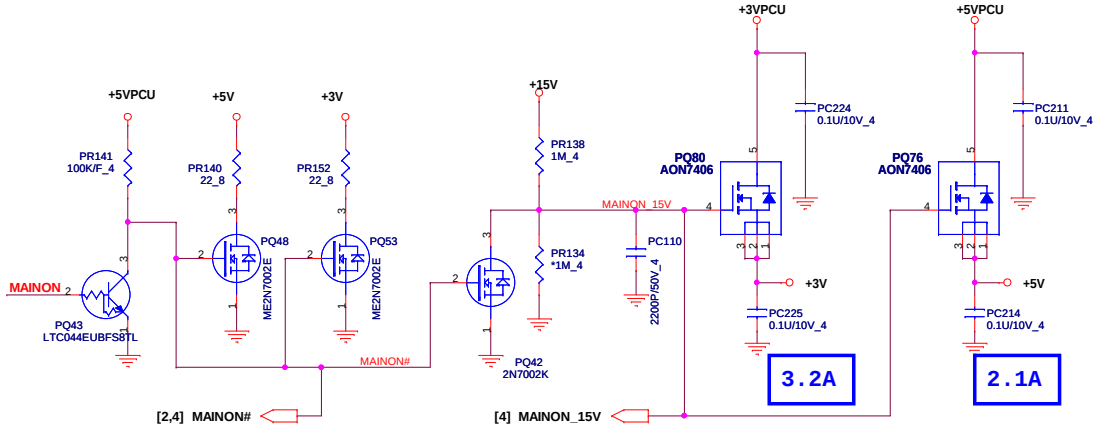

non-connect GND for ESD

**PROJECT LZ1**
**Quanta Computer Inc.**

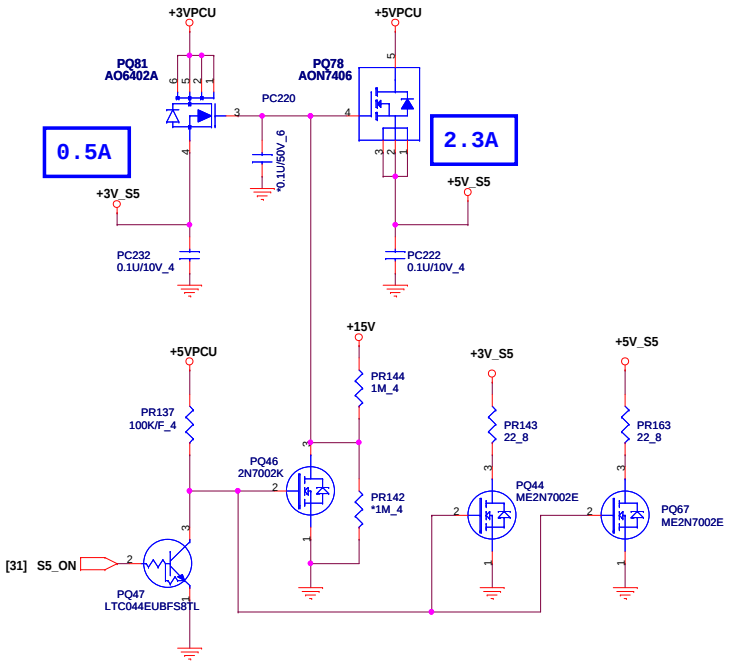
| Size | Document Number | Rev |
|---|---|---|
| Custom | HOLE &SCREW | 1B |

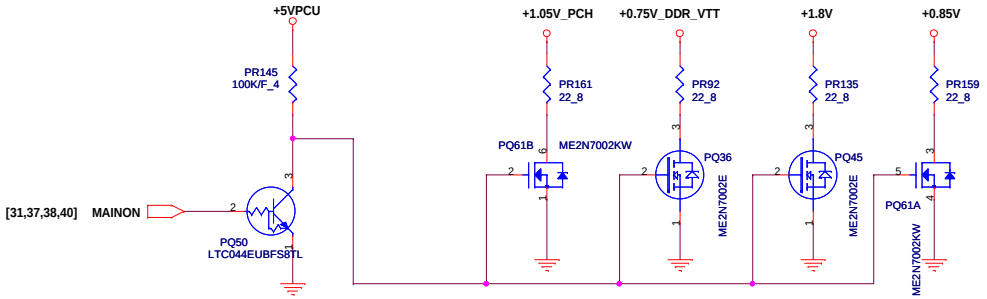
Date: Monday, January 09, 2012 Sheet 33 of 46

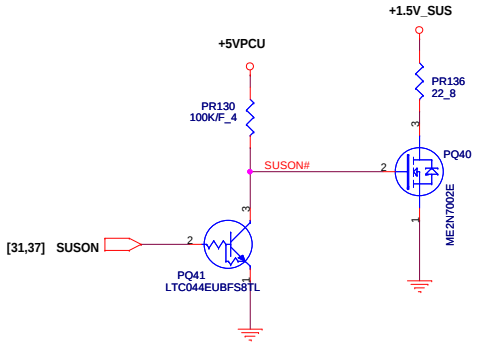
## +3V, +5V,+1.5V



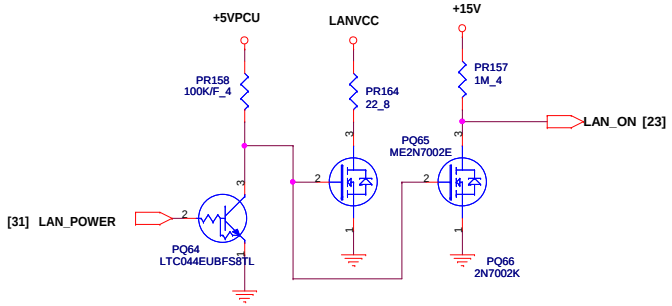

## 3V_S5, 5V_S5



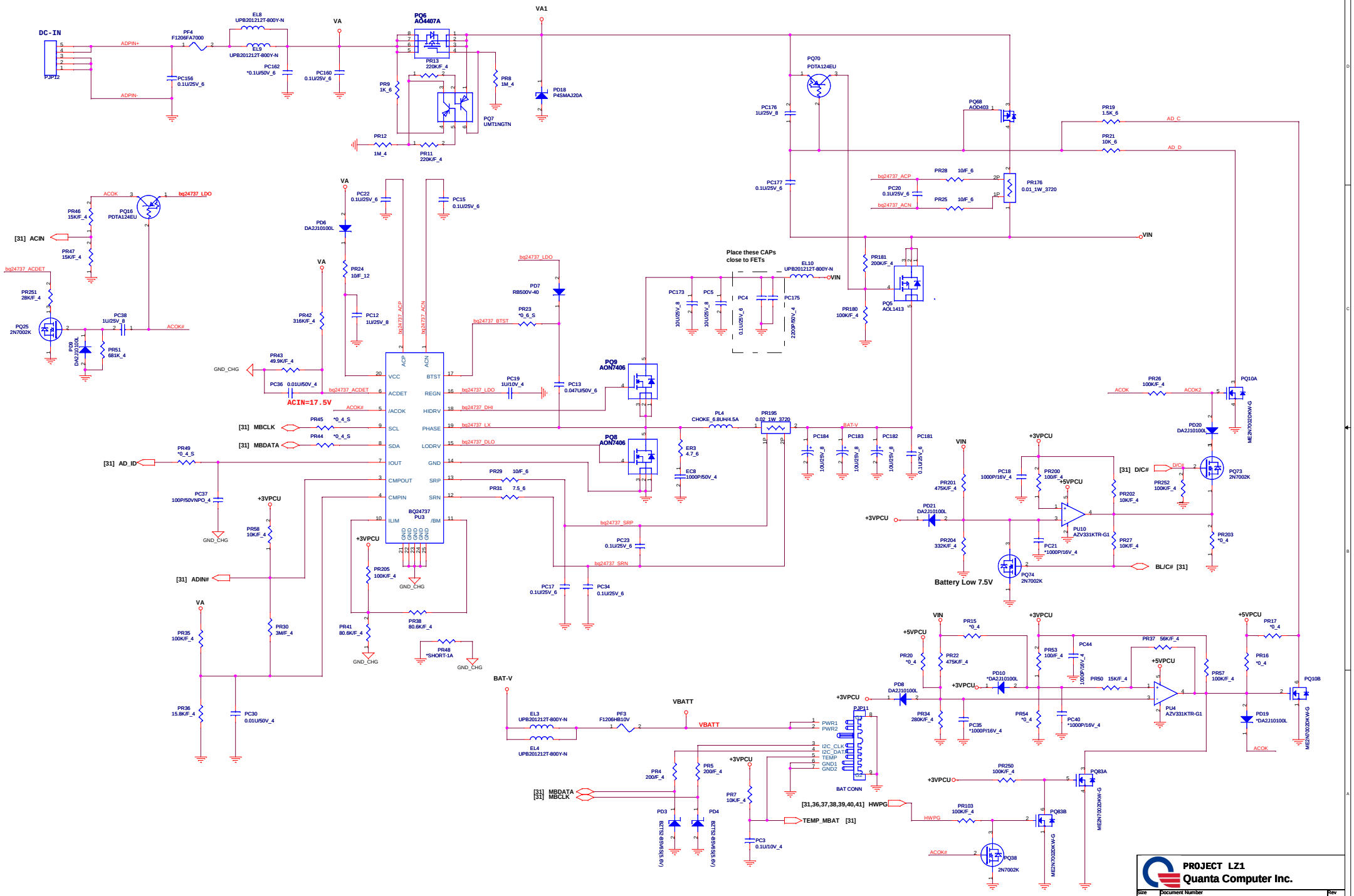




## LANVCC




PROJECT LZ1
Quanta Computer Inc.

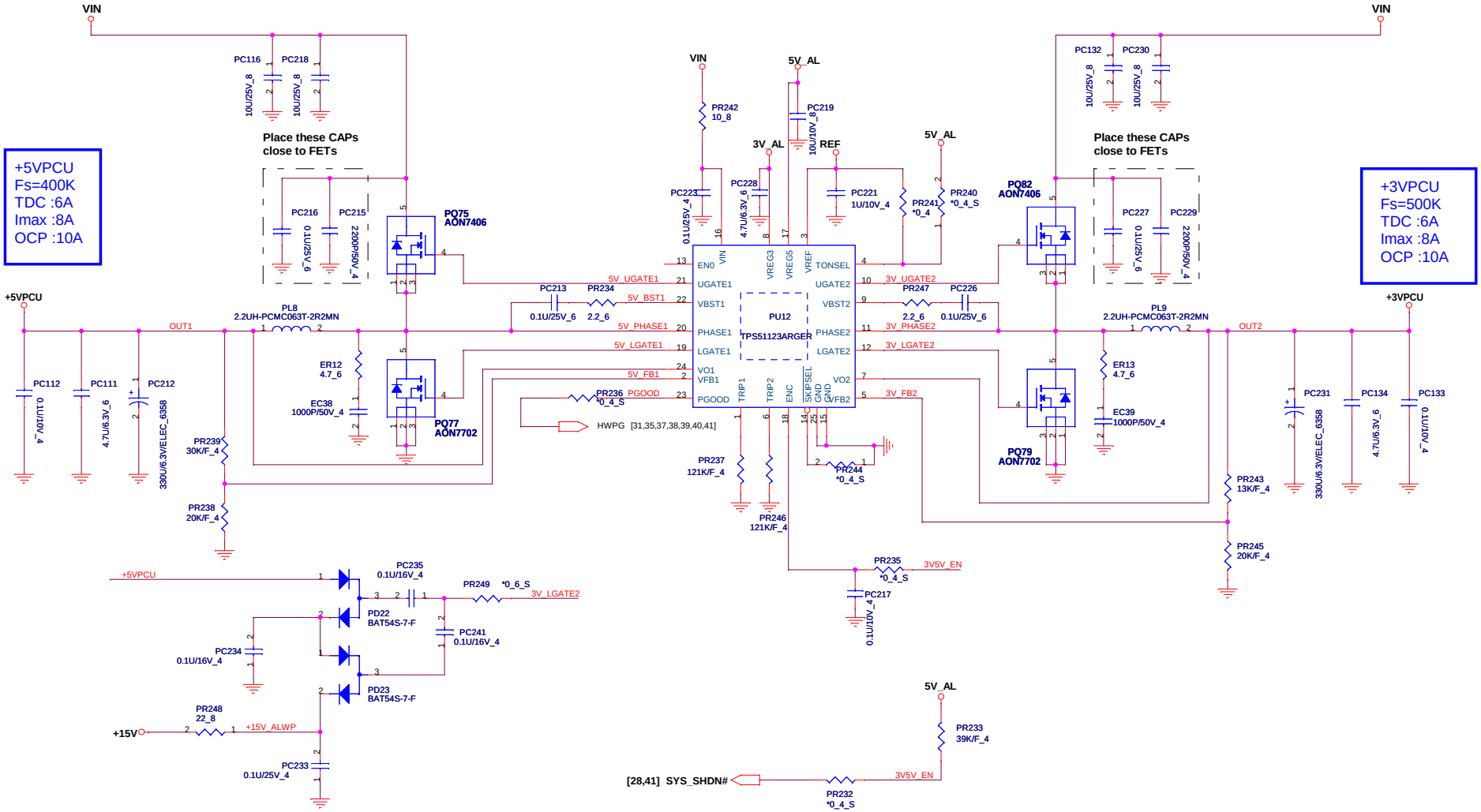
| Size | Document Number | Rev |
|---|---|---|
| | Discharge | |
| Date: Monday, January 09, 2012 | Sheet 34 of 46 | |




PROJECT LZ1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Charger (BQ24737) | 1B |

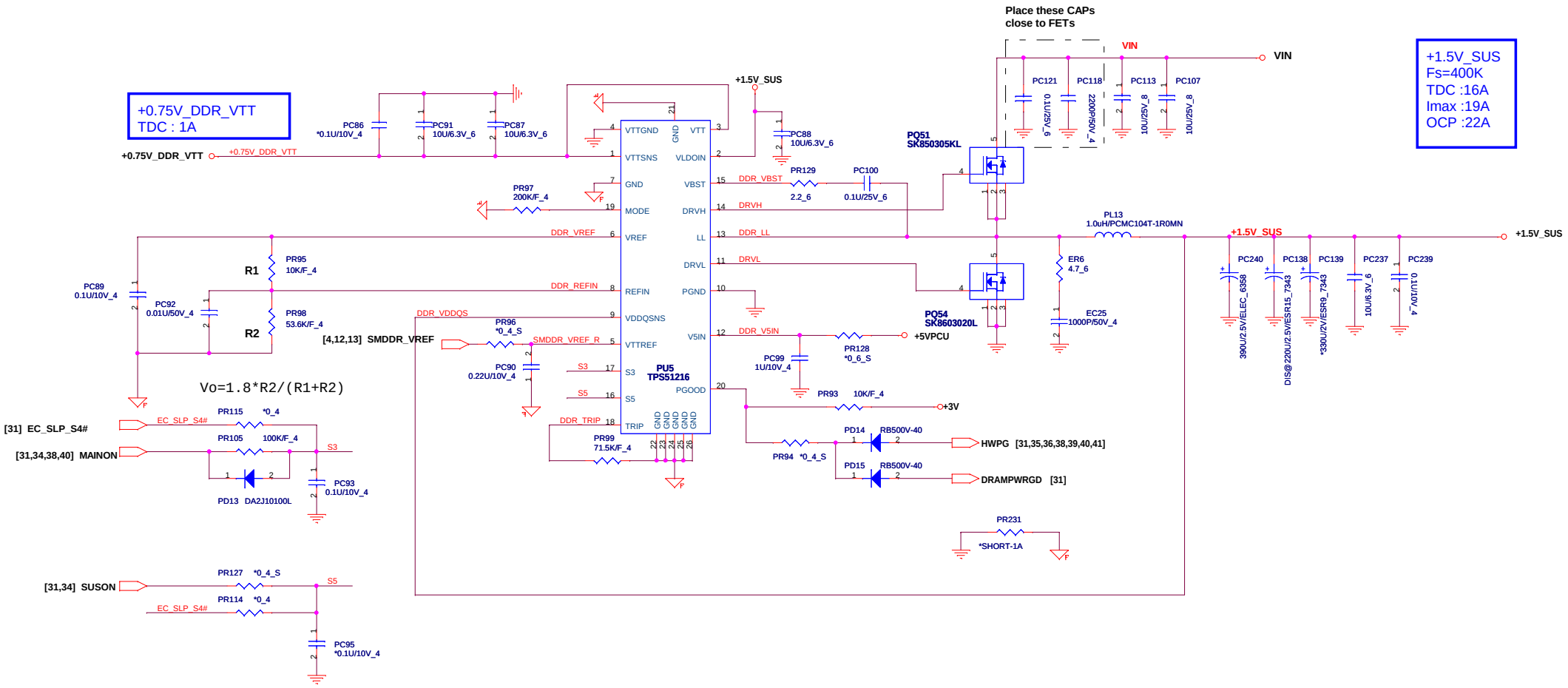
Date: Monday, January 09, 2012 Sheet 35 of 46




PROJECT LZ1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | 3V/5V (TPS51123ARGER) | 1B |

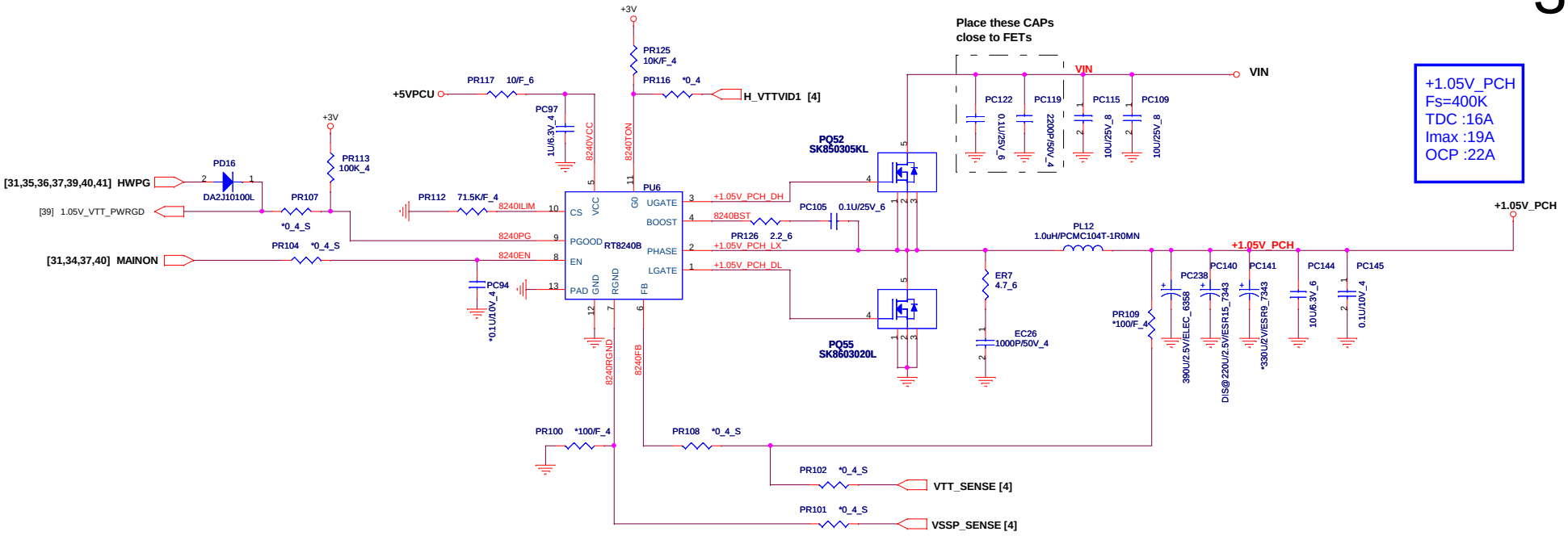
Date: Monday, January 09, 2012 Sheet 36 of 46



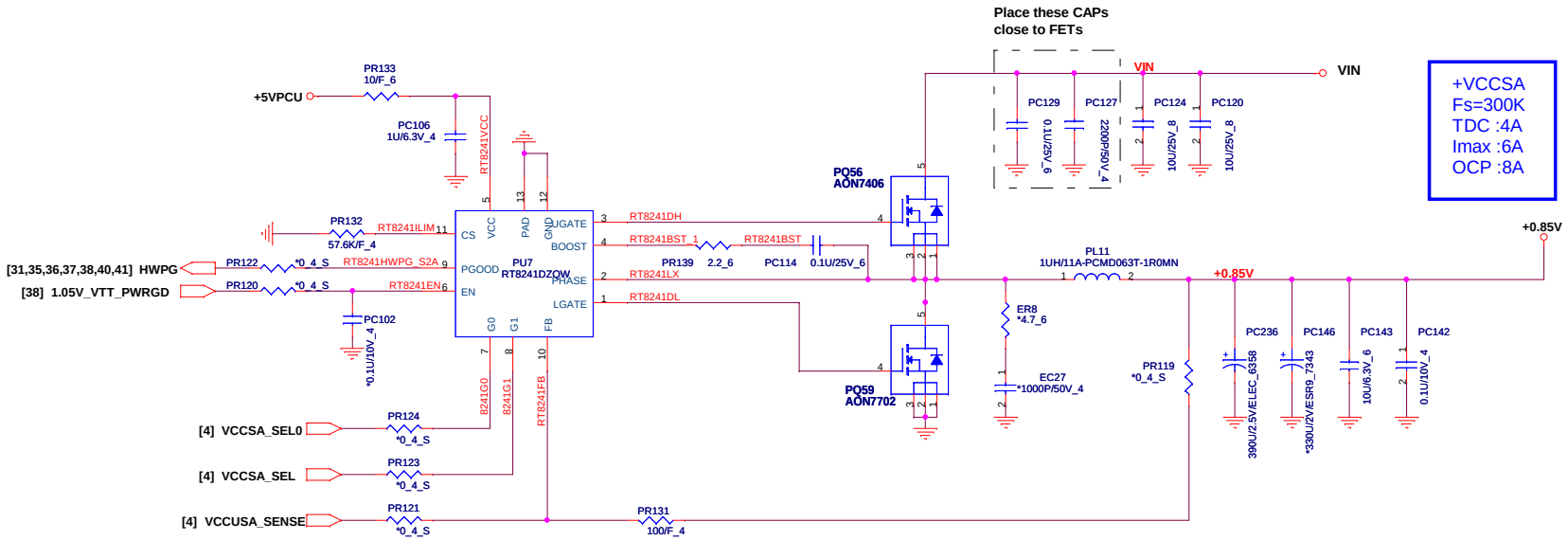

**PROJECT LZ1**
**Quanta Computer Inc.**

| Size | Document Number | Rev |
|---|---|---|
| Custom | DDR3/0.75V (TPS51216) | 1B |

Date: Monday, January 09, 2012 Sheet 37 of 46




| | |
|---|---|
| PROJECT LZ1 | |
| Quanta Computer Inc. | |
| Size: Custom | Document Number: +1.05V_VTT&+1.05V_PCH |
| Rev: 1B | |
| Date: Monday, January 09, 2012 | Sheet 38 of 46 |



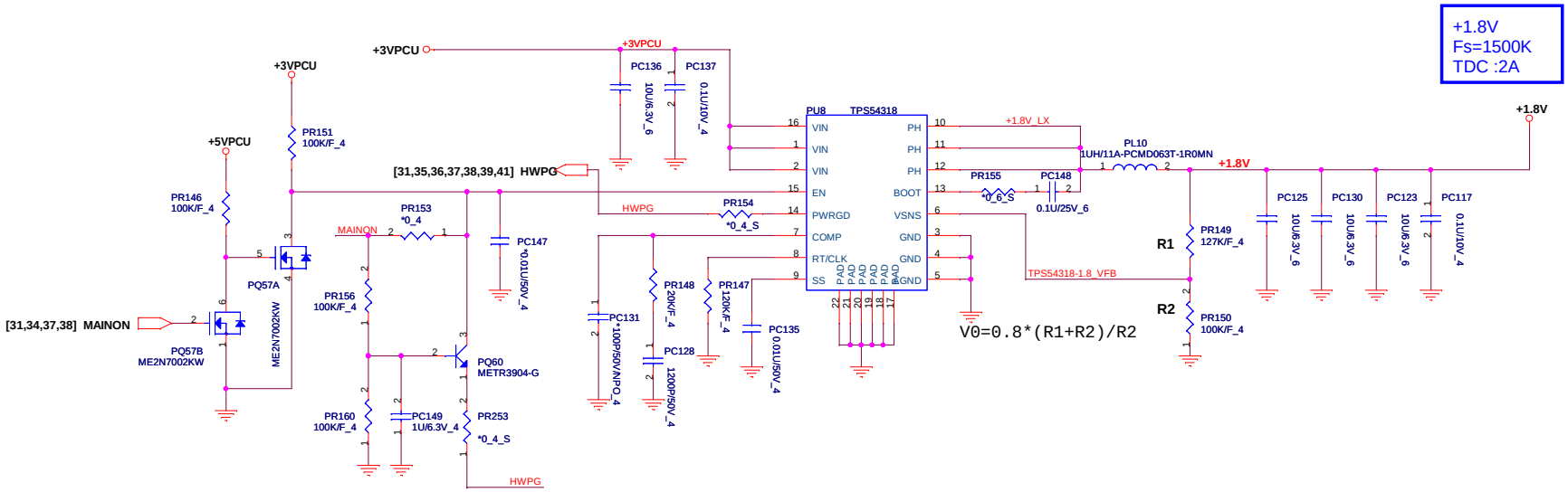

| G0 | G1 | VCCSA |
|---|---|---|
| 0 | 0 | 0.9V |
| 0 | 1 | 0.8V |
| 1 | 0 | 0.725V |
| 1 | 1 | 0.675V |

default 0.9V

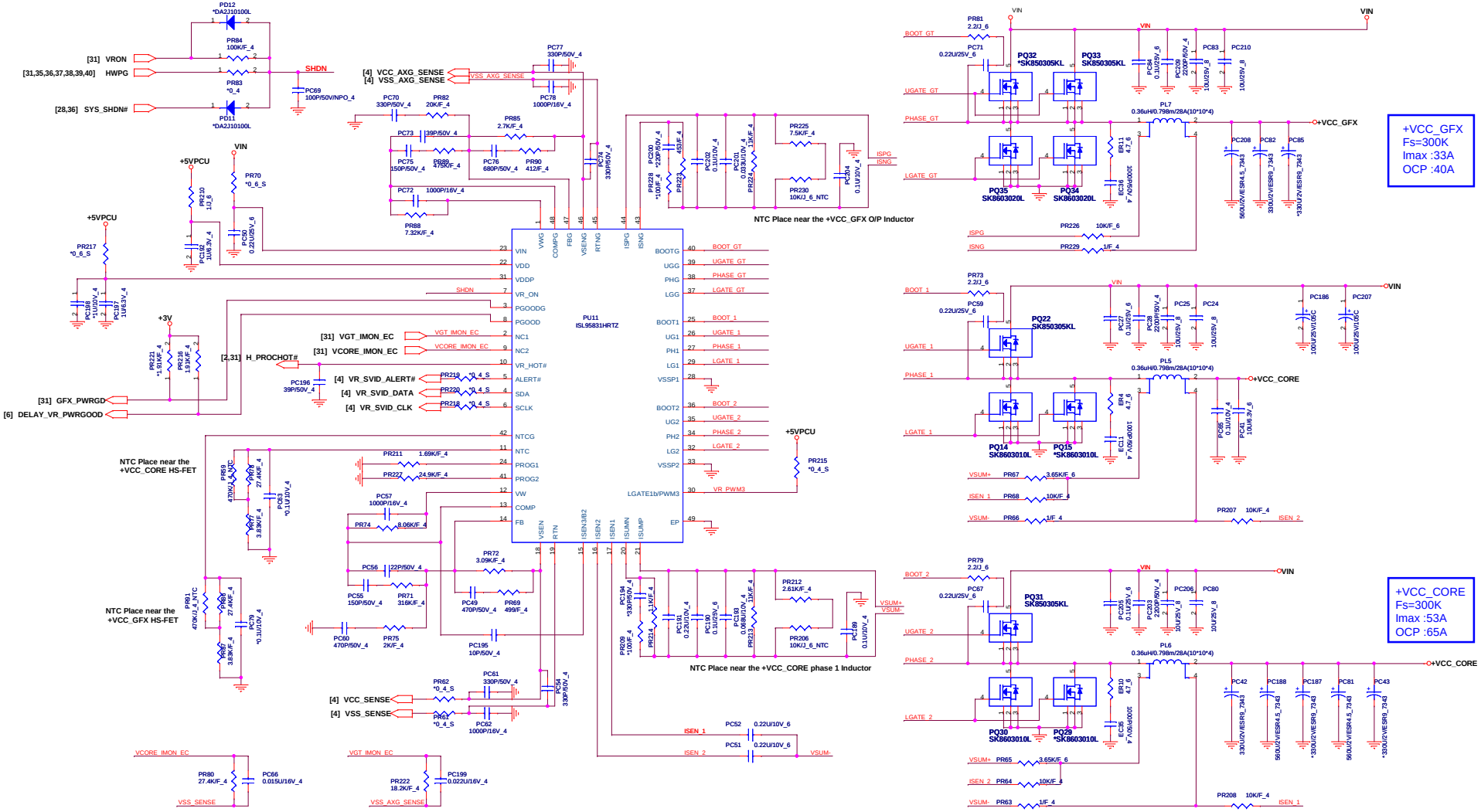
PROJECT LZ1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | VCCSA (RT8241A) | 1B |

Date: Monday, January 09, 2012 Sheet 39 of 46



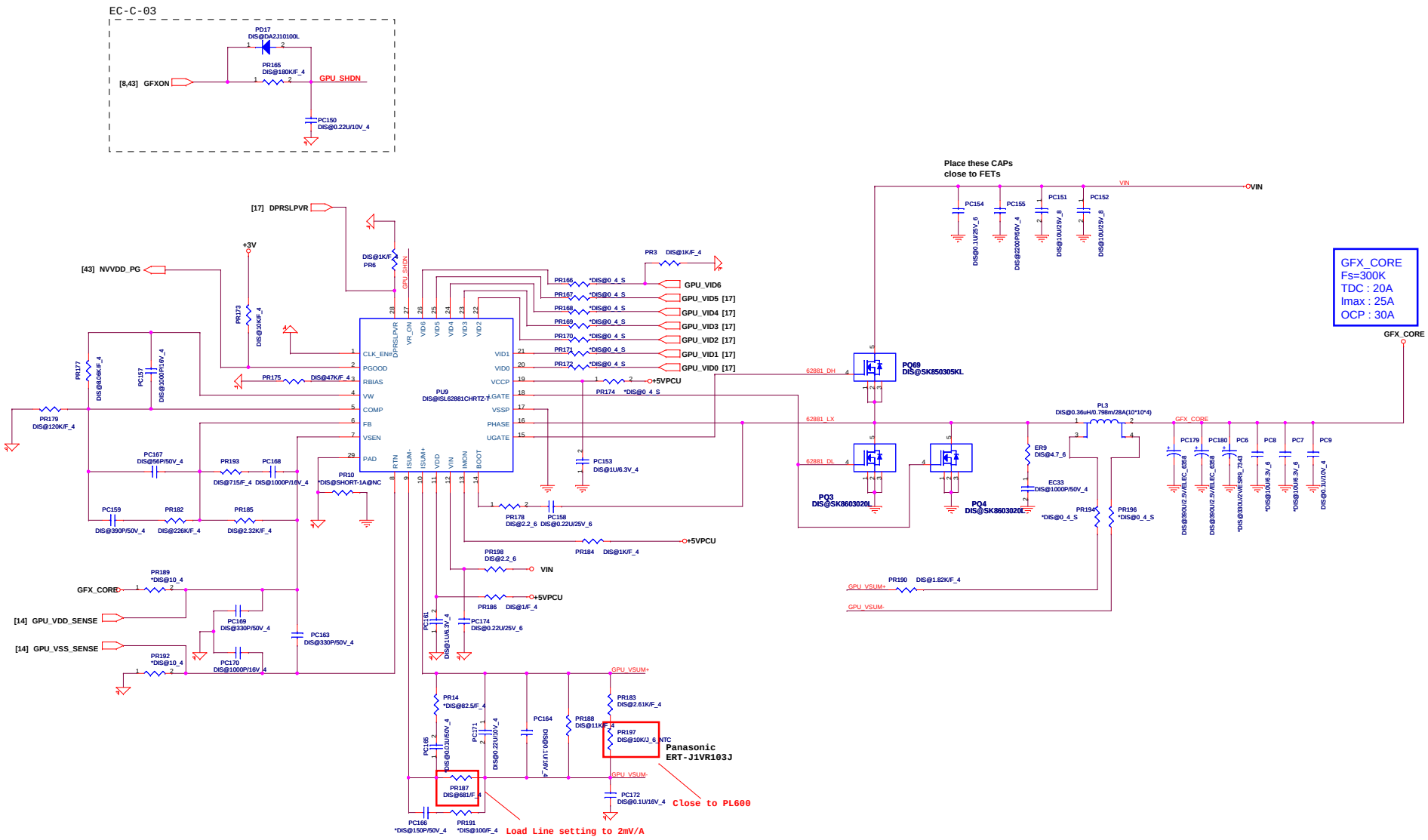

| | | |
|---|---|---|
| PROJECT LZ1 | | |
| Quanta Computer Inc. | | |
| Size: Custom | Document Number: 1.8V (TPS54318) | Rev: 1B |
| Date: Monday, January 09, 2012 | Sheet 40 of 46 | |




PROJECT LZ1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | CPU(ISL95831)IMVP2+1 | 1B |

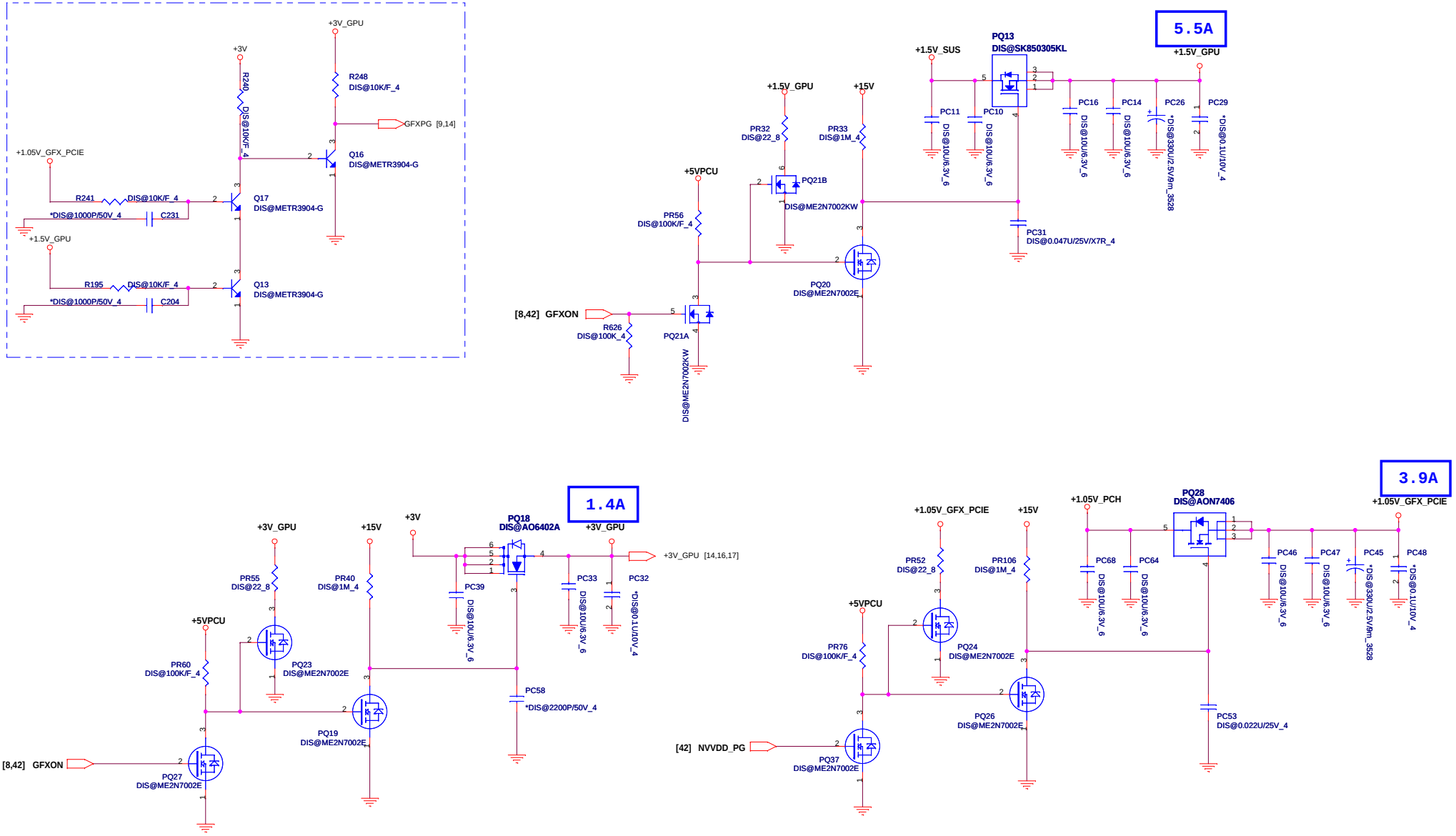
Date: Monday, January 09, 2012 Sheet 41 of 46




**PROJECT LZ1**
**Quanta Computer Inc.**

| Size | Document Number | Rev |
|---|---|---|
| Custom | DGPU (ISL62881CHRTZ-T) | 1B |

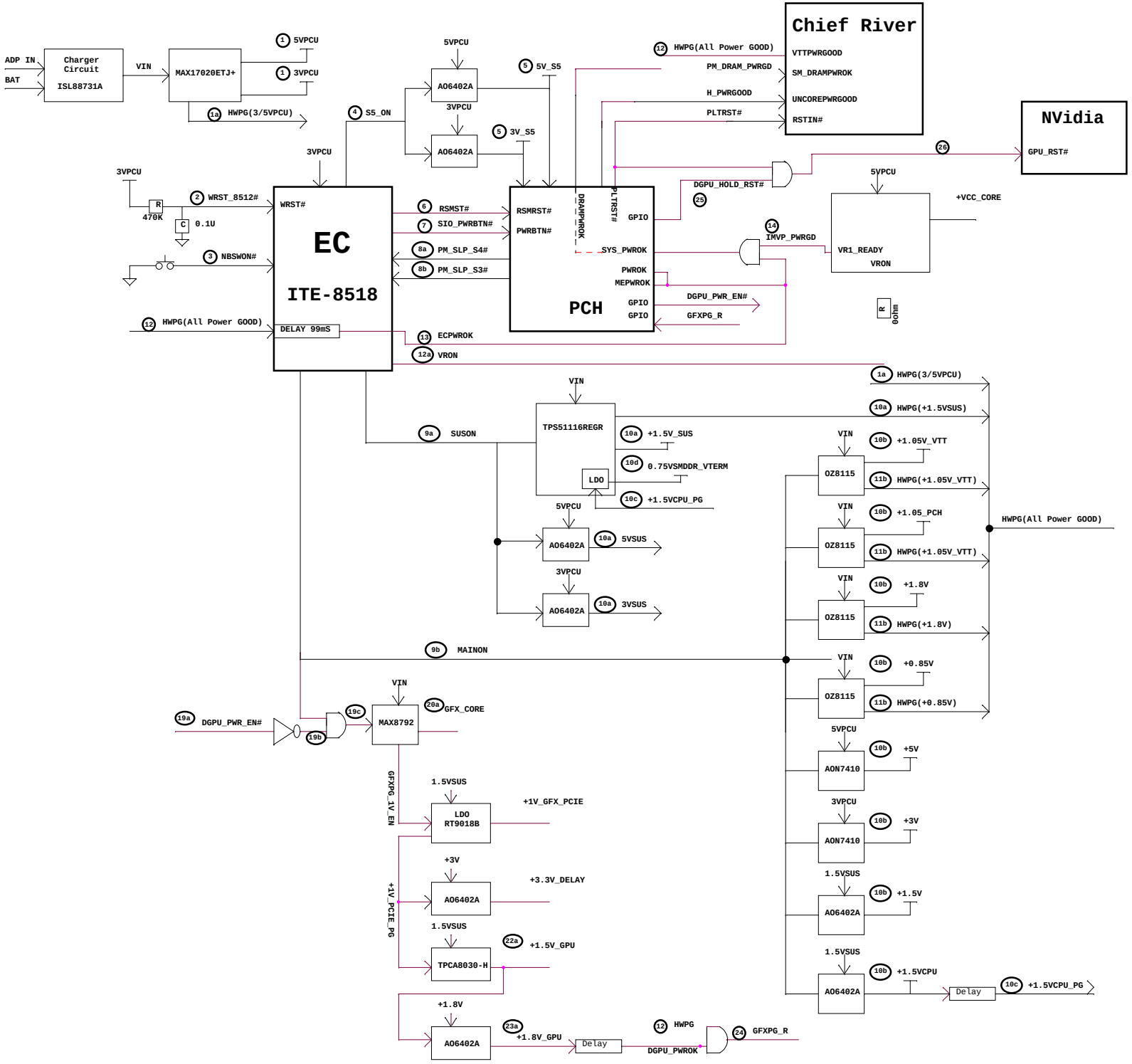
Date: Tuesday, January 10, 2012 Sheet 42 of 46




**PROJECT LZ1**
**Quanta Computer Inc.**

| Size | Document Number | Rev |
|---|---|---|
| Custom | GPU | 1B |

Date: Monday, January 09, 2012 Sheet 43 of 46




PROJECT LZ1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Power Sequence Diagram | 1B |

Date: Monday, January 09, 2012 Sheet 44 of 46

# LZ1 / Z380 Chief River Schematic EC Tracking Record B ( for SDV,A --> SIV,B )OCT. 07, 2011

| EC # | Page | Description | Date |
|---|---|---|---|
| EC-B-01 | 24 | Change INT_MIC type from DIP to Cable. | 2011.09.14A |
| | 33 | Change VGA NUT P/N type for ME request. | 2011.09.28A |
| EC-B-02 | 09 | Modify Syatem ID & Board ID. | 2011.09.19A |
| EC-B-03 | 22 | Add and reverse 6.8pf to GND for RF request. | 2011.09.20A |
| EC-B-05 | 30 | Setting K/B ID. | 2011.09.21A |
| EC-B-06 | 26 | Modify WLAN & BT COMBO function. | 2011.09.22A |
| EC-B-07 | 26 | Modify AOAC function. | 2011.09.22A |
| EC-B-08 | 20,23,27,30,33 | Add and reverse 0.1uf to GND for EMI Request. | 2011.09.22A |
| EC-B-09 | 2,6,7,10,31 | Add and reverse some material for Deep S3 function. | 2011.09.23A |
| EC-B-10 | 33 | Reverse 0.1uf to GND for ESD Request. | 2011.09.25A |
| EC-B-11 | 28,31 | Change and reverse FAN control from EC . | 2011.09.29A |

## LZ1 / Z380 Chief River Schematic EC Tracking Record B ( for SIV,B --> SIT1,C1 )NOV. 07, 2011

| EC # | Page | Description | Date |
|---|---|---|---|
| EC-B-01 | 2,7,10,12,13,31 | Modify schematoc for Deep S3 function. | 2011.11.07A |
| EC-B-02 | 09 | Modify Board ID. | 2011.11.16A |
| EC-B-03 | 42,43 | Tune GPU Sequence from Nvidia request. | 2011.11.17A |
| EC-B-05 | 12,22 | Add 3.3pf & 6.8pf to GND For RF Request. | 2011.11.17B |
| EC-B-06 | 7,8 | Modify schematic for support HM70. | 2011.11.28A |
| EC-B-07 | 23 | Change Transformer type for 家電下鄉surge. | 2011.11.28A |
| EC-B-08 | 22 | Modify brightness control from EC or PCH. | 2011.11.28A |
| EC-B-09 | 24 | Change INT_MIC footprint. | 2011.11.28A |