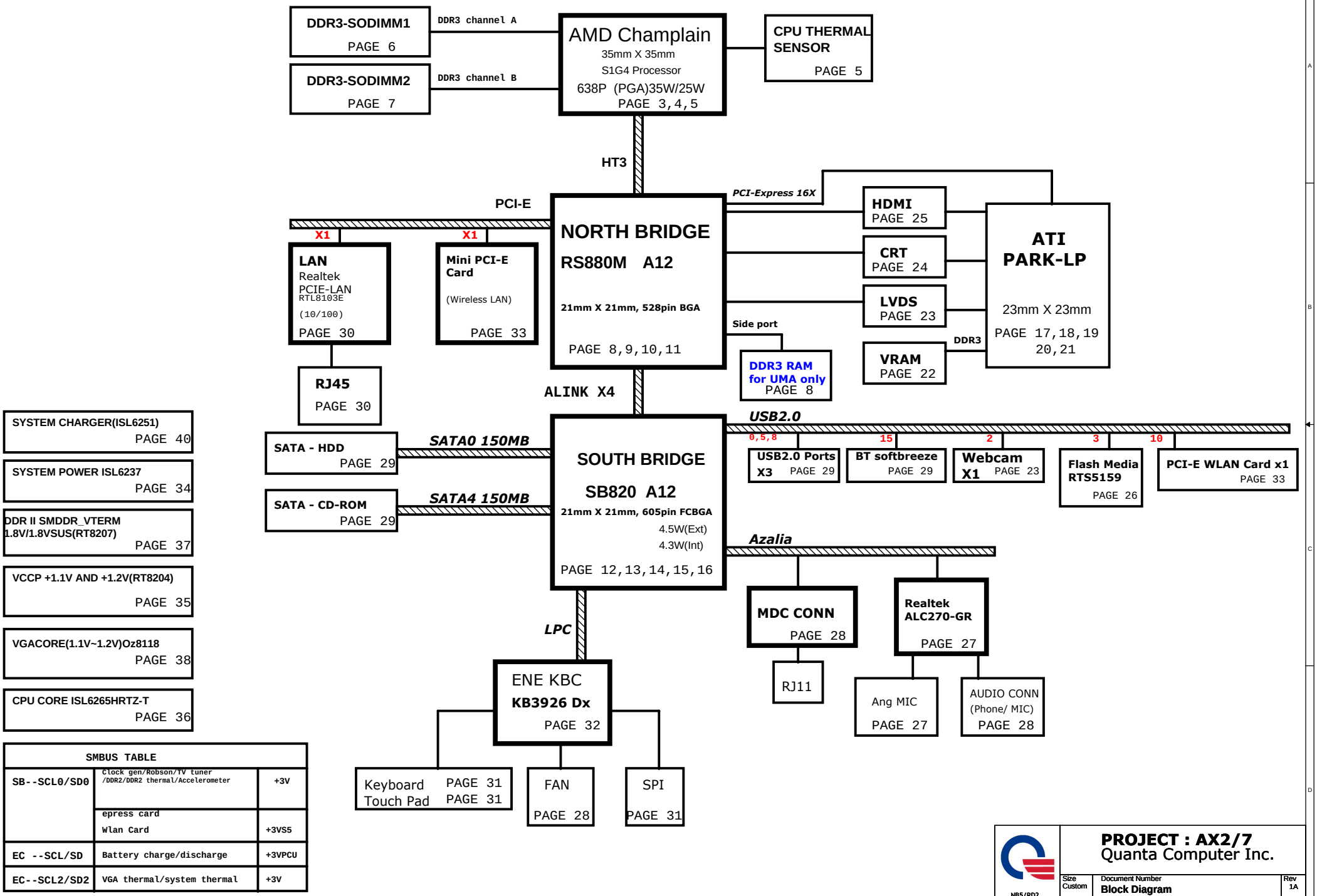
AX2/7 SYSTEM DIAGRAM

AMD Smarter Choice

01



SMBUS TABLE		
SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

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PV,delete all external clock GEN reserve material

VLDT use 1.5A Max current

+1.1V — R164 *0_6/S — +1.1V_VLDT

+1.1V — R83 *0_6/S — +1.1V_VLDT_R

+2.5V — BLM21PG221SN1D(220,100M,2A)_8 — L34 — +CPUVDDA W/S= 15 mil/20mil

C418 4.7U/6.3V_6 (LS0805-100M-N) C392 4.7U/6.3V_6 C302 0.22U/25V_6 C304 3300P/50V_4

CPU CLK

12 CPUCLKP — CPUCLKP

12 CPUCLKN — CPUCLKN

Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"

CPUCLKIN — R149 169/F_4 — CPUCLKIN#

CPUCLKP — C402 3900P/25V_4 — CPUCLKIN

CPUCLKN — C401 3900P/25V_4 — CPUCLKIN#

H_THRMDC 5
H_THRMDA 5

CPU_PWRGD — 300_4 — R146
CPU_LDT_RST# — 300_4 — R148
CPU_LDT_STOP# — 300_4 — R166
CPU_LDT_REQ# CPU — *300/F_4 — R144 — +1.5V

+CPUVDDA 250mA

W/S= 15 mil/20mil

C396 10U/6.3V_8
C390 0.22U/6.3V_4
C389 180P/50V_4

+1.1V_VLDT D1 D2 D3 D4

U21A — HT LINK — SOCKET_638_PIN

VLDT_A0 VLDT_A1 VLDT_A2 VLDT_A3

VLDT_B0 VLDT_B1 VLDT_B2 VLDT_B3

+1.1V_VLDT_R 10U/6.3V_8 — C99
+1.1V_VLDT_R 0.22U/6.3V_4 — C113
+1.1V_VLDT_R 180P/50V_4 — C120
+1.1V_VLDT_R 10U/6.3V_8 — C594

HT_NB_CPU_CAD_H0 … HT_NB_CPU_CAD_H15 ↔ L0_CADIN_H0 … L0_CADIN_H15
HT_NB_CPU_CAD_L0 … HT_NB_CPU_CAD_L15 ↔ L0_CADIN_L0 … L0_CADIN_L15
HT_CPU_NB_CAD_H0 … HT_CPU_NB_CAD_H15 ↔ L0_CADOUT_H0 … L0_CADOUT_H15
HT_CPU_NB_CAD_L0 … HT_CPU_NB_CAD_L15 ↔ L0_CADOUT_L0 … L0_CADOUT_L15

HT_NB_CPU_CLK_H0 … HT_NB_CPU_CLK_H1 ↔ L0_CLKIN_H0 … L0_CLKIN_L1
HT_CPU_NB_CLK_H0 … HT_CPU_NB_CLK_H1 ↔ L0_CLKOUT_H0 … L0_CLKOUT_L1

HT_NB_CPU_CTL_H0 … HT_NB_CPU_CTL_L1 ↔ L0_CTLIN_H0 … L0_CTLIN_L1
HT_CPU_NB_CTL_H0 … HT_CPU_NB_CTL_L1 ↔ L0_CTLOUT_H0 … L0_CTLOUT_L1

8 HT_NB_CPU_CAD_H[15..0] — HT_NB_CPU_CAD_H[15..0]
8 HT_NB_CPU_CAD_L[15..0] — HT_NB_CPU_CAD_L[15..0]
8 HT_NB_CPU_CLK_H[1..0] — HT_NB_CPU_CLK_H[1..0]
8 HT_NB_CPU_CLK_L[1..0] — HT_NB_CPU_CLK_L[1..0]
8 HT_NB_CPU_CTL_H[1..0] — HT_NB_CPU_CTL_H[1..0]
8 HT_NB_CPU_CTL_L[1..0] — HT_NB_CPU_CTL_L[1..0]
8 HT_CPU_NB_CAD_H[15..0] — HT_CPU_NB_CAD_H[15..0]
8 HT_CPU_NB_CAD_L[15..0] — HT_CPU_NB_CAD_L[15..0]
8 HT_CPU_NB_CLK_H[1..0] — HT_CPU_NB_CLK_H[1..0]
8 HT_CPU_NB_CLK_L[1..0] — HT_CPU_NB_CLK_L[1..0]
8 HT_CPU_NB_CTL_H[1..0] — HT_CPU_NB_CTL_H[1..0]
8 HT_CPU_NB_CTL_L[1..0] — HT_CPU_NB_CTL_L[1..0]

SideBand Temp sense I2C

5 CPU_SIC — CPU_SIC — AF4
5 CPU_SID — CPU_SID — AF5
5 CPU_ALERT — CPU_ALERT — AE6

+1.5VSUS — R163 510/F_4 — CPUTEST25H — CPUTEST25L — R162 510/F_4

+1.1V_VLDT — R114 44.2/F_4 — R115 44.2/F_4 — CPU_HTREF0 — CPU_HTREF1 — R6 — P6 — place them to CPU within 1.5"

36 CPU_VDD0_RUN_FB_H — F6
36 CPU_VDD0_RUN_FB_L — E6
36 CPU_VDD1_RUN_FB_H — Y6
36 CPU_VDD1_RUN_FB_L — AB6

CPU_DBRDY — G10
CPU_TMS — AA9
CPU_TCK — AC9
CPU_TRST# — AD9
CPU_TDI — AF9

T7 CPUTEST23 AD7
T26 CPUTEST18 H10
T30 CPUTEST19 G9
CPUTEST25H E9
CPUTEST25L E8
place them to CPU within 1.5"
T127 CPUTEST21 AB8
CPUTEST20 AF7
CPUTEST24 AF7
CPUTEST22 AE8
T8 CPUTEST12 AC8
T6 CPUTEST27 AF8

R157 *0_4/S — C2 — AA6

RSVD1 A3 RSVD2 A5 RSVD3 B3 RSVD4 B5 RSVD5 C1

RSVD10 M11 RSVD9 W18 RSVD8 AA7 RSVD7 D5 RSVD6 C5

VSS RSVD11

CLKIN_H A9 CLKIN_L A8

RESET_L B7
PWROK A7
LDTSTOP_L F10
LDTREQ_L C6

SIC AF4
SID AF5
ALERT_L AE6

HT_REF0 R6
HT_REF1 P6

VDD0_FB_H F6
VDD0_FB_L E6
VDD1_FB_H Y6
VDD1_FB_L AB6

DBRDY G10
TMS AA9
TCK AC9
TRST_L AD9
TDI AF9

TEST23 AD7
TEST18 H10
TEST19 G9
TEST25_H E9
TEST25_L E8
TEST21 AB8
TEST20 AF7
TEST24 AF7
TEST22 AE8
TEST12 AC8
TEST27 AF8
TEST9 C2
TEST6 AA6

VDDA1 F8
VDDA2 F9

CLKIN_H A9
CLKIN_L A8

RESET_L B7
PWROK A7
LDTSTOP_L F10
LDTREQ_L C6

SIC AF4
SID AF5
ALERT_L AE6

HT_REF0 R6
HT_REF1 P6

VDD0_FB_H F6
VDD0_FB_L E6
VDD1_FB_H Y6
VDD1_FB_L AB6

DBRDY G10
TMS AA9
TCK AC9
TRST_L AD9
TDI AF9

TEST23 AD7
TEST18 H10
TEST19 G9
TEST25_H E9
TEST25_L E8
TEST21 AB8
TEST20 AF7
TEST24 AF7
TEST22 AE8
TEST12 AC8
TEST27 AF8
TEST9 C2
TEST6 AA6

RSVD1 A3
RSVD2 A5
RSVD3 B3
RSVD4 B5
RSVD5 C1

VSS M11
RSVD11 W18

A6 CPU_SVC_R
A4 CPU_SVD_R

AF6 CPU_THERMTRIP_L#
AC7 CPU_PROCHOT_L#
AA8 CPU_MEMHOT_L# — T15

THERMDC W7 H_THRMDC
THERMDA W8 H_THRMDA

VDDIO_FB_H W9 — VDDIO_FB_H 37
VDDIO_FB_L Y9 — VDDIO_FB_L 37

VDDNB_FB_H H6 — CPU_VDDNB_RUN_FB_H 36
VDDNB_FB_L G6 — CPU_VDDNB_RUN_FB_L 36

DBREQ_L F10 CPU_DBREQ#
TDO AE9 CPU_TDO

J7 H8

D7 CPUTEST17 — T37
E7 CPUTEST16 — T38
F7 CPUTEST15 — T29
C7 CPUTEST14 — T49

C3 K8 R156 *300/F_4 +1.1V_VLDT

C4 CPUTEST29H — T46
R130 80.6/F_4
C9 C8 CPUTEST29L — T45

H18 H19 AA7 D5 C5

Route as 80ohm, diff

+1.5VSUS — R172 300/F_4 CPU_DBREQ#
R338 1K/F_4 CPUTEST27
R339 *300/F_4

FOX PZ63826-284R-41F
DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)

MV can remove reserve for debug

+1.5VSUS — R207 10K/F_4 CNTR_VREF — Q19 MMBT3904 — CPU_LDT_RST# — CPU_LDT_RST_HTPA# — +3V — R186 1K/F_4

Serial VID

+1.5VSUS — R170 *1K/F_4 — R171 *1K/F_4 — +1.5V

R189 1K/F_4 — +1.5VSUS
R190 1K/F_4 — +1.5V

CPU_SVC_R — R176 0_4 — CPU_SVC
CPU_SVD_R — R175 0_4 — CPU_SVD
CPU_PWRGD — R177 0_4 — CPU_PWRGD_SVID_REG

CPU_SVC 36
CPU_SVD 36
CPU_PWRGD_SVID_REG 36

R184 *220_4
R183 *220_4
R185 *220_4

VFIX MODE — VID Override table (VDD)

SVC	SVD	Output Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

CPUTEST20 R340 1K/F_4
CPUTEST21 R81 1K/F_4
CPUTEST22 R80 1K/F_4
CPUTEST24 R69 1K/F_4

HDT Connector

+1.5VSUS

CPU_DBREQ#
CPU_DBRDY
CPU_TCK
CPU_TMS
CPU_TDI
CPU_TRST#
CPU_TDO

C74 *0.1U/10V_4

KEY

CPU_LDT_RST_HTPA#

CN6 *HDT CONN

CPUTEST12 R70 1K/F_4
CPUTEST19 R124 1K/F_4
CPUTEST18 R125 1K/F_4

+1.5VSUS — R224 10K/F_4 — Q22 MMBT3904 — CPU_PROCHOT_L# — R205 0_4 — R219 0_4 — 32 CPU_PROCHOT# — CPU_PROCHOT_R# — CPU_PROCHOT_R 12

+1.5VSUS — R225 300_4

EC new option

+1.5VSUS — R181 10K/F_4 — Q18 MMBT3904 — R180 1K/F_4 — 5 CPU_THERMTRIP_L# — CPU_THERMTRIP_L# — CPU_THERMTRIP# 13

SI , add R205 for P-state implement

NB5/RD2	**PROJECT : AX2/7** Quanta Computer Inc.	
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Processor Memory Interface

04

VDDR = 0.9V for 25W & 35W CPU

VDDR = 1.05V for 35V & 45W CPU

PLACE THEM CLOSE TO CPU WITHIN 1"

PV, change to short pad

SI , change from 0.01u to 0.1u from AMD recommand

Place close to socket

Reserved for AMD suggest

U21B MEM:CMD/CTRL/CLK

SOCKET_638_PIN

U21C MEM:DATA

SOCKET_638_PIN

PROJECT : AX2/7
Quanta Computer Inc.

NB5/RD2

Size	Document Number	Rev
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PROCESSOR POWER AND GROUND

U21E — SOCKET_638_PIN

+VCORE: G4, H2, J9, J11, J13, J15, K6, K10, K12, K14, L4, L7, L9, L11, L13, L15, M2, M6, M8, M10, N7, N9, N11

+CPUVDDNB: 4A — K16, M16, P16, T16, V16

+1.5VSUS: 2A — H25, J17, K18, K21, K23, K25, L17, M18, M21, M23, M25, N17

+VCORE: P8, P10, R4, R7, R9, R11, T2, T6, T8, T10, T12, T14, U7, U9, U11, U13, U15, V6, V8, V10, V12, V14, W4, Y2, AC4, AD2

+1.5VSUS: Y25, V25, V23, V21, V18, U17, T25, T23, T21, T18, R17, P25, P23, P21, P18

U21F — SOCKET_638_PIN

AA4, AA11, AA13, AA15, AA17, AA19, AB2, AB7, AB9, AB23, AB25, AC11, AC13, AC15, AC17, AC19, AC21, AD6, AD8, AD25, AE11, AE13, AE15, AE17, AE19, AE21, AE23, B4, B6, B8, B9, B11, B13, B15, B17, B19, B21, B23, B25, D6, D8, D9, D11, D13, D15, D17, D19, D21, D23, D25, E4, F2, F11, F13, F15, F17, F19, F21, F23, F25, H7, H9, H21, H23, J4

VSS1–VSS65

VSS66, J6, J8, J10, J12, J14, J16, J18, K2, K7, K9, K11, K13, K15, K17, L6, L8, L10, L12, L14, L16, L18, M7, M9, AC6, M17, N4, N8, N10, N16, N18, P2, P7, P9, P11, P17, R8, R10, R16, R18, T7, T9, T11, T13, T15, T17, U4, U6, U8, U10, U12, U14, U16, U18, V2, V7, V9, V11, V13, V15, V17, W6, Y21, Y23, N6

VSS67–VSS129

BOTTOM SIDE DECOUPLING

+VCORE: C180 22U/6.3V_8, C216 22U/6.3V_8, C230 22U/6.3V_8, C247 22U/6.3V_8, C256 0.22U/6.3V_4, C255 0.01U/16V_4, C254 180P/50V_4

+VCORE: C242 22U/6.3V_8, C250 22U/6.3V_8, C228 22U/6.3V_8, C215 22U/6.3V_8, C177 0.22U/6.3V_4, C178 0.01U/16V_4, C176 180P/50V_4

+CPUVDDNB: C223 22U/6.3V_8, C212 22U/6.3V_8, C235 22U/6.3V_8

+1.5VSUS: C214 22U/6.3V_8, C227 22U/6.3V_8, C238 0.22U/6.3V_4, C257 0.22U/6.3V_4, C258 180P/50V_4

DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE

+1.5VSUS: C115 4.7U/6.3V_6, C126 4.7U/6.3V_6, C291 4.7U/6.3V_6, C288 4.7U/6.3V_6, C119 0.22U/6.3V_4, C123 0.22U/6.3V_4

+1.5VSUS: C135 0.22U/6.3V_4, C133 0.22U/6.3V_4, C188 0.01U/16V_4, C172 0.1U/10V_4, C287 180P/50V_4, C284 180P/50V_4, C189 0.1U/10V_4

SI , change SMB connection

+1.5VSUS: R228 2K/F_4, R198 2K/F_4, R173 2K/F_4

+1.5VSUS: R214 1K/F_4, R187 1K/F_4, R178 1K/F_4

32,40 MBCLK — MBCLK — Q23 MMBT3904 — CPU_SIC — CPU_SIC 3

32,40 MBDATA — MBDATA — Q21 MMBT3904 — CPU_SID — CPU_SID 3

RB501V-40 D19; RB501V-40 D16

SMBALERT# — Q17 *MMBT3904 — CPU_ALERT — CPU_ALERT 3

SI , add Q21,Q23,D16,D19

+3V: R424 10K/F_4, R423 10K/F_4, R416 10K/F_4

+3V: R405 200/F_6, C693 0.1U/10V_4

U25 MSOP: SCLK, SDA, ALERT#, OVERT#, VCC, DXP, DXN, GND

18,32 MBCLK2; 18,32 MBDATA2; 13 PM_THERM#

H_THRMDA 3; H_THRMDC 3; C695 1000P/50V_4

PV ,Change from +1.5VSUS to +1.5V for leakage current issue

G786P8

SMBALERT#

+1.5V — R428 10K/F_4 — Q33 MMBT3904 — CPU_THERMTRIP_L# — 3 CPU_THERMTRIP_L#

SI , add Q33,R428

reserve for power shutdown (if can)

R212 *0_4 — SYS_SHDN# — SYS_SHDN# 34

D17 *CH500H

R203 *0_4/S — 3920_RST# — 3920_RST# 32

Q20 MMBT3904

D18 CH501H-40PT — ECPWROK — ECPWROK 16,32

R218 10K/F_4 — +3V

PQ18 *2N7002E-G

R174 *10K/F_4 — TEMP_FAIL 18

ADD VGA TEMP_ FAIL function

M92 is active Hi

+VIN: EC13 0.1U/10V_4

PV,add for EMI suggest

+1.5V_VGA: EC10 0.01U/16V_4 — +3V

+1.8V_VGA: EC12 0.01U/16V_4 — +3V

+VGA_CORE: EC8 0.01U/16V_4 — +3V

+VIN: EC7 0.01U/16V_4 — +3V

+5V: EC1 *0.01U/16V_4 — +3V

+VGA_CORE: EC2 *0.01U/16V_4 — +1.8V_VGA

+VGA_CORE: EC15 0.1U/10V_4; +3V: EC6 *0.1U/10V_4

+1.5V_VGA: EC9 0.01U/16V_4 — +3V

+1.5VSUS: EC11 0.01U/16V_4 — +1.1V

For fix HyperTransport nets across plane splits

NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

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Custom	S1G4 PWR & GND 3/3	1A

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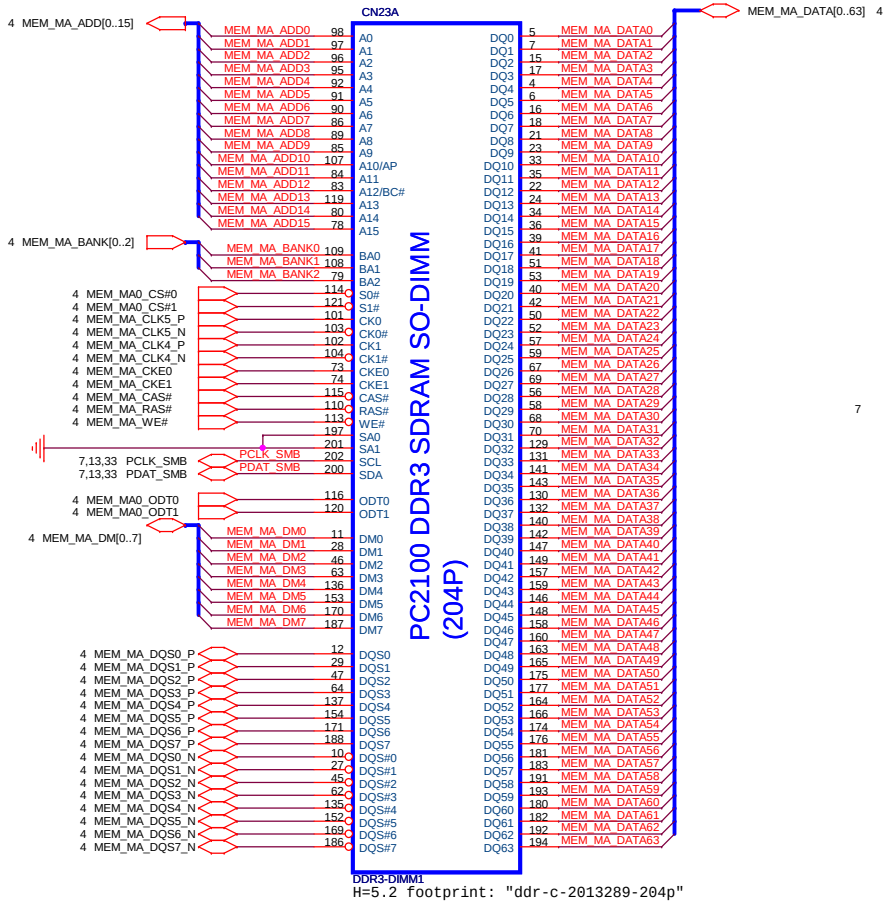
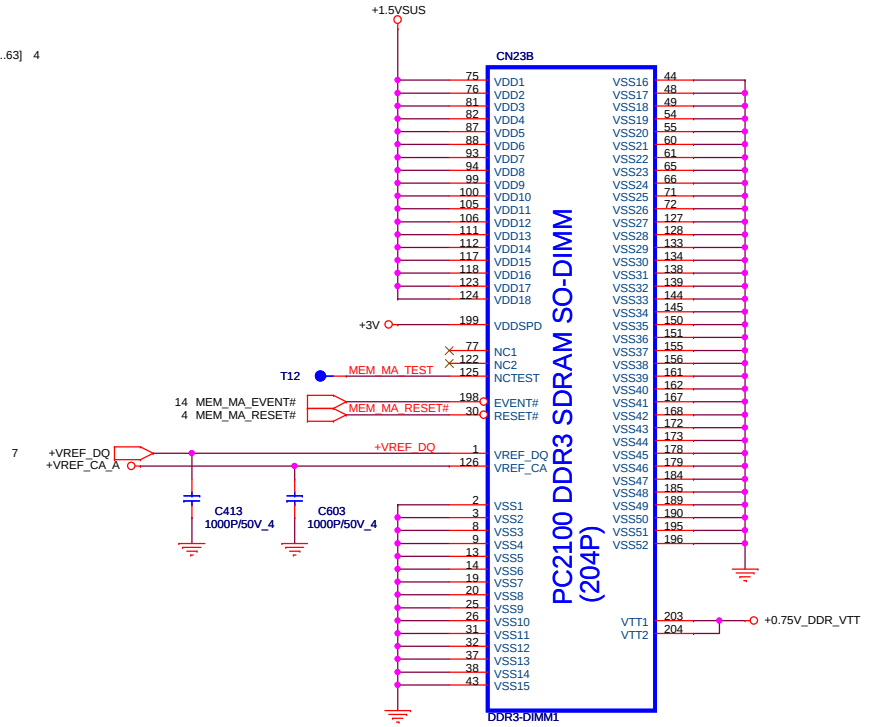
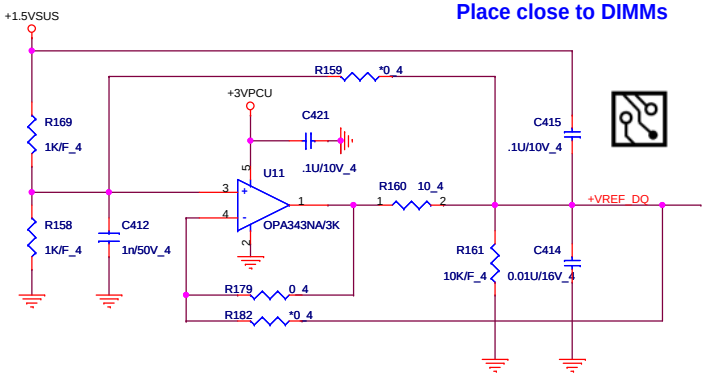


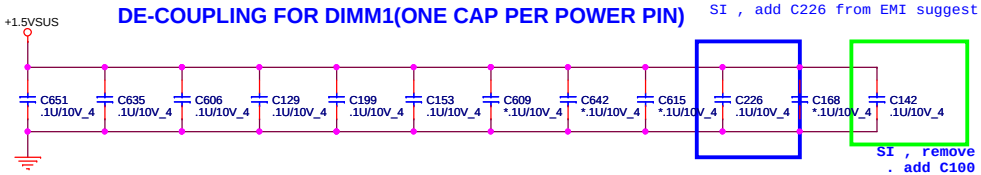


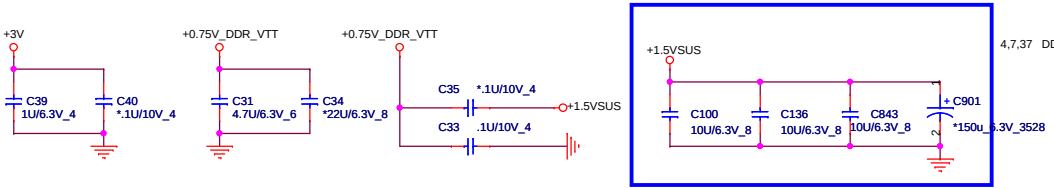
SO-DIMM BYPASS PLACEMENT :

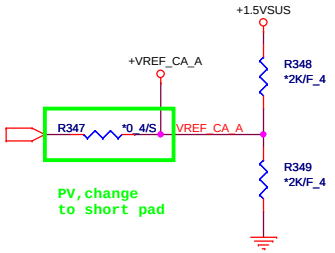
Place these Caps near So-Dimm1.

No Vias Between the Trace of PIN to CAP.









PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 SODIMMS: A/B CHANNEL	1A

NB5/RD2

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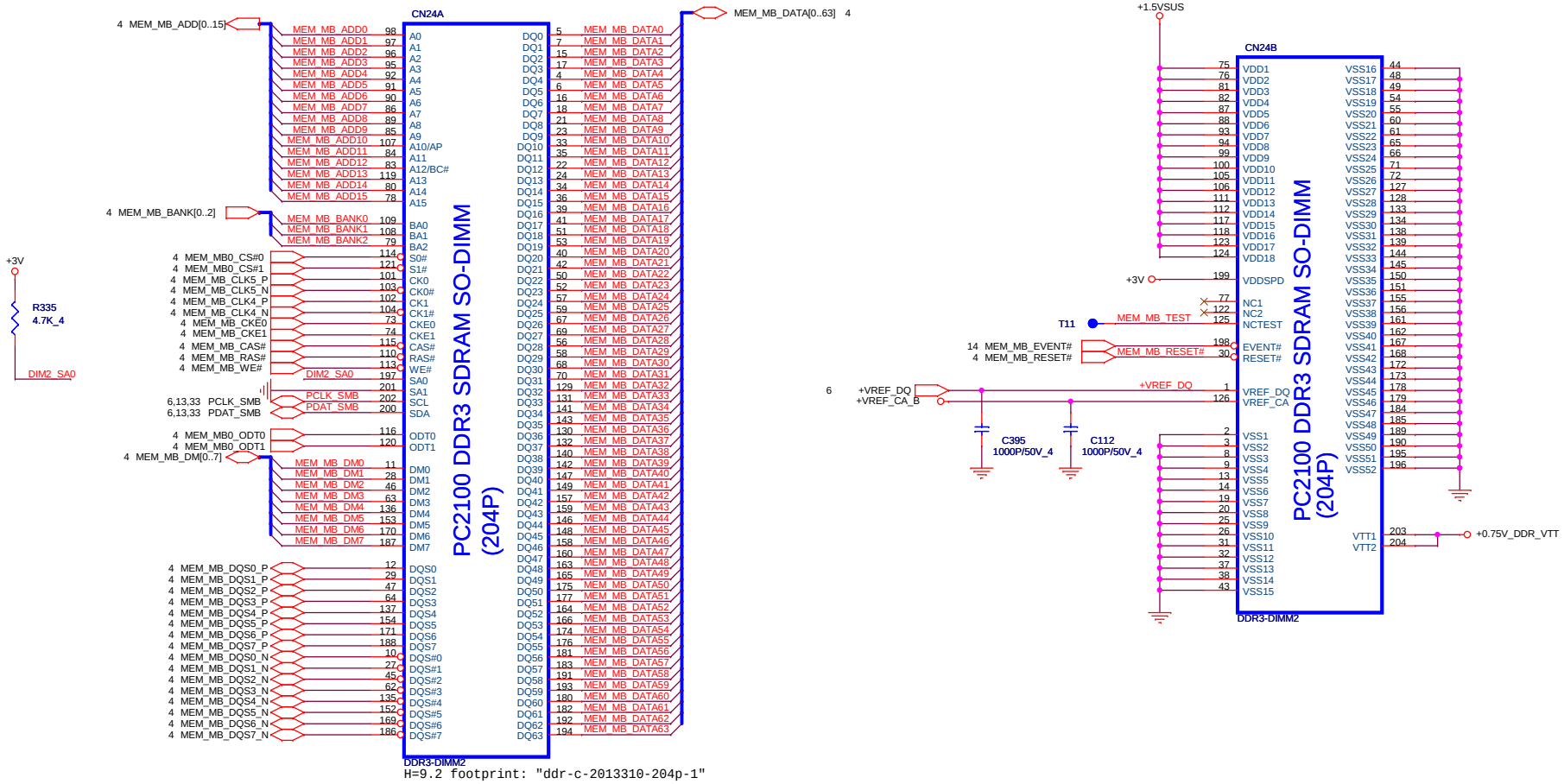
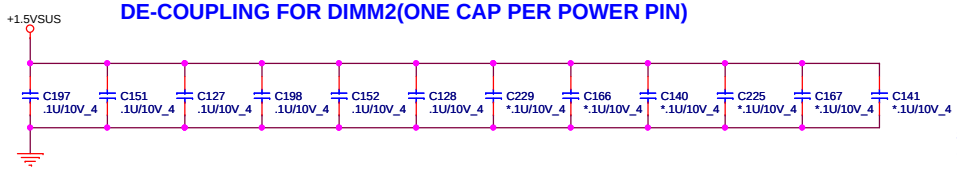


SO-DIMM BYPASS PLACEMENT :

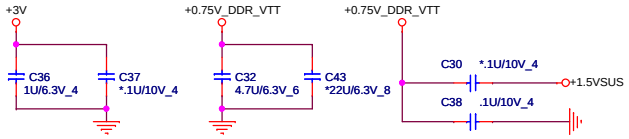
Place these Caps near So-Dimm1.

No Vias Between the Trace of PIN to CAP.

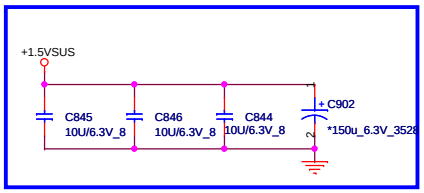
DE-COUPLING FOR DIMM2(ONE CAP PER POWER PIN)

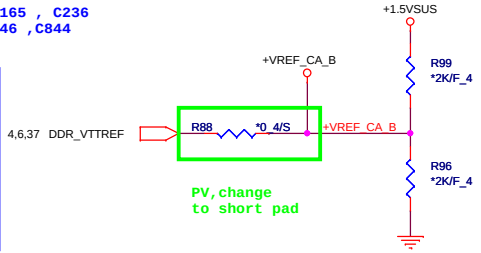


DE-COUPLING FOR DIMM2



SI , remove C165 , C236
add C845 , C846 ,C844
Reserve C902





PV,change
to short pad

NB5/RD2	PROJECT : AX2/7 Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 SODIMMS TERMINATIONS	Rev: 1A
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HT_CPU_NB_CAD_H[15..0] — HT_CPU_NB_CAD_H[15..0] 3
HT_CPU_NB_CAD_L[15..0] — HT_CPU_NB_CAD_L[15..0] 3
HT_CPU_NB_CLK_H[1..0] — HT_CPU_NB_CLK_H[1..0] 3
HT_CPU_NB_CLK_L[1..0] — HT_CPU_NB_CLK_L[1..0] 3
HT_CPU_NB_CTL_H[1..0] — HT_CPU_NB_CTL_H[1..0] 3
HT_CPU_NB_CTL_L[1..0] — HT_CPU_NB_CTL_L[1..0] 3
HT_NB_CPU_CAD_H[15..0] — HT_NB_CPU_CAD_H[15..0] 3
HT_NB_CPU_CAD_L[15..0] — HT_NB_CPU_CAD_L[15..0] 3
HT_NB_CPU_CLK_H[1..0] — HT_NB_CPU_CLK_H[1..0] 3
HT_NB_CPU_CLK_L[1..0] — HT_NB_CPU_CLK_L[1..0] 3
HT_NB_CPU_CTL_H[1..0] — HT_NB_CPU_CTL_H[1..0] 3
HT_NB_CPU_CTL_L[1..0] — HT_NB_CPU_CTL_L[1..0] 3

U22A

HYPER TRANSPORT CPU I/F — PART 1 OF 6

HT_CPU_NB_CAD_H0	Y25	HT_RXCAD0P	HT_TXCAD0P	D24	HT_NB_CPU_CAD_H0
HT_CPU_NB_CAD_L0	Y24	HT_RXCAD0N	HT_TXCAD0N	D25	HT_NB_CPU_CAD_L0
HT_CPU_NB_CAD_H1	V22	HT_RXCAD1P	HT_TXCAD1P	E24	HT_NB_CPU_CAD_H1
HT_CPU_NB_CAD_L1	V23	HT_RXCAD1N	HT_TXCAD1N	E25	HT_NB_CPU_CAD_L1
HT_CPU_NB_CAD_H2	V25	HT_RXCAD2P	HT_TXCAD2P	F24	HT_NB_CPU_CAD_H2
HT_CPU_NB_CAD_L2	V24	HT_RXCAD2N	HT_TXCAD2N	F25	HT_NB_CPU_CAD_L2
HT_CPU_NB_CAD_H3	U24	HT_RXCAD3P	HT_TXCAD3P	F23	HT_NB_CPU_CAD_H3
HT_CPU_NB_CAD_L3	U25	HT_RXCAD3N	HT_TXCAD3N	F22	HT_NB_CPU_CAD_L3
HT_CPU_NB_CAD_H4	T25	HT_RXCAD4P	HT_TXCAD4P	H23	HT_NB_CPU_CAD_H4
HT_CPU_NB_CAD_L4	T24	HT_RXCAD4N	HT_TXCAD4N	H22	HT_NB_CPU_CAD_L4
HT_CPU_NB_CAD_H5	P22	HT_RXCAD5P	HT_TXCAD5P	J25	HT_NB_CPU_CAD_H5
HT_CPU_NB_CAD_L5	P23	HT_RXCAD5N	HT_TXCAD5N	J24	HT_NB_CPU_CAD_L5
HT_CPU_NB_CAD_H6	P25	HT_RXCAD6P	HT_TXCAD6P	K24	HT_NB_CPU_CAD_H6
HT_CPU_NB_CAD_L6	P24	HT_RXCAD6N	HT_TXCAD6N	K25	HT_NB_CPU_CAD_L6
HT_CPU_NB_CAD_H7	N24	HT_RXCAD7P	HT_TXCAD7P	K23	HT_NB_CPU_CAD_H7
HT_CPU_NB_CAD_L7	N25	HT_RXCAD7N	HT_TXCAD7N	K22	HT_NB_CPU_CAD_L7
HT_CPU_NB_CAD_H8	AC24	HT_RXCAD8P	HT_TXCAD8P	F21	HT_NB_CPU_CAD_H8
HT_CPU_NB_CAD_L8	AC25	HT_RXCAD8N	HT_TXCAD8N	G21	HT_NB_CPU_CAD_L8
HT_CPU_NB_CAD_H9	AB25	HT_RXCAD9P	HT_TXCAD9P	G20	HT_NB_CPU_CAD_H9
HT_CPU_NB_CAD_L9	AB24	HT_RXCAD9N	HT_TXCAD9N	H21	HT_NB_CPU_CAD_L9
HT_CPU_NB_CAD_H10	AA24	HT_RXCAD10P	HT_TXCAD10P	J20	HT_NB_CPU_CAD_H10
HT_CPU_NB_CAD_L10	AA25	HT_RXCAD10N	HT_TXCAD10N	J21	HT_NB_CPU_CAD_L10
HT_CPU_NB_CAD_H11	Y22	HT_RXCAD11P	HT_TXCAD11P	J18	HT_NB_CPU_CAD_H11
HT_CPU_NB_CAD_L11	Y23	HT_RXCAD11N	HT_TXCAD11N	K17	HT_NB_CPU_CAD_L11
HT_CPU_NB_CAD_H12	W21	HT_RXCAD12P	HT_TXCAD12P	L19	HT_NB_CPU_CAD_H12
HT_CPU_NB_CAD_L12	W20	HT_RXCAD12N	HT_TXCAD12N	J19	HT_NB_CPU_CAD_L12
HT_CPU_NB_CAD_H13	V21	HT_RXCAD13P	HT_TXCAD13P	M19	HT_NB_CPU_CAD_H13
HT_CPU_NB_CAD_L13	V20	HT_RXCAD13N	HT_TXCAD13N	L18	HT_NB_CPU_CAD_L13
HT_CPU_NB_CAD_H14	U20	HT_RXCAD14P	HT_TXCAD14P	M21	HT_NB_CPU_CAD_H14
HT_CPU_NB_CAD_L14	U21	HT_RXCAD14N	HT_TXCAD14N	P21	HT_NB_CPU_CAD_L14
HT_CPU_NB_CAD_H15	U19	HT_RXCAD15P	HT_TXCAD15P	P18	HT_NB_CPU_CAD_H15
HT_CPU_NB_CAD_L15	U18	HT_RXCAD15N	HT_TXCAD15N	M18	HT_NB_CPU_CAD_L15
HT_CPU_NB_CLK_H0	T22	HT_RXCLK0P	HT_TXCLK0P	H24	HT_NB_CPU_CLK_H0
HT_CPU_NB_CLK_L0	T23	HT_RXCLK0N	HT_TXCLK0N	H25	HT_NB_CPU_CLK_L0
HT_CPU_NB_CLK_H1	AB23	HT_RXCLK1P	HT_TXCLK1P	L21	HT_NB_CPU_CLK_H1
HT_CPU_NB_CLK_L1	AA22	HT_RXCLK1N	HT_TXCLK1N	L20	HT_NB_CPU_CLK_L1
HT_CPU_NB_CTL_H0	M22	HT_RXCTL0P	HT_TXCTL0P	M24	HT_NB_CPU_CTL_H0
HT_CPU_NB_CTL_L0	M23	HT_RXCTL0N	HT_TXCTL0N	M25	HT_NB_CPU_CTL_L0
HT_CPU_NB_CTL_H1	R21	HT_RXCTL1P	HT_TXCTL1P	P19	HT_NB_CPU_CTL_H1
HT_CPU_NB_CTL_L1	R20	HT_RXCTL1N	HT_TXCTL1N	R18	HT_NB_CPU_CTL_L1
HT_RXCALP	C23	HT_RXCALP	HT_TXCALP	B24	HT_TXCALP
HT_RXCALN	A24	HT_RXCALN	HT_TXCALN	B25	HT_TXCALN

R412 301/F_4 HT_RXCALP
HT_RXCALN
R411 301/F_4 HT_TXCALP
HT_TXCALN

RS880

signals	RS880	RX880
HT_TXCALP	R430 301 ohm 1%	R430 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R434 301 ohm 1%	R434 1.21k ohm 1%
HT_RXCALN		

U18

SPM_VREF1	M9	VREFCA	DQL0	E4	SPM_DQ2
SPM_VREF2	H2	VREFDQ	DQL1	F8	SPM_DQ1
			DQL2	F3	SPM_DQ5
SPM_A0	N4	A0	DQL3	F9	SPM_DQ3
SPM_A1	P8	A1	DQL4	H4	SPM_DQ7
SPM_A2	P4	A2	DQL5	H9	SPM_DQ0
SPM_A3	N3	A3	DQL6	G3	SPM_DQ4
SPM_A4	P9	A4	DQL7	H8	SPM_DQ6
SPM_A5	P3	A5			
SPM_A6	R9	A6			
SPM_A7	R3	A7	DQU0	D8	SPM_DQ13
SPM_A8	T9	A8	DQU1	C4	SPM_DQ8
SPM_A9	R4	A9	DQU2	C9	SPM_DQ10
SPM_A10	L8	A10/AP	DQU3	C3	SPM_DQ12
SPM_A11	R8	A11	DQU4	A8	SPM_DQ15
SPM_A12	N8	A12/BC	DQU5	A3	SPM_DQ11
SPM_A13	T4	A13	DQU6	B9	SPM_DQ14
	T8	A14	DQU7	A4	SPM_DQ9
	M8	A15			
SPM_BA0	M3	BA0	VDD#B3	B3	+1.5V_MEM_VDDQ
SPM_BA1	N9	BA1	VDD#D10	D10	
SPM_BA2	M4	BA2	VDD#G8	G8	
			VDD#K3	K3	
			VDD#K9	K9	
			VDD#N2	N2	
SPM_CLKP	J8	CK	VDD#N10	N10	
SPM_CLKN	K8	CK	VDD#R2	R2	
SPM_CKE	K10	CKE	VDD#R10	R10	+1.5V_MEM_VDDQ
SPM_ODT	K2	ODT	VDDQ#A2	A2	
SPM_CS#	L3	CS	VDDQ#A9	A9	
SPM_RAS#	J4	RAS	VDDQ#C2	C2	
SPM_CAS#	K4	CAS	VDDQ#C10	C10	
SPM_WE#	L4	WE	VDDQ#D3	D3	
			VDDQ#E10	E10	
SPM_DQS0P	F4	DQSL	VDDQ#F2	F2	
SPM_DQS1P	C8	DQSU	VDDQ#H3	H3	
			VDDQ#H10	H10	
SPM_DM0	E8	DML	VSS#A10	A10	
SPM_DM1	D4	DMU	VSS#B4	B4	
			VSS#E2	E2	
			VSS#G9	G9	
SPM_DQS0N	G4	DQSL	VSS#J3	J3	
SPM_DQS1N	B8	DQSU	VSS#J9	J9	
			VSS#M2	M2	
			VSS#M10	M10	
			VSS#P2	P2	
			VSS#P10	P10	
	T3	RESET	VSS#T2	T2	
VMA_ZQ2	L9	ZQ	VSS#T10	T10	
			VSSQ#B2	B2	
			VSSQ#B10	B10	
			VSSQ#D2	D2	
			VSSQ#D9	D9	
			VSSQ#E3	E3	
			VSSQ#E9	E9	
	J2	NC#J2	VSSQ#F10	F10	
	L2	NC#L2	VSSQ#G2	G2	
	J10	NC#J10	VSSQ#G10	G10	
	L10	NC#L10			

100-BALL SDRAM DDR3
*H5TQ1G63AFR-14C

SI, exchange net name

R95 *100_4

+1.5V_MEM_VDDQ
R343 *10K/F_4
13 SP_DDR3_RST#
R91 *243/F_4

This block is for UMA only , DIS can remove all component

U22D

SBD_MEM/DVO_I/F — PAR 4 OF 6

SPM_A0	AB12	MEM_A0(NC)	MEM_DQ0/DVO_VSYNC(NC)	AA18	SPM_DQ0
SPM_A1	AE16	MEM_A1(NC)	MEM_DQ1/DVO_HSYNC(NC)	AA20	SPM_DQ1
SPM_A2	V11	MEM_A2(NC)	MEM_DQ2/DVO_DE(NC)	AA19	SPM_DQ2
SPM_A3	AE15	MEM_A3(NC)	MEM_DQ3/DVO_D0(NC)	Y19	SPM_DQ3
SPM_A4	AA12	MEM_A4(NC)	MEM_DQ4(NC)	V17	SPM_DQ4
SPM_A5	AB16	MEM_A5(NC)	MEM_DQ5/DVO_D1(NC)	AA17	SPM_DQ5
SPM_A6	AB14	MEM_A6(NC)	MEM_DQ6/DVO_D2(NC)	AA15	SPM_DQ6
SPM_A7	AD14	MEM_A7(NC)	MEM_DQ7/DVO_D4(NC)	Y15	SPM_DQ7
SPM_A8	AD13	MEM_A8(NC)	MEM_DQ8/DVO_D3(NC)	AC20	SPM_DQ8
SPM_A9	AD15	MEM_A9(NC)	MEM_DQ9/DVO_D5(NC)	AD19	SPM_DQ9
SPM_A10	AC16	MEM_A10(NC)	MEM_DQ10/DVO_D6(NC)	AE22	SPM_DQ10
SPM_A11	AE13	MEM_A11(NC)	MEM_DQ11/DVO_D7(NC)	AC18	SPM_DQ11
SPM_A12	AC14	MEM_A12(NC)	MEM_DQ12(NC)	AB20	SPM_DQ12
SPM_A13	Y14	MEM_A13(NC)	MEM_DQ13/DVO_D9(NC)	AD22	SPM_DQ13
			MEM_DQ14/DVO_D10(NC)	AC22	SPM_DQ14
SPM_BA0	AD16	MEM_BA0(NC)	MEM_DQ15/DVO_D11(NC)	AD21	SPM_DQ15
SPM_BA1	AE17	MEM_BA1(NC)			
SPM_BA2	AD17	MEM_BA2(NC)	MEM_DQS0P/DVO_IDCKP(NC)	Y17	SPM_DQS0P
			MEM_DQS0N/DVO_IDCKN(NC)	W18	SPM_DQS0N
SPM_RAS#	W12	MEM_RASb(NC)	MEM_DQS1P(NC)	AD20	SPM_DQS1P
SPM_CAS#	Y12	MEM_CASb(NC)	MEM_DQS1N(NC)	AE21	SPM_DQS1N
SPM_WE#	AD18	MEM_WEb(NC)			
SPM_CS#	AB13	MEM_CSb(NC)	MEM_DM0(NC)	W17	SPM_DM0
SPM_CKE	AB18	MEM_CKE(NC)	MEM_DM1/DVO_D8(NC)	AE19	SPM_DM1
SPM_ODT	V14	MEM_ODT(NC)			
			IOPLLVDD18(NC)	AE23	+1.8V_IOPLLVDD18
SPM_CLKP	V15	MEM_CKP(NC)	IOPLLVDD(NC)	AE24	+1.1V_IOPLLVDD
SPM_CLKN	W14	MEM_CKN(NC)			
			IOPLLVSS(NC)	AD23	
	AE12	MEM_COMPP(NC)		AE18	SPM_VREF
	AD12	MEM_COMPN(NC)	MEM_VREF(NC)		

RS880

T21
R357 *40.2/F_4 SPM_COMPP
R352 *40.2/F_4 SPM_COMPN
+1.5V_MEM_VDDQ

40mils wdith or more
+1.5V_MEM_VDDQ
+1.5V
R341 *0_6
C86 *1U/10V_4
C71 *10U/6.3V_8
C66 *10U/6.3V_8
C84 *0.1U/10V_4
C92 *0.1U/10V_4
C87 *1U/10V_4

*PBY160808T-221Y-N L54 +1.8V
*PBY160808T-221Y-N L16 +1.1V
C630 *2.2U/6.3V_6
C146 *2.2U/6.3V_6

R356 *1K/F_4
R355 *1K/F_4
C619 *0.1U/10V_4
C620 *0.1U/10V_4
+1.5V_MEM_VDDQ

SPM_VREF1
R73 *1K/F_4
R75 *1K/F_4
C85 *0.1U/10V_4
C77 *0.1U/10V_4
+1.5V_MEM_VDDQ

SPM_VREF2
R100 *1K/F_4
R101 *1K/F_4
C121 *0.1U/10V_4
C138 *0.1U/10V_4
+1.5V_MEM_VDDQ

NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS880-HT LINK I/F 1/5	1A

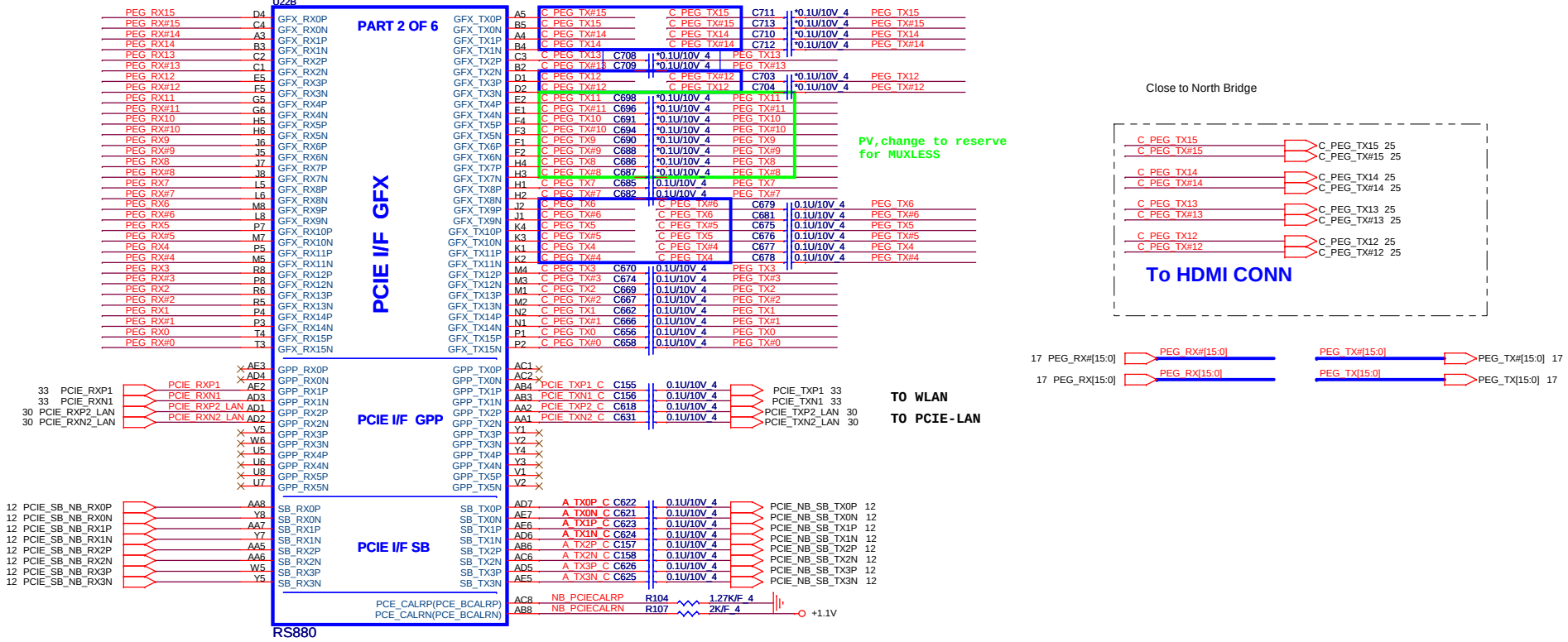
Date: Thursday, December 24, 2009 Sheet 8 of 42

GFX_RX can remove
at next stage for MUXLESS

SI , for routing smooth
GFX_TX 0/1/3/9/10/11

UMA can remove all GFX_TX CAP

SI remove C711,C713,C710,
C712,C708,C709,C703,C704
for MUXLESS



Close to North Bridge

RS880 Display Port Support (muxed on GFX)

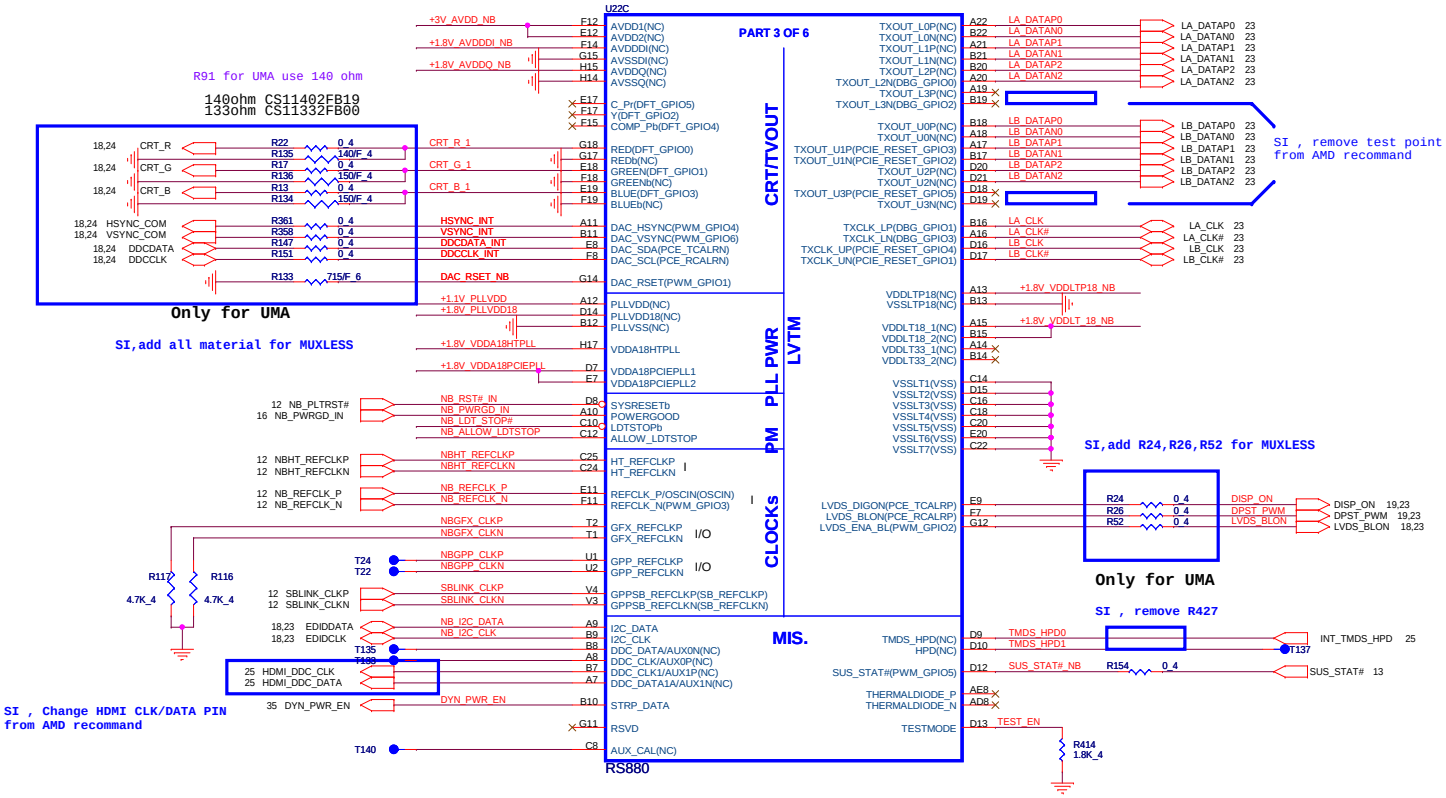
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

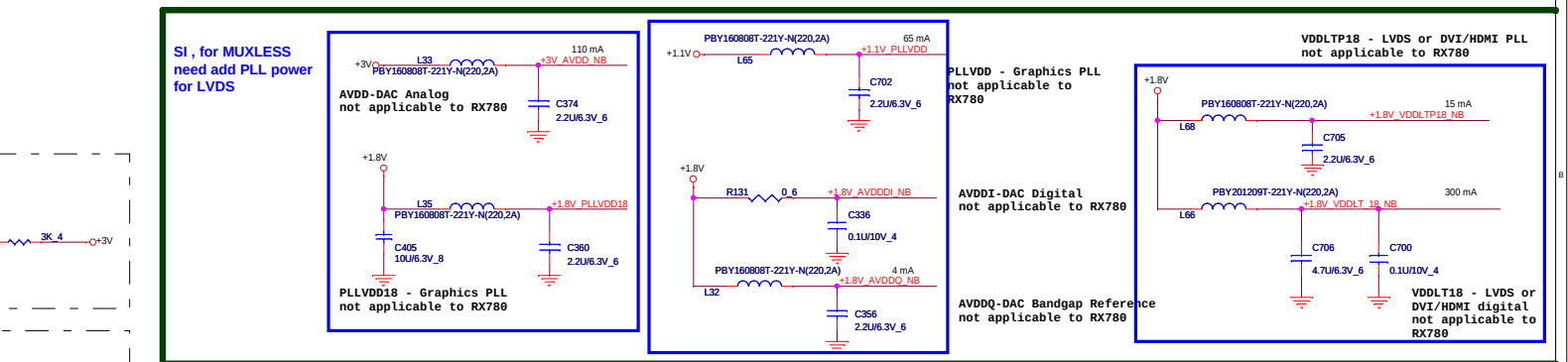
NB5/RD2

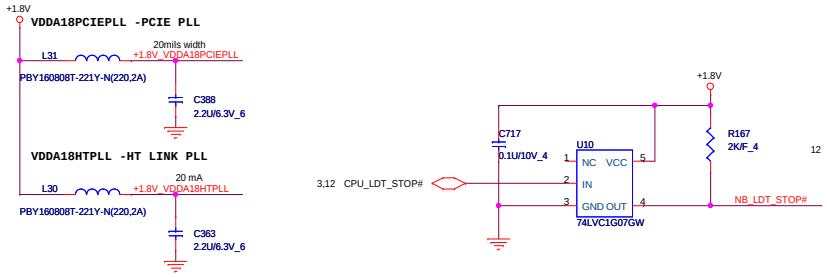
PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS880-PCIE I/F 2/5	1A

Date: Thursday, December 24, 2009 | Sheet 9 of 42







STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

RS880M	
1 Disable	
0 Enable	

RS880M: Enables Side port memory

RS880M:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

For external EEPROM Debug only

RS780/RX780

N85/RD2	PROJECT : AX2/7 Quanta Computer Inc.		
Size: Custom	Document Number: RS880-SYSTEM I/F 3/5	Rev: 1A	
Date: Thursday, December 24, 2009	Sheet 10 of 42		

RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC

U22F — PART 6/6 — GROUND

U22E — PART 5/6 — POWER — RS880

VDDHT - HT LINK digital I/O for RX780/RS780

+1.1V 2A for RS880M

VDDHTRX - HT LINK RX I/O for RX780/RS780

VDDHTTX - HT LINK TX I/O for RS880

+1.1V 2A for RS880M

+1.8V 1A for RS780M+SB700

VDDA18PCIE - PCIE TX stage I/O for RX780/RS780

VDD18 - RS780 I/O transform

VDD18_MEM For UMA RS780 only Not applicable to RX780 memory I/O transform

VDDPCIE - PCIE-E Main power

VDDC - Core Logic power

VDD_MEM For UMA RS780 only Not applicable to RX780 memory I/O transform

SI , change footprint to 0603

VDD33 - 3.3V I/O Not applicable to RX780

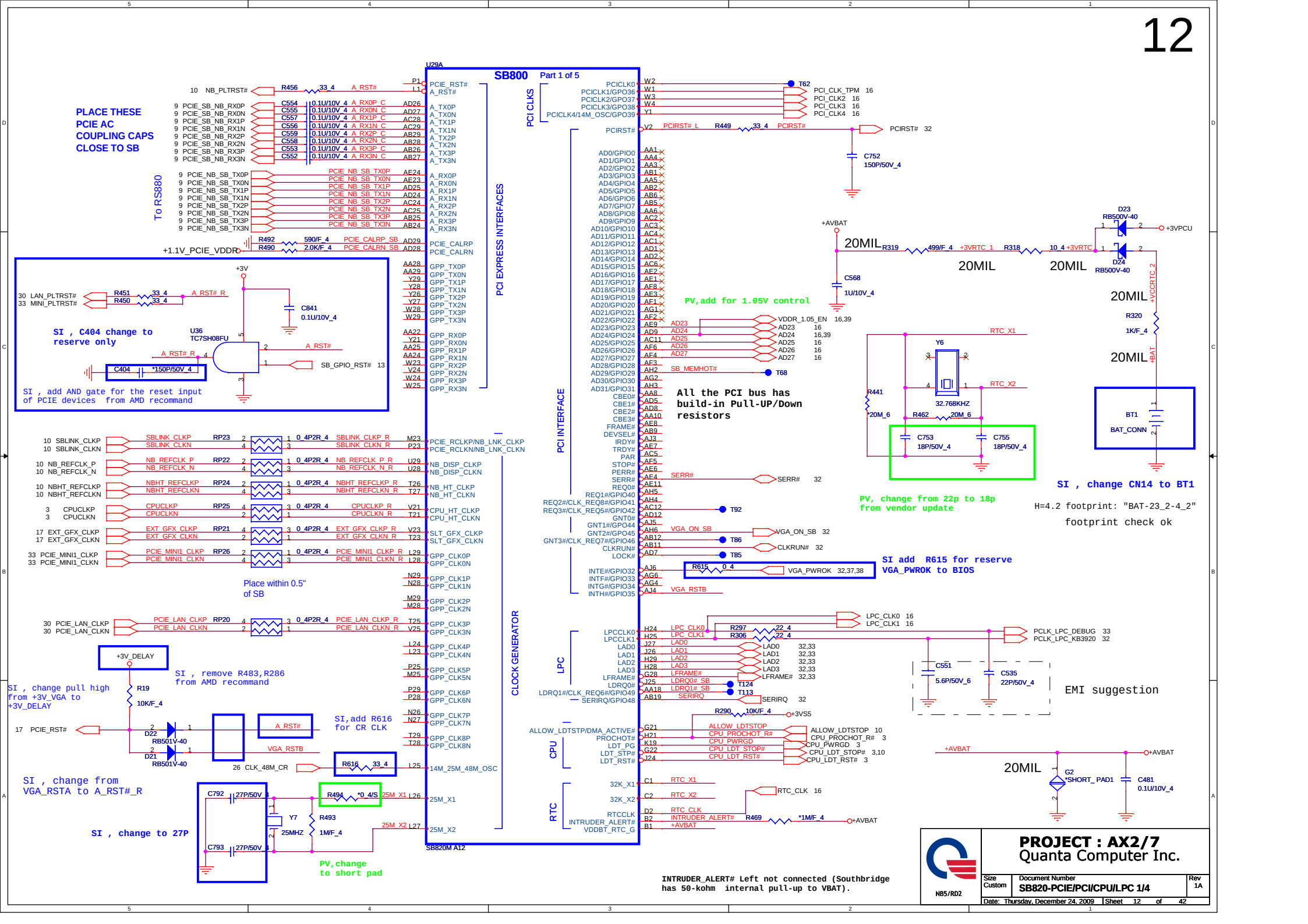
This is side port power DIS remove L55 , change C205 to 0 ohm and short to GND

PROJECT : AX2/7
Quanta Computer Inc.

NB5/RD2

Size	Document Number	Rev
Custom	RS880-POWER5/5	1A

Date: Tuesday, December 22, 2009 Sheet 11 of 42


U29A
SB800
Part 1 of 5
PCI CLKS
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC
To RS880
PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB
PCIE_RST#
A_RST#
PCIE_CALRP_SB
PCIE_CALRN_SB
PCIE_CALRP
PCIE_CALRN
+1.1V_PCIE_VDDR
SI , C404 change to reserve only
SI , add AND gate for the reset input of PCIE devices from AMD recommand
U36
TC7SH08FU
C404 *150P/50V_4
C841 0.1U/10V_4
SB_GPIO_RST# 13
PV,add for 1.05V control
All the PCI bus has build-in Pull-UP/Down resistors
SERR# 32
T68
T92
T86
T85
VGA_ON_SB 32
CLKRUN# 32
VGA_PWROK 32,37,38
SI add R615 for reserve VGA_PWROK to BIOS
VGA_RSTB
Place within 0.5" of SB
SI , remove R483,R286 from AMD recommand
SI , change pull high from +3V_VGA to +3V_DELAY
R19 10K/F_4
SI,add R616 for CR CLK
SI , change from VGA_RSTA to A_RST#_R
SI , change to 27P
C792 27P/50V
C793 27P/50V
Y7 25MHZ
R493 1M/F_4
R494 *0_4/S
PV,change to short pad
C752 150P/50V_4
C568 1U/10V_4
+AVBAT
20MIL
R319 499/F_4
R318 10_4
+3VRTC_1
+3VRTC
+3VPCU
D23 RB500V-40
D24 RB500V-40
+VCCRTC_2
R320 1K/F_4
+BAT
BT1
BAT_CONN
Y6 32.768KHZ
R441 *20M_6
R462 20M_6
C753 18P/50V_4
C755 18P/50V_4
PV, change from 22p to 18p from vendor update
SI , change CN14 to BT1
H=4.2 footprint: "BAT-23_2-4_2"
footprint check ok
C551 5.6P/50V_6
C535 22P/50V_4
EMI suggestion
C481 0.1U/10V_4
*SHORT_PAD1
INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).
SB820M A12
NB5/RD2
PROJECT : AX2/7
Quanta Computer Inc.
Size Custom
Document Number SB820-PCIE/PCI/CPU/LPC 1/4
Rev 1A
Date: Thursday, December 24, 2009
Sheet 12 of 42

NC,no install by default

+3VS5 R253 *2.2K_4 SB_TEST0
R470 *2.2K_4 SB_TEST1
R245 *2.2K_4 SB_TEST2

remove pull hi
(chip internal
have pull hi)

SI , Add SB_GPIO_RST#
form AMD recommand

+3VS5 SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it
R459 2.2K_4 SB_SMBCLK1
R460 2.2K_4 SB_SMBDATA1

+3V SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R312 2.2K_4 PCLK_SMB
R311 2.2K_4 PDAT_SMB

Clock gen/Robson/TV
tuner
/DDR2/DDR2
thermal/Accelerometer

+3V
R561 10K/F_4
RB501V-40 D38
37 VGA_REQ

SI , add R561,D38 for VGA_CLK_REQ

+3VS5 SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R296 2.2K_4 SB_SCLK2
R292 2.2K_4 SB_SDATA2
R576 *10K_4 SYS_RST#

PV,Reserve for system stable

+3VS5 R458 2.2K_4 DNBSWON#

+3V R457 4.7K_4 SUS_STAT#
R332 8.2K_4 WLAN_CLKREQ#
R334 8.2K_4 LAN_CLKREQ#

SI , add from HP request

To Azalia

ACZ_SDOUT R247 33_4 C478 *10P/50V_4 ACZ_SDOUT_AUDIO 27
ACZ_SYNC R251 33_4 C484 *10P/50V_4 ACZ_SYNC_AUDIO 27
PV, change to 27P
from EMI suggest
ACZ_BCLK R254 33_4 C479 27P/50V_4 BIT_CLK_AUDIO 27
ACZ_RST# R242 33_4 ACZ_RST#_AUDIO 27
ACZ_SDIN0 ACZ_SDIN0 27
Remove short pad

To Modem Board

ACZ_SDOUT R246 33_4 C477 *10P/50V_4 ACZ_SDOUT_AUDIO_MDC 28
ACZ_SYNC R248 33_4 C473 *10P/50V_4 ACZ_SYNC_AUDIO_MDC 28
ACZ_BCLK R256 33_4 C486 27P/50V_4 BIT_CLK_AUDIO_MDC 28
PV, change to 27P
from EMI suggest
ACZ_RST# R249 33_4 ACZ_RST#_AUDIO_MDC 28
ACZ_SDIN1 ACZ_SDIN1 28
Remove short pad

SB JTAG
CN32 +3VSUS C833 10P/50V_4
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
*S/W JTAG DEBUG

14 MEM_GEVEN# J2
RI# K1
T144 SPI_CS3# D3
T73 SUSB# E1
32 SUSB# SUSB# H1
32 SUSC# SUSC# F2
32 DNBSWON# SB_PWRGD_IN H5
16 SB_PWRGD_IN SUS_STAT# G6
10 SUS_STAT# SB_TEST0 B3
SB_TEST1 C4
SB_TEST2 F6
32 GATEA20 GATEA20 AD21
32 RCIN# RCIN# AE21
K2
32 KBSMI# J29
32 SCI# SCI# H2
SYS_RST# J1
30,33 PCIE_WAKE# H6
F3
3 CPU_THERMTRIP# J6
16 WD_PWRGD WD_PWRGD AC19
C500 100P/50V_4
32 RSMRST# RSMRST# G1
T119 AD19
30 LAN_CLKREQ# AA16
30,32 LAN_DISABLE# R444 *0_4 LAN_DISABLE# SB AB21
12 SB_GPIO_RST# AC18
T123 AF20
T114 AE19
27 ACZ_SPKR ACZ_SPKR AF19
6,7,33 PCLK_SMB PCLK_SMB AD22
6,7,33 PDAT_SMB PDAT_SMB AE22
SB_SMBCLK1 F5
SB_SMBDATA1 F4
33 WLAN_CLKREQ# AH21
VGA_REQ_R AB18
E1
T69 AJ21
T152 H4
8 SP_DDR3_RST# D5
T67 D7
T78 G5
T77 K3
T74 AA20
T121 EXT_SB_OSC
H3
D1
5 PM_THERM# R243 *0_4 SMBALERT# 1 E4
+3VS5 R244 10K/F_4 D4
SB_JTAG_TDO E8
SB_JTAG_TCK E7
SB_JTAG_TDI E7
SB_JTAG_RST# F8

R255 *10K/F_4
16 ACZ_SDOUT R455 *10K/F_4 M3
R453 *10K/F_4 N1
R454 *10K/F_4 L2
R452 *10K/F_4 M2
M1
M4
N2
P2

HD audio
interface is
3.3S5 voltage

PV,change from pull
high to pull low from
AMD update

SI , add pull up resistor
from AMD recommend

EMI suggestion

R483 10K/F_4 T1
R505 10K/F_4 T4
L6
+3VS5 R509 10K/F_4 L5
T9
U1
U3
T2
U2
T5
V5
R511 10K/F_4 P5
M5
P9
T7
P7
M7
P4
M9
R545 10K/F_4 V7
T118 E23
T166 E24
F21
T167 G29
D27
E28
E29
E27

SB800
Part 4 of 5
SB820M A12

PCI_PME#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#
CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQGG#/GPIO65/OSCIN
BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR
PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

ACPI / WAKE UP EVENTS
USB 1.1 USB MISC
GPIO
USB 2.0
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL

PV,remove workaround
PV,delete R272
SI,add R272 for PARK LP 14M CLK source

USBCLK/14M_25M_48M_OSC A10 CLK_48M_USB
USB_RCOMP G19 USB_RCOMP_SB R291 11.8K/F_6
USB_FSD1P/GPIO186 J10 USBP15+ 29
USB_FSD1N H11 USBP15- 29 BLUETOOTH
USB_FSD0P/GPIO185 H9 T83
USB_FSD0N J8 T82
USB_HSD13P B12 T99
USB_HSD13N A12 T88
USB_HSD12P F11 T90
USB_HSD12N E11 T100
USB_HSD11P E14 USBP11+ 26
USB_HSD11N E12 USBP11- 26 USB card reader
USB_HSD10P J12 USBP10+ 33
USB_HSD10N J14 USBP10- 33 WLAN Min-Card
USB_HSD9P A13 T103
USB_HSD9N B13 T87
USB_HSD8P D13 T105
USB_HSD8N C13 T94
USB_HSD7P G12 T101
USB_HSD7N G14 T96
USB_HSD6P G16 USBP6+ 29
USB_HSD6N G18 USBP6- 29 USB Connector
USB_HSD5P D16 USBP5+ 29
USB_HSD5N C16 USBP5- 29 USB Connector
USB_HSD4P B14 T148
USB_HSD4N A14 T150
USB_HSD3P E18 T109
USB_HSD3N E16 T112
USB_HSD2P J16 USBP2+ 23
USB_HSD2N J18 USBP2- 23 Carama USB
USB_HSD1P B17 T107
USB_HSD1N A17 T149
USB_HSD0P A16 USBP0+ 29
USB_HSD0N B16 USBP0- 29 USB Connector

CLK_48M_USB
C509 *2.2P/50V_4
for EMI

SCL2/GPIO193 D25 SB_SCLK2
SDA2/GPIO194 F23 SB_SDATA2
SCL3_LV/GPIO195 B26 SB_SCLK3 T168
SDA3_LV/GPIO196 E26 5159_RST_R# 5159_RST_R# 26
EC_PWM0/EC_TIMER0/GPIO197 F25
EC_PWM1/EC_TIMER1/GPIO198 E22
EC_PWM2/EC_TIMER2/GPIO199 F22 SB_GPIO199 SB_GPIO199 16
EC_PWM3/EC_TIMER3/GPIO200 F21 SB_GPIO200 SB_GPIO200 16 SPI/LPC define

KSI_0/GPIO201 G24
KSI_1/GPIO202 G25
KSI_2/GPIO203 E28
KSI_3/GPIO204 E29
KSI_4/GPIO205 D29
KSI_5/GPIO206 D28
KSI_6/GPIO207 C29
KSI_7/GPIO208 C28
KSO_0/GPIO209 B28
KSO_1/GPIO210 A27
KSO_2/GPIO211 B27
KSO_3/GPIO212 D26
KSO_4/GPIO213 A26
KSO_5/GPIO214 C26
KSO_6/GPIO215 A24
KSO_7/GPIO216 B25
KSO_8/GPIO217 A25
KSO_9/GPIO218 D24
KSO_10/GPIO219 B24
KSO_11/GPIO220 C24
KSO_12/GPIO221 B23
KSO_13/GPIO222 A23
KSO_14/GPIO223 D22
KSO_15/GPIO224 C22
KSO_16/GPIO225 A22
KSO_17/GPIO226 B22

NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB820-ACPI/GPIO/USB 2/4	1A

Date: Thursday, December 24, 2009 Sheet 13 of 42

SATA PORT 0,1,2,3 can support AHCI mode

PLACE SATA AC COUPLING CAPS CLOSE TO SB820

IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

SI define side port ID

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
1	0	0	Samsung
1	0	1	Hynix
0	0	0	No support side port

SATA1

SATA ODD

PLVDD_SATA-- SATA PLL POWER

XTLVDD_SATA-- SATA crystal power

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB820

NOTE:
R361 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

U29B

SB800
Part 2 of 5

SERIAL ATA

FLASH

HW MONITOR

SPI ROM

SB820M A12

SI , remove test point from AMD recommand

PV,change to short pad

For blue tooth & wireless merge card

SI , change to reserve only

SI define board ID

ID4	ID3	ID2	ID1	ID0	
0	0	0	0	0	AX2 UMA DF
0	0	0	0	1	AX7 UMA DF
0	0	0	1	0	AX2 PARK DF
0	0	0	1	1	AX7 PARK DF
0	0	1	0	0	AX2 UMA FF
0	0	1	0	1	AX7 UMA FF
0	0	1	1	0	AX2 PARK FF
0	0	1	1	1	AX7 PARK FF
0	1	0	1	0	AX2 M93 DF
0	1	0	1	1	AX7 M93 DF
0	1	1	1	0	AX2 M93 FF
0	1	1	1	1	AX7 M93 FF

PV define for M93

PROJECT : AX2/7
Quanta Computer Inc.

NB5/RD2

Size: Custom | Document Number: SB820-ACPI/GPIO/USB 2/4 | Rev: 1A

Date: Thursday, December 24, 2009 | Sheet 14 of 42

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

U29C

SB800

Part 3 of 5

SB820M A12

POWER

VDDQ--3.3V I/O power 131mA

VDD33_18--3.3V IDE I/O power
1.8V flash memory I/O power 71mA

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

Delete Cap and change +1.8V to pull low from AMD command , due to no IDE & flash mode

PV,change to short pad

PCIE_VDDR--PCIE I/O power 600mA

43mA

93mA

AVDD_SATA--SATA phy power 567mA

For support USB wakeup-->3V_S5

AVDDTX--USB Phy Analog I/O power 658mA

TBDmA

VDD-- S/B CORE power

510mA

CKVDD_1.1V--Internal clock Generator I/O power

TBDmA

S5_3.3--3.3v standby power

32mA

S5_1.1V--1.1V standby power

113mA

TBDmA

197mA

47mA

62mA

17mA

5mA

32mA

SI , remove R272 from AMD recommand

SI , remove L48

To meet SB800 SCL1.02: Separate ferrite bead is not required for VDDPL_33_USB_S, Del B603/600ohm bead.

U29E

SB800

GROUND

Part 5 of 5

SB820M A12

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB820-PWR/DECOUPLING 4/4	1A

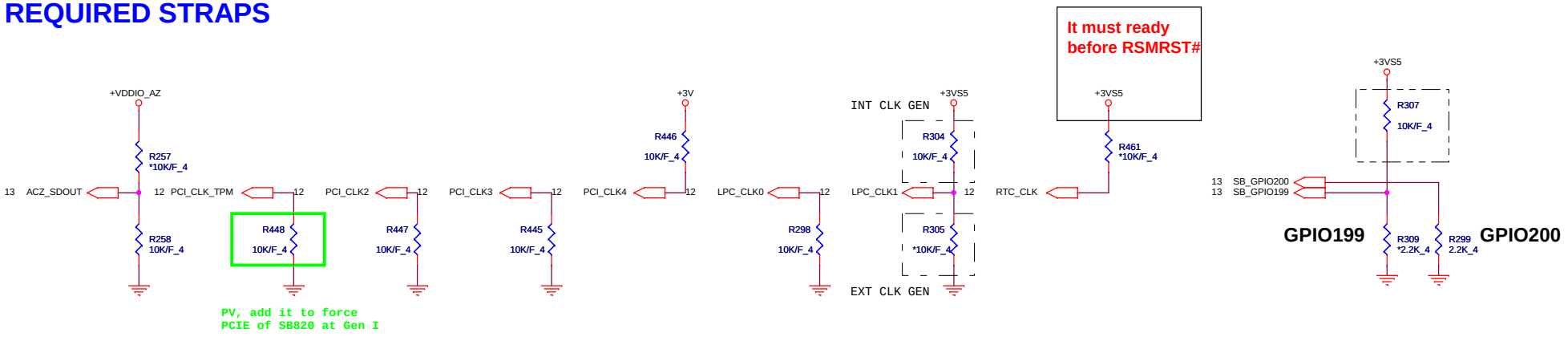
Date: Tuesday, December 22, 2009 | Sheet 15 of 42

NB5/RD2

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

intermal have pull Hi 10K , confirm AMD ward this pull Hi not need

REQUIRED STRAPS



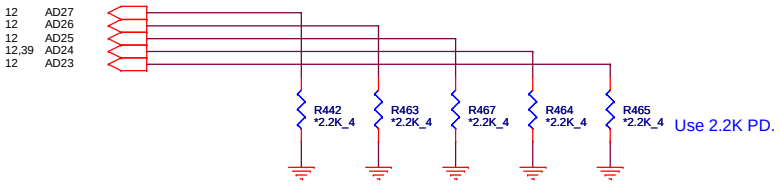
PV, add it to force PCIE of SB820 at Gen I

REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM

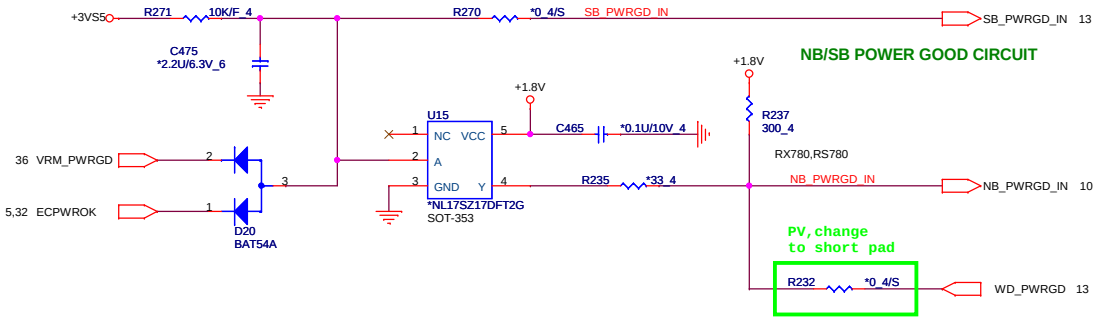
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



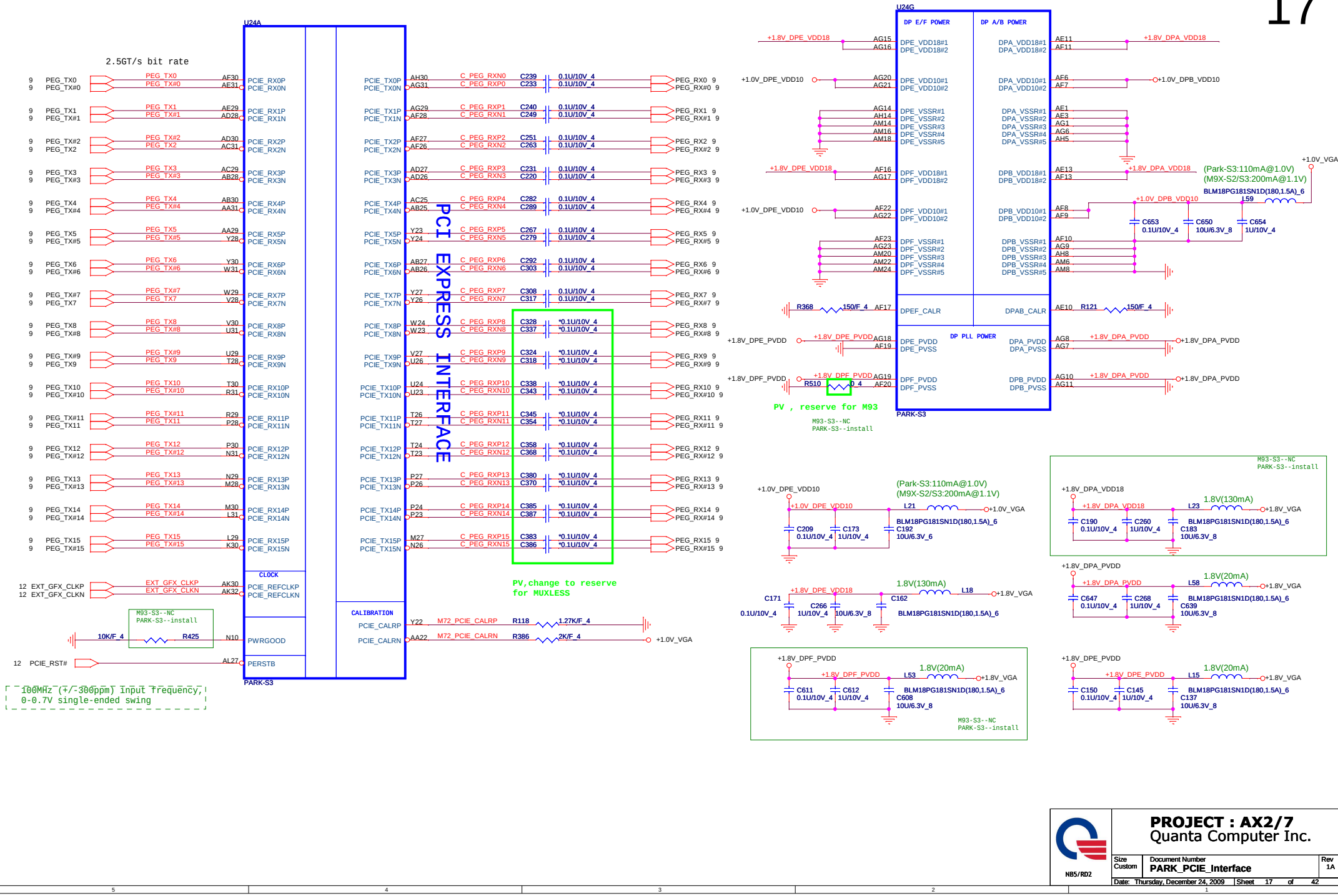
AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

PROJECT : AX2/7
Quanta Computer Inc.

NB5/RD2

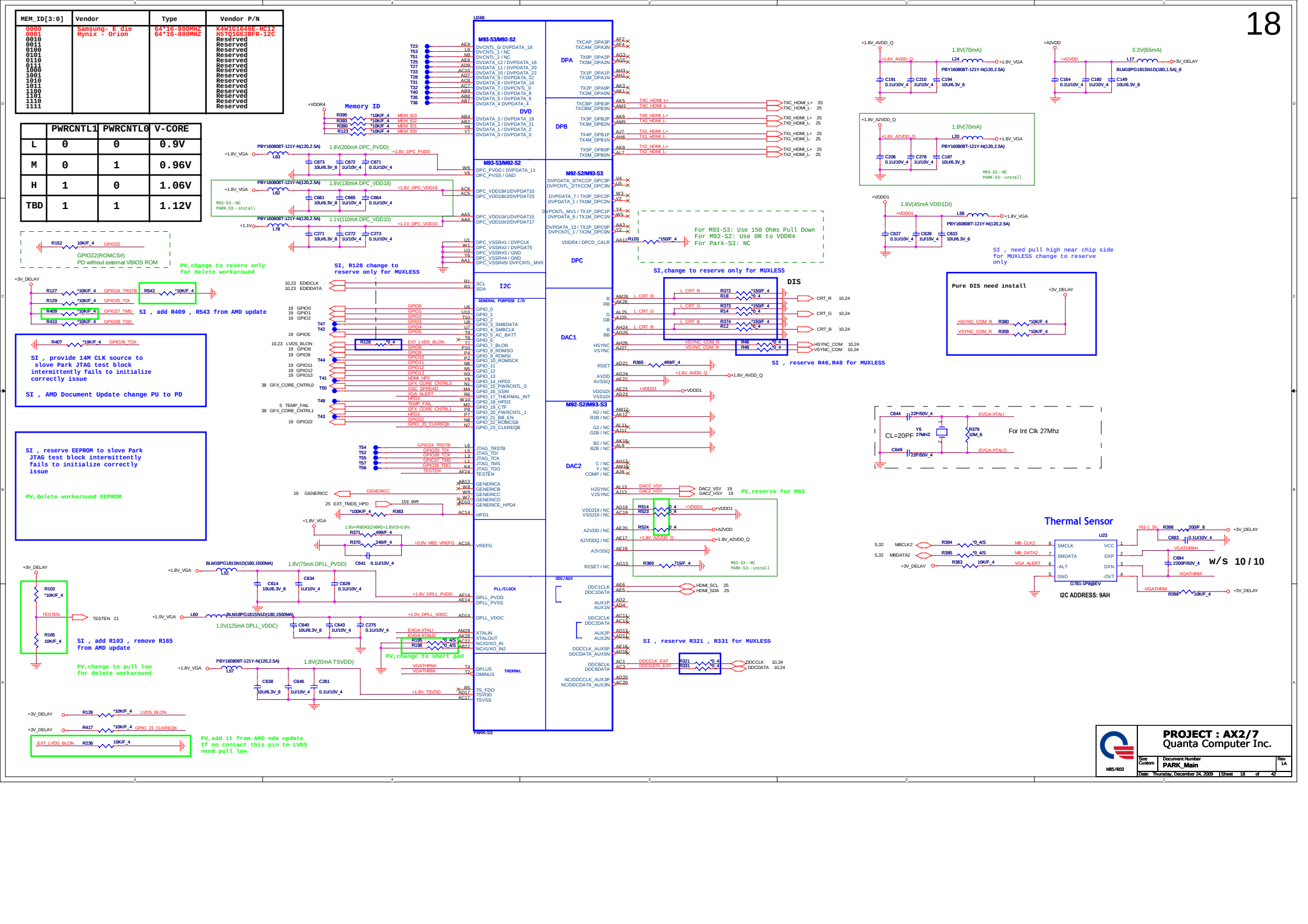
Size	Document Number	Rev
Custom	SB820-STRAPS	1A

Date: Thursday, December 24, 2009 Sheet 16 of 42


U24A
2.5GT/s bit rate
PCI EXPRESS INTERFACE
PEG_TX0 AF30 PCIE_RX0P
PEG_TX#0 AE31 PCIE_RX0N
PEG_TX1 AE29 PCIE_RX1P
PEG_TX#1 AD28 PCIE_RX1N
PEG_TX#2 AD30 PCIE_RX2P
PEG_TX2 AC31 PCIE_RX2N
PEG_TX3 AC29 PCIE_RX3P
PEG_TX#3 AB28 PCIE_RX3N
PEG_TX4 AB30 PCIE_RX4P
PEG_TX#4 AA31 PCIE_RX4N
PEG_TX5 AA29 PCIE_RX5P
PEG_TX#5 Y28 PCIE_RX5N
PEG_TX6 Y30 PCIE_RX6P
PEG_TX#6 W31 PCIE_RX6N
PEG_TX#7 W29 PCIE_RX7P
PEG_TX7 V28 PCIE_RX7N
PEG_TX8 V30 PCIE_RX8P
PEG_TX#8 U31 PCIE_RX8N
PEG_TX#9 U29 PCIE_RX9P
PEG_TX9 T28 PCIE_RX9N
PEG_TX10 T30 PCIE_RX10P
PEG_TX#10 R31 PCIE_RX10N
PEG_TX#11 R29 PCIE_RX11P
PEG_TX11 P28 PCIE_RX11N
PEG_TX12 P30 PCIE_RX12P
PEG_TX#12 N31 PCIE_RX12N
PEG_TX13 N29 PCIE_RX13P
PEG_TX#13 M28 PCIE_RX13N
PEG_TX14 M30 PCIE_RX14P
PEG_TX#14 L31 PCIE_RX14N
PEG_TX15 L29 PCIE_RX15P
PEG_TX#15 K30 PCIE_RX15N
CLOCK
EXT_GFX_CLKP AK30 PCIE_REFCLKP
EXT_GFX_CLKN AK32 PCIE_REFCLKN
M93-S3--NC
PARK-S3--install
10K/F_4 R425 N10 PWRGOOD
PCIE_RST# AL27 PERSTB
CALIBRATION
PCIE_CALRP Y22 M72_PCIE_CALRP R118 1.27K/F_4
PCIE_CALRN AA22 M72_PCIE_CALRN R386 2K/F_4 +1.0V_VGA
PCIE_RX0P AH30 C_PEG_RXN0 C239 0.1U/10V_4
PCIE_RX0N AG31 C_PEG_RXP0 C233 0.1U/10V_4
PCIE_RX1P AG29 C_PEG_RXP1 C240 0.1U/10V_4
PCIE_RX1N AF28 C_PEG_RXN1 C249 0.1U/10V_4
PCIE_RX2P AF27 C_PEG_RXP2 C251 0.1U/10V_4
PCIE_RX2N AF26 C_PEG_RXN2 C263 0.1U/10V_4
PCIE_RX3P AD27 C_PEG_RXP3 C231 0.1U/10V_4
PCIE_RX3N AD26 C_PEG_RXN3 C220 0.1U/10V_4
PCIE_RX4P AC25 C_PEG_RXP4 C282 0.1U/10V_4
PCIE_RX4N AB25 C_PEG_RXN4 C289 0.1U/10V_4
PCIE_RX5P Y23 C_PEG_RXP5 C267 0.1U/10V_4
PCIE_RX5N Y24 C_PEG_RXN5 C279 0.1U/10V_4
PCIE_RX6P AB27 C_PEG_RXP6 C292 0.1U/10V_4
PCIE_RX6N AB26 C_PEG_RXN6 C303 0.1U/10V_4
PCIE_RX7P Y27 C_PEG_RXP7 C308 0.1U/10V_4
PCIE_RX7N Y26 C_PEG_RXN7 C317 0.1U/10V_4
PCIE_RX8P W24 C_PEG_RXP8 C328 *0.1U/10V_4
PCIE_RX8N W23 C_PEG_RXN8 C337 *0.1U/10V_4
PCIE_RX9P V27 C_PEG_RXP9 C324 *0.1U/10V_4
PCIE_RX9N U26 C_PEG_RXN9 C318 *0.1U/10V_4
PCIE_RX10P U24 C_PEG_RXP10 C338 *0.1U/10V_4
PCIE_RX10N U23 C_PEG_RXN10 C343 *0.1U/10V_4
PCIE_RX11P T26 C_PEG_RXP11 C345 *0.1U/10V_4
PCIE_RX11N T27 C_PEG_RXN11 C354 *0.1U/10V_4
PCIE_RX12P T24 C_PEG_RXP12 C358 *0.1U/10V_4
PCIE_RX12N T23 C_PEG_RXN12 C368 *0.1U/10V_4
PCIE_RX13P P27 C_PEG_RXP13 C380 *0.1U/10V_4
PCIE_RX13N P26 C_PEG_RXN13 C370 *0.1U/10V_4
PCIE_RX14P P24 C_PEG_RXP14 C385 *0.1U/10V_4
PCIE_RX14N P23 C_PEG_RXN14 C387 *0.1U/10V_4
PCIE_RX15P M27 C_PEG_RXP15 C383 *0.1U/10V_4
PCIE_RX15N N26 C_PEG_RXN15 C386 *0.1U/10V_4
PEG_RX0 9 PEG_RX#0 9
PEG_RX1 9 PEG_RX#1 9
PEG_RX2 9 PEG_RX#2 9
PEG_RX3 9 PEG_RX#3 9
PEG_RX4 9 PEG_RX#4 9
PEG_RX5 9 PEG_RX#5 9
PEG_RX6 9 PEG_RX#6 9
PEG_RX7 9 PEG_RX#7 9
PEG_RX8 9 PEG_RX#8 9
PEG_RX9 9 PEG_RX#9 9
PEG_RX10 9 PEG_RX#10 9
PEG_RX11 9 PEG_RX#11 9
PEG_RX12 9 PEG_RX#12 9
PEG_RX13 9 PEG_RX#13 9
PEG_RX14 9 PEG_RX#14 9
PEG_RX15 9 PEG_RX#15 9
PARK-S3
PV,change to reserve for MUXLESS
100MHz (+/-300ppm) input frequency, 0-0.7V single-ended swing
U24G
DP E/F POWER
DP A/B POWER
DPE_VDD18#1 AG15
DPE_VDD18#2 AG16
DPA_VDD18#1 AE11
DPA_VDD18#2 AF11
+1.8V_DPE_VDD18
+1.8V_DPA_VDD18
DPE_VDD10#1 AG20
DPE_VDD10#2 AG21
DPA_VDD10#1 AF6
DPA_VDD10#2 AF7
+1.0V_DPE_VDD10
+1.0V_DPB_VDD10
DPE_VSSR#1 AG14
DPE_VSSR#2 AH14
DPE_VSSR#3 AM14
DPE_VSSR#4 AM16
DPE_VSSR#5 AM18
DPA_VSSR#1 AE1
DPA_VSSR#2 AE3
DPA_VSSR#3 AG1
DPA_VSSR#4 AG6
DPA_VSSR#5 AH5
DPB_VDD18#1 AF16
DPB_VDD18#2 AG17
DPB_VDD10#1 AF22
DPB_VDD10#2 AG22
DPB_VSSR#1 AF23
DPB_VSSR#2 AG23
DPB_VSSR#3 AM20
DPB_VSSR#4 AM22
DPB_VSSR#5 AM24
+1.0V_VGA
(Park-S3:110mA@1.0V)
(M9X-S2/S3:200mA@1.1V)
BLM18PG181SN1D(180,1.5A)_6
L59
C653 0.1U/10V_4
C650 10U/6.3V_8
C654 1U/10_4
DPEF_CALR AF17
R368 150/F_4
DPAB_CALR AE10
R121 150/F_4
DP PLL POWER
DPE_PVDD AG18
DPE_PVSS AF19
DPA_PVDD AG8
DPA_PVSS AG7
+1.8V_DPE_PVDD
+1.8V_DPA_PVDD
DPF_PVDD AG19
DPF_PVSS AF20
DPB_PVDD AG10
DPB_PVSS AG11
+1.8V_DPF_PVDD
R510 0_4
PV , reserve for M93
M93-S3--NC
PARK-S3--install
PARK-S3
(Park-S3:110mA@1.0V)
(M9X-S2/S3:200mA@1.1V)
L21
C209 0.1U/10V_4
C173 1U/10V_4
C192 10U/6.3V_6
1.8V(130mA)
L18
C171 0.1U/10V_4
C266 1U/10V_4
C162 10U/6.3V_8
BLM18PG181SN1D(180,1.5A)_6
L23
C190 0.1U/10V_4
C260 1U/10V_4
C183 10U/6.3V_8
1.8V(20mA)
L58
C647 0.1U/10V_4
C268 1U/10V_4
C639 10U/6.3V_8
L53
C611 0.1U/10V_4
C612 1U/10V_4
C608 10U/6.3V_8
L15
C150 0.1U/10V_4
C145 1U/10V_4
C137 10U/6.3V_8
+1.8V_VGA
+1.0V_VGA
+1.8V_DPA_PVDD
+1.8V_DPE_PVDD
+1.8V_DPF_PVDD
+1.8V_DPB_PVDD
NB5/RD2
PROJECT : AX2/7
Quanta Computer Inc.
Size Custom
Document Number PARK_PCIE_Interface
Rev 1A
Date: Thursday, December 24, 2009
Sheet 17 of 42

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Samsung- E die	64*16-800MHZ	K4W1G1646E-HC12
0001	Hynix - Orion	64*16-800MHZ	H5TQ1G63BFR-12C
0010	Reserved		
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		
1000	Reserved		
1001	Reserved		
1010	Reserved		
1011	Reserved		
1100	Reserved		
1101	Reserved		
1110	Reserved		
1111	Reserved		

	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0.9V
M	0	1	0.96V
H	1	0	1.06V
TBD	1	1	1.12V

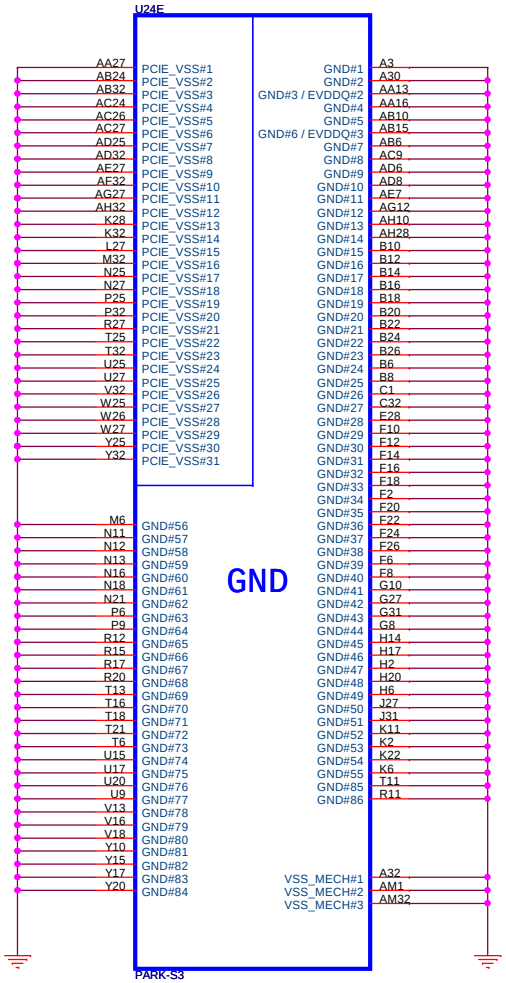


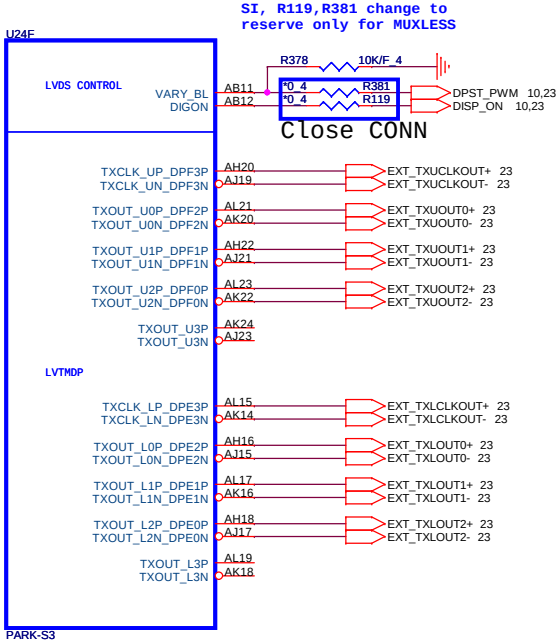
PROJECT : AX2/7
Quanta Computer Inc.

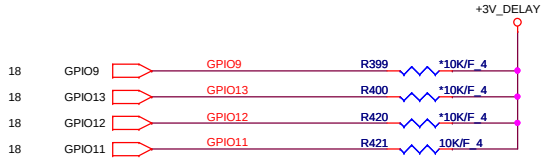
N85/RD2

Size	Document Number	Rev
Custom	PARK_Main	1A

Date: Thursday, December 24, 2009 | Sheet 18 of 42







CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

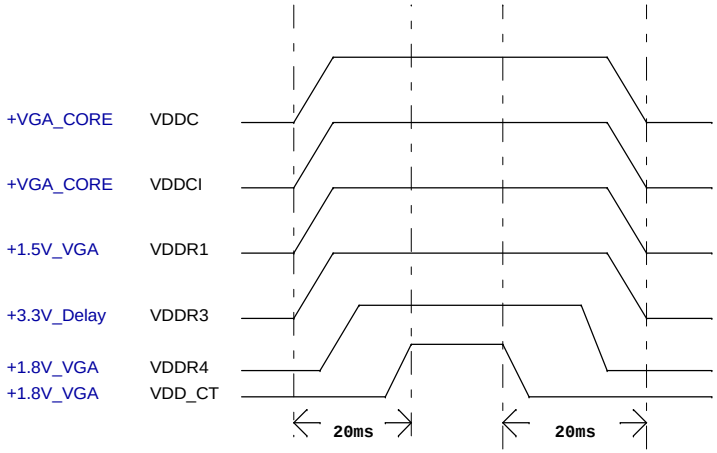
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

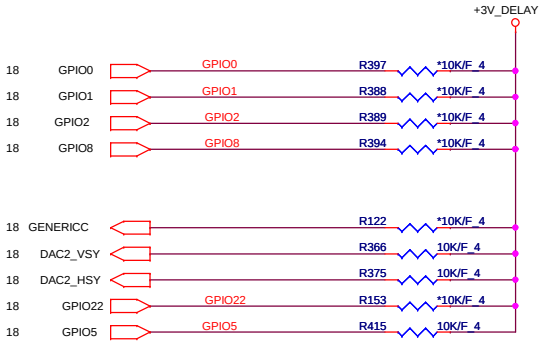
Power Up/Down Sequence



Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



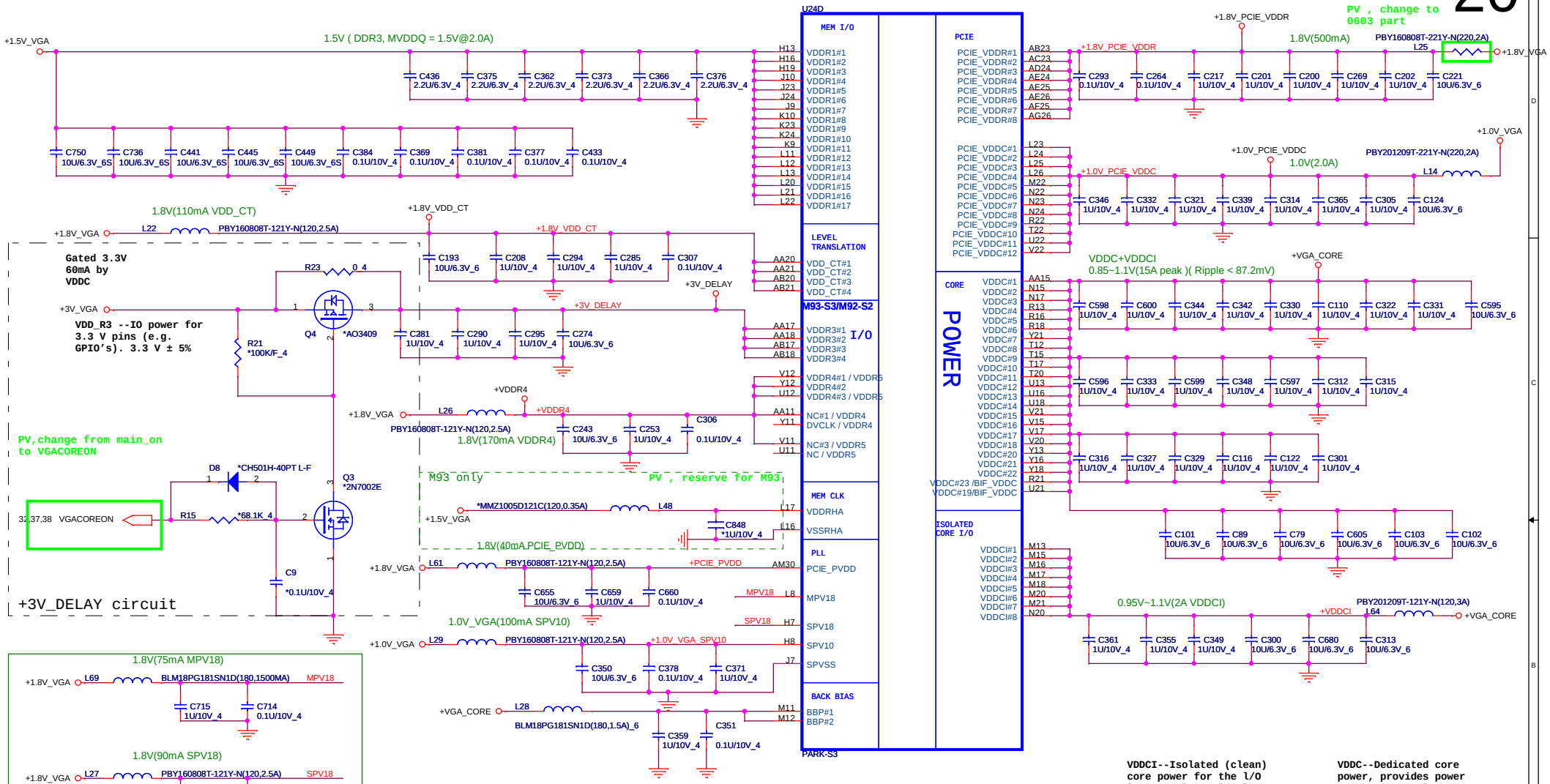
NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PARK_GND / LVDS/ Straps	1A

Date: Thursday, December 24, 2009 Sheet 19 of 42

PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%



VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC

VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)

PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%

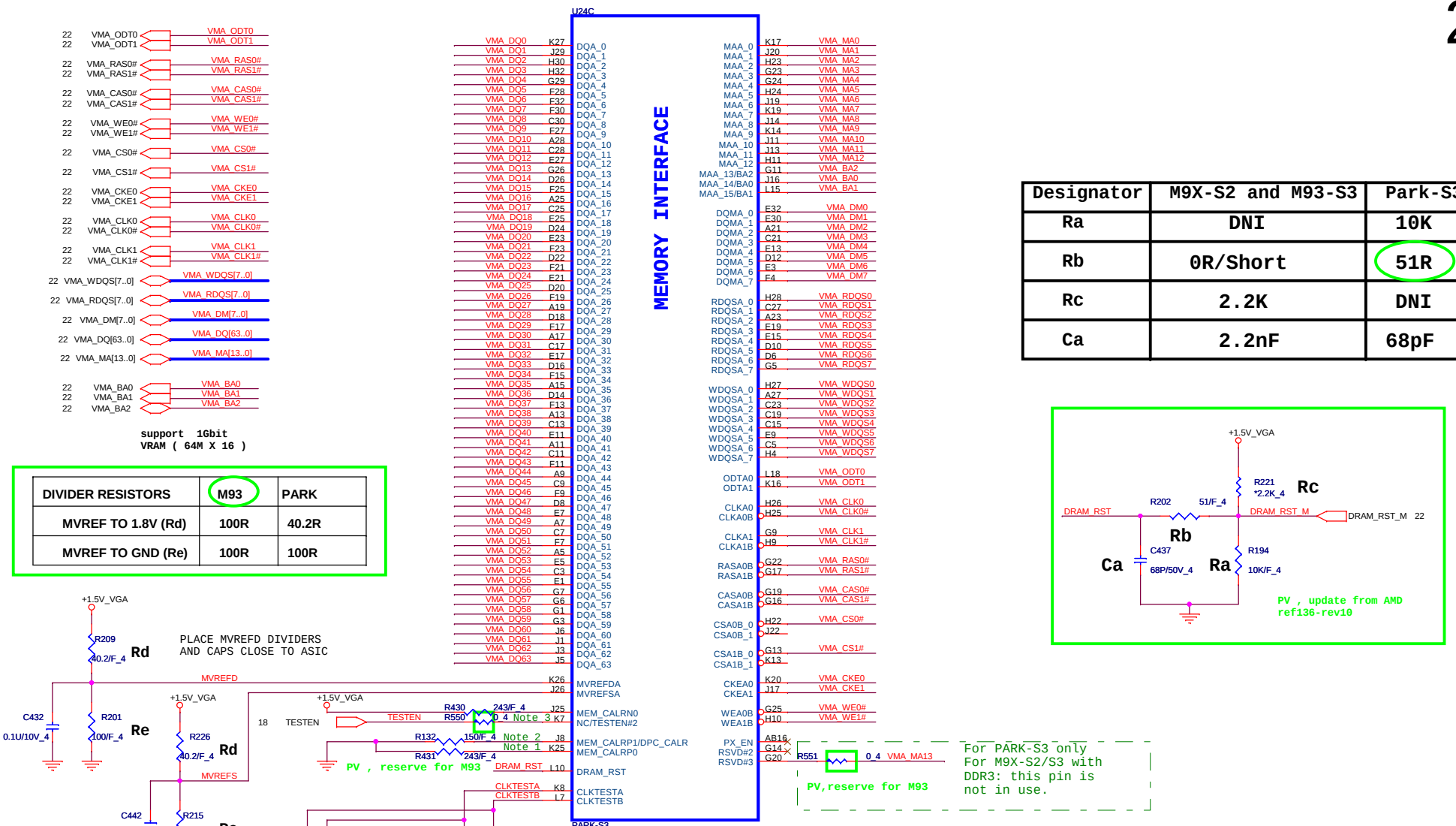
VDDRH_1 & VDDRH_2 --Dedicated power pins for memory clock pads for each channel. Should have the same voltage level as VDDR1.

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PARK_Power_and_NC	1A

NB5/RD2

Date: Thursday, December 24, 2009 | Sheet 20 of 42



Designator	M9X-S2 and M93-S3	Park-S3
Ra	DNI	10K
Rb	0R/Short	51R
Rc	2.2K	DNI
Ca	2.2nF	68pF

DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R

Note 1 :Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.
Note 2 :For M9X-S2/S3,J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
For Park-S3,J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR
Note 3 :For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected.
For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24

NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PARK/MEM_Interface	1A

Date: Thursday, December 24, 2009 | Sheet 21 of 42

512MB DDR3

21 VMA_MA[13..0]
21 VMA_DM[7..0]
VMA_MA[13..0]
21 VMA_DQ[63..0]
21 VMA_WDQS[7..0]
21 VMA_RDQS[7..0]

U13 / U26 / U12 / U27 — K4W1G1646E-HC12 (100-BALL SDRAM DDR3)

Should be 240 Ohms +-1%

R223 243/F_4 — R435 243/F_4 — R210 243/F_4 — R432 243/F_4

+1.5V_VGA

R439 4.99K/F_4 — R188 4.99K/F_4 — R437 4.99K/F_4 — R191 4.99K/F_4 — R231 4.99K/F_4 — R216 4.99K/F_4 — R434 4.99K/F_4 — R429 4.99K/F_4

R438 4.99K/F_4 — R192 4.99K/F_4 — R440 4.99K/F_4 — R197 4.99K/F_4 — R230 4.99K/F_4 — R227 4.99K/F_4 — R436 4.99K/F_4 — R433 4.99K/F_4

VREFC_VMA1 / VREFD_VMA1 / VREFC_VMA2 / VREFD_VMA2 / VREFC_VMA3 / VREFD_VMA3 / VREFC_VMA4 / VREFD_VMA4

C738 .1U/10V_4 — C434 .1U/10V_4 — C744 .1U/10V_4 — C727 .1U/10V_4 — C447 .1U/10V_4 — C443 .1U/10V_4 — C734 .1U/10V_4 — C726 .1U/10V_4

VMA_CLK0 — R206 56.2/F_4 — VMA_CLK0_COMM — C440 .01U/16V_4
VMA_CLK0# / VMA_CLK1 — R213 56.2/F_4
R199 56.2/F_4 — VMA_CLK1_COMM — C431 .01U/16V_4
R208 56.2/F_4 — VMA_CLK1#

+1.5V_VGA

C429 C430 C456 C444 C438 C428 C425 C747 1U/6.3V_4
C721 C719 C745 C424 C748 C739 C718 C716 1U/6.3V_4
C751 C749 C741 C448 C451 C454 C742 C746 1U/6.3V_4
C724 C722 C720 C729 C730 C735 C446 C450 1U/6.3V_4
C743 C723 C459 C461 C458 10U/6.3V_6S
C725 C737 C740 C728 C457 C460 C452 10U/6.3V_6S

	QCI PN
SAMSUNG	AKD5LGGT502
HYNIX	AKD5LZGTW00

NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

Size: Custom | Document Number: PARK VRAM(DDR3 BGA96) | Rev: 3A
Date: Thursday, December 24, 2009 | Sheet 22 of 42

1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

OPTION SIGNAL FROM NB to LVDS for UMA

OPTION SIGNAL FROM PARK to LVDS for discrete

SI, new option for MUXLESS

SI , add C21 from EMI suggest

SI, R34,R35 change to reserve only and add R33,R37 for MUXLESS

PV, add Q9 for BIOS check

Vari bright function

Do not use it

CAMERA

SI , update foortprint to 88266-05001-06-5P-L-SMT

Reserve for EMI

PROJECT : AX2/7	Quanta Computer Inc.
Size: Custom	Document Number: LCD CONN
Rev: 1A	
NB5/RD2	
Date: Thursday, December 24, 2009	Sheet 23 of 42

CRT PORT

PV , change footprint
to F3_2X1_65-2_8

PV , change footprint to
dsub-dsd-15aebb-15p-v-smt

R20 for UAM & MUXLESS use 140 ohm
for DIS use 150 ohm (AMD)

+5VCRT C6 0.1U/10V_4

F1 40 mils FUSE1A6V_POLY

40 MIL

CRT_R L3 BK1608LL680(0.2A,68)_6 CRT_R1
CRT_G L2 BK1608LL680(0.2A,68)_6 CRT_G1
CRT_B L1 BK1608LL680(0.2A,68)_6 CRT_B1

R20 140/F_4 R16 150/F_4 R11 150/F_4
C13 5.6P/50V_6 C10 5.6P/50V_6 C7 5.6P/50V_6
C8 5.6P/50V_6 C11 5.6P/50V_6 C12 5.6P/50V_6

close conn
within 600mils

EMI

CRT CONN
CN17

10,18 CRT_R CRT_R
10,18 CRT_G CRT_G
10,18 CRT_B CRT_B

C3 0.1U/10V_4

U1 AHCT1G125DCH
U2 AHCT1G125DCH

10,18 VSYNC_COM
10,18 HSYNC_COM

R1 *0_4/S CRTDDCCLK2
PR_VSYNC R5 33_4 CRTVSYNC
PR_HSYNC R6 33_4 CRTHSYNC
R8 *0_4/S CRTDDCDAT2

C1 *470P/50V_4 C2 *47P/50V_4 C4 *47P/50V_4 C5 *47P/50V_4

+3V_DELAY R4 *4.7K_4
+3V R3 4.7K_4

10,18 DDCCLK DDCCLK
Q1 2N7002E
DDCCLK2

+3V_DELAY R10 *4.7K_4
+3V R9 4.7K_4

10,18 DDCDATA DDCDATA
Q2 2N7002E
DDCDAT2

SI, R4,R10 change
to reserve only and
add R3,R9 for MUXLESS

R2 6.81K_4 R7 6.81K_4

+5VCRT +5VCRT CH501H-40PT +5V_CRT2 D3

D9 BAV99W CRT_R1
D7 BAV99W CRT_G1
D5 BAV99W CRT_B1
D1 BAV99W DDCCLK2
D2 BAV99W CRTVSYNC
D4 BAV99W CRTHSYNC
D6 BAV99W DDCDAT2

PV,add for ESD

NB5/RD2	PROJECT : AX2/7 Quanta Computer Inc.	
Size: Custom	Document Number: CRT	Rev: 1A
Date: Thursday, December 24, 2009	Sheet 24 of 42	

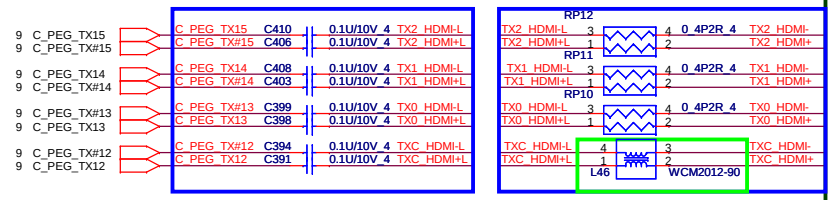
UMA/DISCRETE select for HDMI

From RS880M

SI , all add for MUXLESS

for Layout concern ,placement close north bridge

for Layout concern ,placement close HDMI conn

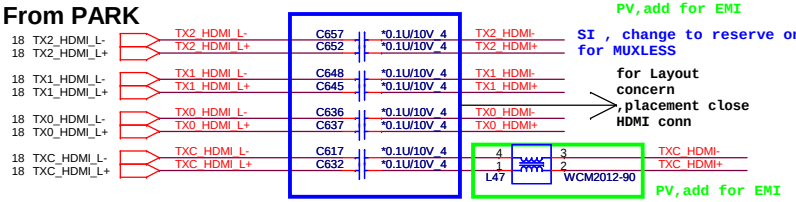


From PARK

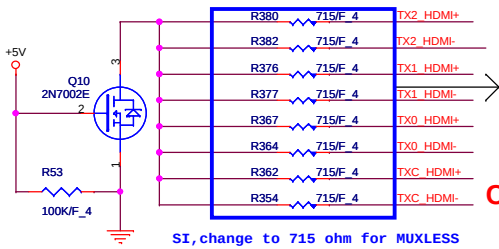
PV,add for EMI

SI , change to reserve only for MUXLESS

for Layout concern ,placement close HDMI conn



PV,add for EMI



UMA RS780M
上 715 ohm CS17152FB17

DIS M92-S
上 499 ohm CS14992FB24

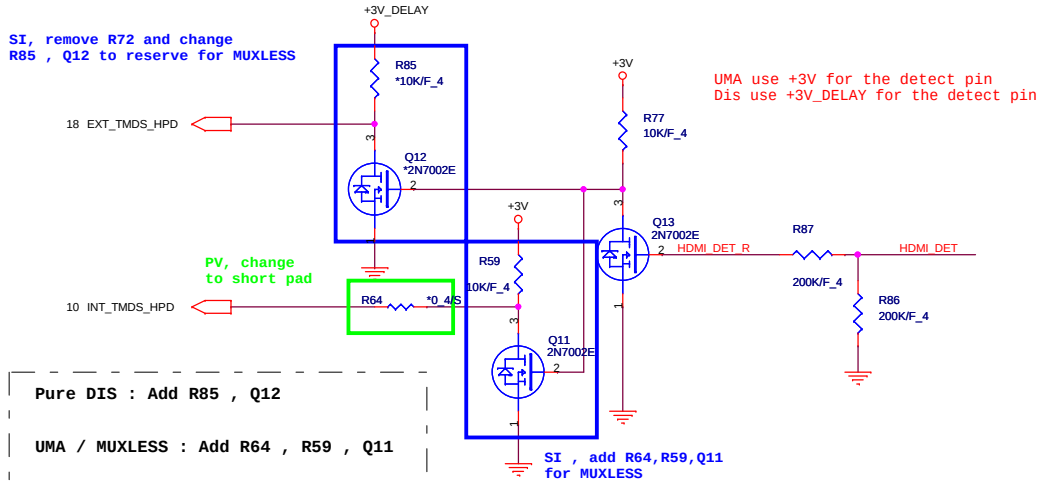
Close to HDMI Connector

SI,change to 715 ohm for MUXLESS

HDMI HPD SENSE

SI, remove R72 and change R85 , Q12 to reserve for MUXLESS

UMA use +3V for the detect pin
Dis use +3V_DELAY for the detect pin



Pure DIS : Add R85 , Q12

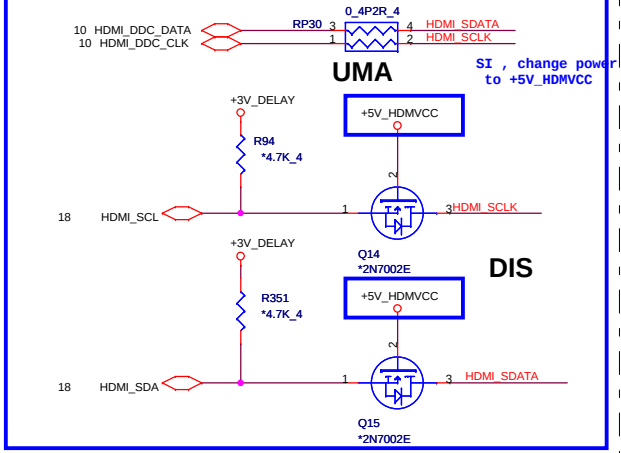
UMA / MUXLESS : Add R64 , R59 , Q11

SI , add R64,R59,Q11 for MUXLESS

UMA AND DISCRETE HDMI I2C SELECT

Close to HDMI Connector

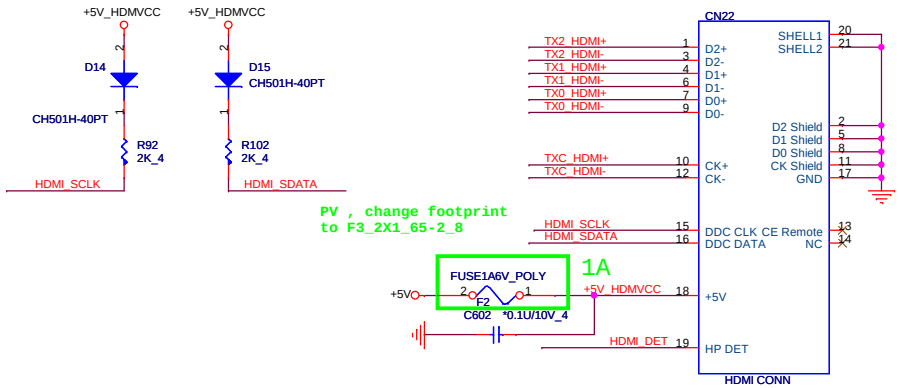
UMA DDC4 is 5V tolerance , the MOSFET level shifter no need
Discrete DDC is 3V tolerance,the MOSFET level shifter is need



SI , change power source to +5V_HDMVCC

SI, remove R93 , R350 . Add RP30 R94,R351,Q14,Q15 change to reserve only for MUXLESS

HDMI PORT



PV , change footprint to F3_2X1_65-2_8

PIN 13	CLK source	Remark
Floating	12M Hz	Xtal
Pull high	48M Hz	Input to RTS5159 pin48

SI , change CLK source from SB internal CLK GEN

AL005158B10 -->RTS5158E
AL005159B00 -->RTS5159GR

Note:

	SD/MMC	MS	XD
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

PV,change to short pad

SP7	R517 *0_4/S	MS-D0_SD-D0_XD-D6	
SP6	R515 *0_4/S	MS-D1_XD-D3_SD_D1	
SP8	R520 *0_4/S	MS-D2_XD-D2	
SP16	R535 *0_4/S	XD-RE#_SD-D2	
SP5	R513 *0_4/S	MS-BS_XD-D5	
SP15	R539 *0_4/S	SD-D3_XD-WE	
SP11	R527 *0_4/S	SD_CLK_MS_CLK	
SP2	R504 *0_4/S	SD_WP	
SP13	R533 *0_4/S	XD-WP#	
SP19	R541 *0_4/S	XD-CLE	
SP4	R507 *0_4/S	XD-D4	
SP10	R521 *0_4/S	MS-D3_XD-D7	
SP14	R534 *0_4/S	XD-RB#	
SP12	R528 *0_4/S	XD-D0	
SP17	R540 *0_4/S	XD-ALE	
SP18	R536 *0_4/S	XD-CE#	
SD_CMD_R	R529 *0_4/S	SD-CMD	

Realtek RTS5159

SI , change to 22P then change to reserve only

SI , Add R537 from vendor suggestion

Internal have pull H1 200K

RTS5159 max output current for ..
XD card 250mA
SD/MMC 250mA
MS/MSPRO 250mA

SI, change power source from +3VSUS to +3V

Close to Chipset

Can not more than 10p

PV, change to short pad

*RB501V-40

Add diode for 5158E cardreader driver lost issue

PV , change footprint to 4in1-cm4s-125-36p-r-v-smt

CARD READER SOCKET

5 IN1 CARD-READER (PUSH-PUSH)

Support SD/SD PRO/MMC/MS/MS PRO/xD Cards

VGA Hole

CPU Hole

SI , update foortprint to spad-ax2-1np

SI, add CPU & VGA hold pad from EMI request

SI , add for ESD testing

PV,add new pad for new outline

CLOSE CONN

PROJECT :	AX2/7
Quanta Computer Inc.	
Size: Custom	Document Number: RTS5159 & CR SOCKET &HOLE
Rev: 1A	
Date: Thursday, December 24, 2009	Sheet 26 of 42

NB5/RD2

PV , change to short pad

+3V R519 *0_6/S C830 1U/6.3V_4

+3V_DVDD
C819 1U/10V_4 C821 10U/6.3V_8 — Close to Pin1
C816 10U/6.3V_8 C817 1U/10V_4 — Close to Pin9

+5V
C812 10U/6.3V_8 C810 .1U/10V_4 — Close to Pin46
C822 10U/6.3V_8 C809 .1U/10V_4 — Close to Pin39

+5VAVDD
C782 10U/6.3V_6 C780 1U/10V_4 — AGND AGND — Close to Pin25
C784 10U/6.3V_8 C786 1U/10V_4 — AGND AGND — Close to Pin38

PV,delete C824
ACZ_SDIN0_R C815 *27P/50V_4
FOR EMI

PV, change to reserve only
+5V L74 *PBY201209T-221Y-N 1.3A +5VAVDD
C772 10U/6.3V_6
C774 4.7U/6.3V_6
C775 1U/6.3V_4
C783 .1U/10V_4
AGND

PV , change from 220 to 47

PV, change footprint and value

MIC1-VERFL MIC1-VERFR MIC2-VERFO
28 EARP_L R489 47/F_4 HP-L
28 EARP_R R488 47/F_4 HP-R
AGND C777 2.2U/6.3V_6 CPVEE
269CBN C776 269CBP 2.2U/6.3V_6
C778 10U/6.3V_6 AGND
C781 .1U/10V_4
C779 1U/10V_4 — Close to Pin27
AGND
+5VAVDD

U32
AGND 37 AVSS2
+5VAVDD 38 AVDD2
+5V 39 PVDD1
SPKL+ 40 SPK-L+
SPKL- 41 SPK-L-
42 PVSS1
43 PVSS2
SPKR- 44 SPK-R-
SPKR+ 45 SPK-R+
+5V 46 PVDD2
EAPD# 47 EAPD
48 SPDIFO
49–58 PGND
CBP CBN CPVEE HP-OUT-R HP-OUT-L MIC1-VREFO-L MIC1-VREFO-R MIC2-VREFO LDO-CAP VREF AVSS1 AVDD1
LINE1-R LINE1-L MIC1-R MIC1-L MONO-OUT JDREF Sense-B MIC2-R MIC2-L LINE2-R LINE2-L Sense A
DVDD1 GPIO0 GPIO1 PD# SDATA-OUT BIT-CLK DVSS2 SDATA-IN DVDD-IO SYNC RESET# PCBEEP
ALC270A-GR

Ditigal Analog

MIC1-VERFL R497 4.7K_4
MIC1-VERFR R491 4.7K_4
EXT_MIC1-R_C C789 4.7U/6.3V_6 EXT_MIC1-R_R R495 1K/F_4 EXT_MIC_R 28
EXT_MIC1-L_C C795 4.7U/6.3V_6 EXT_MIC1-L_R R496 1K/F_4 EXT_MIC_L 28
R498 20K/F_4 AGND — Place near CODEC
INT_MIC_R C801 4.7U/6.3V_6 INT_MIC
INT_MIC_L C803 4.7U/6.3V_6
Place near CODEC
SENSEA R502 39.2K/F_4 SA_A# — SA_A# 28
R501 20K/F_4 SA_B# — SA_B# 28

SA_A# -->EXT Ear Phone

SA_B# -->EXT MIC

+3V_DVDD
T169 T170
PD#
13 ACZ_SDOUT_AUDIO
13 BIT_CLK_AUDIO
PCBEEP
ACZ_RST#_AUDIO 13
ACZ_SYNC_AUDIO 13
+3V_DVDD
ACZ_SDIN0_R R512 33_4 ACZ_SDIN0 13

SI, remove R511
C814 *27P/50V_4
SI , change to reserve only

PV , add LDO
+5VAVDD
U33 G9191-475T1U
Vout Vin BYP GND EN
C842 1U/6.3V_4
R571 10K/F_4
C847 0.047U/25V_4
+5V
AGND

SI , remove L79,L80,L83,L84

Place near CODEC
SPKR-
C802 *180p/50V_4
C806 *1U/16V_6
C808 *180p/50V_4
SPKR+
SPKL-
C798 *180p/50V_4
C796 *1U/16V_6
C794 *180p/50V_4
SPKL+

SI , change L6,L7,L8,L9 to CX5AG601001 from EMI suggest

SPEAKER

Place near SPEAKER CONN
L9 L7 L6 L8 BLM15AG601SS1D
CN3 INT SPEAKER CONN
C45 C42 C46 C47 220P/50V_6

SI , add C42,C45,C46,C47 from EMI suggestion

SI , update foortprint to 88266-020L-2P-R-SMT

Place near CODEC
+5VAVDD +INTMIC_BIAS
R485 *10K/F_4
R484 *10K/F_4
C768 *1U/6.3V_4
U31 *TLV2461IDBVRG4
C762 *100P/50V_4
INT_MIC
INT_MIC_IN_C_R
R481 *10K/F_4
C761 *100P/50V_4
R480 *10K/F_4
C763 *270P/25V_4
PV, change to reserve only

MIC2-VERFO
R302 3K_4
C540 *.22U/25V_6
INT_MIC_IN_C
INT_MIC_IN L79 BLM15AG601SS1D
CN10 88266-020L
R301 *3K_4
PV,add for EMI
C541 *1U/6.3V_4
R300 *3K_4
C165 *220P/50V_6
AGND AGND
+5VAVDD

R427 0_6
PV , add R427

TO Internal Mic

PV,add for test
Place Under CODEC
R328 0_6 RC0603
R315 *0_6/S short0603
R261 *0_6/S short0603
R473 *0_6/S short0603
R313 *0_6/S short0603
R482 *0_6/S short0603
R506 *0_6/S short0603
AGND

PC-BEEP

C835 close to C820 and C820 close to chip

+5VAVDD
AGND C825 *0.047U/10V
PV , remove U33,C825,C811 C820,R523,R524 R510,R514
Add this circuit same as AX1/3
R566 10K/F_4
C811 .1U/10V_4 PCBBEP_R2 R546 47K_4 PCBBEP_L C820 .1U/10V_4 PCBEEP
Q36 2N7002E
13 ACZ_SPKR
R549 4.7K_4
C835 .1U/10V_4
R549 close to R546
AGND AGND

SI,remove U35,C681 , add D40 for audio function not stable

+3V_DVDD
R516 *10K_4
EAPD# ACZ_RST#_AUDIO
R522 0_4 *0_4 R518
EAPD# R
32 VOLMUTE#
D40 BAT54A
PD#

NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia 92HD75B2X5	1A

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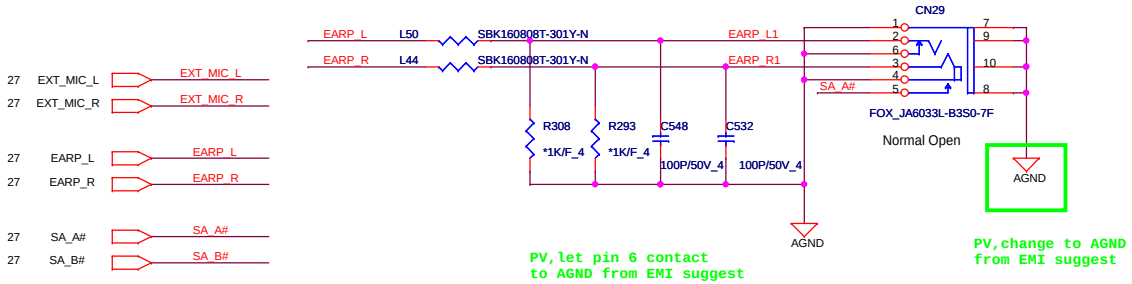
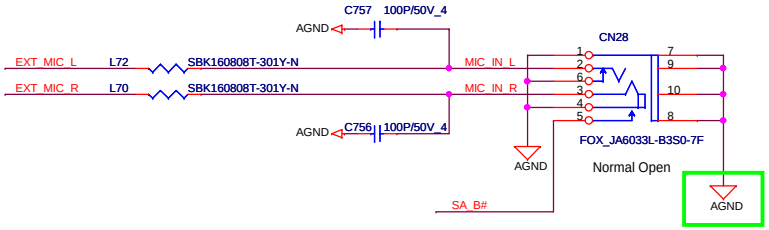
Line out



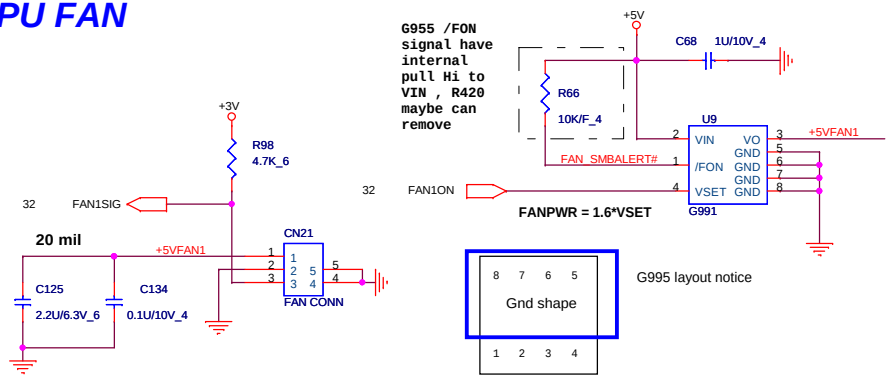
SA_A# -->EXT Ear Phone

SA_B# -->EXT MIC

MIC

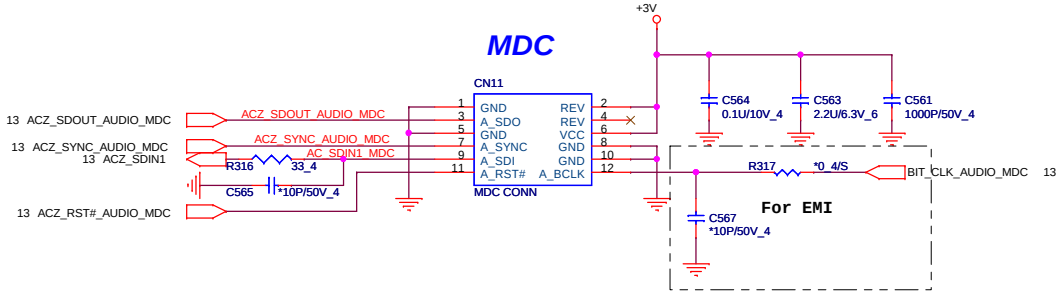


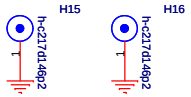
CPU FAN



Modem CONN

MDC

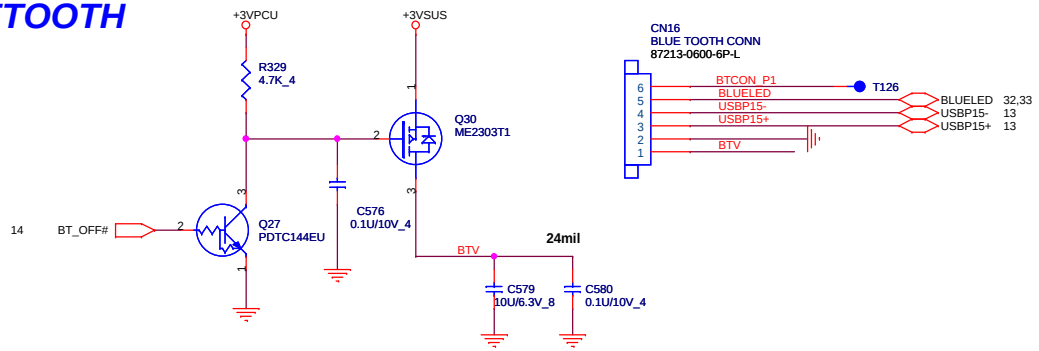




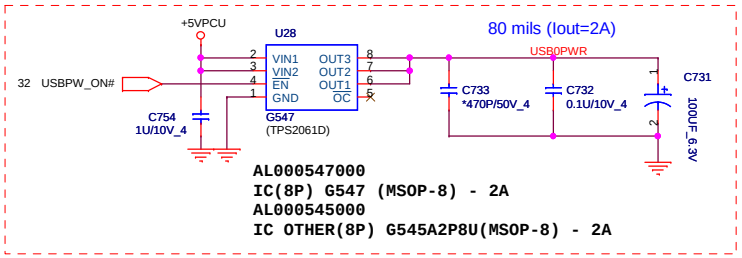
Nut PN:MBCA6002013

NB5/RD2	PROJECT : AX2/7 Quanta Computer Inc.	
Size: Custom	Document Number: AMP_TPA6017/MDC1.5/CPU FAN	Rev: 1A
Date: Thursday, December 24, 2009	Sheet 28 of 42	

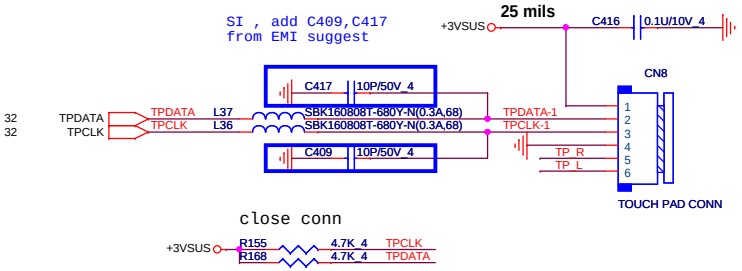
BLUETOOTH



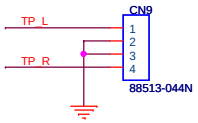
LEFT SIDE USBX2

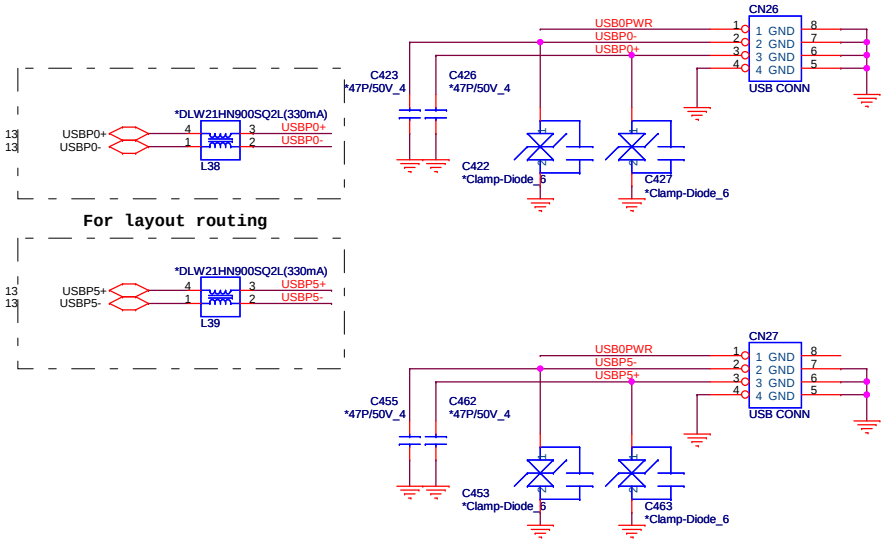


TOUCH PAD CONN



To TOUCH PAD SW board

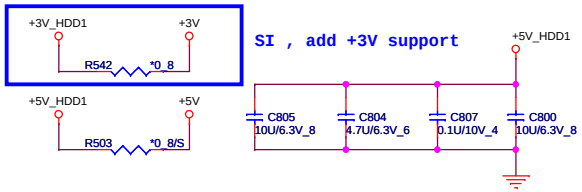


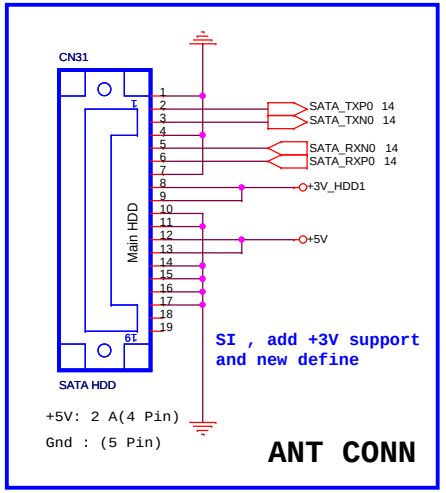


SATA HDD CONNECTOR

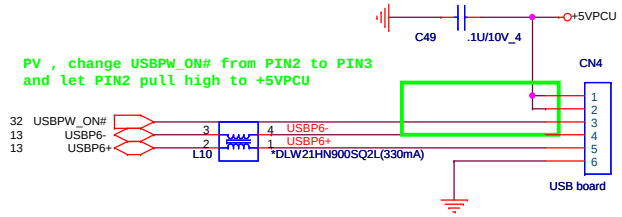
SI , update P/N : DFHS13FS019

SI , delete CN30 change to ANT CONN





Right SIDE USBX1



NB5/RD2	PROJECT : AX2/7 Quanta Computer Inc.	
Size: Custom	Document Number: BT/USBX3/TP/HDD	Rev: 1A
Date: Thursday, December 24, 2009	Sheet 29 of 42	

+CTRL12DVDD R40 *0_6/S

Power trace Layout 寬度> 30mil

+DVDD12

C54 .1U/10V_4 C52 .1U/10V_4 C107 .1U/10V_4 C88 .1U/10V_4

CLOSE to Pin 10, 13, 30, 36

+EVDD12

C67 1U/10V_4 C76 1U/10V_4

LAN-AGND

close to pin 19

SI , remove EEPROM
U5,C48,R42,R50

+3VLANVCC

Power trace Layout 寬度> 30mil

LANVCC
1.2W
364mA

C53 4.7U/6.3V_6 C109 .1U/10V_4

+3V_LAN

C56 .1U/10V_4 C55 .1U/10V_4

CLOSE to Pin 29,37

+3V_A_LAN

C604 .1U/10V_4 C601 *.1U/10V_4

CLOSE to Pin 1

+CTRL12DVDD

C97 10U/6.3V_8 C83 .1U/10V_4

R97 2.49K/F_4 LANRSET

+CTRL12A

C111 10U/6.3V_8 C108 .1U/10V_4

XTAL2 XTAL1 C62 33P/50V_4 Y2 25MHZ C69 33P/50V_4

LAN_WLED# +3V_LAN

U7

RTL8103EL

+3V_A_LAN

MDI0+ MDI0- MDI1+ MDI1-

+DVDD12

AVDD33 MDIP0 MDIN0 NC/FB12 MDIP1 MDIN1 GND1 NC/MDIP2 NC/MDIN2 DVDD12/AVDD12 NC/MDIP3 NC/MDIN3

VCTRL12A/SROUT12 GND4 RSET VCTR12DVDDSR NCVDDSR NC/ENSWRES CKTALL CKTALL NC/AVDD33 NC/LV_PLL LED0 VD33B

DVDD12B LED1/EESK LED2/EEDI LED3/EEDO EECS GND3 DVDD12A VDD33A ISOLATEB PERSTB LANWAKEB CLKREQB

EESK_LED100# EEDI_LED10# EECS ISOLATEB LAN_REST_R# PCIE_WAKE# R45 *0_4 R569 0_4

LAN_REST# 32
PCIE_WAKE# 13,33
LAN_CLKREQ# 13

PV, add for debug SI , add from HP request

SI , add for DSM

LAN CABLE DETECT 32

DVDD12 GND2 HSIP HSIN REFCLK_P REFCLK_N EVDD12 HSOP HSON EGND NC/SMCLK NC/SMDATA

+DVDD12 LAN-AGND

9 PCIE_TXP2_LAN
9 PCIE_TXN2_LAN
12 PCIE_LAN_CLKP
12 PCIE_LAN_CLKN

PCIE_LAN_CLKP PCIE_LAN_CLKN

PCIE_RXN2_LAN_L PCIE_RXP2_LAN_L C70 .1U/10V_4 C78 .1U/10V_4

PCIE_RXN2_LAN 9
PCIE_RXP2_LAN 9

+EVDD12

SI , change to AL08103EB01
for support DSM chip

+3V

Delete R261 and add D38 as current loss issue

R55 *1K/F_4 R44 100/F_4 ISOLATEB D13 *RB501V-40 LAN_DISABLE# 13,32 R51 15K/F_4

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

PV , add R333 pull high and R350 pull low to fix LAN LED behavior abnormal

R333 3.6K_4 +3V_LAN R350 1K/F_4

+3V_LAN

U6 C64 0.1U/10V_4

12 LAN_PLTRST#

TC7SH08FU

LAN_REST_R#

R60 *0_6/S R57 *0_6/S

LAN-AGND

DB modified to short-pad

HP request reserve
white LED driver circuit

LAN_WLED#

Q31 *DTC144EUA R404 *10K/F_4 +3VLANVCC

Q32 *DTC144EUA LAN_WLED# Q

LAN_WLED# R413 *0_4/S

PV, change
to short pad

SI , rotate 180 degree
for EMI suggestion

Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
LED0	O	57	38	
LED1	O	56	35	
LED2	O	55	34	
LED3	O	54	33	

LEDS1-0	00	01	10	11
LED0	Tx/Rx	Tx/Rx	Tx	Tx
LED1	LINK100	LINK	LINK	LINK100
LED2	LINK10	FULL	Rx	LINK10
LED3	NA	NA	NA	NA

LAN_Transformer

U20

LAN_MX1- LAN_MX1+ LAN_MCT1 LAN_MX0- LAN_MX0+ LAN_MCT0

RD+ RD- CT TD+ TD- CT

RX+ CT RX- TX- CMT TX+

MDI1- V_DAC_2 MDI1+ MDI0+ V_DAC_1 MDI0-

NS681684

75/F_4 R112 LAN_MCT0_2 C161 0.01U/100V_0603

75/F_4 R111 LAN_MCT0_1 C159 0.01U/100V_0603

C610 1000P/3KV_1808

C117 .01U/16V_4

C118 .01U/16V_4

SI , change footprint
to CC1808

Bios need change

EEDI_LED10# R392 *0_6

EESK_LED100# R391 *0_6/S

LAN_AMLED#

LAN_WLED#

LAN_WLED# C668 *.01U/16V_4 C699 *.01U/16V_4

EMI suggestion

C663 1U/10V_4

RJ45

CN25

+3V_LAN R387 330_4 LAN_AMLED LAN_AMLED#

LED_AMBER_P LED_AMBER_N

LAN_MX1- LAN_MX1+ LAN_MX0- LAN_MX0+

RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+ GND1 GND

+3V_LAN R403 330_4 LAN_WLED LAN_WLED# Q

LED_WHITE_P LED_WHITE_N

RJ45_CONN

C697 .1U/10V_4

EMI suggestion

Link

Fixed RJ45 Pin define (0829)

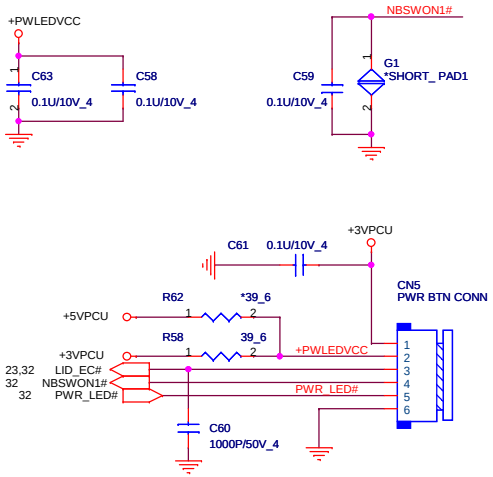
NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8102EL/RJ45	1A

Date: Thursday, December 24, 2009 Sheet 30 of 42

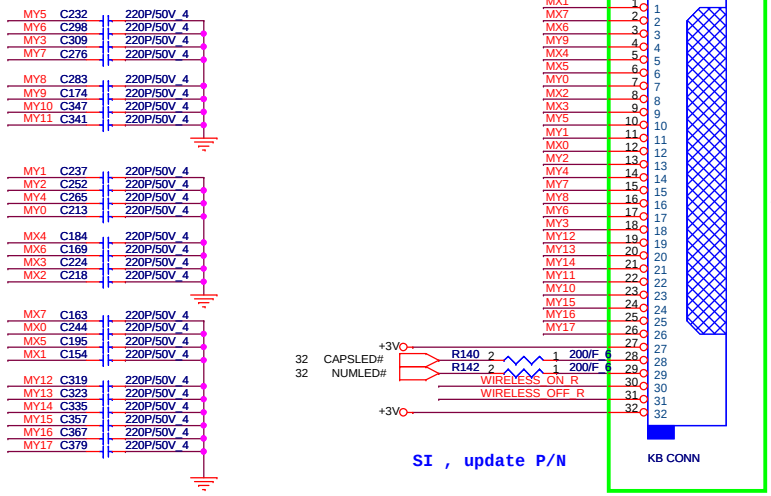
POWER BUTTON CONNECTOR



1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

KEYBOARD CONN

PV,update footprint to bl135h-32rla-tand-32p-l-smt

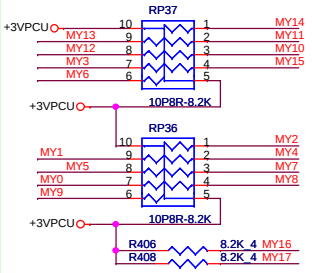


SI , update P/N

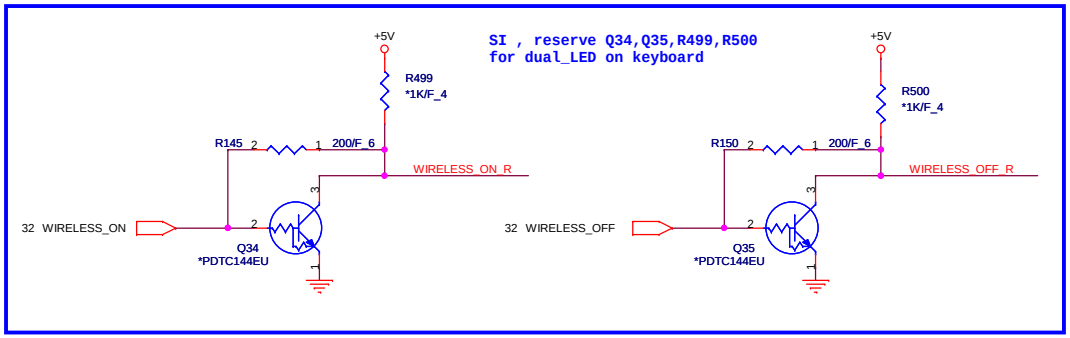
32 MY[0..17] MY[0..17]

32 MX[0..7] MX[0..7]

KEYBOARD PULL-UP

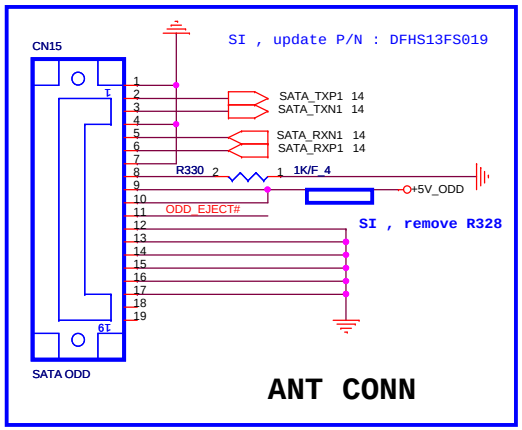


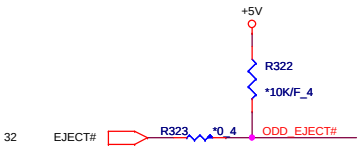
SI , reserve Q34,Q35,R499,R500 for dual_LED on keyboard

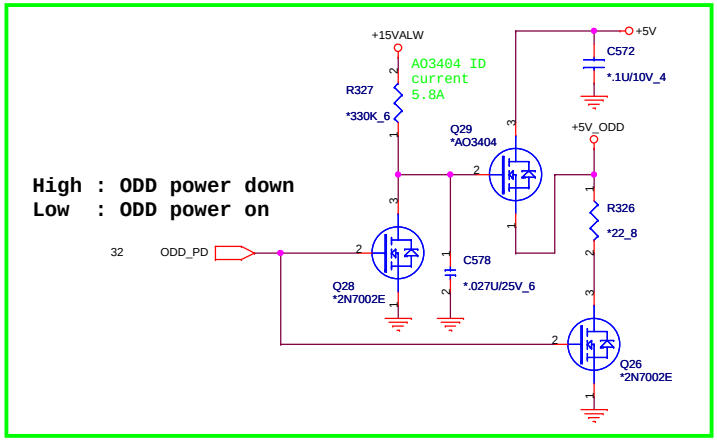


SATA CD-ROM

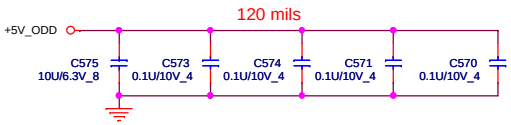
SI , delete CN13 change to ANT CONN

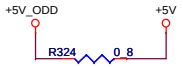






PV, change to reserve only





NB5/RD2	**PROJECT : AX2/7** Quanta Computer Inc.	
Size: Custom	Document Number: KEYBOARD/SW_BOARD/ODD	Rev: 1A
Date: Thursday, December 24, 2009	Sheet 31 of 42	

U8

SERIRQ
LFRAME#
LAD0
LAD1
LAD2
LAD3
PCICLK
PCIRST/GPIO5
CLKRUN
SCI/GPIOE
GA20/GPIO0
KBRST/GPIO1
ECRST
KSI0/GPIO30
KSI1/GPIO31
KSI2/GPIO32
KSI3/GPIO33
KSI4/GPIO34
KSI5/GPIO35
KSI6/GPIO36
KSI7/GPIO37
KSO0/GPIO20
KSO1/GPIO21
KSO2/GPIO22
KSO3/GPIO23
KSO4/GPIO24
KSO5/GPIO25
KSO6/GPIO26
KSO7/GPIO27
KSO8/GPIO28
KSO9/GPIO29
KSO10/GPIO2A
KSO11/GPIO2B
KSO12/GPIO2C
KSO13/GPIO2D
KSO14/GPIO2E
KSO15/GPIO2F
KSO16/GPIO48
KSO17/GPIO49
PSCLK1/GPIO4A
PSDAT1/GPIO4B
PSCLK2/GPIO4C
PSDAT2/GPIO4D
PSCLK3/GPIO4E
PSDAT3/GPIO4F
RD
WR
SELMEM/SPICS
SELIO/GPIO50
AD5/GPI43
D0/GPXD0
D1/GPXD1
D2/GPXD2
D3/GPXD3
D4/GPXD4
D5/GPXD5
D6/GPXD6
D7/GPXD7
A0/GPXA0
A1/GPXA1
A2/GPXA2
A3/GPXA3
A4/GPXA4
A5/GPXA5
A6/GPXA6
A7/GPXA7
A8/GPXA8
A9/GPXA9
A10/GPXA10
A11/GPXA11
V18R
VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
AVCC
AD0/GPI38
AD1/GPI39
AD2/GPI3A
AD3/GPI3B
DA0/GPO3C
DA1/GPO3D
DA2/GPO3E
DA3/GPO3F
PWM1/GPIOF
PWM2/GPIO10
FANPWM1/GPIO12
FANPWM2/GPIO13
FANFB1/GPIO14
FANFB2/GPIO15
SCL1/GPIO44
SDA1/GPIO45
SCL2/GPIO46
SDA2/GPIO47
GPIO4
GPIO7
GPIO8
GPIOA
GPIOB
GPIOC
GPIOD
GPIO11
GPIO16
GPIO17
GPIO18
GPIO19
GPIO1A
GPIO40
GPIO41
AD4/GPI42
GPIO52
GPIO53
GPIO54
GPIO55
GPIO56
GPIO57
GPIO58
GPIO59
XCLKO
XCLKI
GND1
GND2
GND3
GND4
GND5
AGND
KB3926

C584 4.7U/6.3V_6
C143 0.1U/10V_4
C590 0.1U/10V_4
C592 0.1U/10V_4
C589 0.1U/10V_4
C586 0.1U/10V_4
C591 0.1U/10V_4
C131 4.7U/6.3V_6
+3VPCU_EC

TEMP_MBAT 40
AD_TYPE
AD_AIR 40
SYS_I 40
CC-SET
CC-SET 40
CELL_SLT 40
FAN1ON 28
D/C# 40
PWM_VADJ
KEY_BEEP (1KHz)
PWM_VADJ 23
T91
EC_ACLIM
EC_ACLIM 40
FAN1SIG 28
ODD_PD 31
MBCLK
MBDATA
MBCLK2
MBDATA2
MBCLK 5,40
MBDATA 5,40
MBCLK2 5,18
MBDATA2 5,18
SUSB#
SUSB# 13
HWPG
HWPG 23,34,35,37,39
CPU_PROCHOT#
CPU_PROCHOT# 3
SUSC#
SUSC# 13
M93_STRP
T5
NBSWON1#
NBSWON1# 31
LAN_REST# 30
EC_DEBUG1 33
EMU_LID
EMU_LID 23
KBSMI#1
VRON
NUMLED#
VRON 35,36,37,39
NUMLED# 31
EJECT#
EJECT# 31
T9
T10
OP_FAN_SEL
DNBSWON#1
CAPSLED#
CAPSLED# 31
PWR_LED#
PWR_LED# 31
ECPWROK
ECPWROK 5,16
RSMRST#
RSMRST# 13
VOLMUTE#
VOLMUTE# 27
SPI_CLK
LID_EC#
LID_EC# 23,31
CRY2
CRY1
C57 27P/50V
C50 27P/50V
32.768KHZ
Y1

+3V R71 10K/F_4 HWPG
+3VPCU R78 10K/F_4 NBSWON1#
R74 10K/F_4 SLPBTN#
R346 4.7K_4 MBCLK
R345 4.7K_4 MBDATA
RSMRST# RSMRST# 13
+3VPCU R336 *8.2K_4
C588 2.2U/6.3V_6

PV , change to test point

Battery charge/discharge
Cap button
VGA thermal
system thermal

SI , add for DSM

12 SERR# R61 *0_4/S
12 VGA_ON_SB
12,37,38 VGA_PWROK
T1
T2
33 RF_LINK#
30 LAN CABLE DETECT
T3
29 USBPW_ON#
37,39 SUSON
34,37,39,40 MAINON
39 LAN_POWER
35,39 S5_ON
39 VR2.5_ON
13,30 LAN_DISABLE#
20,37,38 VGACOREON
40 MBATLED0#
40 AC_LED_ON#
31 WIRELESS_ON
31 WIRELESS_OFF
40 ACIN
29 TPCLK
29 TPDATA
SLPBTN#
Vari_ON
ACIN
TPCLK
TPDATA
BIOS_RD#
BIOS_WR#
BIOS_CS#
VGA_ON_SB
VGA_PWROK
RF_LINK#
BLUELED
USBPW_ON#
SUSON
MAINON
LAN_POWER
S5_ON
VR2.5_ON
VGACOREON
MBATLED0#
AC_LED_ON#

C585 0.1U/10V_4
C587 4.7U/6.3V_6
For KB3926 C version

PV, change from 18p to 27p
from vendor update

SI , change package

SI , enable Vari-bright
need pull low

+3VPCU
R65 *10K/F_4
Vari_ON
R68 10K/F_4

+3VPCU
C80 0.1U/10V_4
U17
BIOS_CS#
SPI_CLK
BIOS_WR#
BIOS_RD#
R89 33_4
R84 10K/F_4 SPI_3P
CE# VDD
SCK
SI
SO HOLD#
WP# VSS
SPI_7P
R76 10K/F_4
MX25L1605DM2I-12G

MAX AKE38FP0Z00 2M byte
WINBOND AKE38FP0N01 SPI
EON AKE38ZA0Q00 BIOS
SOCKET DG008000031

M93_STRP
R552 *1K/F_4

PV,reserve for identify M93-LP VGA chip

Project Model	GPIO42
AX 14"	High
AX 15.6"	Low
AX 17.3"	Middle (1.5V)

GPIO42 control fan table

OP_FAN_SEL R79 10K/F_4
R90 *10K/F_4 +3VPCU

3920_RST# 3920_RST# 5
+3VPCU R105 47K_4
C144 0.1U/10V_4
29,33 BLUELED BLUELED R41 100K/F_4

SCI1# D25 CH501H-40PT SCI# 13
DNBSWON#1 D12 RB500V-40 DNBSWON# 13
KBSMI#1 D27 RB500V-40 KBSMI# 13

Change D12, D16 to RB500
for current loss

MAINON C464 2200P/50V_4
PV,add for EMI

+3VPCU_EC
+3VPCU
L13
*SBK160808T-680Y-N(0.3A,68)
U19
VOUT VIN
SHDN
NR/FB GND
TPS73133
C114 4.7U/6.3V_6
C130 *1U/6.3V_4
C613 *1U/6.3V_4
+5VPCU

+3VPCU
D26 1SS355
AD_TYPE R109 100/F_4 AD_ID 40
C147 0.1U/10V_4
R108 24.3K/F_4

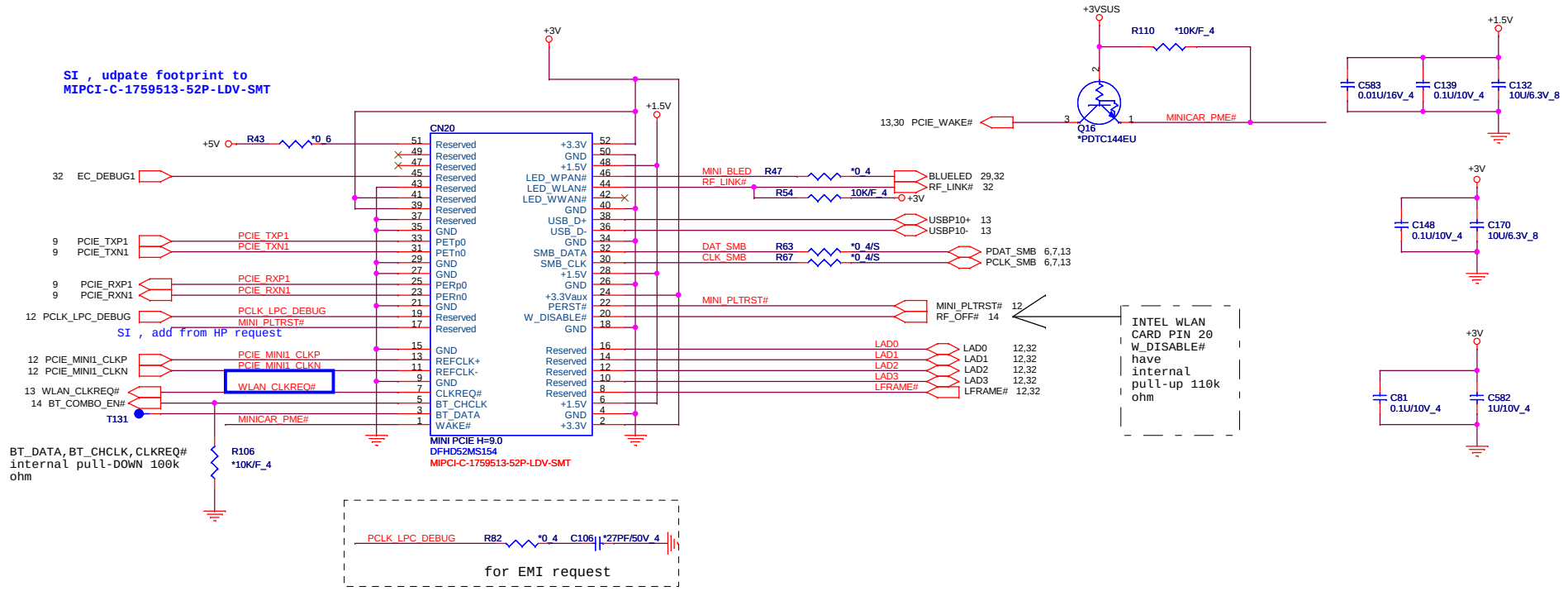
NB5/RD2

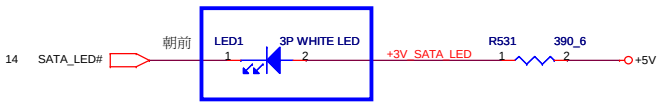
PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB3926/ROM/TP	1A

Date: Thursday, December 24, 2009 Sheet 32 of 42

Mini PCI-E Card 1 WLAN

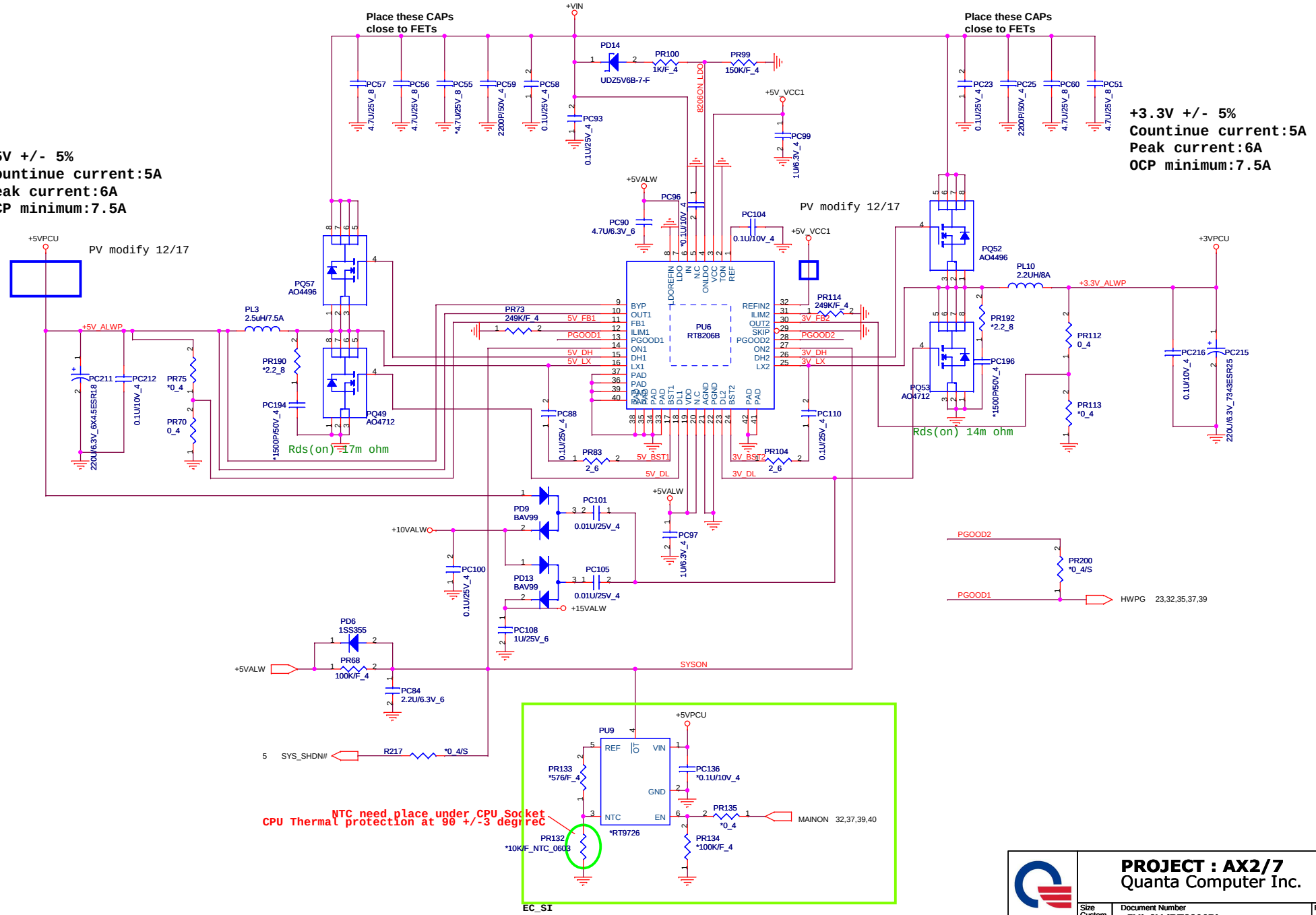




SI , change footprint to ledl-s110kgct-3p-nb5

NB5/RD2	PROJECT : AX2/7 Quanta Computer Inc.		
	Size: Custom	Document Number: Mini CARD/LED	Rev: 1A
	Date: Thursday, December 24, 2009	Sheet 33 of 42	

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

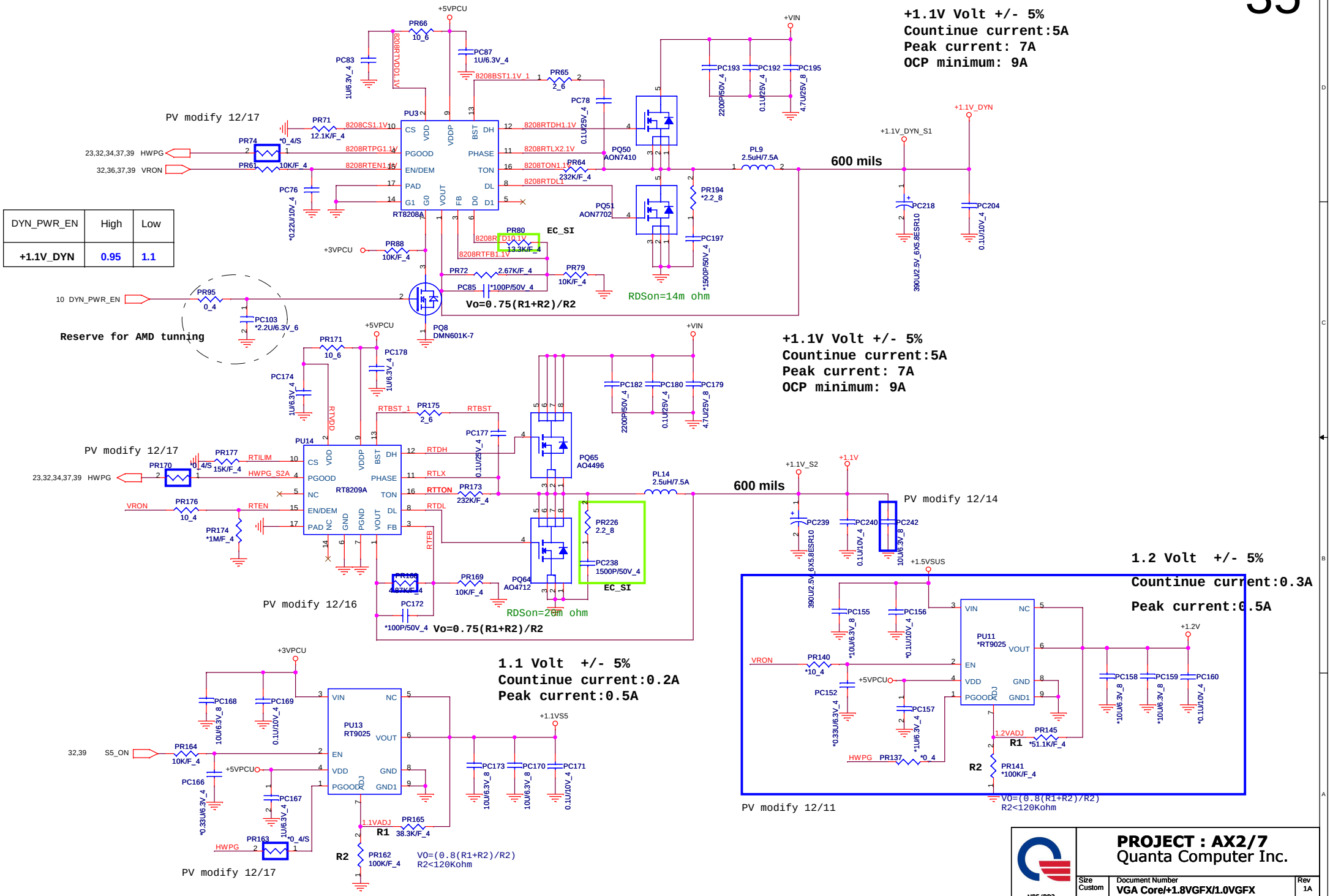


PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+5V/+3V (RT8206B)	1A

NB5/RD2

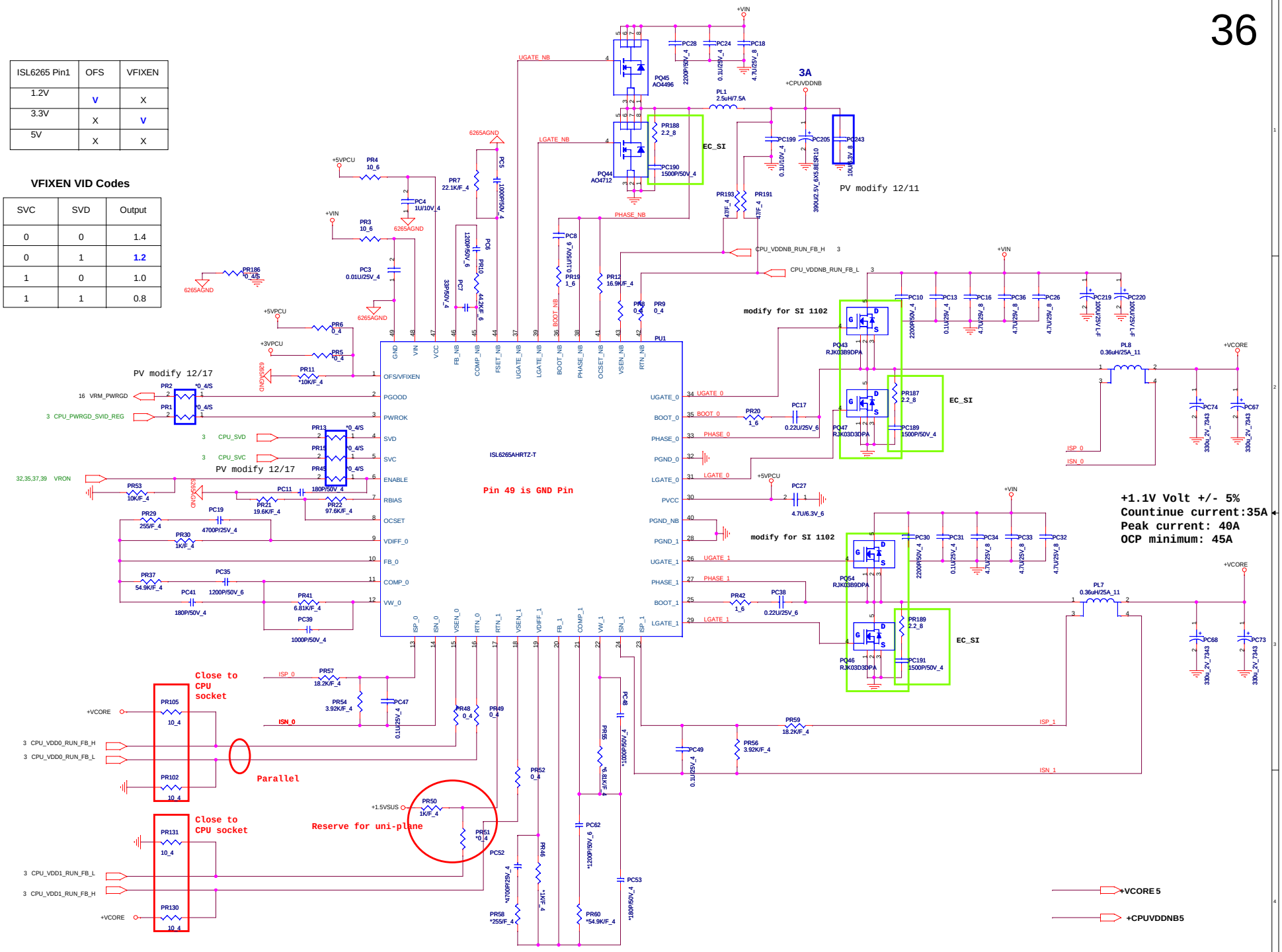
Date: Thursday, December 24, 2009 | Sheet 34 of 42


+1.1V Volt +/- 5%
Countinue current:5A
Peak current: 7A
OCP minimum: 9A
PV modify 12/17
RT8208A
PU3
PQ50 AON7410
PQ51 AON7702
PL9 2.5uH/7.5A
600 mils
+1.1V_DYN
+1.1V_DYN_S1
PC218
PC204
DYN_PWR_EN | High | Low
+1.1V_DYN | 0.95 | 1.1
RDSon=14m ohm
Vo=0.75(R1+R2)/R2
Reserve for AMD tunning
PQ8 DMN601K-7
+1.1V Volt +/- 5%
Countinue current:5A
Peak current: 7A
OCP minimum: 9A
PV modify 12/17
PU14
RT8209A
PQ65 AO4496
PQ64 AO4712
PL14 2.5uH/7.5A
600 mils
PV modify 12/14
PV modify 12/16
RDSon=26m ohm
Vo=0.75(R1+R2)/R2
1.2 Volt +/- 5%
Countinue current:0.3A
Peak current:0.5A
PU11 *RT9025
PV modify 12/11
1.1 Volt +/- 5%
Countinue current:0.2A
Peak current:0.5A
PU13 RT9025
PV modify 12/17
R1
R2
VO=(0.8(R1+R2)/R2)
R2<120Kohm
PROJECT : AX2/7
Quanta Computer Inc.
NB5/RD2
Size Custom
Document Number
VGA Core/+1.8VGFX/1.0VGFX
Rev 1A
Date: Thursday, December 24, 2009
Sheet 35 of 42

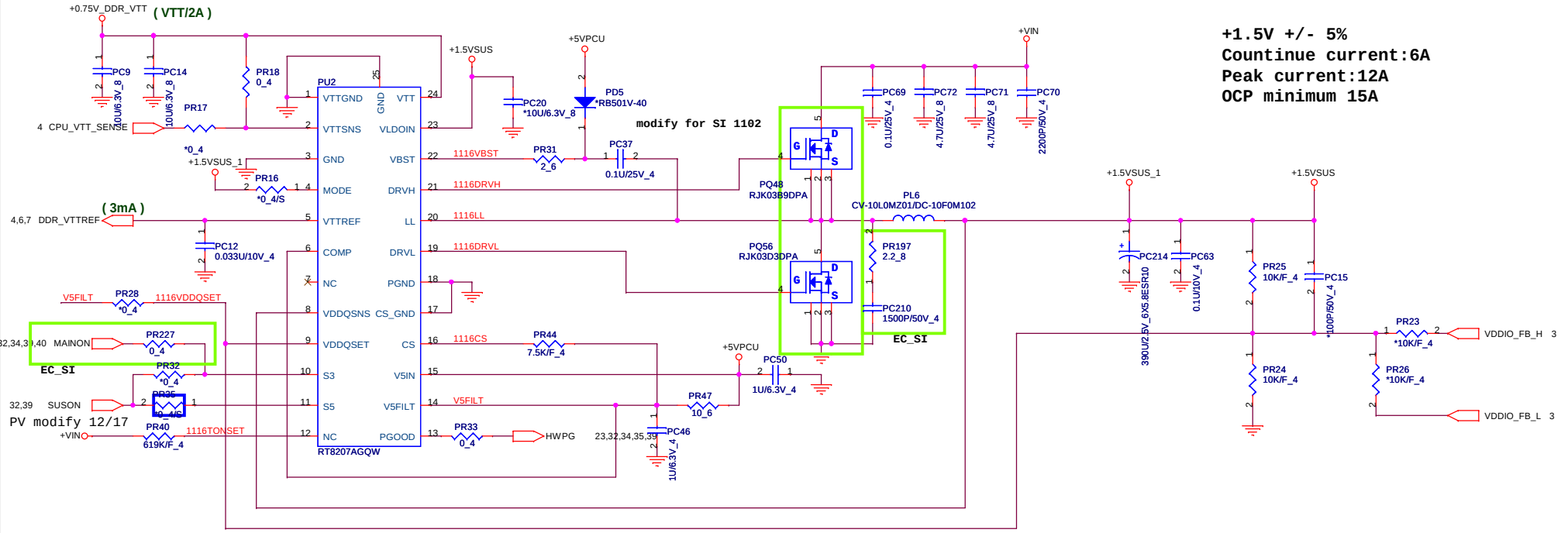
ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

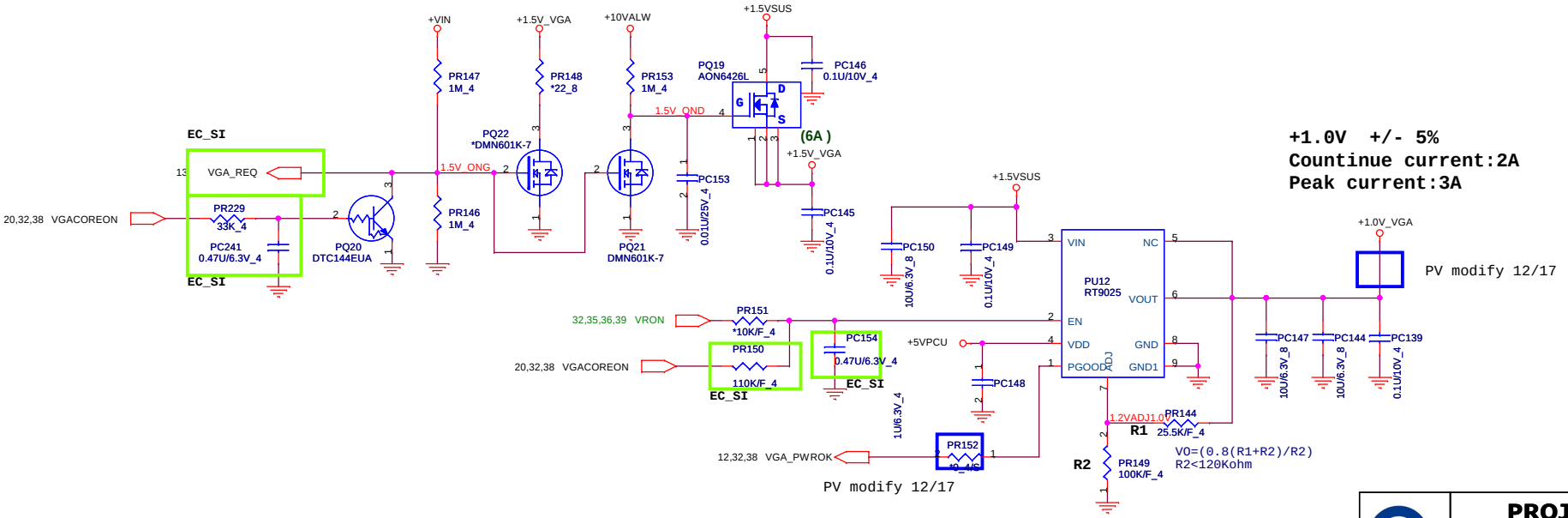
SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



PROJECT : AX2/7 Quanta Computer Inc.		
Size C	Document Number CPU_CORE(ISL6265)	Rev 1A
NB5/RD2	Date: Thursday, December 24, 2009	Sheet 36 of 42



+1.5V +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

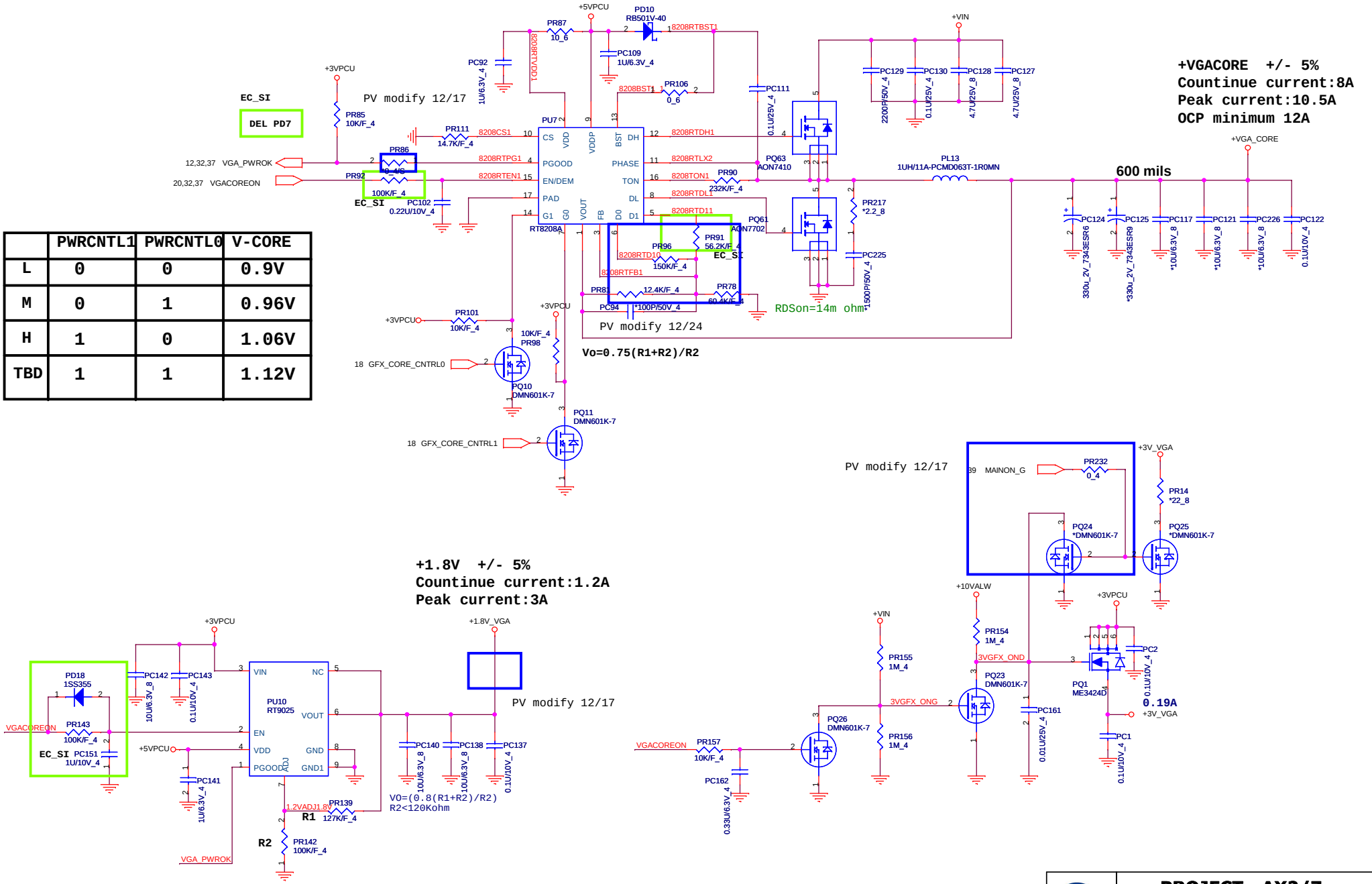


+1.0V +/- 5%
Countinue current:2A
Peak current:3A

PROJECT : AX2/7
Quanta Computer Inc.
SANTOS INTEL

Size	Document Number	Rev
	DDR3 (RT8207)	1A
NB5/RD2	Date: Thursday, December 24, 2009	Sheet 37 of 42

VGA Core



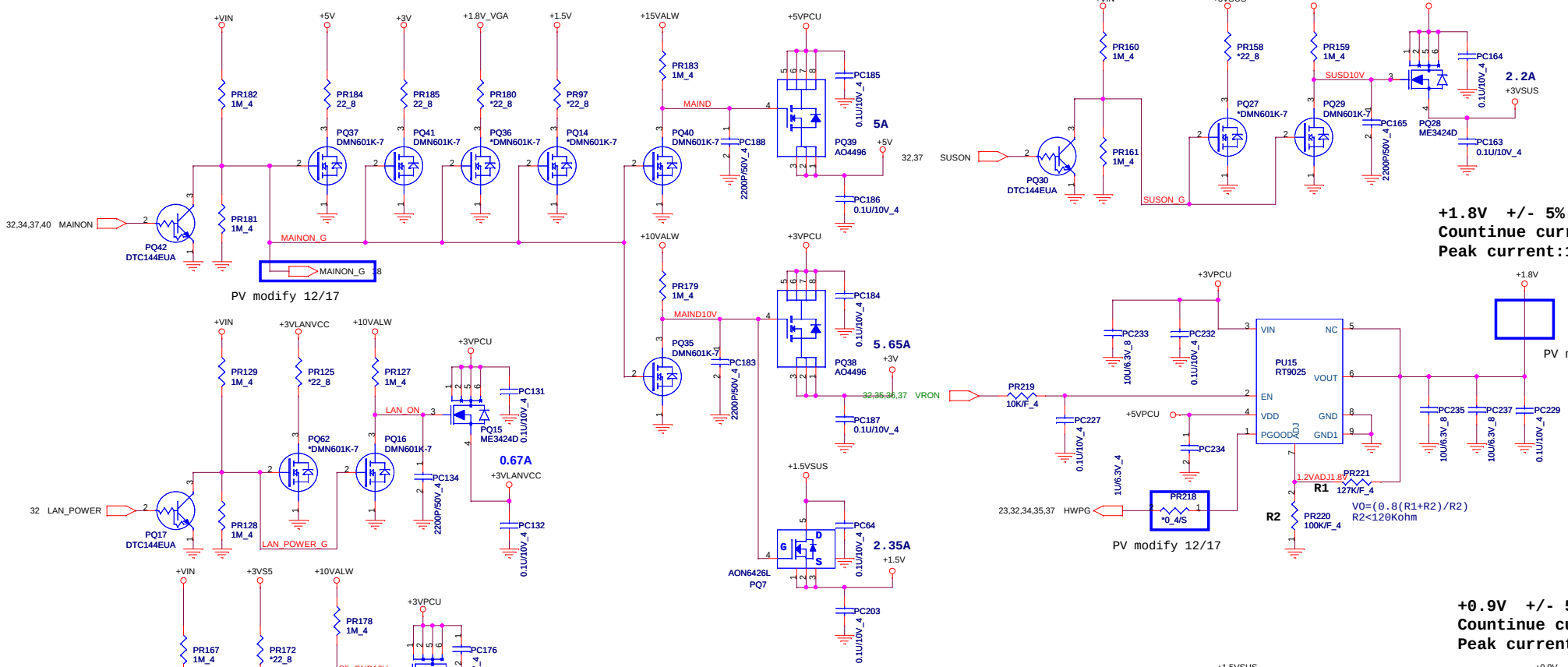
	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0.9V
M	0	1	0.96V
H	1	0	1.06V
TBD	1	1	1.12V

PROJECT : AX2/7
Quanta Computer Inc.

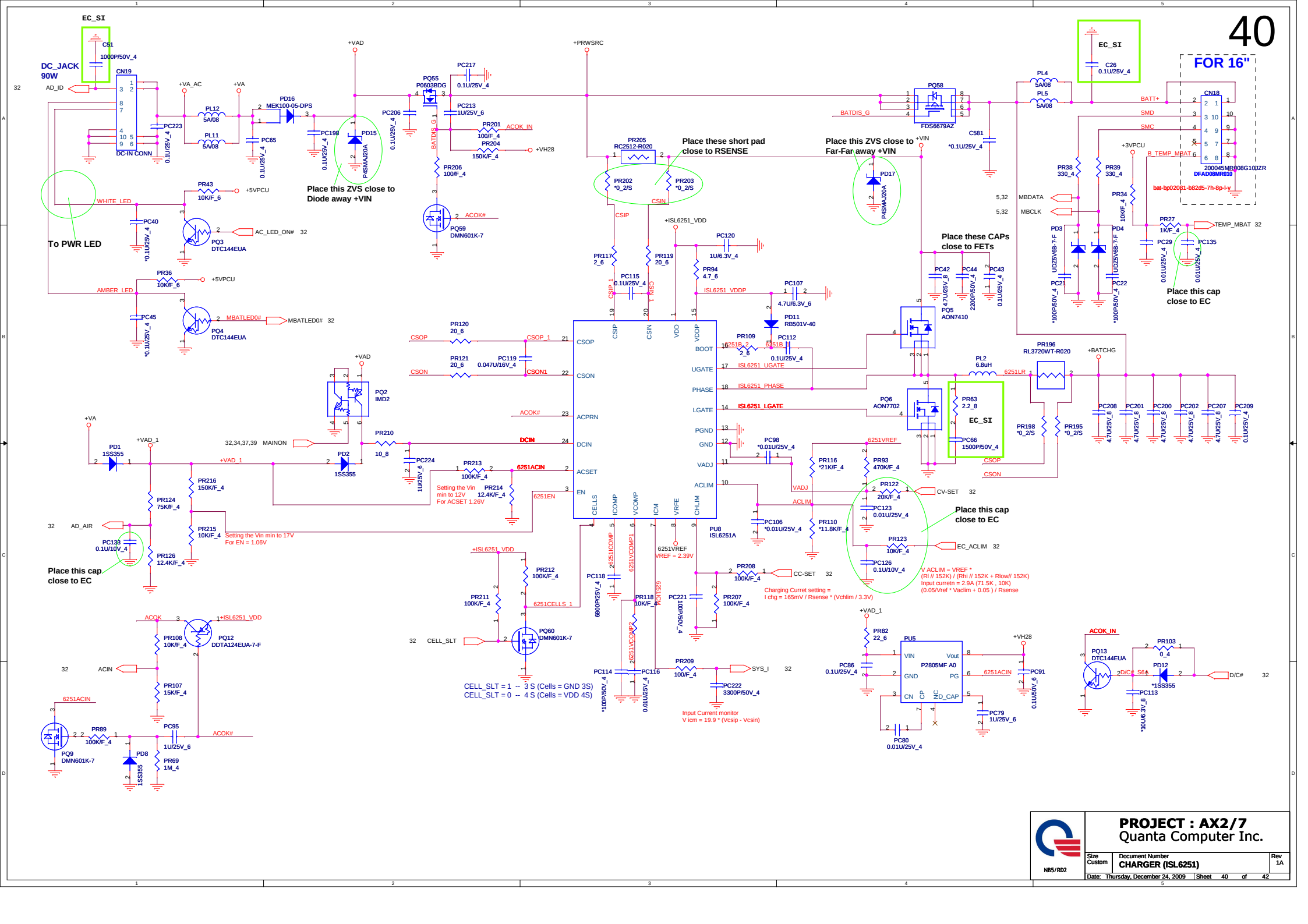
Size	Document Number	Rev
Custom	+VGACORE (RT8208/1.8V)	1A

Date: Thursday, December 24, 2009 | Sheet 38 of 42

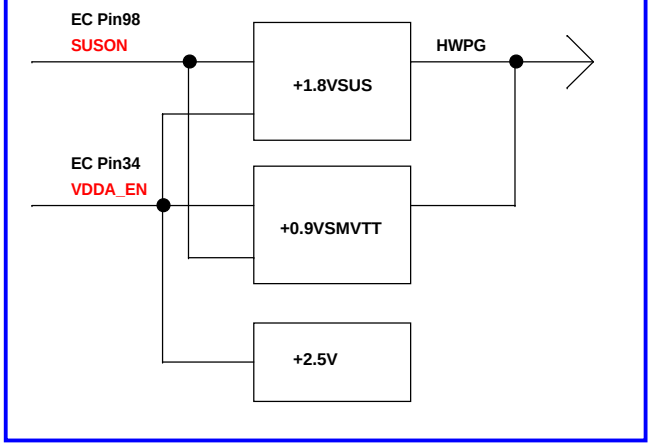
NB5/RD2



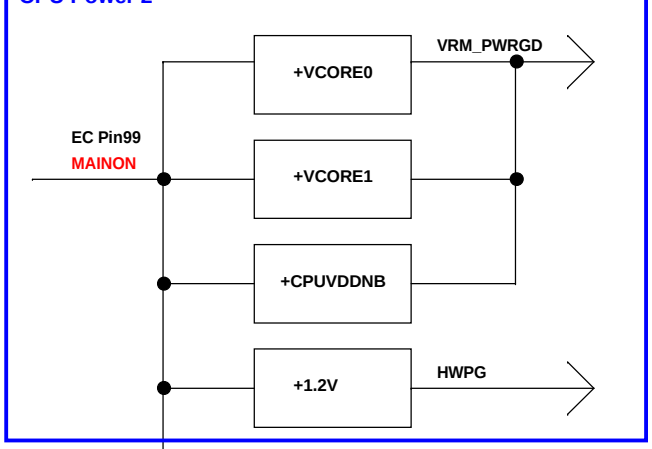
PROJECT : AX2/7 Quanta Computer Inc.			
Size: Custom	Document Number: DISCHARGE/3VS5/5VS5/LAN		Rev: ?
N85/RD2	Date: Thursday, December 24, 2009	Sheet: 39of	42

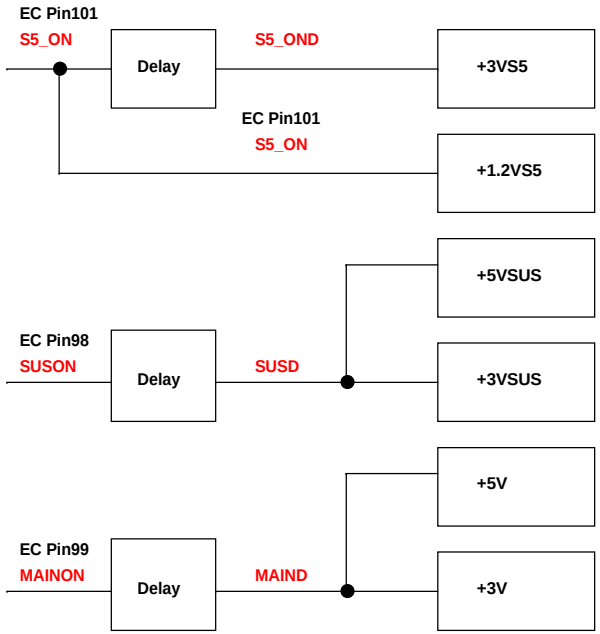

EC_SI
C51
1000P/50V_4
DC_JACK
90W
CN19
DC-IN CONN
AD_ID
+VA_AC
+VA
PL12
5A/08
PL11
5A/08
PC223
0.1U/25V_4
PC65
0.1U/25V_4
PD16
MEK100-05-DPS
+VAD
PC198
0.1U/25V_4
PD15
P4SMA20A
Place this ZVS close to
Diode away +VIN
PC206
0.1U/25V_4
PQ55
P0603BDG
BATDIS_G
PC217
0.1U/25V_4
PC213
1U/25V_6
PR201
100/F_4
ACOK_IN
PR204
150K/F_4
+VH28
PR206
100/F_4
ACOK#
PQ59
DMN601K-7
+PRWSRC
PR205
RC2512-R020
PR202
*0_2/S
PR203
*0_2/S
CSIP
CSIN
Place these short pad
close to RSENSE
PR43
10K/F_6
+5VPCU
WHITE_LED
PC40
*0.1U/25V_4
PQ3
DTC144EUA
AC_LED_ON#
32
To PWR LED
PR36
10K/F_6
+5VPCU
AMBER_LED
PC45
*0.1U/25V_4
PQ4
DTC144EUA
MBATLED0#
MBATLED0#
32
+ISL6251_VDD
PC120
1U/6.3V_4
PR94
4.7_6
PR117
2_6
PR119
20_6
PC115
0.1U/25V_4
ISL6251_VDDP
PC107
4.7U/6.3V_6
PD11
RB501V-40
PR109
6251B_2
2_6
PC112
0.1U/25V_4
ISL6251_UGATE
ISL6251_PHASE
ISL6251_LGATE
PR120
20_6
CSOP
CSOP_1
PR121
20_6
PC119
0.047U/16V_4
CSON
CSON1
ACOK#
DCIN
PR210
10_8
PC224
1U/25V_6
PR213
100K/F_4
6251ACIN
PR214
12.4K/F_4
Setting the Vin
min to 12V
For ACSET 1.26V
6251EN
Setting the Vin min to 17V
For EN = 1.06V
PU8
ISL6251A
CELLS
ICOMP
VCOMP
ICM
VRFE
CHLIM
BOOT
UGATE
PHASE
LGATE
PGND
GND
VADJ
ACLIM
VDD
VDDP
CSIP
CSIN
ACPRN
DCIN
ACSET
EN
PQ2
IMD2
PD1
1SS355
PD2
1SS355
+VA
+VAD_1
32,34,37,39 MAINON
PR216
150K/F_4
PR124
75K/F_4
PR215
10K/F_4
PR126
12.4K/F_4
32 AD_AIR
PC133
0.1U/10V_4
Place this cap
close to EC
PR212
100K/F_4
PR211
100K/F_4
6251CELLS_1
32 CELL_SLT
PQ60
DMN601K-7
CELL_SLT = 1 -- 3 S (Cells = GND 3S)
CELL_SLT = 0 -- 4 S (Cells = VDD 4S)
6251VREF
VREF = 2.39V
PC118
6800P/25V_4
6251ICOMP
6251VCOMP1
PR118
10K/F_4
6251VCOMP2
PC221
*100P/50V_4
PC114
*100P/50V_4
PC116
0.01U/25V_4
PR209
100/F_4
PC222
3300P/50V_4
SYS_I
32
Input Current monitor
V icm = 19.9 * (Vcsip - Vcsin)
PR208
100K/F_4
CC-SET
32
Charging Curret setting =
I chg = 165mV / Rsense * (Vchlim / 3.3V)
PR116
*21K/F_4
PR110
*11.8K/F_4
PC106
*0.01U/25V_4
PC98
*0.01U/25V_4
6251VREF
PR93
470K/F_4
PR122
20K/F_4
CV-SET
32
PC123
0.01U/25V_4
PR123
10K/F_4
EC_ACLIM
32
PC126
0.1U/10V_4
Place this cap
close to EC
V ACLIM = VREF *
(Rl // 152K) / (Rhi // 152K + Rlow// 152K)
Input curretn = 2.9A (71.5K , 10K)
(0.05/Vref * Vaclim + 0.05) / Rsense
PQ58
FDS6679AZ
BATDIS_G
Place this ZVS close to
Far-Far away +VIN
PD17
P4SMA20A
+VIN
C581
*0.1U/25V_4
Place these CAPs
close to FETs
PC42
4.7U/25V_6
PC44
2200P/50V_4
PC43
0.1U/25V_4
PQ5
AON7410
PQ6
AON7702
PL2
6.8uH
6251LR
PR63
2.2_8
EC_SI
PC66
1500P/50V_4
PR196
RL3720WT-R020
+BATCHG
PR198
*0_2/S
PR195
*0_2/S
PC208
4.7U/25V_8
PC201
4.7U/25V_8
PC200
4.7U/25V_8
PC202
4.7U/25V_8
PC207
4.7U/25V_8
PC209
0.1U/25V_4
CSOP
CSON
PR82
22_6
PU5
P2805MF A0
VIN
Vout
GND
PG
CN
CP
NC
ND_CAP
PC86
0.1U/25V_4
PC80
0.01U/25V_4
PC79
1U/25V_6
PC91
0.1U/50V_6
+VH28
6251ACIN
PL4
5A/08
PL5
5A/08
EC_SI
C26
0.1U/25V_4
FOR 16"
CN18
200045MR008G100ZR
DFAD08MR010
BATT+
SMD
SMC
B_TEMP_MBAT
bat-bp02081-b82d5-7h-8p-l-v
+3VPCU
PR38
330_4
PR39
330_4
PR34
10K/F_4
5,32 MBDATA
5,32 MBCLK
PR27
1K/F_4
TEMP_MBAT
32
PC29
0.01U/25V_4
PC135
0.01U/25V_4
Place this cap
close to EC
PD3
UDZ5V6B-7-F
PD4
UDZ5V6B-7-F
PC21
*100P/50V_4
PC22
*100P/50V_4
ACOK_IN
PQ13
DTC144EUA
PR103
0_4
PD12
*1SS355
PC113
*10V/6.3V_8
D/C#
32
ACOK
PR108
10K/F_4
PQ12
DDTA124EUA-7-F
+ISL6251_VDD
32 ACIN
PR107
15K/F_4
6251ACIN
PR89
100K/F_4
PQ9
DMN601K-7
PC95
1U/25V_6
ACOK#
PD8
1SS355
PR69
1M_4
N85/RD2
PROJECT : AX2/7
Quanta Computer Inc.
Size
Custom
Document Number
CHARGER (ISL6251)
Rev
1A
Date: Thursday, December 24, 2009
Sheet 40 of 42

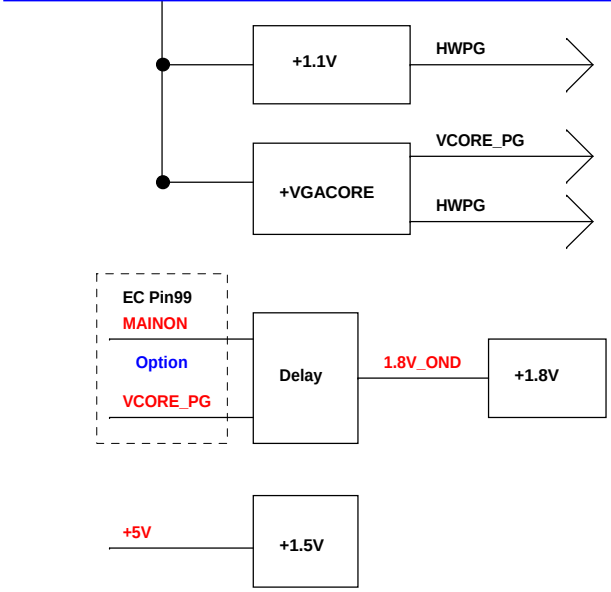
CPU Power 1



CPU Power 2







1 S5_ON, S5_OND, RSMRST# → 2 SUSON, SUSD → 3 MAINON, MAIND → 4 HWPG, VCORE_PG, VRM_PWRGD → EC Pin76 ECPWROK, Delay 600ms → SB_PWRGD_IN, 3.3V → NB_PWRGD_IN, 1.8V

NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Power control	3A

Date: Thursday, December 24, 2009 | Sheet 41 of 42

Power & Ground

Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (19V)	
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VLANVCC	S0		LAN_POWER
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+5V	S0		MAINON
+5V_VCC1			
+5VALW			
+10VALW			
+15VALW			
+1.8V	S0		+1.5_ON
+1.8VSUS	S0, S3		
+1.5V	S0		MAINON
+1.5VSUS	S0, S3	DDR CORE POWER	SUSON
+1.5VSUS_1			
+1.5V_VGA	S0	VGA , VRAM POWER	+1.5_ON
+1.2V	S0		VRON
+1.2VSUS	S0, S3		SUSON
+1.1V	S0	VDDPCIE - PCIE-E MAIN POWER	VRON
+1.1VS5	S0, S3, S4, S5	STANDBY POWER	S5_ON
+1.1V_DYN	S0	NB VDDC - CORE LOGIC POWER	DYN_PWR_EN
+1.05V	S0	HT POWER (1.05V)	VRON
+1.0V_VGA	S0	PARK DPX_VDD10 POWER	VRON
+2.5V	S0	CPU VDDA POWER	VR2.5_ON
+VCORE0	S0	CPU CORE POWER (?V)	VRON
+VCORE1	S0	CPU CORE POWER (?V)	VRON
+CPUVDDNB	S0	CPU VDDNB POWER	VRON
+0.75_DDR_VTT	S0	DDR COMMAND & CONTROL PULL UP POWER	SUSON
DDR_VTTREF	S0, S3	DDR REFERENCE POWER	SUSON
+VGA_CORE	S0	VGA CORE POWER	MAINON
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER（3_3V）	

SMBUS

DEVICE	ADDRESS	BUS
CLOCK GENERATOR		
DDR3		
CPU THERMAL SENSOR		
CHARGER		

PCB STACK UP

LAYER 1 : TOP
LAYER 2 :GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT

Custom<Doc>
NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
		1A

Date: Wednesday, December 23, 2009 Sheet 42 of 42