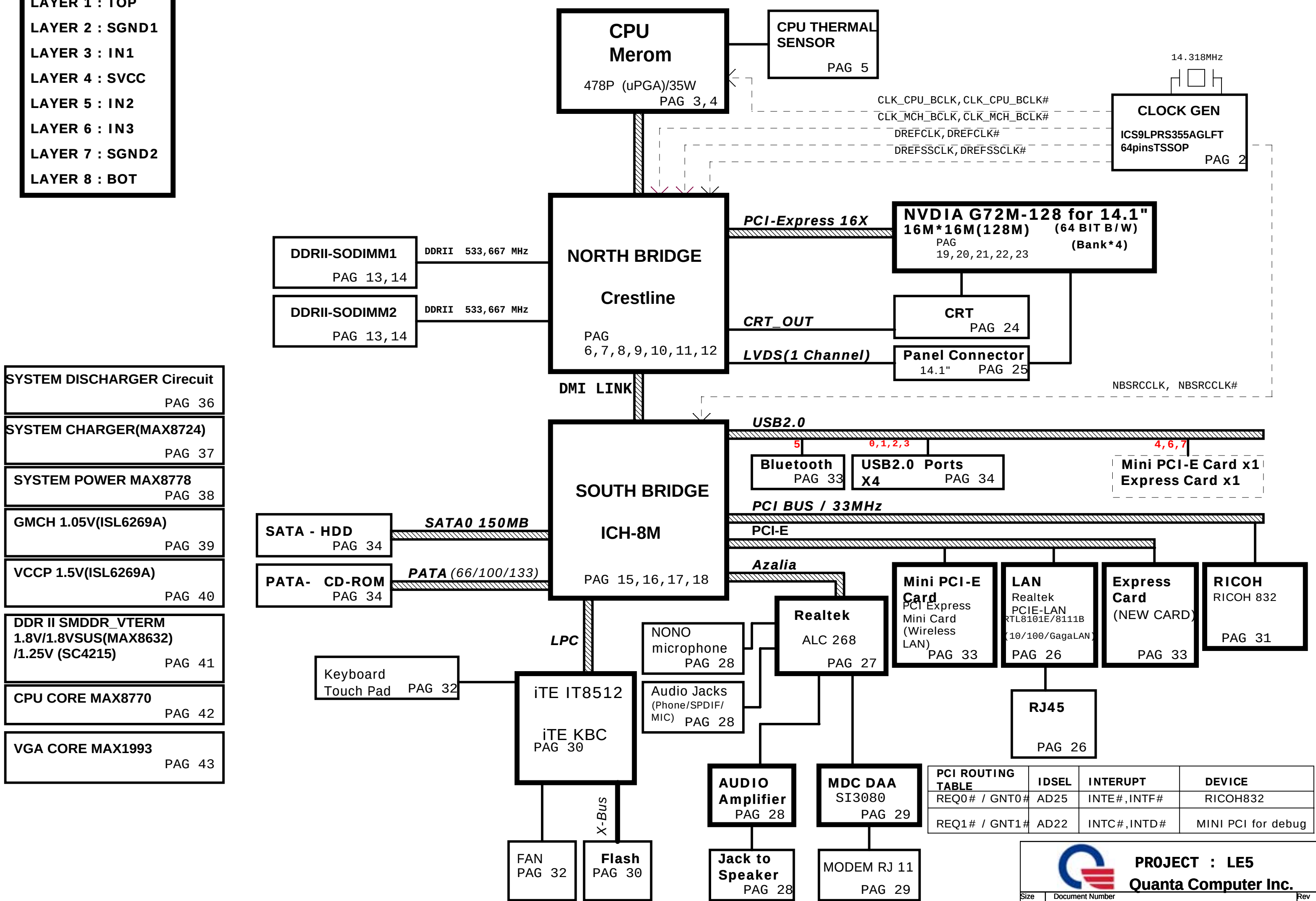
LE5 BLOCK DIAGRAM(module)

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : SVCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT



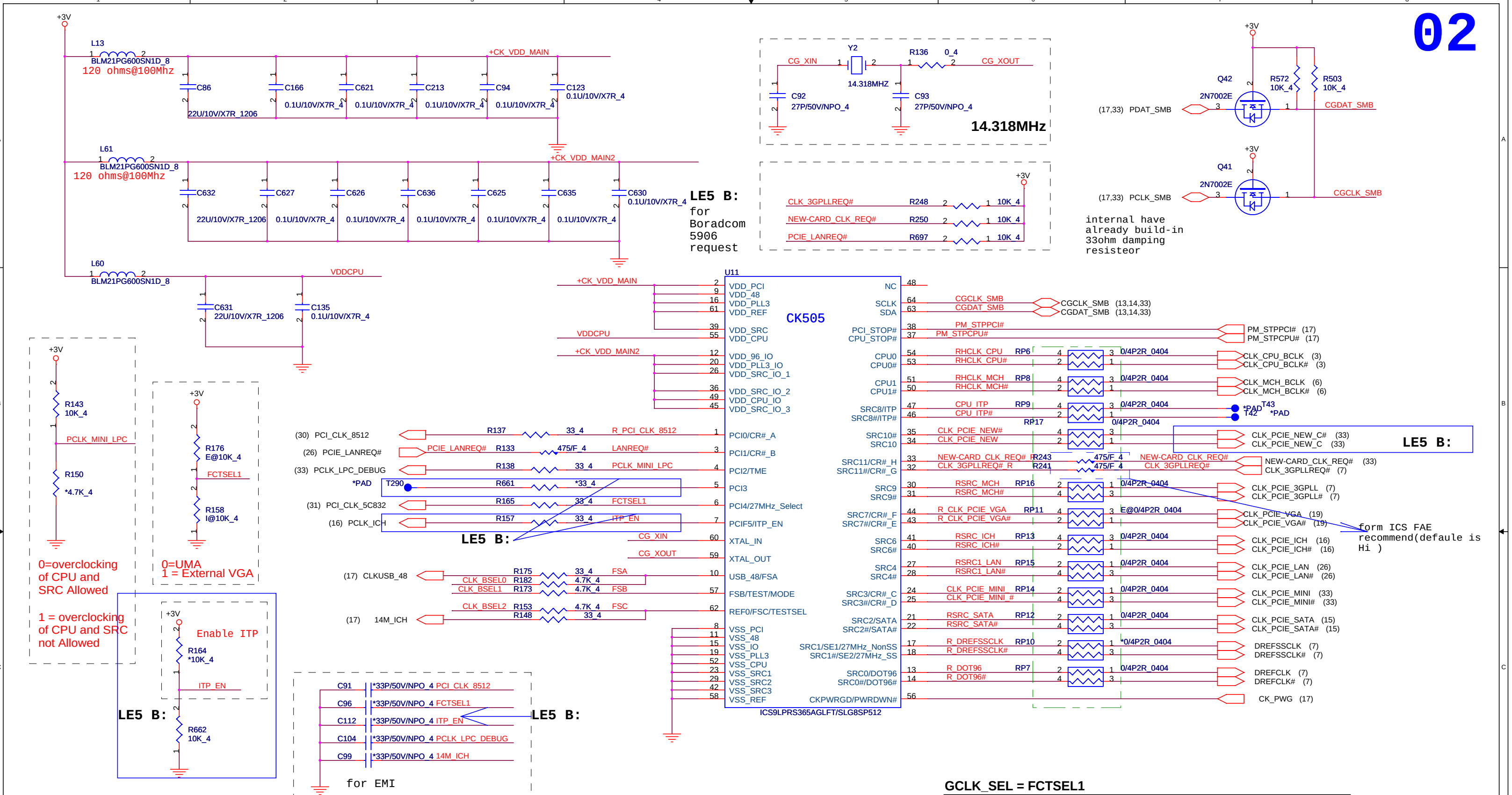
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	2B

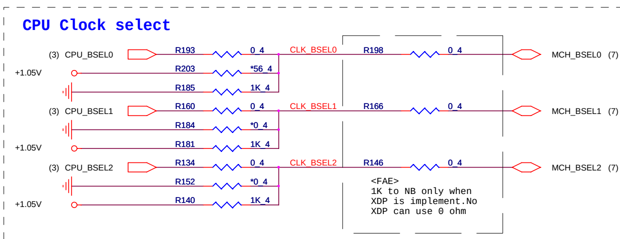
Date: Wednesday, November 22, 2006 Sheet 1 of 43



GCLK_SEL = FCTSEL1

FCTSEL1 (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

CPU Clock select



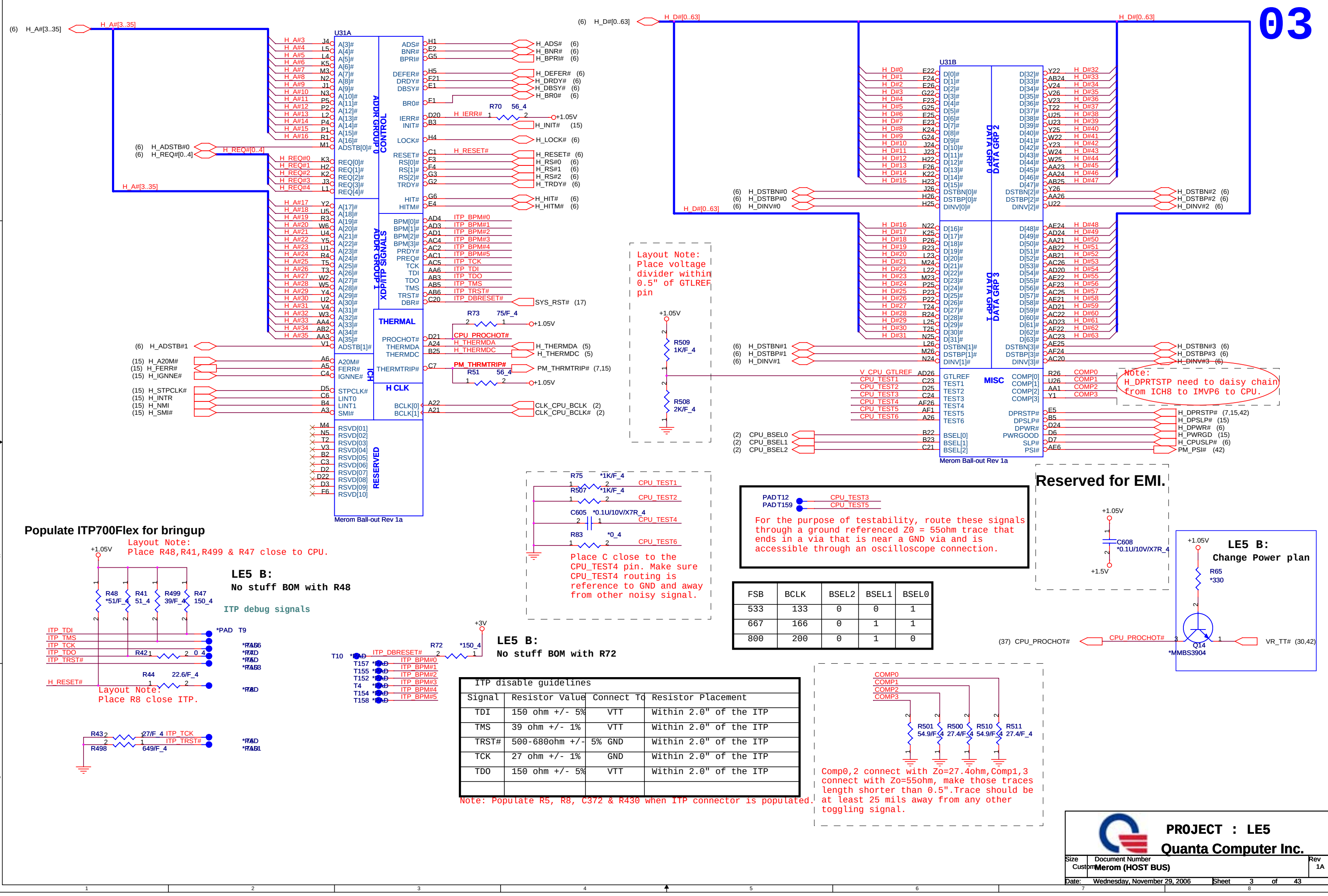
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	1A

Date: Wednesday, November 29, 2006 | Sheet 2 of 43



Populate ITP700Flex for bringup

Layout Note:
Place R48,R41,R499 & R47 close to CPU.

LE5 B:
No stuff BOM with R48

Layout Note:
Place R8 close ITP.

LE5 B:
No stuff BOM with R72

Layout Note:
Place voltage divider within 0.5" of GTLREF pin

Place C close to the CPU_TEST4 pin. Make sure CPU_TEST4 routing is reference to GND and away from other noisy signal.

For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

Note:
H_DPRTSTP need to daisy chain from ICH8 to IMVP6 to CPU.

LE5 B:
Change Power plan

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP

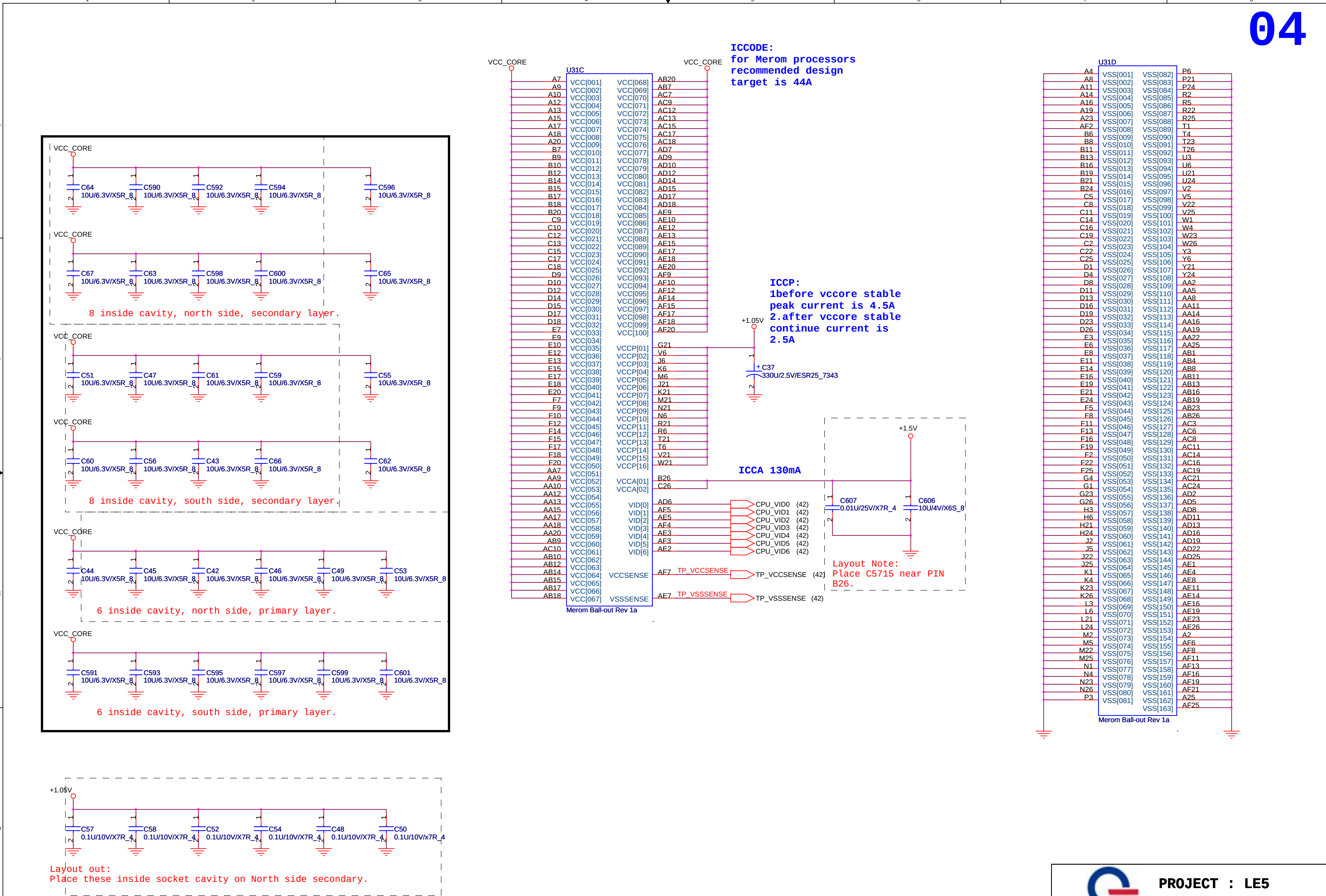
Note: Populate R5, R8, C372 & R430 when ITP connector is populated.

Comp0,2 connect with Zo=27.4ohm,Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5".Trace should be at least 25 mils away from any other toggling signal.

PROJECT : LE5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Merom (HOST BUS)	1A

Date: Wednesday, November 29, 2006 Sheet 3 of 43

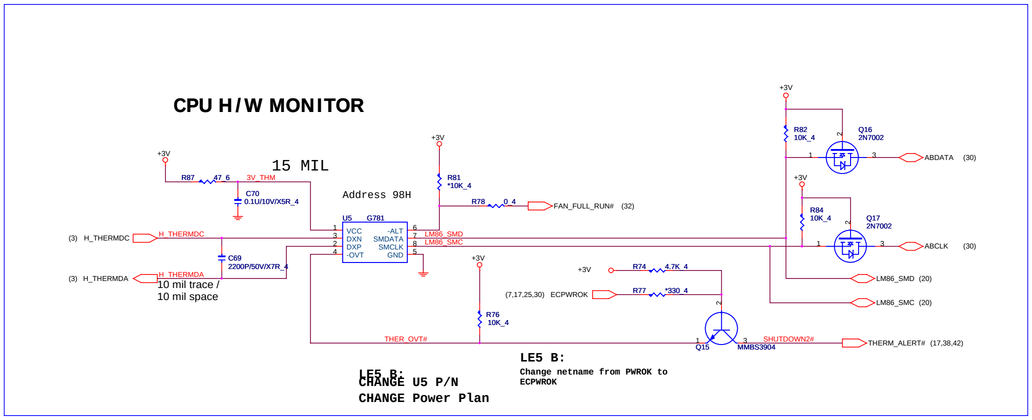


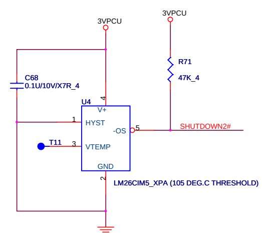
PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Merom (POWER/NC)	1A

Date: Wednesday, November 29, 2006 Sheet 4 of 43



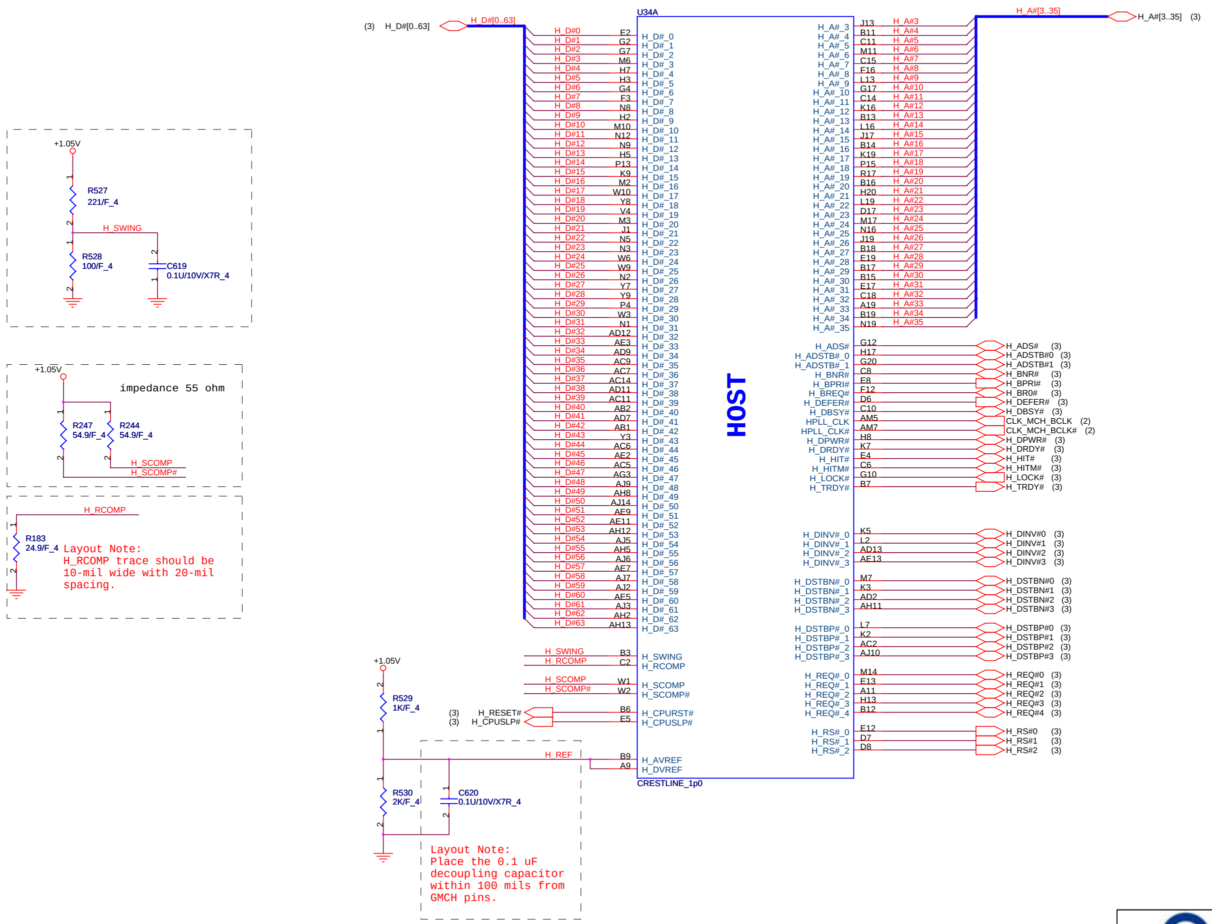


PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
C	CPU THERMAL/HW PRODCT	2B

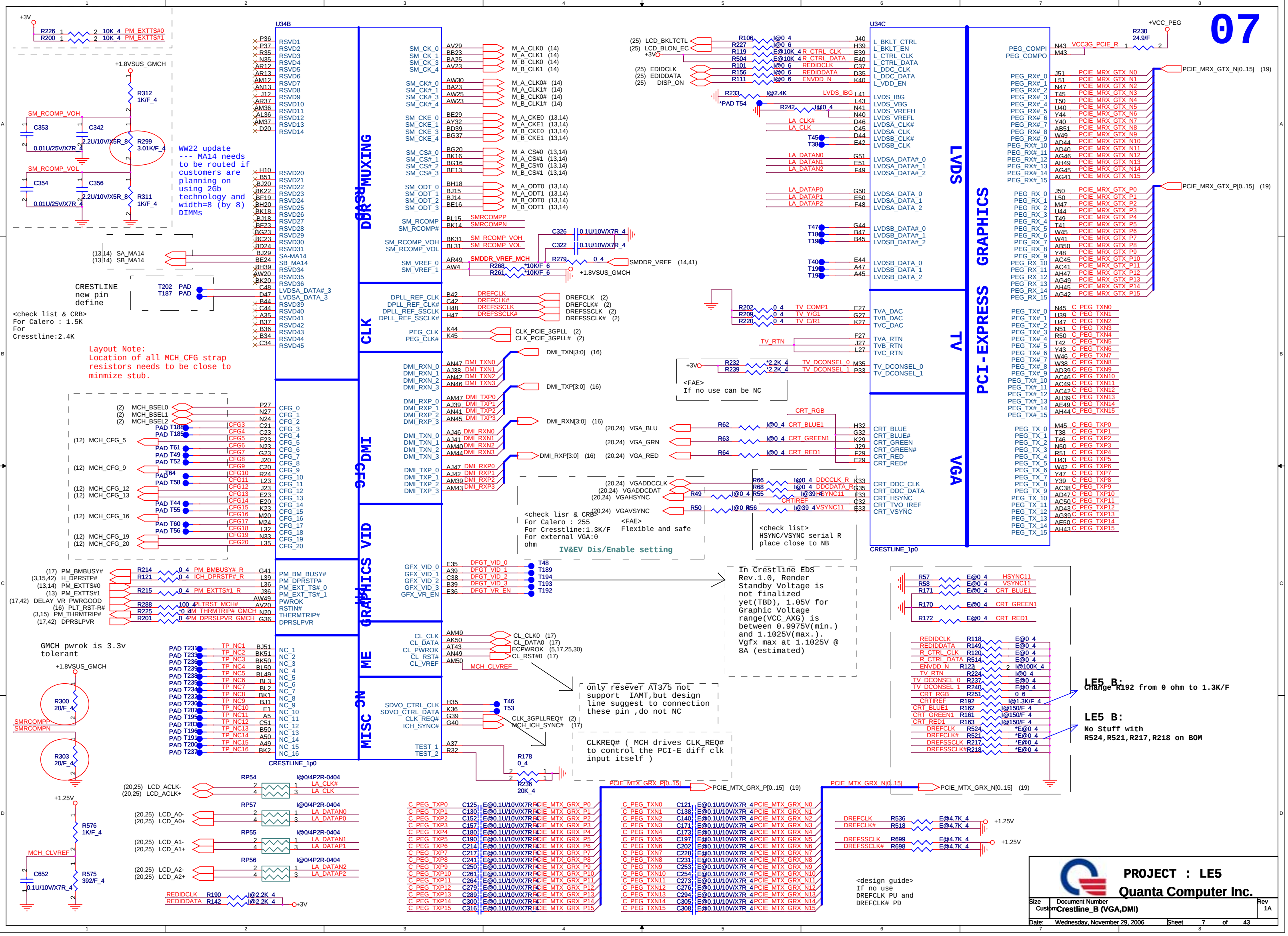
Date: Wednesday, November 29, 2006 Sheet 5 of 43



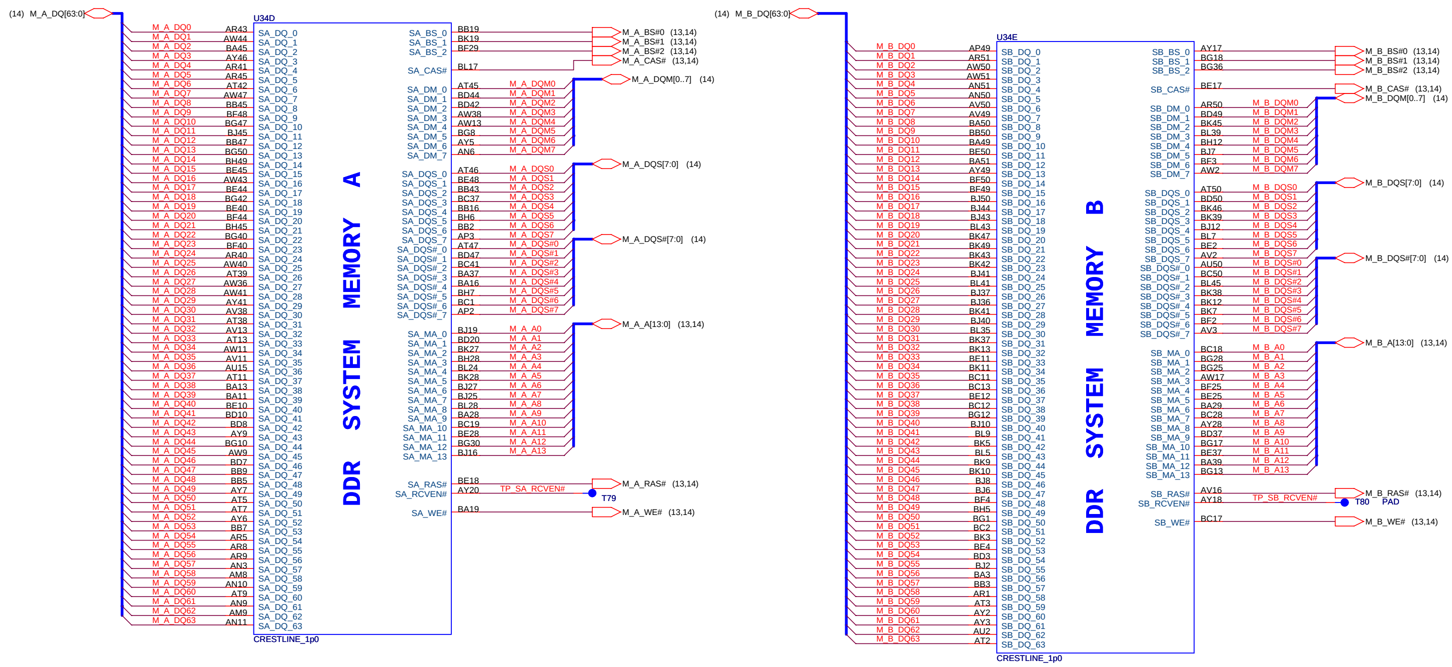
PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
Custom	**Crestline_A (HOST)**	1A
Date: Wednesday, November 29, 2006	Sheet 6 of 43	



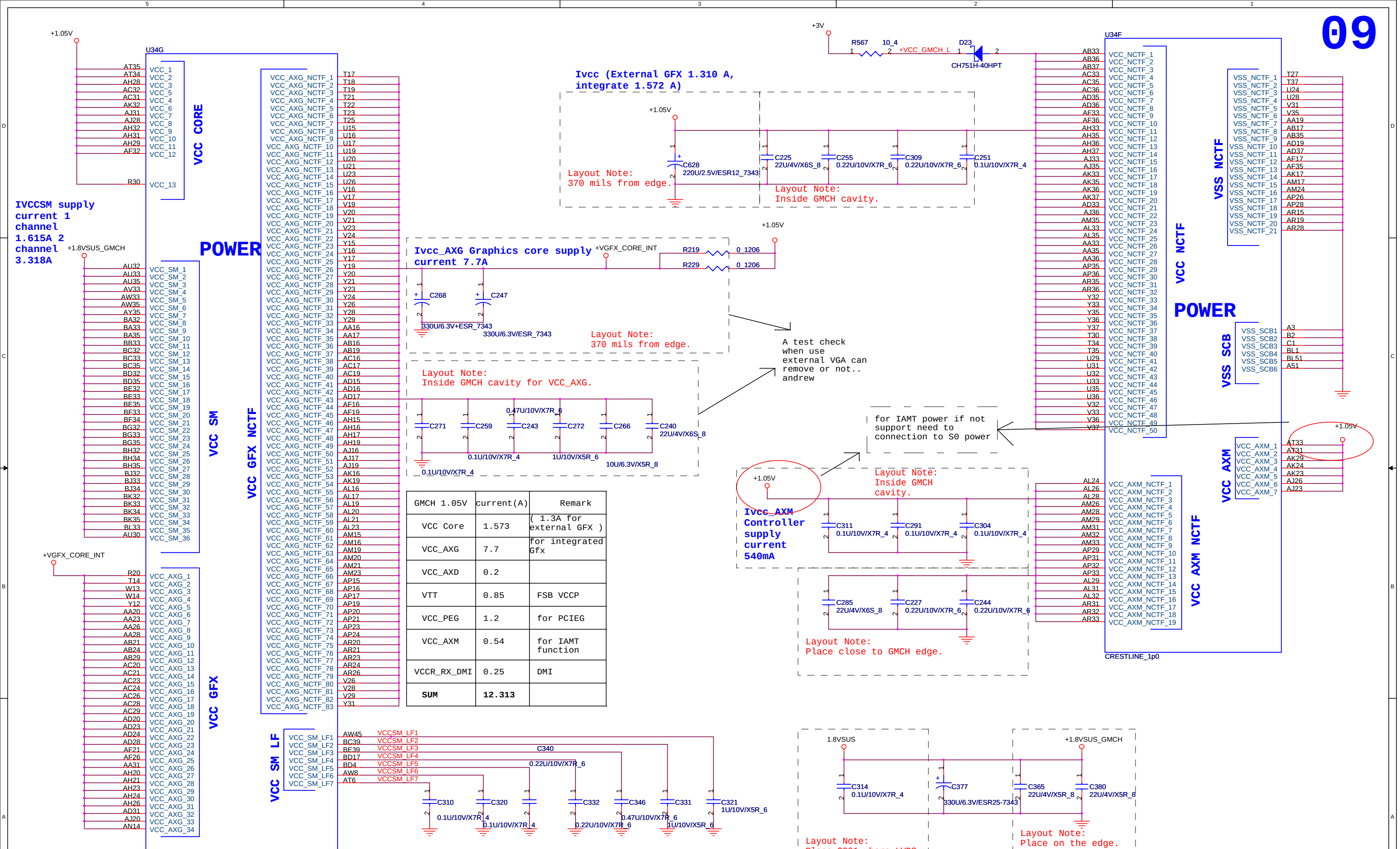
07
WW22 update
--- MA14 needs to be routed if customers are planning on using 2Gb technology and width=8 (by 8) DIMMs
CRESTLINE new pin define
<check list & CRB>
For Calero : 1.5K
For Cresstline:2.4K
Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minmize stub.
GMCH pwrok is 3.3v tolerant
DDR MUXING
CLK
DMI
CFG
GRAPHICS VID
ME
MISC NC
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
<FAE>
If no use can be NC
<check lisr & CRB>
For Calero : 255
For Cresstline:1.3K/F
For external VGA:0 ohm
<FAE>
Flexible and safe
IV&EV Dis/Enable setting
<check list>
HSYNC/VSYNC serial R place close to NB
In Crestline EDS Rev.1.0, Render Standby Voltage is not finalized yet(TBD), 1.05V for Graphic Voltage range(VCC_AXG) is between 0.9975V(min.) and 1.1025V(max.). Vgfx max at 1.1025V @ 8A (estimated)
only reserver AT3/5 not support IAMT,but design line suggest to connection these pin ,do not NC
CLKREQ# (MCH drives CLK_REQ# to control the PCI-E diff clk input itself)
LE5 B:
Change R192 from 0 ohm to 1.3K/F
LE5 B:
No Stuff with R524,R521,R217,R218 on BOM
<design guide>
If no use DREFCLK PU and DREFCLK# PD
CRESTLINE_1p0
PROJECT : LE5
Quanta Computer Inc.
Size Custom
Document Number
Crestline_B (VGA,DMI)
Rev 1A
Date: Wednesday, November 29, 2006
Sheet 7 of 43



PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline_C (DDR2)	1A
Date: Wednesday, November 29, 2006	Sheet 8 of 43	

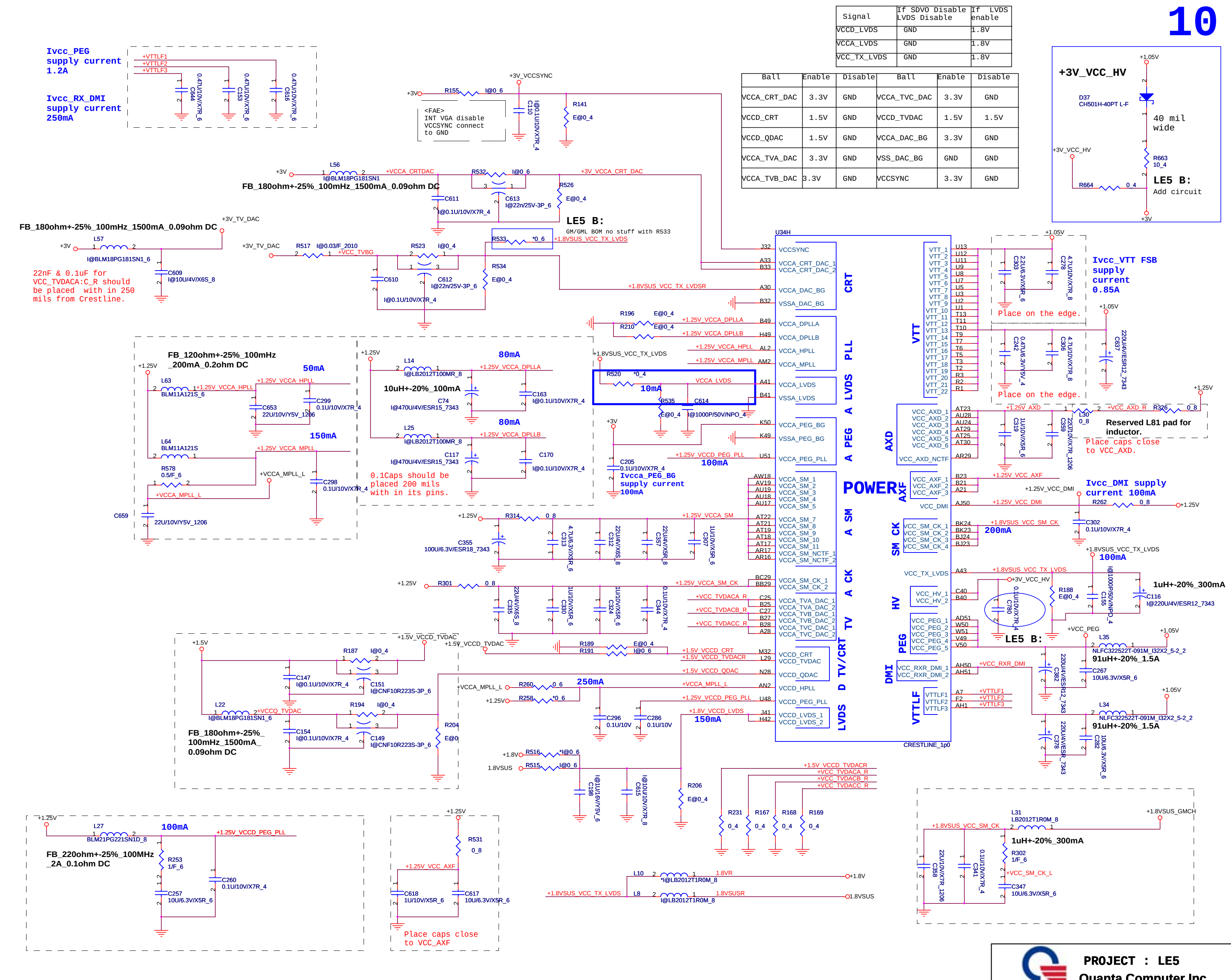


GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX)
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	**12.313**	

PROJECT : LE5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline_D (VCC,NCTF)	1A

Date: Thursday, October 12, 2006 Sheet 9 of 43

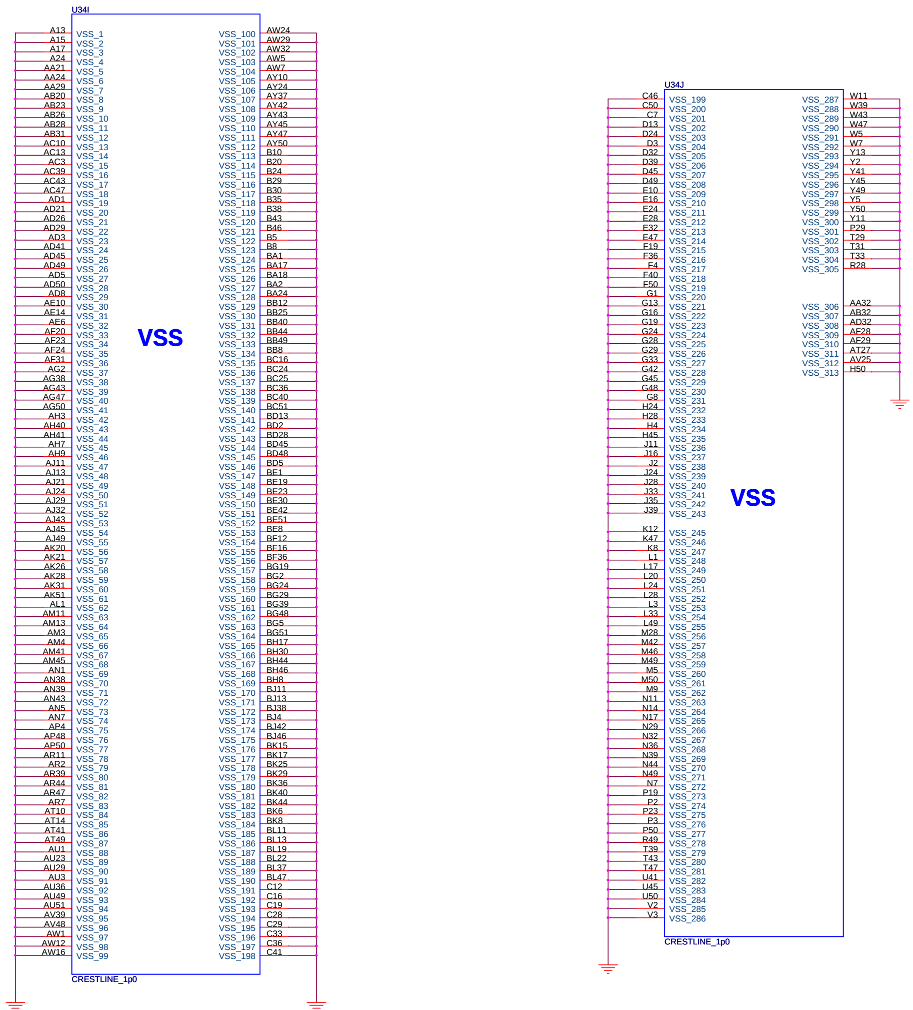


Signal	If SDVO Disable LVDS Disable	If LVDS enable
VCCD_LVDS	GND	1.8V
VCCA_LVDS	GND	1.8V
VCC_TX_LVDS	GND	1.8V

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT_DAC	3.3V	GND	VCCA_TVC_DAC	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVDAC	1.5V	1.5V
VCCD_QDAC	1.5V	GND	VCCA_DAC_BG	3.3V	GND
VCCA_TVA_DAC	3.3V	GND	VSS_DAC_BG	GND	GND
VCCA_TVB_DAC	3.3V	GND	VCCSYNC	3.3V	GND

PROJECT : LE5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline_E (POWER)	1A



PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline_F (VSS)	1A
Date: Tuesday, October 03, 2006	Sheet 11 of 43	

Strap table

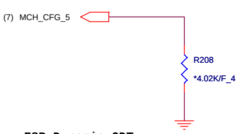
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

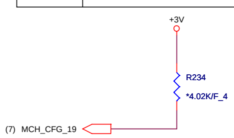
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



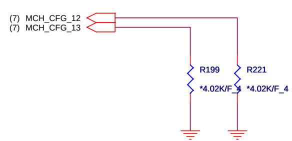
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane



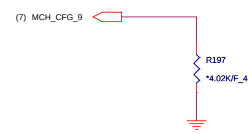
XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

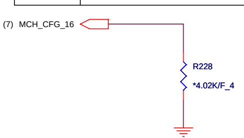


SDVO Present

Strap define at External DVI control page

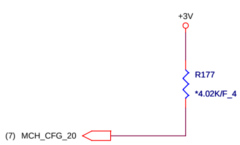
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)

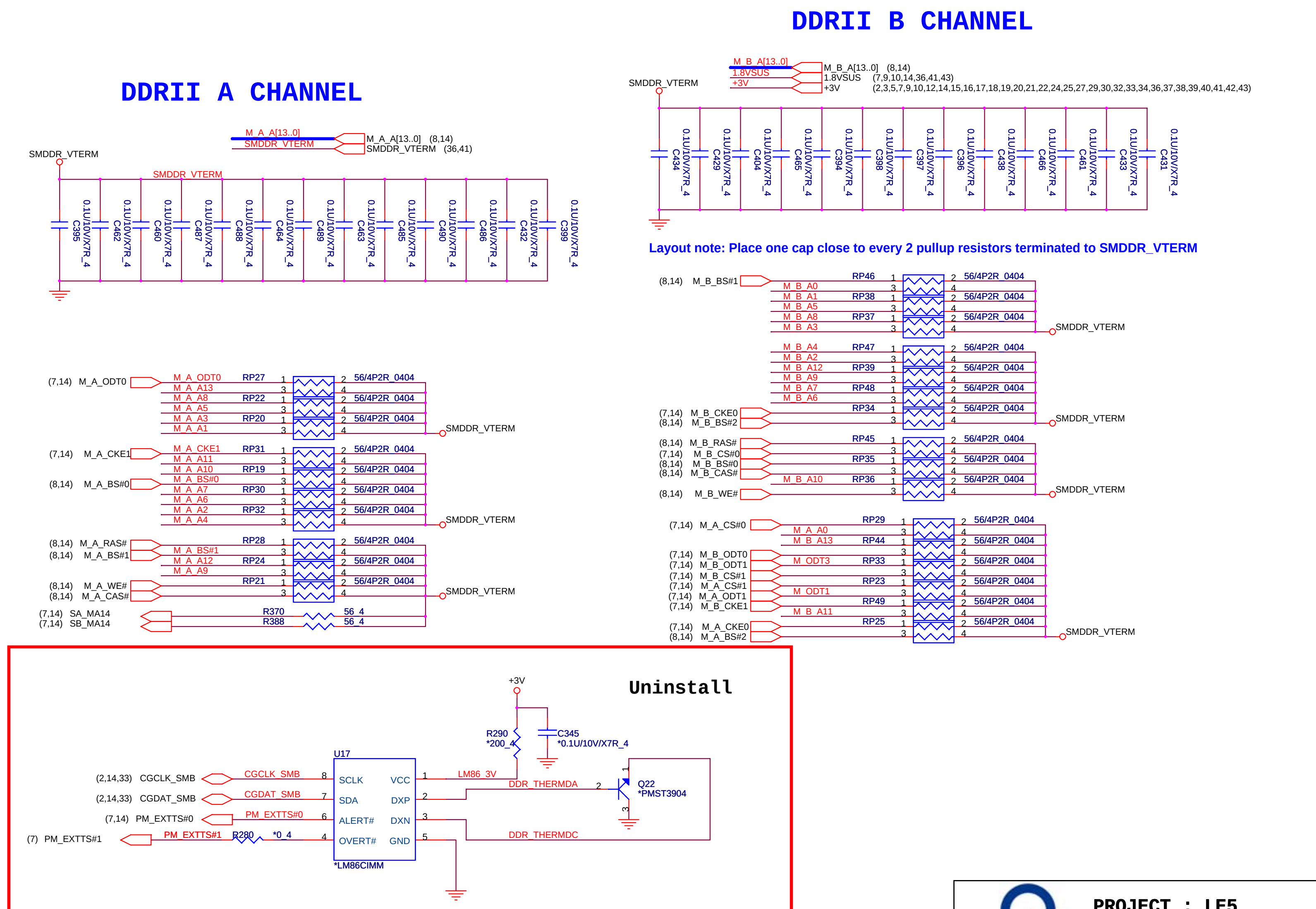


SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port



DDRII DUAL CHANNEL A,B.

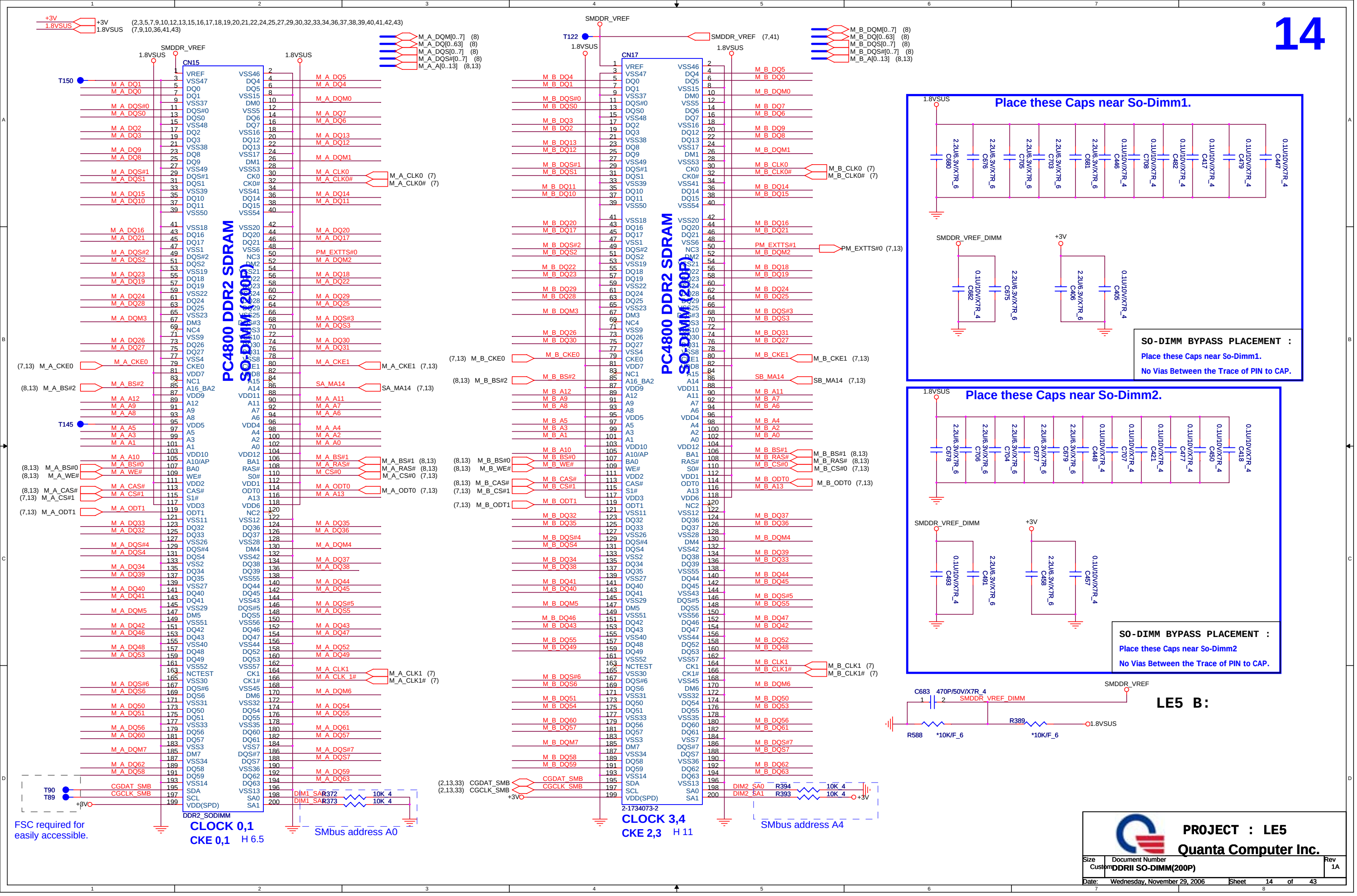


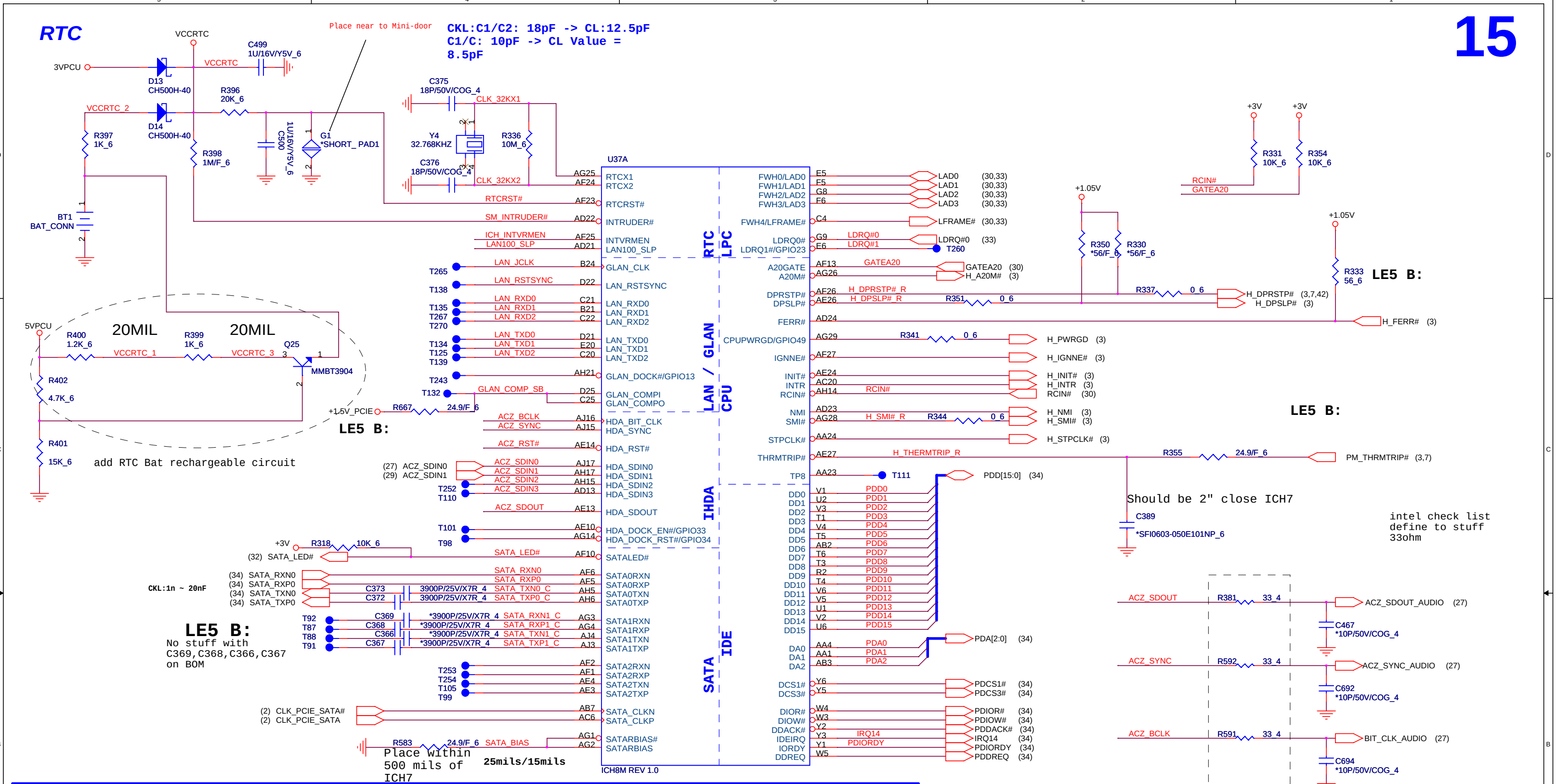
PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDRII RES. ARRAY	1A

Date: Wednesday, November 29, 2006 Sheet 13 of 43


PC4800 DDR2 SDRAM SO-DIMM (200P)
CN15
DDR2_SODIMM
CN17
2-1734073-2
SMDDR_VREF
1.8VSUS
+3V
Place these Caps near So-Dimm1.
Place these Caps near So-Dimm2.
SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.
SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm2
No Vias Between the Trace of PIN to CAP.
SMDDR_VREF_DIMM
C683 470P/50V/X7R_4
R588 *10K/F_6
R389 *10K/F_6
LE5 B:
FSC required for
easily accessible.
CLOCK 0,1
CKE 0,1 H 6.5
SMbus address A0
CLOCK 3,4
CKE 2,3 H 11
SMbus address A4
PROJECT : LE5
Quanta Computer Inc.
Size Custom
Document Number DDRII SO-DIMM(200P)
Rev 1A
Date: Wednesday, November 29, 2006
Sheet 14 of 43



SB Strap

ICH8-M Internal VR Enable strap
(Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

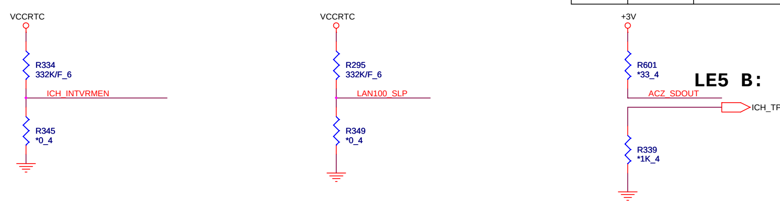
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

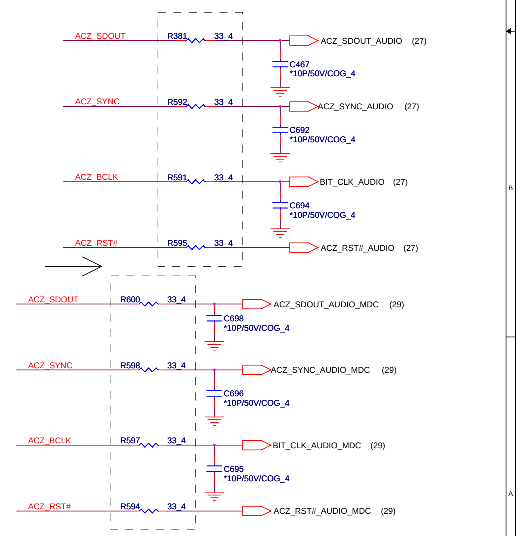
ICH8-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

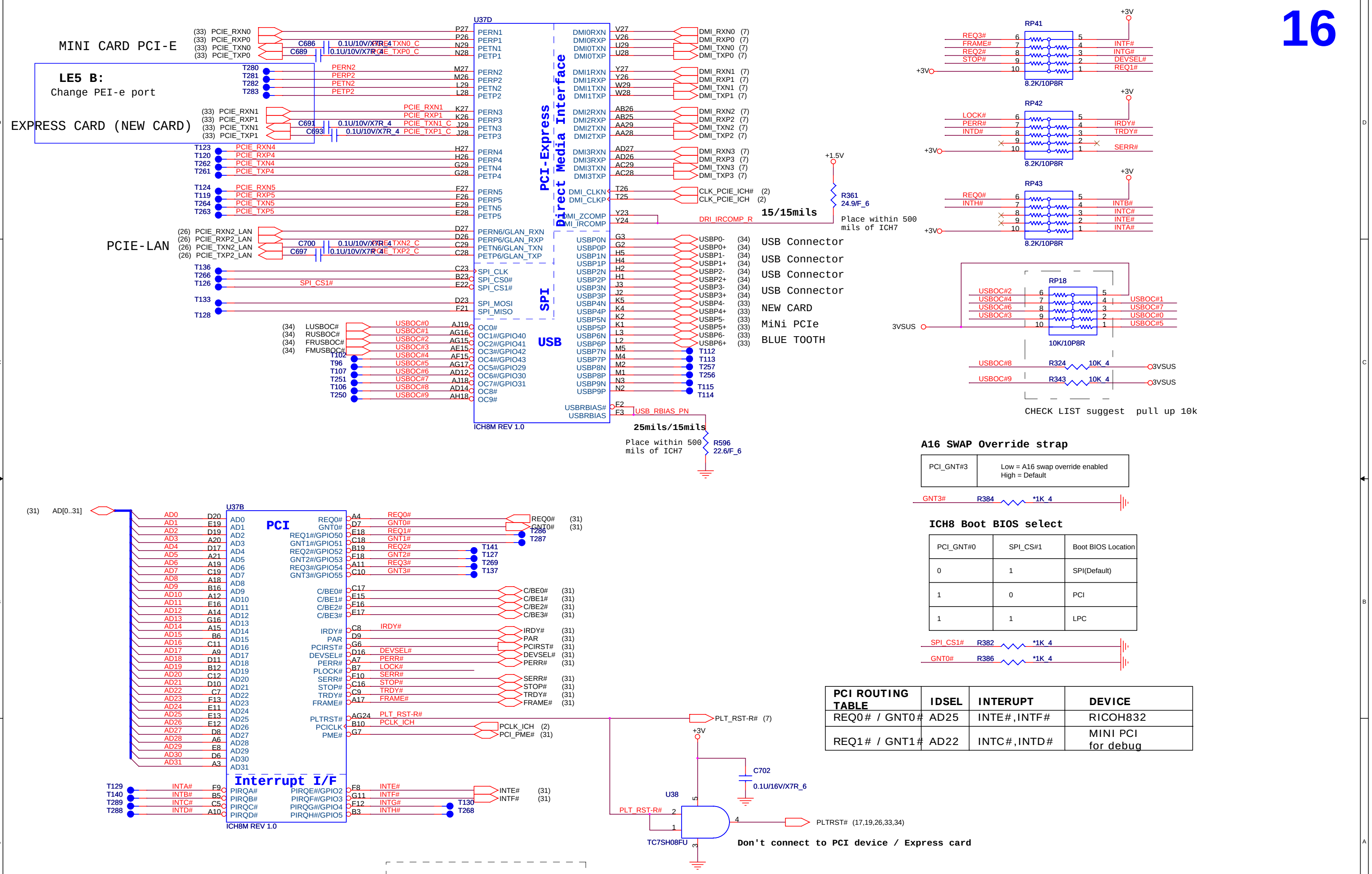




PROJECT : LE5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH8 HOST (1 of 4)	1A

Date: Wednesday, November 29, 2006 | Sheet 15 of 43



A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

ICH8 Boot BIOS select

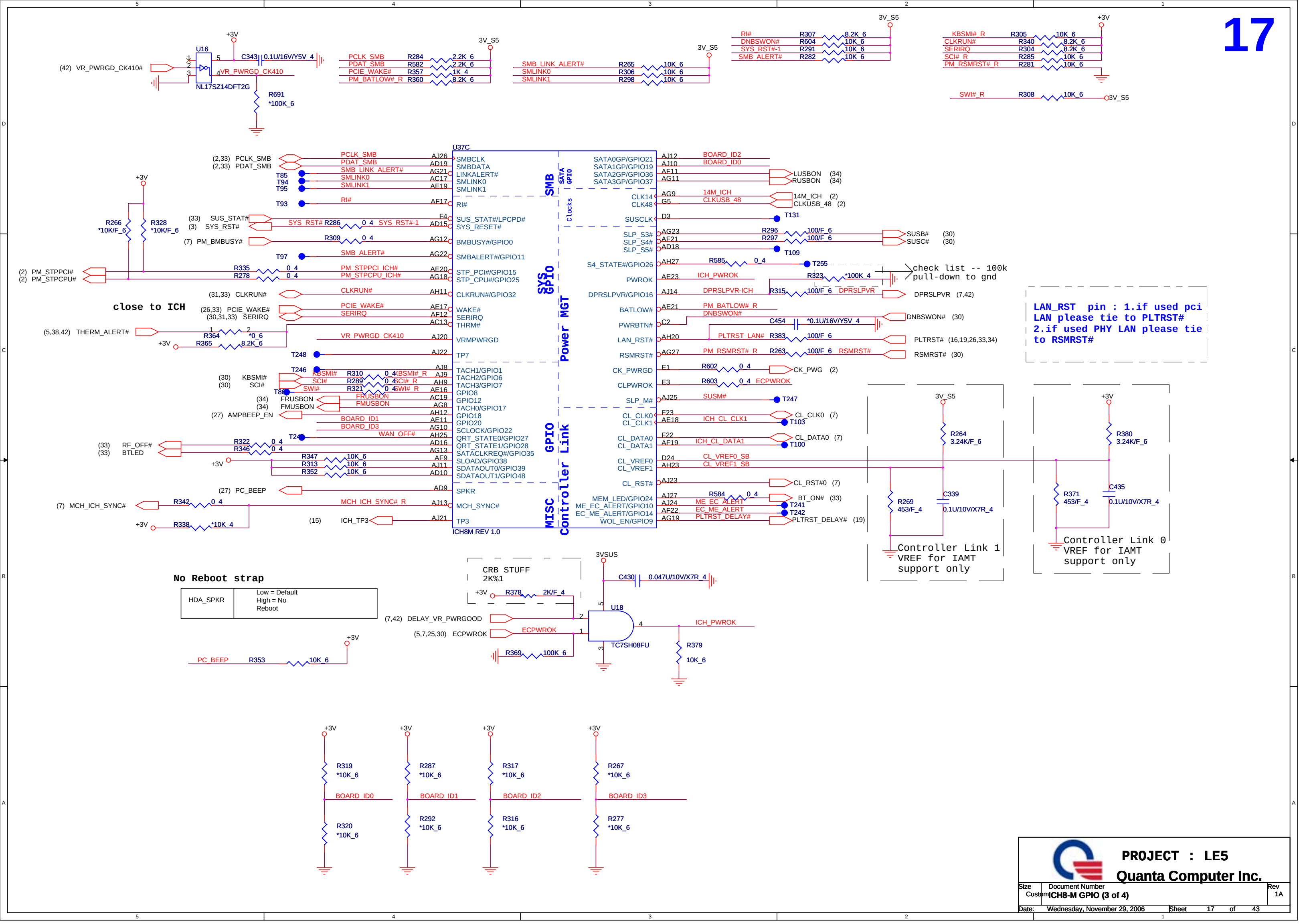
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

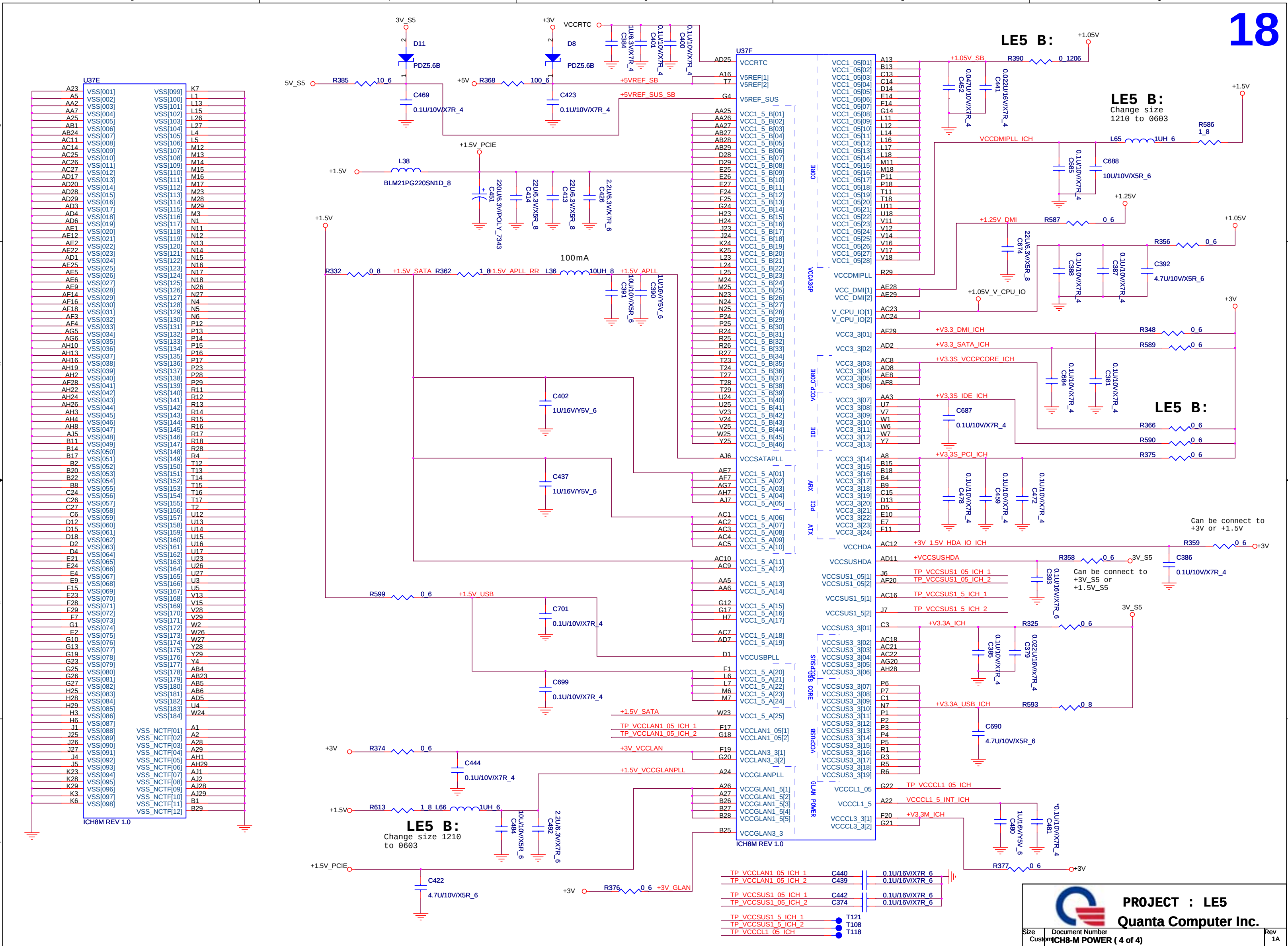
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

PROJECT : LE5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH8-M PCI E (2 of 4)	1A

Date: Wednesday, November 29, 2006 Sheet 16 of 43


17
U37C
ICH8M REV 1.0
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
close to ICH
check list -- 100k pull-down to gnd
LAN_RST pin : 1.if used pci LAN please tie to PLTRST#
2.if used PHY LAN please tie to RSMRST#
Controller Link 1 VREF for IAMT support only
Controller Link 0 VREF for IAMT support only
No Reboot strap
HDA_SPKR
Low = Default
High = No Reboot
CRB STUFF 2K%1
U16
NL17SZ14DFT2G
U18
TC7SH08FU
PROJECT : LE5
Quanta Computer Inc.
Size Custom
Document Number ICH8-M GPIO (3 of 4)
Rev 1A
Date: Wednesday, November 29, 2006
Sheet 17 of 43

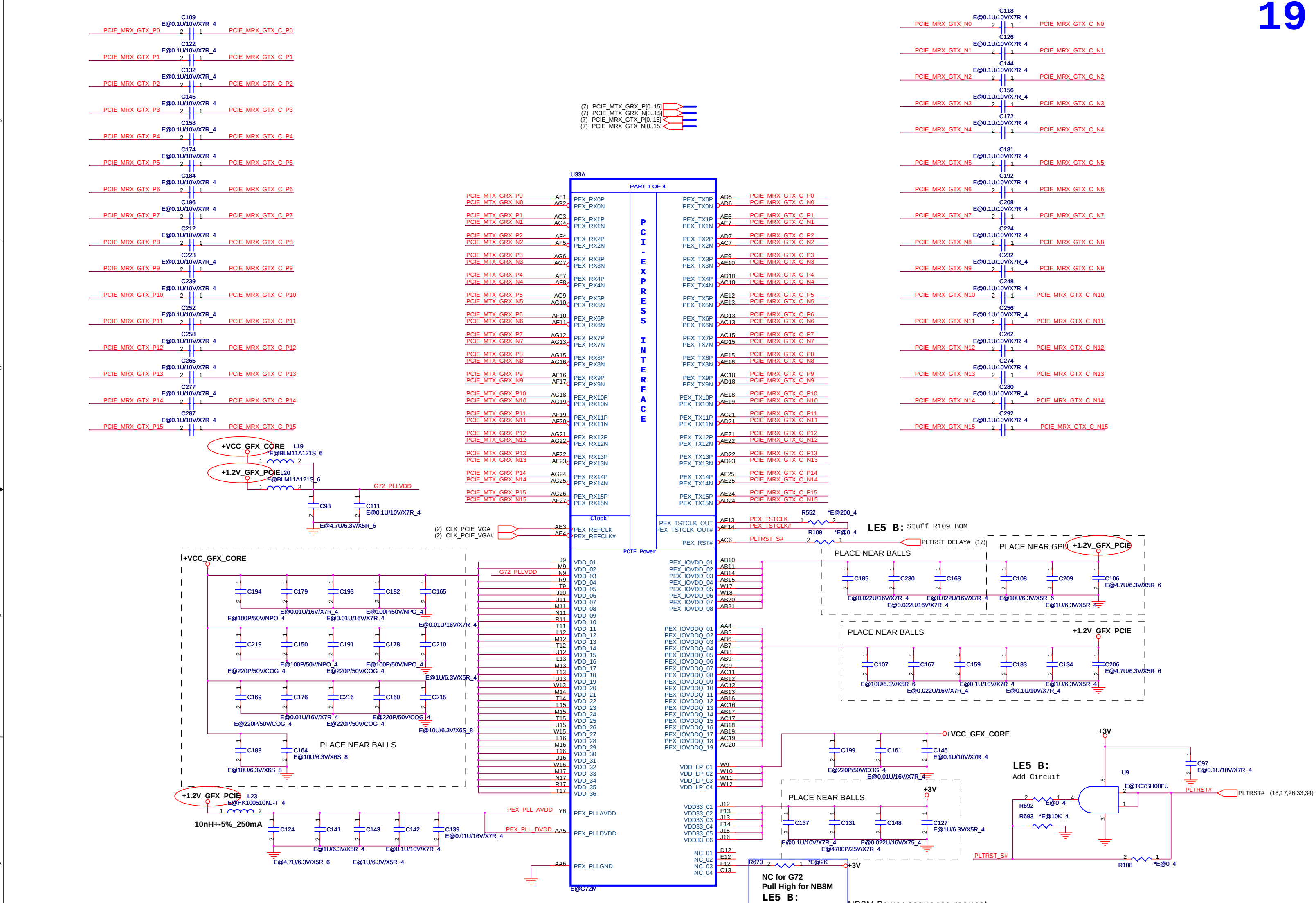


PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH8-M POWER (4 of 4)	1A

Date: Tuesday, November 28, 2006 Sheet 18 of 43



NB8M Power sequence request

3.3V-->1.2V-->1.8V

G72M Power sequence request

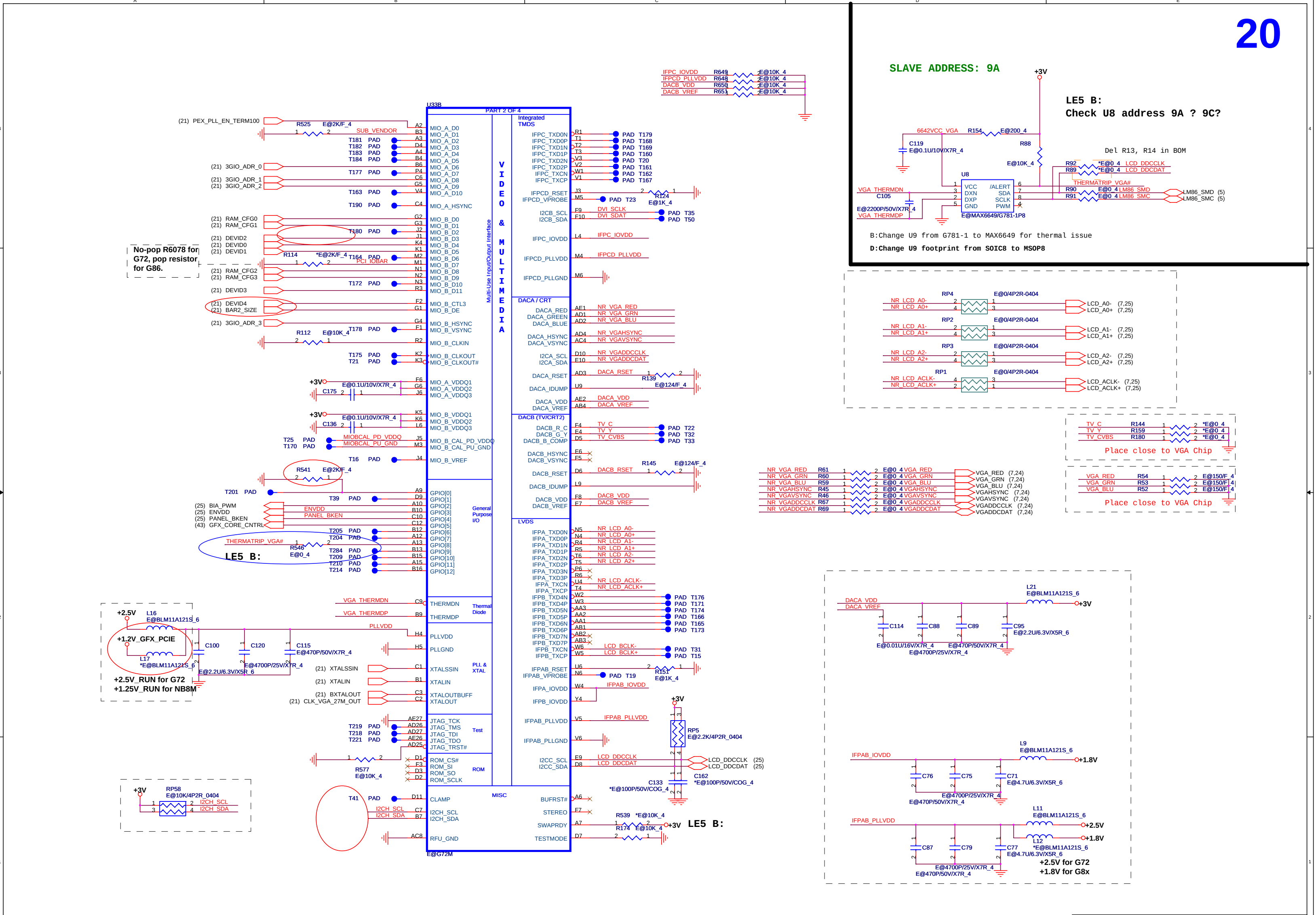
3.3V -->2.5V -->1.2V-->1.8V

PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
C	VGA-G72M (PCIe,POWER)	1A

Date: Wednesday, November 29, 2006 Sheet 19 of 43

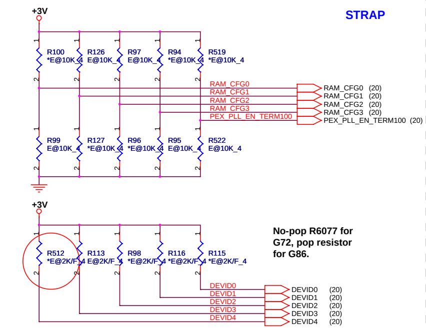


PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
C	VGA-G72M (VIDEO)	1A

Date: Wednesday, November 29, 2006 Sheet 20 of 43

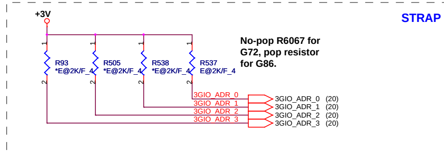


Infineon/Hynix	CFG3	CFG2	CFG1	CFG0
128MB(16M*16)	0	0	1	0
256MB(32M*16)	0	1	1	0
	DEV3	DEV2	DEV1	DEV0
(256MB)G72GLM	1	X	0	0
(128MB)G72MV	0	1	1	1

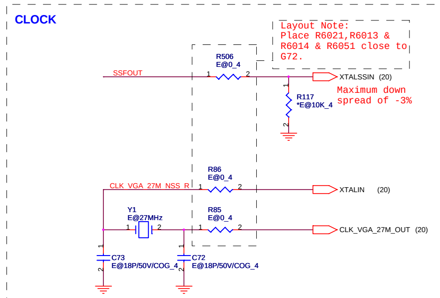
Note: 256MB: Pop R606; depop R6001.
128MB: Pop R6001; depop R606.

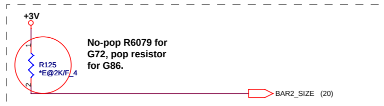
RAM_CFG[3:0]	RAM_CFG[3:0]	Vendor	
0000	DDR2 16Mx16x4,64bit,128MB	Elpida	
0001	DDR2 16Mx16x4,64bit,128MB	Samsung	V(0000)
0010	DDR2 16Mx16x4,64bit,128MB	Infineon	V(0020)
0011	DDR2 16Mx16x4,64bit,128MB	Hynix	V(0010)
0100	Reserve		
0101	DDR2 32Mx16x4,64bit,256MB	Samsung	
0110	DDR2 32Mx16x4,64bit,256MB	Infineon	
0111	DDR2 32Mx16x4,64bit,256MB	Hynix	
1000	DDR2 16Mx16x2,32bit,64MB	Elpida	
1001	DDR2 16Mx16x2,32bit,64MB	Samsung	
1010	DDR2 16Mx16x2,32bit,64MB	Infineon	
1011	DDR2 16Mx16x2,32bit,64MB	Hynix	

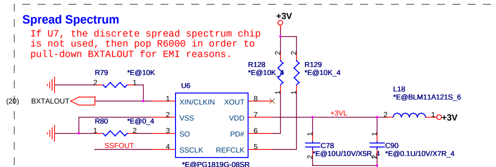
PCI_DEVID[4:0]	Description
00000	NB8M
01000	G72M



3GIO_ADR_X	ADR3	ADR2	ADR1	ADR0
Desktop	0	0	0	0
Mobile	0	0	0	1





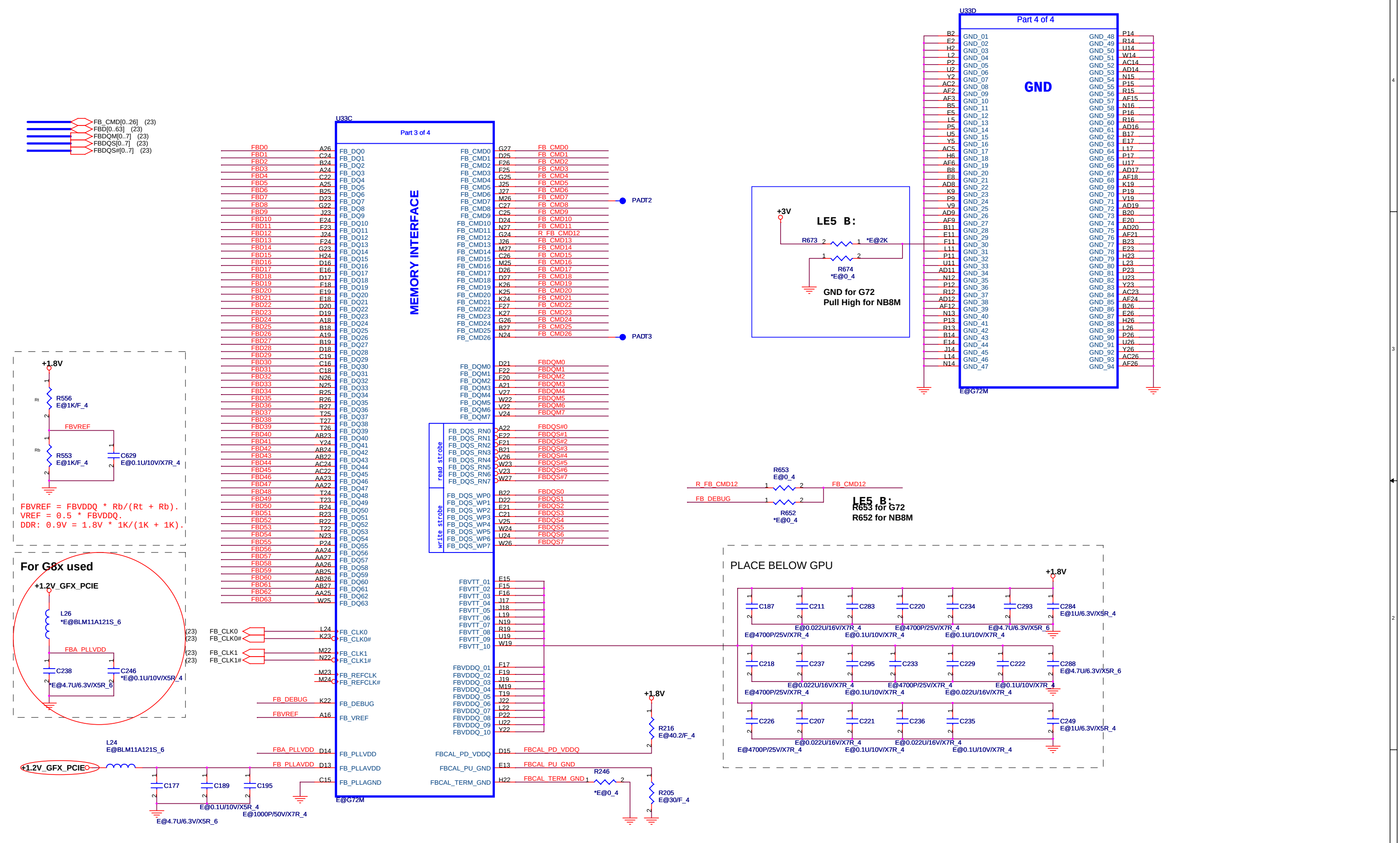


	S0
-1.75% (DOWN)	0
0.85% (CENTER)	1

PROJECT : LE5
Quanta Computer Inc.

Size	Document Number	Rev
C	VGA-G72M (STRAP,CLOCK)	1A

Date: Wednesday, November 29, 2006 Sheet 21 of 43

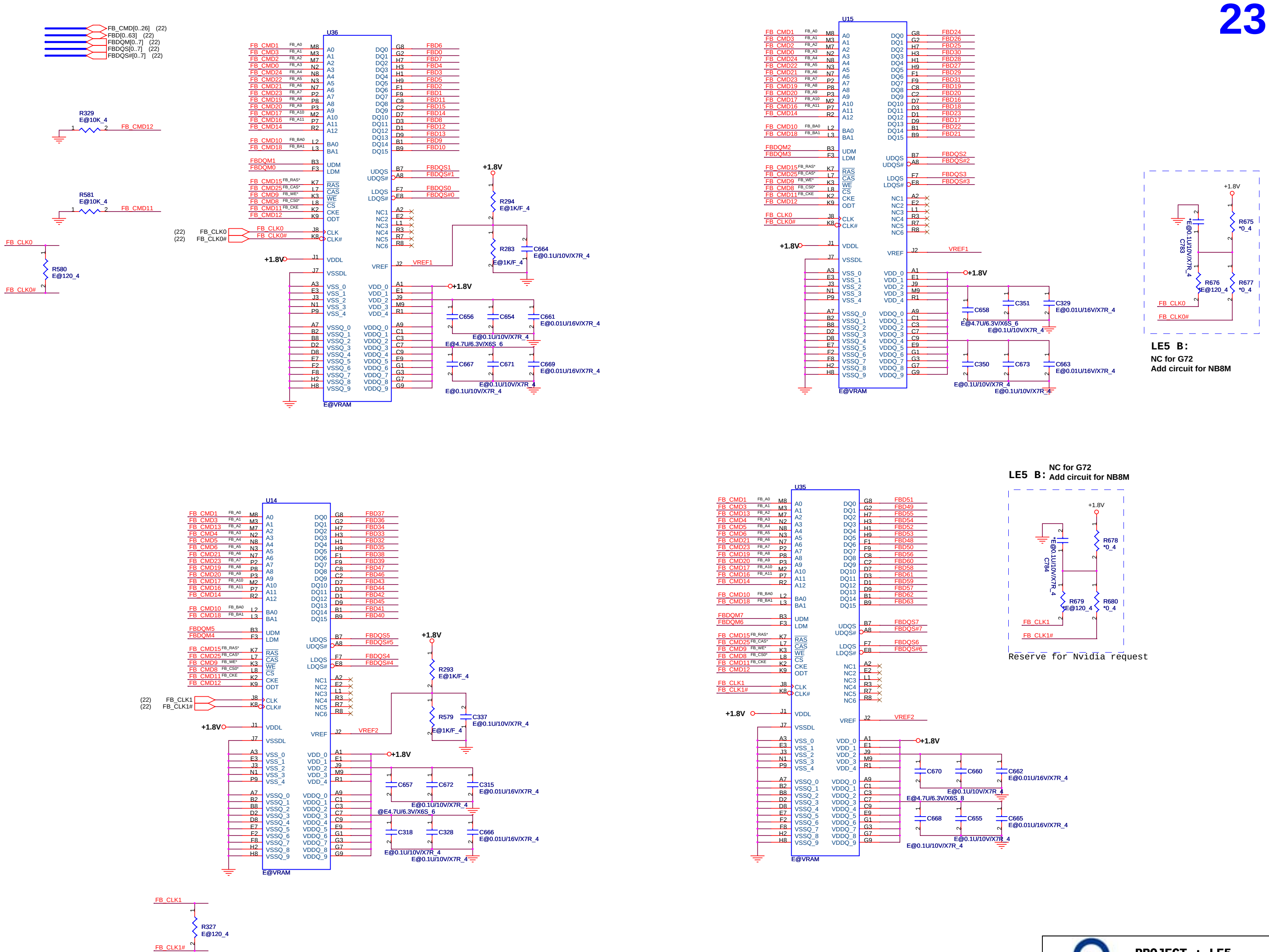


PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
C	VGA-G72M (MEMORY,GUD)	1A

Date: Wednesday, November 29, 2006 Sheet 22 of 43



PROJECT : LE5

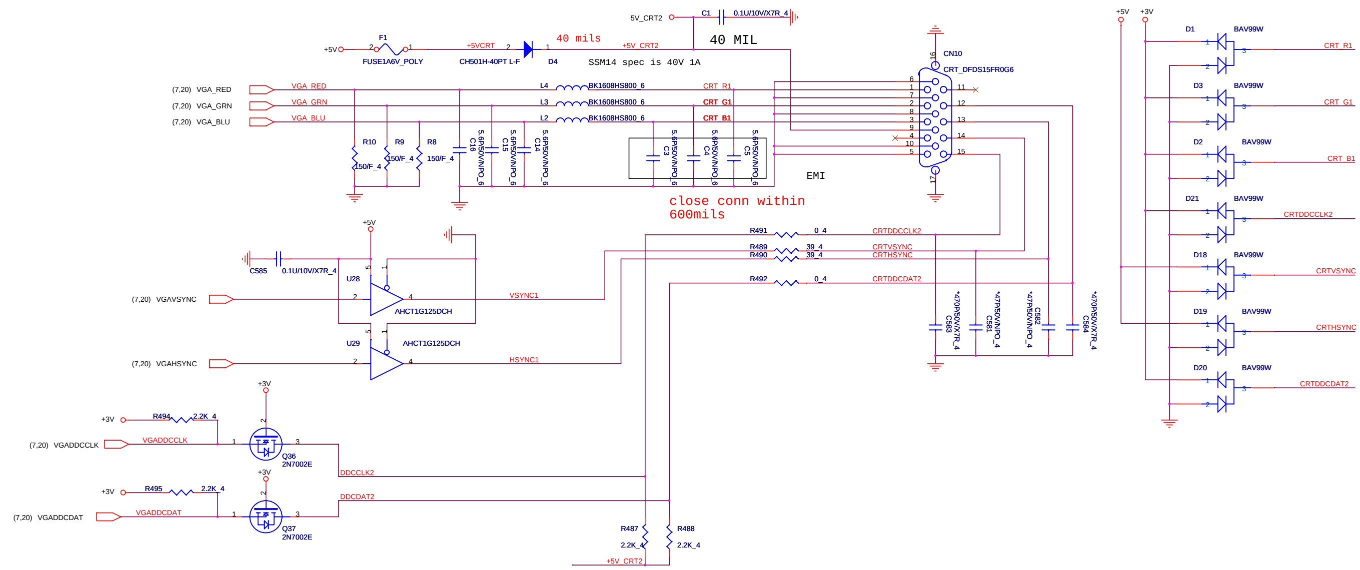
Quanta Computer Inc.

Size	Document Number	Rev
C	VGA-G72M (VRAM)	1A

Date: Wednesday, November 29, 2006 Sheet 23 of 43

CRT PORT

25

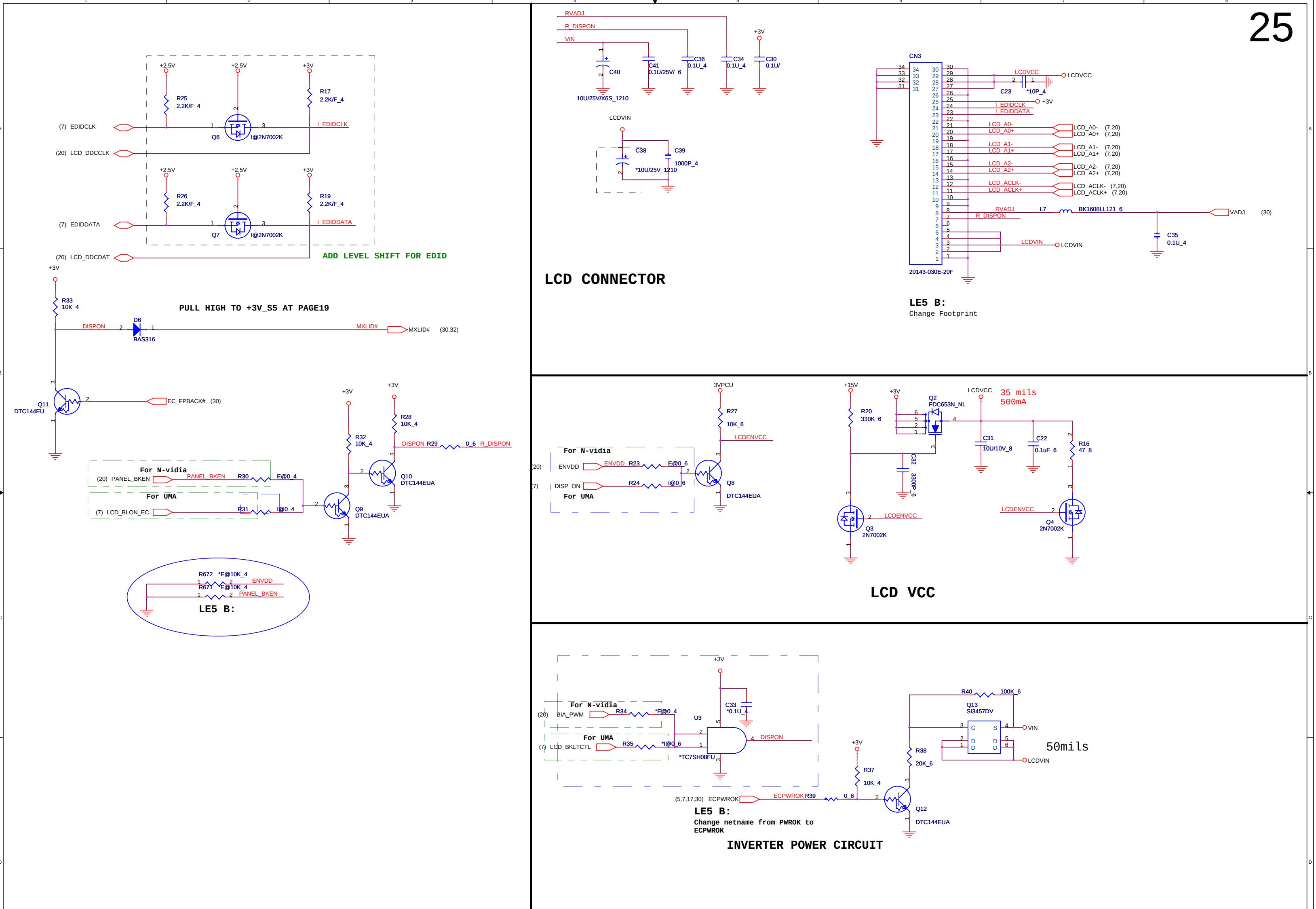


PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
C	CRT	1A

Date: Wednesday, November 29, 2006 | Sheet 24 of 43

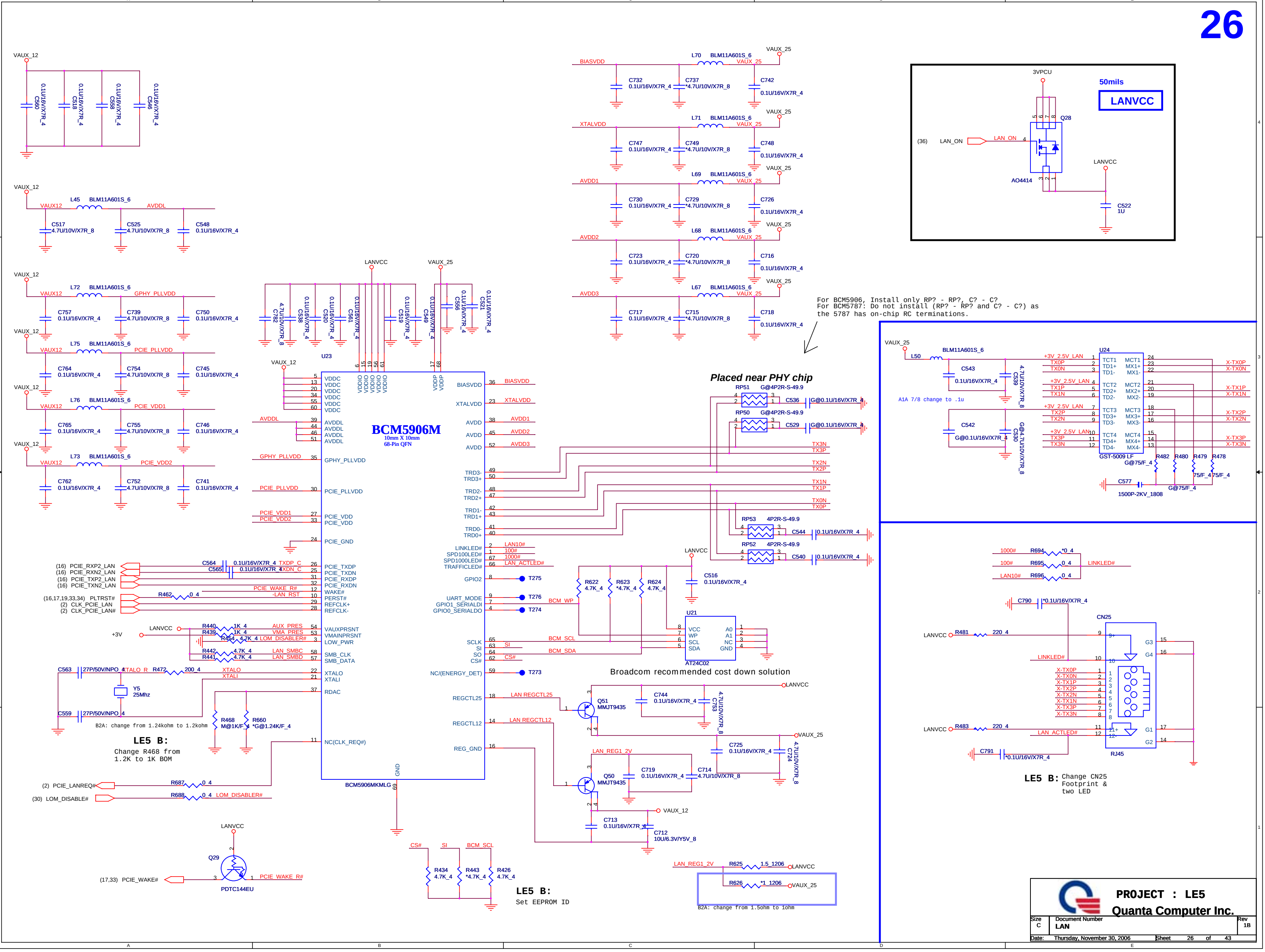


PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
C	LCDCONNECTOR	1A

Date: Wednesday, November 29, 2006 Sheet 25 of 43

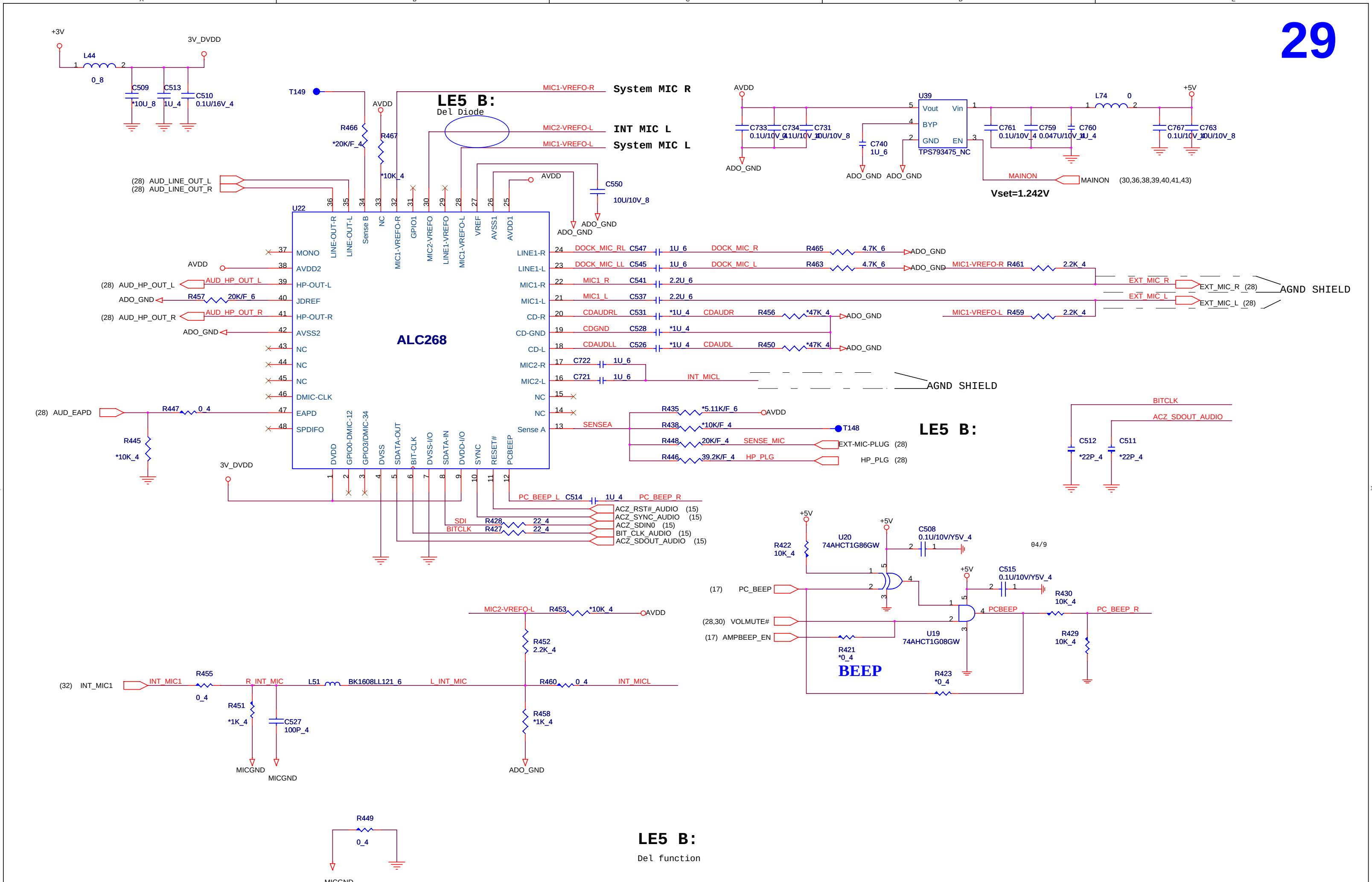


PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
C	LAN	1B

Date: Thursday, November 30, 2006 Sheet 26 of 43



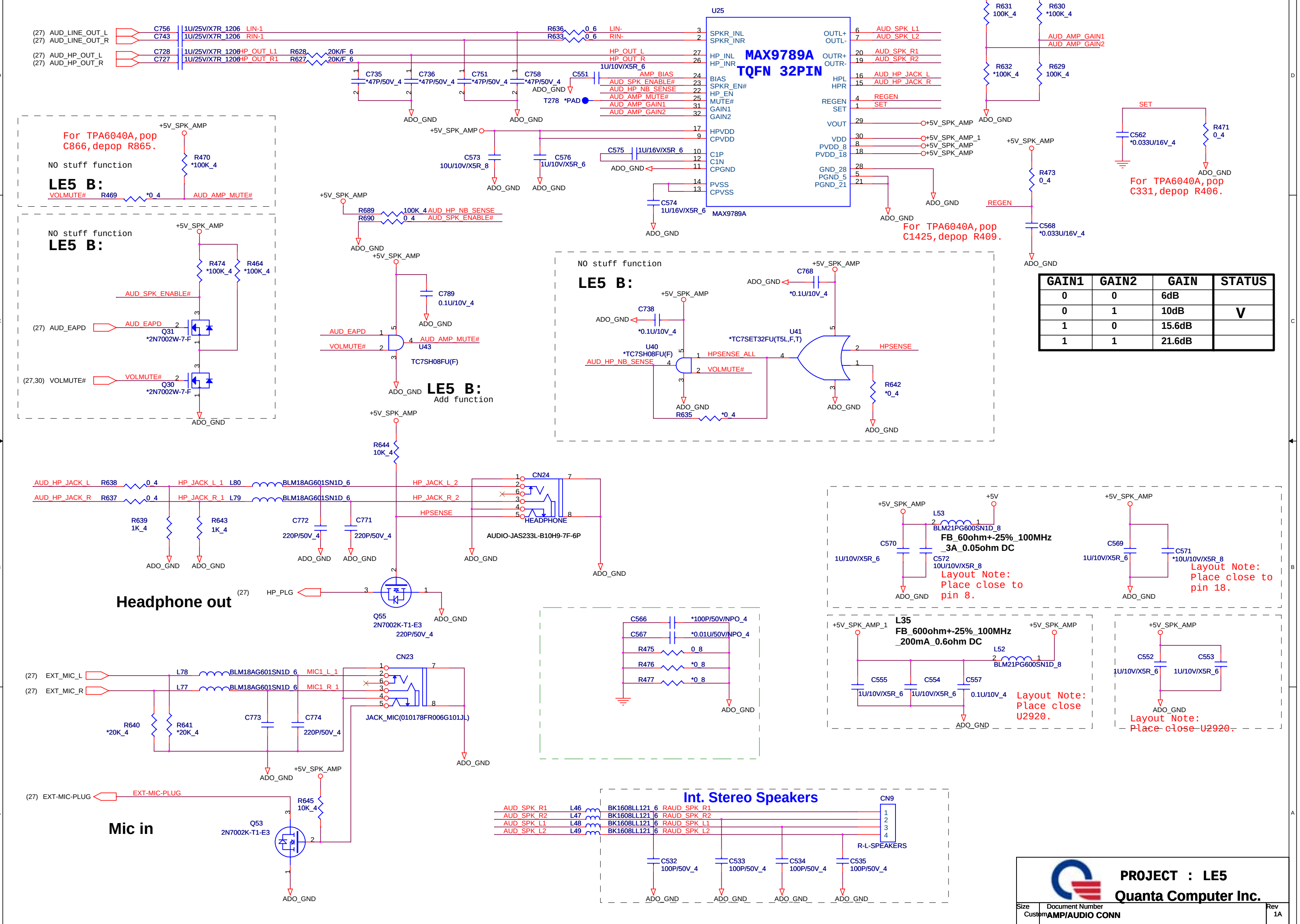
PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia ALC268	1A

Date: Thursday, November 30, 2006 Sheet 27 of 43

AUDIO AMPLIFIER



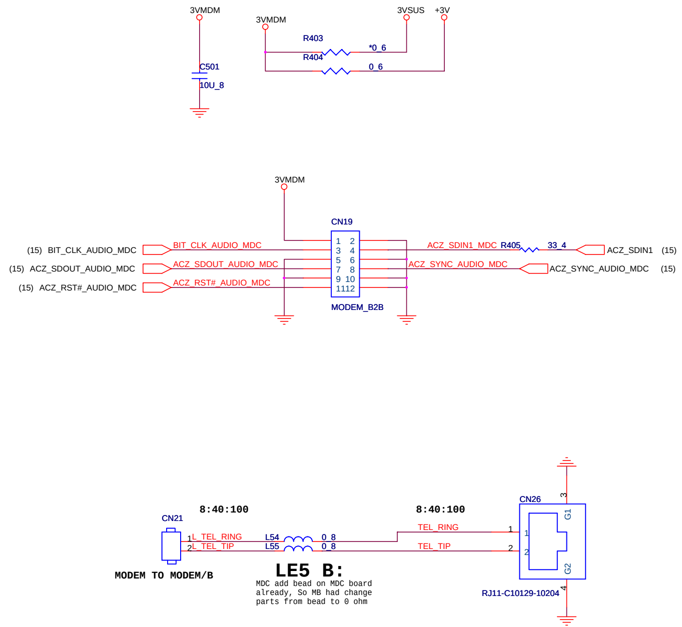
GAIN1	GAIN2	GAIN	STATUS
0	0	6dB	
0	1	10dB	V
1	0	15.6dB	
1	1	21.6dB	

PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP/AUDIO CONN	1A

Date: Thursday, November 30, 2006 Sheet 28 of 43

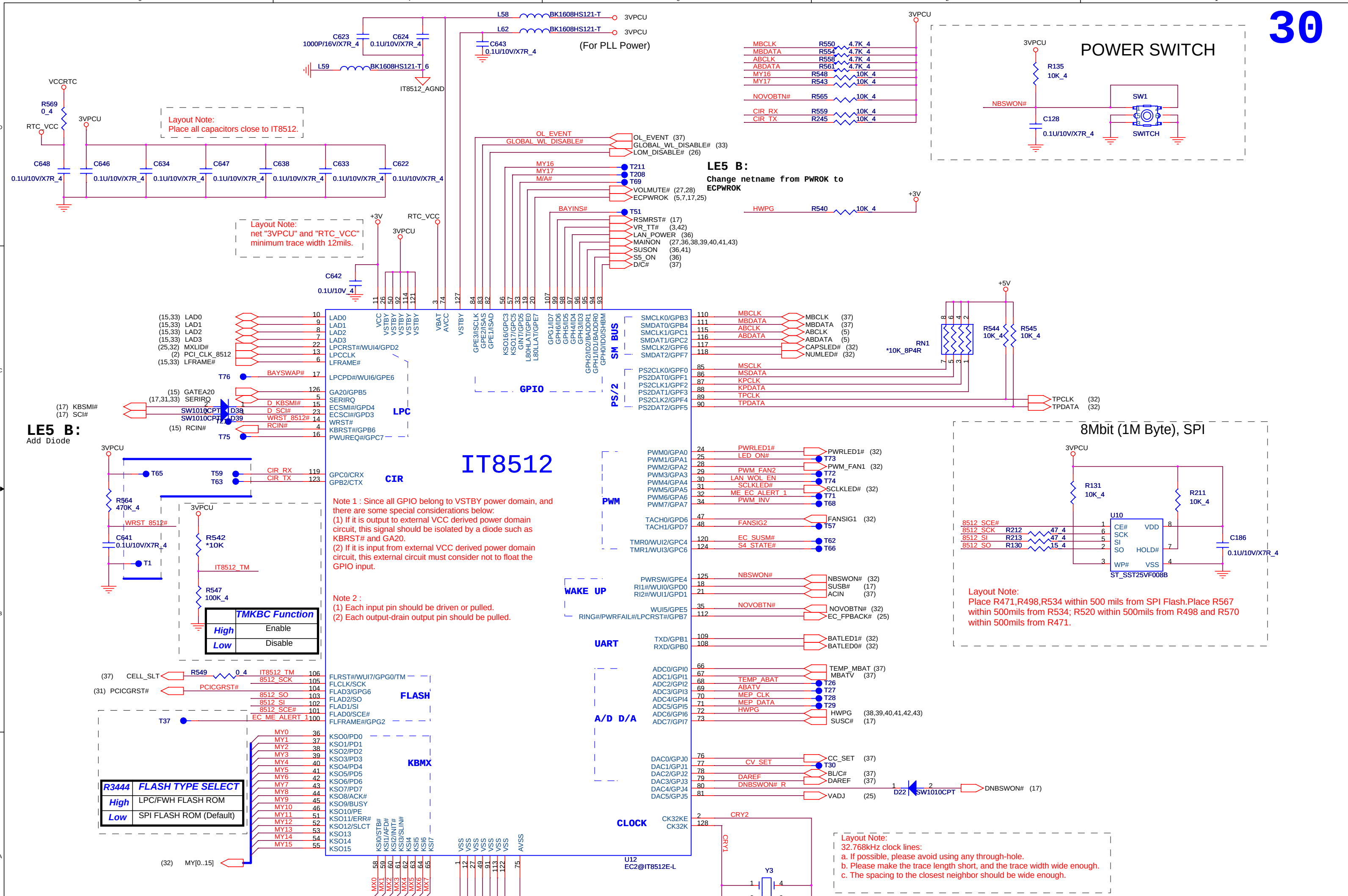


PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
Custom	**MDC conn & RJ11**	1A

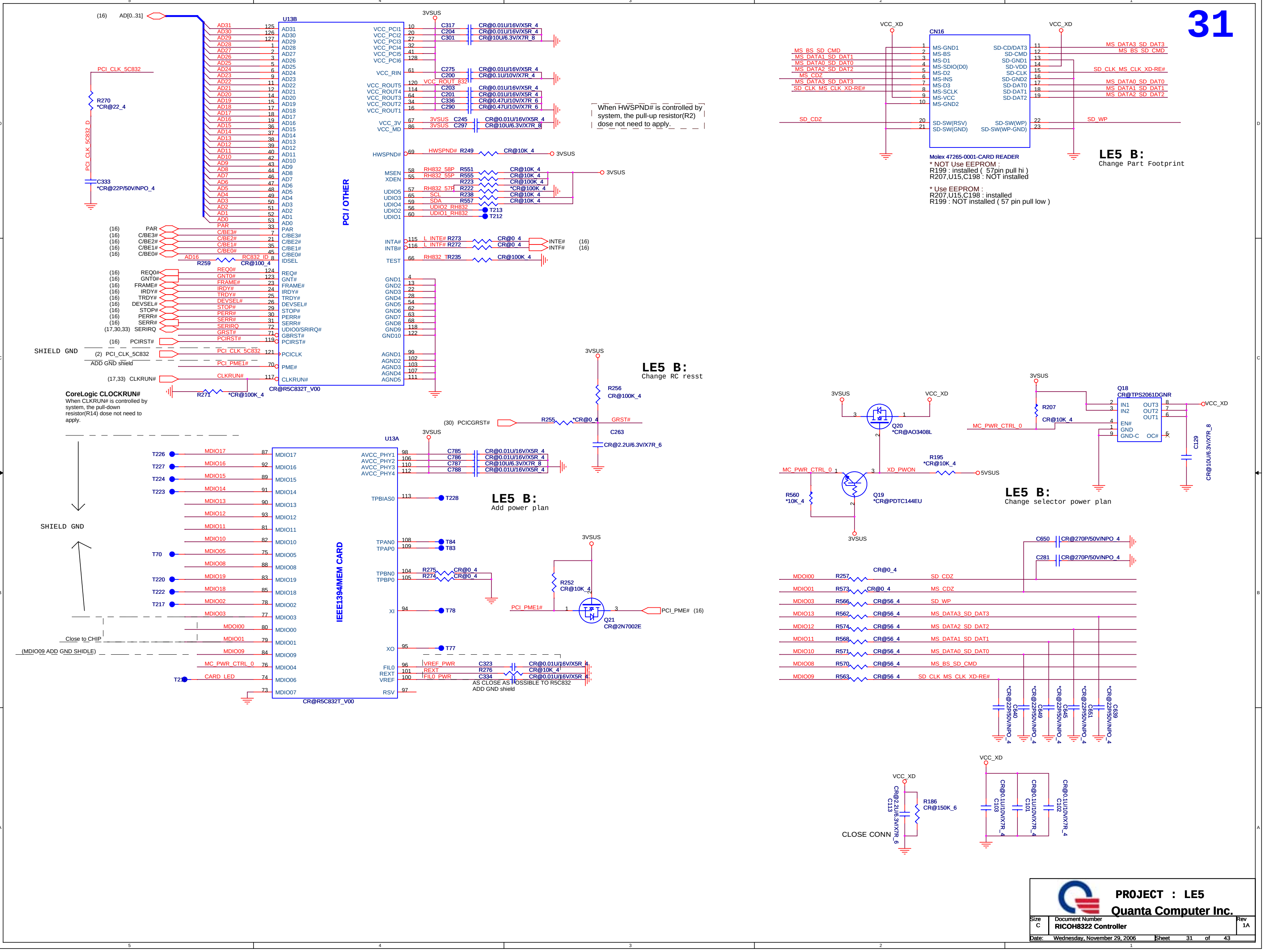
Date: Wednesday, November 29, 2006 | Sheet 29 of 43



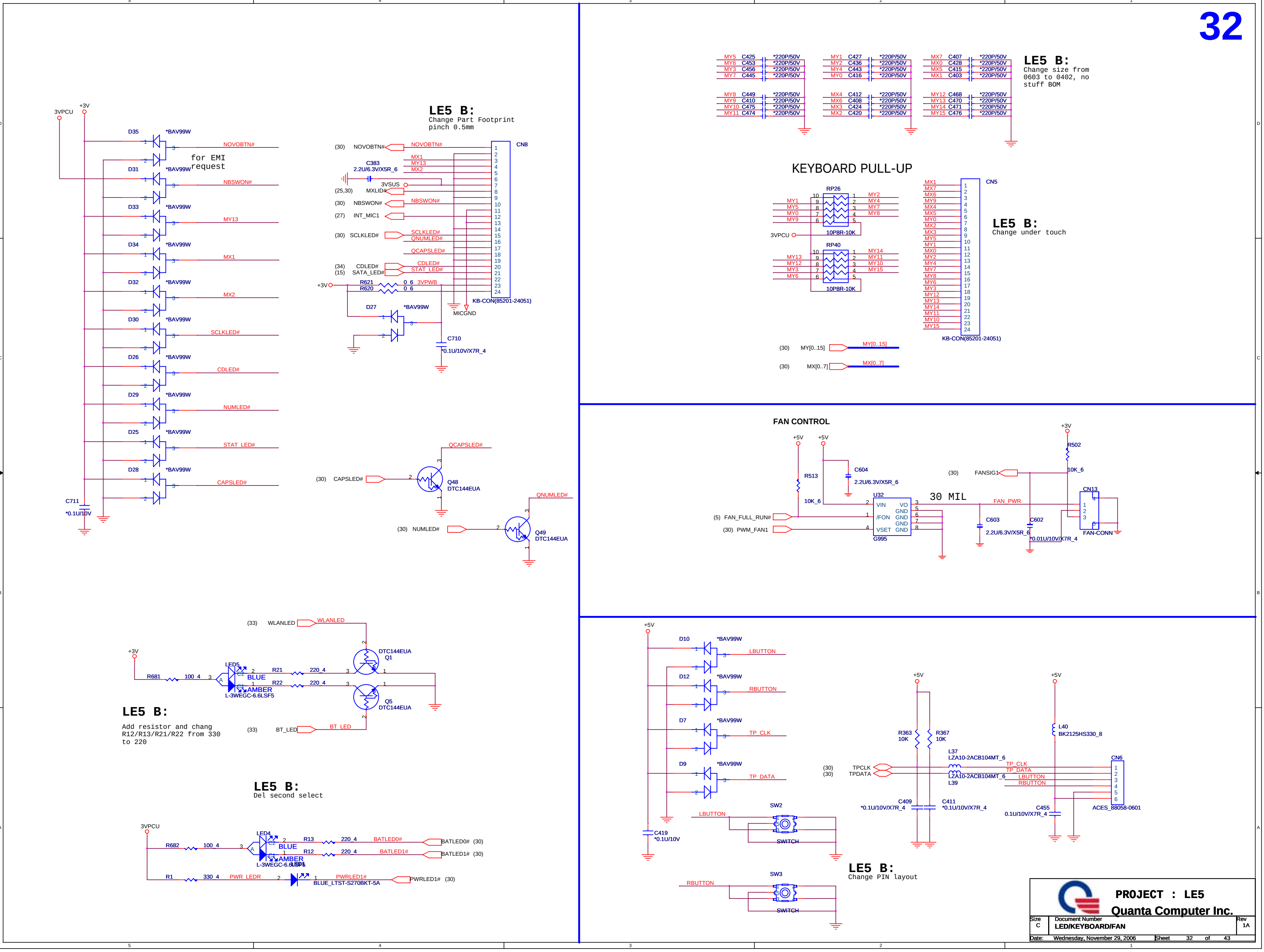
PROJECT : LE5
Quanta Computer Inc.

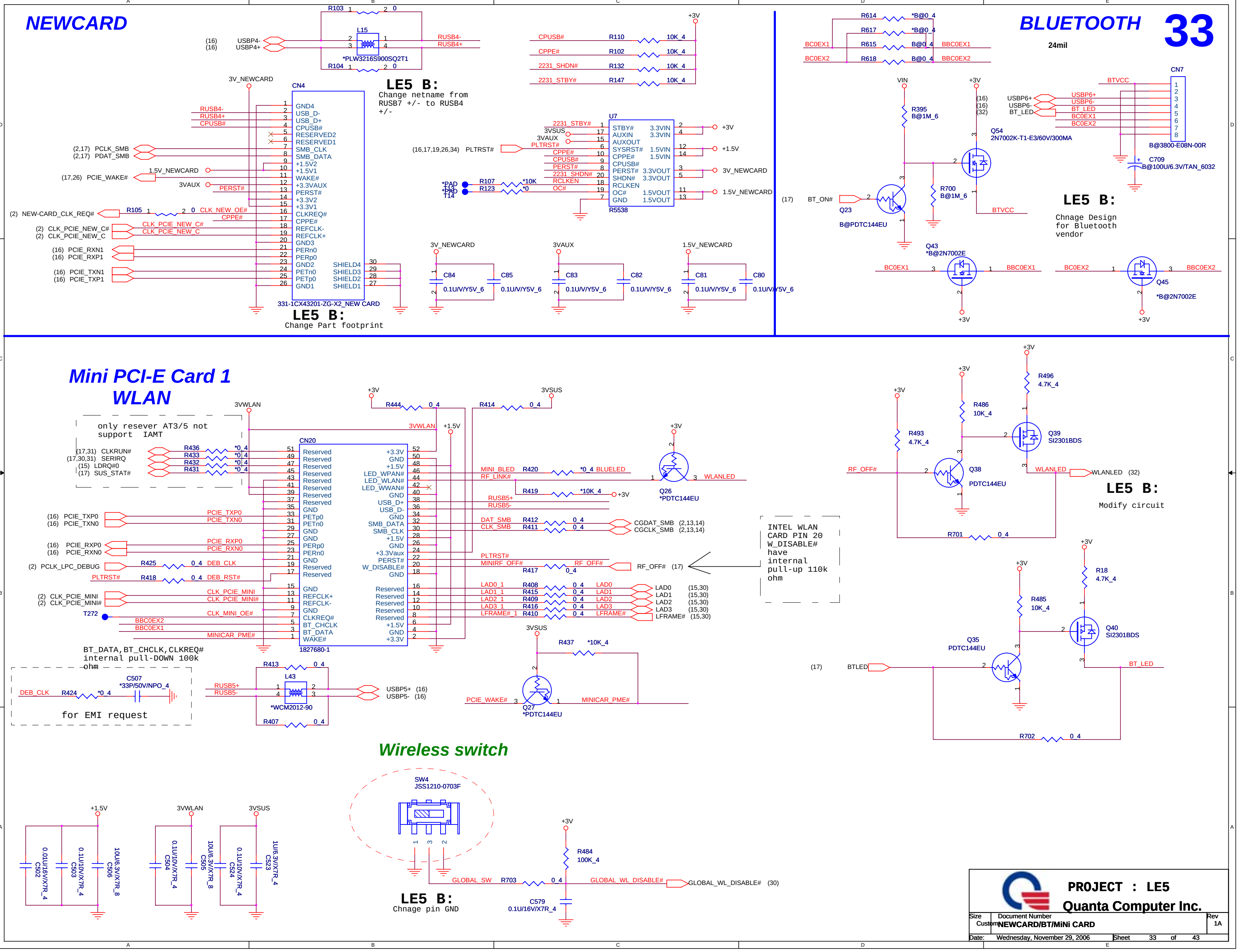
Size	Document Number	Rev
Custom	KBC-IT8512	1A

Date: Wednesday, November 29, 2006 Sheet 30 of 43

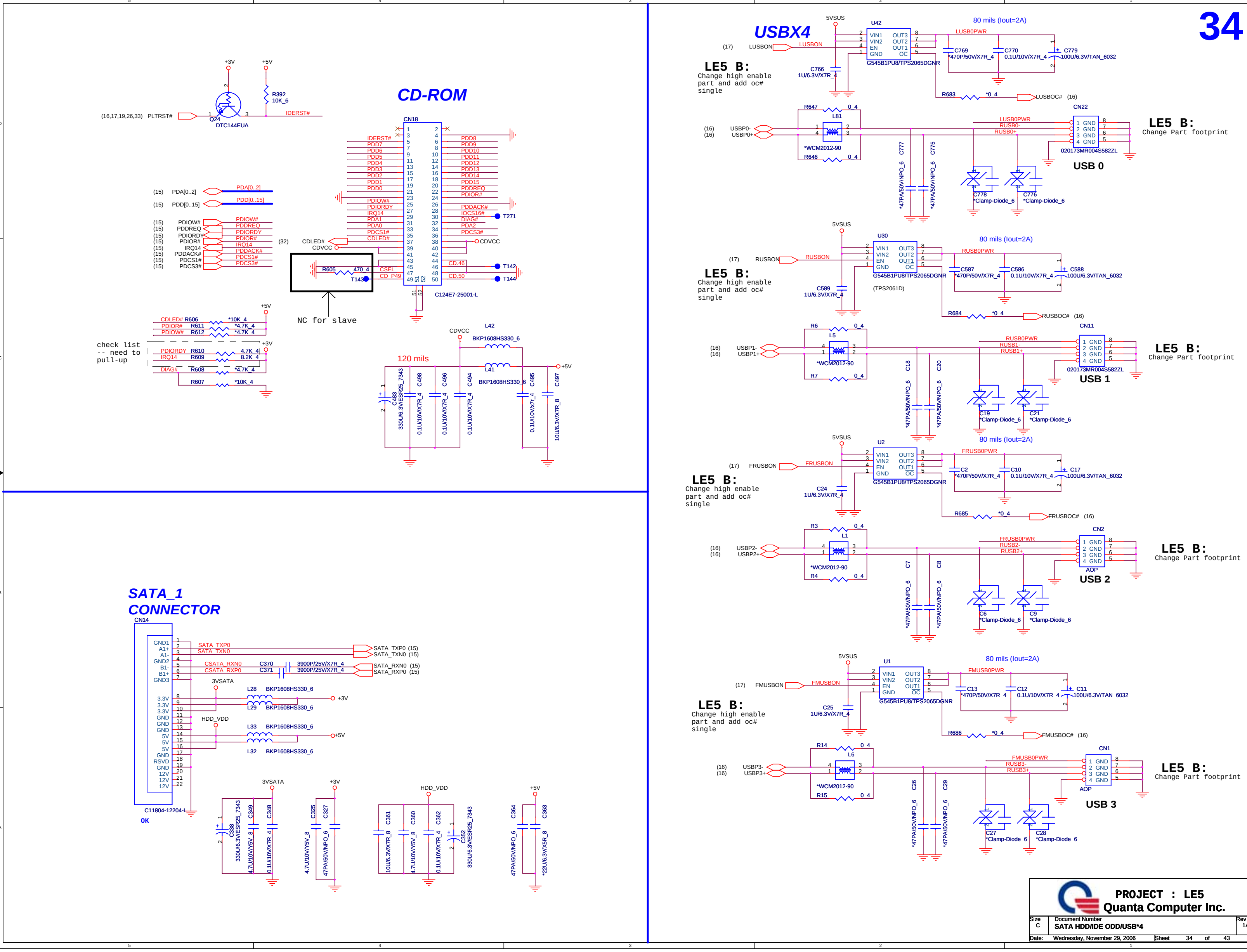


31
PCI / OTHER
U13B
CR@R5C832T_V00
IEEE1394/MEM CARD
U13A
When HWSPND# is controlled by system, the pull-up resistor(R2) dose not need to apply.
CoreLogic CLOCKRUN#
When CLKRUN# is controlled by system, the pull-down resistor(R14) dose not need to apply.
SHIELD GND
ADD GND shield
Close to CHIP
(MDIO09 ADD GND SHIDLE)
AS CLOSE AS POSSIBLE TO R5C832
ADD GND shield
LE5 B:
Change RC resst
LE5 B:
Add power plan
LE5 B:
Change Part Footprint
LE5 B:
Change selector power plan
CN16
Molex 47265-0001-CARD READER
* NOT Use EEPROM :
R199 : installed (57pin pull hi)
R207,U15,C198 : NOT installed
* Use EEPROM :
R207,U15,C198 : installed
R199 : NOT installed (57 pin pull low)
Q18
CR@TPS2061DGNR
Q20
*CR@AO3408L
Q19
*CR@PDTC144EU
Q21
CR@2N7002E
CLOSE CONN
PROJECT : LE5
Quanta Computer Inc.
Size C
Document Number
RICOH8322 Controller
Rev 1A
Date: Wednesday, November 29, 2006
Sheet 31 of 43

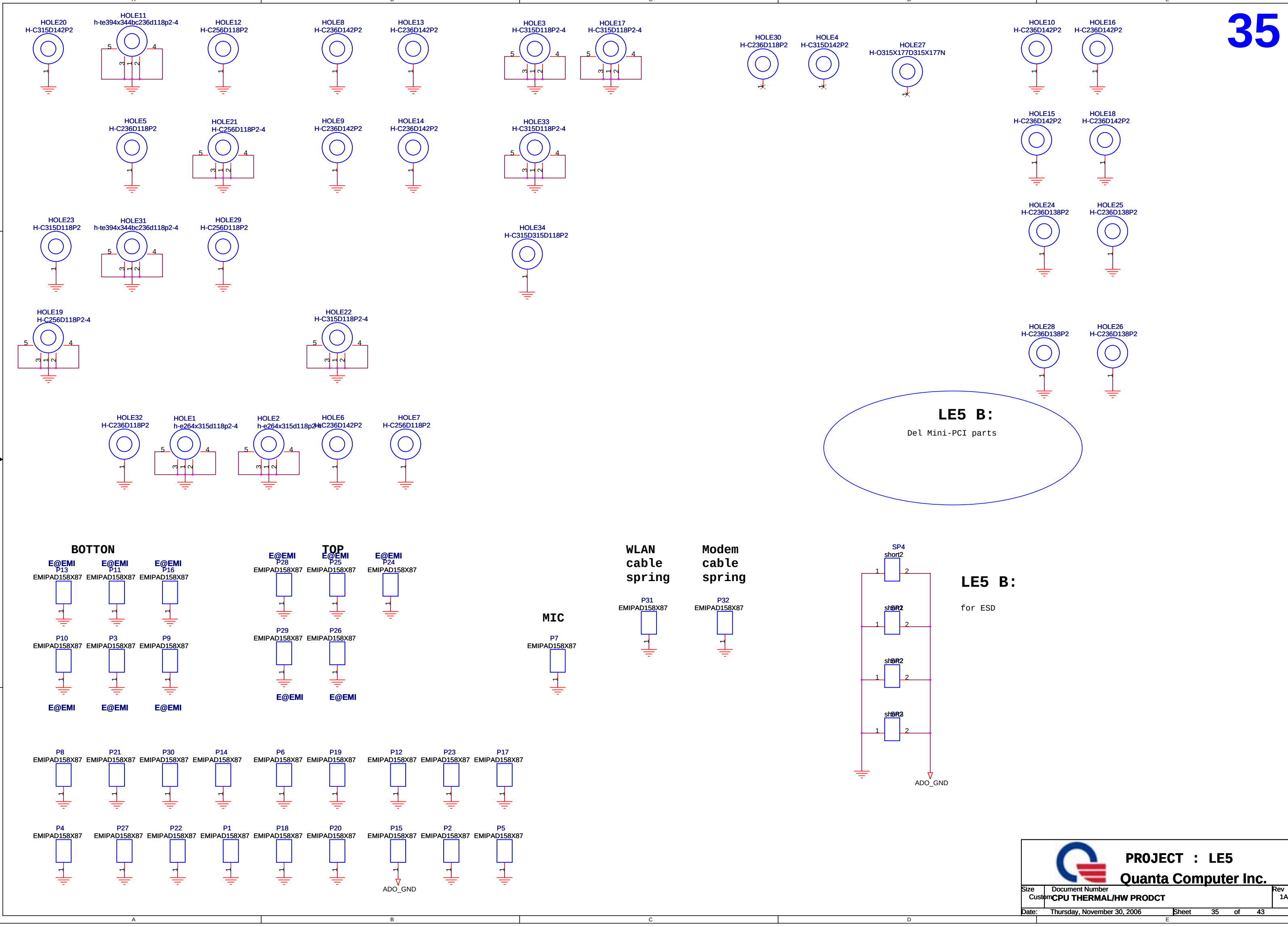

LE5 B:
Change Part Footprint
pinch 0.5mm
for EMI
request
LE5 B:
Change size from
0603 to 0402, no
stuff BOM
KEYBOARD PULL-UP
LE5 B:
Change under touch
FAN CONTROL
30 MIL
LE5 B:
Add resistor and chang
R12/R13/R21/R22 from 330
to 220
LE5 B:
Del second select
LE5 B:
Change PIN layout
KB-CON(85201-24051)
DTC144EUA
G995
FAN-CONN
ACES_88058-0601
SWITCH
L-3WEGC-6.6LSF5
BLUE_LTST-S270BKT-5A
PROJECT : LE5
Quanta Computer Inc.
Size C
Document Number LED/KEYBOARD/FAN
Rev 1A
Date: Wednesday, November 29, 2006
Sheet 32 of 43



NEWCARD
BLUETOOTH
33
24mil
USBP4-
USBP4+
R103
R104
L15
*PLW3216S900SQ2T1
RUSB4-
RUSB4+
LE5 B:
Change netname from RUSB7 +/- to RUSB4 +/-
CPUSB#
CPPE#
2231_SHDN#
2231_STBY#
R110 10K_4
R102 10K_4
R132 10K_4
R147 10K_4
+3V
3V_NEWCARD
CN4
GND4
USB_D-
USB_D+
CPUSB#
RESERVED2
RESERVED1
SMB_CLK
SMB_DATA
+1.5V2
+1.5V1
WAKE#
+3.3VAUX
PERST#
+3.3V2
+3.3V1
CLKREQ#
CPPE#
REFCLK-
REFCLK+
GND3
PERn0
PERp0
GND2
PETn0
PETp0
GND1
SHIELD4
SHIELD3
SHIELD2
SHIELD1
331-1CX43201-ZG-X2_NEW CARD
LE5 B:
Change Part footprint
(2,17) PCLK_SMB
(2,17) PDAT_SMB
1.5V_NEWCARD
(17,26) PCIE_WAKE#
3VAUX
PERST#
(2) NEW-CARD_CLK_REQ#
R105
CLK_NEW_OE#
CPPE#
(2) CLK_PCIE_NEW_C#
(2) CLK_PCIE_NEW_C
CLK_PCIE_NEW_C#
CLK_PCIE_NEW_C
(16) PCIE_RXN1
(16) PCIE_RXP1
(16) PCIE_TXN1
(16) PCIE_TXP1
U7
R5538
STBY#
AUXIN
AUXOUT
SYSRST#
CPPE#
CPUSB#
PERST#
SHDN#
RCLKEN
OC#
GND
3.3VIN
1.5VIN
3.3VOUT
1.5VOUT
(16,17,19,26,34) PLTRST#
*PAD T14
R107 *10K
R123 *0
RCLKEN
OC#
+1.5V
1.5V_NEWCARD
C84 0.1U/V/Y5V_6
C85 0.1U/V/Y5V_6
C83 0.1U/V/Y5V_6
C82 0.1U/V/Y5V_6
C81 0.1U/V/Y5V_6
C80 0.1U/V/Y5V_6
R614 *B@0_4
R617 *B@0_4
R615 B@0_4
R618 B@0_4
BC0EX1
BC0EX2
BBC0EX1
BBC0EX2
VIN
R395 B@1M_6
Q54 2N7002K-T1-E3/60V/300MA
R700 B@1M_6
(17) BT_ON#
Q23
B@PDTC144EU
BTVCC
(16) USBP6+
(16) USBP6-
(32) BT_LED
CN7
B@3800-E08N-00R
C709 B@100U/6.3V/TAN_6032
LE5 B:
Chnage Design for Bluetooth vendor
Q43 *B@2N7002E
Q45 *B@2N7002E
Mini PCI-E Card 1 WLAN
3VWLAN
only resever AT3/5 not support IAMT
(17,31) CLKRUN#
(17,30,31) SERIRQ
(15) LDRQ#0
(17) SUS_STAT#
R436 *0_4
R433 *0_4
R432 *0_4
R431 *0_4
R444 0_4
R414 0_4
3VSUS
CN20
1827680-1
Reserved
+3.3V
GND
+1.5V
LED_WPAN#
LED_WLAN#
LED_WWAN#
USB_D+
USB_D-
SMB_DATA
SMB_CLK
+3.3Vaux
PERST#
W_DISABLE#
PETp0
PETn0
PERp0
PERn0
REFCLK+
REFCLK-
CLKREQ#
BT_CHCLK
BT_DATA
WAKE#
(16) PCIE_TXP0
(16) PCIE_TXN0
(16) PCIE_RXP0
(16) PCIE_RXN0
(2) PCLK_LPC_DEBUG
R425 0_4 DEB_CLK
PLTRST#
R418 0_4 DEB_RST#
(2) CLK_PCIE_MINI
(2) CLK_PCIE_MINI#
T272
CLK_MINI_OE#
BBC0EX2
BBC0EX1
MINICAR_PME#
MINI_BLED
RF_LINK#
R420 *0_4 BLUELED
R419 *10K_4
Q26 *PDTC144EU
WLANLED
RUSB5+
RUSB5-
DAT_SMB
CLK_SMB
R412 0_4
R411 0_4
CGDAT_SMB (2,13,14)
CGCLK_SMB (2,13,14)
MINIRF_OFF#
R417 0_4
RF_OFF#
RF_OFF# (17)
INTEL WLAN CARD PIN 20 W_DISABLE# have internal pull-up 110k ohm
LAD0_1
LAD1_1
LAD2_1
LAD3_1
LFRAME#_1
R408 0_4
R415 0_4
R409 0_4
R416 0_4
R410 0_4
LAD0 (15,30)
LAD1 (15,30)
LAD2 (15,30)
LAD3 (15,30)
LFRAME# (15,30)
BT_DATA,BT_CHCLK,CLKREQ# internal pull-DOWN 100k ohm
C507 *33P/50V/NPO_4
DEB_CLK
R424 *0_4
for EMI request
R413 0_4
L43
*WCM2012-90
R407 0_4
USBP5+ (16)
USBP5- (16)
R437 *10K_4
PCIE_WAKE#
Q27 *PDTC144EU
R496 4.7K_4
R486 10K_4
R493 4.7K_4
Q39 SI2301BDS
Q38 PDTC144EU
WLANLED (32)
LE5 B:
Modify circuit
R701 0_4
R18 4.7K_4
R485 10K_4
Q40 SI2301BDS
Q35 PDTC144EU
(17) BTLED
BT_LED
R702 0_4
Wireless switch
SW4
JSS1210-0703F
+3V
R484 100K_4
GLOBAL_SW
R703 0_4
GLOBAL_WL_DISABLE#
GLOBAL_WL_DISABLE# (30)
C579 0.1U/16V/X7R_4
LE5 B:
Chnage pin GND
C502 0.01U/16V/X7R_4
C503 0.1U/10V/X7R_4
C506 10U/6.3V/X7R_8
C504 0.1U/10V/X7R_4
C505 10U/6.3V/X7R_8
C524 0.1U/10V/X7R_4
C523 1U/6.3V/X7R_4
PROJECT : LE5
Quanta Computer Inc.
Size Custom
Document Number NEWCARD/BT/MINI CARD
Rev 1A
Date: Wednesday, November 29, 2006
Sheet 33 of 43



34
CD-ROM
CN18
C124E7-25001-L
IDERST#
DTC144EUA
Q24
R392
10K_6
PLTRST#
PDA[0..2]
PDD[0..15]
PDIOW#
PDDREQ
PDIORDY
PDIOR#
IRQ14
PDDACK#
PDCS1#
PDCS3#
CDLED#
CDVCC
CSEL
R605
470_4
T143
T142
T144
T271
NC for slave
check list
-- need to
pull-up
R606 *10K_4
R611 *4.7K_4
R612 *4.7K_4
R610 4.7K_4
R609 8.2K_4
R608 *4.7K_4
R607 *10K_4
120 mils
L42
L41
BKP1608HS330_6
C483
330U/6.3V/ESR25_7343
C498
C496
C494
C495
C497
0.1U/10V/X7R_4
10U/6.3V/X7R_8
SATA_1
CONNECTOR
CN14
C11804-12204-L
OK
SATA_TXP0
SATA_TXN0
SATA_RXN0
SATA_RXP0
C370
C371
3900P/25V/X7R_4
3VSATA
HDD_VDD
L28
L29
L33
L32
+3V
+5V
USBX4
5VSUS
U42
G545B1PU8/TPS2065DGNR
LUSBON
LUSB0PWR
80 mils (Iout=2A)
C769
C770
C779
C766
*470P/50V/X7R_4
0.1U/10V/X7R_4
100U/6.3V/TAN_6032
1U/6.3V/X7R_4
LE5 B:
Change high enable
part and add oc#
single
R683
*0_4
LUSBOC#
R647
R646
L81
*WCM2012-90
USBP0-
USBP0+
CN22
020173MR004S582ZL
USB 0
LE5 B:
Change Part footprint
C777
C775
*47PA/50V/NPO_6
C778
C776
*Clamp-Diode_6
U30
RUSBON
RUSB0PWR
C587
C586
C588
C589
(TPS2061D)
R684
RUSBOC#
R6
R7
L5
USBP1-
USBP1+
CN11
USB 1
C18
C20
C19
C21
U2
FRUSBON
FRUSB0PWR
C2
C10
C17
C24
R685
FRUSBOC#
R3
R4
L1
USBP2-
USBP2+
CN2
AOP
USB 2
C7
C8
C6
C9
U1
FMUSBON
FMUSB0PWR
C13
C12
C11
C25
R686
FMUSBOC#
R14
R15
L6
USBP3-
USBP3+
CN1
USB 3
C26
C29
C27
C28
PROJECT : LE5
Quanta Computer Inc.
Size C
Document Number
SATA HDD/IDE ODD/USB*4
Rev 1A
Date: Wednesday, November 29, 2006
Sheet 34 of 43



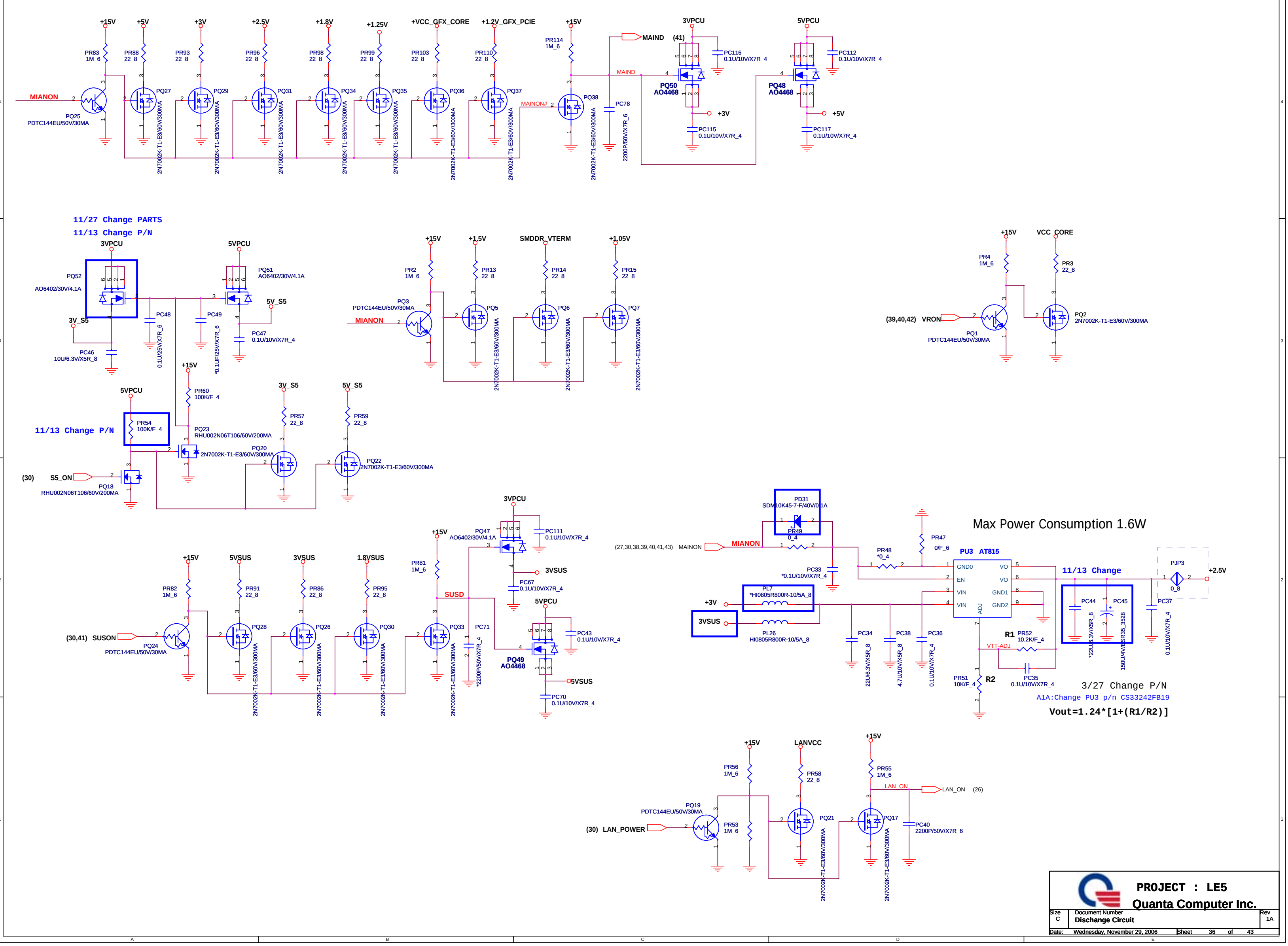
PROJECT : LE5

Quanta Computer Inc.

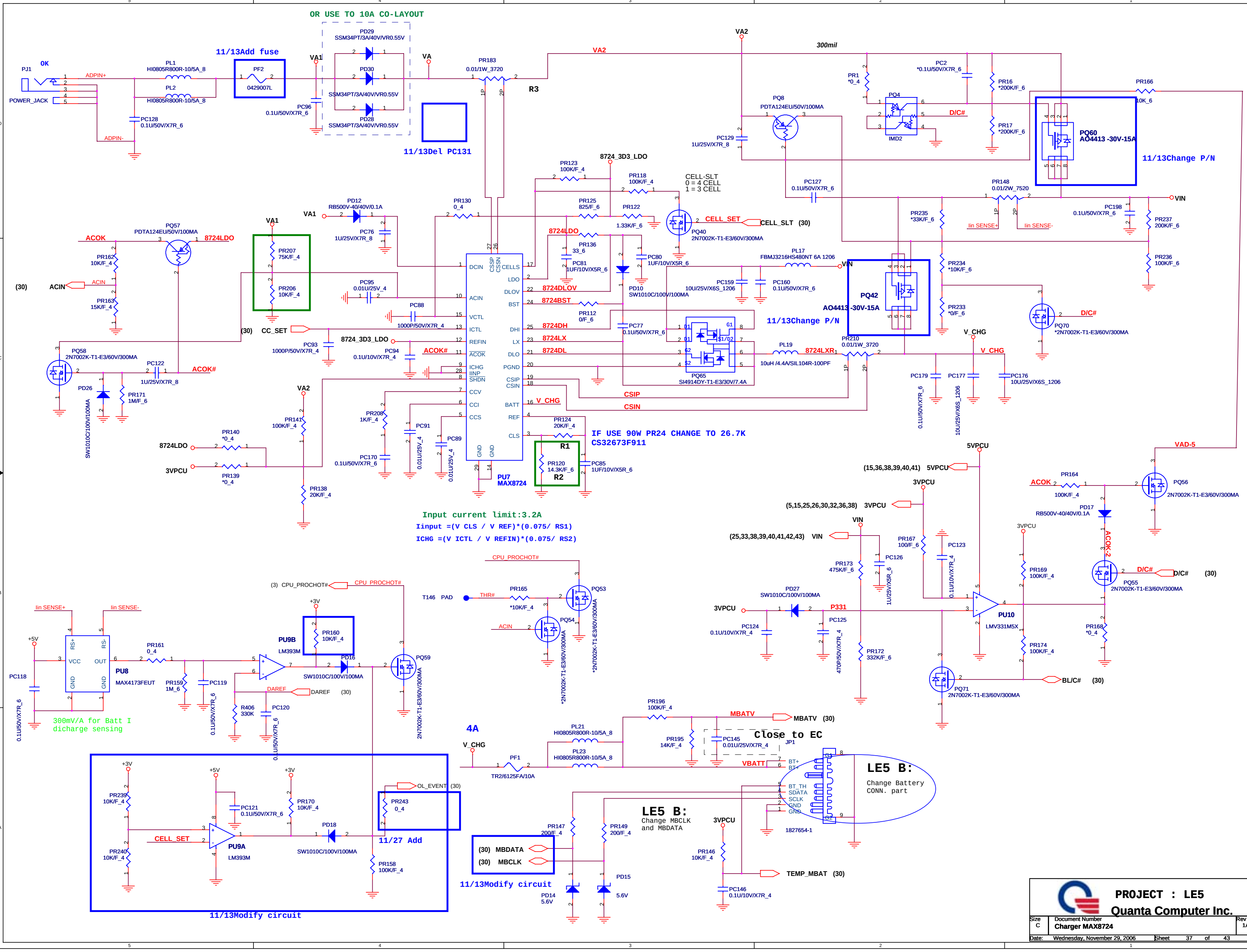
Size	Document Number	Rev
Custom	CPU THERMAL/HW PRODCT	1A

Date: Thursday, November 30, 2006 Sheet 35 of 43

DISCHARGE



MIANON
PQ25 PDTC144EU/50V/30MA
+15V
+5V
+3V
+2.5V
+1.8V
+1.25V
+VCC_GFX_CORE
+1.2V_GFX_PCIE
PR83 1M_6
PR88 22_8
PR93 22_8
PR96 22_8
PR98 22_8
PR99 22_8
PR103 22_8
PR110 22_8
PR114 1M_6
PQ27
PQ29
PQ31
PQ34
PQ35
PQ36
PQ37
PQ38
2N7002K-T1-E3/60V/300MA
MAINON#
PC78 2200P/50V/X7R_6
MAIND (41)
3VPCU
5VPCU
PQ50 AO4468
PQ48 AO4468
PC116 0.1U/10V/X7R_4
PC112 0.1U/10V/X7R_4
PC115 0.1U/10V/X7R_4
PC117 0.1U/10V/X7R_4
+3V
+5V
11/27 Change PARTS
11/13 Change P/N
PQ52 AO6402/30V/4.1A
PQ51 AO6402/30V/4.1A
3V_S5
5V_S5
PC46 10U/6.3V/X5R_8
PC48 0.1U/25V/X7R_6
PC49 *0.1U/25V/X7R_6
PC47 0.1U/10V/X7R_4
PR60 100K/F_4
PR54 100K/F_4
PQ23 RHU002N06T106/60V/200MA
PQ20 2N7002K-T1-E3/60V/300MA
PQ22 2N7002K-T1-E3/60V/300MA
PR57 22_8
PR59 22_8
(30) S5_ON
PQ18 RHU002N06T106/60V/200MA
+1.5V
SMDDR_VTERM
+1.05V
PR2 1M_6
PR13 22_8
PR14 22_8
PR15 22_8
PQ3 PDTC144EU/50V/30MA
PQ5
PQ6
PQ7
VCC_CORE
PR4 1M_6
PR3 22_8
(39,40,42) VRON
PQ1 PDTC144EU/50V/30MA
PQ2 2N7002K-T1-E3/60V/300MA
PQ47 AO6402/30V/4.1A
PC111 0.1U/10V/X7R_4
3VSUS
PC67 0.1U/10V/X7R_4
5VSUS
1.8VSUS
PR81 1M_6
SUSD
PR82 1M_6
PR91 22_8
PR86 22_8
PR95 22_8
(30,41) SUSON
PQ24 PDTC144EU/50V/30MA
PQ28
PQ26
PQ30
PQ33
PC71 *2200P/50V/X7R_4
PQ49 AO4468
PC43 0.1U/10V/X7R_4
PC70 0.1U/10V/X7R_4
PD31 SDM10K45-7-F/40V/0.1A
(27,30,38,39,40,41,43) MAINON
PR49 0_4
PC33 *0.1U/10V/X7R_4
PR48 *0_4
PR47 0/F_6
PL7 *HI0805R800R-10/5A_8
PL26 HI0805R800R-10/5A_8
Max Power Consumption 1.6W
PU3 AT815
GND0 VO EN VO VIN GND1 VIN GND2 ADJ
11/13 Change
PJP3 0_8
+2.5V
PC34 22U/6.3V/X5R_8
PC38 4.7U/10V/X5R_8
PC36 0.1U/10V/X7R_4
R1
PR52 10.2K/F_4
VTT-ADJ
PC35 0.1U/10V/X7R_4
PR51 10K/F_4
R2
PC44 *22U/6.3V/X5R_8
PC45 150U/4V/ESR35_3528
PC37 0.1U/10V/X7R_4
3/27 Change P/N
A1A:Change PU3 p/n CS33242FB19
Vout=1.24*[1+(R1/R2)]
LANVCC
PR56 1M_6
PR58 22_8
PR55 1M_6
LAN_ON
LAN_ON (26)
PQ19 PDTC144EU/50V/30MA
(30) LAN_POWER
PR53 1M_6
PQ21
PQ17
PC40 2200P/50V/X7R_6
PROJECT : LE5
Quanta Computer Inc.
Size C
Document Number
Dischange Circuit
Rev 1A
Date: Wednesday, November 29, 2006
Sheet 36 of 43


OR USE TO 10A CO-LAYOUT
11/13Add fuse
OK
PJ1
POWER_JACK
ADPIN+
ADPIN-
PL1
HI0805R800R-10/5A_8
PL2
HI0805R800R-10/5A_8
PF2
0429007L
PC128
0.1U/50V/X7R_6
PC96
0.1U/50V/X7R_6
VA1
VA
PD29
SSM34PT/3A/40V/VR0.55V
PD30
SSM34PT/3A/40V/VR0.55V
PD28
SSM34PT/3A/40V/VR0.55V
11/13Del PC131
PR183
0.01/1W_3720
R3
VA2
300mil
PR1
*0_4
PC2
*0.1U/50V/X7R_6
PR16
*200K/F_6
PR17
*200K/F_6
PQ4
IMD2
D/C#
PQ8
PDTA124EU/50V/100MA
PC129
1U/25V/X7R_8
PR166
10K_6
PQ60
AO4413 -30V-15A
11/13Change P/N
PR123
100K/F_4
8724_3D3_LDO
PR118
100K/F_4
CELL-SLT
0 = 4 CELL
1 = 3 CELL
PC127
0.1U/50V/X7R_6
PR148
0.01/2W_7520
VIN
PC198
0.1U/50V/X7R_6
PR237
200K/F_6
PD12
RB500V-40/40V/0.1A
PR130
0_4
PR125
825/F_6
PR122
1.33K/F_6
PQ40
2N7002K-T1-E3/60V/300MA
CELL_SET
CELL_SLT (30)
PR235
*33K/F_6
Iin SENSE+
Iin SENSE-
PQ57
PDTA124EU/50V/100MA
ACOK
8724LDO
PR162
10K/F_4
(30) ACIN
PR163
15K/F_4
PR207
75K/F_4
PR206
10K/F_4
PC76
1U/25V/X7R_8
PC95
0.01U/25V_4
PC88
1000P/50V/X7R_4
PR136
33_6
PC81
1UF/10V/X5R_6
PC80
1UF/10V/X5R_6
PD10
SW1010C/100V/100MA
PL17
FBMJ3216HS480NT 6A 1206
PC159
10U/25V/X6S_1206
PC160
0.1U/50V/X7R_6
PQ42
AO4413 -30V-15A
PR234
*10K/F_6
PR236
100K/F_6
DCIN
ACIN
VCTL
ICTL
REFIN
ACOK
ICHG
IINP
SHDN
CCV
CCI
CCS
CELLS
LDO
DLOV
BST
DHI
LX
DLO
PGND
CSIP
CSIN
BATT
REF
CLS
GND
8724DLOV
8724BST
8724DH
8724LX
8724DL
PR112
0/F_6
PC77
0.1U/50V/X7R_6
PQ65
SI4914DY-T1-E3/30V/7.4A
11/13Change P/N
PR233
*0/F_6
PQ70
*2N7002K-T1-E3/60V/300MA
V_CHG
PL19
10uH /4.4A/SIL104R-100PF
8724LXR
PR210
0.01/1W_3720
V_CHG
(30) CC_SET
PC93
1000P/50V/X7R_4
8724_3D3_LDO
PC94
0.1U/10V/X7R_4
ACOK#
PQ58
2N7002K-T1-E3/60V/300MA
PC122
1U/25V/X7R_8
ACOK#
PD26
SW1010C/100V/100MA
PR171
1M/F_6
VA2
PR141
100K/F_4
PR208
1K/F_4
PC91
0.01U/25V_4
PC89
0.01U/25V_4
V_CHG
CSIP
CSIN
PC179
0.1U/50V/X7R_6
PC177
10U/25V/X6S_1206
PC176
10U/25V/X6S_1206
8724LDO
PR140
*0_4
3VPCU
PR139
*0_4
PR138
20K/F_4
PC170
0.1U/50V/X7R_6
PU7
MAX8724
PR124
20K/F_4
R1
R2
PR120
14.3K/F_6
PC85
1UF/10V/X5R_6
IF USE 90W PR24 CHANGE TO 26.7K
CS32673F911
5VPCU
VAD-5
(15,36,38,39,40,41) 5VPCU
3VPCU
ACOK
PR164
100K/F_4
PQ56
2N7002K-T1-E3/60V/300MA
PD17
RB500V-40/40V/0.1A
ACOK-2
(5,15,25,26,30,32,36,38) 3VPCU
VIN
(25,33,38,39,40,41,42,43) VIN
PR167
100/F_6
PC123
0.1U/10V/X7R_4
PC126
1U/25V/X5R_6
PR173
475K/F_6
3VPCU
PR169
100K/F_4
PQ55
2N7002K-T1-E3/60V/300MA
D/C#
D/C# (30)
Input current limit:3.2A
Iinput =(V CLS / V REF)*(0.075/ RS1)
ICHG =(V ICTL / V REFIN)*(0.075/ RS2)
CPU_PROCHOT#
(3) CPU_PROCHOT#
T146 PAD
THR#
PR165
*10K/F_4
PQ53
*2N7002K-T1-E3/60V/300MA
ACIN
PQ54
*2N7002K-T1-E3/60V/300MA
3VPCU
PD27
SW1010C/100V/100MA
P331
PC124
0.1U/10V/X7R_4
PC125
470P/50V/X7R_4
PR172
332K/F_6
PU10
LMV331M5X
PR168
*0_4
PR174
100K/F_4
PQ71
2N7002K-T1-E3/60V/300MA
BL/C# (30)
Iin SENSE+
Iin SENSE-
+5V
PC118
0.1U/50V/X7R_6
PU8
MAX4173FEUT
PR161
0_4
PR159
1M_6
PC119
0.1U/50V/X7R_6
+3V
PR160
10K/F_4
PU9B
LM393M
PD16
SW1010C/100V/100MA
PQ59
2N7002K-T1-E3/60V/300MA
DAREF
DAREF (30)
R406
330K
PC120
0.1U/50V/X7R_6
300mV/A for Batt I
dicharge sensing
4A
V_CHG
PF1
TR2/6125FA/10A
PR196
100K/F_4
PL21
HI0805R800R-10/5A_8
PL23
HI0805R800R-10/5A_8
MBATV
MBATV (30)
PR195
14K/F_4
PC145
0.01U/25V/X7R_4
Close to EC
JP1
VBATT
BT+
BT+
BT_TH
SDATA
SCLK
GND
GND
1827654-1
LE5 B:
Change Battery
CONN. part
LE5 B:
Change MBCLK
and MBDATA
+3V
+5V
+3V
PR239
10K/F_4
PR240
10K/F_4
CELL_SET
PC121
0.1U/50V/X7R_6
PU9A
LM393M
PR170
10K/F_4
PD18
SW1010C/100V/100MA
OL_EVENT (30)
PR243
0_4
11/27 Add
PR158
100K/F_4
11/13Modify circuit
PR147
200/F_4
PR149
200/F_4
(30) MBDATA
(30) MBCLK
11/13Modify circuit
PD14
5.6V
PD15
5.6V
3VPCU
PR146
10K/F_4
TEMP_MBAT (30)
PC146
0.1U/10V/X7R_4
PROJECT : LE5
Quanta Computer Inc.
Size C
Document Number
Charger MAX8724
Rev 1A
Date: Wednesday, November 29, 2006
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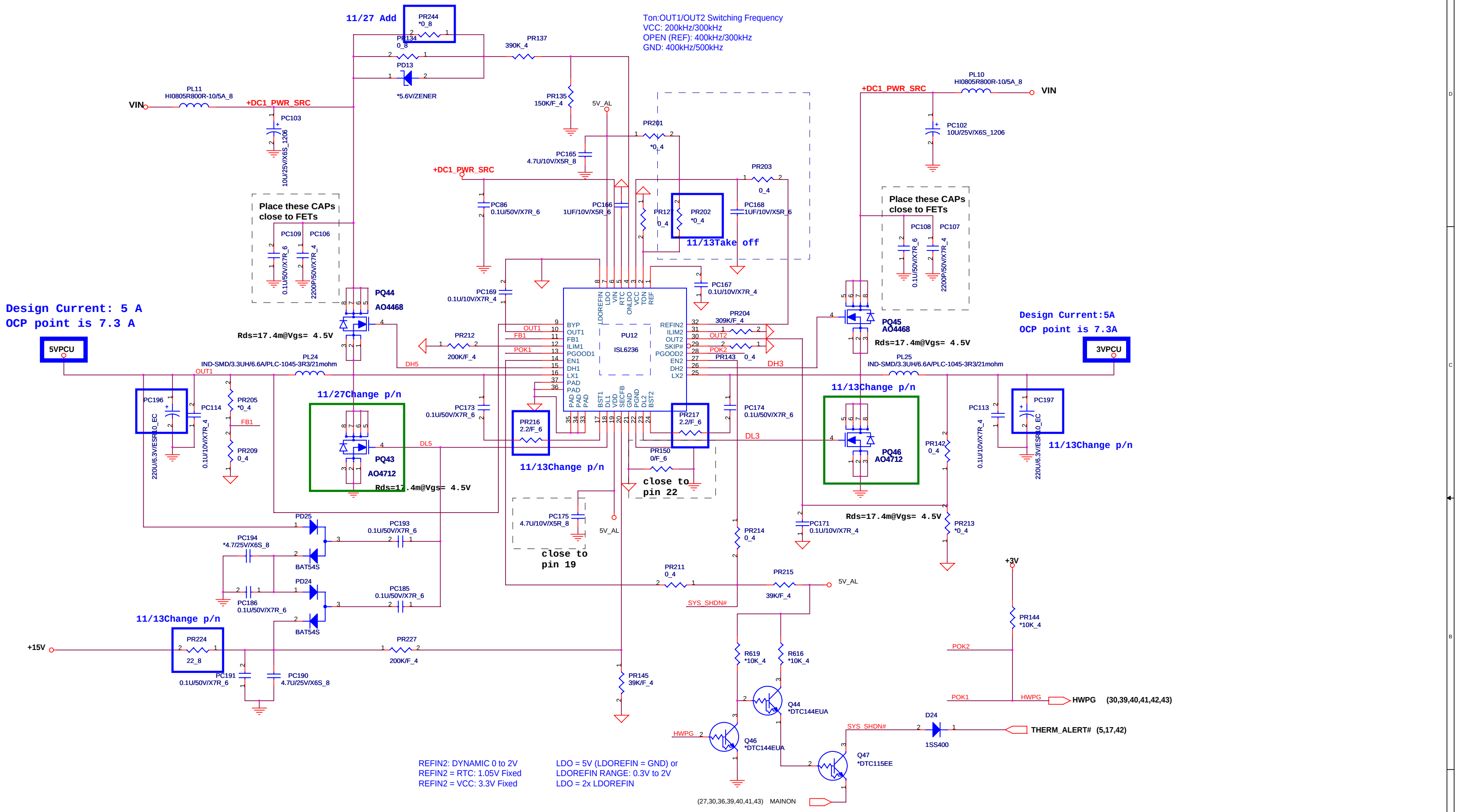
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

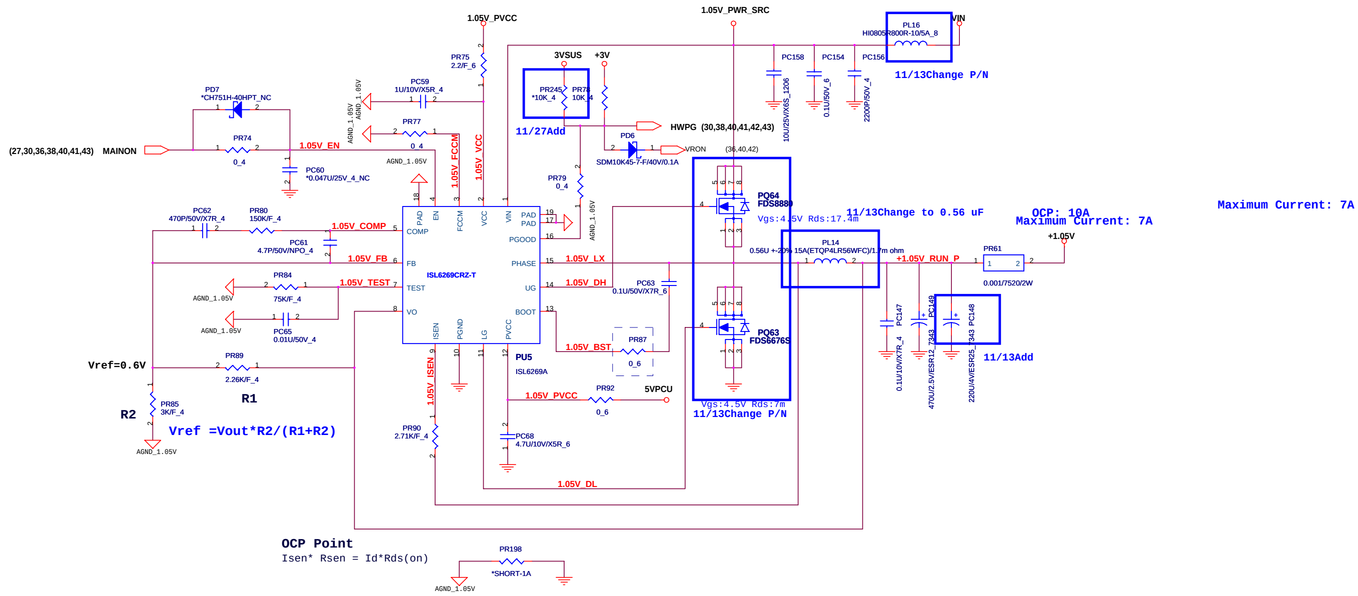


PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
C	D/D Power(ISL6263)	1A

Date: Wednesday, November 29, 2006 Sheet 38 of 43

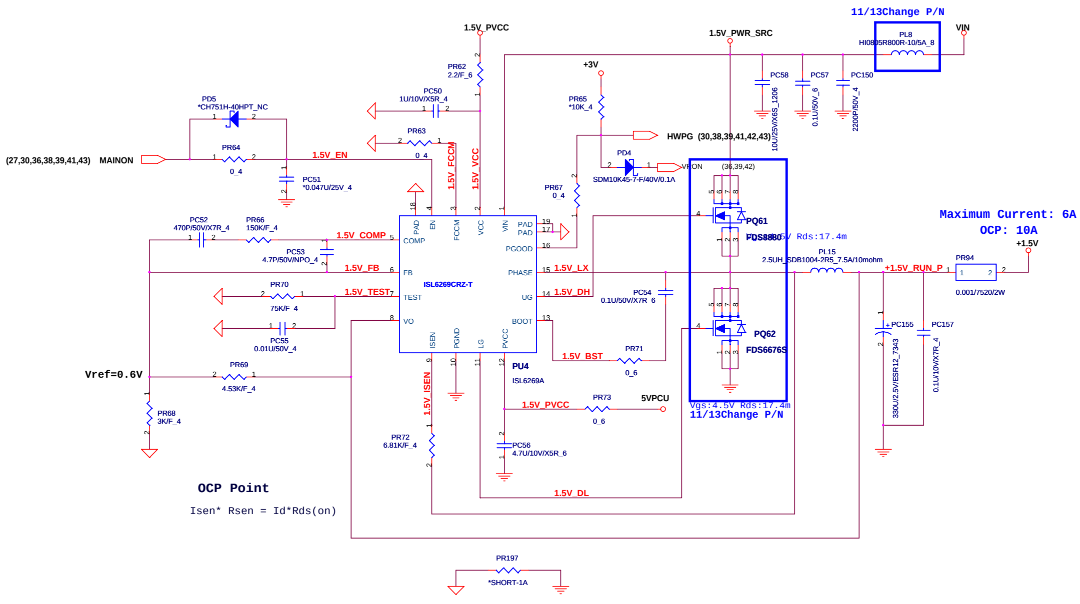


PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
C	1.05V(ISL6269A)	1A

Date: Wednesday, November 29, 2006 Sheet 39 of 43

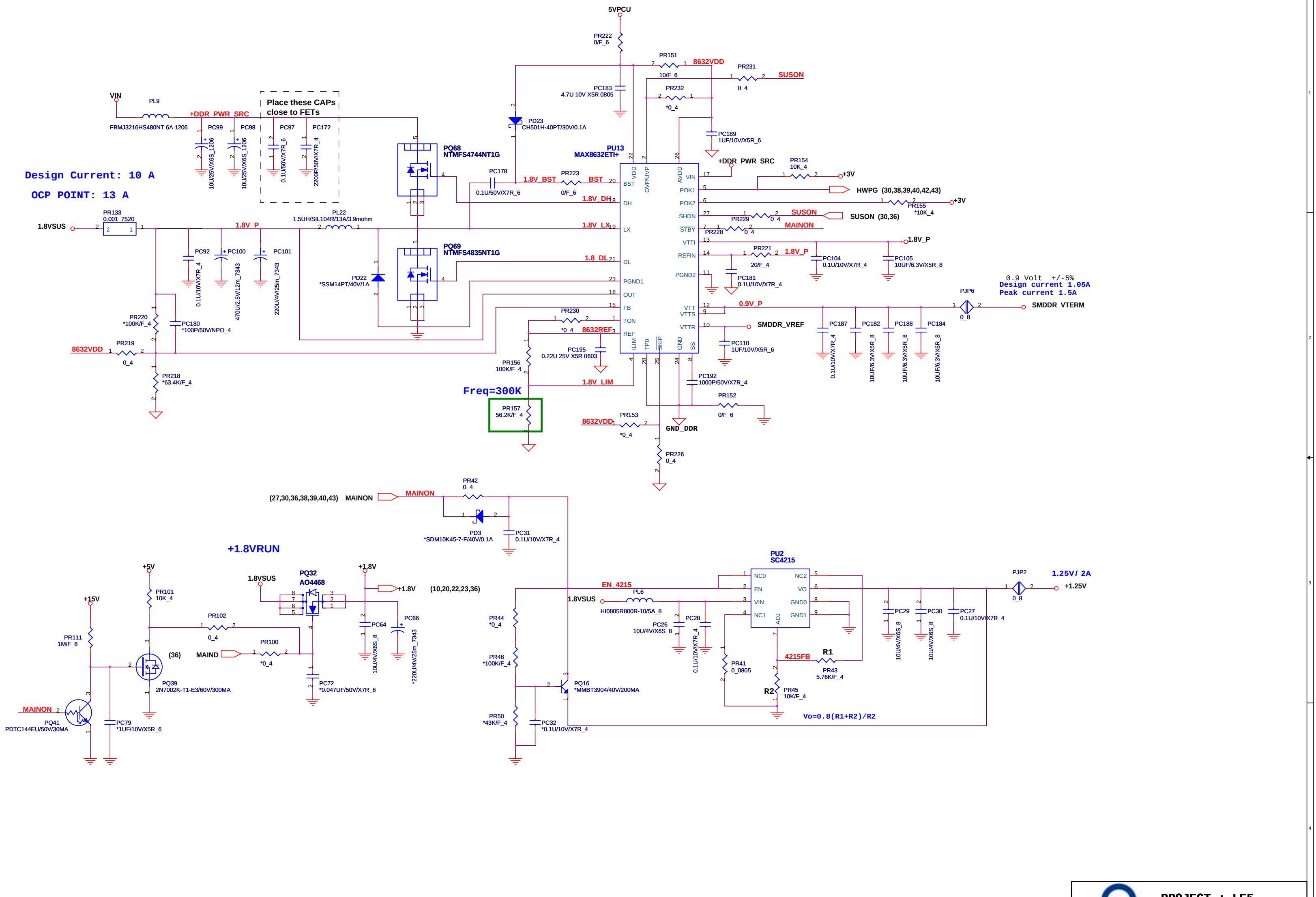


PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
C	1.5V(ISL6269A)	1A

Date: Wednesday, November 29, 2006 Sheet 40 of 43



PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
C	dDDR2 (MAX8632)	1A

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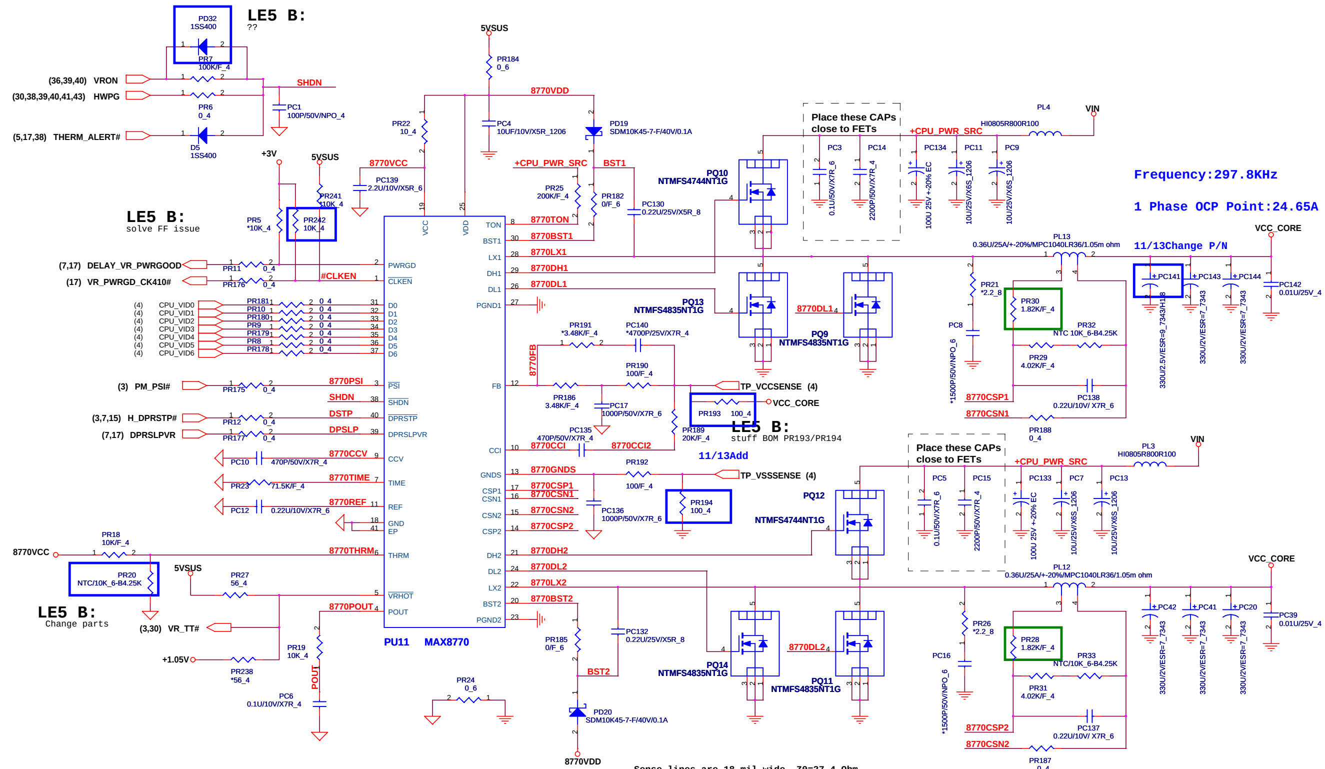

Add layout note on pins 22 and 28 of MAX8770 controller. These nets have large voltage swings. Need to route them away from the sensitive areas that are trying to detect small changes in voltage, such as the voltage sense VccSense VssSense lines.

Sense lines are 18 mil wide, Z0=27.4 Ohm.
Use differential routing with 7 mil spacing.
Route external layer with solid GND reference (no split planes).
Use 25 mil separation from any other signal.

distribute evenly between N side and S side, preferably on secondary side.

Use differential routing away from switch nodes 8770LX1 and 8770LX2

PROJECT : LE5		
Quanta Computer Inc.		
Size C	Document Number CPU Core (MAX8770)	Rev 1A
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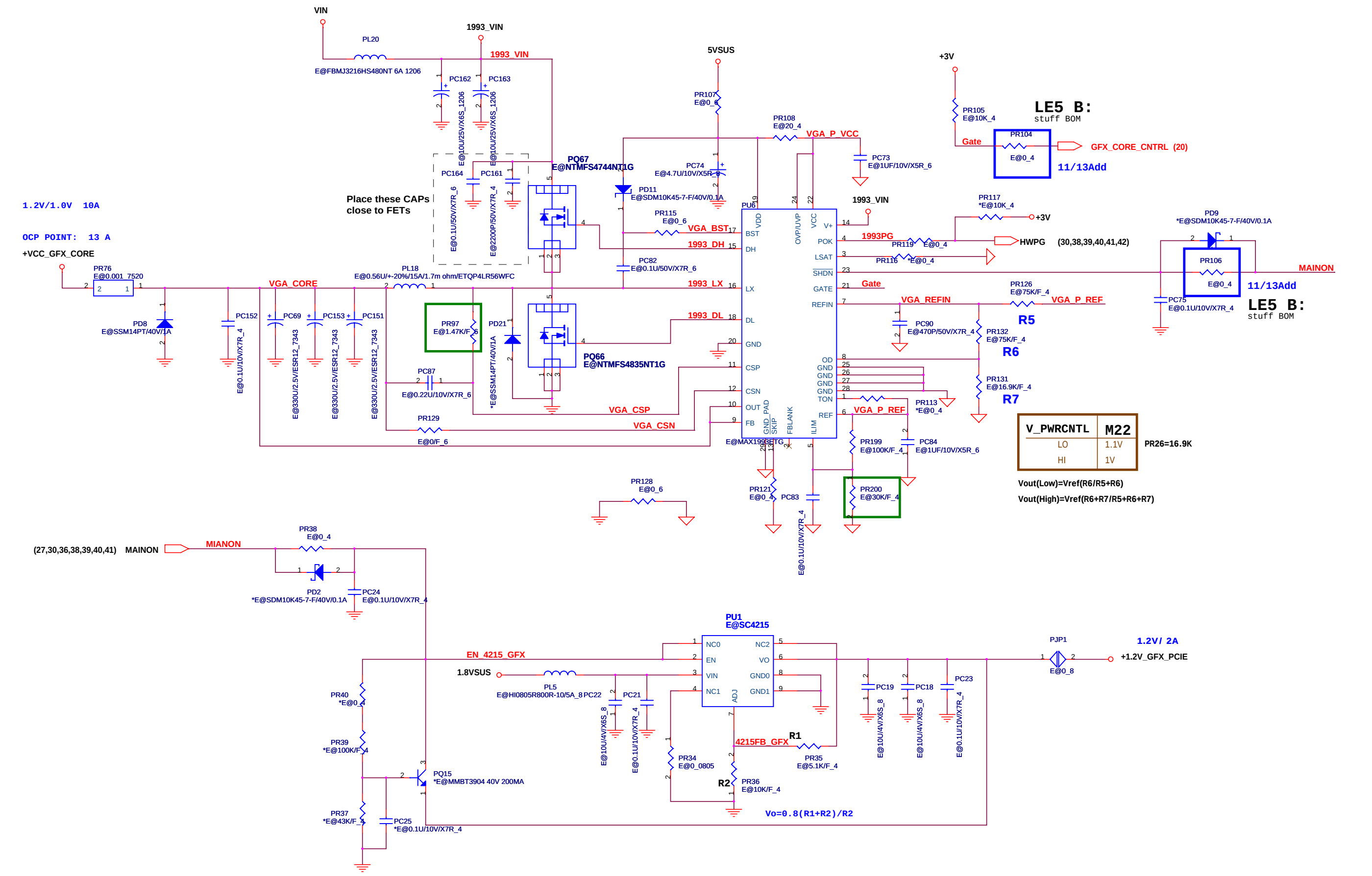

PROJECT : LE5

Quanta Computer Inc.

Size	Document Number	Rev
C	VGA (MAX1993)	1A

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