

# Bitland Confidential

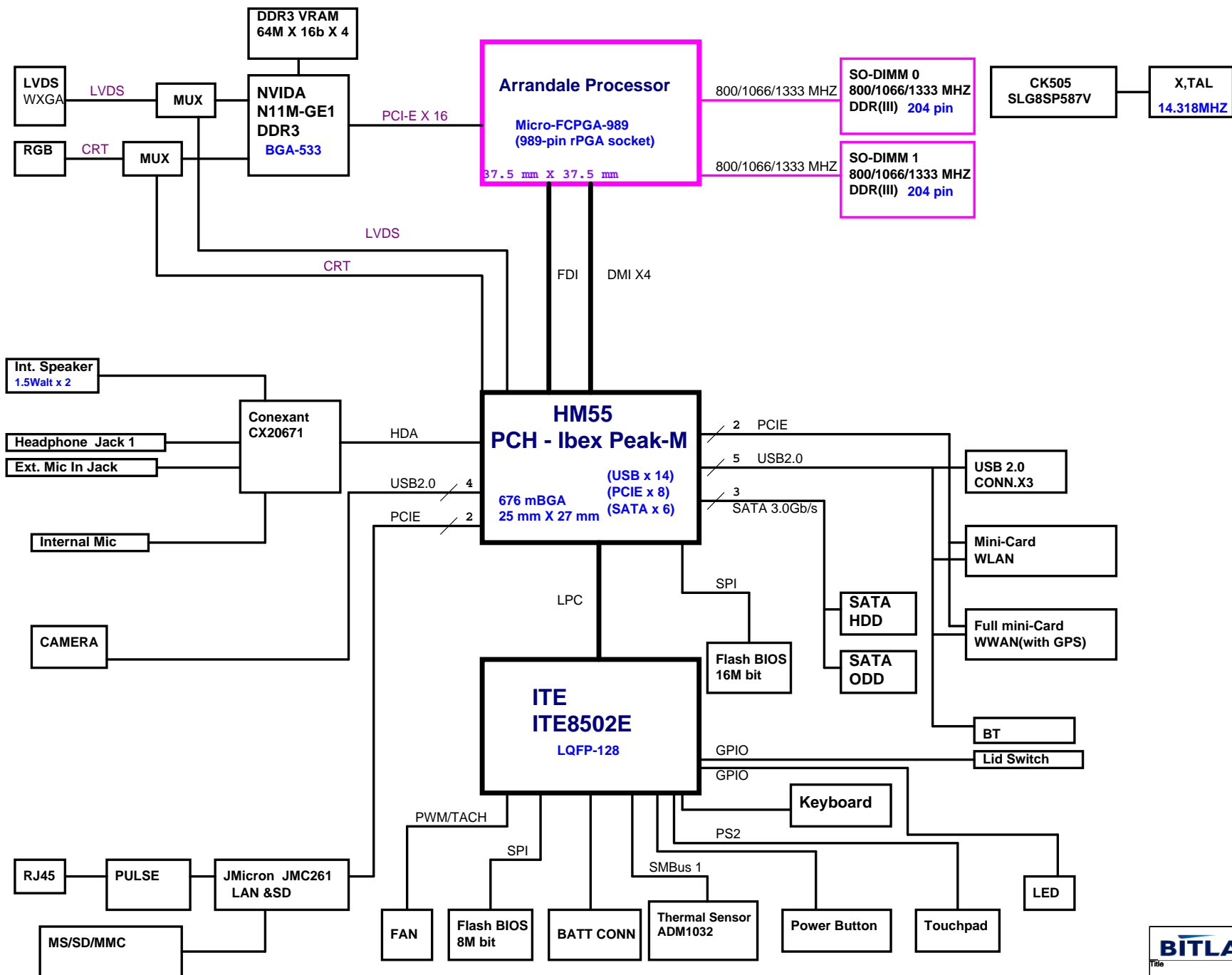
## BM5958 M/B Schematics Document

Intel Arrandale Processor with Ibexpeak(HM55) + DDRIII

2010-5-26

REV:1.3

<b>BITLAND</b>		Bitland Information Technology Co., Ltd. Notebook R&D Division
Title <b>Cover Page</b>		
Size A3	Document Number <b>BM5958</b>	Rev 1.0
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## Voltage Rails

Power Plane	Description	S1	S3	S5
DC_IN	Adapter power supply (19V)	N/A	N/A	N/A
DCBATOUT	AC or battery power rail for power circuit.	N/A	N/A	N/A
+V_CORE	Core voltage for CPU	ON	OFF	OFF
+0_75V	0_75VRUN LDO power rail for DDR terminator	ON	OFF	OFF
+1.05VRUN	1.05V switched power rail	ON	OFF	OFF
+5VRUN	5V switched power rail	ON	OFF	OFF
+1_5VSUS	1.5V power rail for DDR	ON	ON	OFF
+1.5VRUN	1.5V switched power rail	ON	OFF	OFF
+1.8VRUN	1.8V power rail for system	ON	OFF	OFF
+1.5V_CPU	1.5V switched power rail	ON	OFF	OFF
+1.1VTT	VTT switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VSUS	3.3V power rail for SB	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF
+3VRUN	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VSUS	5V switched power rail	ON	ON	OFF
PEX_VDD	PEX LDO power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON
NV_VDD	Core voltage for GPU	ON	OFF	OFF

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
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## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADT7421	1001 100X b
MEDIA CONSOLE	1010 000X b	NB9M THERMAL SENSOR	

## HM55 SM Bus address

Device	Address
Clock Generator (SLG8SP587V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

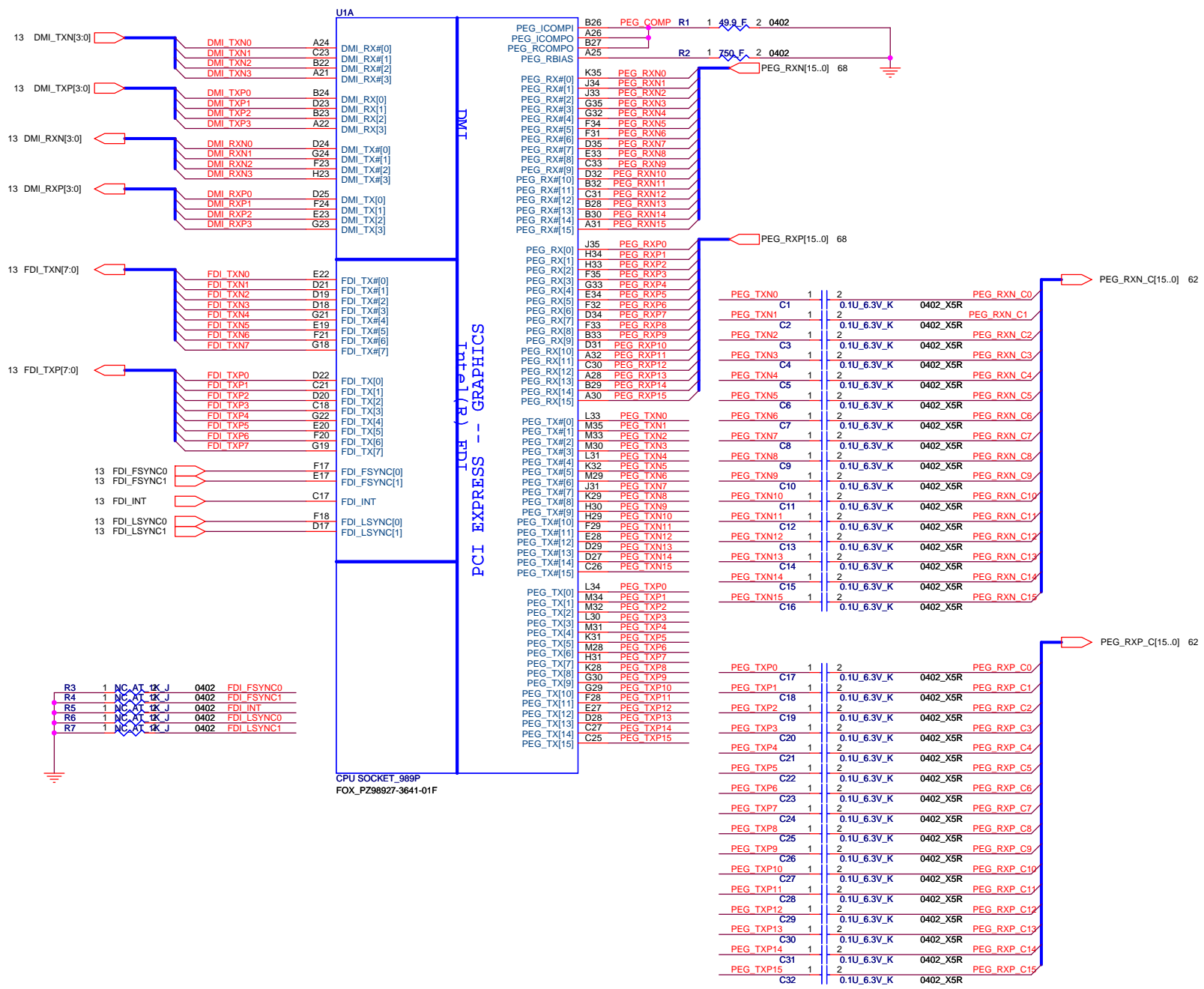
STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+SUS	+RUN	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

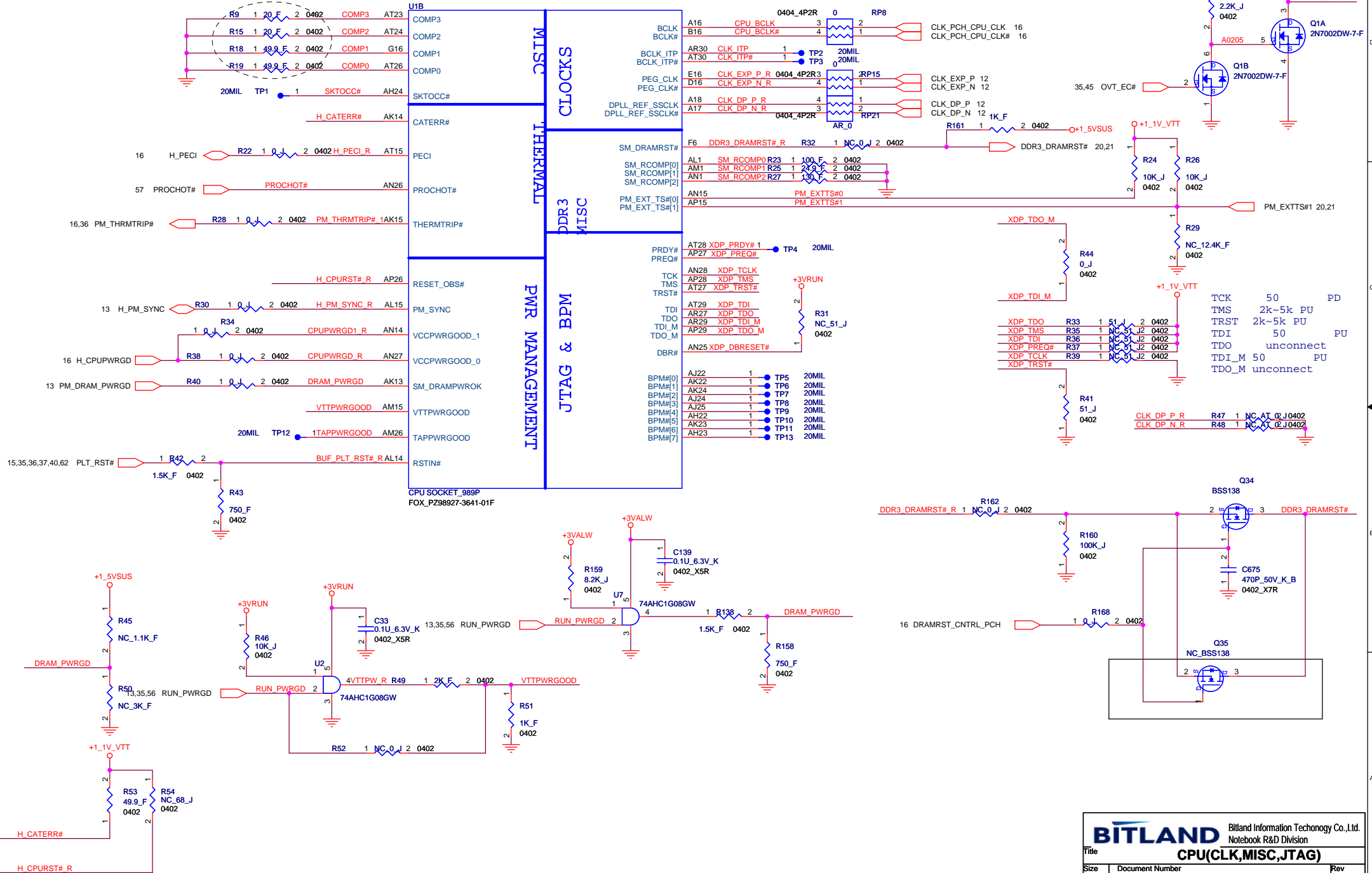
## BOARD ID Table

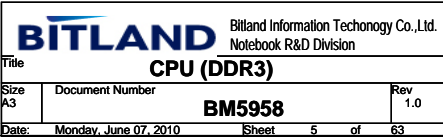
Board ID	PCB Revision
0	0.1
1	1.0
2	1.1
3	1.2
4	1.3
5	
6	
7	

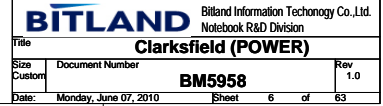


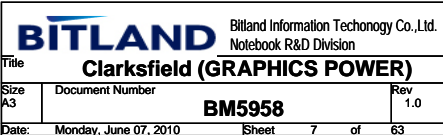
Layout Note:  
Comp0,2 connect with Zo=27.4 ohm, make trace  
length shorter then 0.5". Width=20mil(MS)  
Comp1,3 connect with Zo=55 ohm, make trace  
length shorter then 0.5". Width=5mil(MS)

Place close to chip

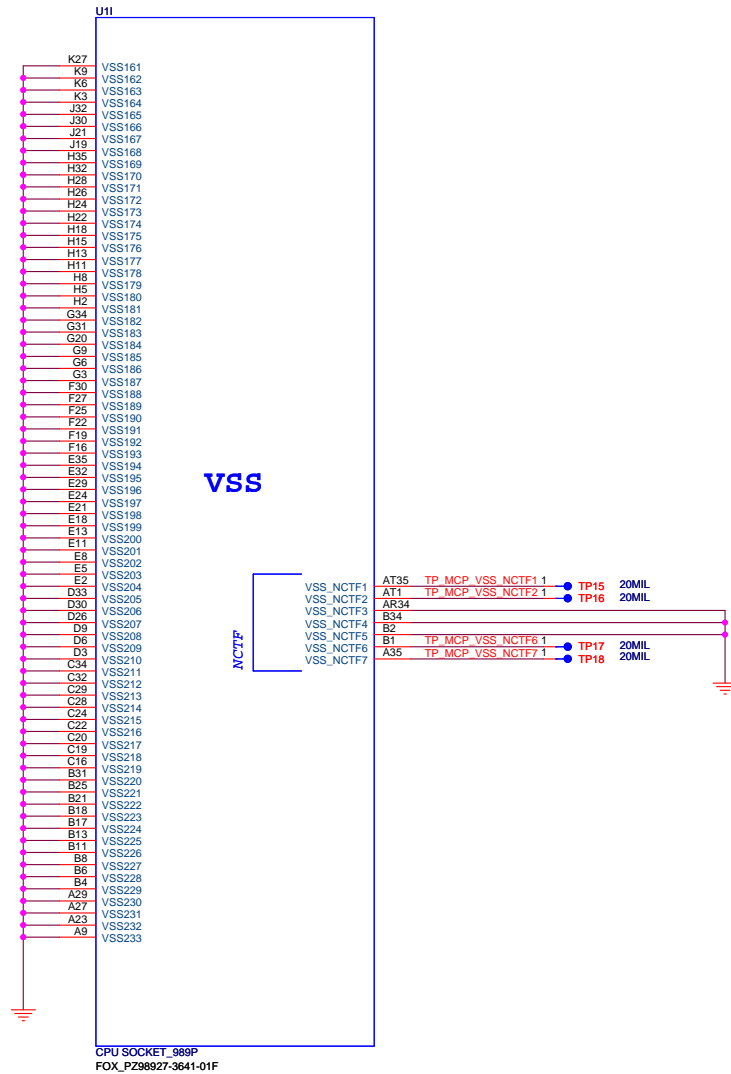
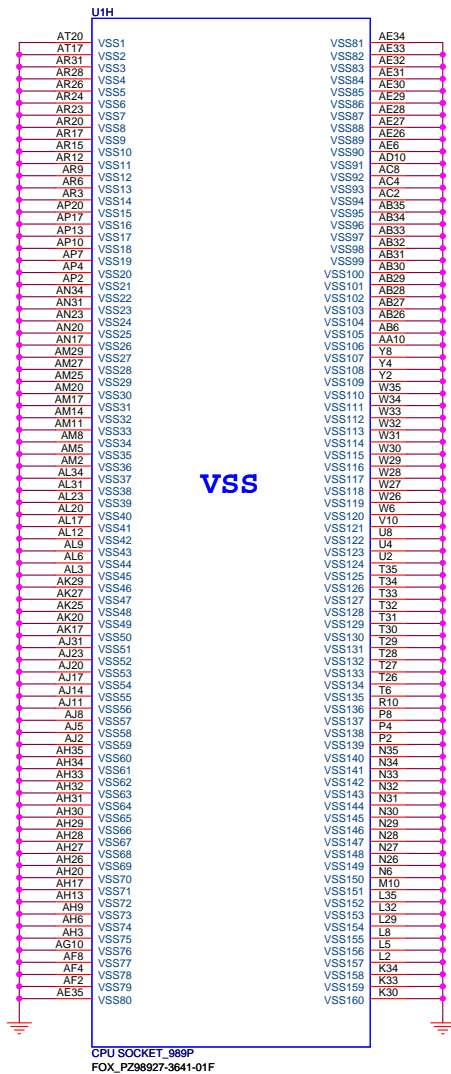




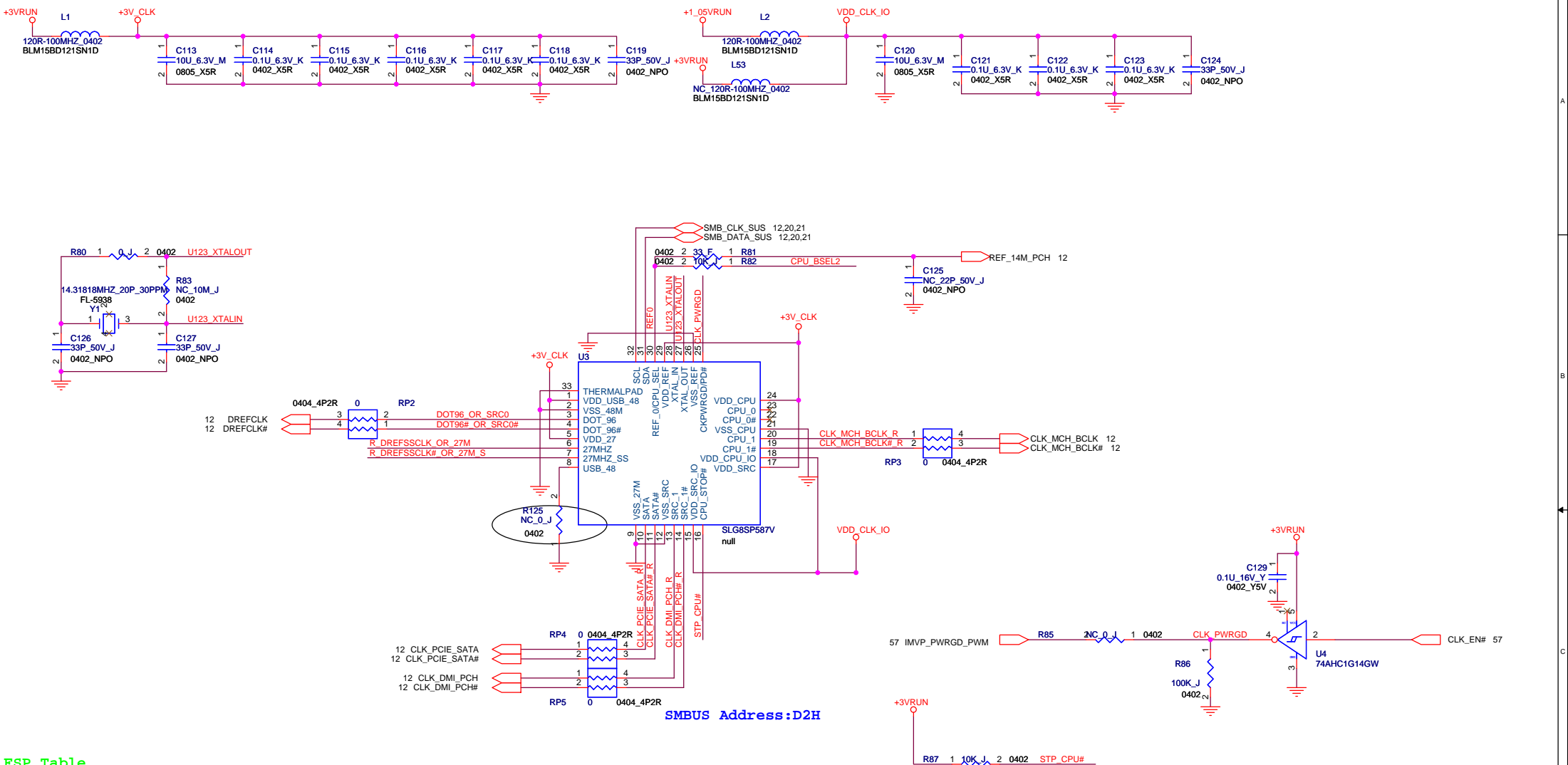












FSP Table

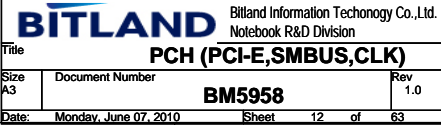
FS	CPU	Power On	SRC	SATA	DOT96	27MHz	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						

CPU\_BSEL2

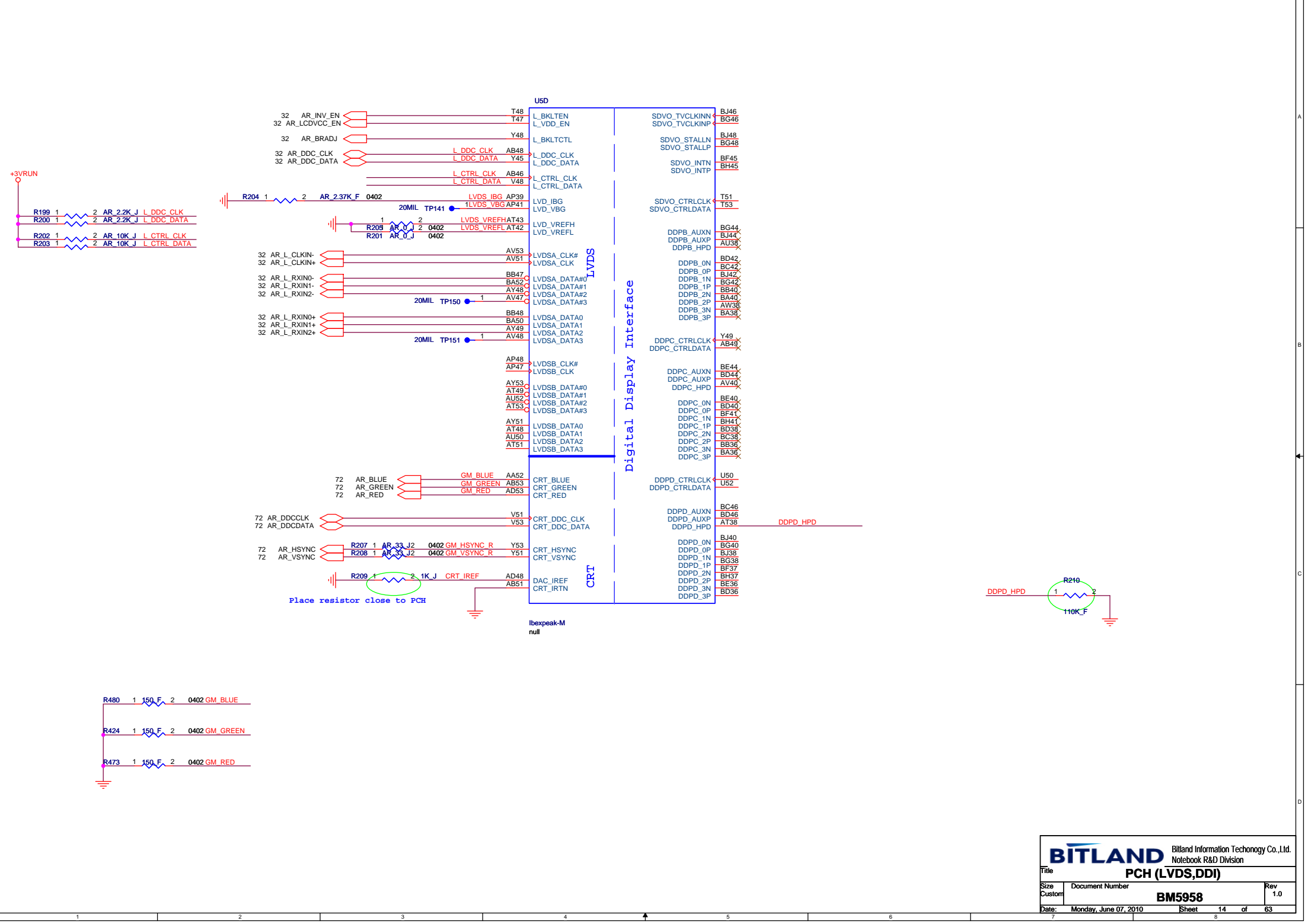
H:100 MHz  
L:133 MHz

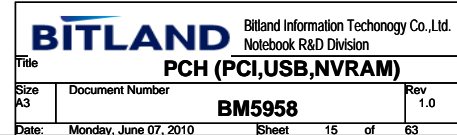


Port	Function
Port1	LAN
Port2	Express Card
Port3	WLAN
Port4	Un-used
Port5	Un-used
Port6	Un-used
Port7	Un-used
Port8	Un-used



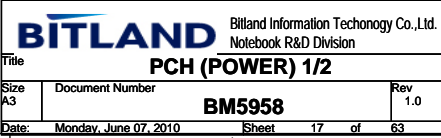




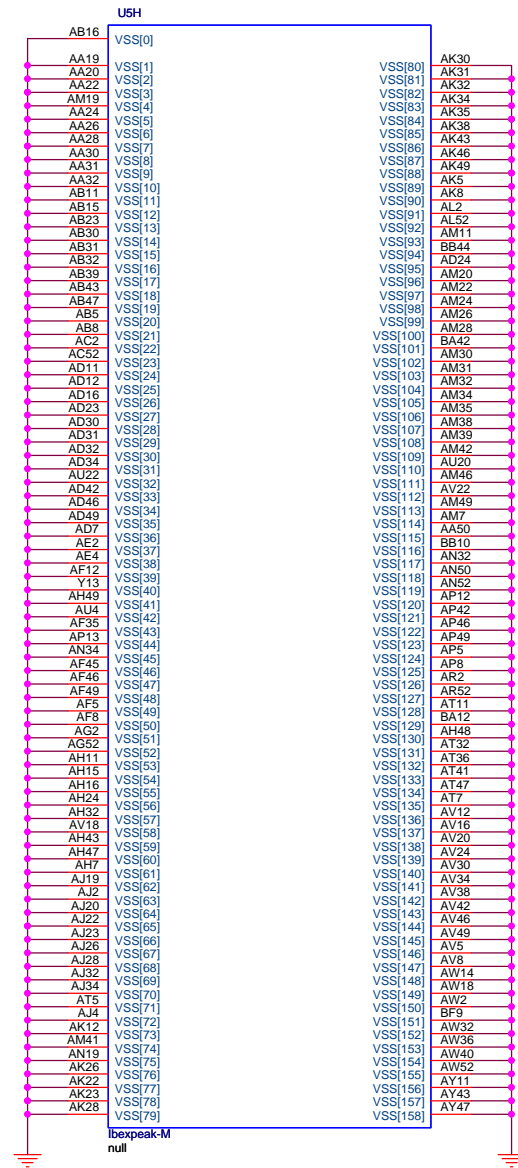
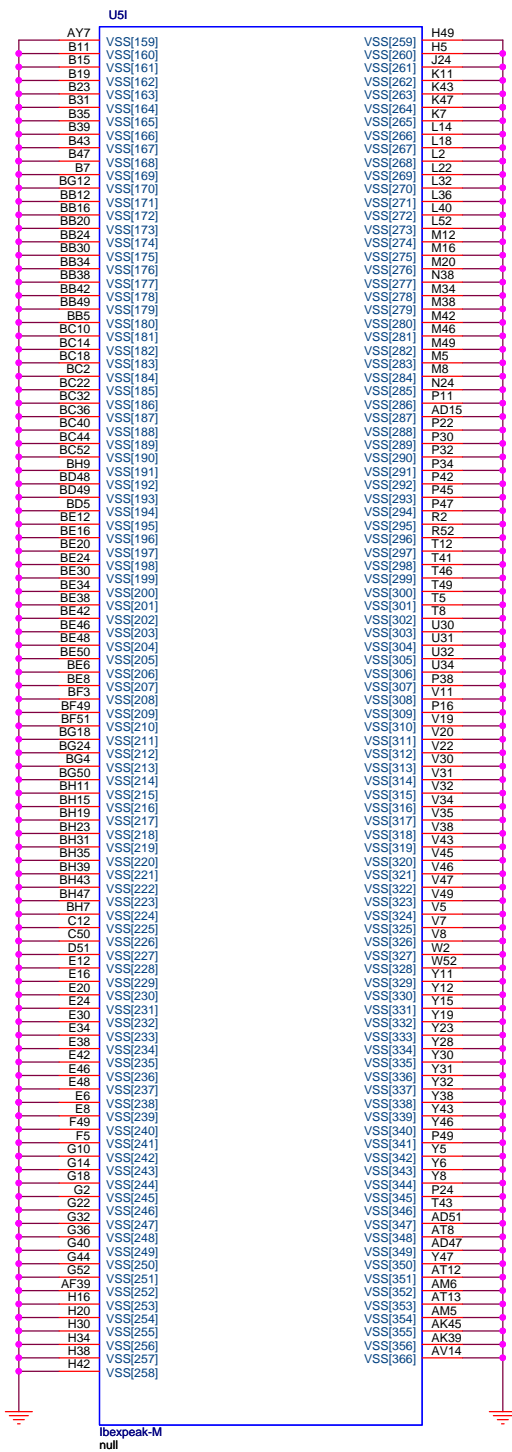


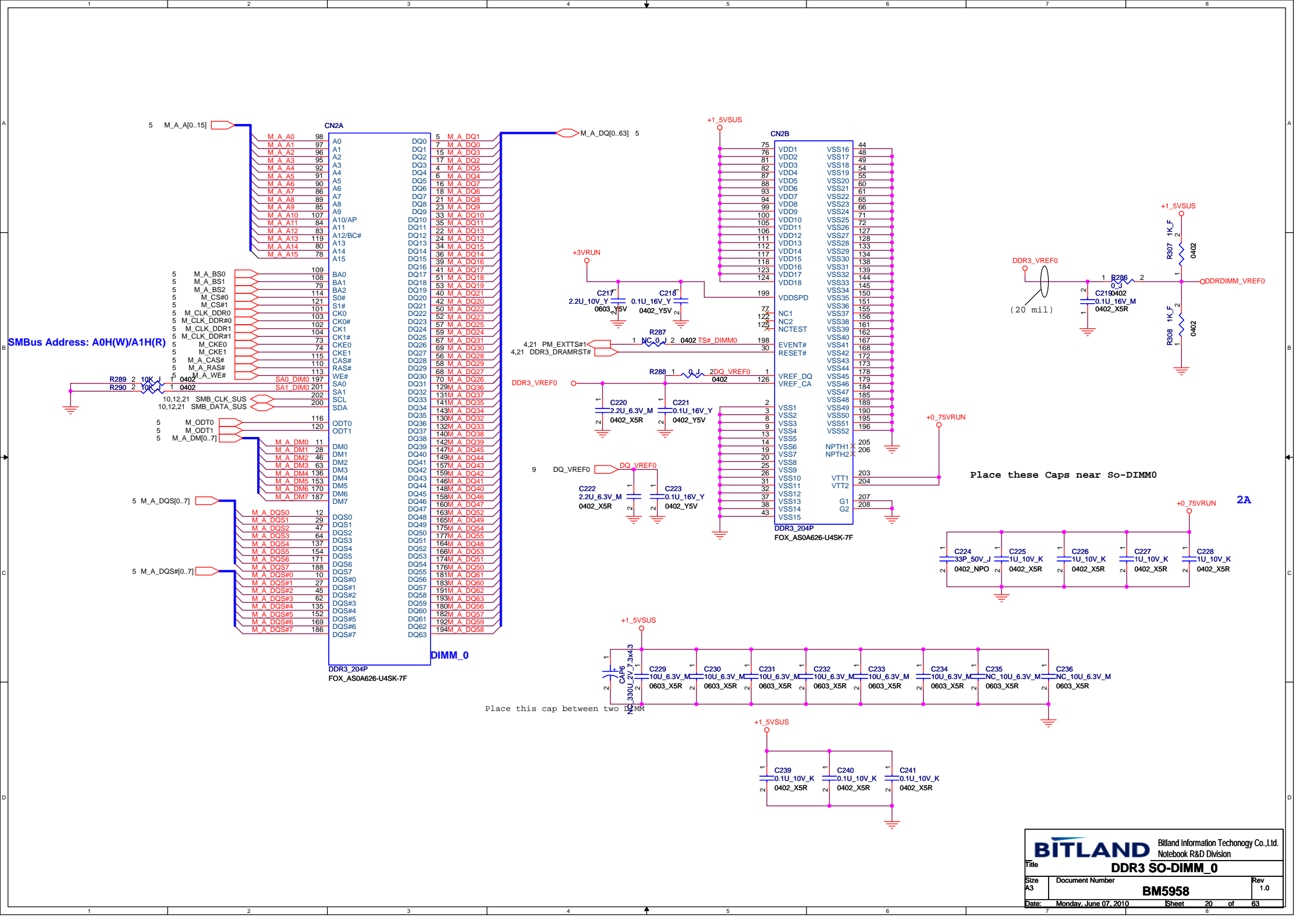


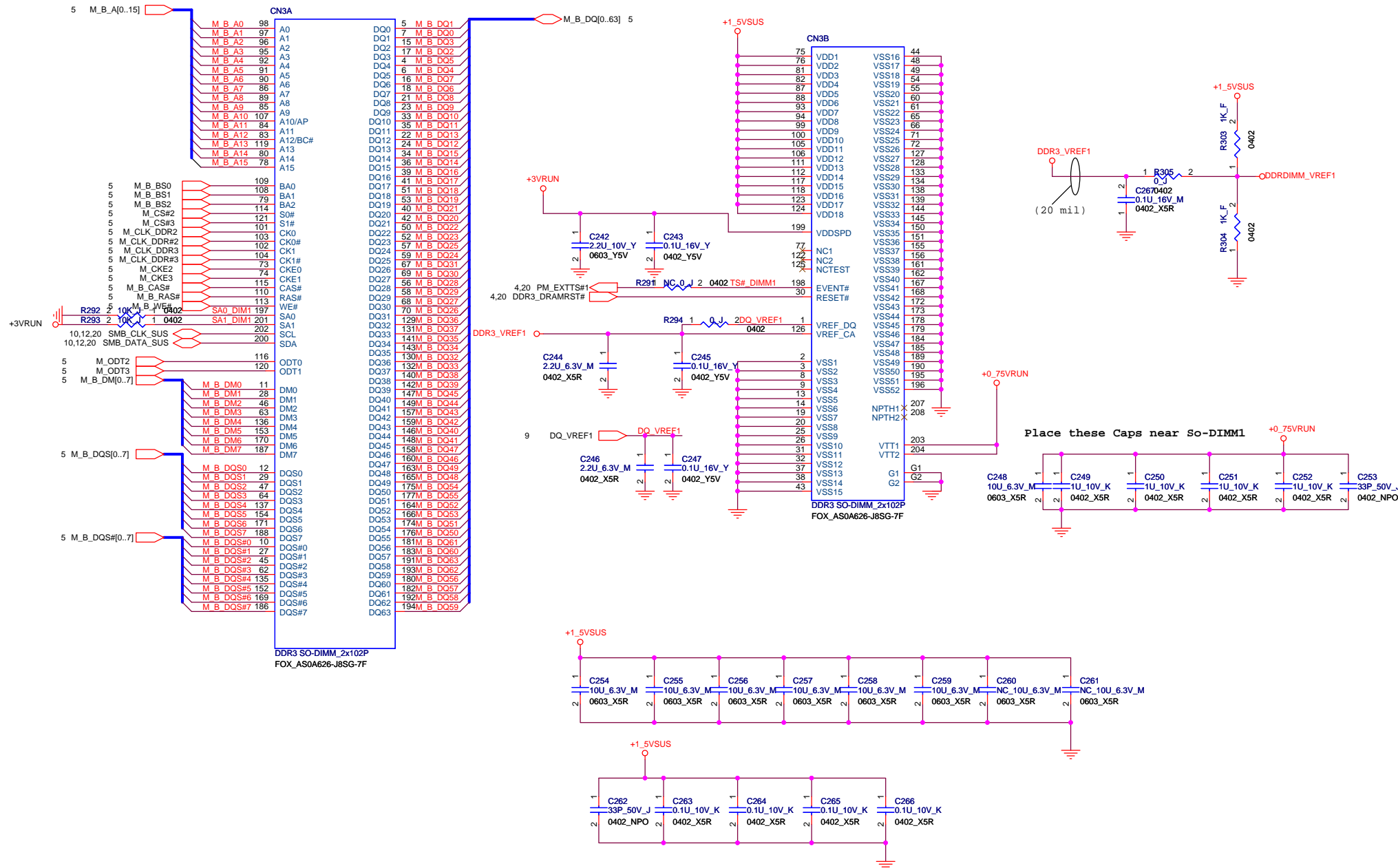


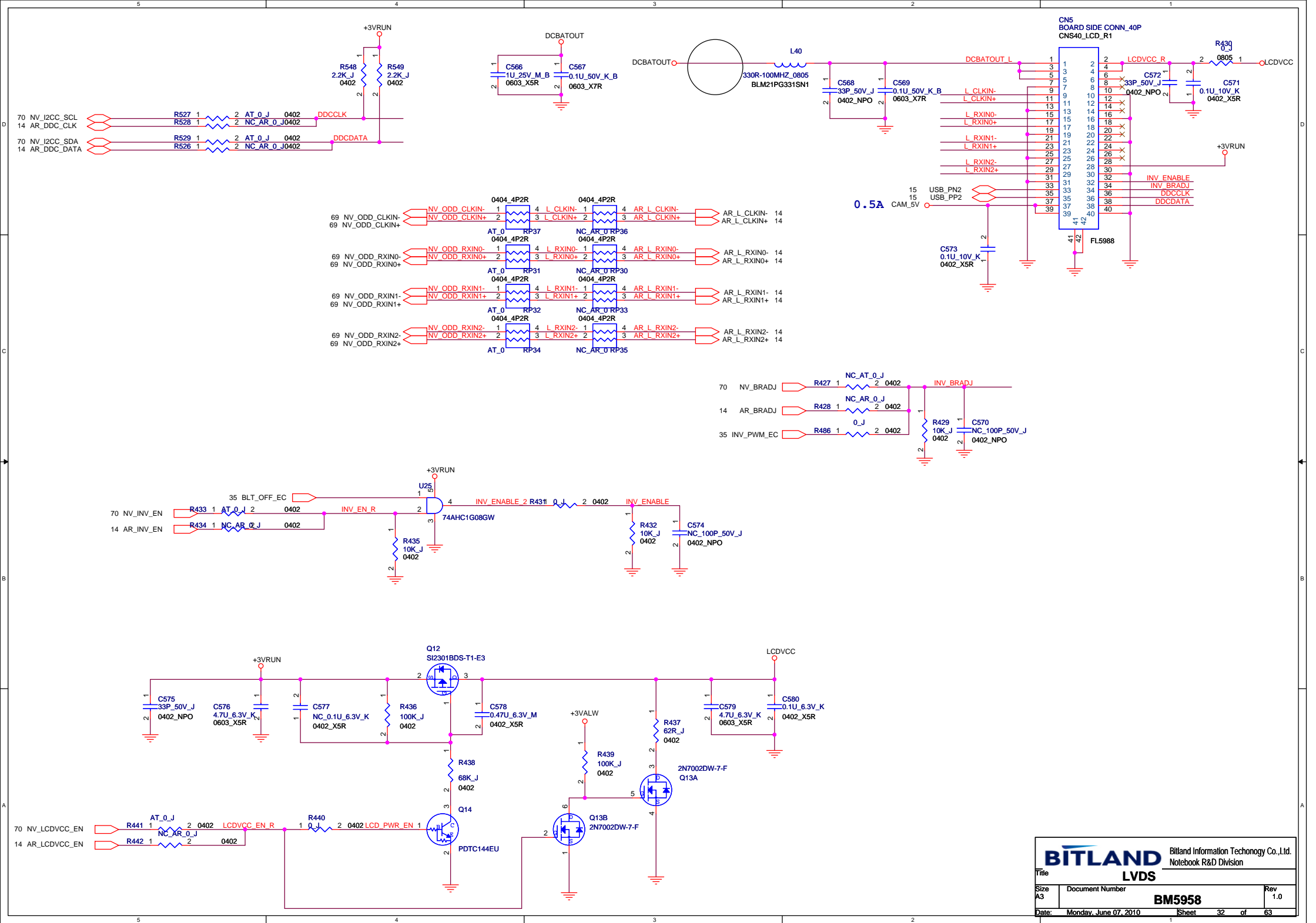










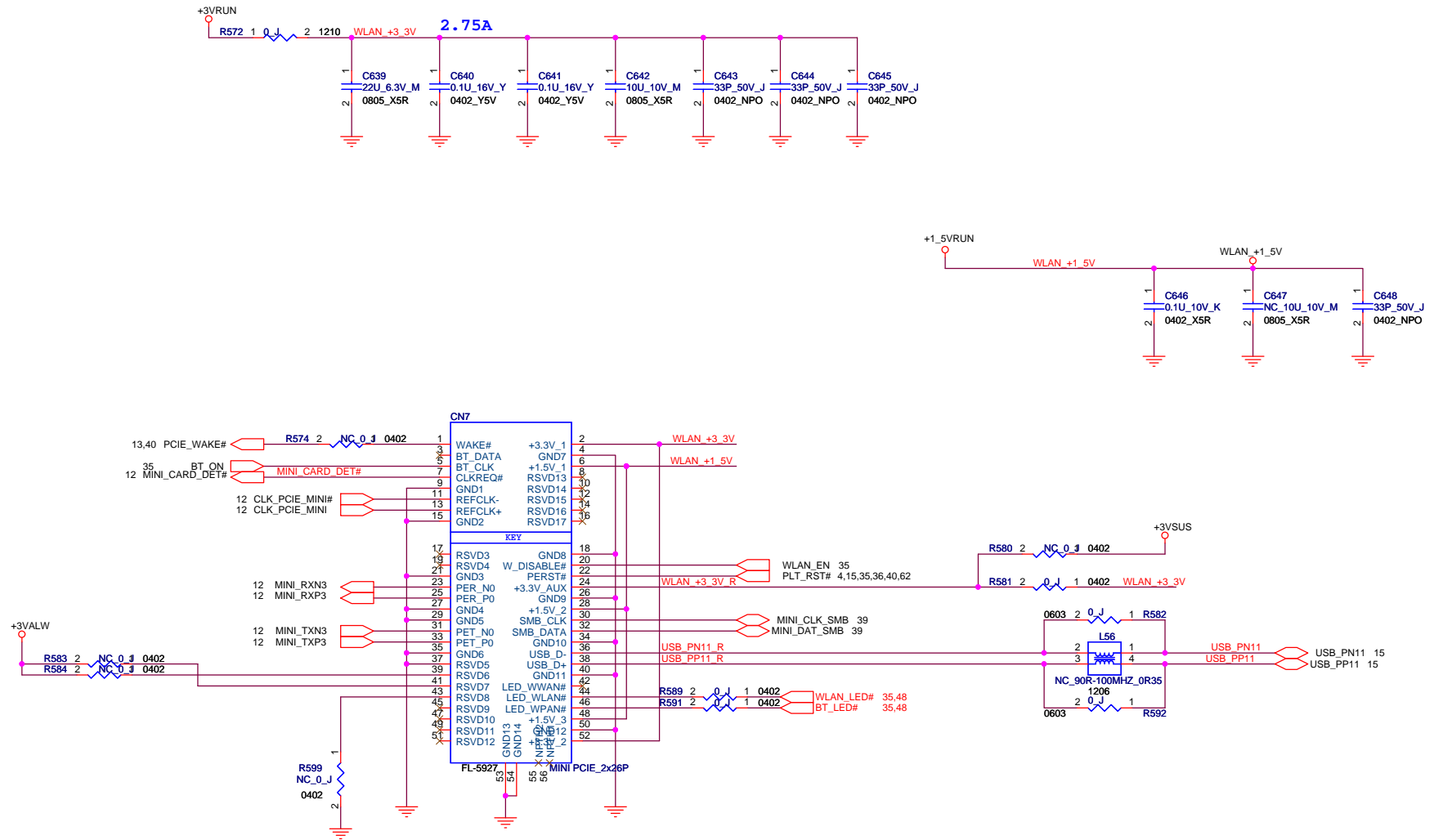
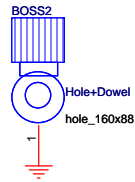




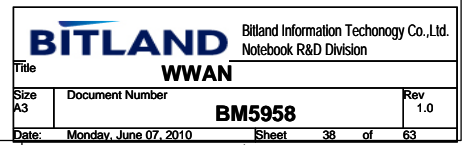




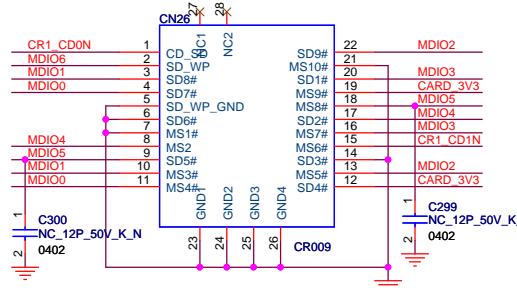
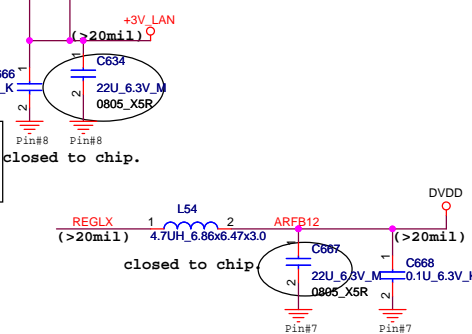
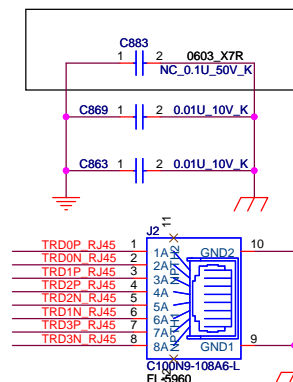
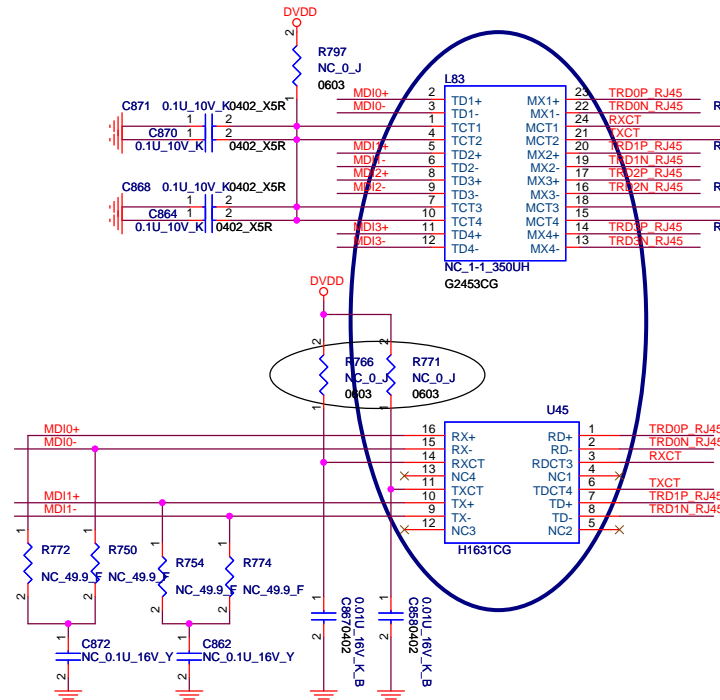
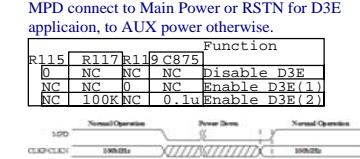
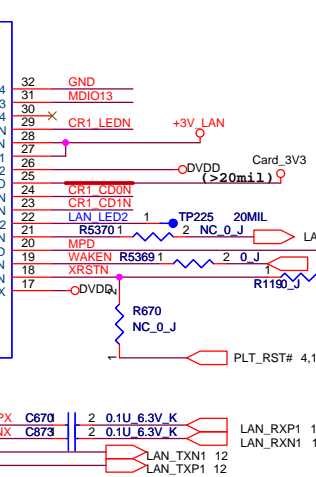
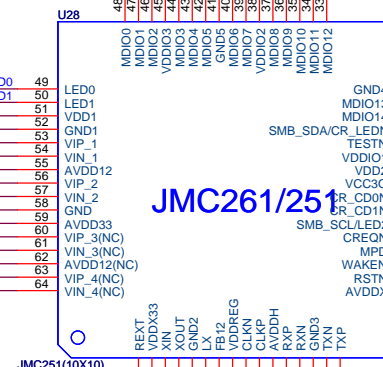
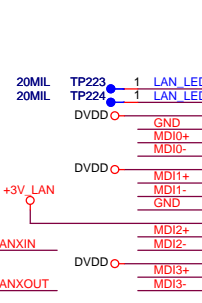
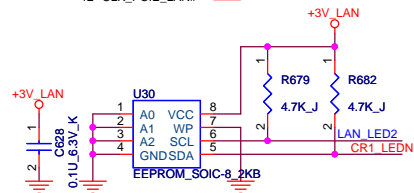


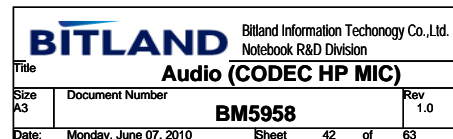


Pin30, 32, 36, 38 is Reserved in Kedron pin-out definition

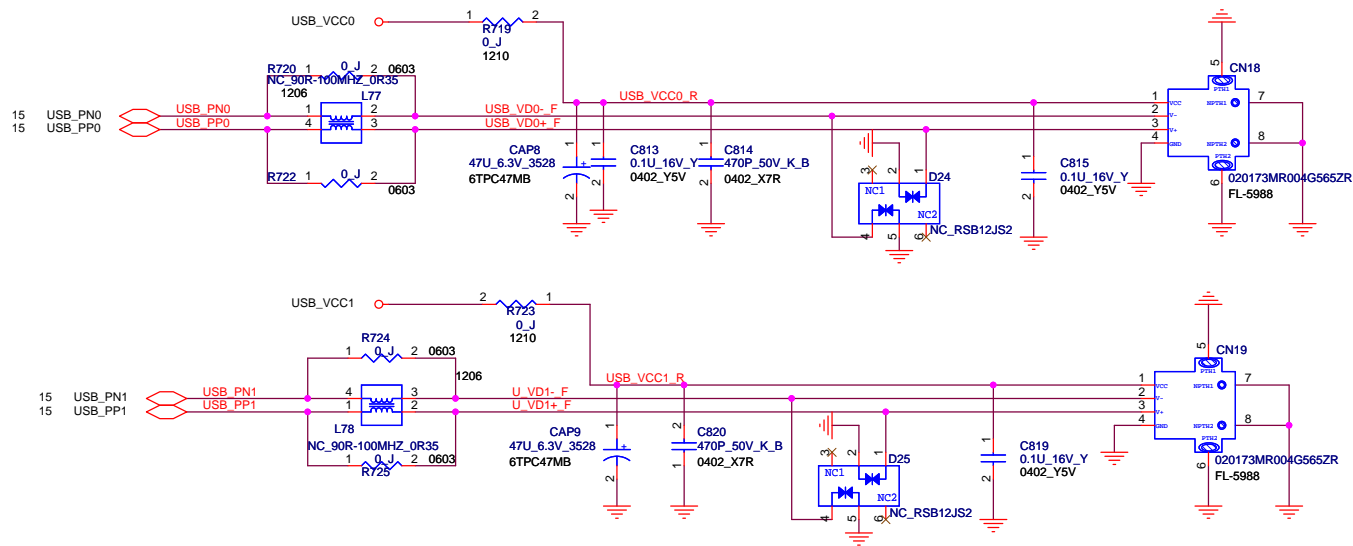
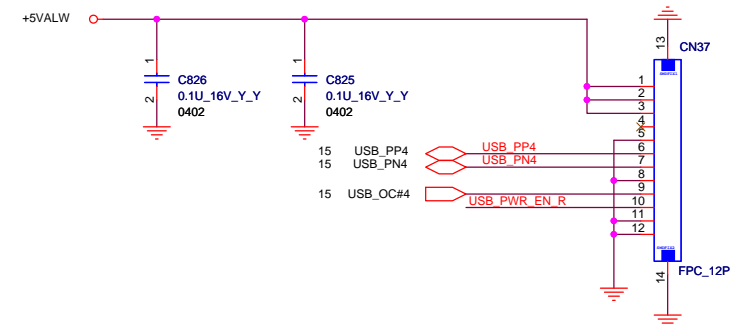
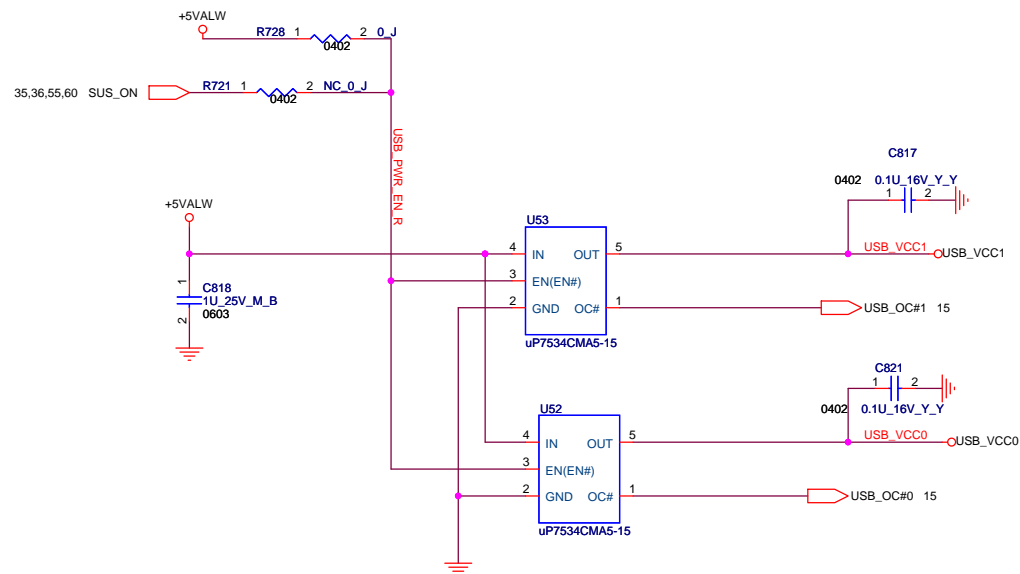




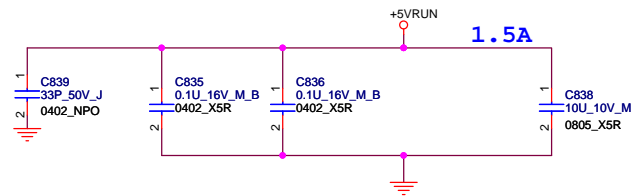




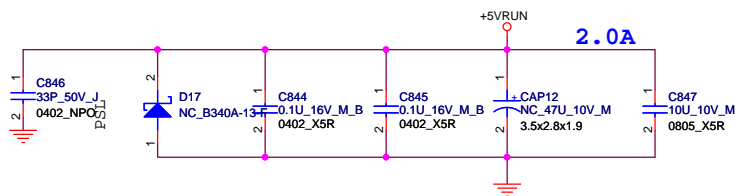
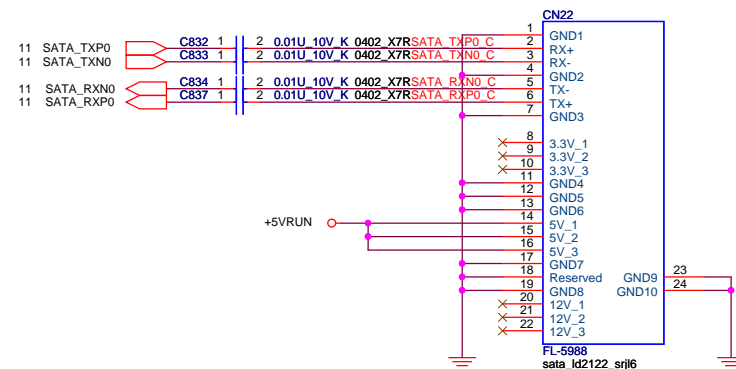




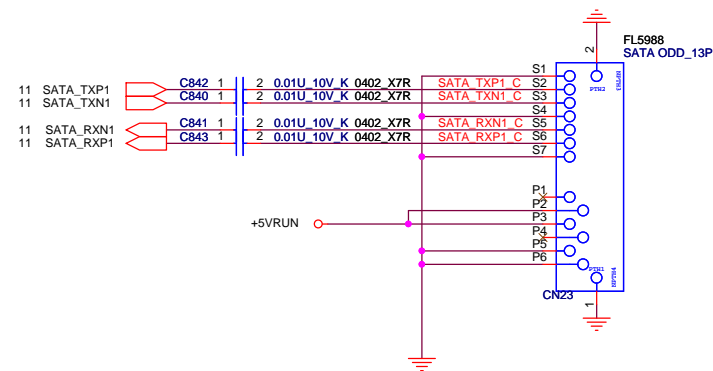


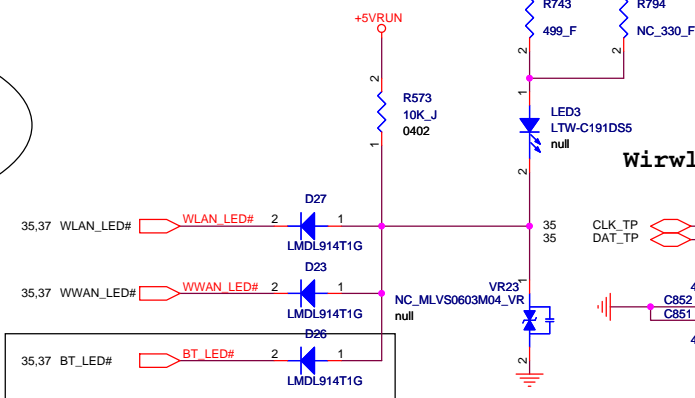
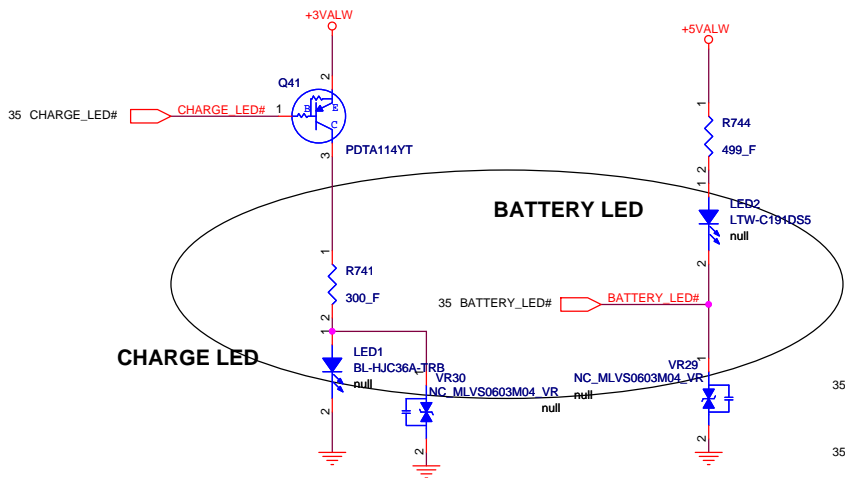


## SATA HDD CONN

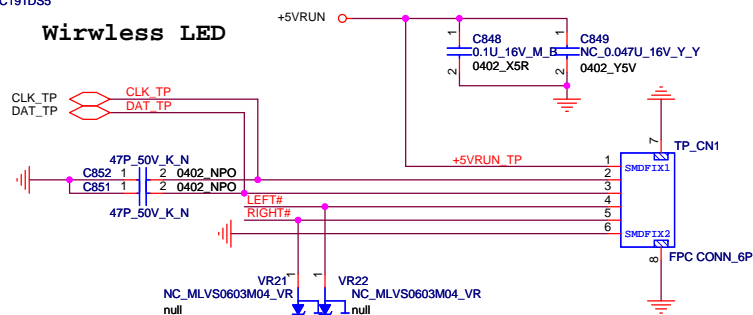


## SATA ODD CONN

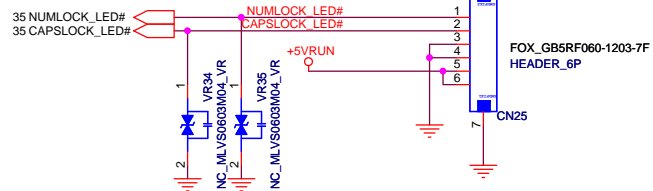
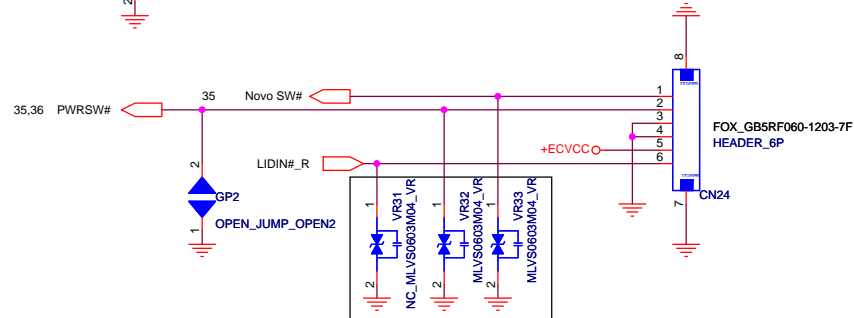
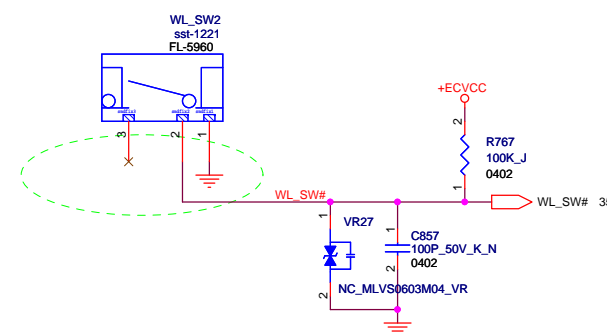
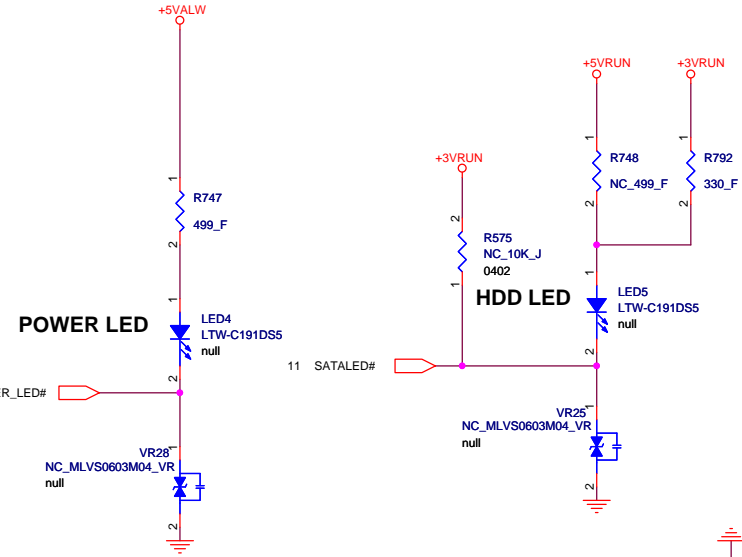
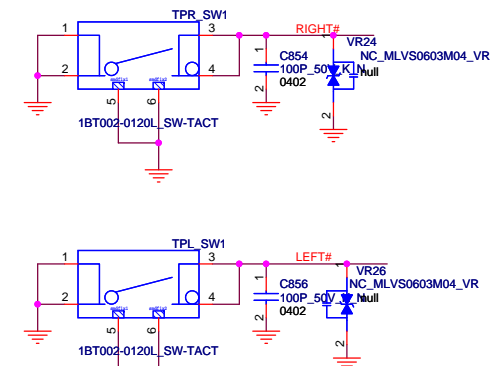




### Wireless LED

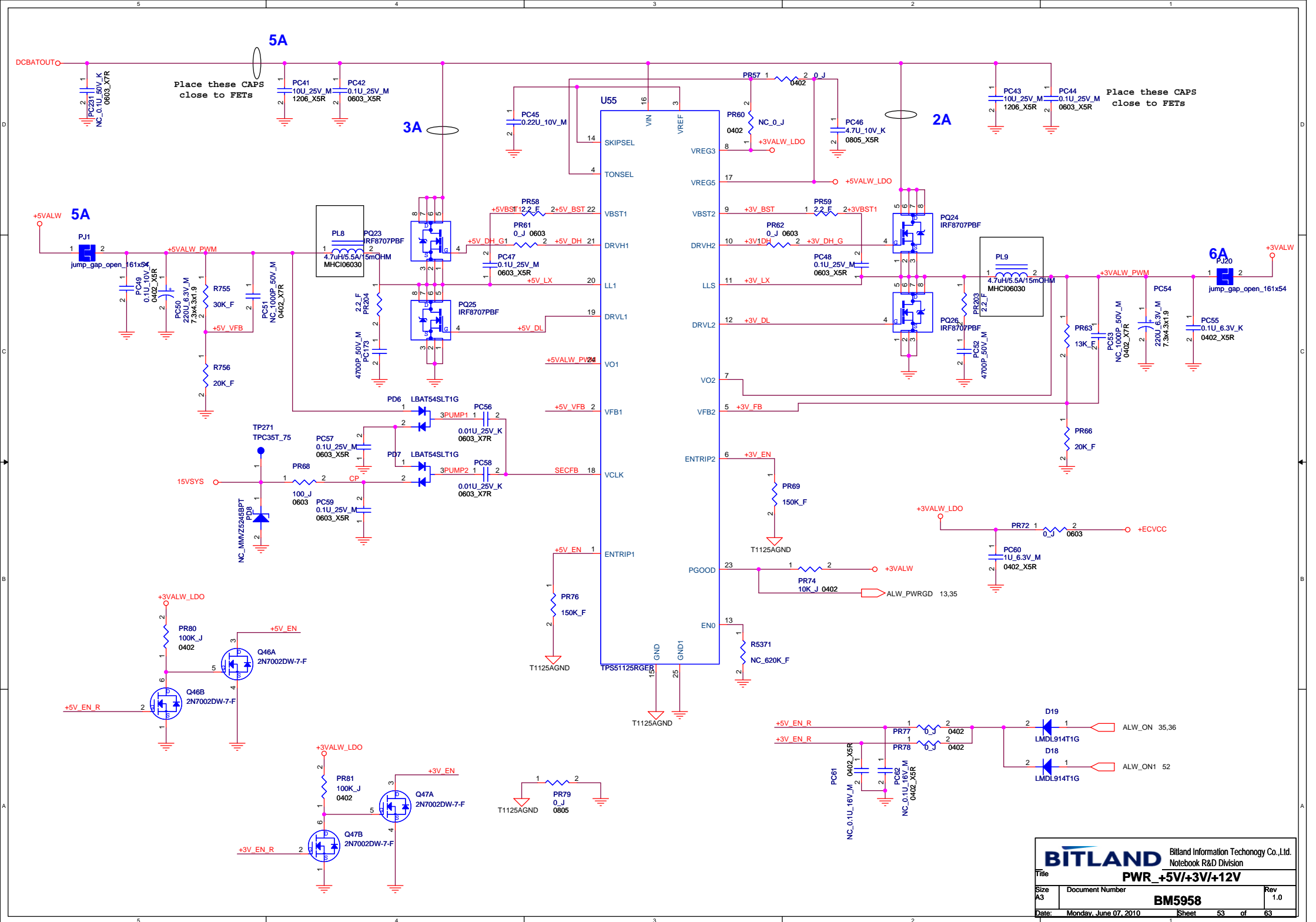


### TOUCH PAD CONN.

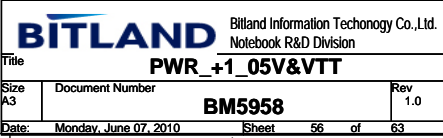


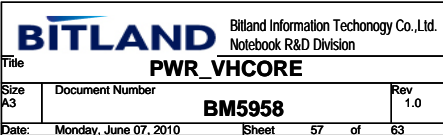






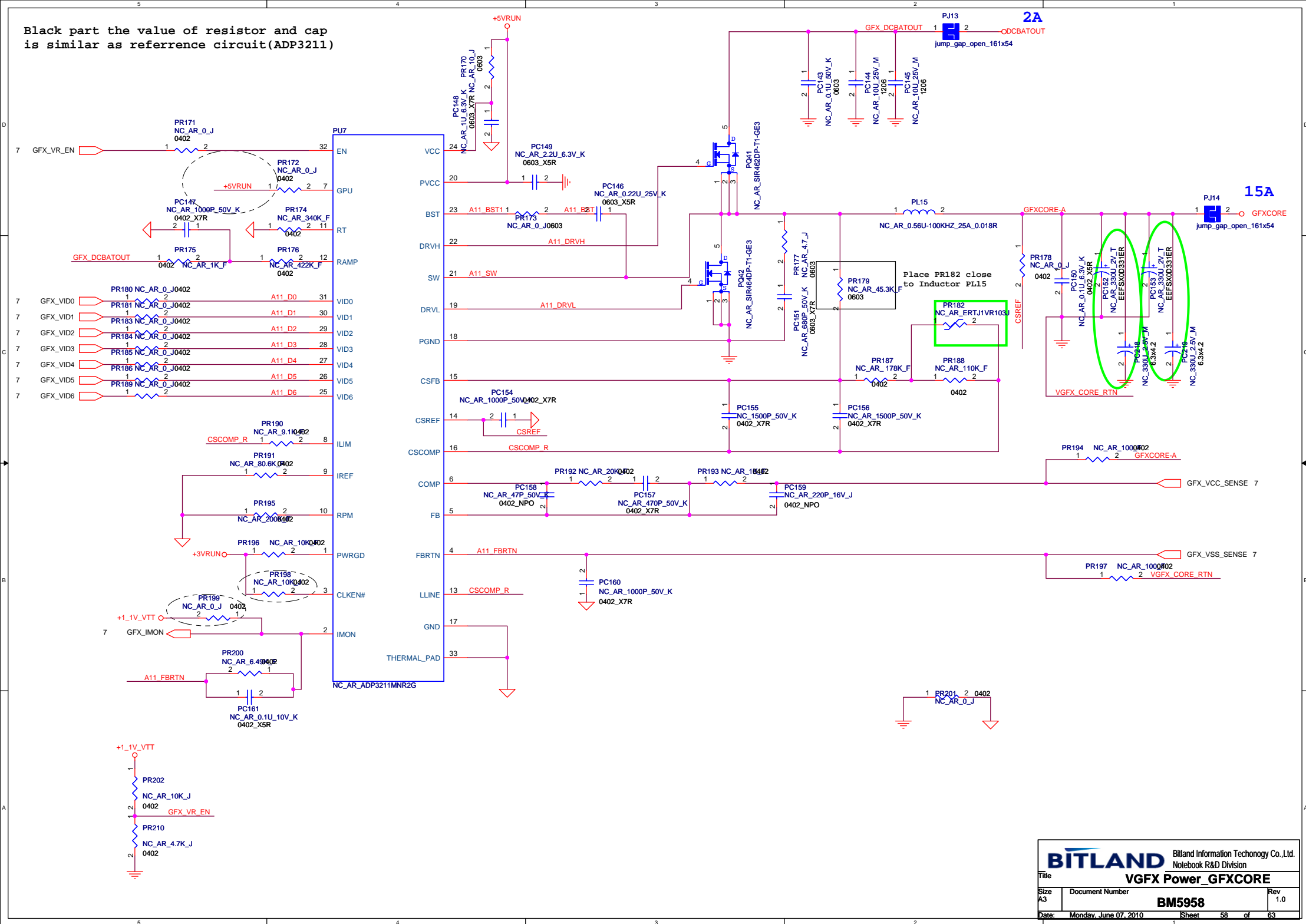


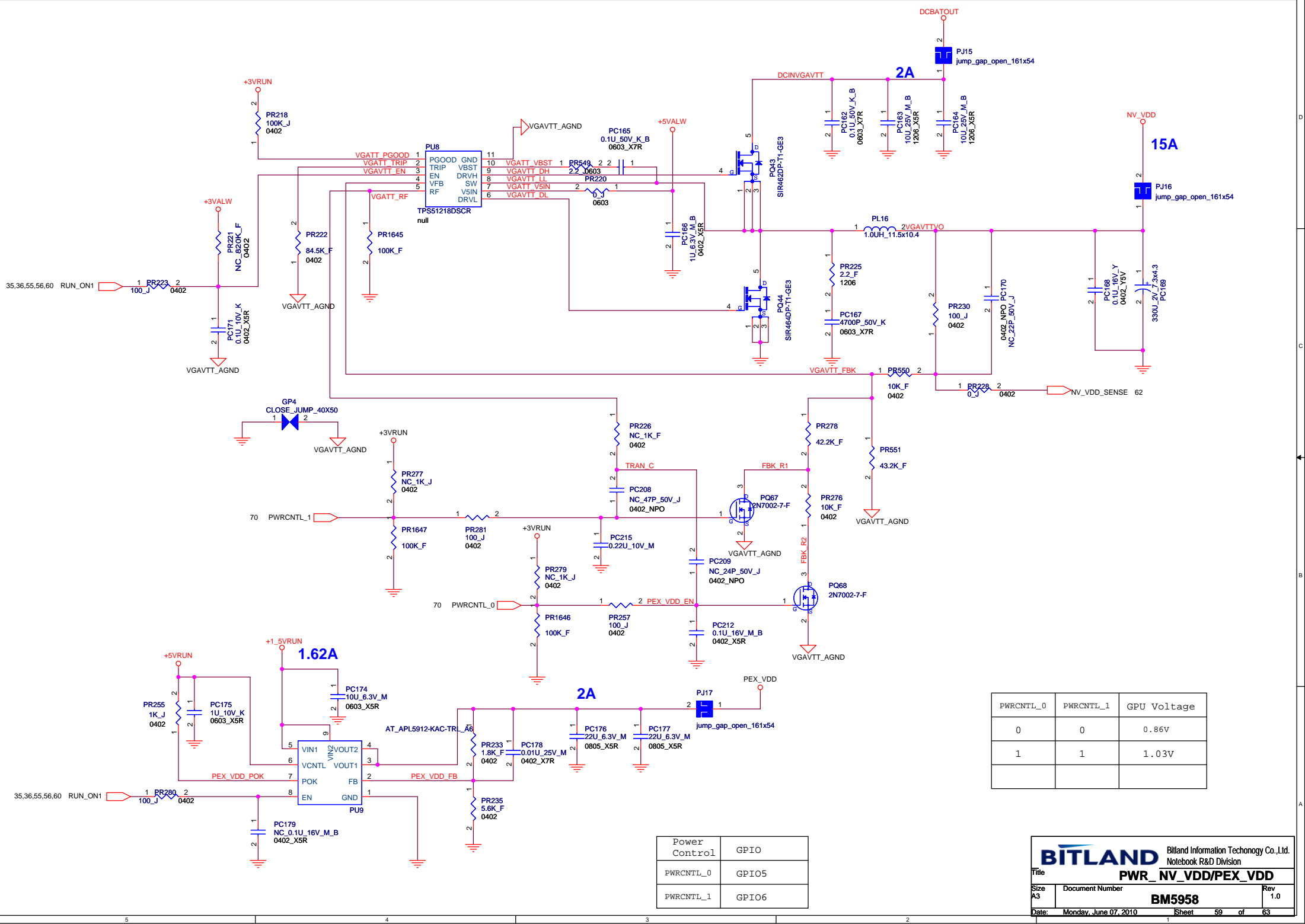






Black part the value of resistor and cap is similar as reference circuit(ADP3211)





PWRCNTL_0	PWRCNTL_1	GPU Voltage
0	0	0.86V
1	1	1.03V

Power Control	GPIO
PWRCNTL_0	GPIO5
PWRCNTL_1	GPIO6

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Document Number

Rev 1.0

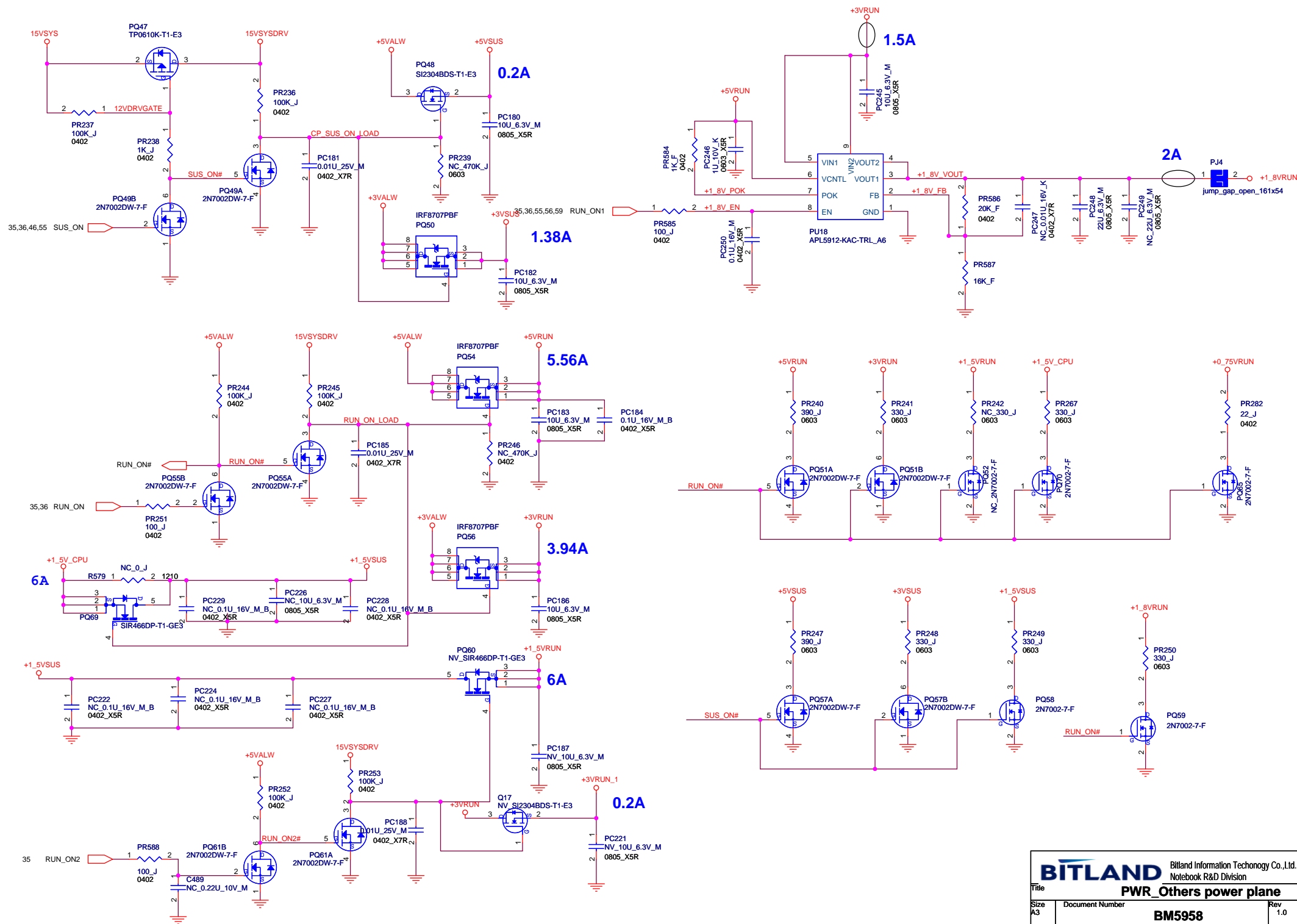
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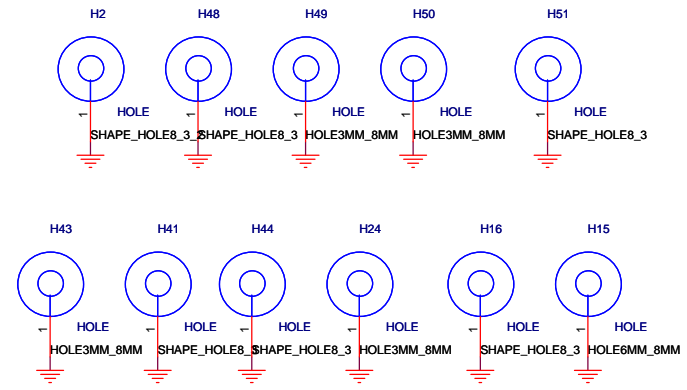
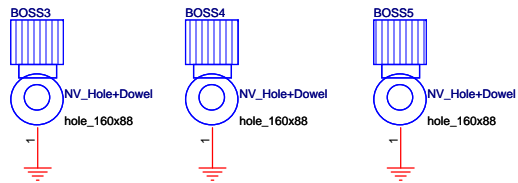
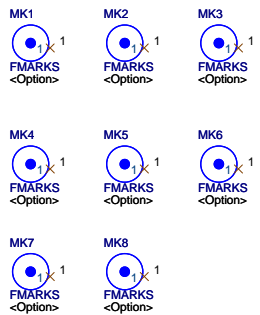
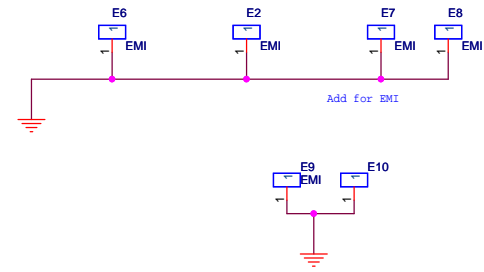
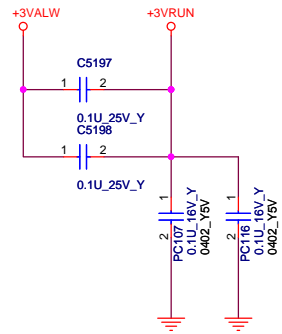
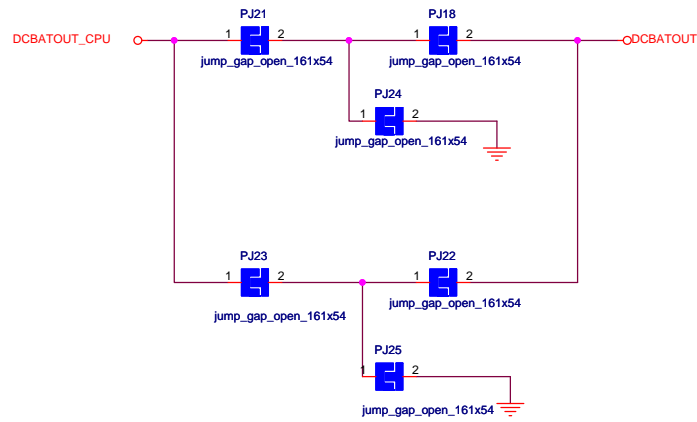
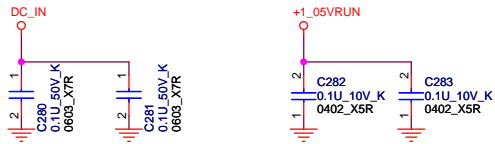
Monday, June 07, 2010

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of 63

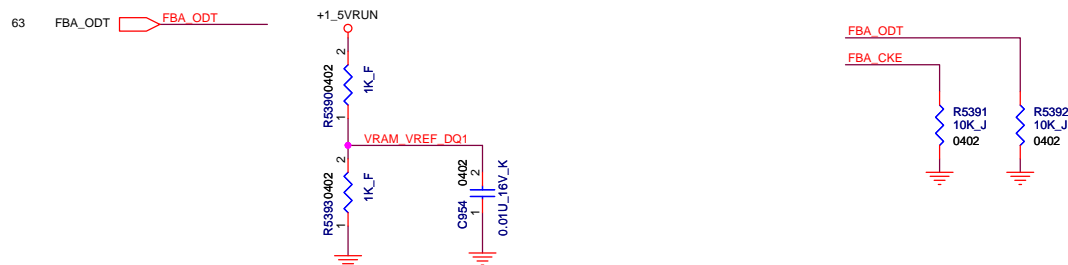
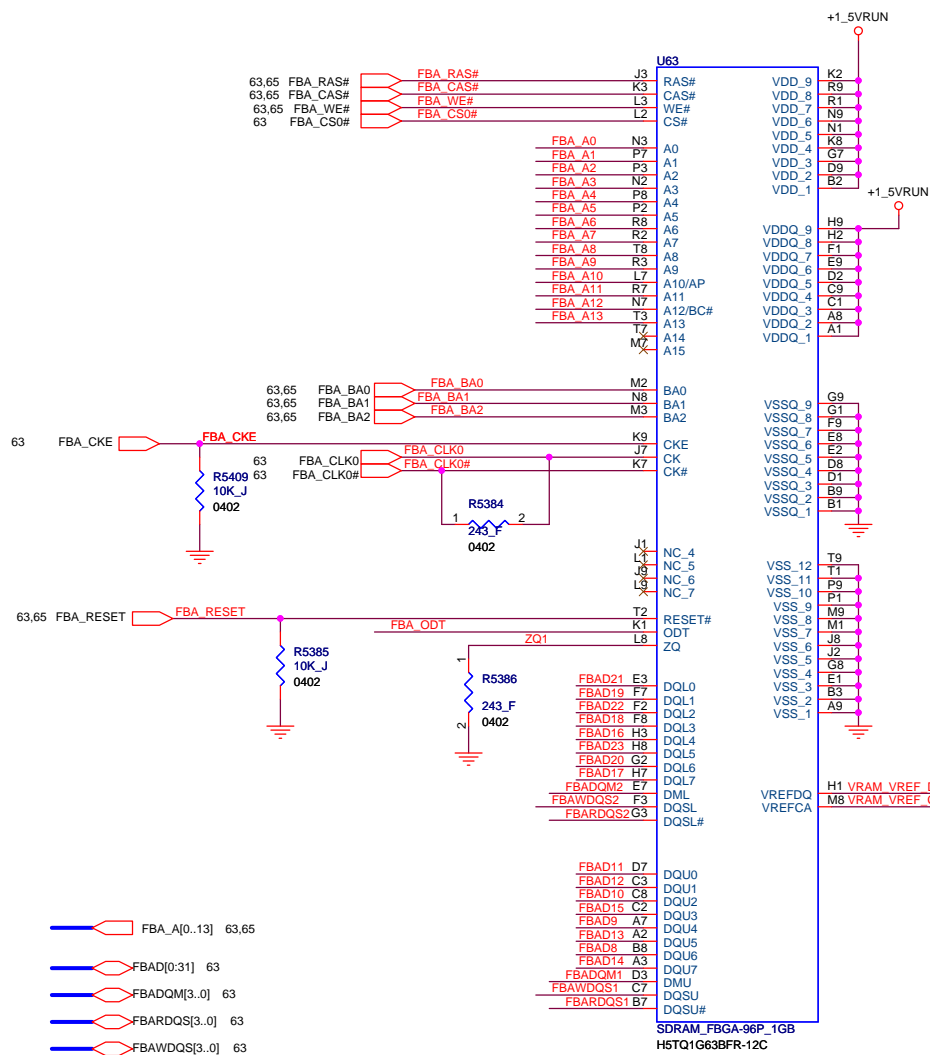
Title: **PWR\_NV\_VDD/PEX\_VDD**



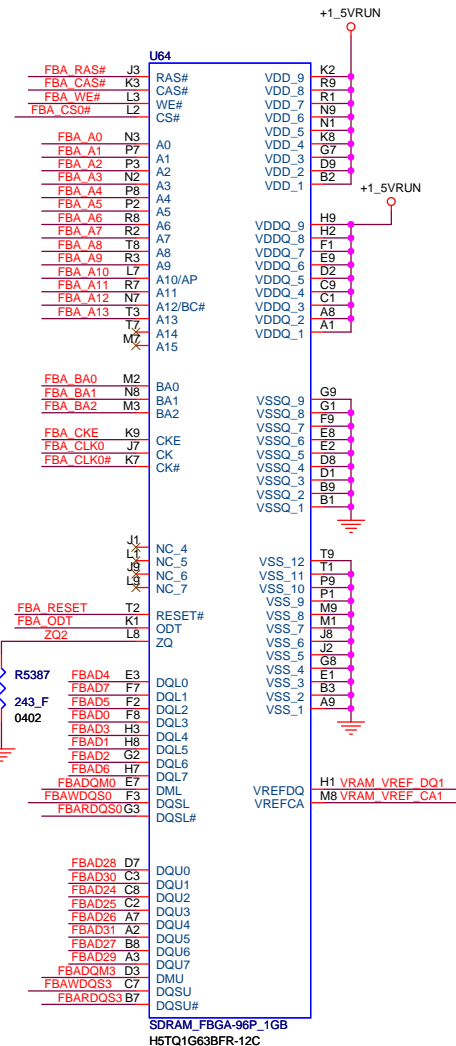








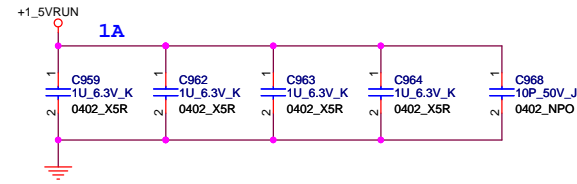
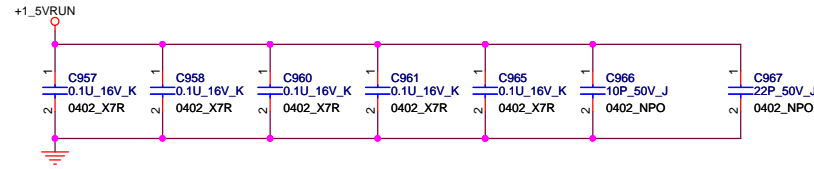
	0...30	32...63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4	A2	
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS0#	
CMD30	ODT	



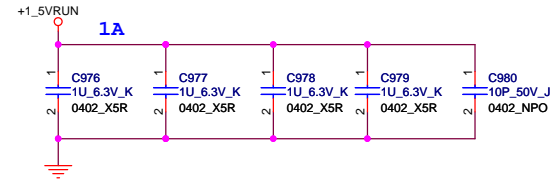
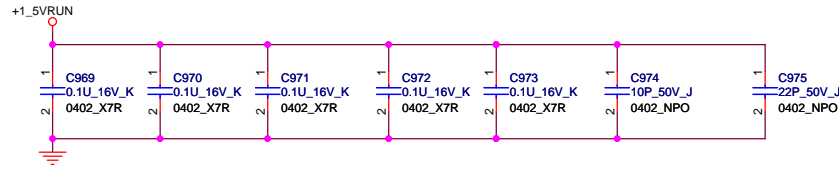




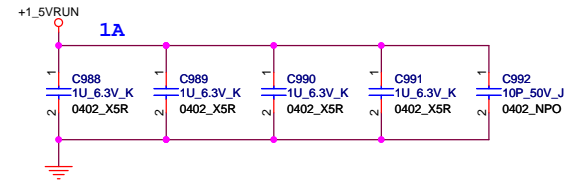
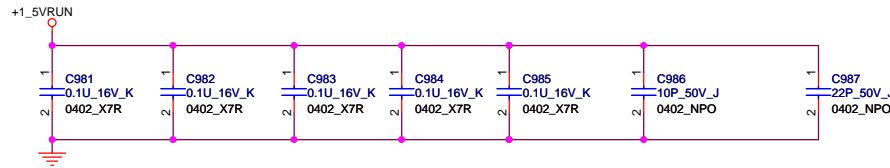
Place around the VRAM U63



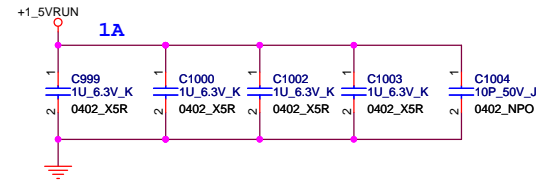
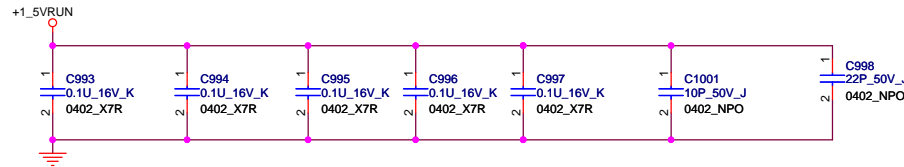
Place around the VRAM U64



Place around the VRAM U65

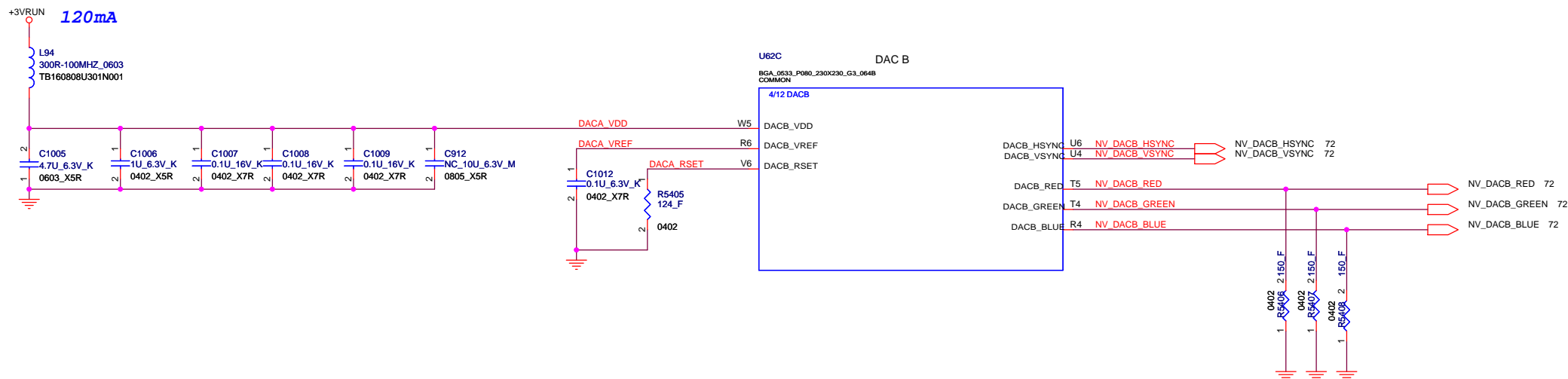
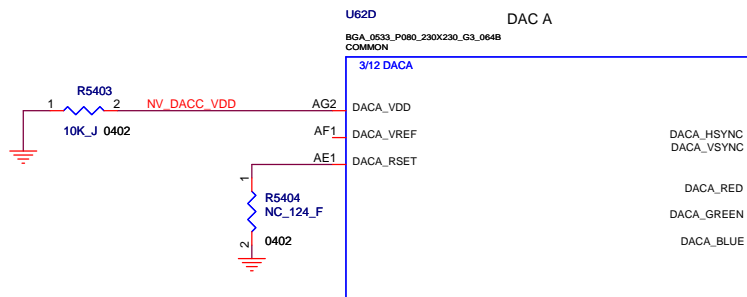


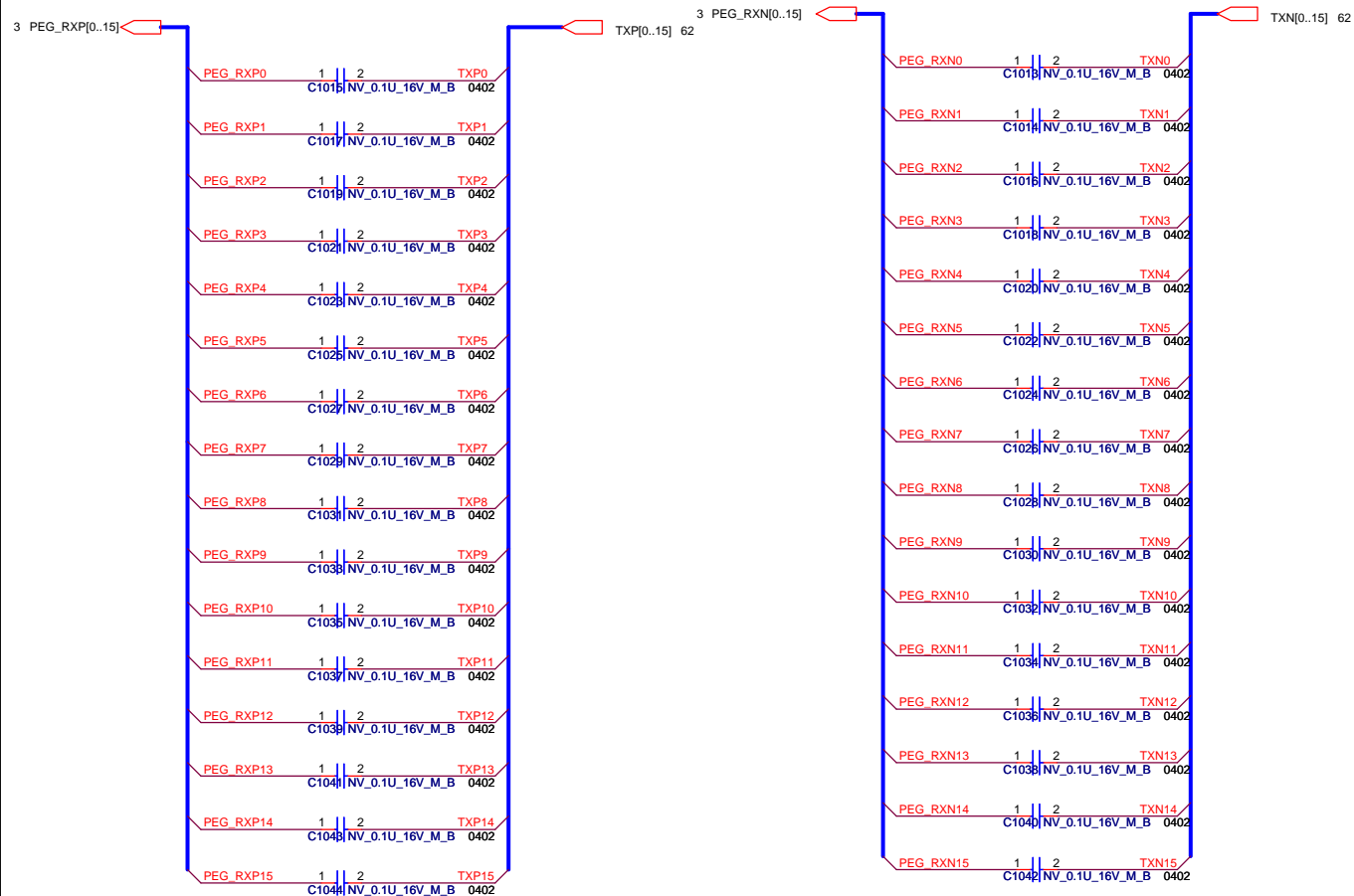
Place around the VRAM U66



PLACE 1UF CAPACITORS CLOSE TO THE MEMORY DEVICE.

PLACE 0.1UF CAPS UNDER THE MEMORY DEVICE.





STRAP0: USER[3:0]  
 STRAP1: 3GIO\_PADCFG\_LUT\_ADR[3:0]  
 STRAP2: PCI\_DEVID[3:0]

ROM\_SCLK: PCIDEVID\_EXT,SUB\_VENDOR,SLOT\_CLK,PEX\_PLL\_EN  
 ROM\_SI: RAMCFG[3:0]  
 ROM\_SO: XCLK\_277,TVMODE[2:0] \*\* G98  
 ROM\_SO: XCLK\_417,FB\_0\_BAR\_SIZE,SMB\_ALT\_ADDR,VGA\_DEVICE \*\*GT218

