

# Compal Confidential

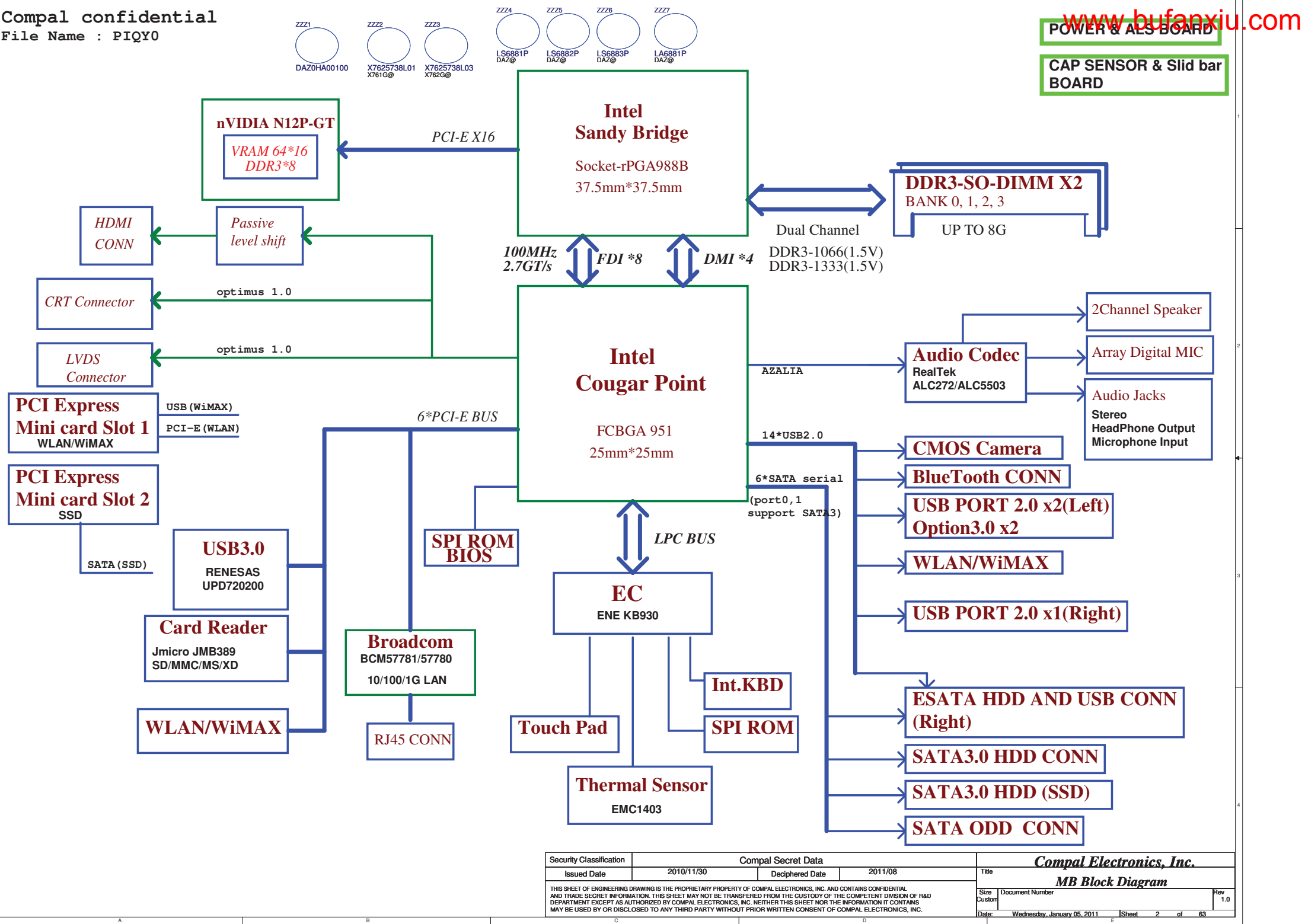
## PIQY0 M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH  
nVIDIA N12P-GT

2010-12-30

REV:1.0

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## Voltage Rails

power plane	State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
S0		○	○	○	○
S3		○	○	○	✗
S5 S4/AC		○	○	✗	✗
S5 S4/ Battery only		○	✗	✗	✗
S5 S4/AC & Battery don't exist		✗	✗	✗	✗

## SMBUS Control Table

	SOURCE	VGA	BATT	KB930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB930 +3VALW	✗	✓ +3VALW	✗	✗	✗	✗	✗
SMB_EC_CK2 SMB_EC_DA2	KB930 +3VALW	✗	✗	✗	✗	✗	✗	✓ +3VS
SMBCLK SMBDATA	PCH +3VALW	✗	✗	✗	✓ +3VS	✓ +3VS	✗	✗
SML0CLK SML0DATA	PCH +3VALW	✗	✗	✗	✗	✗	✗	✗
SML1CLK SML1DATA	PCH +3VALW	✓ +3VS	✗	✓ +3VS	✗	✗	✓ +3VS	✗

## EC SM Bus1 address

## EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor EMC1403-2	1001_101xb

## PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

## BOM Structure Table

BTO Item	BOM Structure
UMA	
UMA Only	UMA_ONLY@
Optimus	OPTI@
VRAM	X76@
HDMI	HDMI@
Blue Tooth	BT@
USB3.0	USB30@
ESATA	ESATA@
USB Charger	USB_CHG@
No USB Charger	NO_CHG@
Unpop	@
Codec ALC272	272@
Codec ALC5503	5503@
LAN 57781	57781@
LAN 57780	57780@
Ventura Feature	VENTURA@
Camera	CMOS@

### VRAM BOM Config

X761G@: X7625738L01	Samsung 1GB
Sub: X7625738L02	Hynix 1GB
X762G@: X7625738L03	Samsung 2GB
Sub: X7625738L04	Hynix 2GB

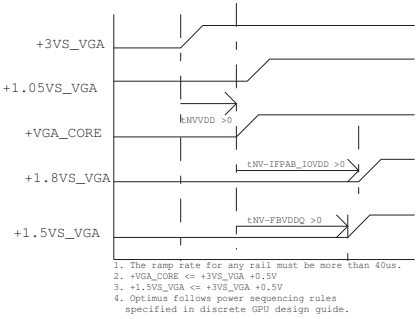
### GPU BOM Config

N12P SKU:	OPTI@
GS SKU:	GS@
GT SKU:	GT@

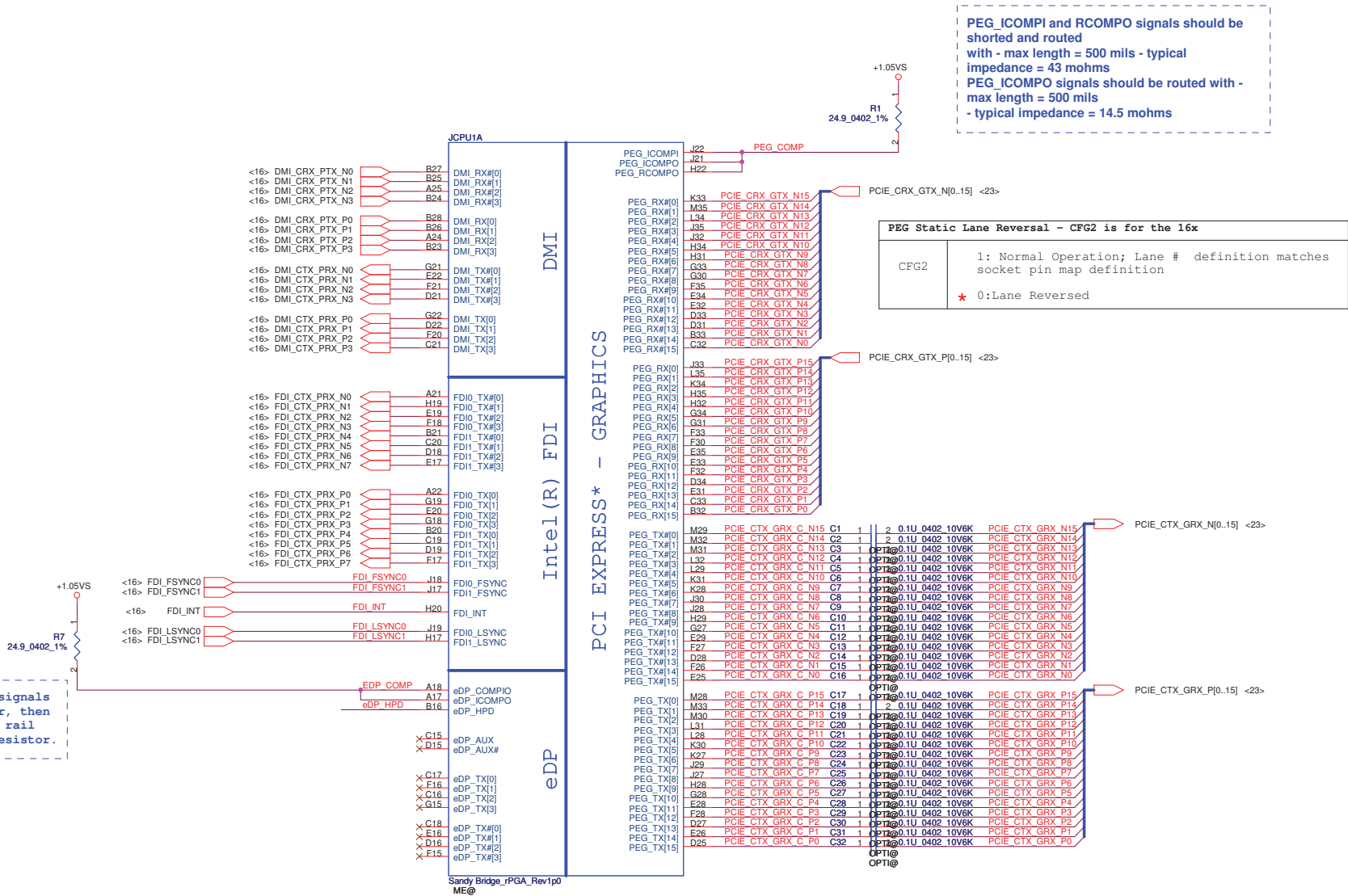
## USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/Cable (Right Side)
		1	USB Port (Right Side COMBO)
	UHCI1	2	USB/B (Left Side)
		3	USB/B (Left Side)
	UHCI2	4	
		5	Camera
EHCI2	UHCI3	6	
		7	
	UHCI4	8	
		9	Mini Card(WLAN)
	UHCI5	10	
		11	
	UHCI6	12	
		13	Blue Tooth

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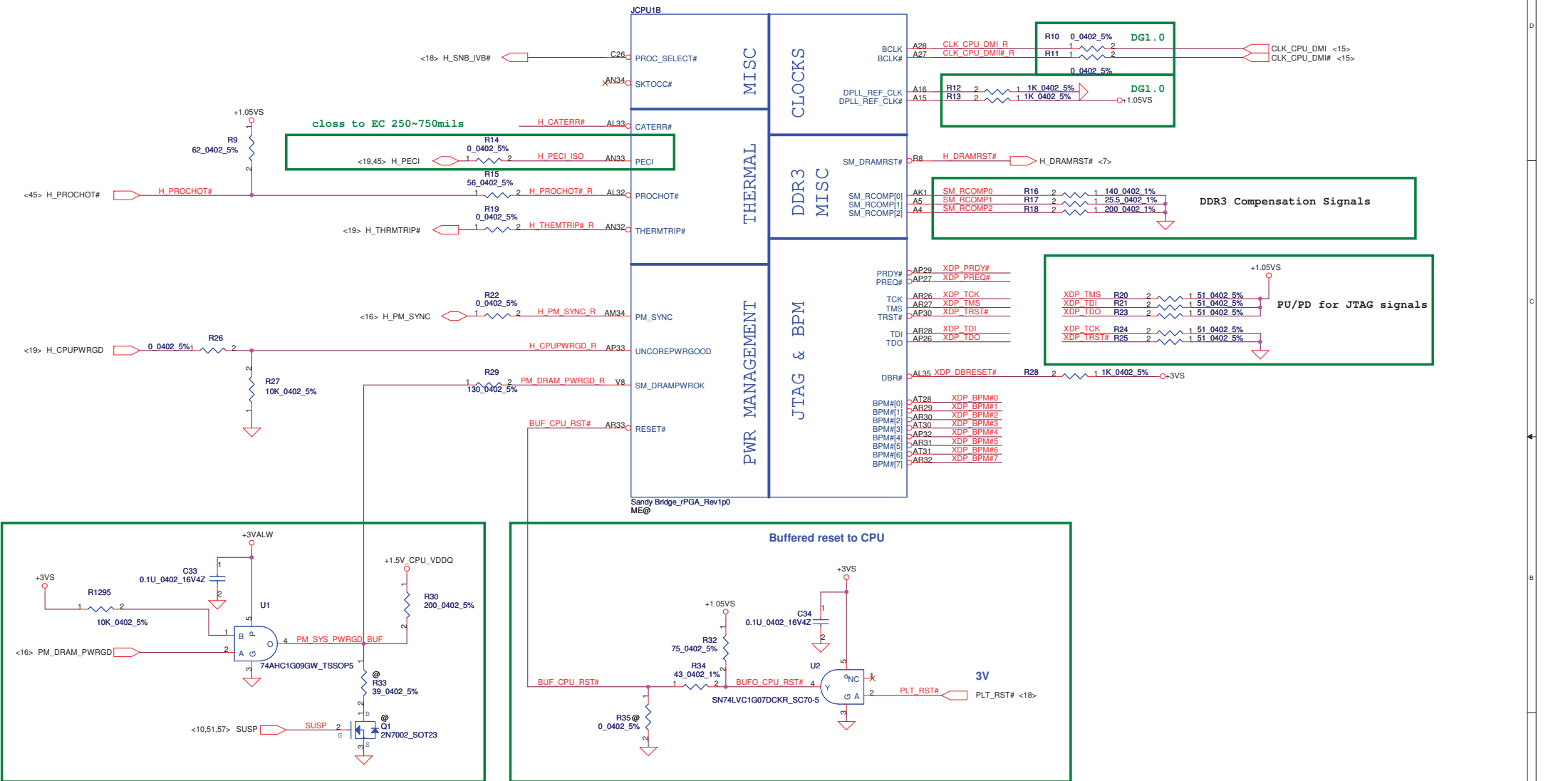


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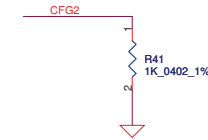


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Title			
<b>PROCESSOR(1/7) DMI,FDI,PEG</b>			
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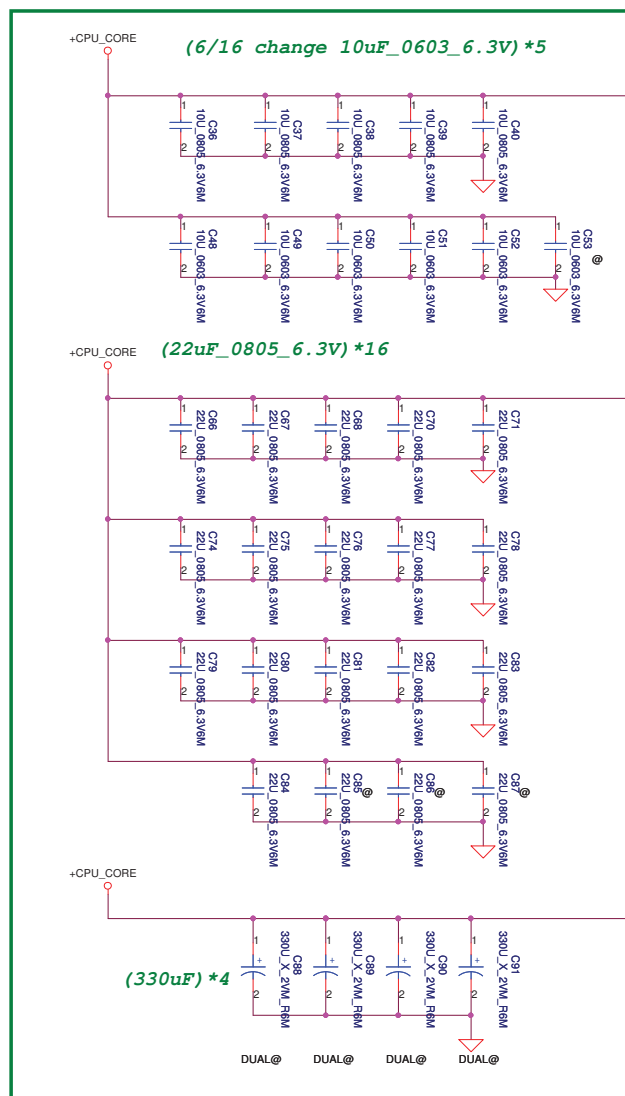


The schematic shows a differential pair of transistors. The gates of both transistors are connected to a common-mode feedback network consisting of two resistors, R43 and R44, both labeled as 1K\_0402\_1%. The gates are also connected to a common-mode input signal, CFG5. The drains of the transistors are connected to a differential-mode feedback network consisting of two resistors, R45 and R46, both labeled as 1K\_0402\_1%. The drains are also connected to a differential-mode input signal, CFG6. The sources of the transistors are connected to a common-mode output signal, CMOUT.

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## POWER

QC=94A  
DC=53A

JCPU1F

AG35 VCC1  
AG34 VCC2  
AG33 VCC3  
AG32 VCC4  
AG31 VCC5  
AG30 VCC6  
AG29 VCC7  
AG28 VCC8  
AG27 VCC9  
AG26 VCC10  
AF35 VCC11  
AF34 VCC12  
AF33 VCC13  
AF32 VCC14  
AF31 VCC15  
AF30 VCC16  
AF29 VCC17  
AF28 VCC18  
AF27 VCC19  
AF26 VCC20  
AD35 VCC21  
AD34 VCC22  
AD33 VCC23  
AD32 VCC24  
AD31 VCC25  
AD30 VCC26  
AD29 VCC27  
AD28 VCC28  
AD27 VCC29  
AD26 VCC30  
AC35 VCC31  
AC34 VCC32  
AC33 VCC33  
AC32 VCC34  
AC31 VCC35  
AC30 VCC36  
AC29 VCC37  
AC28 VCC38  
AC27 VCC39  
AC26 VCC40  
AA35 VCC41  
AA34 VCC42  
AA33 VCC43  
AA32 VCC44  
AA31 VCC45  
AA30 VCC46  
AA29 VCC47  
AA28 VCC48  
AA27 VCC49  
AA26 VCC50  
Y35 VCC51  
Y34 VCC52  
Y33 VCC53  
Y32 VCC54  
Y31 VCC55  
Y30 VCC56  
Y29 VCC57  
Y28 VCC58  
Y27 VCC59  
Y26 VCC60  
Y25 VCC61  
Y24 VCC62  
Y23 VCC63  
Y22 VCC64  
Y21 VCC65  
Y20 VCC66  
Y19 VCC67  
Y18 VCC68  
Y17 VCC69  
Y16 VCC70  
Y15 VCC71  
Y14 VCC72  
Y13 VCC73  
Y12 VCC74  
Y11 VCC75  
Y10 VCC76  
Y09 VCC77  
Y08 VCC78  
Y07 VCC79  
Y06 VCC80  
Y05 VCC81  
Y04 VCC82  
Y03 VCC83  
Y02 VCC84  
Y01 VCC85  
R35 VCC86  
R34 VCC87  
R33 VCC88  
R32 VCC89  
R31 VCC90  
R30 VCC91  
R29 VCC92  
R28 VCC93  
R27 VCC94  
R26 VCC95  
R25 VCC96  
R24 VCC97  
R23 VCC98  
R22 VCC99  
R21 VCC100

## CORE SUPPLY

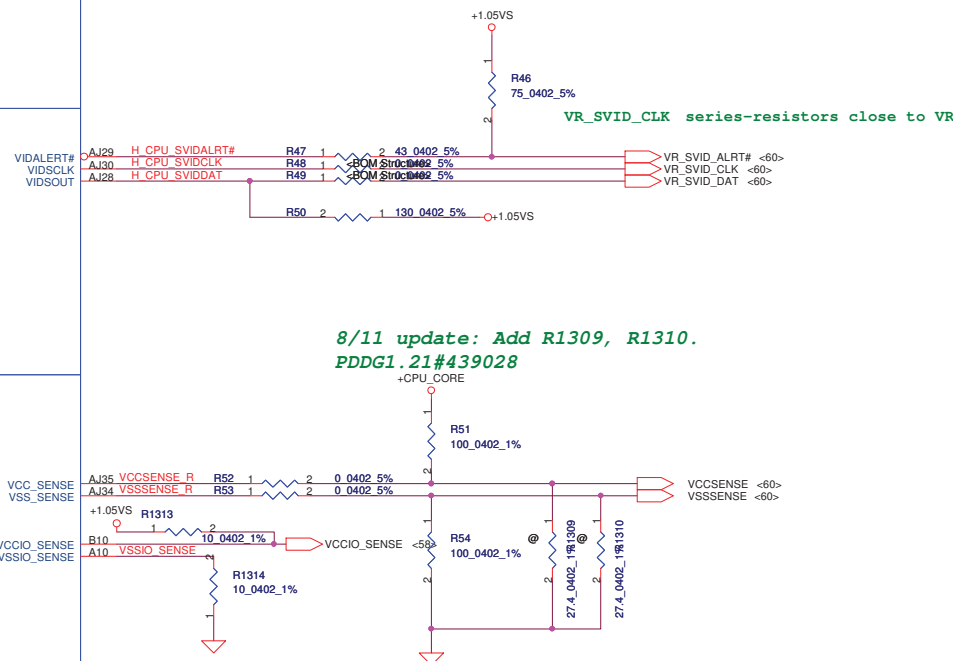
## SVID

## SENSE LINES

## PEG AND DDR

## SVID

## SENSE LINES

Sandy Bridge\_rPGA Rev1.0  
ME@

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2010/11/30

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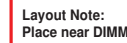
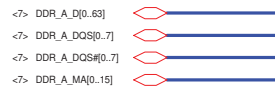
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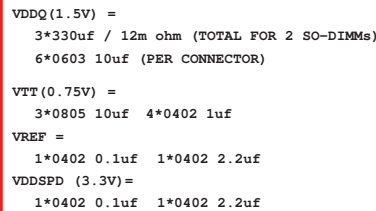
Compal Electronics, Inc.  
**PROCESSOR(5/7) PWR,BYPASS**  
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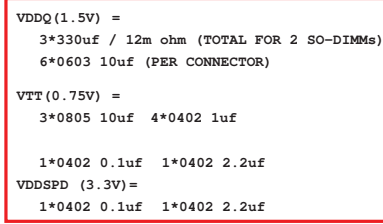
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Place near DIMM



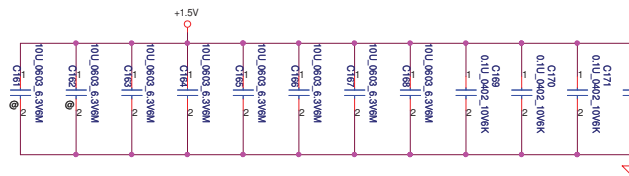
**Layout Note:**  
Short to ground

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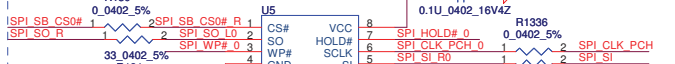
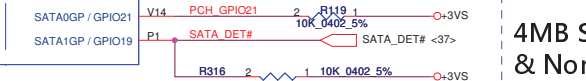
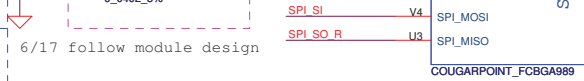


(10uF\_0603\_6.3V) \*8  
(0.1uF\_402\_10V) \*4



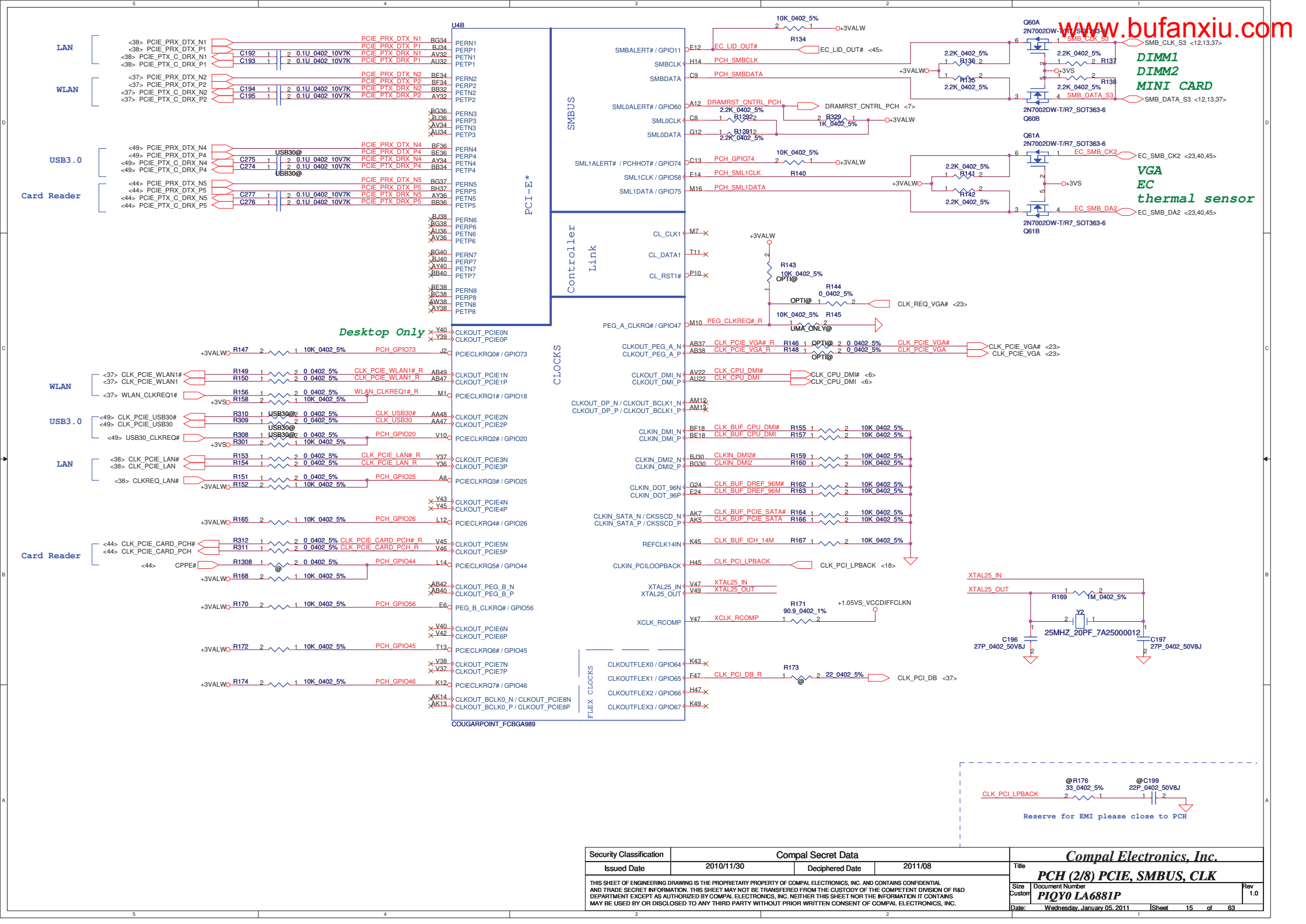
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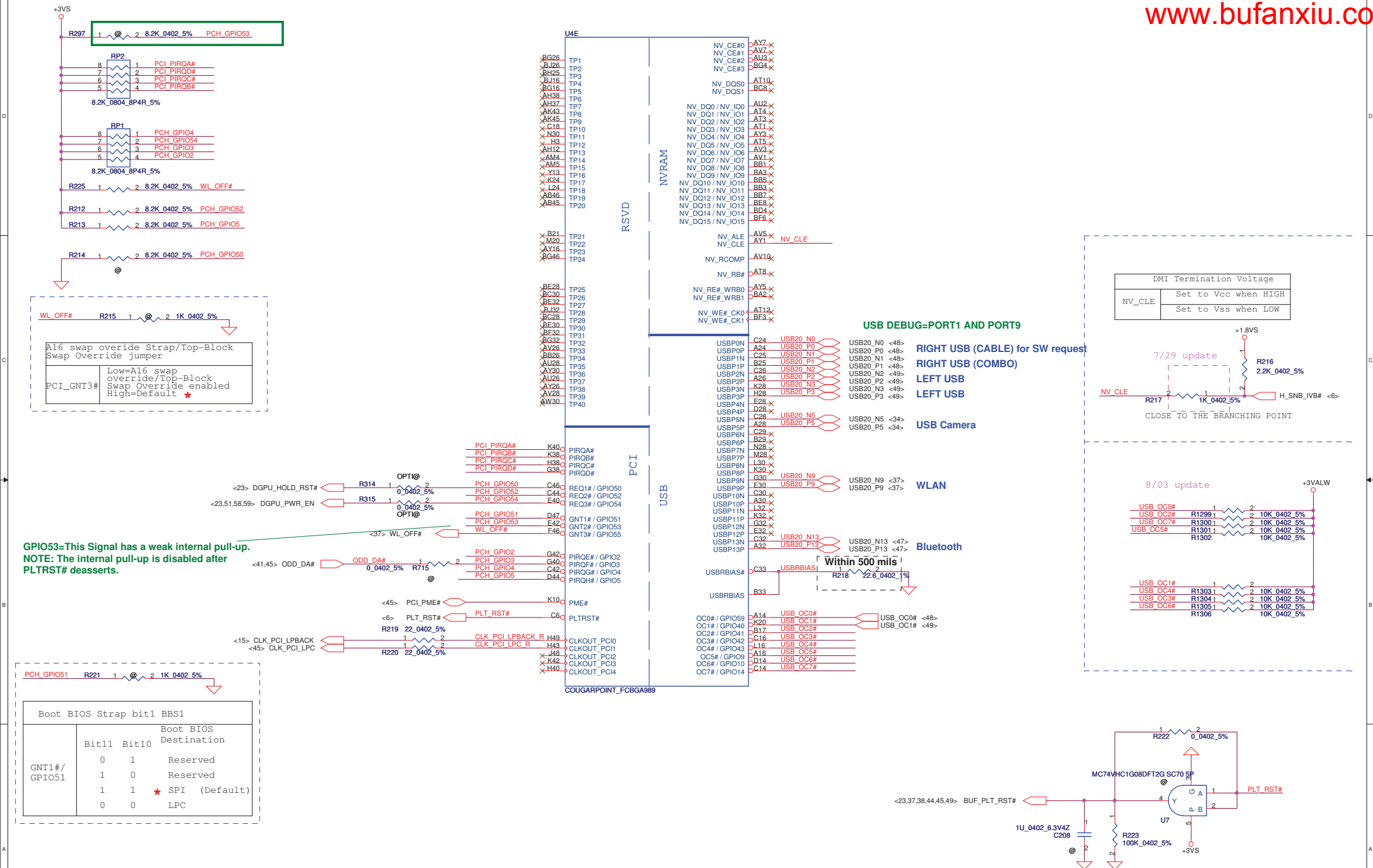




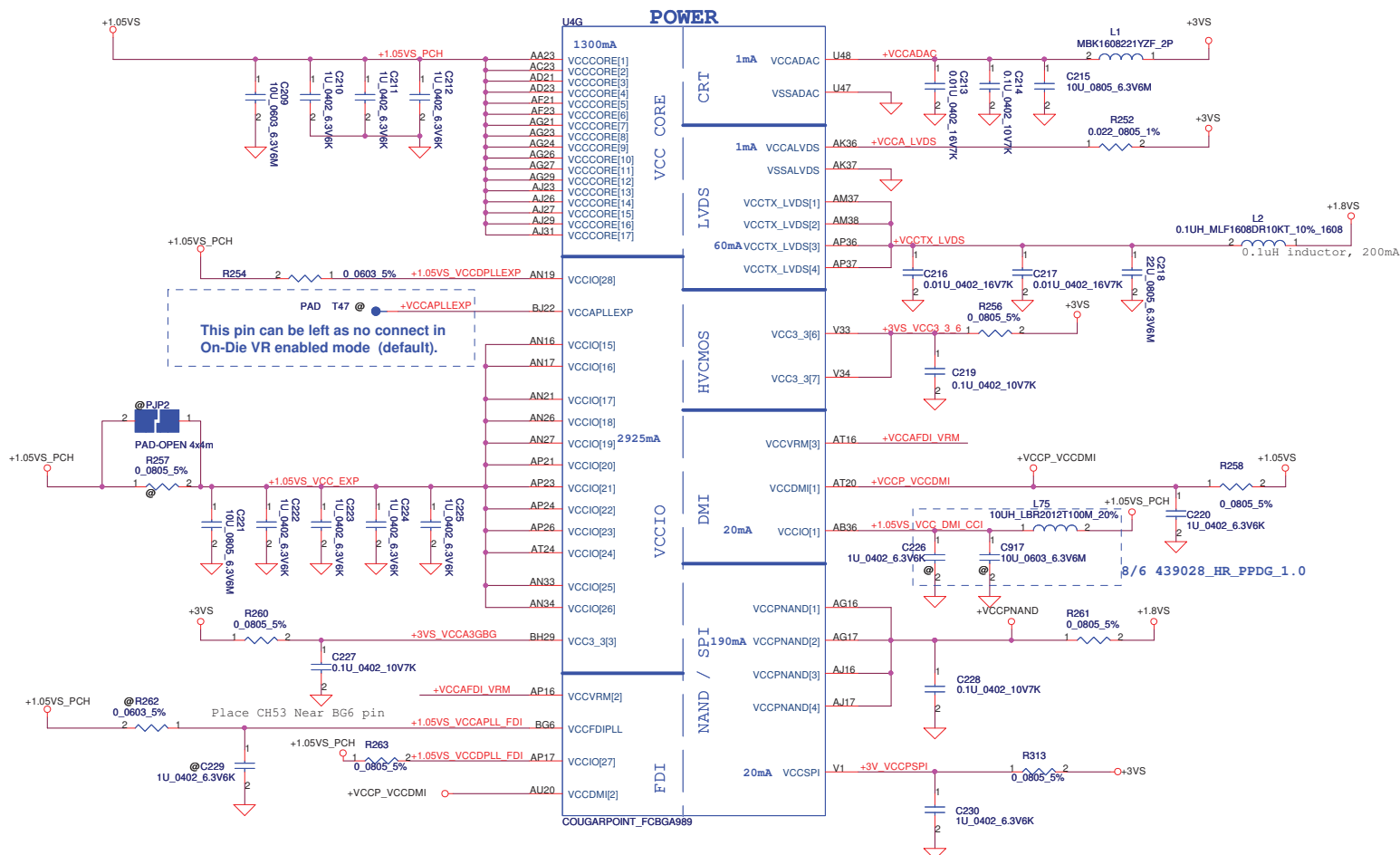








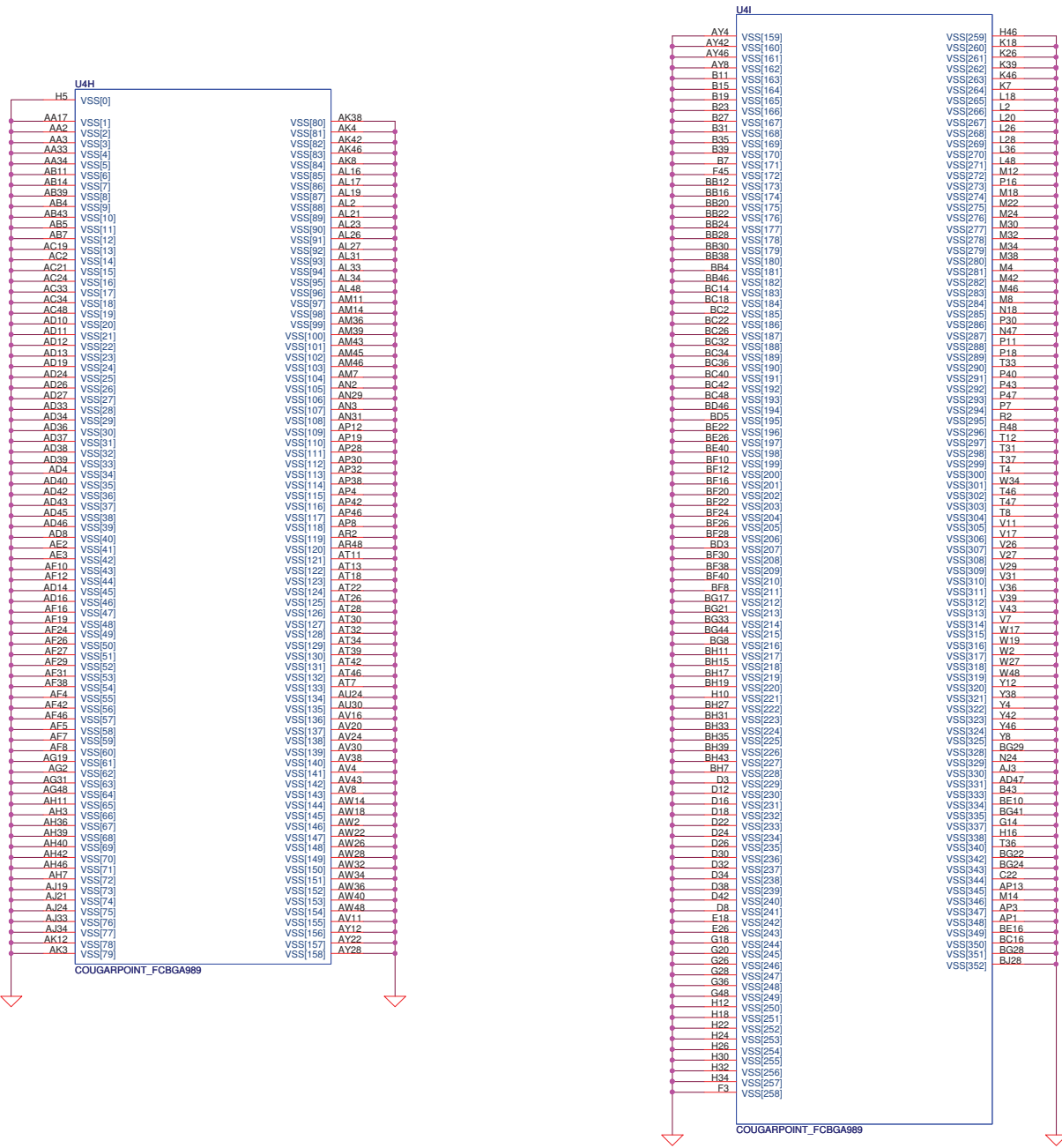




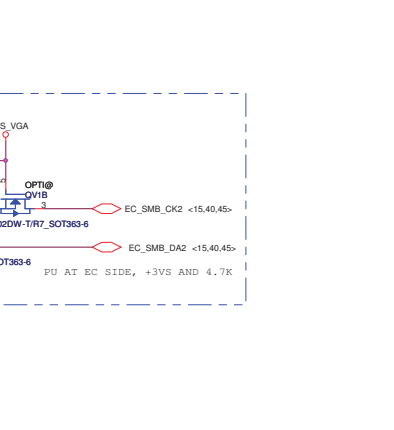
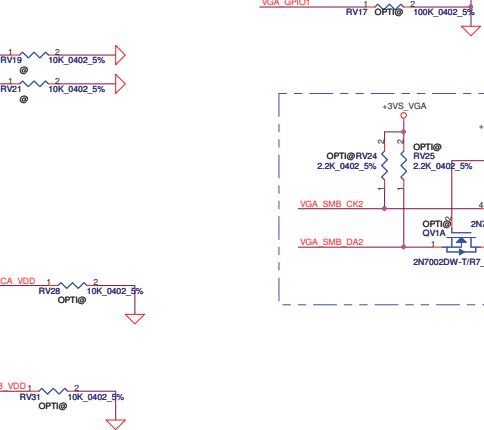
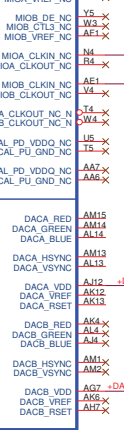
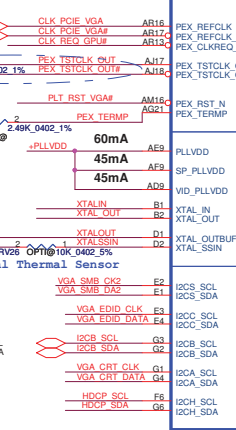
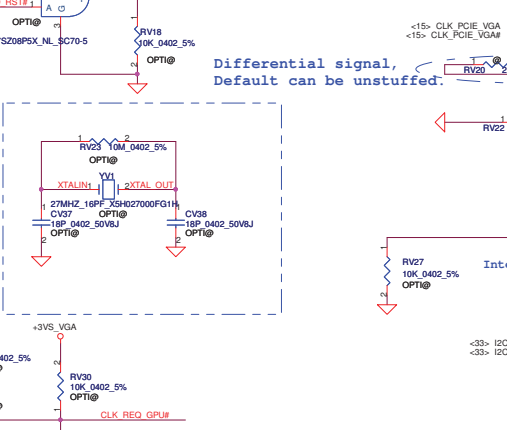
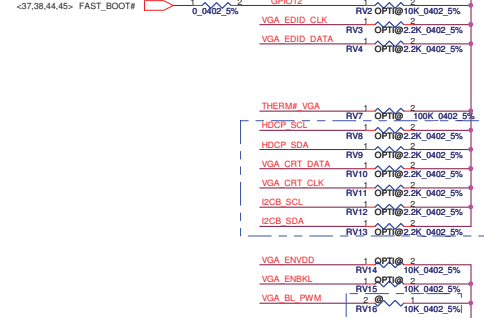
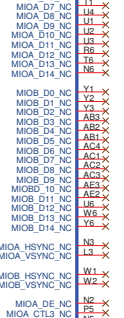
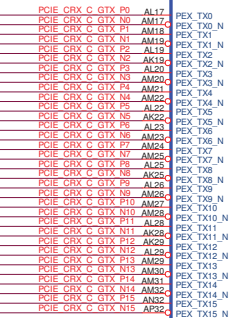
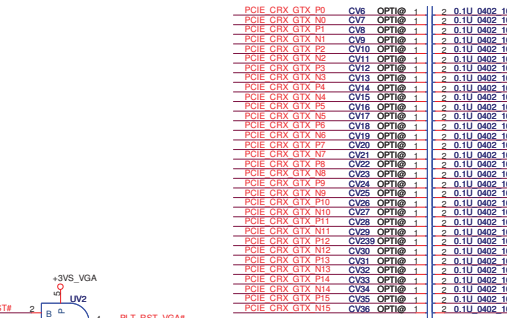
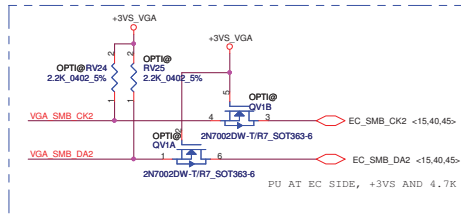
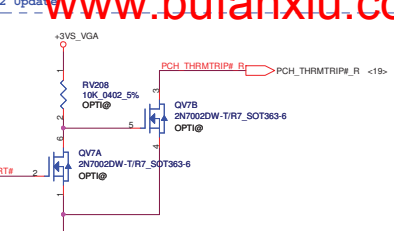
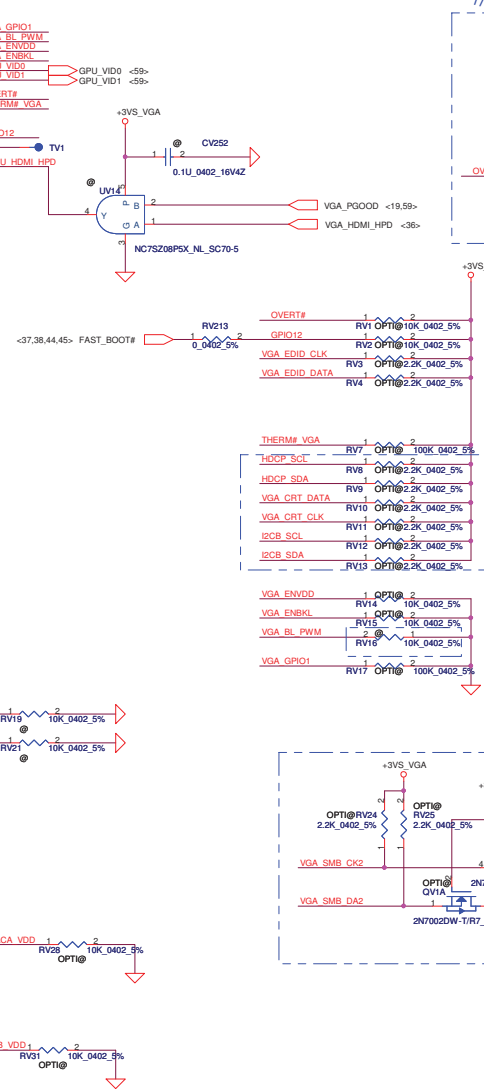
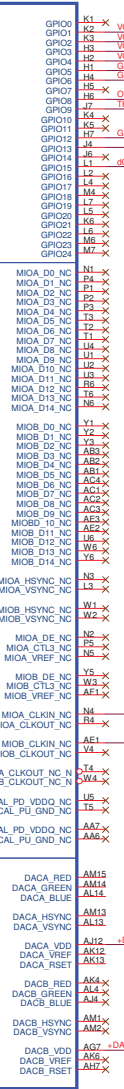
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06



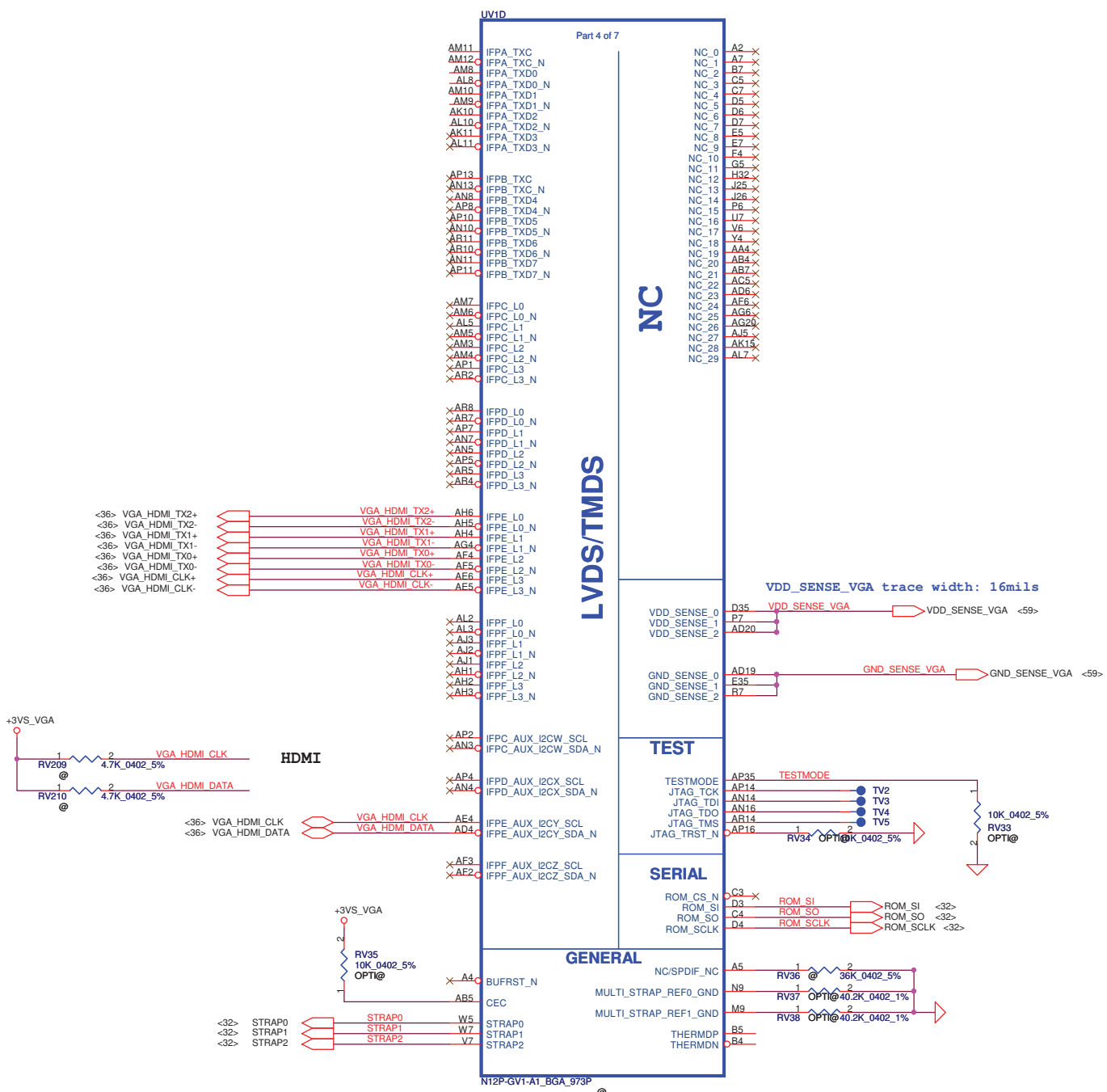
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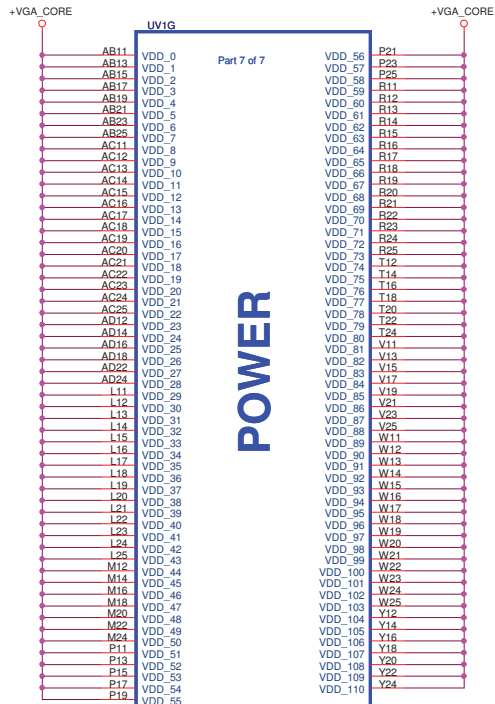
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		24		of	
		63			





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30.54A (41.02A Peak)



N12P-GV1-A1\_BGA\_973P

®

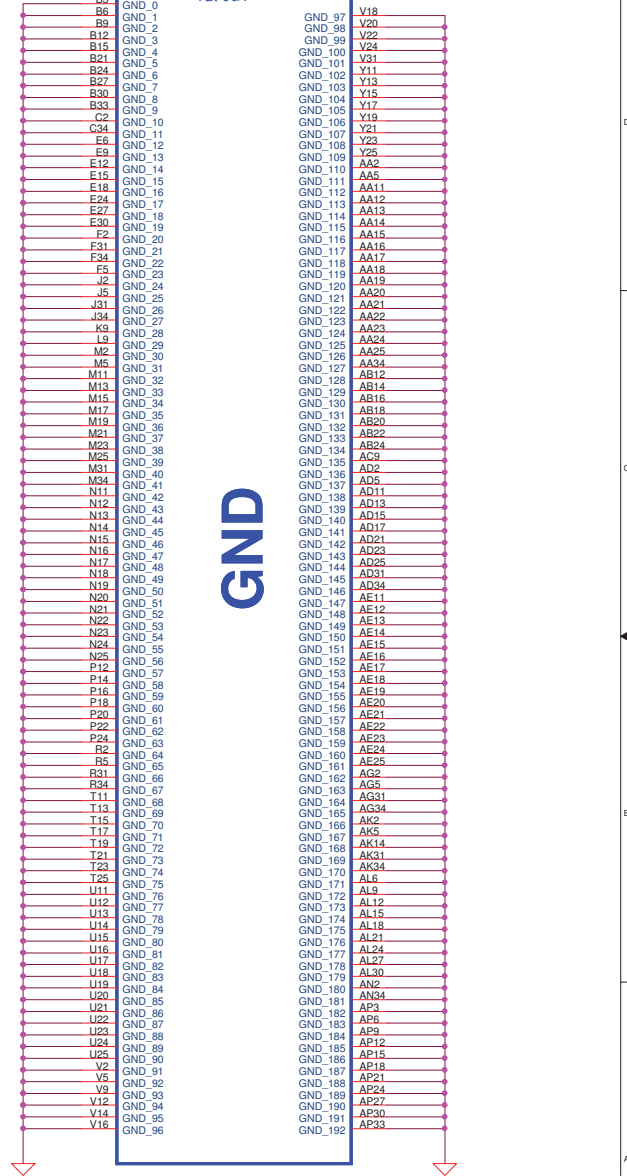
Near GPU

Under GPU

Under GPU

UVIF

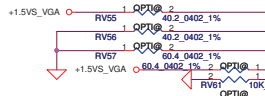
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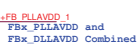
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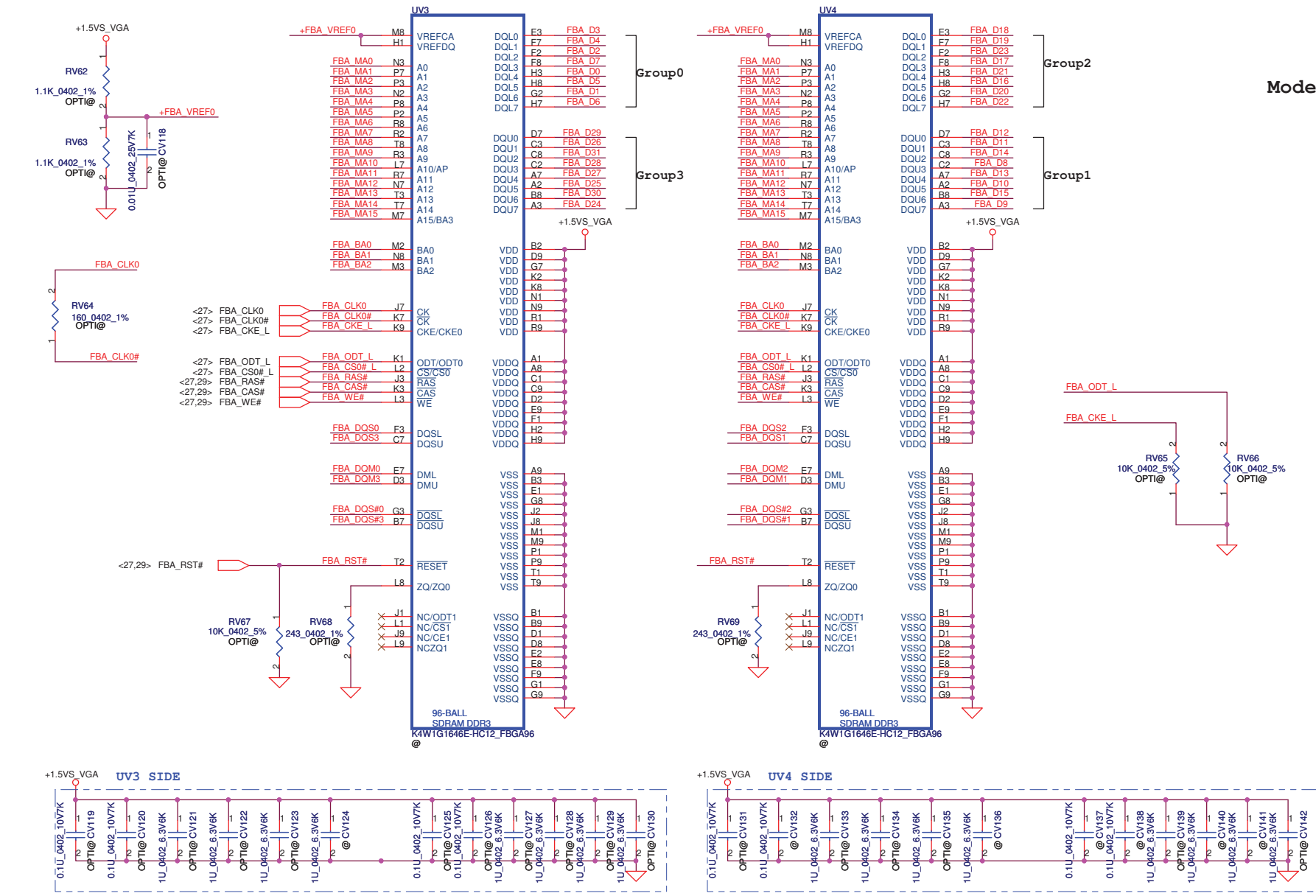


	DATA Bus	
Address	0..31	32..63
FBX_CMD0	CS0#_L	
FBX_CMD1		
FBX_CMD2	ODT_L	
FBX_CMD3	CKE_L	
FBX_CMD4	A14	A14
FBX_CMD5	RST	RST
FBX_CMD6	A9	A9
FBX_CMD7	A7	A7
FBX_CMD8	A2	A2
FBX_CMD9	A0	A0
FBX_CMD10	A4	A4
FBX_CMD11	A1	A1
FBX_CMD12	BA0	BA0
FBX_CMD13	WE#	WE#
FBX_CMD14	A15	A15
FBX_CMD15	CAS#	CAS#
FBX_CMD16		CS0#_H
FBX_CMD17		
FBX_CMD18		ODT_H
FBX_CMD19		CKE_H
FBX_CMD20	A13	A13
FBX_CMD21	A8	A8
FBX_CMD22	A6	A6
FBX_CMD23	A11	A11
FBX_CMD24	A5	A5
FBX_CMD25	A3	A3
FBX_CMD26	BA2	BA2
FBX_CMD27	BA1	BA1
FBX_CMD28	A12	A12
FBX_CMD29	A10	A10
FBX_CMD30	RAS#	RAS#



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				Date:	Wednesday, January 05, 2011
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Memory Partition A - Lower 32 bits

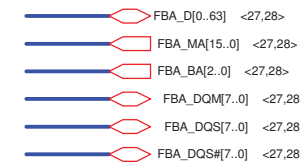
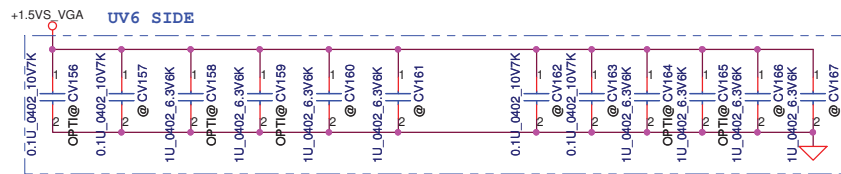
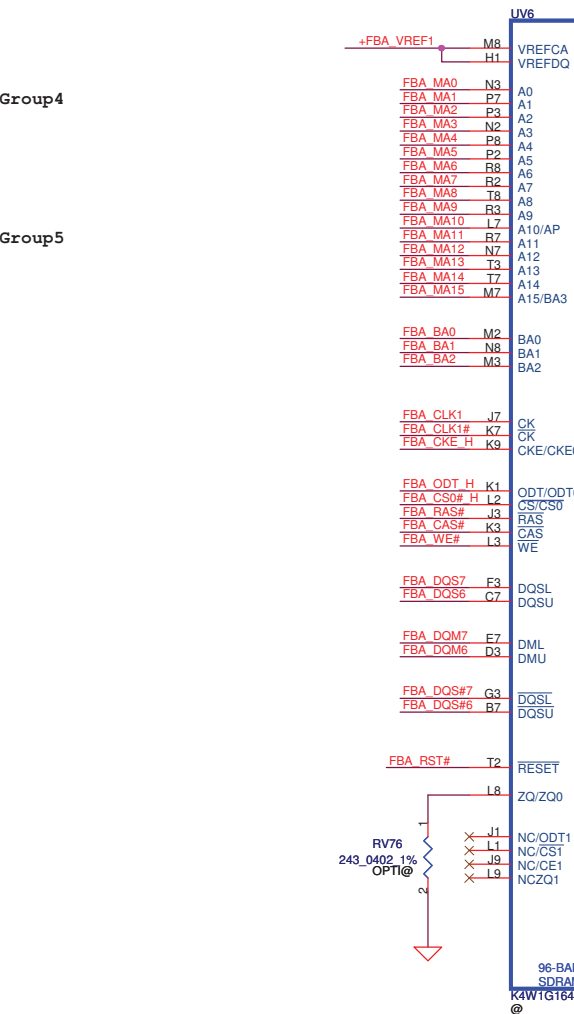
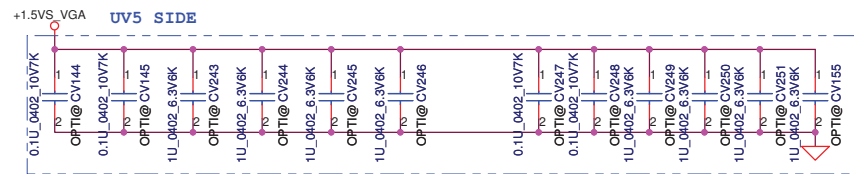
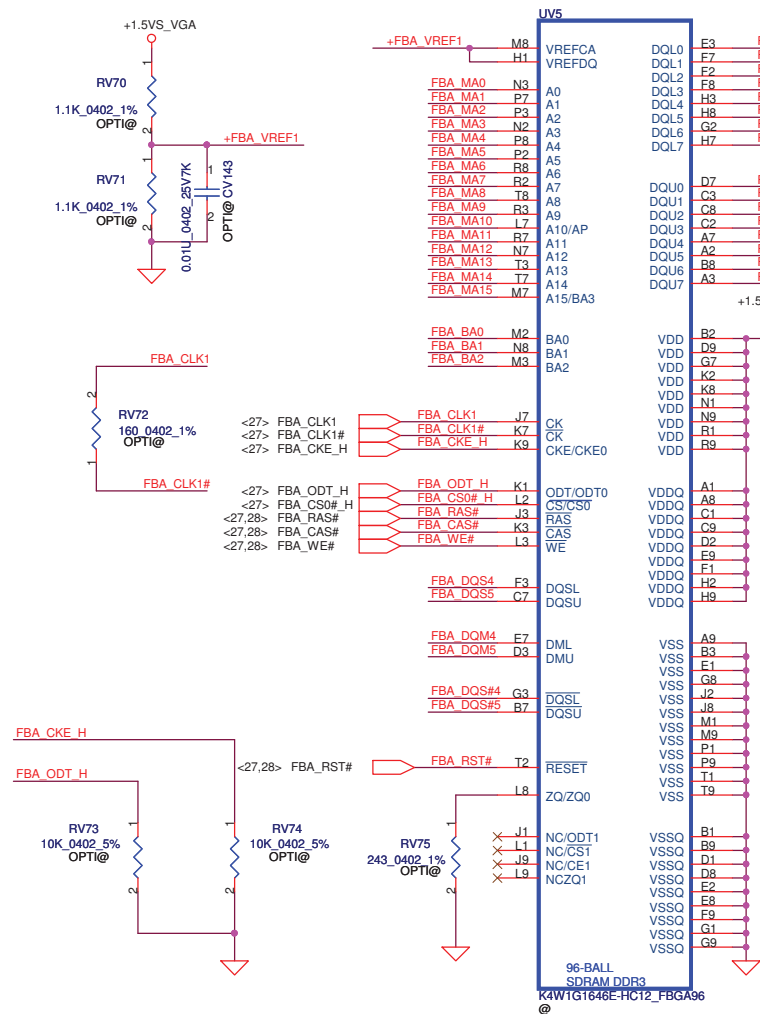


- FBA\_MA[15..0] <27,29>
- FBA\_BA[2..0] <27,29>
- FBA\_DQM[7..0] <27,29>
- FBA\_DQS[7..0] <27,29>

Mode D - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

# Memory Partition A - Upper 32 bits



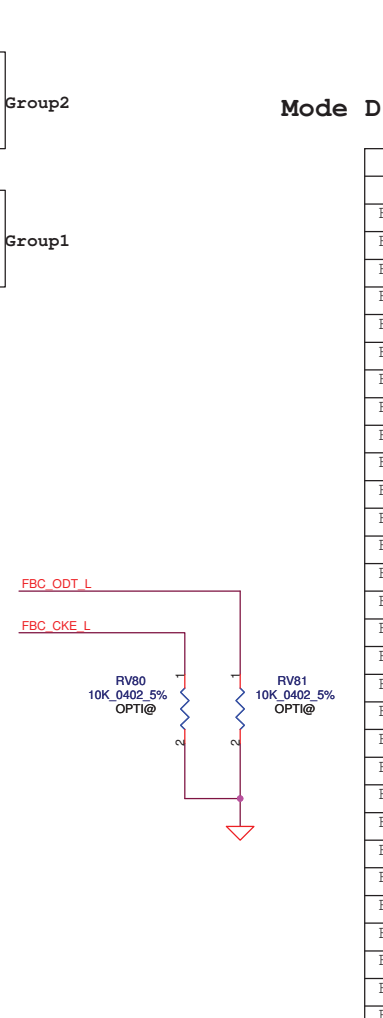
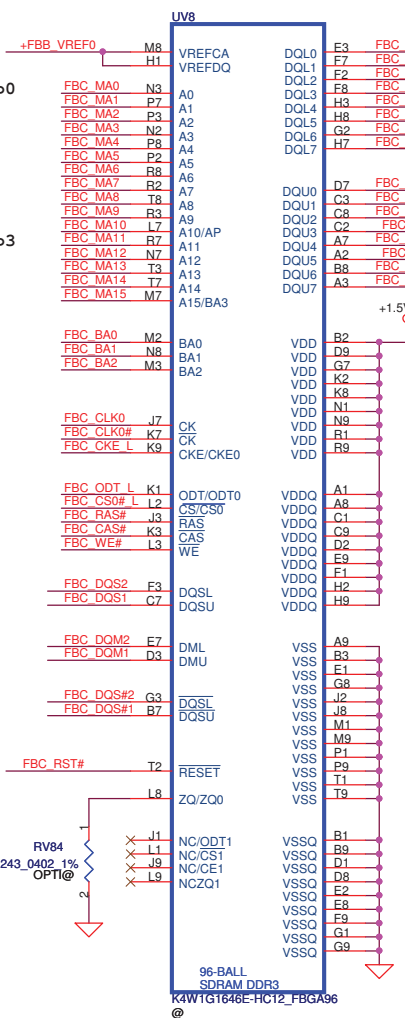
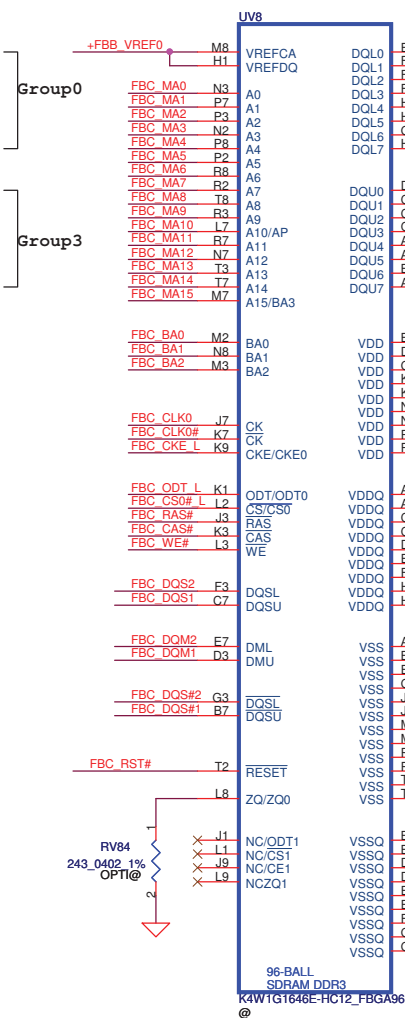
## Mode D - Mirror Mode Mapping

Address	DATA Bus	
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		ODT_H
FBx_CMD18		CKE_H
FBx_CMD19	A13	A13
FBx_CMD20	A8	A8
FBx_CMD21	A6	A6
FBx_CMD22	A11	A11
FBx_CMD23	A5	A5
FBx_CMD24	A3	A3
FBx_CMD25	BA2	BA2
FBx_CMD26	BA1	BA1
FBx_CMD27	A12	A12
FBx_CMD28	A10	A10
FBx_CMD29	RAS#	RAS#
FBx_CMD30		

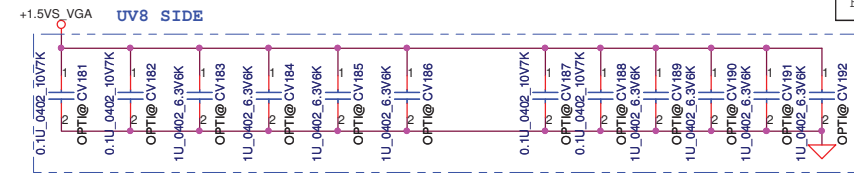
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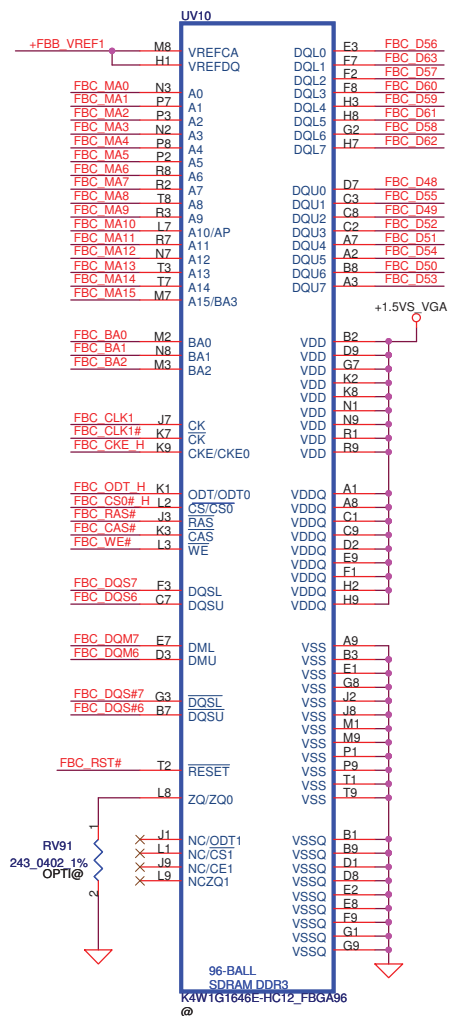
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	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
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FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

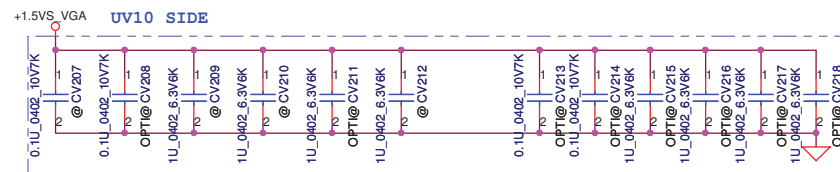
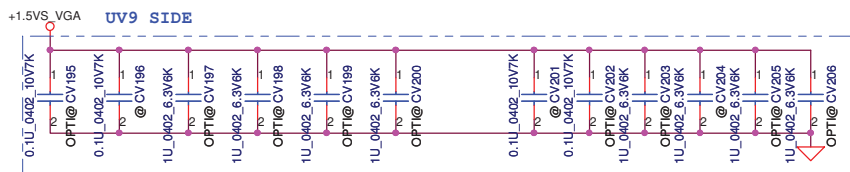


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## Mode D - Mirror Mode Mapping

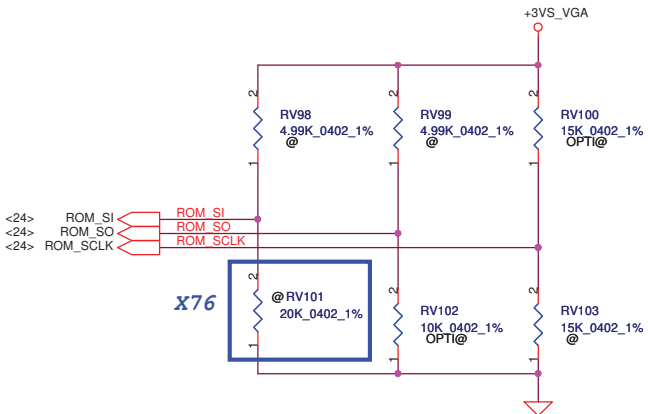
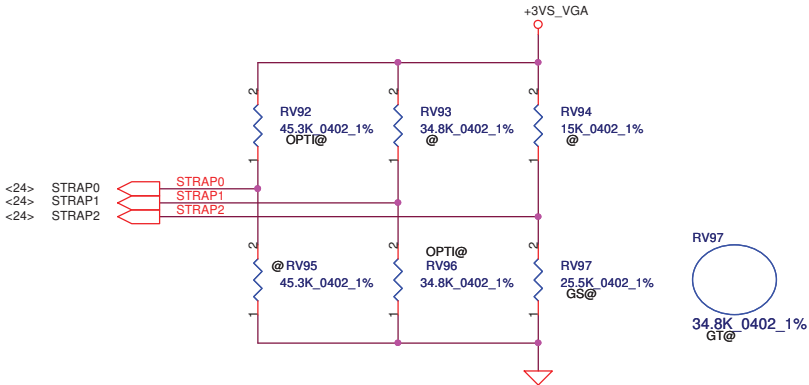
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Address	0...31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



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Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_VGA	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



ROM\_SO : PD-10K  
ROM\_SCLK : PH-15K  
ROM\_SI : PD20K (Samsung)  
Strap 2 : N12P-GS, PD-25K,  
N12P-GT, PD35K,  
Strap 1 : PD-35K  
Strap 0 : PH-45K

	DeviceID	ROM_SCLK	STRAP2
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GT	0x0DF6	Pull up 15K	Pull down 35K

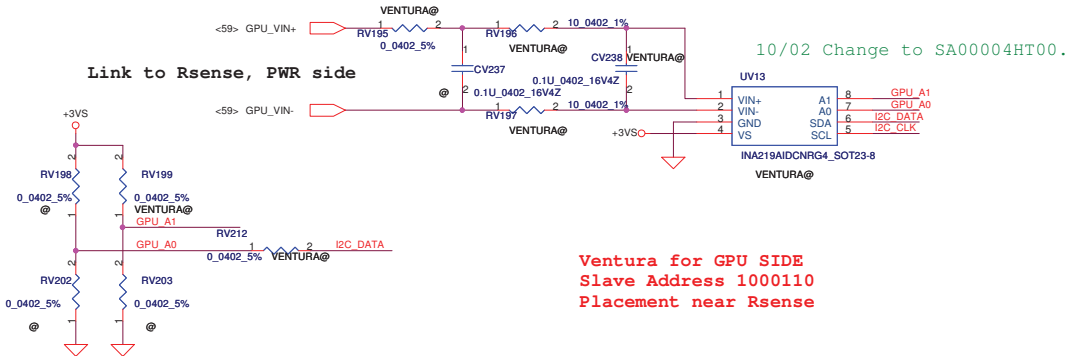
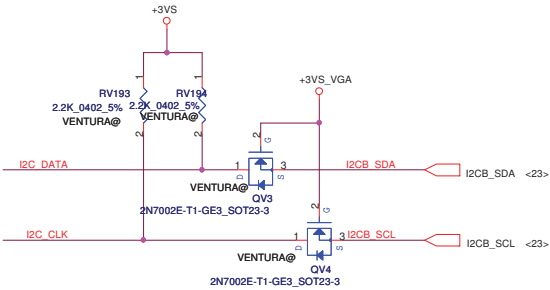
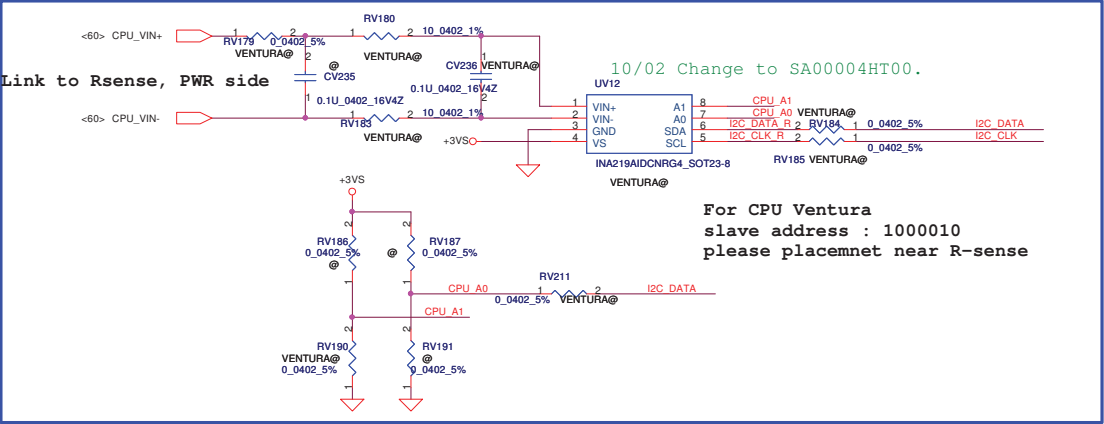
Hynix	H5TQ1G63BFR-12C	64Mx16	0010	PD 15K	SA000041S30
		128Mx16	0110	PD 35K	SA00003Y000
Samsung	K4W1G1646E-HC12	64Mx16	0011	PD 20K	SA000041T10
		128Mx16	0111	PD 45K	SA000047Q10

<b>SUB_VENDOR</b>		<b>XCLK_417</b>	
0	No VBIOS ROM	0	277MHz (Default)
1	BIOS ROM is present (Default)	1	Reserved
<b>FB_0_BAR_SIZE</b>		<b>USER Straps</b>	
0	256MB (Default)	User [3:0]	
1	Reserved	1000-1100	Customer defined
<b>3GIO_PADCFG</b>		<b>PEX_PLL_EN_TERM</b>	
3GIO_PADCFG[3:0]		0	Disable (Default)
0110	Notebook Default	1	Enable
<b>SLOT_CLK_CFG</b>			
0	GPU and MCH don't share a common reference clock		
1	GPU and MCH share a common reference clock (Default)		
<b>SMBUS_ALT_ADDR</b>		<b>VGA_DEVICE</b>	
0	0x9E (Default)	0	3D Device (Class Code 302h)
1	0x9C (Multi-GPU usage)	1	VGA Device (Default)

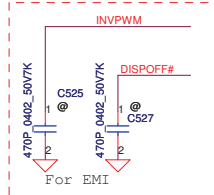
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				Date: Wednesday, January 05, 2011	Rev 1.0
				Sheet 32 of 63	



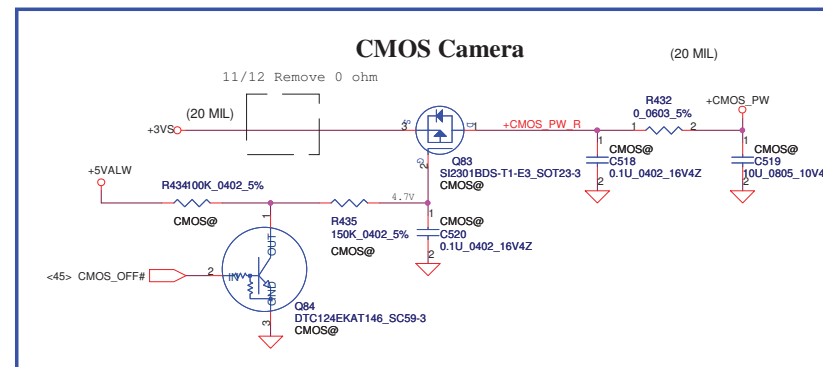
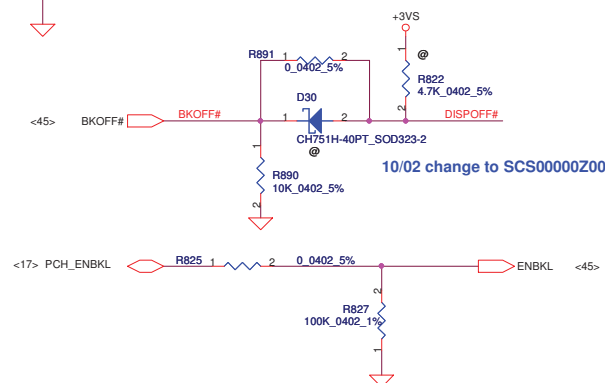
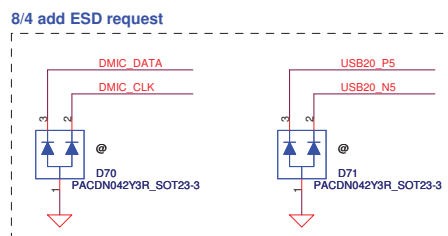
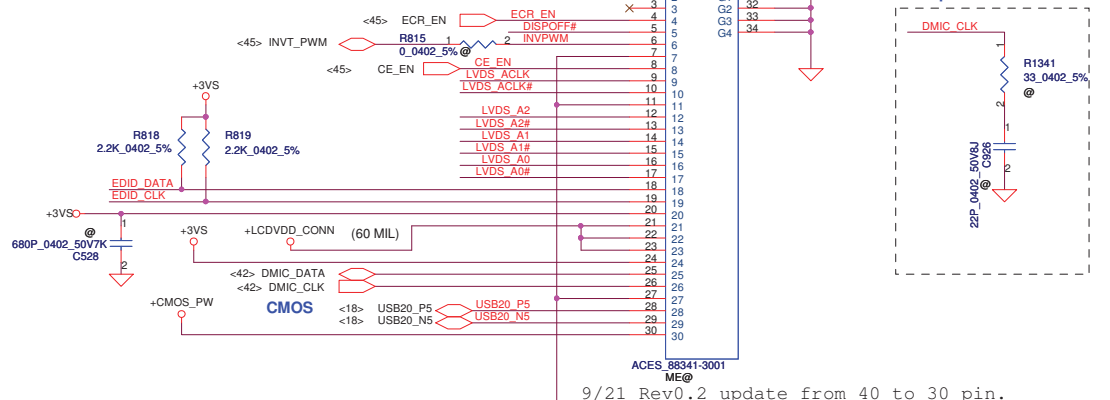
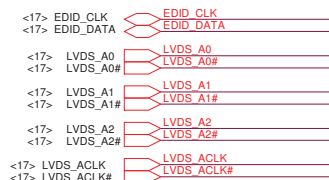
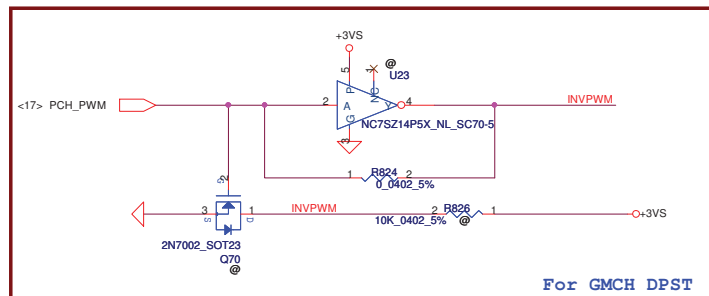
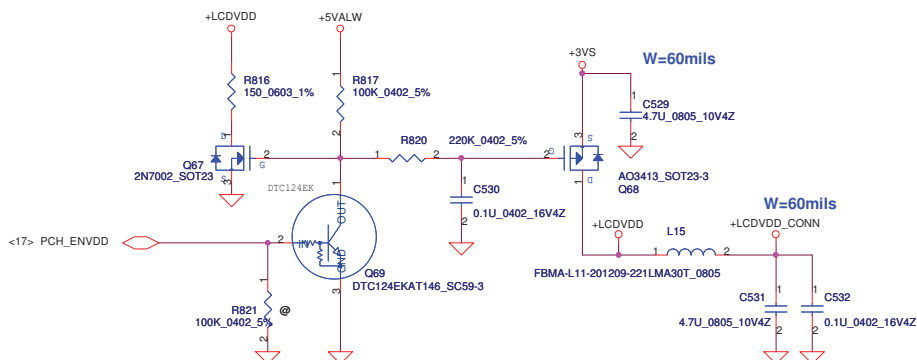
TOP side (under inductor)



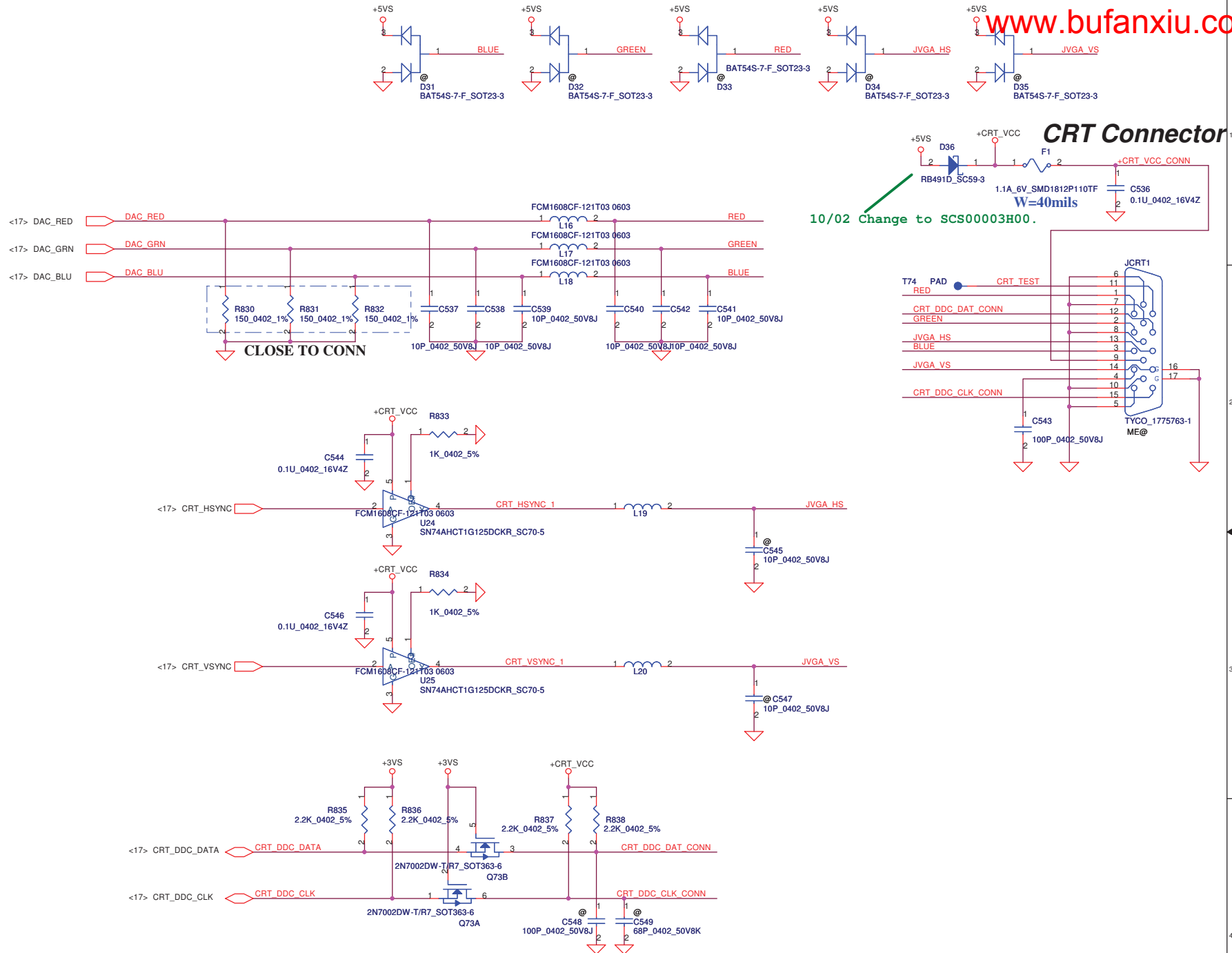
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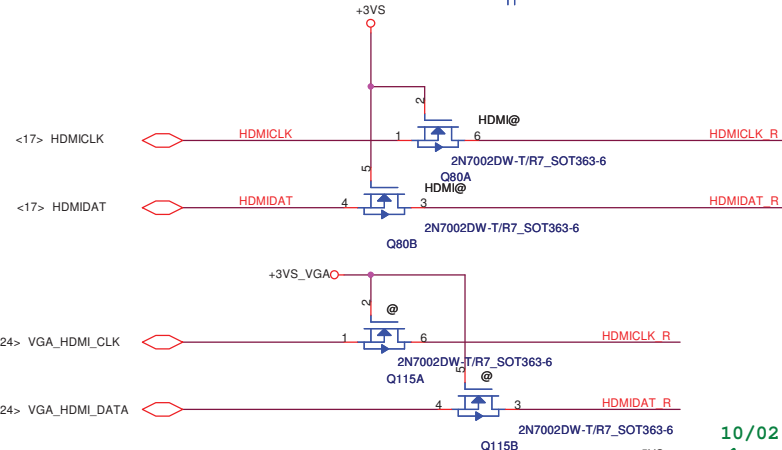
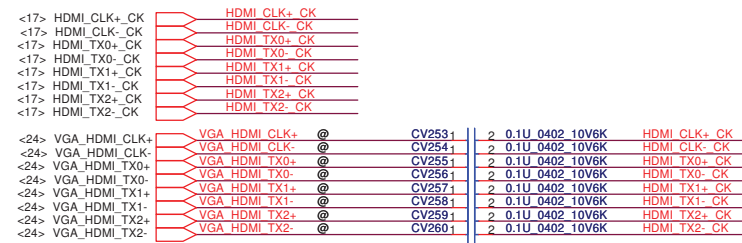
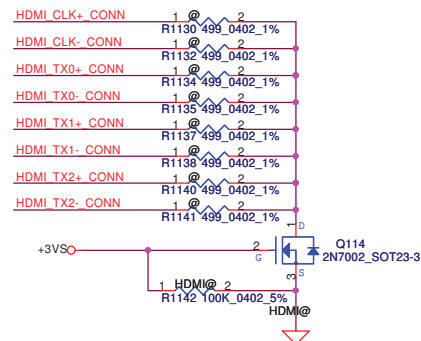
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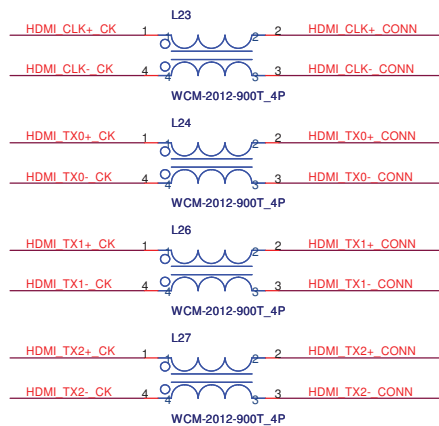
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Issued Date				2010/11/30				Deciphered Date			
				2011/08				2011/08			
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Size B				Document Number				Rev 1.0			
				PIQY0 LA6881P				34 of 63			



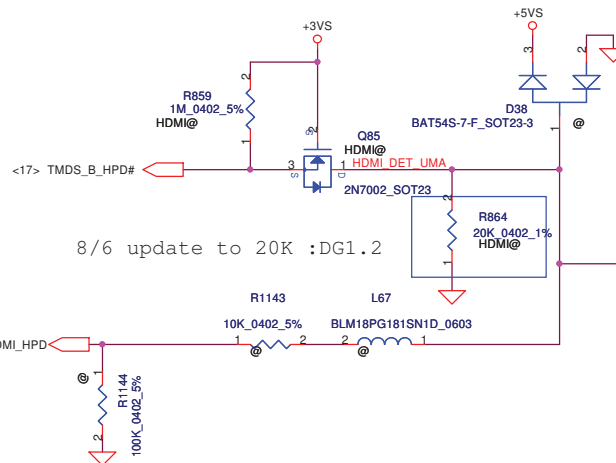
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/11/30	Deciphered Date	2011/08	Title	
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				Custom	PIQY0 LA6881P
				Date	Wednesday, January 05, 2011
				Sheet	35 of 63
				Rev	1.0



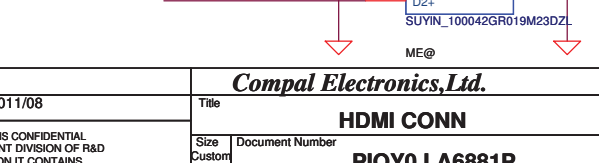
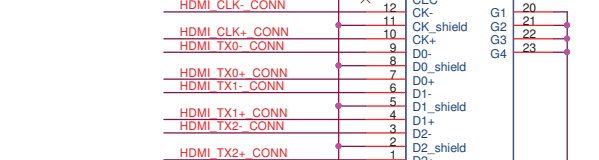
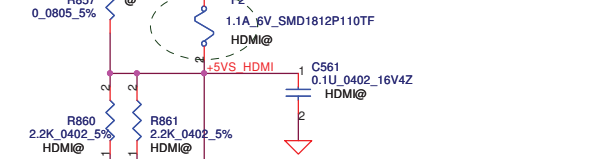
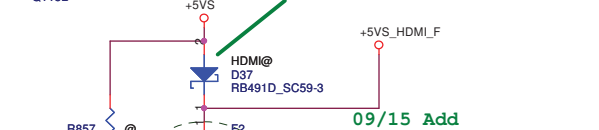
DVT, Change to SM070000I00 for EMI request.



HDMI CLK+ CK	R855	1	@	2	0	0402	5%	HDMI CLK+ CONN
HDMI CLK- CK	R856	1	@	2	0	0402	5%	HDMI CLK- CONN
HDMI TX0+ CK	R867	1	@	2	0	0402	5%	HDMI TX0+ CONN
HDMI TX0- CK	R868	1	@	2	0	0402	5%	HDMI TX0- CONN
HDMI TX1+ CK	R869	1	@	2	0	0402	5%	HDMI TX1+ CONN
HDMI TX1- CK	R870	1	@	2	0	0402	5%	HDMI TX1- CONN
HDMI TX2+ CK	R871	1	@	2	0	0402	5%	HDMI TX2+ CONN
HDMI TX2- CK	R872	1	@	2	0	0402	5%	HDMI TX2- CONN



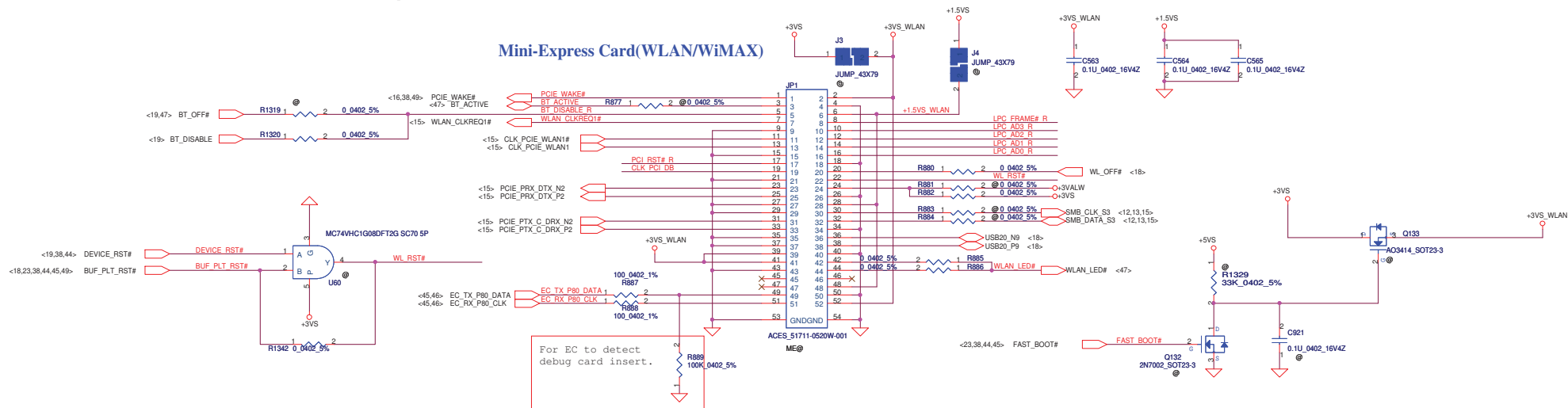
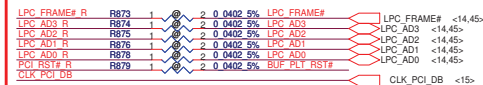
10/02 Change to SCS00003H00.



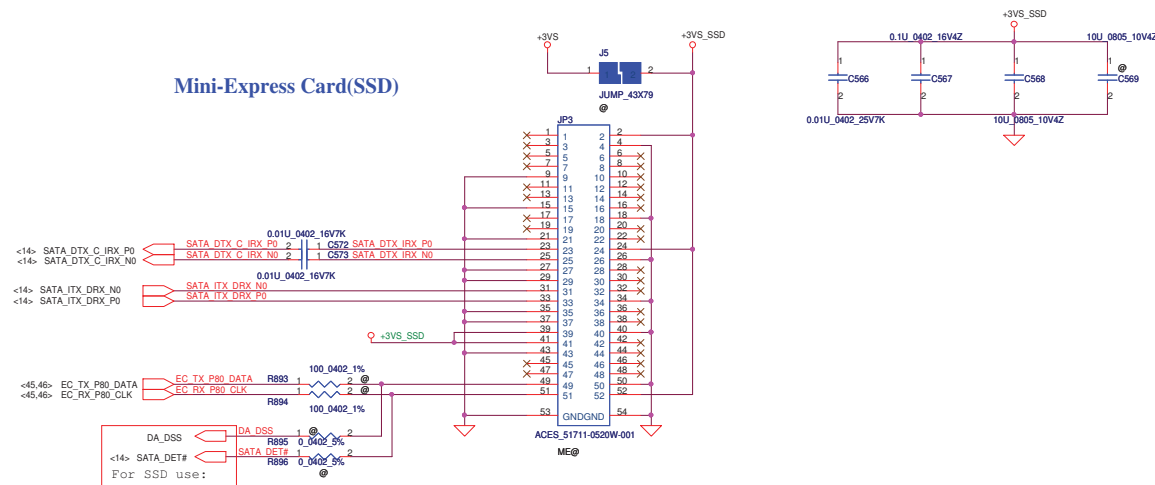
Security Classification				Compal Secret Data				Compal Electronics, Ltd.			
Issued Date				2010/11/30				Deciphered Date			
2010/11/30				2011/08				Title			
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								Document Number			
								PIQY0 LA6881P			
								Date: Wednesday, January 05, 2011			
								Sheet 36 of 63			

# Mini-Express Card for WLAN/WiMAX(Half) Mini-Express Card for SSD(Full)

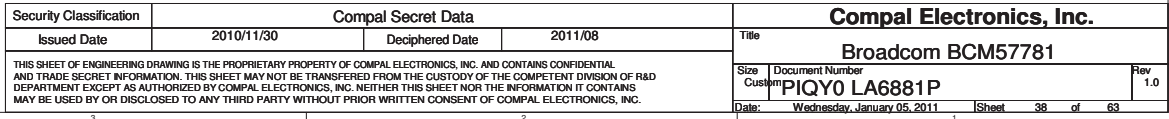
Reserve for SW mini-pcie debug card.  
Series resistors closed to KBC side.

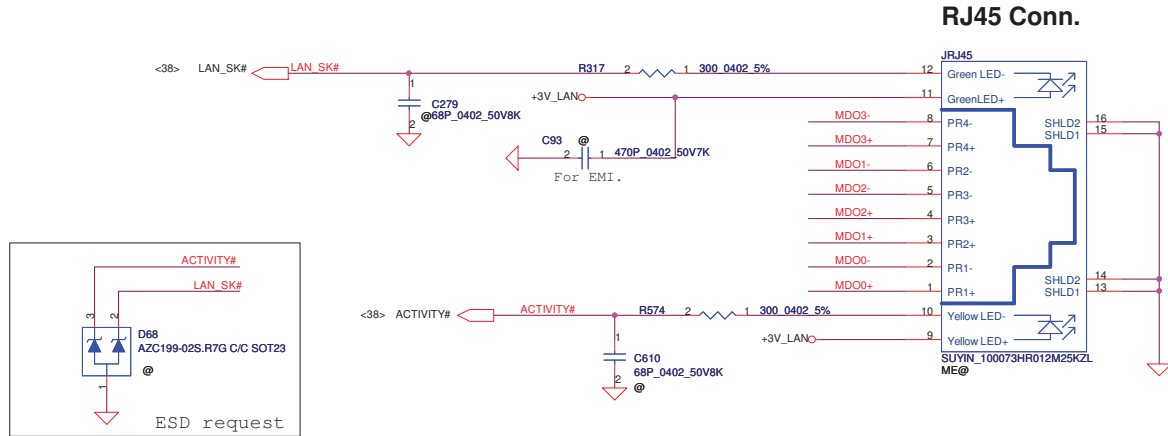
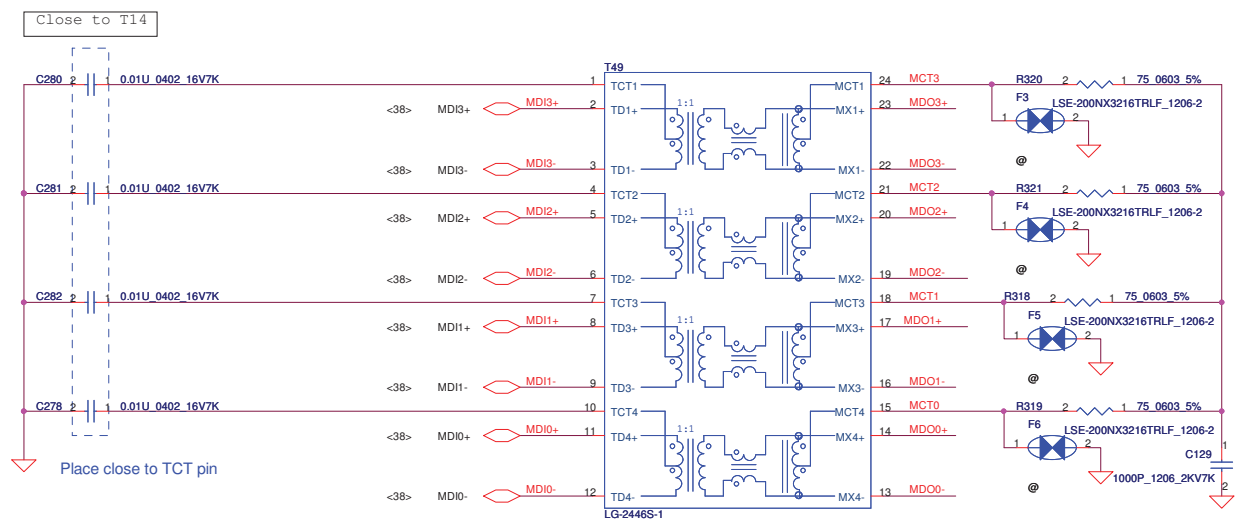


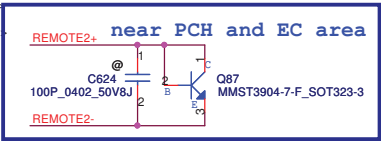
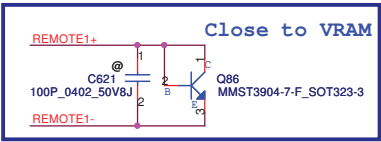
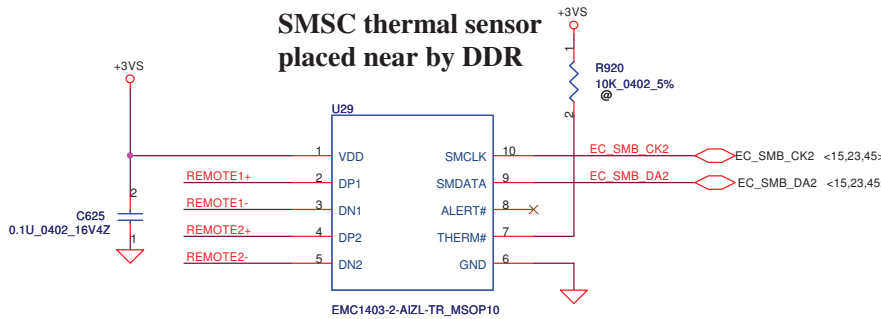
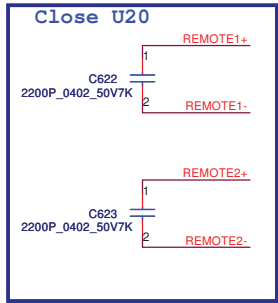
SSD Active:0.22W(0.06A)



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Issued Date	2010/11/30	Deciphered Date	2011/08	Title
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Size	Document Number	PIQY0 LA6881P		Rev 1.0
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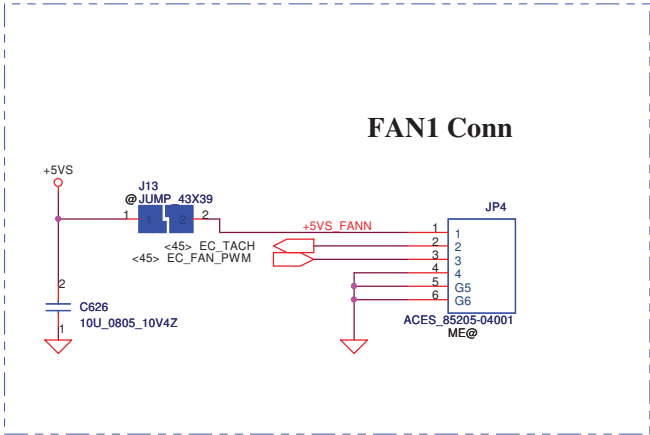
Address 1001\_101xb

8/02 Change PN to SA000046C00, Fintek.

REMOTE1,2+/-:

Trace width/space:10/10 mil

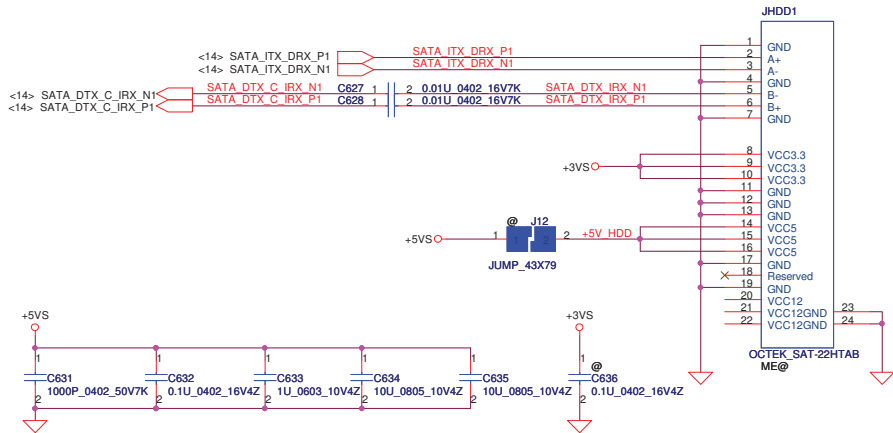
Trace length:<8"



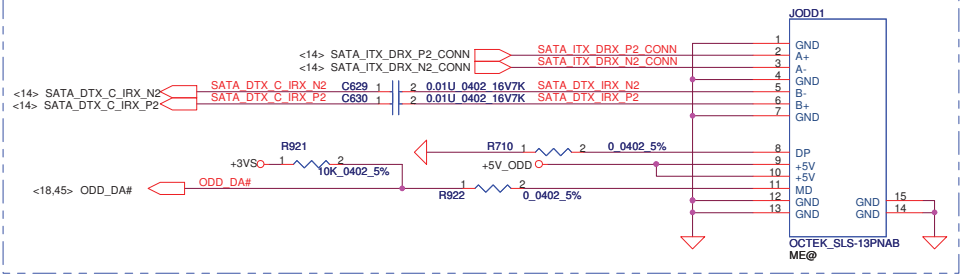
Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
Issued Date	2010/11/30	Deciphered Date	2011/08	Title	EMC1403_ Thermal sensor/FAN
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				Date: Wednesday, January 05, 2011	Sheet 40 of 63



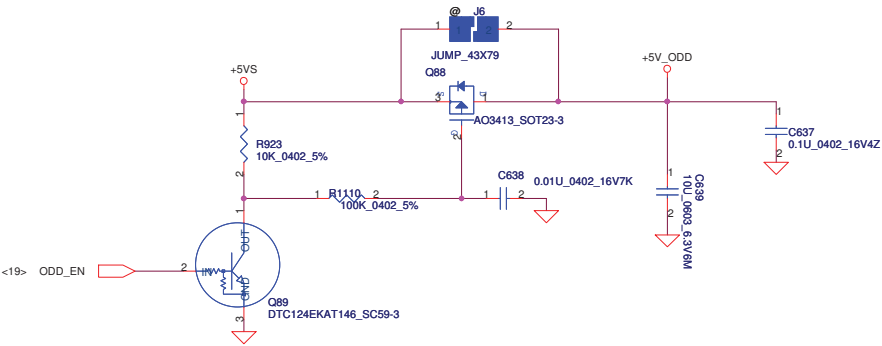
SATA HDD Conn.



SATA ODD Conn.



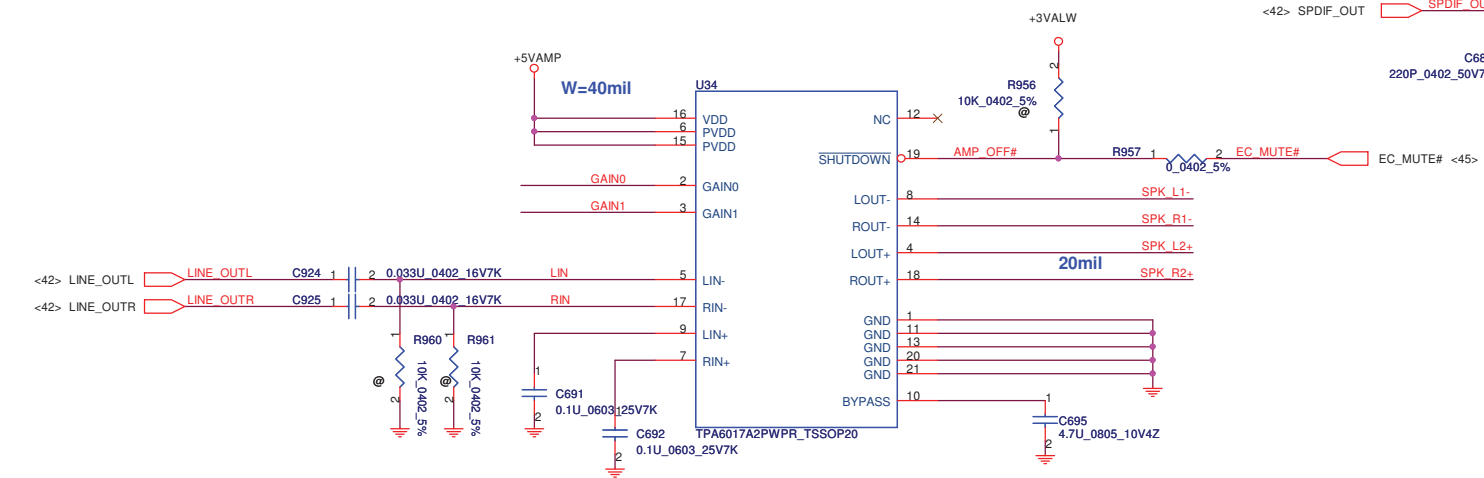
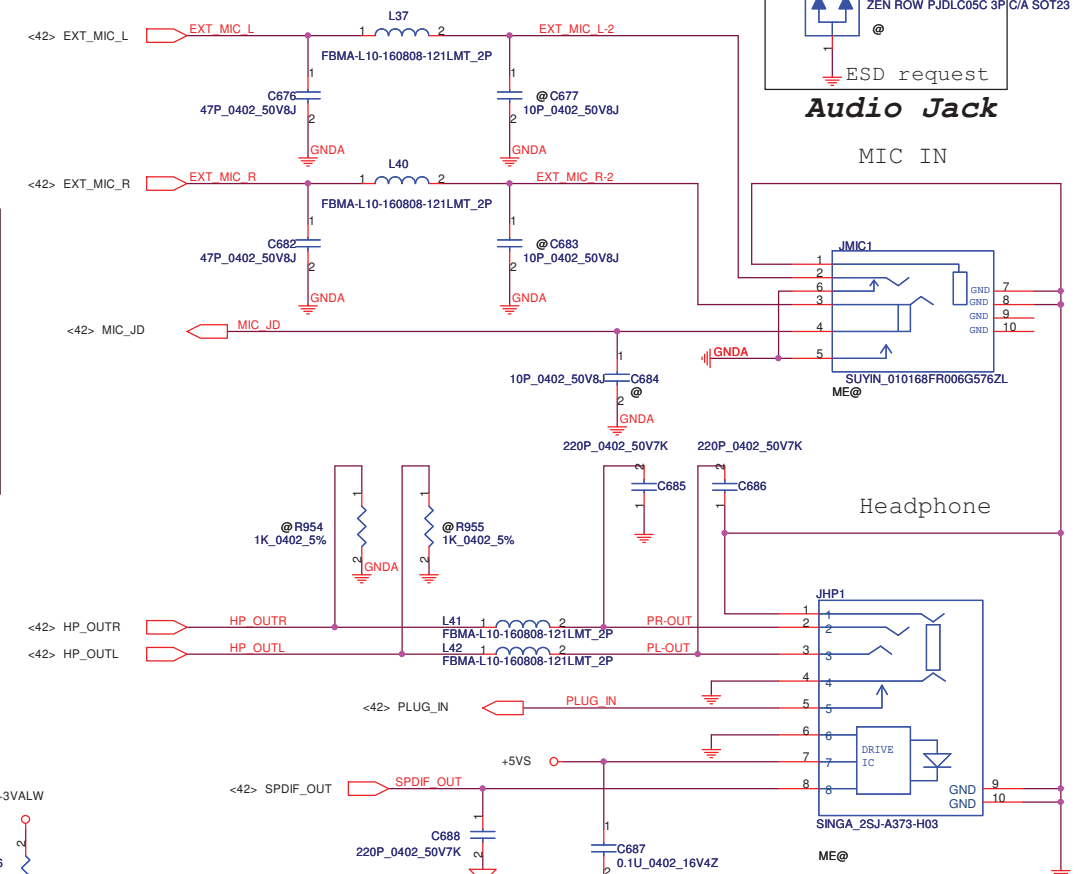
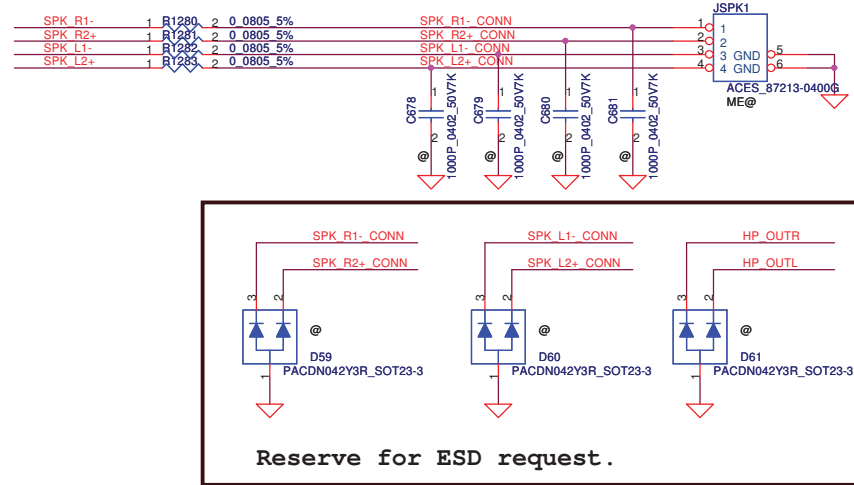
ODD Power Control



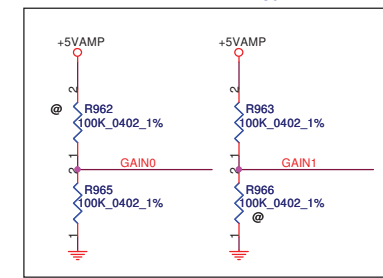
Security Classification	Compal Secret Data			Title	
Issued Date	2010/11/30	Deciphered Date	2011/08	HDD/ODD Connector	
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wide 20MIL



GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

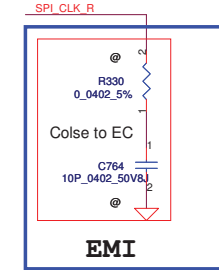






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Issued Date	2010/11/30	Deciphered Date	2011/08	Title <b>BIOS &amp; EC I/O Port</b>		
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				Date: Wednesday, January 05, 2011	ISheet 45 of 63	



[illegible]

### BT MODULE CONN

BT MODULE CONN

5V VALV

BT@

R1022 100K\_0402\_5%

R1025 100K\_0402\_5%

C775 0.1U\_0402\_16V4Z

Q92 DTC124EKAT146\_SC59-3 BT@

Q94 DTC124EKAT146\_SC59-3

BT LED#

Q93 AO3413\_SOT23-3

30mils

0.1U\_0402\_16V4Z

C776 BT@

JP8

1 2 3 4 5 6 7 8

ACES\_87213-0600G ME@

<19,37> BT\_OFF#

<18> USB20\_P13

<18> USB20\_N13

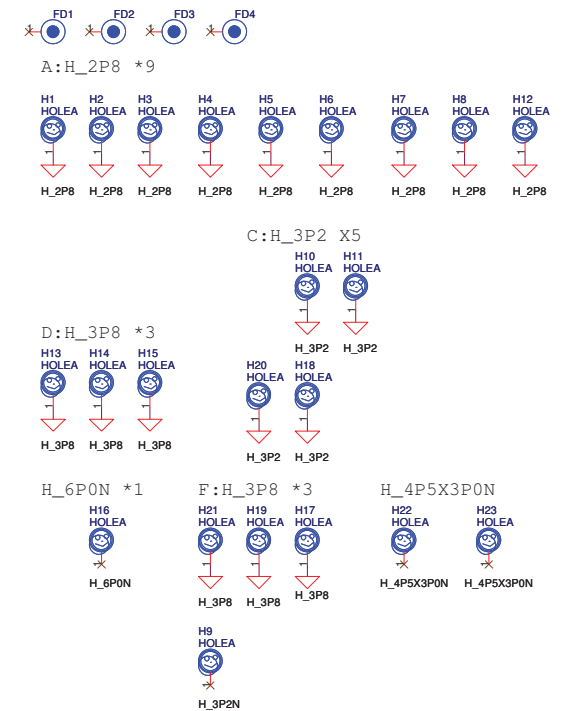
<37> BT\_ACTIVE

USB20\_P13

USB20\_N13

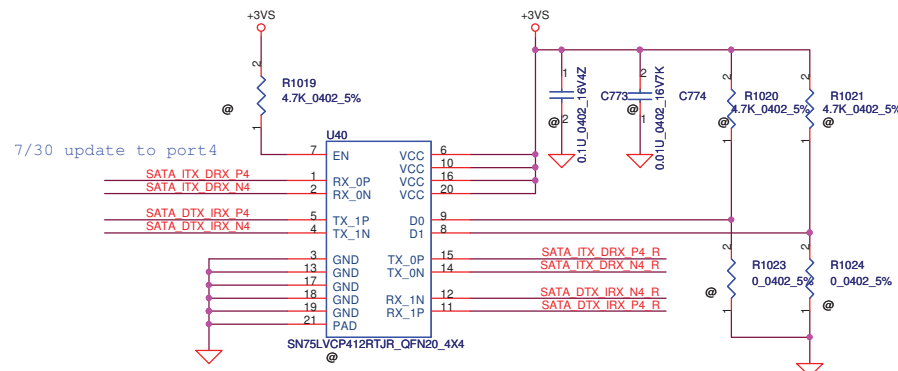
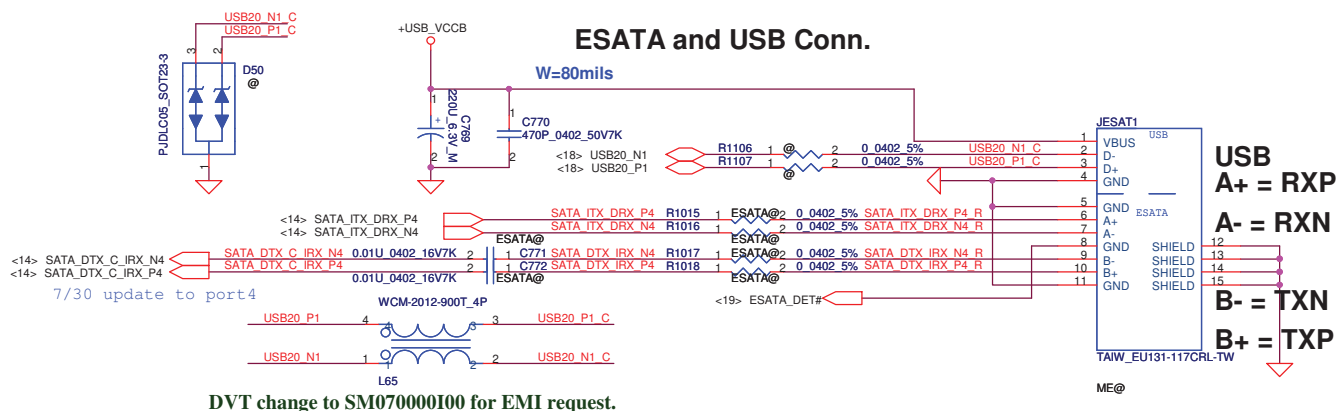
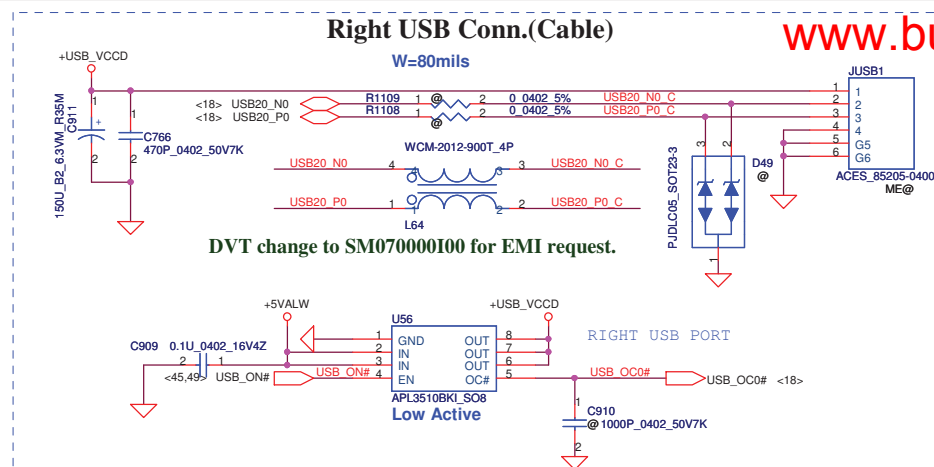
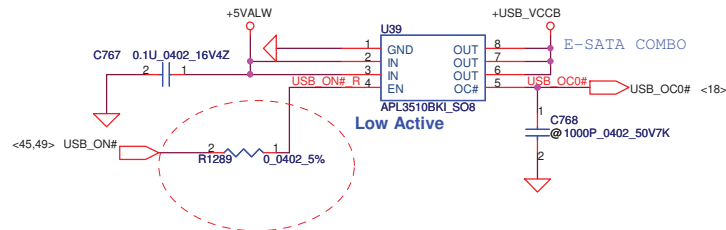
BTON\_LED

BT\_ACTIVE

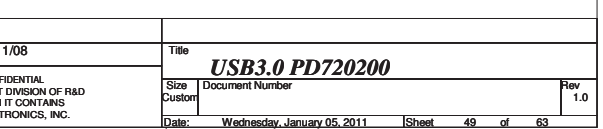
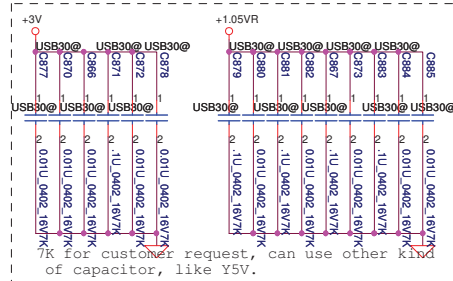


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Issued Date	2010/11/30	Deciphered Date	2011/08	<b>LED/EC SPI ROM/BT</b>					
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						Size	Document Number			PIQY0 LA6881P		Rev	1.0
						Custom							
						Date:	Wednesday, January 05, 2011		Sheet	48	of	63	



Title			
<b>USB3.0 PD720200</b>			
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Date:	Wednesday, January 05, 2011	Sheet	49 of 63

**Power Button**

SMT1-05\_4P

**TOP Side**

**Bottom Side**

J7

1 2

SHORT PADS @

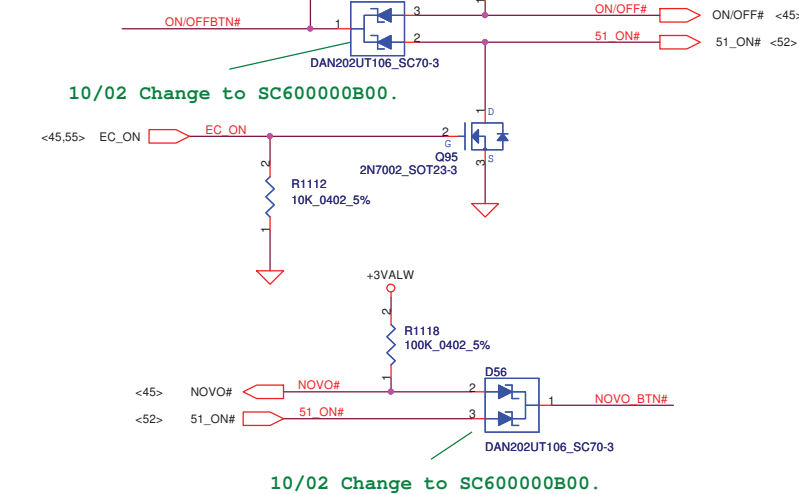


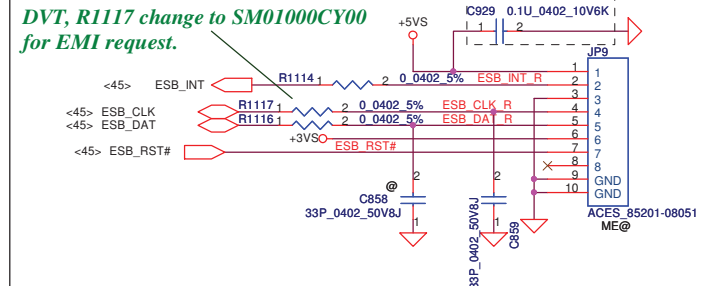
Diagram illustrating the connection of the JP13 header to the board components:

- 5VSW and 5VS power sources are connected to pins 1 and 2 of JP13.
- Control signals (CAPS\_LED#, NUM\_LED#, HDD\_LED#, NOVO\_BTN#, ON/OFFBTN#, PWR\_LED#) are connected to pins 3 through 8 of JP13.
- Ground connections are shown for pins 9, 10, 11, and 12.
- The ACES\_87151-1207G component is connected to pin 13.
- The ME@ connector is connected to pin 13.
- The D54 component (PJSOT24C 3P C/A SOT-23) is connected to pins 13 and 14.
- The text "9/30 remove EC\_SMB" is present in green.

**EMI REQUEST 1ST = SCA00000E00**  
**2ST = SCA00000R00**

www.bufanxiu.com

*DVT, R1117 change to SM01000CY00  
for EMI request.*

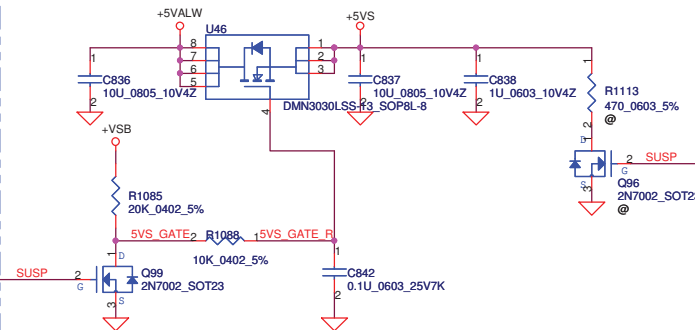


9/30 remove EC\_SMB\_CK2, EC\_SMB\_DA2

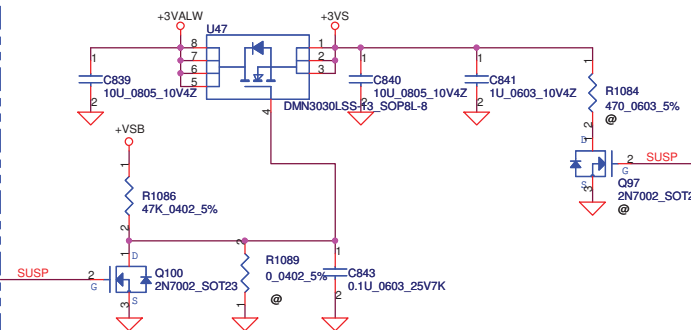
[illegible]

Security Classification		Compal Secret Data		<b>Compal Electronics, Ltd.</b> <b>other IO connector</b>	
Issued Date	2010/11/30	Deciphered Date	2011/08	Title	
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				Custom	1.0
				Document Number <b>PIQY0 LA6881P</b>	
Date: Wednesday, January 05, 2011		Sheet 50 of 63			

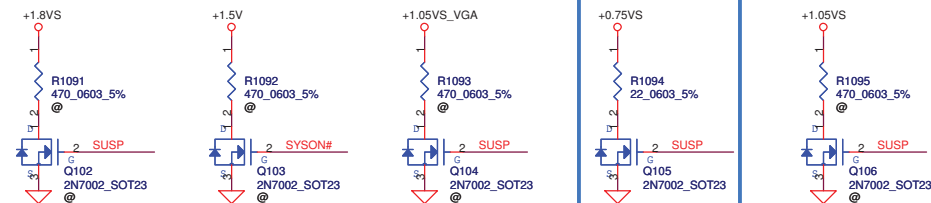
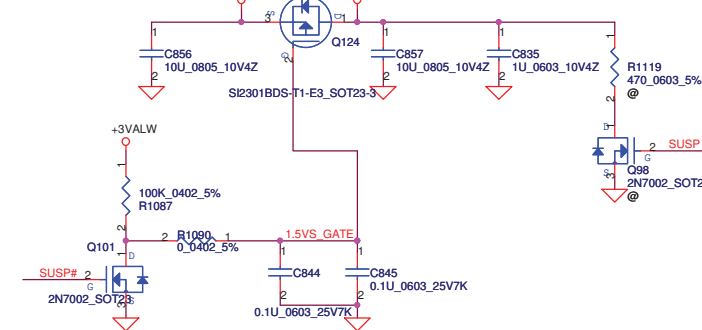
### +5VALW TO +5VS



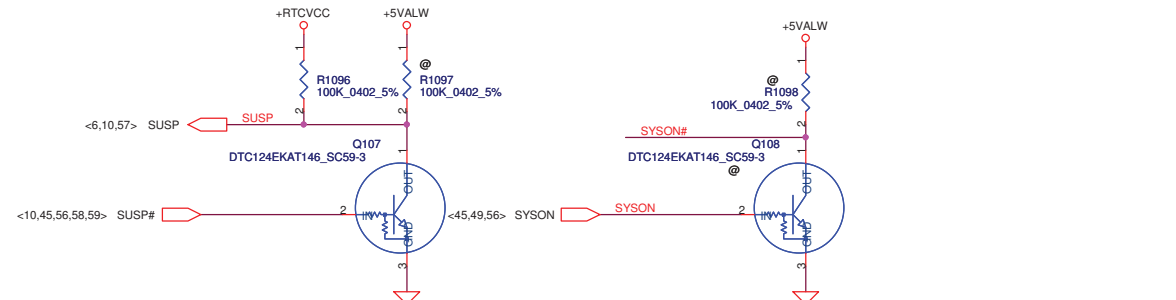
### +3VALW TO +3VS



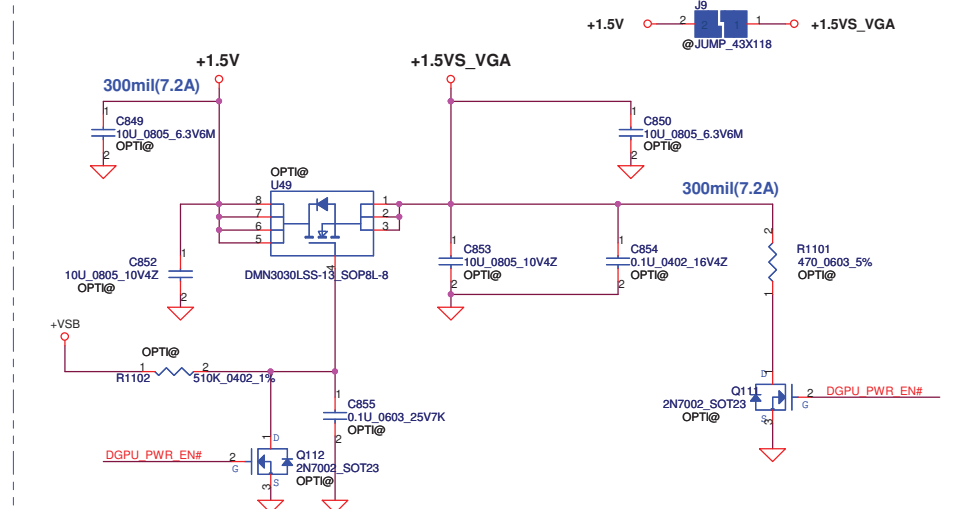
### +1.5V to +1.5VS



For Intel S3 Power Reduction.

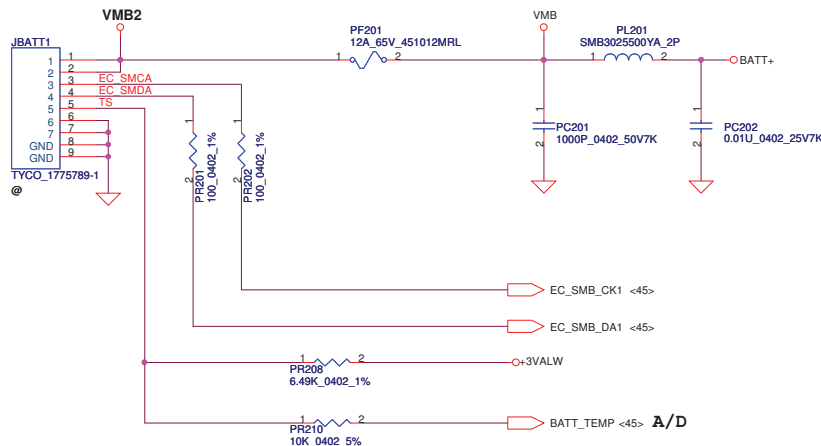


### +1.5V to +1.5VS\_VGA Transfer

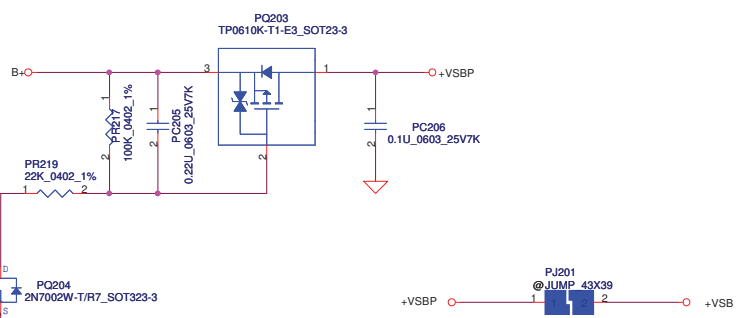
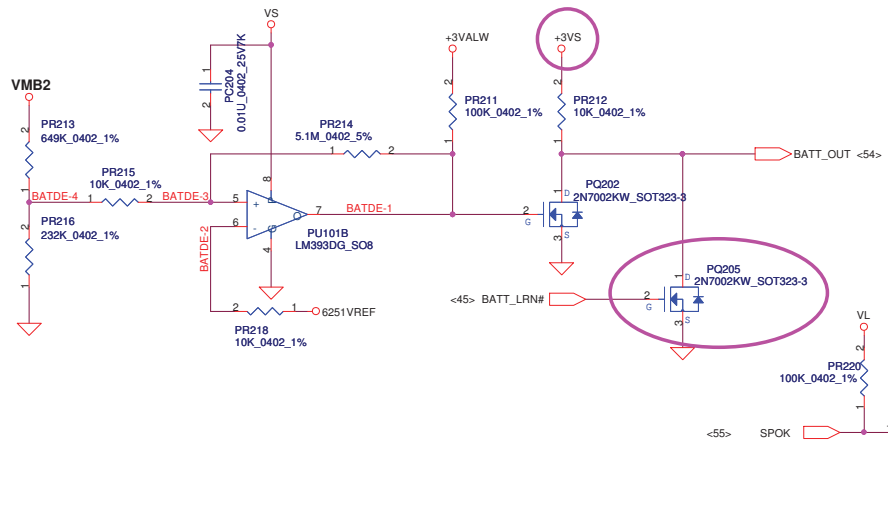
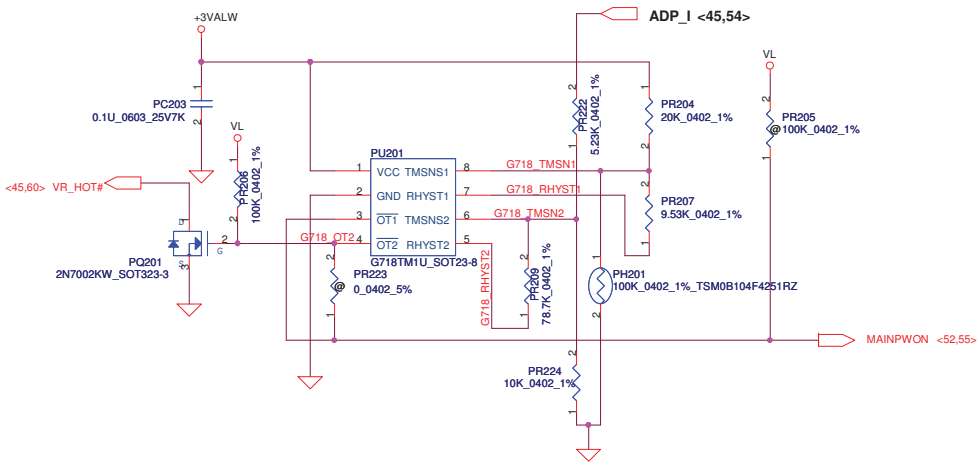


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								Custom		PIQY0 LA6881P		1.0	
								Date		Wednesday, January 05, 2011		Sheet	





PH201 under CPU botten side :  
CPU thermal protection at 95 degree C  
Recovery at 56 degree C



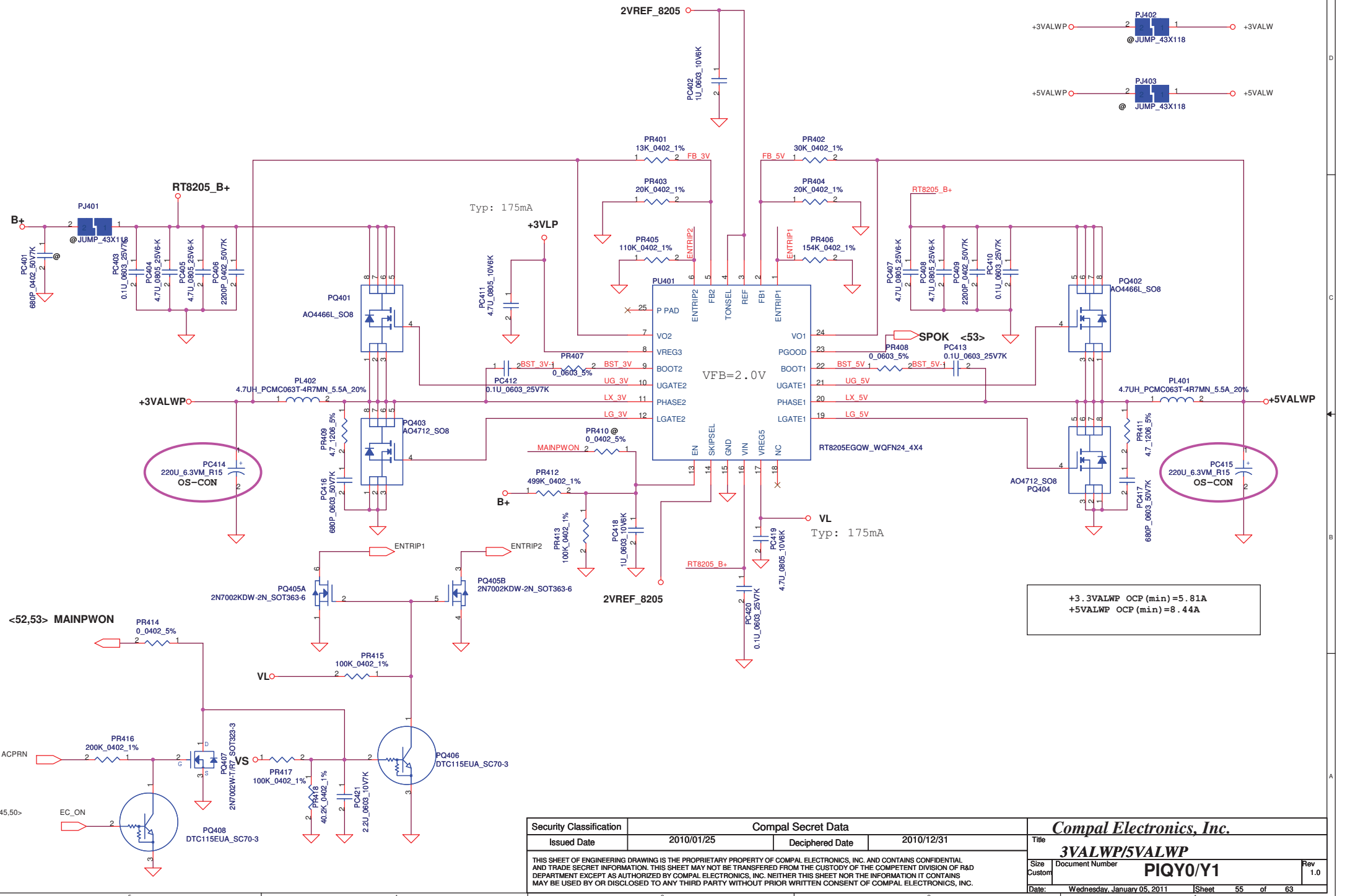
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Issued Date		2010/01/25		Title	
		Deciphered Date		PWR-BATTERY CONN/OTP	
		2010/12/31		Document Number	
				PIQY0/Y1	
				Rev	
				1.0	
				Date: Wednesday, January 05, 2011	
				Sheet 53 of 63	

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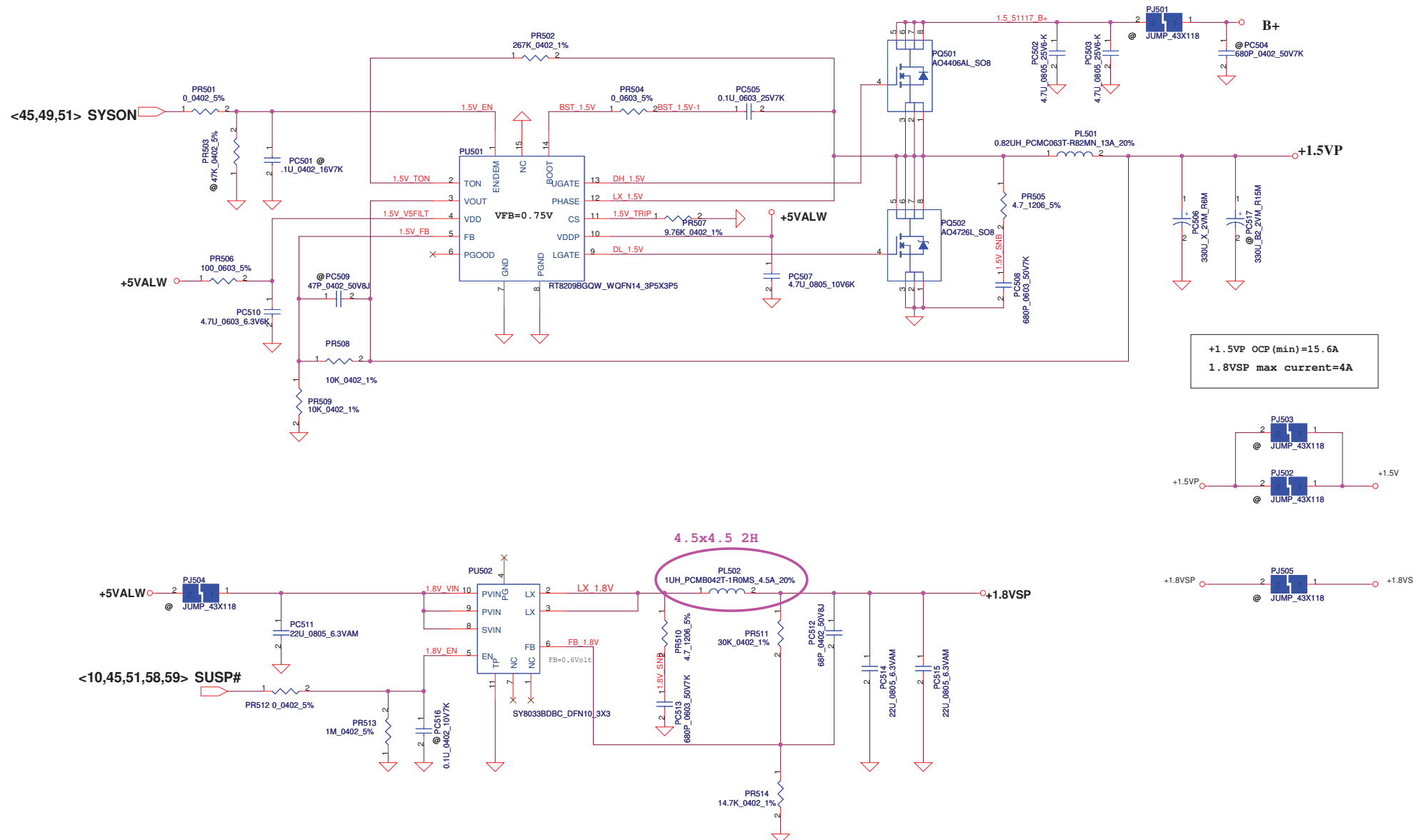




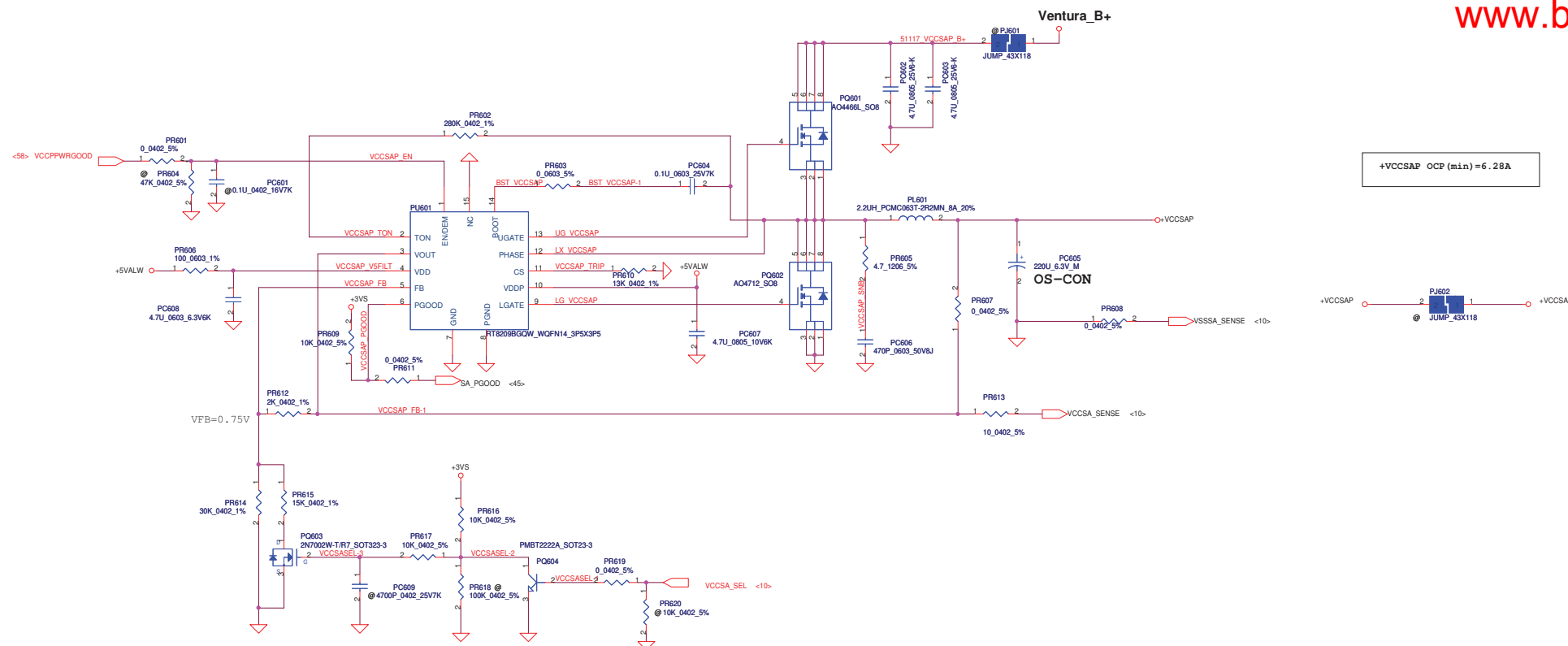
Note:  
Use TPS51125 IC can remove RTC refernece LDO  
Use TPS51427 IC must keep RTC refernece LDO



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Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title	3VALWP/5VALWP
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				Date	Wednesday, January 05, 2011
				Sheet	55 of 63
				Rev	1.0

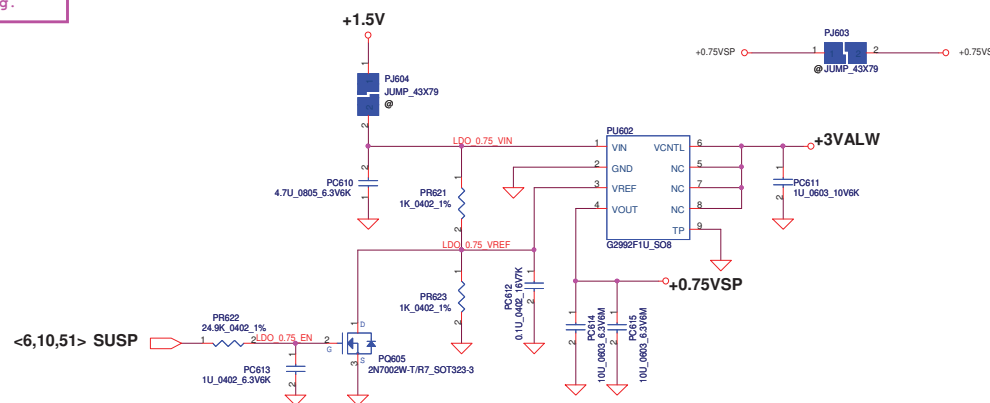


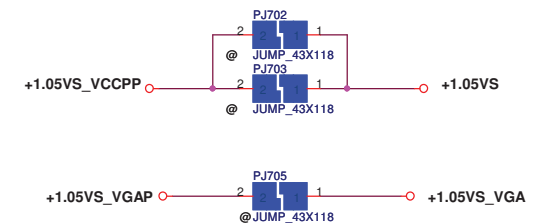
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VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012	Required
0	0	0.9 V	Yes/Yes	
0	1	0.8 V	Yes/Yes	
1	1	0.75V	No/Yes	
1	1	0.65V	No/Yes	

Note: Use VCCSA\_SEL to switch High & Low Level for VID[1] (ie. VCCSA\_SEL) due to the VID[0] is don't care for this setting.





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						Size	Document Number		Rev 1.0
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GS: PR840, PR845, PR847, PR853  
GT/GT1: PR843, PR844, PR846, PR854

N12P-GS

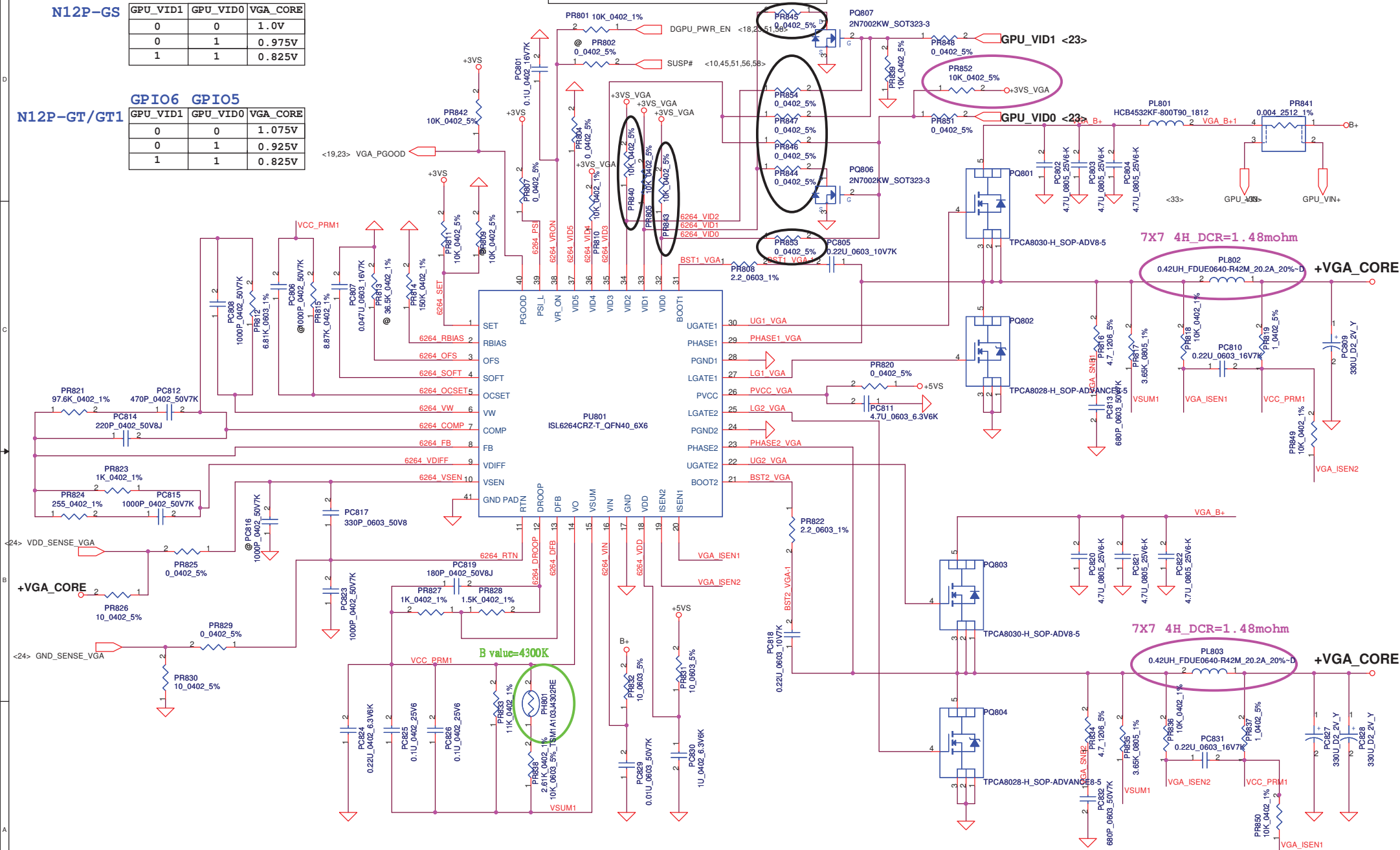
GPIO6 GPIO5

GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.0V
0	1	0.975V
1	1	0.825V

N12P-GT/GT1

GPIO6 GPIO5

GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.075V
0	1	0.925V
1	1	0.825V



Security Classification

Compal Secret Data

Issued Date

2006/12/12

Deciphered Date

2007/12/12

Compal Electronics, Inc.

Title

Power-VGA\_CORE

Size

Document Number

PIQY0/Y1

Rev

1.0

Date:

Wednesday, January 05, 2011

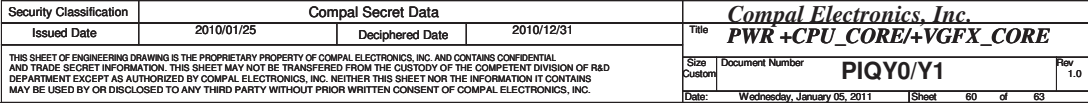
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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					



PIQY0 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
----- EVT TO DVT				
1		P18	Reserve R297	Reserve pull down for PCH GP1053.
2		P18	Exchange SATA port0 & port1	For fast boot function.
3		P50	Change KB light control circuit	Change KB light control from PWM to on/off.
			Delete U55, C908, R1233, R1235, R1236, 1238, R1230, R1231, Q121	
4		P36	Add F2 (poly-fuse)	For HDMI port diode protection.
5		P19	Stuff R303, unstuff R340	Change ESATA_DET# to GP101.
6		P49	Stuff R1068, reserve R1326, Q130	Reserve USB3.0 power swith control inverter circuit.
7		P48	Add R1327	For CHG_ON# pull down.
8		P45	Stuff R996, R139, C815, unstuff R1000, C732, C733, Y5	Change EC CLK from crystal to SUSCLK.
9		P37	Add U60, Q132, C921, R1329, Q133, R1328	Add WLAN power switch circuit
10		P34	Modify JLVDS1	Modify connector from 40pin to 30pin.
11		P09	Add C922	Add C922 to place at CPU sdie.
12		P21	Add R1330	Add for INTVREN control
13		P41	Modify C639	Modify type from 0805 to 0603
14		P45	Modify TP_LED#, PCH_DPWROK and LED_KB_PWM link	Change LED_KB_PWM to U36. pin26 GP1012.
15		P18	Delete EN_CARD_PW#, EN_WOL#	Add FAST_BOOT# to replace EN_CARD_PW# and EN_WOL#
16		P48		Remove USB charger function
17		P42	Change C660, C661 from 3300p to 0.1u	For 100Hz High Pass filter
18		P43	Replace R958, R959 to C924, C925 0.033u	For 100Hz High Pass filter
19		P14	Add one more SPI-ROM circuit	For dual BIOS function
20		P50	Remove EC_SMB_CK2, EC_SMB_DA2 link to JP13	Remove light sensor function
21		P14	Add Q134, R1345, R1346	Add for Fast boot SPI ROM selection by EC.
22		P34	Add R1341, C926	Added for EMI request
23		P37, P44	Add R1342, R1343	Added for WLAN and CARD reader Reset signal.
24		P19	Add R1344	Added for VENTURA detection.
----- DVT TO PVT				
1		P10	Add R1347, Change R56 to 20K,	Modify S3 1.5V reduction sequence.
2		P45	Add Q135	Modify PROCHOT control circuit.
			Modify R980 link to +5VALW	Change USB_ON PU power rail
----- PVT TO SVT				
1		P23, P45	FAST_BOOT#	Link FAST_BOOT# to VGA GP1012
2		P50	Add C929	EMI Request
2		P14	Add R1348	INTEL Design Guide update

