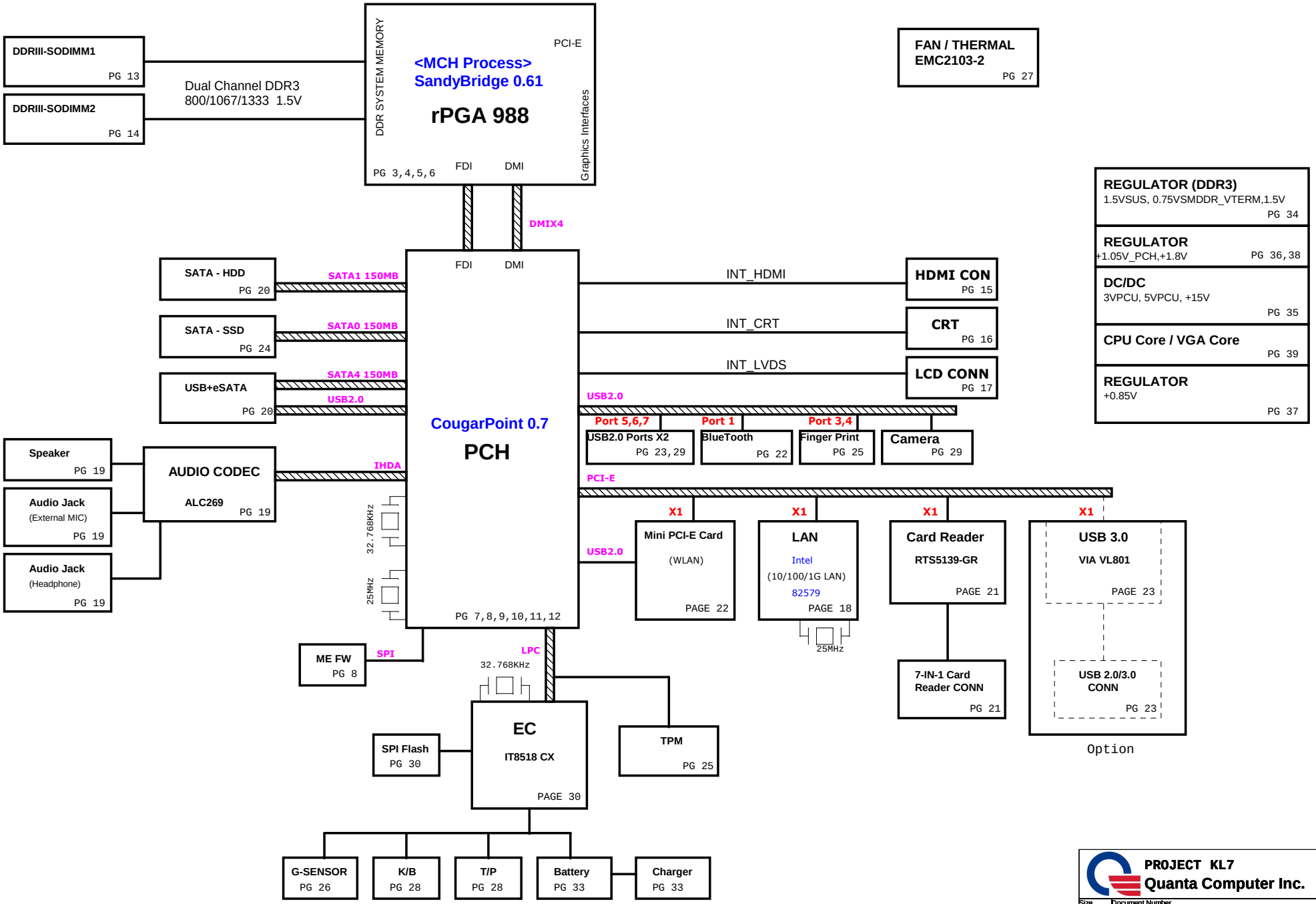
KL7 Intel Huron River Platform (UMA)



PROJECT KL7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> BLOCK DIAGRAM	0D

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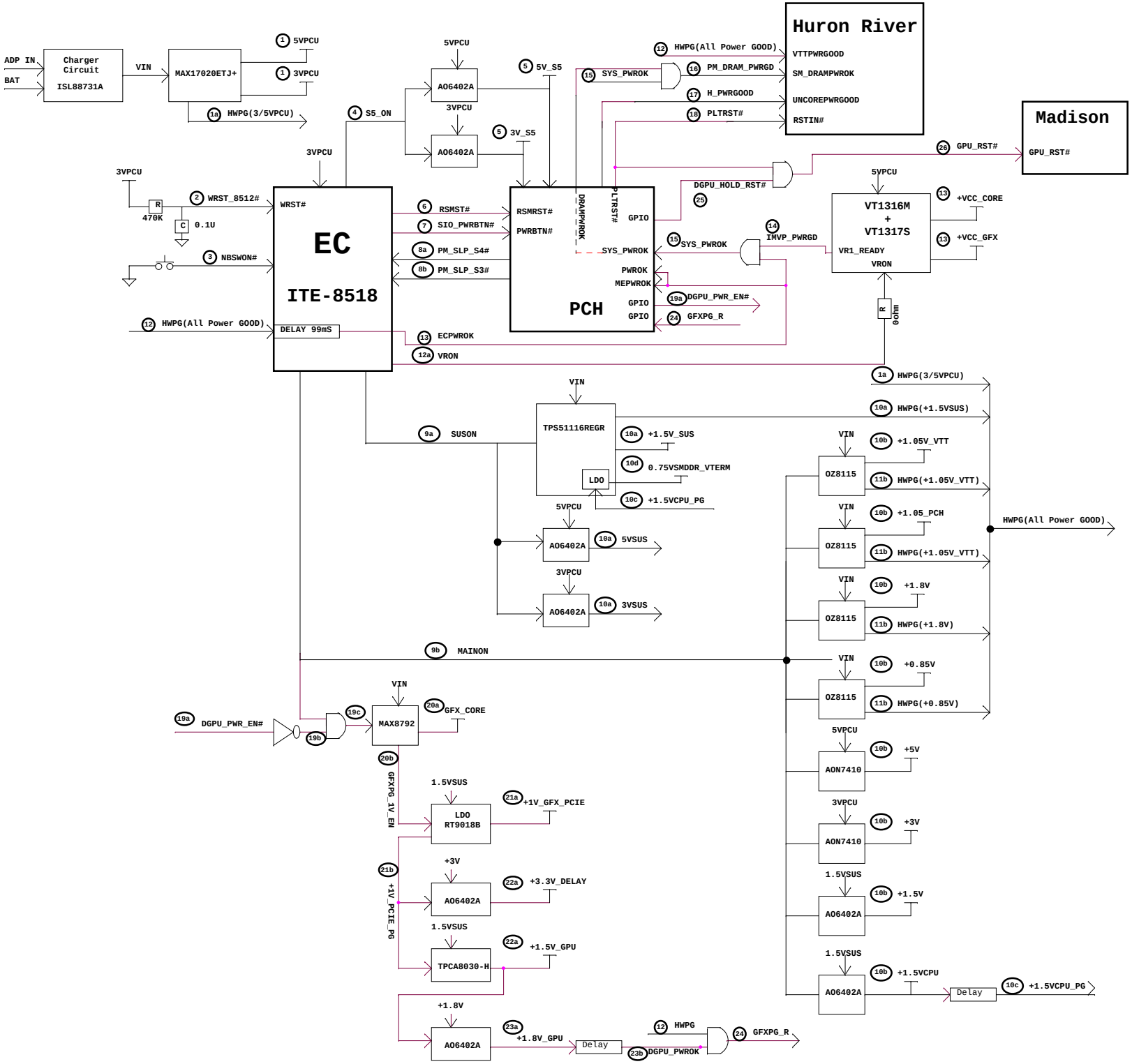

PROJECT KL7
Quanta Computer Inc.

Size	Document Number	Rev
A2	<Doc> POWER SEQUENCE DIAGRAM	0D

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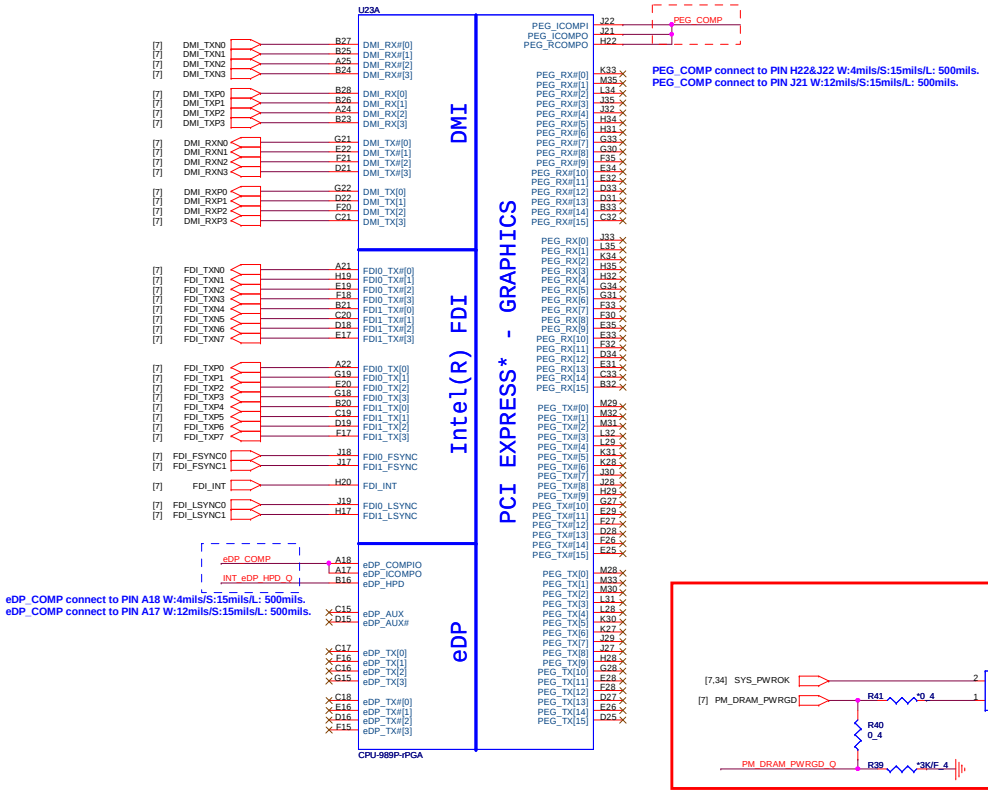
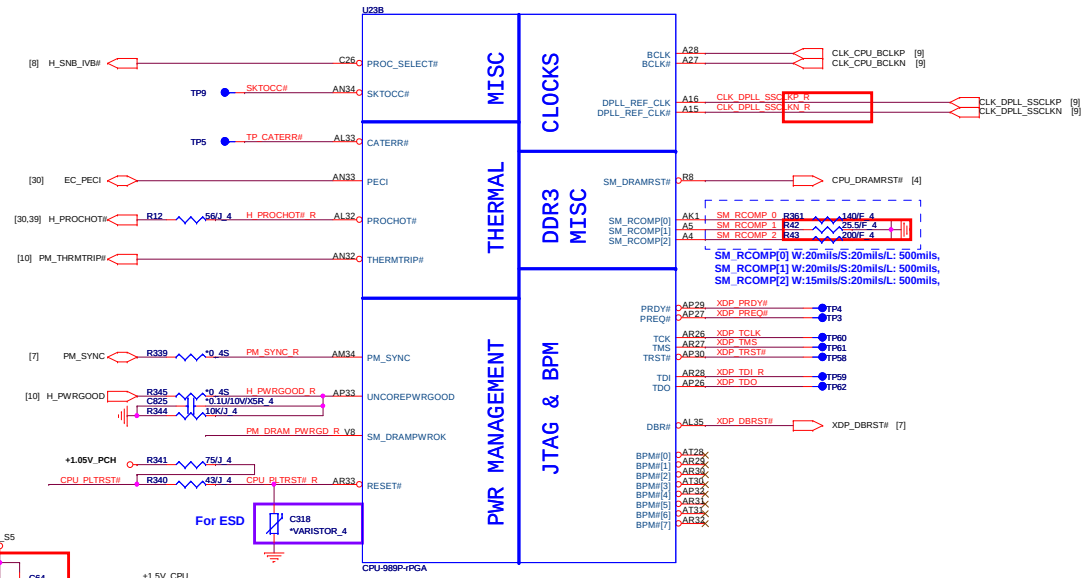
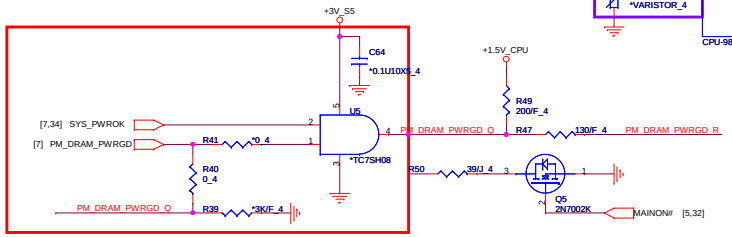
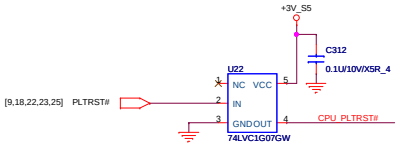
Sandy Bridge Processor (DMI,PEG,FDI)



Sandy Bridge Processor (CLK,MISC,JTAG)







DP & PEG Compensation

+1.05V_PCH — R353 — 24.9/F_4 — PEG_COMP

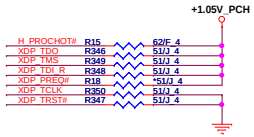
PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils
typical impedance = 14.5 mohms

+1.05V_PCH — R355 — 10K_4 — INT_eDP_HPD_Q

+1.05V_PCH — R354 — 24.9/F_4 — eDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Processor pull-up(CPU)



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Quanta Computer Inc.

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Custom	<Doc> BLOCK DIAGRAM	0D

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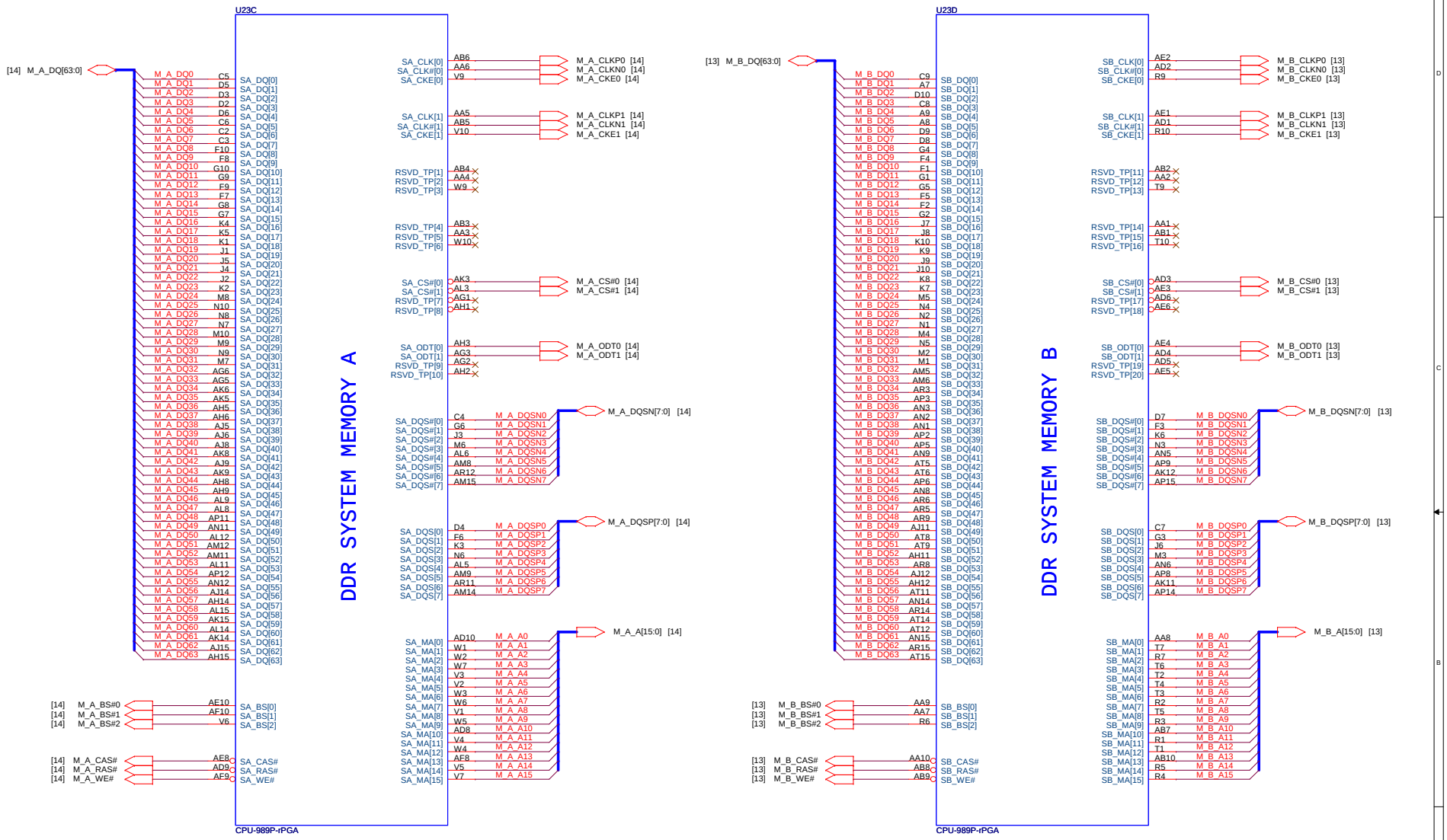
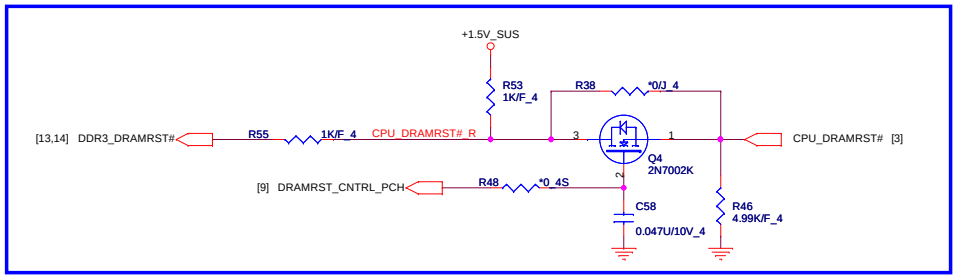
Sandy Bridge Processor (DDR3)

[5,11,13,14,32,34] +1.5V_SUS

04





PROJECT KL7

Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> SNB 2/4(DDR3 I/F)	0D

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Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

[32,39] +VCC_GFX
[3] +1.5V_CPU
[32,37] +0.85V
[4,11,13,14,32,34] +1.5V_SUS
[3,7,8,9,11,23,32,38] +1.05V_PCH
[8,11,32,36] +1.8V
[32,39] +VCC_CORE
[13,14,34] SMDDR_VREF

CPU Core Power

SNB 45W:55A
22uF x 32
22uF x 3 (Non-stuff)

+VCC_CORE

C331 C330 C329 C29 (22U/6.3V_8)
C328 C21 C334 C323 (22U/6.3V_8)
C23 C22 C25 C314 (22U/6.3V_8)
C335 C336 C315 C319 (22U/6.3V_8)
C24 C340 C341 C322 (22U/6.3V_8)
C31 C321 C30 C20 (22U/6.3V_8)
C14 C15 C317 C320 (22U/6.3V_8)
C12 C316 C16 C17 (22U/6.3V_8)

Reserved
C311 C10 C313 (*22U/6.3V_8)

U23F — **POWER**

CORE SUPPLY: AG35, AG34, AG33, AG32, AG31, AG30, AG29, AG28, AG27, AG26, AF35, AF34, AF33, AF32, AF31, AF30, AF29, AF28, AF27, AF26, AD35, AD34, AD33, AD32, AD31, AD30, AD29, AD28, AD27, AD26, AC35, AC34, AC33, AC32, AC31, AC30, AC29, AC28, AC27, AC26, AA35, AA34, AA33, AA32, AA31, AA30, AA29, AA28, AA27, AA26, Y35, Y34, Y33, Y32, Y31, Y30, Y29, Y28, Y27, Y26, V35, V34, V33, V32, V31, V30, V29, V28, V27, V26, U35, U34, U33, U32, U31, U30, U29, U28, U27, U26, R35, R34, R33, R32, R31, R30, R29, R28, R27, R26, P35, P34, P33, P32, P31, P30, P29, P28, P27, P26

PEG AND DDR: VCC1, VCC2, VCC3, VCC4, VCC5, VCC6, VCC7, VCC8, VCC9, VCC10, VCC11, VCC12, VCC13, VCC14, VCC15, VCC16, VCC17, VCC18, VCC19, VCC20, VCC21, VCC22, VCC23, VCC24, VCC25, VCC26, VCC27, VCC28, VCC29, VCC30, VCC31, VCC32, VCC33, VCC34, VCC35, VCC36, VCC37, VCC38, VCC39, VCC40, VCC41, VCC42, VCC43, VCC44, VCC45, VCC46, VCC47, VCC48, VCC49, VCC50, VCC51, VCC52, VCC53, VCC54, VCC55, VCC56, VCC57, VCC58, VCC59, VCC60, VCC61, VCC62, VCC63, VCC64, VCC65, VCC66, VCC67, VCC68, VCC69, VCC70, VCC71, VCC72, VCC73, VCC74, VCC75, VCC76, VCC77, VCC78, VCC79, VCC80, VCC81, VCC82, VCC83, VCC84, VCC85, VCC86, VCC87, VCC88, VCC89, VCC90, VCC91, VCC92, VCC93, VCC94, VCC95, VCC96, VCC97, VCC98, VCC99, VCC100

SVID: VIDALERT#, VIDSCLK, VIDSOUT

SENSE LINES: VCC_SENSE, VSS_SENSE, VCCIO_SENSE, VSSIO_SENSE

CPU-989P-rPGA

CPU VTT

SNB 45W:8.5A
22uF x 10
22uF x 6 (Non-stuff)

+1.05V_PCH

VCCIO1 AH13, VCCIO2 AH10, VCCIO3 AG10, VCCIO4 AC10, VCCIO5 Y10, VCCIO6 P10, VCCIO7 L10, VCCIO8 J14, VCCIO9 J13, VCCIO10 J12, VCCIO11 J11, VCCIO12 H14, VCCIO13 H12, VCCIO14 H11, VCCIO15 G14, VCCIO16 G13, VCCIO17 G12, VCCIO18 F14, VCCIO19 F13, VCCIO20 E12, VCCIO21 F11, VCCIO22 E14, VCCIO23 E12, VCCIO24 E11, VCCIO25 D14, VCCIO26 D13, VCCIO27 D12, VCCIO28 D11, VCCIO29 C14, VCCIO30 C13, VCCIO31 C12, VCCIO32 C11, VCCIO33 B14, VCCIO34 B12, VCCIO35 A14, VCCIO36 A13, VCCIO37 A12, VCCIO38 A11, VCCIO39, VCCIO40 J23

C42 C45 C43 C41 C40 C39 (22U/6.3V_8; 10U/6.3V_6)
C349 C350 C351 C46 C38 C44 (*22U/6.3V_8; 10U/6.3V_6)

22uF (Reserved)
C345 C346 C347 C348 (*22U/6.3V_8)

+1.05V_VTT_40 — R352 *0_4S — +1.05V_PCH

H_CPU_SVIDALRT# AJ29
H_CPU_SVIDCLK AJ30
H_CPU_SVIDDAT AJ28

VCC_SENSE AJ35 — R337 100/J_4 — +VCC_CORE — VCC_SENSE [39]
VSS_SENSE AJ34 — R342 100/J_4 — VSS_SENSE [39]
VCCIO_SENSE B10 — VTT_SENSE [38]
VSSIO_SENSE A10 — TP64

CPU VGT

SNB 45W:22A
22uF x 12
22uF x 4 (Reserved)

+VCC_GFX

C333 C338 C342 C327 (22U/6.3V_8)
C28 C32 C34 C36 (22U/6.3V_8)
C37 C332 C33 C35 (22U/6.3V_8)
C344 C337 C343 C324 (*22U/6.3V_8)

EC12 EC13 EC14 EC15 EC16
68P/50V/COG_4 68P/50V/COG_4 68P/50V/COG_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4

EMI request

U23G — **POWER**

GRAPHICS: AT24, AT23, AT21, AT20, AT18, AT17, AR24, AR23, AR21, AR20, AR18, AR17, AP24, AP23, AP21, AP20, AP18, AP17, AN24, AN23, AN21, AN20, AN18, AN17, AM24, AM23, AM21, AM20, AM18, AM17, AL24, AL23, AL21, AL20, AL18, AL17, AK24, AK23, AK21, AK20, AK18, AK17, AJ24, AJ23, AJ21, AJ20, AJ18, AJ17, AH24, AH23, AH21, AH20, AH18, AH17

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

1.8V RAIL: VCCPLL1 B6, VCCPLL2 A6, VCCPLL3 A2

CPU-989P-rPGA

SENSE LINES: VAXG_SENSE AK35, VSSAXG_SENSE AK34 — TP56, TP57 — R343 100/J_4 — +VCC_GFX — VCC_AXG_SENSE [39] — R338 100/J_4 — VSS_AXG_SENSE [39]

VREF: SM_VREF AL1 — +VDDR_REF_CPU — +VDDR_REF_CPU

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

DDR3 -1.5V RAILS: VDDQ1 AF7, VDDQ2 AF4, VDDQ3 AF1, VDDQ4 AC7, VDDQ5 AC4, VDDQ6 AC1, VDDQ7 V7, VDDQ8 V4, VDDQ9 V1, VDDQ10 U7, VDDQ11 U4, VDDQ12 U1, VDDQ13 P7, VDDQ14 P4, VDDQ15 P1

CPU MCH

SNB 45W: 5A
330uF/6mohm x 1
10uF x 6

+1.5V_CPU

C51 C57 C50 C52 (10U/6.3V_6)
C49 C54 C53 C63 C60 (10U/6.3V_6; *330U/2V_7343; 22U/6.3V_8)

22uF (Reserved)

SA RAIL: VCCSA1 M27, VCCSA2 M26, VCCSA3 L26, VCCSA4 J26, VCCSA5 J25, VCCSA6 J24, VCCSA7 H26, VCCSA8 H25

C27 C26 C325 C326 (10U/6.3V_6; *10U/6.3V_6) — +0.85V

CPU SA

SNB 45W: 6A
330uF/7mohm x 1
10uF x 3

MISC: VCCSA_SENSE H23 — VCCUSA_SENSE [37]
FC_C22 C22 — H_FC_C22 — R27 10K/J_4 — VCCSA_SEL [37]
VCCSA_VID1 C24 — R26 10K/J_4

CPU VCCPL

SNB 45W:3A
330uF/7mohm x 1
10uF x 1
1uF x 2

+1.8V

C355 C354 C356 C361 (10U/6.3V_6; 1U/6.4V_4; *330U/2V_7343)

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK
+1.05V_PCH — Close to VR — R19 54.9/F_4
H_CPU_SVIDCLK — R25 *0_4S — VR_SVID_CLK [39]

Place PU resistor close to CPU
+1.05V_PCH — R22 130/F_4

SVID DATA
+1.05V_PCH — Close to VR — R17 *130/F_4
H_CPU_SVIDDAT — R23 *0_4S — VR_SVID_DATA [39]

Place PU resistor close to CPU
+1.05V_PCH — R16 75/J_4

SVID ALERT
H_CPU_SVIDALRT# — R21 43/J_4 — R14 *0_4S — VR_SVID_ALERT# [39]

+VDDR_REF_CPU
[13,14,34] SMDDR_VREF — R364 *0_8 — Q37 2N7002K — MAINON_15V — R362 100K/J_4

4.5A

+1.5V_SUS — +1.5V_CPU — +1.5V_SUS
C67 C68 C65 C66 (0.1U/10V_4)
3/26 DB add for Intel. Placement close to CPU.
[32] MAINON_15V — C62 *470P/50V_4 — Q7 AO4496 — R54 220/J_8
[3,32] MAINON# — Q8 DMN601K-7

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Custom	<Doc> SNB 3/4(POWER)	0D

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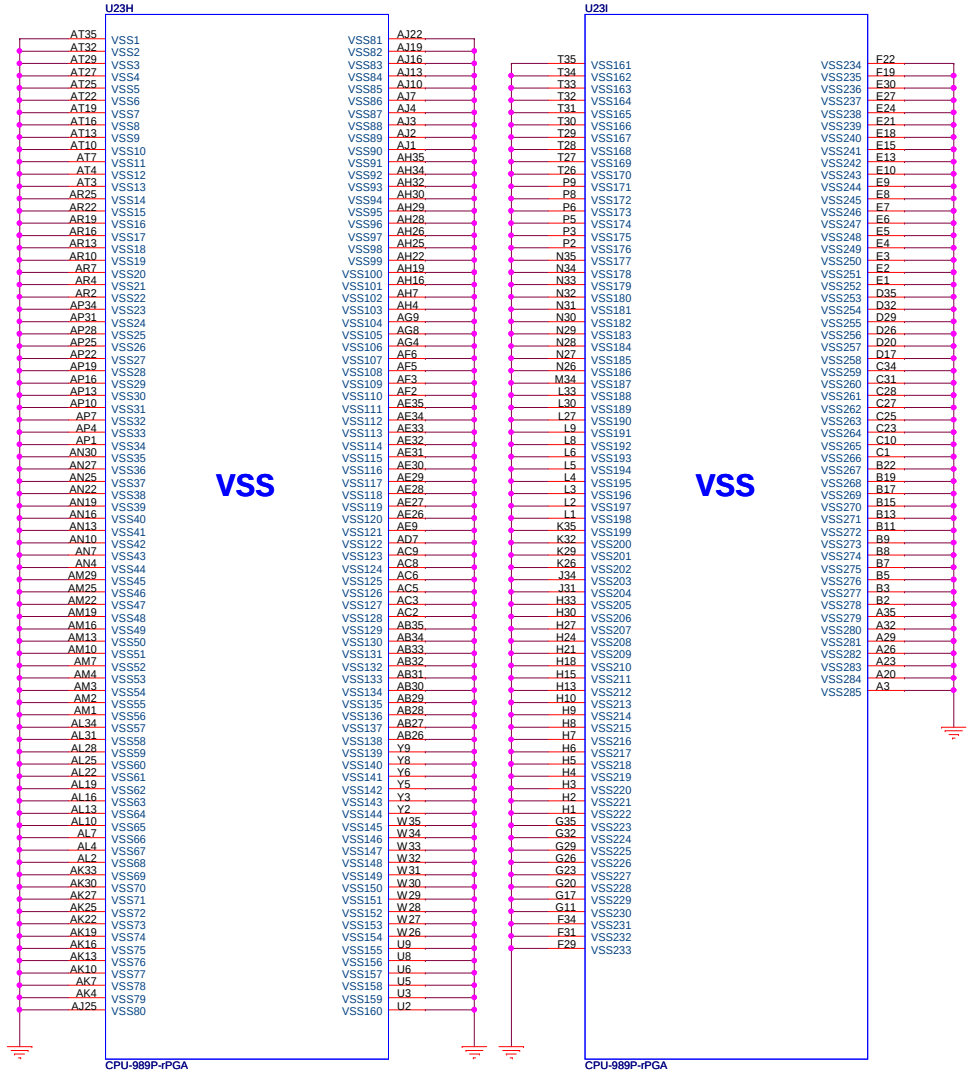
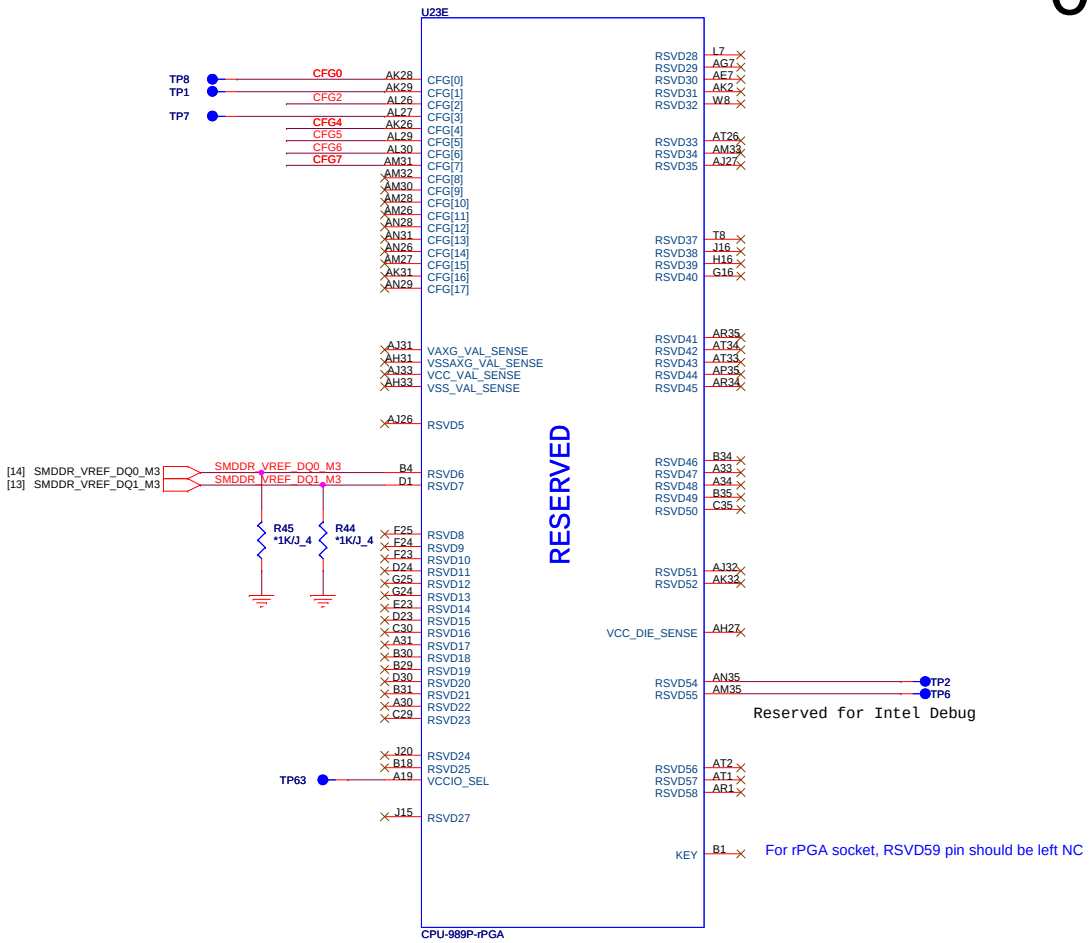
Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)

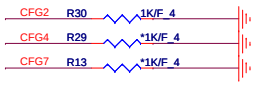
06

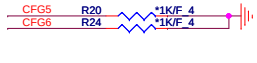


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training





CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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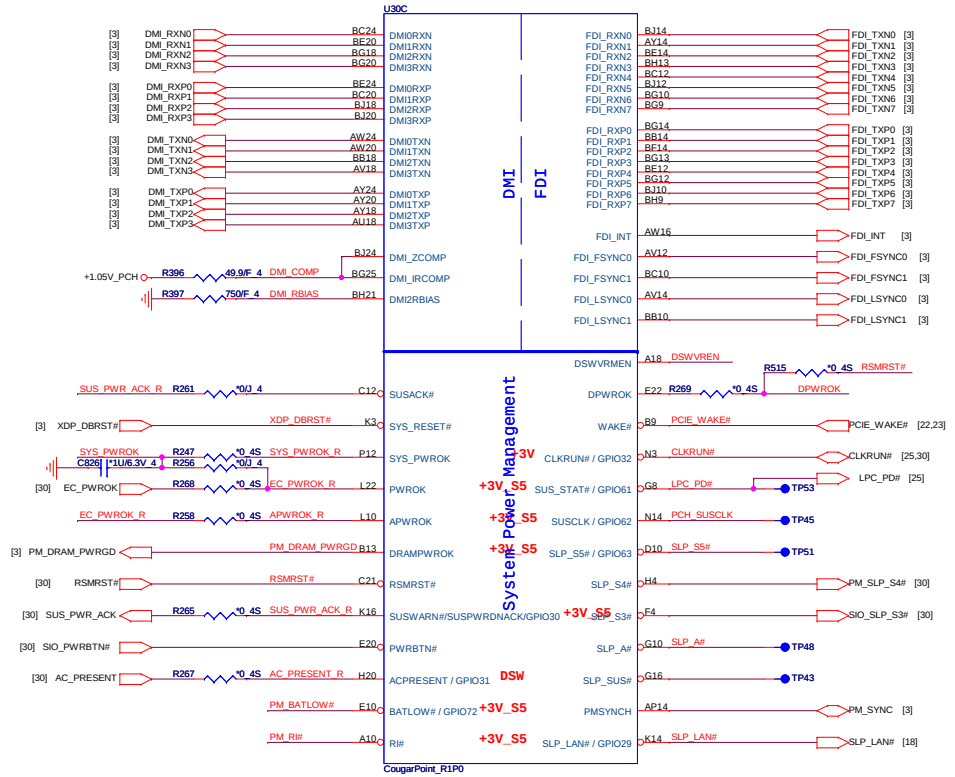
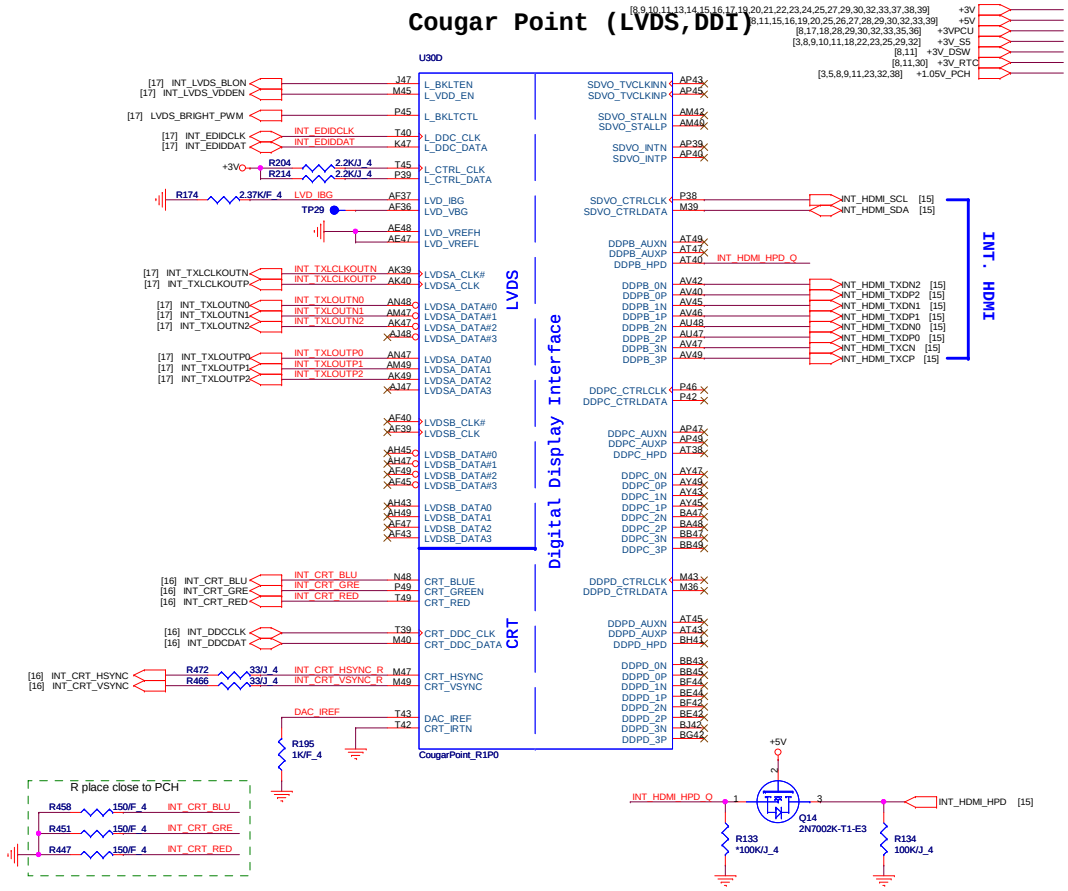
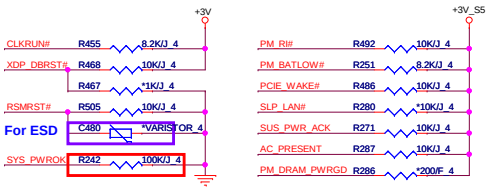
Cougar Point (DMI,FDI,PM)



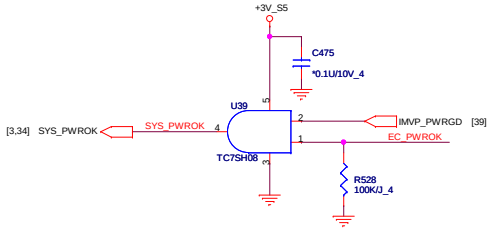
Cougar Point (LVDS,DDI)

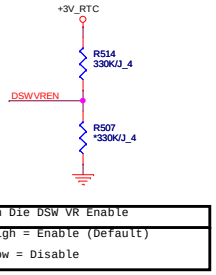


PCH Pull-high/low(CLG)

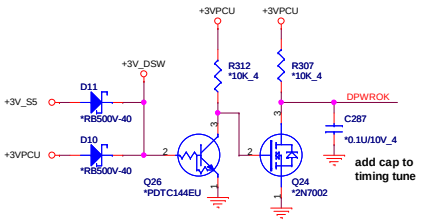


System PWR_OK(CLG)





DPWROK FOR DSW (n/c)



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Size	Document Number	Rev
Custom	<Doc> PCH 1/6 (DMI/FDI/VIDEO)	0D

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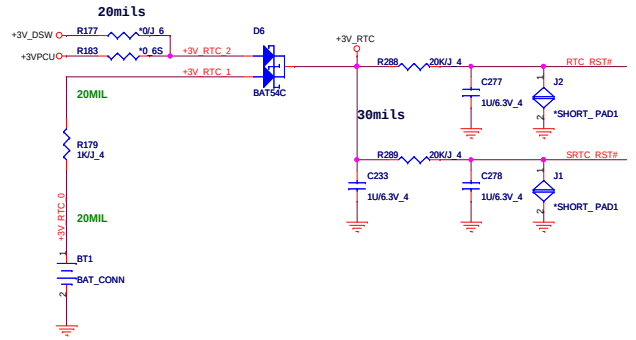
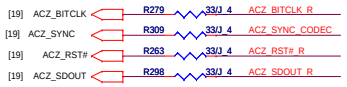
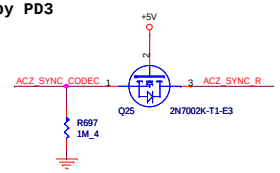
RTC Circuitry(RTC)



HDA Bus(CLG)



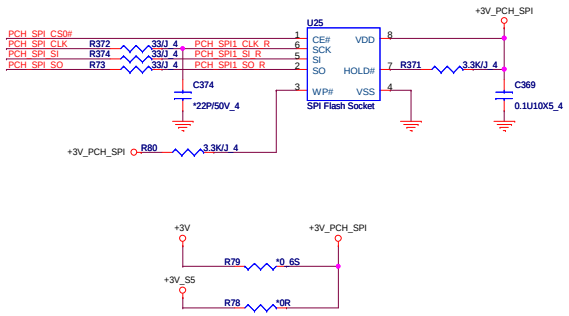
To Separate Codec Sync by PD3



PCH JTAG Debug (CLG)

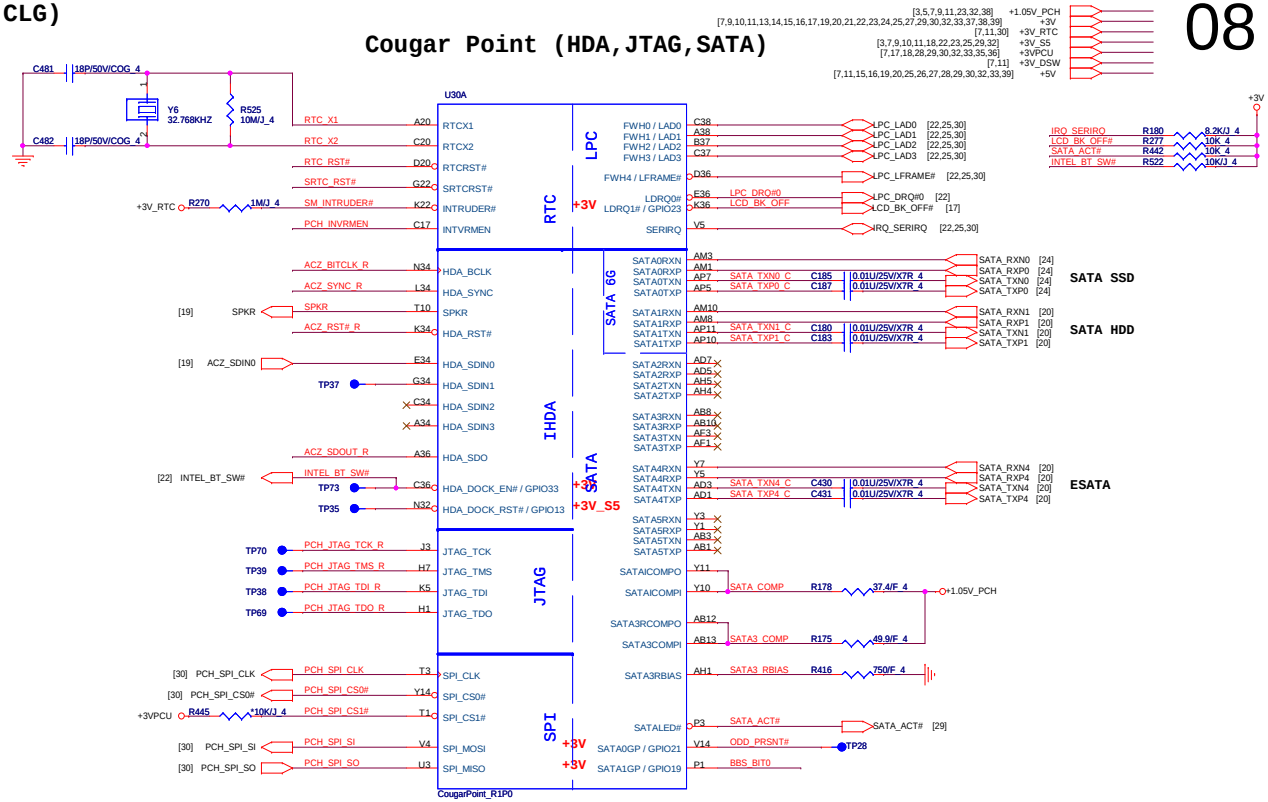
PCH Dual SPI (CLG)

MXIC 4M P/N: AKE39FP0Z02
WND 4M P/N: AKE391P0N00
Socket: DG008000031



PCH2(CLG)

Cougar Point (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R184 *1K/J_4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R240 *1K/J_4 PCI_GNT3# [9]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R506 330K/J_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location 1 / 1 / SPI * 0 / 0 / LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS] R246 *1K/J_4 BBS_BIT1 [9] R446 *1K/J_4 BBS_BIT0
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V_S5 R302 *1K/J_4 ACZ_SDOUT_R
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R400 2.2K/J_4 +1.8V R399 4.7K/J_4 DF_TVS [10] H_SNB_IVB# [3]
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R205 *1K/J_4 PLL_ODVR_EN [10]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R311 1K/J_4 ACZ_SYNC_R
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R182 *1K/J_4 PCH_SPI_SI
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)	

PROJECT KL7
Quanta Computer Inc.

Size	Document Number	Rev
C	<Doc> PCH 2/6(SATA/RTC/HDA/LPC)	0D

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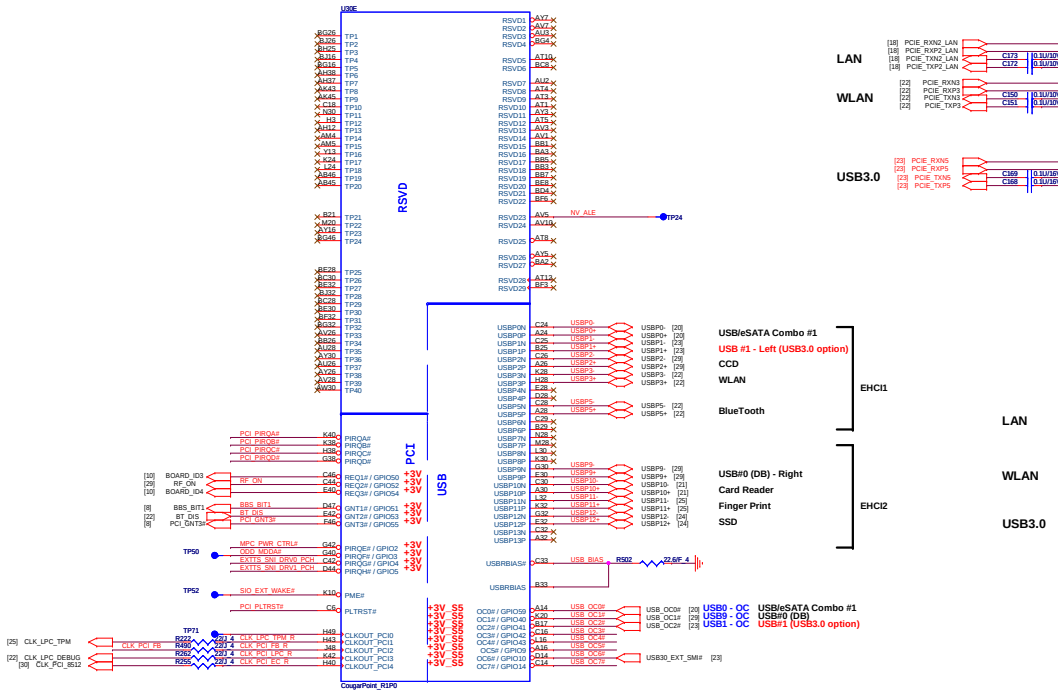
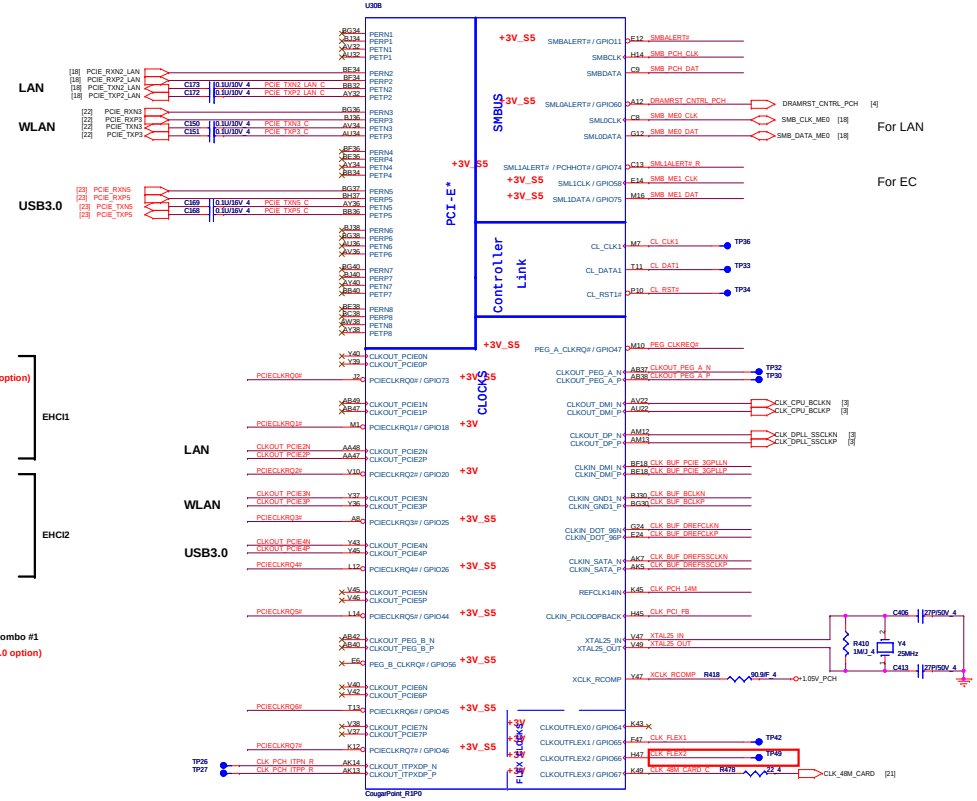
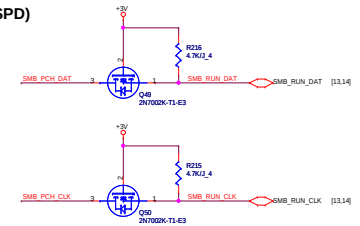
Cougar Point-M (PCI,USB,NVRAM)



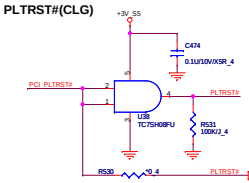
Cougar Point-M (PCI-E,SMBUS,CLK)



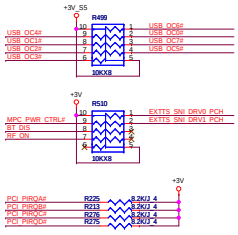
SMBus(SPD)



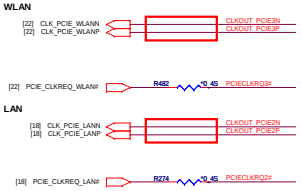
PLTRST#(CLG)



PCI/USBOC# Pull-up(CLG)



WLAN

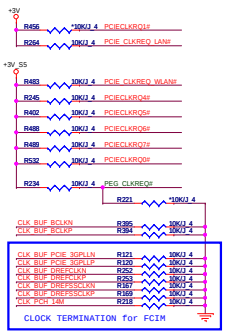


LAN

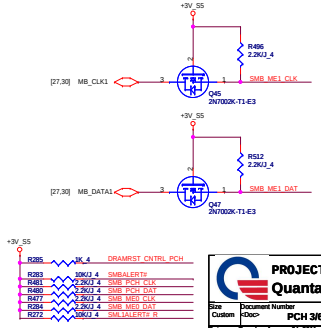
USB3.0 Chip

MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



PROJECT KL7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> PCH 3/6(PCIE/USB/CLK/NV)	0D

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Cougar Point (GPIO,VSS_NCTF,RSVD)

[7,8,9,11,13,14,15,16,17,19,20,21,22,23,24,25,27,29,30,32,33,37,38,39] +3V
[3,7,8,9,11,18,22,23,25,29,32] +3V_S5

10

U30F

Signal	Pin	Power
S_GPIO R193 100_4	T7	BMBUSY# / GPIO0 +3V
[30] EC_EXT_SMI# EC_EXT_SMI#	A42	TACH1 / GPIO1 +3V
BOARD_ID0	H36	TACH2 / GPIO6 +3V
[30] EC_EXT_SCI# EC_EXT_SCI#	E38	TACH3 / GPIO7 +3V
SYSTEM_ID	C10	GPIO8 +3V_S5
[18] LAN_DISABLE# LAN_DISABLE#	C4	LAN_PHY_PWR_CTRL / GPIO12 +3V_S5
HOST_ALERT#1_R	G2	GPIO15 +3V_S5
[22] WLAN_OFF# WLAN_OFF#	U2	SATA4GP / GPIO16 +3V
TP46 DGPU_PWROK	D40	TACH0 / GPIO17 +3V
BIOS_REC	T5	SCLOCK / GPIO22 +3V
[24] SDD_DA_DSS SDD_DA_DSS	E8	GPIO24 / MEM_LED +3V_S5
GPIO27	E16	GPIO27 DSW
[8] PLL_ODVR_EN R206 *0_4S PLL_ODVR_EN_R	P8	GPIO28 +3V_S5
STP_PCI#	K1	STP_PCI# / GPIO34 +3V
[22] BT_ON# BT_ON#	K4	GPIO35 +3V
TP31 DMI_OVRVLTG	V8	SATA2GP / GPIO36 +3V
FDI_OVRVLTG	M5	SATA3GP / GPIO37 +3V
MFG_MODE	N2	SLOAD / GPIO38 +3V
TP81	M3	SDATAOUT0 / GPIO39 +3V
TEST_SET_UP	V13	SDATAOUT1 / GPIO48 +3V
[27,30] TEMP_ALERT#	V3	SATA5GP / GPIO49 +3V
SV_DET	D6	GPIO57 +3V_S5

GPIO

Signal	Pin	Power
C40 BOARD_ID1		TACH4 / GPIO68 +3V
B41 R517 1.5K/F_4		TACH5 / GPIO69 +3V
C41 SSD_DETECT# [24]		TACH6 / GPIO70 +3V
A40 BOARD_ID2		TACH7 / GPIO71 +3V
A20GATE	P4	EC_A20GATE [30]
PECI	AU16	TP25
RCIN#	P5	EC_RCIN# EC_RCIN# [30]
PROCPWRGD	AY11	H_PWRGOOD [3]
THRMTRIP#	AY10	PCH_THRMTRIP# R143 390/J_4 PM_THRMTRIP# [3]
INIT3_3V#	T14	
DF_TVS	AY1	DF_TVS [8]
TS_VSS1	AH8	
TS_VSS2	AK11	
TS_VSS3	AH10	
TS_VSS4	AK10	
NC_1	P37	

CPU/MISC

NCTF

Pin	Signal
A4	VSS_NCTF_1
A44	VSS_NCTF_2
A45	VSS_NCTF_3
A46	VSS_NCTF_4
A5	VSS_NCTF_5
A6	VSS_NCTF_6
B3	VSS_NCTF_7
B47	VSS_NCTF_8
BD1	VSS_NCTF_9
BD49	VSS_NCTF_10
BE1	VSS_NCTF_11
BE49	VSS_NCTF_12
BF1	VSS_NCTF_13
BF49	VSS_NCTF_14
BG2	VSS_NCTF_15
BG48	VSS_NCTF_16
BH3	VSS_NCTF_17
BH47	VSS_NCTF_18
BJ4	VSS_NCTF_19
BJ44	VSS_NCTF_20
BJ45	VSS_NCTF_21
BJ46	VSS_NCTF_22
BJ5	VSS_NCTF_23
BJ6	VSS_NCTF_24
C2	VSS_NCTF_25
C48	VSS_NCTF_26
D1	VSS_NCTF_27
D49	VSS_NCTF_28
E1	VSS_NCTF_29
E49	VSS_NCTF_30
F1	VSS_NCTF_31
F49	VSS_NCTF_32

CougarPoint_R1P0

GPIO Pull-up/Pull-down(CLG)

+3V_S5
LAN_DISABLE# R470 10K/J_4

+3V
EC_EXT_SMI# R516 10K/J_4
EC_EXT_SCI# R291 10K/J_4
SSD_DETECT# R503 10K/J_4
STP_PCI# R460 10K/J_4
EC_A20GATE R200 10K/J_4
EC_RCIN# R201 10K/J_4
TEMP_ALERT# R432 10K/J_4
BT_ON# R227 10K/J_4
WLAN_OFF# R370 10K/J_4

GPIO27 R250 10K/J_4

Board ID	ID2 GPIO71	ID1 GPIO68	ID0 GPIO6
KL7	0	0	0
KL8	0	1	0
KL8A	1	0	0
KL9	0	1	1
KL9A	1	0	1

+3V
R282 10K/J_4 BOARD_ID0 R504 *10K/J_4
R290 10K/J_4 BOARD_ID1 R299 *10K/J_4
R501 10K/J_4 BOARD_ID2 R518 *10K/J_4
R398 10K/J_4 BOARD_ID3 R377 *10K/J_4
R542 10K/J_4 BOARD_ID4 R543 *10K/J_4
R487 10K/J_4 SYSTEM_ID R493 *10K/J_4

[9] BOARD_ID3 BOARD_ID3
[9] BOARD_ID4 BOARD_ID4

SV_SET_UP
High = Strong (Default)

+3V_S5
R249 *10K/J_4 SV_DET R243 100K/J_4

+3V
TEST_SET_UP R196 10K/J_4
R443 *0/J_4

+3V_S5
HOST_ALERT#1_R R237 1K/J_4

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

SGPIO

+3V
S_GPIO R190 10K/J_4
R192 *0/J_4

+3V
R257 100K/J_4 FDI_OVRVLTG R254 *1K/F_4

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

+3V
DMI_OVRVLTG R244 *200K/F_4

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

+3V
BIOS_REC R197 10K/J_4
R203 *0/J_4

BIOS RECOVERY	High = Disable (Default) Low = Enable

MFG-TEST

+3V
MFG_MODE R449 10K/J_4
R450 *0/J_4

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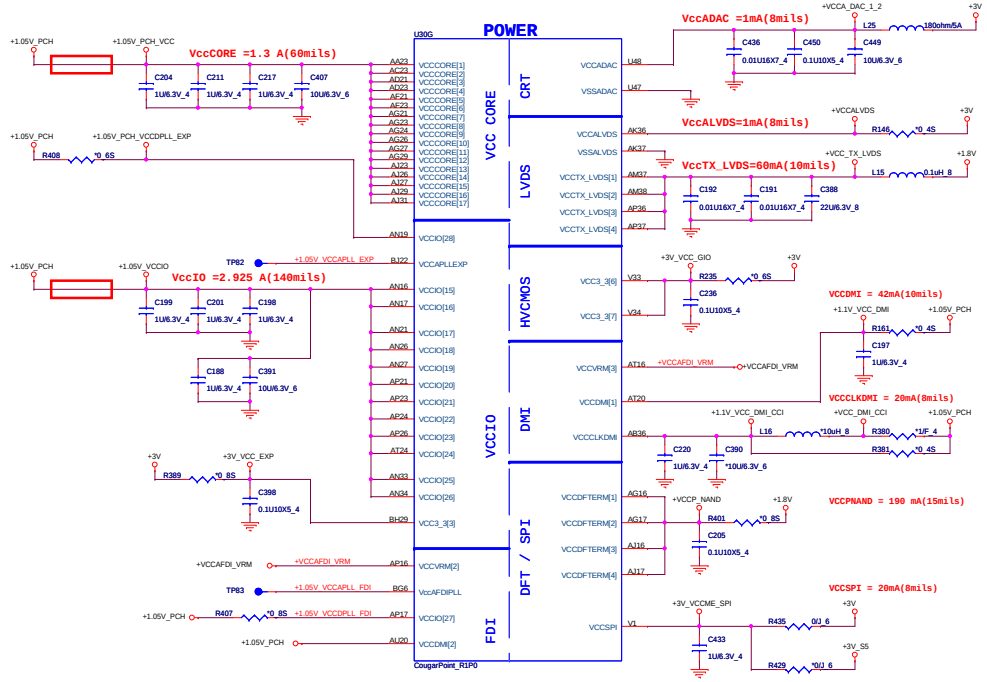
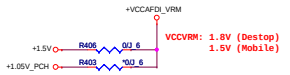
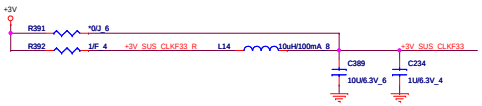
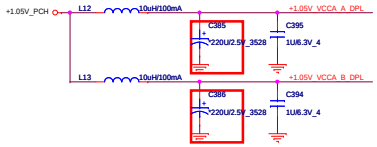
COUGAR POINT (POWER)

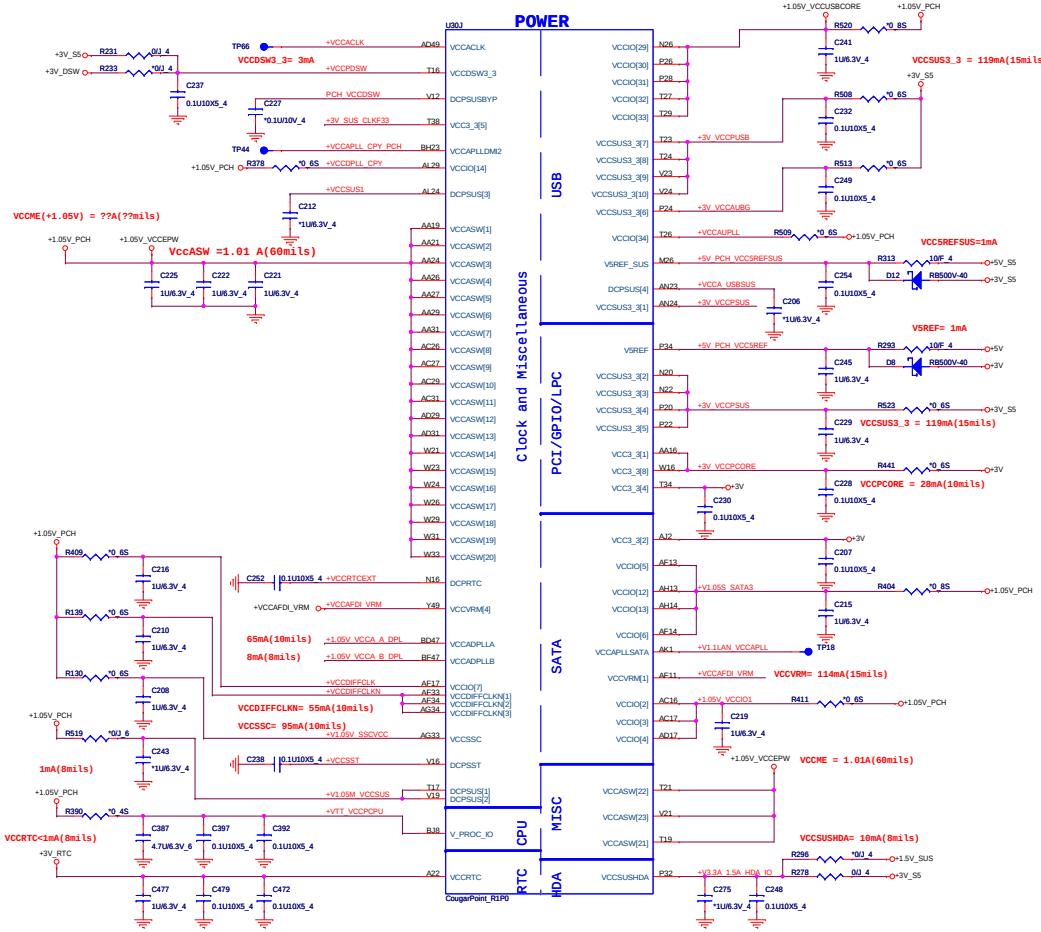








Cougar Point-M (POWER)



PROJECT KL7

Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/6(POWER)	0D

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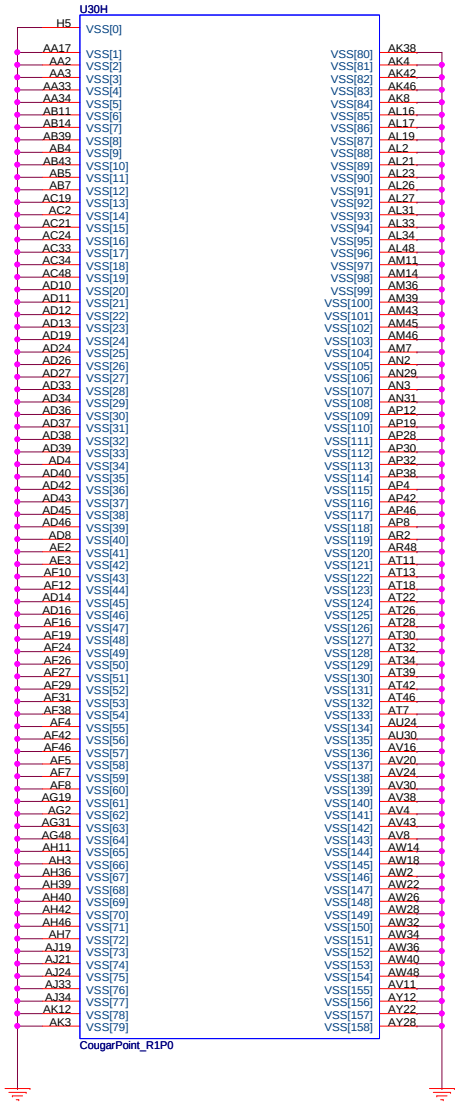
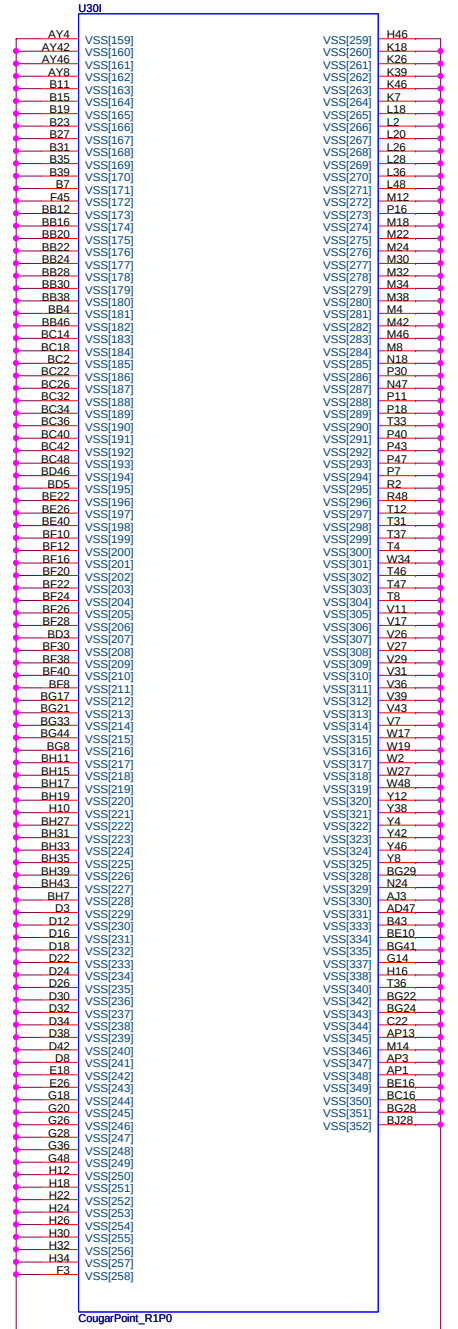
IBEX PEAK-M (GND)





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Custom	<Doc> PCH 6/6(GND)	0D

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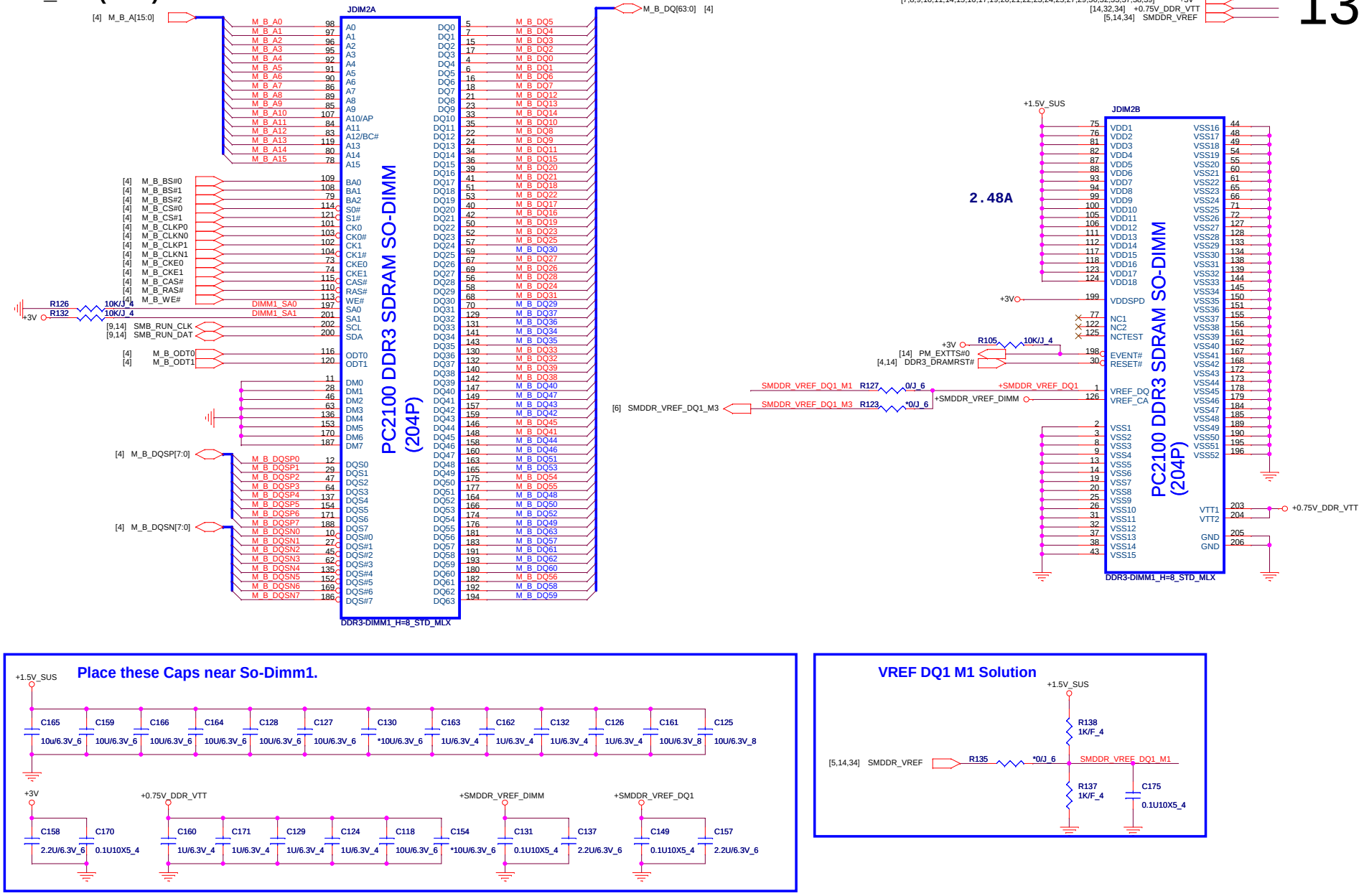
DDR_RVS(DDR)



PROJECT KL7 Quanta Computer Inc.			
Size Custom	Document Number <Doc> DDR3 DIMM-0-RVS(4.0H)		Rev 0D
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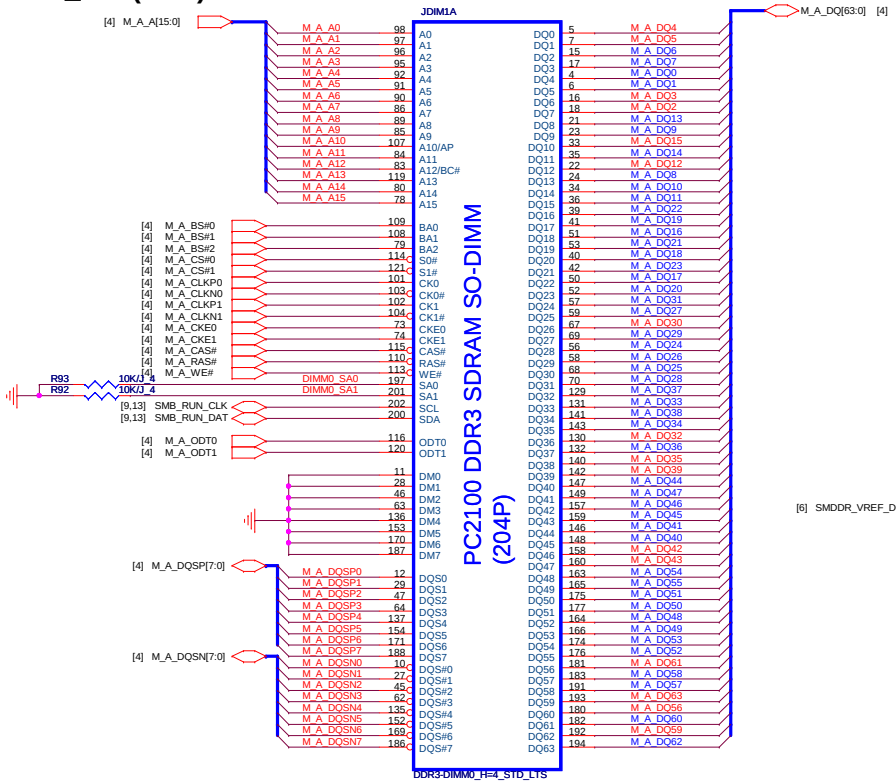
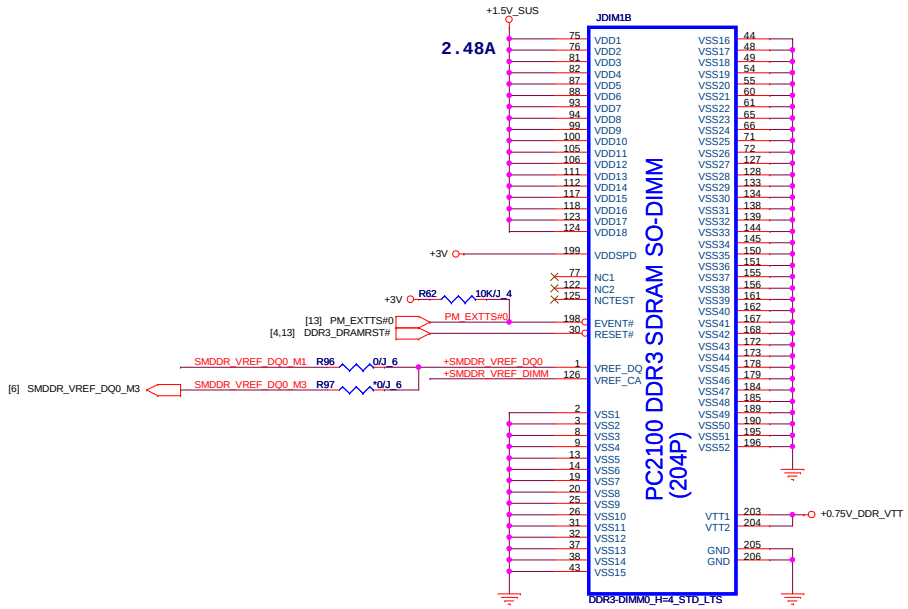
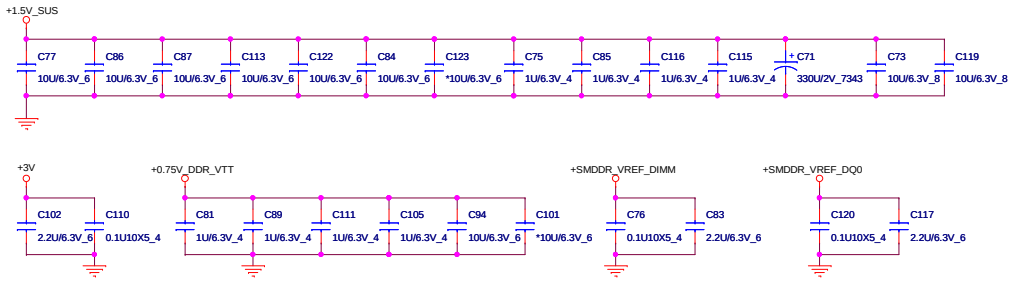
DDR_RVS(DDR)

[4,5,11,13,32,34] +1.5V_SUS
[7,8,9,10,11,13,15,16,17,19,20,21,22,23,24,25,27,29,30,32,33,37,38,39] +3V
[13,32,34] +0.75V_DDR_VTT
[5,13,34] SMDDR_VREF

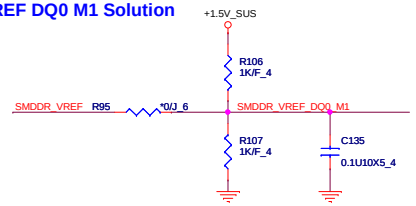


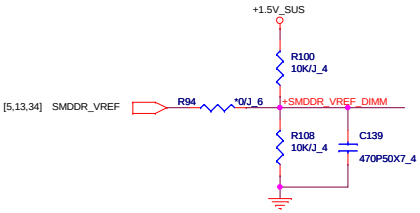


Place these Caps near So-Dimm0.



VREF DQ0 M1 Solution





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Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> DDR3 DIMM-1-RVS(8.0H)	0D

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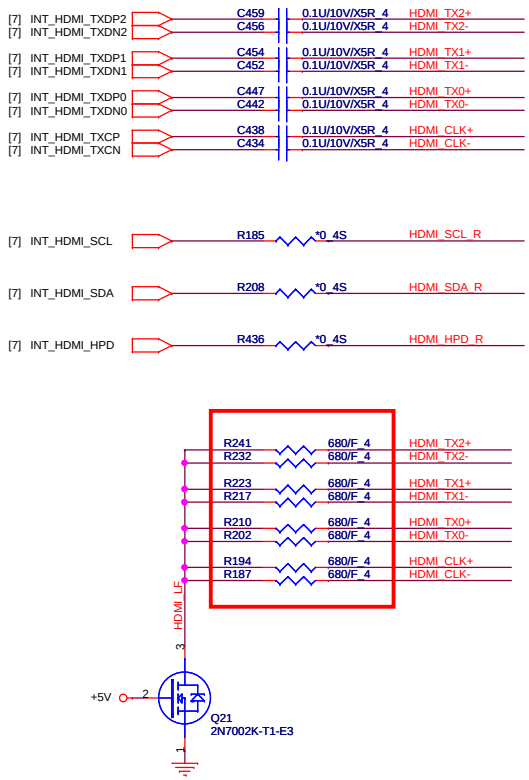
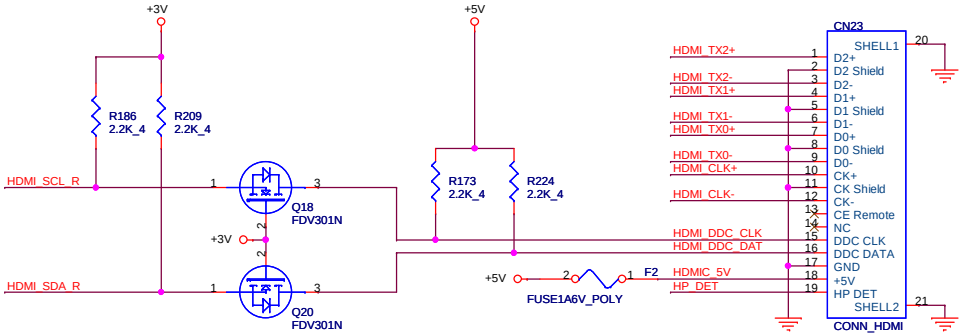
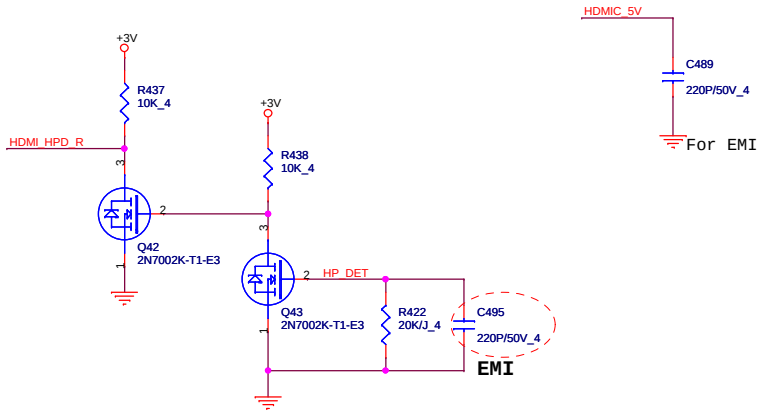
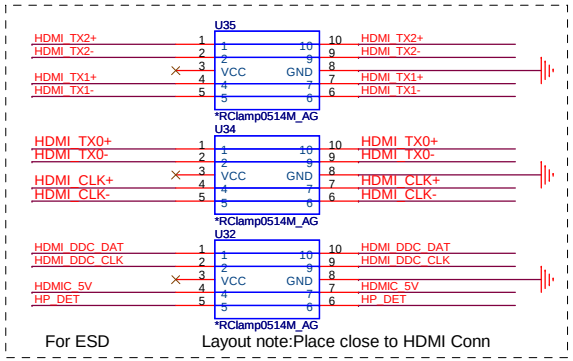
[7,8,11,16,19,20,25,26,27,28,29,30,32,33,39] +5V
[7,8,9,10,11,13,14,16,17,19,20,21,22,23,24,25,27,29,30,32,33,37,38,39] +3V

Cost reduce HDMI Level Shifter

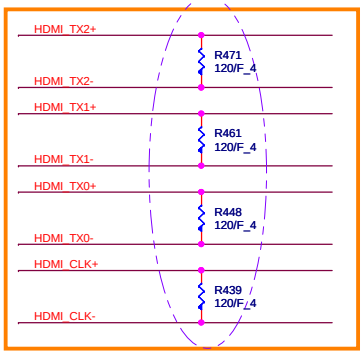








EMI reserve for HDMI



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Size: Custom	Document Number: <Doc> HDMI CONN	Rev: 0D
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[7,8,11,15,19,20,25,26,27,28,29,30,32,33,39] +5V
[7,8,9,10,11,13,14,15,17,19,20,21,22,23,24,25,27,29,30,32,33,37,38,39] +3V

Layout Note:
Setting R,G,B trace impedance to 50 ohm.

[7] INT_CRT_RED
[7] INT_CRT_GRE
[7] INT_CRT_BLU

L10 BK1608LL680
L9 BK1608LL680
L8 BK1608LL680

R366 150/F_4
R365 150/F_4
R363 150/F_4
C366 5.6P/50V/COG_4
C362 5.6P/50V/COG_4
C359 5.6P/50V/COG_4
C360 5.6P/50V/COG_4
C363 5.6P/50V/COG_4
C365 5.6P/50V/COG_4

CRT_R1
CRT_G1
CRT_B1

CRT_VCC
D3 RB500V-40
C47 0.1U/10V/X5R_4
+5V
F1 FUSE1A6V_POLY
C48 *VARISTOR_4
CRT_VCC_R
TP10
CN16 CRT_CONN

ESD PROTECTION

U6 CM1293A-04SO
CRT_R1
DDCDAT
CRT_G1
CRT_B1
+5V

U4 CM1293A-04SO
CRTHSYNC
CRT_VCC_R
CRTVSYNC
DDCCLK
+5V

[7] INT_CRT_VSYNC
[7] INT_CRT_HSYNC

U2 AHCT1G125DCH
U3 AHCT1G125DCH
C55 0.1U/10V/X5R_4
+5V

VGAVSYNC_R
VGAHSYNC_R

R359 10_4
R360 10_4

Place near
U37,U38 < 200 mil

CRT_VSYNC1
CRT_HSYNC1

C357 *10P/50V/COG_4
C352 *10P/50V/COG_4

L6 HB-1T1608-121JT
L7 HB-1T1608-121JT

C358 10P/50V/COG_4
C353 10P/50V/COG_4

CRTVSYNC
CRTHSYNC

Place near CN5002 connector
< 200 mil

+3V
CRT_VCC

R61 2.2K_4
R58 2.2K_4
R59 4.7K_4
R57 4.7K_4

[7] INT_DDCCLK
[7] INT_DDCDAT

Q6 2N7002K-T1-E3
Q9 2N7002K-T1-E3
+3V

DDCCLK
DDCDAT

C72 *10P/50V/COG_4
C59 *10P/50V/COG_4

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Custom	<Doc> CRT CONN	0D

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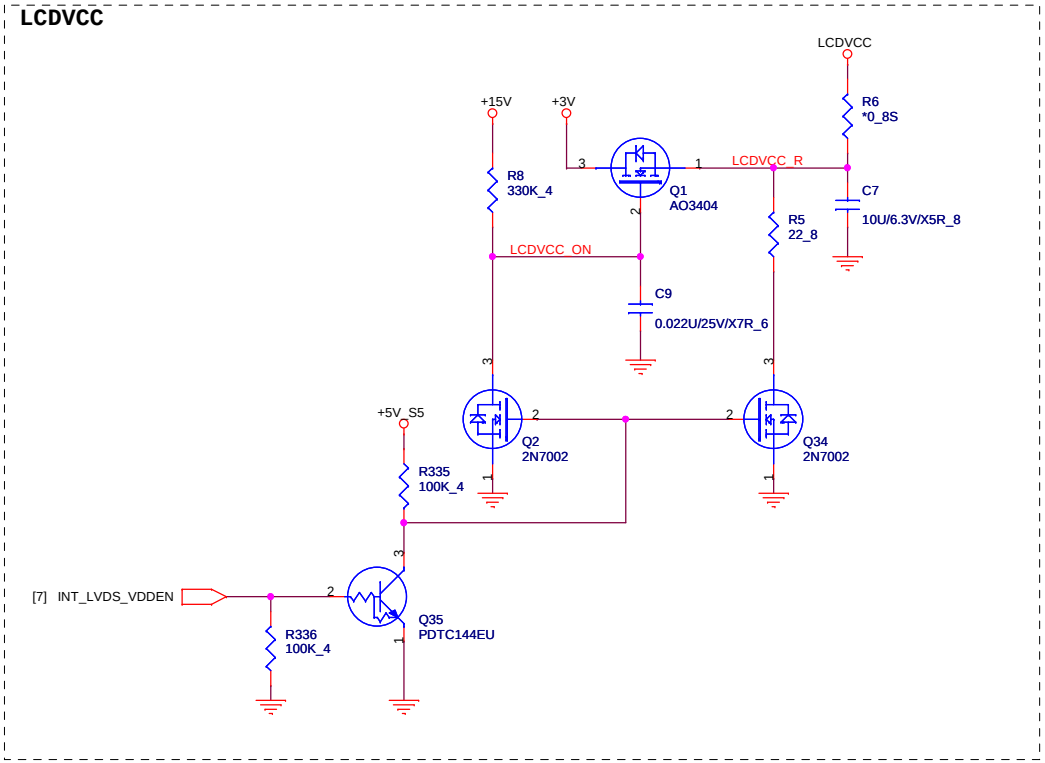
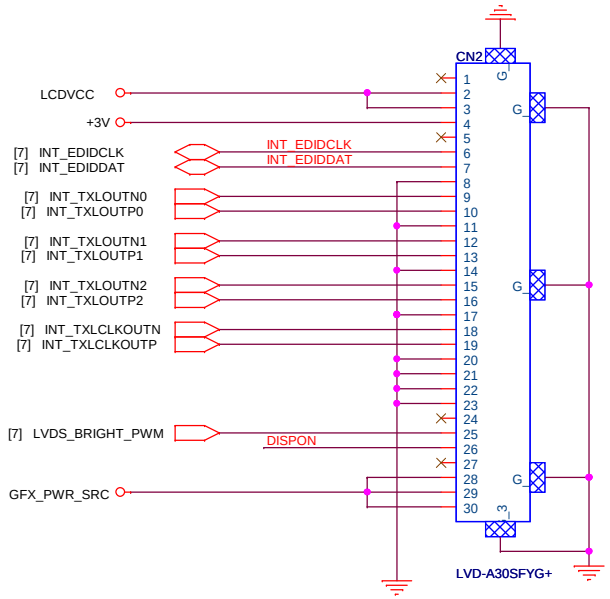
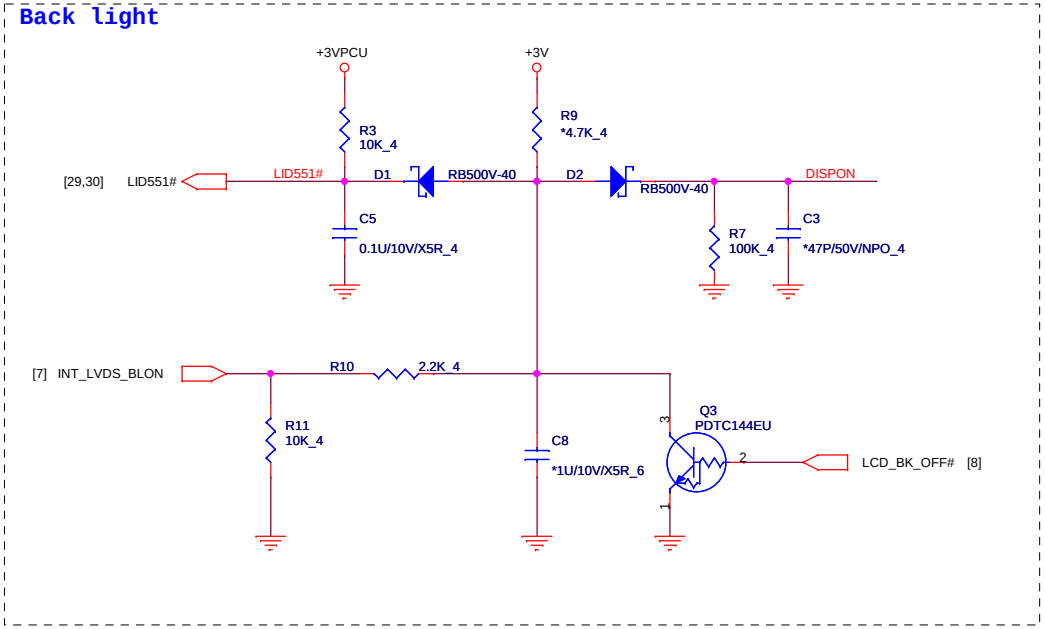
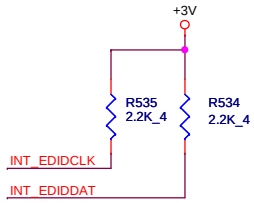
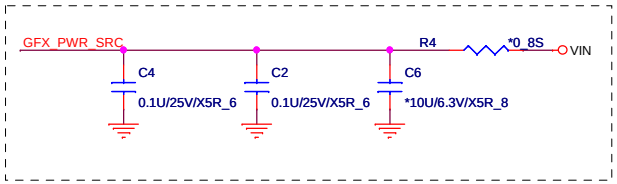
[7,8,9,10,11,13,14,15,16,19,20,21,22,23,24,25,27,29,30,32,33,37,38,39] +3V
[33,34,35,37,38,39] VIN
[22,23,29,32,35] +15V
[7,8,18,28,29,30,32,33,35,36] +3VPCU
[11,20,23,29,31,32] +5V_S5











PROJECT KL7
Quanta Computer Inc.

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Custom	<Doc> LCD CONN	0D

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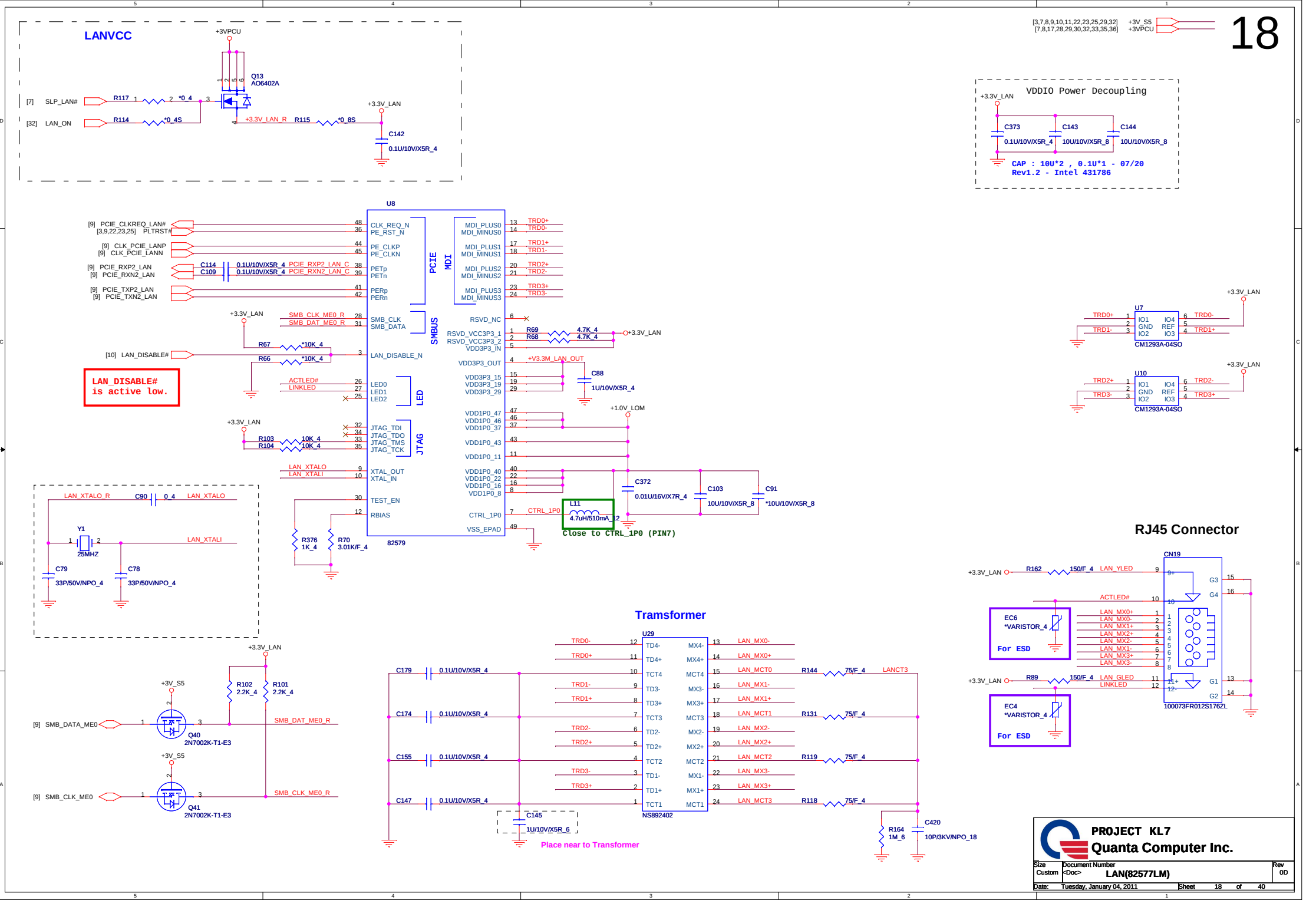
LANVCC
+3VPCU
Q13
AO6402A
[7] SLP_LAN#
R117 1 2 *0_4 3
[32] LAN_ON
R114 *0_4S
+3.3V_LAN_R R115 *0_8S
+3.3V_LAN
C142
0.1U/10V/X5R_4
[3,7,8,9,10,11,22,23,25,29,32] +3V_S5
[7,8,17,28,29,30,32,33,35,36] +3VPCU
VDDIO Power Decoupling
+3.3V_LAN
C373 0.1U/10V/X5R_4
C143 10U/10V/X5R_8
C144 10U/10V/X5R_8
CAP : 10U*2 , 0.1U*1 - 07/20
Rev1.2 - Intel 431786
U8
[9] PCIE_CLKREQ_LAN#
[3,9,22,23,25] PLTRST#
[9] CLK_PCIE_LANP
[9] CLK_PCIE_LANN
[9] PCIE_RXP2_LAN
[9] PCIE_RXN2_LAN
C114 0.1U/10V/X5R_4 PCIE_RXP2_LAN_C
C109 0.1U/10V/X5R_4 PCIE_RXN2_LAN_C
[9] PCIE_TXP2_LAN
[9] PCIE_TXN2_LAN
CLK_REQ_N
PE_RST_N
PE_CLKP
PE_CLKN
PETp
PETn
PERp
PERn
PCIE
MDI_PLUS0 TRD0+
MDI_MINUS0 TRD0-
MDI_PLUS1 TRD1+
MDI_MINUS1 TRD1-
MDI_PLUS2 TRD2+
MDI_MINUS2 TRD2-
MDI_PLUS3 TRD3+
MDI_MINUS3 TRD3-
MDI
+3.3V_LAN
SMB_CLK_ME0_R
SMB_DAT_ME0_R
SMB_CLK
SMB_DATA
SMBUS
RSVD_NC
RSVD_VCC3P3_1 R69 4.7K_4
RSVD_VCC3P3_2 R68 4.7K_4
VDD3P3_IN
[10] LAN_DISABLE#
R67 *10K_4
R66 *10K_4
LAN_DISABLE_N
VDD3P3_OUT +V3.3M_LAN_OUT
C88
1U/10V/X5R_4
LAN_DISABLE#
is active low.
ACTLED#
LINKLED
LED0
LED1
LED2
LED
VDD3P3_15
VDD3P3_19
VDD3P3_29
+1.0V_LOM
VDD1P0_47
VDD1P0_46
VDD1P0_37
VDD1P0_43
VDD1P0_11
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TCK
JTAG
R103 10K_4
R104 10K_4
LAN_XTALO
LAN_XTALI
XTAL_OUT
XTAL_IN
VDD1P0_40
VDD1P0_22
VDD1P0_16
VDD1P0_8
C372
0.01U/16V/X7R_4
C103
10U/10V/X5R_8
C91
*10U/10V/X5R_8
TEST_EN
RBIAS
CTRL_1P0
L11
4.7uH/510mA_12
Close to CTRL_1P0 (PIN7)
VSS_EPAD
R376
1K_4
R70
3.01K/F_4
82579
LAN_XTALO_R
C90 0_4
LAN_XTALO
Y1
25MHZ
LAN_XTALI
C79
33P/50V/NPO_4
C78
33P/50V/NPO_4
U7
TRD0+
TRD1-
IO1 IO4
GND REF
IO2 IO3
TRD0-
TRD1+
CM1293A-04SO
U10
TRD2+
TRD3-
TRD2-
TRD3+
CM1293A-04SO
RJ45 Connector
CN19
+3.3V_LAN
R162 150/F_4 LAN_YLED
ACTLED#
EC6
*VARISTOR_4
For ESD
LAN_MX0+
LAN_MX0-
LAN_MX1+
LAN_MX2+
LAN_MX2-
LAN_MX1-
LAN_MX3+
LAN_MX3-
R89 150/F_4 LAN_GLED
LINKLED
EC4
*VARISTOR_4
For ESD
G3
G4
G1
G2
100073FR012S176ZL
Tramsformer
U29
TRD0-
TRD0+
TRD1-
TRD1+
TRD2-
TRD2+
TRD3-
TRD3+
TD4-
TD4+
TCT4
TD3-
TD3+
TCT3
TD2-
TD2+
TCT2
TD1-
TD1+
TCT1
MX4-
MX4+
MCT4
MX3-
MX3+
MCT3
MX2-
MX2+
MCT2
MX1-
MX1+
MCT1
LAN_MX0-
LAN_MX0+
LAN_MCT0
LAN_MX1-
LAN_MX1+
LAN_MCT1
LAN_MX2-
LAN_MX2+
LAN_MCT2
LAN_MX3-
LAN_MX3+
LAN_MCT3
NS892402
C179 0.1U/10V/X5R_4
C174 0.1U/10V/X5R_4
C155 0.1U/10V/X5R_4
C147 0.1U/10V/X5R_4
R144 75/F_4 LANCT3
R131 75/F_4
R119 75/F_4
R118 75/F_4
C145
1U/10V/X5R_6
Place near to Transformer
R164
1M_6
C420
10P/3KV/NPO_18
+3.3V_LAN
+3V_S5
R102
2.2K_4
R101
2.2K_4
[9] SMB_DATA_ME0
Q40
2N7002K-T1-E3
SMB_DAT_ME0_R
[9] SMB_CLK_ME0
Q41
2N7002K-T1-E3
SMB_CLK_ME0_R
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Quanta Computer Inc.
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<Doc>
LAN(82577LM)
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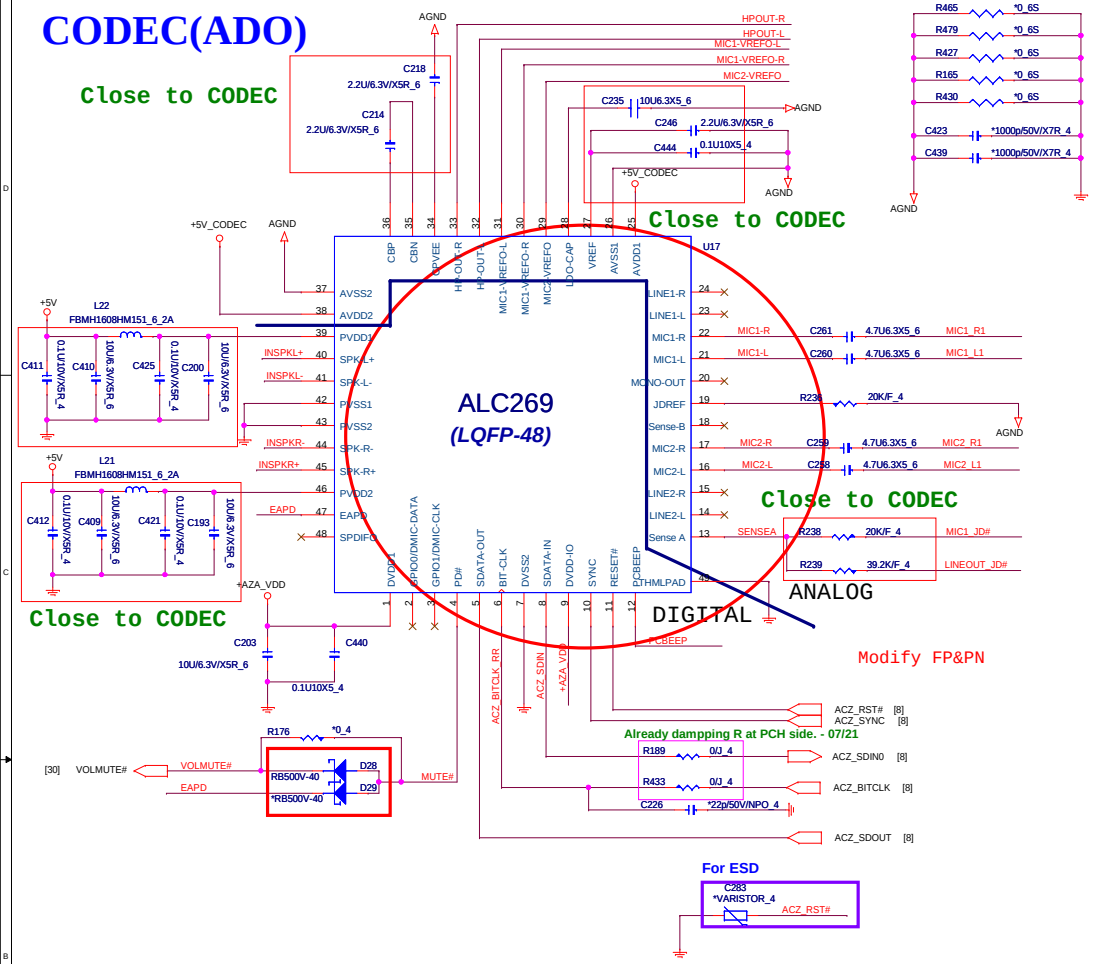
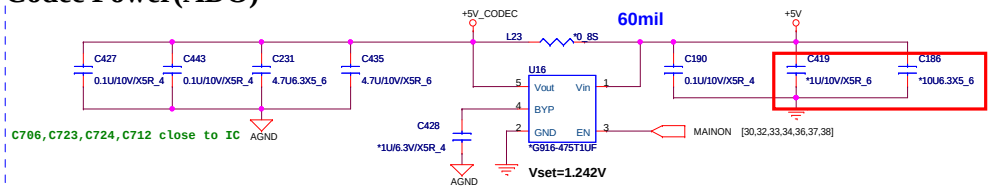
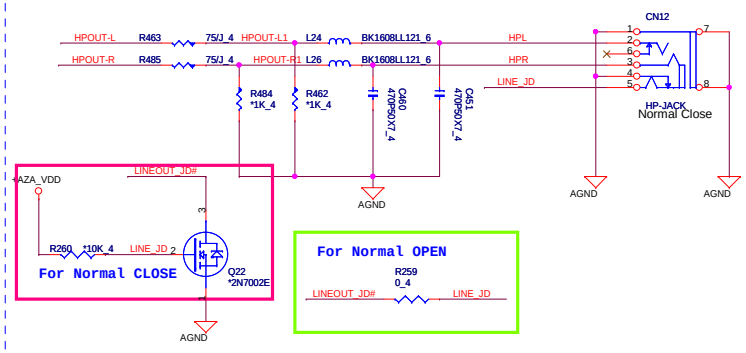
CODEC(ADO)



Codec Power(ADO)

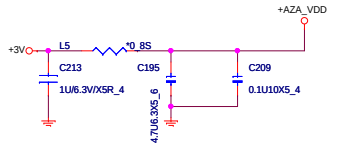


Earphone(AMP)

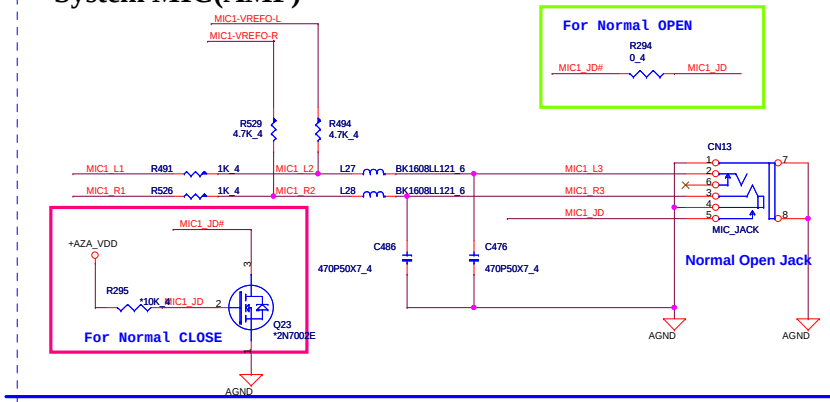


HDA Power(ADO)

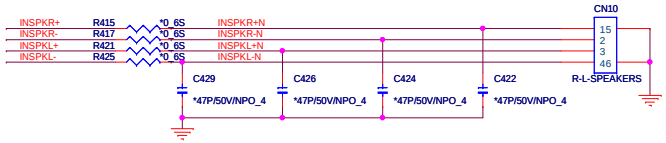
*Intel HDA Either +1.5V_S5 or +3V_S5



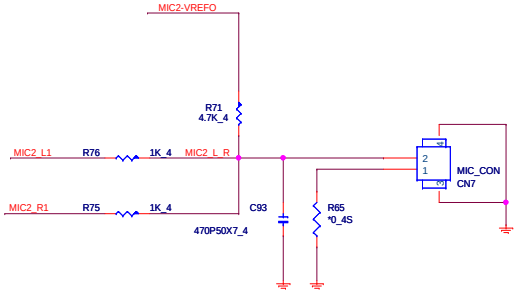
System MIC(AMP)



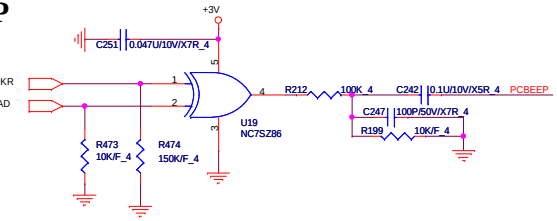
Speaker(AMP)



INTERNAL MIC



PC BEEP



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Custom	AL269/AMP/MIC/LINE-OUT	0D

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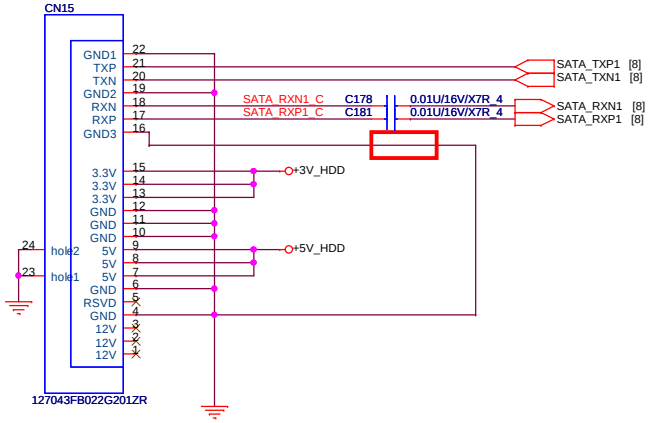
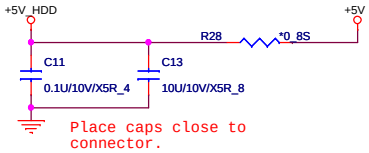
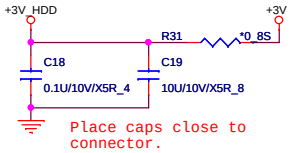
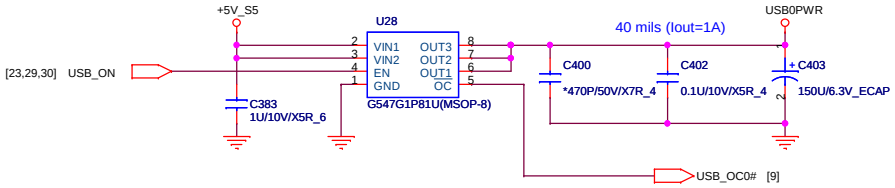
SATA HDD Connector.

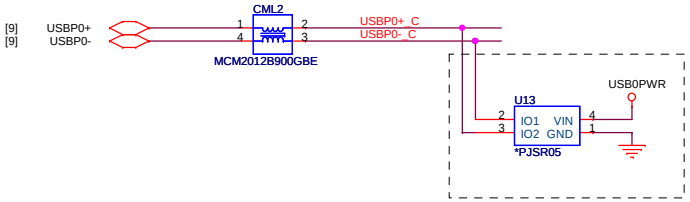


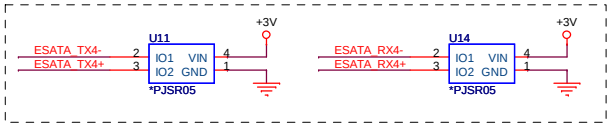




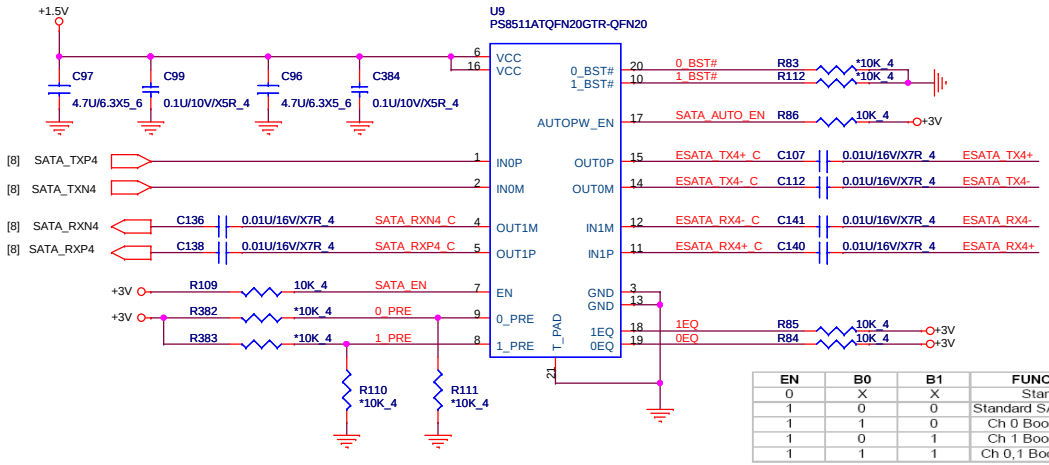
USB + E-SATA



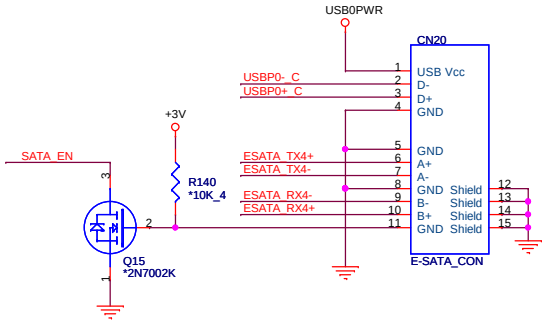




E-SATA RE-DRIVER



EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> SATA HDD/ESATA	0D

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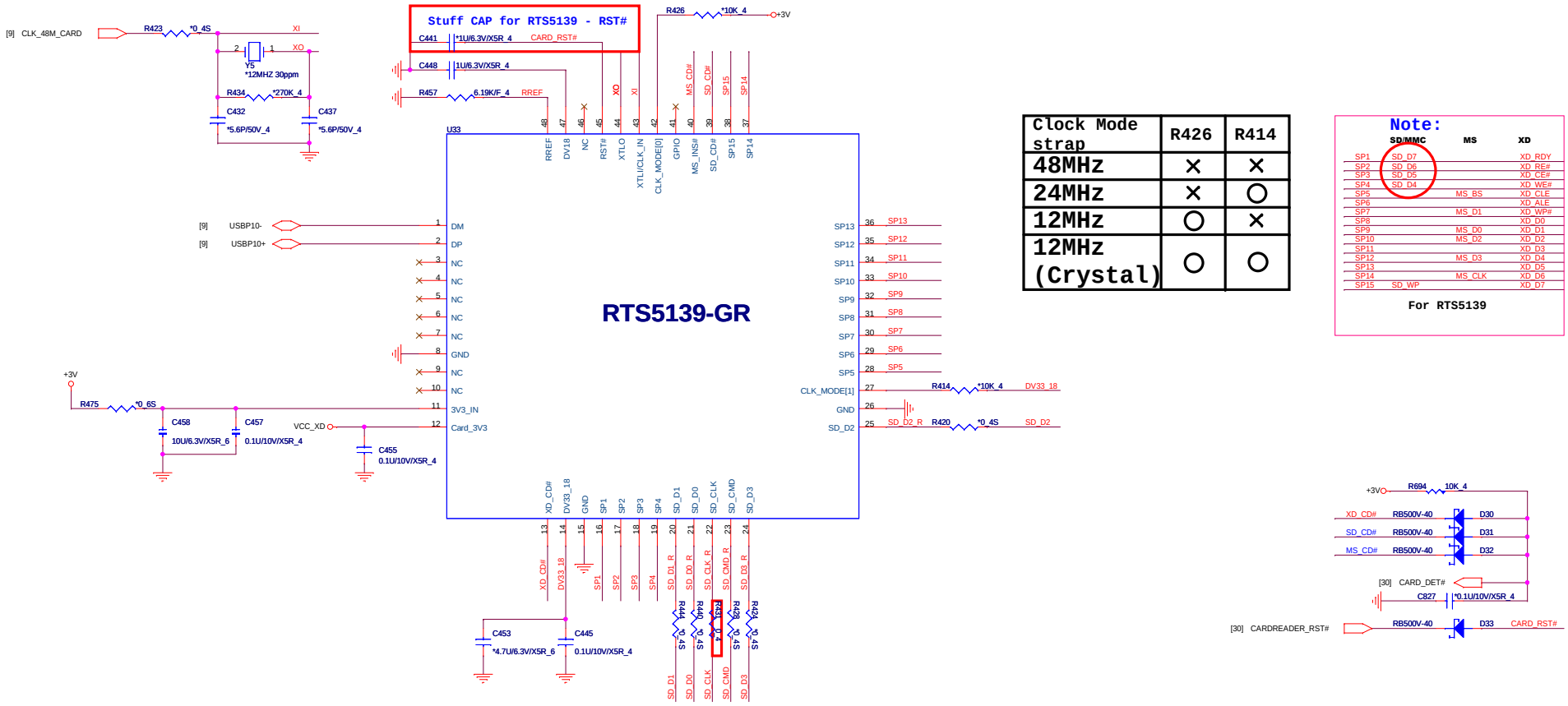
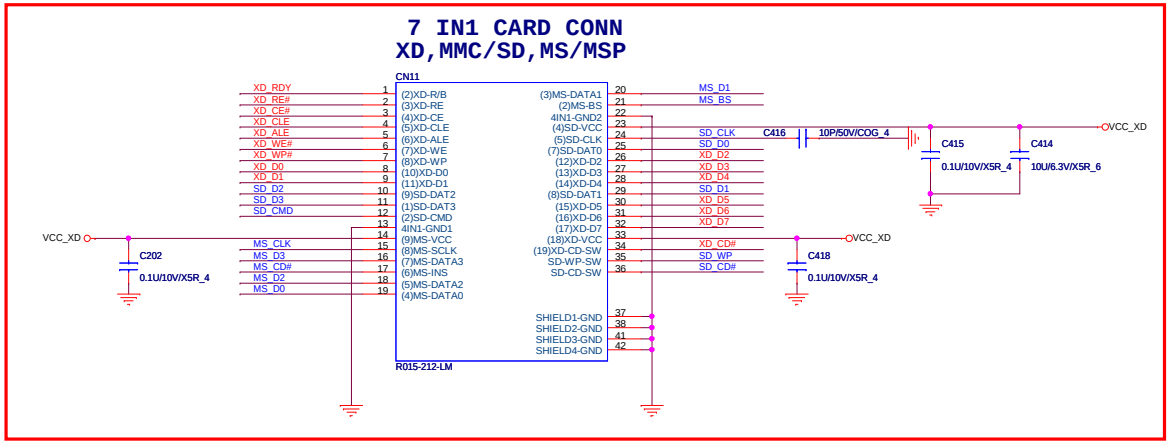


Clock Mode strap	R426	R414
48MHz	×	×
24MHz	×	○
12MHz	○	×
12MHz (Crystal)	○	○

Note:

SD/MMC	MS	XD
SP1 SD_D7		XD_RDY
SP2 SD_D6		XD_RE#
SP3 SD_D5		XD_CE#
SP4 SD_D4		XD_WE#
SP5	MS_BS	XD_CLE
SP6		XD_ALE
SP7	MS_D1	XD_WP#
SP8		XD_D0
SP9	MS_D0	XD_D1
SP10	MS_D2	XD_D2
SP11		XD_D3
SP12	MS_D3	XD_D4
SP13		XD_D5
SP14	MS_CLK	XD_D6
SP15 SD_WP		XD_D7

For RTS5139



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Custom	<Doc> Card Reader (RTS5139)	0D

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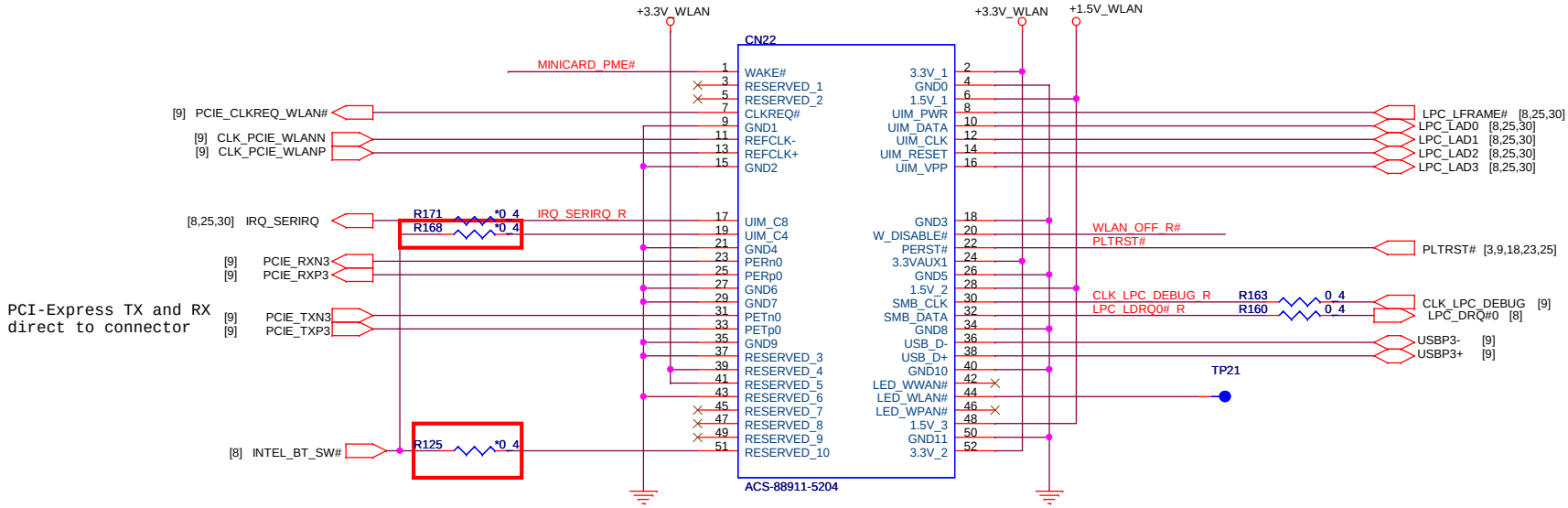
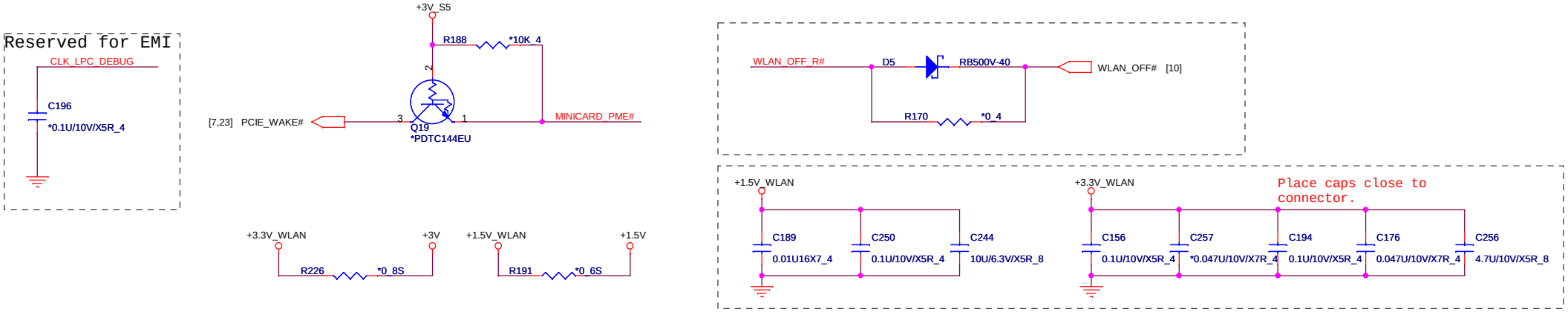
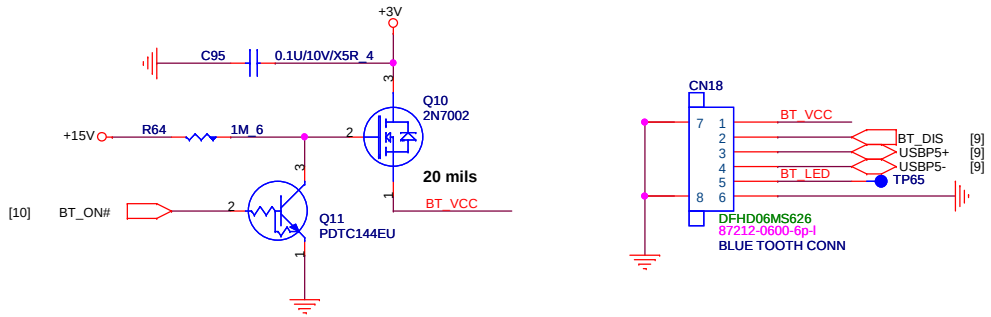
MiniCard WLAN connector

[7,8,9,10,11,13,14,15,16,17,19,20,21,23,24,25,27,29,30,32,33,37,38,39] +3V
[11,20,24,32] +1.5V
[3,7,8,9,10,11,18,23,25,29,32] +3V_S5
[17,23,29,32,35] +15V





BLUETOOTH



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Size	Document Number	Rev
Custom	<Doc> WLAN/BT	0D

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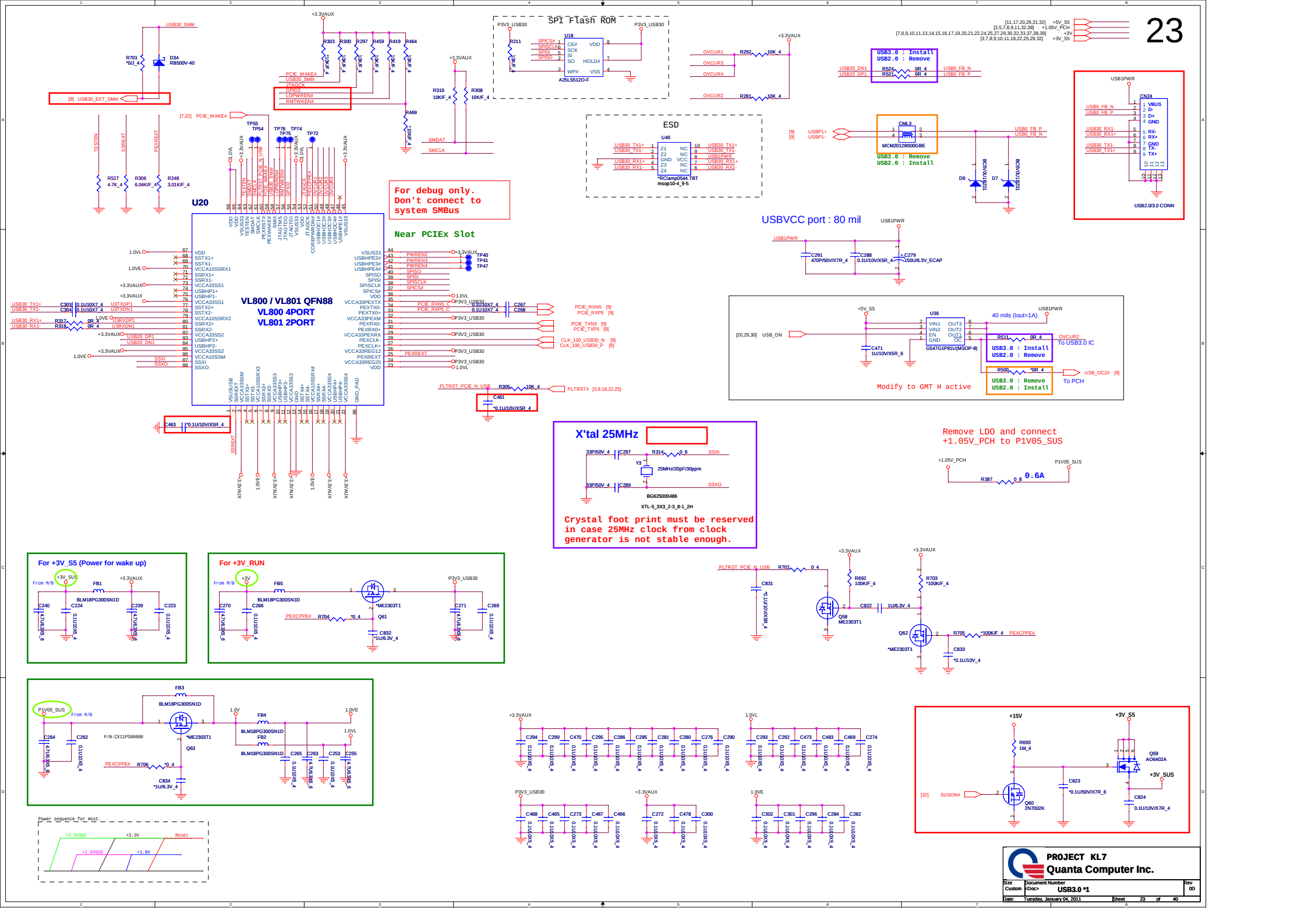
SPI Flash ROM
U18
A25LS512O-F
ESD
U40
*RClamp0544.TBT
msop10-4_9-5
U20
VL800 / VL801 QFN88
VL800 4PORT
VL801 2PORT
For debug only.
Don't connect to
system SMBus
Near PCIEx Slot
USBVCC port : 80 mil
USB3.0 : Install
USB2.0 : Remove
USB3.0 : Remove
USB2.0 : Install
CN24
USB2.0/3.0 CONN
U36
G547G1P81U(MSOP-8)
40 mils (Iout=1A)
To USB3.0 IC
To PCH
Modify to GMT H active
X'tal 25MHz
25MHz/20pF/30ppm
BG625000486
XTL-5_3X3_2-3_8-1_2H
Crystal foot print must be reserved
in case 25MHz clock from clock
generator is not stable enough.
Remove LDO and connect
+1.05V_PCH to P1V05_SUS
0.6A
For +3V_S5 (Power for wake up)
For +3V_RUN
Power sequence for Host.
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Quanta Computer Inc.
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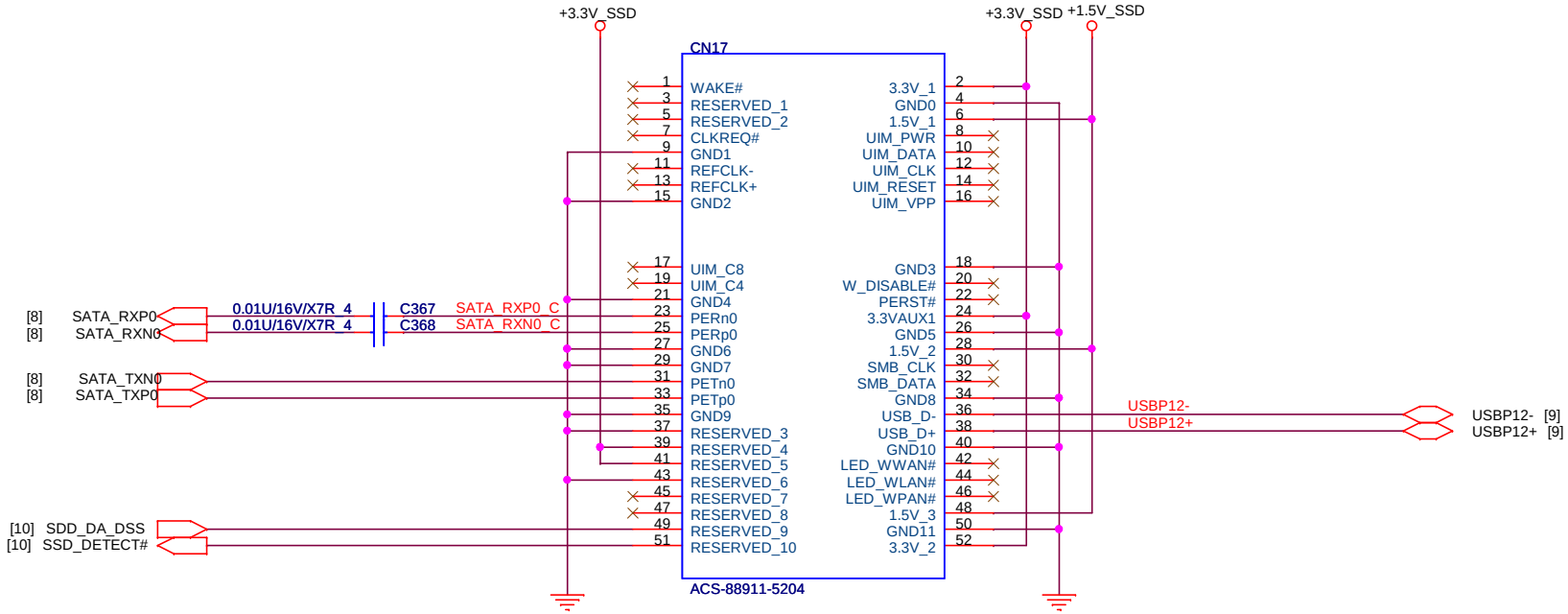
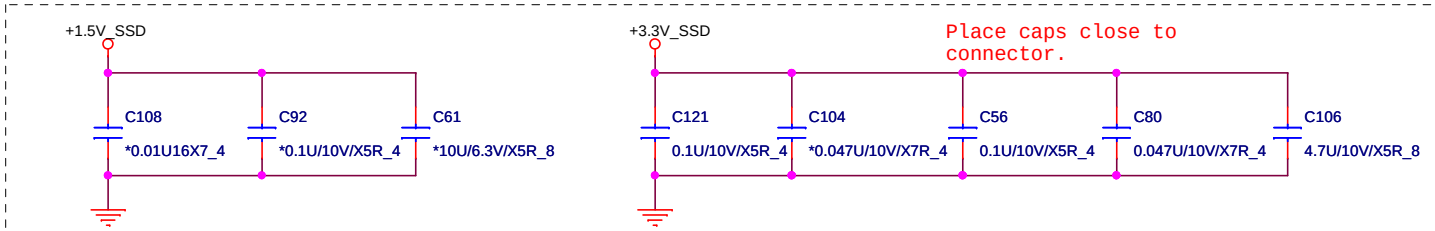
MiniCard SSD connector

[11,20,22,32] +1.5V
[7,8,9,10,11,13,14,15,16,17,19,20,21,22,23,25,27,29,30,32,33,37,38,39] +3V





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Quanta Computer Inc.

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Custom	<Doc> MINI-Card (SSD)	0D

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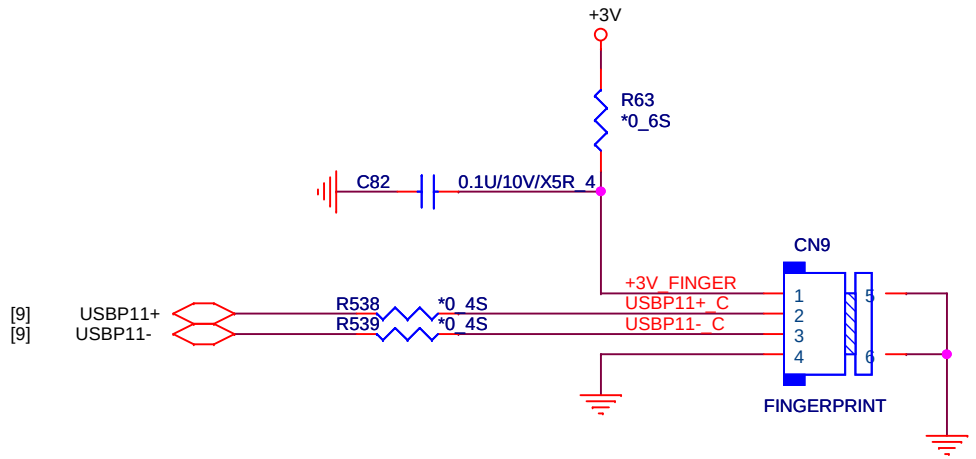
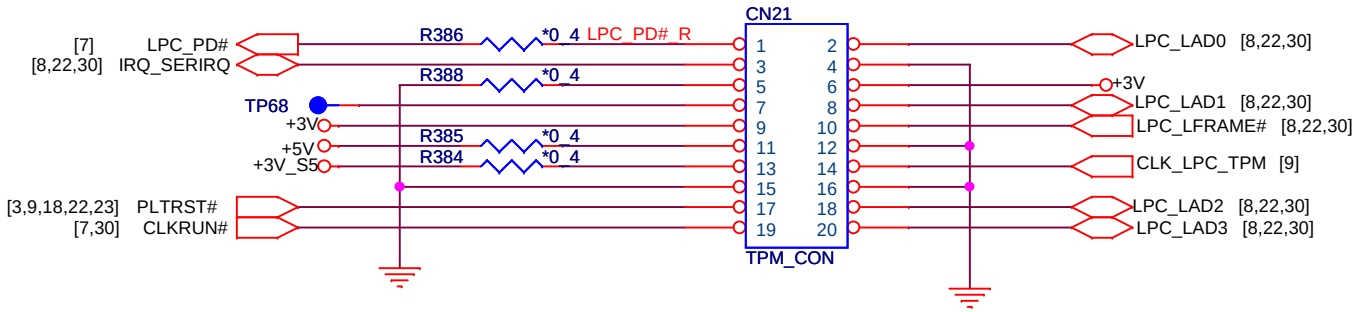
FINGER PRINTER

[7,8,9,10,11,13,14,15,16,17,19,20,21,22,23,24,27,29,30,32,33,37,38,39] +3V
[7,8,11,15,16,19,20,26,27,28,29,30,32,33,39] +5V
[3,7,8,9,10,11,18,22,23,29,32] +3V_S5



TPM



PROJECT KL7

Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> FP/TPM	0D

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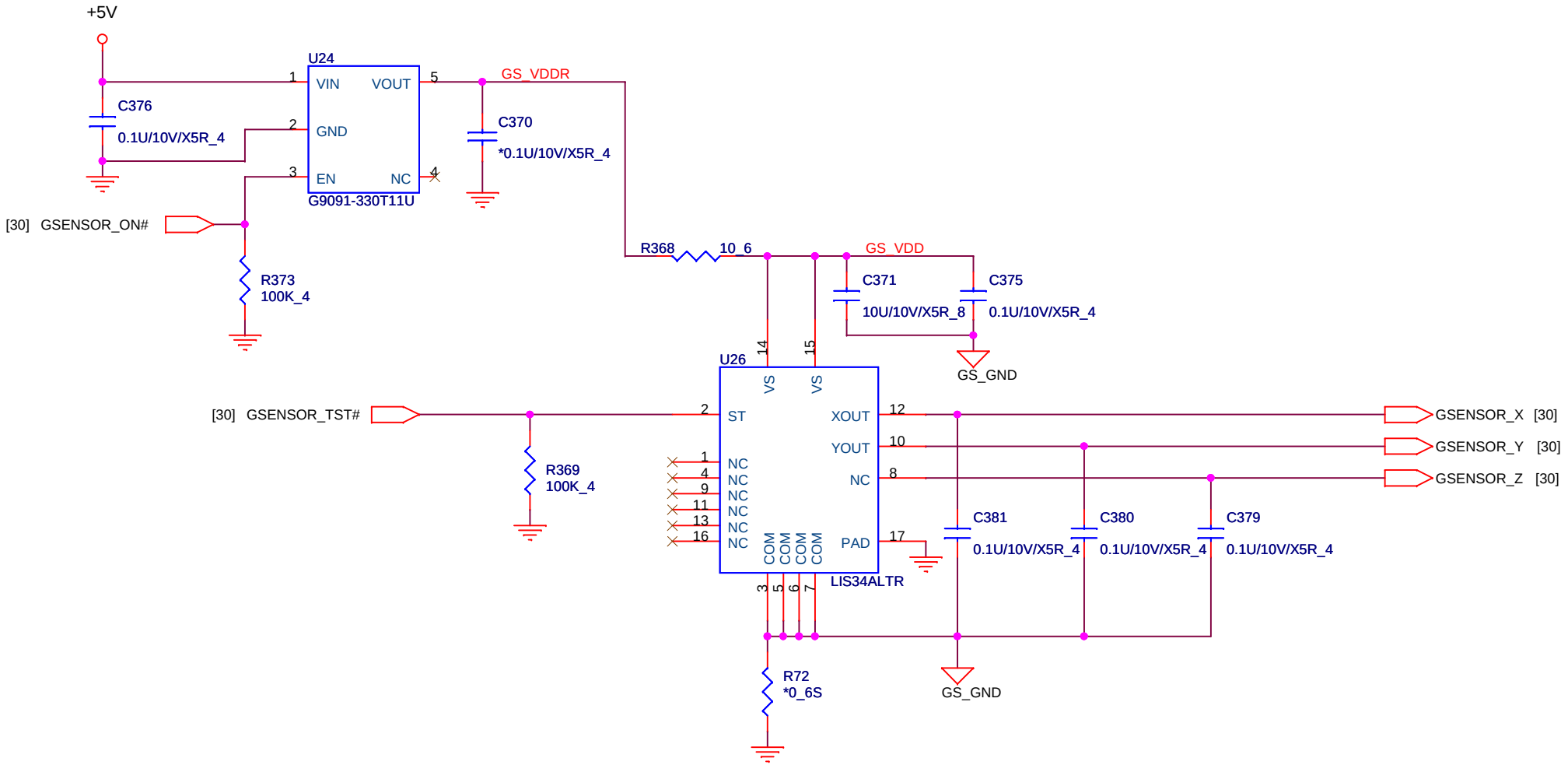
G-SENSOR (3-Axial)

[7,8,11,15,16,19,20,25,27,28,29,30,32,33,39] +5V

38



PROJECT KL7

Quanta Computer Inc.

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Custom	<Doc> G-SENSOR	0D

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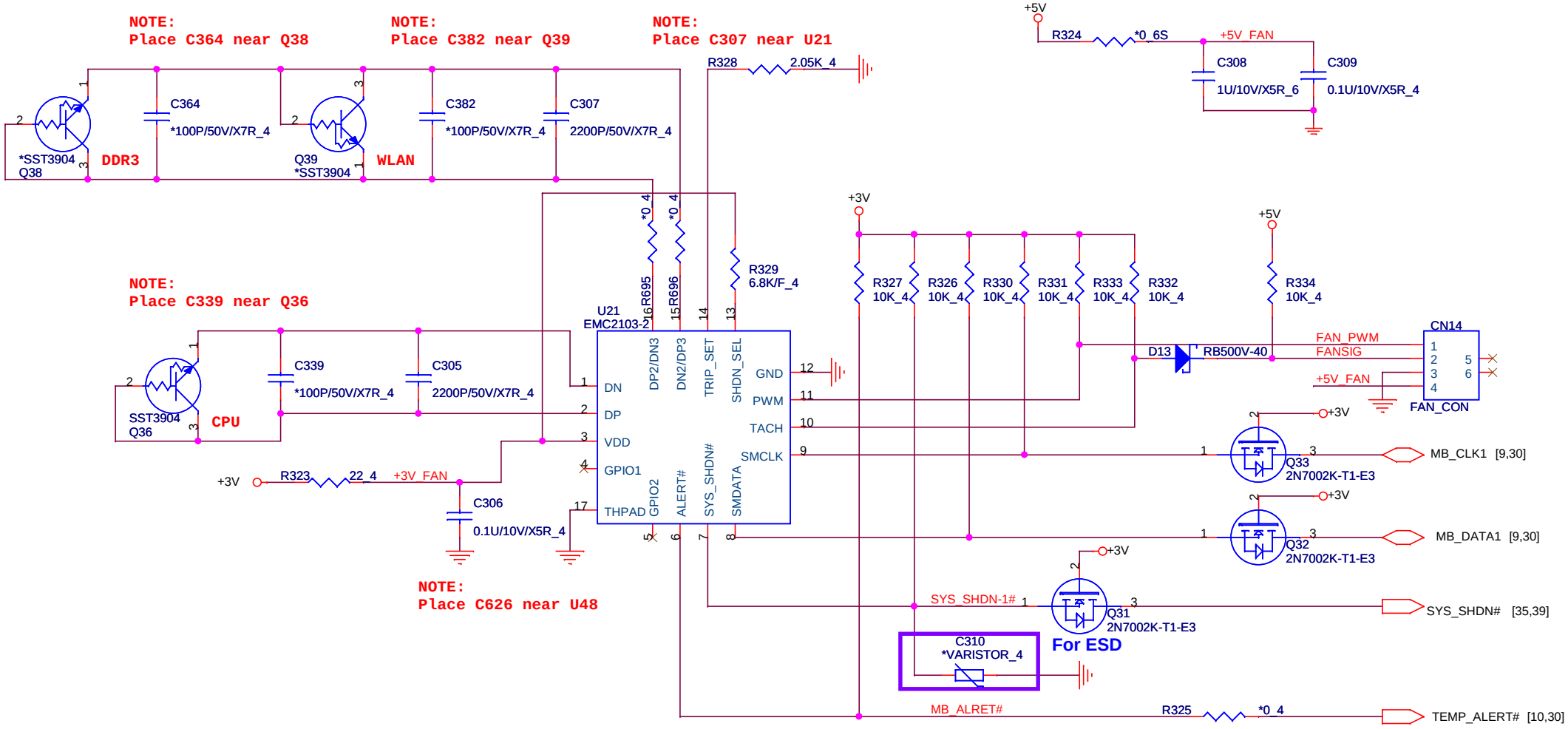
FAN CONTROL

[7,8,9,10,11,13,14,15,16,17,19,20,21,22,23,24,25,29,30,32,33,37,38,39] +3V
[7,8,11,15,16,19,20,25,26,28,29,30,32,33,39] +5V



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> FAN /THERMAL	0D

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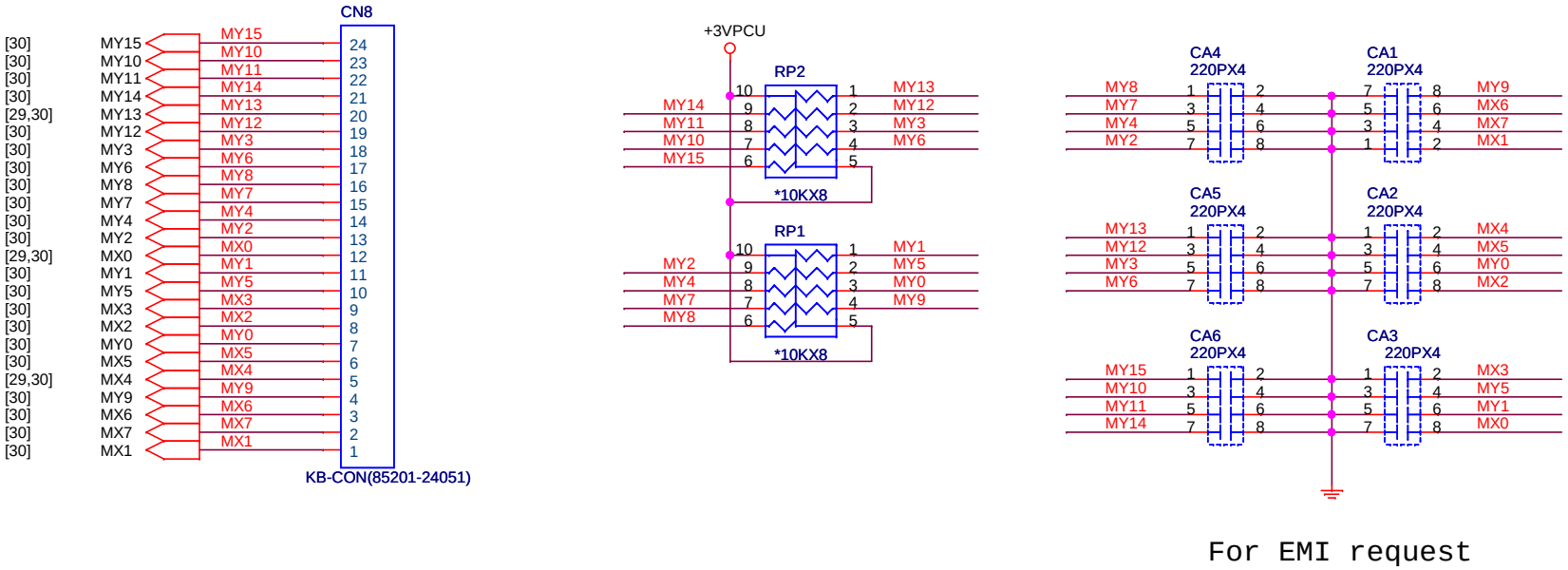
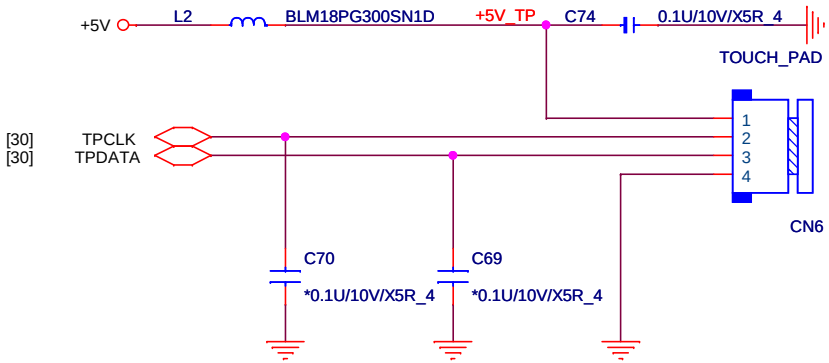
KEYBOARD



Touch pad



PROJECT KL7 Quanta Computer Inc.			
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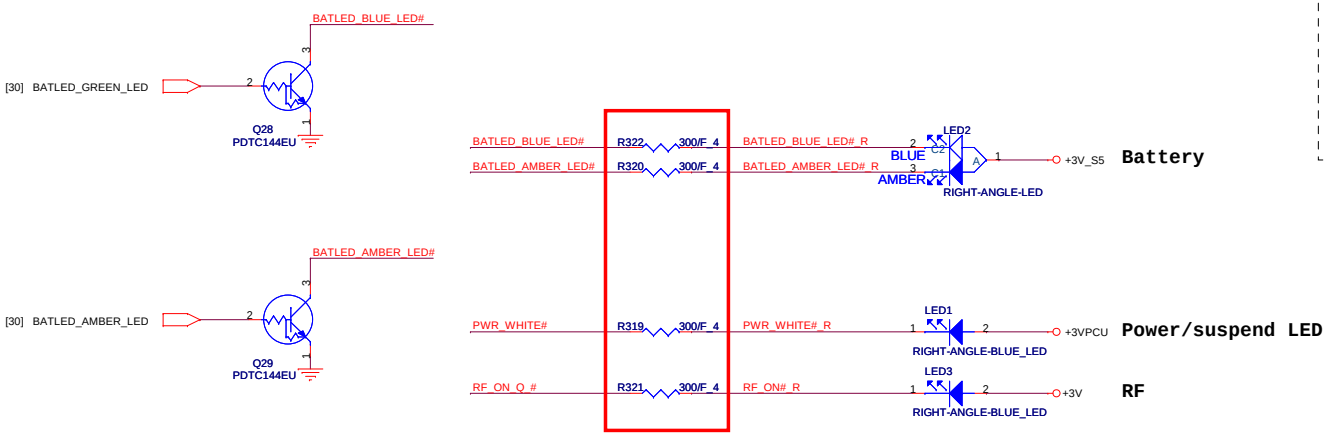
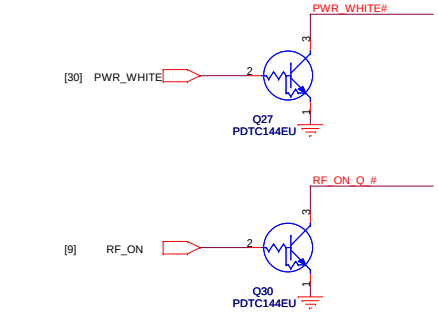
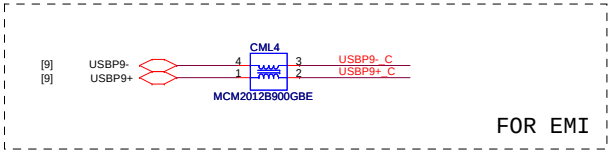
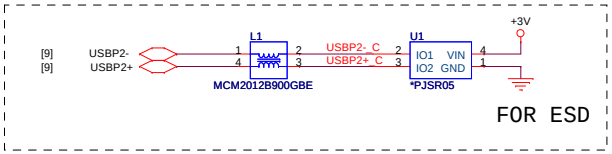
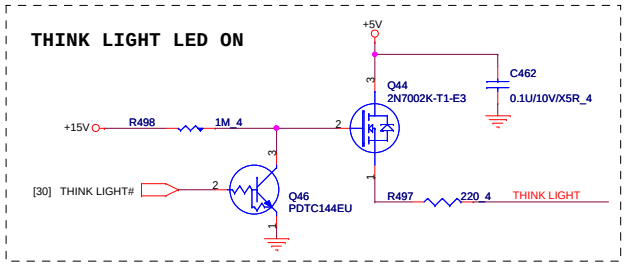
[7,8,9,10,11,13,14,15,16,17,19,20,21,22,23,24,25,27,30,32,33,37,38,39] +3V
[11,17,20,23,31,32] +5V_S5
[3,7,8,9,10,11,18,22,23,25,32] +3V_S5
[7,8,11,15,16,19,20,25,26,27,28,30,32,33,39] +5V

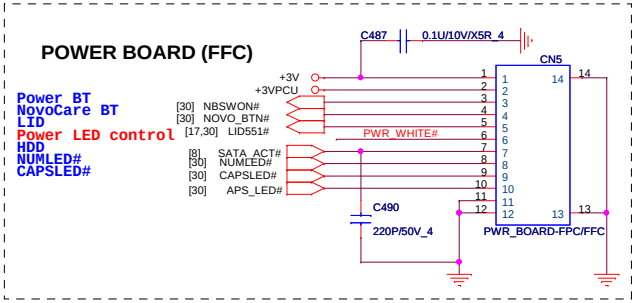


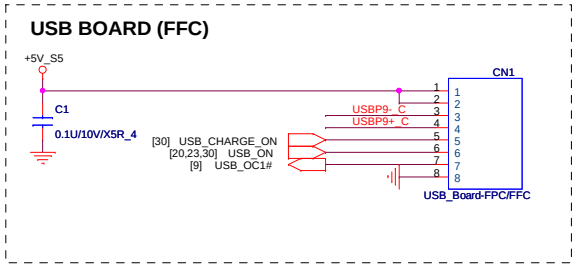


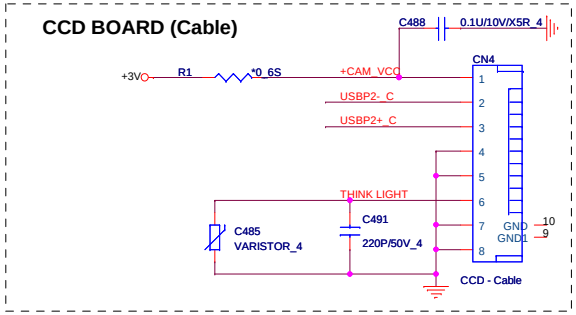


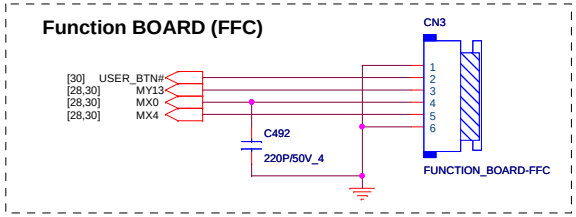












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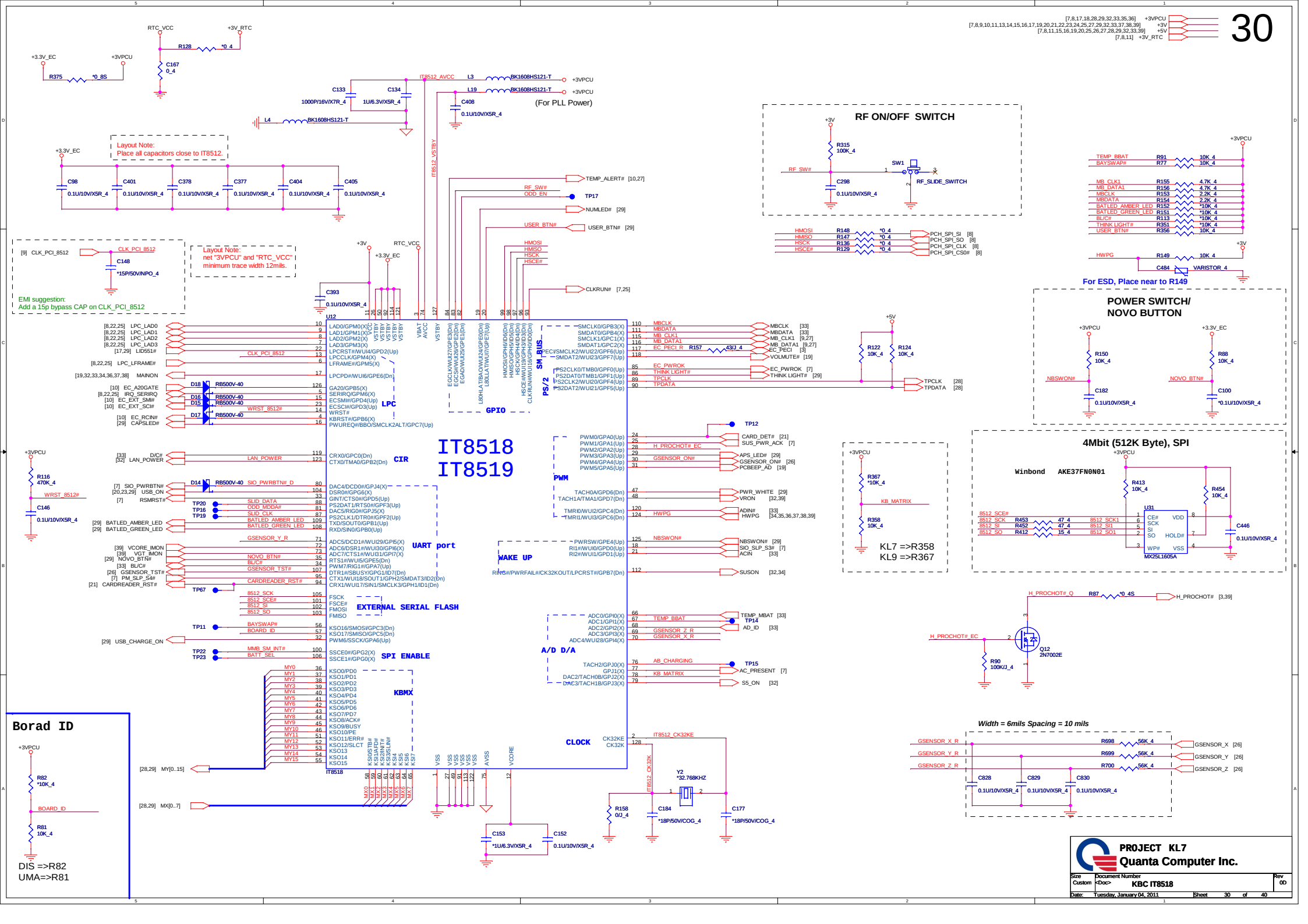
IT8518
IT8519
RF ON/OFF SWITCH
POWER SWITCH/
NOVO BUTTON
4Mbit (512K Byte), SPI
Winbond AKE37FN0N01
MX25L1605A
Borad ID
DIS =>R82
UMA=>R81
KL7 =>R358
KL9 =>R367
(For PLL Power)
Layout Note:
Place all capacitors close to IT8512.
Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.
EMI suggestion:
Add a 15p bypass CAP on CLK_PCI_8512
For ESD, Place near to R149
Width = 6mils Spacing = 10 mils
LPC
GPIO
PS/2
SM BUS
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
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Screw for ME

[11,17,20,23,29,32] +5V_S5

WLAN Nut

Guide pin
H=7mm
(STD)

HOLE22 H-TC217BIC102D63P2
HOLE19 H-TC217BIC102D63P2

H=4mm/7mm

HOLE21 H-TC217BC142D102P2
HOLE20 H-TC217BC142D102P2

SMT NUT H=4/7mm	TBD

PCH Thermal module Nut

Screw - h-tc218bc118i60d60p2

HOLE12 h-tc218bc118i60d60p2
HOLE10 h-tc218bc118i60d60p2

CPU BKT

BKT1
(PTH)
4
3
2
1
cpu-bracket

+5V_S5 C493 560P/50V_4
+5V_S5 C494 560P/50V_4

TPM Nut

Screw - h-tc218bc118i60d60p2

HOLE13 h-tc218bc118i60d60p2
HOLE11 h-tc218bc118i60d60p2
HOLE25 H-TC218BIC60D60NPT

Nut of Minipci(高度為4mm/7mm): H-TC217BC142D102P2 (內層PAD與bottom pad相同 142mil)

Guide of Minipci(高度為4mm): H-TC217BC75I75D35P2 (內層PAD與bottom pad相同 75mil)

Guide of Minipci(高度為7mm): H-TC217BIC102D63P2 (內層PAD與bottom pad相同 102mil)

Nut of VGA: H-TC5_5BC4I3D3P2 (內層不留PAD; 與孔相同 118mil)

Screw - h-c236d90p2

HOLE7 *h-kl7-hdd
HOLE6 *H-C236D236N

HOLE4 *HG-C315D91P2
HOLE3 *HG-C315D91P2

HOLE15 *HG-TKL7BC315D90P2-1
HOLE9 *HG-C315D91P2
HOLE18 *HG-tkl7bc315d91p2-1

AGND

Drink Hole

HOLE8 *h-c274d274na314

ME定位孔

HOLE5 *h-o86x94d86x94n
HOLE14 *h-o55x47d55x47n

HOLE24 *Hg-C236D90P2

Screw for ME

HOLE16 *H-tkl7bc315d87p2-1
HOLE17 H-C236D87P2

HOLE2 *HG-C315D87P2

HOLE23 *spad-re259x213np

PAD1 *spad-s440np

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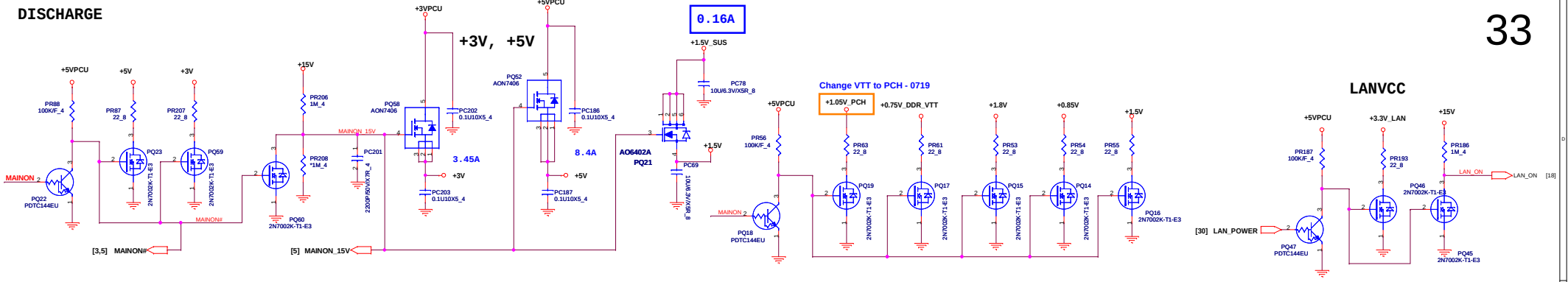
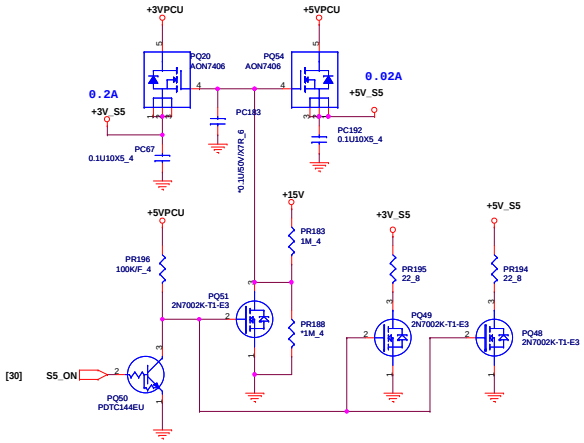
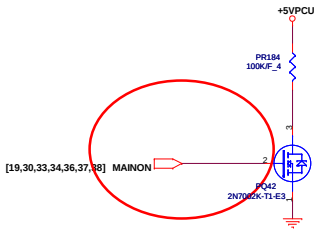
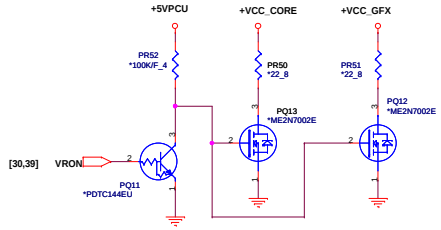
DISCHARGE

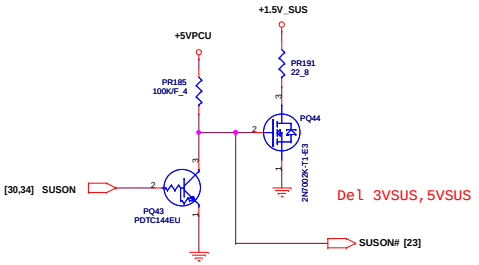


3V_S5, 5V_S5









PROJECT KL7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discharge	0D

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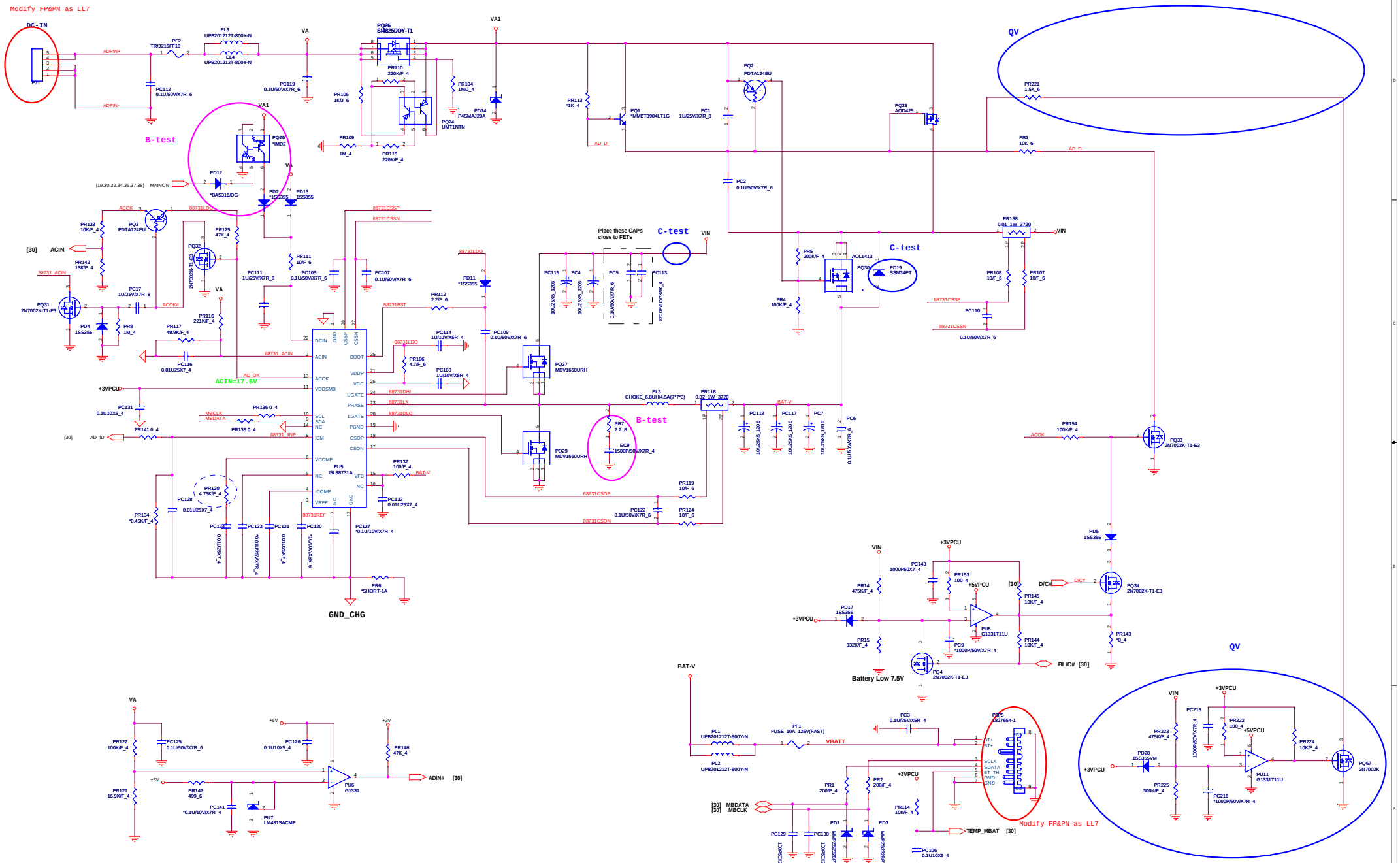

PROJECT KL7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Charger (ISL88731)	0D

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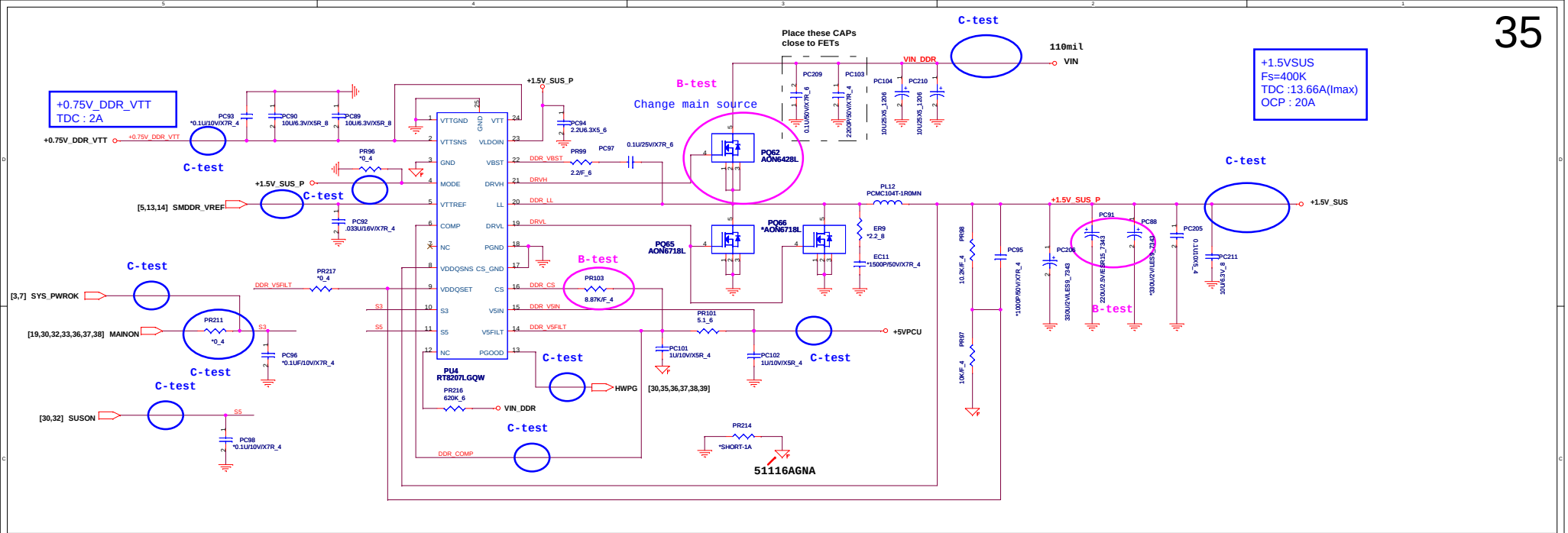

5. Delet IFPAB_IOVDD (+1.8V_GPU)

PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3/0.75V(RT8207LGQW)	0D

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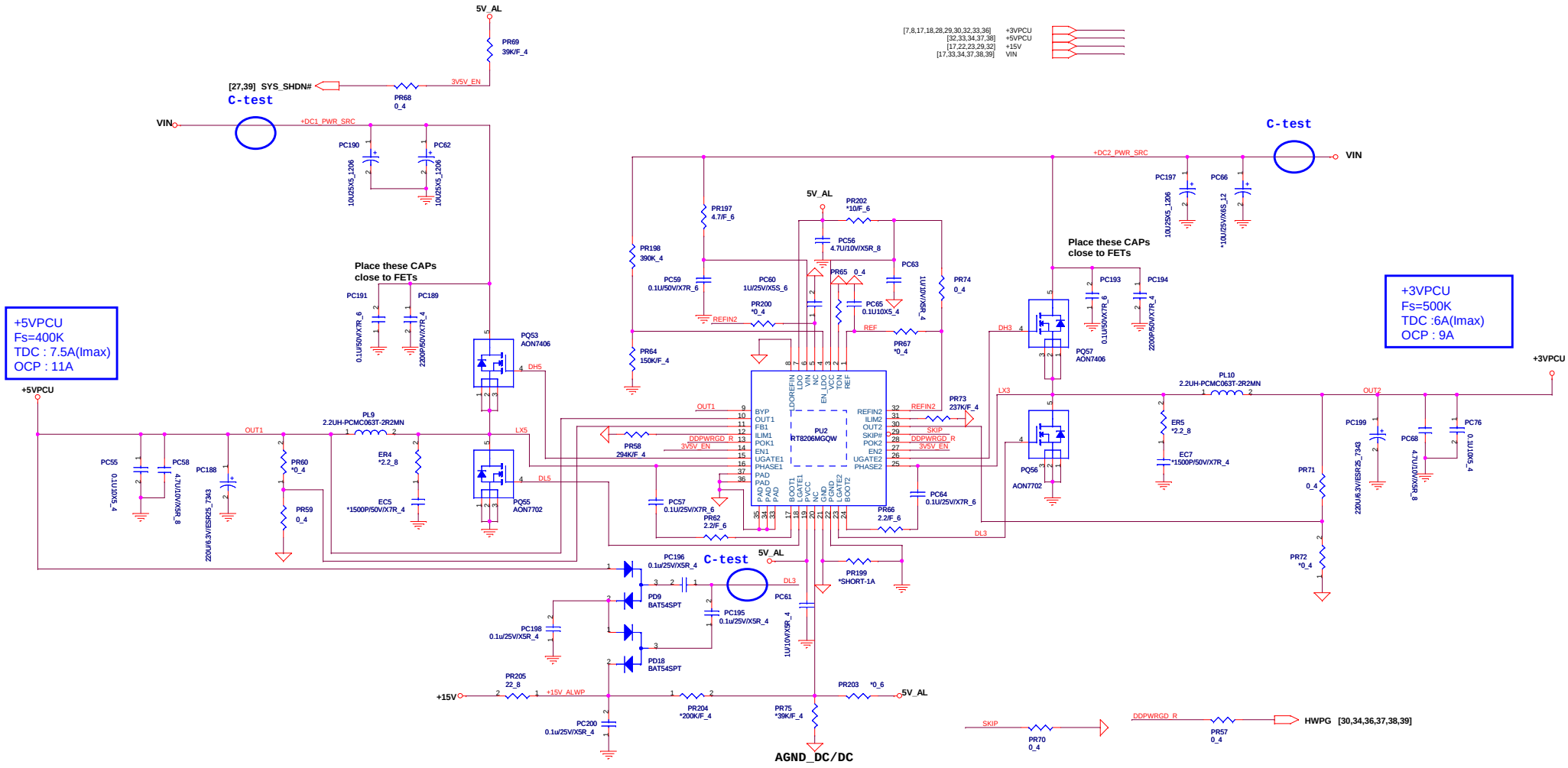

[7,8,17,18,28,29,30,32,33,36]	+3VPCU
[32,33,34,37,38]	+5VPCU
[17,22,23,29,32]	+15V
[17,33,34,37,38,39]	VIN

PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
C	3V/5V (RT8206MGQW)	0D

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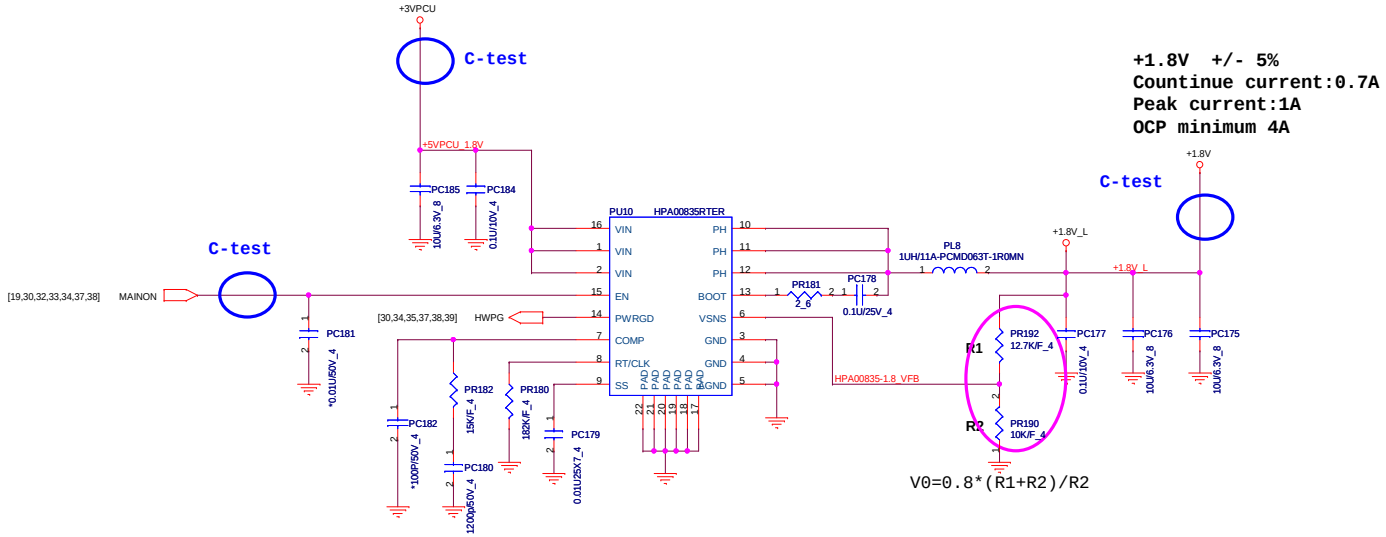

+1.8V +/- 5%
Countinue current:0.7A
Peak current:1A
OCP minimum 4A

4. Delete FBVDDQ (+1.8V_GPU)

PROJECT KL5A Quanta Computer Inc.		
Size Custom	Document Number +1.8V (HPA00835RTER)	Rev 0D
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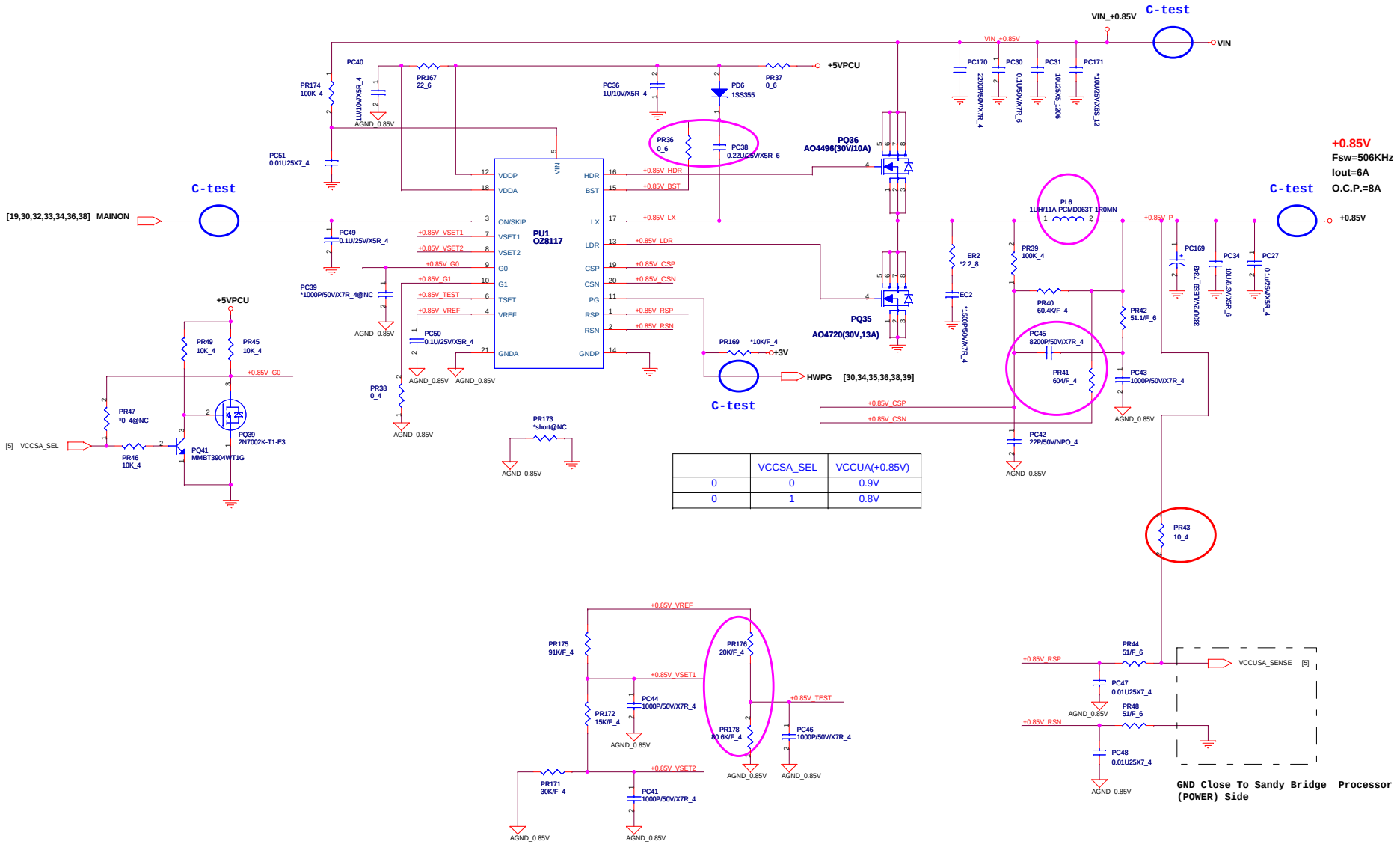

	VCCSA_SEL	VCCUA(+0.85V)
0	0	0.9V
0	1	0.8V

PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
C	+0.85V (OZ8117)	0D

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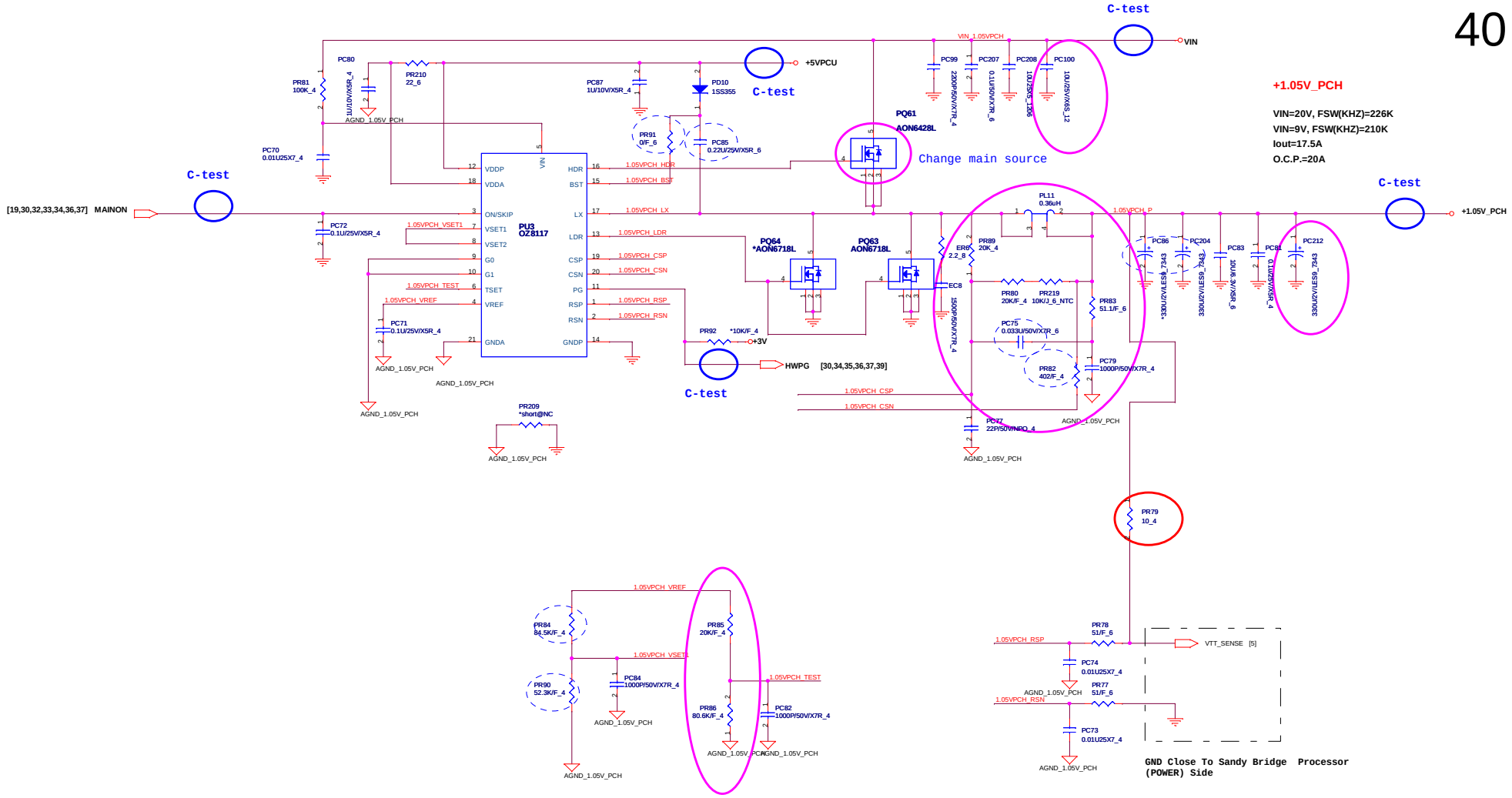

Delete - 1. PEX_VDD (+1.05V)

Delete - 2. VDD33 (+3.3V)

Delete For power-down sequency

Del +1.5V SW

PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.05_PCH (OZ8117)	0D

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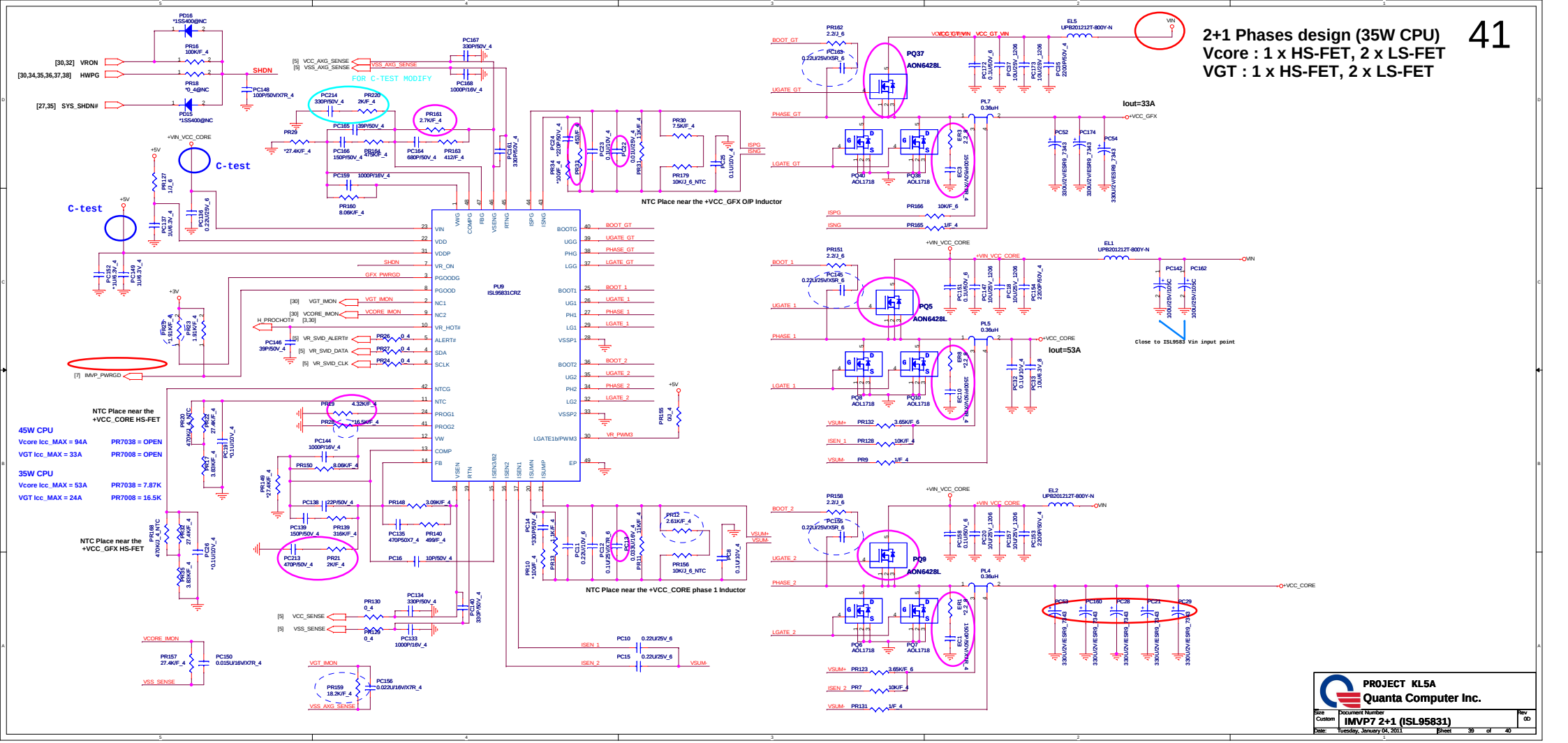
2+1 Phases design (35W CPU)
Vcore : 1 x HS-FET, 2 x LS-FET
VGT : 1 x HS-FET, 2 x LS-FET
41
PU9
ISL95831CRZ
PQ37
AON6428L
PQ5
AON6428L
PQ9
AON6428L
Iout=33A
Iout=53A
NTC Place near the +VCC_GFX O/P Inductor
NTC Place near the +VCC_CORE phase 1 Inductor
NTC Place near the +VCC_CORE HS-FET
NTC Place near the +VCC_GFX HS-FET
45W CPU
Vcore Icc_MAX = 94A
VGT Icc_MAX = 33A
PR7038 = OPEN
PR7008 = OPEN
35W CPU
Vcore Icc_MAX = 53A
VGT Icc_MAX = 24A
PR7038 = 7.87K
PR7008 = 16.5K
C-test
FOR C-TEST MODIFY
Close to ISL9583 Vin input point
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Quanta Computer Inc.
Size Custom
Document Number
IMVP7 2+1 (ISL95831)
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KL7 Intel HW Schematic EC Tracking Record B (for SIV)10 /06/ 2010

EC #	Page	CMVC #	Description	Date	Part Affected
01	03		Remove Disable Internal VGA circuit	2010/10/06	R33,R34,R35,R36,R37,R356,R358
02	03		Change U22 P/N to make sure output is 1.5V level	2010/10/06	U22
03	04		Remove CPU_DRAMRST# from +3V_S5	2010/10/06	R51,R52
04	05		Remove Disable Internal VGA circuit	2010/10/06	R351
05	07		Follow Intel PDG to remove HPD pull-up resister	2010/10/06	R159,R398
06	08		Change compoment footprint and P/N for KL789 common parts.	2010/10/06	BT1,D6
07	08		Remove PCH JTAG pull-up/pull-down resister for S3 leakage issue	2010/10/06	R464,R469,R229,R220,R228,R219,R476
08	08		Change Y6 Load Capacitance value from 18P to 6P	2010/10/06	C481,C482
09	09		Add MB ID[3,4] to separate KL789 model	2010/10/06	
10	09		Follow Intel PDG to add pull-up resister for PCIECLKRQ0,5,6,7 and PEG_CLKREQ#, and change GPIO46 from THINK_LIGHT# to PCIECLKRQ7#	2010/10/06	R402,R488,R489,R532,R234,R221
11	09		Change Y4 Load Capacitance value from 18P to 27P	2010/10/06	C406,C413
12	10		Change GPIO6 to BOARD_ID0, and GPIO68 to BOARD_ID1	2010/10/06	
13	10		Correct PCH strap netname(GPIO36,37)	2010/10/06	
14	10		Remove un-used compoment	2010/10/06	R207,R216,R215
15	10		Add MB ID[3,4] to separate KL789 model	2010/10/06	R398,R377,R542,R543
16	10		Add a pull-up resister for "WLAN_OFF#"	2010/10/06	R370
17	11		Follow Intel PDG to remove un-used compoment and add test point	2010/10/06	L17,C396,R387,R145,R166,L18,C399,R519,C243,L20,C417,TP82,TP83,TP66,TP44,TP18
18	15		Add a 220P CAP on "HDMIC_5V" for EMI	2010/10/06	C489
19	17		Correct LVDS conn pin define as KL8/9	2010/10/06	CN2
20	18		"LAN_DISABLE#" has a pull-up resister on PCH side, so de-pop this resister	2010/10/06	R67
21	18		Disconnect LED1 and LED2 by Intel suggestion	2010/10/06	
22	18		Change C88 from 0.1U to 1U by Intel suggestion	2010/10/06	C88
23	18		Remove "+1.0V_LOM" source from +1.05V_PCH	2010/10/06	R74
24	18		Change C420 from 1000P/3KV to 10P/3KV for EMI	2010/10/06	C420
25	20		Swap U9.4 and U9.5 and correct U9 P/N	2010/10/06	U9
26	20		Correct 0ohm resister and common choke co-layout circuit for USB	2010/10/06	R540,R541
27	21		Change R475 from short-pad to 0ohm resister for power consumption measure.	2010/10/06	R475
28	21		Add SD_D4~D7 to support SDXC	2010/10/06	CN11
29	22		Correct mini-card pin define for debug card	2010/10/06	CN22
30	22		Change CN18 footprint and P/N for ME request	2010/10/06	CN18
31	23		Swap U20.30 and U20.31	2010/10/06	
32	23		Change Y3 Load Capacitance value from 27P to 33P	2010/10/06	C297,C289
33	23		Remove LDO and connect +1.05V_PCH to P1V05_SUS, and change R316 footprint from 0603 to 0402	2010/10/06	U37,R488,R489,C461,C463,C464,R533, R532,C484,C485,R387,R316
34	24		Change CN17 pin define by SSD spec, and remove un-used compoment	2010/10/06	R377,R367,R370,D4,R60,U27
35	25		Correct 0ohm resister and common choke co-layout circuit for USB	2010/10/06	R538,R539
36	27		Change FAN connector pin define for quanta common design	2010/10/06	CN14
37	28		Pop CA1~CA6 for EMI request	2010/10/06	CA1,CA2,CA3,CA4,CA5,CA6
38	29		Change LED footprint and P/N, and connect LED1 from +3V_S5 to 3VPCU, and change R319~R322 footprint from 0603 to 0402	2010/10/06	LED1,LED2,LED3,R319,R320,R321,R322
39	29		Correct 0ohm resister and common choke co-layout circuit for USB	2010/10/06	R536,R537
40	29		Add 220P CAP for EMI request	2010/10/06	C490,C491,C492
41	29		Change CN3 pin define	2010/10/06	CN3
42	30		De-pop Y2,C184,C177 and pop R515 for CX version EC	2010/10/06	Y2,C184,C177,R515
43	30		Swap U12 pin for NB2 common design	2010/10/06	
44	30		Add 10K pull-up resister for "THINK LIGHT#"and"USER_BTN#"	2010/10/06	R351,R356
45	30		Reserve VARISTOR on "HWPG" for ESD	2010/10/06	C484
46	30		Pop R88 for auto power on issue	2010/10/06	R88
47	30		Use a GPIO to separate KL7 and KL9 keyboard matrix	2010/10/06	R358,R367
48	30		Pop R81 and de-pop R82 for charger current control	2010/10/06	R81,R82
49	31		Add 560P CAP on +5V_S5 for EMI request	2010/10/06	C493,C494