

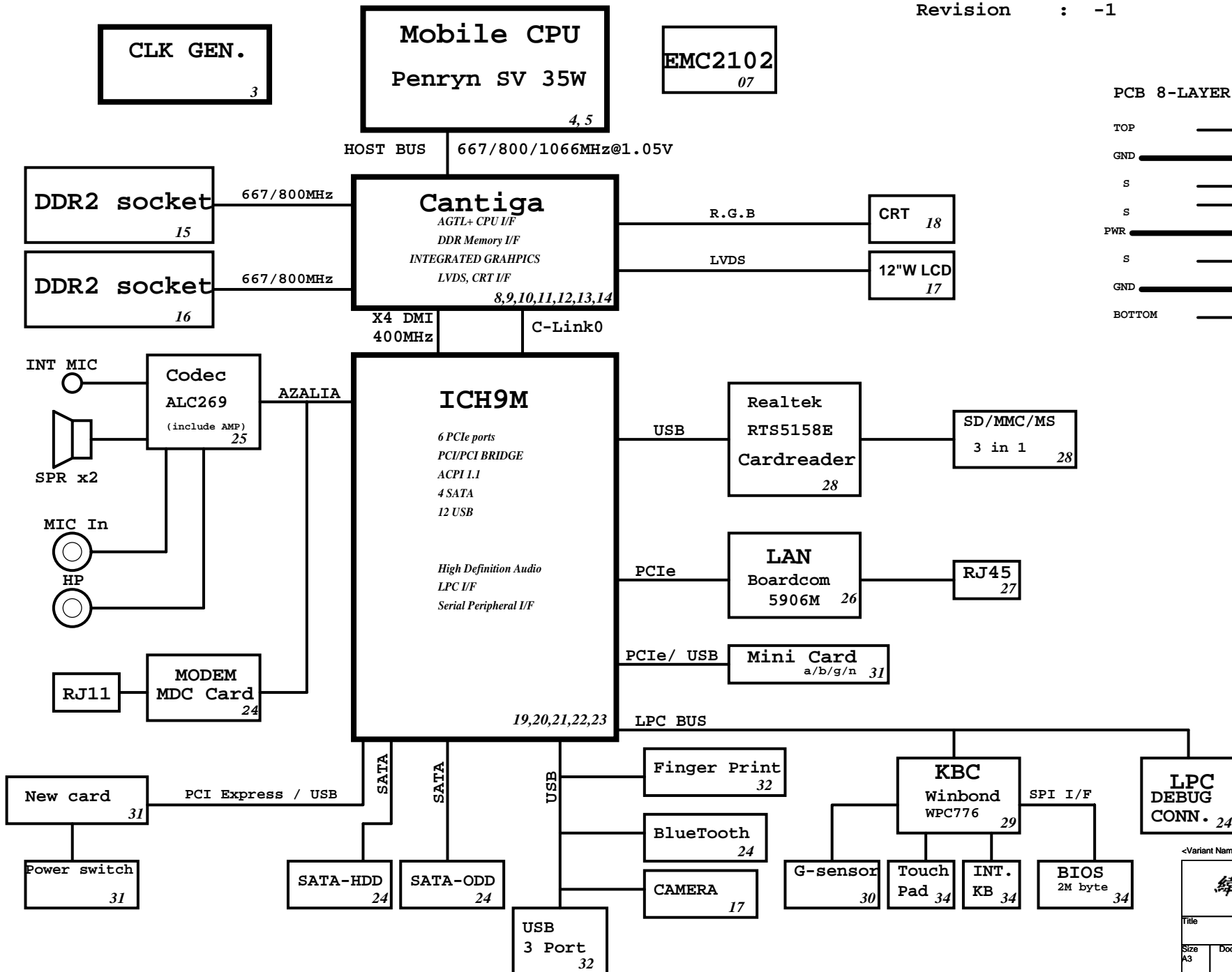
LZ2 Block Diagram

Project code: 91.4K101.001 ZY LZ2
91.4J301.001 XR LX2
PCB P/N : 07260-1
Revision : -1

PCB 8-LAYER STACKUP

TOP _____
GND _____
S _____
S _____
PWR _____
S _____
GND _____
BOTTOM _____

| SYSTEM DC/DC TPS51120 36 | |
|-----------------------------|--------------------------------------|
| INPUTS | OUTPUTS |
| DCBATOUT | 5V_S5 3D3V_S5 |
| SYSTEM DC/DC TPS51124 37 | |
| INPUTS | OUTPUTS |
| DCBATOUT | 1D05V_S0 1D8V_S3 |
| TPS51100 38 | |
| 1D8V_S3 | DDR_VREF_S0 (1.5A) DDR_VREF_S3 |
| APL5912 38 | |
| 1D8V_S3 | 1D5V_NB_S0 |
| APL5912 38 | |
| 1D8V_S3 | 1D5V_SB_S0 |
| CHARGER BQ24740 39 | |
| INPUTS | OUTPUTS |
| DCBATOUT | CHG_PWR 18V UP+5V 5V 100mA |
| CPU DC/DC ADP3208 35 | |
| INPUTS | OUTPUTS |
| DCBATOUT | VCC_CORE |



<Variant Name>

| 緯創資通 Wistron Corporation | |
|--|-----------------|
| 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| BLOCK DIAGRAM | |
| Size | Document Number |
| A3 | LZ2 |
| Date: | Rev |
| Wednesday, May 28, 2008 | SB |
| Sheet | of |
| 1 | 41 |

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

| Signal | Usage/When Sampled | Comment |
|-------------------------------|---|---|
| HDA_SDOUT | XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK | Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down. |
| HDA_SYNC | PCIE config1 bit0, Rising Edge of PWROK. | This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h) |
| GNT2#/GPIO53 | PCIE config2 bit2, Rising Edge of PWROK. | This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h) |
| GPIO20 | Reserved Rising Edge of PWROK. | This signal has a weak internal pull-down. Note: This signal should not be pulled high. |
| GNT1#/GPIO51 | ESI Strap(Server Only) Rising edge of PWROK | Tying this strap low configures DMI for Sicompatible operation. This signal has a weak internal pull-up. NOTE: ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile. |
| GNT3#/GPIO55 | Top-Block Swap Override. Rising Edge of PWROK. | Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down. |
| GNT0#: SPI_CS1#/ GPIO58 | Boot BIOS Destination Selection 0:1. Rising Edge of PWROK. | Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h: bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC. |
| SPI_MOSI | Integrated TPM Enable, Rising Edge of CLPWROK | Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM disable bit is clear, the Integrated TPM will be enable. |
| GPIO49 | DMI Termination Voltage, Rising Edge of PWROK. | The signal is required to be low for desktop applications and required to be high for mobile applications. |
| SATALED# | PCI Express Lane Reversal. Rising Edge of PWROK. | Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8) |
| SPKR | No Reboot. Rising Edge of PWROK. | If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO timer system reboot feature). The status is readable via the NO REBOOT bit. |
| TP3 | XOR Chain Entrance. Rising Edge of PWROK. | This signal should not be pull low unless using XOR Chain testing. |
| GPIO33/ HDA_DOCK_EN# | Flash Descriptor Security Override Strap Rising Edge of PWROK | Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor. |

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

| SIGNAL | Resistor Type/Value |
|--------------------------|---|
| CL_CLK[1:0] | PULL-UP 20K |
| CL_DATA[1:0] | PULL-UP 20K |
| CL_RST0# | PULL-UP 20K |
| DPRSLPVR/GPIO16 | PULL-DOWN 20K |
| ENERGY_DETECT | PULL-UP 20K |
| HDA_BIT_CLK | PULL-DOWN 20K |
| HDA_DOCK_EN#/GPIO33 | PULL-UP 20K |
| HDA_RST# | PULL-DOWN 20K |
| HDA_SDIN[3:0] | PULL-DOWN 20K |
| HDA_SDOUT | PULL-DOWN 20K |
| HDA_SYNC | PULL-DOWN 20K |
| GLAN_DOCK# | The pull-up or pull-down active when configured for native LAN DOCK# functionality and determined by LAN controller |
| GNT[3:0]#/GPIO[55,53,51] | PULL-UP 20K |
| GPIO[20] | PULL-DOWN 20K |
| GPIO[49] | PULL-UP 20K |
| LDA[3:0]#/FWH[3:0]# | PULL-UP 20K |
| LAN_RXD[2:0] | PULL-UP 20K |
| LDRQ[0] | PULL-UP 20K |
| LDRQ[1]/GPIO23 | PULL-UP 20K |
| PME# | PULL-UP 20K |
| PWRBTN# | PULL-UP 20K |
| SATALED# | PULL-UP 15K |
| SPI_CS1#/GPIO58/CLGPIO6 | PULL-UP 20K |
| SPI_MOSI | PULL-DOWN 20K |
| SPI_MISO | PULL-UP 20K |
| SPKR | PULL-DOWN 20K |
| TACH_[3:0] | PULL-UP 20K |
| TP[3] | PULL-UP 20K |
| USB[11:0][P,N] | PULL-DOWN 15K |

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5
page 218

| Pin Name | Strap Description | Configuration |
|--|---|--|
| CFG[2:0] | FSB Frequency Select | 000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved |
| CFG[4:3] CFG8 CFG11 CFG[15:14] CFG[18:17] | Reserved | |
| CFG5 | DMI x2 Select | 0 = DMI x2 1 = DMI x4 (Default) |
| CFG6 | iTPM Host Interface | 0 = The iTPM Host Interface is enabled (Note2) 1 = The iTPM Host Interface is disabled (default) |
| CFG7 | Intel Management engine Crypto strap | 0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default) |
| CFG9 | PCIE Graphics Lane | 0 = Reverse Lanes 15->0, 14->1 ect.. 1 = Normal operation (Default): Lane Numbered in order |
| CFG10 | PCIE Loopback enable | 0 = Enable (Note 3) 1 = Disabled (default) |
| CFG[13:12] | XOR/ALL | 00 = Reserve 10 = XOR mode Enabled 01 = ALL2 mode Enabled (Note 3) 11 = Disabled (default) |
| CFG16 | FSB dynamic ODT | 0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default) |
| CFG19 | DMI Lane Reversal | 0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH -> ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH -> ICH]: (3->0, 2->1) |
| CFG20 | Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe | 0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simultaneously via the PEG port |
| SDVO_CTRLDATA | SDVO Present | 0 = No SDVO Card Present (Default) 1 = SDVO Card Present |
| L_DDC_DATA | Local Flat Panel (LFP) Present | 0 = LFP Disabled (Default) 1 = LFP Card Present / PCIE disabled |

NOTE:

- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-Descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
- Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

| | | |
|--|------------|------------|
| 17,33,35,36,37,39,41 | DCBATOUT | DCBATOUT |
| 7,19,29,34,36,39,40 | 3DV_AUX_S5 | 3DV_AUX_S5 |
| 7,31,33,36,39 | 5V_AUX_S5 | 5V_AUX_S5 |
| 17,20,21,22,23,24,26,29,30,31,33,34,36,41 | 3DV_S5 | 3DV_S5 |
| 22,32,33,36,37,38,41 | 5V_S5 | 5V_S5 |
| 10,12,13,15,16,33,37,38,41 | 1D8V_S3 | 1D8V_S3 |
| 3,7,10,11,13,15,16,17,18,19,20,21,22,23,24,25,26,28,29,31,32,33,34,35,36,37,41 | 3DV_S0 | 3DV_S0 |
| 7,13,17,18,22,23,24,25,33,34,35,41 | 5V_S0 | 5V_S0 |
| 4,5,6,8,10,11,12,13,19,22,33,37 | 1D05V_S0 | 1D05V_S0 |
| 19,20,22,31,33,38 | 1D5V_SB_S0 | 1D5V_SB_S0 |
| 3,5,13,31,33,38 | 1D5V_NB_S0 | 1D5V_NB_S0 |

PCIE Routing

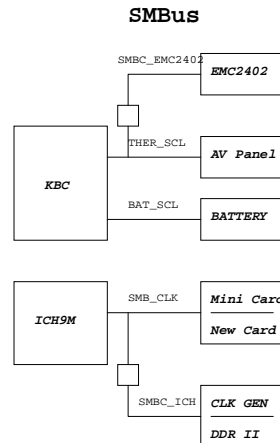
| | |
|-------|---------------|
| LANE1 | BroadCom LAN |
| LANE2 | MiniCard WLAN |
| LANE4 | NewCard |

History:

LAB: 2008/01/02

USB Table

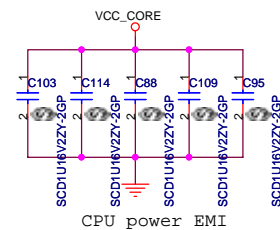
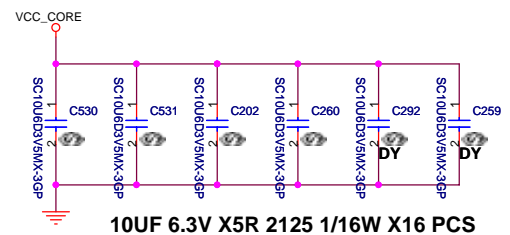
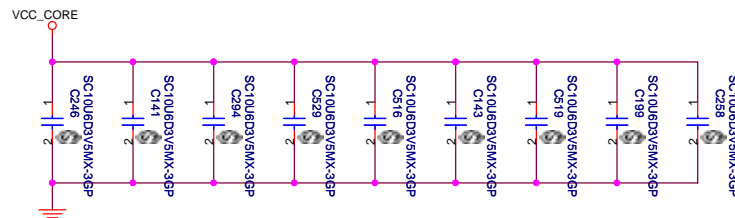
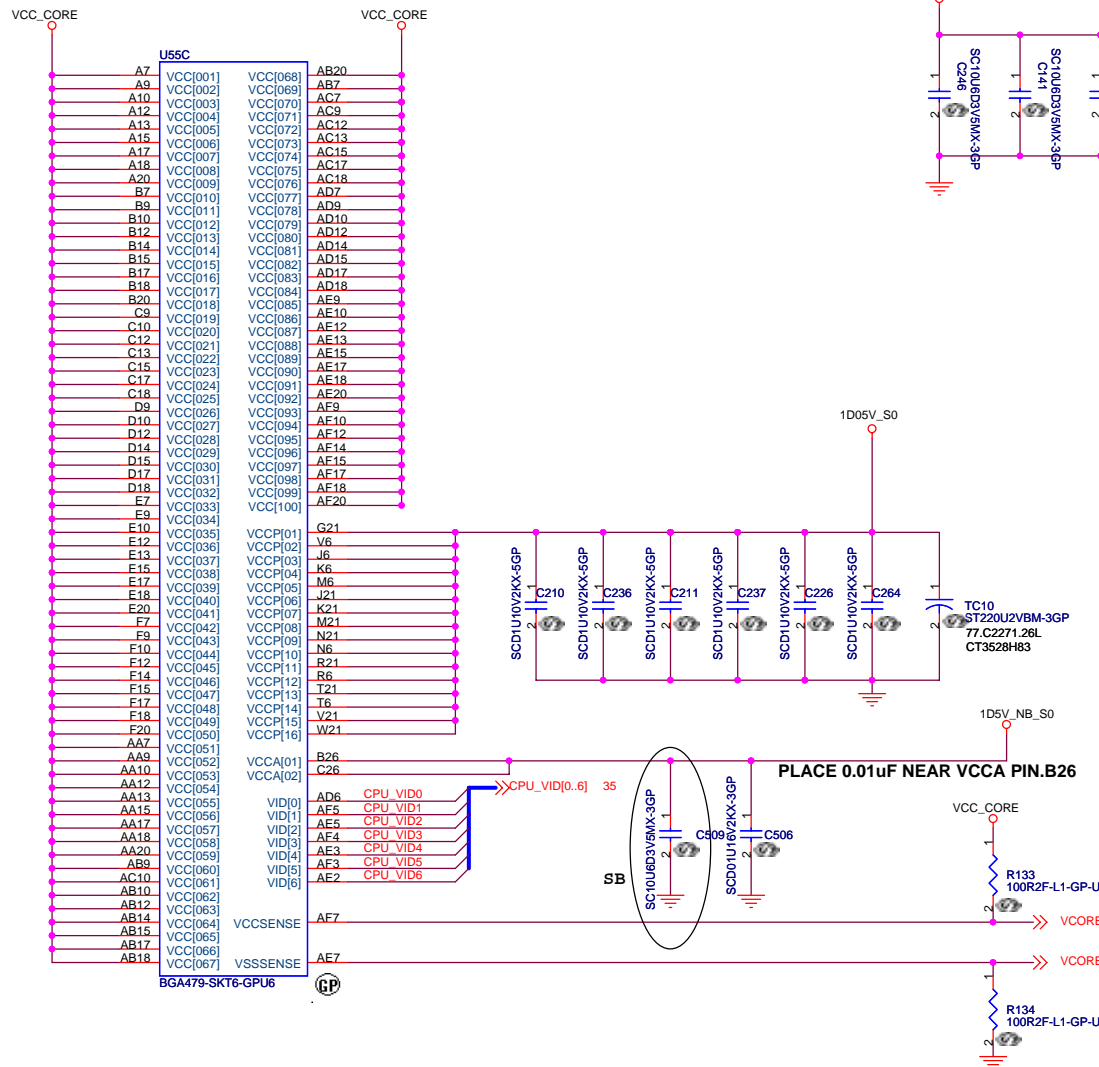
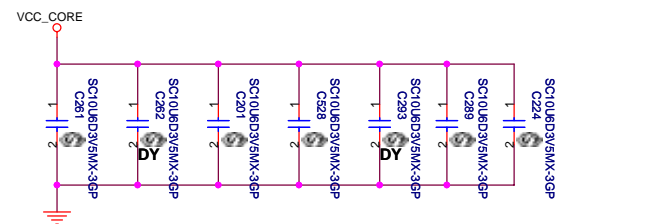
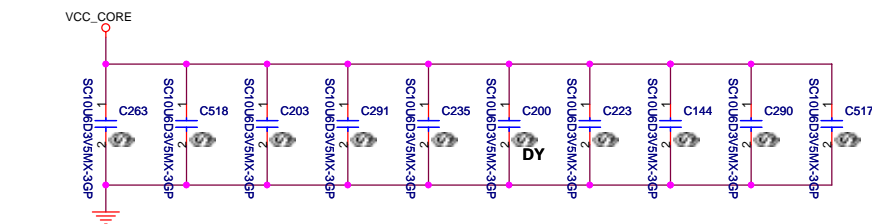
| USB | |
|------|--------------|
| Pair | Device |
| 0 | JACK0 |
| 1 | NC |
| 2 | JACK2 |
| 3 | NC |
| 4 | BLUETOOTH |
| 5 | JACK1 |
| 6 | Finger Print |
| 7 | Mini Card |
| 8 | CAMERA |
| 9 | NEW CARD |
| 10 | CARDREADER |
| 11 | NC |



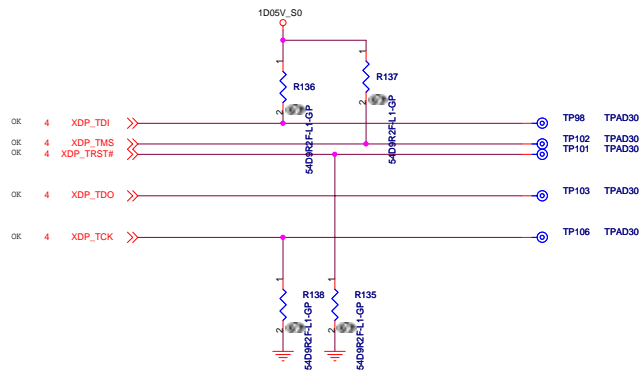
<Variant Name>

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| | | | | |
|-------|-------------------------|-----------|-------|-------|
| File | | Reference | | Rev |
| Size | Document Number | LZ2 | Sheet | SB |
| Date: | Thursday, June 05, 2008 | Sheet | 2 | of 41 |

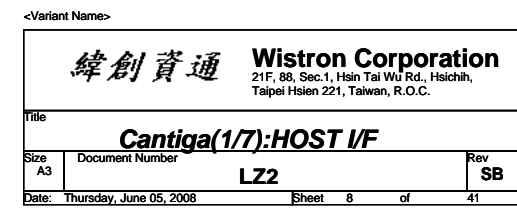


| U55D | | |
|------|-----------|-----------|
| A4 | VSS[0001] | VSS[0082] |
| A8 | VSS[0002] | VSS[0083] |
| A11 | VSS[0003] | VSS[0084] |
| A14 | VSS[0004] | VSS[0085] |
| A16 | VSS[0005] | VSS[0086] |
| A19 | VSS[0006] | VSS[0087] |
| A23 | VSS[0007] | VSS[0088] |
| A2 | VSS[0008] | VSS[0089] |
| B6 | VSS[0009] | VSS[0090] |
| B8 | VSS[0100] | VSS[0091] |
| B11 | VSS[0101] | VSS[0092] |
| B13 | VSS[0102] | VSS[0093] |
| B16 | VSS[0103] | VSS[0094] |
| B19 | VSS[0104] | VSS[0095] |
| B21 | VSS[0105] | VSS[0096] |
| B24 | VSS[0106] | VSS[0097] |
| C5 | VSS[0107] | VSS[0098] |
| C8 | VSS[0108] | VSS[0099] |
| C11 | VSS[0109] | VSS[0100] |
| C14 | VSS[0200] | VSS[0101] |
| C16 | VSS[0201] | VSS[0102] |
| C19 | VSS[0202] | VSS[0103] |
| C2 | VSS[0203] | VSS[0104] |
| C22 | VSS[0204] | VSS[0105] |
| C25 | VSS[0205] | VSS[0106] |
| D1 | VSS[0206] | VSS[0107] |
| D4 | VSS[0207] | VSS[0108] |
| D8 | VSS[0208] | VSS[0109] |
| D11 | VSS[0209] | VSS[0110] |
| D13 | VSS[0300] | VSS[0111] |
| D16 | VSS[0301] | VSS[0112] |
| D19 | VSS[0302] | VSS[0113] |
| D23 | VSS[0303] | VSS[0114] |
| D26 | VSS[0304] | VSS[0115] |
| E3 | VSS[0305] | VSS[0116] |
| F6 | VSS[0306] | VSS[0117] |
| F8 | VSS[0307] | VSS[0118] |
| F11 | VSS[0308] | VSS[0119] |
| F14 | VSS[0309] | VSS[0120] |
| F16 | VSS[0400] | VSS[0121] |
| F19 | VSS[0401] | VSS[0122] |
| F21 | VSS[0402] | VSS[0123] |
| F24 | VSS[0403] | VSS[0124] |
| F5 | VSS[0404] | VSS[0125] |
| F8 | VSS[0405] | VSS[0126] |
| F11 | VSS[0406] | VSS[0127] |
| F13 | VSS[0407] | VSS[0128] |
| F16 | VSS[0408] | VSS[0129] |
| F19 | VSS[0409] | VSS[0130] |
| F2 | VSS[0500] | VSS[0131] |
| F25 | VSS[0501] | VSS[0132] |
| G4 | VSS[0502] | VSS[0133] |
| G1 | VSS[0503] | VSS[0134] |
| G23 | VSS[0504] | VSS[0135] |
| G26 | VSS[0505] | VSS[0136] |
| H3 | VSS[0506] | VSS[0137] |
| H6 | VSS[0507] | VSS[0138] |
| H21 | VSS[0508] | VSS[0139] |
| H24 | VSS[0509] | VSS[0140] |
| J2 | VSS[0600] | VSS[0141] |
| J6 | VSS[0601] | VSS[0142] |
| J22 | VSS[0602] | VSS[0143] |
| J25 | VSS[0603] | VSS[0144] |
| K1 | VSS[0604] | VSS[0145] |
| K4 | VSS[0605] | VSS[0146] |
| K23 | VSS[0606] | VSS[0147] |
| K26 | VSS[0607] | VSS[0148] |
| L3 | VSS[0608] | VSS[0149] |
| L6 | VSS[0609] | VSS[0150] |
| L21 | VSS[0700] | VSS[0151] |
| L24 | VSS[0701] | VSS[0152] |
| M2 | VSS[0702] | VSS[0153] |
| M5 | VSS[0703] | VSS[0154] |
| M22 | VSS[0704] | VSS[0155] |
| M25 | VSS[0705] | VSS[0156] |
| N1 | VSS[0706] | VSS[0157] |
| N4 | VSS[0707] | VSS[0158] |
| N23 | VSS[0708] | VSS[0159] |
| N26 | VSS[0709] | VSS[0160] |
| P3 | VSS[0800] | VSS[0161] |
| B1 | VSS[0801] | VSS[0162] |
| | VSS | VSS[0163] |



Layout notice : Both DN3 and DP3 routing
10 mil trace width and 10 mil spacing





15 M_A_DQ[63..0] <<>>
15 M_A_DM[7..0] <<>>
15 M_A_DQS[7..0] <<>>
15 M_A_DQS# [7..0] <<>>
15 M_A_A[14..0] <<>>

16 M_B_DQ[63..0] <<>>
16 M_B_DM[7..0] <<>>
16 M_B_DQS[7..0] <<>>
16 M_B_DQS# [7..0] <<>>
16 M_B_A[14..0] <<>>

| U56D | | | 4 OF 10 |
|---------|------|----------|---------|
| M_A_D00 | AJ38 | SA_D0_0 | BD21 |
| M_A_D01 | AJ38 | SA_D0_1 | BD21 |
| M_A_D02 | AN38 | SA_D0_2 | BD21 |
| M_A_D03 | AM38 | SA_D0_3 | BD21 |
| M_A_D04 | AJ38 | SA_D0_4 | BD21 |
| M_A_D05 | AJ40 | SA_D0_5 | BD21 |
| M_A_D06 | AM44 | SA_D0_6 | BD21 |
| M_A_D07 | AM42 | SA_D0_7 | BD21 |
| M_A_D08 | AN43 | SA_D0_8 | BD21 |
| M_A_D09 | AN44 | SA_D0_9 | BD21 |
| M_A_D10 | AJ40 | SA_D0_10 | BD21 |
| M_A_D11 | AT38 | SA_D0_11 | BD21 |
| M_A_D12 | AN41 | SA_D0_12 | BD21 |
| M_A_D13 | AN39 | SA_D0_13 | BD21 |
| M_A_D14 | AJ44 | SA_D0_14 | BD21 |
| M_A_D15 | AJ42 | SA_D0_15 | BD21 |
| M_A_D16 | AJ42 | SA_D0_16 | BD21 |
| M_A_D17 | AY44 | SA_D0_17 | BD21 |
| M_A_D18 | BA40 | SA_D0_18 | BD21 |
| M_A_D19 | BD43 | SA_D0_19 | BD21 |
| M_A_D20 | AV41 | SA_D0_20 | BD21 |
| M_A_D21 | AY43 | SA_D0_21 | BD21 |
| M_A_D22 | BB41 | SA_D0_22 | BD21 |
| M_A_D23 | BC40 | SA_D0_23 | BD21 |
| M_A_D24 | AY37 | SA_D0_24 | BD21 |
| M_A_D25 | BD38 | SA_D0_25 | BD21 |
| M_A_D26 | AY37 | SA_D0_26 | BD21 |
| M_A_D27 | AT36 | SA_D0_27 | BD21 |
| M_A_D28 | AY38 | SA_D0_28 | BD21 |
| M_A_D29 | BB38 | SA_D0_29 | BD21 |
| M_A_D30 | AY36 | SA_D0_30 | BD21 |
| M_A_D31 | AW36 | SA_D0_31 | BD21 |
| M_A_D32 | BD13 | SA_D0_32 | BD21 |
| M_A_D33 | AI11 | SA_D0_33 | BD21 |
| M_A_D34 | BC11 | SA_D0_34 | BD21 |
| M_A_D35 | BA12 | SA_D0_35 | BD21 |
| M_A_D36 | AI13 | SA_D0_36 | BD21 |
| M_A_D37 | AV13 | SA_D0_37 | BD21 |
| M_A_D38 | BD12 | SA_D0_38 | BD21 |
| M_A_D39 | BC12 | SA_D0_39 | BD21 |
| M_A_D40 | BB9 | SA_D0_40 | BD21 |
| M_A_D41 | BA9 | SA_D0_41 | BD21 |
| M_A_D42 | AI10 | SA_D0_42 | BD21 |
| M_A_D43 | AV9 | SA_D0_43 | BD21 |
| M_A_D44 | BA11 | SA_D0_44 | BD21 |
| M_A_D45 | BD9 | SA_D0_45 | BD21 |
| M_A_D46 | AY8 | SA_D0_46 | BD21 |
| M_A_D47 | BA6 | SA_D0_47 | BD21 |
| M_A_D48 | AV5 | SA_D0_48 | BD21 |
| M_A_D49 | AV7 | SA_D0_49 | BD21 |
| M_A_D50 | AT9 | SA_D0_50 | BD21 |
| M_A_D51 | AN8 | SA_D0_51 | BD21 |
| M_A_D52 | AU6 | SA_D0_52 | BD21 |
| M_A_D53 | AU6 | SA_D0_53 | BD21 |
| M_A_D54 | AT5 | SA_D0_54 | BD21 |
| M_A_D55 | AN10 | SA_D0_55 | BD21 |
| M_A_D56 | AM11 | SA_D0_56 | BD21 |
| M_A_D57 | AM5 | SA_D0_57 | BD21 |
| M_A_D58 | AJ8 | SA_D0_58 | BD21 |
| M_A_D59 | AJ8 | SA_D0_59 | BD21 |
| M_A_D60 | AN12 | SA_D0_60 | BD21 |
| M_A_D61 | AM13 | SA_D0_61 | BD21 |
| M_A_D62 | AJ11 | SA_D0_62 | BD21 |
| M_A_D63 | AJ12 | SA_D0_63 | BD21 |

DDR SYSTEM MEMORY A

CANTIGA-GM-GP-U-NF



| U56E | | | 5 OF 10 |
|---------|------|----------|---------|
| M_B_D00 | AK47 | SB_DO_0 | BC16 |
| M_B_D01 | AK46 | SB_DO_1 | BC17 |
| M_B_D02 | AP47 | SB_DO_2 | BC33 |
| M_B_D03 | AP46 | SB_DO_3 | BC33 |
| M_B_D04 | AJ46 | SB_DO_4 | BC16 |
| M_B_D05 | AJ48 | SB_DO_5 | BC17 |
| M_B_D06 | AM48 | SB_DO_6 | BC33 |
| M_B_D07 | AP48 | SB_DO_7 | BC16 |
| M_B_D08 | AJ47 | SB_DO_8 | BC17 |
| M_B_D09 | AJ46 | SB_DO_9 | BC33 |
| M_B_D10 | RA48 | SB_DO_10 | BC16 |
| M_B_D11 | AY48 | SB_DO_11 | BC17 |
| M_B_D12 | AT47 | SB_DO_12 | BC33 |
| M_B_D13 | AK47 | SB_DO_13 | BC16 |
| M_B_D14 | BA47 | SB_DO_14 | BC17 |
| M_B_D15 | BC47 | SB_DO_15 | BC33 |
| M_B_D16 | BC46 | SB_DO_16 | BC16 |
| M_B_D17 | BC44 | SB_DO_17 | BC17 |
| M_B_D18 | BC43 | SB_DO_18 | BC33 |
| M_B_D19 | BC43 | SB_DO_19 | BC16 |
| M_B_D20 | BE45 | SB_DO_20 | BC17 |
| M_B_D21 | BC41 | SB_DO_21 | BC33 |
| M_B_D22 | BE40 | SB_DO_22 | BC16 |
| M_B_D23 | BF41 | SB_DO_23 | BC17 |
| M_B_D24 | BC38 | SB_DO_24 | BC33 |
| M_B_D25 | BF38 | SB_DO_25 | BC16 |
| M_B_D26 | BH35 | SB_DO_26 | BC17 |
| M_B_D27 | BC35 | SB_DO_27 | BC33 |
| M_B_D28 | BH40 | SB_DO_28 | BC16 |
| M_B_D29 | BC34 | SB_DO_29 | BC17 |
| M_B_D30 | BC34 | SB_DO_30 | BC33 |
| M_B_D31 | BH34 | SB_DO_31 | BC16 |
| M_B_D32 | BH14 | SB_DO_32 | BC17 |
| M_B_D33 | BC12 | SB_DO_33 | BC33 |
| M_B_D34 | BH11 | SB_DO_34 | BC16 |
| M_B_D35 | BC8 | SB_DO_35 | BC17 |
| M_B_D36 | BH12 | SB_DO_36 | BC33 |
| M_B_D37 | BF11 | SB_DO_37 | BC16 |
| M_B_D38 | BF9 | SB_DO_38 | BC17 |
| M_B_D39 | BC7 | SB_DO_39 | BC33 |
| M_B_D40 | BC5 | SB_DO_40 | BC16 |
| M_B_D41 | AC5 | SB_DO_41 | BC17 |
| M_B_D42 | AV1 | SB_DO_42 | BC33 |
| M_B_D43 | BF8 | SB_DO_43 | BC16 |
| M_B_D44 | BF8 | SB_DO_44 | BC17 |
| M_B_D45 | BA1 | SB_DO_45 | BC33 |
| M_B_D46 | BA1 | SB_DO_46 | BC16 |
| M_B_D47 | BD1 | SB_DO_47 | BC17 |
| M_B_D48 | AV2 | SB_DO_48 | BC33 |
| M_B_D49 | AJ3 | SB_DO_49 | BC16 |
| M_B_D50 | AR3 | SB_DO_50 | BC17 |
| M_B_D51 | AN2 | SB_DO_51 | BC33 |
| M_B_D52 | AY2 | SB_DO_52 | BC16 |
| M_B_D53 | AJ1 | SB_DO_53 | BC17 |
| M_B_D54 | AP3 | SB_DO_54 | BC33 |
| M_B_D55 | AR1 | SB_DO_55 | BC16 |
| M_B_D56 | AL1 | SB_DO_56 | BC17 |
| M_B_D57 | AL2 | SB_DO_57 | BC33 |
| M_B_D58 | AJ1 | SB_DO_58 | BC16 |
| M_B_D59 | AH1 | SB_DO_59 | BC17 |
| M_B_D60 | AM2 | SB_DO_60 | BC33 |
| M_B_D61 | AM3 | SB_DO_61 | BC16 |
| M_B_D62 | AJ3 | SB_DO_62 | BC17 |
| M_B_D63 | AJ3 | SB_DO_63 | BC33 |

DDR SYSTEM MEMORY B

CANTIGA-GM-GP-U-NF

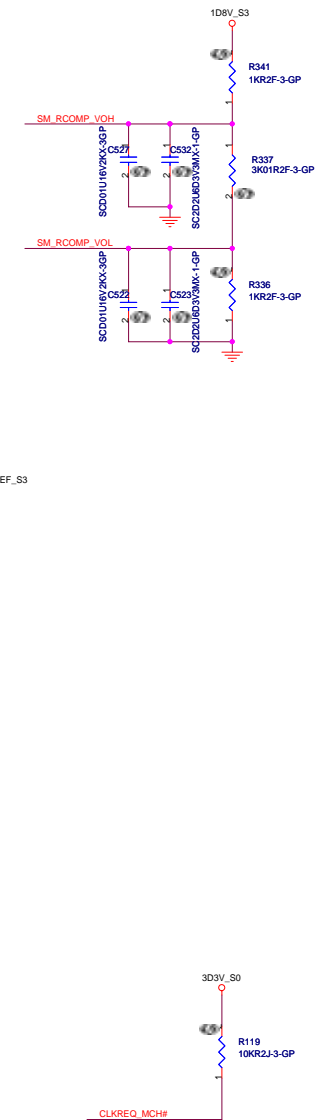
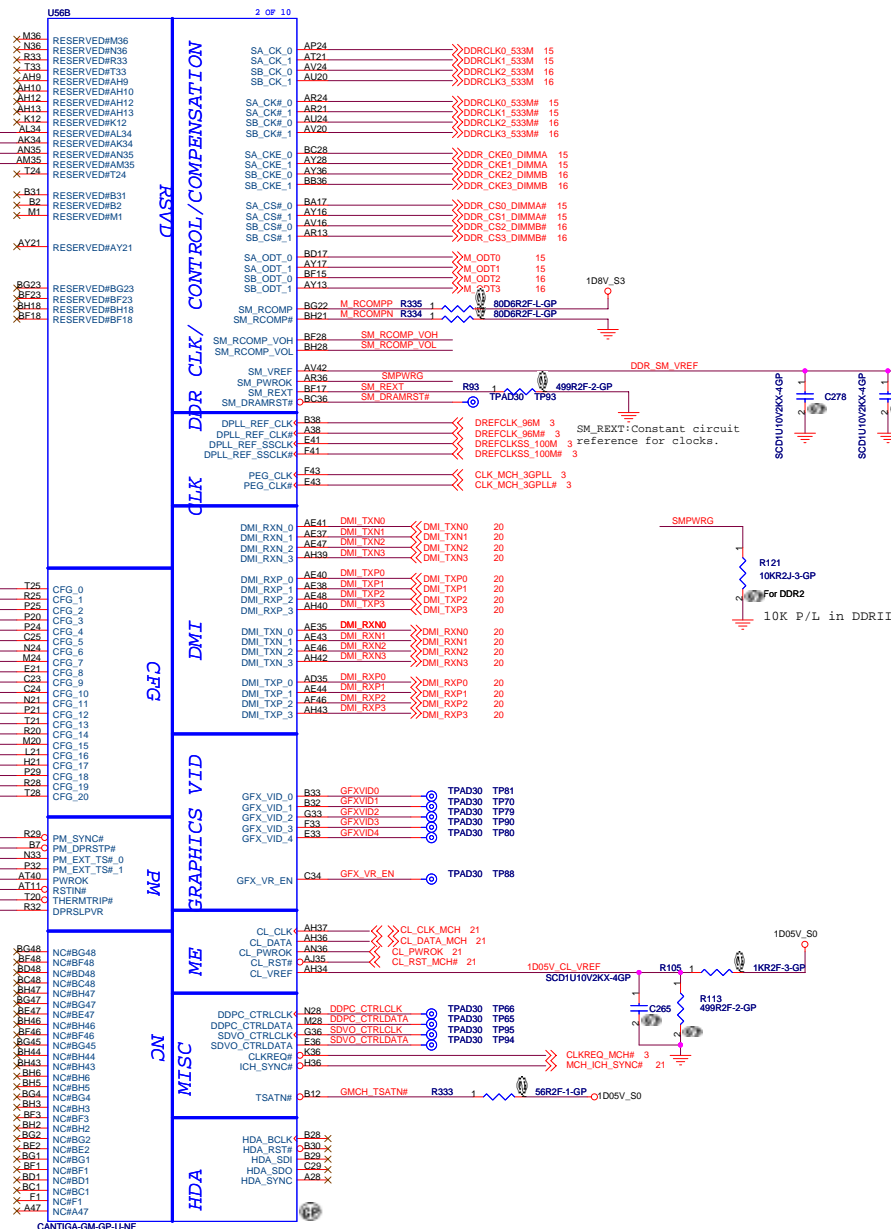
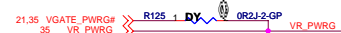
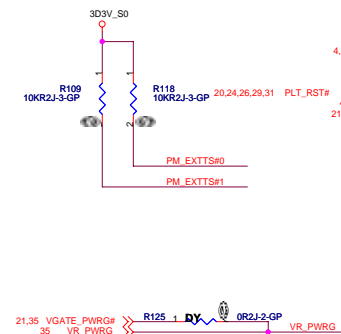


<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title Cantiga(2/7):DDR3
Size C Document Number LZ2 Rev SB
Date: Thursday, June 05, 2008 Sheet 9 of 41

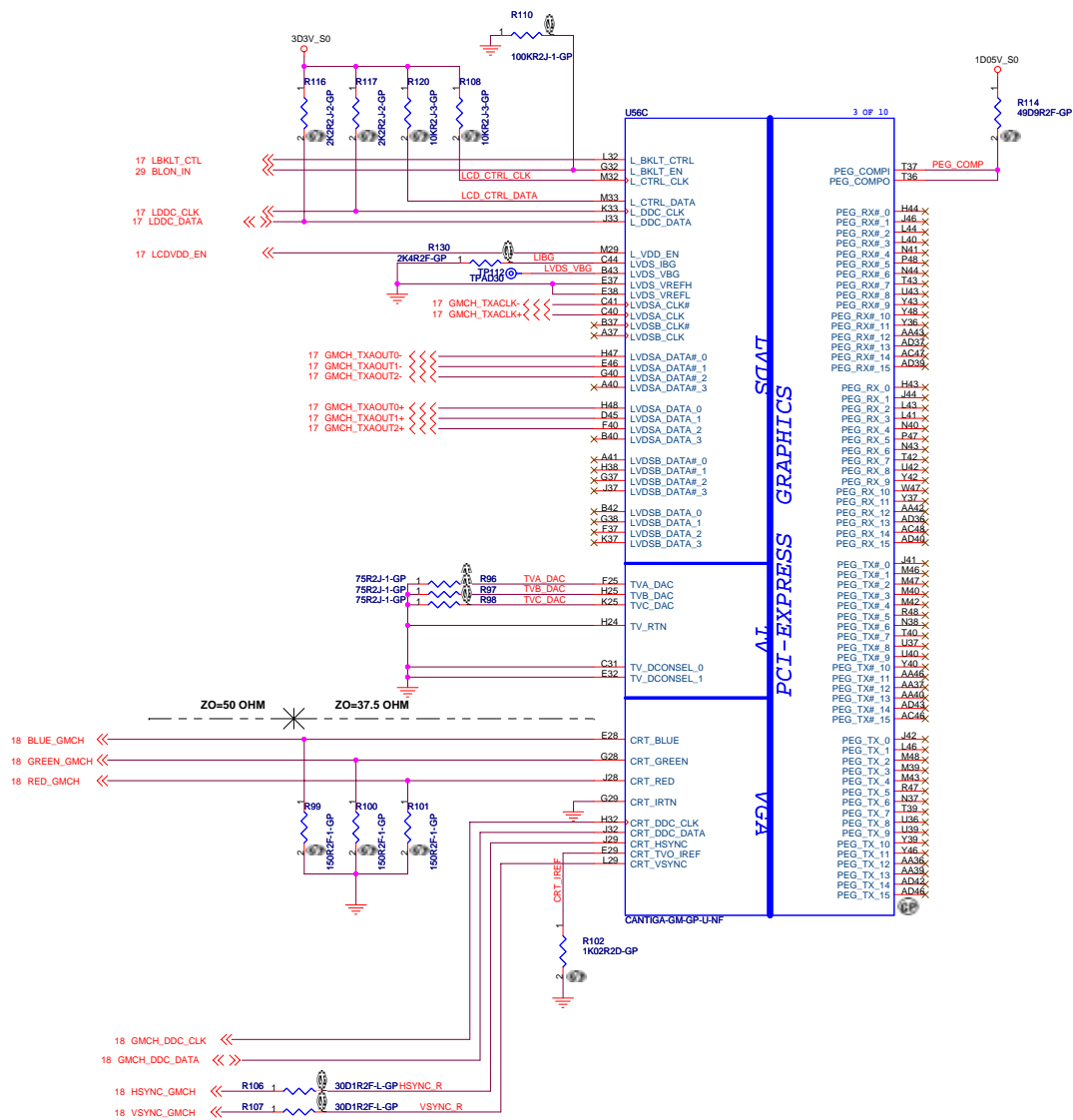
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| RESERVED#AK34 | ME_JTAG_TDI |
| RESERVED#AN35 | ME_JTAG_TDO |
| RESERVED#AM35 | ME_JTAG_TMS |

[illegible]

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| | | | |
|-----------------------------------|-------------------------|-------------|-----------|
| Title | | | |
| Cantiga(3/7):DMI/PM/CFG/GF | | | |
| Size | Document Number | | Rev |
| C | L72 | | SB |
| Date: | Thursday, June 05, 2008 | Sheet 10 of | 41 |



<Variant Name>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CANTIGA(57)-VGA/LVDS

Size

Document Number

C

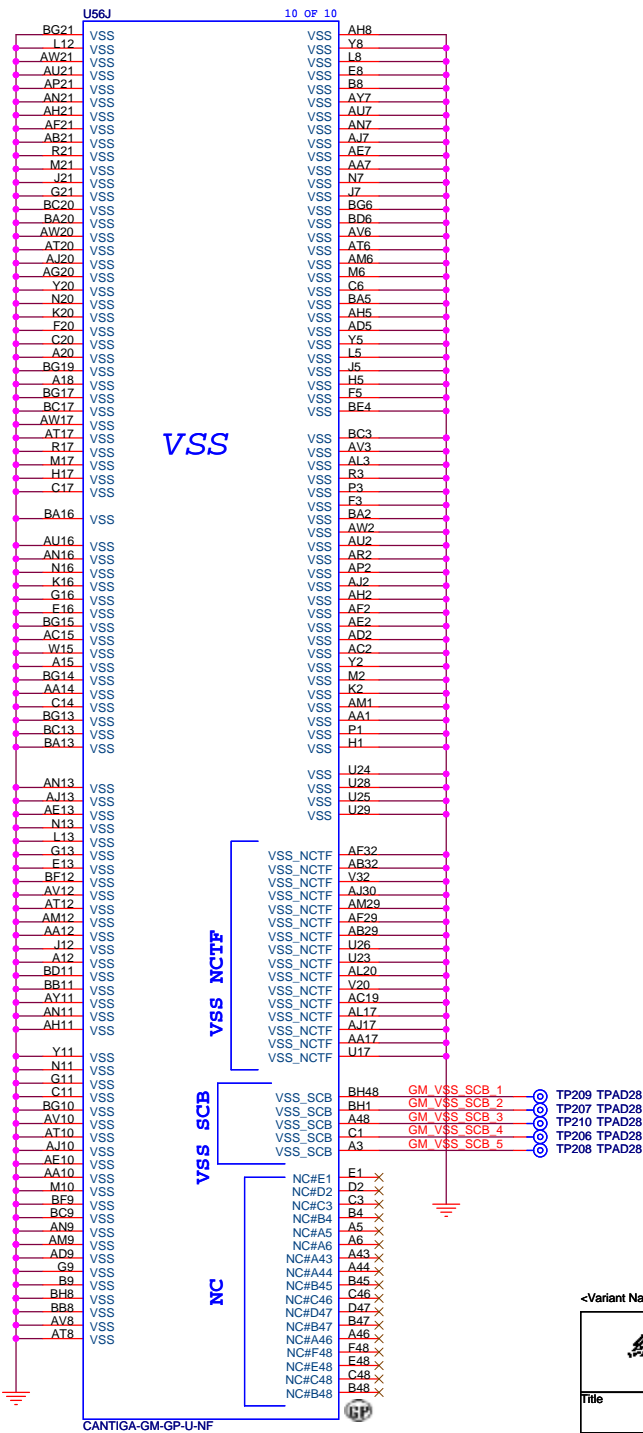
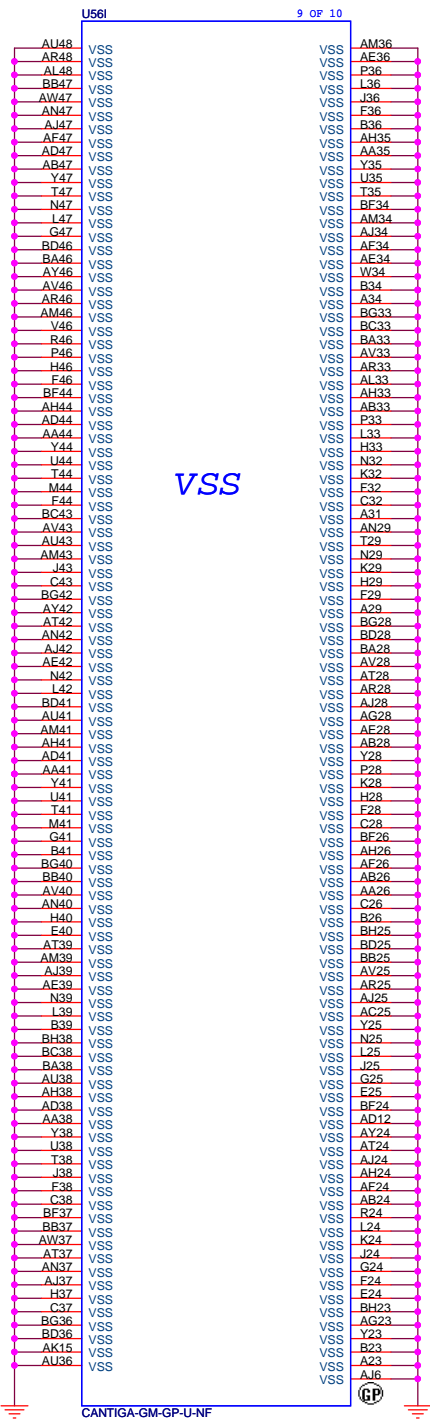
LZ2

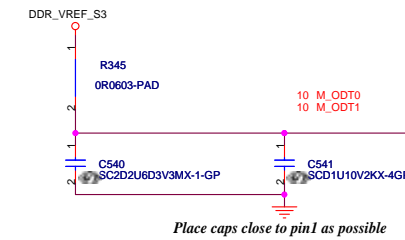
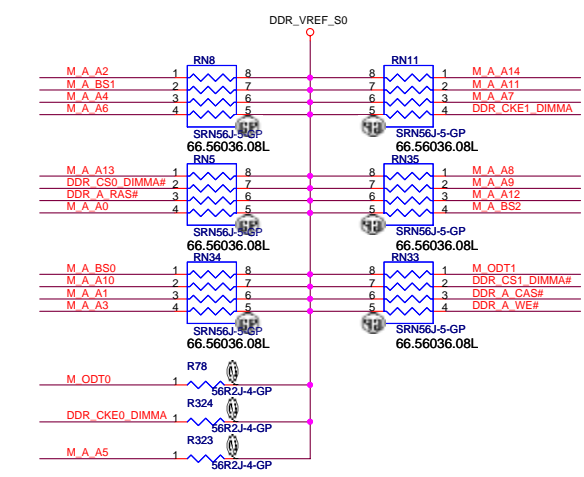
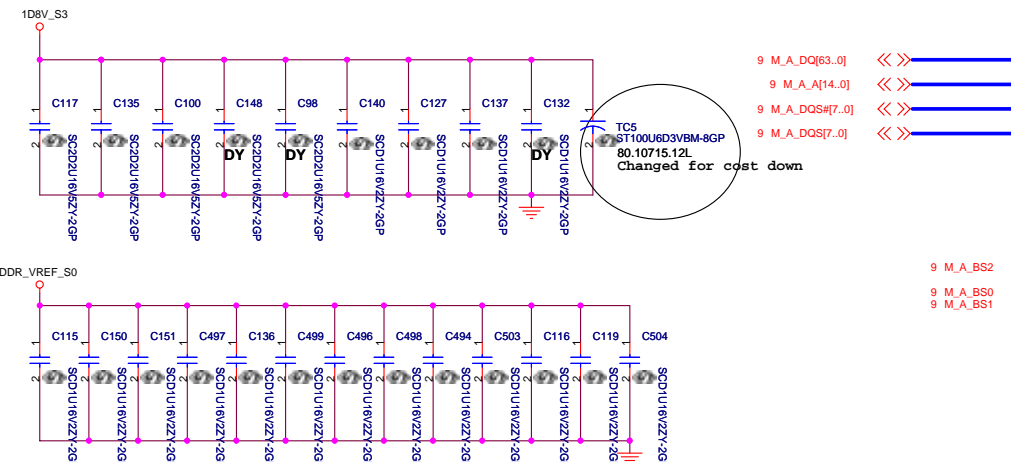
Date: Thursday, June 05, 2008

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Rev

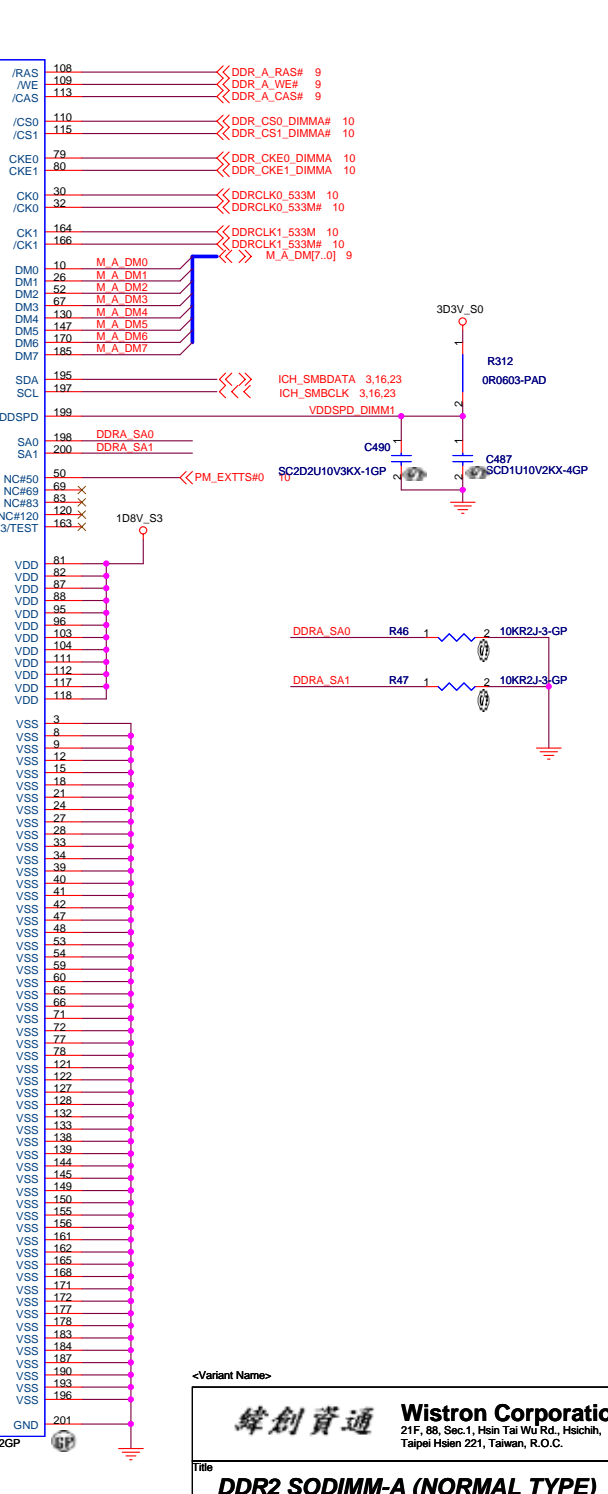
SB





| | | | |
|-----------|-----|------|-----|
| M_A A0 | 102 | DM2 | 108 |
| M_A A1 | 101 | /RAS | 109 |
| M_A A2 | 100 | /WE | 113 |
| M_A A3 | 99 | /CAS | A2 |
| M_A A4 | 98 | | 110 |
| M_A A5 | 97 | | 115 |
| M_A A6 | 94 | | 79 |
| M_A A7 | 92 | | 80 |
| M_A A8 | 93 | | 30 |
| M_A A9 | 91 | | 32 |
| M_A A10 | 105 | | 164 |
| M_A A11 | 90 | | 166 |
| M_A A12 | 89 | | 10 |
| M_A A13 | 116 | | 10 |
| M_A A14 | 86 | | 10 |
| | 84 | | 10 |
| | 85 | | 10 |
| | 107 | | 10 |
| | 106 | | 10 |
| | BA0 | | 10 |
| | BA1 | | 10 |
| M_A DQ0 | 5 | | 10 |
| M_A DQ1 | 7 | | 10 |
| M_A DQ2 | 17 | | 10 |
| M_A DQ3 | 19 | | 10 |
| M_A DQ4 | 4 | | 10 |
| M_A DQ5 | 6 | | 10 |
| M_A DQ6 | 14 | | 10 |
| M_A DQ7 | 16 | | 10 |
| M_A DQ8 | 23 | | 10 |
| M_A DQ9 | 25 | | 10 |
| M_A DQ10 | 35 | | 10 |
| M_A DQ11 | 37 | | 10 |
| M_A DQ12 | 20 | | 10 |
| M_A DQ13 | 22 | | 10 |
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| M_A DQ15 | 38 | | 10 |
| M_A DQ16 | 43 | | 10 |
| M_A DQ17 | 45 | | 10 |
| M_A DQ18 | 55 | | 10 |
| M_A DQ19 | 57 | | 10 |
| M_A DQ20 | 44 | | 10 |
| M_A DQ21 | 46 | | 10 |
| M_A DQ22 | 56 | | 10 |
| M_A DQ23 | 58 | | 10 |
| M_A DQ24 | 61 | | 10 |
| M_A DQ25 | 63 | | 10 |
| M_A DQ26 | 73 | | 10 |
| M_A DQ27 | 75 | | 10 |
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| M_A DQ30 | 74 | | 10 |
| M_A DQ31 | 76 | | 10 |
| M_A DQ32 | 123 | | 10 |
| M_A DQ33 | 125 | | 10 |
| M_A DQ34 | 135 | | 10 |
| M_A DQ35 | 137 | | 10 |
| M_A DQ36 | 124 | | 10 |
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| M_A DQ39 | 136 | | 10 |
| M_A DQ40 | 141 | | 10 |
| M_A DQ41 | 143 | | 10 |
| M_A DQ42 | 151 | | 10 |
| M_A DQ43 | 153 | | 10 |
| M_A DQ44 | 140 | | 10 |
| M_A DQ45 | 142 | | 10 |
| M_A DQ46 | 152 | | 10 |
| M_A DQ47 | 154 | | 10 |
| M_A DQ48 | 157 | | 10 |
| M_A DQ49 | 159 | | 10 |
| M_A DQ50 | 175 | | 10 |
| M_A DQ51 | 173 | | 10 |
| M_A DQ52 | 158 | | 10 |
| M_A DQ53 | 160 | | 10 |
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| M_A DQ55 | 176 | | 10 |
| M_A DQ56 | 179 | | 10 |
| M_A DQ57 | 181 | | 10 |
| M_A DQ58 | 189 | | 10 |
| M_A DQ59 | 191 | | 10 |
| M_A DQ60 | 180 | | 10 |
| M_A DQ61 | 182 | | 10 |
| M_A DQ62 | 192 | | 10 |
| M_A DQ63 | 194 | | 10 |
| M_A DQS#0 | 11 | | 10 |
| M_A DQS#1 | 29 | | 10 |
| M_A DQS#2 | 49 | | 10 |
| M_A DQS#3 | 68 | | 10 |
| M_A DQS#4 | 129 | | 10 |
| M_A DQS#5 | 146 | | 10 |
| M_A DQS#6 | 167 | | 10 |
| M_A DQS#7 | 186 | | 10 |
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| M_A DQS#1 | 31 | | 10 |
| M_A DQS#2 | 51 | | 10 |
| M_A DQS#3 | 70 | | 10 |
| M_A DQS#4 | 131 | | 10 |
| M_A DQS#5 | 148 | | 10 |
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| M_A DQS#7 | 188 | | 10 |
| M_A DQS#0 | 114 | | 10 |
| M_A DQS#1 | 119 | | 10 |
| M_A DQS#2 | 119 | | 10 |
| M_A DQS#3 | 121 | | 10 |
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| M_A DQS#5 | 127 | | 10 |
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| M_A DQS#7 | 132 | | 10 |
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| M_A DQS#7 | 155 | | 10 |
| M_A DQS#0 | 156 | | 10 |
| M_A DQS#1 | 161 | | 10 |
| M_A DQS#2 | 162 | | 10 |
| M_A DQS#3 | 165 | | 10 |
| M_A DQS#4 | 168 | | 10 |
| M_A DQS#5 | 171 | | 10 |
| M_A DQS#6 | 172 | | 10 |
| M_A DQS#7 | 178 | | 10 |
| M_A DQS#0 | 183 | | 10 |
| M_A DQS#1 | 184 | | 10 |
| M_A DQS#2 | 187 | | 10 |
| M_A DQS#3 | 190 | | 10 |
| M_A DQS#4 | 193 | | 10 |
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NORMAL TYPE



<Variant Name>

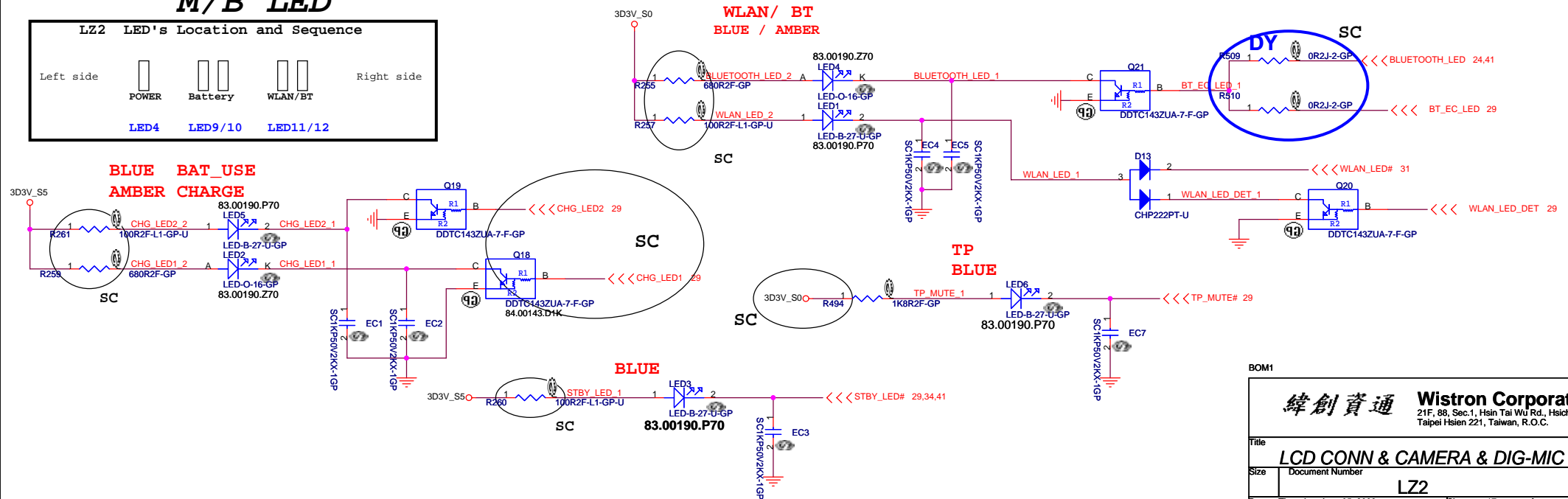
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| Title | | Rev | |
| Wistron Corporation | | SB | |
| 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | | | |
| Size | | Document Number | |
| Custom | | LZ2 | |
| Date: Thursday, June 05, 2008 | | Sheet 15 of 41 | |

Place caps close to pin1 as possible

[illegible]

L2Z LED's Location and Sequence

| | | |
|--|--|---|
| <div style="border: 1px solid black; width: 20px; height: 40px; margin: 0 auto;"></div> <p>POWER</p> <p>LED4</p> | <div style="display: inline-block; border: 1px solid black; width: 15px; height: 40px; margin-right: 5px;"></div> <div style="display: inline-block; border: 1px solid black; width: 15px; height: 40px; margin-left: 5px;"></div> <p>Battery</p> <p>LED9/10</p> | <div style="display: inline-block; border: 1px solid black; width: 15px; height: 40px; margin-right: 5px;"></div> <div style="display: inline-block; border: 1px solid black; width: 15px; height: 40px; margin-left: 5px;"></div> <p>WLAN/BT</p> <p>LED11/12</p> |
| Left side | | Right side |



BOM1

緯創資通

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| | |
|-------|-----------------------------|
| Title | LCD CONN & CAMERA & DIG-MIC |
|-------|-----------------------------|

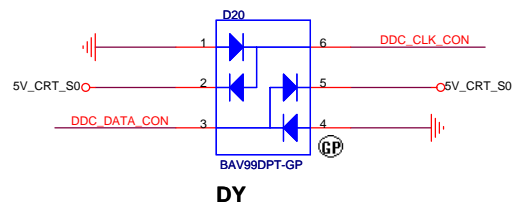
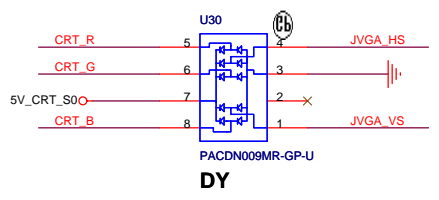
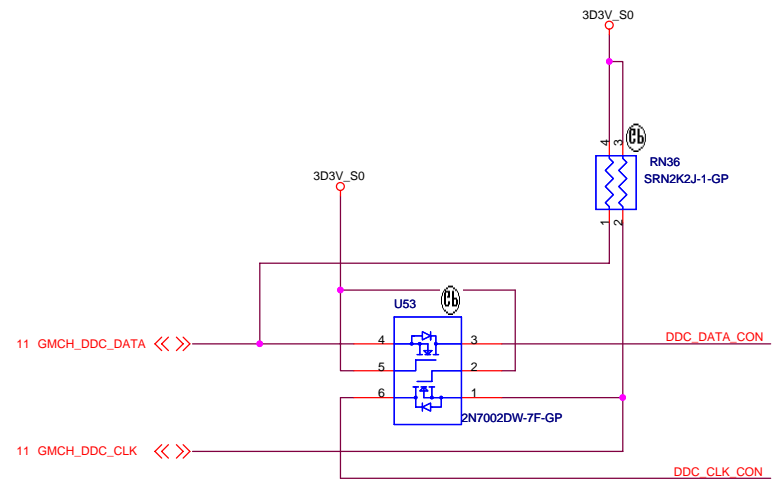
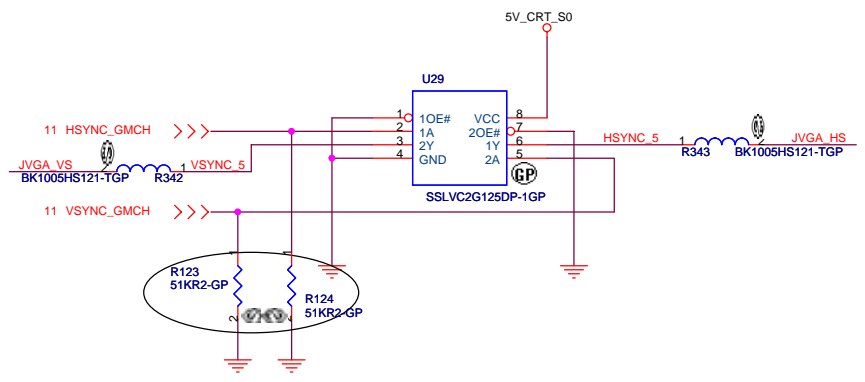
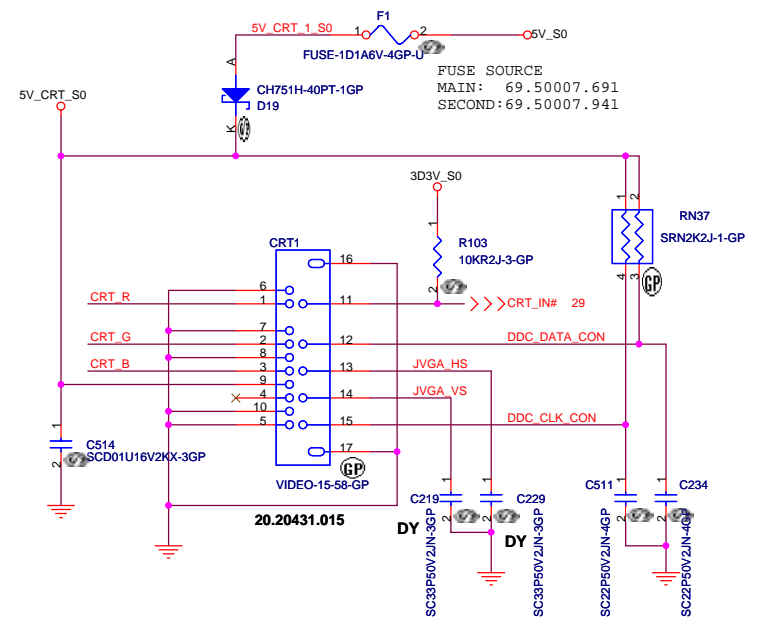
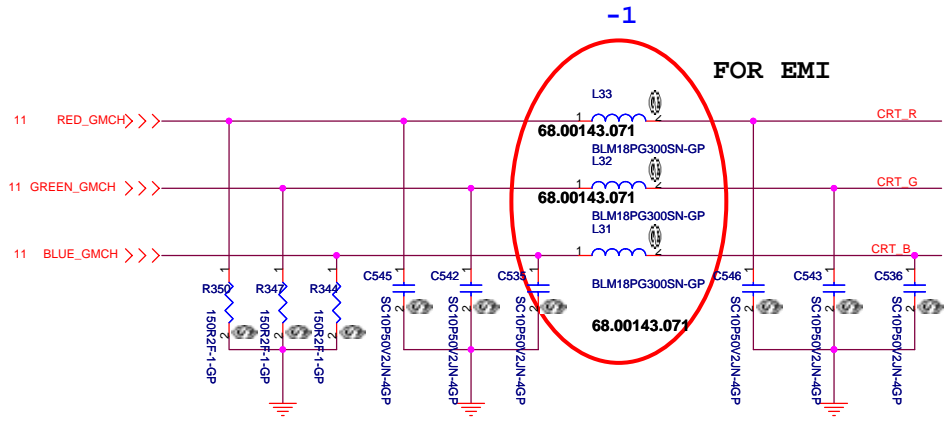
| Size | Document Number |
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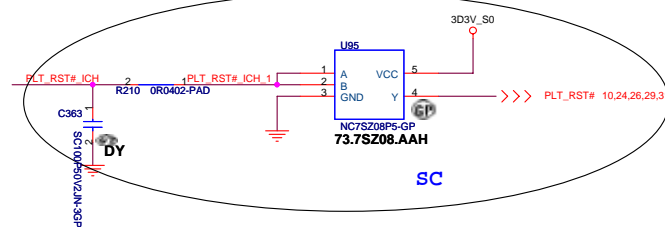
LZ2

SB

Date: Thursday, June 05, 2008

Sheet 17 of 41

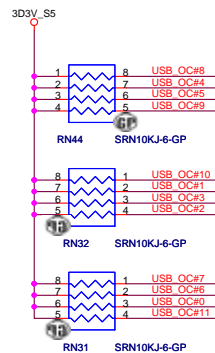
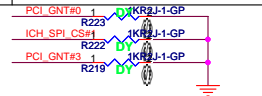




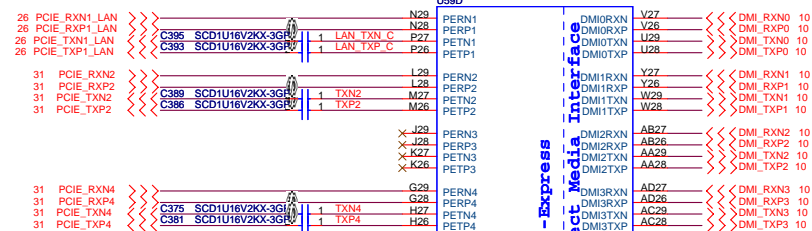
| BOOT BIOS Strap | | |
|-----------------|----------|--------------------|
| PCI_GNT#0 | SPI_CS#1 | BOOT BIOS Location |
| 0 | 1 | SPT |
| 1 | 0 | PCT |
| 1 | 1 | LEC(Default) |

Al6 swap override strap

| PCI_GNT#3 | low = Al6 swap override enable high = default |
|-----------|--|
|-----------|--|

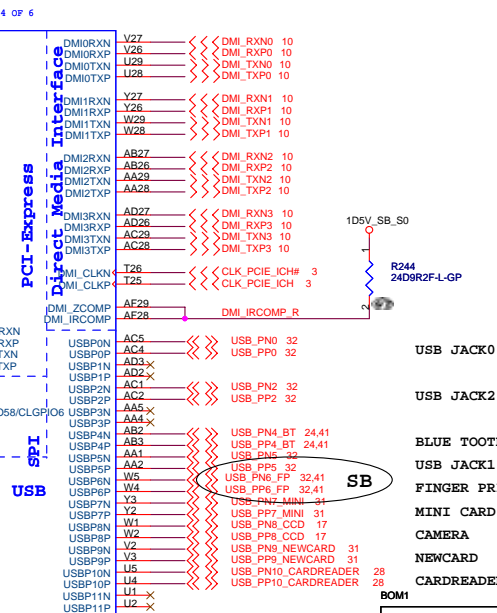


LAN



MINI I/O

NEW COARD



USB JACK0

USB JACK2

BLUE TOOTH

USB JACK1

FINGER PRINT

MINI CARD

MINI CARD

CAMERA

NEWCARD

NEWCARD
CARDREADER

CARDREADER

M1

100

壁創

詳創頁

1000

| | |
|--|-----------------|
| | Document Number |
|--|-----------------|

Document Number

Thursday, June 05, 2014

| | |
|--|-------------------------|
| | Thursday, June 05, 2019 |
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| | | | |
|------------------------|-------------------------|-------------|-----|
| Title | | | |
| ICH9-M (1 of 4) | | | |
| Size | Document Number | | Rev |
| | LZ2 | | S |
| Date: | Thursday, June 05, 2008 | Sheet 20 of | 41 |

VccRTC=6uA in G3

Vcc1_5_B=646mA

*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

V5REF=2mA

VccSATAPLL=47mA

Vcc1_5_A=1.342A

V5REF_Sus=2mA

USBPLL=11mA

VccLAN3_3=19mA

VccGLAN1_5=80mA

VccGLAN3_3=1mA

Vcc1_05=1.634A

Layout Note:Place near ICH9M

VccDMIPLL=23mA

VccDMI=48mA

V_CPU_IO=2mA

VCC3_3=308mA

VccHDA=11mA

VccSusHDA=11mA

VccSus3_3=212mA

VccCL3_3=19mA

緯創資通

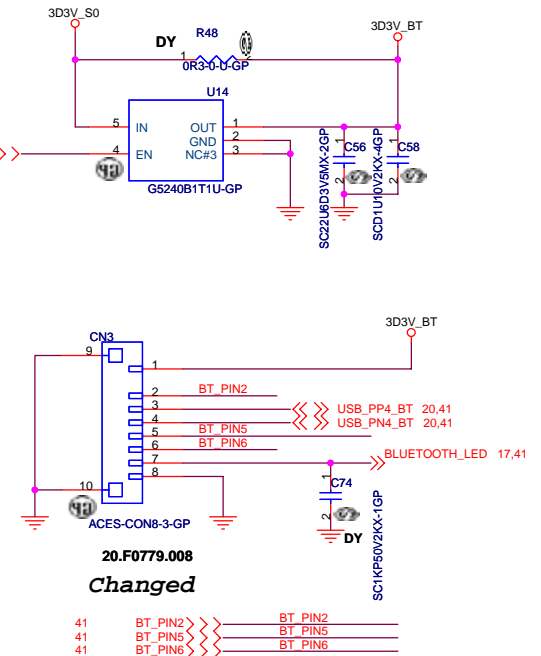
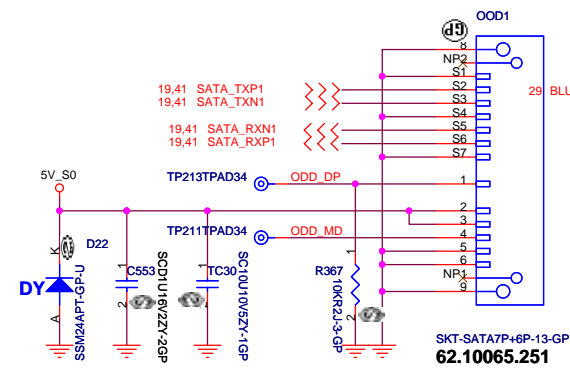
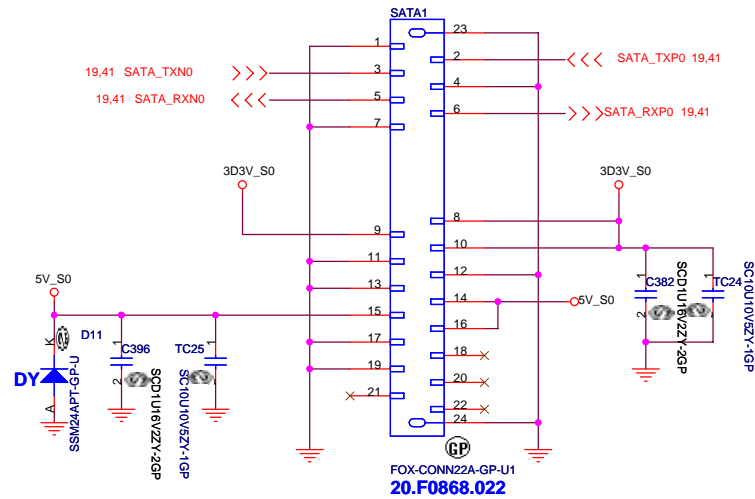
Wistron Corporation

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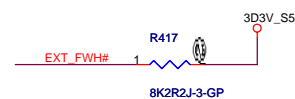
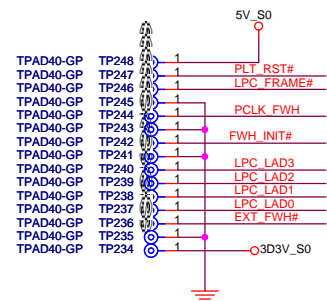
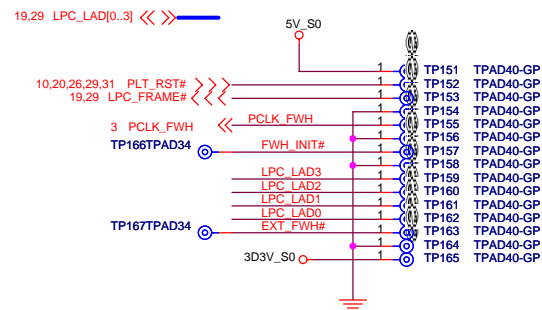
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|-------|-----------------------|-------|-----------------|-------|
| Title | | | ICH9-M (3 of 4) | |
| Size | Document Number | LZ2 | | Rev |
| Date: | Tuesday, May 13, 2008 | Sheet | 22 | of 41 |

ODD Connector

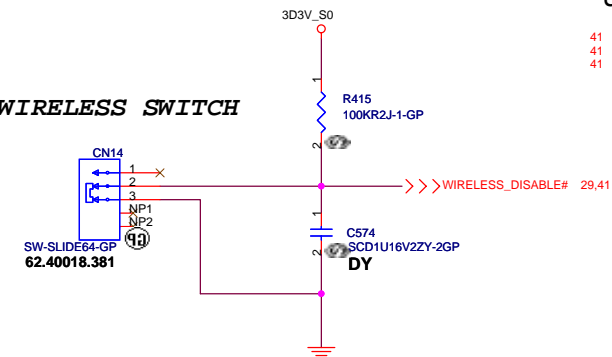
BT CONNECTOR



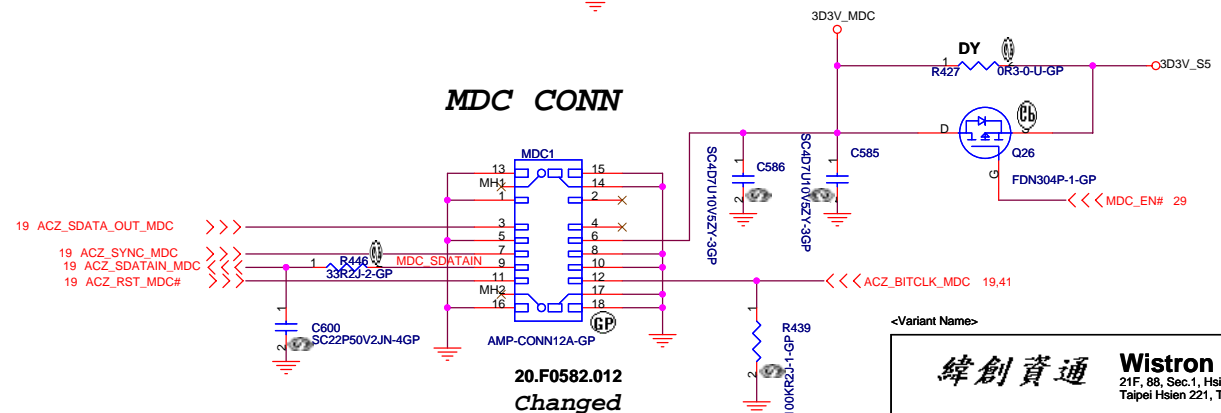
GOLDEN FINGER FOR DEBUG BOARD

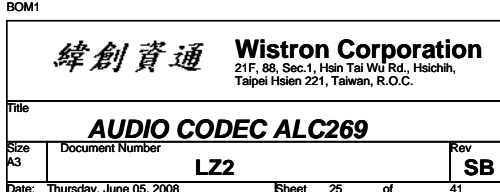


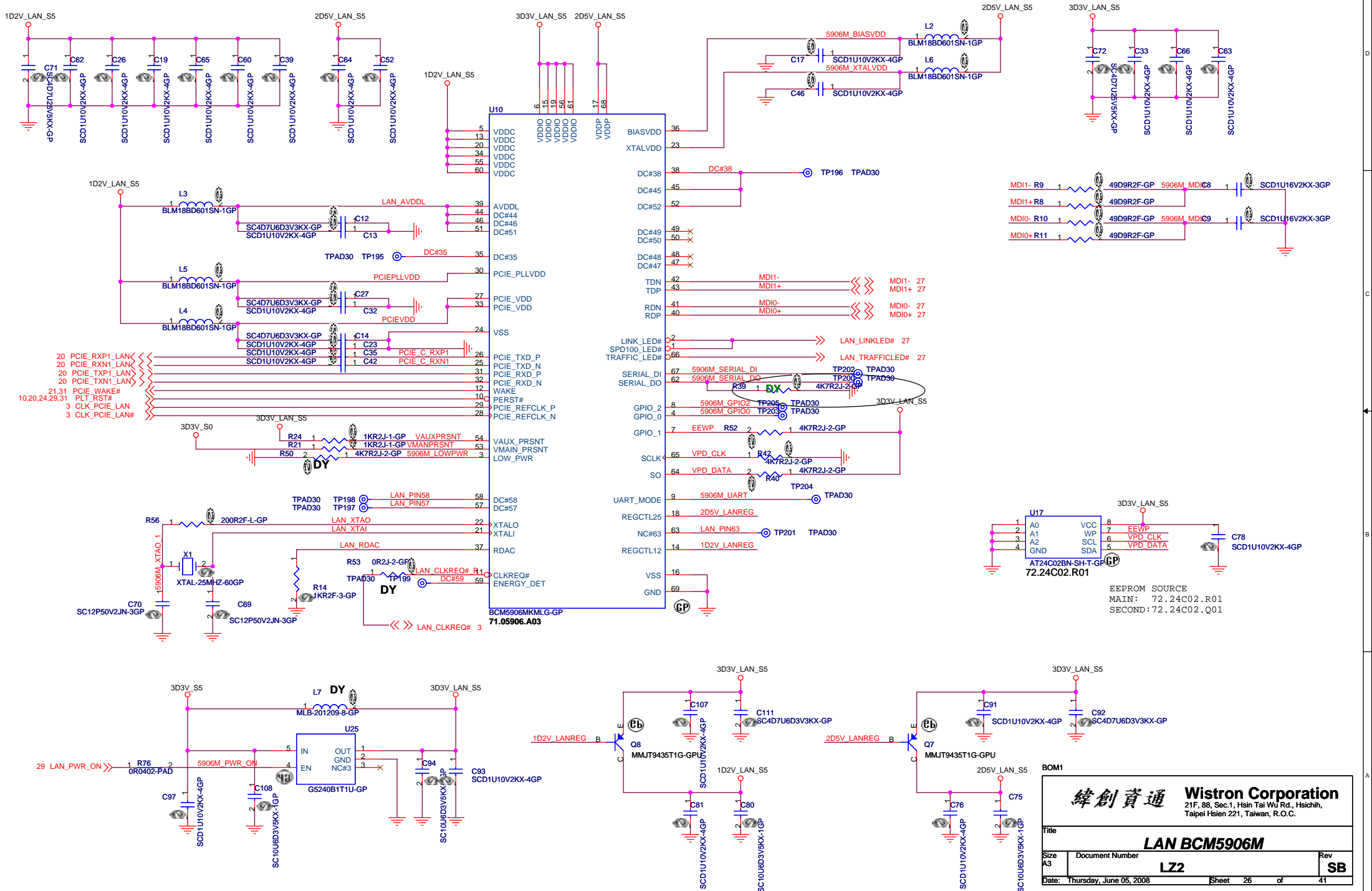
WIRELESS SWITCH



MDC CONN







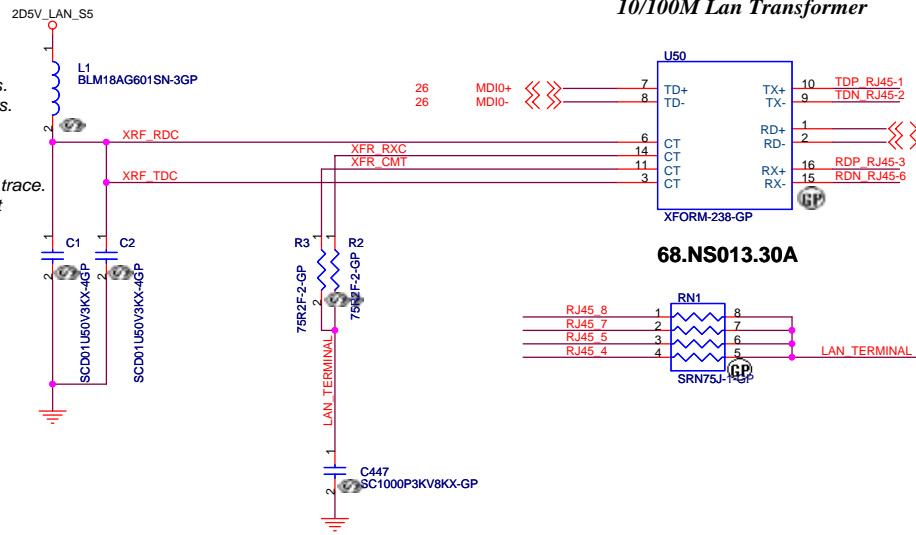
緯創資通

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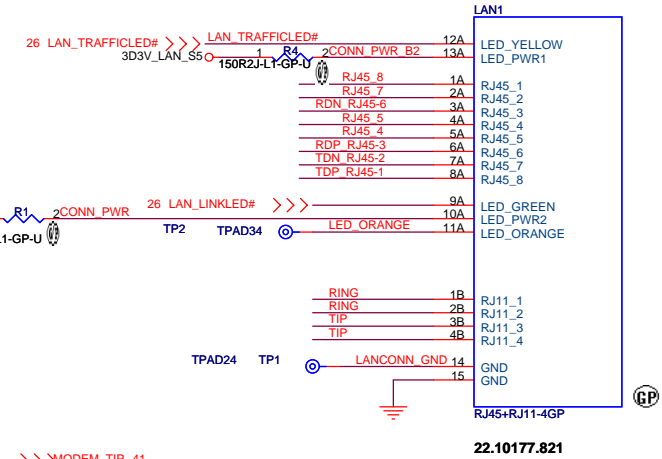
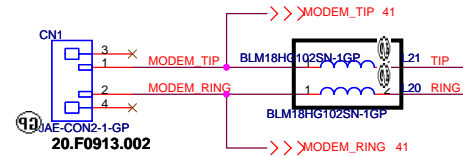
| | | | | | |
|-------|-------------------------|-------|--------------|----|----|
| Title | | | LAN BCM5906M | | |
| Size | Document Number | Rev | | | |
| A3 | LZ2 | SB | | | |
| Date: | Thursday, June 05, 2008 | Sheet | 26 | of | 41 |

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



10/100M Lan Transformer

68.NS013.30A



Changed

<Variant Name>

緯創資通

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LAN connector/NEW CARD/SIM

Size

Document Number

LZ2

Rev

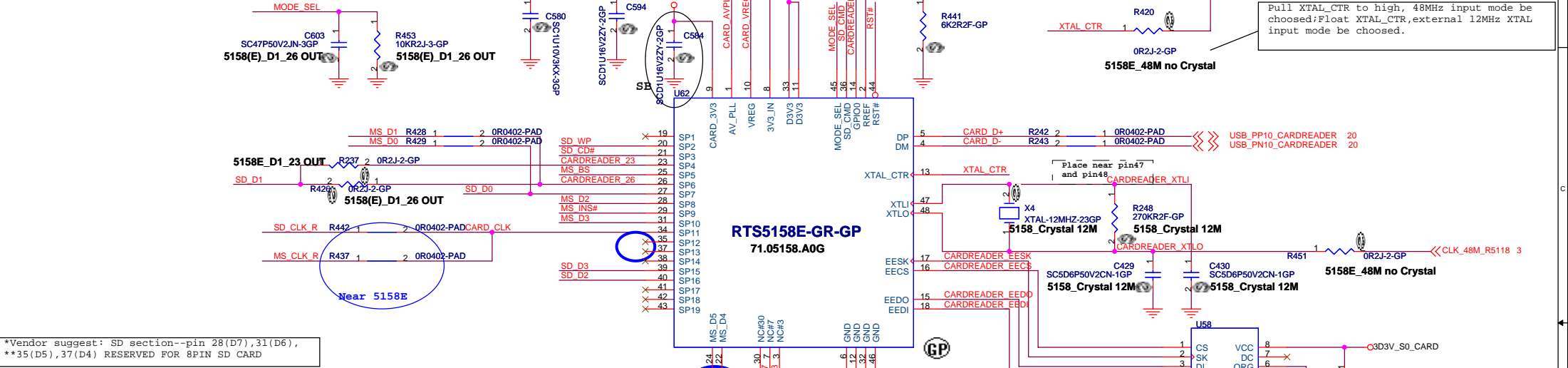
SB

Date: Thursday, June 05, 2008

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For 3in1
SD/MMC/MS CARD

| | | | |
|-------|-------|----------------|------------|
| R1302 | C38 | SD_D1 OUT FROM | IC P/N |
| 10K | 47 PF | PIN 26(MS_D1) | 5158&5158E |
| NC | NC | PIN 23 | 5158E |



| | | |
|----------|--------|--------|
| | R71 | R72 |
| RTS5158 | ASM | ASM |
| RTS5158E | NO ASM | NO ASM |

| CLK CONTROL | R1303 | X7,R1373, C842,C843 |
|-------------|--------|---------------------|
| 48MHZ | ASM | NO ASM |
| 12MHZ | NO ASM | ASM |

VENDOR SUGGEST USE 5.6PF
OR USE 48MHZ DIRECTLY BY CLK GEN.

| Pin 13 (XTAL CTL) | Clock source | Remark |
|-------------------|-------------------------------|---------------------------|
| Floating | 12MHz crystal input | |
| Full high | Clock generator's 48MHz input | Input to RTS5158E(Pin 48) |

<Core Design>

緯創資通

Wistron Corporation

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Title

CARD READER

Size

A3

Document Number

LZ2

Rev

SB

Date

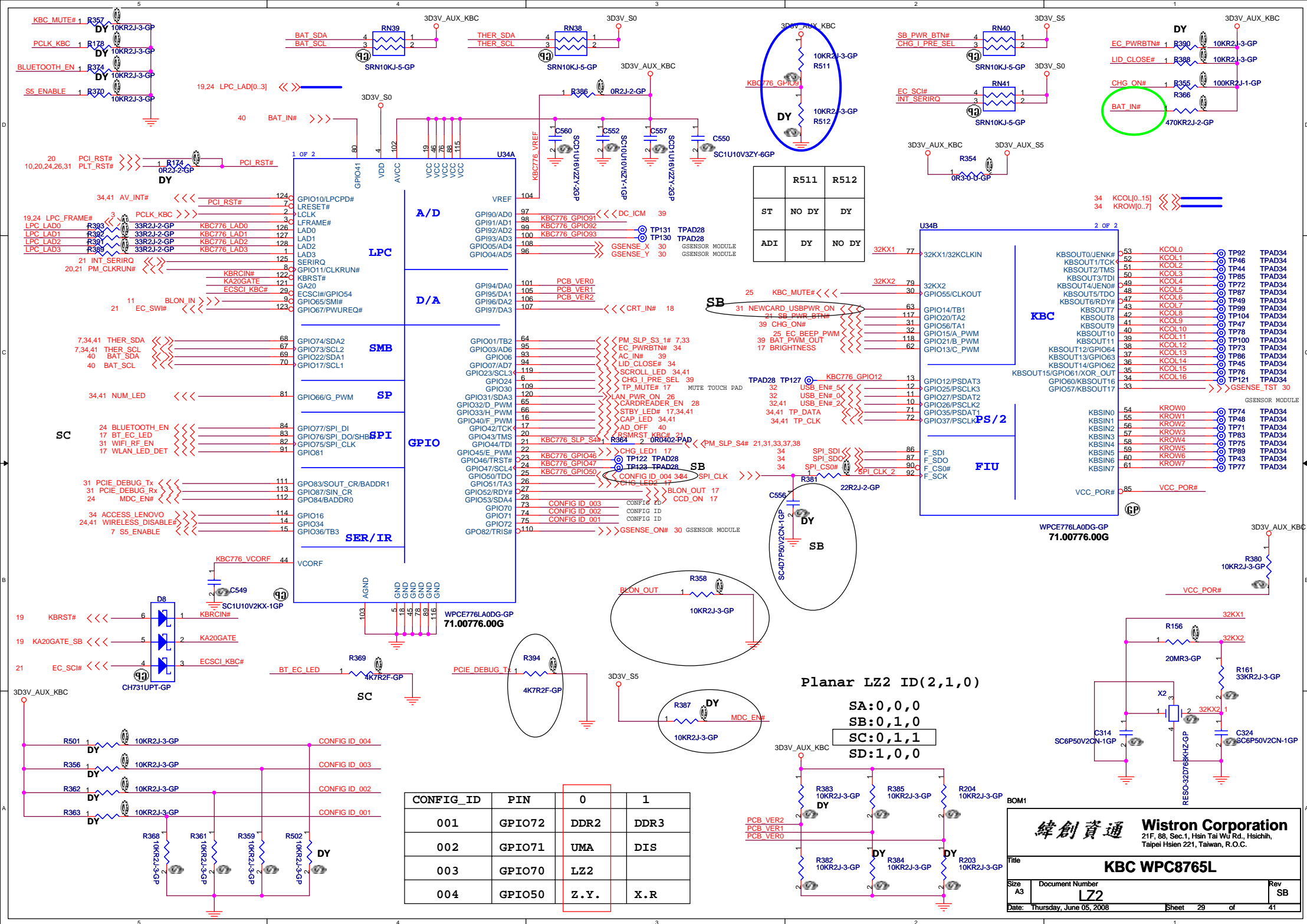
Thursday, June 05, 2008

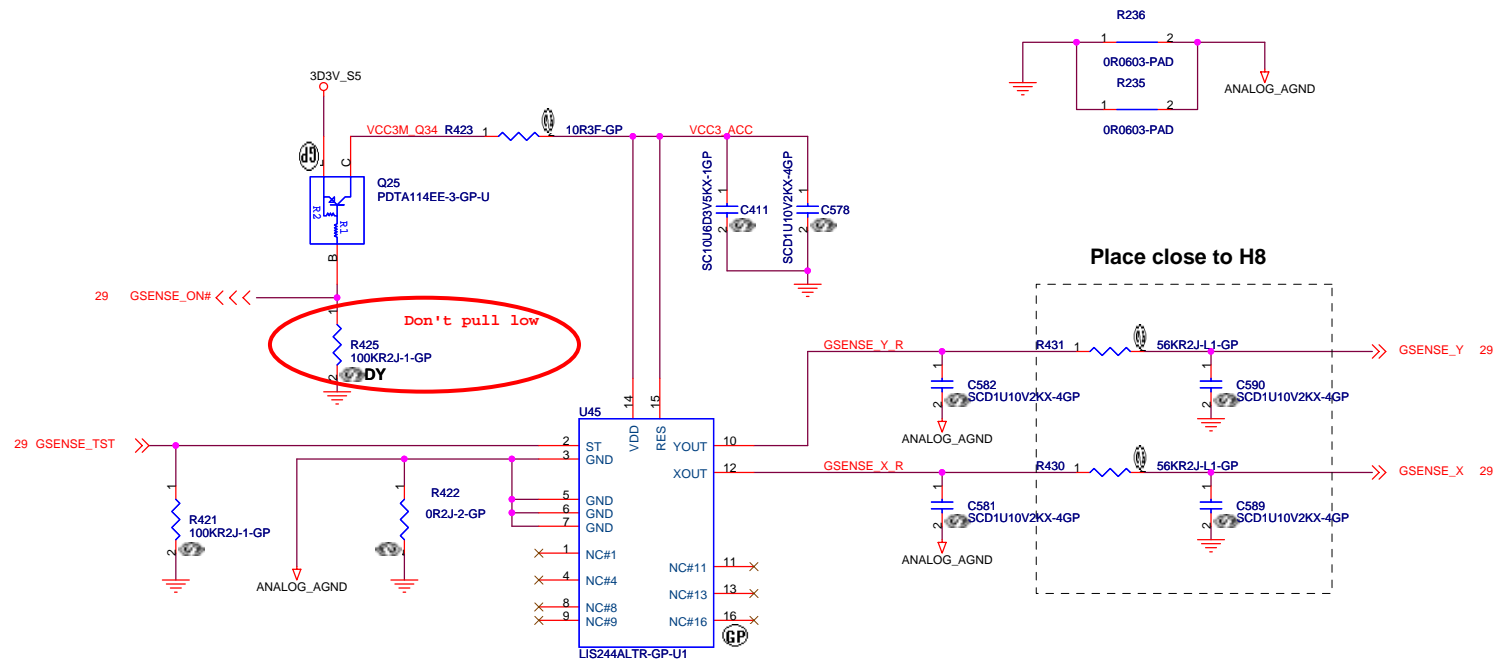
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41





Primary : STMicro LIS244AL
2nd: ADI ADXL322

| | | |
|-----------|---------|----------|
| | ADXL322 | No Accel |
| R545 | NO_ASM | ASM |
| R547 | ASM | ASM |
| All other | ASM | NO_ASM |

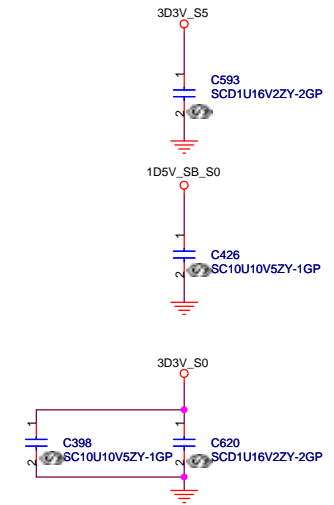
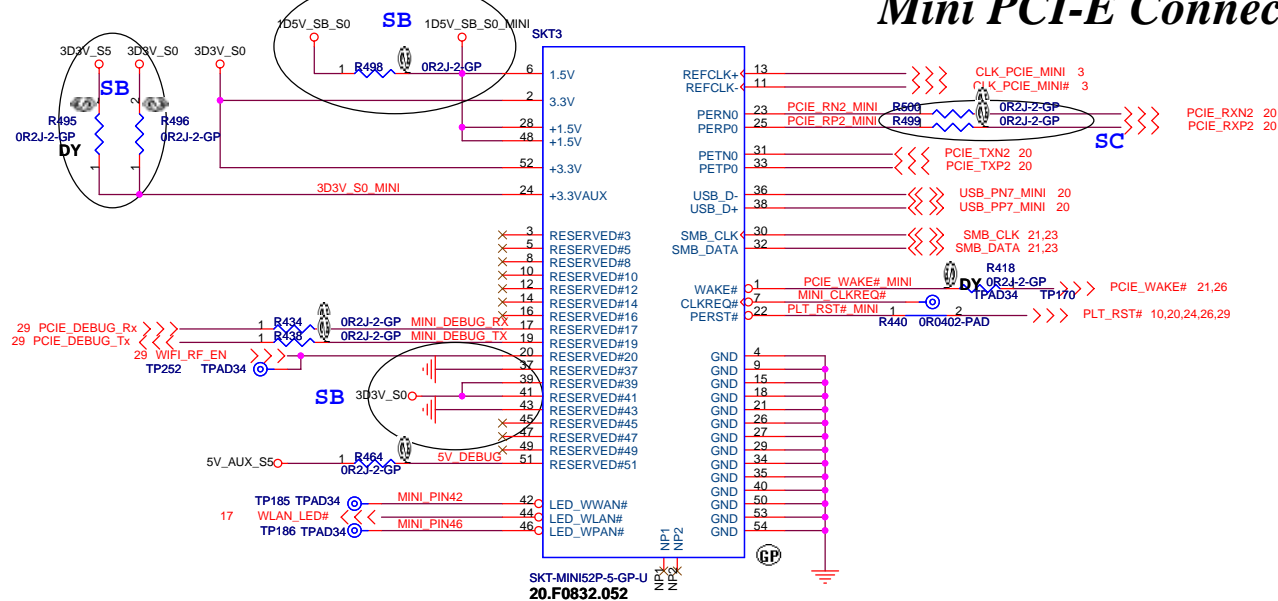
Layout Comment :

- (1) Place C148, C149, Q18, R116, R121, C126, C130, R107, R106 close to U18.
- (2) Avoid routing under DCDC switching area.

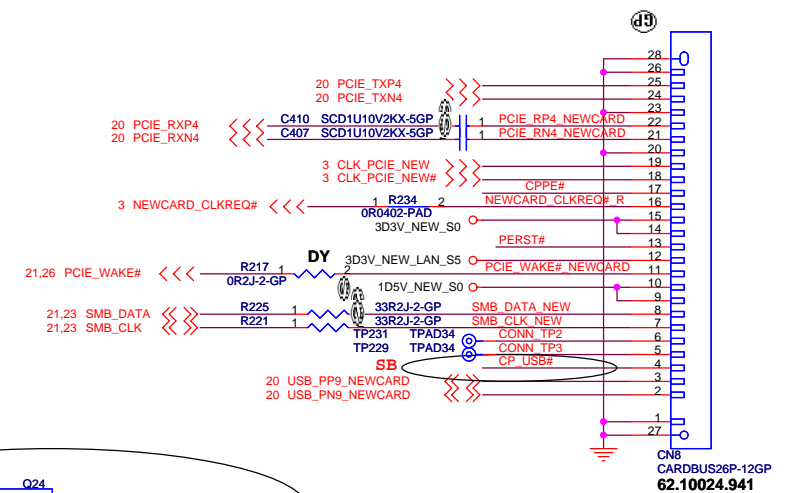
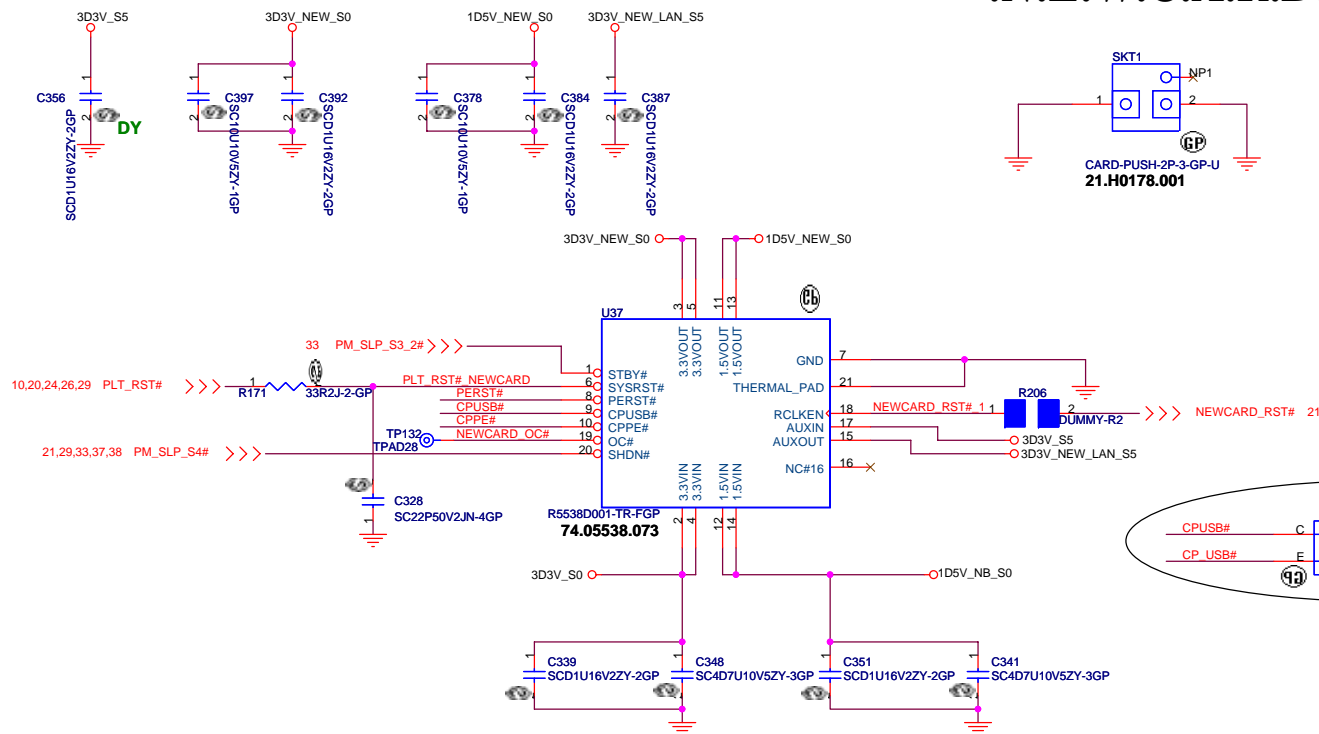
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|-------------------------------|-----------------|---|-----------|
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| Title: GSENSOR | | | |
| Size | Document Number | | Rev |
| | LZ2 | | SB |
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Mini PCI-E Connector



.N.E.W.C.A.R.D. C.O.N.N.

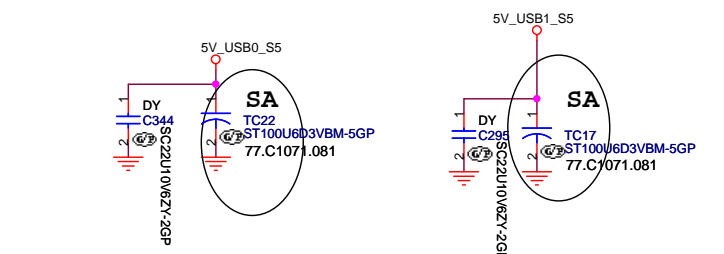
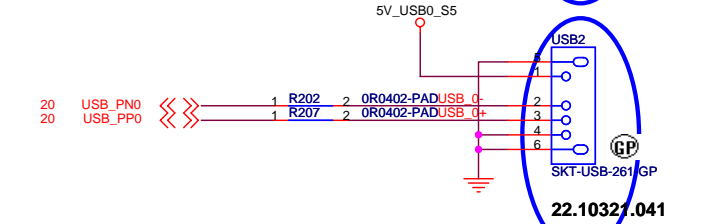
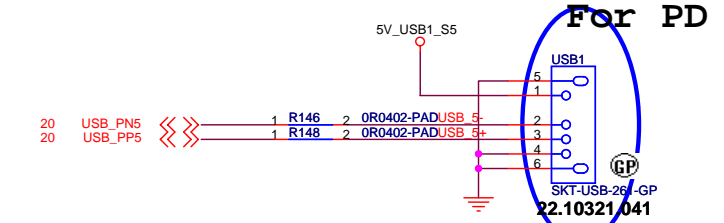
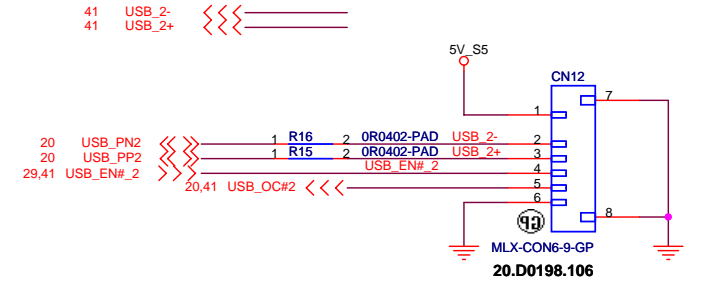
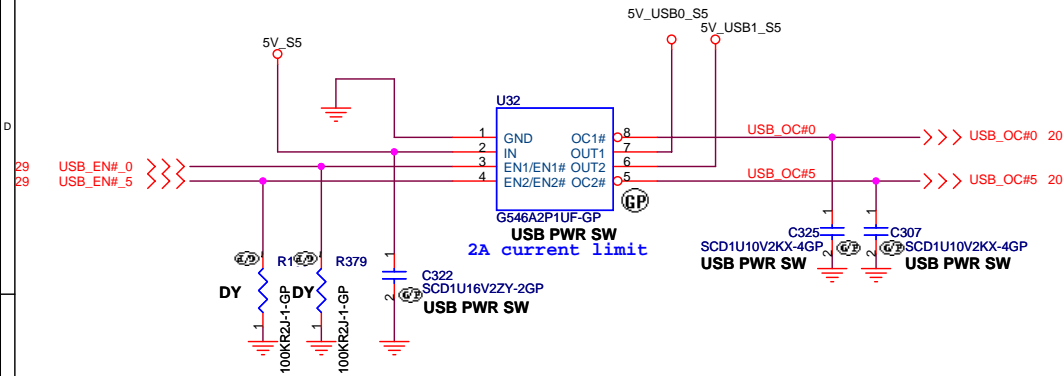


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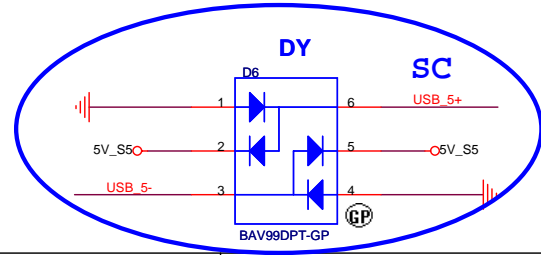
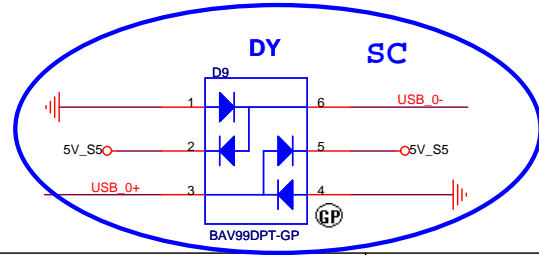
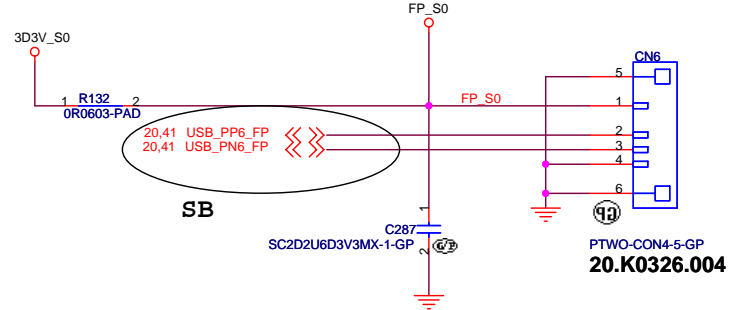
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|--------------------------------|-------------------------|-------|-----------|
| Title | | | |
| MINI CARD & NEWCARD | | | |
| Size A3 | Document Number | Rev | |
| | LZ2 | | SB |
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USB * 3 PORT

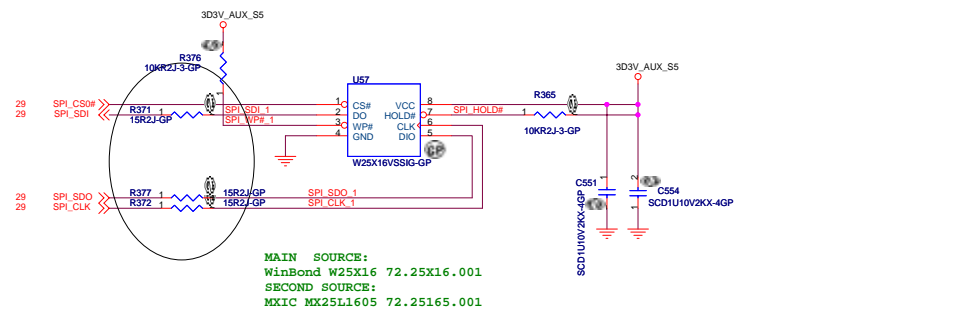


Finger Print

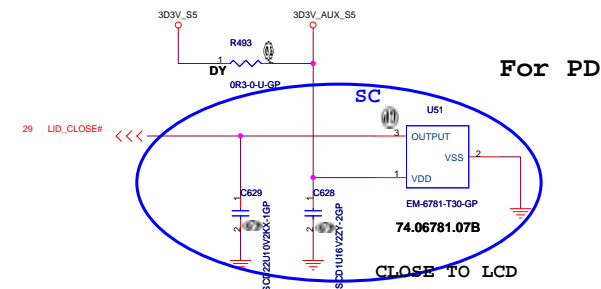


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| USB CONN/FINGER PRINT | | | |
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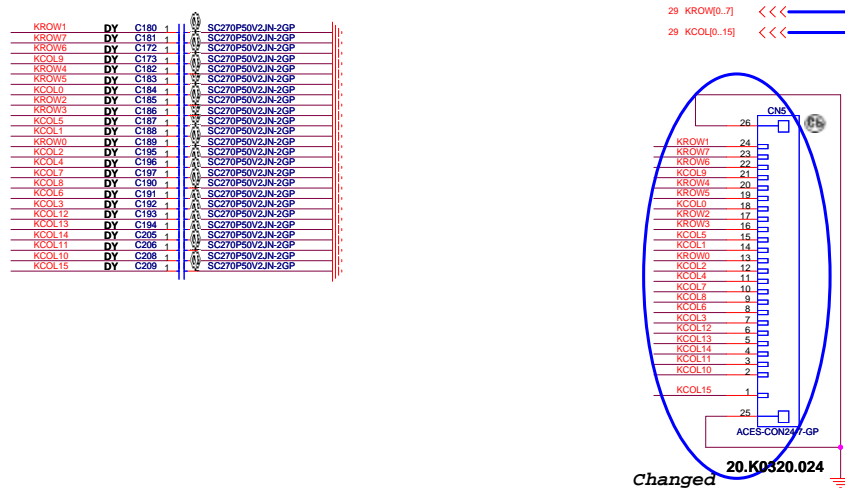
SPI Flash



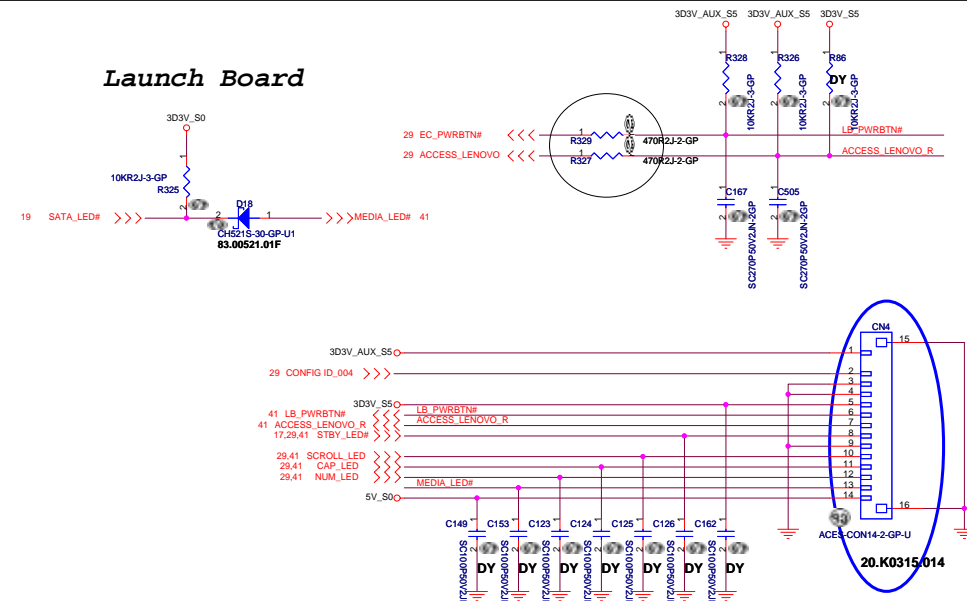
Lid Switch



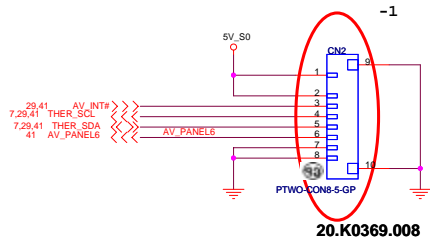
Keyboard Connector



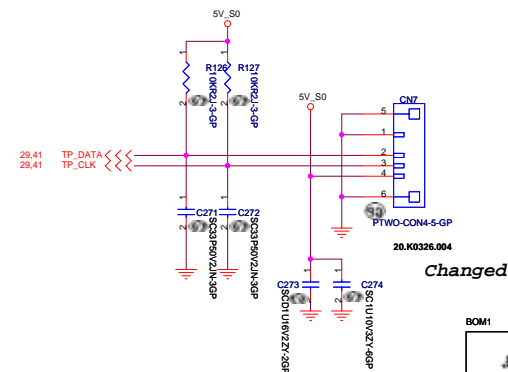
Launch Board

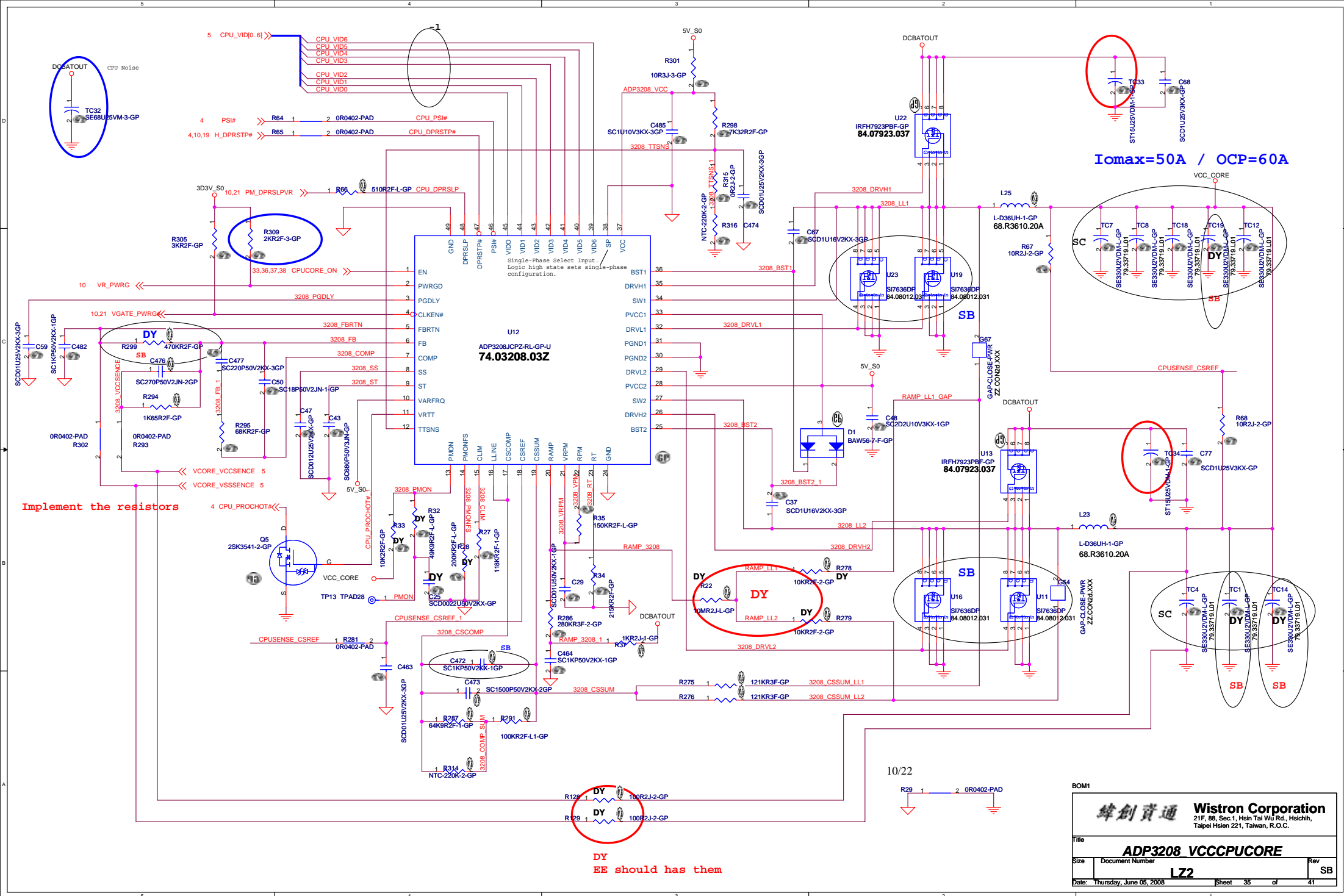


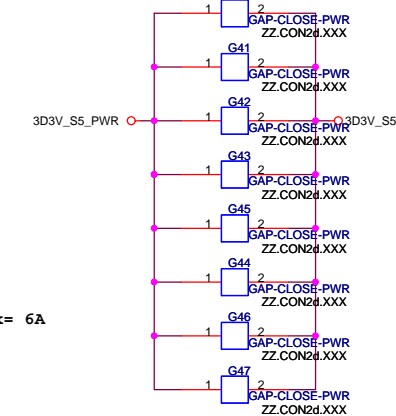
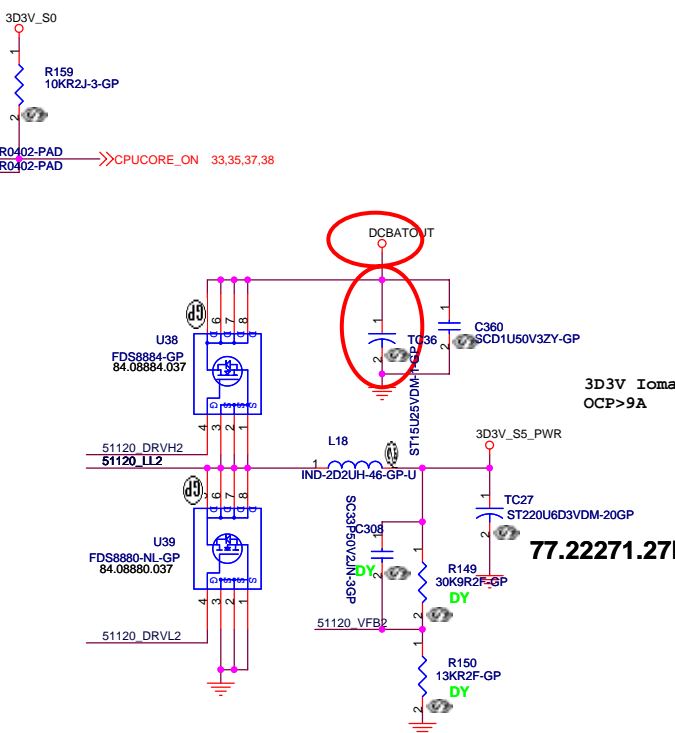
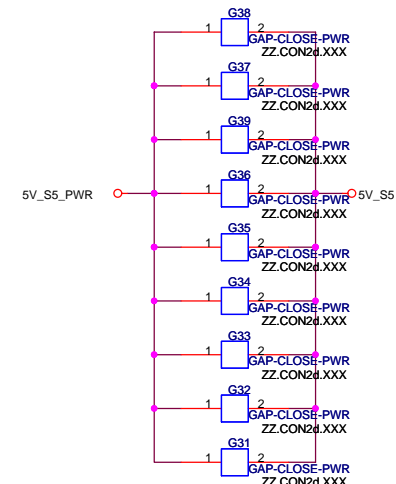
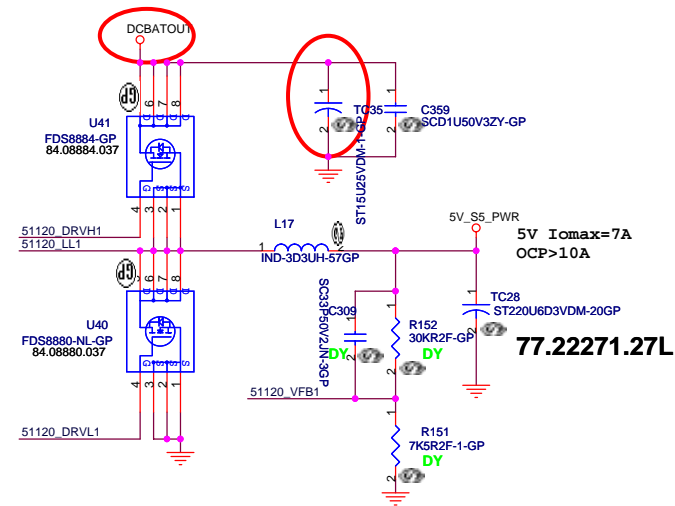
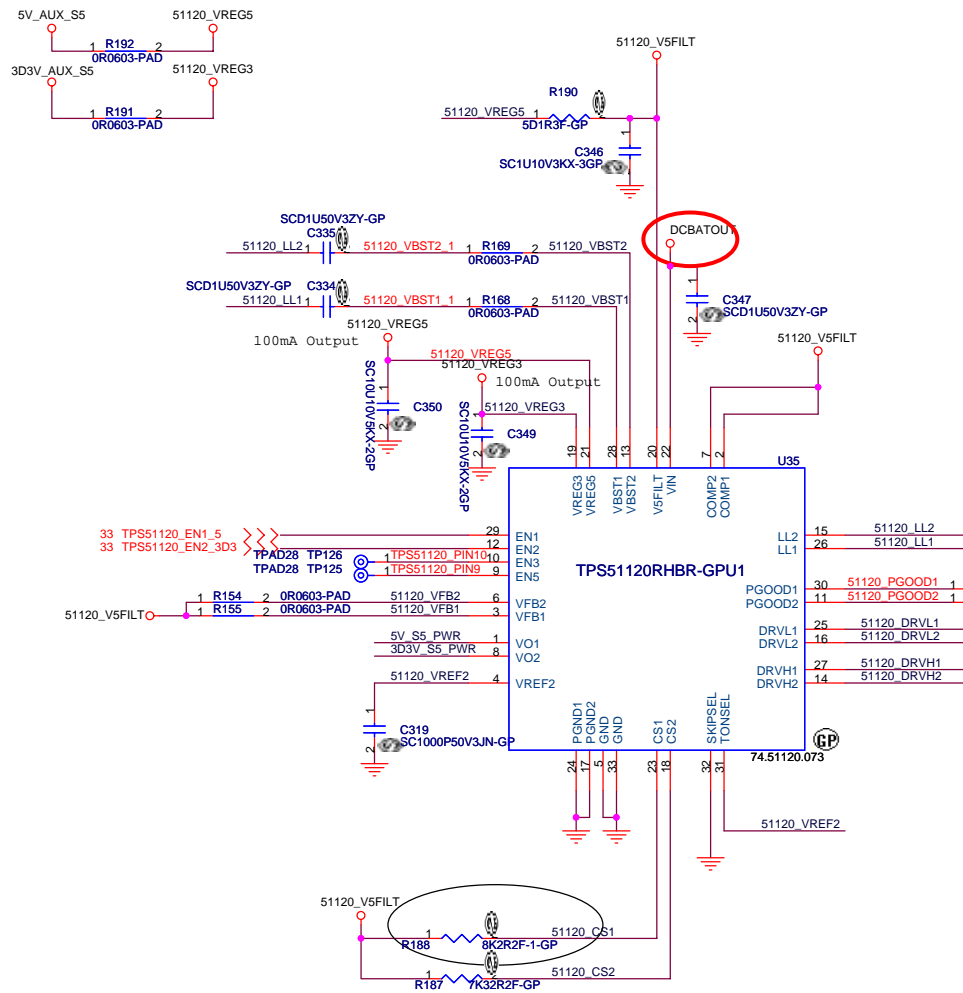
AV Panel



TouchPad Connector







| | GND | VREF2 | FLOAT | V5FILT |
|---------|----------------------|-----------------------|----------------------|----------------------|
| SKIPSEL | AUTOSKIP | AUTOSKIP / FAULTS OFF | PWM | PWM |
| | N/A | N/A | CURRENT MODE | D-Cap MODE |
| | 380k/CH1 590k/CH2 | 280k/CH1 430k/CH2 | 220k/CH1 330k/CH2 | 180k/CH1 280k/CH2 |
| | N/A | not use | ADJ. | 5V Fixed Output |
| | N/A | not use | ADJ. | 3.3V Fixed Output |
| | switcher OFF | not use | Switchchr ON | Switcher ON |
| | LDO OFF | not use | LDO ON | VREG3 on |

For TPS51120,
Vout=5V

1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V

1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

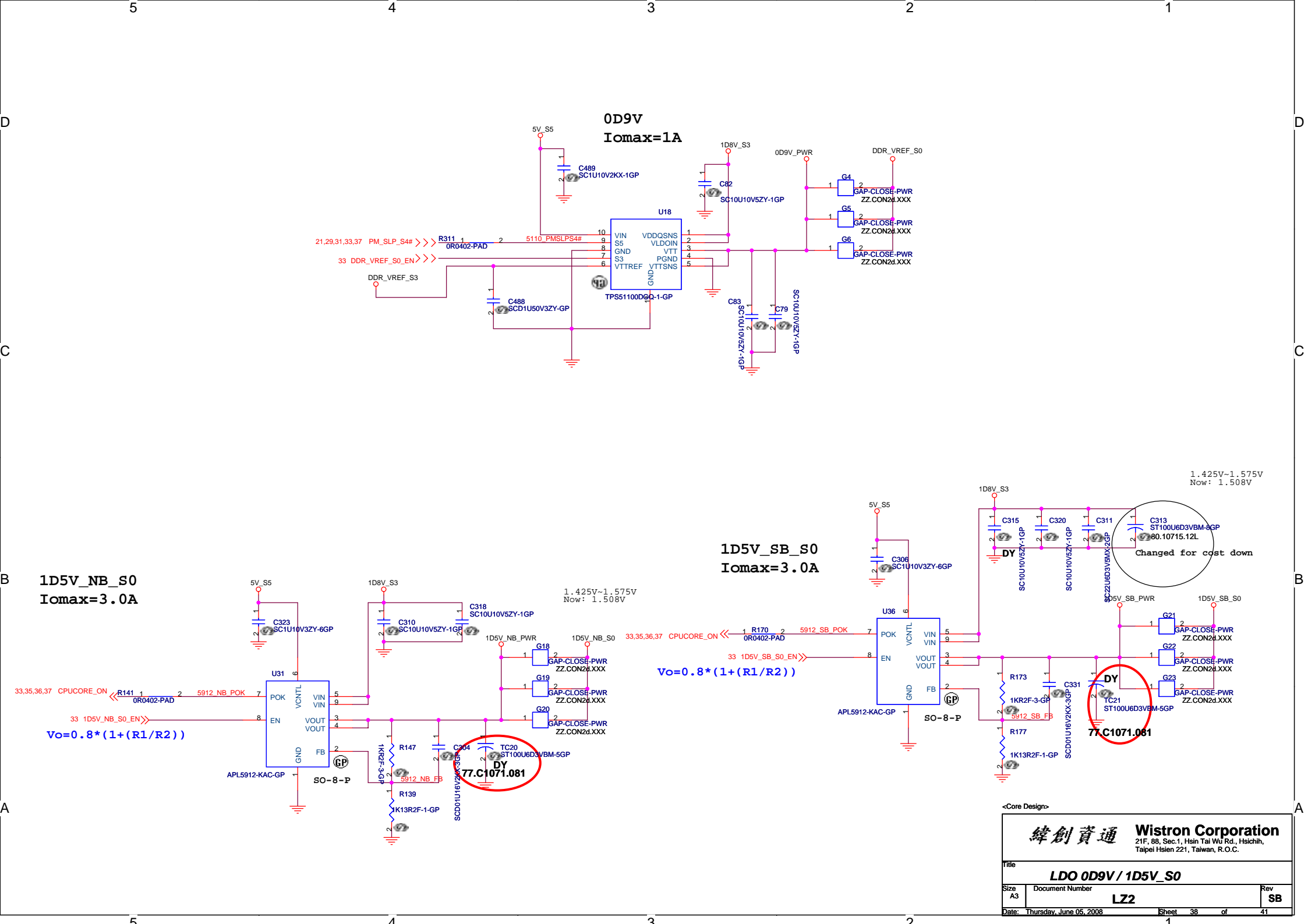
<Core Design>

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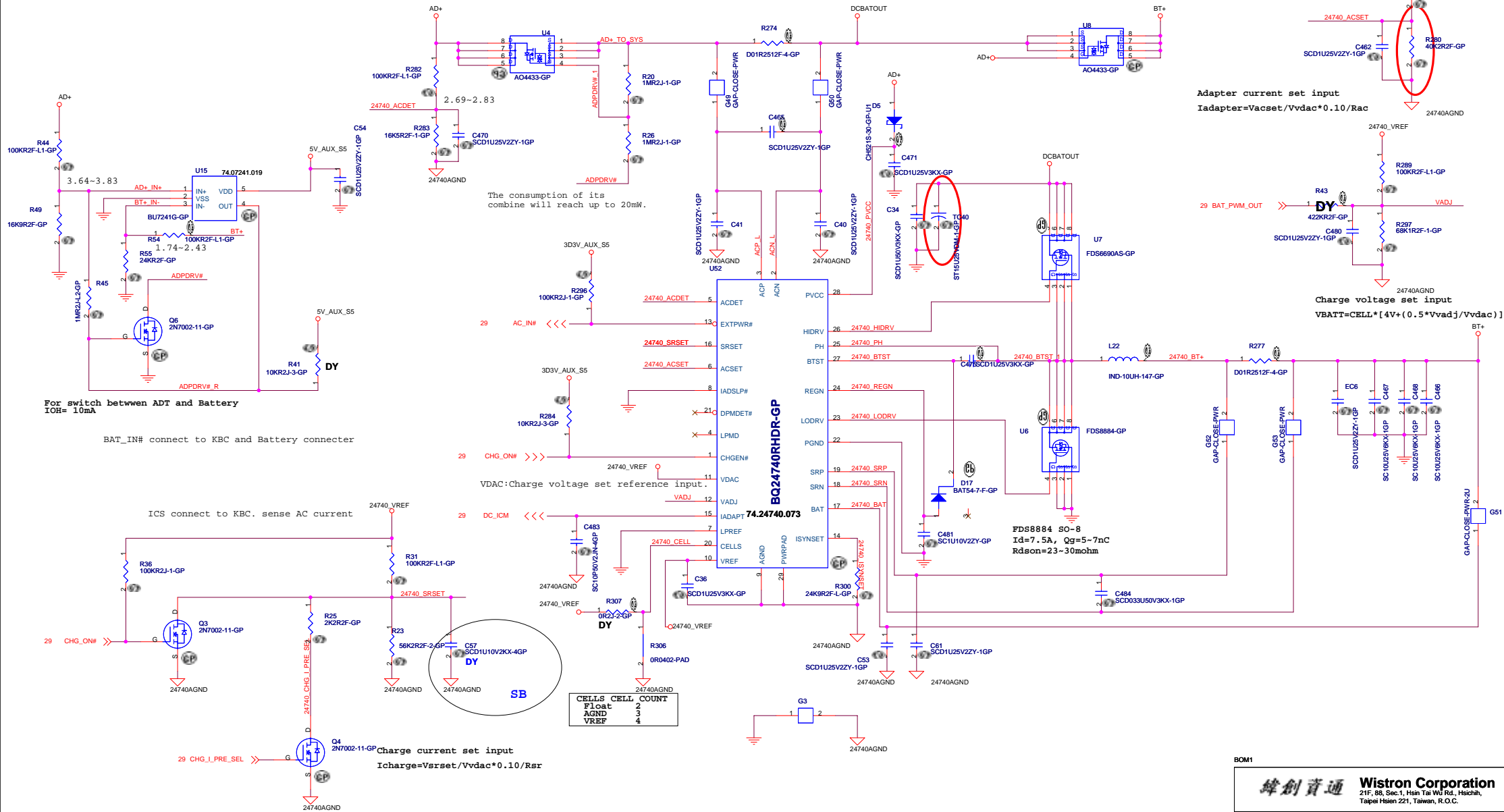
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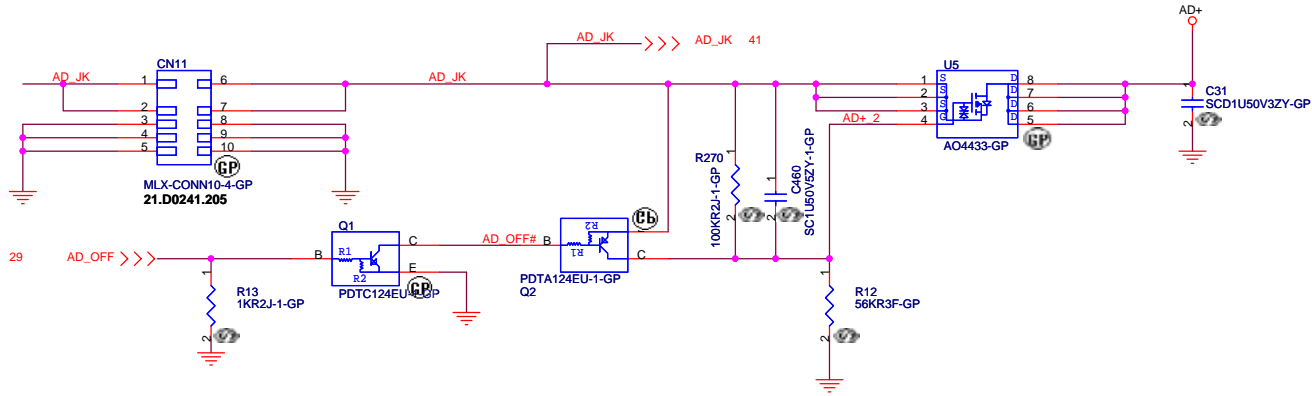
CHARGER



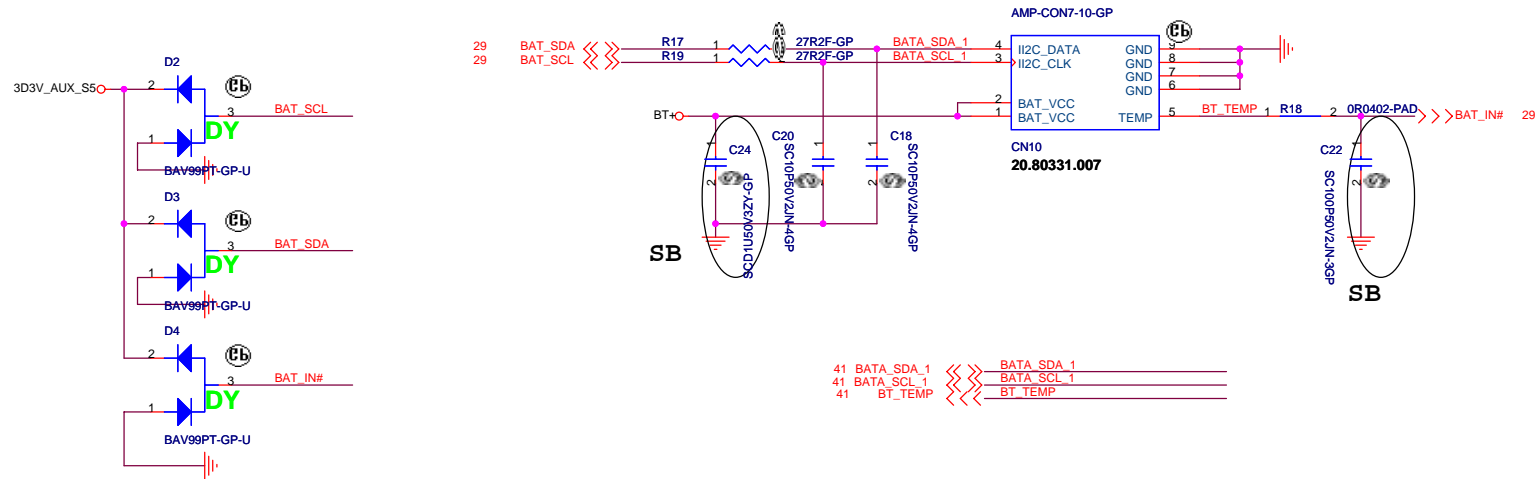
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| Title | | | |
| Charger BQ24740 | | | |
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Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

緯創資通

Wistron Corporation
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|-------|-----------------------------------|

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