

Compal Confidential

Model Name :Q5WV1/Q5WS1

Compal Project Name :

File Name : LA-7912P

Compal Confidential

Q5WV1 M/B Schematics Document
Intel Sandy/Ivy Bridge Processor with DDRIII + Panther Point PCH
Nvidia N13P GS/GL

2011-12-24

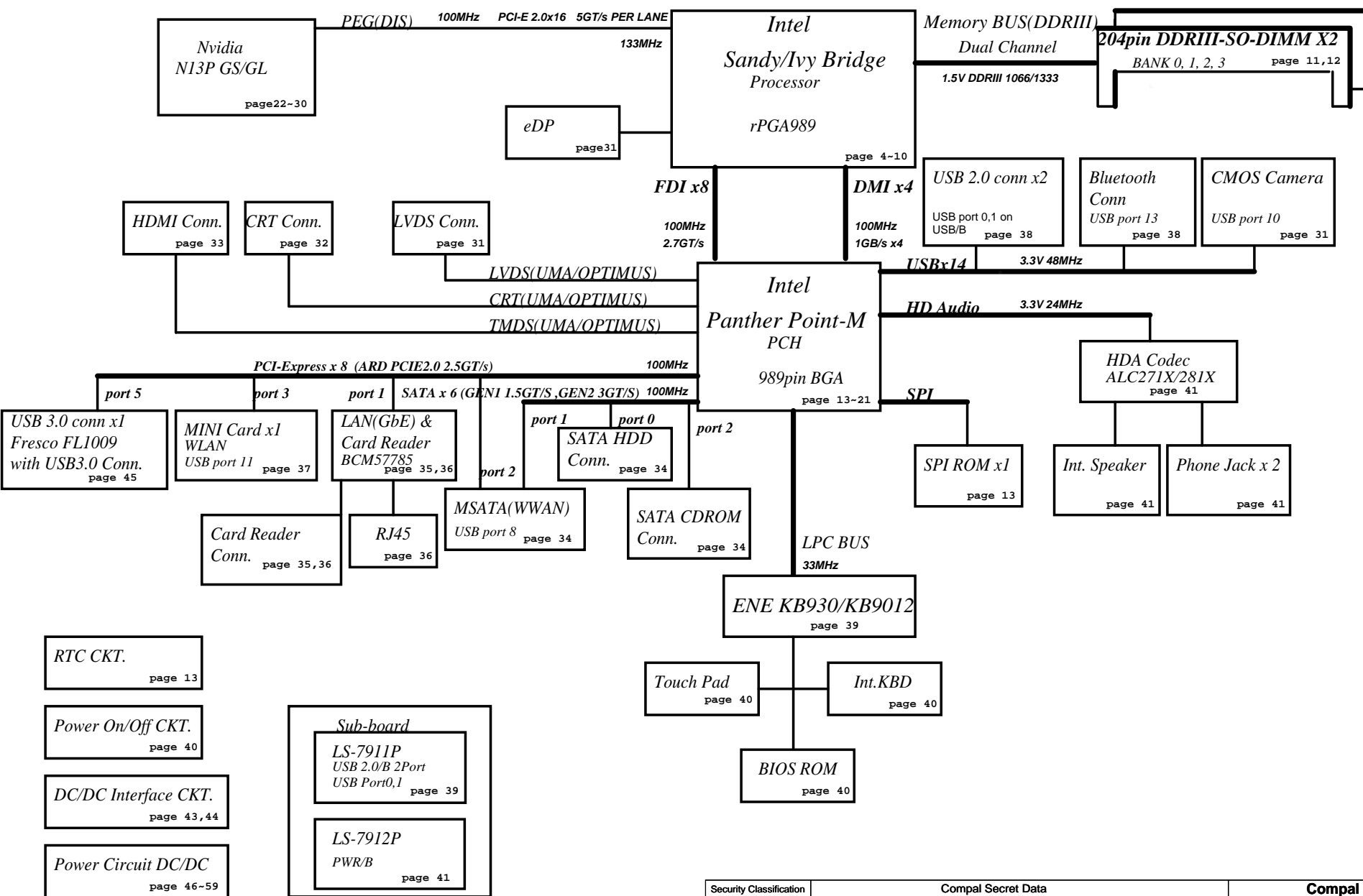
REV : 0 . 2

MB PCB	
Part Number	Description
DA60000SV00	PCB 0N4 LA-7912P REV0 M/B



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Fan Control
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BT & USB30 & USB20 Config

OPTMIUS SKU:DIS@ N13P-GL:GL@ N13P-GS:GS@ N13P-GF108_ES4:GF108@

BT SKU:BT@

internal USB SKU: PUSB@ DIS USB30 SKU:DUSB@

eDP SKU: EDP@

LVDS SKU: LVDS@

EC 930 SKU: 930@ EC 9012 SKU: 9012@

PCH HM65: HM65@ PCH HM76: HM76@

Win8: WIN8@

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	0.1
4	0.2
5	0.3
6	0.4
7	

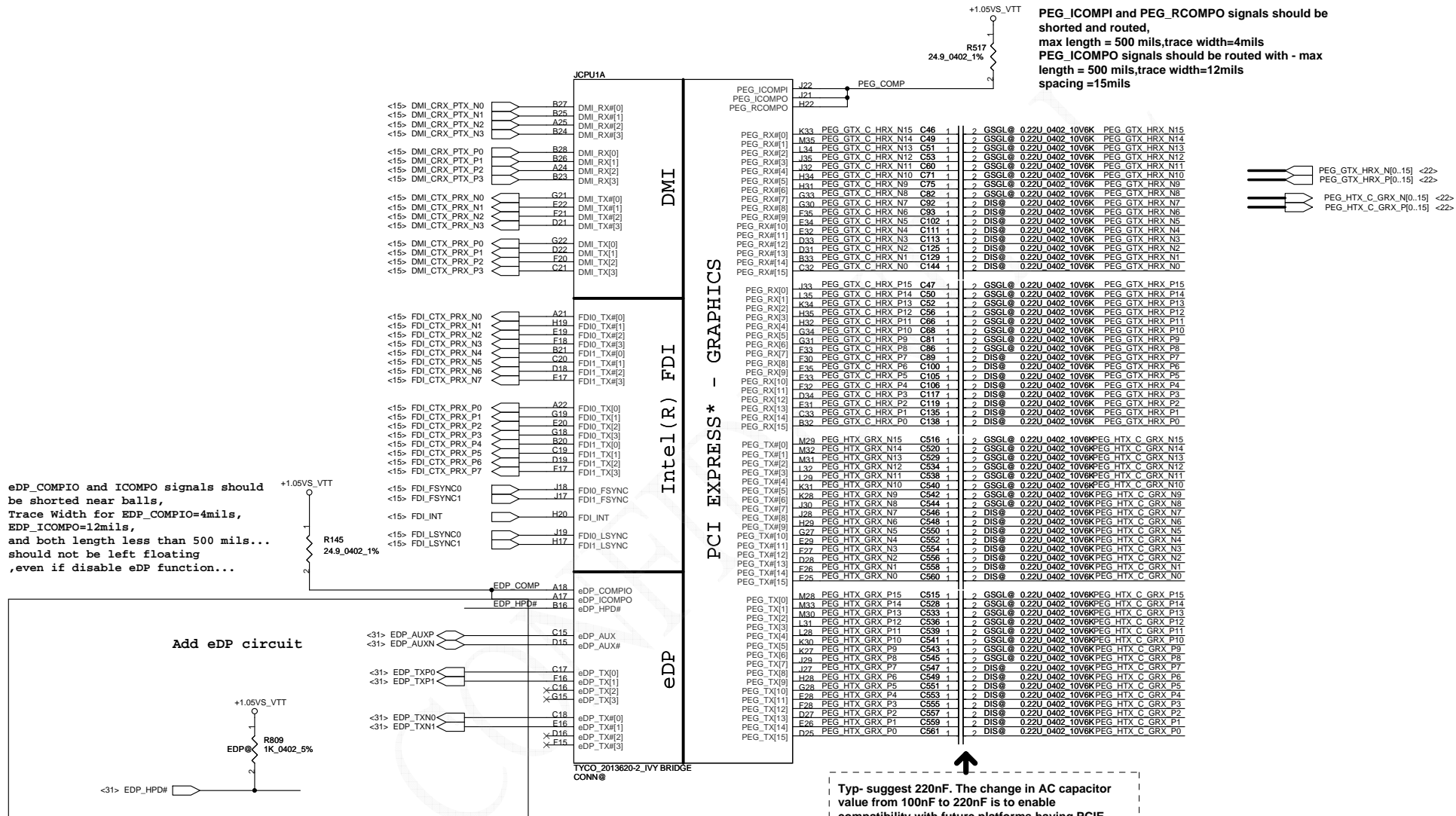
BTO Option Table

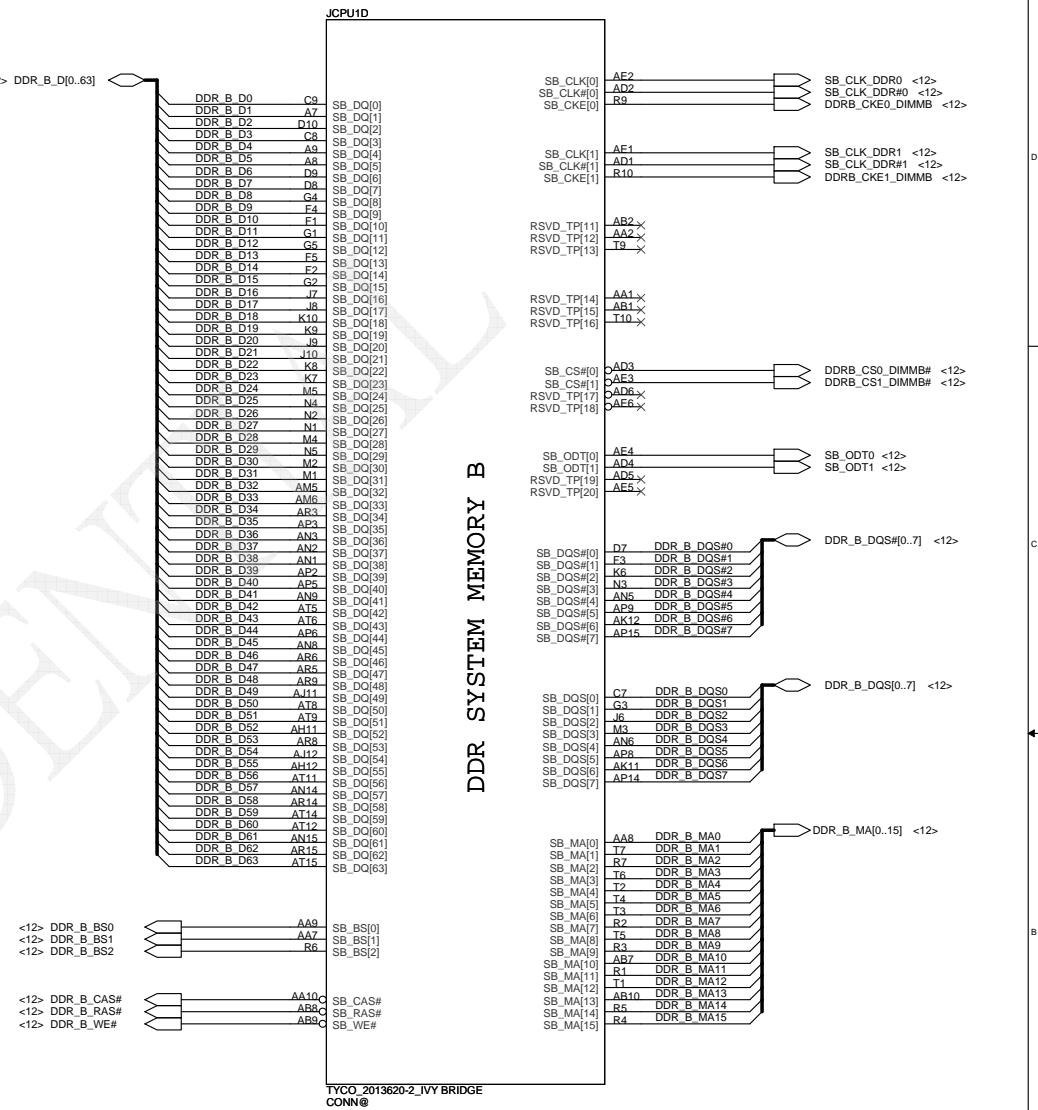
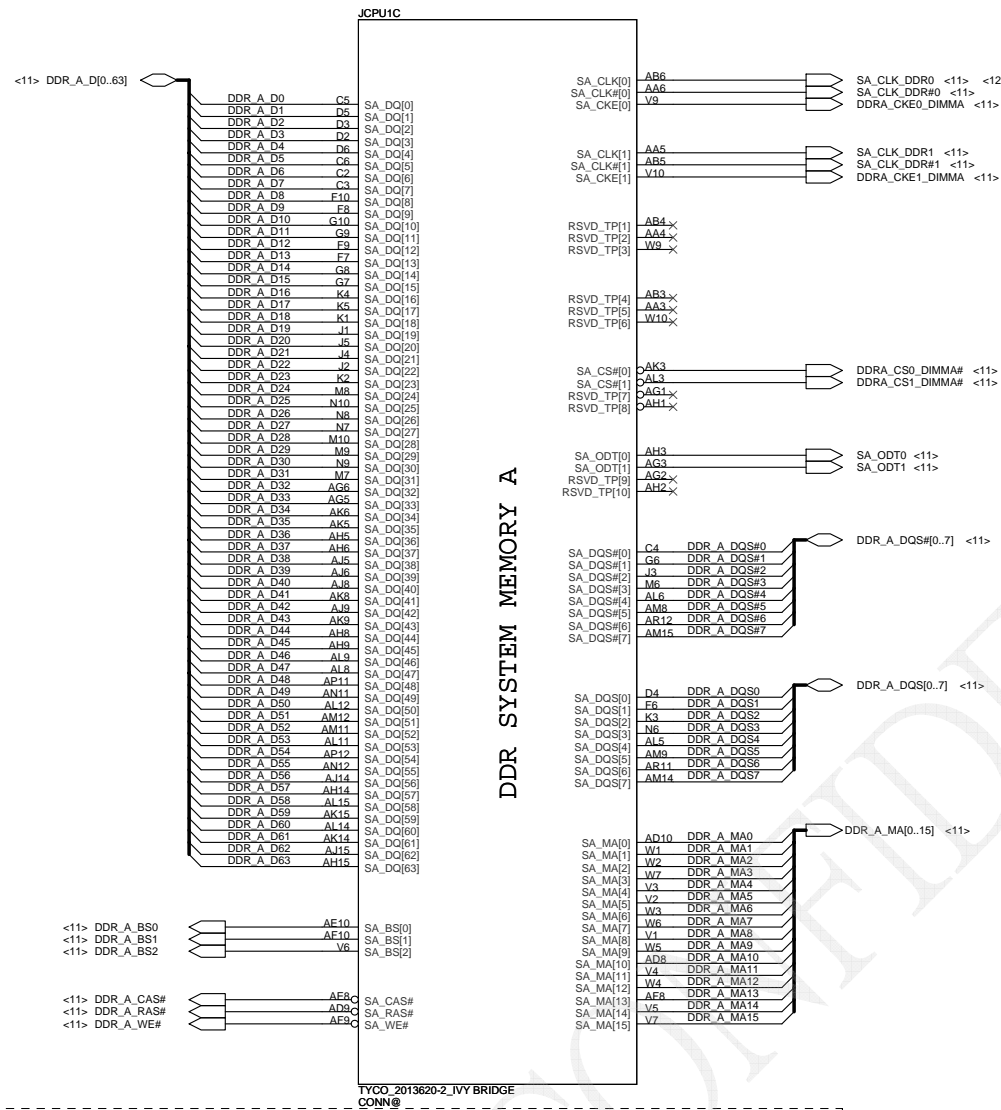
BTO Item	BOM Structure
UMA Only	UMAO@
Dis with OPTIMUS	DIS@
Blue Tooth	BT@
Internal USB 3.0	PUSB@
eDP	eDP@
VRAM	X76@
Connector	CONN@
Unpop	@
N13P-GS	GS@
N13P-GL	GL@
Win8	Win8@
Audio ALC271X	271X@
Audio ALC281X	281X@
PCH HM65	HM65@
PCH HM76	HM76@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB3.0 colay USB2.0 Conn
		1	USB/B (Right Side)
		2	USB/B (Right Side)
	UHCI1	3	
		4	
		5	
EHCI2	UHCI3	6	
		7	
		8	Mini Card 1(WLAN)
	UHCI4	9	
		10	Camera
		11	BlueTooth
	UHCI5	12	
		13	

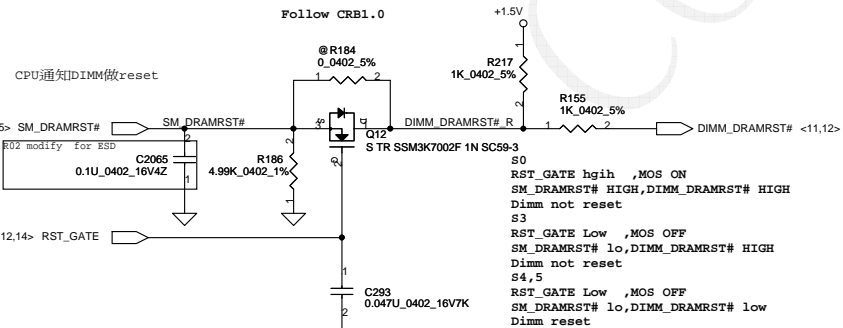
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DDR SYSTEM MEMORY A

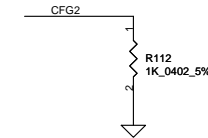
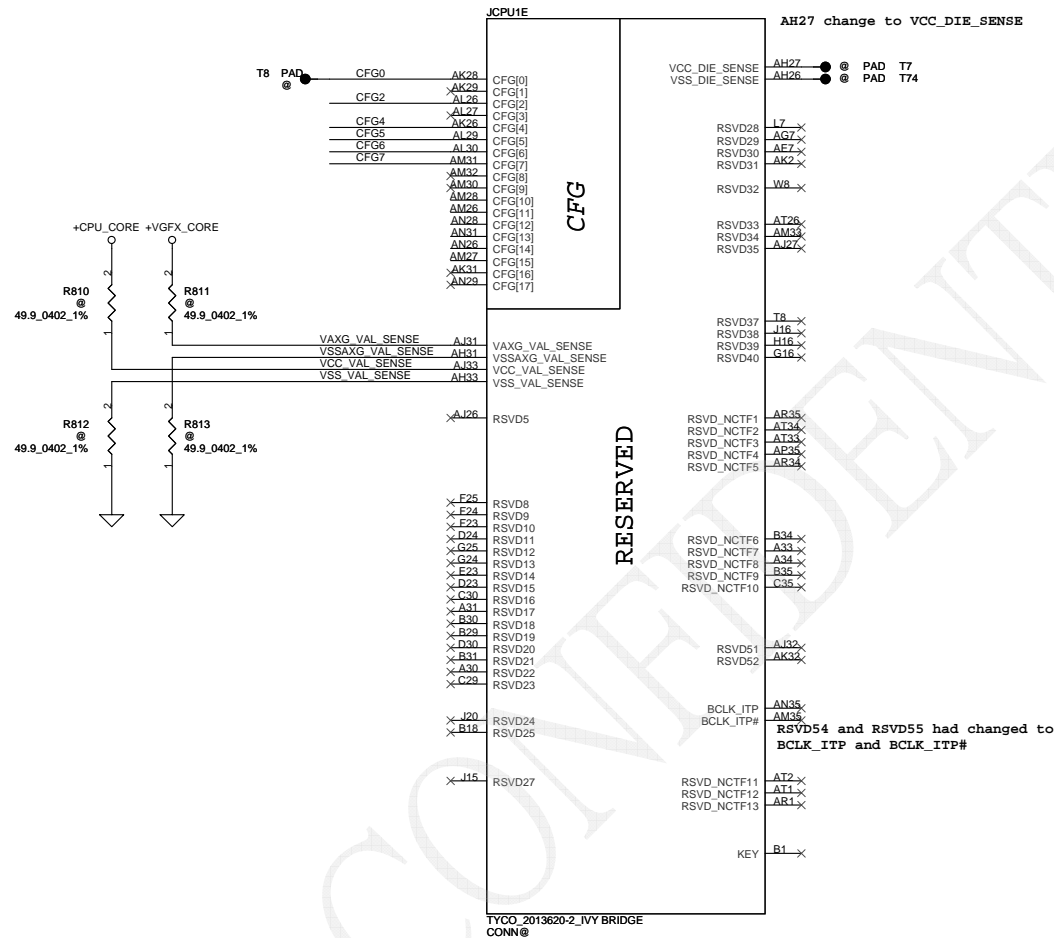
DDR SYSTEM MEMORY B



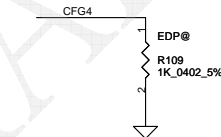
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CFG Straps for Processor

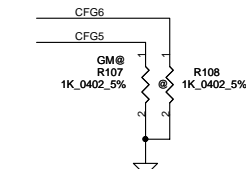
AH26	Sandy	Ivy
	GND	VSS_DIE_SENS



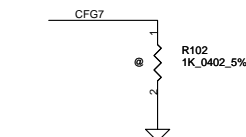
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	<p>1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>* 0: Lane Reversed</p>



Display Port Presence Strap	
CFG4	<p>★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>



PCIE Port Bifurcation Straps	
CFG[6:5]	★11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	<p>1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>

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SV type CPU

JCPU1F

POWER

+CPU_CORE

QC 53A
DC 53A

8.5A

+1.05VS_VTT

VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
VCC7
VCC8
VCC9
VCC10
VCC11
VCC12
VCC13
VCC14
VCC15
VCC16
VCC17
VCC18
VCC19
VCC20
VCC21
VCC22
VCC23
VCC24
VCC25
VCC26
VCC27
VCC28
VCC29
VCC30
VCC31
VCC32
VCC33
VCC34
VCC35
VCC36
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VCC38
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VCC40
VCC41
VCC42
VCC43
VCC44
VCC45
VCC46
VCC47
VCC48
VCC49
VCC50
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VCC56
VCC57
VCC58
VCC59
VCC60
VCC61
VCC62
VCC63
VCC64
VCC65
VCC66
VCC67
VCC68
VCC69
VCC70
VCC71
VCC72
VCC73
VCC74
VCC75
VCC76
VCC77
VCC78
VCC79
VCC80
VCC81
VCC82
VCC83
VCC84
VCC85
VCC86
VCC87
VCC88
VCC89
VCC90
VCC91
VCC92
VCC93
VCC94
VCC95
VCC96
VCC97
VCC98
VCC99
VCC100

VCCIO1
VCCIO2
VCCIO3
VCCIO4
VCCIO5
VCCIO6
VCCIO7
VCCIO8
VCCIO9
VCCIO10
VCCIO11
VCCIO12
VCCIO13
VCCIO14
VCCIO15
VCCIO16
VCCIO17
VCCIO18
VCCIO19
VCCIO20
VCCIO21
VCCIO22
VCCIO23
VCCIO24
VCCIO25
VCCIO26
VCCIO27
VCCIO28
VCCIO29
VCCIO30
VCCIO31
VCCIO32
VCCIO33
VCCIO34
VCCIO35
VCCIO36
VCCIO37
VCCIO38
VCCIO39
VCCIO40

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

VIDALERT#
VIDSCLK
VIDSOUT

A128 H CPU SVIDALRT#
A130 H CPU SVIDCLK
A128 H CPU SVIDDAT

R450 130_0402_1%
R448 43_0402_1%
R446 1 2 0 0.0402 5%
R449 1 2 0 0.0402 5%

Place the PU
resistors close to CPU

VCC_SENSE
VSS_SENSE

A135 VCCSENSE R
A134 VSSSENSE R

R444 1 2 0 0.0402 5%
R443 1 2 0 0.0402 5%

VCCIO_SENSE
VSS_SENSE_VCCIO

R10
A10 VSSIO_SENSE
VSSIO_SENSE
change to
VSS_SENSE_VCCIO

R910 10_0402_5%
R163 10_0402_5%

Should change to connect form
power circuit & layout differential
with VCCIO_SENSE.

+CPU_CORE

R445 100_0402_1%
R442 100_0402_1%

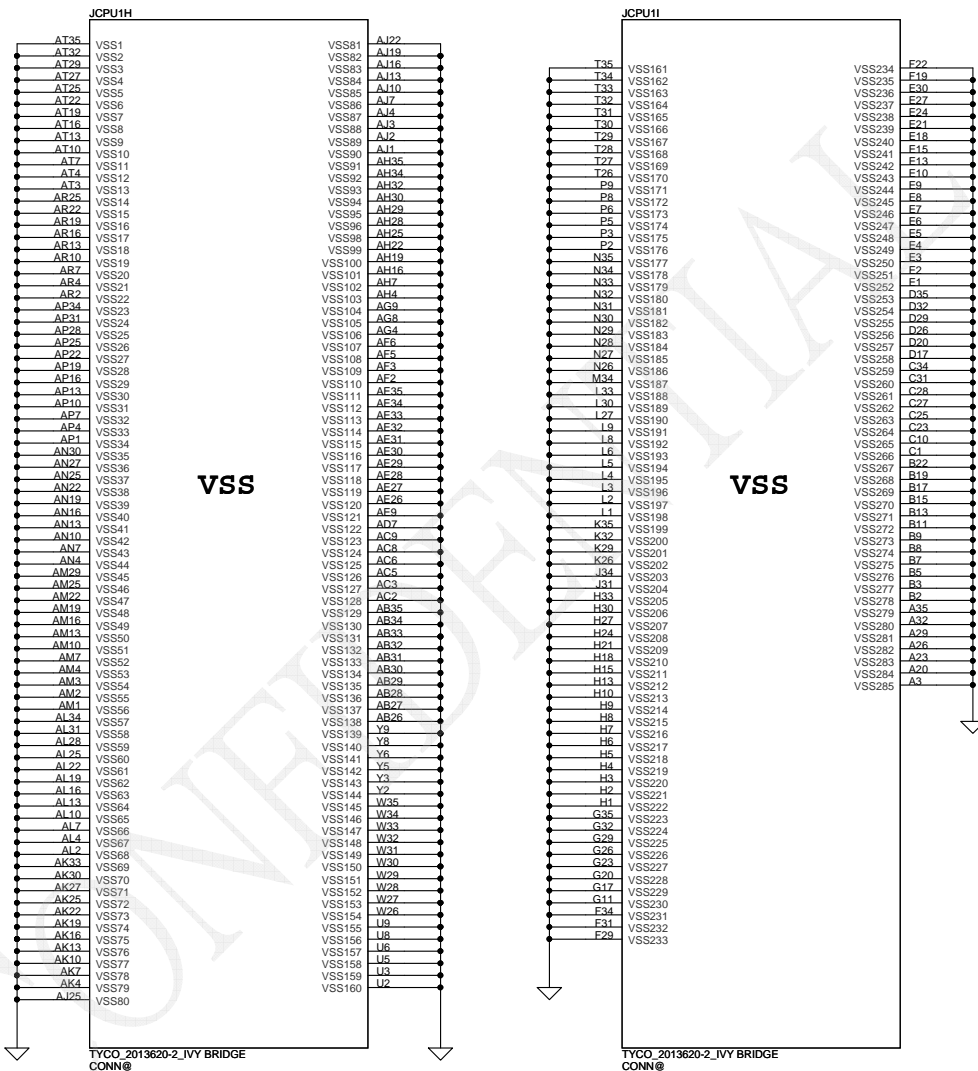
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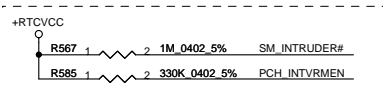
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CONN@

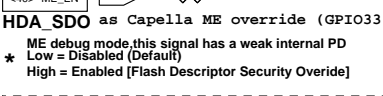
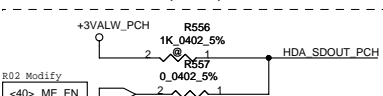
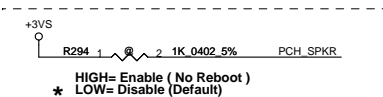
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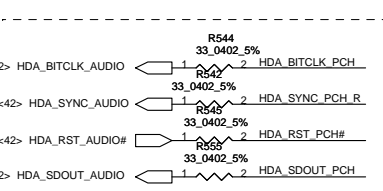




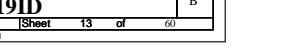
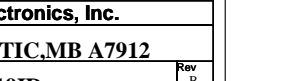
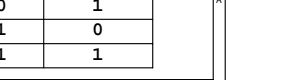
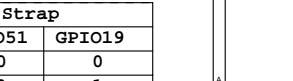
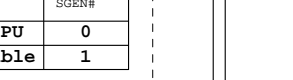
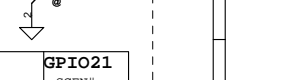
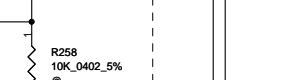
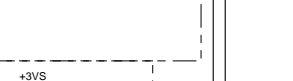
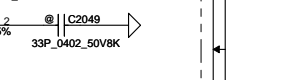
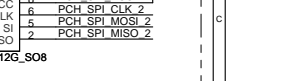
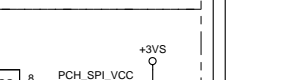
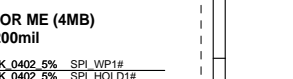
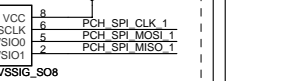
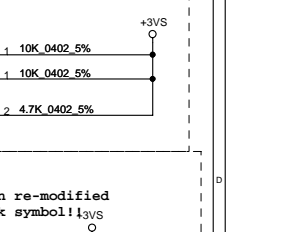
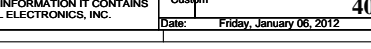
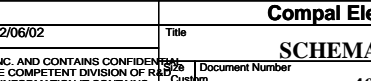
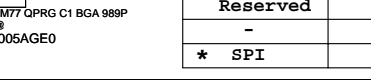
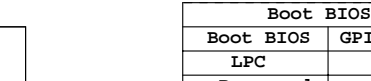
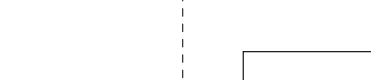
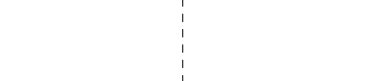
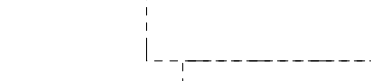
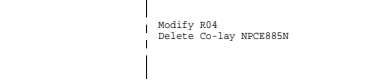
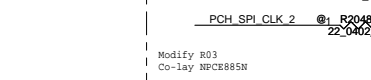
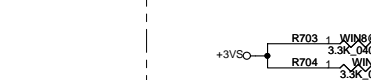
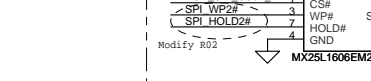
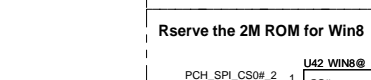
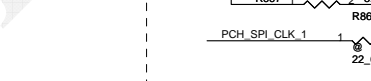
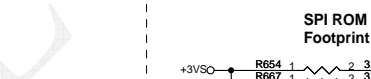
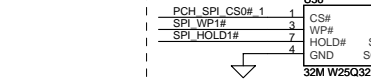
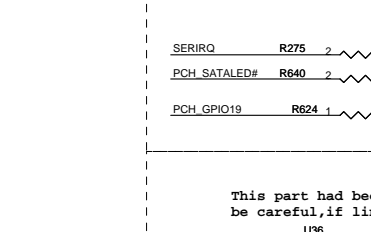
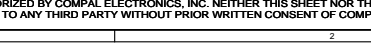
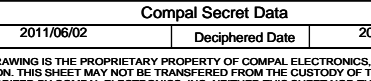
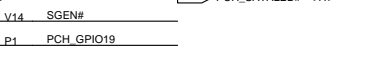
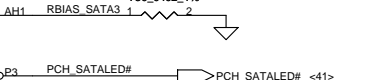
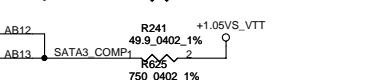
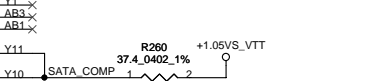
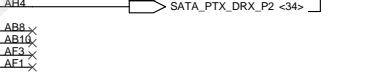
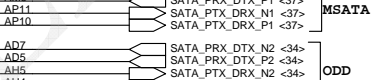
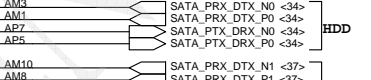
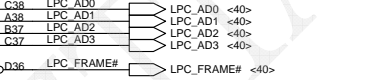
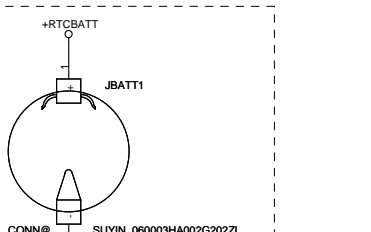
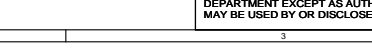
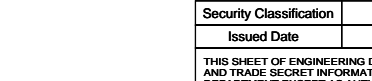
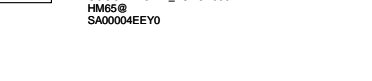
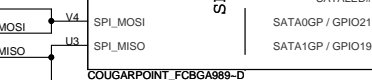
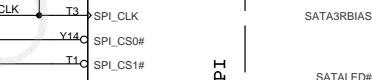
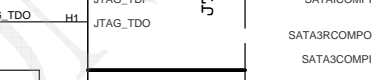
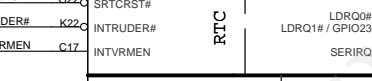
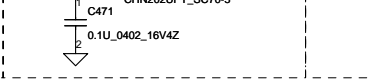
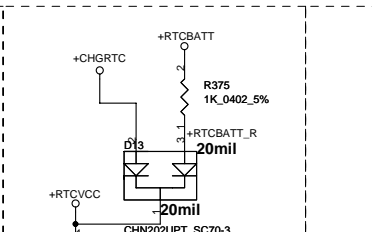
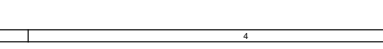
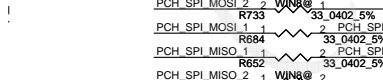
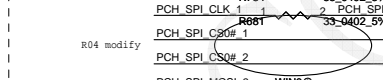
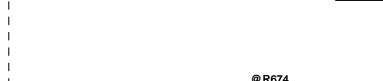
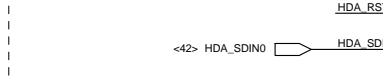
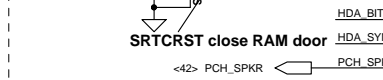
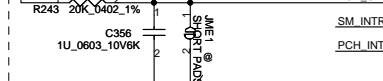
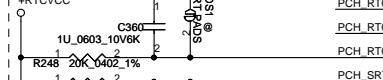
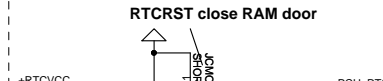
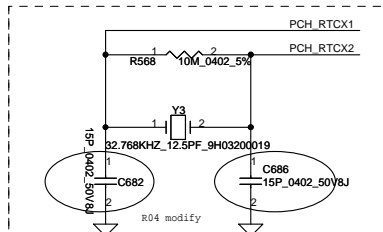
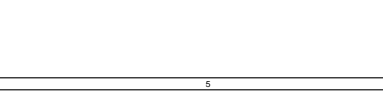
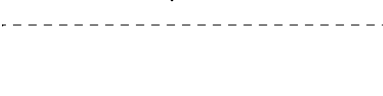
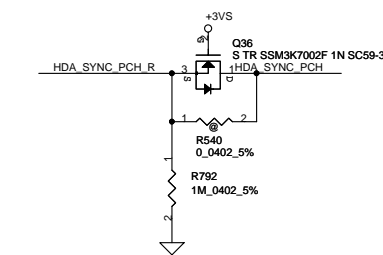
INTVRMEN
★ H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)



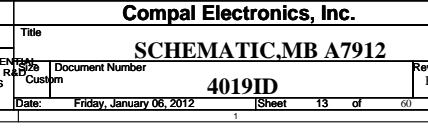
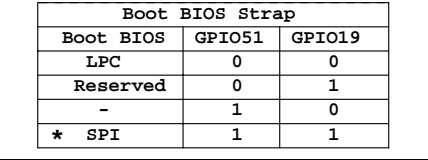
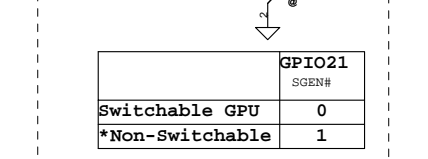
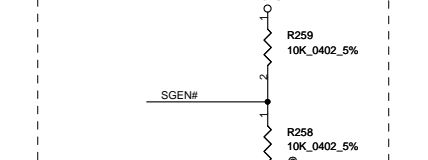
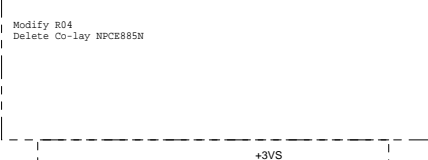
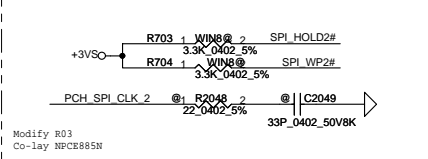
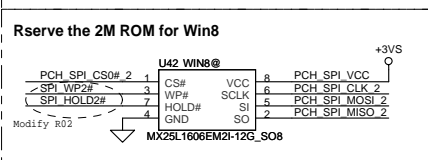
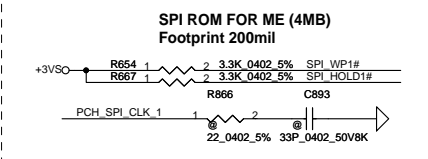
On Die PLL VR Select is supplied by 1.5V when smaped high 1.8V when sampled low Needs to be pulled High for Huron River platform



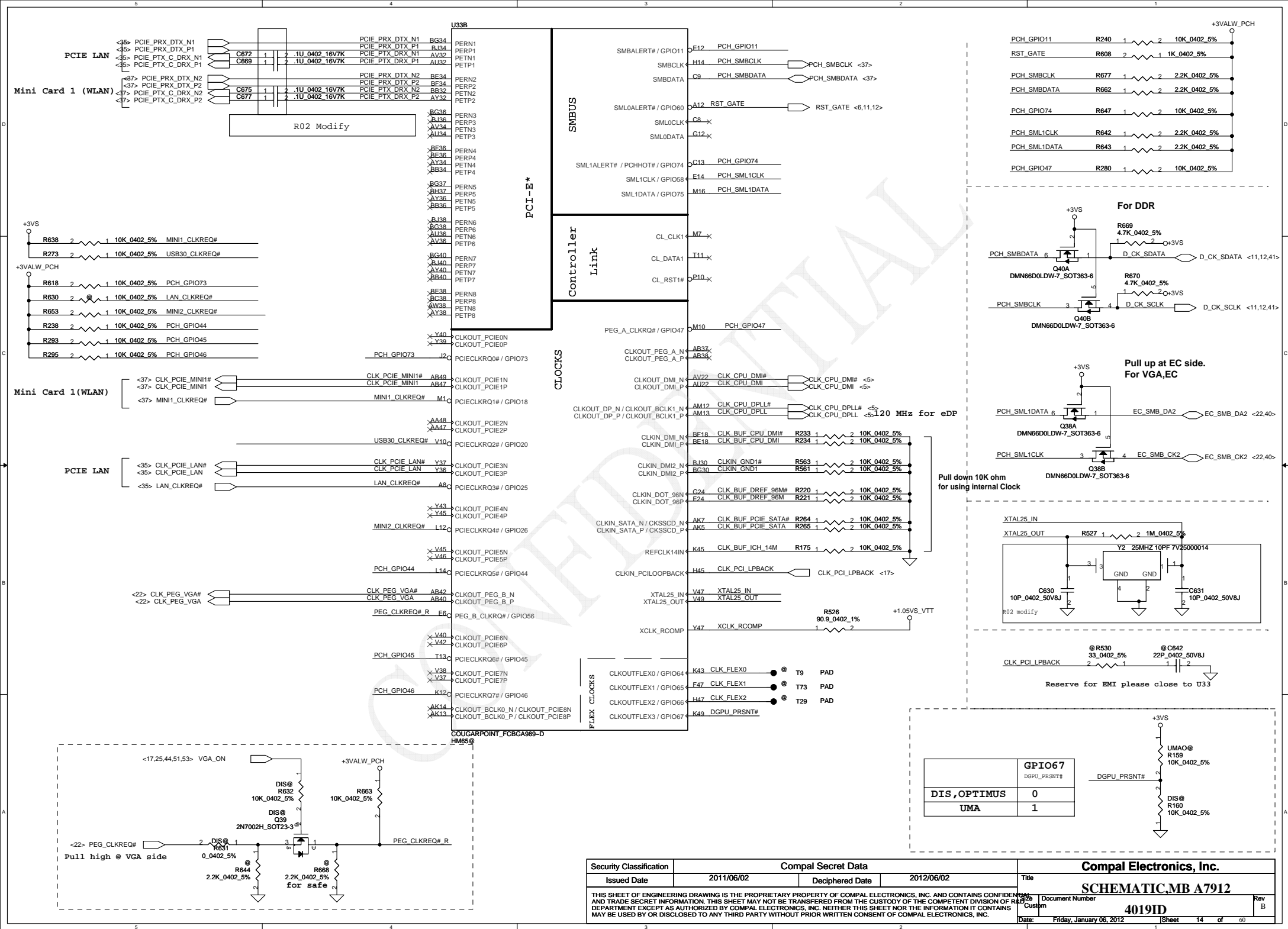
Prevent back drive issue.

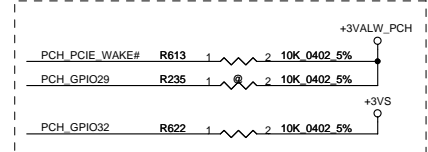
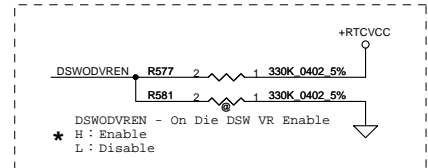
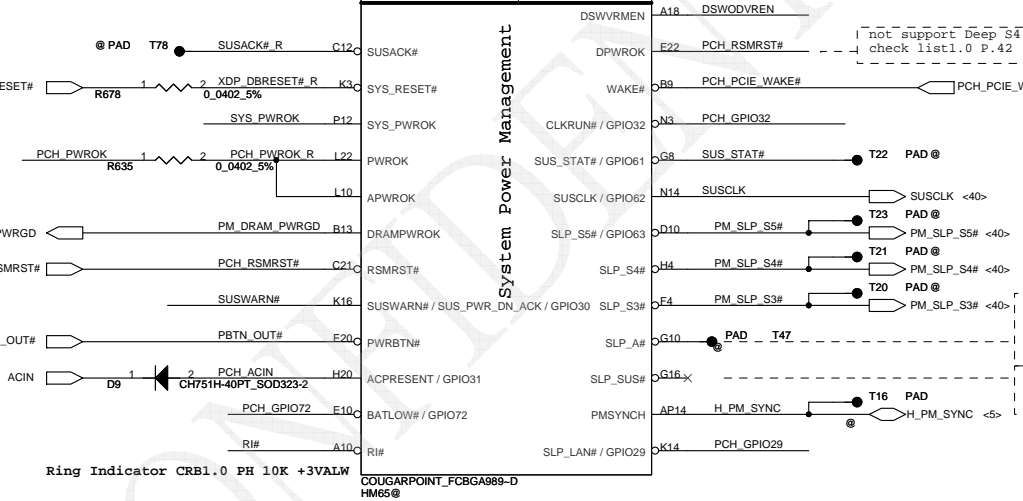
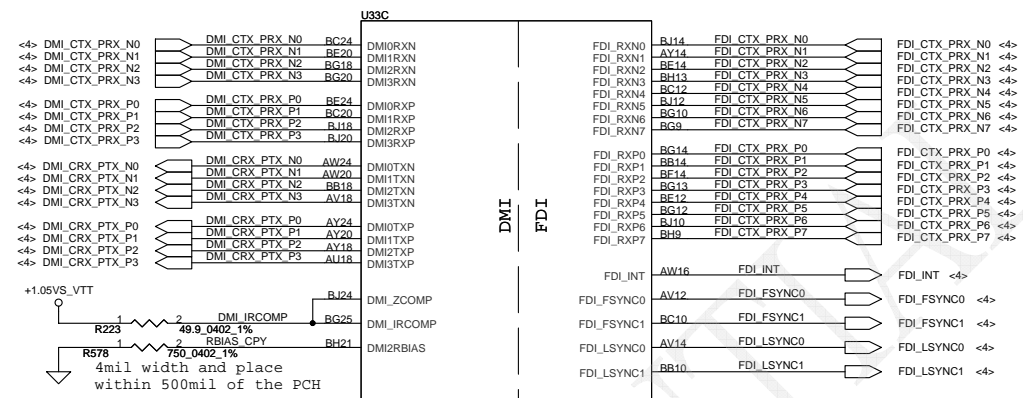
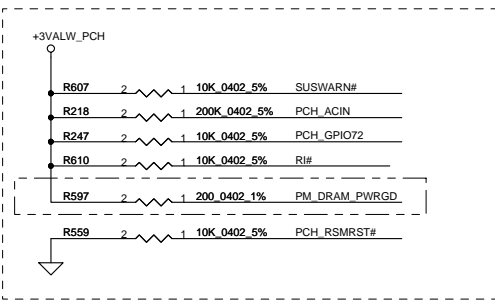


This part had been re-modified be careful, if link symbol!!



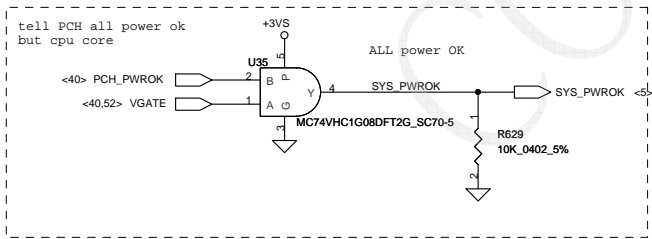
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4019ID			
Date: Friday, January 06, 2012			
Sheet 13 of 60			

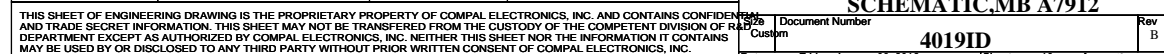


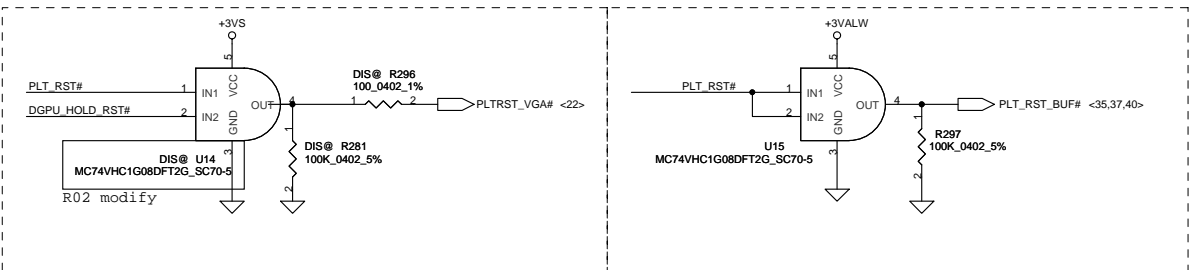
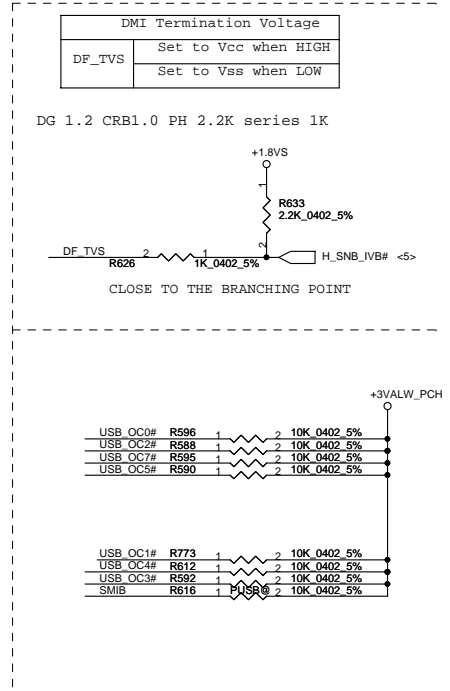
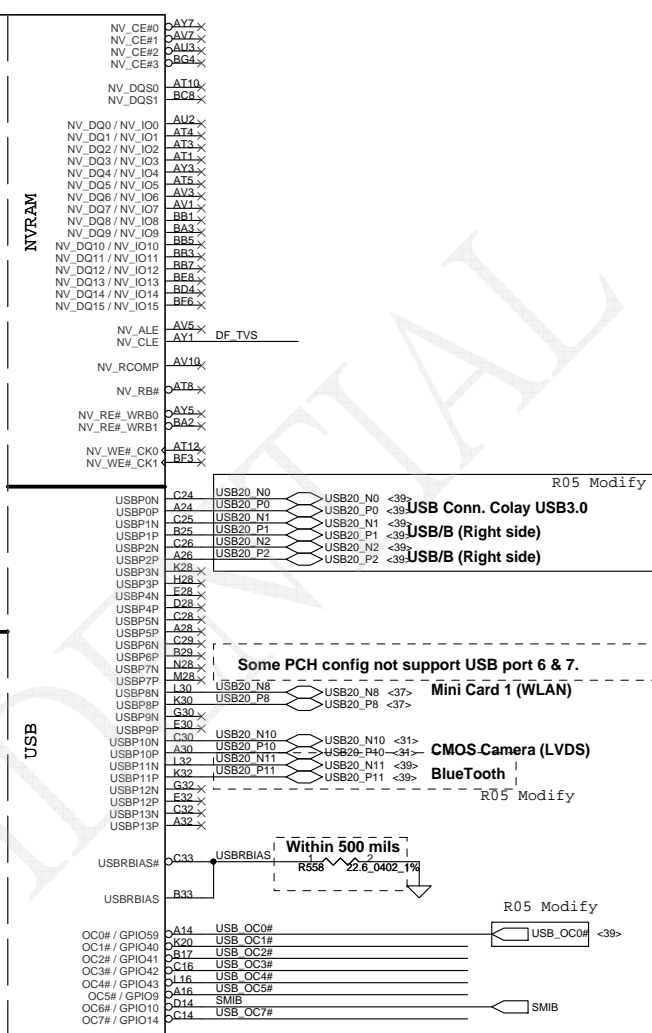
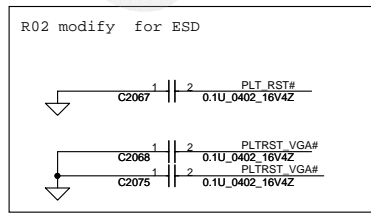
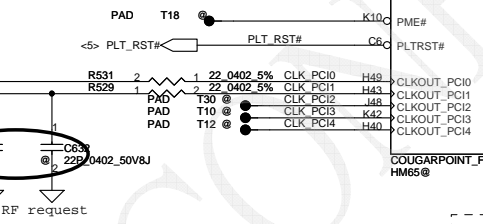
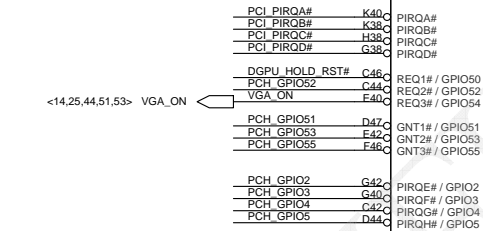
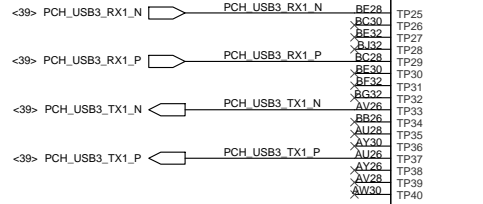
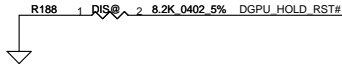
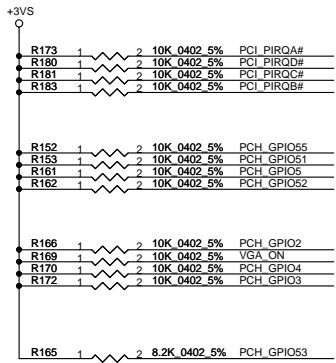


Can be left NC when IAMT is not support on the platform

not support Deep S4,S5 can NC PCH EDS1.2 P.74

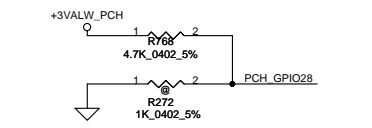




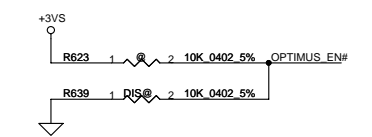
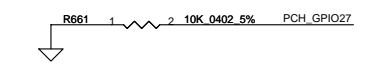


GPI028 HDA_SYNC PH(PLL =+1.5VS)
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

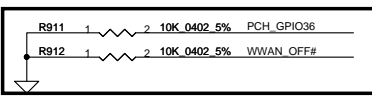
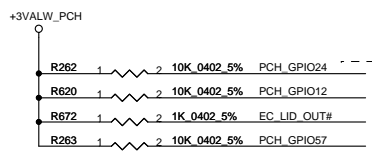
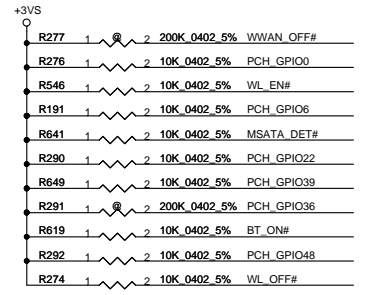
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable



Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPI027
PCH_GPI027 (Have internal Pull-High)
Deep S4,S5 wake event signal
No use PD to GND Check list1.0 P.70

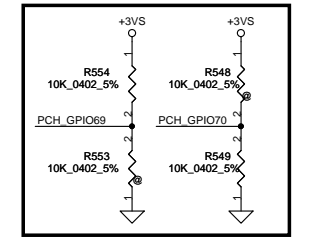
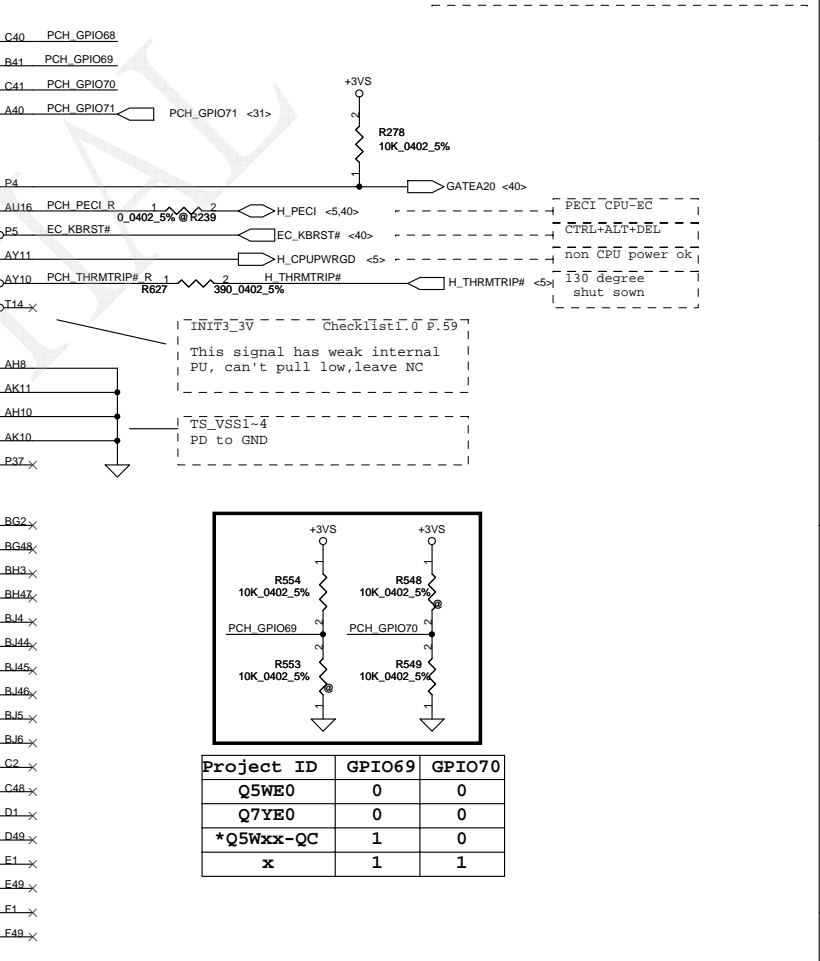
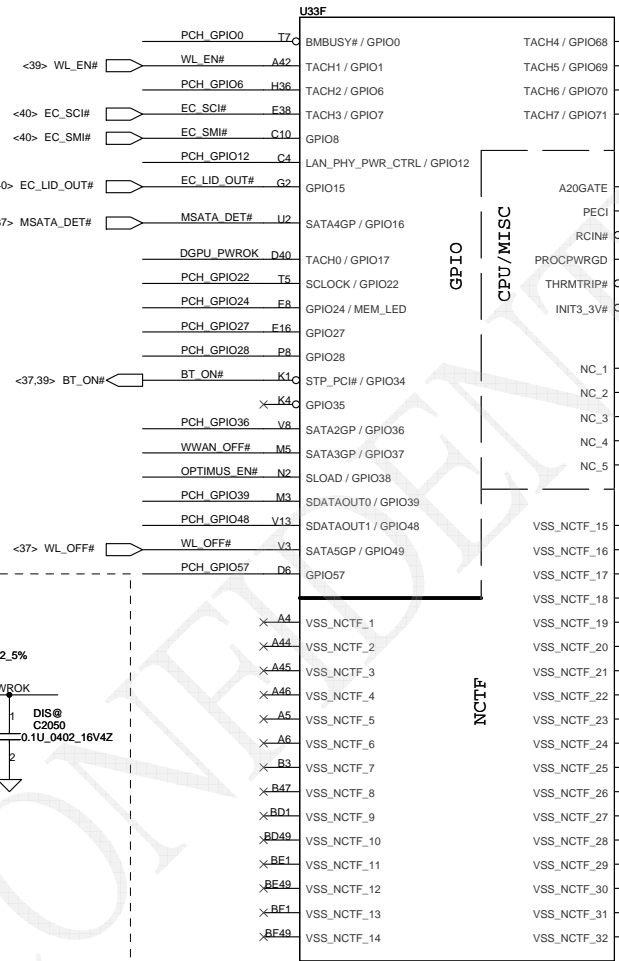


	GPI038
	OPTIMUS_EN#
* OPTIMUS	0
DIS Only	1

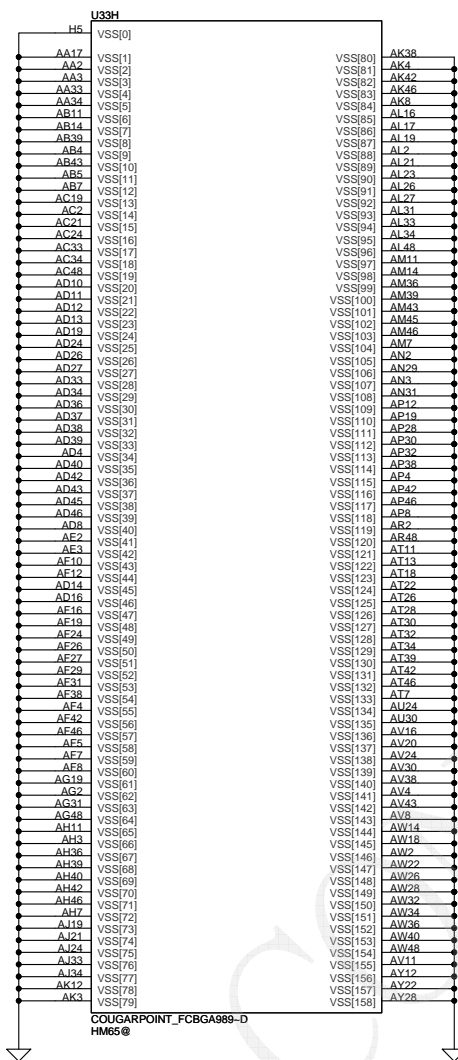


GPI024 Unmultiplexed
NOTE: GPI024 configuration register bits are not cleared by CP9h reset event.
CRB1.0 PH10K to +3VALW

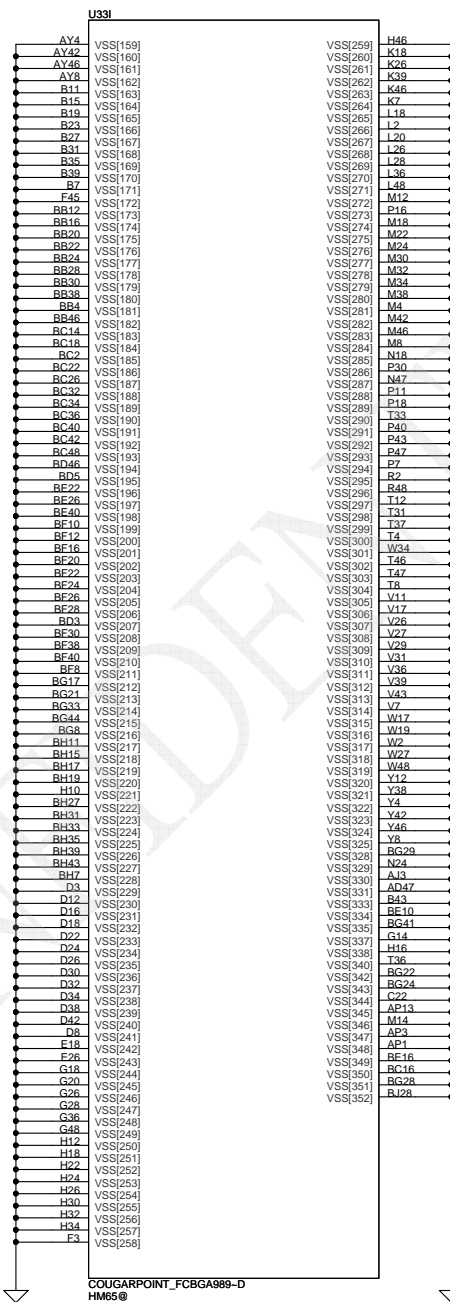
GPI036/GPI037 is Strap functionality that requires internal pull down to be sampled at rising PWROK. When uses as SATA2GP/SATA3GP for mechanical presence detect -use a external pull up 150K-200K ohm to Vcc3_3
When used as GP input -ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA*GP -use 8.2K-10K pull-down
check list page 47



Project ID	GPI069	GPI070
Q5WE0	0	0
Q7YE0	0	0
*Q5Wxx-QC	1	0
x	1	1

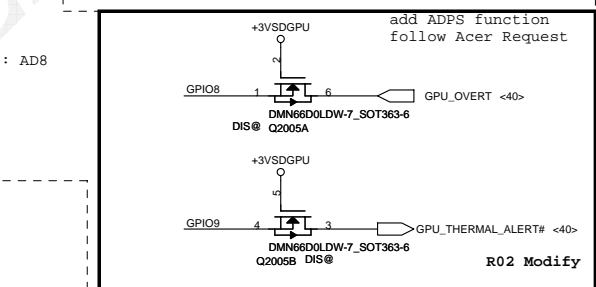
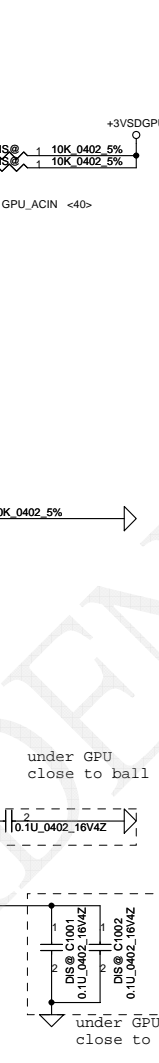
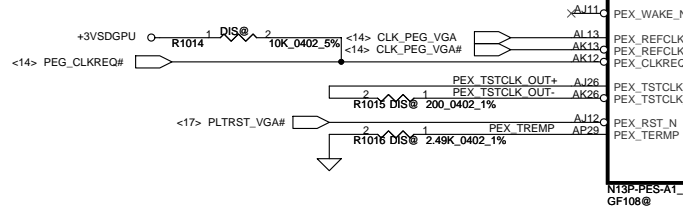


COUGARPOINT_FCBGA989-D
HM65@

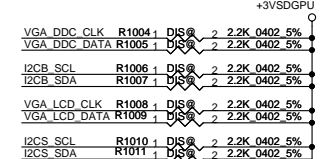
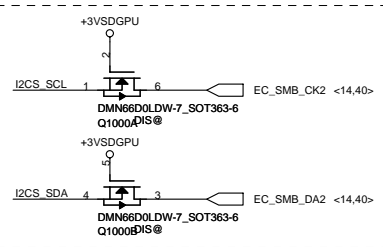


COUGARPOINT_FCBGA989-D
HM65@

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				Rev	B

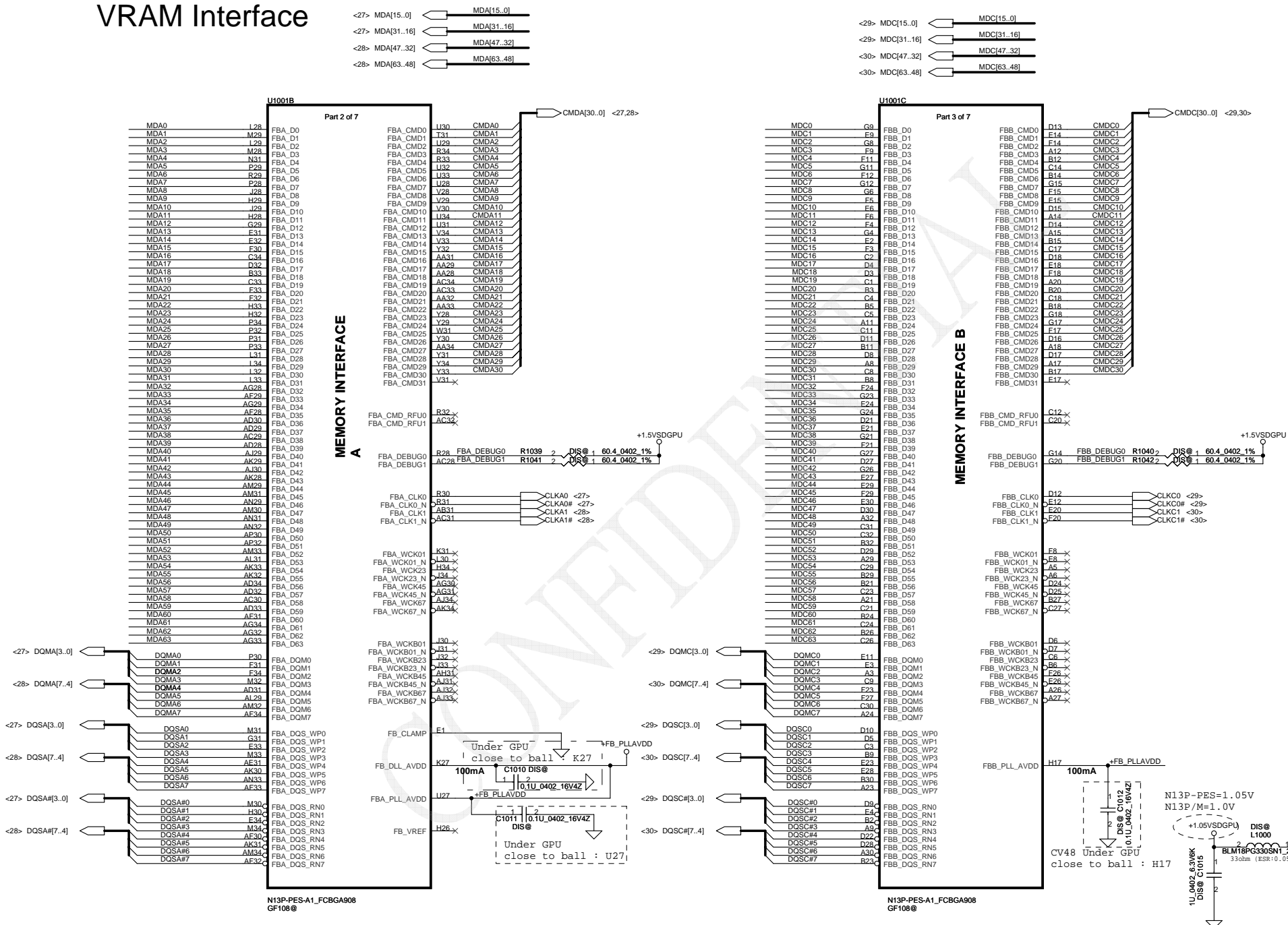


U1001
N13M-GS FCBGA 908P G
GM@
SA000057F20



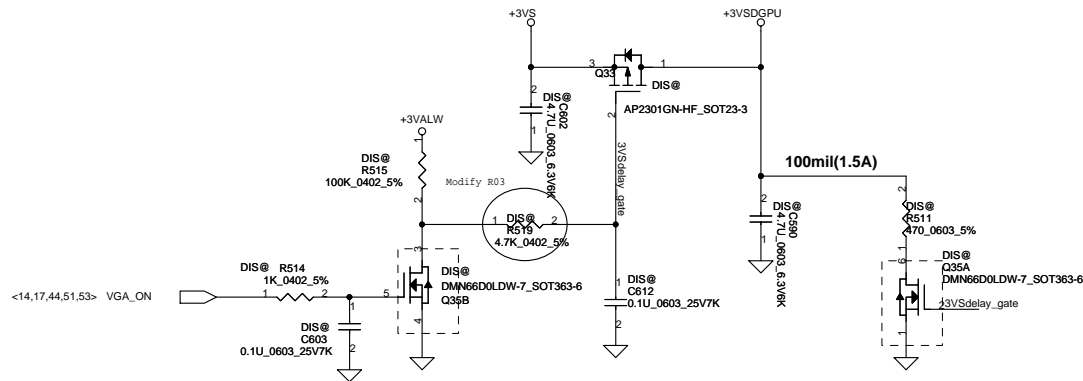
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				Custom	4019ID	
				B		
Date:	Friday, January 06, 2012			Sheet	22	of 60

VRAM Interface

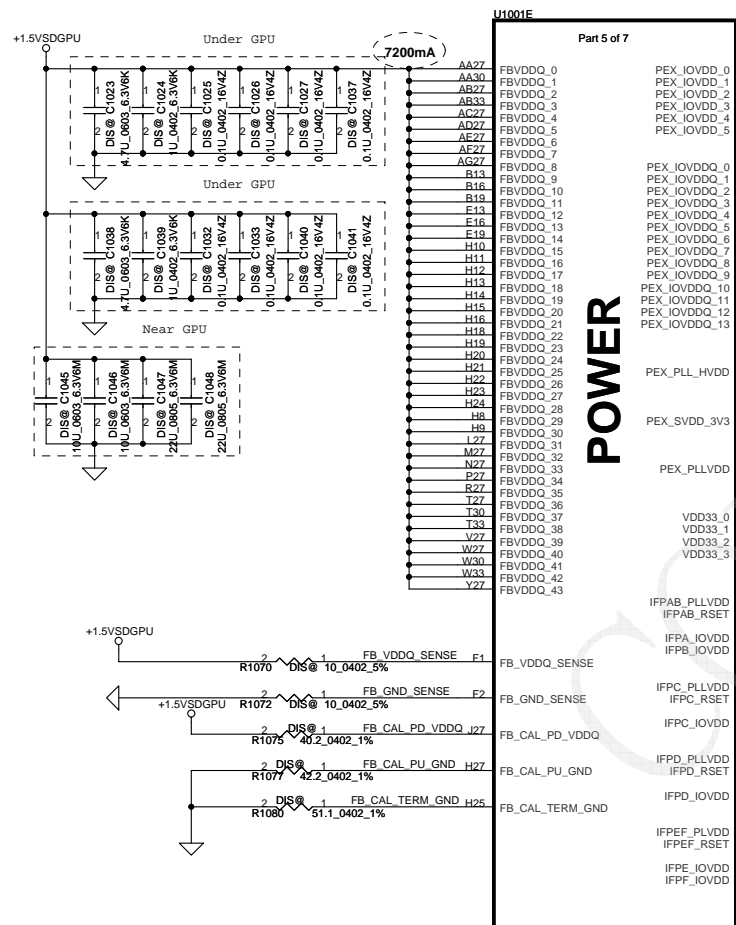


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+3VS to +3VSDGPU for GPU

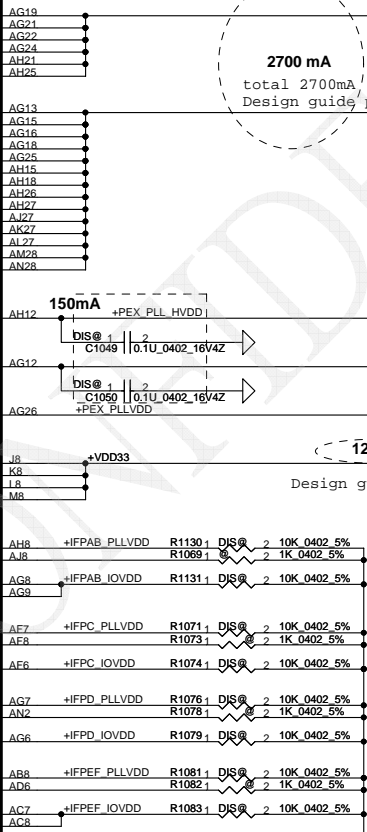


Design guide no define

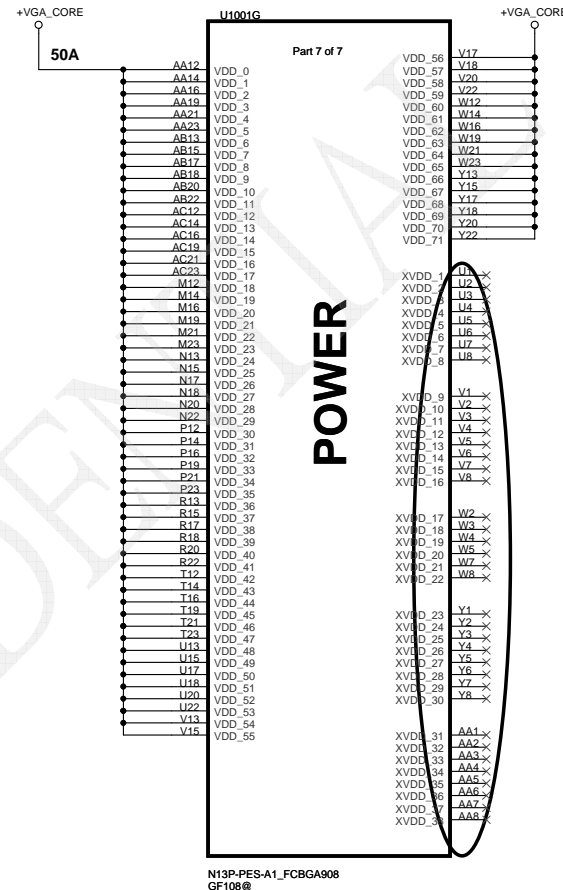
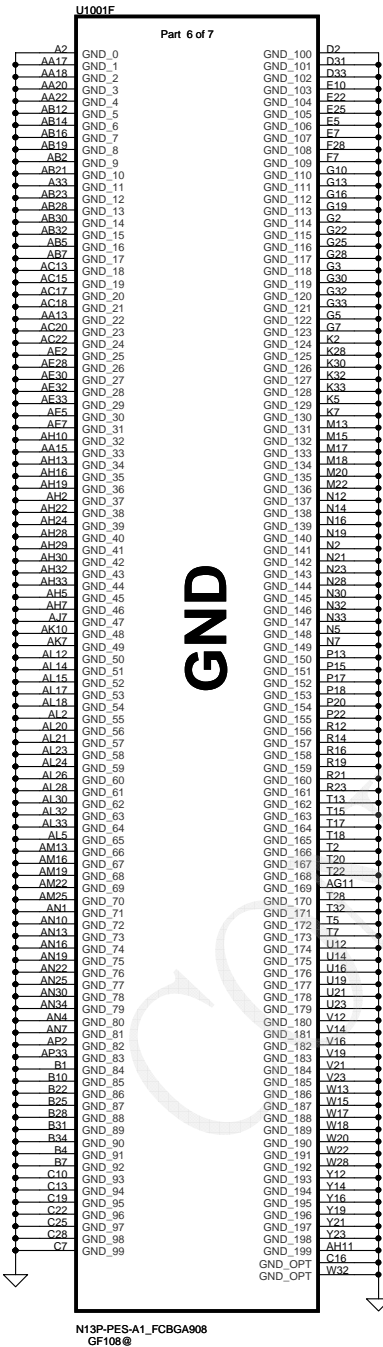


POWER

N13P-PPS-A1_FCBGA908
GF108@



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						Part Number		4019ID		Rev B	
						Document Number		4019ID			
						Customer					
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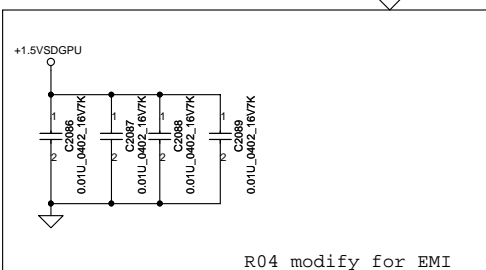
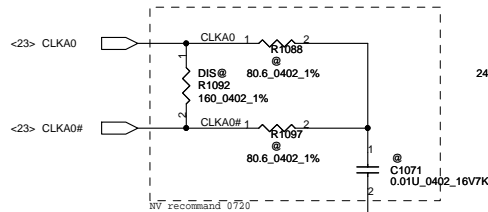
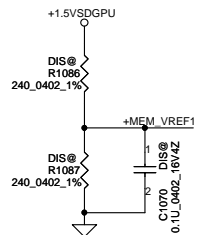
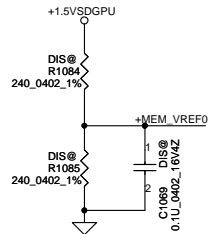


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										4019ID					
										Date:		Friday, January 06, 2012		Sheet 26 of 60	

VRAM DDR3 chips (1GB)

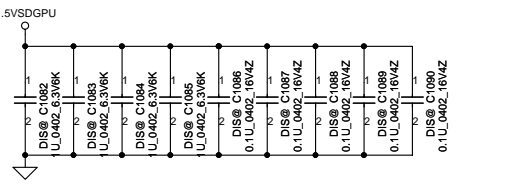
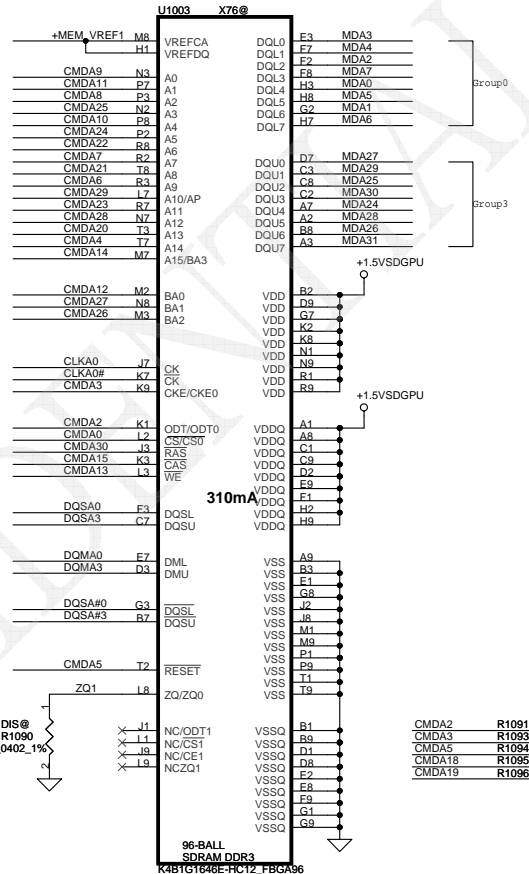
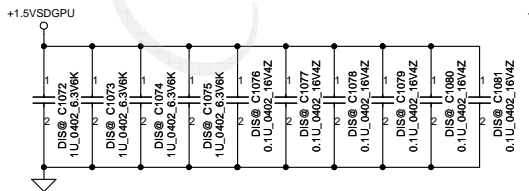
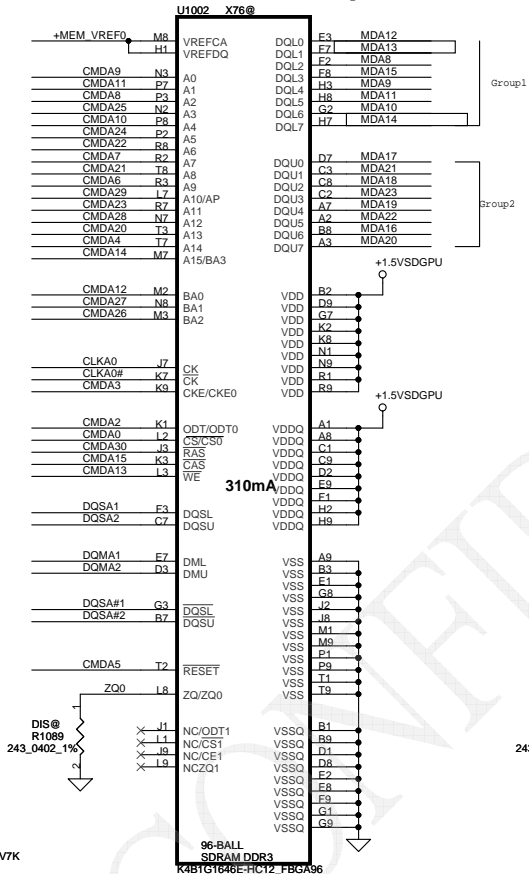
64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB

<23,28> DQSA[7..0] DQSA[7..0]
<23,28> DQSA#7..0 DQSA#7..0
<23,28> DQMA[7..0] DQMA[7..0]
<23,28> MDA[63..0] MDA[63..0]
<23,28> CMDA[30..0] CMDA[30..0]



R04 modify for EMI

R02 modify
Swap MDA13 and MDA14



CMDA2 R1091 DIS@ 2 10K 0402 5%
CMDA3 R1093 DIS@ 2 10K 0402 5%
CMDA5 R1094 DIS@ 2 10K 0402 5%
CMDA18 R1095 DIS@ 2 10K 0402 5%
CMDA19 R1096 DIS@ 2 10K 0402 5%

Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CAS*	No Termination

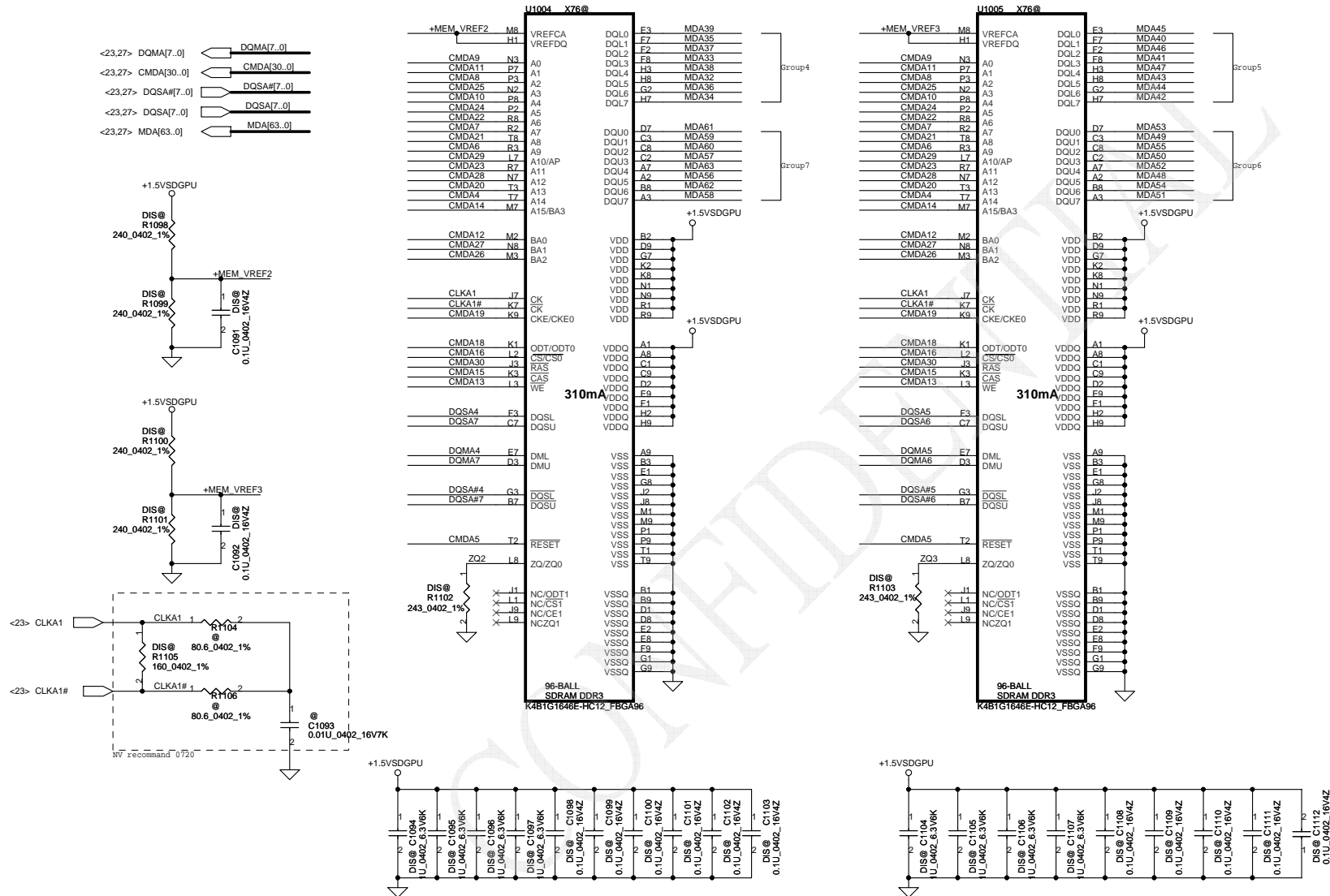
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		ODT_H
CMD18		CKE_H
CMD19		
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available	LOW	HIGH

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB



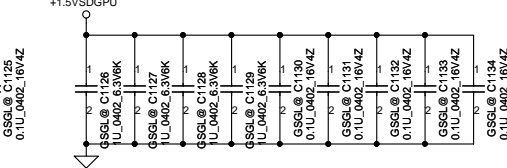
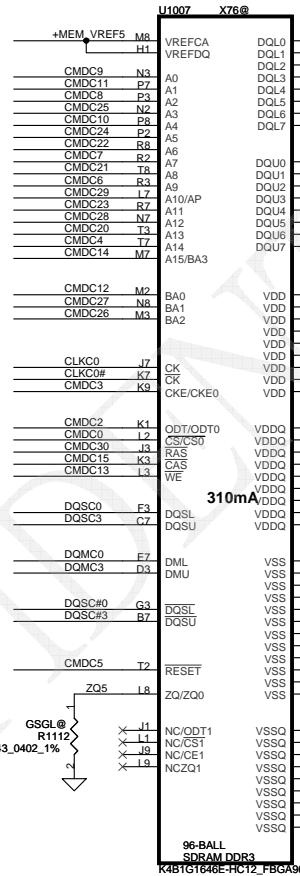
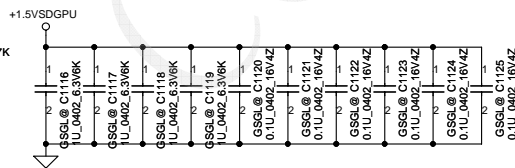
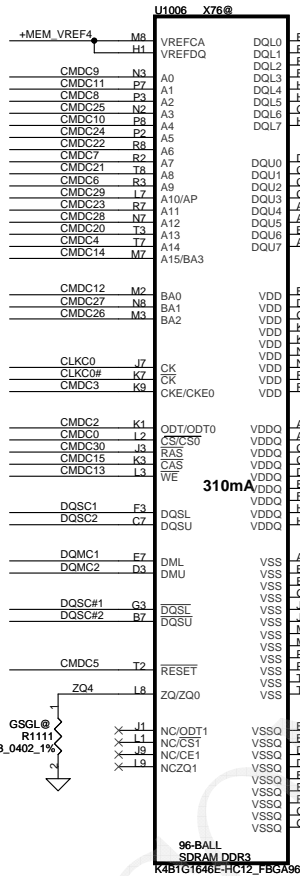
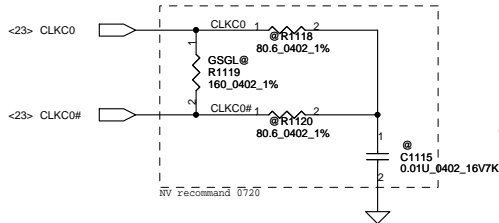
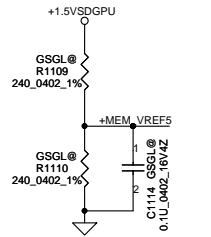
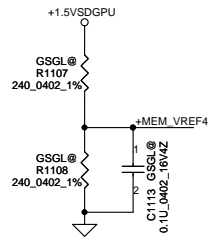
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
LOW		HIGH

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB

<23,30> DQSC[7..0] DQSC[7..0]
<23,30> DQSC# [7..0] DQSC# [7..0]
<23,30> DQMC[7..0] DQMC[7..0]
<23,30> MDC[63..0] MDC[63..0]
<23,30> CMDC[30..0] CMDC[30..0]



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CS*	No Termination

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Date		Rev
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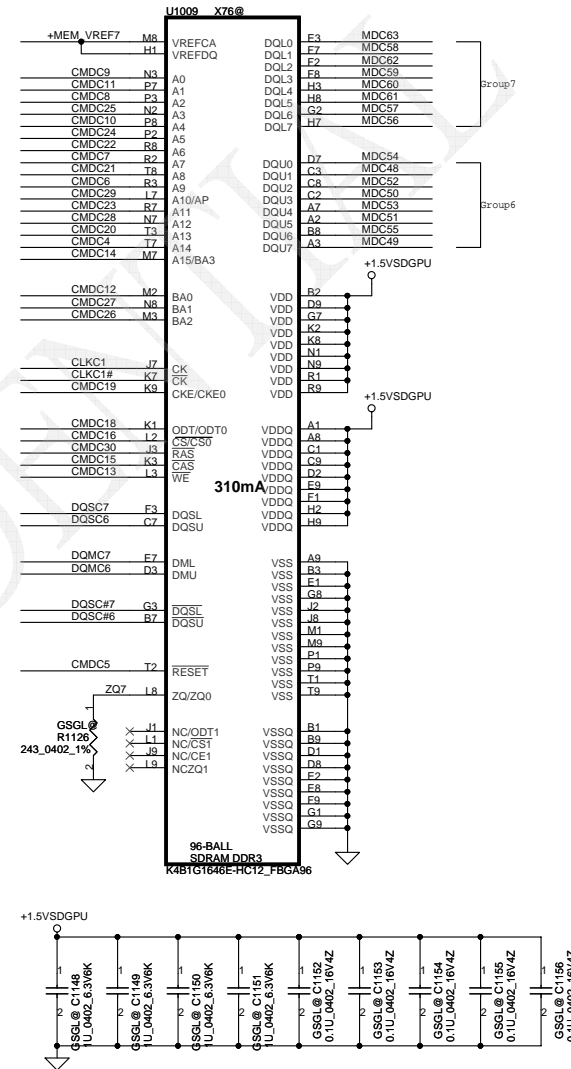
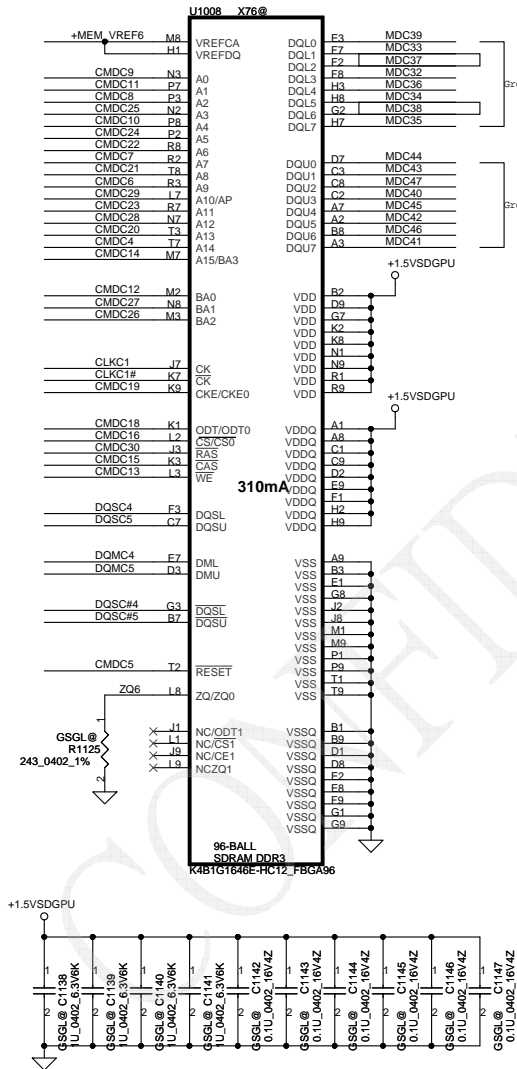
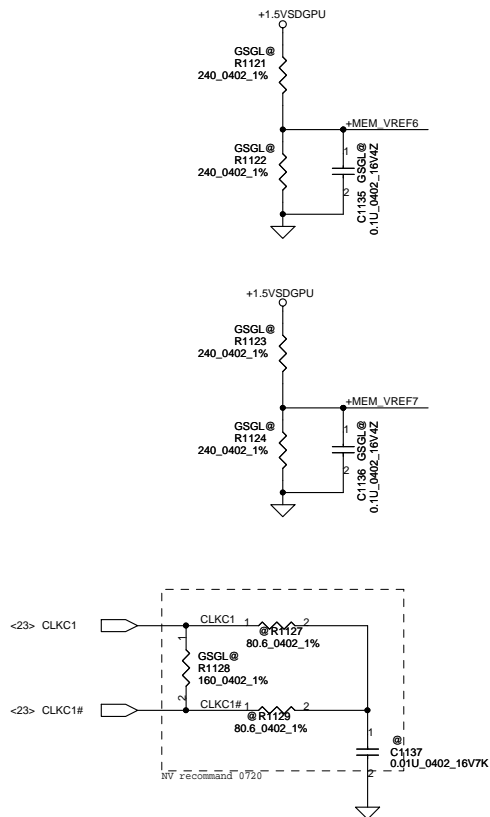
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB

<23,29> DQMC[7..0] ← DQMC[7..0]
<23,29> CMD[30..0] ← CMD[30..0]
<23,29> DQSC[7..0] ← DQSC[7..0]
<23,29> DQSC[7..0] ← DQSC[7..0]
<23,29> MDC[63..0] ← MDC[63..0]

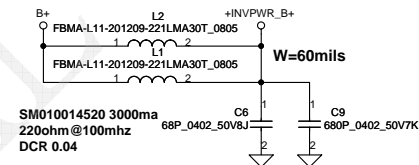
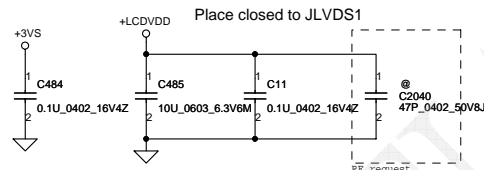
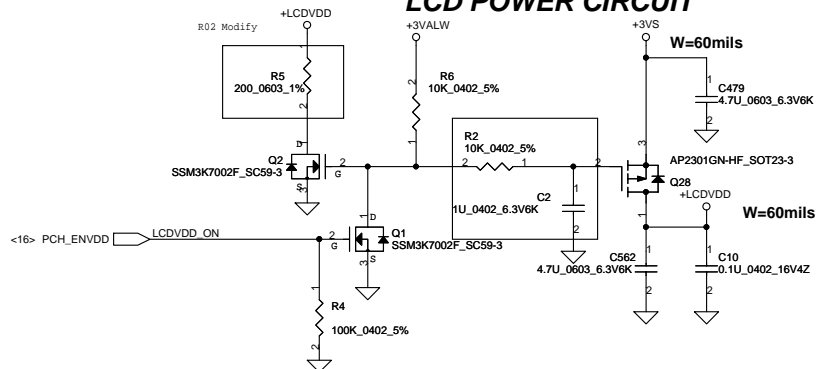
R02 modify
Swap MDC37 and MDC38



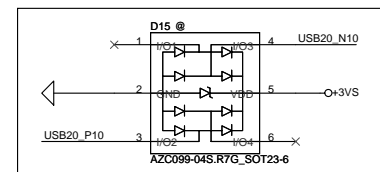
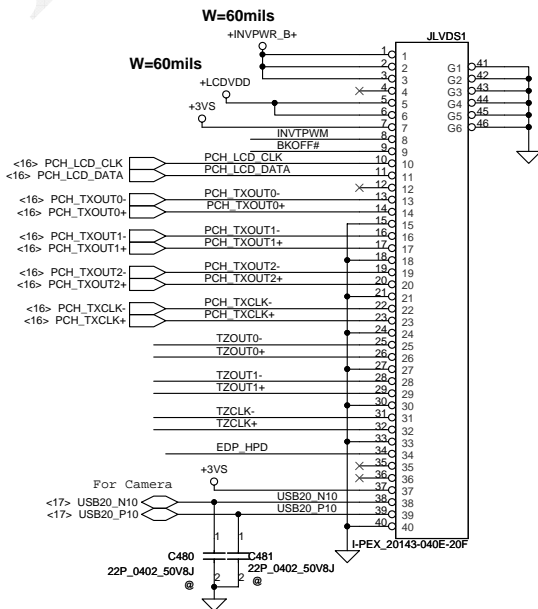
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

LCD POWER CIRCUIT

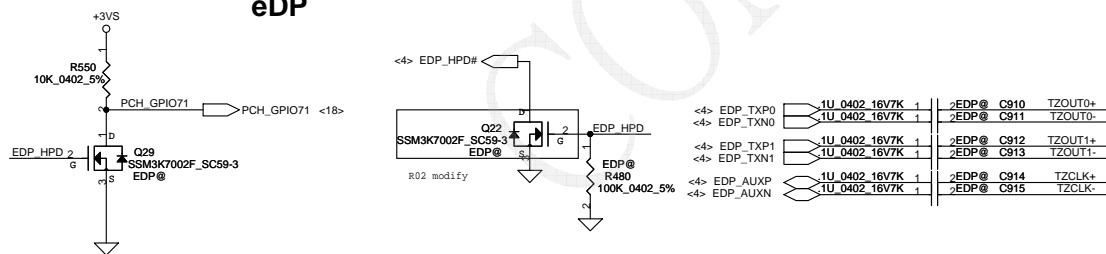


LCD/LED PANEL Conn.

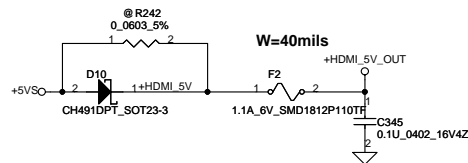


Modify R02

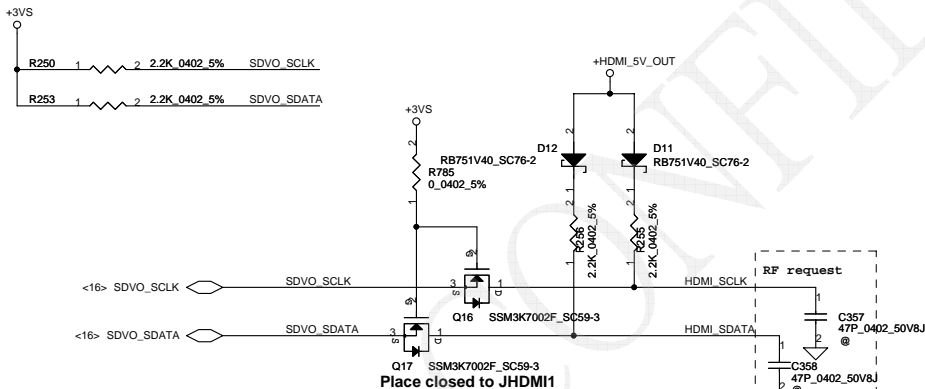
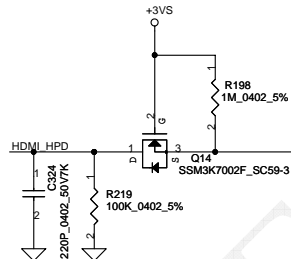
eDP



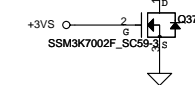
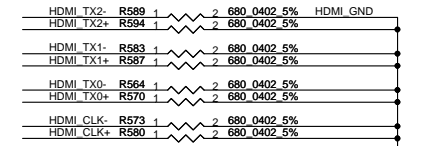
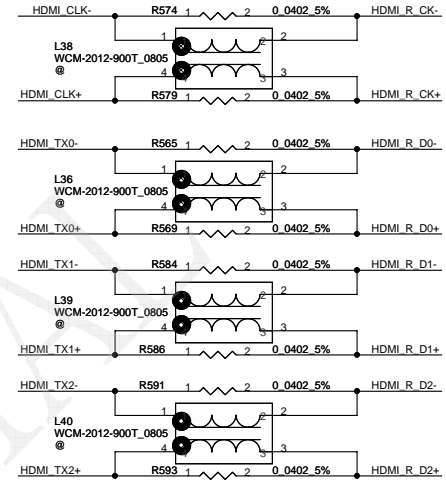
	GPIO71
	PCH_GPIO71
eDP	0
LVDS	1



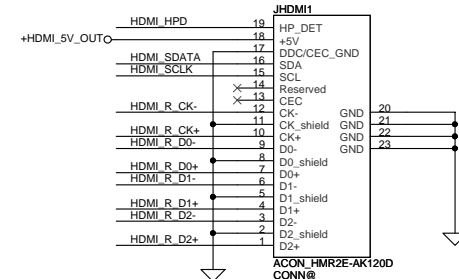
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<16> PCH_DPB_P0	C281	2	1	.1U_0402_16V7K	HDMI TX2+
<16> PCH_DPB_N1	C283	2	1	.1U_0402_16V7K	HDMI TX1-
<16> PCH_DPB_P1	C282	2	1	.1U_0402_16V7K	HDMI TX1+
<16> PCH_DPB_N2	C287	2	1	.1U_0402_16V7K	HDMI TX0-
<16> PCH_DPB_P2	C286	2	1	.1U_0402_16V7K	HDMI TX0+
<16> PCH_DPB_N3	C285	2	1	.1U_0402_16V7K	HDMI CLK-
<16> PCH_DPB_P3	C284	2	1	.1U_0402_16V7K	HDMI CLK+



SM070001310 400ma 90ohm@100mhz DCR 0.3



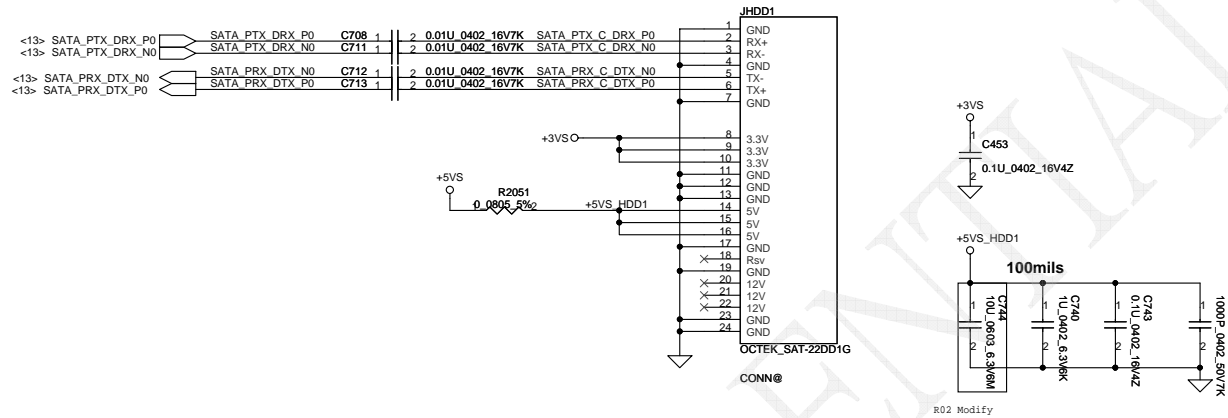
HDMI connector



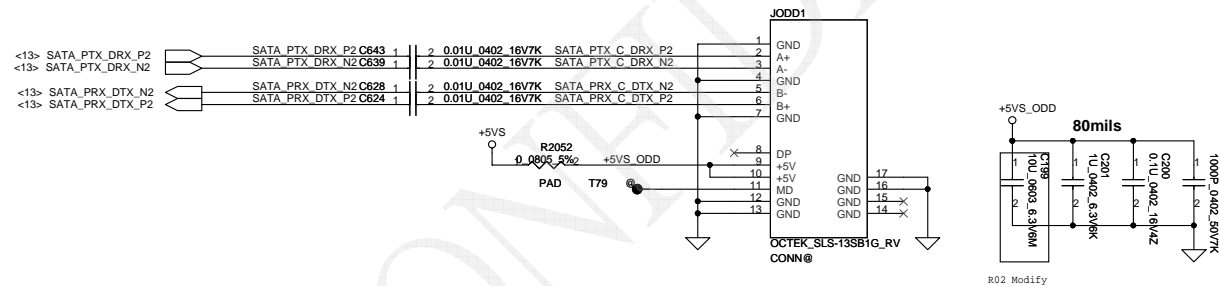
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SATA HDD1 Conn.

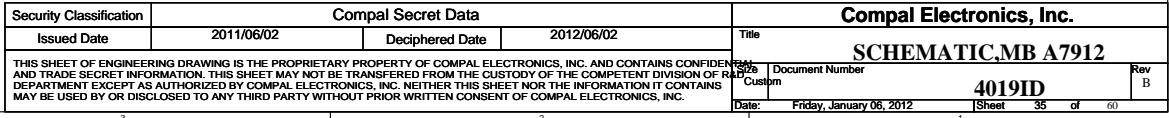
CL 4.0 mm

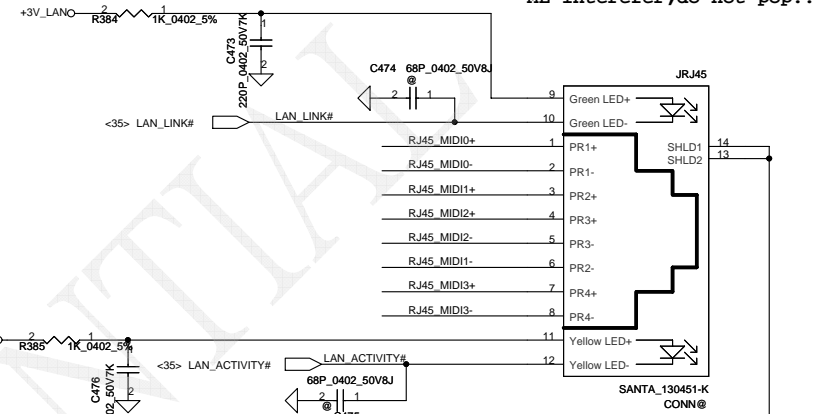


SATA ODD Conn.

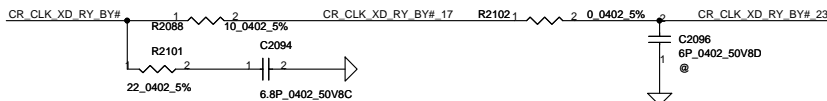
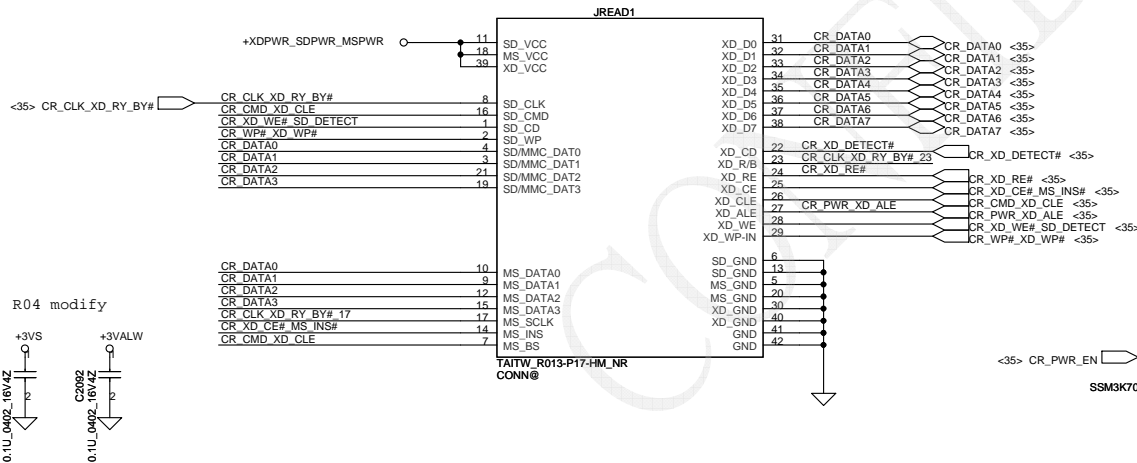


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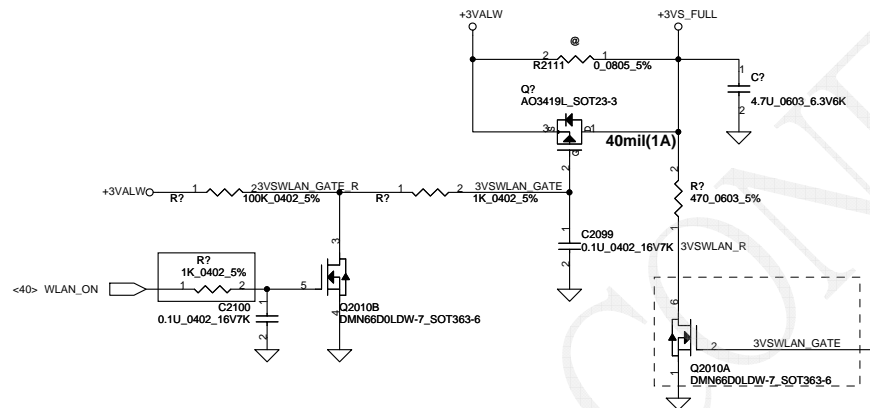
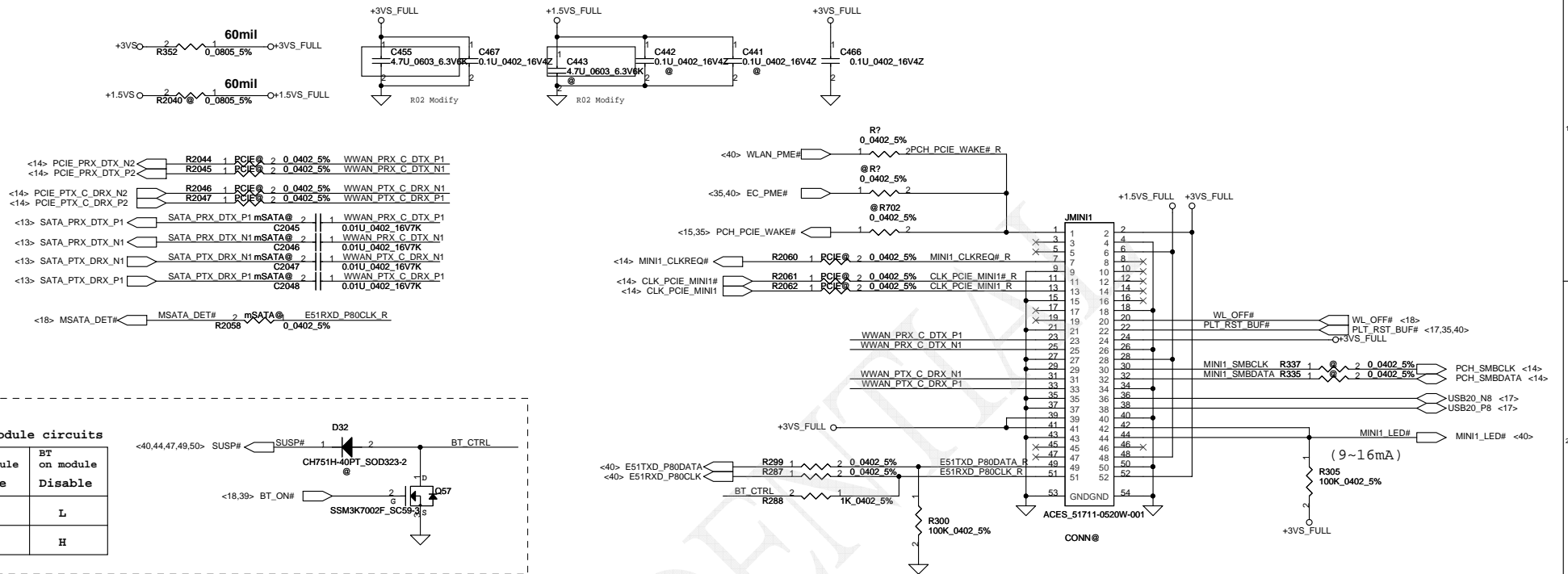


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For Wireless LAN or MSATA



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Deciphered Date				2012/06/02				Schematic, MB A7912			
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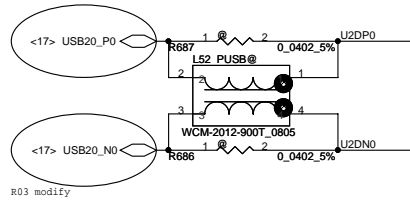
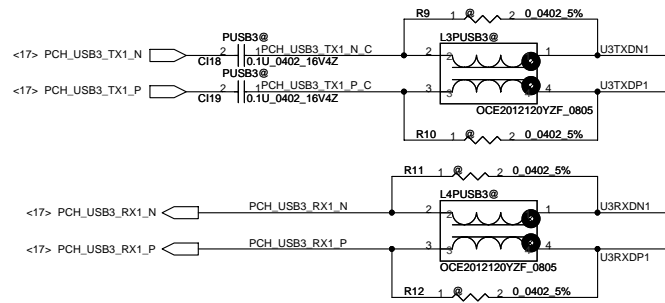
CONFIDENTIAL

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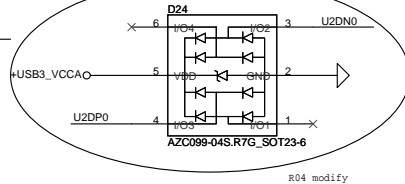
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For USB2.0 ESD request

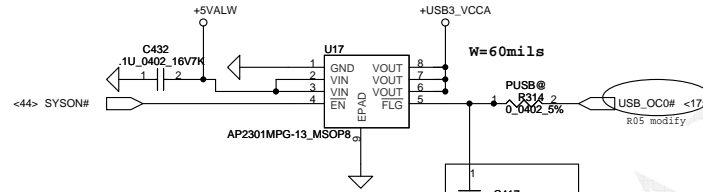
Deafult use PCH side USB3.0 signal



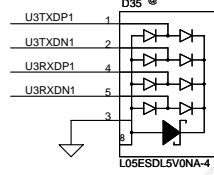
For USB2.0 ESD request



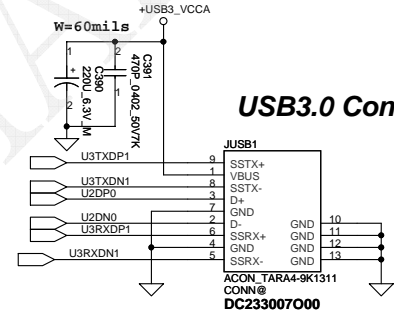
R04 modify



For ESD request



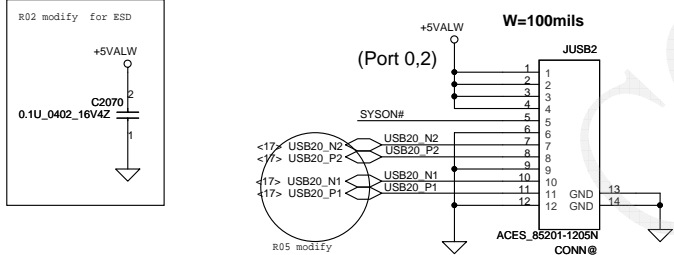
U3TXDP1
U3TXDN1
U2DP0
U2DN0
U3RXDP1
U3RXDN1



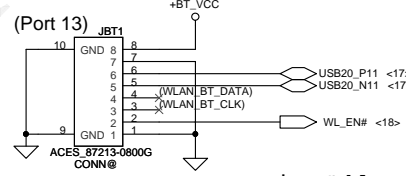
USB3.0 Conn.

USB/B Conn.

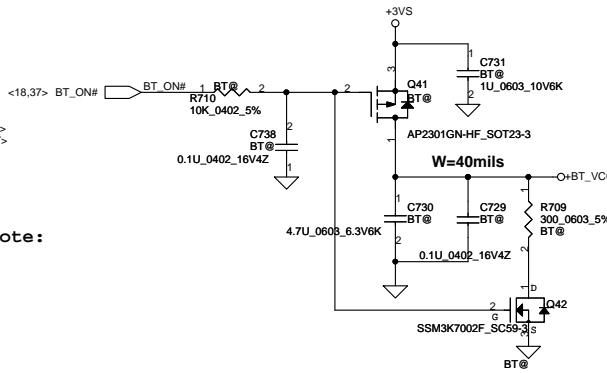
BT Conn.



R05 modify



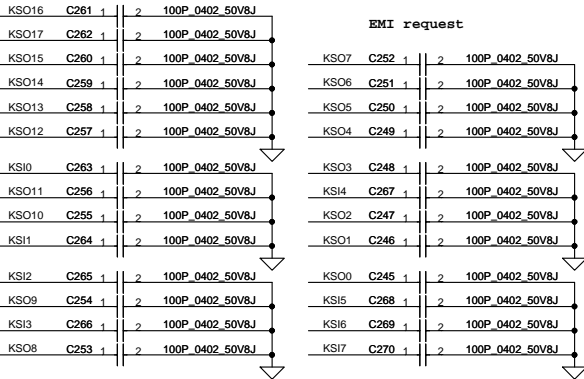
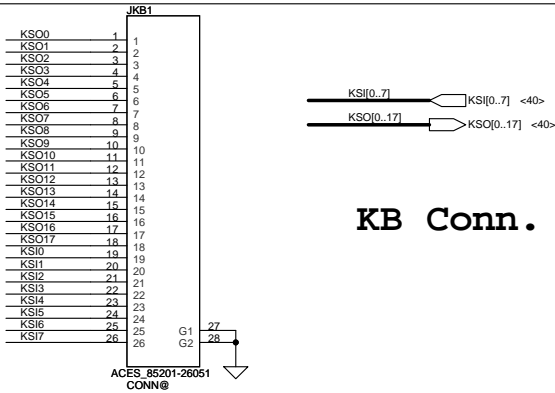
BT Wire Cable Note:
Pin 3, Pin 4 NC



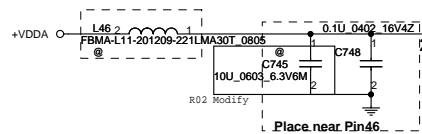
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Deciphered Date				2012/06/02				Schematic, MB A7912			
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ON/OFF BTN

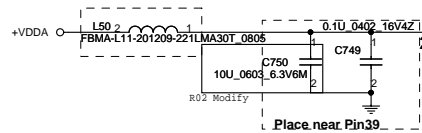
Test Only
Bottom Side



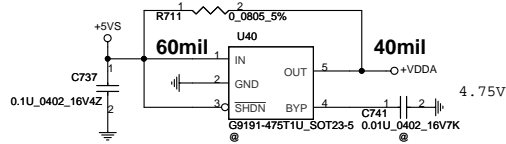
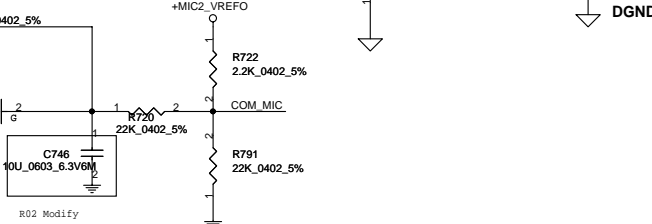
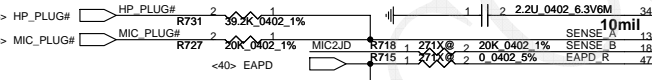
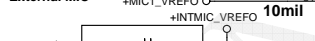
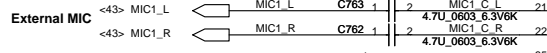
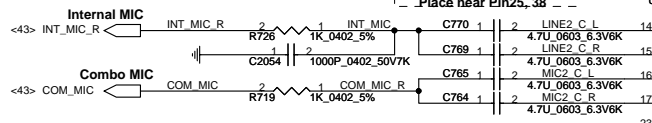
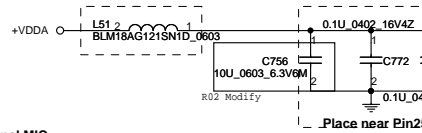
SM010014520 3000ma 220ohm@100mhz DCR 0.04



SM010014520 3000ma 220ohm@100mhz DCR 0.04

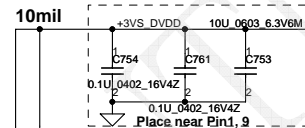


SM010030010 200ma 120ohm@100mhz DCR 0.2

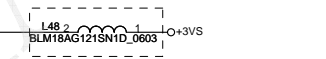


(output = 300 mA)

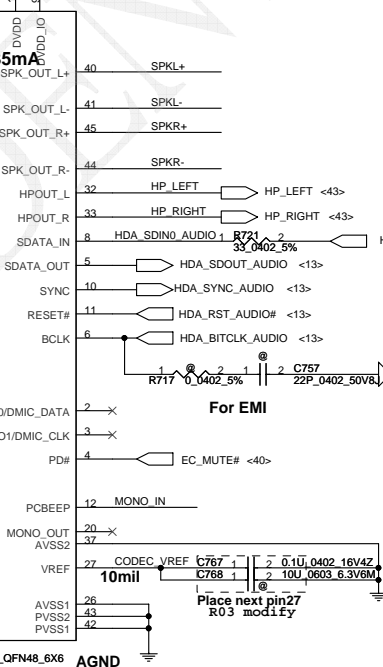
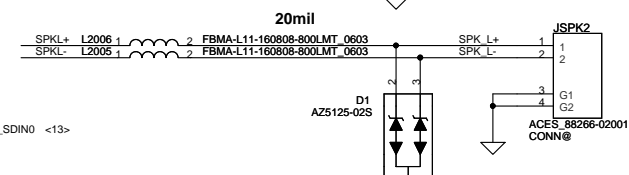
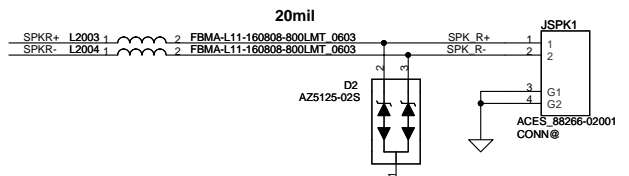
HD Audio Codec



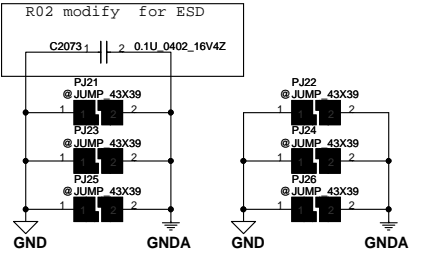
SM010030010 200ma 120ohm@100mhz DCR 0.2



Int. Speaker Conn.



For EMI



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Singatron 2SJ2326
DC021007151

Headphone Out

SINGA_2SJ2326-001111
CONN@

MIC JACK

SINGA_2SJ-A960-C01
CONN@

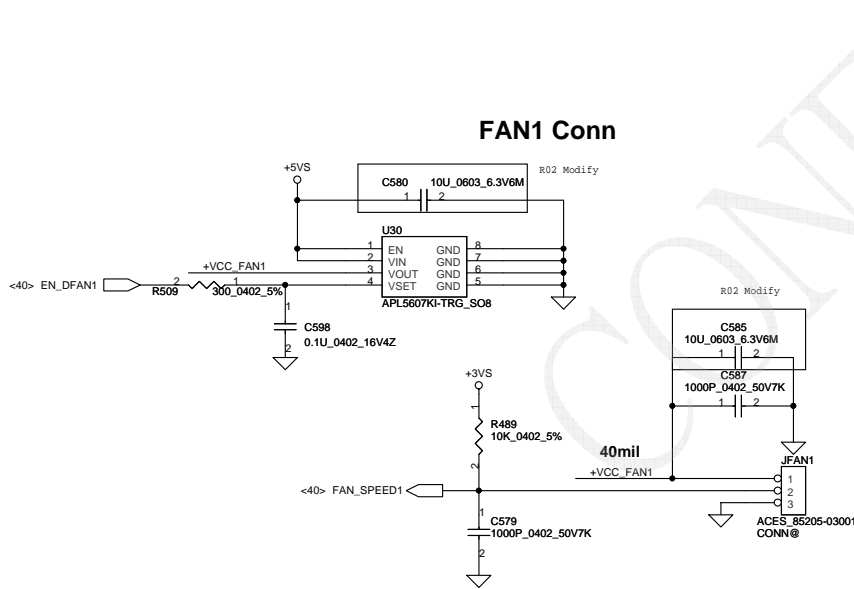
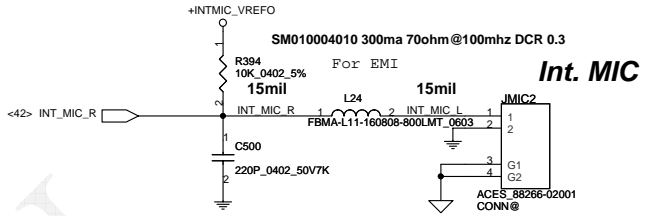
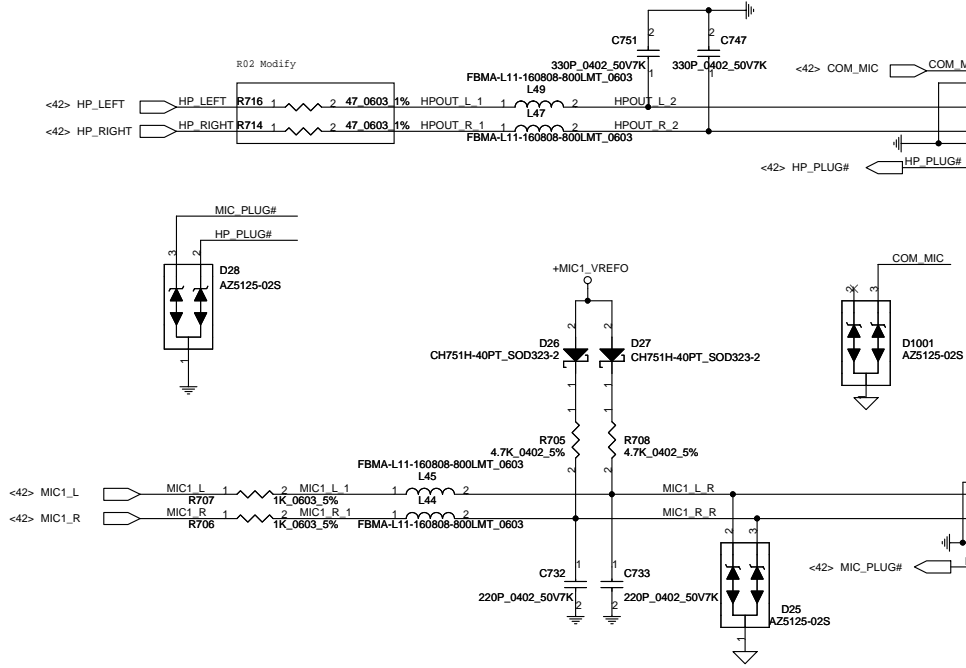
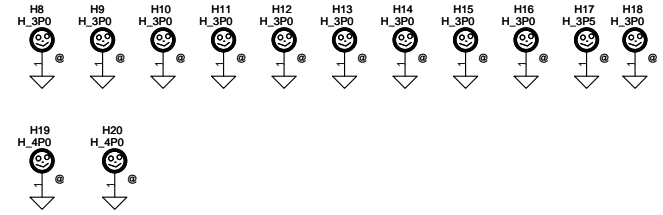
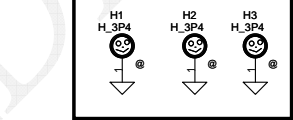
Int. MIC

ACES_88266-02001
CONN@

FAN Stand-Off

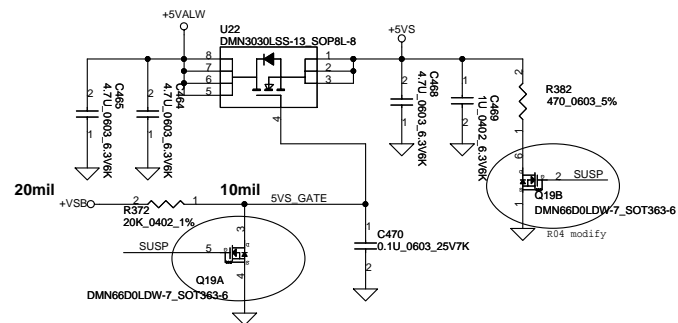
JUSB3 Stand-Off

FAN1 Conn

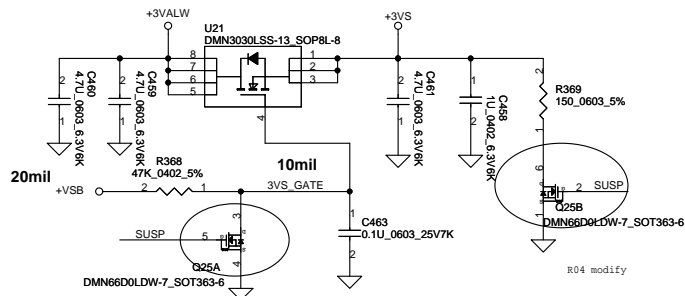


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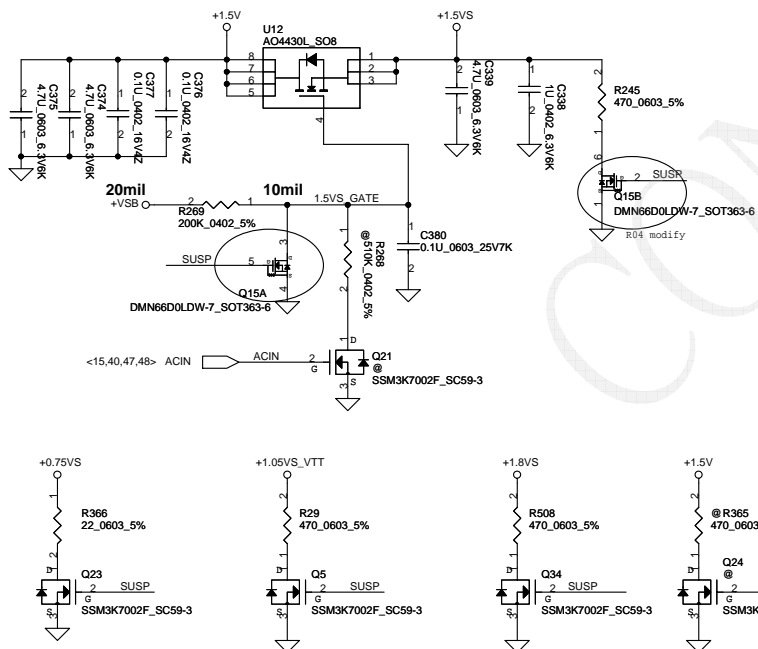
+5VALW TO +5VS



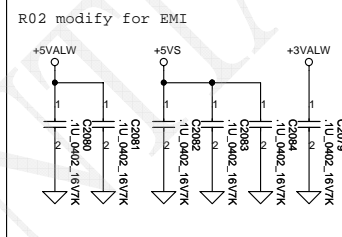
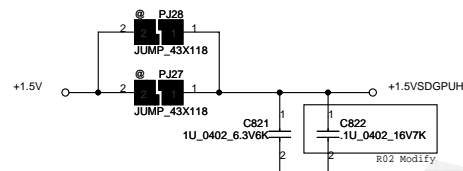
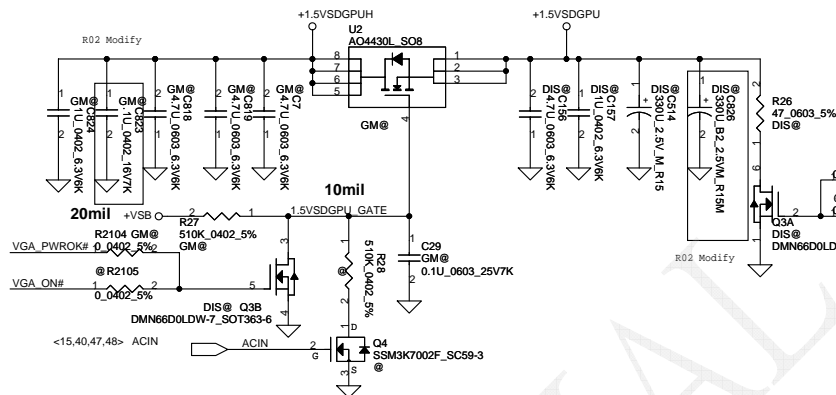
+3VALW TO +3VS



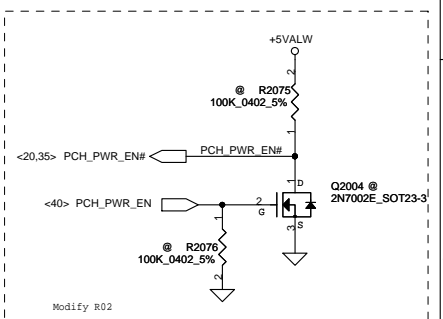
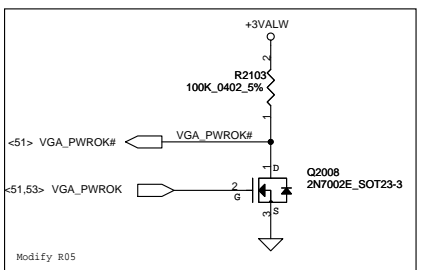
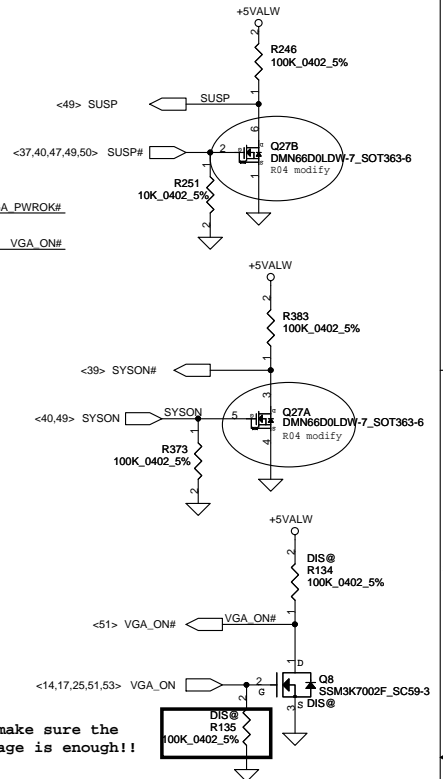
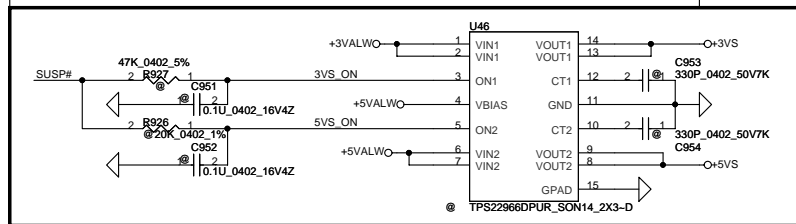
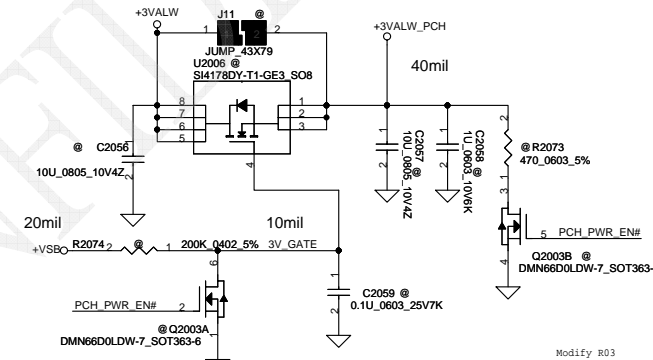
+1.5V to +1.5VS



+1.5VSDGPUH to +1.5VSDGPU for GPU

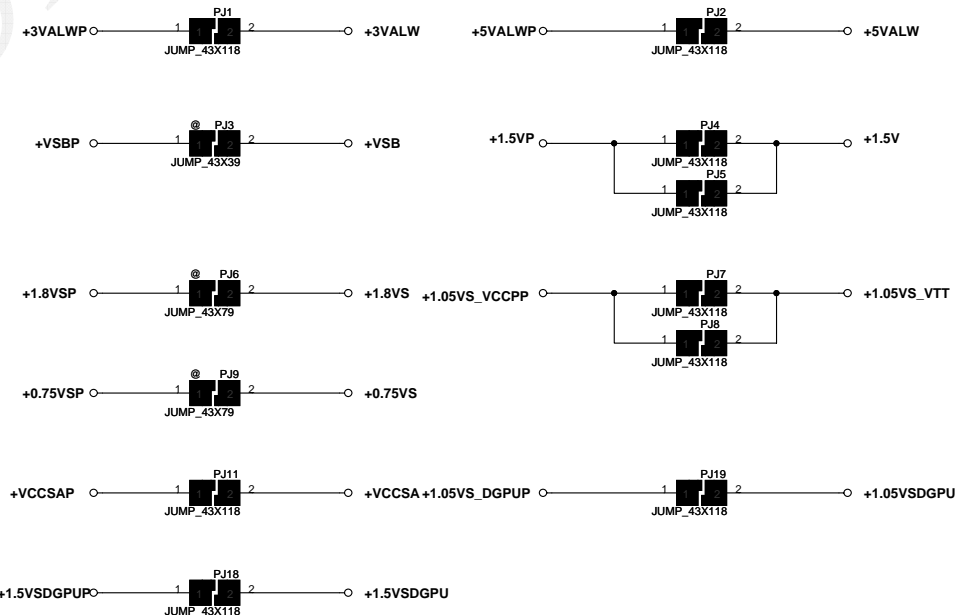
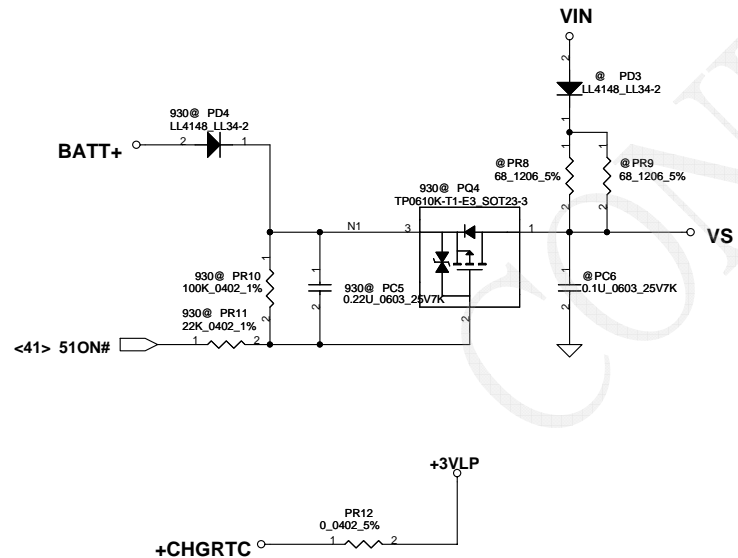
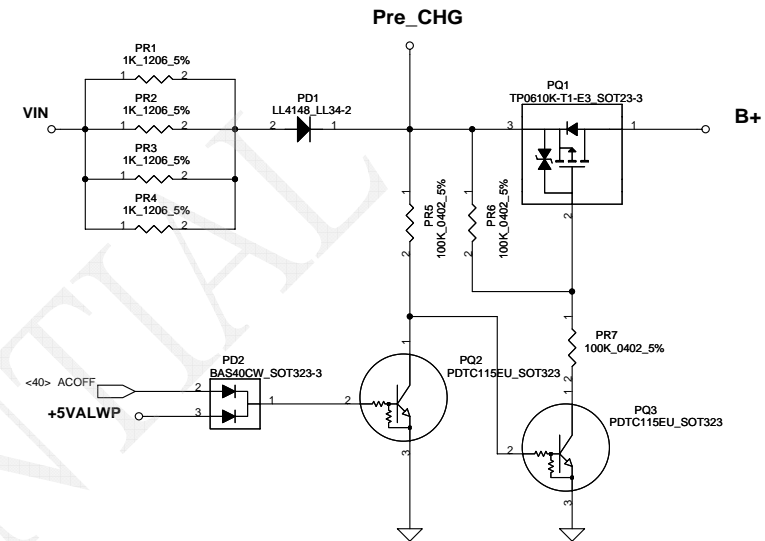
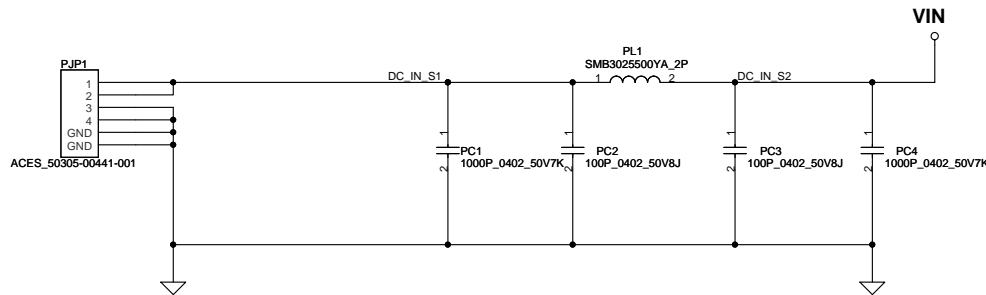


+3VALW TO +3VALW(PCH AUX Power)

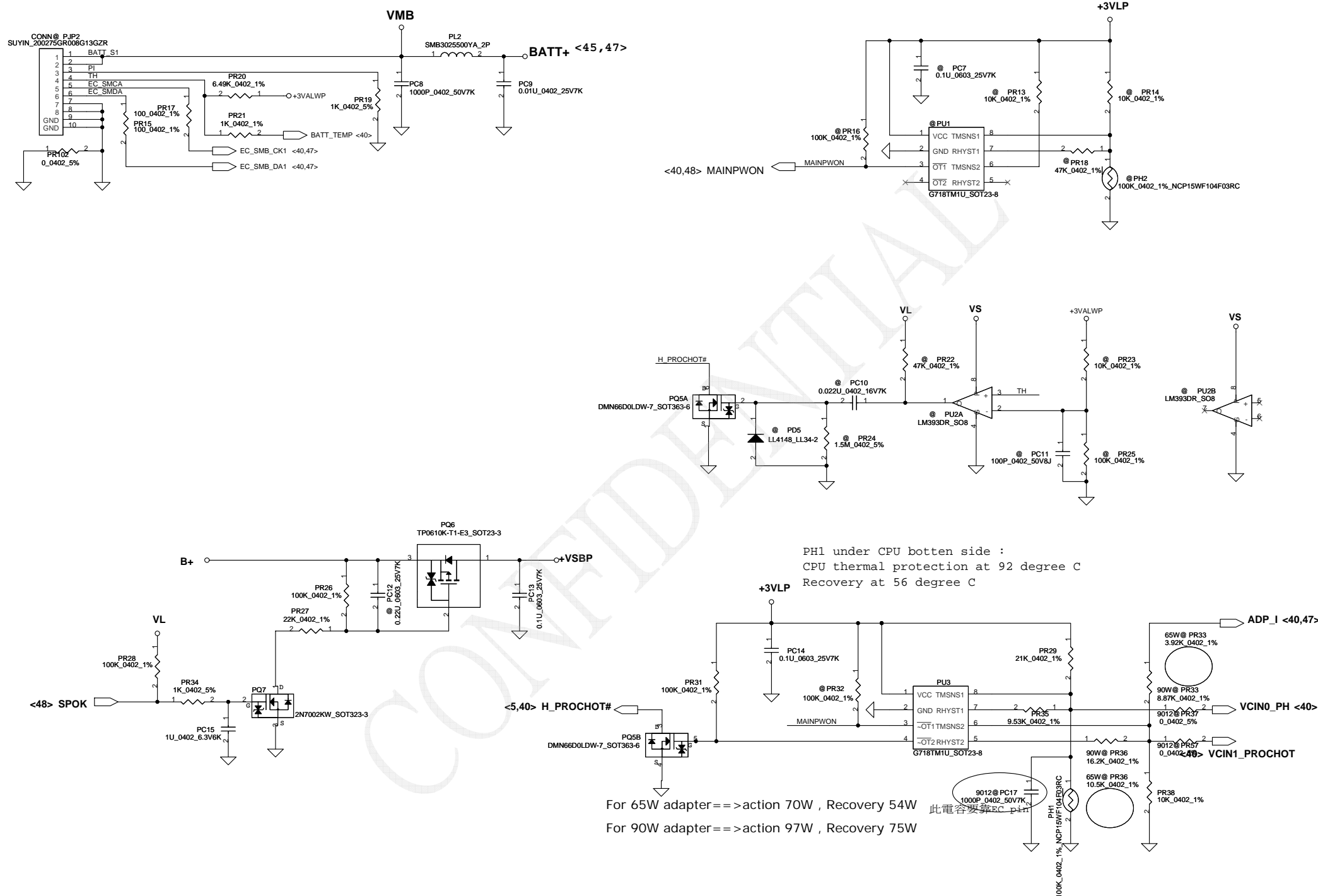


Reserved

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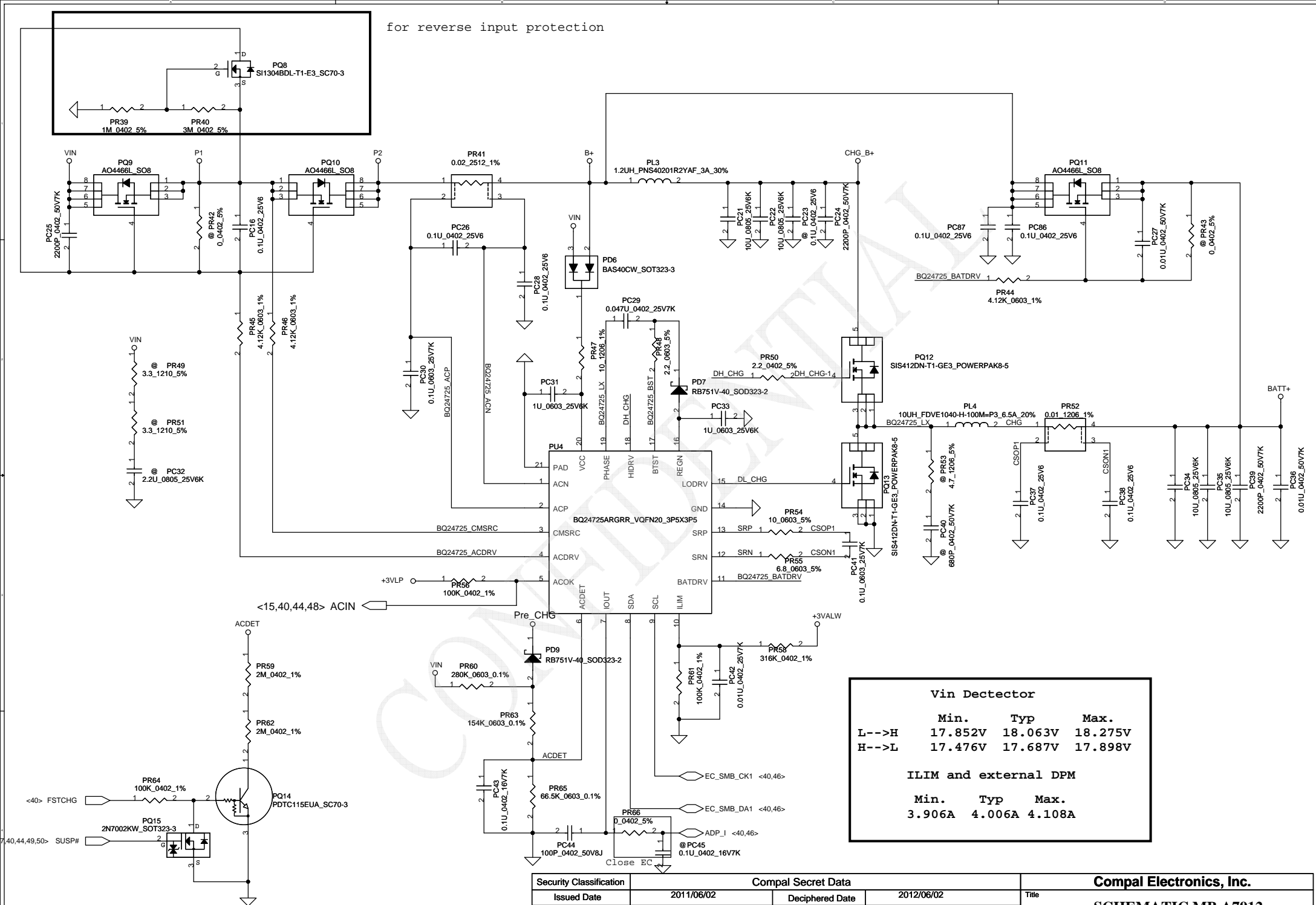


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for reverse input protection



Vin Detector

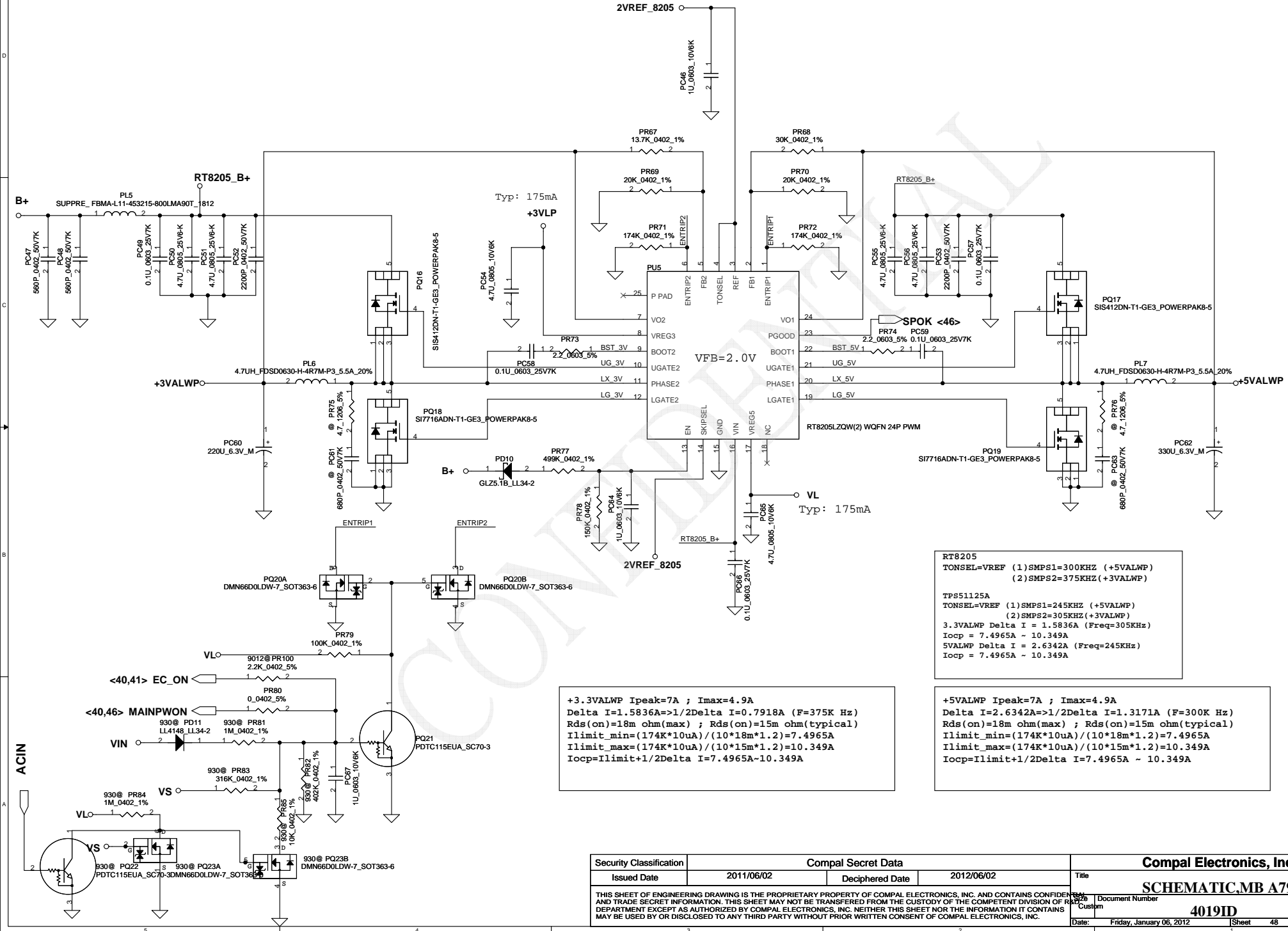
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L-->H	17.852V	18.063V	18.275V
H-->L	17.476V	17.687V	17.898V

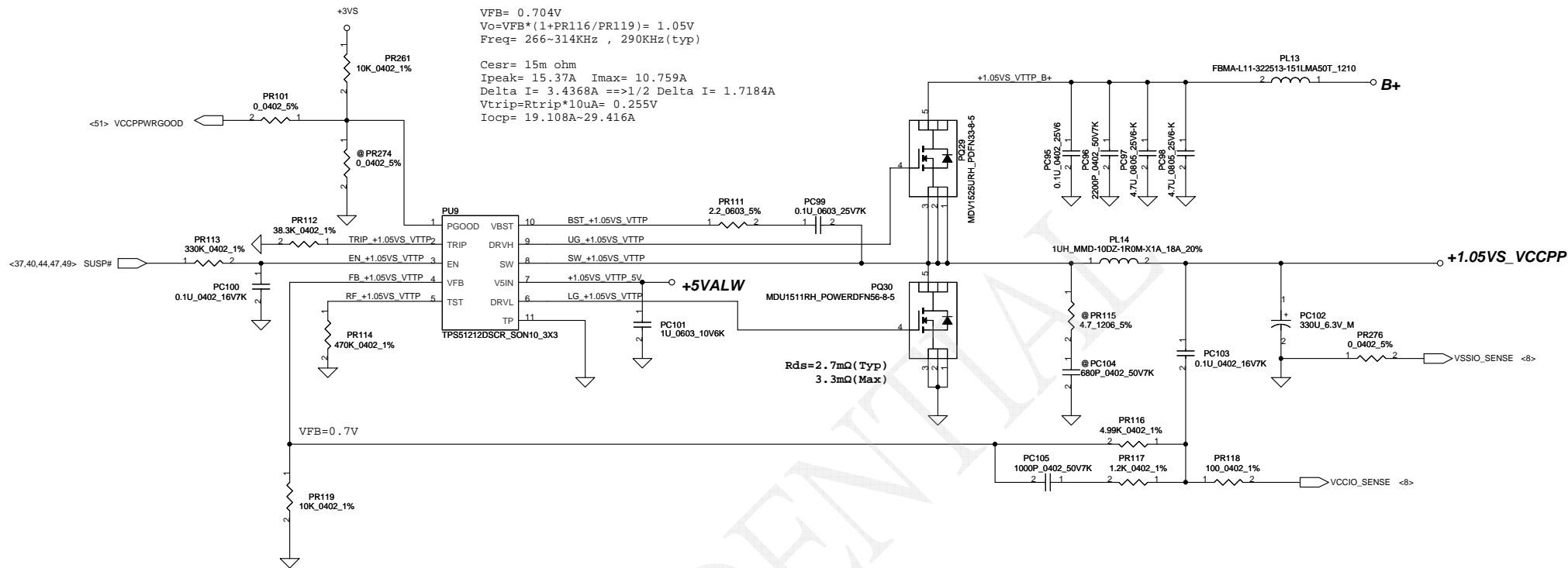
ILIM and external DPM

	Min.	Typ	Max.
	3.906A	4.006A	4.108A

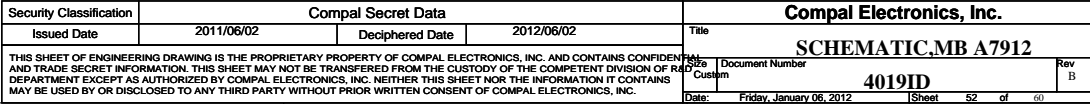
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Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO

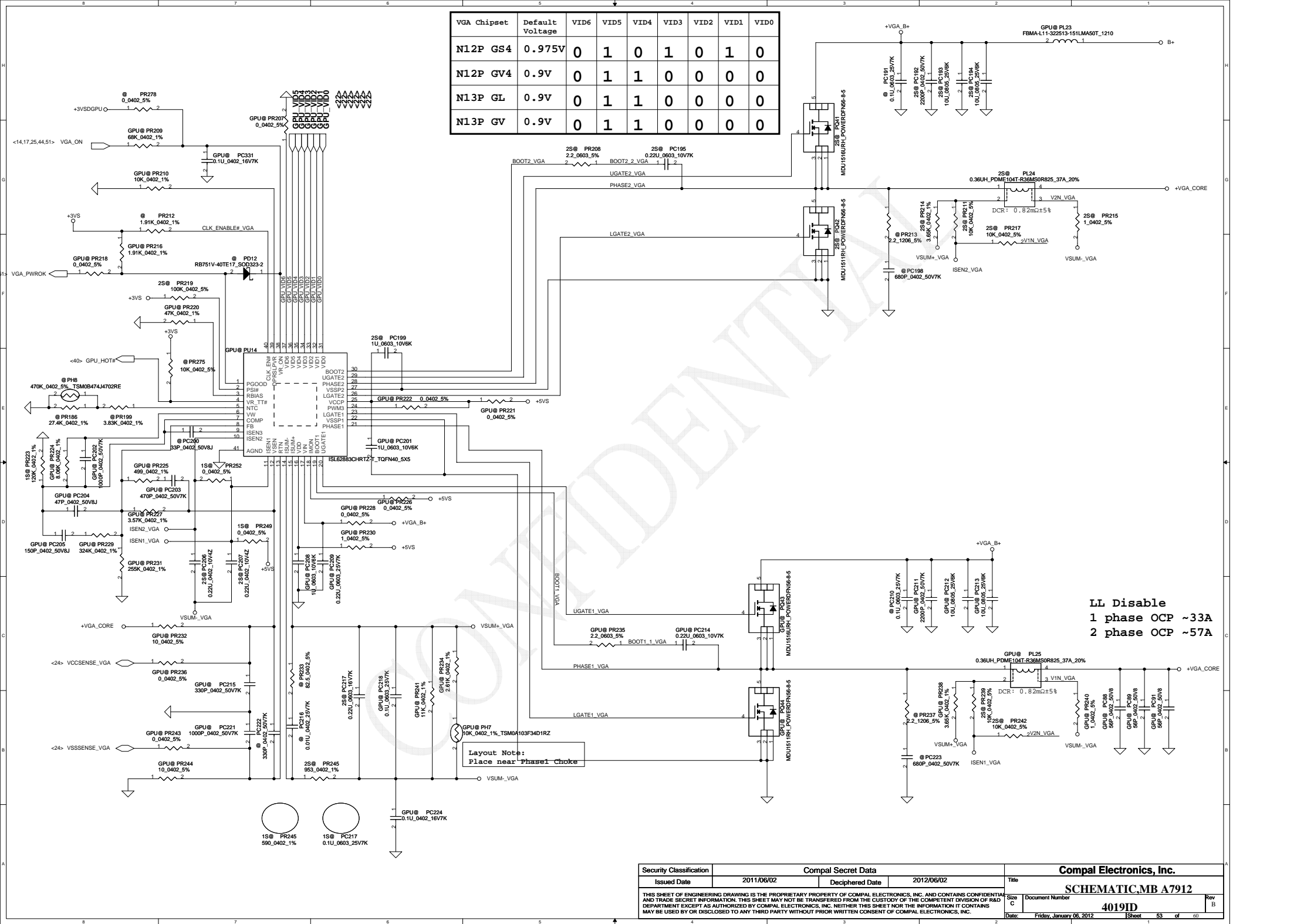




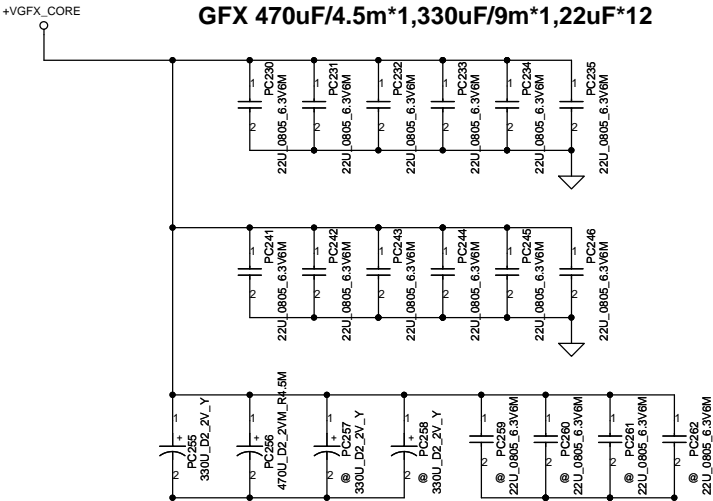
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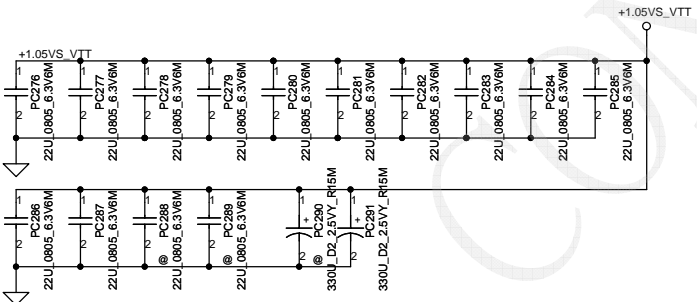


PWR Rule
CPU 330uF/9m *5,22uF *16,10uF*10
GFX 470uF/4.5m*1,330uF/9m*1,22uF*12

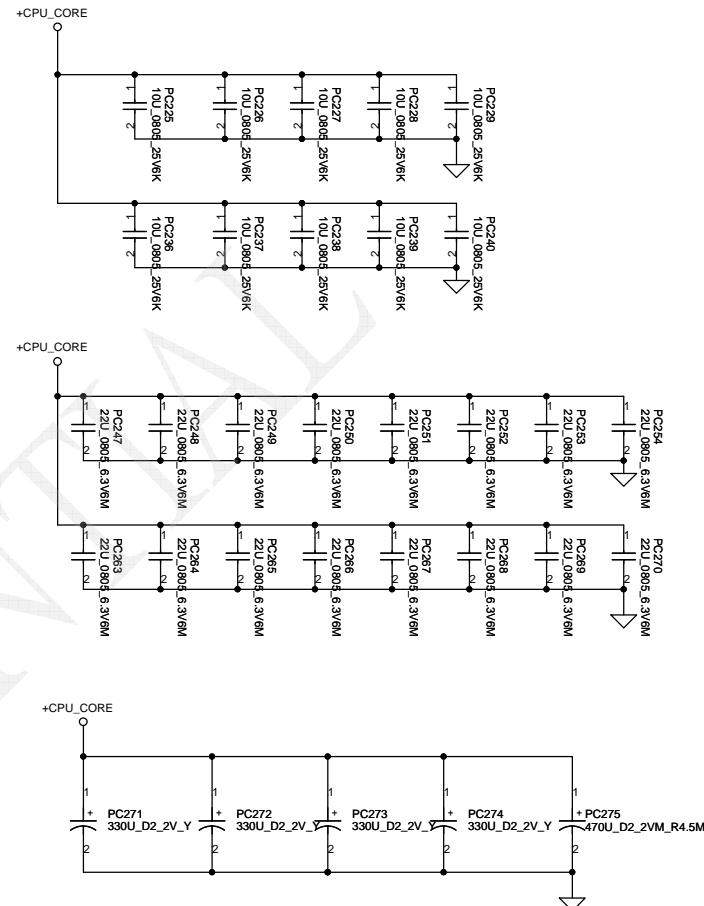


Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed



INTEL Recommend
3*330uF(1 in other page),12*22uF, 5 no stuff
from PDDG 1.0



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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	S3 sequence @ DC	Meet Intel sequence SPEC		49	Change RP91 to 267K	2011 1208	DVT
2	1.5VSDGPU lose	Improve FB pin anit-noise		51	Change RP248 to 2K, PR255 to 1.74K, PR253 to 137K	2011 1208	DVT
3	Cut-in SMT memo			52	Add PC182, PC184	2011 1208	DVT
4		Standard design			Change PR138, PR150, PR178, PR194, RP205 , PR235 to 2.2		
5	Vth has risk			51	Change PU16 from G971 to APL5930	2011 1212	DVT
6		Enable select		51	Add PR266	2011 1217	DVT
7	Cut-in EMI solution			53	Add PC88, PC89, PC91	2011 1221	DVT
8							
9							
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11							
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
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2							
3							
4							
5							
6							
7							
8							
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1	P.40.13		9/7	EC	Change th HDA_SDO to ME_EN		0.2
2	P.40		9/7	HW	Add R2085 ,change the EC_ACIN pull high to +3VLP		0.2
3	P.37		9/7	HW	Add f11009 USB3.0 TX coupling capacitor (c2060,c2061)		0.2
4	P.38.39.40		9/7	HW	Add USB chargeaer schematic(C2060.C2061.R2077~R2084,R2065~R2072)		0.2
5	P.22.40		9/7	HW	Follow ABO request,add ADPS function(Q2005),R2086.R2087)		0.2
6	P.20		9/7	HW	Add +5VALW TO +5VALW_PCH schematic(Q2006.C2062.R2088)		0.2
7	P.44		9/7	HW	Add +3VALW TO +3VALW_PCH schematic(U2006,R2073~R2076,C2056~C2059,Q2003,Q2004)		0.2
8	P.43		9/7	HW	For FSOV spec,Chang R714,R716 from 75ohm to 47ohm.		0.2
9	P.13		9/7	HW	For WIN8,Change R681.R651.R684.R652 to 33ohm		0.2
10	P.44		9/7	HW	Delete C817,Change C826 from D2 size to B2 size		0.2
11	P.17.37		9/7	HW	Follow chief river common design, please chang Mini-Card 2(port 11) to port 9		0.2
12	P.38		9/7	HW	Delete +1.5V to +1.05V_V128 Transfer(U2002.R2002.R2003.R2005.C2002.C2003.C2005.R2008)		0.2
13	P.38		9/7	HW	Delete USB3.0 EEPROM(U2004.R2035.R2034.C2039)		0.2
14	P.37		9/7	HW	Reserve Mini-Card 2		0.2
15	P.19		9/7	HW	F2 flick issue on projector P5202 D-sub Add C2063.C2064		0.2
16	P.22.40		9/8	HW	Change VGA GPIO12 of dGPU connection to EC controlled for the power limited usage Add EC pin 107-->GPU ACIN		0.2
17	P41		9/14	HW	Add SW5.SW6 for EG project.		0.2
18	P27.30		9/14	HW	Swap MDC37 and MDC38 Swap MDA13 and MDA14		0.2
19	P06.11.17.35. P39.40.42		9/14	HW	For ESD request Add C2065~C2075		0.2
20	P16		9/16	HW	For HDMI PCH_DPB_HPD noise Add C2076		0.2
21	P31		9/16	HW	For LVDS power sequence Change R5 from 300 to 200 ohm Change R2 from 1k to 10k ohm change C2 from 0.047uF to 1uF		0.2
22	P18		9/16	HW	Delete PCH test ponit(T31~T46,T49~T61,T63~T65)		0.2
23	P21,40		9/19	HW	Change Q22,Q26 from SB000008J10 to SB000009080		0.2
24	P14,22,35,38		9/19	HW	For Crystal Change Y2 ,Y4 from SJ10000DJ00 to SJ10000E800 Change Y1000 from SJ10000DK00 to SJ100009700 Change C630,C631,C2019,C2028,C1008,C1009 to 10pF Change C681,C679 to 15pF		0.2

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25	P.44		9/20	EMI	For EMI request (Add C2079~C2084)		0.2
26	P.36		9/20	HW	For SD3.0 issue (Add R2088,R2089)		0.2
27	P.20		10/17	HW	Add +5VALW TO +5VALW_PCH schematic(Q2006.C2062.R2090)		0.3
28	P.44		10/17	HW	Add +3VALW TO +3VALW_PCH schematic(U2006,R2073~R2076,C2056~C2059,Q2003,Q2004)		0.3
29	P.40		10/17	HW	Board ID error. Add R353.		0.3
30	P.40		10/17	HW	Board ID 0.3. Change R353 to 18K		0.3
31	P.17,39		10/17	HW	Follow Intel's suggestion; Change USB3.0 from port 2 to port 1 Change USB2.0 from port 0,1 to port 2,9		0.3
32	P.18		10/18	HW	Support eDP GPIO71-->0 (eDP) GPIO71-->1 (LVDS)		0.3
33	P.13.40		10/25	HW	Co_lay NPCE885N Delete U38,C722,R690,R695,C727 Add C2085,R2091~R2096		0.3

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43	P.41		11/16	ME		Delete SW5,SW6, Pop SW2,SW3	0.4
44	P.05		11/16	HW	BUF_CPU_RST# noise	Add C2090	0.4
45	P.35		11/17	HW	LAN SPROM on Chip	De-pop U31,R537 Pop R538	0.4
46	P.36		11/17	EMI		Change C478 to 10P_50V	0.4
47	P.13		11/17	HW	RTC issue	Change C682,C686 to 15P	0.4
48	P.31,32,41		11/17	ESD		De-pop D3,D4,D17,D18,D15 Pop D24,D36	0.4
49	P.40		11/17	HW		De-pop R891,R893	0.4
50	P.24		11/21	HW		N13P_GS Change strap2 to PD 15k Change strap4 to PD 10k	0.4
51	P.13		11/21	HW		Chip Select Change R651,R2049 to 0ohm	0.4
52	P.13,40		11/21	HW		Delete NPCE885N (R2091.R2092.R2094.R2095.R2096,R698, R699,R692,C2085)	0.4
53	P.45		11/22	HW		Change +1.05VSDGPU JUMP size PJ19 change to 43x118	0.4
55	P.35,36		11/23	HW		Card Reader Change R216 to 22 ohm Change R2088 to 47ohm Change R2089 to 22 ohm Add C2091~C2093 Change R525,R536,R537,R538 to 1k	0.4
56	P.13		11/23	HW		Delete R2093,R2049,R651(0ohm)	0.4
57	P.13		11/23	HW		Change N13P-GS to SA000051880 Change U33 to SA00005AG00	0.4
58	P.35, P36		11/23	HW		Del C2093, R222, R2089, net(CR_CLK_XD_RY_BY#_23) Add R2101, C2094	0.4
59	P.36		11/24	HW		ADD R2102, C2096 for EMI ISSUE	0.4

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