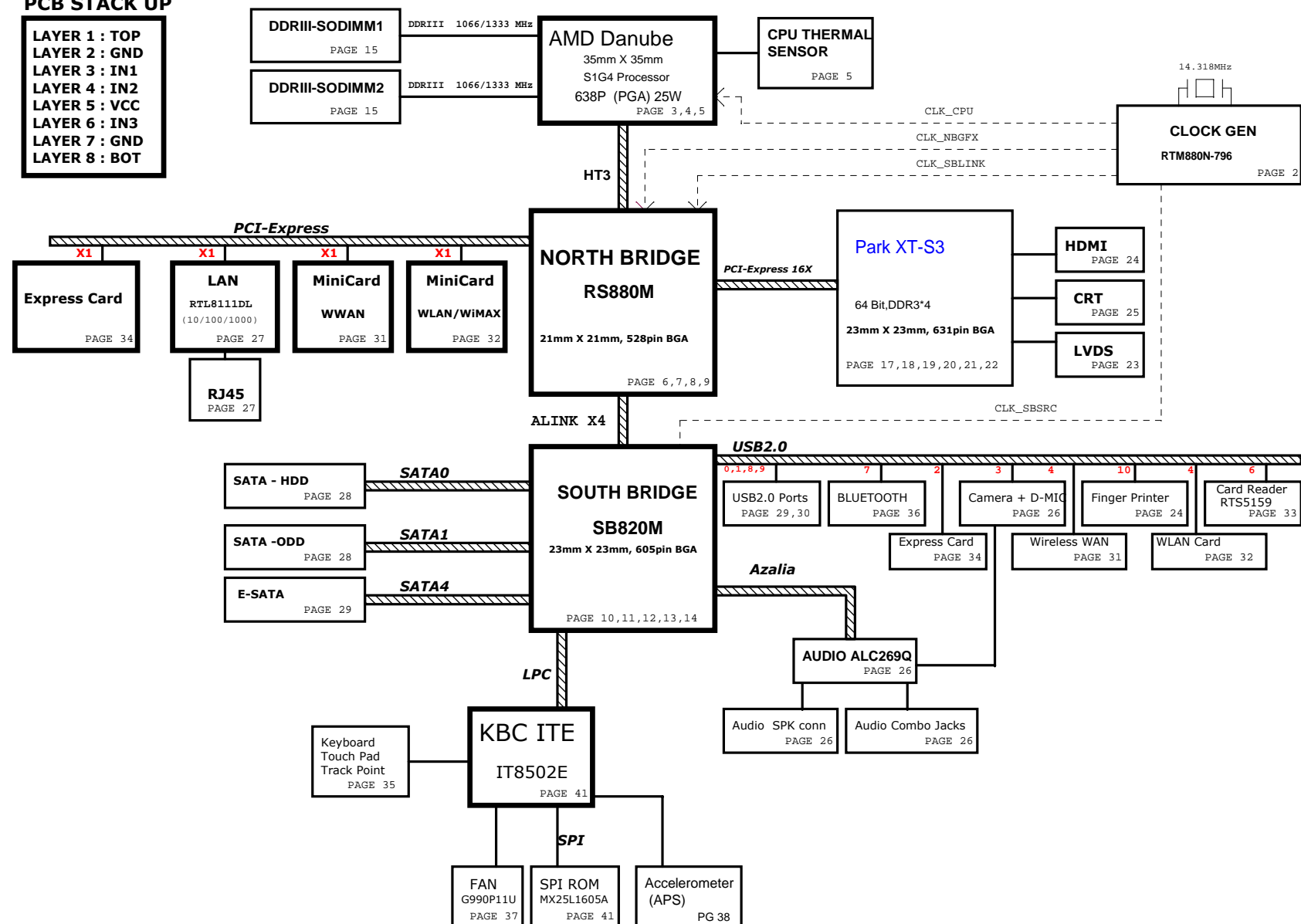


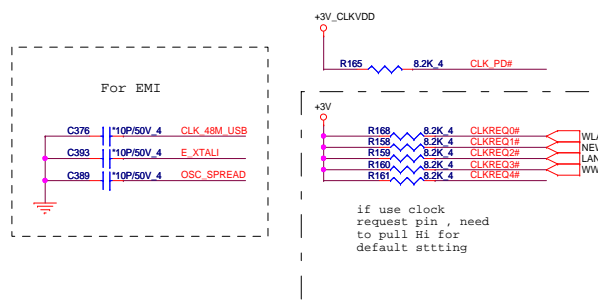
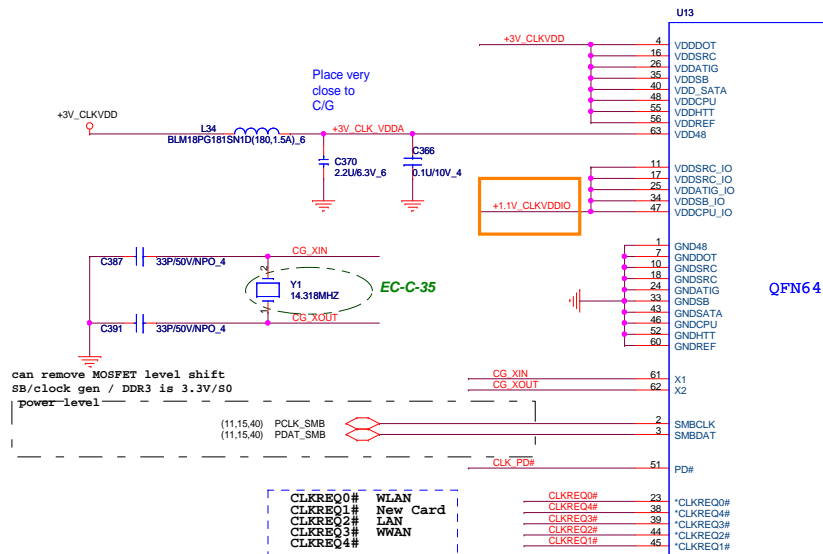
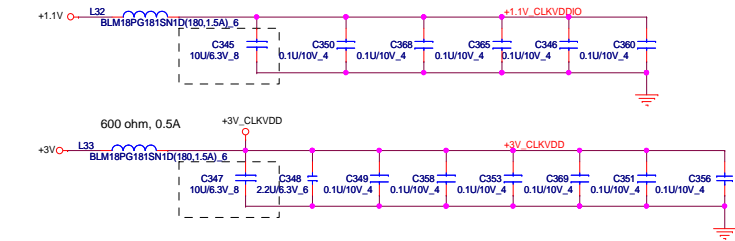
LD-Note Block Diagram -- AMD Danube

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

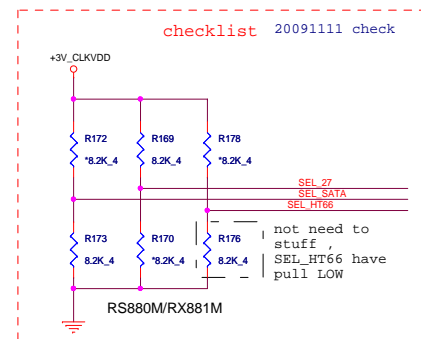
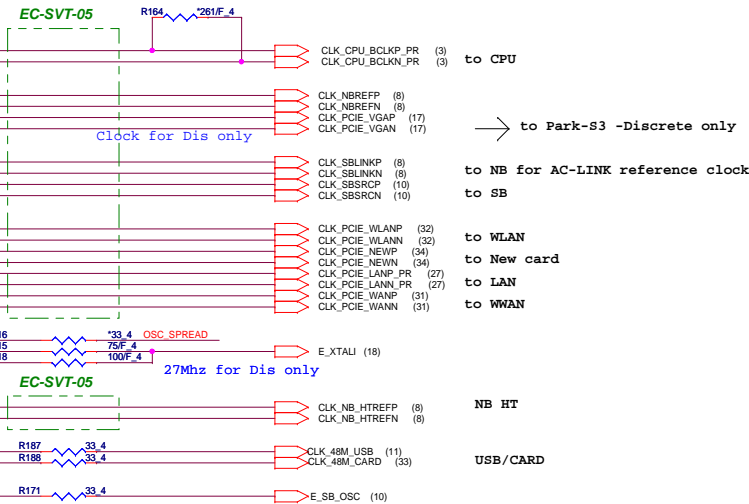


CLOCKS name	Discrete	Clock pin function
EXT GFX CLKP EXT_GFX_CLKN	RP47 STUFF	to Park-S3 external reference clock -Discrete only
SBLINK CLKP SBLINK_CLKN	RP43 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_NSS CLK_VGA_27M_SS	R213,R215 STUFF	To Park-S3 27Mhz - Discrete only

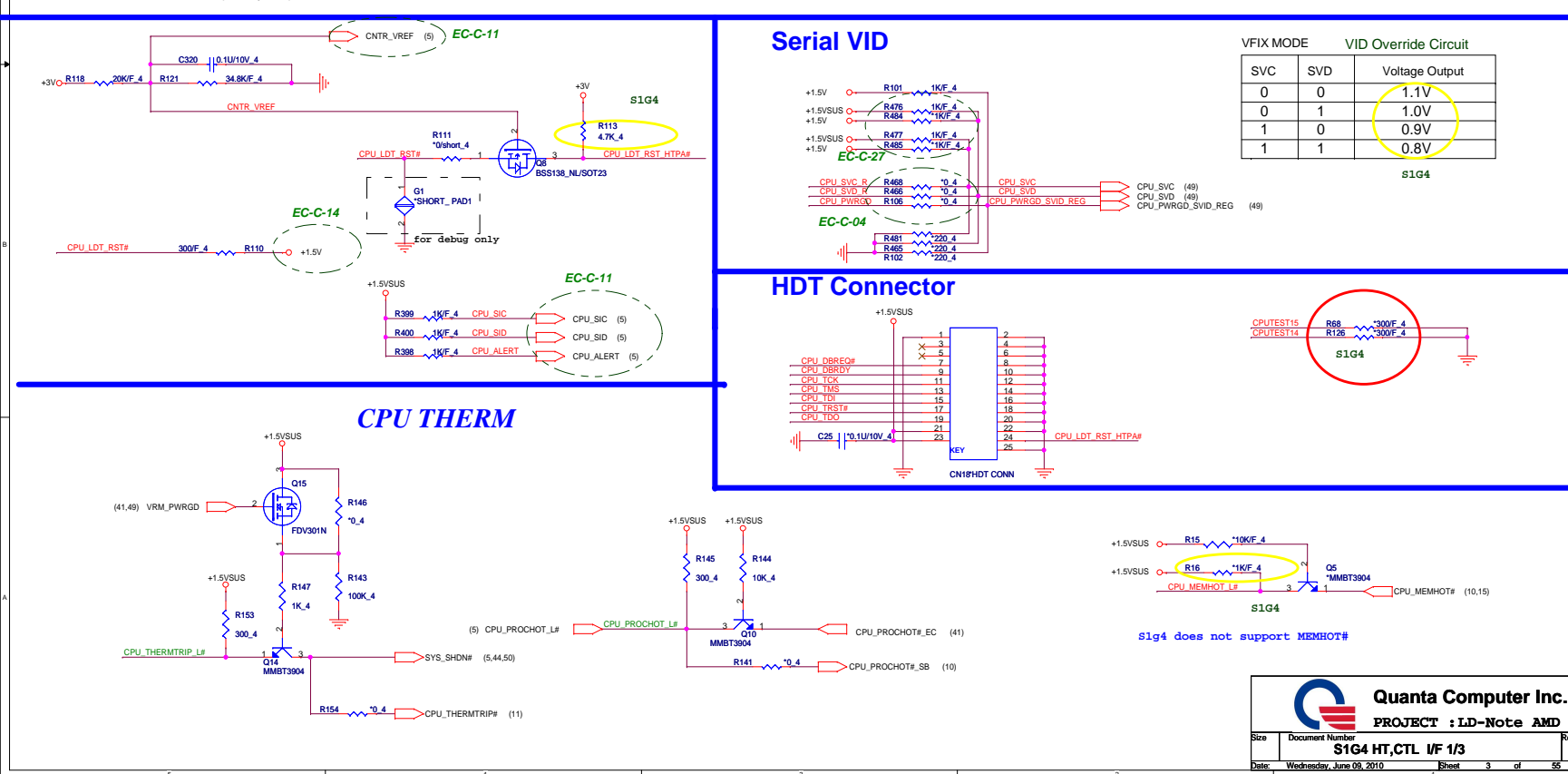
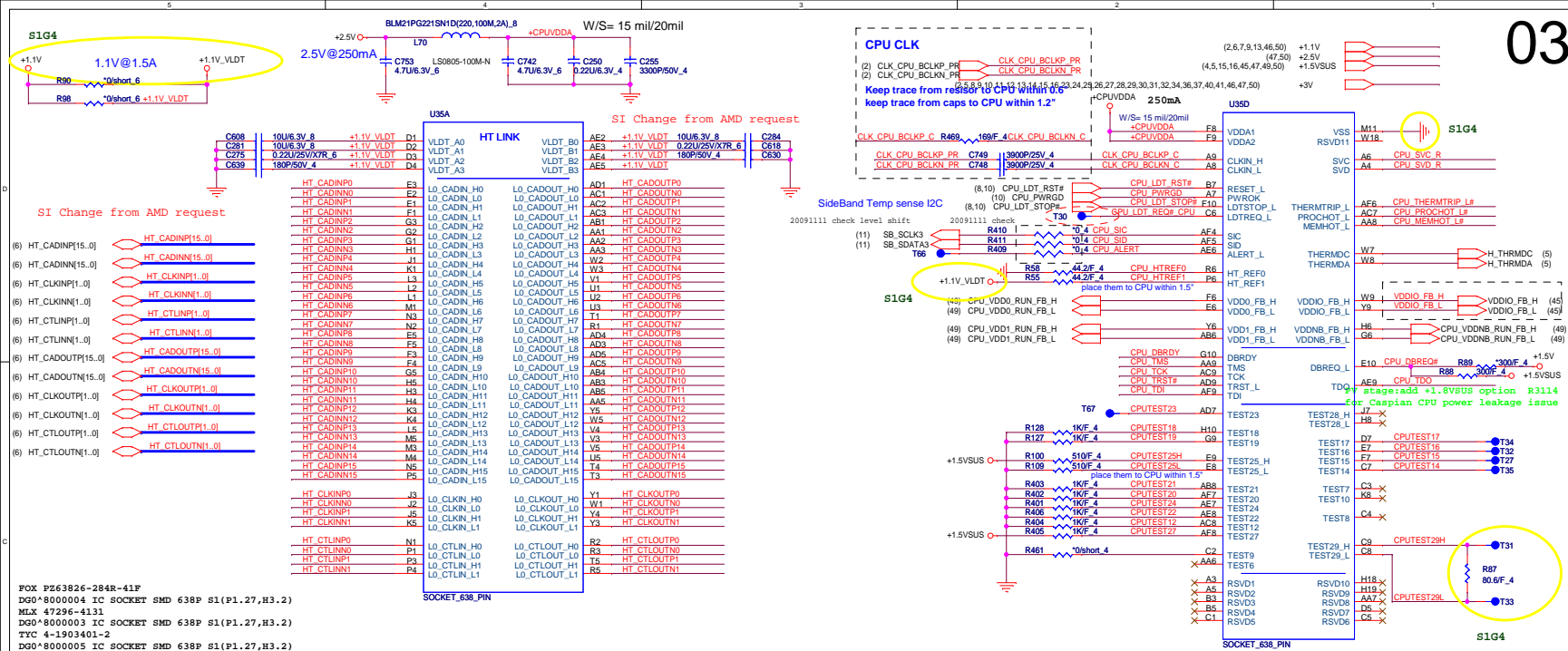


IDT ICS9LPRS476AKLFT
SLG SLG8SP628VTR--AL8SP628000
RTL RTM880N-796-- AL000880001

* default	
SEL_HTT66	1 66 MHz 3.3V single ended HTT clock
SEL_HTT66	0* 100 MHz differential HTT clock
SEL_SATA	1 100 MHz non-spreading differential SRC clock
SEL_SATA	0* 100 MHz spreading differential SRC clock
SEL_27	1* 27MHz non-spreading singled clock
SEL_27	0 100 MHz spreading differential SRC clock



Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

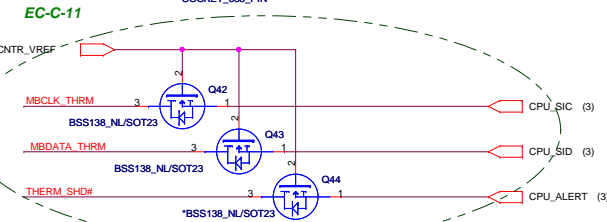
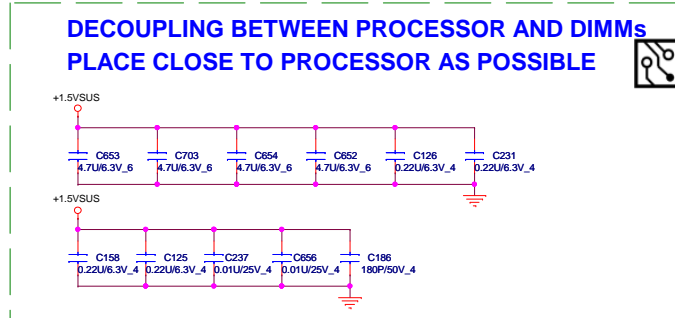
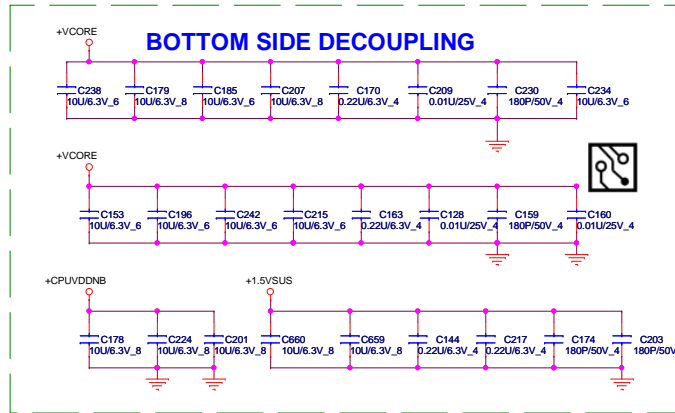
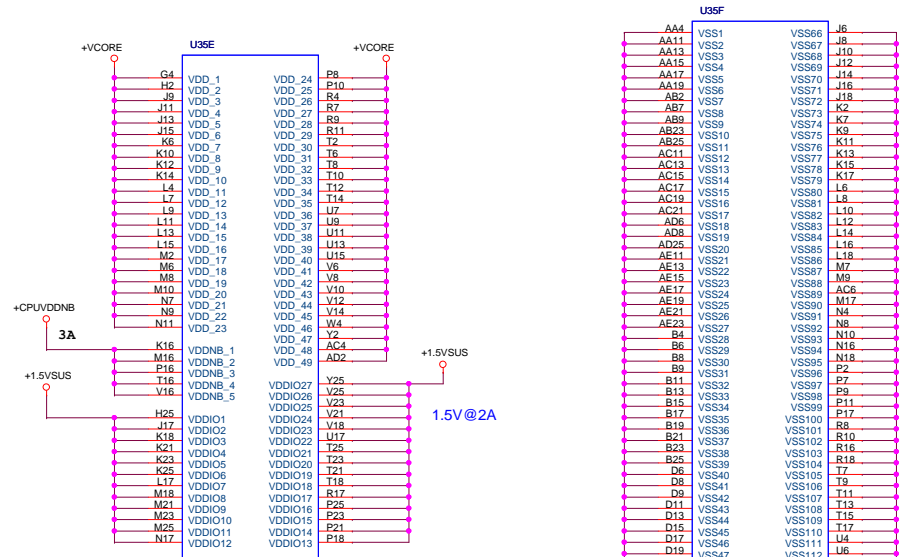




PROCESSOR POWER AND GROUND

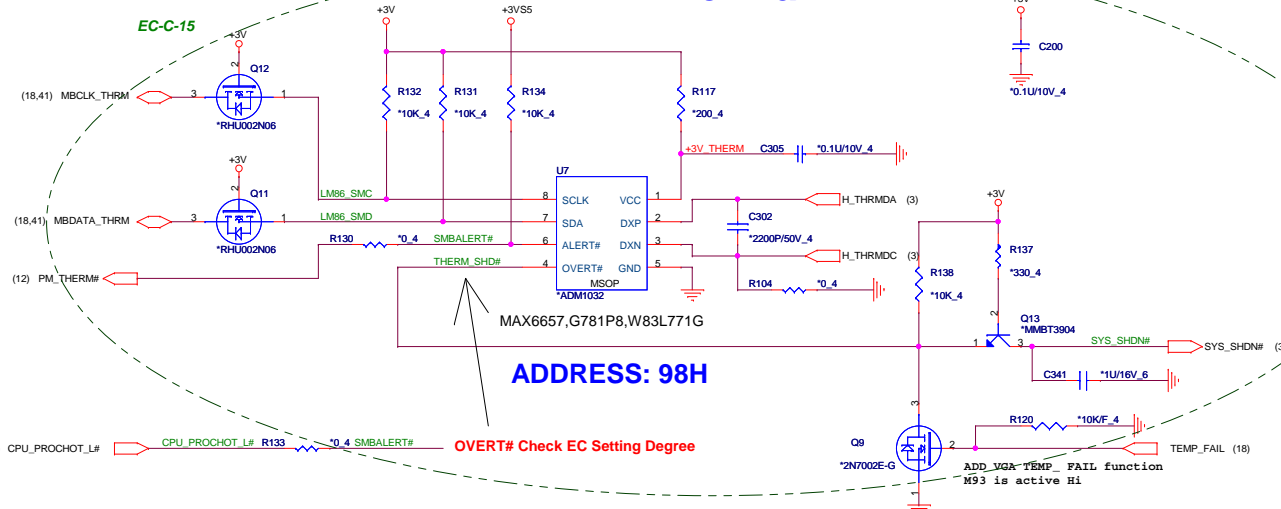
(49,50) +VCORE
(49,50) +CPUVDDNB
(3,4,15,16,45,47,49,50) +1.5VSUS
(2,3,8,9,10,11,12,13,14,15,16,23,24,25,26,27,28,29,30,31,32,34,36,37,40,41,46,47,50) +3V

05



CPU H/W MONITOR

Thermal



U34A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

HT_CADOUTP0	Y25	HT_RXCAD0P
HT_CADOUTN0	Y24	HT_RXCAD0N
HT_CADOUTP1	Y22	HT_RXCAD1P
HT_CADOUTN1	V23	HT_RXCAD1N
HT_CADOUTP2	V25	HT_RXCAD2P
HT_CADOUTN2	V24	HT_RXCAD2N
HT_CADOUTP3	U24	HT_RXCAD3P
HT_CADOUTN3	U25	HT_RXCAD3N
HT_CADOUTP4	T25	HT_RXCAD4P
HT_CADOUTN4	T24	HT_RXCAD4N
HT_CADOUTP5	P22	HT_RXCAD5P
HT_CADOUTN5	P23	HT_RXCAD5N
HT_CADOUTP6	P25	HT_RXCAD6P
HT_CADOUTN6	P24	HT_RXCAD6N
HT_CADOUTP7	N24	HT_RXCAD7P
HT_CADOUTN7	N25	HT_RXCAD7N
HT_CADOUTP8	AC24	HT_RXCAD8P
HT_CADOUTN8	AC25	HT_RXCAD8N
HT_CADOUTP9	AB25	HT_RXCAD9P
HT_CADOUTN9	AB24	HT_RXCAD9N
HT_CADOUTP10	AA24	HT_RXCAD10P
HT_CADOUTN10	AA25	HT_RXCAD10N
HT_CADOUTP11	Y22	HT_RXCAD11P
HT_CADOUTN11	Y23	HT_RXCAD11N
HT_CADOUTP12	W21	HT_RXCAD12P
HT_CADOUTN12	W20	HT_RXCAD12N
HT_CADOUTP13	V21	HT_RXCAD13P
HT_CADOUTN13	V20	HT_RXCAD13N
HT_CADOUTP14	U20	HT_RXCAD14P
HT_CADOUTN14	U21	HT_RXCAD14N
HT_CADOUTP15	U19	HT_RXCAD15P
HT_CADOUTN15	U18	HT_RXCAD15N
HT_CLKOUTP0	T22	HT_RXCLK0P
HT_CLKOUTN0	T23	HT_RXCLK0N
HT_CLKOUTP1	AB23	HT_RXCLK1P
HT_CLKOUTN1	AA22	HT_RXCLK1N
HT_CTLOUTP0	M22	HT_RXCTL0P
HT_CTLOUTN0	M23	HT_RXCTL0N
HT_CTLOUTP1	B21	HT_RXCTL1P
HT_CTLOUTN1	R20	HT_RXCTL1N

HT_TXCAD0P	D24	HT_CADINP0
HT_TXCAD0N	D25	HT_CADINN0
HT_TXCAD1P	E24	HT_CADINP1
HT_TXCAD1N	E25	HT_CADINN1
HT_TXCAD2P	F24	HT_CADINP2
HT_TXCAD2N	F25	HT_CADINN2
HT_TXCAD3P	F23	HT_CADINP3
HT_TXCAD3N	F22	HT_CADINN3
HT_TXCAD4P	H23	HT_CADINP4
HT_TXCAD4N	H22	HT_CADINN4
HT_TXCAD5P	J25	HT_CADINP5
HT_TXCAD5N	J24	HT_CADINN5
HT_TXCAD6P	K24	HT_CADINP6
HT_TXCAD6N	K25	HT_CADINN6
HT_TXCAD7P	K23	HT_CADINP7
HT_TXCAD7N	K22	HT_CADINN7
HT_TXCAD8P	F21	HT_CADINP8
HT_TXCAD8N	G21	HT_CADINN8
HT_TXCAD9P	G20	HT_CADINP9
HT_TXCAD9N	H21	HT_CADINN9
HT_TXCAD10P	J20	HT_CADINP10
HT_TXCAD10N	J21	HT_CADINN10
HT_TXCAD11P	J18	HT_CADINP11
HT_TXCAD11N	K17	HT_CADINN11
HT_TXCAD12P	L19	HT_CADINP12
HT_TXCAD12N	J19	HT_CADINN12
HT_TXCAD13P	M19	HT_CADINP13
HT_TXCAD13N	L18	HT_CADINN13
HT_TXCAD14P	M21	HT_CADINP14
HT_TXCAD14N	P21	HT_CADINN14
HT_TXCAD15P	P18	HT_CADINP15
HT_TXCAD15N	M18	HT_CADINN15
HT_TXCLK0P	H24	HT_CLKINP0
HT_TXCLK0N	H25	HT_CLKINN0
HT_TXCLK1P	L21	HT_CLKINP1
HT_TXCLK1N	L20	HT_CLKINN1
HT_TXCTL0P	M24	HT_CTLINP0
HT_TXCTL0N	M25	HT_CTLINN0
HT_TXCTL1P	F19	HT_CTLINP1
HT_TXCTL1N	R18	HT_CTLINN1
HT_TXCALP	B24	HT_TXCALN
HT_TXCALN	B25	HT_TXCALN

HT_CADOUTP[15..0]	HT_CADOUTP[15..0] (3)
HT_CADOUTN[15..0]	HT_CADOUTN[15..0] (3)
HT_CLKOUTP[1..0]	HT_CLKOUTP[1..0] (3)
HT_CLKOUTN[1..0]	HT_CLKOUTN[1..0] (3)
HT_CTLOUTP[1..0]	HT_CTLOUTP[1..0] (3)
HT_CTLOUTN[1..0]	HT_CTLOUTN[1..0] (3)
HT_CADINP[15..0]	HT_CADINP[15..0] (3)
HT_CADINN[15..0]	HT_CADINN[15..0] (3)
HT_CLKINP[1..0]	HT_CLKINP[1..0] (3)
HT_CLKINN[1..0]	HT_CLKINN[1..0] (3)
HT_CTLINP[1..0]	HT_CTLINP[1..0] (3)
HT_CTLINN[1..0]	HT_CTLINN[1..0] (3)

(2,3,7,9,13,46,50) +1.1V
 (3,8,31,32,34,50) +1.5V
 (8,9,14,46,50) +1.8V

Close to NB within 1"



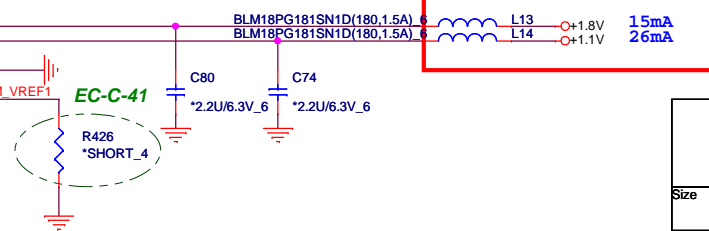
Close to NB within 1"

U34D

PAR 4 OF 6

AB12	MEM_A0(NC)	MEM_DQ0/DVO_VSYNC(NC)	AA18
AE16	MEM_A1(NC)	MEM_DQ1/DVO_HSYNC(NC)	AA20
V11	MEM_A2(NC)	MEM_DQ2/DVO_DE(NC)	AA19
AE15	MEM_A3(NC)	MEM_DQ3/DVO_D0(NC)	Y19
AB12	MEM_A4(NC)	MEM_DQ4(NC)	Y17
AB16	MEM_A5(NC)	MEM_DQ5/DVO_D1(NC)	AA17
AD14	MEM_A6(NC)	MEM_DQ6/DVO_D2(NC)	AA15
AD13	MEM_A7(NC)	MEM_DQ7/DVO_D4(NC)	Y15
AD15	MEM_A8(NC)	MEM_DQ8/DVO_D3(NC)	AC20
AC16	MEM_A9(NC)	MEM_DQ9/DVO_D5(NC)	AD19
AE13	MEM_A10(NC)	MEM_DQ10/DVO_D6(NC)	AE22
AC14	MEM_A11(NC)	MEM_DQ11/DVO_D7(NC)	AC18
Y14	MEM_A12(NC)	MEM_DQ12(NC)	AB20
AD17	MEM_A13(NC)	MEM_DQ13/DVO_D9(NC)	AD22
AD16	MEM_BA0(NC)	MEM_DQ14/DVO_D10(NC)	AC22
AE17	MEM_BA1(NC)	MEM_DQ15/DVO_D11(NC)	AD21
AD17	MEM_BA2(NC)	MEM_DQS0P/DVO_IDCKP(NC)	Y17
W12	MEM_RASb(NC)	MEM_DQS0N/DVO_IDCKN(NC)	W18
Y12	MEM_CASb(NC)	MEM_DQS1P(NC)	AD20
AD18	MEM_WEb(NC)	MEM_DQS1N(NC)	AE21
AB13	MEM_CSb(NC)	MEM_DM0(NC)	W17
AB18	MEM_CKE(NC)	MEM_DM1/DVO_D8(NC)	AE19
V14	MEM_ODT(NC)	IOPLLVD18(NC)	AE23
V15	MEM_CKP(NC)	IOPLLVD18(NC)	AE24
W14	MEM_CKN(NC)	IOPLLVD18(NC)	AD23
AE12	MEM_COMP(NC)	IOPLLVD18(NC)	AE18
AD12	MEM_COMP(NC)	MEM_VREF(NC)	

RS880/RX881



Quanta Computer Inc.

PROJECT : LD-Note AMD DIS

Size	Document Number	Rev
	RS880M-HT LINK I/F 1/4	1A
Date	Wednesday, June 09, 2010	Sheet 6 of 55

(17) PEG_RXN[0..15]

PEG_RXN0
PEG_RXN1
PEG_RXN2
PEG_RXN3
PEG_RXN4
PEG_RXN5
PEG_RXN6
PEG_RXN7
PEG_RXN8
PEG_RXN9
PEG_RXN10
PEG_RXN11
PEG_RXN12
PEG_RXN13
PEG_RXN14
PEG_RXN15

(17) PEG_RXP[15..0]

PEG_RXP15
PEG_RXP14
PEG_RXP13
PEG_RXP12
PEG_RXP11
PEG_RXP10
PEG_RXP9
PEG_RXP8
PEG_RXP7
PEG_RXP6
PEG_RXP5
PEG_RXP4
PEG_RXP3
PEG_RXP2
PEG_RXP1
PEG_RXP0

PEG_RXP15 D4
PEG_RXN15 C4
PEG_RXP14 B3
PEG_RXP13 C2
PEG_RXN13 C1
PEG_RXP12 E5
PEG_RXN12 E5
PEG_RXN13 G5
PEG_RXN11 G6
PEG_RXP10 H5
PEG_RXN10 H6
PEG_RXP9 J5
PEG_RXN9 J5
PEG_RXP8 J7
PEG_RXN8 J8
PEG_RXP7 L5
PEG_RXN7 L6
PEG_RXP6 M8
PEG_RXN6 L8
PEG_RXP5 P7
PEG_RXN5 M7
PEG_RXP4 P9
PEG_RXN4 M5
PEG_RXP3 R8
PEG_RXN3 P8
PEG_RXP2 R6
PEG_RXN2 R5
PEG_RXP1 P4
PEG_RXN1 P3
PEG_RXP0 T4
PEG_RXN0 T3

U34B

PART 2 OF 6

PCIE I/F GFX

GFX_RX0P A5
GFX_RX0N A5
GFX_RX1P A4
GFX_RX1N A4
GFX_RX2P C3
GFX_RX2N B2
GFX_RX3P D1
GFX_RX3N D2
GFX_RX4P E1
GFX_RX4N E2
GFX_RX5P F4
GFX_RX5N F3
GFX_RX6P F2
GFX_RX6N H4
GFX_RX7P H3
GFX_RX7N H3
GFX_RX8P H1
GFX_RX8N H2
GFX_RX9P J1
GFX_RX9N K4
GFX_RX10P K3
GFX_RX10N K3
GFX_TX10P K1
GFX_TX10N K2
GFX_TX11P M4
GFX_TX11N M3
GFX_TX12P M3
GFX_TX12N M1
GFX_TX13P M2
GFX_TX13N M2
GFX_TX14P N1
GFX_TX14N P1
GFX_TX15P P2
GFX_TX15N P2

PEG_C_TXP15 C712
PEG_C_TXP14 C708
PEG_C_TXP13 C704
PEG_C_TXP12 C687
PEG_C_TXP11 C685
PEG_C_TXP10 C681
PEG_C_TXP9 C678
PEG_C_TXP8 C673
PEG_C_TXP7 C672
PEG_C_TXP6 C669
PEG_C_TXP5 C141
PEG_C_TXP4 C667
PEG_C_TXP3 C664
PEG_C_TXP2 C662
PEG_C_TXP1 C657
PEG_C_TXP0 C650

0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
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0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4

PEG_TXP15
PEG_TXP14
PEG_TXP13
PEG_TXP12
PEG_TXP11
PEG_TXP10
PEG_TXP9
PEG_TXP8
PEG_TXP7
PEG_TXP6
PEG_TXP5
PEG_TXP4
PEG_TXP3
PEG_TXP2
PEG_TXP1
PEG_TXP0

PEG_TXP[15..0] (17)

PEG_C_TXN15 C715
PEG_C_TXN14 C710
PEG_C_TXN13 C706
PEG_C_TXN12 C691
PEG_C_TXN11 C686
PEG_C_TXN10 C684
PEG_C_TXN9 C680
PEG_C_TXN8 C676
PEG_C_TXN7 C674
PEG_C_TXN6 C671
PEG_C_TXN5 C151
PEG_C_TXN4 C668
PEG_C_TXN3 C666
PEG_C_TXN2 C663
PEG_C_TXN1 C661
PEG_C_TXN0 C658

0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4

PEG_TXN15
PEG_TXN14
PEG_TXN13
PEG_TXN12
PEG_TXN11
PEG_TXN10
PEG_TXN9
PEG_TXN8
PEG_TXN7
PEG_TXN6
PEG_TXN5
PEG_TXN4
PEG_TXN3
PEG_TXN2
PEG_TXN1
PEG_TXN0

PEG_TXN[0..15] (17)

(34) PCIE_RXP0
(34) PCIE_RXN0
(27) PCIE_RXP1_LAN
(27) PCIE_RXN1_LAN
(32) PCIE_RXP2
(32) PCIE_RXN2
(31) PCIE_RXP3
(31) PCIE_RXN3

PCIE_RXP0 AE3
PCIE_RXN0 AD4
PCIE_RXP1_LAN AE2
PCIE_RXN1_LAN AD3
PCIE_RXP2 AD1
PCIE_RXN2 AD2
PCIE_RXP3 V5
PCIE_RXN3 V6
X U5
X U6
X U8
X U7

PCIE I/F GPP

GPP_RX0P
GPP_RX0N
GPP_RX1P
GPP_RX1N
GPP_RX2P
GPP_RX2N
GPP_RX3P
GPP_RX3N
GPP_RX4P
GPP_RX4N
GPP_RX5P
GPP_RX5N

AC1 PCIE_TXP0_C C628
AC2 PCIE_TXN0_C C627
AB4 PCIE_TXP1_LAN_C C625
AB3 PCIE_TXN1_LAN_C C626
AA2 PCIE_TXP2_C C643
AA1 PCIE_TXN2_C C641
Y1 PCIE_TXP3_C C647
Y2 PCIE_TXN3_C C646

0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4

PCIE_TXP0 (34)
PCIE_TXN0 (34)
PCIE_TXP1_LAN (27)
PCIE_TXN1_LAN (27)
PCIE_TXP2 (32)
PCIE_TXN2 (32)
PCIE_TXP3 (31)
PCIE_TXN3 (31)

TO NEW CARD
TO PCIE-LAN
TO WLAN
TO WWAN

(10) A_RXP0
(10) A_RXN0
(10) A_RXP1
(10) A_RXN1
(10) A_RXP2
(10) A_RXN2
(10) A_RXP3
(10) A_RXN3

AA8 SB_RX0P
Y8 SB_RX0N
AA7 SB_RX1P
Y7 SB_RX1N
AA5 SB_RX2P
AA6 SB_RX2N
V5 SB_RX3P
Y5 SB_RX3N

PCIE I/F SB

SB_TX0P
SB_TX0N
SB_TX1P
SB_TX1N
SB_TX2P
SB_TX2N
SB_TX3P
SB_TX3N

AD7 A_TXP0_C C636
AE7 A_TXN0_C C635
AE6 A_TXP1_C C612
AD6 A_TXN1_C C613
AB6 A_TXP2_C C633
AC6 A_TXN2_C C634
AD5 A_TXP3_C C631
AE5 A_TXN3_C C632

0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4
0.1U/10V/X7R 4

A_TXP0 (10)
A_TXN0 (10)
A_TXP1 (10)
A_TXN1 (10)
A_TXP2 (10)
A_TXN2 (10)
A_TXP3 (10)
A_TXN3 (10)

PCE_CALRP(PCE_BCALRP)
PCE_CALRN(PCE_BCALRN)

RS880/RX881

AC8 NB_PCIECALRP R43
AB8 NB_PCIECALRN R425

1.27K/F 4
2K/F 4

+1.1V



Keep the impedance of PCIE lane to 85ohm +/-15%
Including the A-link



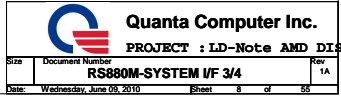
All PCIE lane shou route 8" max for Gen2 connector and max 12" for Gen2 on board devices
Guam has the Lasso lane over 8" due to the large board, should use shorter lasso calbe for Guam.
Customer need to follow the MBDG.



Quanta Computer Inc.

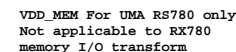
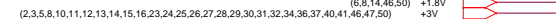
PROJECT :LD-Note AMD DIS

Size	Document Number	Rev
	RS880M-PCIE I/F 2/4	1A
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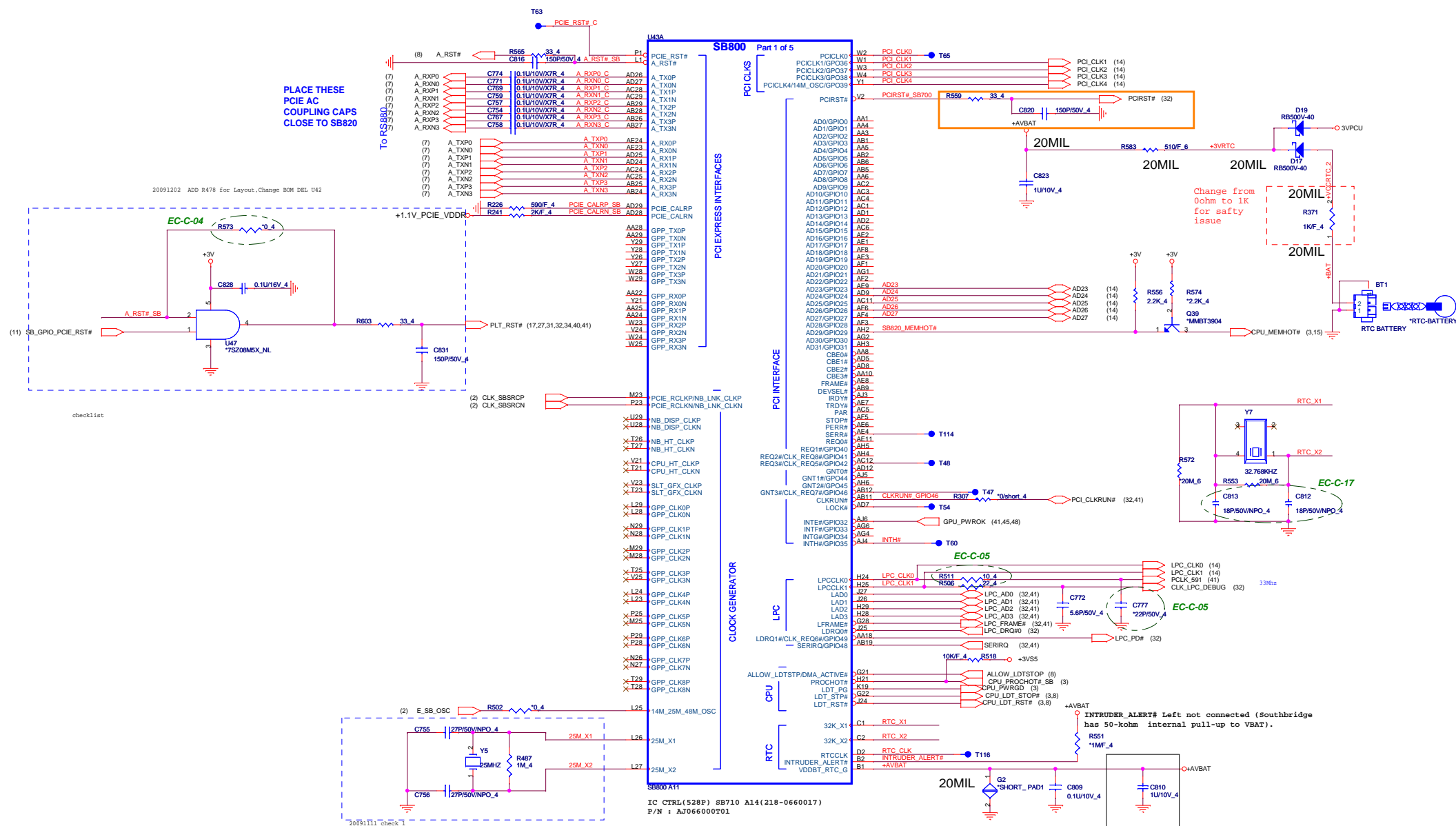




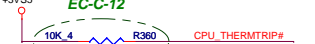
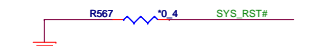
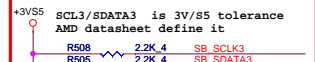
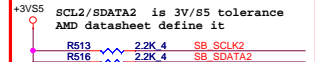
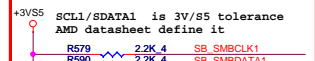
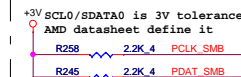
PIN NAME	RX881	RS880	PIN NAME	RX881	RS880
VDDHT	+1.1V	+1.1V	AVDDI	GND	GND
VDDHTRX	+1.1V	+1.1V	AVDDQ	GND	GND
VDDHTTX	+1.2V	+1.1V	PLLVD	GND	GND
VDDA18PCIE	+1.8V	+1.8V	PLLVD018	GND	GND
VDDG18	+1.8V	+1.8V	VDDA18PCIEPLL	GND	GND
VDD18_MEM	GND	GND	VDDA18HTFLL	GND	GND
VDDPCE	+1.1V	+1.1V	VDDLTP18	GND	GND
VDDC	+1.1V	+NB_CORE	VDDL18	GND	GND
VDD_MEM	GND	GND	VDDL13	NC	NC
VDDG33	+3.3V	+3.3V			
AVDD	GND	GND			



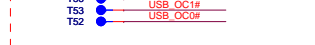
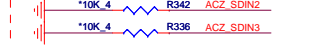
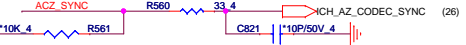
(5,11,12,13,14,29,32,50) +3VS5
 (2,3,5,8,9,11,12,13,14,15,16,23,24,25,26,27,28,29,30,31,32,34,36,37,40,41,46,47,50) +3V
 (41) +3VRTC
 (23,27,35,39,41,43,44,45,46,47,48,50) 3VPCU



NC only ,Can't be install

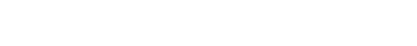
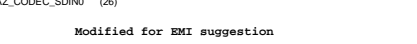
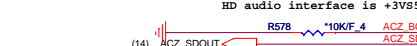
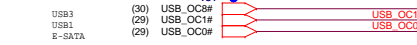
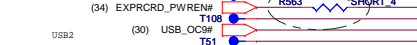
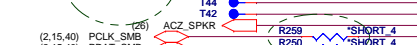
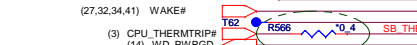
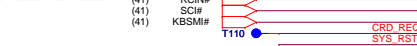
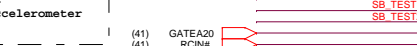
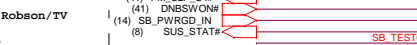
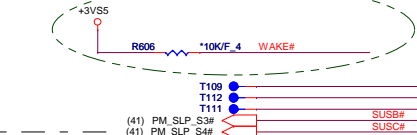


To Azalia

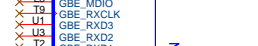
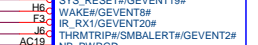
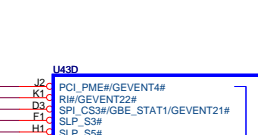


checklist

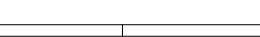
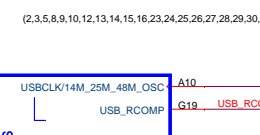
EC-C-25



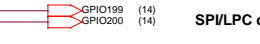
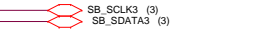
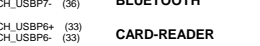
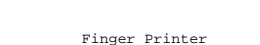
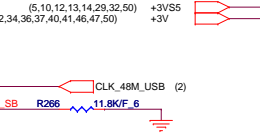
EC-C-24



EC-C-25



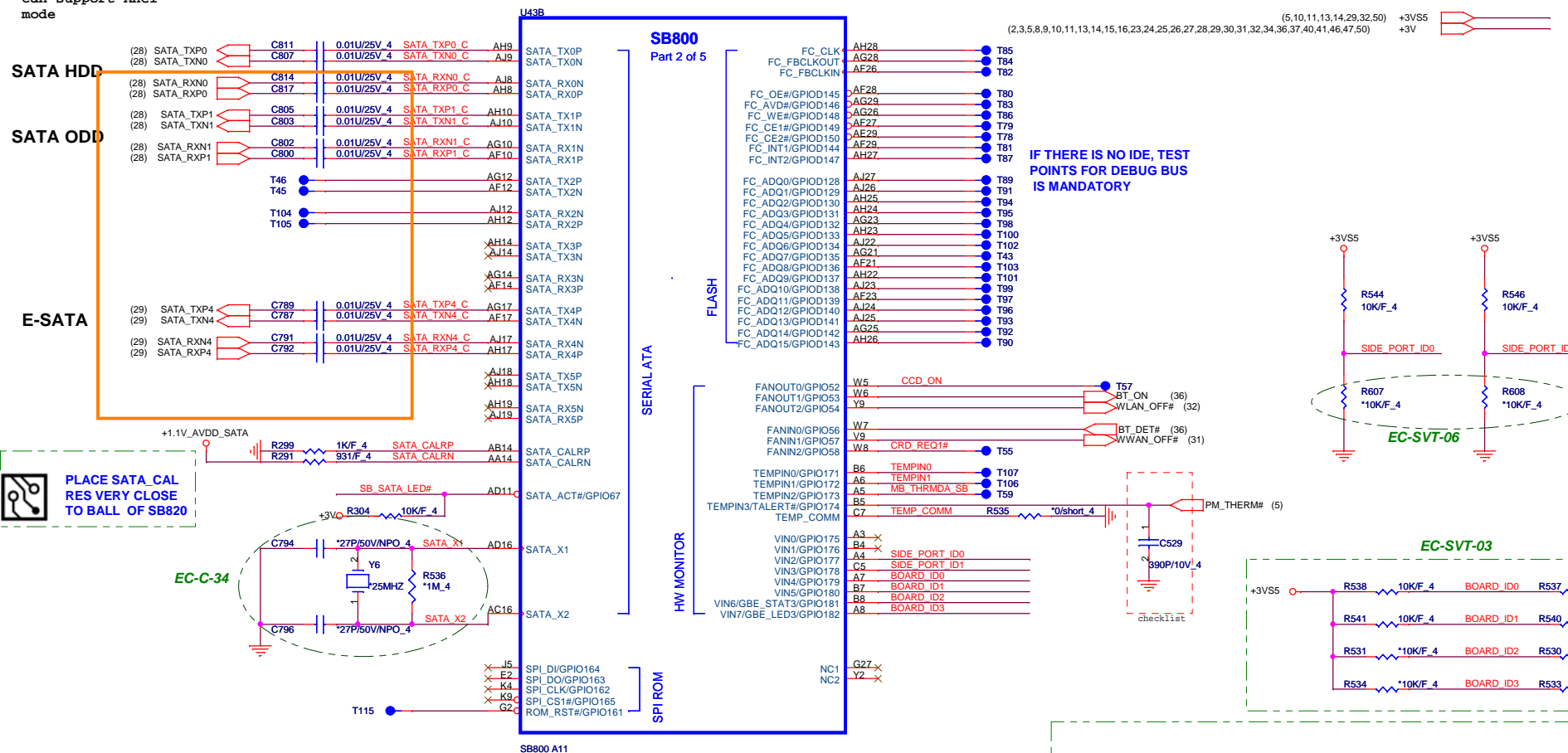
EC-C-26



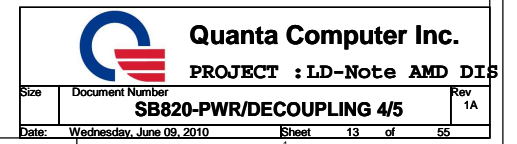
EC-C-27



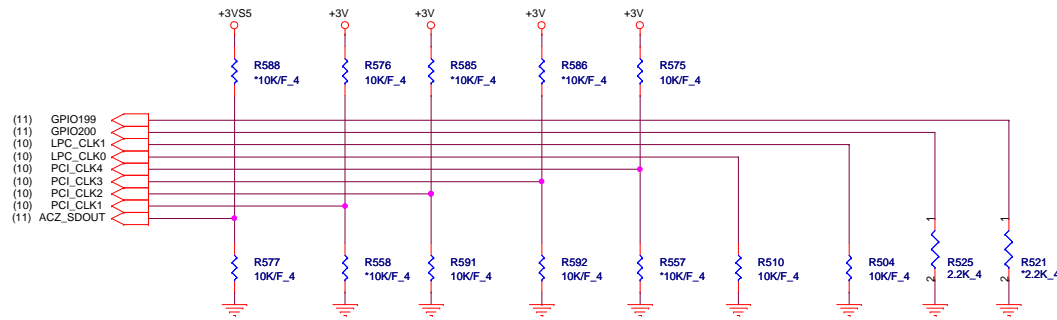
SATA PORT 0,1,2,3
can support AHCI
mode



EC_ID1	ID3	ID2	ID1	ID0	
	0	X	X	X	BL GC5C UMA(14")
	1	X	X	X	LD GC6C UMA(15")
0	X	0	0	0	SDV
0	X	0	0	1	SIT
0	X	0	1	0	SIT-R2
0	X	0	1	1	SVT
0	X	1	0	0	SOVP
	X	1	1	1	USB HW solution implementation



REQUIRED STRAPS



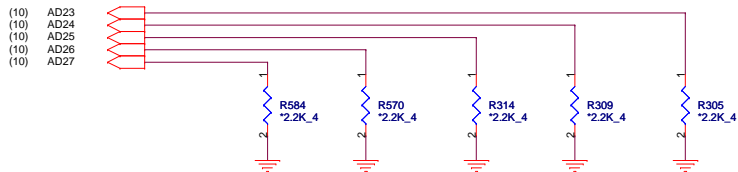
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED	H, H=Reserved H, L=SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	L, H=LPC ROM DEFAULT L, L=FWH ROM	

internal have
pull Hi 10K

NB_PWRGD_IN:
R5880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



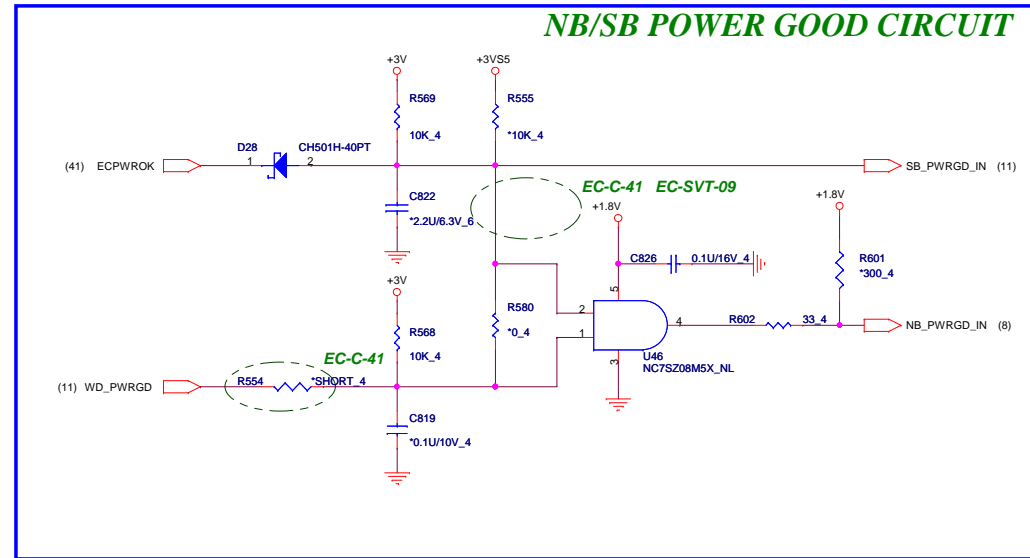
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

14

NB/SB POWER GOOD CIRCUIT



AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5



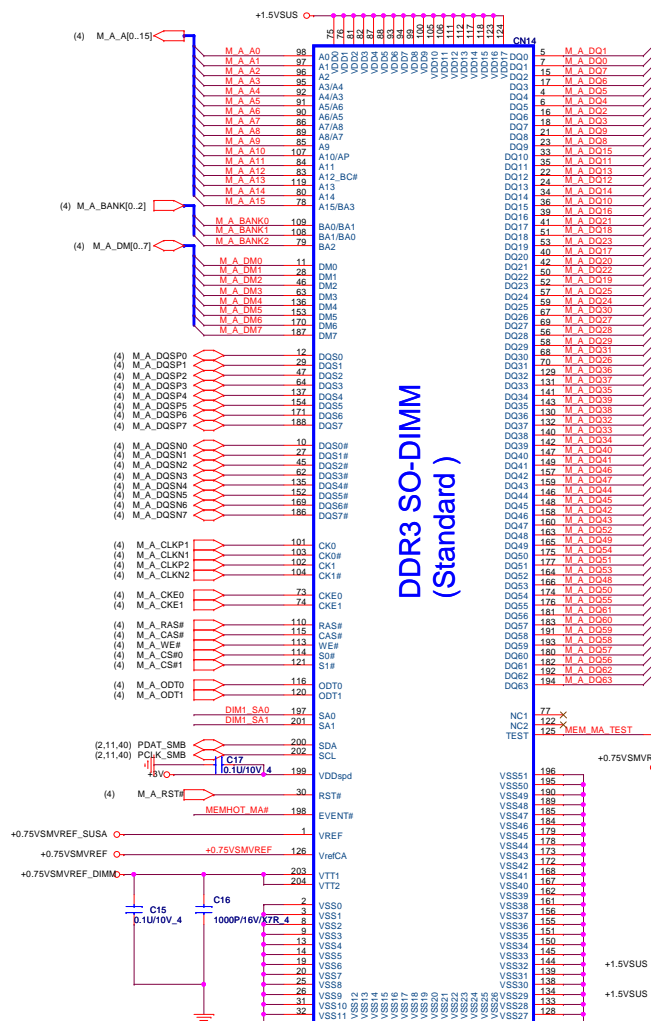
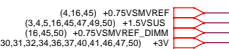
Quanta Computer Inc.

PROJECT :LD-Note AMD DIS

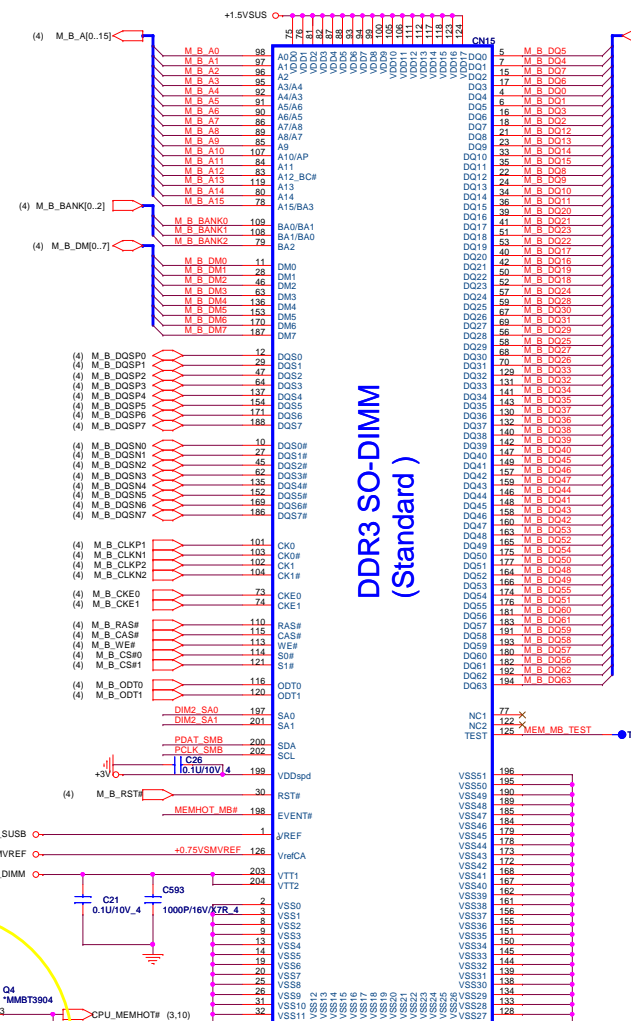
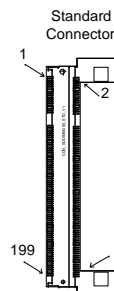
Size	Document Number	Rev
	SB820-STRAPS 5/5	1A
Date:	Monday, June 14, 2010	Sheet 14 of 55

Place these Caps near So-Dimm0.

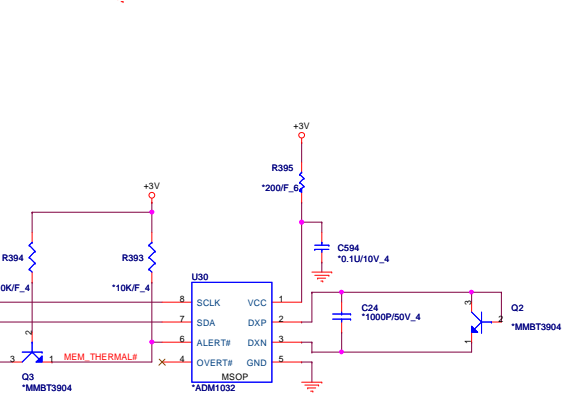
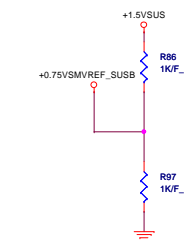
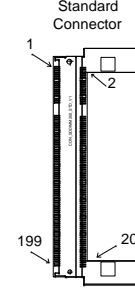
Place these Caps near So-Dimm1.



DDR3 SO-DIMM
(Standard)

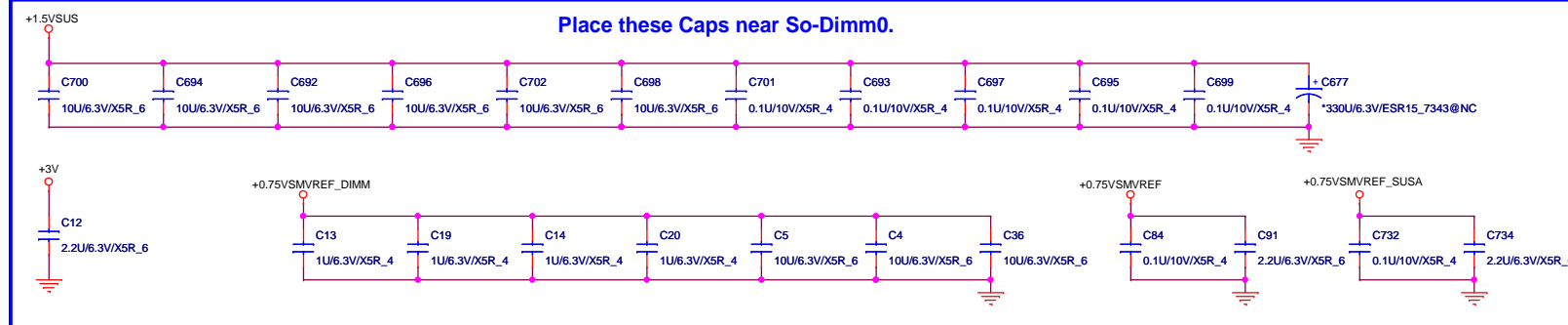


DDR3 SO-DIMM
(Standard)

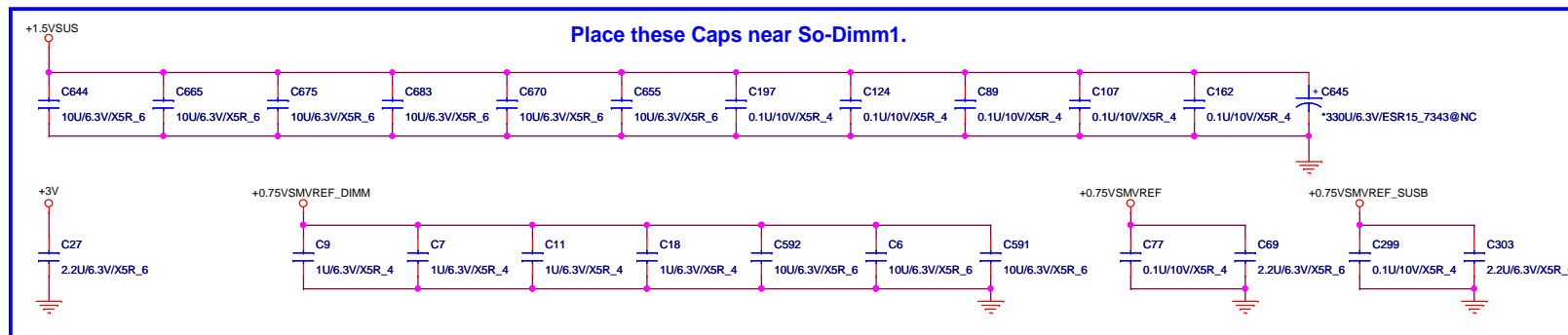


Close DDR3 socket

Place these Caps near So-Dimm0.



Place these Caps near So-Dimm1.

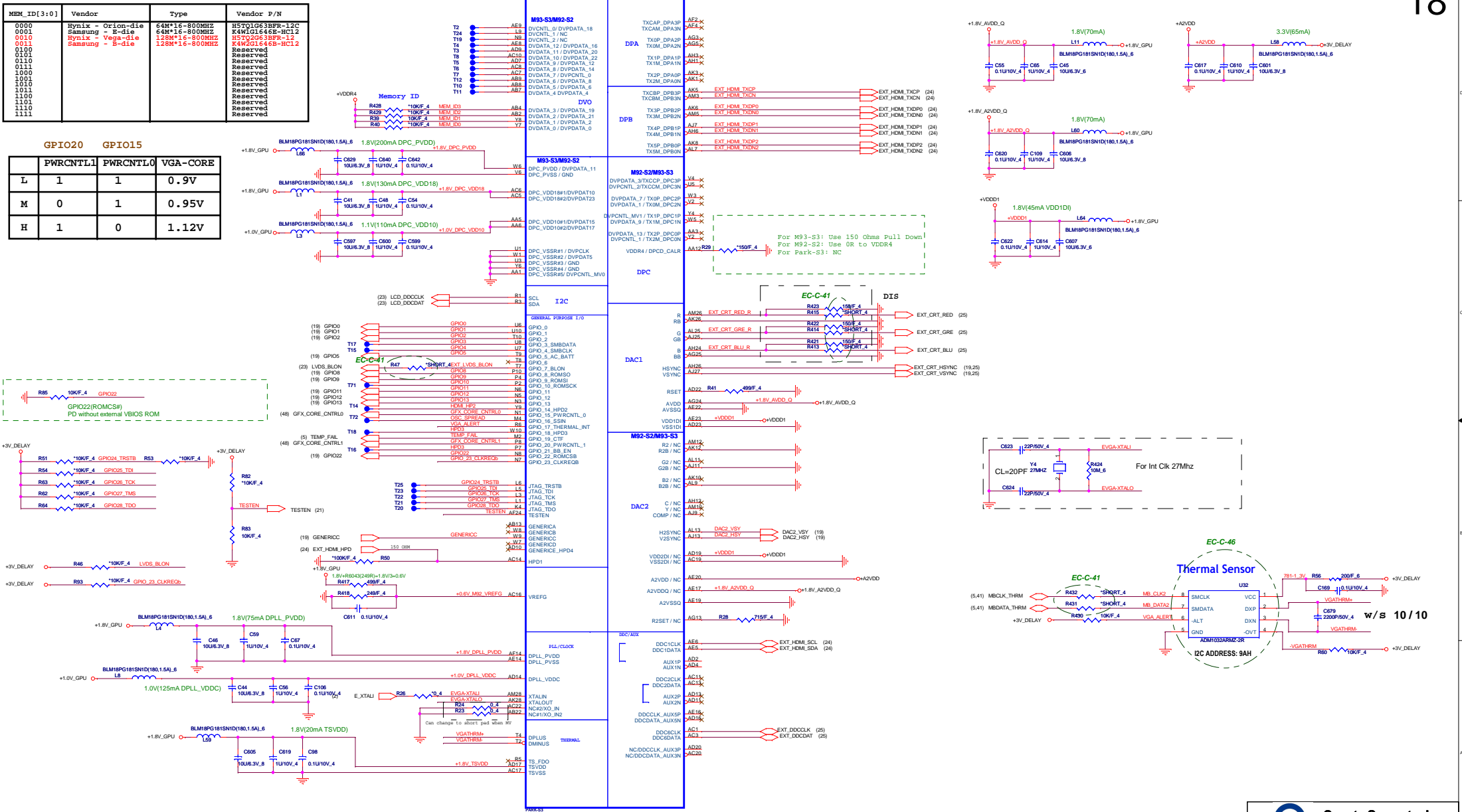




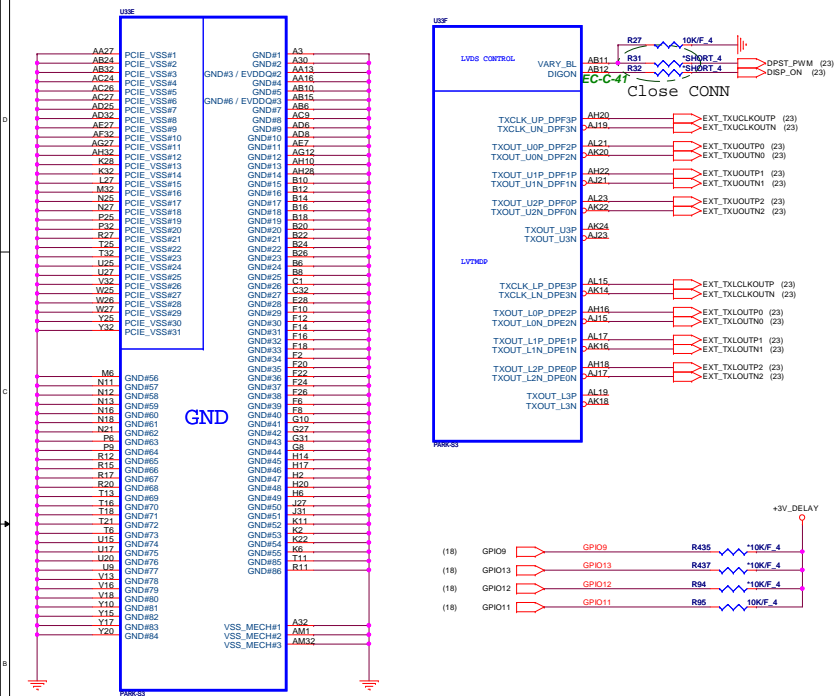
A

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Rhynix - Grion-die	64M*16=800MHZ	H5TQ16G3BFR-12C
0001	Samung - E-die	64M*16=800MHZ	K4W1G1646B-HC12
0010	Rhynix - Vega-die	128M*16=800MHZ	H5TQ16G3BFR-12C
0011	Samung - B-die	128M*16=800MHZ	K4W2G1646B-HC12
0100	Reserved		Reserved
0101	Reserved		Reserved
0110	Reserved		Reserved
0111	Reserved		Reserved
1000	Reserved		Reserved
1001	Reserved		Reserved
1010	Reserved		Reserved
1011	Reserved		Reserved
1100	Reserved		Reserved
1101	Reserved		Reserved
1110	Reserved		Reserved
1111	Reserved		Reserved

	GPIO20	GPIO15	
	PWRCNTL1	PWRCNTL0	VGA-CORE
L	1	1	0.9V
M	0	1	0.95V
H	1	0	1.12V

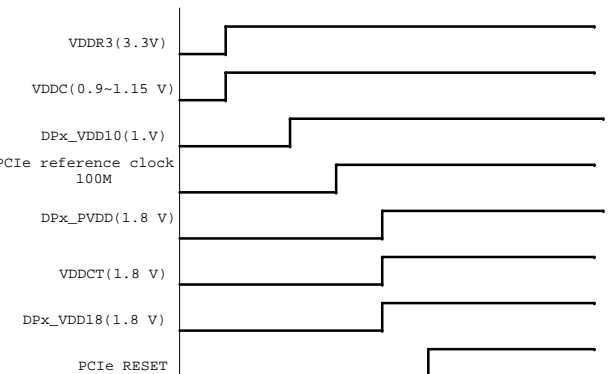


Power-Up Sequence

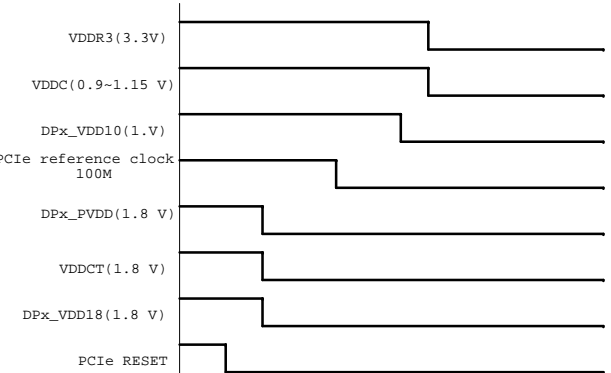


CONFIGURATION STRAPS			RECOMMENDED SETTINGS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			0 = DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG2(2)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SVC	IGNORE VIP DEVICE STRAPS	0
RSVD AUDI[1] AUDI[0]	GENERICC HSYNC VSYNC	AUDI[1] AUDI[0] 0: No audio function 0: 1 Audio for DisplayPort and HDMI if dongle is detected 1: 0 Audio for DisplayPort only 1: 1 Audio for both DisplayPort and HDMI	0 11

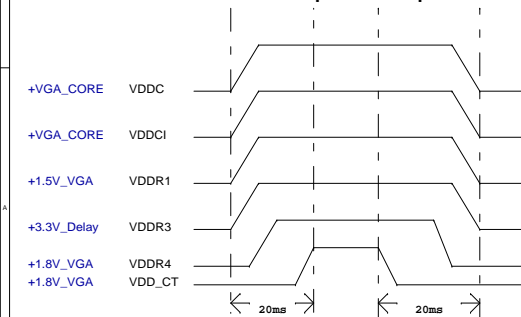
<p align="center">AMD RESERVED CONFIGURATION STRAPS</p> <p align="center">ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET</p>	
HQSYNC	GENERICC
<p align="center">PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET</p>	
GPIO21_BB_EN	



Power-down Sequence



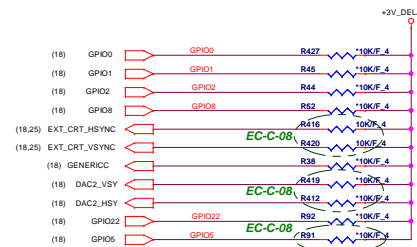
Power Up/Down Sequence

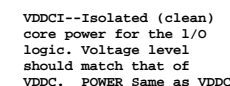


Memory Aperture size

GPI09		GPI013	GPI012	GPI011
BIOSROM		ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

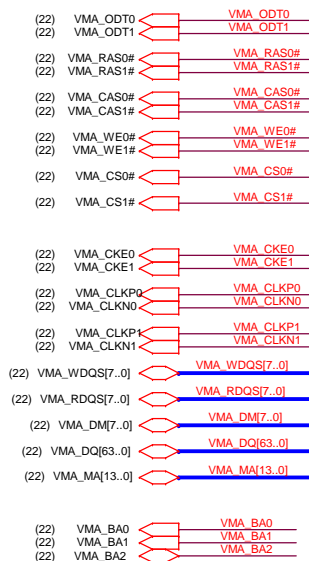




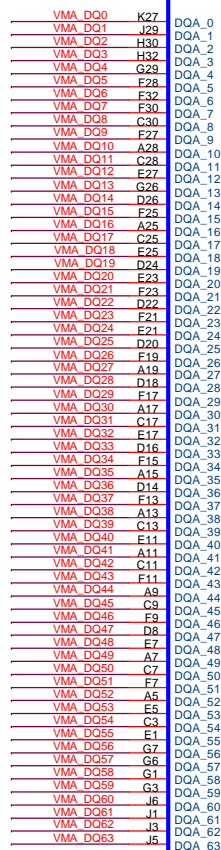
VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V ($\pm 5\%$)

PCIE_VDDC--PCI-E
Digital Power
Supply (Either 1.0
V or 1.1 V) 1.0 V
-5% to 1.1 V +5%

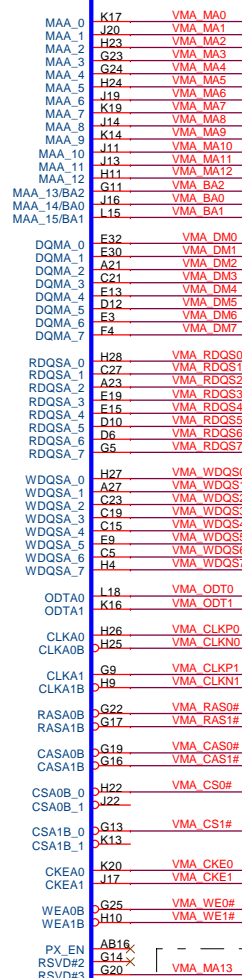
Quanta Computer Inc.
PROJECT : LD-Note AMD DIS



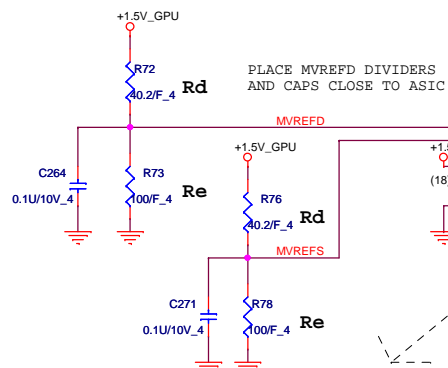
support 1gbt
VRAM (64M X 16)



MEMORY INTERFACE



For PARK-S3 only
For M9X-S2/S3 with
DDR3: this pin is
not in use.

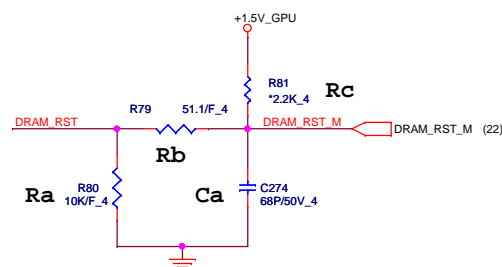


Do not Install for
M9X-S2/S3
Install 240 Ohms
0.5% Resistor
for PARK-S3

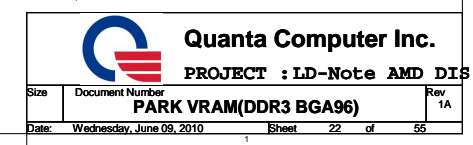
EC-SVT-07

route 50ohms
single-ended/100ohms diff
and keep short

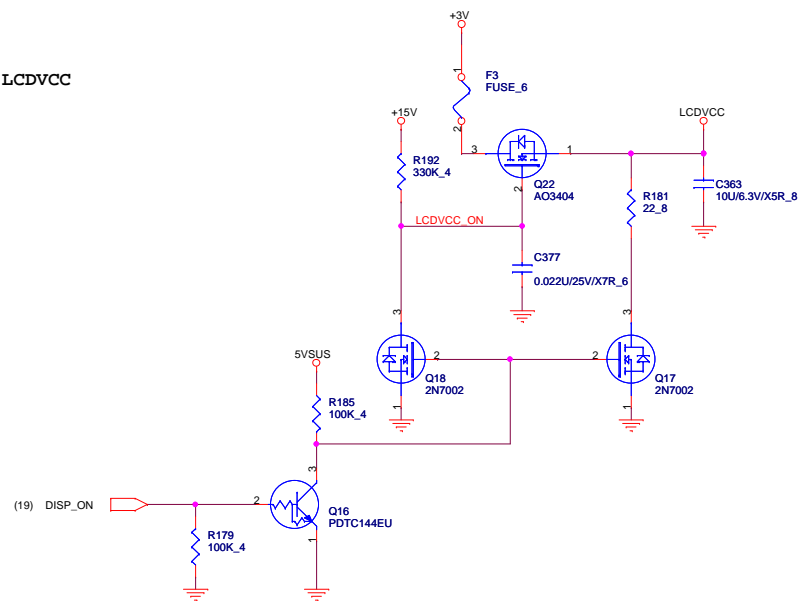
DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R



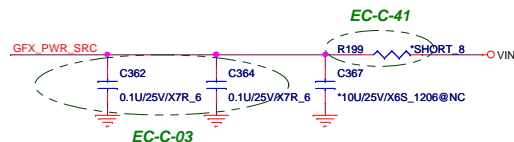
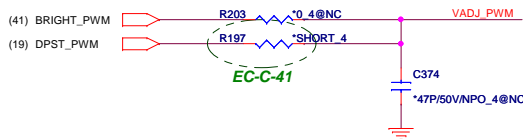
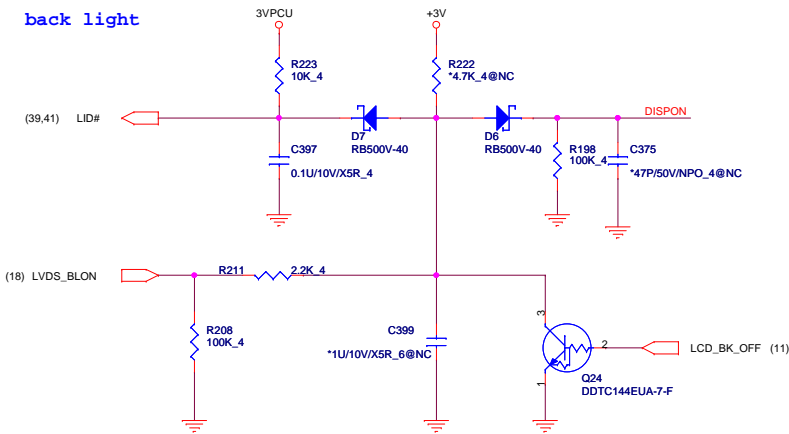
Designator	M9X-S2 and M93-S3	Park-S3
Ra	DNI	10K
Rb	0R/Short	51R
Rc	2.2K	DNI
Ca	2.2nF	68pF



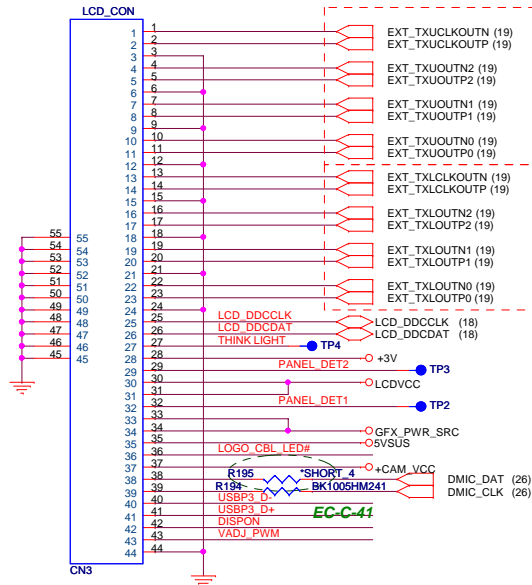
LCDVCC



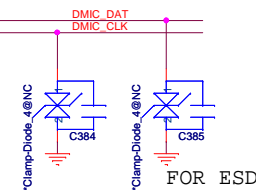
back light



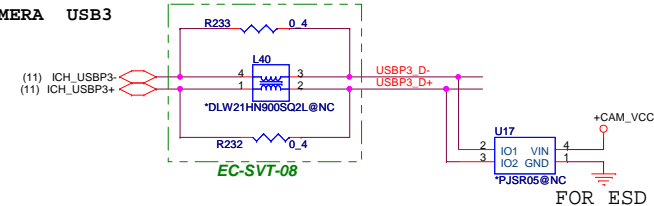
LCD_CON



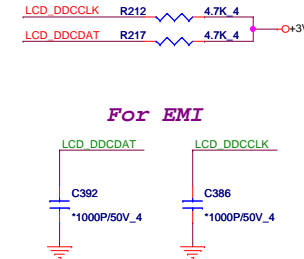
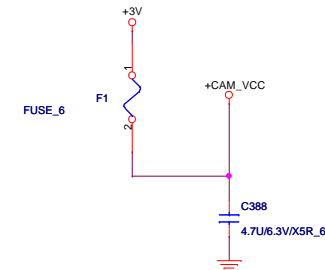
Address : A9H --Contrast
AAH --Backlight



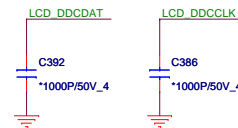
CAMERA USB3



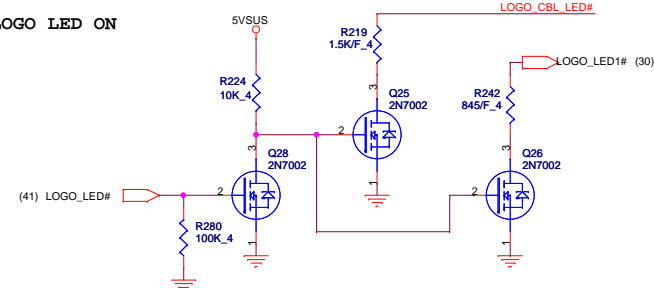
CAMERA VCC Control

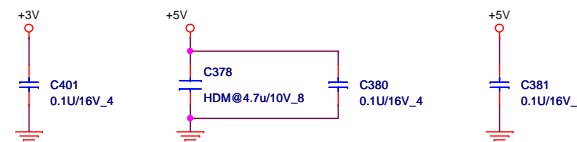
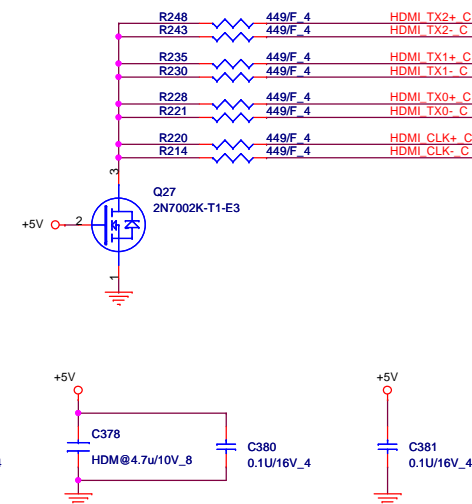
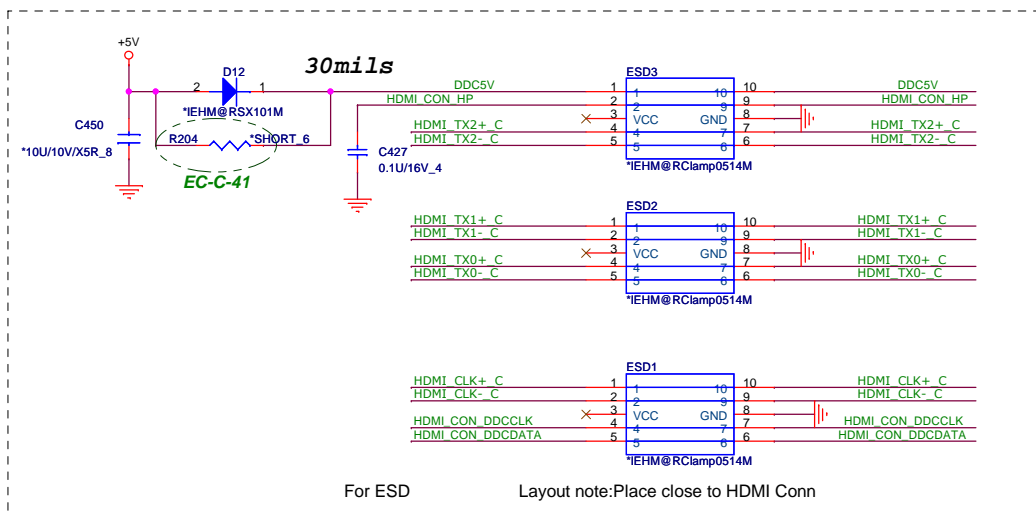
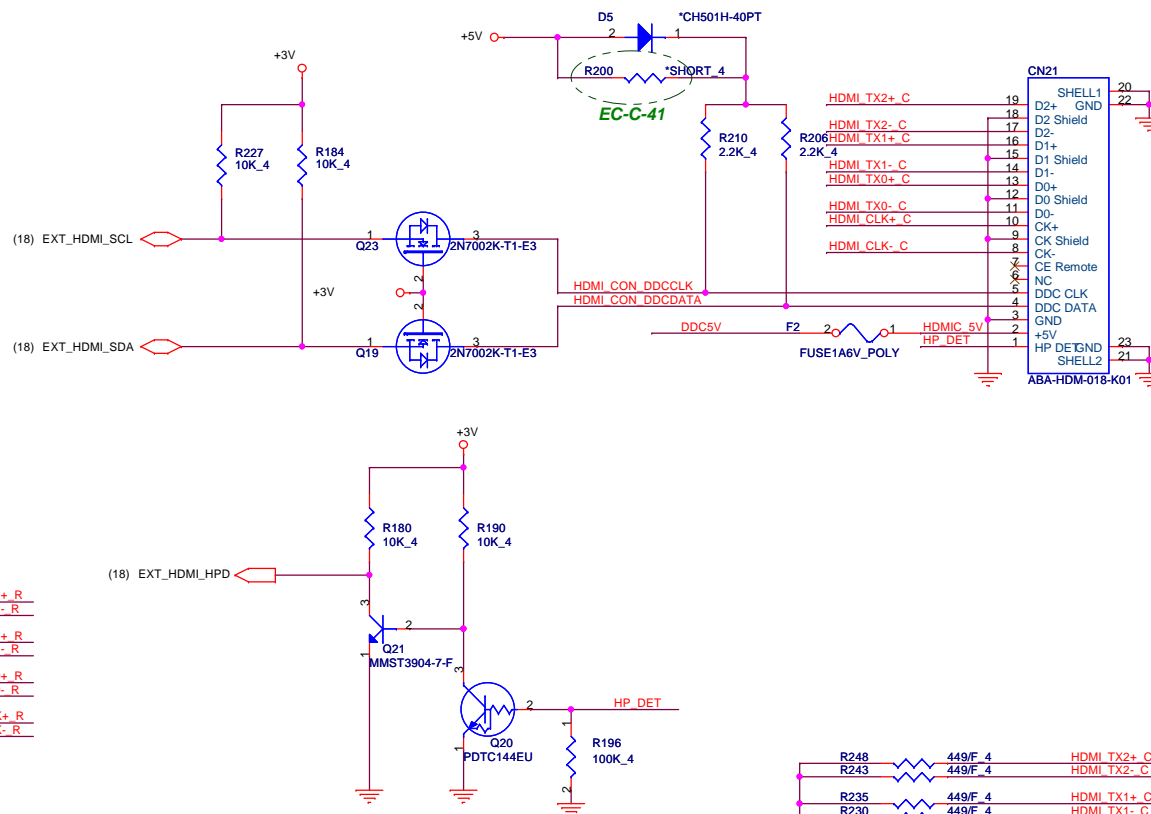
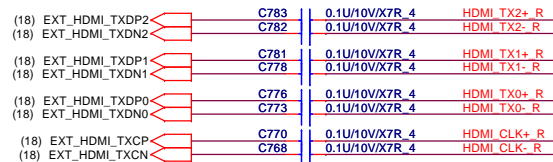
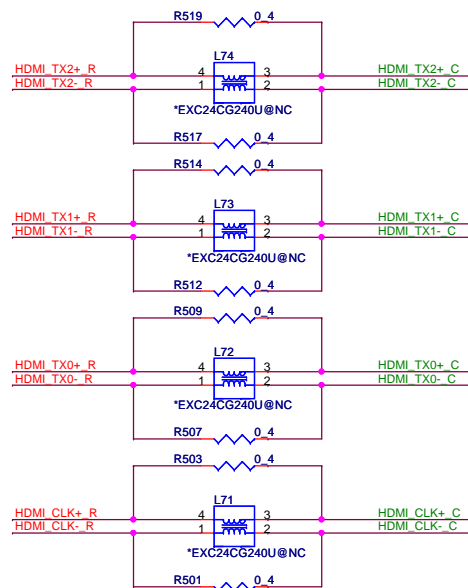


For EMI



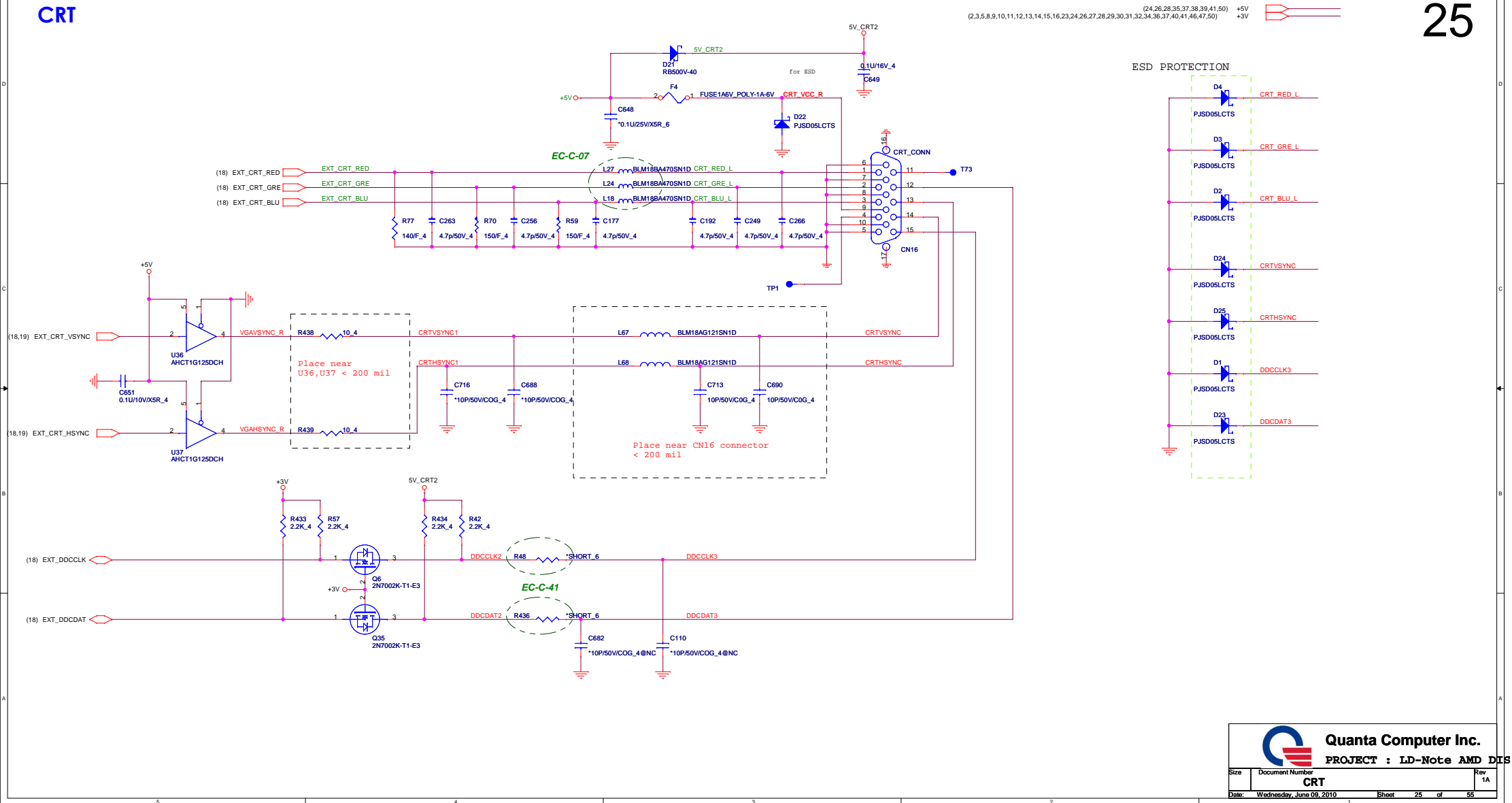
LOGO LED ON



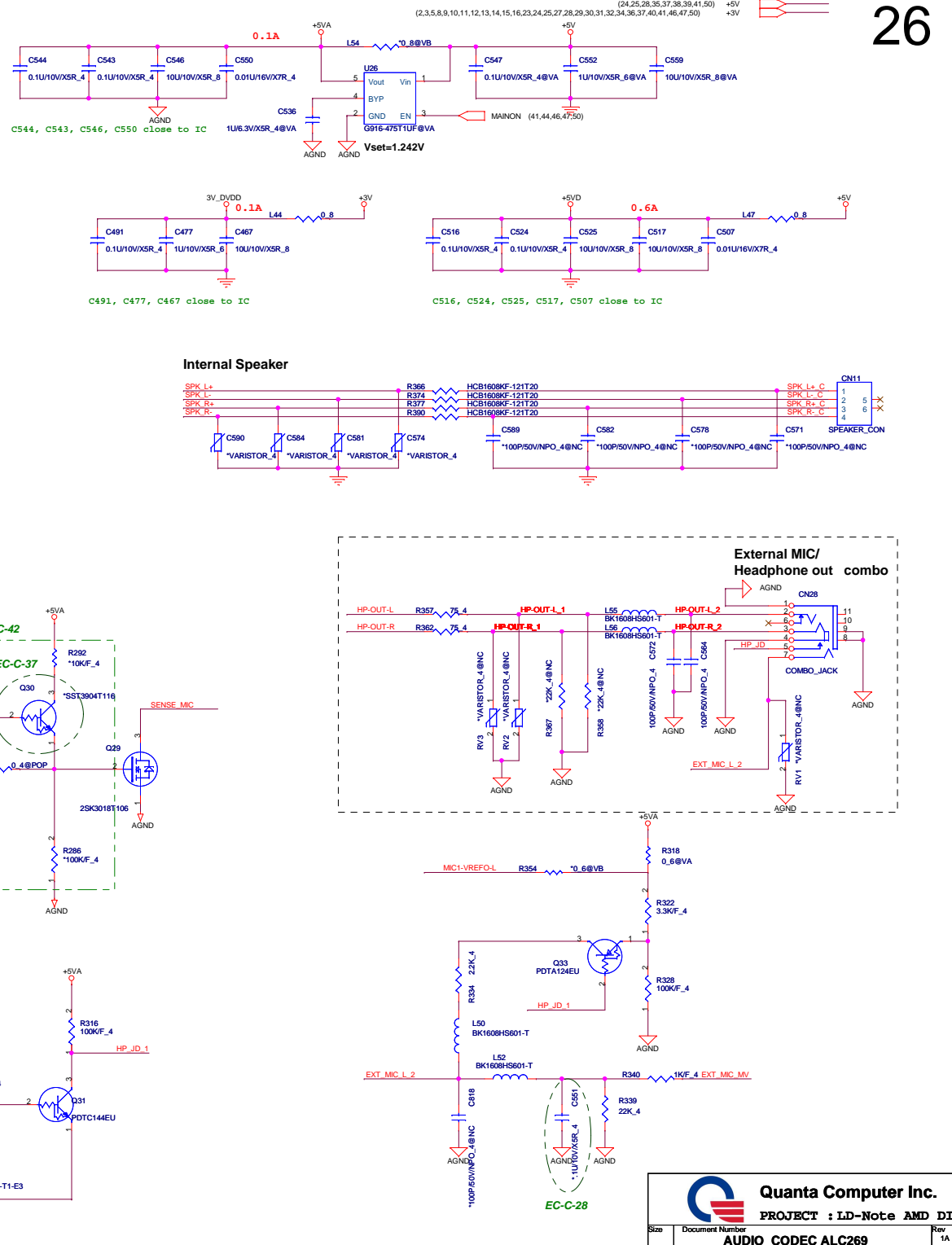
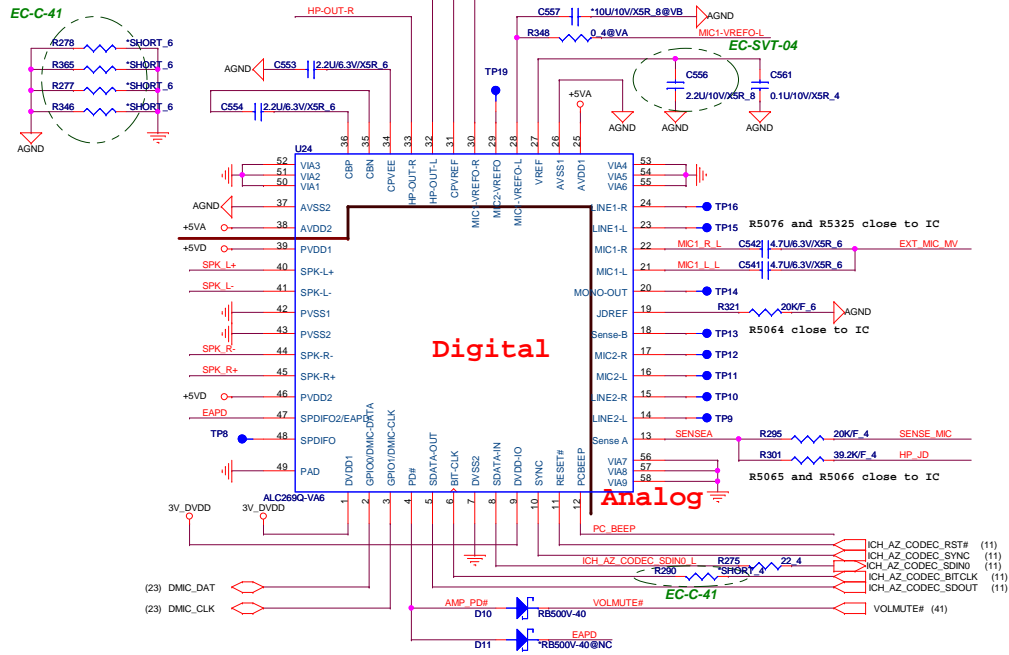


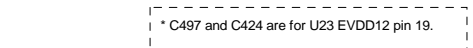
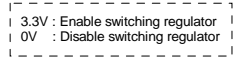
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PROJECT : LD-Note AMD DIS

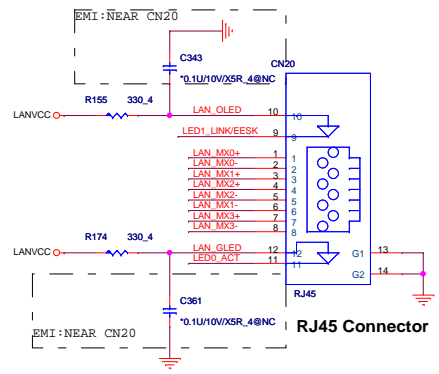


HDAudio Codec

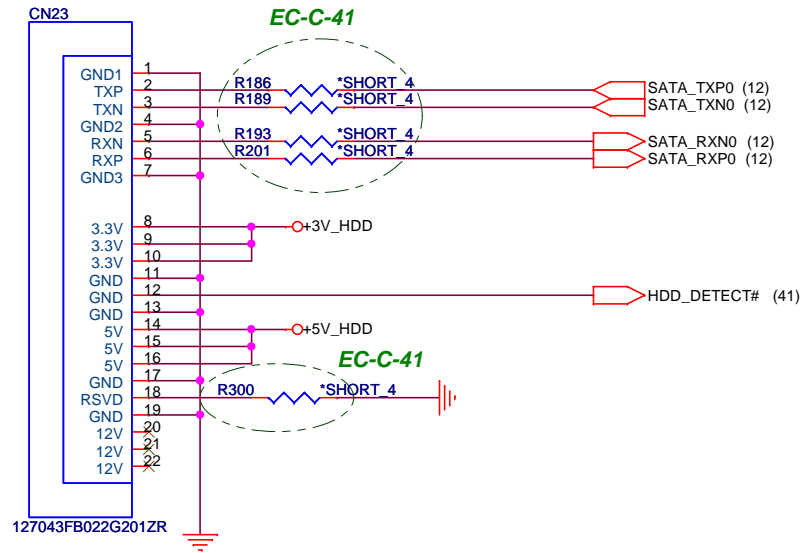




Place C473 ,C447 closed to U23 pins44,45.



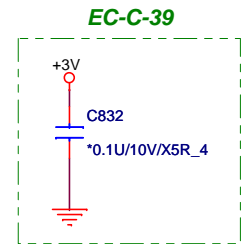
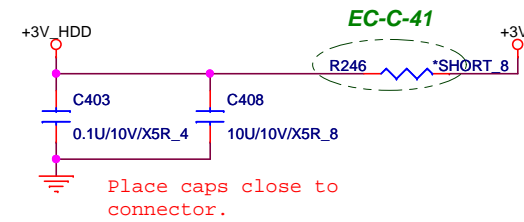
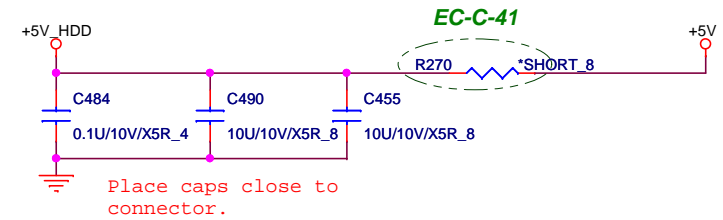
SATA HDD Connector.



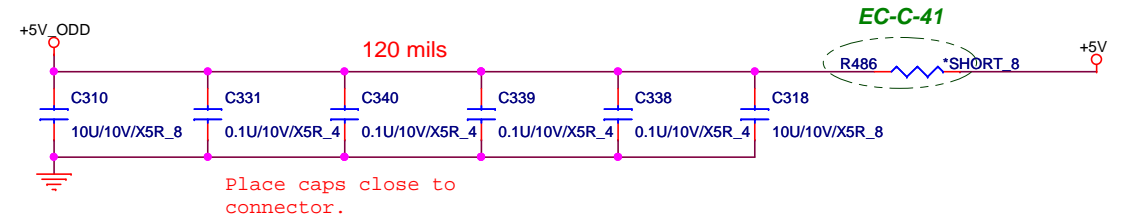
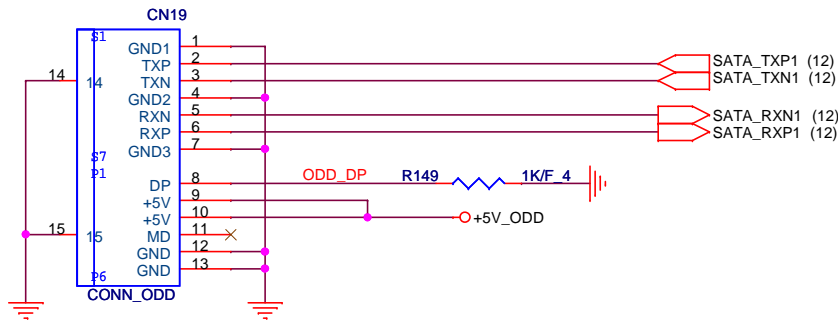
(2,3,5,8,9,10,11,12,13,14,15,16,23,24,25,26,27,29,30,31,32,34,36,37,40,41,46,47,50) +5V +3V



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ODD Connector



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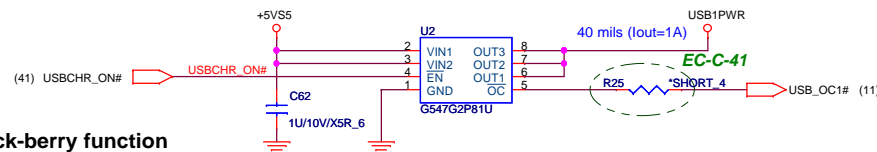
PROJECT :LD-Note AMD DIS

Size	Document Number	Rev
	SATA (HDD&CD_ROM)	1A
Date:	Wednesday, June 09, 2010	Sheet 28 of 55

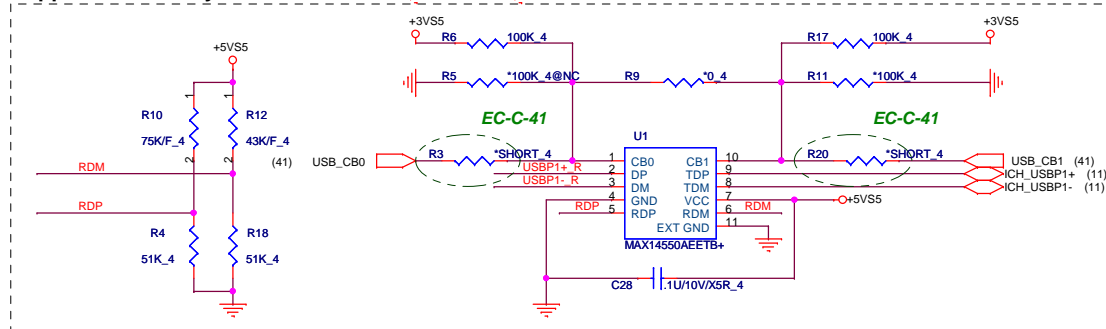
USBX1

29

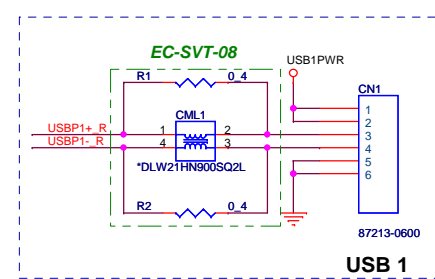
(30,50) +5VSS
(2,3,5,8,9,10,11,12,13,14,15,16,23,24,25,26,27,28,30,31,32,34,36,37,40,41,46,47,50) +3V
(5,10,11,12,13,14,32,50) +3VSS



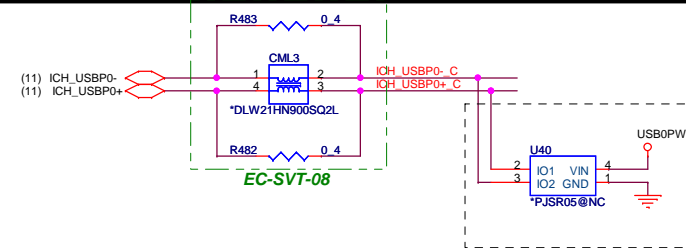
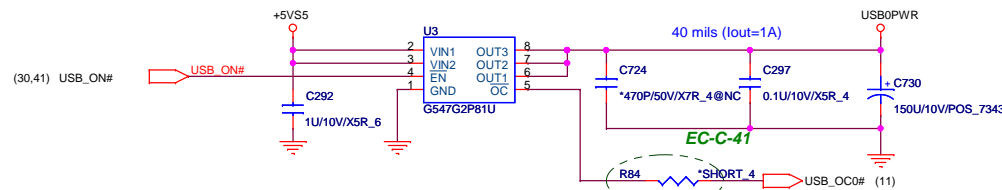
Support Black-berry function



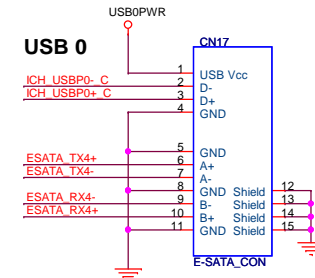
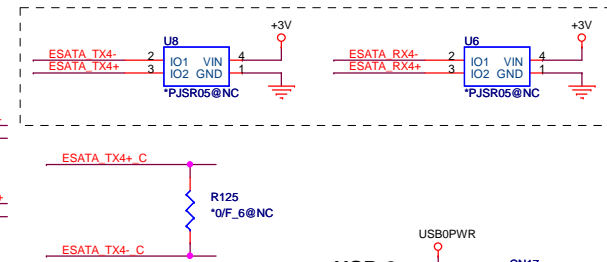
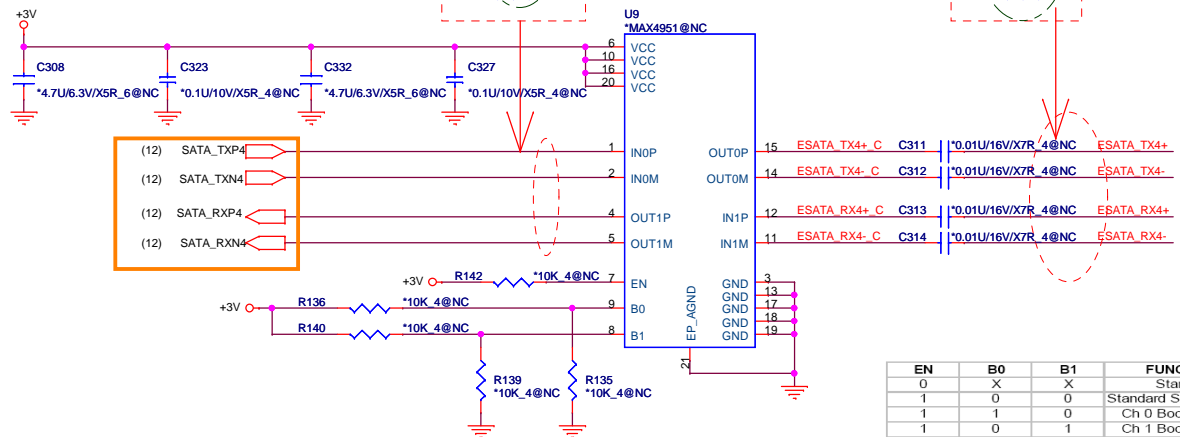
USB X1----> Wire to board conn



USB + E-SATA



E-SATA RE-DRIVER



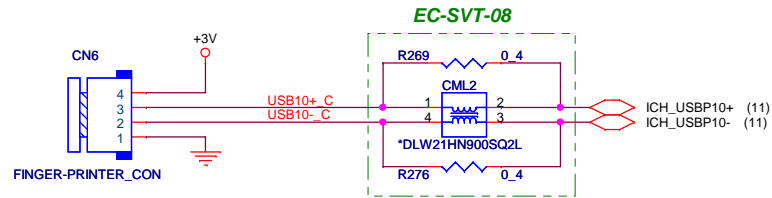
EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output



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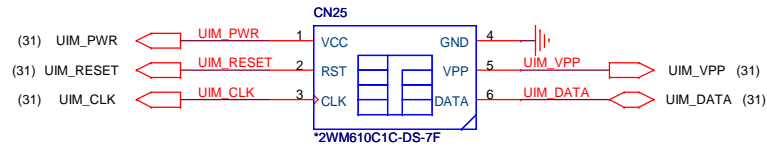
PROJECT :LD-Note AMD DIS

Finger Print

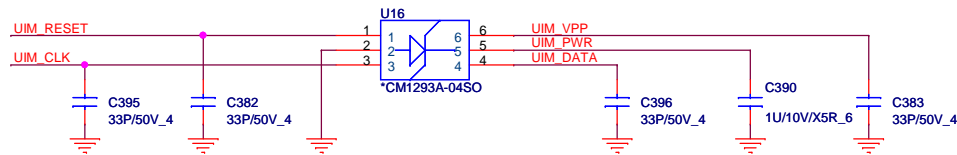


EC-C-30

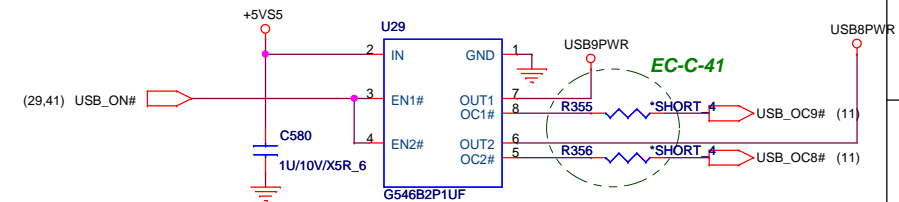
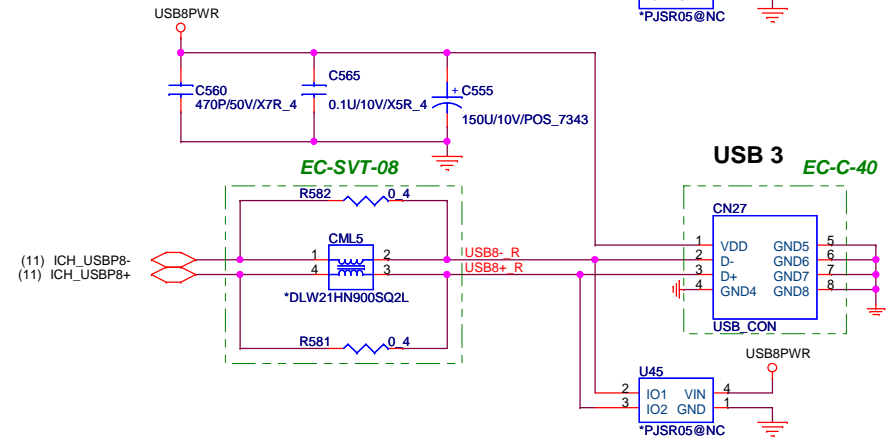
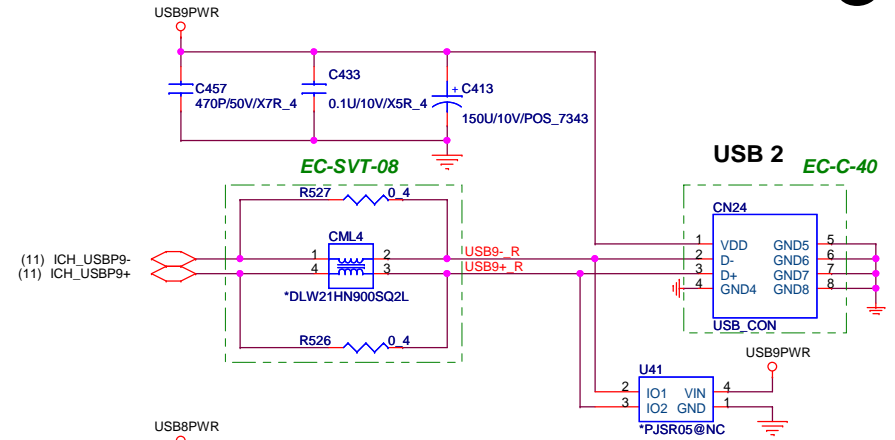
SIM Card CONN



Layout Note:
UIM_RESET, UIM_CLK, UIM_DATA routing as short as possible



FRONT LEDs



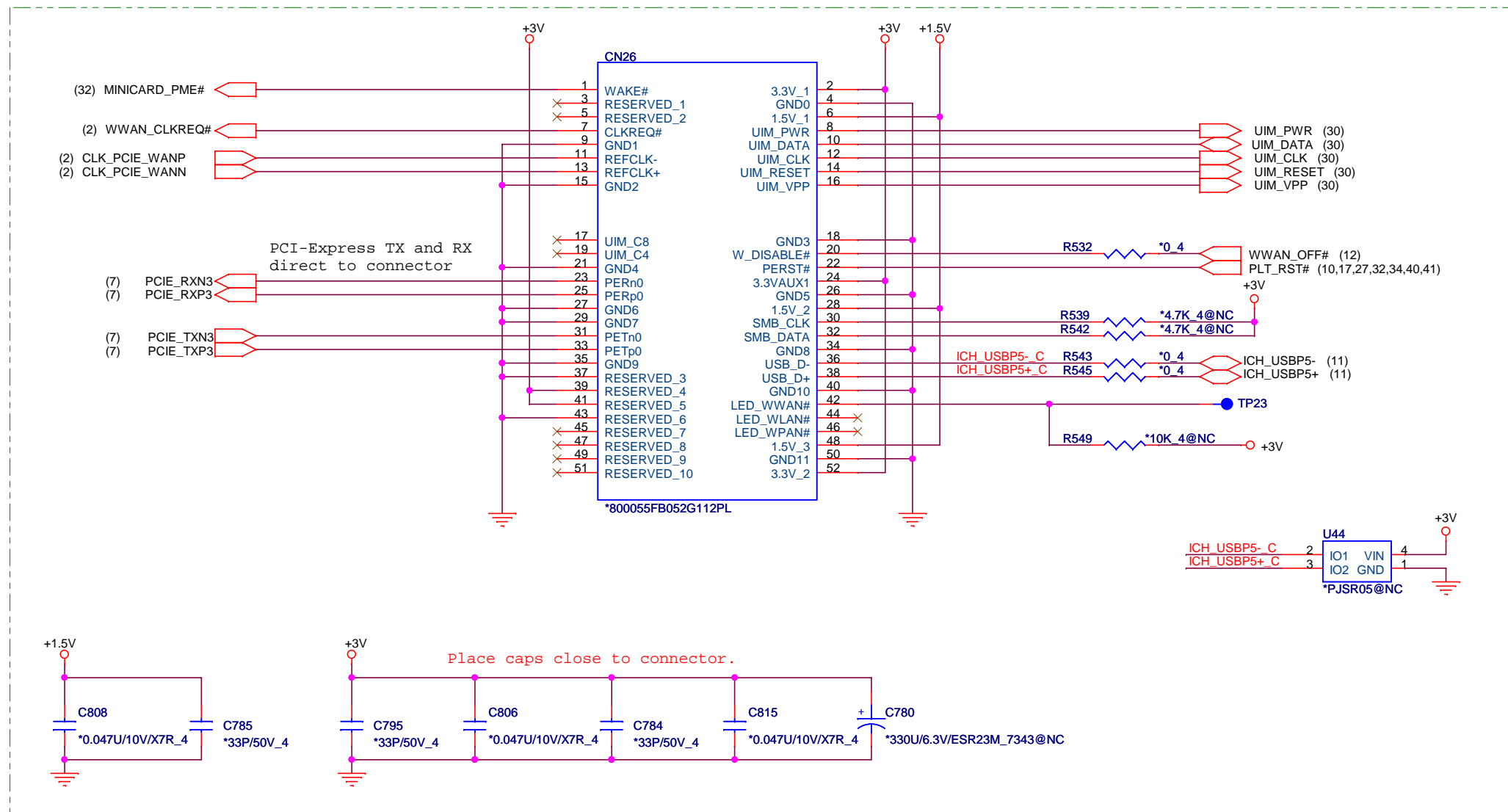
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PROJECT :LD-Note AMD DIS

Size	Document Number	Rev
	USB X2/SIM_CARD/LEDs/RF	1A
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MiniCard WWAN connector

EC-C-30



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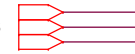
PROJECT :LD-Note AMD DIS

Size	Document Number	Rev
	MINI-Card (UWB, WWAN)	1A
Date:	Wednesday, June 09, 2010	Sheet 31 of 55

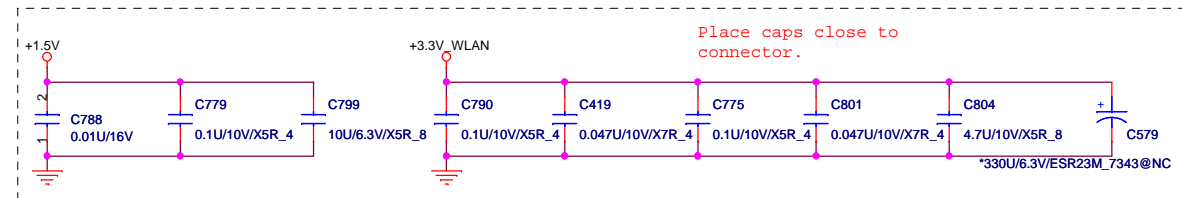
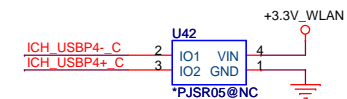
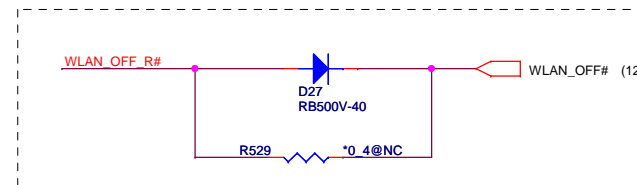
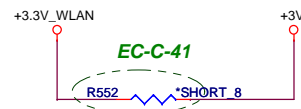
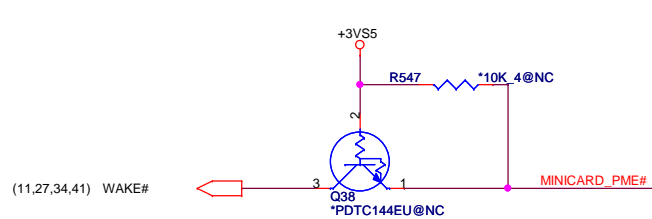
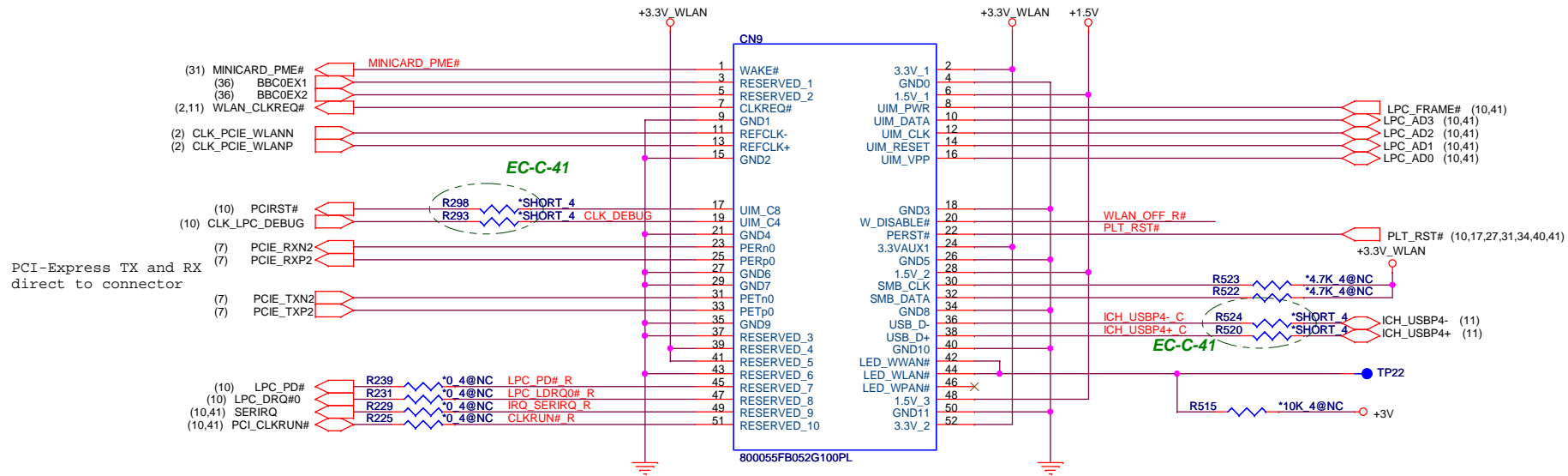
MiniCard WLAN/WiMAX connector

(2,3,5,8,9,10,11,12,13,14,15,16,23,24,25,26,27,28,29,30,31,34,36,37,40,41,46,47,50)

+3V
(5,10,11,12,13,14,29,50)
+3VS5
(3,8,31,34,50)
+1.5V



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PROJECT :LD-Note AMD DIS

Size Document Number **MINI-Card (WLAN)** Rev 1A

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Left NC if Pin23
connected to XD-D4

CARD READER

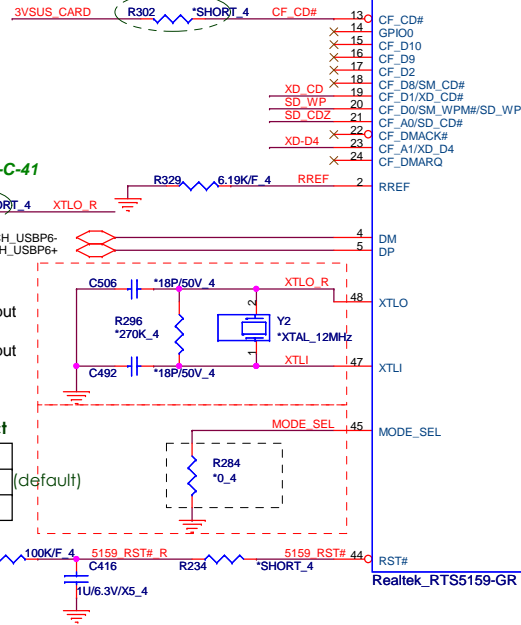
For external 12Mhz clock input
pin13 floating
For external 48Mhz clock input
pin13 pull high

Card Reader Model Select

Pin 45	R20
RTS5159-GR	0 ohm
RTS5158-GR	N.C

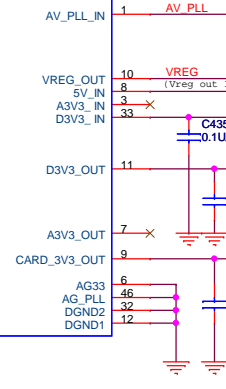
(default)

EC-C-41



0515 EMI Changes

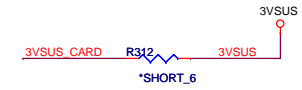
XD_CLE/CF_D3	43	XD-CLE
XD_CE#/CF_D11	42	XD-CE#
XD_ALE/CF_D4	41	XD-ALE
CF_CD#	13	
CF_D10	14	
CF_D9	15	
CF_D2	16	
CF_D8/SM_CD#	17	
CF_D1/XD_CD#	18	
CF_D0/SM_WP#/#SD_WP	19	
CF_A0/SD_CD#	20	
CF_DMACK#	21	
CF_A1/XD_D4	22	
CF_DMARQ	23	
SD_CMD	36	SD CMD
SD_DAT5/XD_D0/CF_D14	35	XD-D0
SD_CLK/XD_D1/MS_CLK/CF_D7	34	SP11
SD_DAT6/XD_D7/MS_D3/CF_D15	31	SP10
CF_CS0#	30	SP9
MS_INS#/CF_IORD#	29	SP8
SD_DAT7/XD_D2/MS_D2/CF_IOWR#	28	SP7
SD_DAT0/XD_D6/MS_D0/CF_RST#	27	SP6
SD_DAT1/XD_D3/MS_D1/CF_IORDY	26	SP5
XD_D5/MS_BS/CF_A2	25	



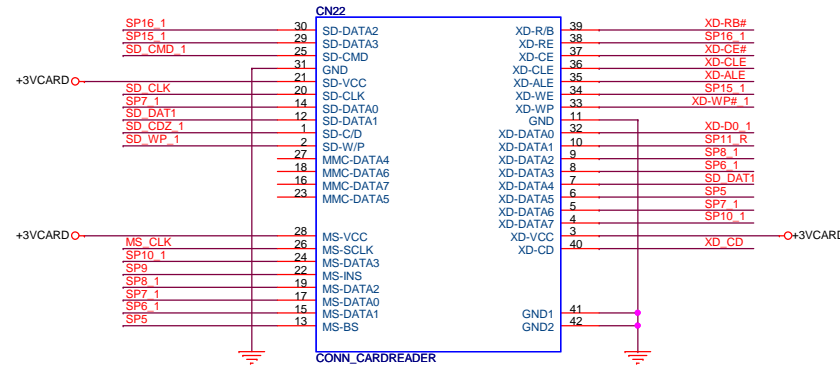
(30,34,41,46,47,49,50) 3VSUS

Note:

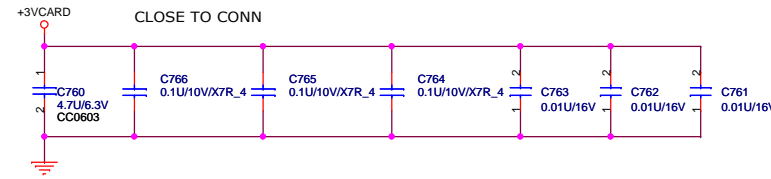
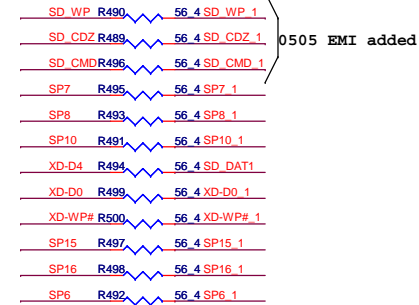
SD/MMC	MS	XD
SP0		XD_CD#
SP1	SD_WP	
SP2	SD_CD#	
SP3		XD D4
SP4	MS_BS	XD D5
SP5	MS_D1	XD D3
SP6	SD_DAT0	MS D0
SP7	SD DAT7	XD D2
SP8	MS_INS#	
SP9	SD DAT6	MS D3
SP10	SD DAT5	XD D1
SP11	SD DAT4	XD WP#
SP12	XD_R/#	
SP13	XD D0	
SP14	XD D1	
SP15	XD D2	
SP16	XD D3	
SP17	XD D4	
SP18	XD D5	
SP19	XD D6	



7 in 1 Socket(MS, MS PRO,SD, MMC, xD)



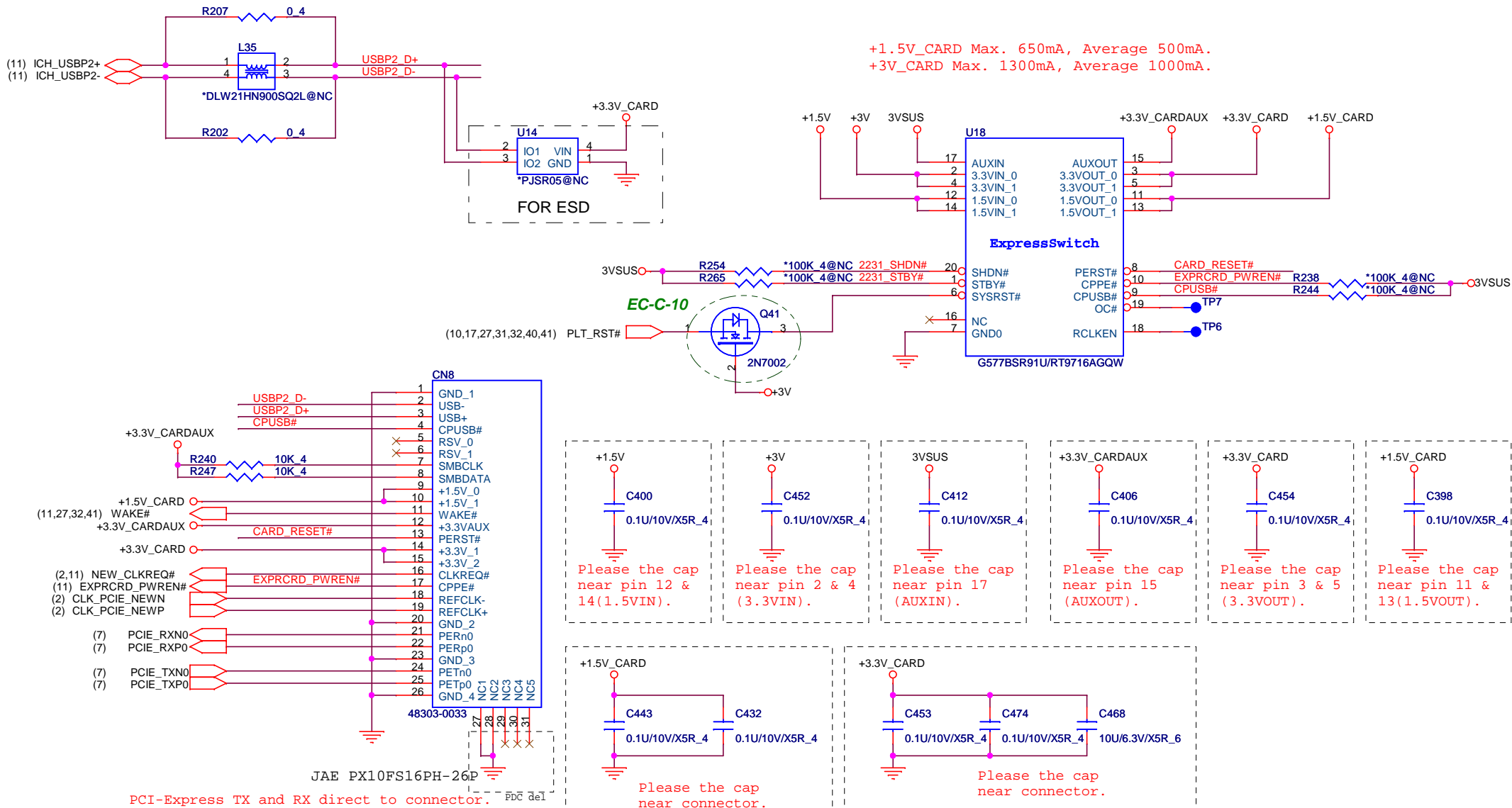
0616 Add 10K to GND for +3VCARD discharge in Ver.B



Express Card

(2,3,5,8,9,10,11,12,13,14,15,16,23,24,25,26,27,28,29,30,31,32,36,37,40,41,46,47,50) +3V
(3,8,31,32,50) +1.5V
(30,33,41,46,47,49,50) 3VSUS

34

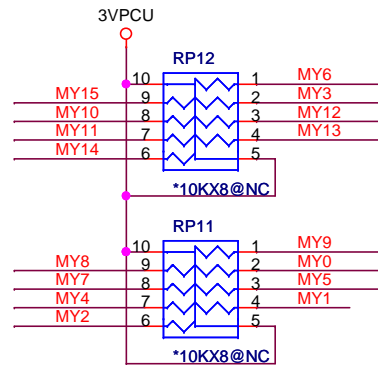
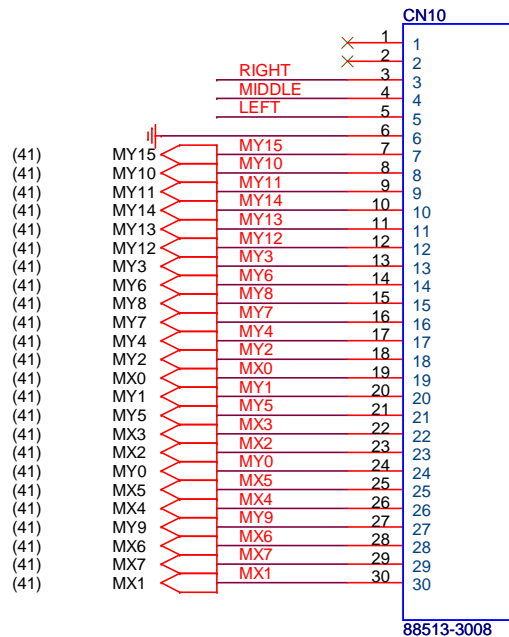


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PROJECT :LD-Note AMD DIS

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	Express Card	1A
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KEYBOARD

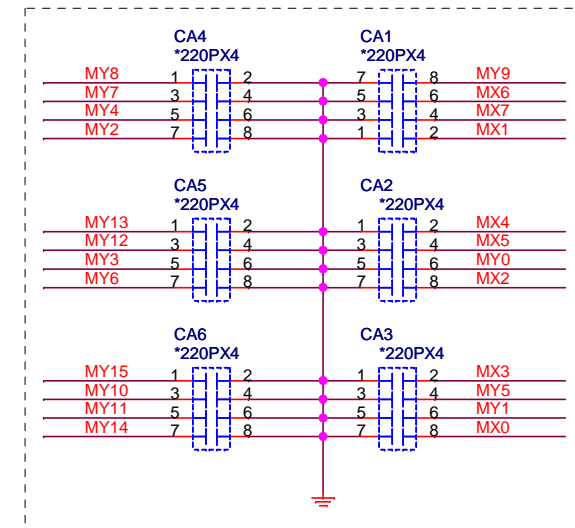
KEYBOARD connector



(24,25,26,28,37,38,39,41,50) +5V
(10,23,27,39,41,43,44,45,46,47,48,50) 3VPCU

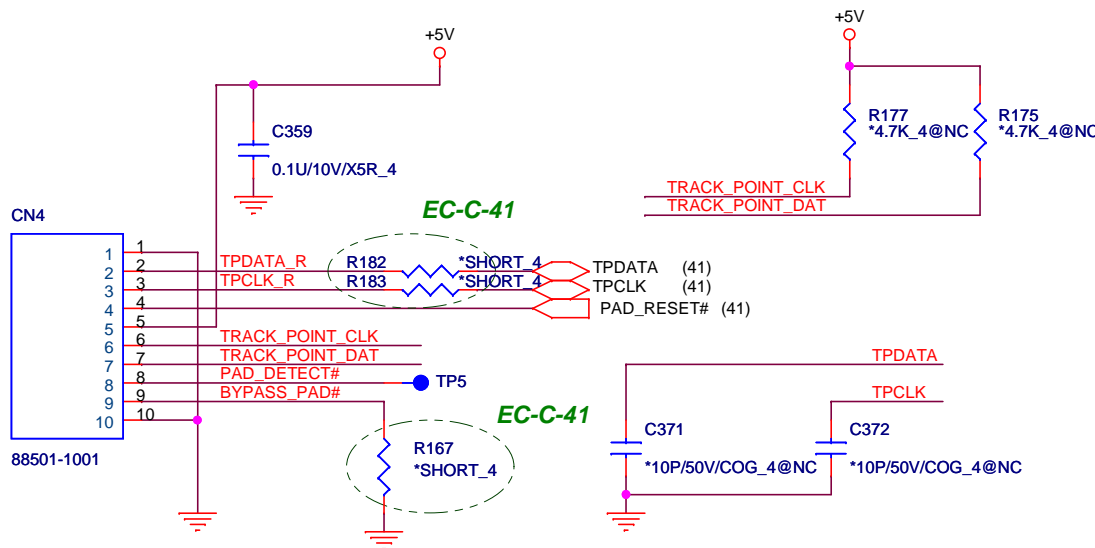


35

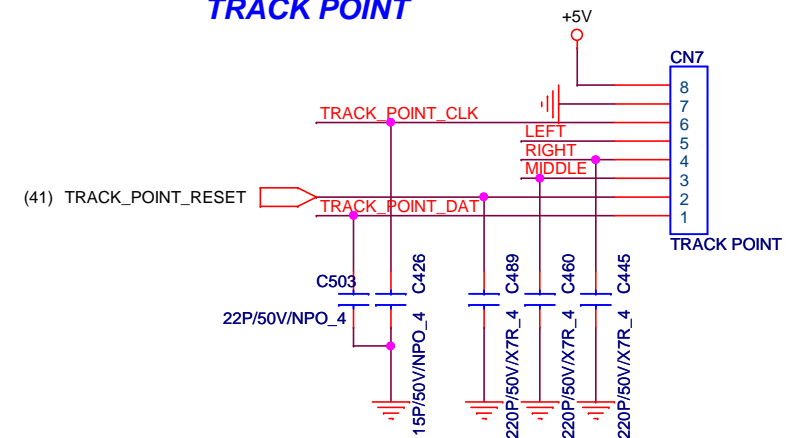



For EMI request

Touch pad



TRACK POINT





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PROJECT :LD-Note AMD DIS

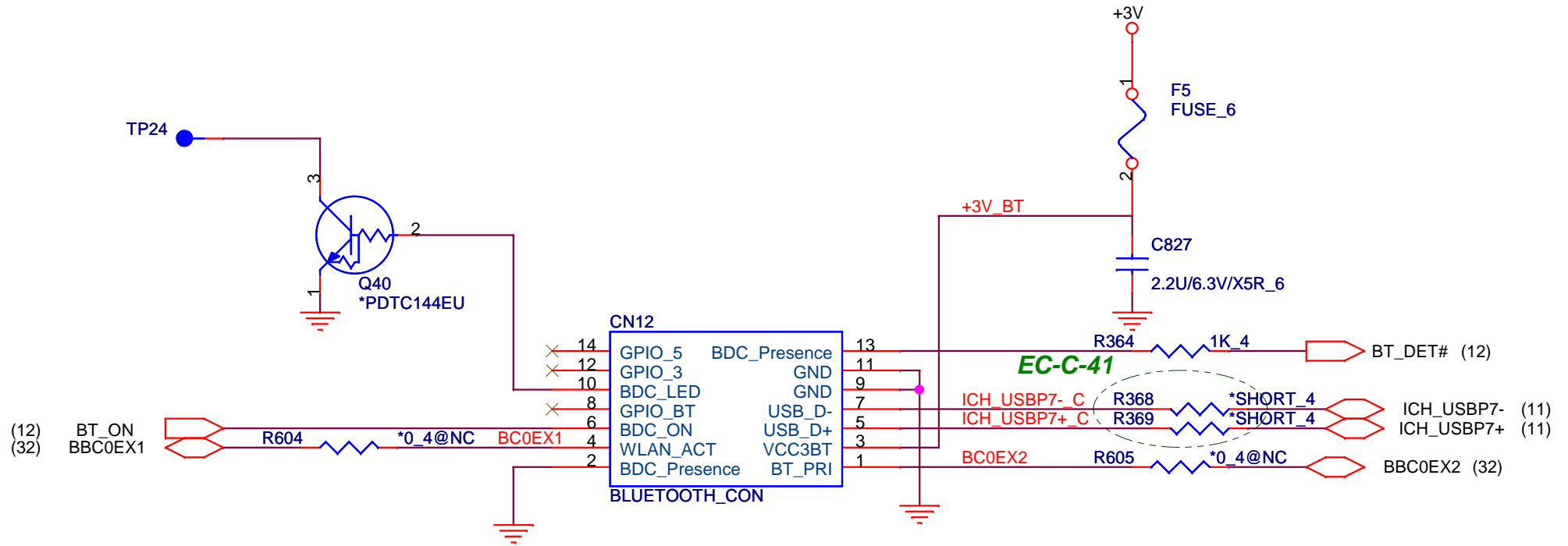
Size	Document Number	Rev
	K/B, T/P	1A
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BLUETOOTH

(2,3,5,8,9,10,11,12,13,14,15,16,23,24,25,26,27,28,29,30,31,32,34,37,40,41,46,47,50)

+3V

36

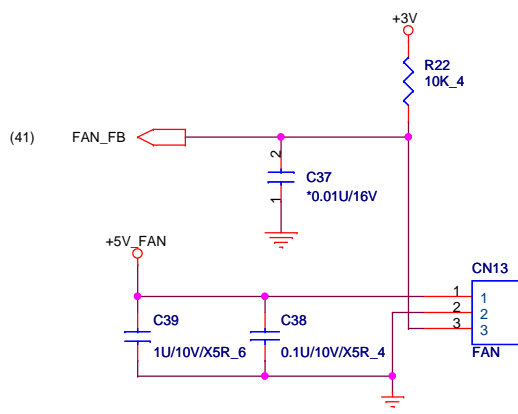
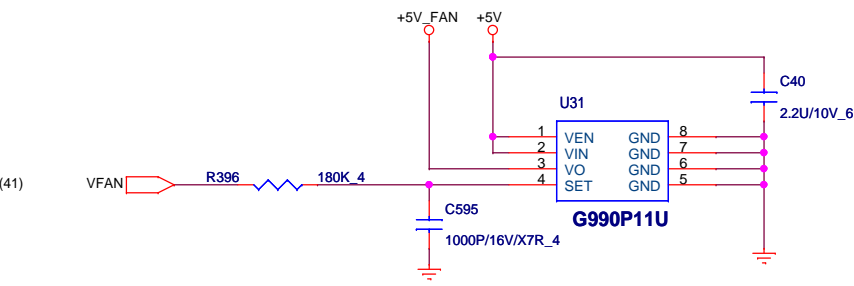


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PROJECT :LD-Note AMD DIS

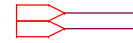
Size	Document Number B/T	Rev 1A
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FAN CONTROL

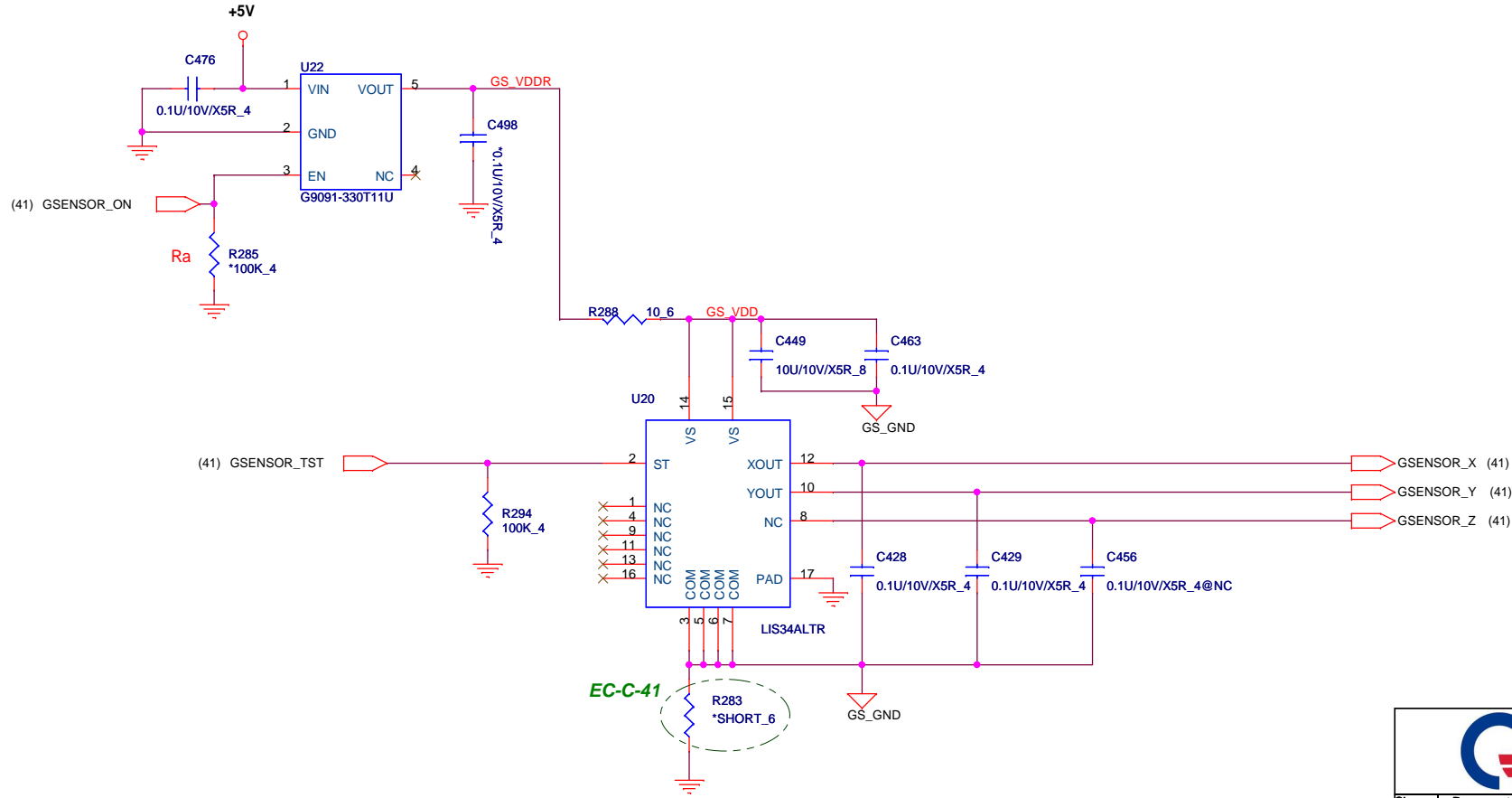



G-SENSOR (3-Axial)

(2,3,5,8,9,10,11,12,13,14,15,16,23,24,25,26,27,28,29,30,31,32,34,36,37,40,41,46,47,50) +3V
(23,44,45,48,50) +15V



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Quanta Computer Inc.
PROJECT : LD-Note AMD DIS

Size	Document Number	Rev
	G-SENSOR	1A
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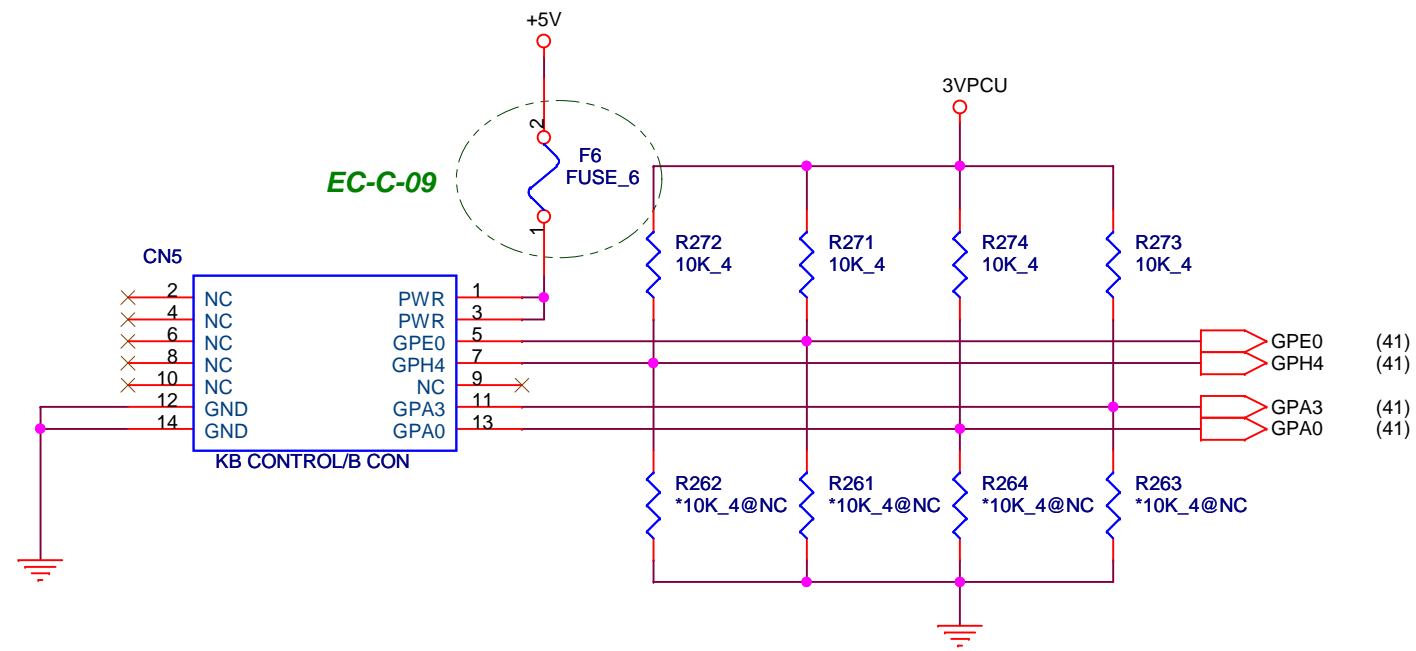
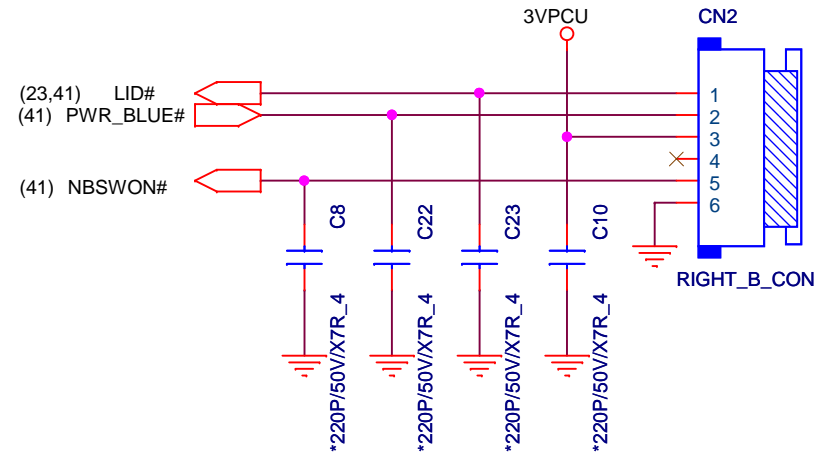
FFC TO B LED RIGHT SIDE CONNECTOR


(10,23,27,35,41,43,44,45,46,47,48,50)

3VPCU



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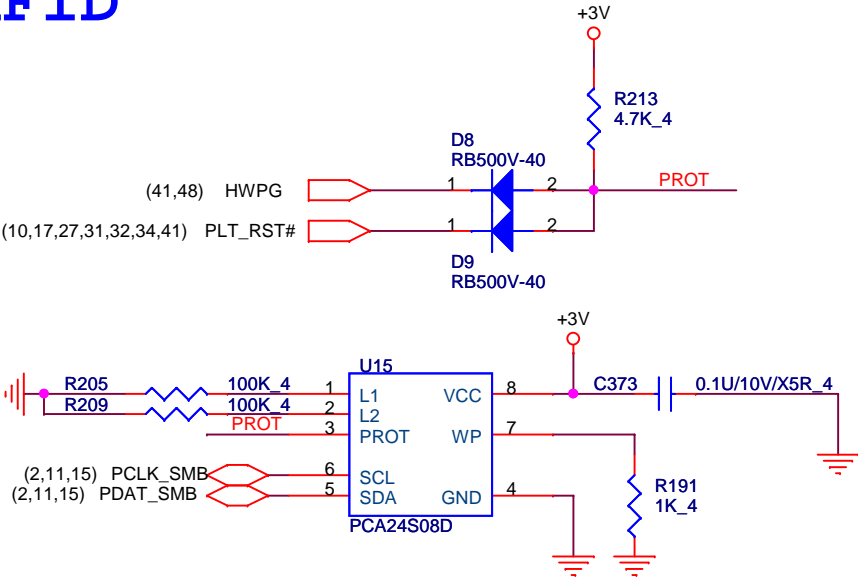


Quanta Computer Inc.
PROJECT :LD-Note AMD DIS

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	B TO B CON	1A
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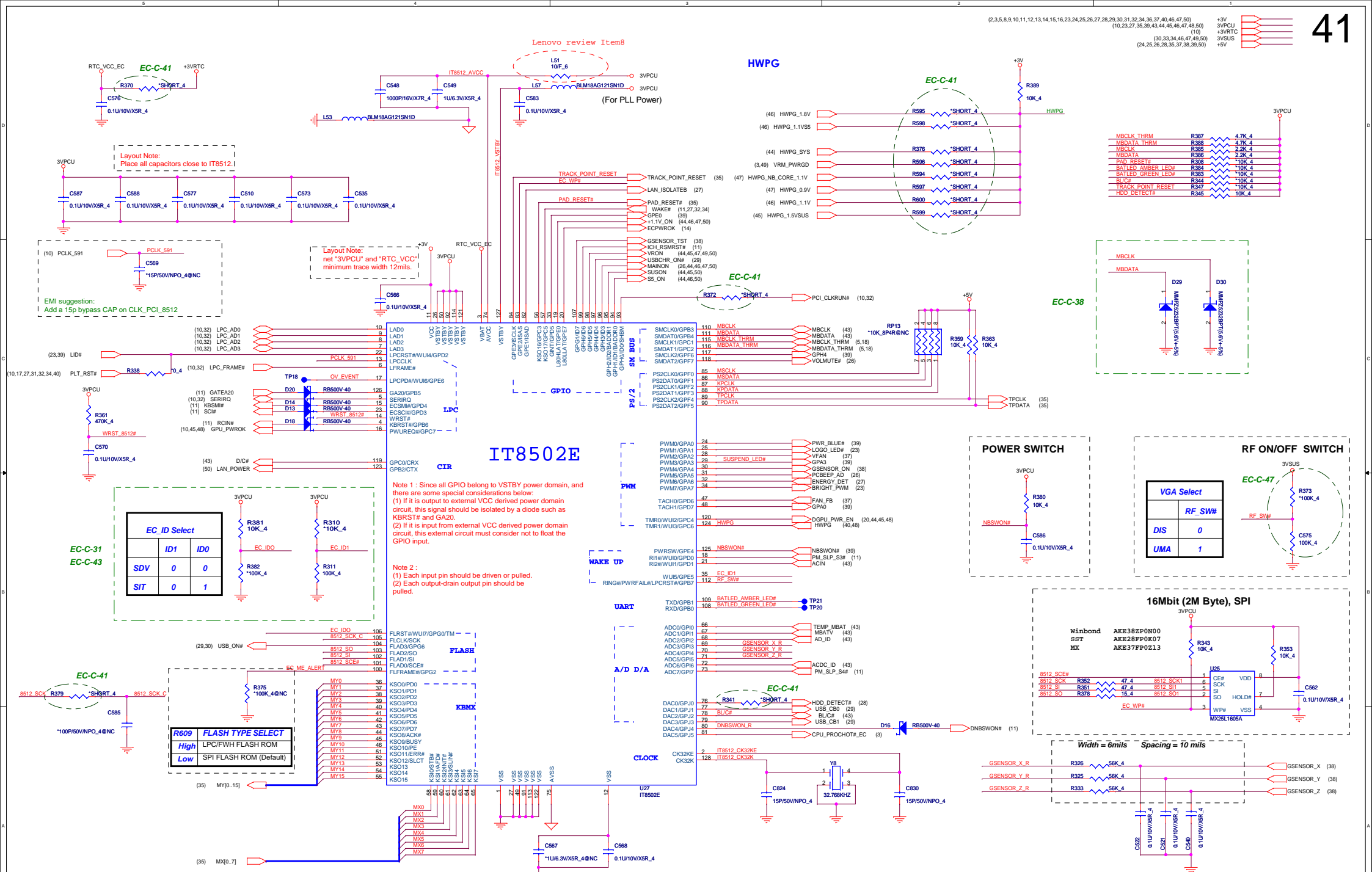
RFID

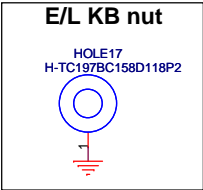
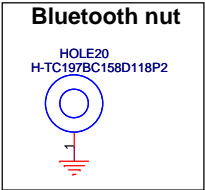
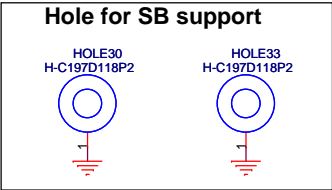
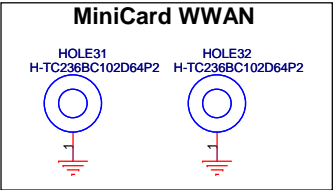
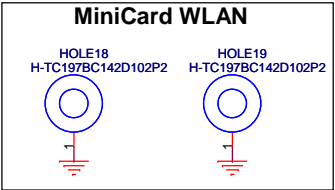


Quanta Computer Inc.

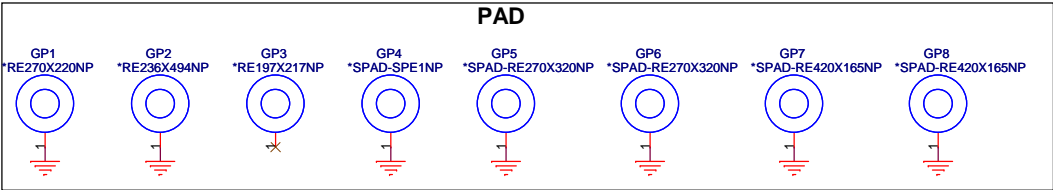
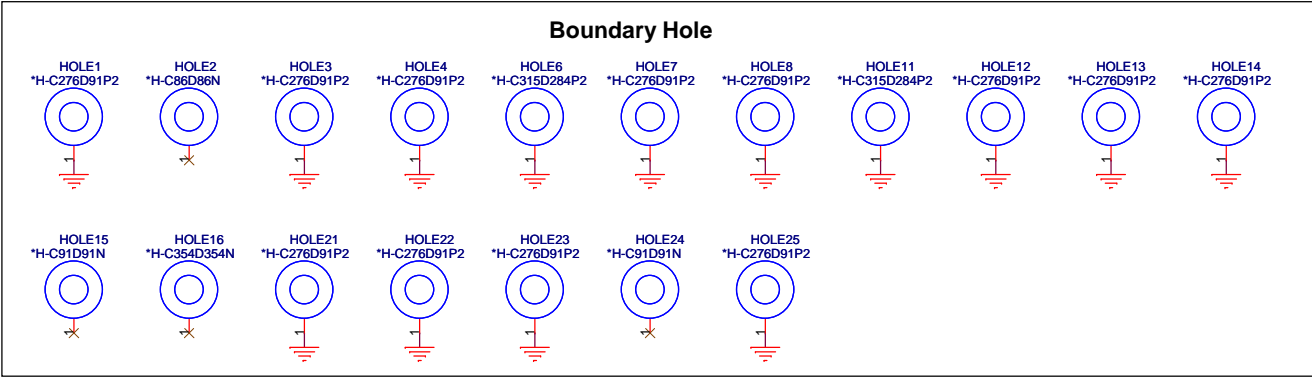
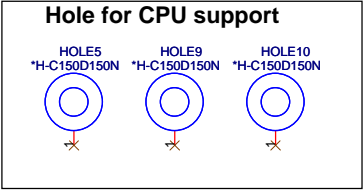
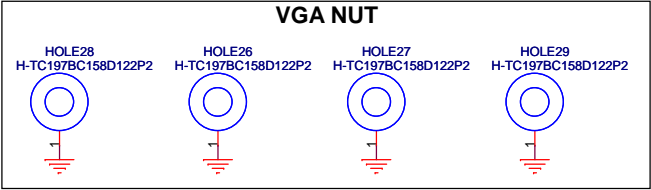
PROJECT :LD-Note AMD DIS

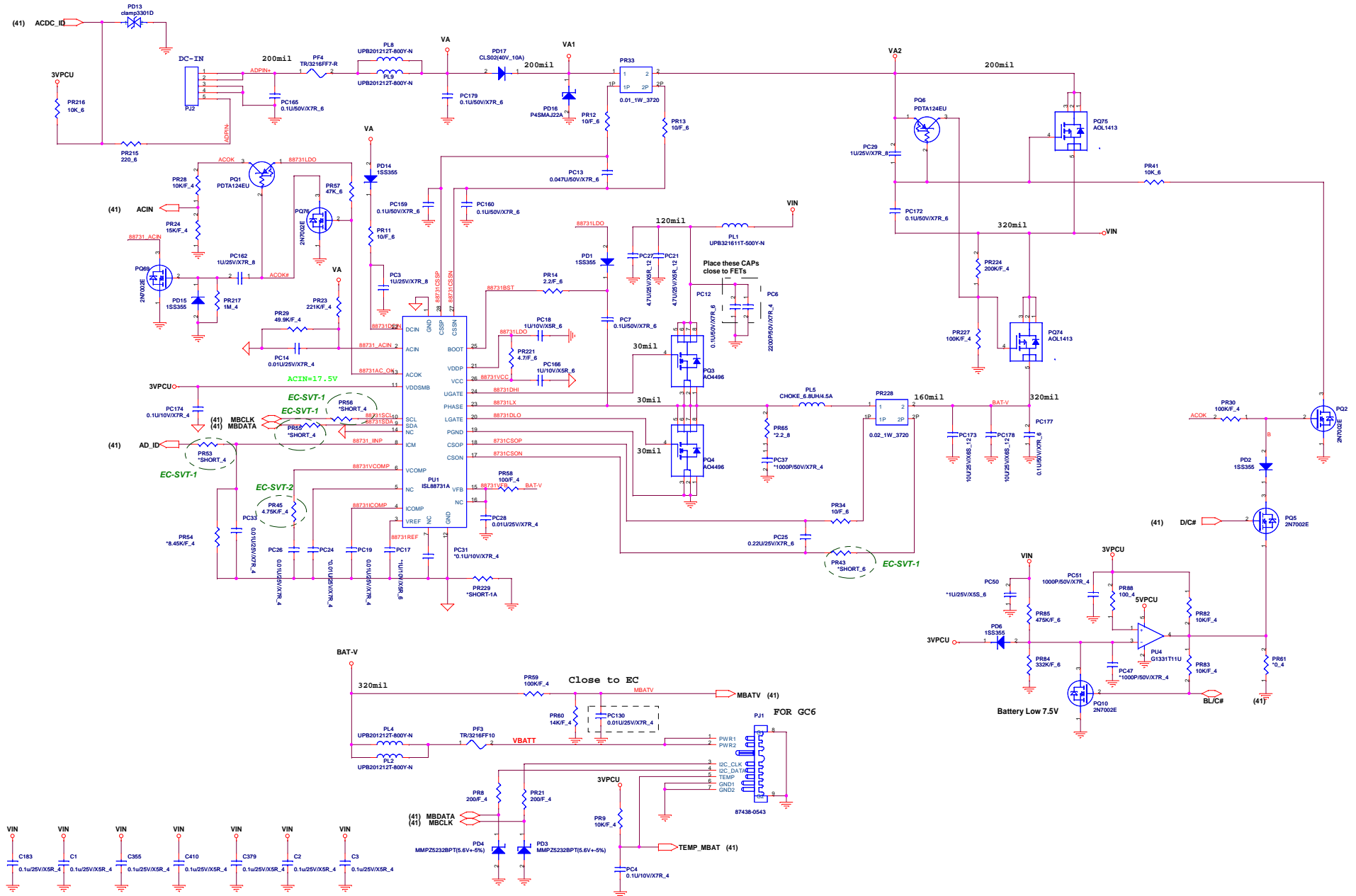
Size	Document Number	Rev
	RFID EEPROM	1A
Date:	Wednesday, June 09, 2010	Sheet 40 of 55



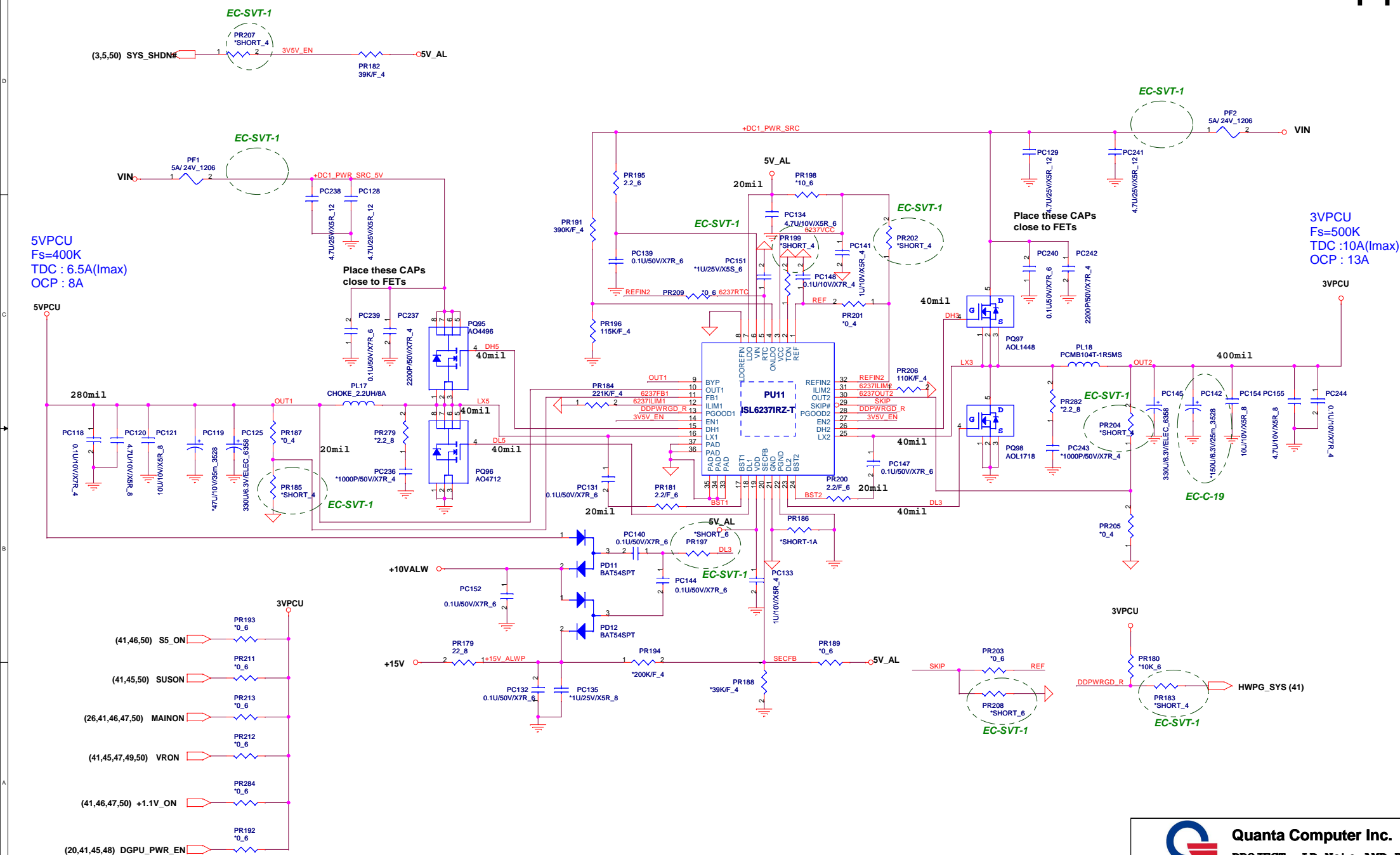


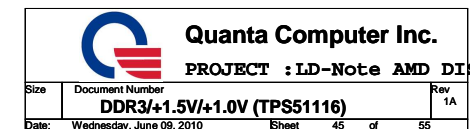
42

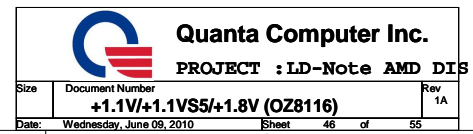


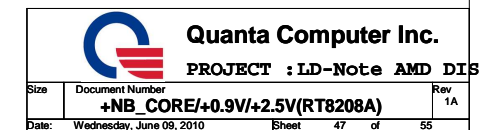
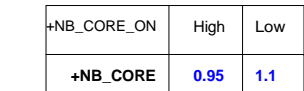


EMI Bypass capacitor



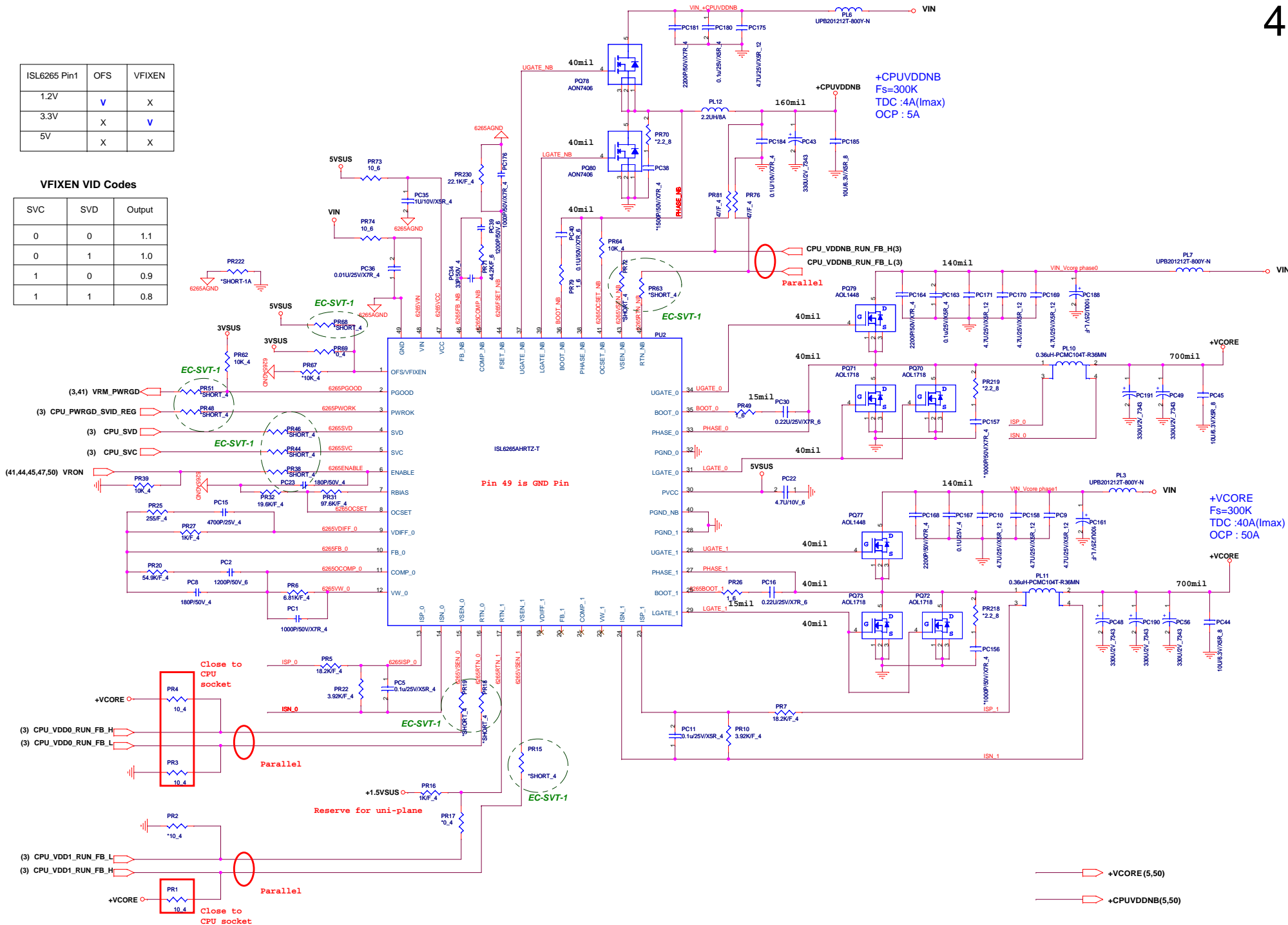




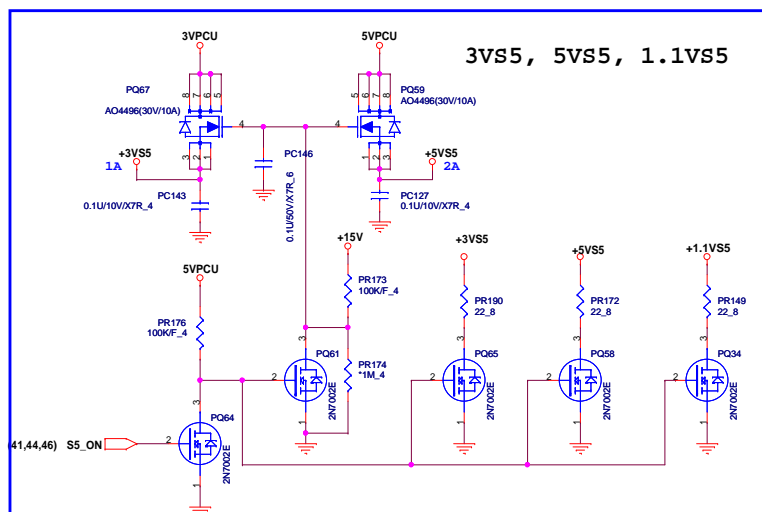
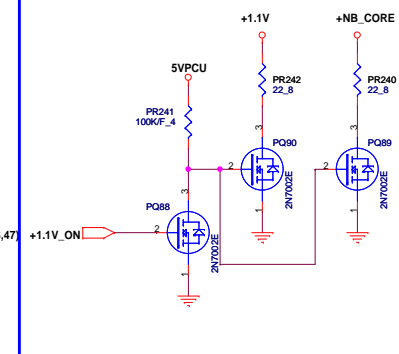
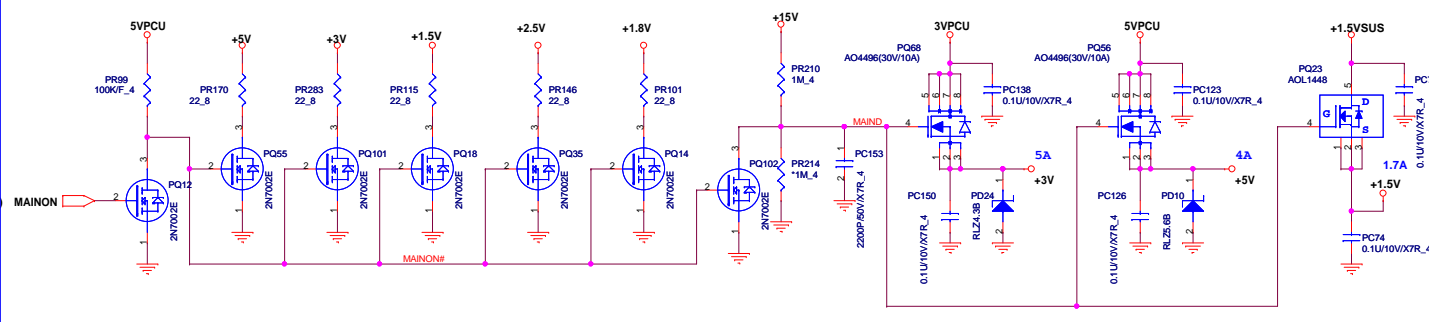
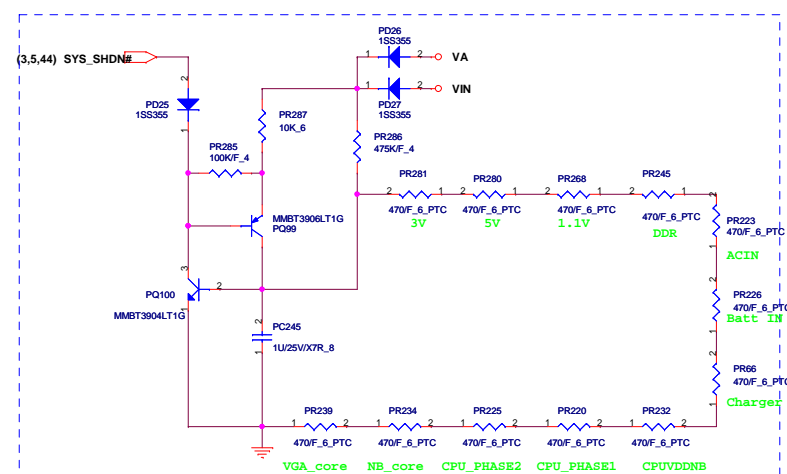
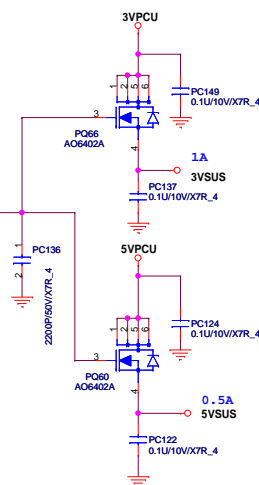
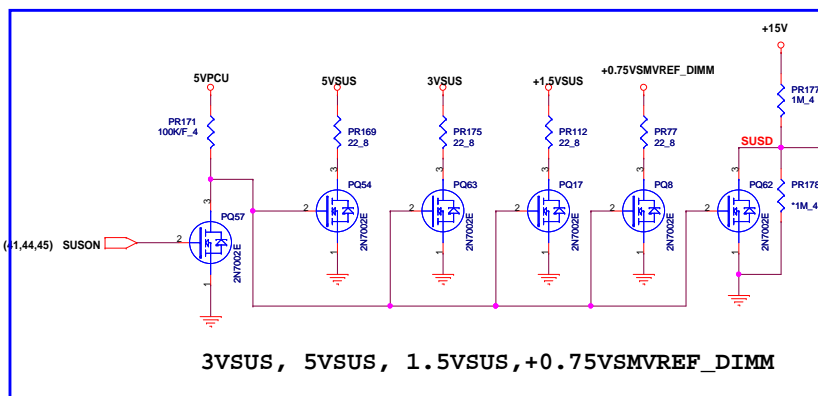


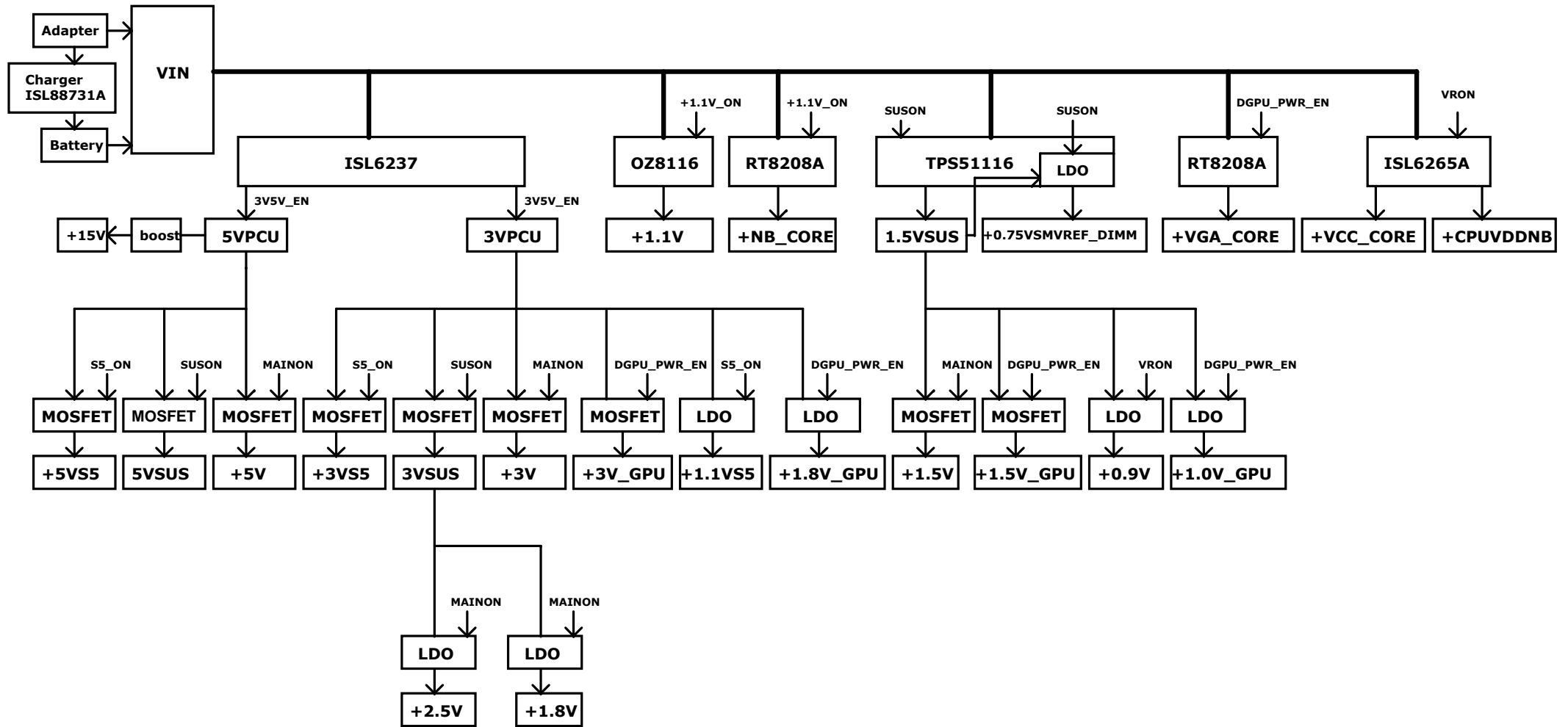
VFIXEN VID Codes

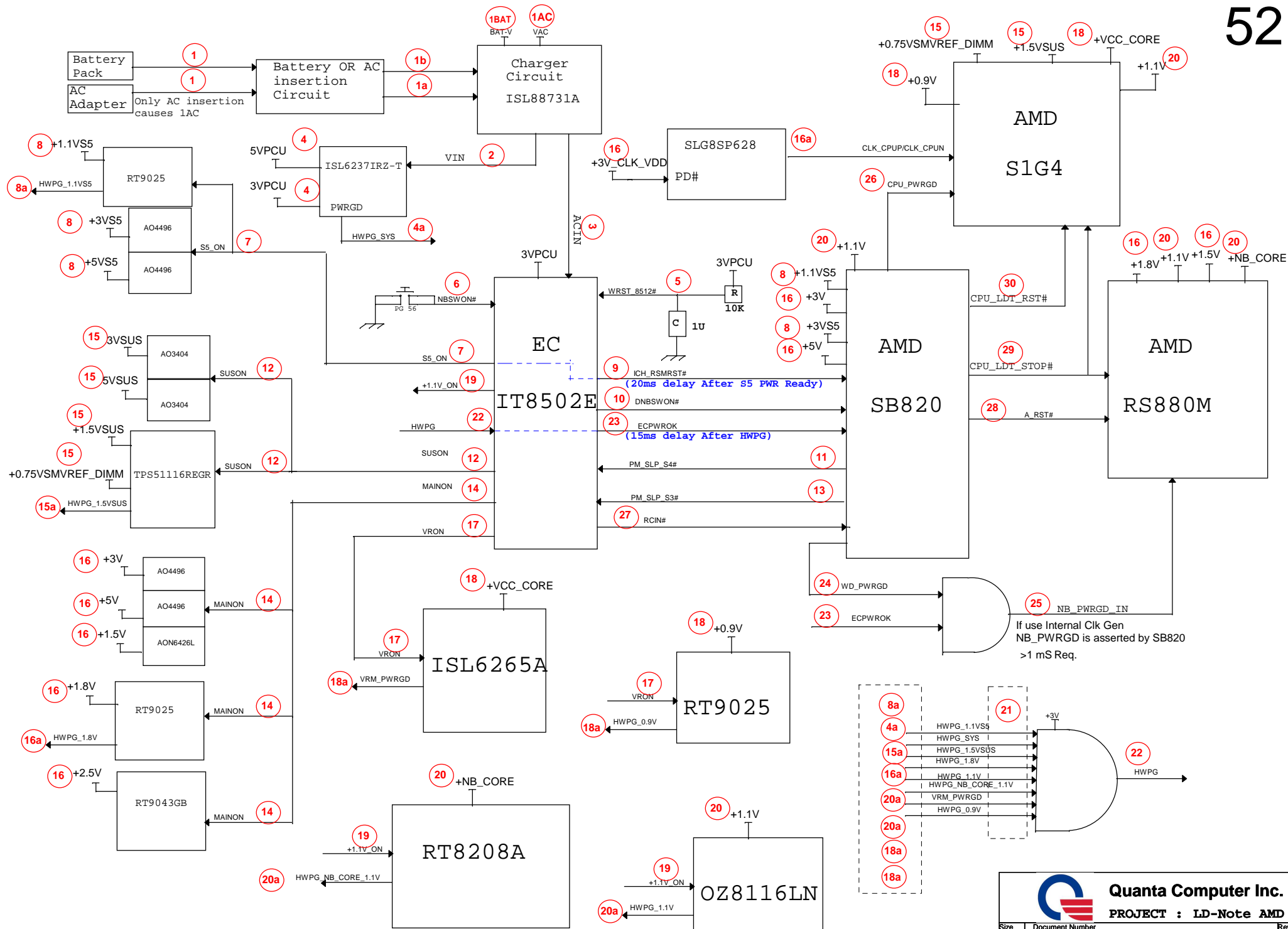
SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

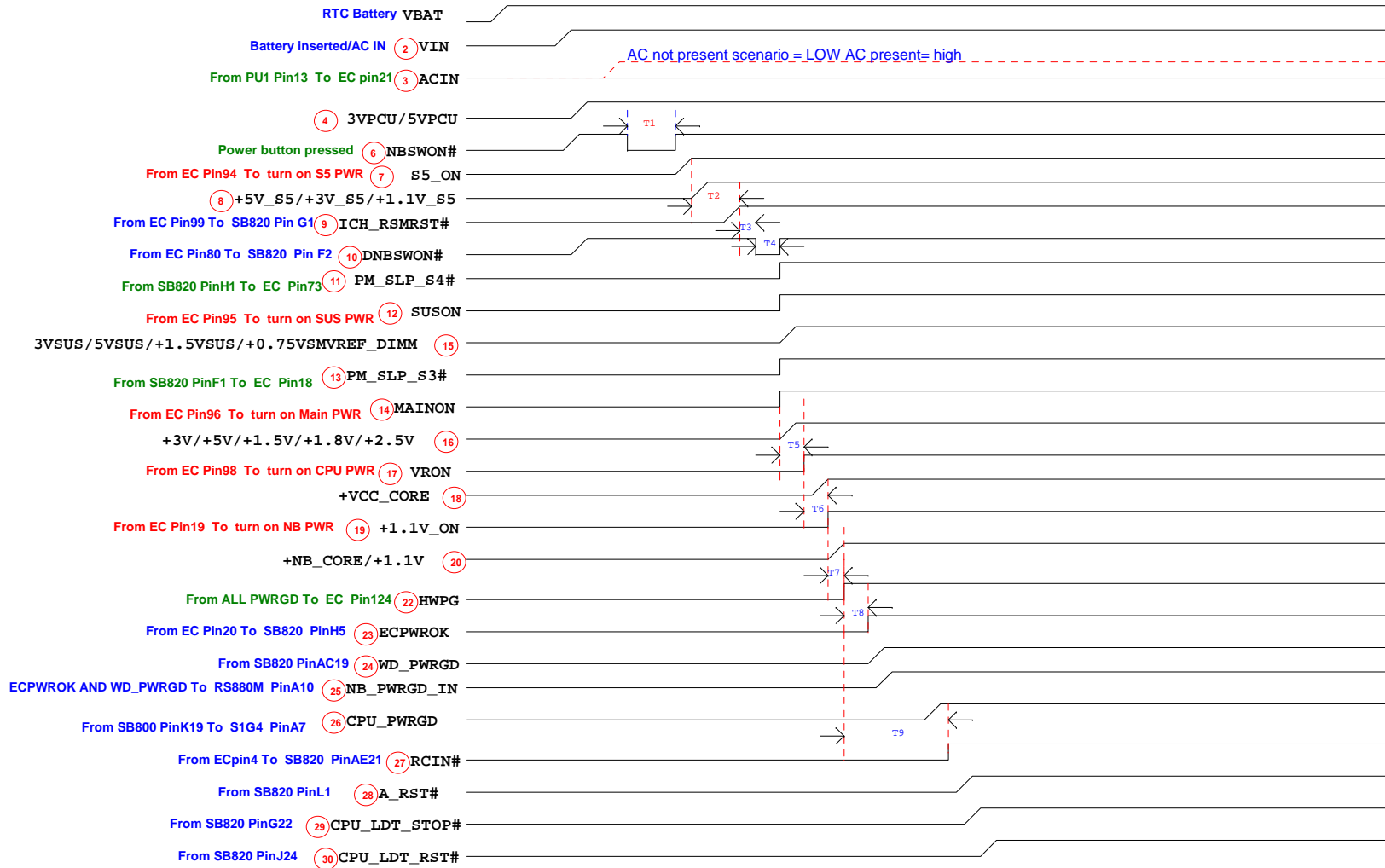


DISCHARGE

[illegible][illegible]







T1	>16ms
T2	20ms
T3	5ms
T4	1ms
T5	15ms
T6	5ms
T7	5ms
T8	15ms
T9	108ms

EC #	Page	Description	Part Affected
EC-C-01	20	Change error 10u footprint from 0603 to 0805	C51,C68,C78,C93,C236,C244,C247,C254,C257,C265,C270,C273,C602,C604,C705,C709,C714
EC-C-02		Layout change: Change TEST PAD size from 30mil to 20mil to increase ICT percentage	T1~T116,TP1~TP24
EC-C-03	23	Change X5R to X7R due to X5R stock is EOL	C362,C364
EC-C-04	3 10 11	Add value with ' ' ' due to it is a short pad originally	R106,R466,R468 R573 R268,R566
EC-C-05	10	Un-stuff 22P coupling CAP & change RES from 22ohm to 10ohm to fix LPC_CLK rising time issue	C777,R511
EC-C-06	48 45	Modify some RC value to meet VGA power up sequence From 10K to 0 ohm From 0.33U to NA From 0.01U to 2200P From 0.33U to 0.1U From 0.33U to 0.047U	PR165 PC115 PC117 PC103 PC113
EC-C-07	25	Change RGB bead value to fix EA rising time issue	L18,L24,L27
EC-C-08	19	AMD suggest remove pull high RES AMD suggest add pull high RES	R91,R412,R419 R416,R420
EC-C-09	39	Add fuse for EL keyboard UL suggestion	F6
EC-C-10	34	Add 2N7002 to reduce leakage current	Q41
EC-C-11	5	Add transistors for EC to monitor thermal of CPU (SB_TSI mode)	Q42,Q43,Q44
EC-C-12	11	Stuff the RES due to BOM error	R360
EC-C-13	8	Change BOM to meet "CPU_LDT_STOP#" Replace Q36 with U48,delete R454,R451,change R452 from 4.7K to 2.2K	Q36,U48,R454,R451,R452
EC-C-14	3,8	AMD suggest "CPU_LDT_RST#" & "CPU_LDT_STOP#"connect to +1.5V power for prevent current leakage	R110,R453
EC-C-15	5	Delete thermal sensor schematic due to AMD suggest that don't use external thermal IC to prevent thermal shut down issue.	Q11,Q12,U7,R131,R132,R117,C302,C305,R138,R137,C341,Q13,R120
EC-C-16	46	To improve +1.1VS5 rise time waveform. Modify CAP value.	PC80
EC-C-17	10	For RTC test accurately, modify 32.768KHz XTAL coupling CAP	C812,C813
EC-C-18	48	AMD fine tune VBIOS to meet VGA_CORE table	
EC-C-19	44	BOM error,remove the component	PC142
EC-C-20		Change the power jump to short pad	PJP1~PJP18
EC-C-21	45	Reserve RC circuit to modify power sequence	PR288,PC246
EC-C-22	45	Change RES value to fine tune +1.0_GPU prevent from voltage drop issue	PR152
EC-C-23	11	Add NEW_CLKREQ#, LAN_CLKREQ#, WLAN_CLKREQ# function at BIOS side	U38D pin AA16,AC18,AH21
EC-C-24	11	Delete single net SP_DDR3_RST# & 0 ohm RES	R337
EC-C-25	11	Add WAKE# net with +3VS5 pull high	R606
EC-C-26	27	Add thansistor to avoide leakage current of CLK request and wake up function of LAN. Delete 0 ohm RES	Q45,Q46,R337 R317
EC-C-27	3	Un-stuff RES for leakage issue Stuff RES for leakage issue	R484,R485 R476,R477
EC-C-28	26	Vendor suggest reserve it,BOM not mount	C551
EC-C-29	12	Update board ID table for BIOS to verify PCB version	
EC-C-30	30 31	Because sku in1 build WWAN, reserve all of components about WWAN function	CN25,U16,C395,C382,C396,C390,C383 CN26,R532,R543,R545,C808,C785,C795,C806,C784,C815
EC-C-31	41	Because we add LDO circuit to control G-Sensor power and we change GSENSOR_ON to high enable. We need to verify EC version	R381,R382
EC-C-32		Layout modify: modify SB & NB footprint due to customer request	U34,U43
EC-C-33	8	AMD comment DIS only supply 1.1V for NB_CORE,no need to stuff strap pin RES	R442
EC-C-34	12	AMD comment unstuff SB SATA 25MHz XTAL if we had stuff 25MHz internal XTAL	Y6,C794,C796,R536
EC-C-35	2	Follow up GC5C design to change 14.318 XTAL from 30ppm to 10ppm	Y1
EC-C-36	27	Change LAN chip version to reduce power consumption	U23
EC-C-37	26	Follow up GC5 design to change sense MIC switch from BJT to MOSFET	Q30
EC-C-38	41	ESD solution	D28,D29
EC-C-39	28	Reserve 0.1u CAP due to ESD solution	C832
EC-C-40	30	Modify USB CONN footprint due to SMT request	CN24,CN27
EC-C-41		Change 0 ohm RES footprint from 0402 to short pad	R397,R431,R432,R459,R197,R200,R370,R372,R379,R250,R259,R563,R287,R306,R320,R182,R183 R426,R290,R186,R189,R193,R201,R148,R150,R151,R152,R20,R25,R3,R472,R473,R474,R475, R84,R355,R356,R293,R298,R520,R524,R167,R376,R594,R595,R596,R597,R598,R599,R600, R313,R300,R341,R195,R302,R368,R369,R413,R414,R415,R31,R32,R47,R447,R449,R450,R554, R571,R283,R436,R48,R227,R278,R346,R365,R204,R199,R252,R253,R267,R246,R270,R486,R552
EC-C-42	26	For MIC not be found issue, stuff R281,un-stuff R292,Q30,R286	R281,R292,Q30,R286
EC-C-43	41	Modify EC ID table for EC setting	R381,R382
EC-C-44	12	Modify board ID table for BIOS setting	R537,R538
EC-C-45	48	Remove 2N7002 due to BOM error	PQ51
EC-C-46	19	Change VGA thermal IC to ADM1032-2 in order to change address to 4D	U32
EC-C-47	41	BIOS set RF_SW# GPIO pull down to detect UMA & DISCRETE planer	R373,C575

