

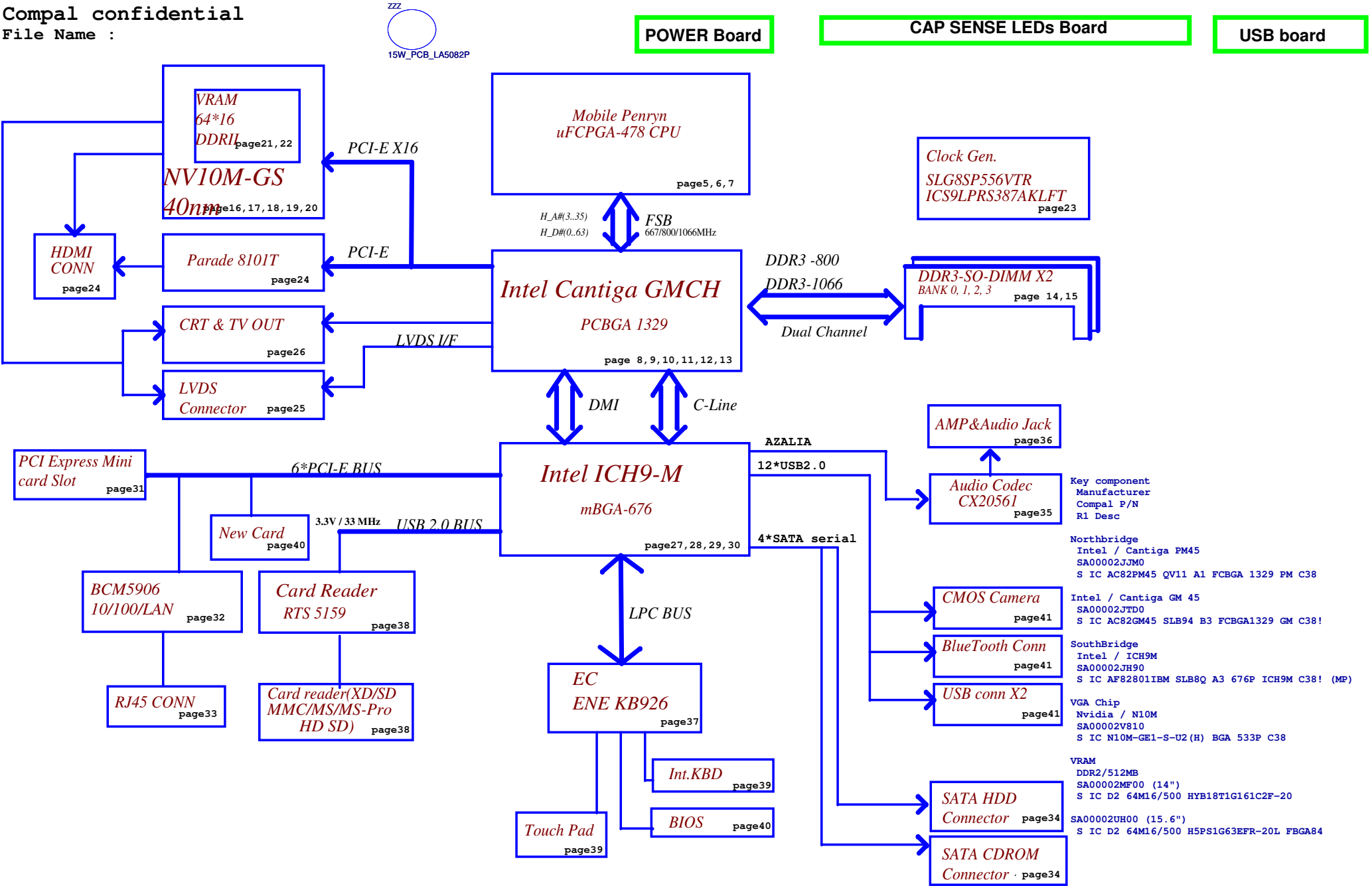
KIWA7/A8

Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM/PM+ICH9-M core logic

REV: 0.4

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DDR3 Voltage Rails

<div>power plane</div> <div>State</div>	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	X	X	X	X	X	X	V	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBCLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMICLK_NB HDMIDAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCCLK VGA_DDCDATA	VGA	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	VGA	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT	VGA	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	VGA	X	X	X	V	X	X	X	X	X	X	X	X	X
FSEL#SPICS#_SB FRD#SPI_SO_SB SPI_CLK_SB FWR#SPI_SI_SB	ICH9	X	X	X	X	X	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPI_SO SPI_CLK FWR#SPI_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

VGA and DDR2 Voltage Rails (N10M)

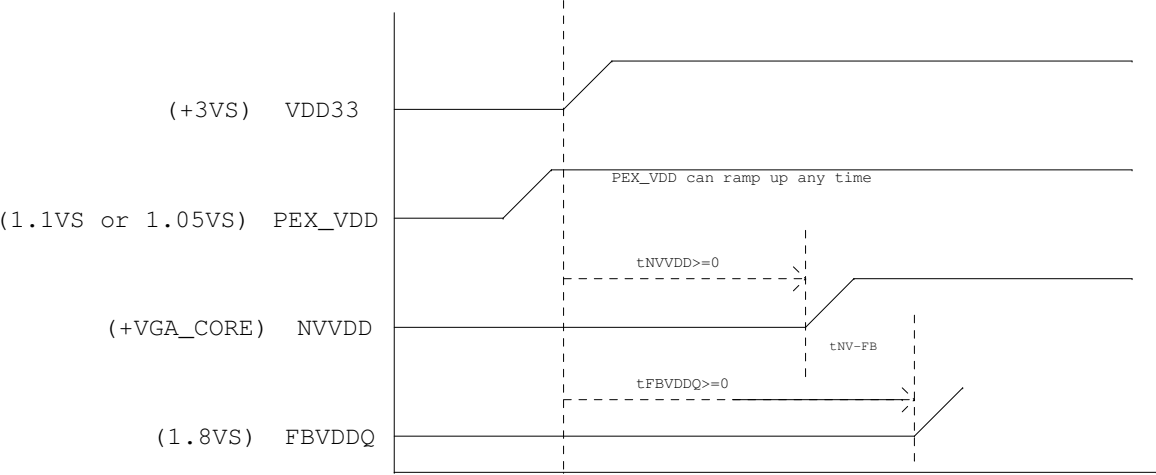
State \ power plane				
				+3VS +VGA_CORE +1.1VS (for 55nm) +1.05VS (for 40nm) +1.8VS
	S0	○	○	○
	S1	○	○	○
	S3	○	○	✗
	S5 S4/AC	○	○	✗
	S5 S4/ Battery only	○	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

EDP at Tj = 97C*

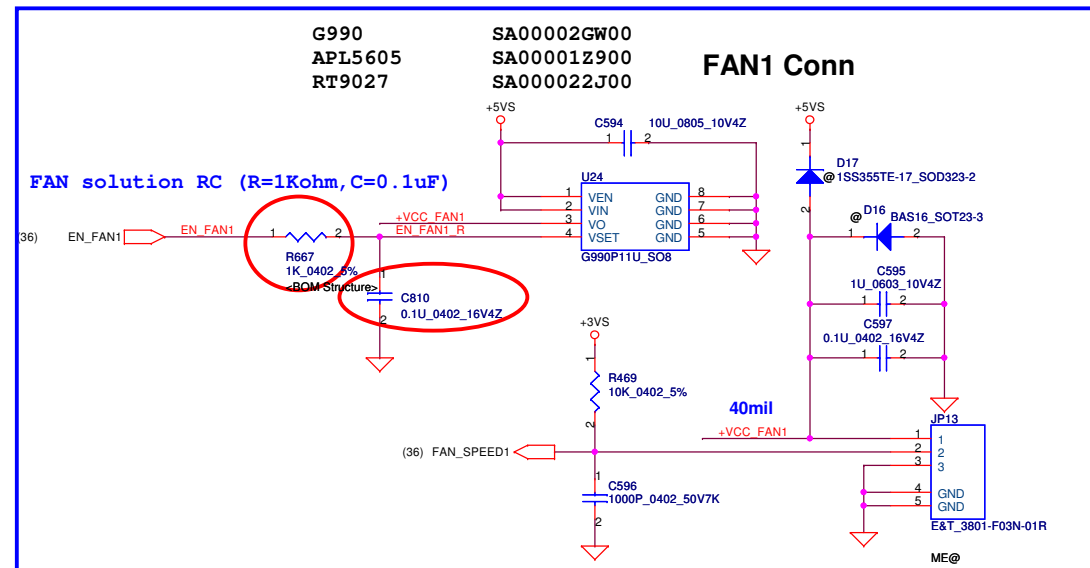
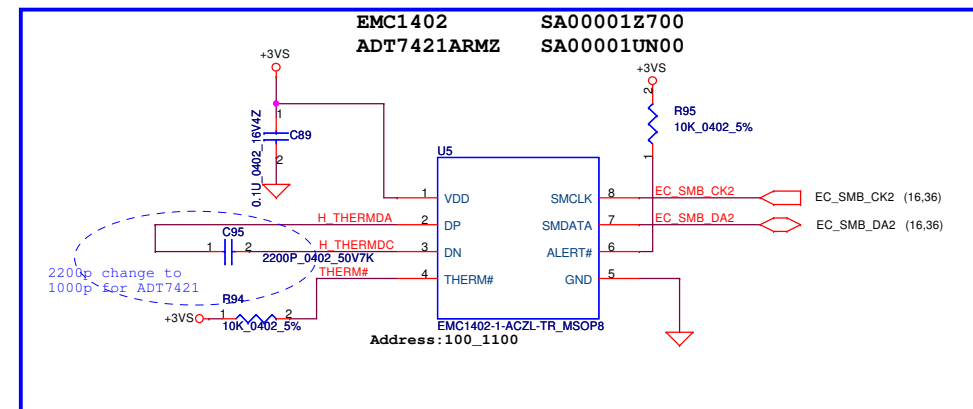
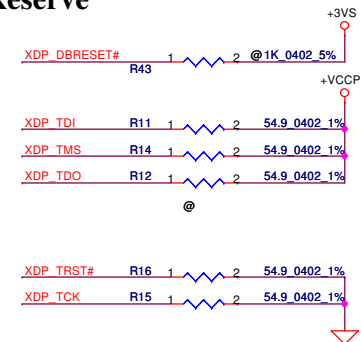
Power Supply Rail (V)		NB9M-GS		N10M-GE1-S	
		GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	11.22A	10.87A	13.56A	13.47A
FB_DLLAVDD	1.1	25mA		25mA	
FB_PLLAVDD	1.1	10mA		10mA	
IFPC_IOVDD	1.1	385mA		180mA	
IFPD_IOVDD	1.1	385mA		180mA	
IFPE_IOVDD	1.1	385mA		180mA	
IFPF_IOVDD	1.1	385mA		180mA	
PEX_IOVDD/Q	1.1	1550mA		1550mA	
PEX_PLLVDD	1.1	165mA		65mA	
PLLVDD	1.1	55mA		30mA	
SP_PLLVDD	1.1	25mA		10mA	
VID_PLLVDD	1.1	50mA		25mA	
TOTAL	1.1	3.425A		2.435A	
FBVDD/Q	1.8	2.24A	1.65A	2.24A	1.75A
IFPA_IOVDD	1.8	50mA		50mA	
IFPB_IOVDD	1.8	50mA		50mA	
IFPAB_PLLVDD	1.8	100mA		75mA	
IFPCD_PLLVDD	1.8	160mA		80mA	
IFPEF_PLLVDD	1.8	160mA		80mA	
TOTAL	1.8	2.76A	2.17A	2.575A	2.085A
DACA_VDD	3.3	110mA		110mA	
DACB_VDD	3.3	125mA		125mA	
DACC_VDD	3.3	110mA		110mA	
MIOA_VDDQ	3.3	10mA		10mA	
MIOB_VDDQ	3.3	10mA		10mA	
VDD33	3.3	80mA		80mA	
TOTAL	3.3	0.445A		0.445A	

POWER SEQUENCE

The ramp time for any rail must be more than 40us



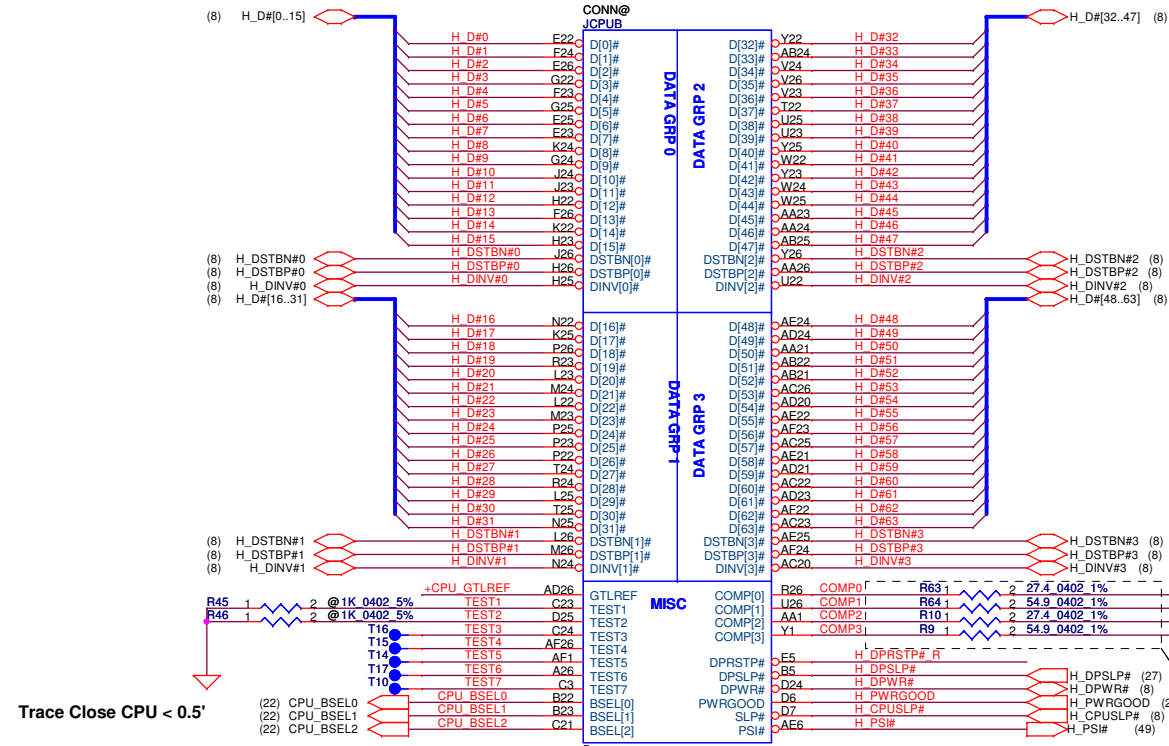
XDP Reserve



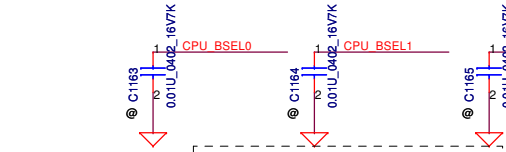
H_THERMDA, H_THERMDC routing together,
 Trace width / Spacing = 10 / 10 mil

RSVD pins on the CPU
 should be left as NO
 CONNECT

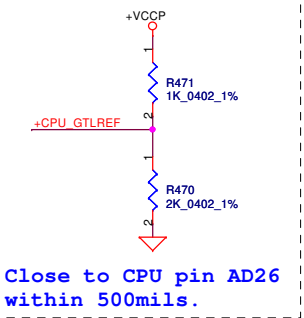
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Width=4 mil ,
Spacing: 15mil
(55Ohm)



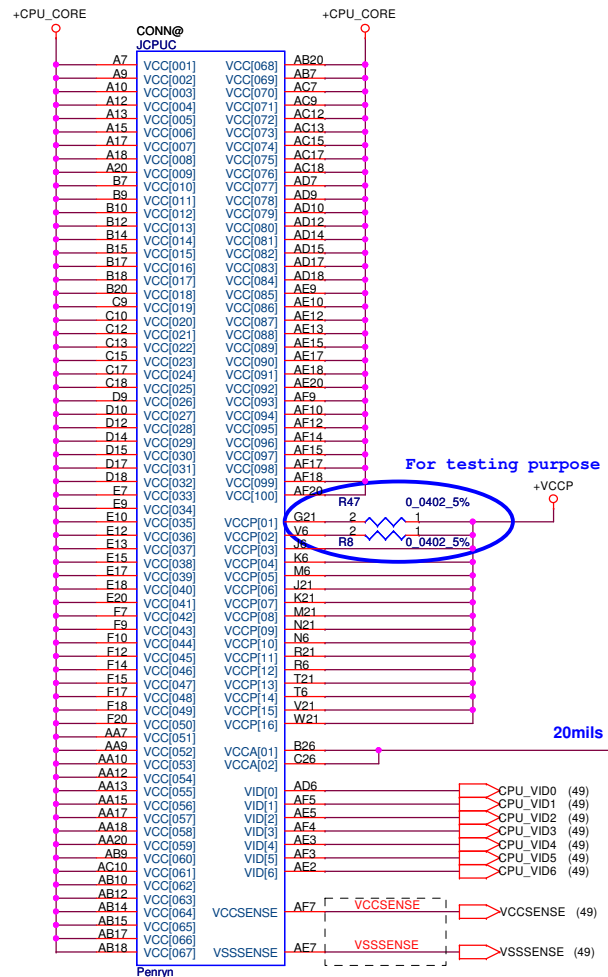
Layout note: Z0=55 ohm
0.5" max for GTLREF.



layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

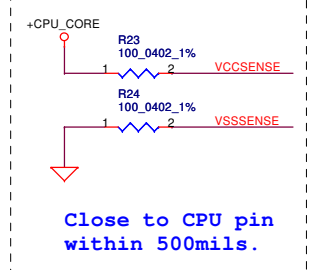
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

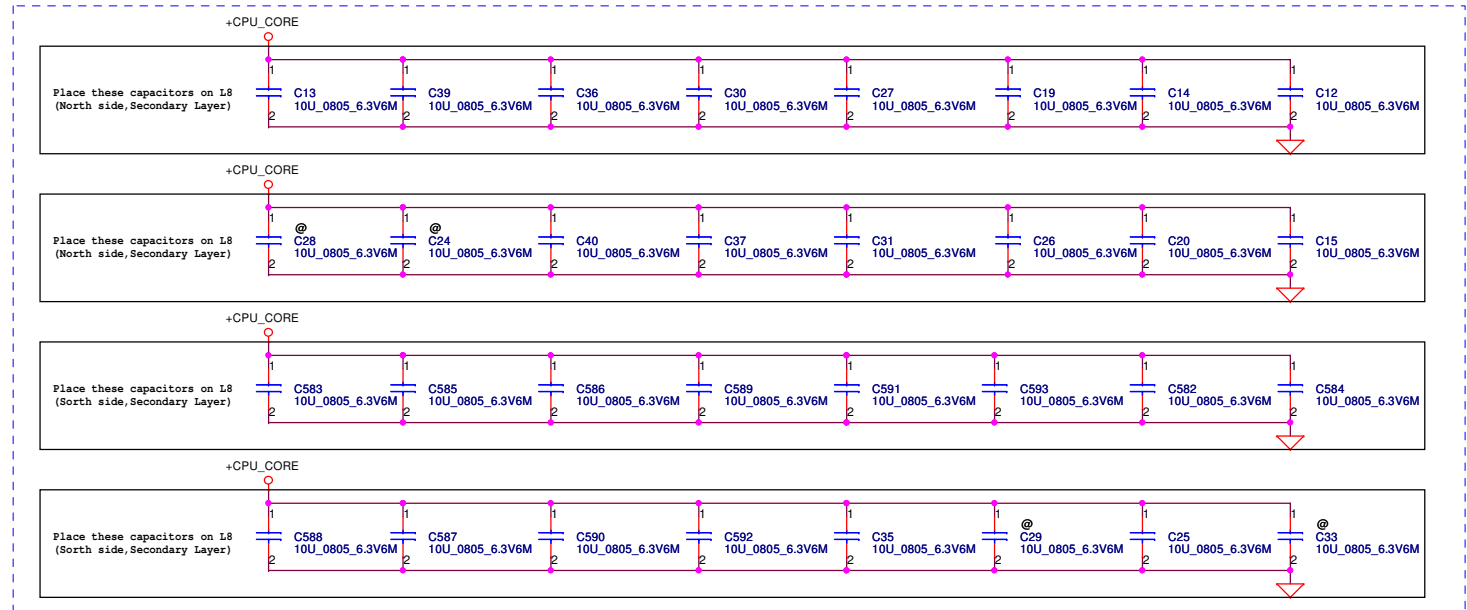
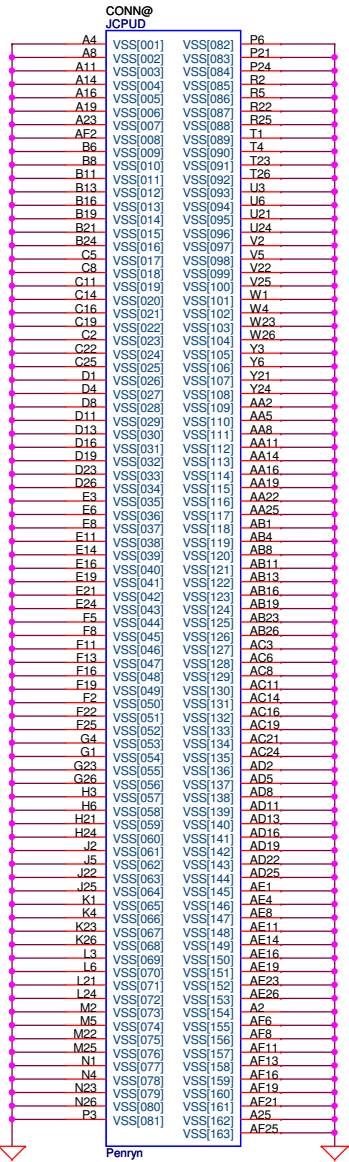
TRACE CLOSELY CPU < 0.5"
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)



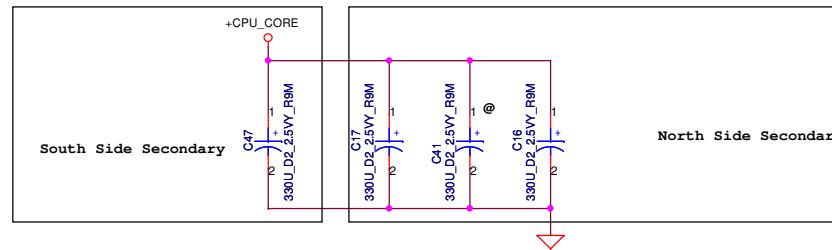
Length match within 25 mils.
The trace width/space/other is
16/7/25.

Layout Note:
Route VCCSENSE and VSSSENSE traces at
27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.



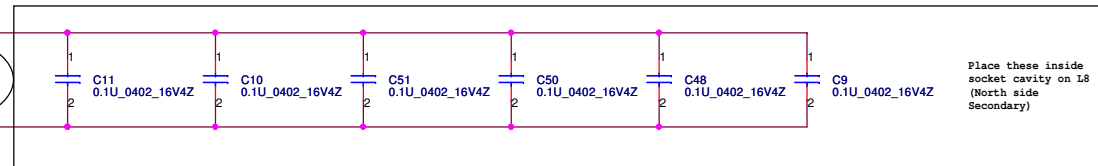
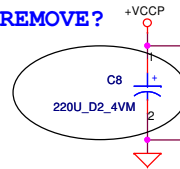


Mid Frequency Decoupling

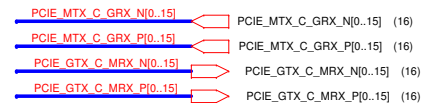
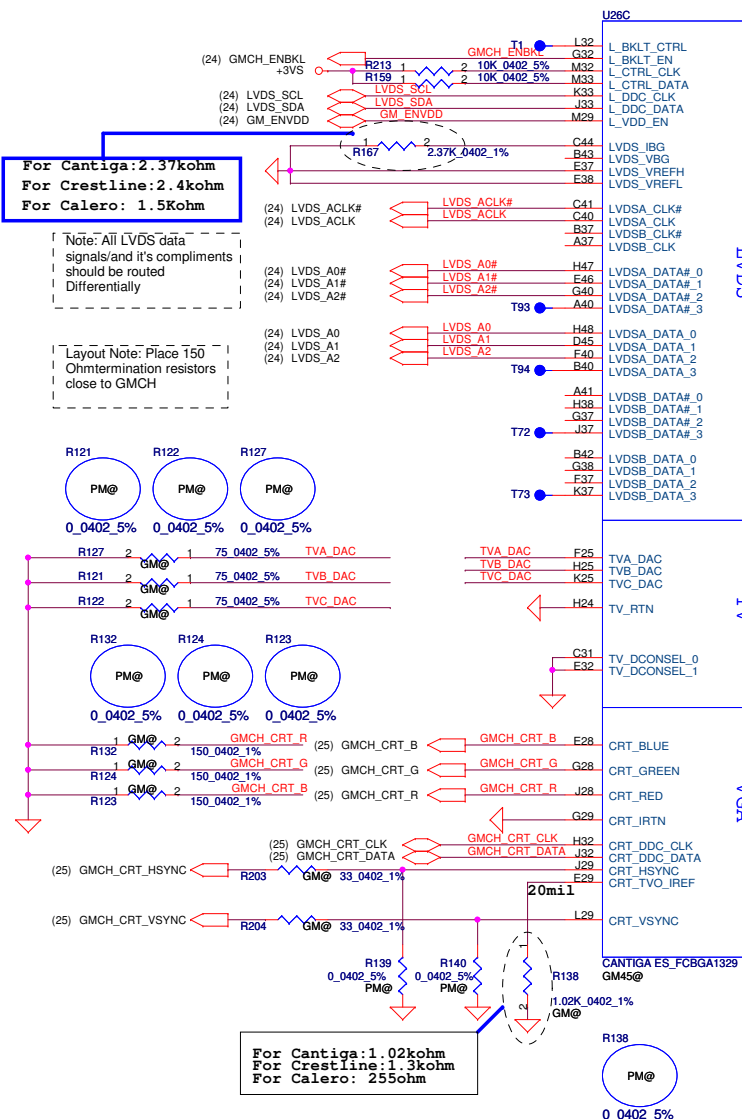


ESR <= 1.5m ohm
Capacitor > 1980uF

REMOVE?

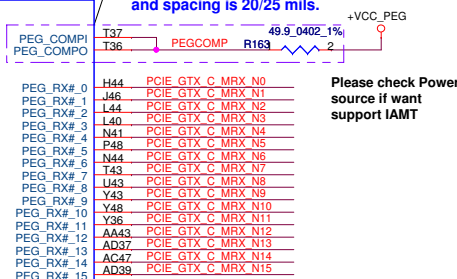


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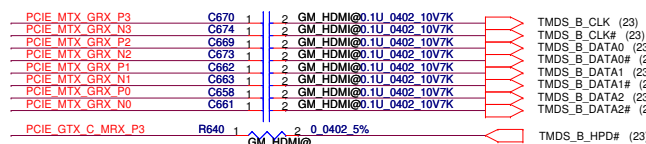
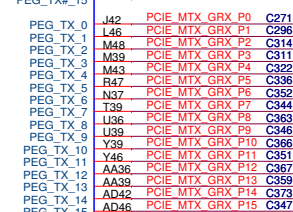
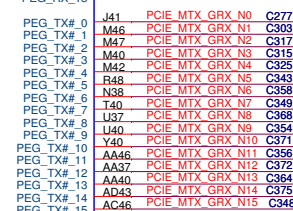
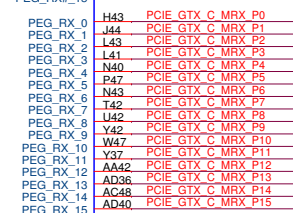


Place the resistor within 500mils (1.27mm) of the (G)MCH

PEGCOMP trace width
and spacing is 20/25 mils.

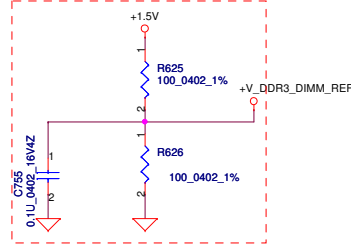
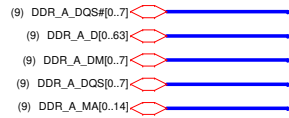


Please check Power source if want support IAMT



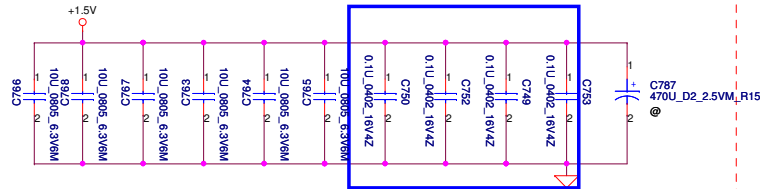
Strap Pin Table

Strap Pin Table	
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable 1 = The ITPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation, Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

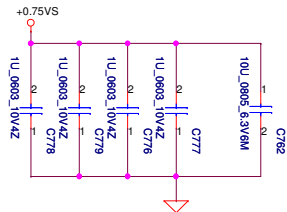


Layout Note:
Place near JP4

Layout Note: Place these 4 Caps near Command
and Control signals of DIMMA

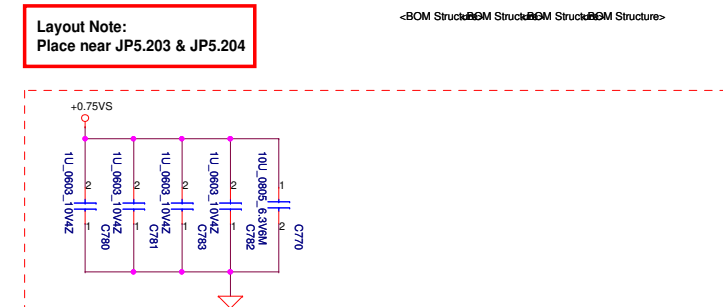
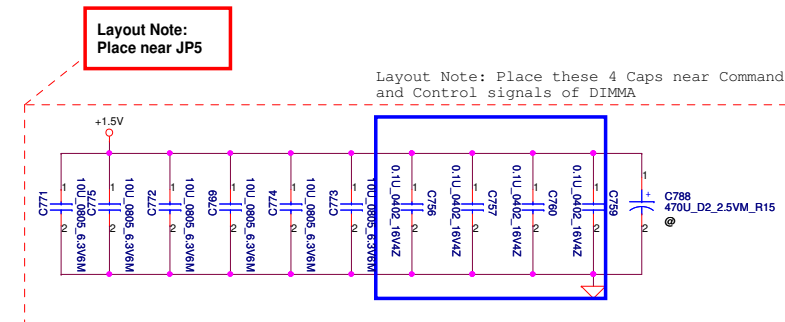
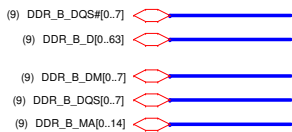


Layout Note:
Place near JP4.203 & JP4.204



DDR3 SO-DIMM A REVERSE

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PLACE NEAR BGA

0.022U_0402_16V7K 0.022U_0402_16V7K 0.1U_0402_16V4Z 0.1U_0402_16V4Z 4.7U_6.3V_K_X5R_0603 4.7U_6.3V_K_X5R_0603 1.8VS

C971 PM@ C972 PM@ C973 PM@ C974 PM@ C975 @ C976 PM@

0.022U_0402_16V7K 0.1U_0402_16V4Z 4.7U_6.3V_K_X5R_0603

PLACE BELOW GPU **FBAVDDQ=2.24A**

4700P_0402_25V7K 4700P_0402_25V7K 1U_0603_10V4Z 1.8VS

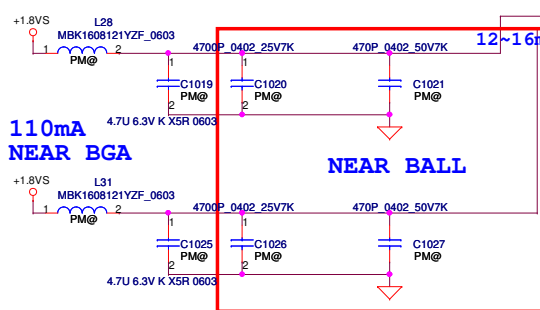
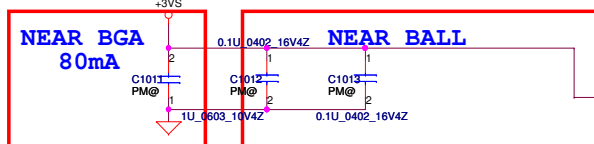
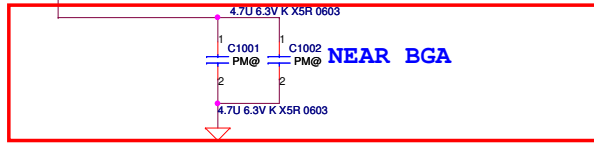
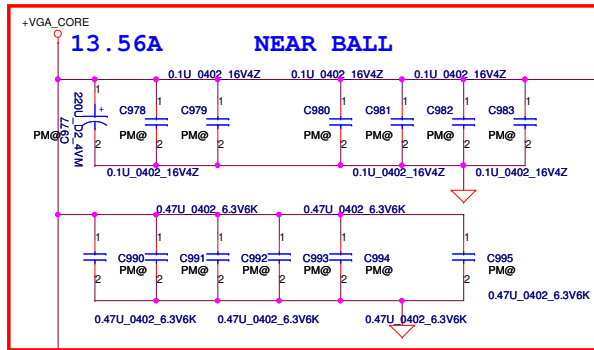
C984 PM@ C985 PM@ C986 PM@ C987 PM@ C988 PM@ C989 PM@

4700P_0402_25V7K 0.022U_0402_16V7K 0.1U_0402_16V4Z

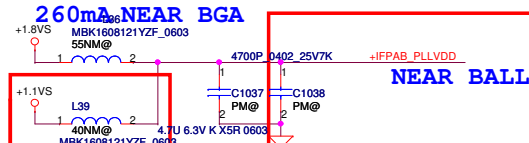
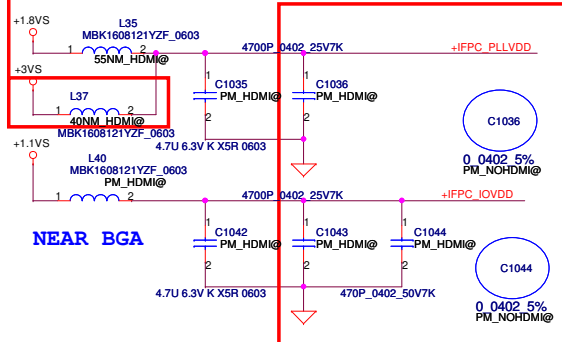
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C996 PM@ C997 PM@ C998 PM@ C999 PM@ C1000 PM@

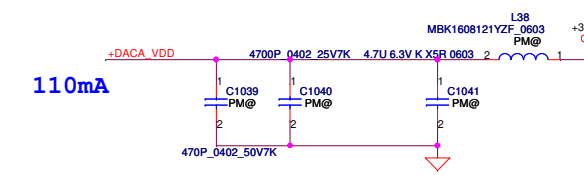
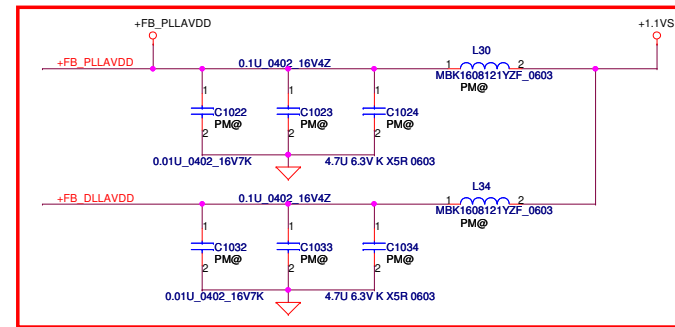
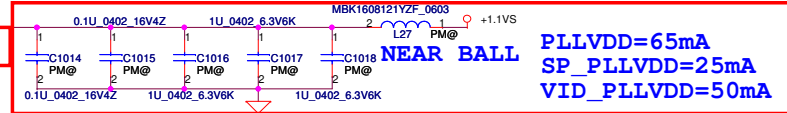
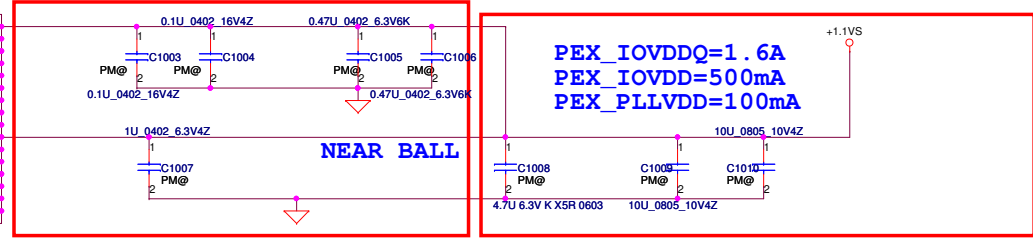
4700P_0402_25V7K 0.1U_0402_16V4Z



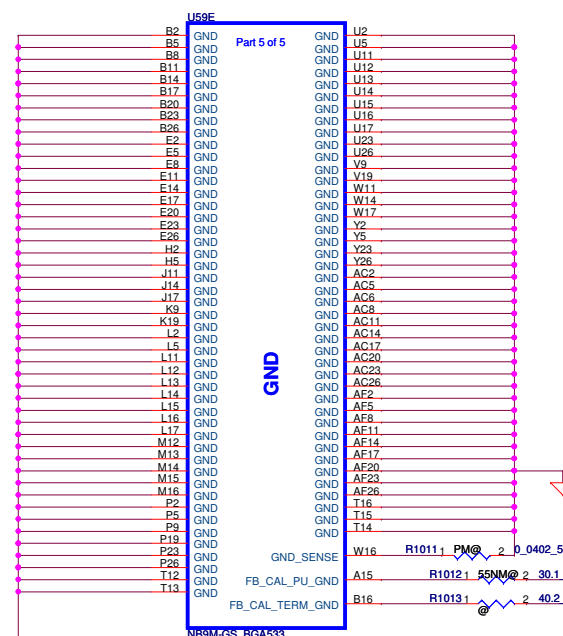
IFPC_PLLVDD: please add option to support both 1.8V (for G9X) and 3.3V(for GT21X)



IFPAB_PLLVDD: please add option to support both 1.8V(for G9X) and 1.05V(for GT21X)



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Memory/PKG	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR2	30.1ohm	30.1ohm	NC
GDDR3	33.2ohm	44.2ohm	40.2ohm

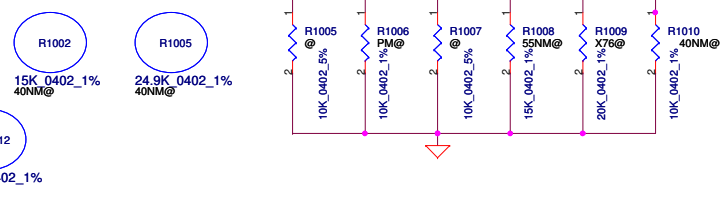
To update for NV PUN-03304-001_V06 (2008/4/01)



A total of 8 signals are required for GB1 strapping this includes
2 reference signals
6 physical strapping pins
4 logical strapping bits
A total of 24 logical strapping bits are available

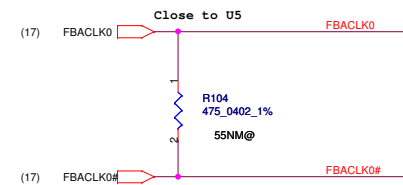
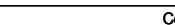
R148 pop 25K ohm
when use N10M-GE1-S (55nm)

- (17) STRAP2
- (17) STRAP1
- (17) STRAP0
- (17) ROM_SCLK
- (17) ROM_SI
- (17) ROM_SO



GB1 Family GPU Strap Options

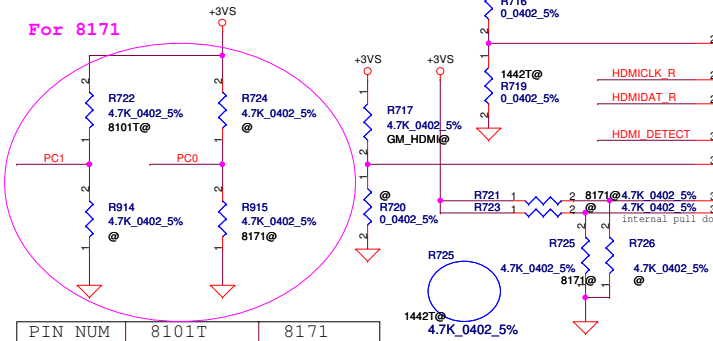
GPU	FB Memory (DDR2)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N10M-GE1-S (0x6EC) 55nm	Samsung	64Mx16	PU 5K	PD 15K	PD 10K	PU 5K	PD 10K PU 45K
	Hynix	64Mx16	PU 5K	PD 15K	PD 5K	PU 5K	PD 10K PU 45K
	Qimonda	64Mx16	PU 5K	PD 15K	PD 15K	PU 5K	PD 10K PU 45K
GPU	FB Memory (DDR2)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N10M-GS (0x6EC) 40nm	Samsung	64Mx16	PD 10K	PD 15K	PD 10K	PU 10K	PD 10K PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 5K	PU 10K	PD 10K PU 45K
	Qimonda	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 10K PU 45K



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				VRAM DDRA		
				Size Custom	Document Number KIWA5/6 LA-5081P	Rev 0.4
				Date: Wednesday, March 18, 2009		
				Sheet	20	of 53

10/30 update PS8171 co-lay circuit

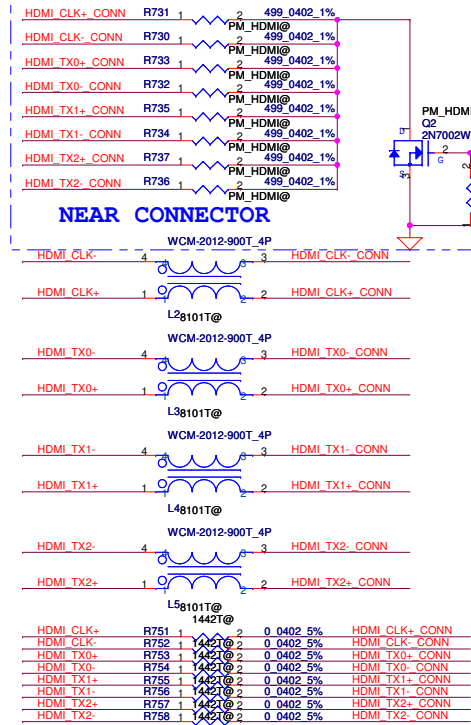
For 8171



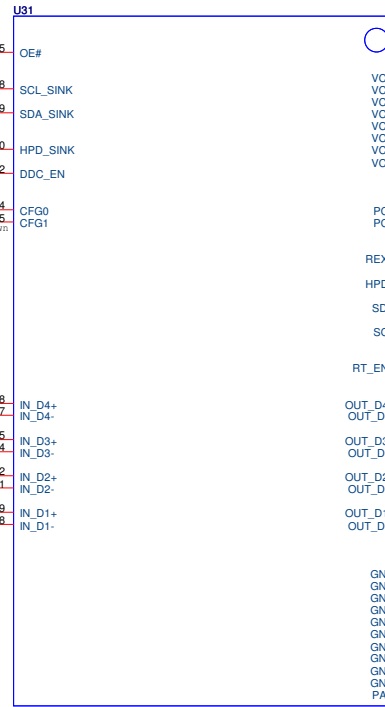
PIN NUM	8101T	8171
PIN1	GND	ASQ0
PIN3	PC0	PEQ
PIN4	PC1	PTO
PIN7	HPD#	HPDX
PIN10	RE_EN#	CEXT
PIN11	VCC	ASQ1
PIN12	GND	APD
PIN27	GND	EMI0
PIN33	VCC	EMI1
PIN34	DCCBUF_EN	DCCBUF
PIN35	CFG	PRE

```
For 8171 net name:
EMI0, EMI1
ASQ0, ASQ1
APD
```

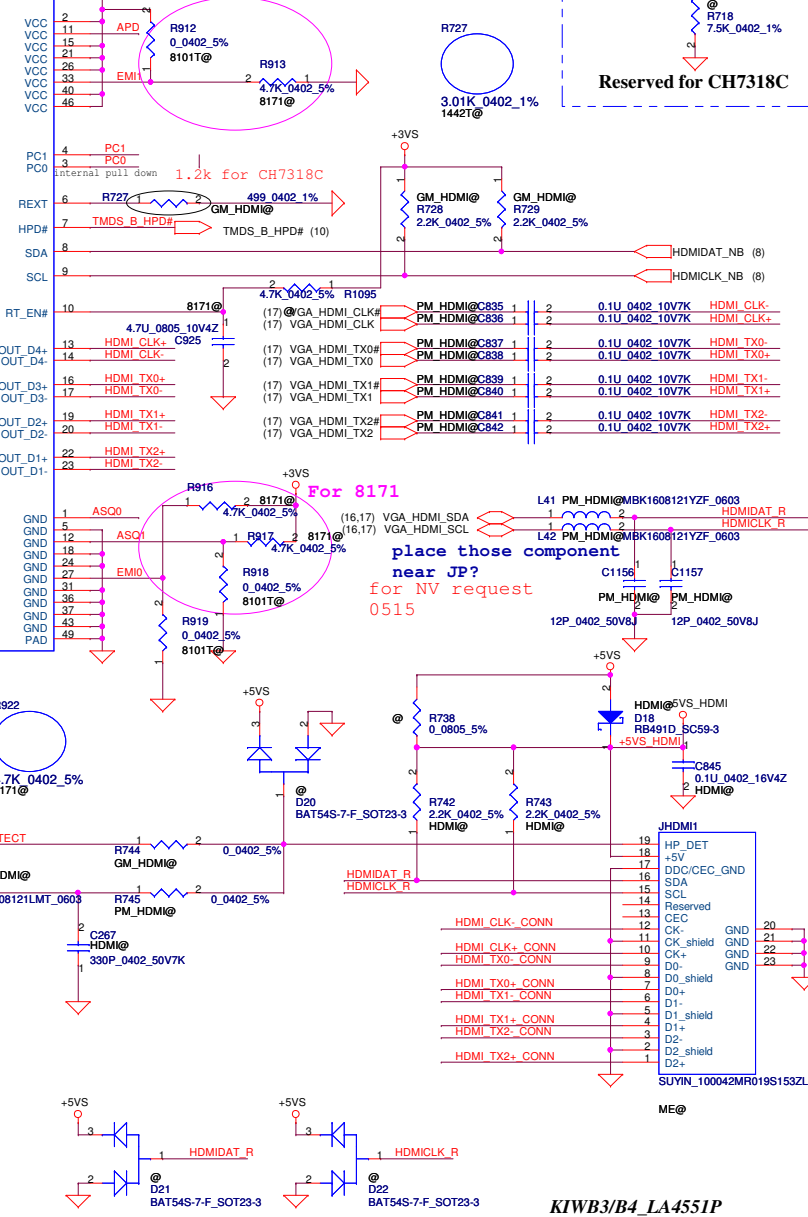
TMDS pull down (500ohm) resistors for ATI M92-S2 XT



P/N: SA00002D700 (8101T)
P/N: SA00001U920 (CH7318C)



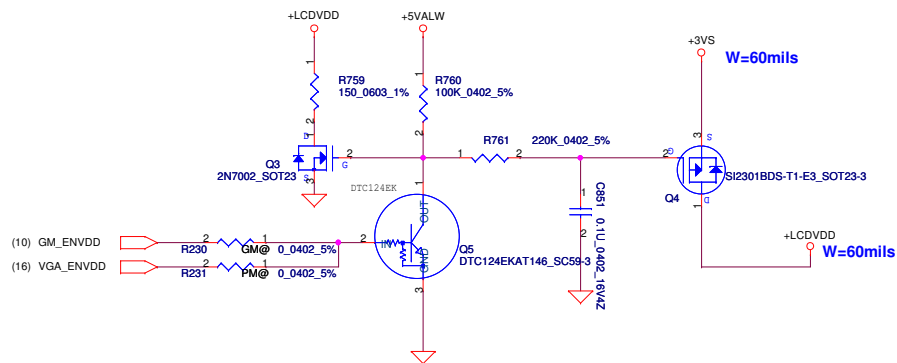
For 8171



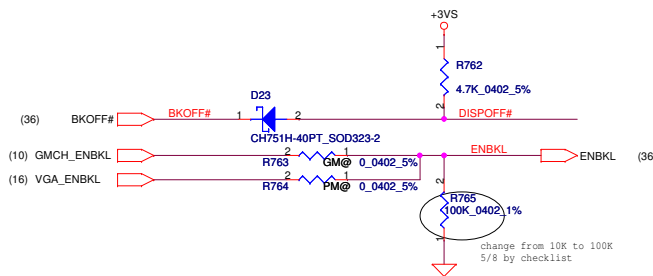
KIWB3/B4_LA4551P

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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	Level Shifter_PS8101T	
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				Custom	KIWAY_LA-5082P	0
				Date:	Wednesday, March 18, 2009	Sheet 23 of 53

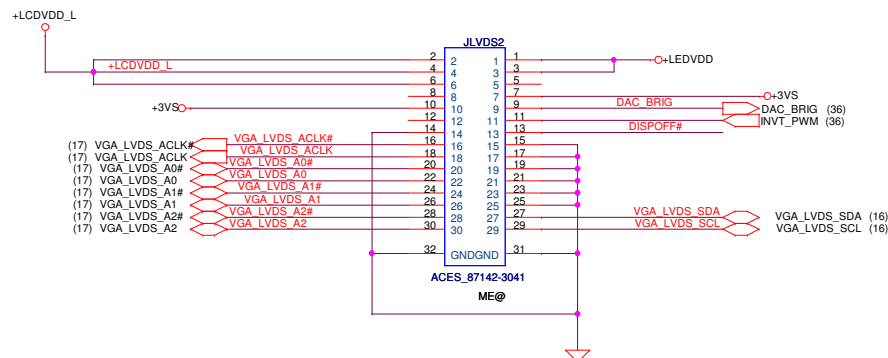
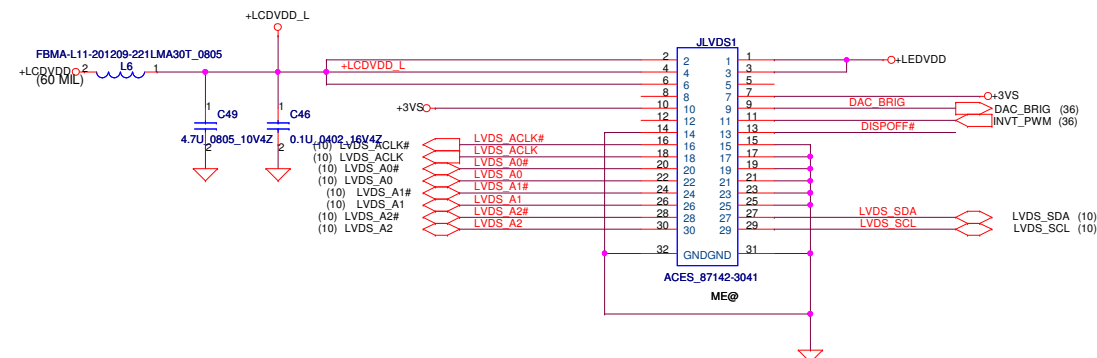
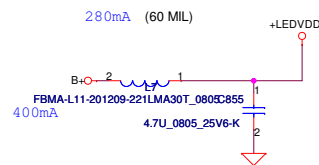
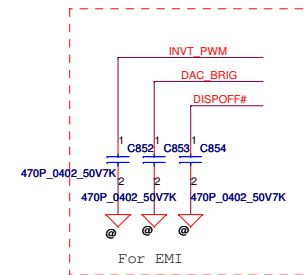
LCD POWER CIRCUIT



LCD/PANEL BD. Conn. FOR UMA



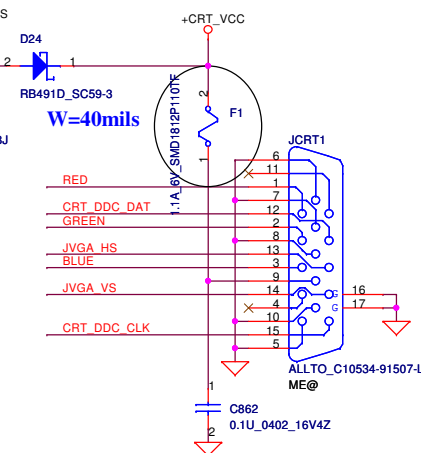
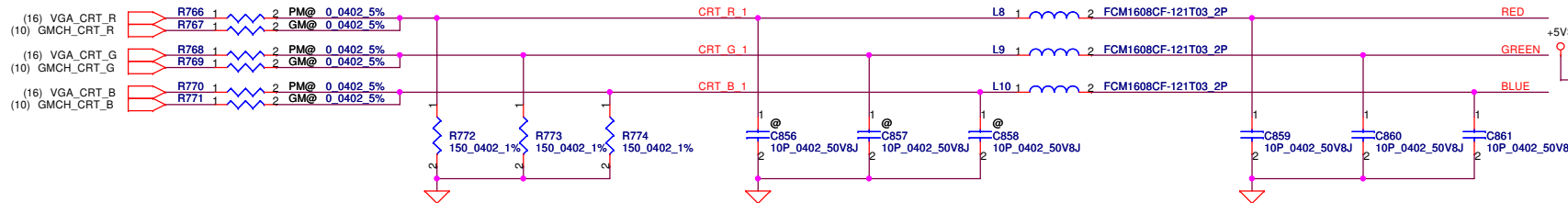
LCD/PANEL BD. Conn. FOR DIS



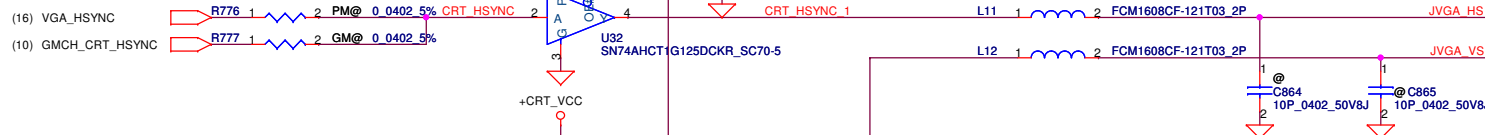
Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
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				Size B	Rev 0.4
Date: Wednesday, March 18, 2009				Sheet 24	of 53

CRT Connector

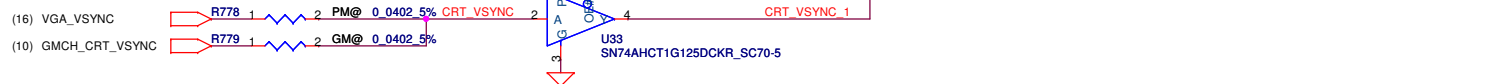
CLOSE TO CONN



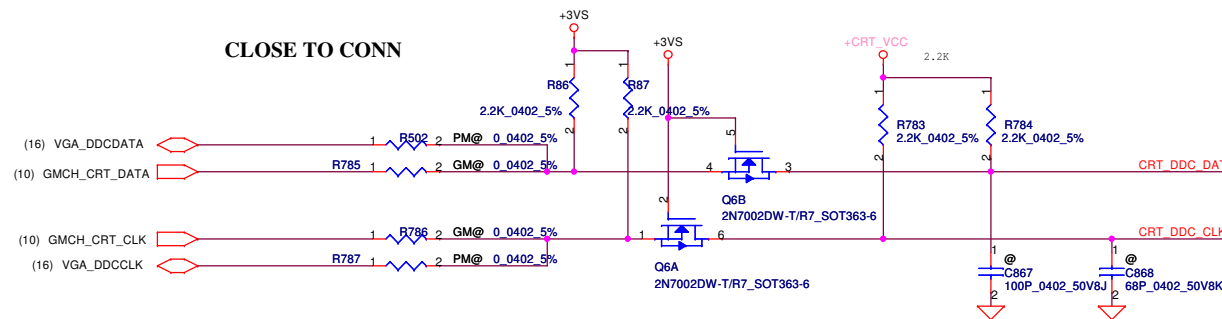
CLOSE TO CONN



CLOSE TO CONN



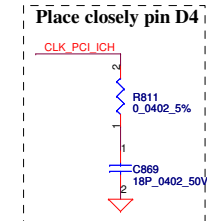
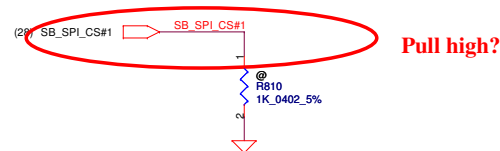
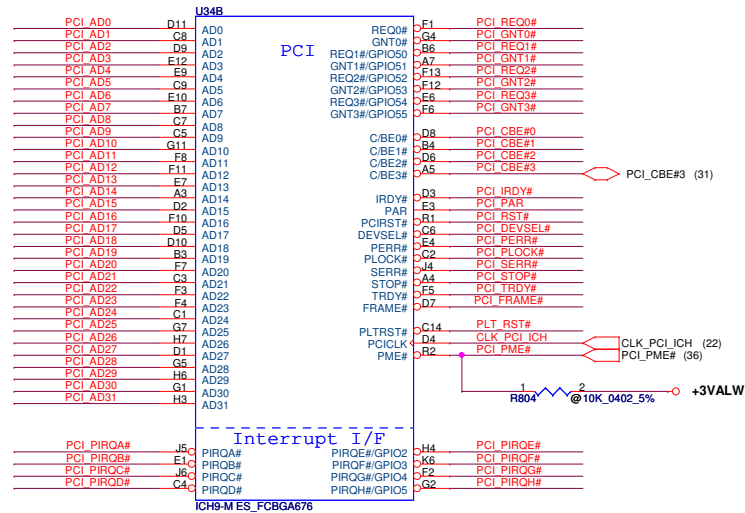
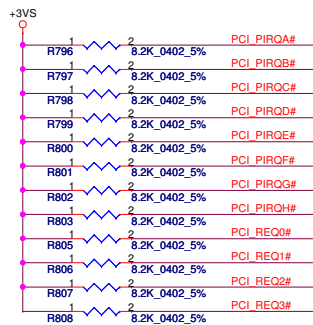
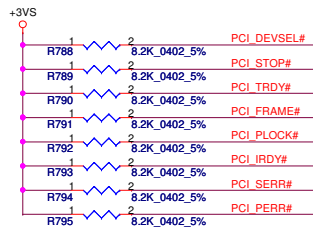
CLOSE TO CONN



PIN ASSIGMENT

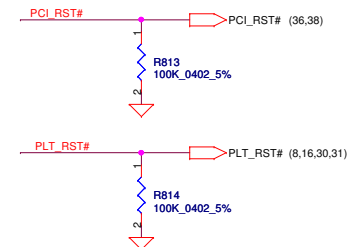
D-SUB	FUNCTION
9	+CRT_VCC
1	RED
6	GND
2	GREEN
7, 5	GND
3	BLUE
8	GND
14	VSYNC
10	GND
13	HSYNC
11	SENSE
12	SM_DAT
15	SM_CLK
4	PIN4

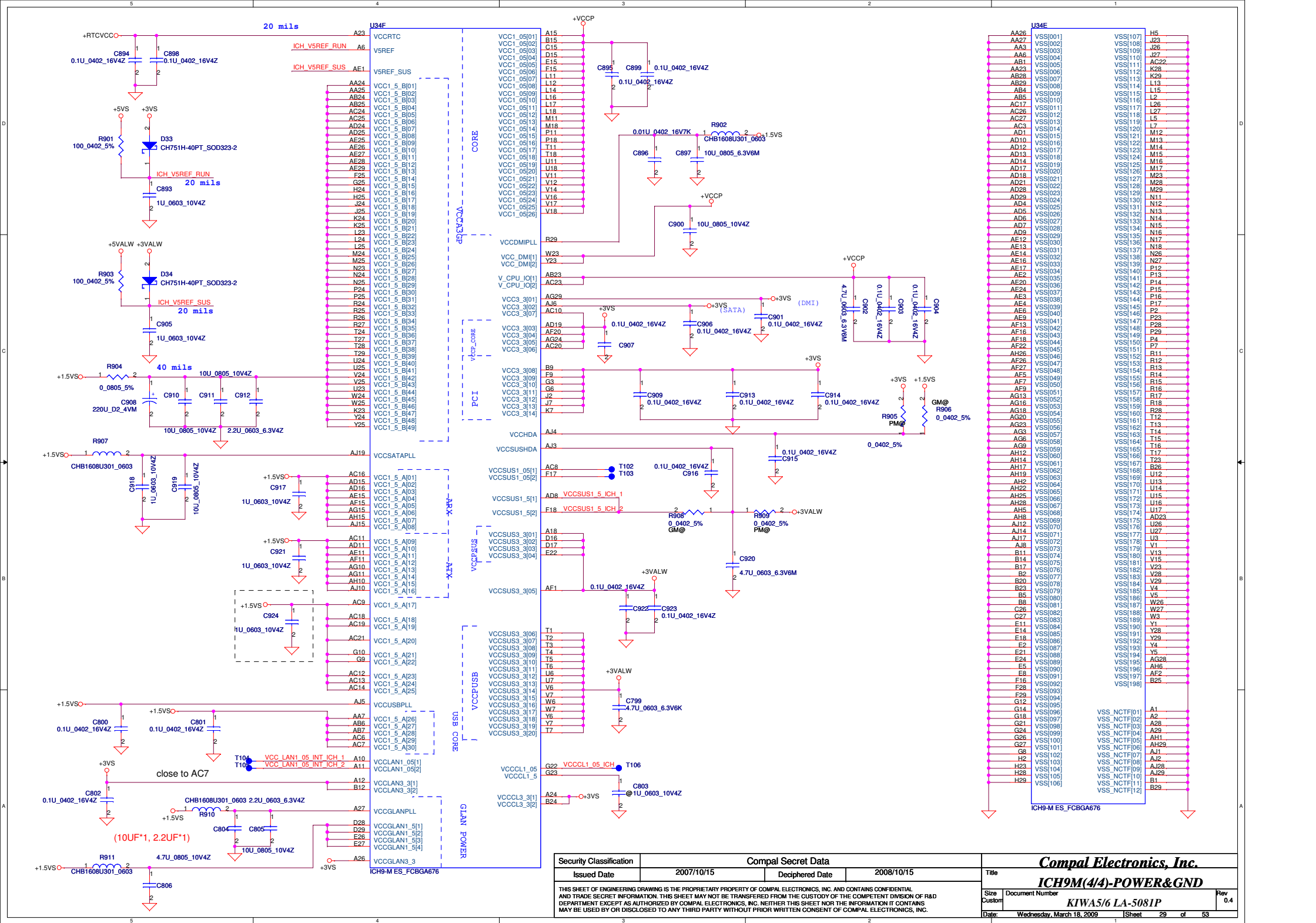
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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Size	Custom	Document Number	KIWA5/6 LA-5081P		Rev
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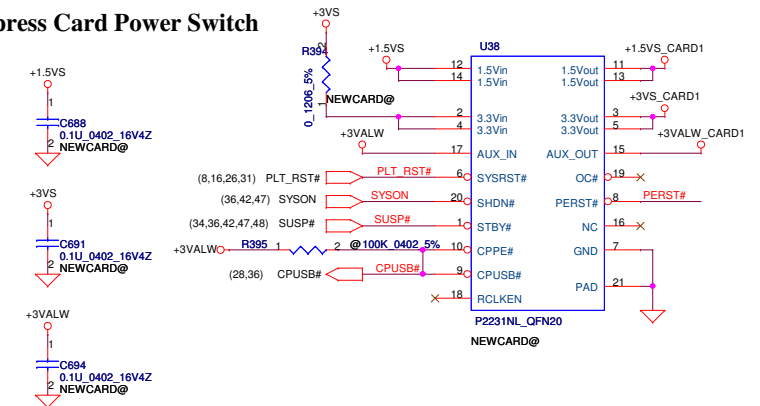
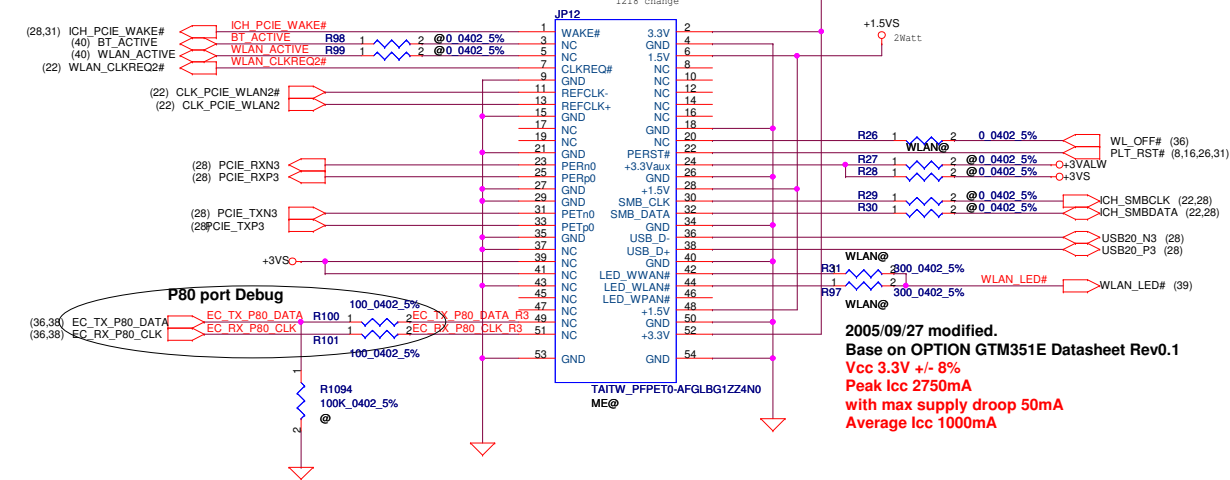
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*





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				Custom	KIWA56 LA-5081P	0.4	
				Date:	Wednesday, March 18, 2009	Sheet	29 of 53

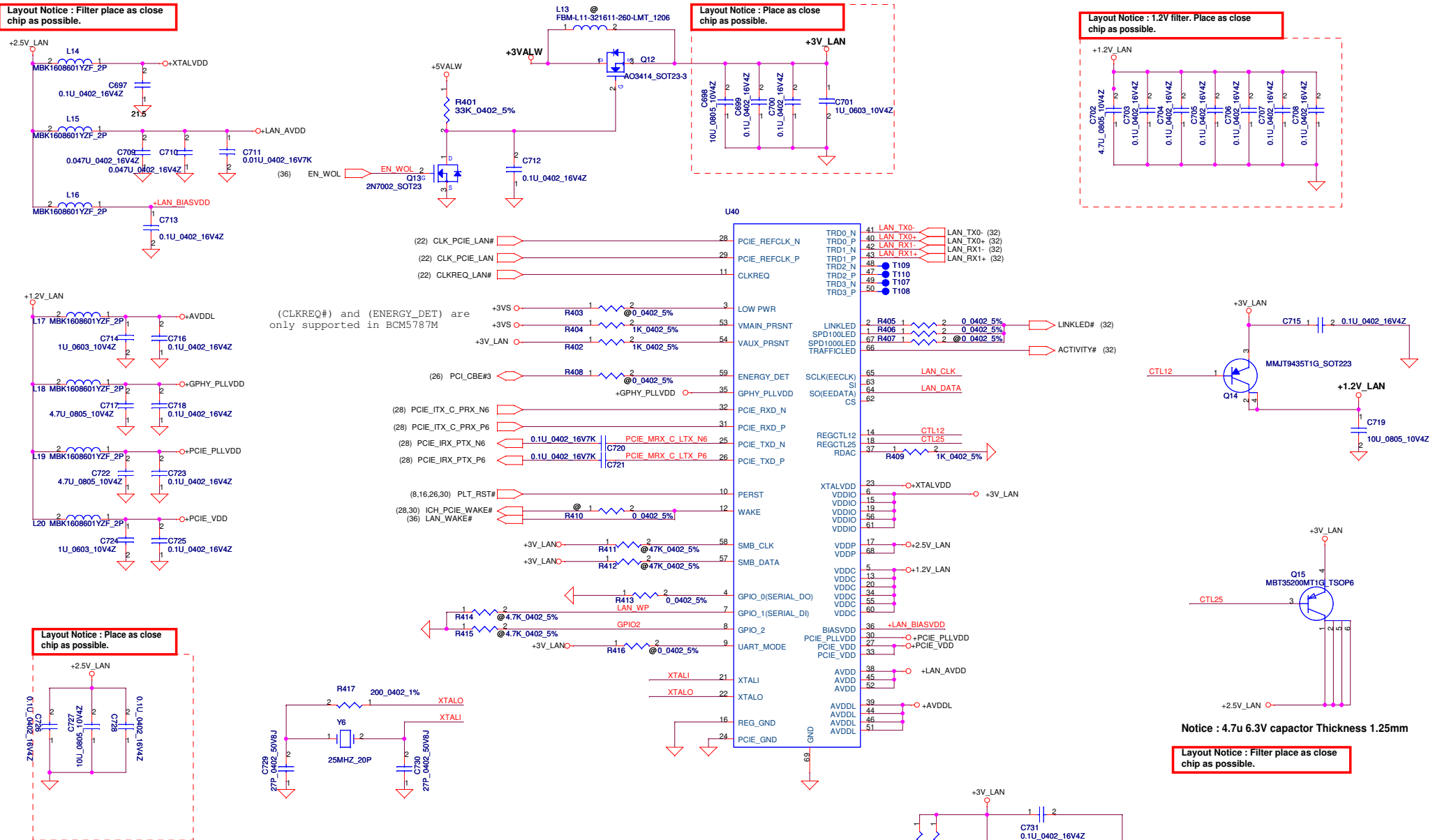


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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title Mini-Card/3G/TV /BT		
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					KIWAX_LA-5082P	0.4
Date:				Wednesday, March 18, 2009	Sheet	30 of 53

Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close to the chip as possible.

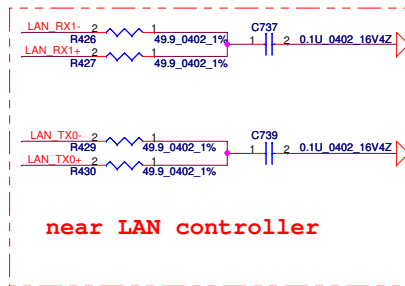
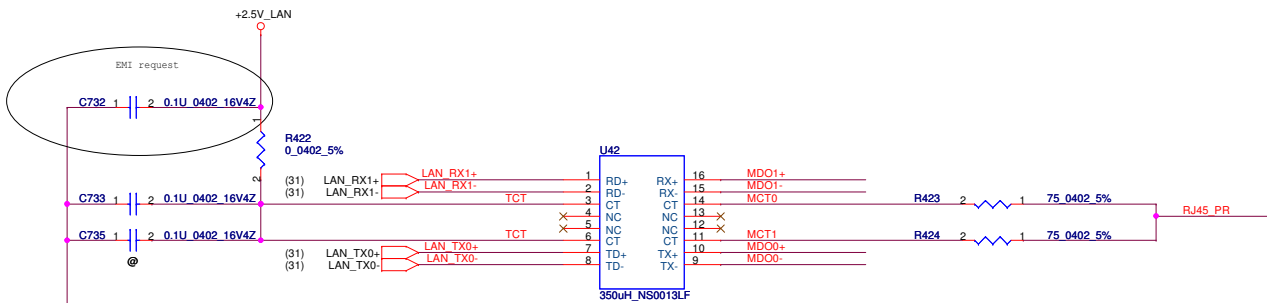
Layout Notice : 1.2V filter. Place as close chip as possible.



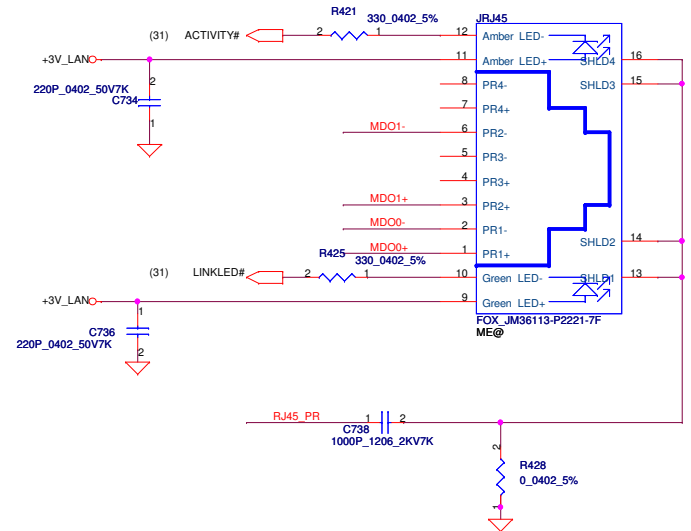
Notice : 4.7u 6.3V capactor Thickness 1.25mm

Layout Notice : Filter place as close chip as possible.

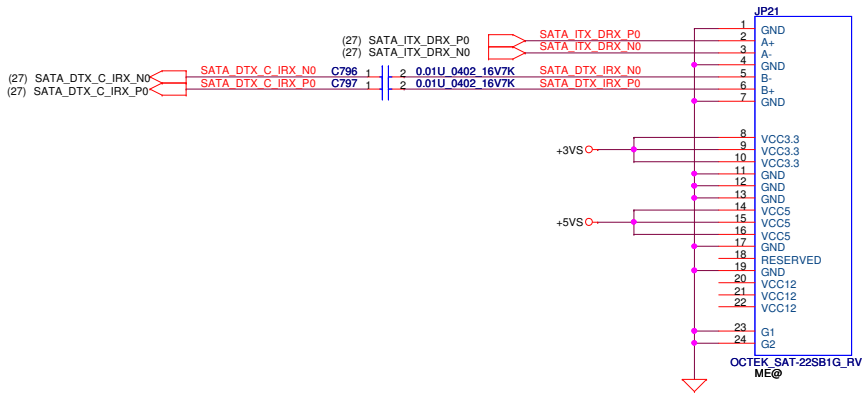
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title BCM5787MKML		
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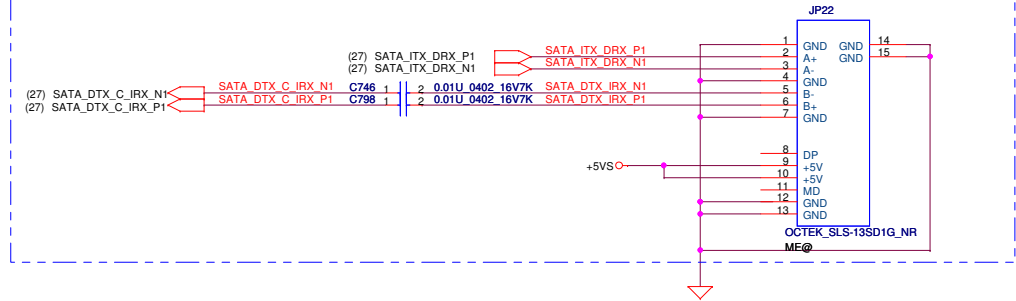
RJ45 CONN



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Issued Date				2007/10/15				Title			
Deciphered Date				2008/10/15				LAN CONTROLLER			
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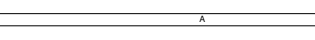
SATA ODD Conn.



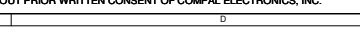
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Issued Date		2007/10/15		Deciphered Date		2008/10/15		Title						
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								Size B	Document Number	KIWA5/6 LA-5081P				Rev 0.4
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0308_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680p

For Layout:
Place decoupling caps near the power pins of SmartAMC device.



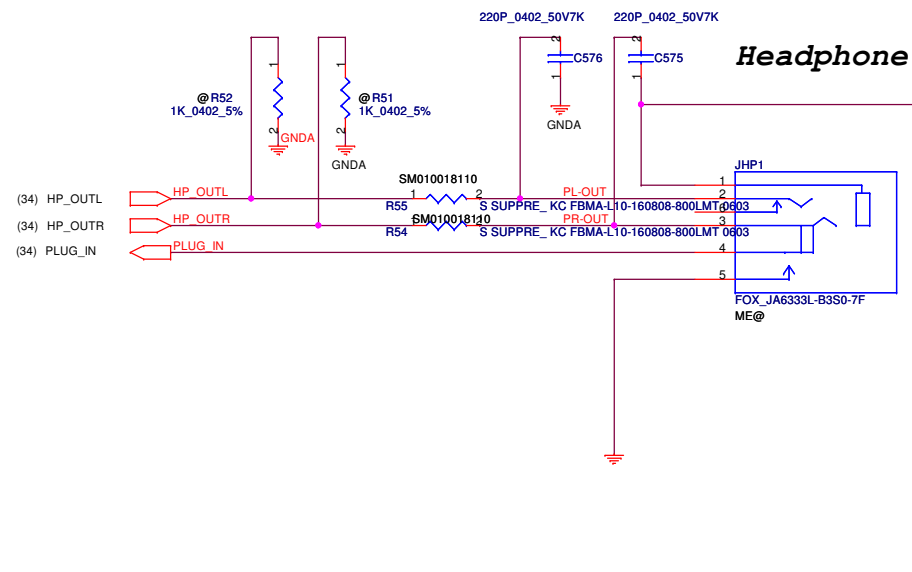
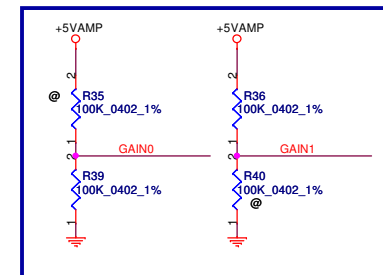
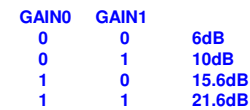
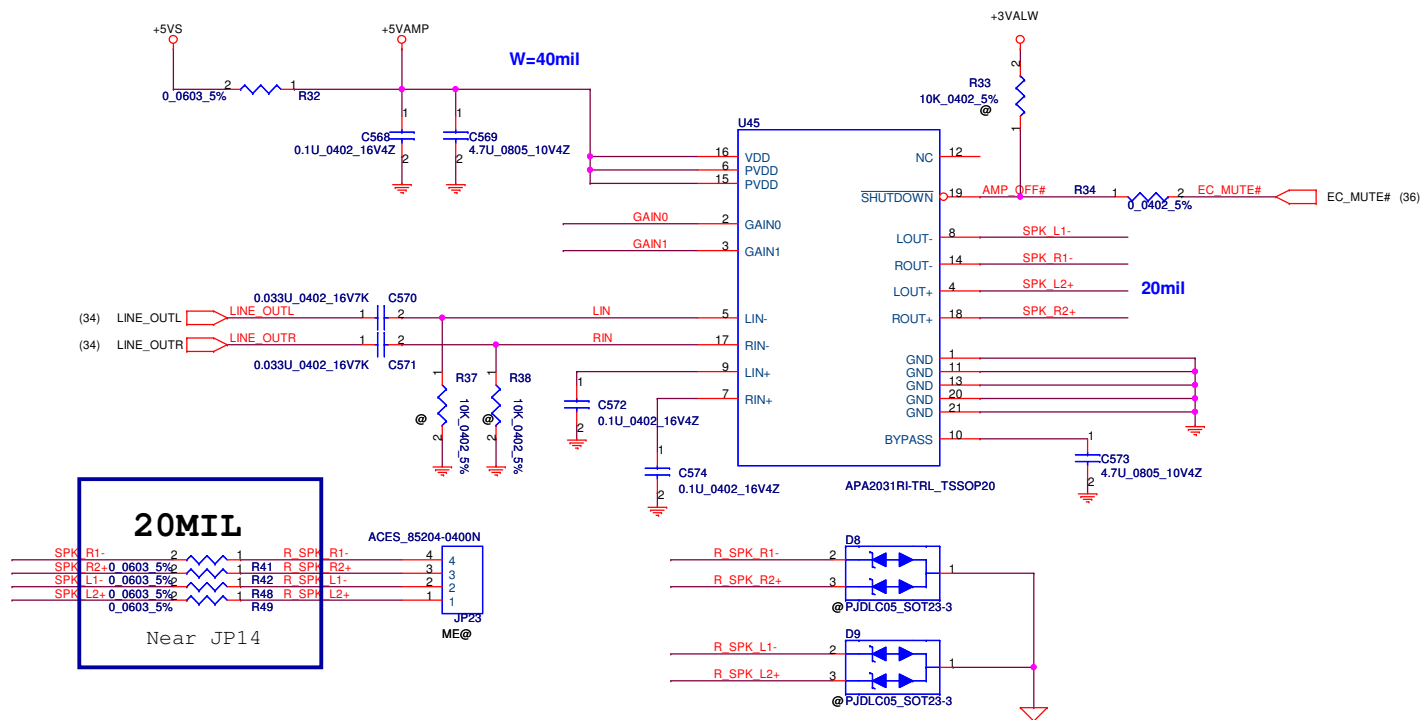
(3.33V)
250mW



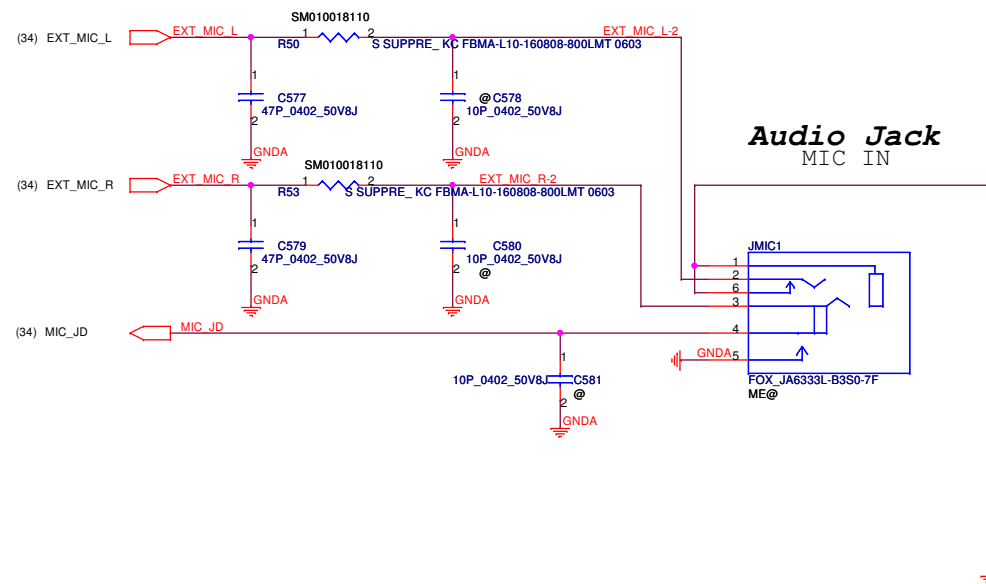
Place these C and R around AGND and DGND,
then choose the one which is close to Codec
to populate

Compal Electronics, Inc.			
Title			
CX20561-AMOM Codec			
Size	Document Number		Rev
Custom	KIWA5/6 LA-5081P		0.4
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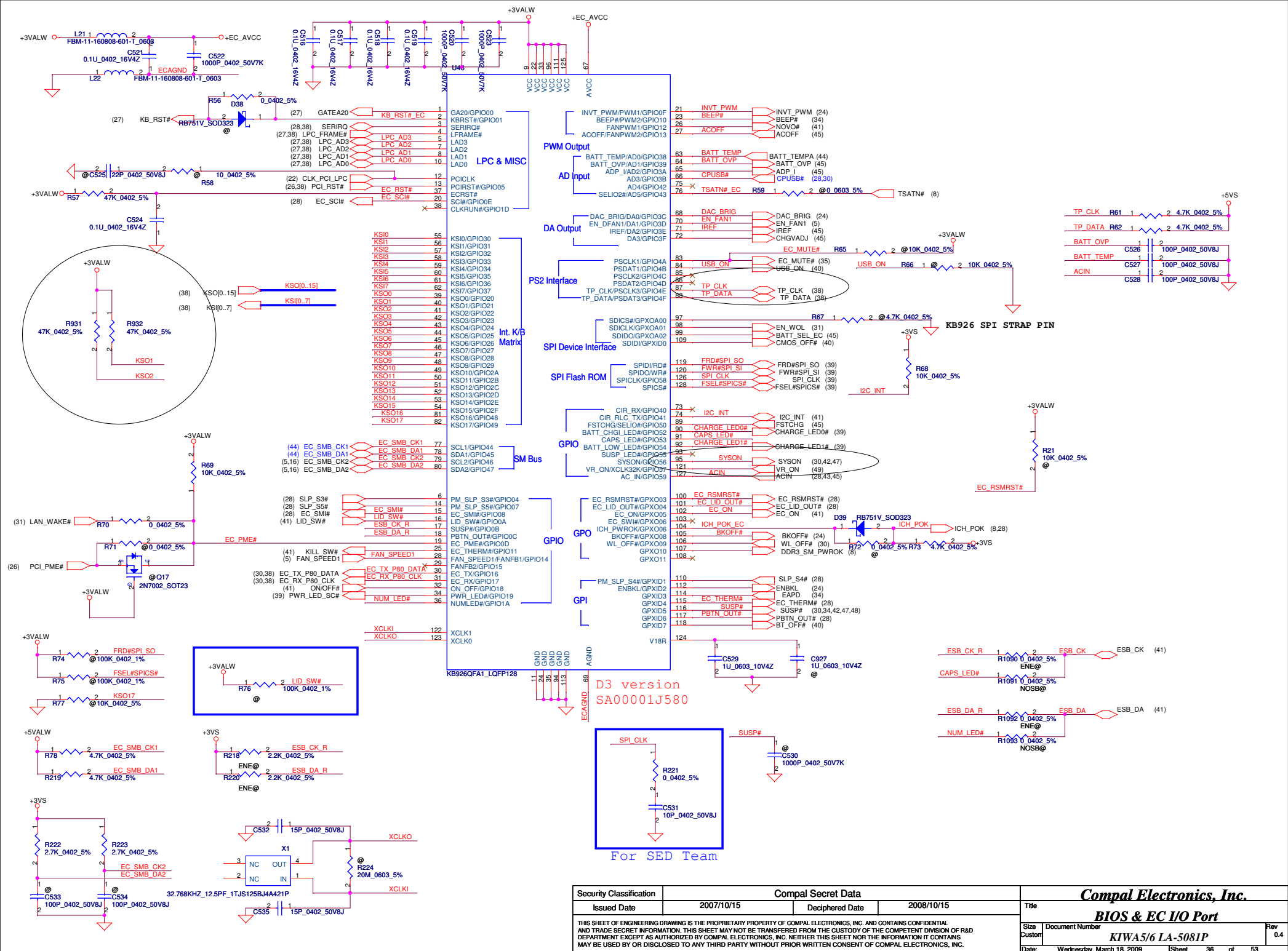
Speaker Connector



Audio Jack



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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	AMP,Audio speaker CONN
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				Custom	
				Date: Wednesday, March 18, 2009	

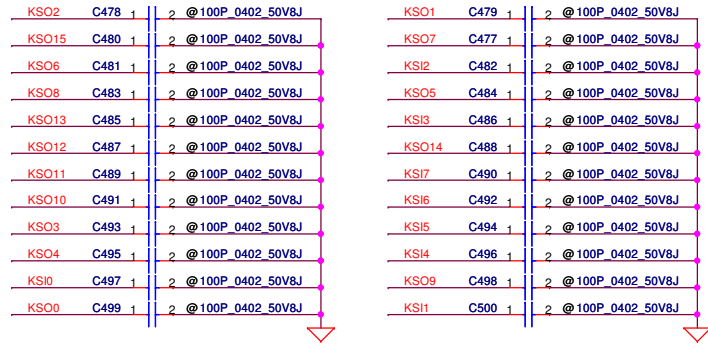


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				Custom	0.4
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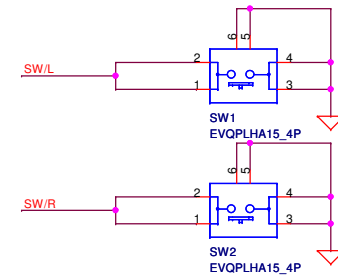
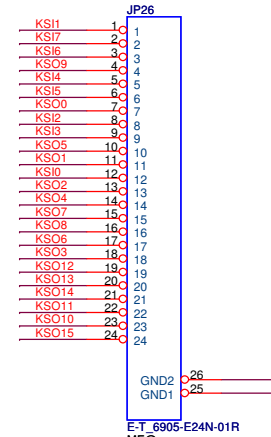
Source:SP010001E00
2nd source:SP010001F00
30 pin

INT_KBD Conn.

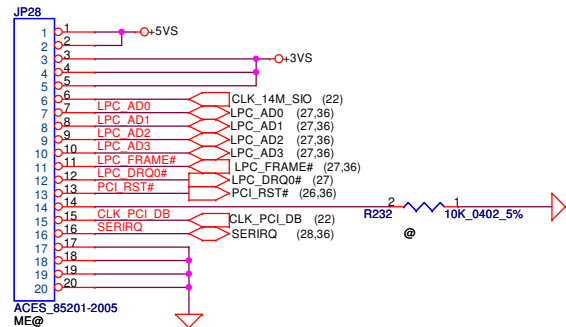
KS[0..7] (36)
KSO[0..15] (36)



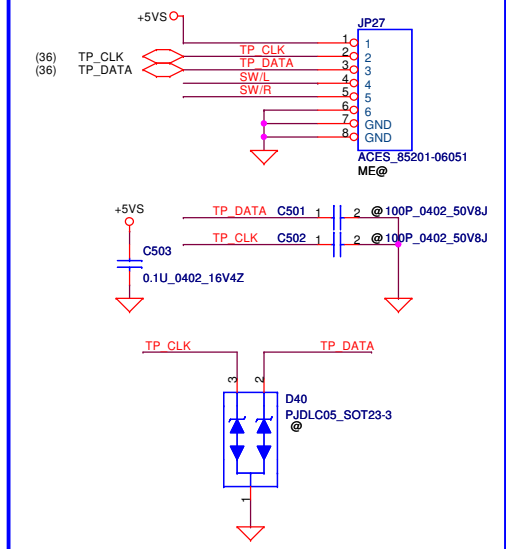
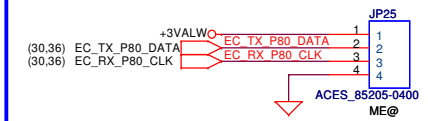
CONN PIN define need double check



FOR LPC SIO DEBUG PORT

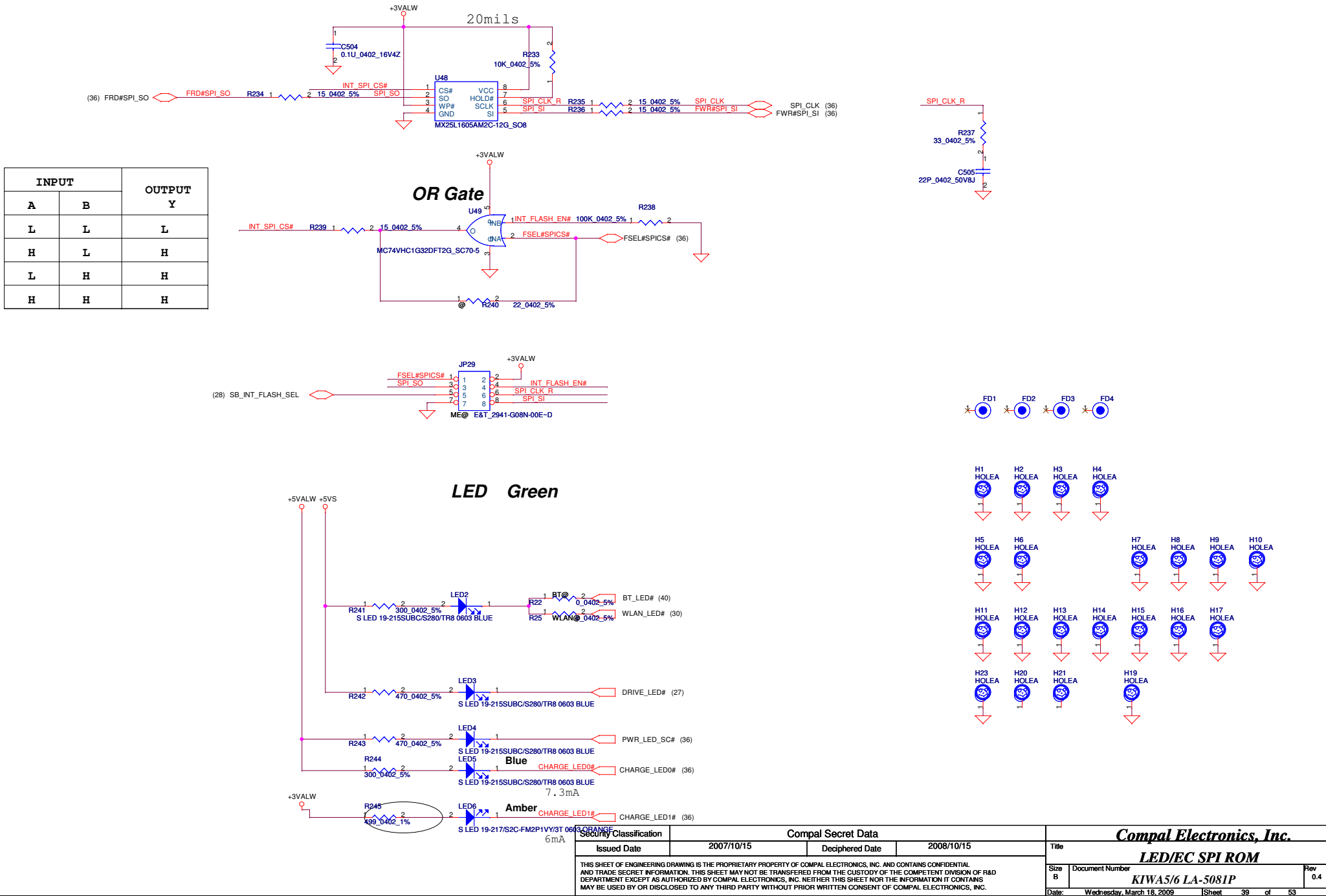


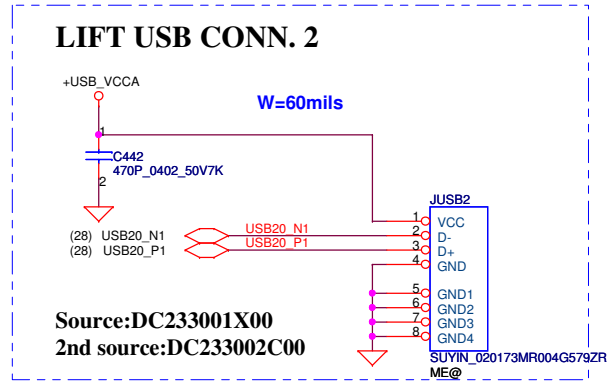
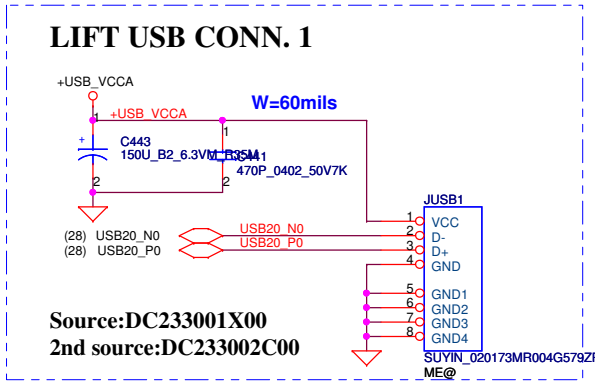
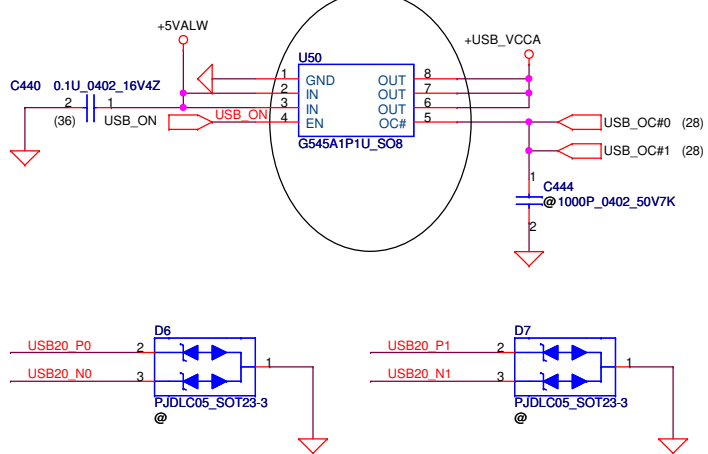
EC DEBUG PORT



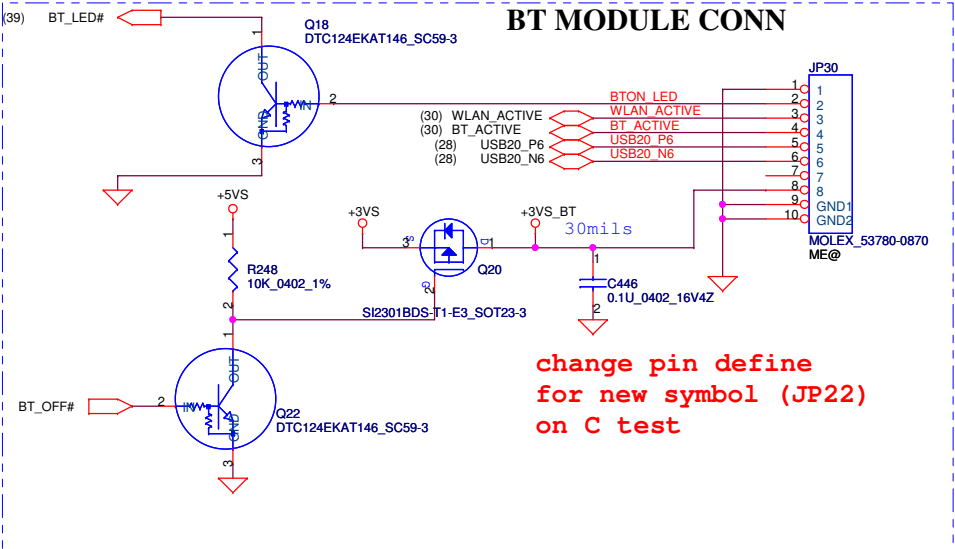
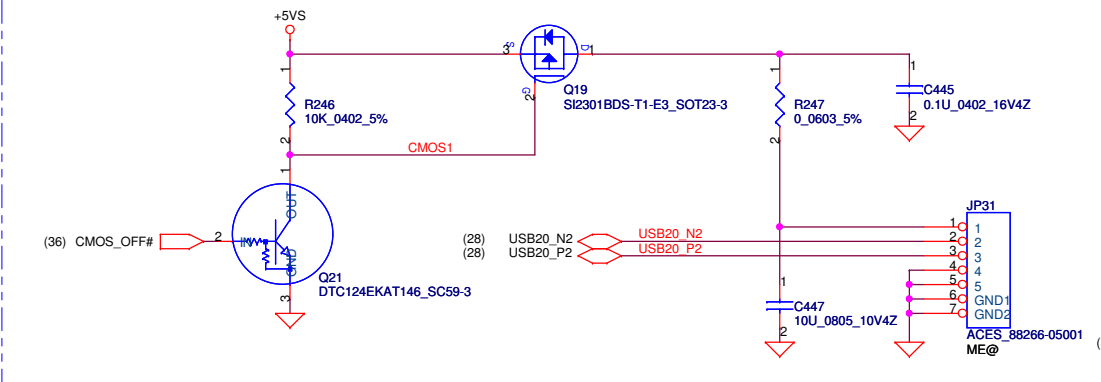
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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				Rev	0.4

FOR EC 16M SPI ROM

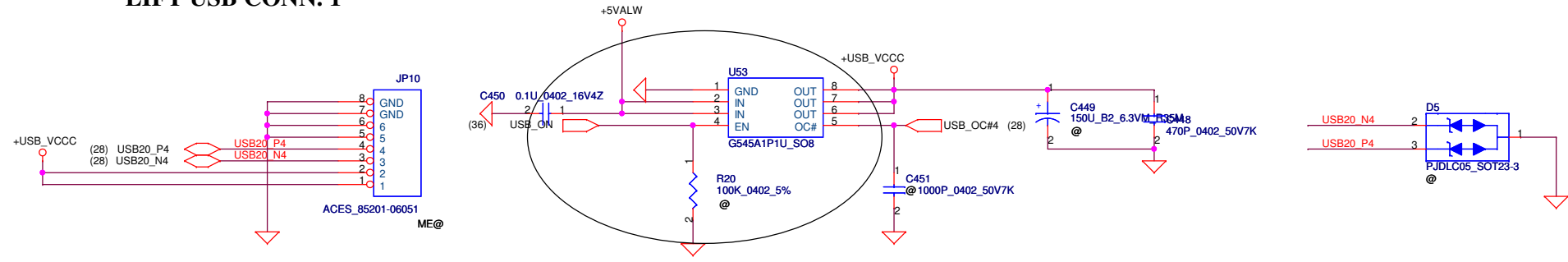




CMOS Camera Conn

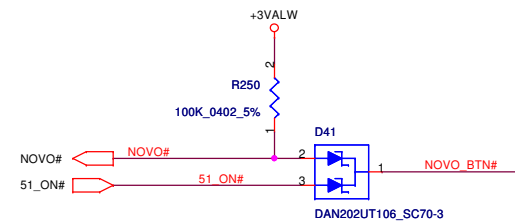


LIFT USB CONN. 1



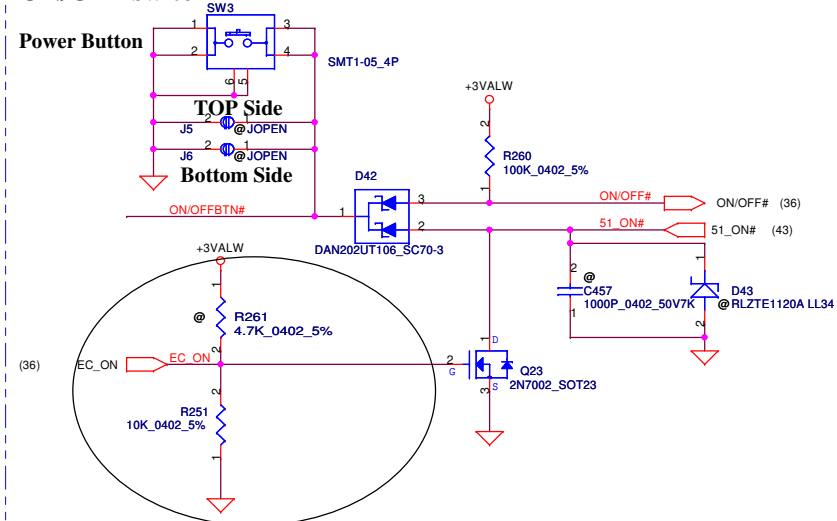
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(36)
(43)

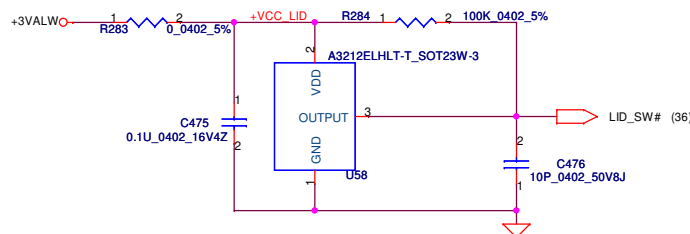


ON/OFF switch

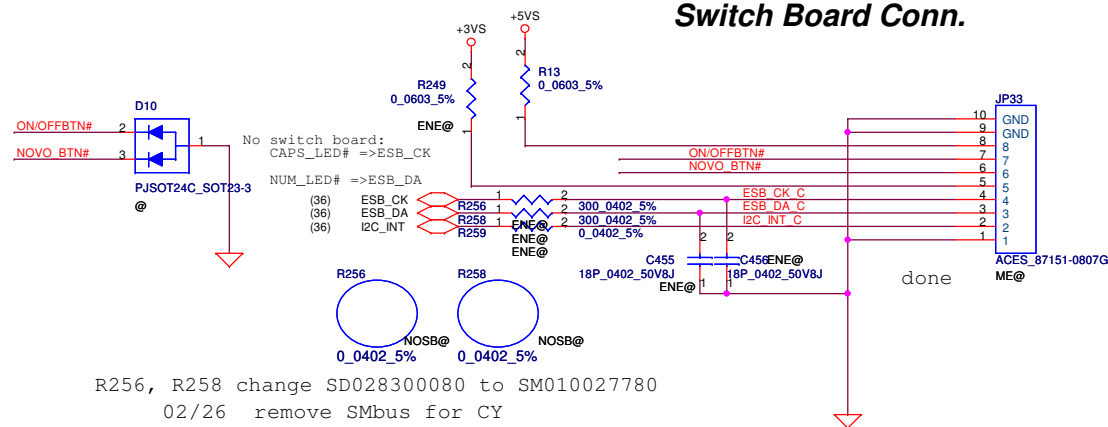
Power Button



Lid Switch

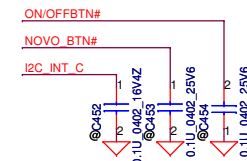
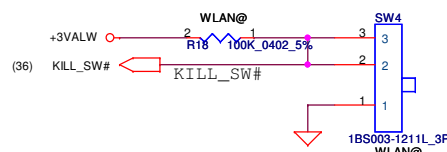


Switch Board Conn.



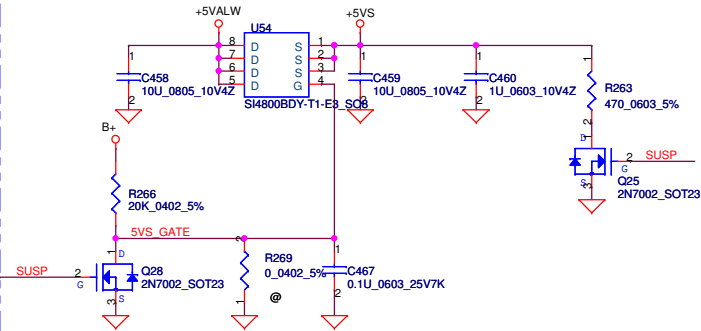
R256, R258 change SD028300080 to SM010027780
02/26 remove SMBus for CY

Kill Switch

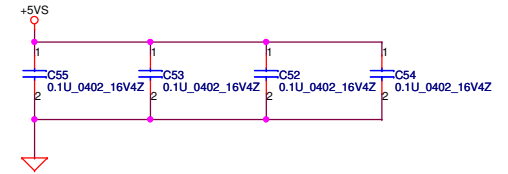
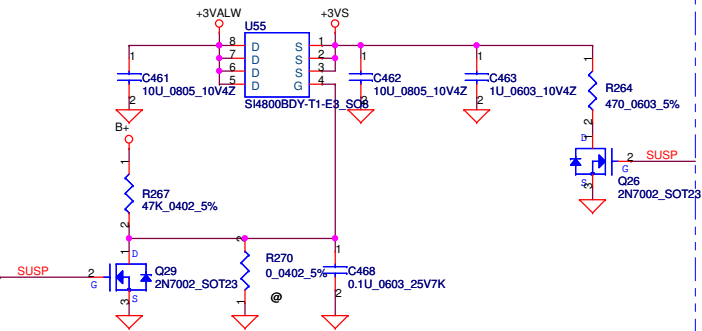


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				Size Custom
				Document Number
				Rev 0.4
				Date: Wednesday, March 18, 2009
				Sheet 41 of 53

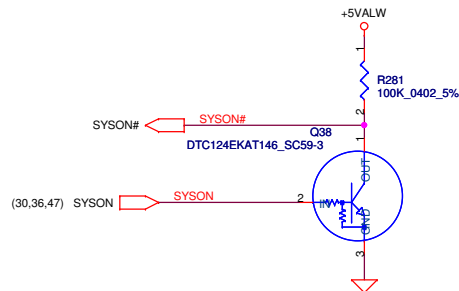
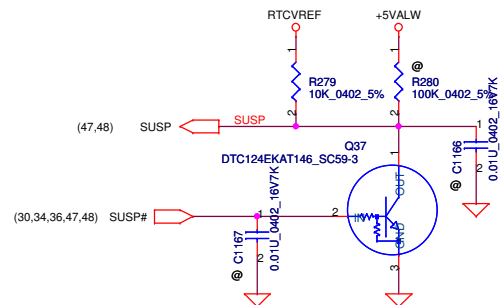
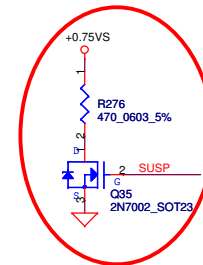
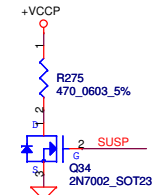
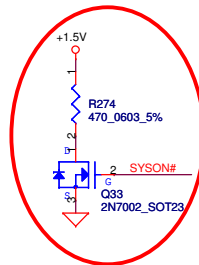
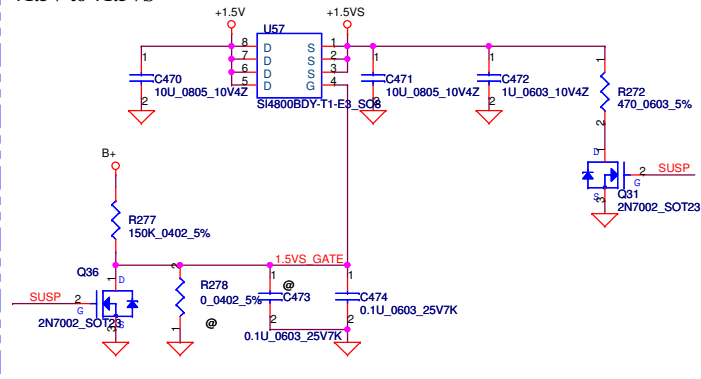
+5VALW TO +5VS



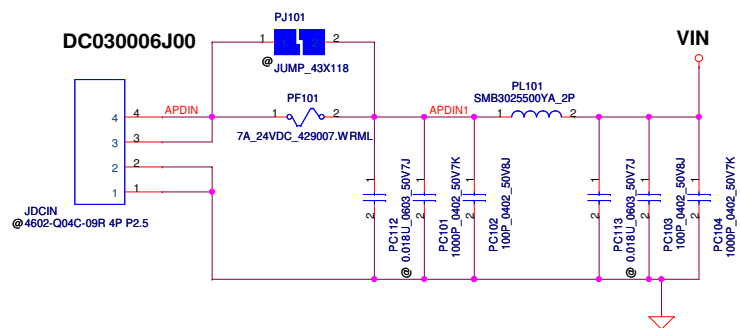
+3VALW TO +3VS



+1.5V to +1.5VS

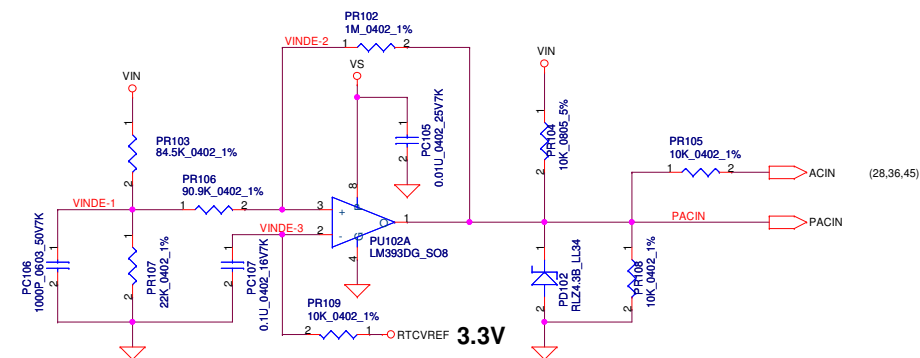


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Size	Document Number	KIWA5/6 LA-508IP		Rev	0.4
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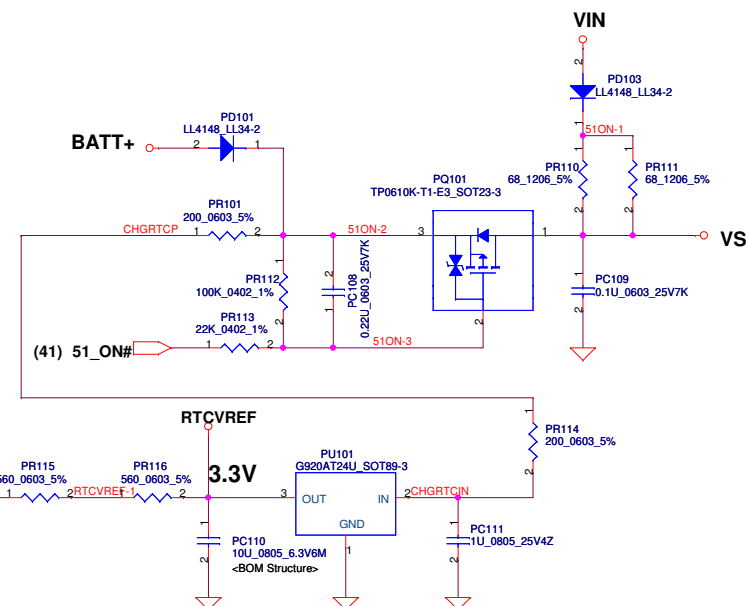


Vin Detector

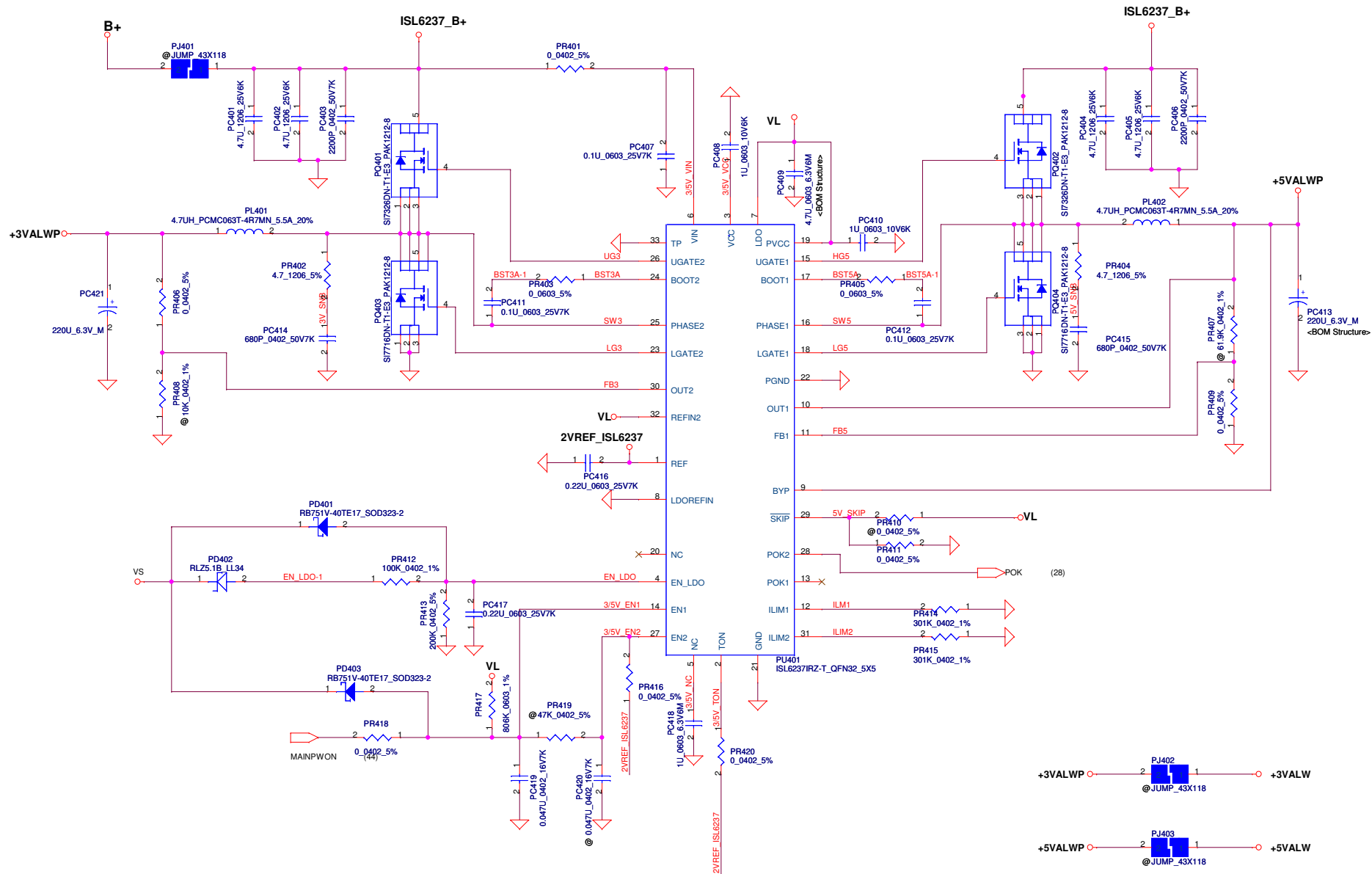
High 17.944 17.706 17.470
Low 16.242 16.027 15.808



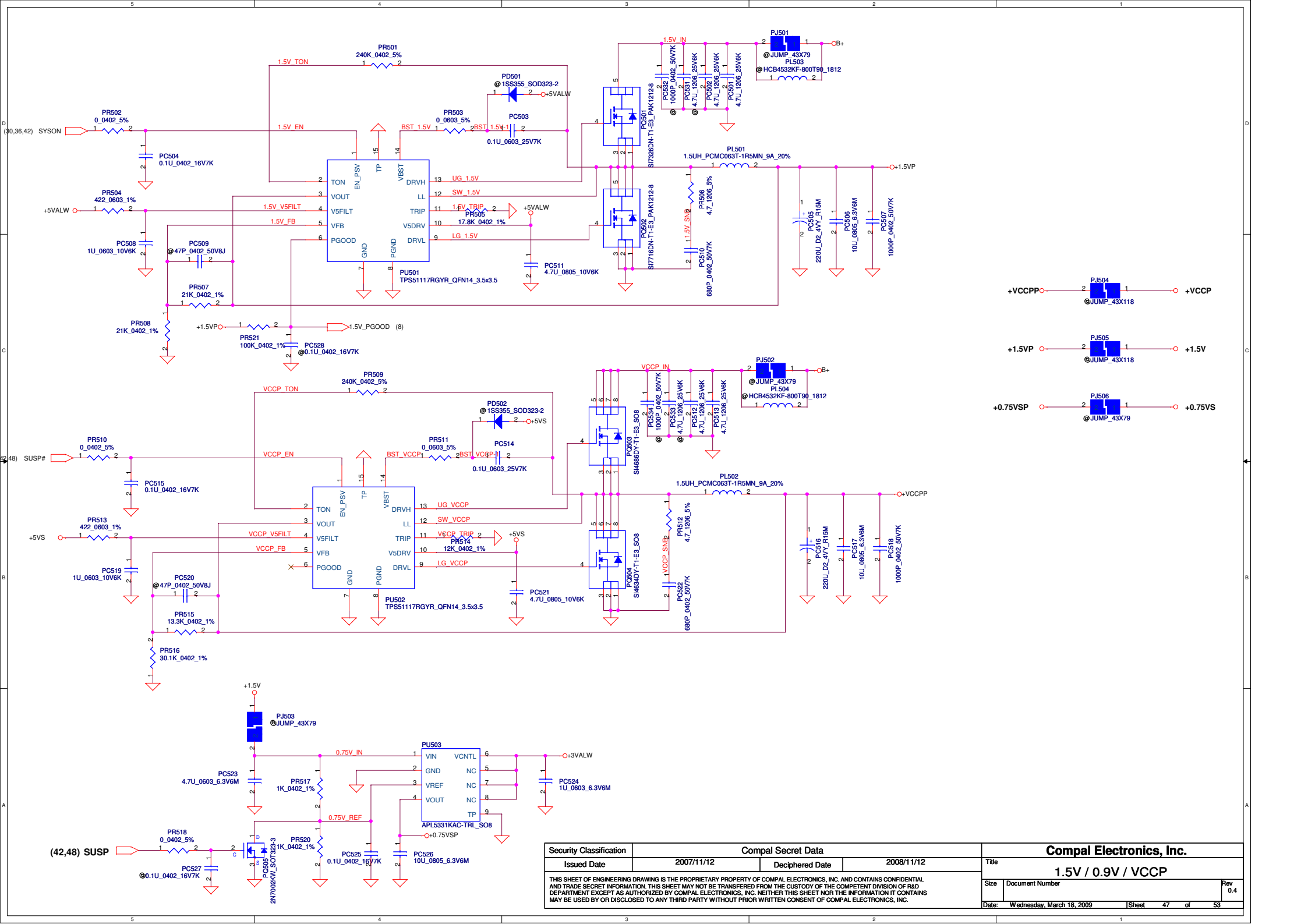
RTC Battery



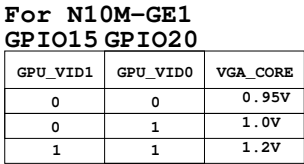
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Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title	
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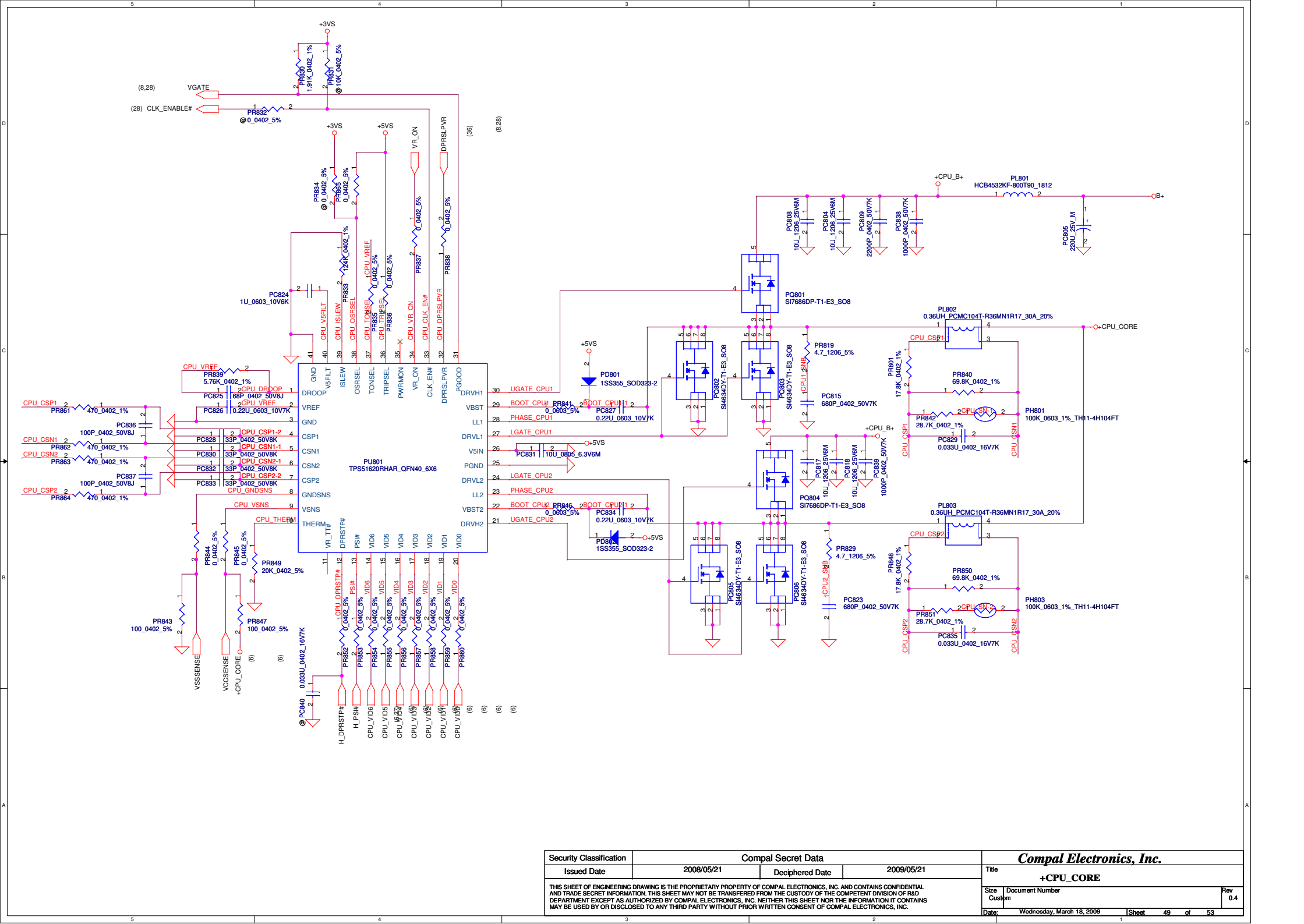


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PR622=>2.21K
PR629,PR630,PC625,PQ606,PR620=>un-pop
PR621,PR624,PC632,PQ607,PR618=>un-pop

Compal Electronics, Inc.		
Title VGA_CORE/1.8V/1.1VS		
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		modify battery select circuit			add PQ312 and PR338	2009.01.14	
2		change +1.1VS voltage to +1.05V			change P622 to 2.21K only for N10M-GS(40nm)		
3							
4							
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17							
18							
19							
20							
21							

NO			DATE			PAGE	MODIFICATION LIST	PURPOSE
1	12/10	39	Remove D11, and add R22, R25					
	12/10	36	change PWR_LED_SC# from U46.38 to U46.34					

A

B

C

D

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Size B

Document Number KWAX_LA-5082P

Title HW PIR

Rev 0.4

Compal Electronics, Inc.

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	1/15	39	modify H19 hold size, and change the H5、H6 and H19 hold type.	
		42	add 4 CAPs C52, C53, C54 and C55 for EMI.	
		35	change C572 and C574 footprint from 0603 to 0402.	
		34	add R44 for BEEP# test	
2	1/16	30	Remove one Mini-PCIE function! (Connector Side) Remove component is JP18, R363, R364, R367, R369, R371, R373, R375, R377, R378, R379, R380 and R383 Remove 3G function! Remove component is JP14, D12, R6, C6, C7, R7 and D13	
		28	Remove one Mini-PCIE function!(SB side) Remove component is C884 and C885	

Compal Electronics, Inc.

HW PIR

Size BDocument NumberKIWAX_LA-5082PRev 0.4

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/16	06	add R1089, C1162 and H_DPRSTP#_R	
			add C1163, C1164,and C1165 for EMC request.	
		08	change H_DPRSTP# to H_DPRSTP#_R	
		19	P19 add Bom structure 40nm@ GPU and 55nm@ GPU	
			R999 change to 24.9K	
		23	add R1095 pull high	
		35	swap HP_OUTL and HP_OUTR	
		36	add R1090, R1091, R1092, R1093	
			CAPS_LED#, NUJM_LED#, ESB_CK_R, and ESB_DA_R	
		41	add R256, R258 Bom configuration	
			Remove CY SMBus	
		42	add C1166, C1167 for EMC request.	
2	3/16	28	change PCIE Port1 to Port3	
		30	change PCIE Port1 to Port3	

Compal Electronics, Inc.

HW PIR

Size B

Document Number

KIWAX_LA-5082P

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