

MODEL NAME : *PALB0*
PCB NO : *LA-6801P (DAB00000410)*
BOM P/N : *46198531L01 -->R3*
46198531L02 -->R1
46198531L03 -->R3
46198531L04 -->R1

Dell/Compal Confidential

Schematic Document

Specter (Huron River)

Sandy Bridge (PGA) + Cougar Point (standard)

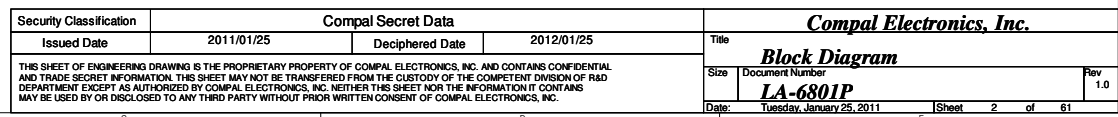
DISCRETE VGA N12E-GE-B (optimus)

2011-01-25

Rev: 1.0

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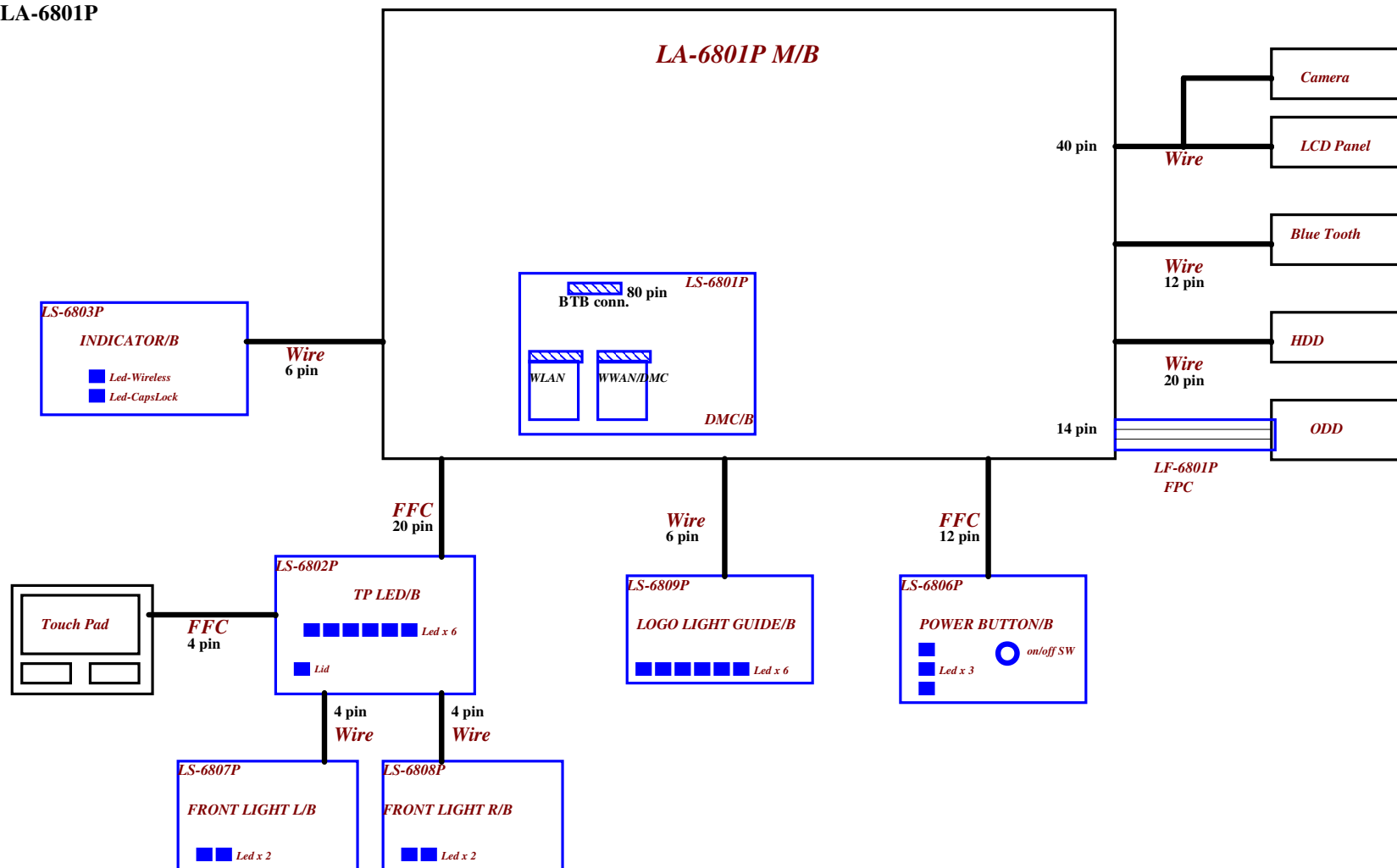
Project Code : PALB0
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Project Code : PALB0

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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID_min	VAD_BID_typ	VAD_BID_max	EC_AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

PCH

USB PORT#	DESTINATION
0	None
1	JUSB1 (2.0 Ext Left Side)
2	Bluetooth
3	CAMERA
4	JMINI1 (WLAN)
5	JMINI2 (WWAN/DMC)
6	ELC 8051
7	None
8	None
9	None
10	None
11	None
12	None
13	None

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Thermal Sensor 1	Thermal Sensor 2	FFS	VGA Thermal Sensor	VGA	DMC	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB930			V									
EC_SMB_CK2 EC_SMB_DA2	KB930					V	V		V				
PCH_SML0CLK PCH_SML0DATA	PCH												
PCH_SML1CLK PCH_SML1DATA	PCH												V
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V			V		V	V	V	

Link

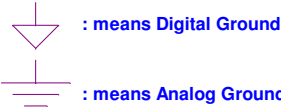
CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	MINI CARD-2 WWAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	USB 3.0		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

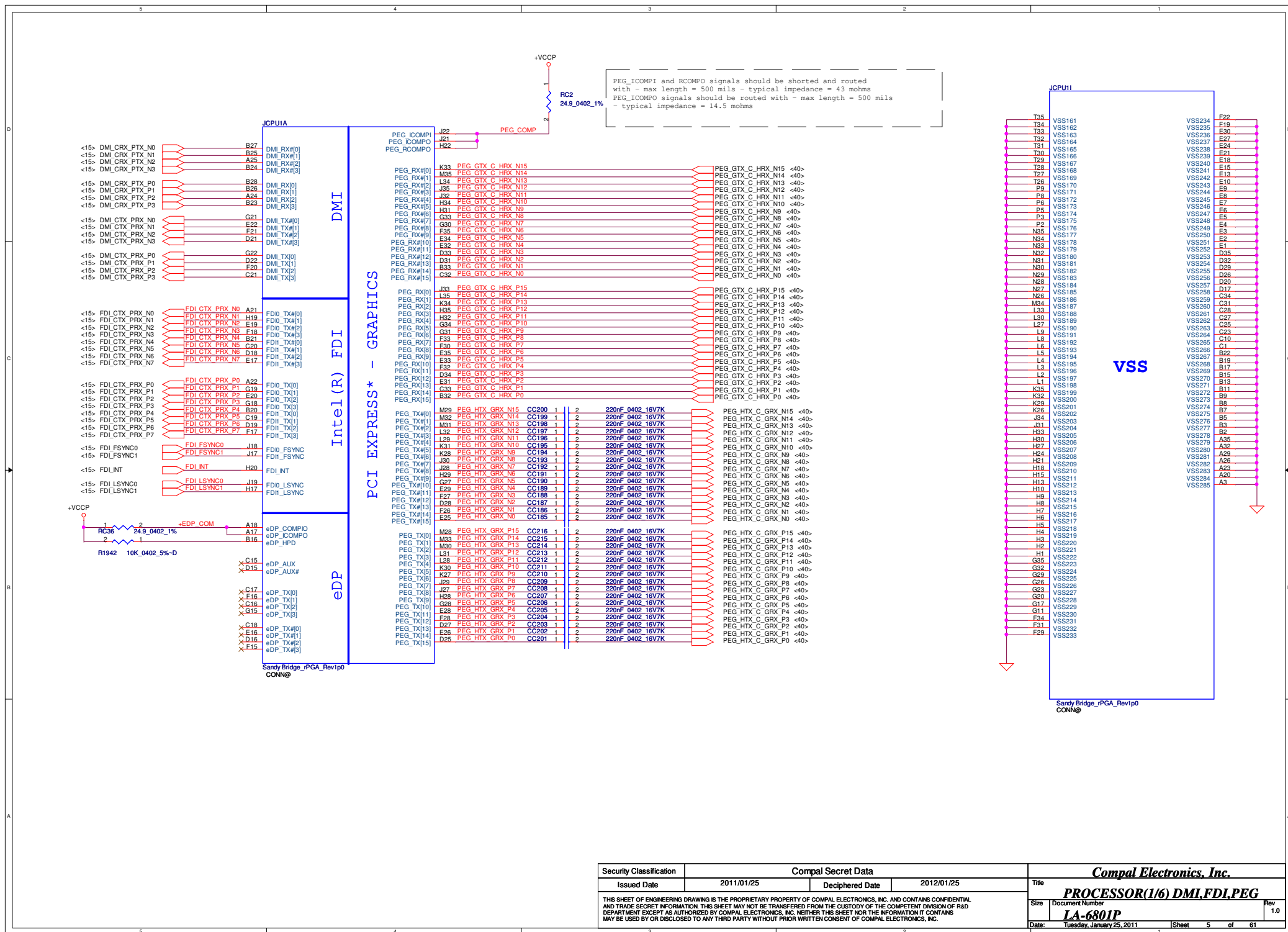
SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 WWAN/DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	USB 3.0
Lane 7	None
Lane 8	None

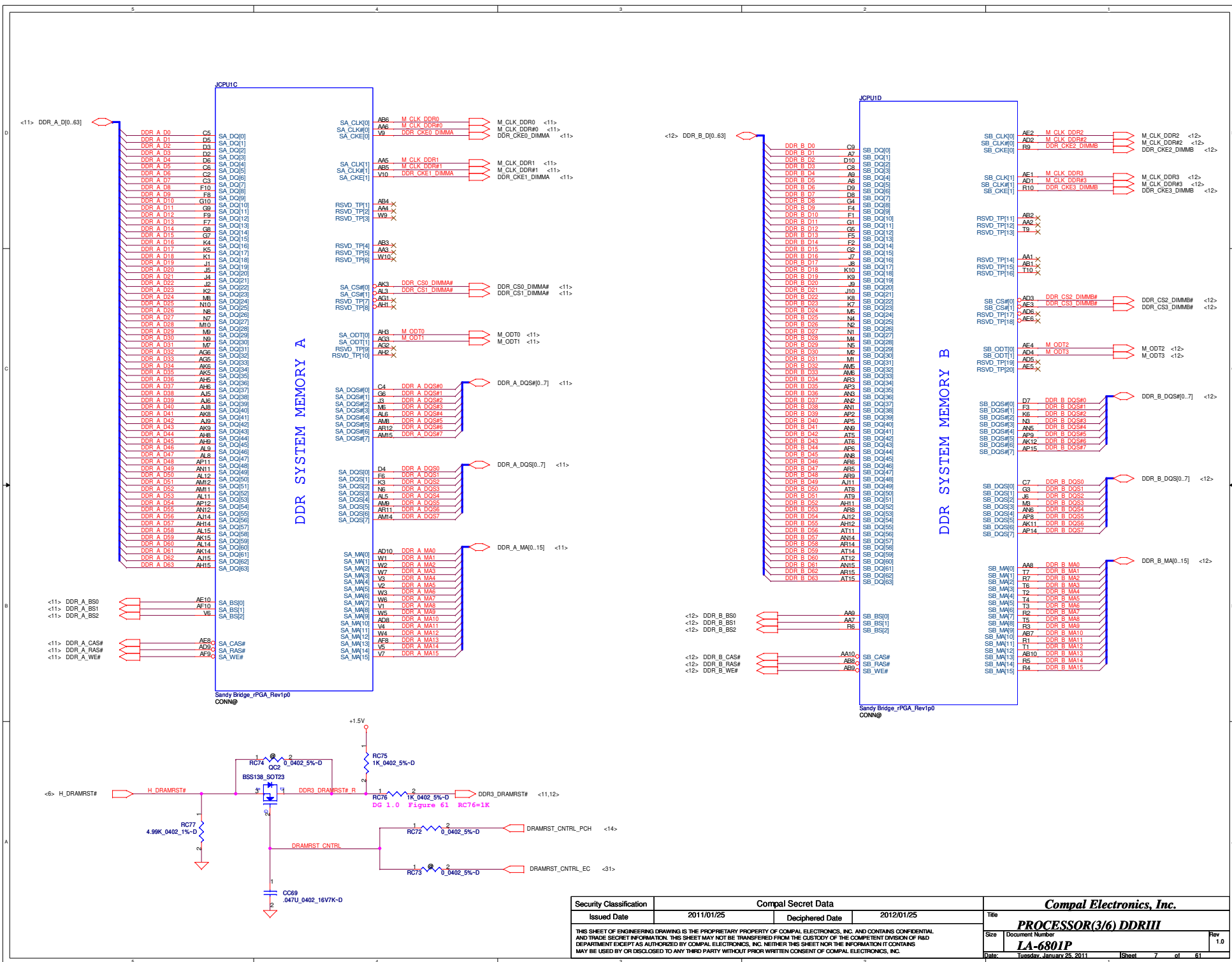
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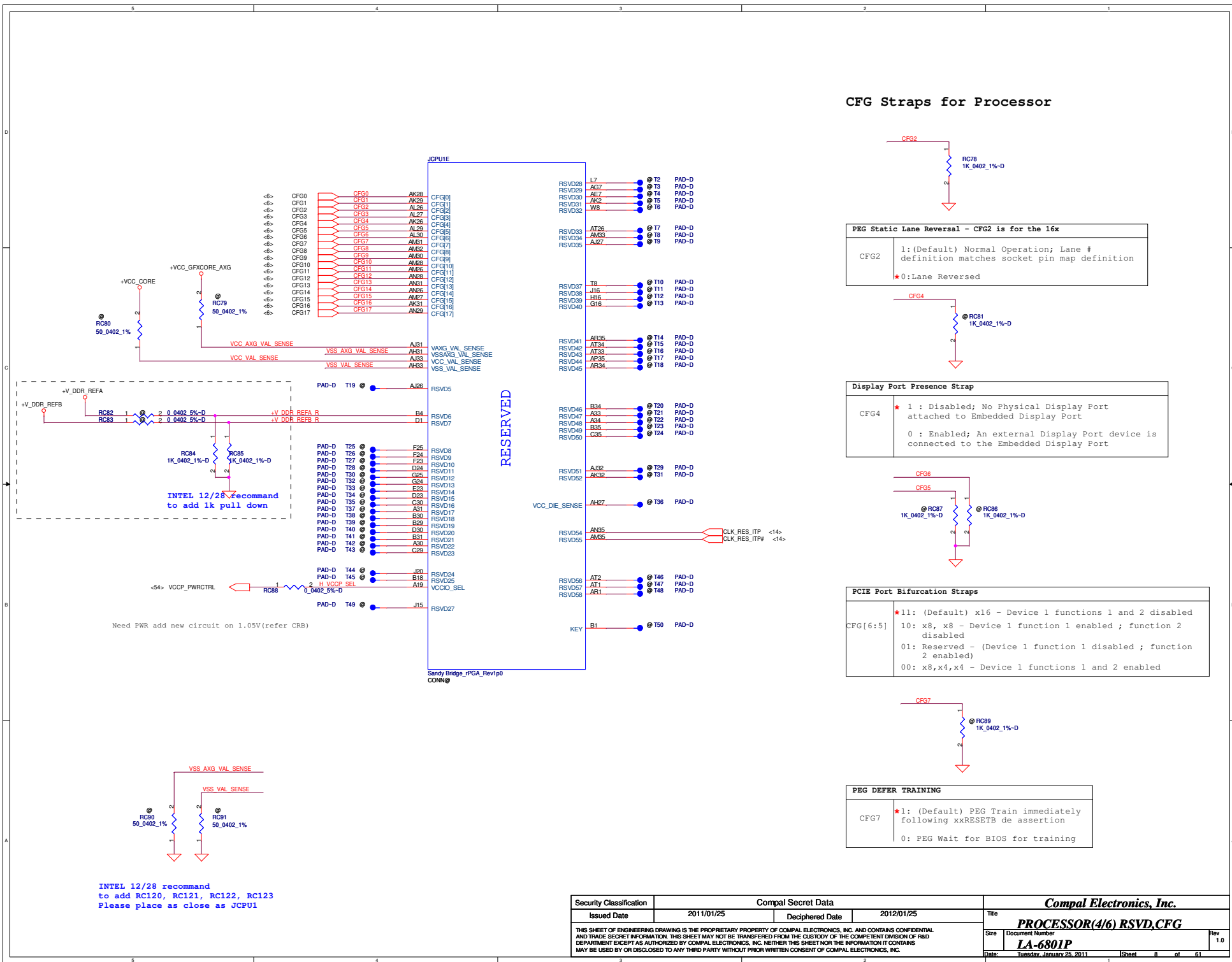


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CFG Straps for Processor

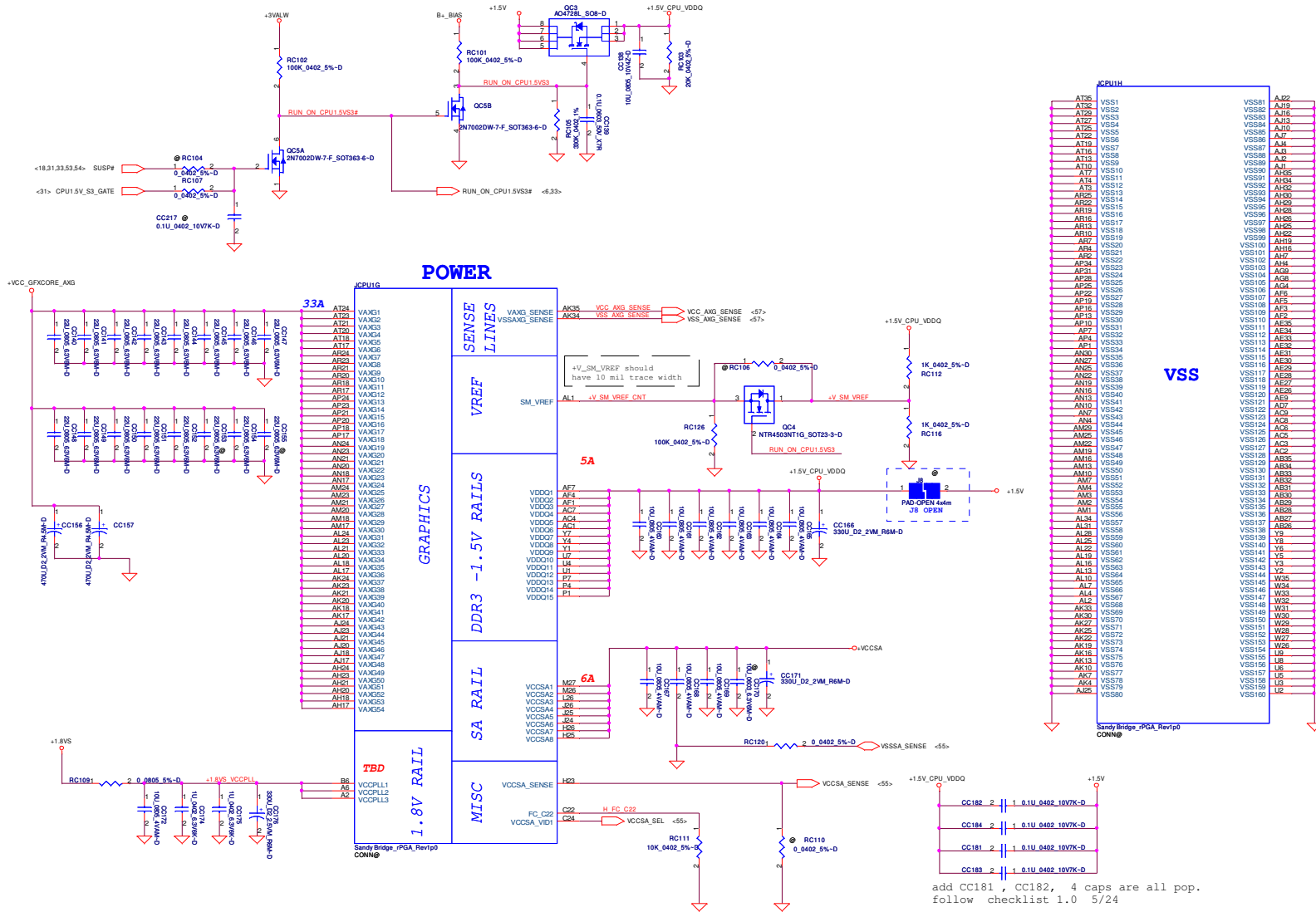
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition *0: Lane Reversed

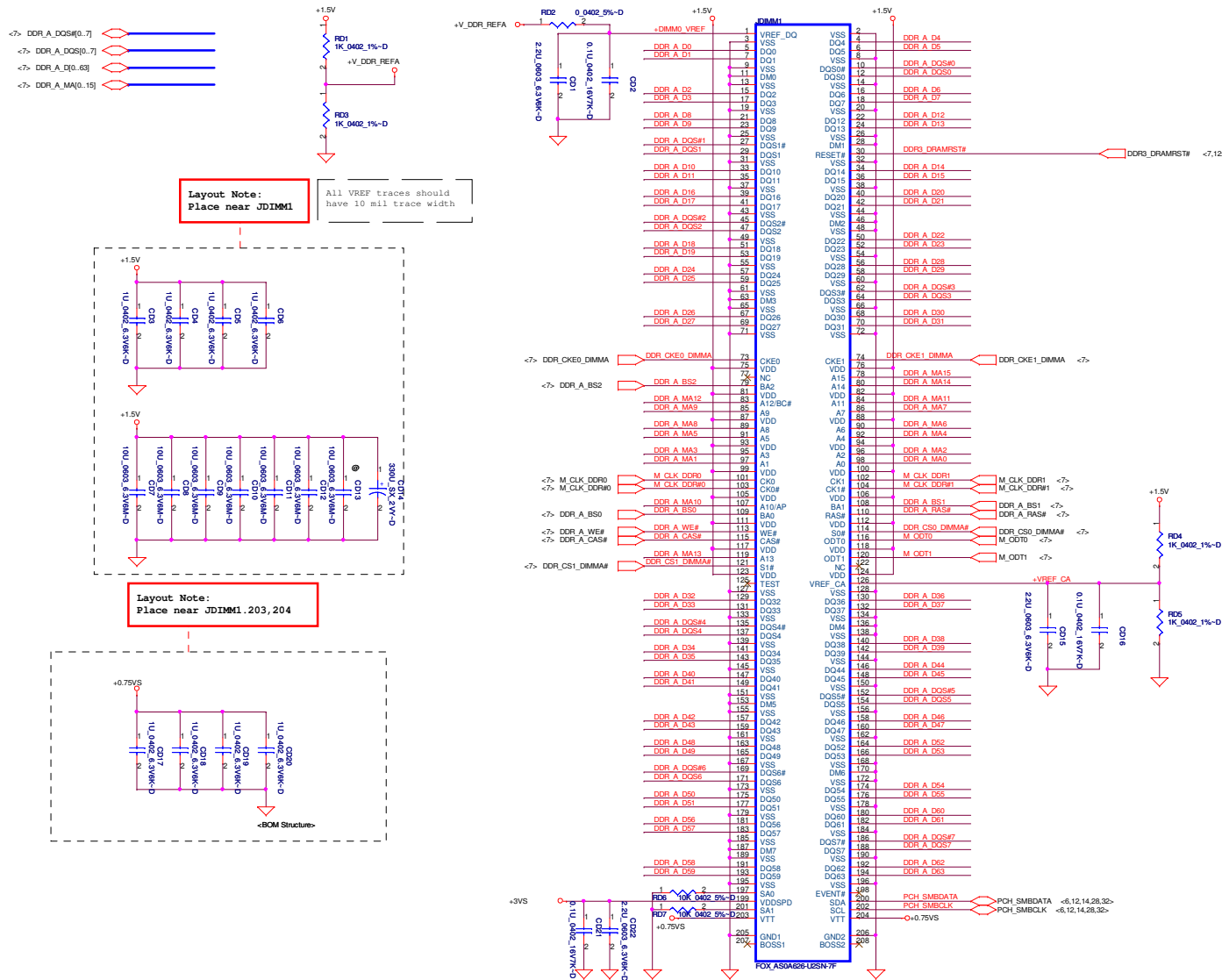
Display Port Presence Strap	
CFG4	*1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

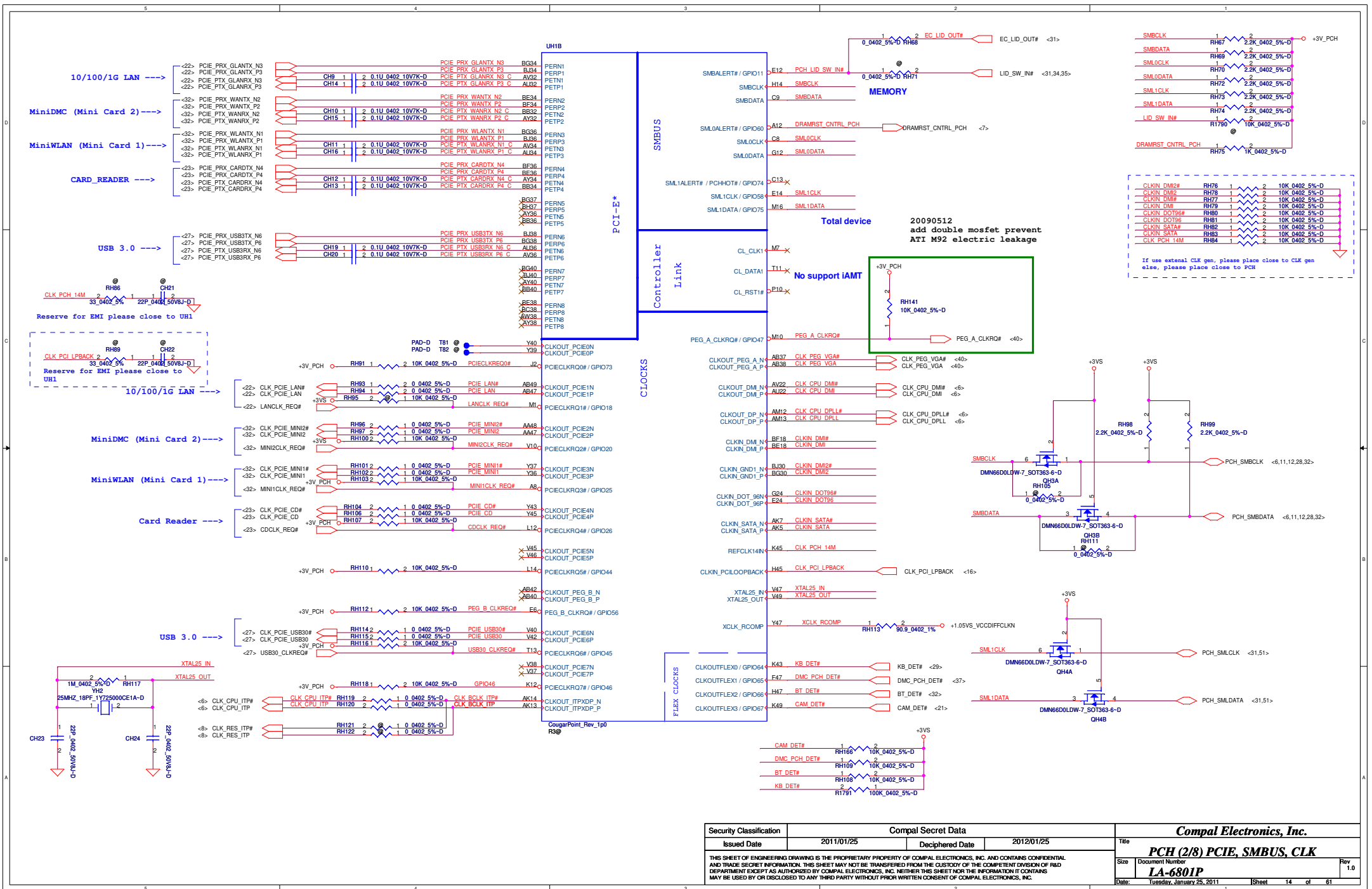
PEG DEFER TRAINING	
CFG7	*1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

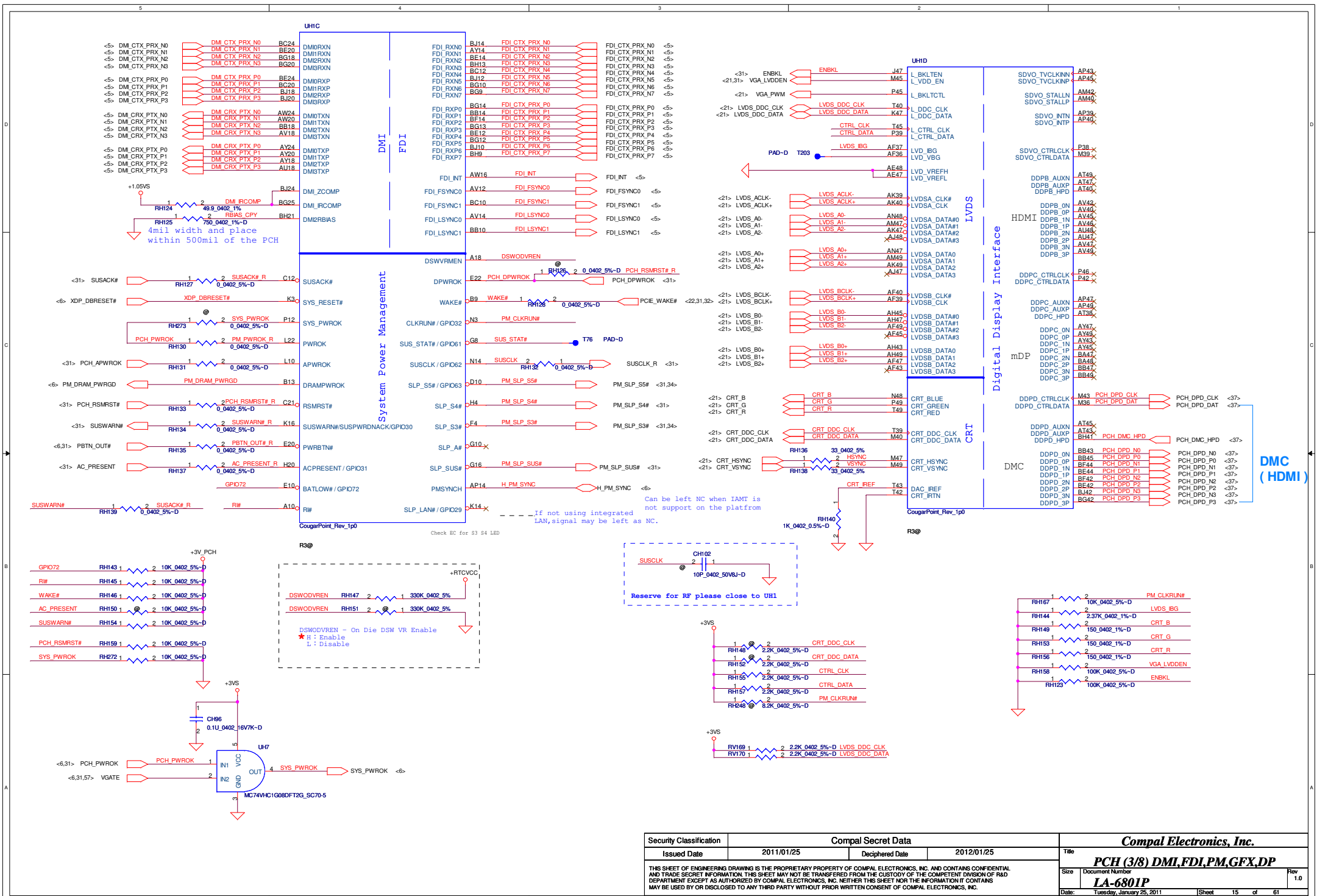
+1.5V_CPU_VDDQ Source



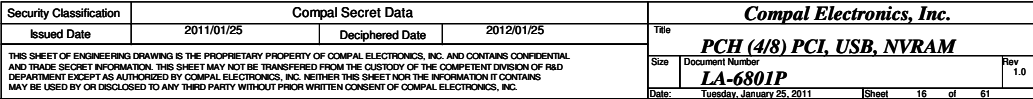


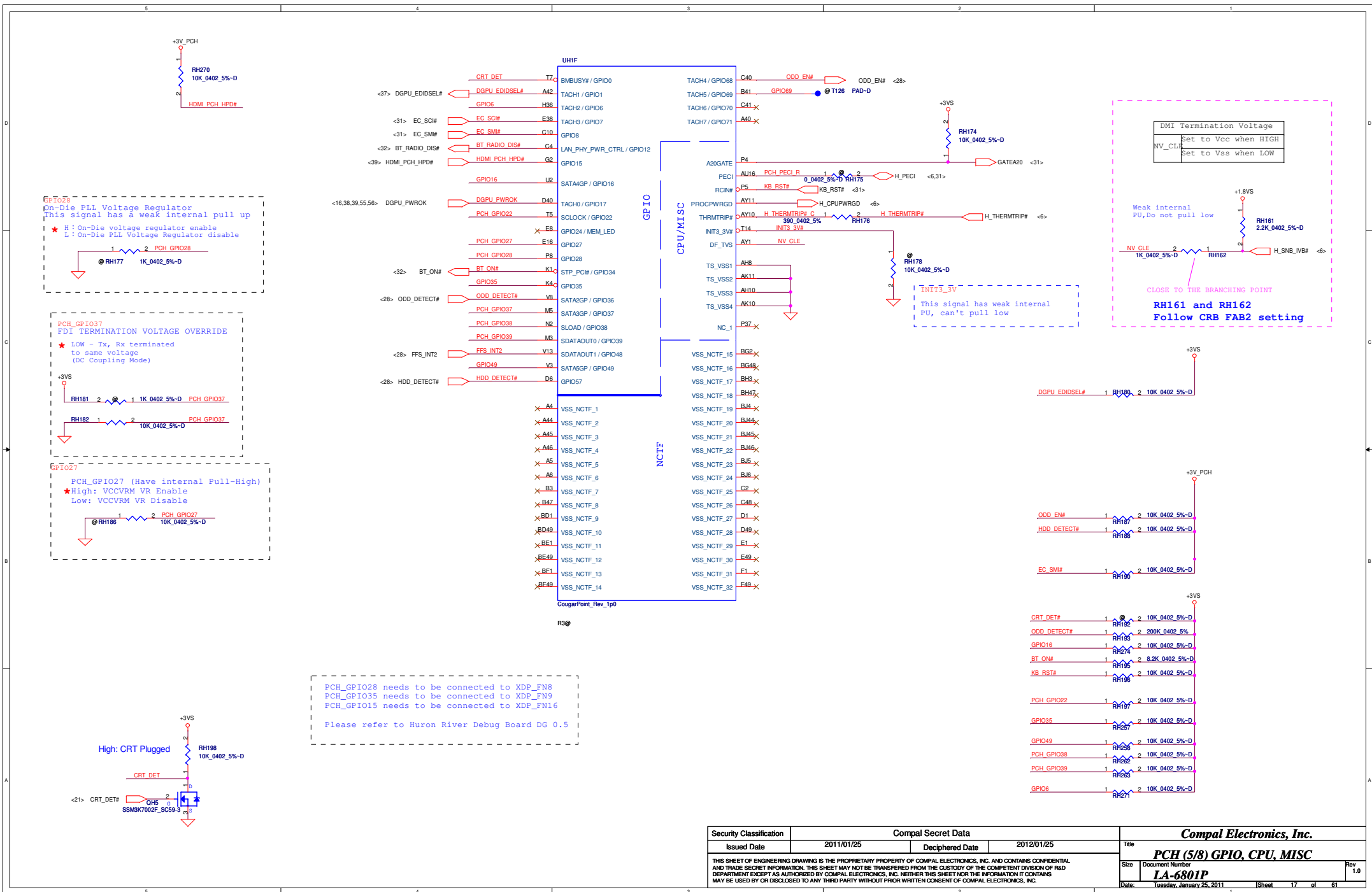
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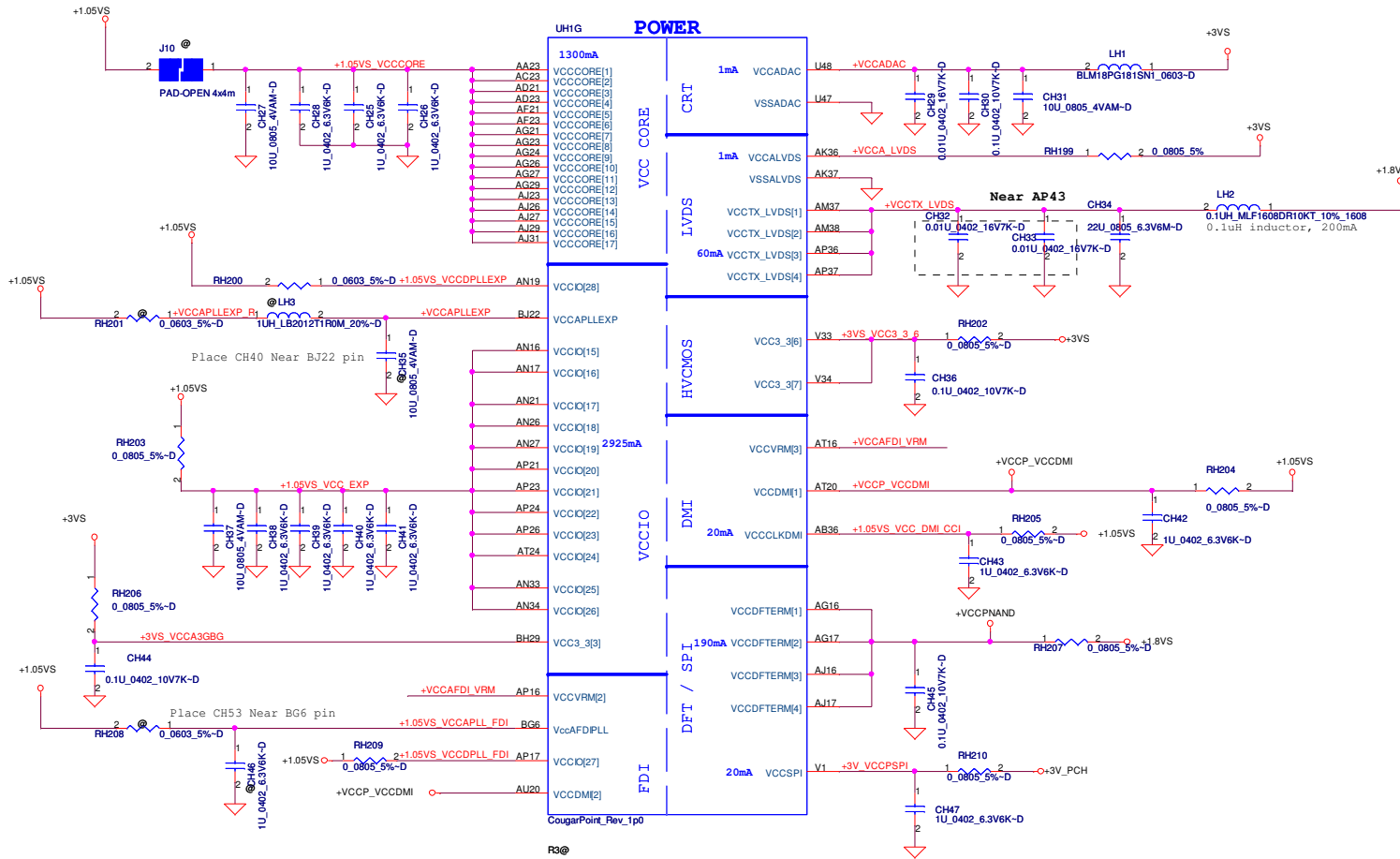


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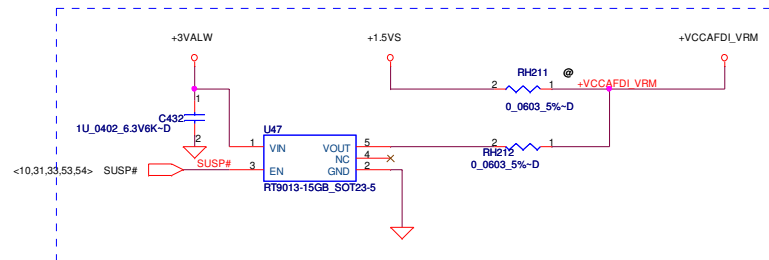


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PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADFLA	1.05	0.08
VccADFLB	1.05	0.08
VccCoxe	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

VCCVRM = 160mA detail waiting for newest spec

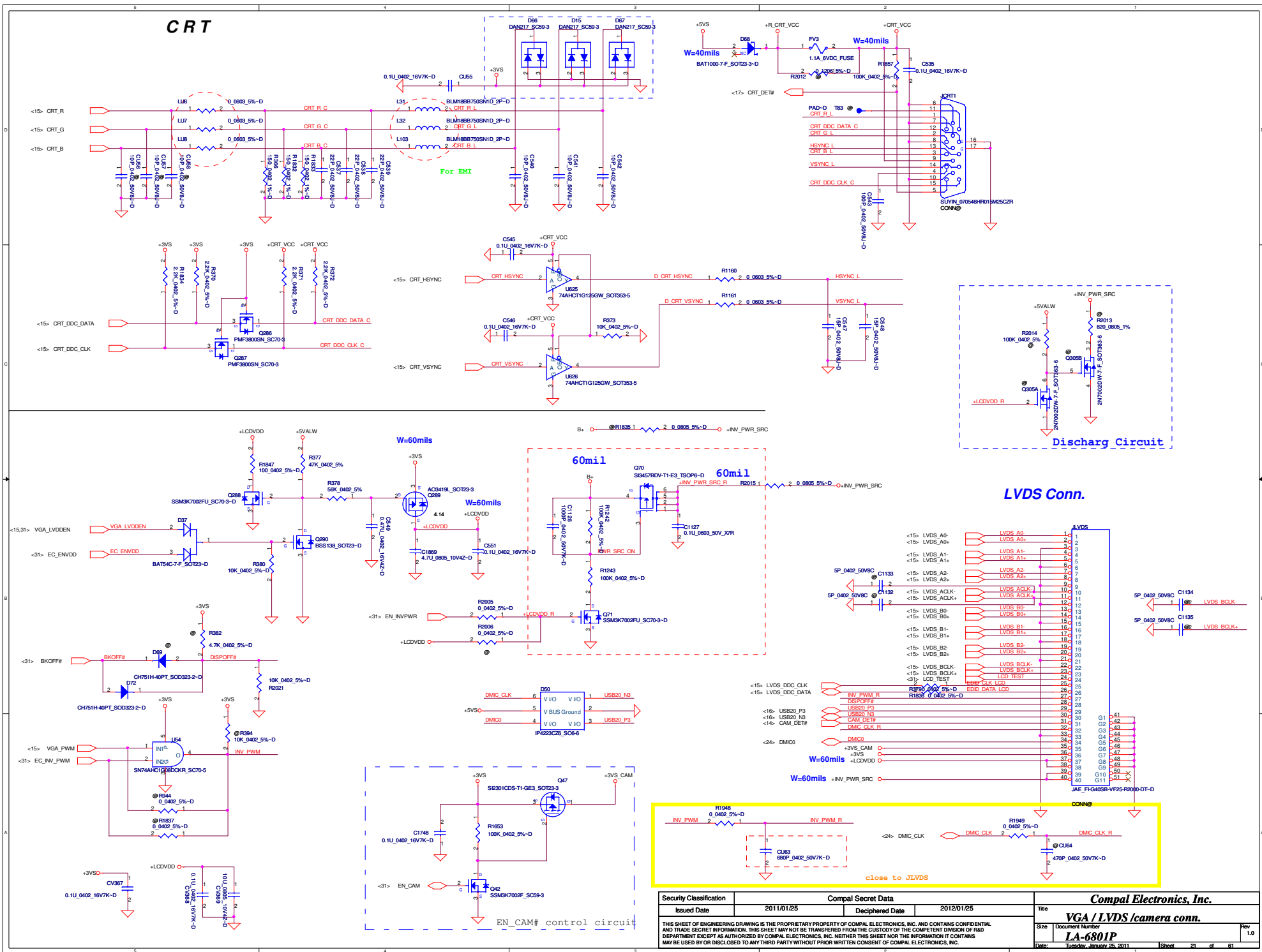


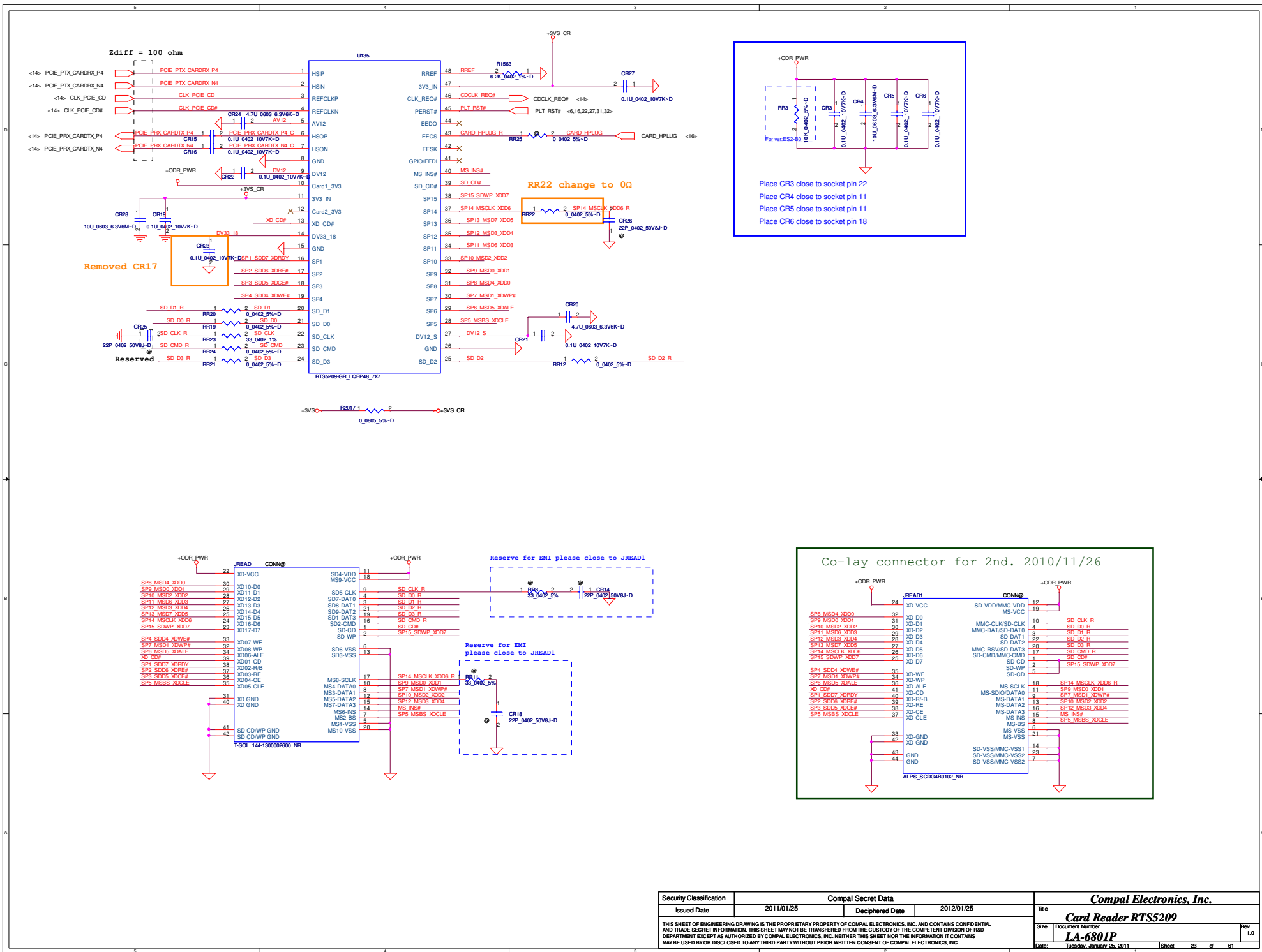
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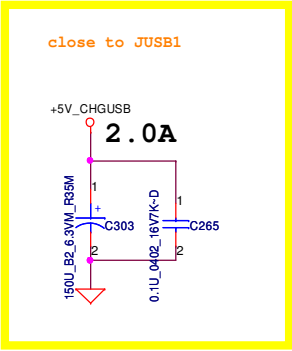
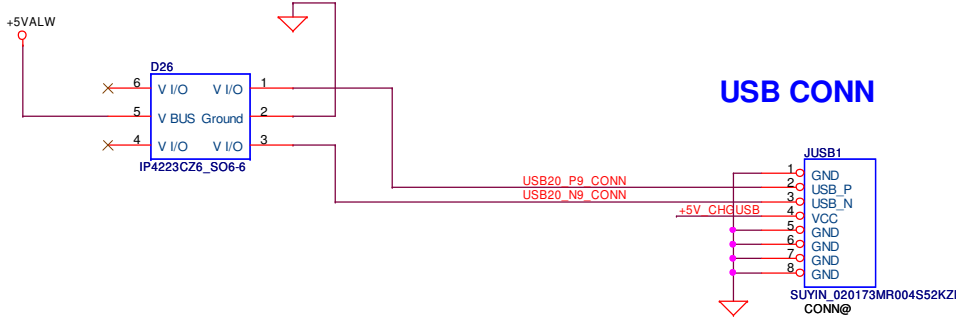
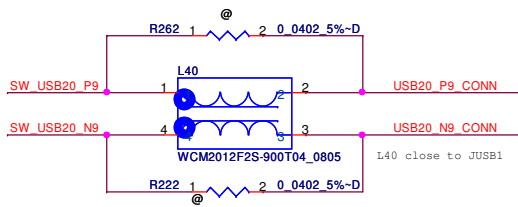
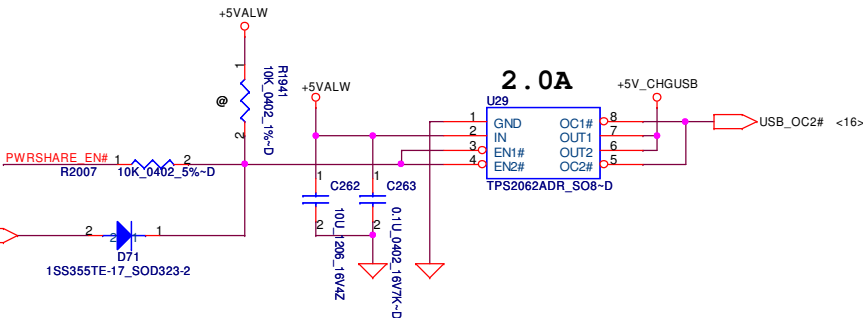
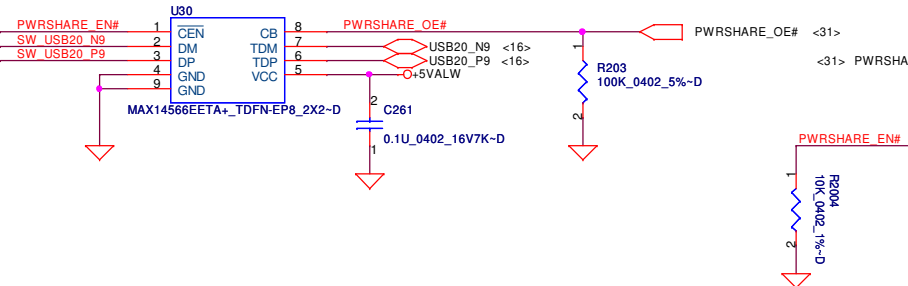
CRT



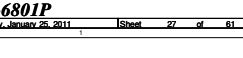


Power share

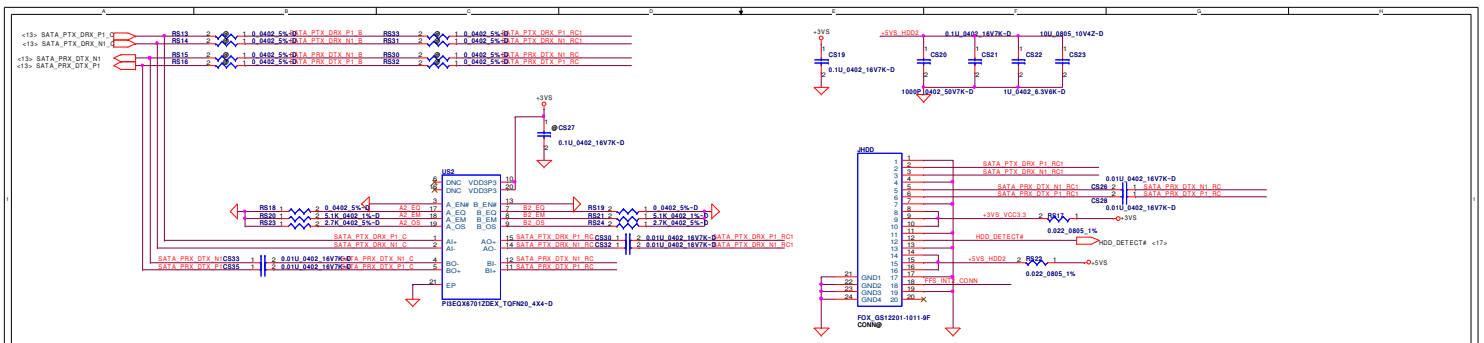
CB	Function
L	auto detection charger identification active
H	DP/DM=TDP/TDM



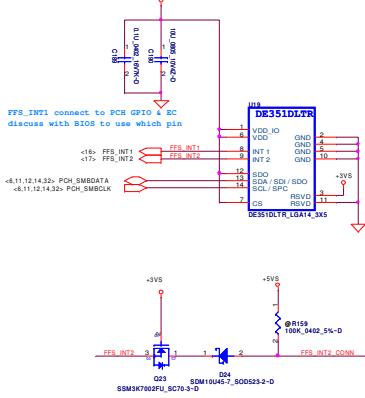
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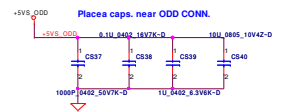
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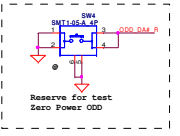
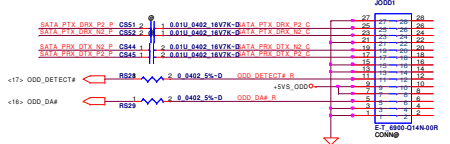
Free Fall Sensor



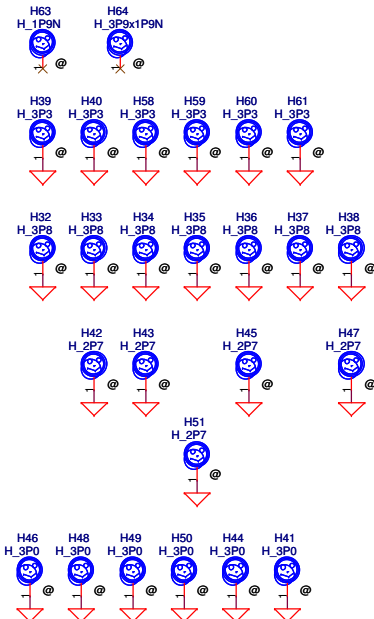
	MAXIM <small>max11</small>	TI <small>2nd</small>
P/N	SA00003LH1L	SA00003EX0L
RS43 RS44	pop	depop
RS47 RS48	depop	pop
RS53 RS54	pop	depop



SATA ODD Conn.



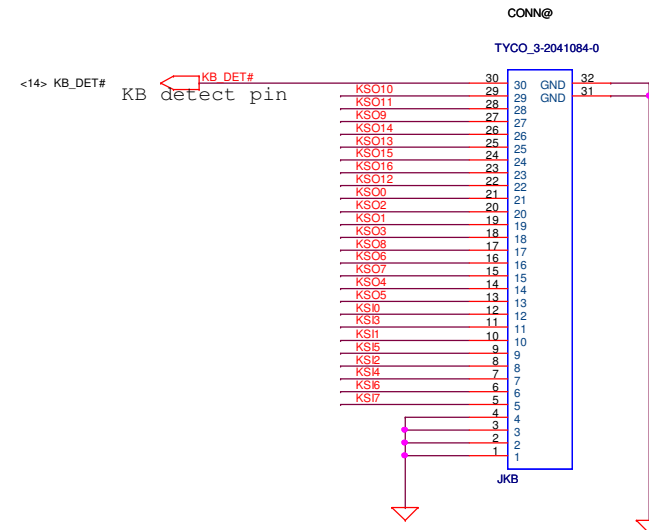
Power Button



PCB-MB

PCBA-DMC/B

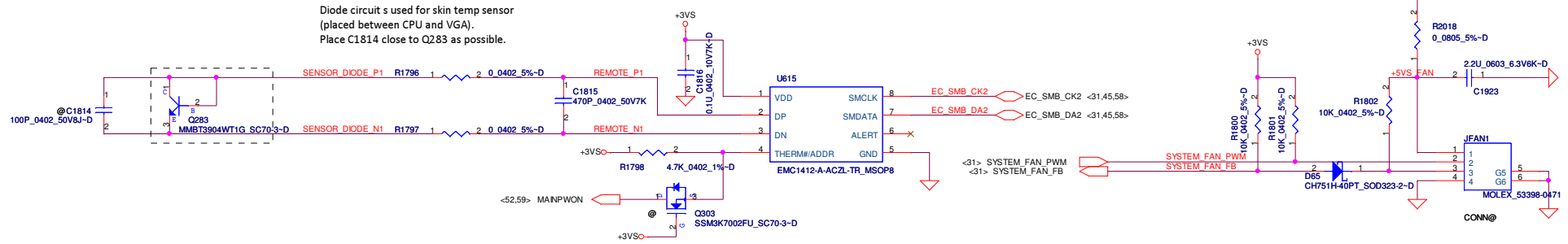
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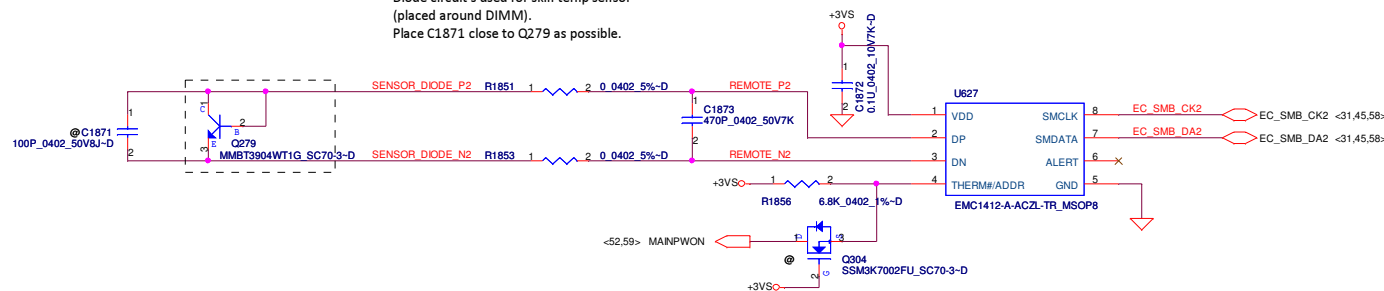
System Thermal Sensor 1

Diode circuit s used for skin temp sensor
(placed between CPU and VGA).
Place C1814 close to Q283 as possible.

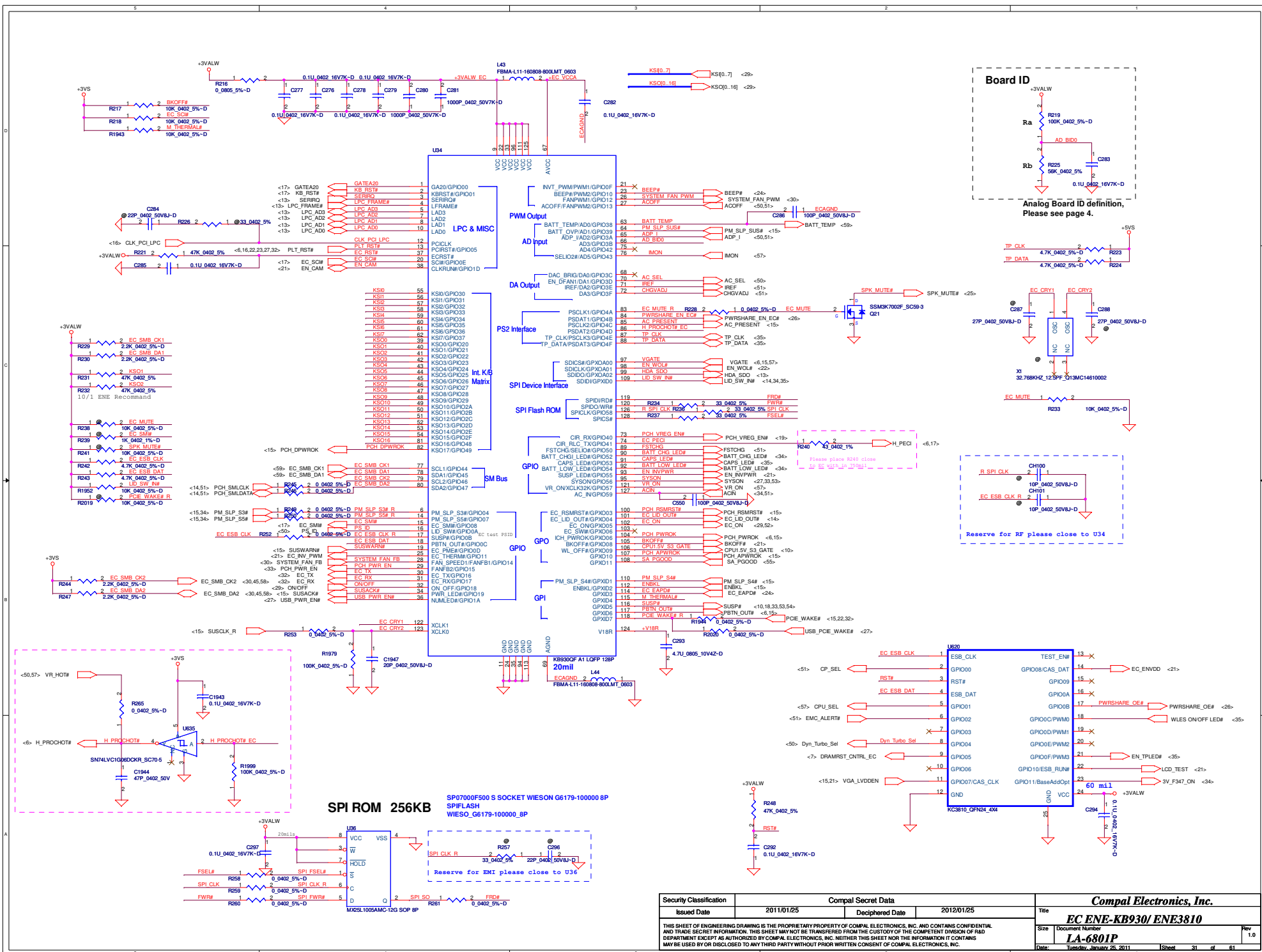


System Thermal Sensor 2

Diode circuit s used for skin temp sensor
(placed around DIMM).
Place C1871 close to Q279 as possible.

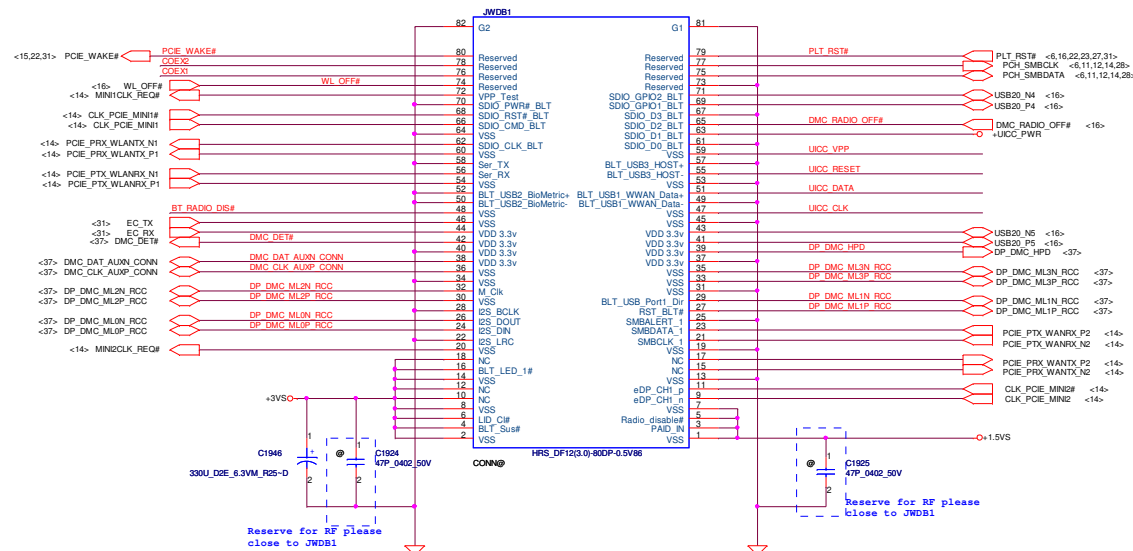


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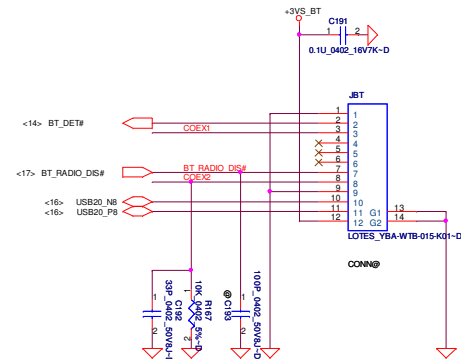
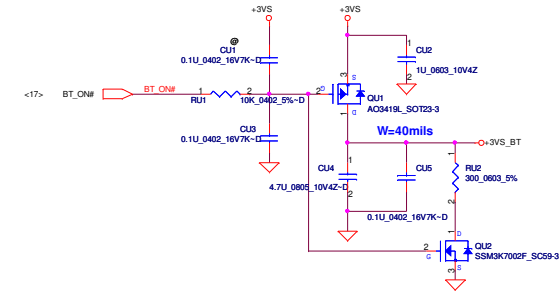


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To DMC PCB connector

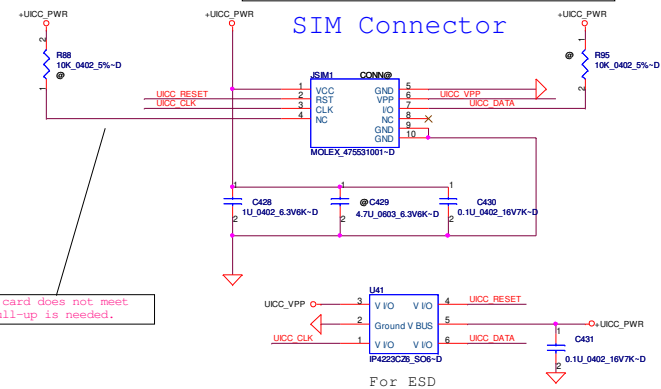


BlueTooth



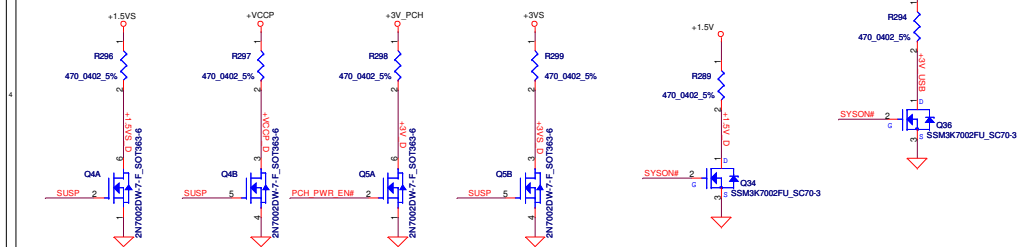
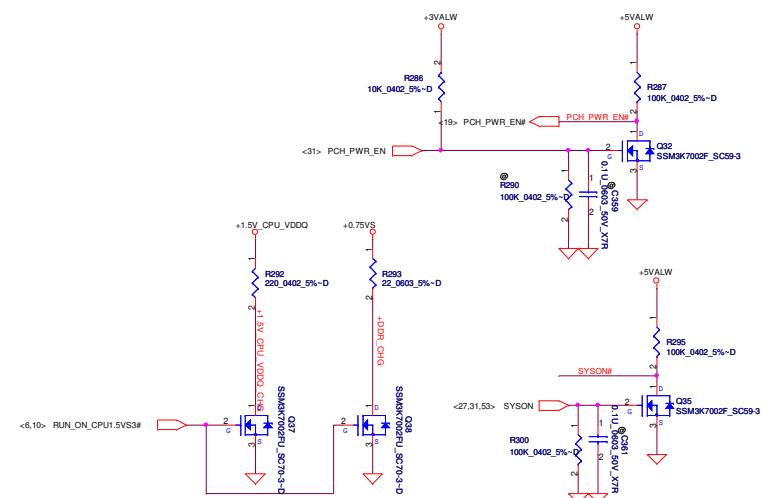
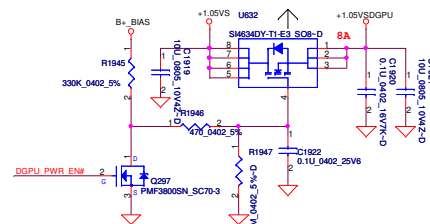
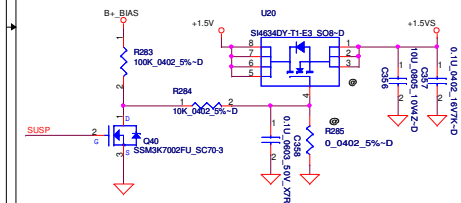
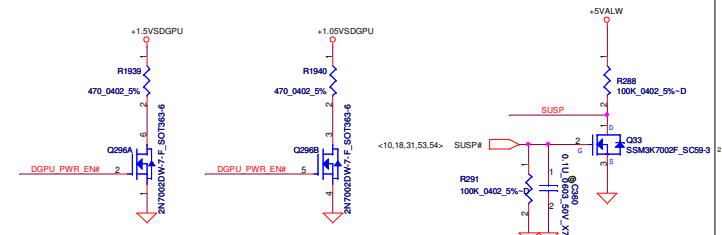
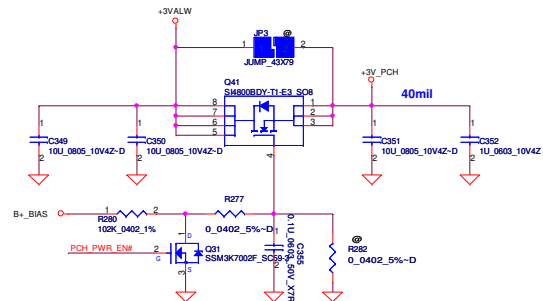
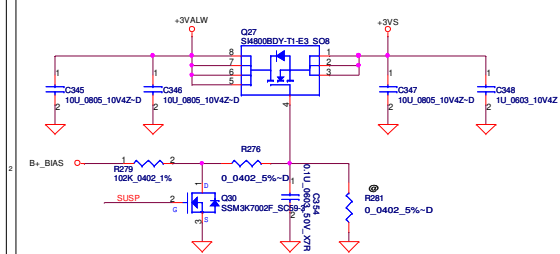
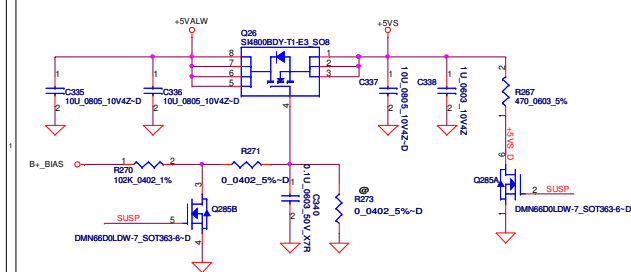
SIM card board 4.7uF change to 1uF for Tiger detect issue.

SIM Connector

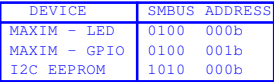


Reserve for SIM card does not meet rise time and pull-up is needed.

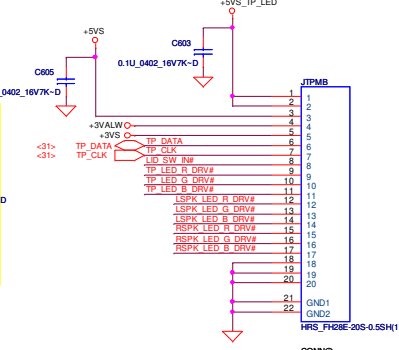
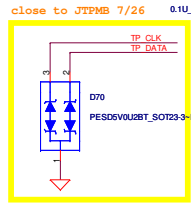
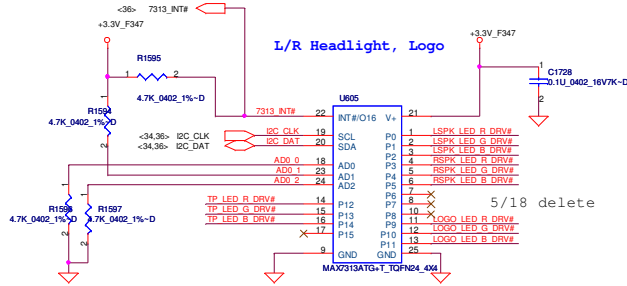
Security Classification		Compal Secret Data		Title	
Issued Date	2011/01/25	Deciphered Date	2012/01/25	Mini Card - WLAN / DMC / BT	
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				LA-6801P	New 1.0
				Date:	Tuesday, January 25, 2011
				Sheet	32 of 61



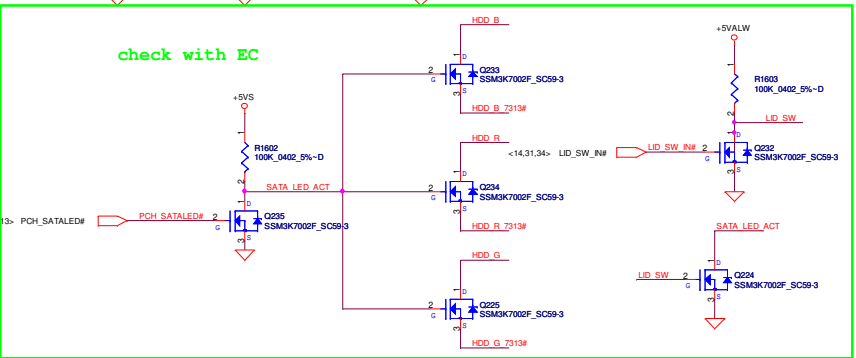
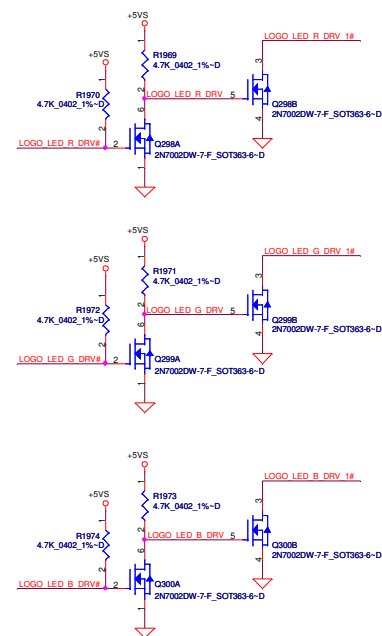
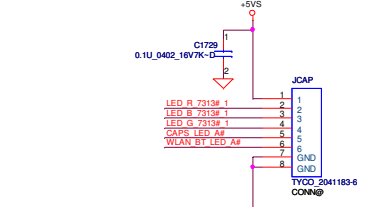
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/01/25	Deciphered Date	2012/01/25	Title	DC/DC Interface	
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				LA-6801P		1.0
Date: Tuesday, January 25, 2011				Sheet	33	of 61



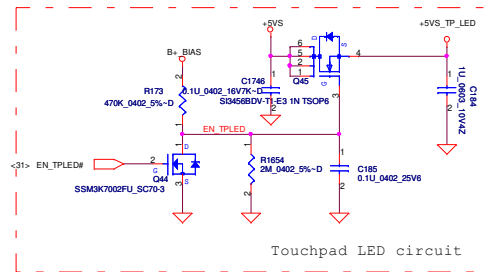
Touchpad LED CONN



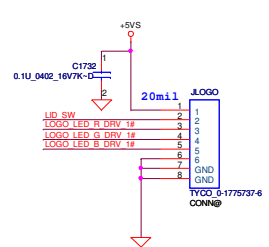
Indicator CONN



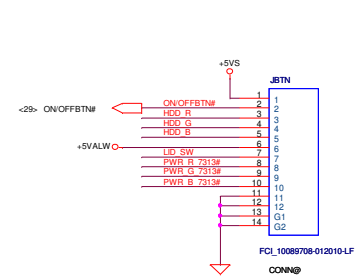
Reference	AD2	AD1	AD0	MAX7313
U605	0	1	0	L/R Headlight, Logo, TP
U608	0	1	1	Num, CAP, SCR EJECT, REV, PLAY/PAUSE FFWD, Vol_DWN, Vol_UP Wireless ON/OFF AWCC Button Alien Adrenaline Power Button Eyes Power Button Rim



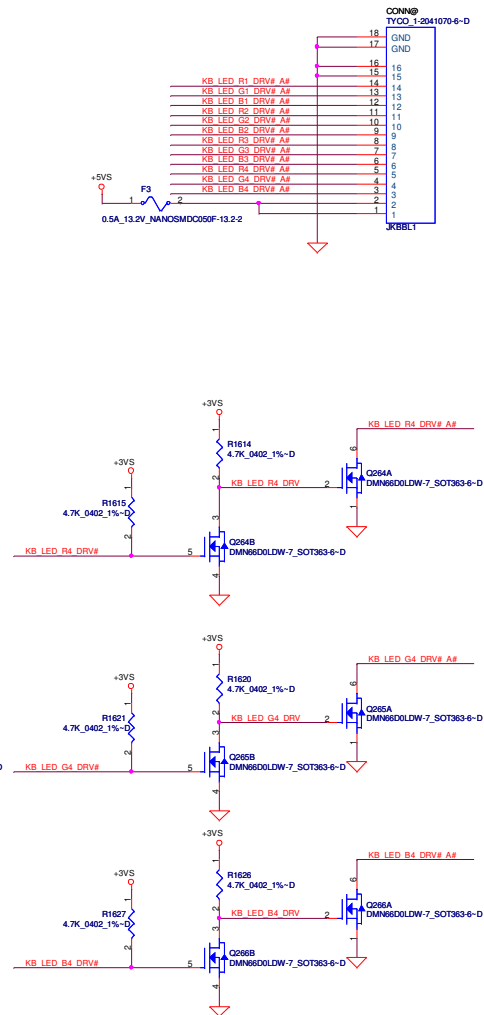
LOGO Board CONN



PWR BTN Board CONN

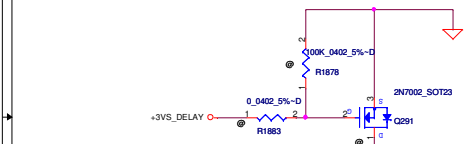
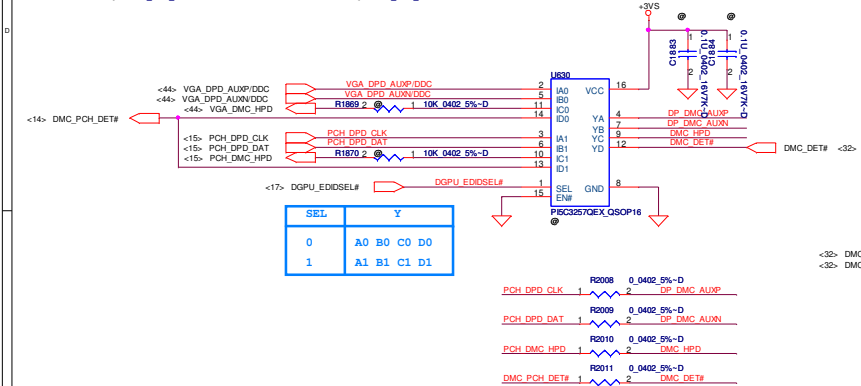


Security Classification	Compal Secret Data		Title	
Issued Date	2011/01/25	Deciphered Date	2012/01/25	ELC (2)
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Date:	Tuesday, January 25, 2011	Sheet	36	of 61

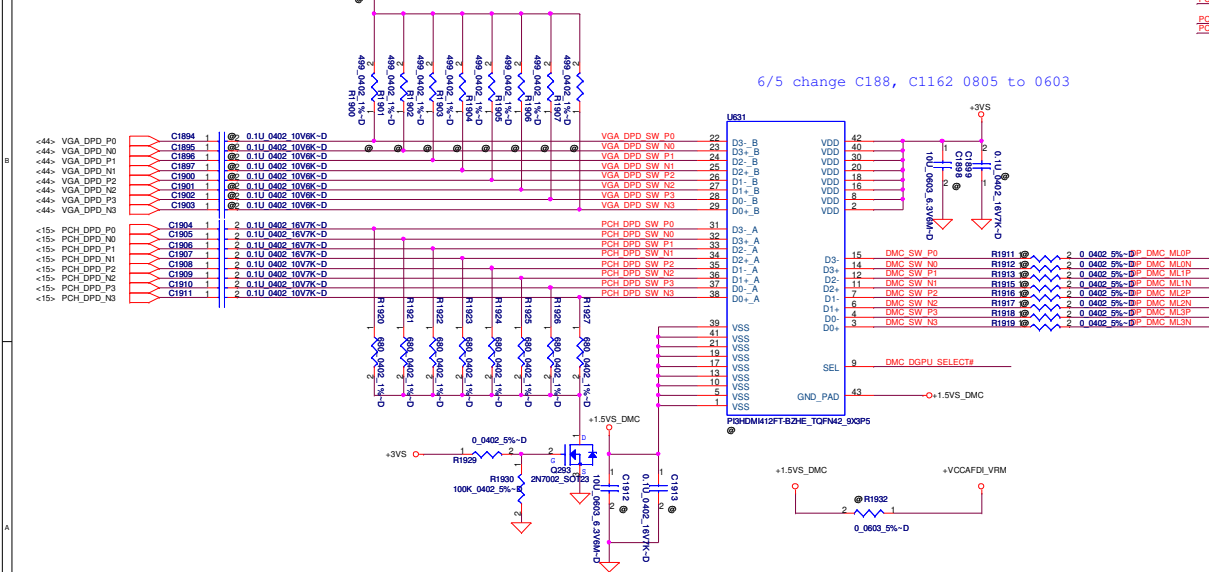


Security Classification		Compal Secret Data		Title	
Issued Date	2011/01/25	Deciphered Date	2012/01/25	ELC (3)	
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</p>				Size	Document Number
				<p>LA-6801P</p>	
Date:				January 26, 2011	Sheet 36 of 61

PCH/GPU DDC SW for DMC

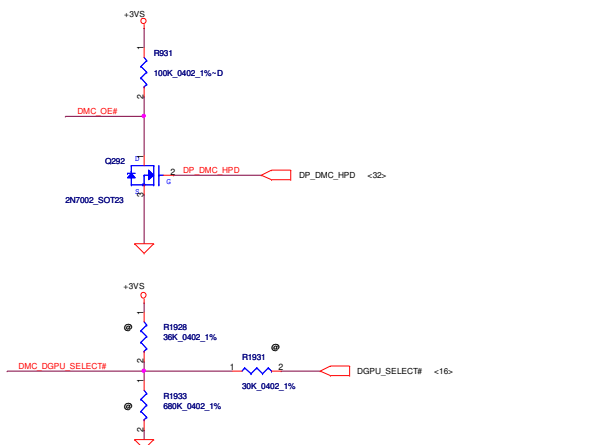
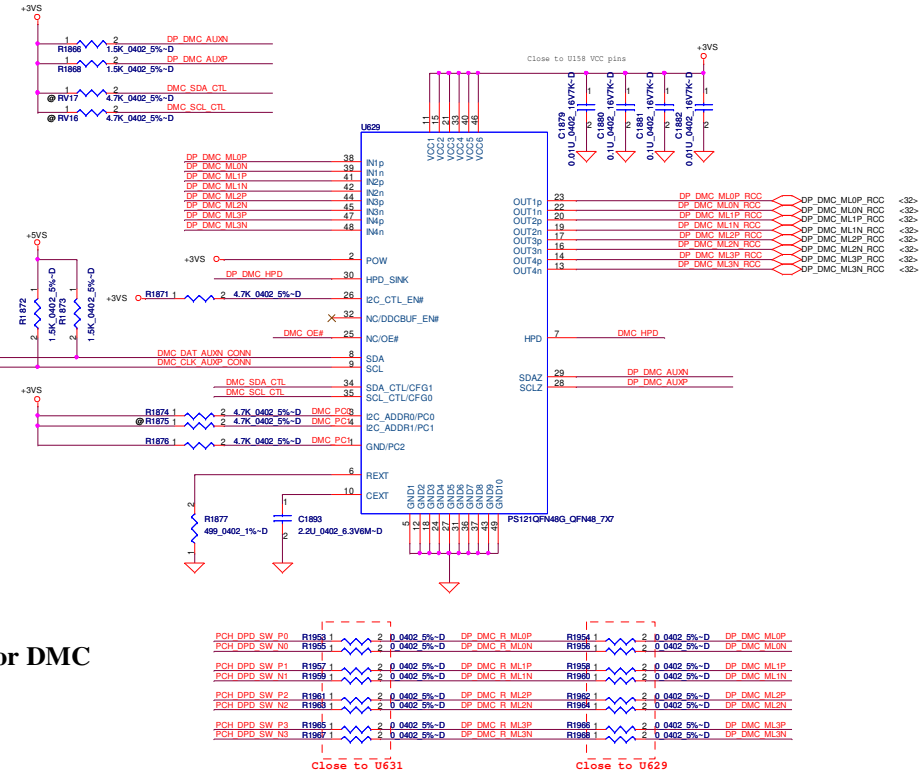


PCH/GPU AUX&LANE SW for DMC



AUX_SEL/SEL1&2	Chanel	Source
0	A	GPU
1	B	PCH

DMC Redriver



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/25	Deciphered Date	2012/01/25	Title	DMC MUX/Redriver
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				C	1.0
				Document Number LA-6801P	
Date:		Tuesday, January 25, 2011		Sheet	37 of 61

DP Redriver

6/5 change C61 0805 to 0603

GPU DDC Dongle SW for DP

Dongle **Normal**

DP HPD for OPT DGPU output

07/29/2010

DP HPD for OPT DGPU output

Security Classification: Compal Secret Data

Issued Date: 2011/01/25

Deciphered Date: 2012/01/25

Compal Electronics, Inc.

Mini Display Port

Size: 16801P

Customer: LA-6801P

Date: Tuesday, January 25, 2011

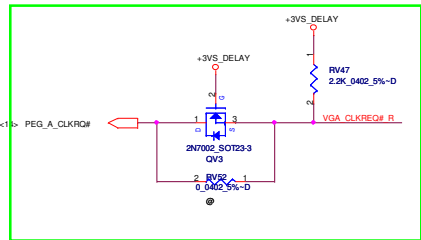
Sheet: 38 of 61

[illegible]

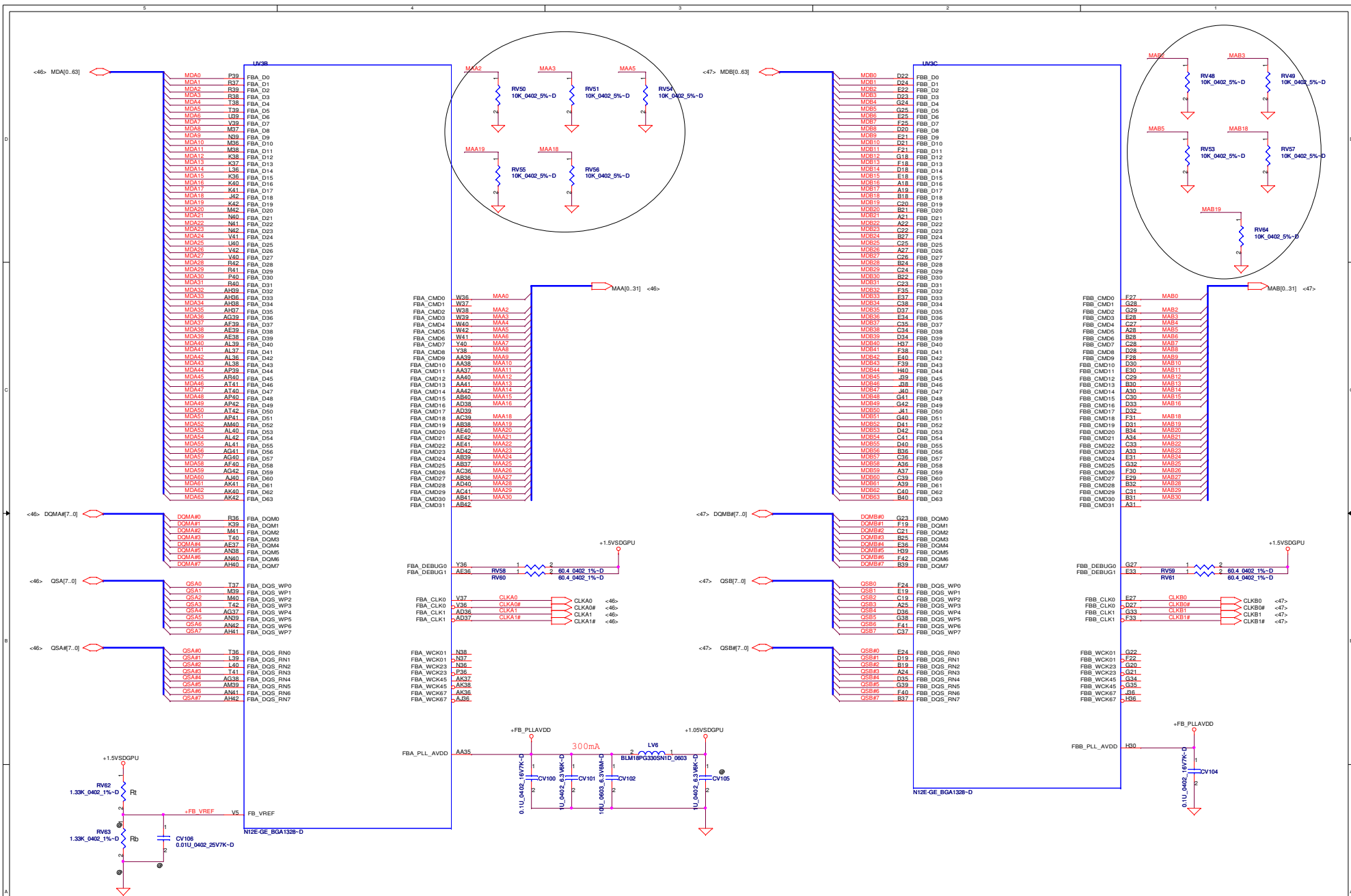
07/29/2010
DP HPD for OPT DGPU output

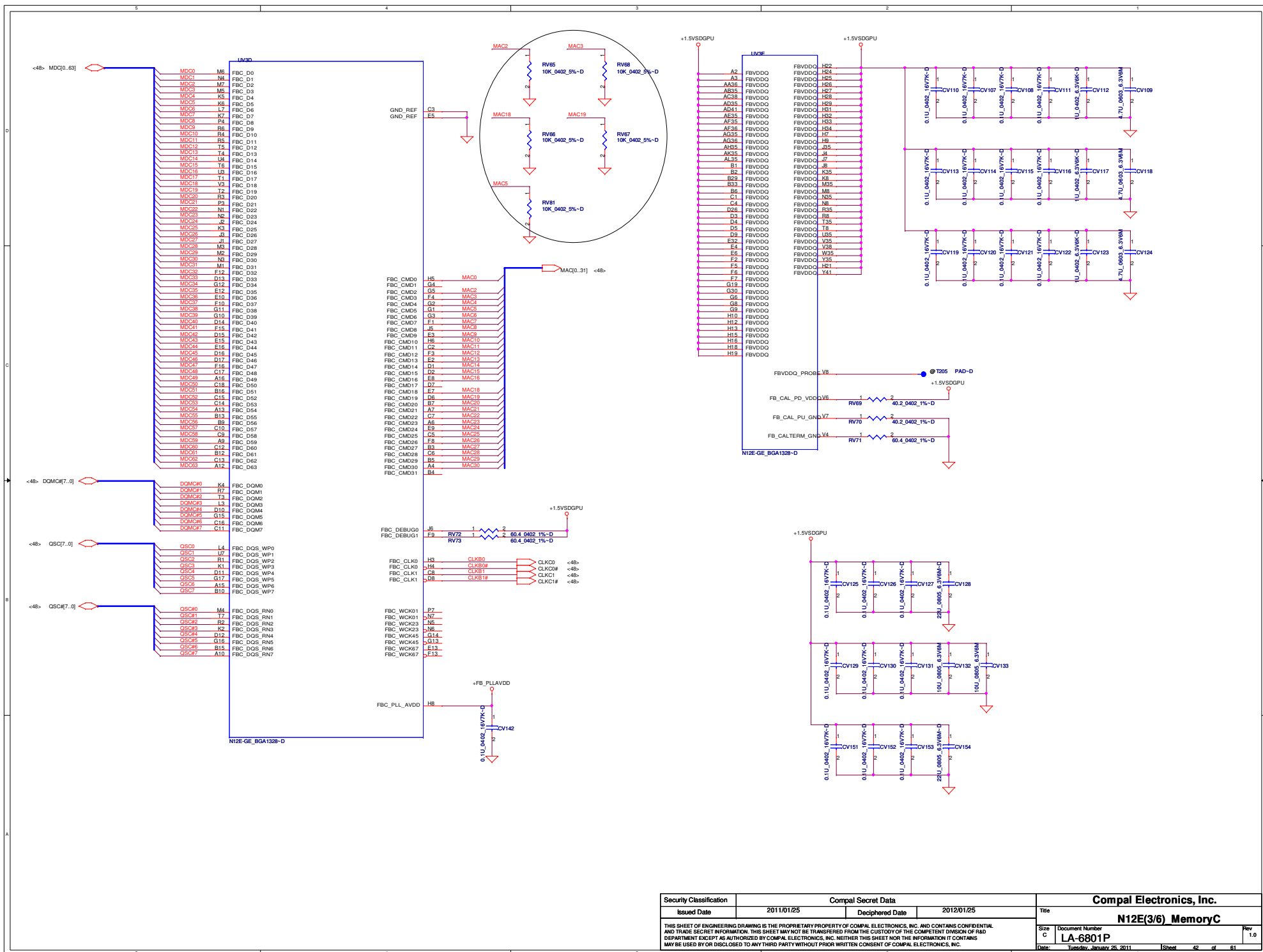
The diagram shows a circuit for generating a DP HPD signal. It starts with a 3V3 supply connected to a 0.1uF capacitor (CV506). The output of the capacitor is connected to the input of a UV17 component. The UV17 component is also connected to a 0.0402 5%-D resistor (RV239). The output of RV239 is connected to the input of a SN74AHC1G08DCKR_SC70-5 logic chip. The logic chip is also connected to a 10K 0402 5%-D resistor (RV280) and a 0.0402 5%-D resistor (RV240). The output of the logic chip is connected to the DP_HPDP signal. The circuit is labeled with component values and pin numbers.

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/01/25	Deciphered Date	2012/01/25	Title	Mini Display Port	
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				Custom	LA-6801P	1.0
				Date:	Tuesday, January 25, 2011	Sheet 38 of 61

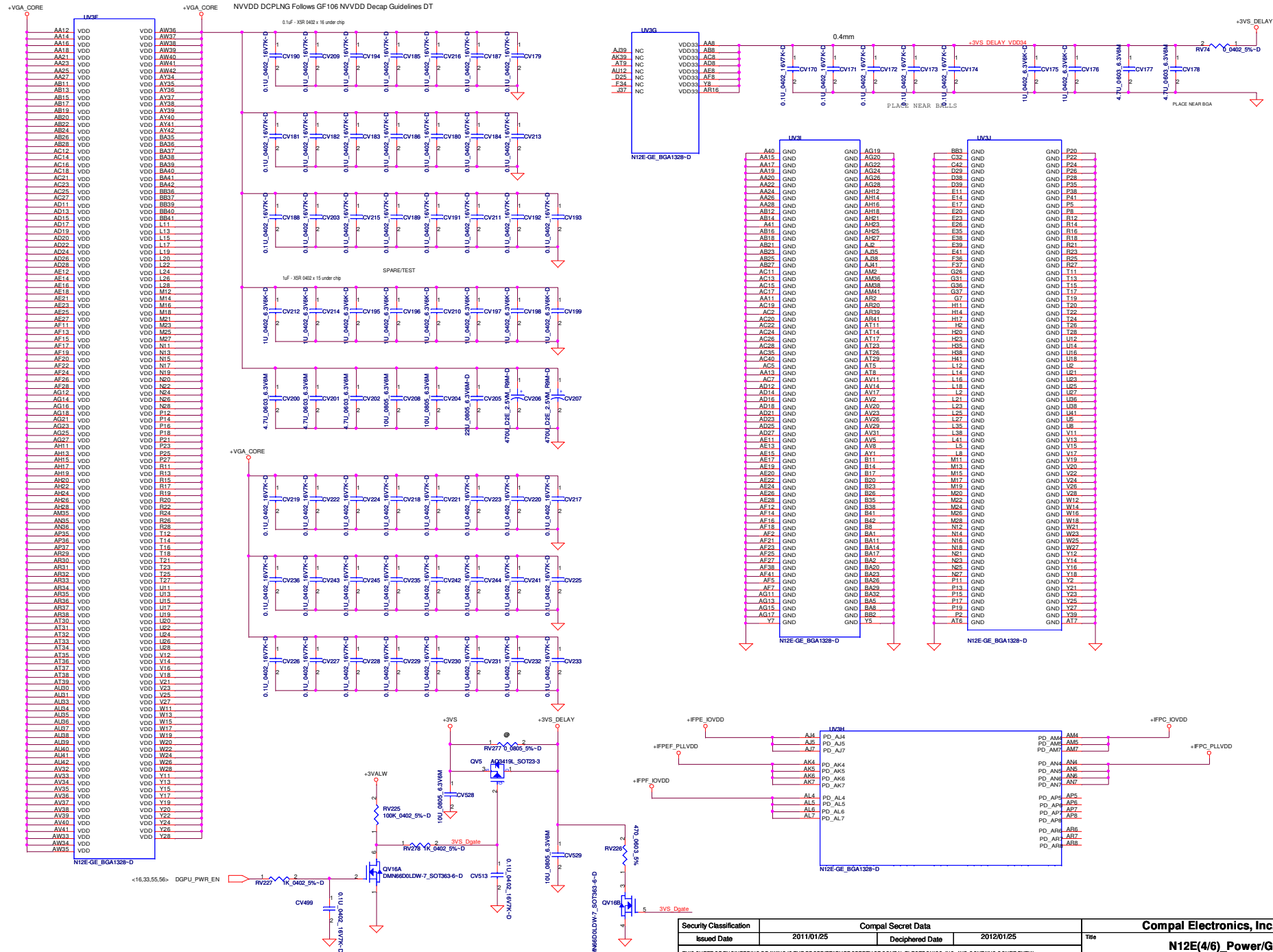


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Issued Date	2011/01/25	Deciphered Date	2012/01/25	Title	
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				LA-6801P	
				Date: <u>January 26, 2011</u> Sheet <u>40</u> of <u>61</u>	

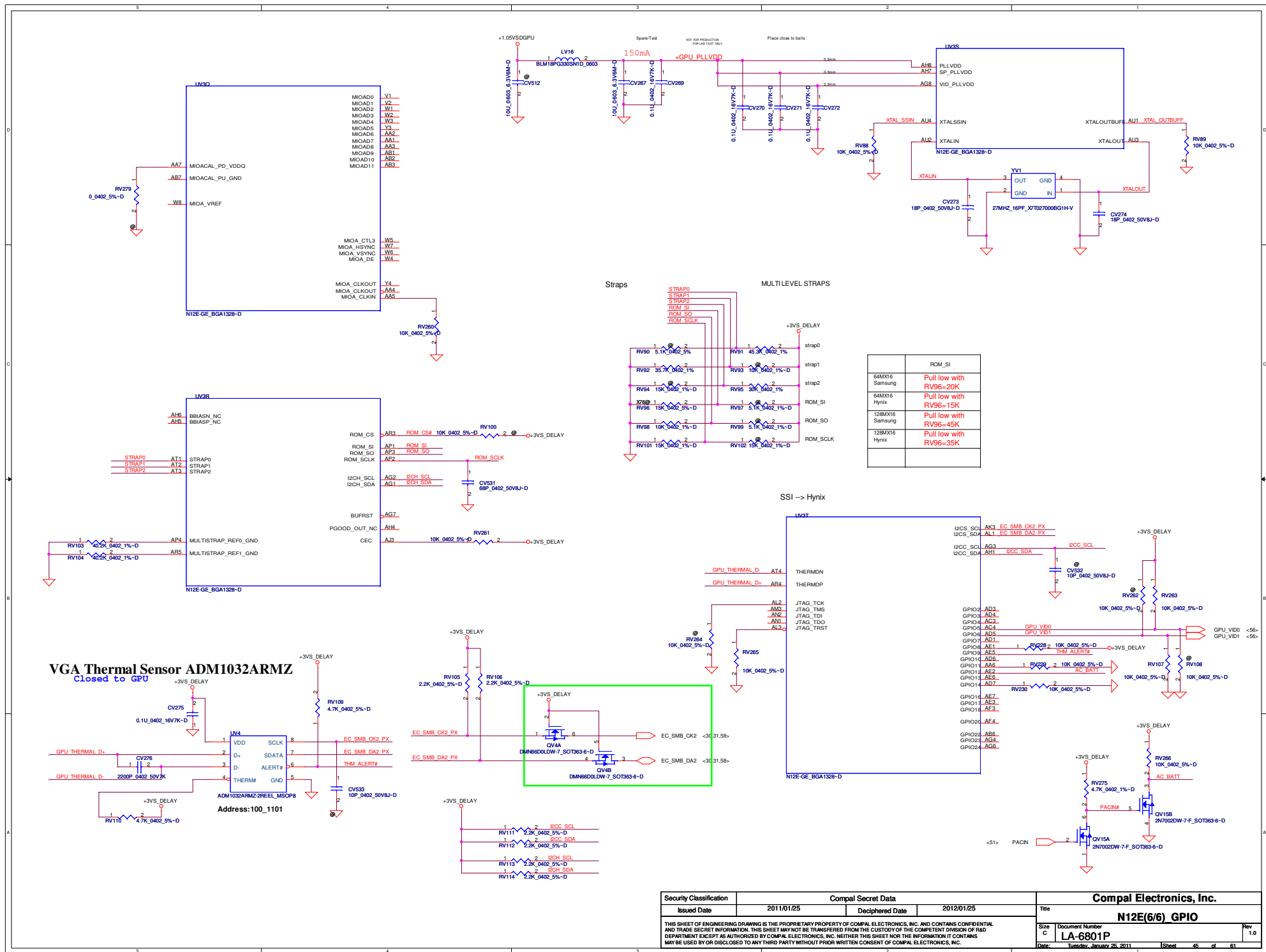


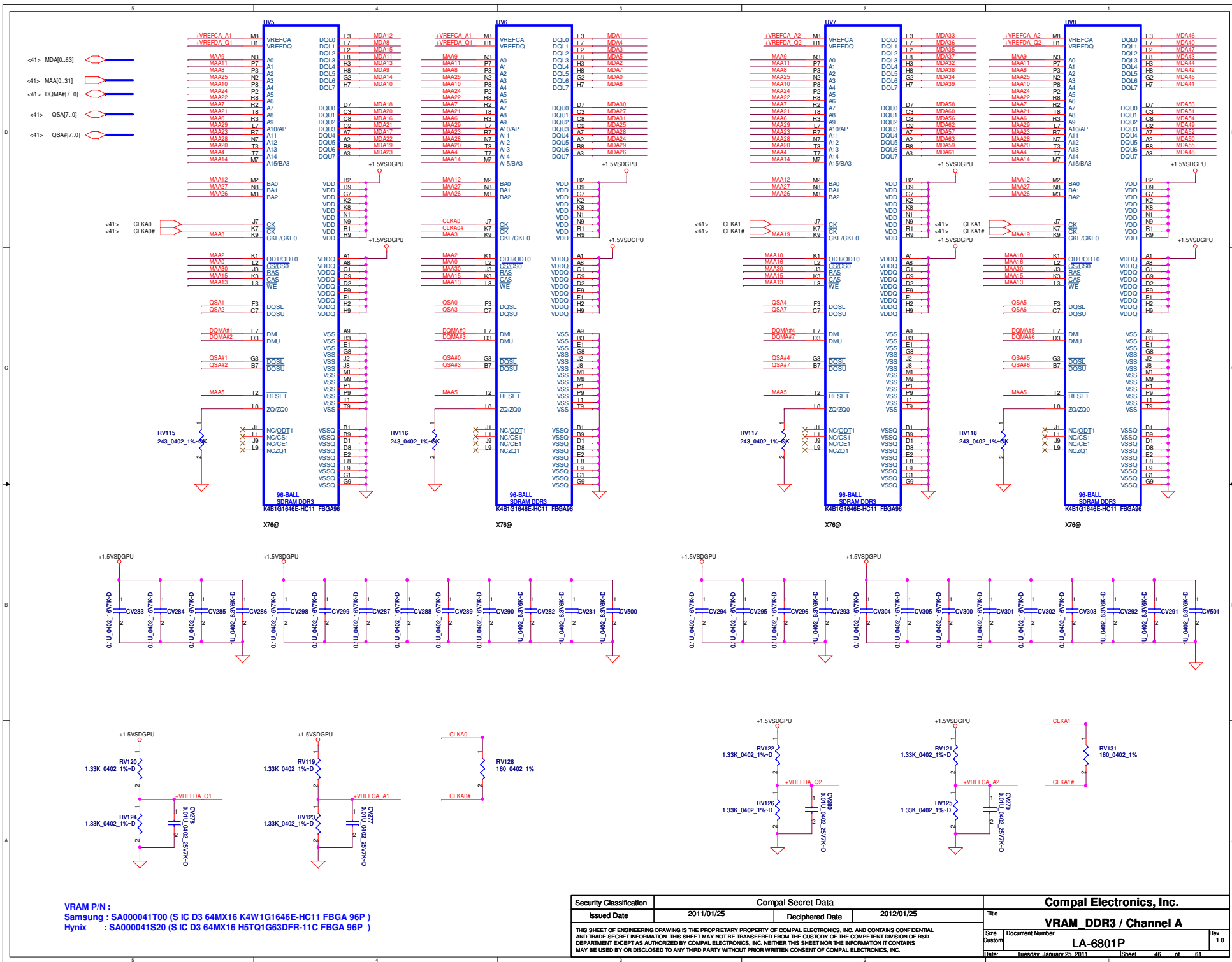


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/25	Deciphered Date	2012/01/25	Title	N12E(3/6) MemoryC
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					LA-6801P
				Date:	Tuesday, January 25, 2011
				Sheet	42 of 61

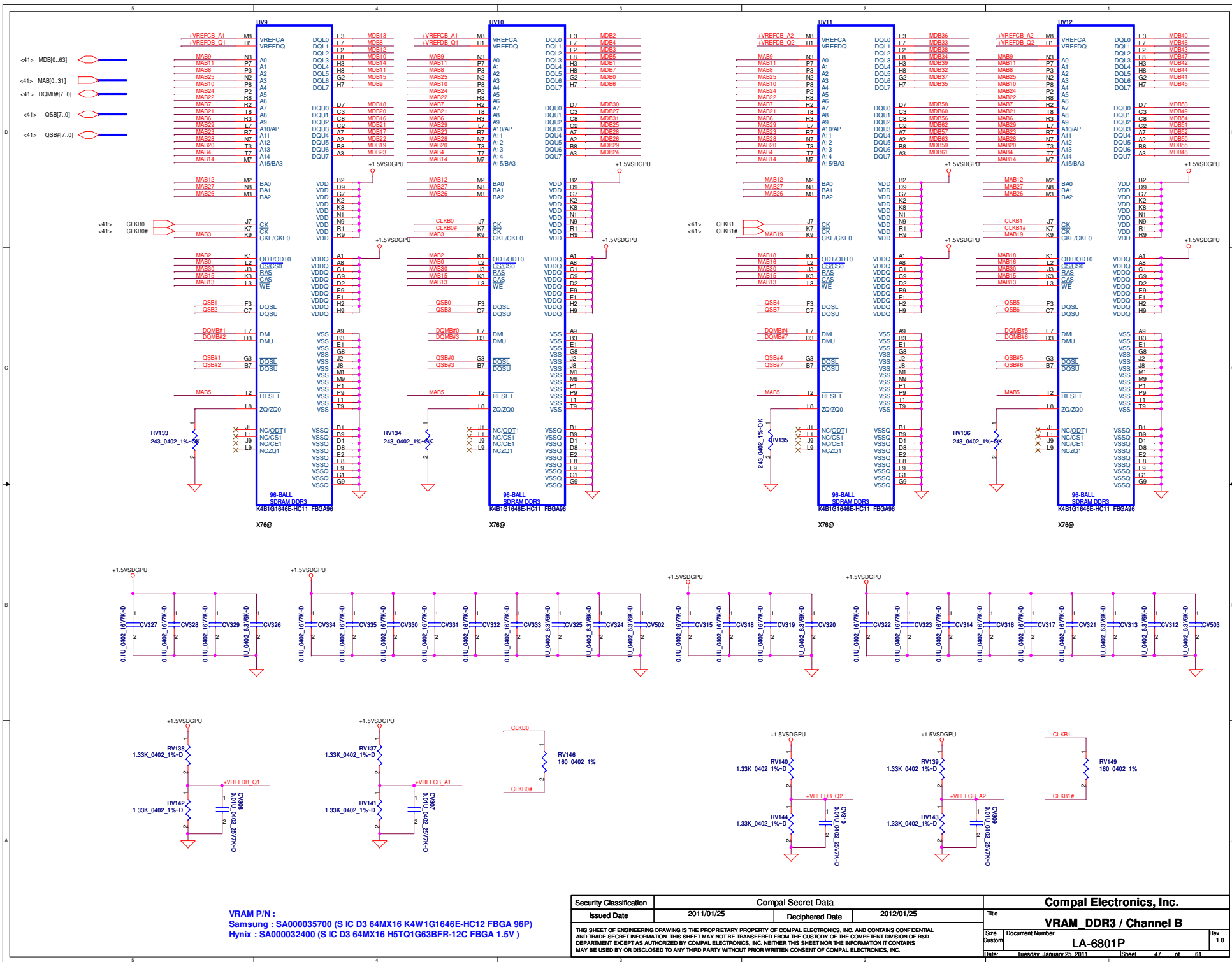


Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		N12E(4/6) Power/GND	
2011/01/25		2012/01/25		Size	
				C	
				LA-6801P	
				Date: Tuesday, January 25, 2011	
				Sheet 43 of 61	



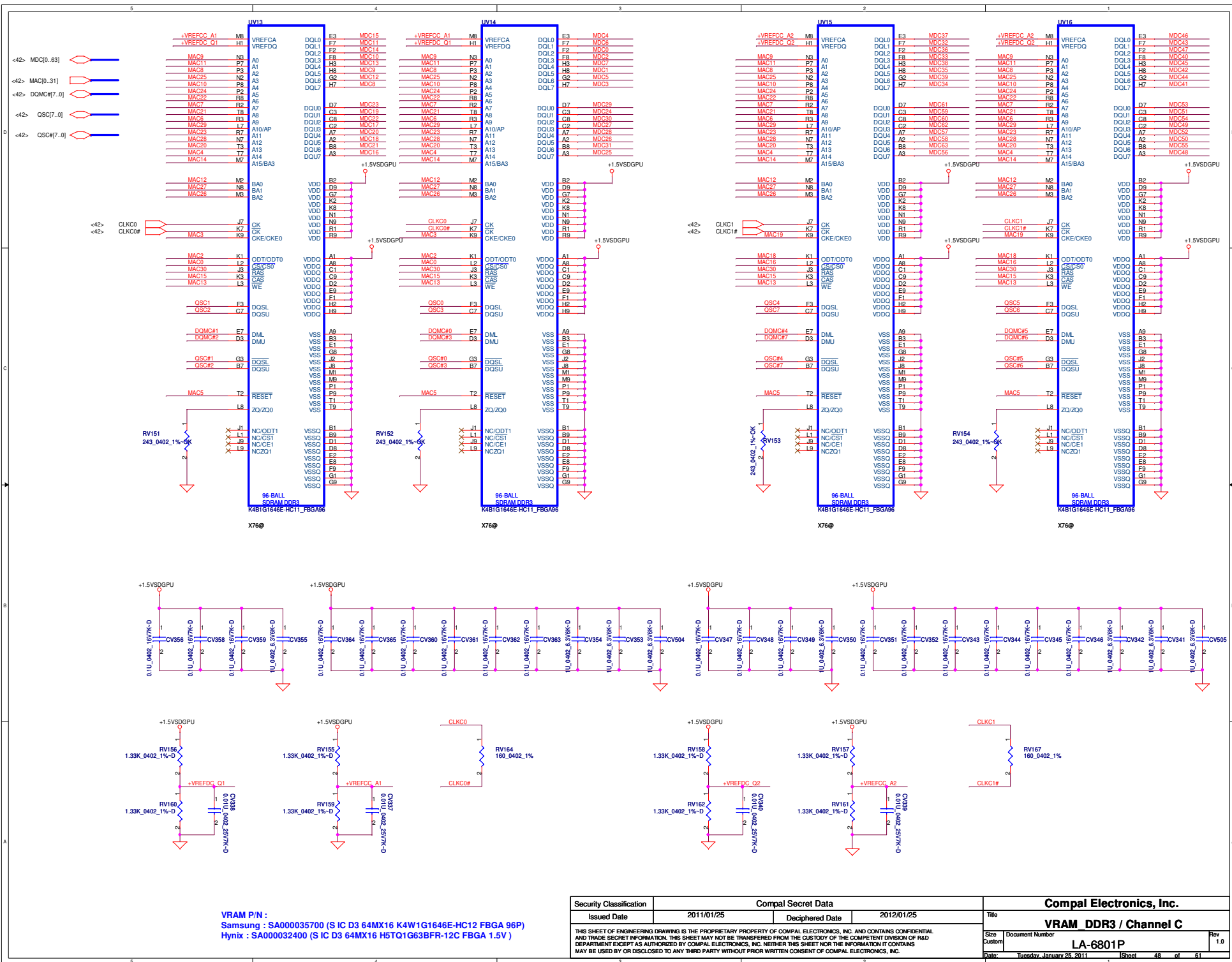


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/25	Deciphered Date	2012/01/25	Title	VRAM_DDR3 / Channel A
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				Date	Tuesday, January 25, 2011
				Sheet	46 of 61

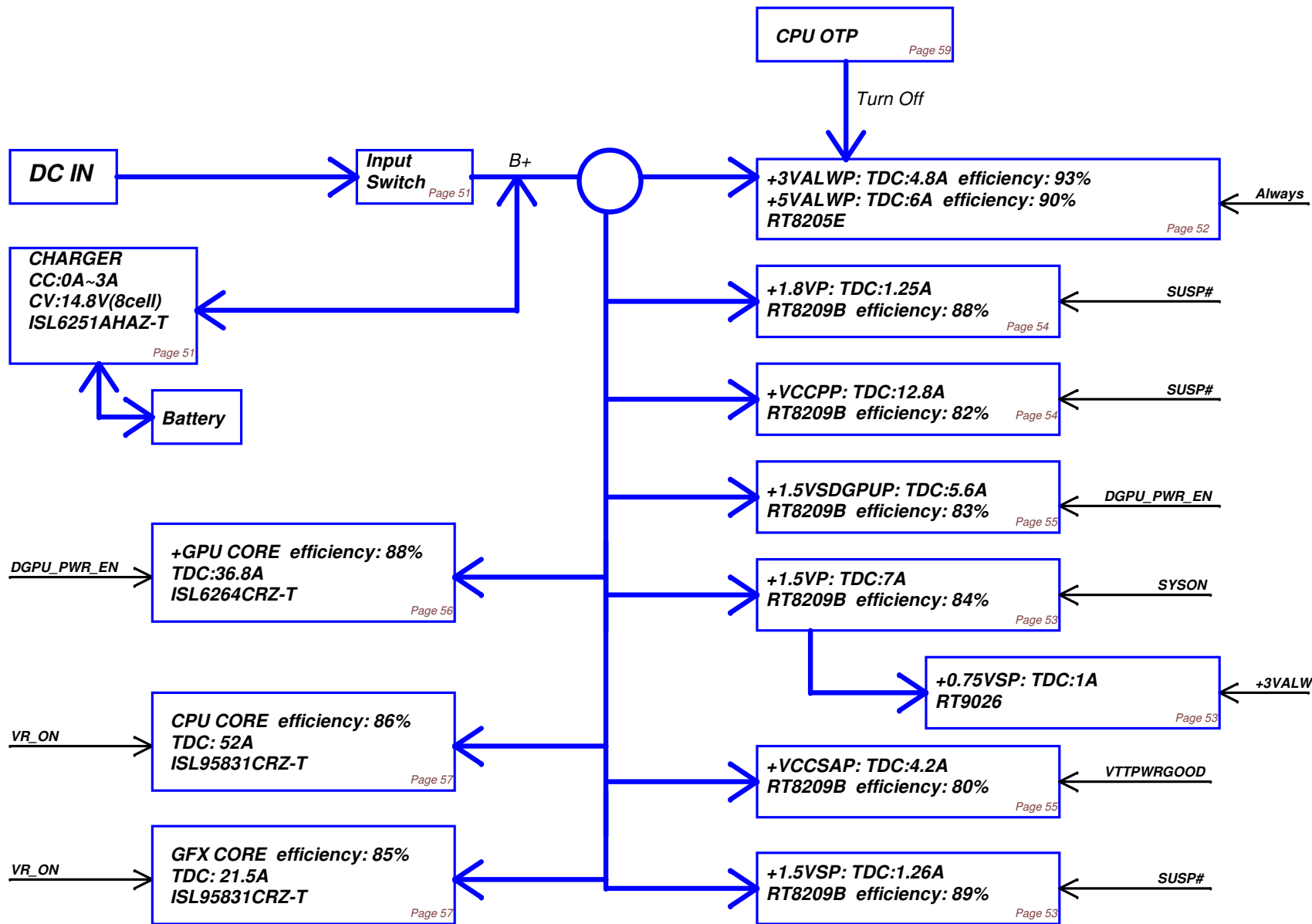


VRAM P/N :
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

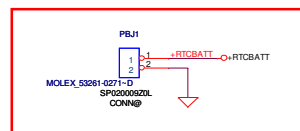
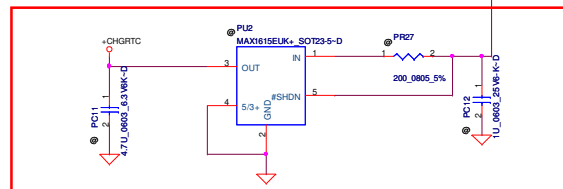
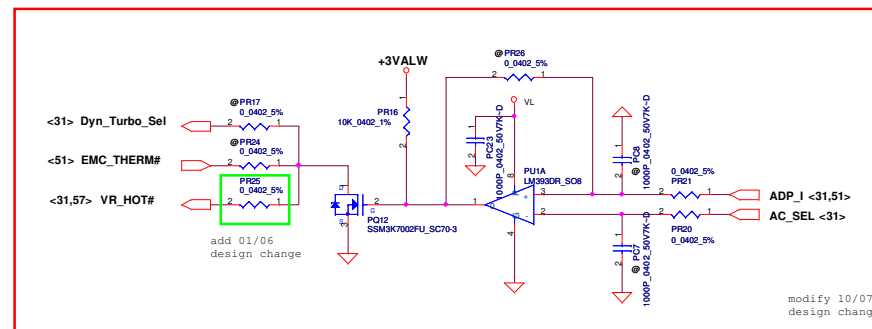
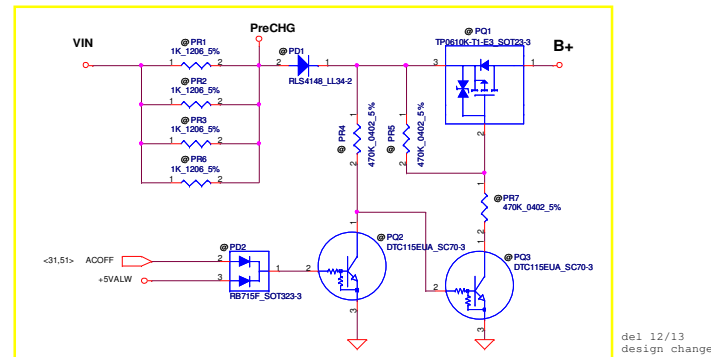
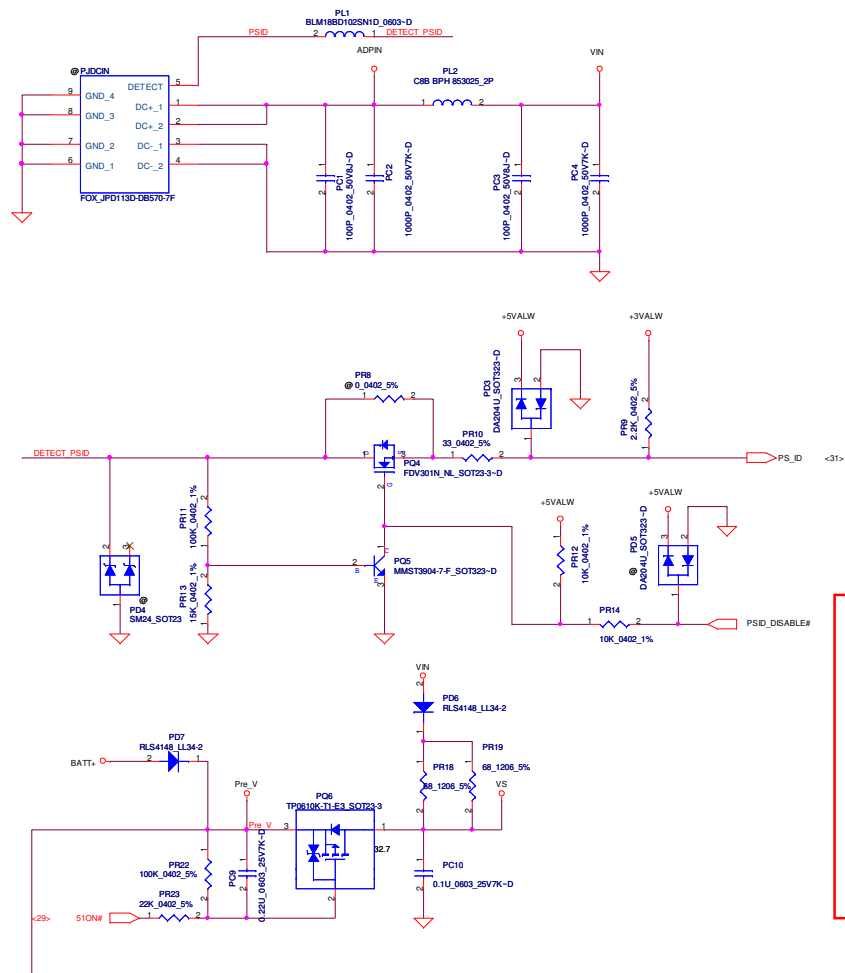
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/25	Deciphered Date	2012/01/25	Title	VRAM_DDR3 / Channel B
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				Date	Tuesday, January 25, 2011
				Sheet	47 of 61



Power block



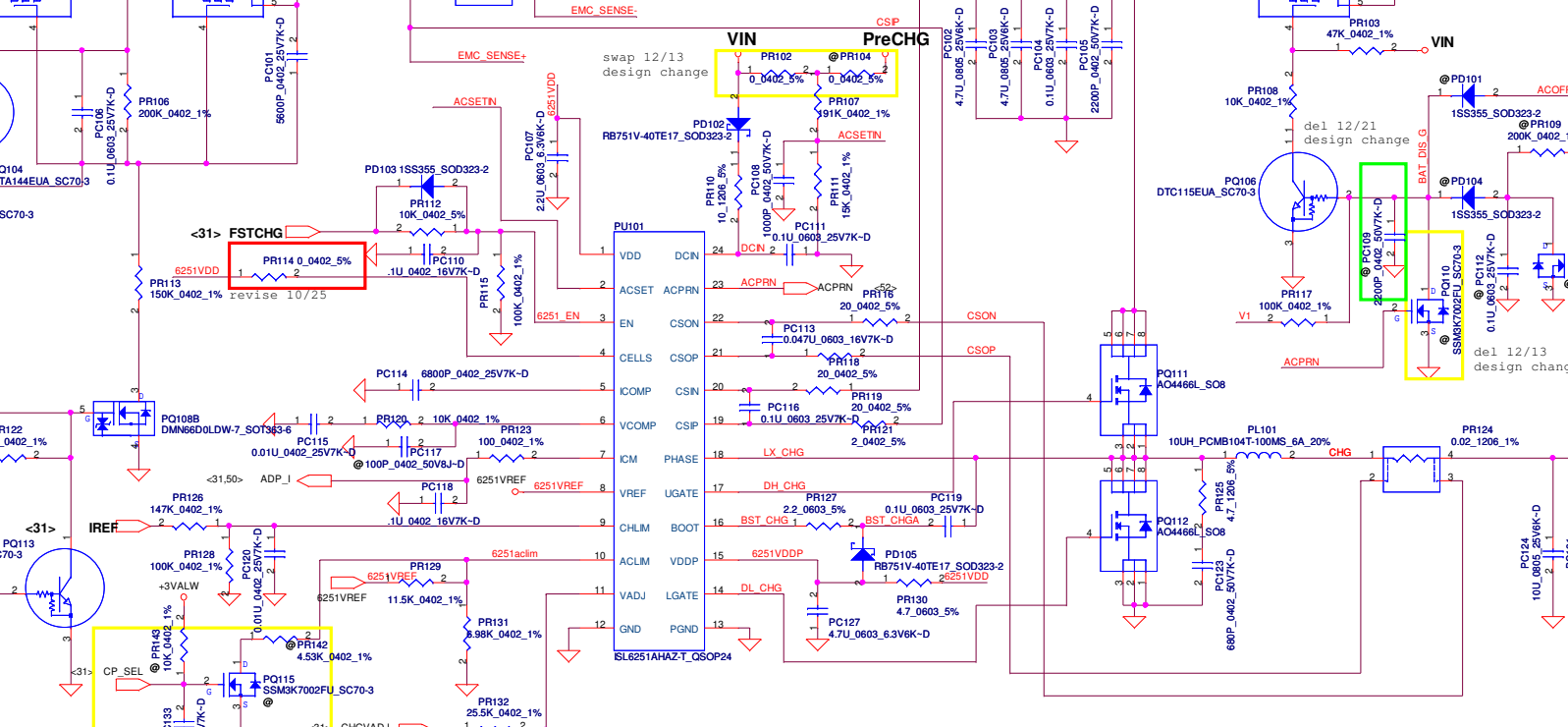
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/25	Deciphered Date	2012/01/25	Title	POWER BLOCK DIAGRAM
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				Document Number	LA-6801P
				Date	Tuesday, January 25, 2011
				Sheet	49 of 61
				Rev	1.0



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/25	Deciphered Date	2012/01/25	Title	PWR-DCIN / Vin Detector
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				C	LA-6301P
				Date:	Tuesday, January 25, 2011
				Sheet	50 of 61

$$CP = 90\% \cdot I_{ada} ; CP = 6.92A$$

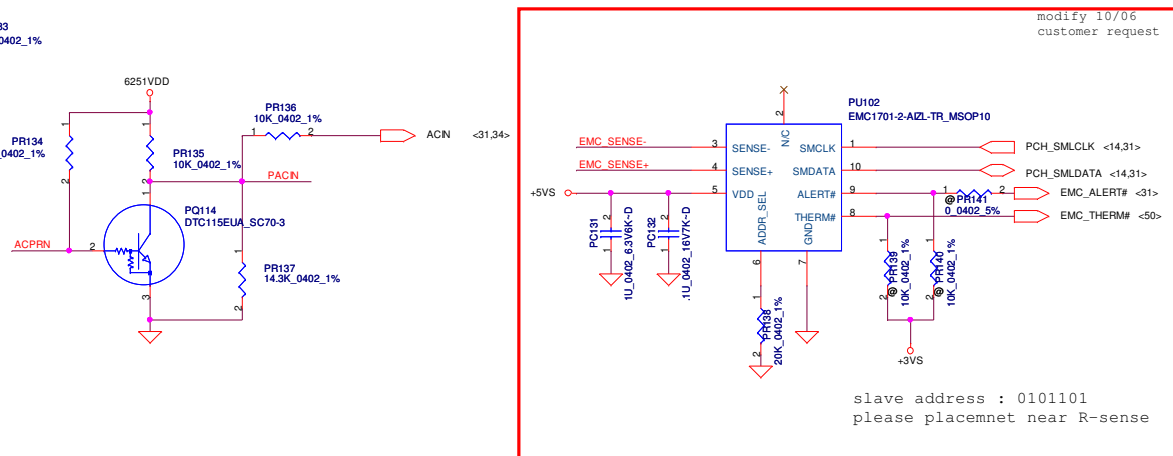
```
add 01/20
for EMI request
```


$$\begin{aligned} I_{\text{input}} &= (1/0.02) (0.05 \cdot V_{\text{aclm}}/2.39 + 0.05) \\ V_{\text{aclm}} &= 2.39 \cdot ((6.98\text{K}/152\text{K}) / ((11.5\text{K}/152\text{K}) + (6.98\text{K}/152\text{K}))) \end{aligned}$$

IREF=0.25V~3.3V

CHGVADJ	CV mode
0V	3.99V per cell
1.93V	4.2V per cell
3.3V	4.35V per cell

BATT Type	Charging Voltage (0x15)	CV mode
Normal 4S LI-ON Cells	14800mV	14.80V



Security Classification		Compal Secret Data		Compal Electronics, Inc.					
Issued Date		2011/01/25	Deciphered Date		2012/01/25	Title			
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						Size	Document Number		Rev 1.0
						Custom	LA-6801P		
Date:		Tuesday, January 25, 2011	Sheet	51	of	61			

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO

add 01/20
for EMI request

12UH_1281AS-H-1R2N-P3_9A_30%

PL201 HCB2012KF-121T50_0805

PL204

PJP205

JUMP_43X118

reserve 01/21

RT8205E_B+

Typ: 175mA

+3VALWP

3.3VALWP

TDC 4.8 A

Peak Current 8.93 A

OCF current 10.67 A

+3VALW

PJP201

JUMP_43X118

PJP202

JUMP_43X118

330U_D.6.5VW_R18M-D

PC214

PL202

4.7UH_FDVE1040-H-4R7M-P3_10A_20%-D

PR208

PC215

680P_0402_50V7K-D

PC216

PC217

PC218

PC219

PC220

PC221

PC222

PC223

PC224

PC225

PC226

PC227

PC228

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PC469

PC470

PC471

PC472

PC473

PC474

<27,31,33> SYSON

+5VALW

<16> 1.5VDDR_VID0

<16> 1.5VDDR_VID1

<10,18,31,33,54> SUSP#

DDR GPIO Output Voltage Selection		
bit2 = 1.5DDR_VID0	bit1 = 1.5DDR_VID1	DDR Vout
0	0	1.65V
0	1	1.6V
1	0	1.55V
1	1	1.5V (Default)

+3VALW

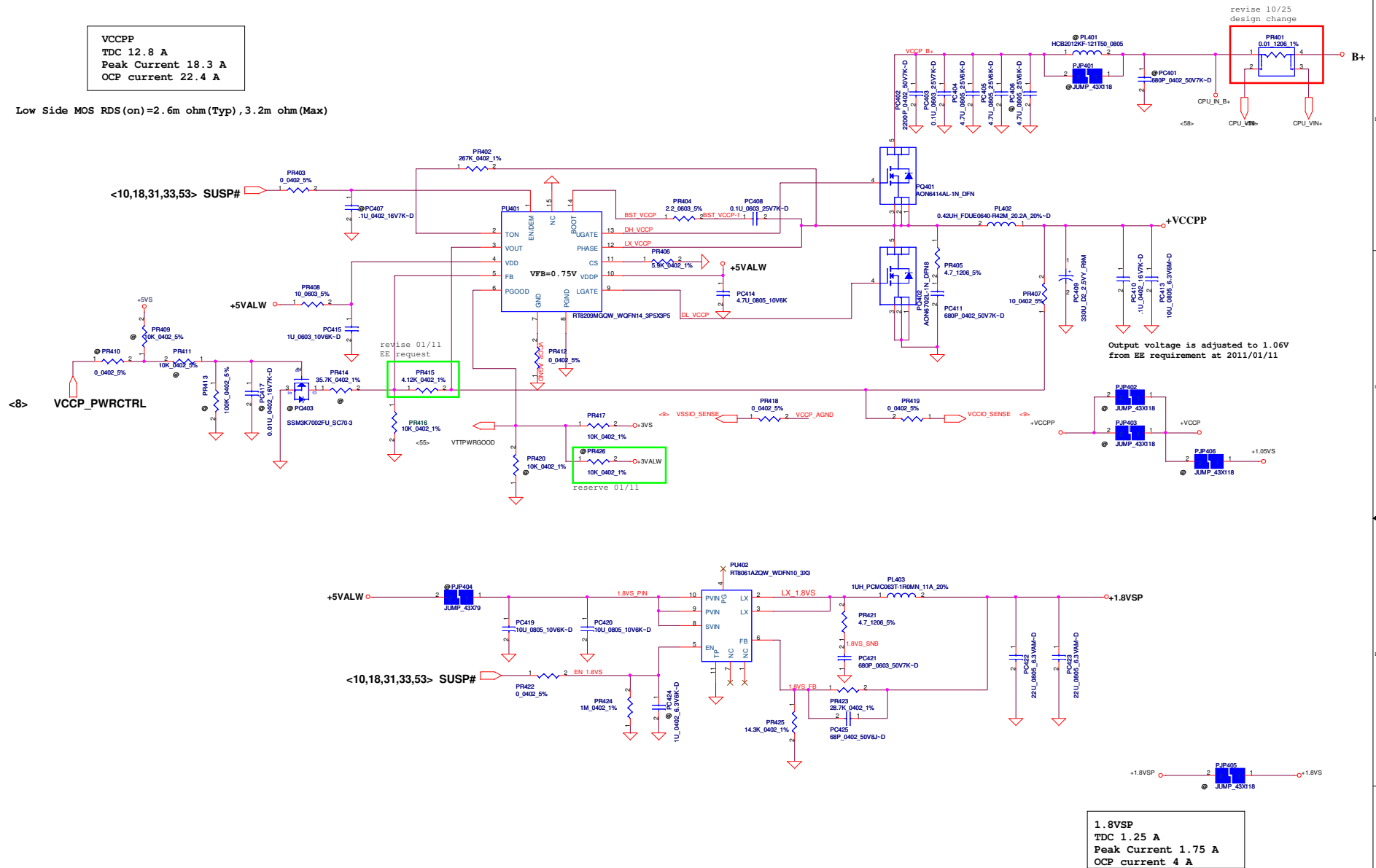
+1.5VSP
Imax=1.26A
Ipeak=1.8A
Iocp (minimum)=4A

Low Side MOS RDS(on)=5.5m ohm(Typ), 6.7m ohm(Max)

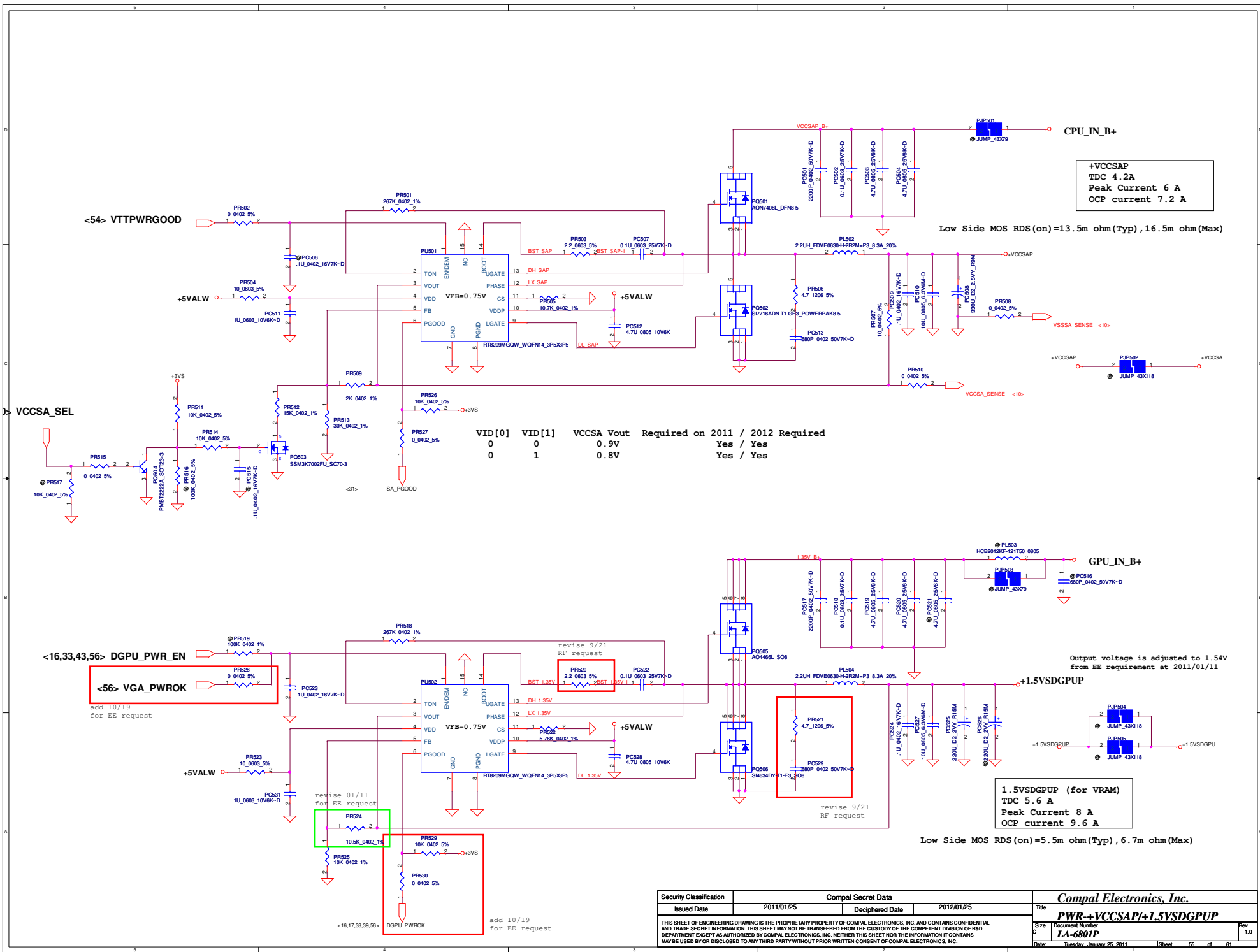
1.5VP
TDC 7 A
Peak Current 10 A
OCP current 12 A

VCCPP
TDC 12.8 A
Peak Current 18.3 A
OCP current 22.4 A

Low Side MOS RDS(on)=2.6m ohm(Typ), 3.2m ohm(Max)

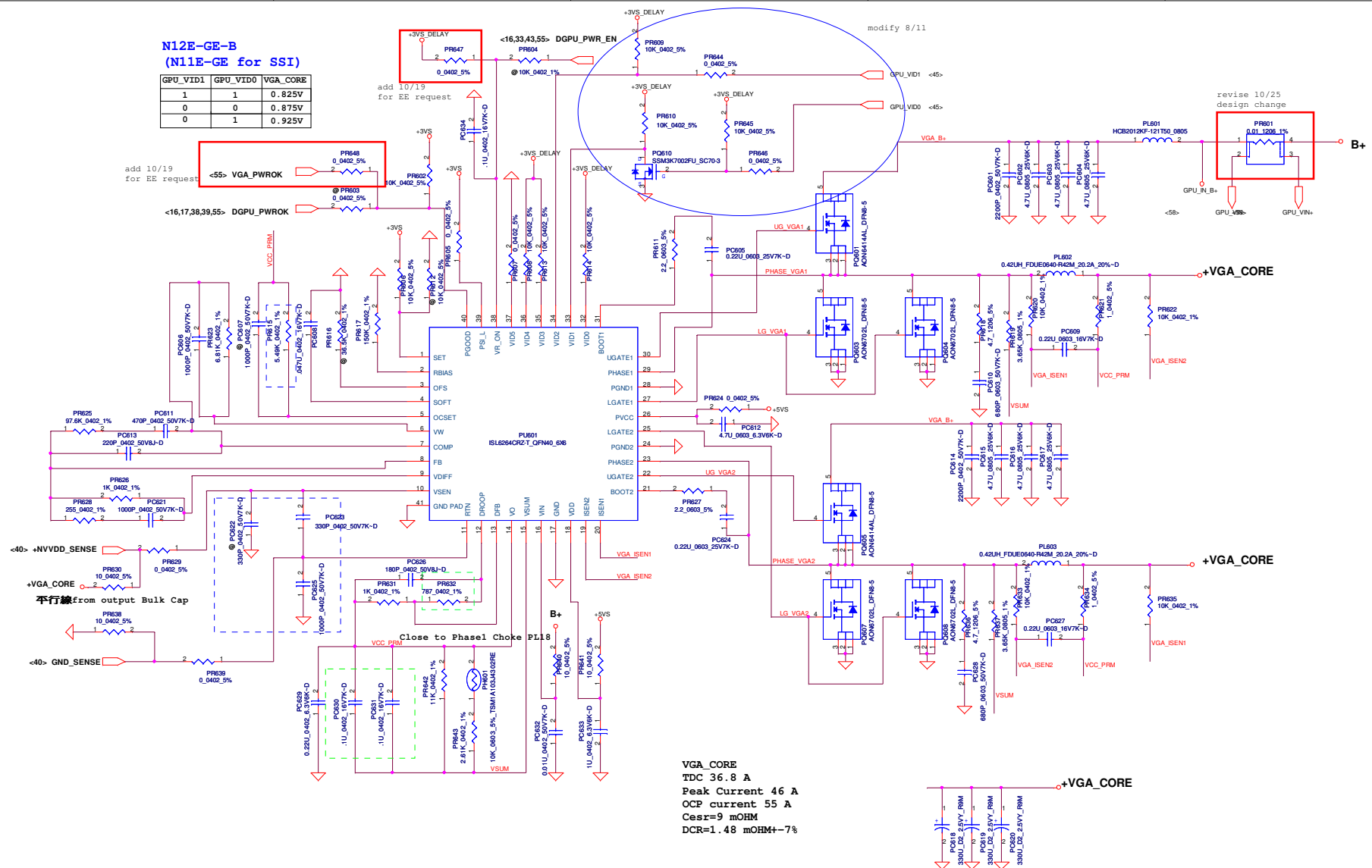


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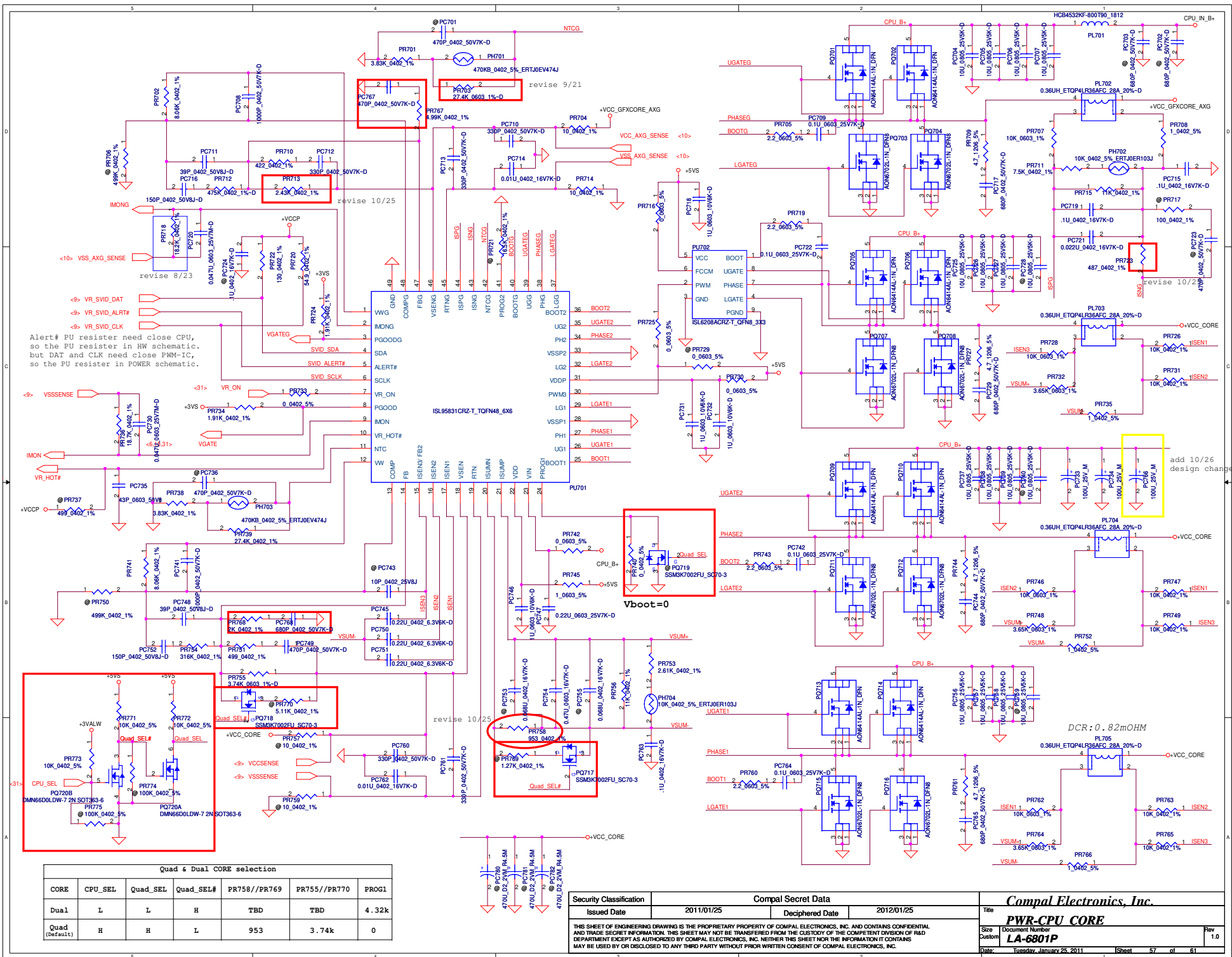
N12E-GE-B
(N11E-GE for SSI)

GPU_VID1	GPU_VID0	VGA_CORE
1	1	0.825V
0	0	0.875V
0	1	0.925V

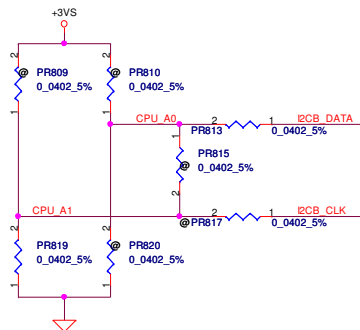
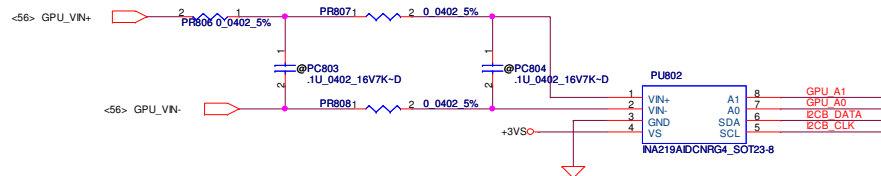
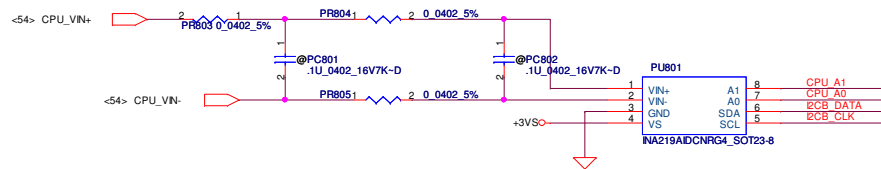
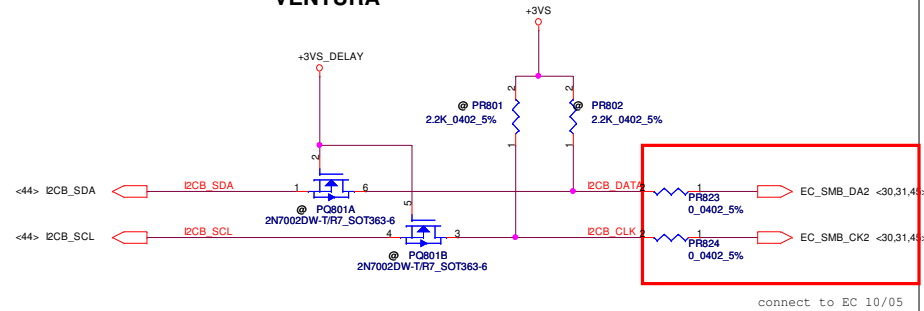


VGA_CORE
TDC 36.8 A
Peak Current 46 A
OCP current 55 A
Cesi=9 mOHM
DCR=1.48 mOHM+-7%

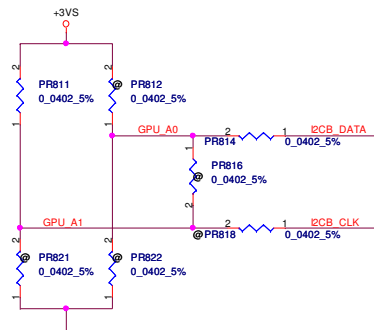
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Issued Date	2011/01/25	Deciphered Date	2012/01/25	VGA CORE	
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VENTURA



Ventura for CPU side
slave address : 1000010
please placemnet near R-sense



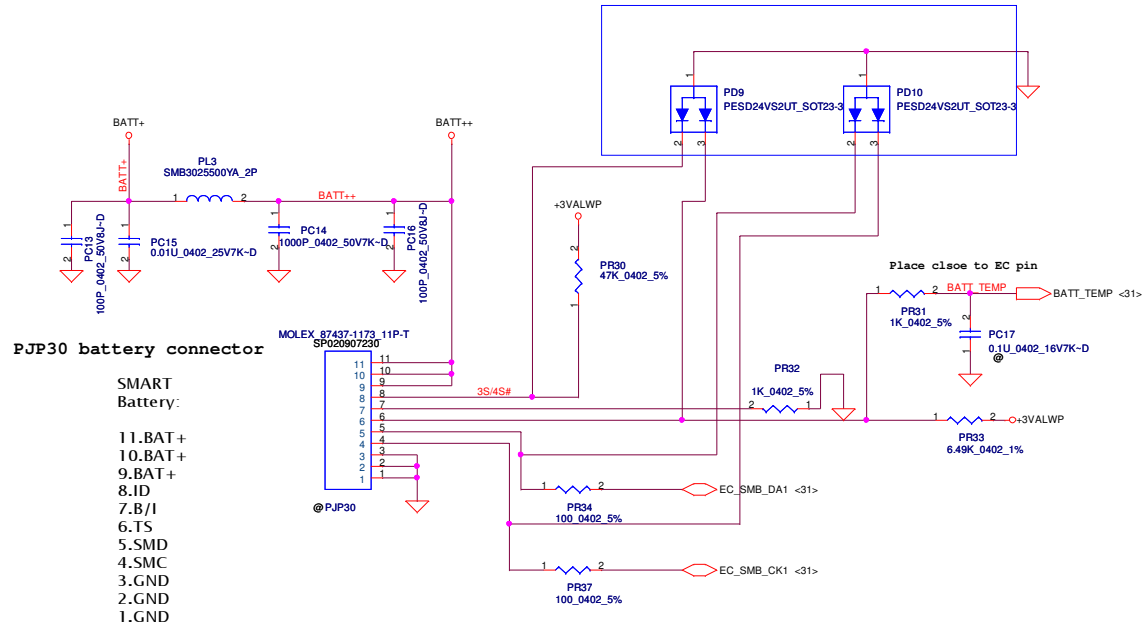
Ventura for GPU side
slave Address 1000110
please placement near R-sense

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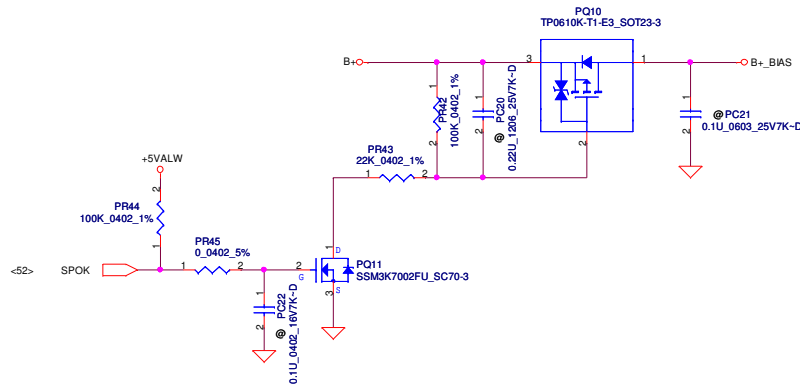
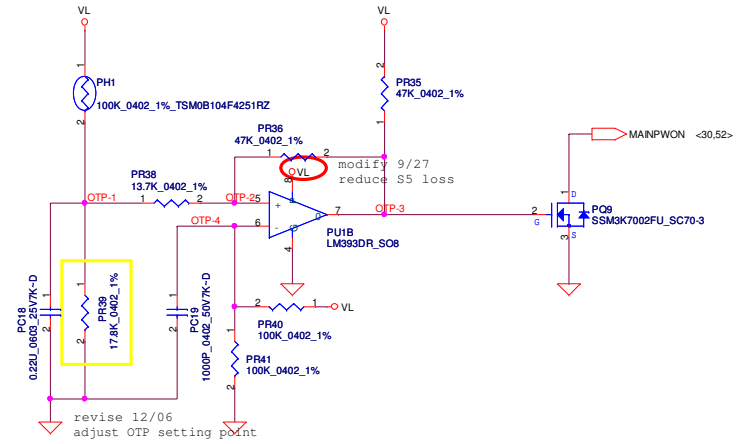
VENTURA

revise 8/09
ESD request



Battery Connect/OTP

PH1 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 50 degree C



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Version Change List (P. I. R. List)

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	50	PWR-DCIN / Vin Detector	10/09/17	COMPAL	reduce SS loss	add PU2;PR27;PC11;PC12	0.2
2	55	+VCCSAP/+1.5VSDGUP	10/09/21	COMPAL	RF request	add PR521;PC529 change PR520 from 0 to 2.2	0.2
3	57	+CPU_CORE	10/09/21	COMPAL	design change	change PR703 from 0 to 27.4K	0.2
4	51	CHARGER	10/10/06	COMPAL	design change	change PC131 from 0.1u to 1u	0.2
5	50	PWR-DCIN / Vin Detector	10/10/07	COMPAL	design change	add PQ12;PC23	0.2
6	54	+VCCPP/+1.8VSP	10/10/07	COMPAL	design change	modify 1.8VSP solution	0.2
7	51	CHARGER	10/10/19	COMPAL	EMI request	add PC126;PC128	0.2
8	55	+VCCSAP/+1.5VSDGUP	10/10/19	COMPAL	EE request	add PR528;PR529;PR530 del PR519	0.2
9	56	+VGA_CORE	10/10/19	COMPAL	EE request	add PR647;PR648 del PR603;PR604	0.2
10	51	CHARGER	10/10/25	COMPAL	design change	change PR114 from 47K to 0	0.2
11	54	+VCCPP/+1.8VSP	10/10/25	COMPAL	design change for use ventura curcuit	change PR401 from 0 to 0.01	0.2
12	56	+VGA_CORE	10/10/25	COMPAL	design change for use ventura curcuit	change PR601 from 0 to 0.01	0.2
13	57	+CPU_CORE	10/10/25	COMPAL	change CPU OCP setting	change PR758 from 887 to 953	0.2
14	57	+CPU_CORE	10/10/25	COMPAL	change GFX OCP & LL setting	change PR723 from 442 to 487 change PR713 from 2.61K to 2.43K	0.2
15	57	+CPU_CORE	10/10/25	COMPAL	quad & dual core CPU switch setting design	add PQ717;PQ718;PQ720;PR771;PR772;PR773;PR767;PR768;PC767;PC768	0.2
16	58	VENTURA	10/10/25	COMPAL	add ventura connect to EC	add PU801;PU802;PR803;PR804;PR805;PR806;PR807;PR808	0.2
						;PR811;PR813;PR814;PR819;PR823;PR824	0.2
17	57	+CPU_CORE	10/10/26	COMPAL	design change for solve acoustic issue	add PC766	0.3
18	52	3VALWP/5VALWP	10/10/27	COMPAL	design change for reserve adjust working frequency	add PR222	0.3
19	59	BATTERY CONN	10/12/06	COMPAL	adjust OTP setting point	change PR39 from 16.9K to 17.8K	0.3
20	50	PWR-DCIN / Vin Detector	10/12/13	COMPAL	design change for delete prechange circuit	del PR1;PR2;PR3;PR4;PR5;PR6;PR7;PD1;PD2;PQ1;PQ2;PQ3	0.3
21	51	CHARGER	10/12/13	COMPAL	design change for delete prechange circuit	del PR104;PQ110 add PR102	0.3
22	53	+1.5VP/+0.75VSP/+1.5VSP	10/12/13	COMPAL	EE request for use memory over clocking circuit	add PR312;PR318	0.3
23	53	+1.5VP/+0.75VSP/+1.5VSP	10/12/20	COMPAL	design change for adjust original output voltage	swap PR314;PR317 and PR320;PR323	0.4
24	51	CHARGER	10/12/21	COMPAL	design change for delete prechange circuit	del PC109	0.4
25	50	PWR-DCIN / Vin Detector	11/01/06	COMPAL	design change for add AC peak power function	add PR25	0.4
26	54	+VCCPP/+1.8VSP	11/01/11	COMPAL	EE request for adjust output voltage	change PR415 from 4.02K to 4.12K	0.4
27	55	+VCCSAP/+1.5VSDGUP	11/01/11	COMPAL	EE request for adjust output voltage	change PR524 from 10K to 10.5K	0.4
28	51	CHARGER	11/01/20	COMPAL	EMI request	add PL102	0.4
29	52	3VALWP/5VALWP	11/01/20	COMPAL	EMI request	add PL204	0.4

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