Easy to Use Power Bank Solution (EZPBS™) Integrated Chip with Switch Charger, MCU, ADC, and Load Switch

General Description

The RT9485 is a high integration and easy to use power solution for Li-ion power bank and other powered handheld applications. We call it EZPBS™ (Easy to Use Power Bank Solution). This single chip includes a Switching Charger with OTG function, MCU, Analog to Digital Converter (ADC), USBOUT Load Switch, Adapter Detection with BC1.2, DCP controller and LDO. The battery volume and the state of charging and discharging can be indicated by 4LEDs.

Applications

- Power Bank

Ordering Information

RT9485 □□-□

- Programmed Firmware Code AAX
  - AA : Application Code
  - X : Version Code
- Package Type
  - QV : VQFN-32L 4x4 (V-Type)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

AB= : Product Code

YMDNN : Date Code

AAX : Firmware Code

Features

System

- **High Accuracy Voltage/Current Regulation**
  - **±1% Charge Voltage Regulation**
  - **±0.1A Charge Current Regulation**
  - **±3% Boost Output Voltage Regulation**
- **Thermal Shutdown Protection**
- **Reverse Leakage Protection to Prevent Battery Drainage**
- **Built-in USBOUT DCP Controller**
- **Built-in USBOUT Attach/Detach Detection**
- **Built-in USBOUT Light Load Detection**
- **Built-in Load Switch with Current Regulation Thermal Regulation and Output Short Current Protection**
- **Built-In Adapter Detection with BC1.2**
- **Built-In Accurate ADC to Measure VBAT, VBUS, TS, IBAT, USBOUT and IUSBOUT**
- **Built-In LDO**
- **OTP Based MCU**
- **4 LED Driver Pin**
- **Button Key**

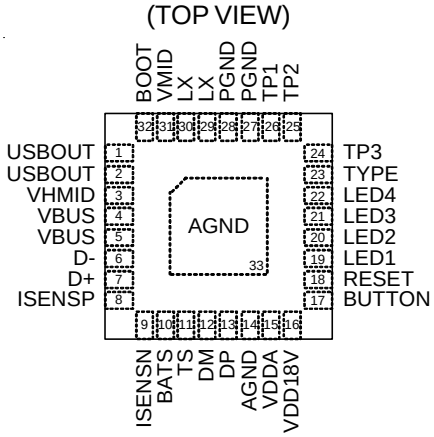
Charge Mode

- **Charge Voltage Regulation**
- **Charge Current Regulation**
- **Minimum Input Voltage Regulation (MIVR)**
- **Average Input Current Regulation (AICR)**
- **Thermal Regulation**
- **VMID Under-Voltage Protection**
- **VBUS Over-Voltage Protection**
- **Battery Over-Voltage Protection**
- **Battery Temperature Protection**

Boost Mode

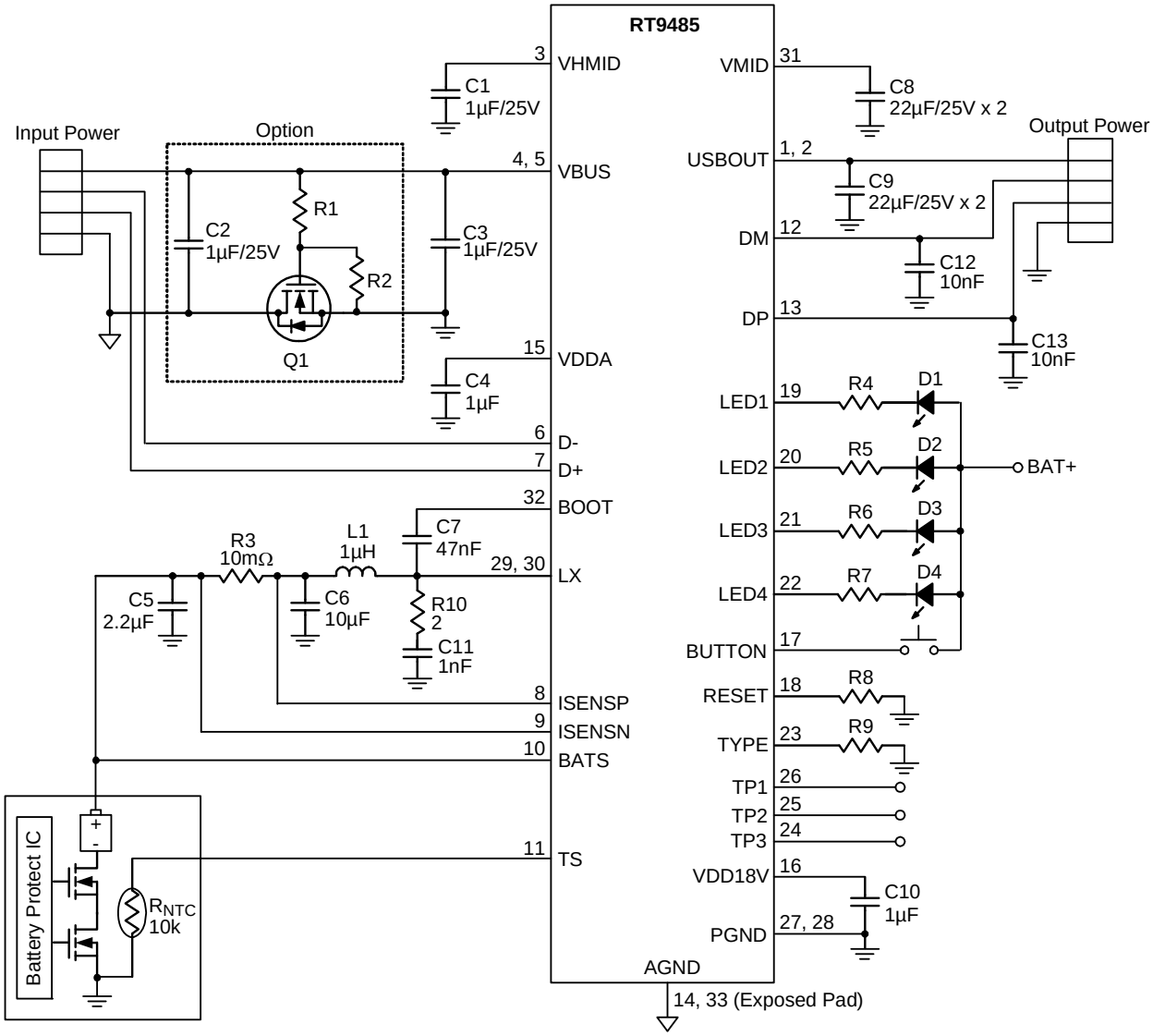
- **OTG Boost Current Up to 3A**
- **Battery Under-Voltage Protection**
- **VMID Over-Voltage Protection**

Pin Configuration



VQFN-32L 4x4

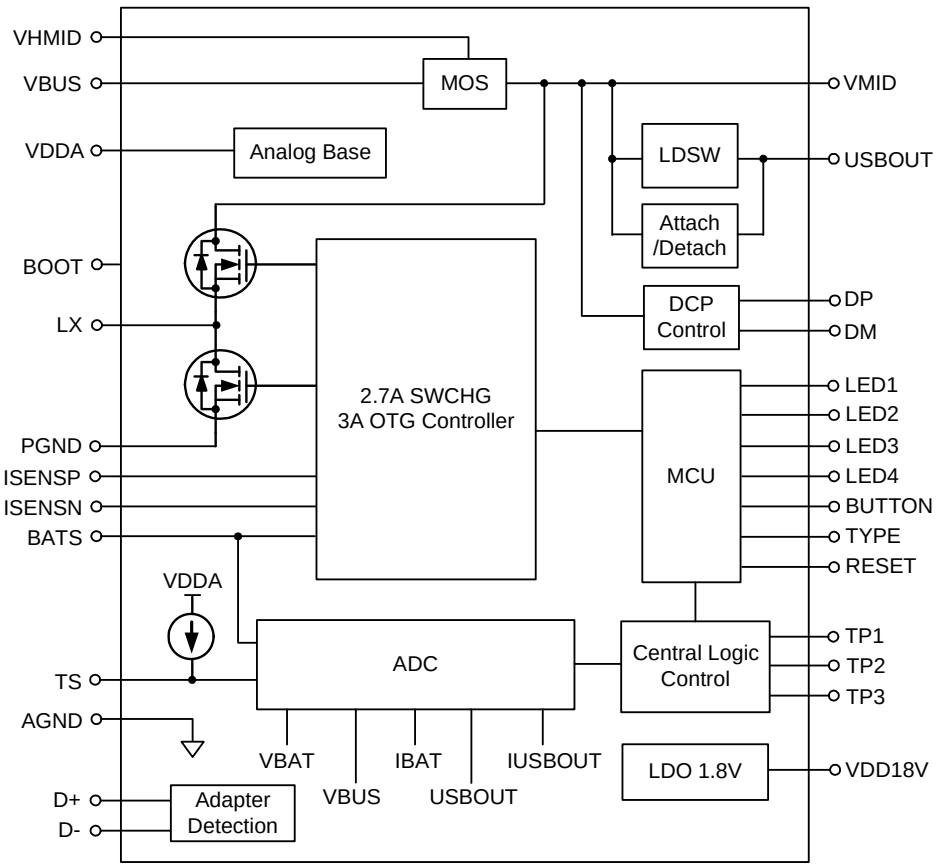
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 2	USBOUT	USB power output.
3	VHMID	Internal use only.
4, 5	VBUS	VBUS power supply.
6	D-	D- input for adapter detection.
7	D+	D+ input for adapter detection.
8	ISENSP	Charging current sensing positive node.
9	ISENSN	Charging current sensing negative node and connect to battery plus terminal.
10	BATS	Battery voltage sensing node.
11	TS	Battery temperature detection pin.
12	DM	DCP controller DM output.
13	DP	DCP controller DP output.
14, 33 (Exposed Pad)	AGND	Analog ground node. The exposed pad must be soldered to a large PCB and connected to AGND for maximum power dissipation.
15	VDDA	Internal power for analog blocks, put 1μF to GND.
16	VDD18V	External use LDO output.
17	BUTTON	Button detection pin.
18	RESET	Reset for internal use. Connect 10kΩ resister to ground.
19	LED1	Current sink output for LED1.
20	LED2	Current sink output for LED2.
21	LED3	Current sink output for LED3.
22	LED4	Current sink output for LED4.
23	TYPE	General input pin for select battery charge voltage low is 4.2V and high is 4.35V.
24	TP3	Test pin. Keep floating. (SCL).
25	TP2	Test pin. Keep floating. (SDA).
26	TP1	Test pin. Keep floating. (INT).
27, 28	PGND	Power ground for switching charger.
29, 30	LX	Internal switch node to output inductor connection.
31	VMID	Connection point between reverse blocking and high-side.
32	BOOT	Bootstrap power node for switching charger.

Functional Block Diagram



Operation

The RT9485 is a high integrated IC for Li-Ion battery power bank. It includes a Switch charger 2.7A, a synchronous Boost 5V.

Charge Current

Base on thermal regulation function, the charging current can support up to 2.7A.

VBUS Over Voltage Protection

If the input voltage (VBUS) is higher than the threshold voltage VOVP, the internal OVP signal will go high and the charger will stop charging until VIN is below V_{OVP} - hysteresis.

VMID Over Voltage Protection

If the internal voltage (VMID) is higher than the threshold voltage V_{OVP}, the internal OVP signal will go high and the charger will stop charging until VMID is below V_{OVP} - hysteresis.

VMID Under Voltage Protection

If the internal voltage (VMID) is lower than the threshold voltage VUVP, the internal VMID_UVP signal will go high and the system will disable LDSW function in order to protect system from short-to-ground current damages.

USBOUT SCP

The USBOUT short circuit protection (SCP) function will prevent system from burning out by monitoring the voltage drop between LDSW. If the USBOUT is short to ground, the inrush current will make the VDS voltage too large to damage chip. The SCP function also reports this condition to protect chip in time.

Boost OCP

The converter senses the current signal when the high-side P-MOSFET turns on. As a result, The OCP is cycle by-cycle current limitation. If the OCP occurs, the converter holds off the next on pulse until inductor current drops below the OCP limit.

OTP

The converter has an over-temperature protection.

When the junction temperature is higher than the thermal shutdown rising threshold, the system will be latched and the output voltage will no longer be regulated until the junction temperature drops under the falling threshold.

CC/CV/TR Multi Loop Controller

There are constant current loop, constant voltage loop and thermal regulation loop to control the charging current.

Base Circuits

Base circuits provide the internal power, VDDA and reference voltage and bias current.

Buck Regulator for Charging and Boost Regulator as BOOST

The multi-loop controller controls the operation of charging process and current supply to the system. It also controls the circuits as a Boost converter for BOOST applications.

USB Charger Detection

The RT9485 detects USB Charger (Standard Charger Port, Charging Downstream Port and Dedicated Charger Port) via D+ and D- pins.

USBOUT Attach/Detach Detection

RT9485 includes an auto attach detection for the power bank product. The attach detection has a current threshold which represent an attach condition. When the attach detection is enable, the USBOUT will generate a 1.6V to monitor the load current. Once load current is greater than 5μA, the attach flag will be reported until the load current is removed.

Embedded Micro-Controller

The MCU control the power bank behavior, decide the operation mode for charging, discharging or relax. MCU also detects the button press, battery type and control LED flash function. It is use One Time Programmable (OTP) memory, the power bank function can flexible adjust for different application.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VBUS, VHMID ---------- –0.3V to 18V
- VMID ---------- –0.3V to 6.7V
- LX ---------- –0.3V to 6V
- BOOT ---------- –0.3V to 12V
- BOOT – LX ---------- –0.3V to 6V
- VHMID – VBUS ---------- –0.3V to 6V
- VHMID – VMID ---------- –0.3V to 18V
- Others ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  VQFN-32L 4x4 ---------- 3.59W
- Package Thermal Resistance (Note 2)
  VQFN-32L 4x4, θ_{JA} ---------- 27.8°C/W
  VQFN-32L 4x4, θ_{JC} ---------- 4.6°C/W
- Junction Temperature Range ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VBAT, VBUS ---------- 4.3V to 5.65V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{BUS} = 5V, V_{BAT} = 4.2V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Power Source						
VBUS Operation Range			4	--	5.65	V
VBUS Supply Current	I_Q	PWM switching, I_{CHG} = I_{BAT} = 0mA	--	10	--	mA
		High impendence mode	--	--	200	μA
Leakage Current from Battery	I_{BAT_LEAK}	V_{BAT} = 4.2V, V_{BUS} = 0V, Charger off. 1/80 ADC execution time duty	--	50	70	μA
Protection						
VBUS OVP Threshold Voltage	V_{BUS_OVP}	VBUS rising	5.7	6	6.3	V
VBUS OVP Hysteresis	$V_{BUS\_OVP\_HYS}$	VBUS falling	--	200	--	mV
VBUS UVLO	V_{BUS_UVLO}	VBUS rising	3	3.25	3.5	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VBUS UVLO Hysteresis	$V_{BUS\_UVLO\_HYS}$	VBUS falling	--	150	--	mV
ISENSN OVP	V_{BAT_OVP}	VISENSN rising	103	107	114	%
ISENSN OVP Hysteresis	$V_{BAT\_OVP\_HYS}$	VISENSN falling	--	5	--	%
Over-Temperature Protection	T_{OTP}	(Note 5)	--	160	--	°C
OTP Hysteresis	T_{OTP_HYS}		--	20	--	°C
Thermal Regulation Threshold	T_{REG}	(Programmable)	--	120	--	°C
Input Power Source Detection						
Poor Source Detect Threshold	V_{BUS_pr}	Bad voltage source detection	3.6	3.8	4	V
Poor Source Detect Deglitch	$t_{VBUS\_pr\_dg}$		--	30	--	ms
Poor Source Detect Hysteresis	$V_{BUS\_pr\_hys}$	VBUS rising	100	--	200	mV
Current Sink to GND	I_{VBUS_pr}	During poor source detection	--	50	--	mA
Detection Interval Time	$t_{VBUS\_pr\_int}$		--	2	--	s
Sleep Mode Comparator						
Sleep-Mode Entry Threshold VBUS - ISENSN	V_{SLP}	3V < V_{ISENSN} < V_{BATREG}, VBUS Falling	--	40	100	mV
Sleep-Mode Exit Hysteresis VBUS – ISENSN	$V_{SLPEXIT}$	3V < V_{ISENSN} < V_{BATREG}, VBUS Rising	40	120	200	mV
Sleep-Mode Deglitch Time	t_{SLP}	VBUS Rising Above V_{SLP} + $V_{SLPEXIT}$	--	30	--	ms
Minimum Input Voltage Regulation (MIVR)						
Minimum Input Voltage Regulation	V_{MIVR}	(Programmable)	4.2	--	4.8	V
V_{MIVR} Accuracy			–5	--	5	%
Average Input Current Regulation (AICR) Accuracy	I_{AICR_100mA}	I_{AICR} = 100mA	80	90	100	mA
	I_{AICR_500mA}	I_{AICR} = 500mA	400	450	500	
	I_{AICR_700mA}	I_{AICR} = 700mA	560	630	700	
	I_{AICR_1000mA}	I_{AICR} = 1000mA	800	900	1000	
AICR	I_{AICR}	(Programmable)	100	--	2000	mA
VDDA Regulator						
VDDA Voltage	VDDA	V_{VBUS} > 4.5V	--	4.5	--	V
		V_{VBUS} < V_{ISENSN}	--	V_{ISENSN}	--	
VDDA UVLO	V_{DDA_UV}	VDDA rising	2.4	2.5	2.6	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDDA UVLO Hysteresis	$V_{DDA\_UV\_hys}$	VDDA falling	--	150	--	mV
Battery Voltage Regulation						
Battery Voltage Regulation	V_{BATREG}	(Programmable)	3.65	--	4.6	V
V_{BATREG} Accuracy			–1	--	1	%
Re-Charge Threshold	ΔV_{REG}	V_{ISENSN} falling, $\Delta V_{REG} = (V_{BATREG} - V_{REC})$	50	125	200	mV
Re-Charge Deglitch Time	t_{REC}		--	128	--	ms
Charging Current Regulation						
Output Charging Current	I_{CHG}	R_{SENSE} = 10mΩ (Programmable)	0.7	--	2.7	A
I_{CHG} Accuracy	I_{CHG_ACC}	R_{SENSE} = 10mΩ	–100	--	100	mA
Pre-Charge Threshold	V_{PREC}	Rising, (programmable)	2.3	--	3.8	V
V_{PREC} Accuracy			–5	--	5	%
Pre-Charge Current	I_{PREC}	(Programmable)	200	300	500	mA
I_{PREC} Accuracy			–20	--	20	%
Charge Termination Detection						
End of Charge Current	I_{EOC}	R_{SENSE} = 10mΩ (Programmable)	150	--	600	mA
I_{EOC} Accuracy		R_{SENSE} = 10mΩ	–100	--	100	mA
Deglitch Time for EOC	t_{EOC}	$I_{CHG} < I_{EOC}$, $V_{ISENSN} > (V_{BATREG} - \Delta V_{REG})$ (Programmable)	4	--	32	ms
Charger Timer Protection						
Fast-Charge Time-Out		(Programmable)	6	--	20	Hrs
Pre-Charge Time-Out		(Programmable)	30	--	60	Mins
PWM Switching Charger						
VBUS to LX Resistance	$R_{DS(ON)\_VBUS\_LX}$	From VBUS to LX, as IAICR disable or I_{AICR} = 2A	--	130	--	mΩ
VBUS to USBOUT Resistance	$R_{DS(ON)\_VBUS\_USBOUT}$	From VBUS to USBOUT	--	120	--	mΩ
Low-Side On-Resistance	$R_{DS(ON)\_LS}$	From LX to PGND	--	40	--	mΩ
Efficiency for Charge	EFF_CHG	V_{BUS} = 5V, V_{ISENSN} = 4V, and I_{CHG} = 2A	--	90	--	%
Oscillator Frequency	f_{OSC}		--	0.75	--	MHz
Frequency Accuracy			–10	--	10	%
Maximum Duty Cycle	D_{MAX}	At minimum voltage input	--	95	--	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Minimum Duty Cycle	$D_{(MIN)}$		0	--	--	%
Peak OCP as Charger Mode			--	4.5	--	A
Boost Mode Operation						
Output Voltage Level	V_{BOOST}	To VMID (programmable)	3.625	--	5.2	V
Output Voltage Accuracy			–3	--	3	%
Output Current On VMID	I_{BST}	V_{BAT} > 3V	3	--	--	A
Efficiency for Boost	EFF_BST	V_{MID} = 5V, V_{ISENSN} = 4V, and loading = 2A	--	92	--	%
Peak OCP as Boost Mode	I_{OCP_BST}		--	6	--	A
VMID OVP as Reverse Boost	V_{OVP_BST}	VMID rising	--	6	--	V
VMID OVP Hysteresis	$V_{OVP\_BST\_HYS}$	VMID falling	--	200	--	mV
Battery UVP for Boost	V_{BATMIN}	Falling, (programmable)	2.5	--	3.2	V
NTC Function						
Current Source for NTC 10kΩ	ITS_10k		33	35	37	μA
Load Switch for USBOUT						
Supply Voltage	V_{SW}		2.5	5	5.5	V
Load Switch On Resistance of MOSFET	$R_{DS(ON)\_SW}$	VMID = 5V, I_O = 1000mA	--	35	--	mΩ
Load Switch UVP Delta	$V_{SW\_UVP\_D}$	VMID – VUSBOUT	--	1.4	--	V
Light Load Detection Current	I_{DET}	Detection current	--	10	--	mA
Thermal Regulation Threshold of the Load Switch	T_{REG_LSW}	(Programmable)	--	100	--	°C
Adapter Detection						
D+ Voltage Source	V_{D+_SRC}		0.5	--	0.7	V
VDAT_REF Voltage	V_{DAT_REF}		0.25	--	0.4	V
VLGC Voltage	V_{LGC}		0.8	--	2	V
D- Sink Current	I_{DN_SINK}		50	--	150	μA
USBOUT Attach/Detach Detection						
USBOUT Attach Voltage		I_{USBOUT} = 1.5μA	1.4	1.6	1.8	V
USBOUT Attach/Detach Threshold		C_{USBOUT} = 40μF (Note 6)	1	5	10	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Detect Time 1		V_{BAT} = 3V, C_{OUT} = 30μF, 0x24[4:2] = 010	--	375	--	ms
Detect Time 2		V_{BAT} = 3V, C_{OUT} = 50μF, 0x24[4:2] = 100	--	600	--	ms
LDO 1.8V						
Output Voltage	$V_{OUT\_1.8V}$	C_{OUT} = 1μF	1.71	1.8	1.89	V
Output Current	$I_{OUT\_1.8V}$		10	--	--	mA
The Time for V_{OUT} Ready	$t_{RDY\_1.8V}$	C_{OUT} = 1μF	1	--	3	ms
ADC Characteristics						
Resolution			--	12	--	Bit
Measurement Error	V_{GERR}	VBAT, TS	–10	--	10	mV
		VBUS, USBOUT	–50	--	50	mV
		I_{BAT} < 1A	–100	--	100	mA
		I_{BAT} > 1A	–10	--	20	%
		I_{USBOUT} < 1A	–100	--	100	mA
		I_{USBOUT} > 1A	–10	--	10	%
Conversion Time	t_{CONV}		--	--	25	ms
Input Power						
DCP Controller Power UVLO Threshold Voltage from VMID	$V_{UVLO\_R\_DCP\_CTRL}$	Rising	3.9	4.1	4.3	V
UVLO Hysteresis	$V_{UVLO\_F\_DCP\_CTRL}$	Falling	100	200	300	mV
DCP Controller Supply Current	I_{DCP_CTRL}	4.5V < V_{UID} < 5V	--	150	200	μA
BC1.2 DCP Mode						
DP and DM Shorting Resistance	R_{DPM_SHORT}	V_{DP} = 0.8V, I_{DM} = 1 mA	--	157	200	Ω
Resistance between DP/DM and GND	R_{DCHG_SHORT}	DP = 0.8V	350	656	1150	kΩ
Voltage Threshold on DP1 Under which the Device goes back to Divider Mode	$V_{DPL\_TH\_DET}$	Falling	310	330	350	mV
Hysteresis	$V_{DPL\_TH\_DET\_HYS}$	Rising	--	50	--	mV
DIVIDER Mode						
DP Output Voltage for DIVIDER Mode	$V_{DP\_2.7V}$	V_{UID} = 5V	2.57	2.7	2.84	V
DM Output Voltage for DIVIDER Mode	$V_{DM\_2.7V}$	V_{UID} = 5V	2.57	2.7	2.84	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
DP Output Impedance for DIVIDER Mode		R_{DP_PAD1}	I_{DP} = –5μA	24	30	36	kΩ
DM Output Impedance for DIVIDER Mode		R_{DM_PAD1}	I_{DM} = –5mA	24	30	36	kΩ
DP and DM Shorting Resistance		R_{PM_short}		--	150	200	Ω
1.2V / 1.2V Mode							
DP Output Voltage for 1.2V Mode		$V_{DP\_1.2V}$		1.12	1.2	1.28	V
DP Output Impedance for 1.2V Mode		R_{DP_PAD}		80	102	130	kΩ
TYPE Level							
TYPE	Logic-High	V_{IH_B}		0.7 x VDDA	--	--	V
	Logic-Low	V_{IL_B}		--	--	0.3 x VDDA	
BUTTON Level							
BUTTON	Logic-High	V_{IH_B}		0.7 x VDDA	--	--	V
	Logic-Low	V_{IL_B}		--	--	0.3 x VDDA	
RESET Level							
RESET	Logic-High	V_{IH_B}		0.7 x VDD18V	--	--	V
	Logic-Low	V_{IL_B}		--	--	0.3 x VDD18V	
LED Output							
LED Open Drain		V_{LED}	I_{SINK} = 10mA	--	--	200	mV

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

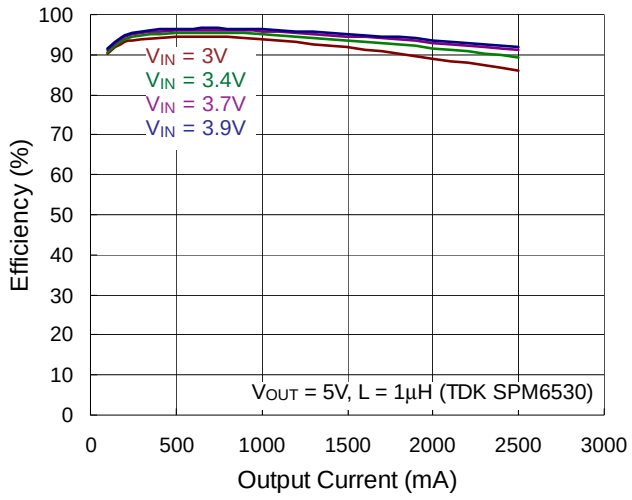
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guarantee by Design.

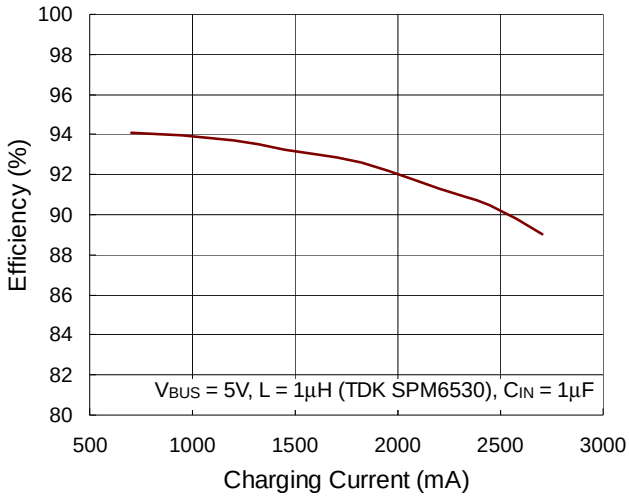
Note 6. It will attach when only plug-in APPLE charging line.

Typical Operating Characteristics

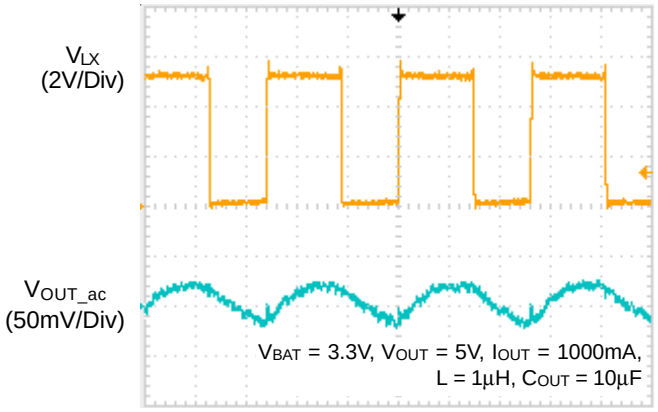
Boost Efficiency vs Output Current



Charging Efficiency vs. Charging Current



Steady State



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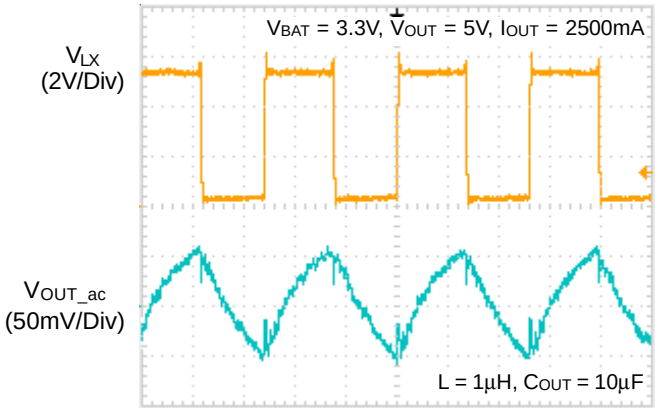

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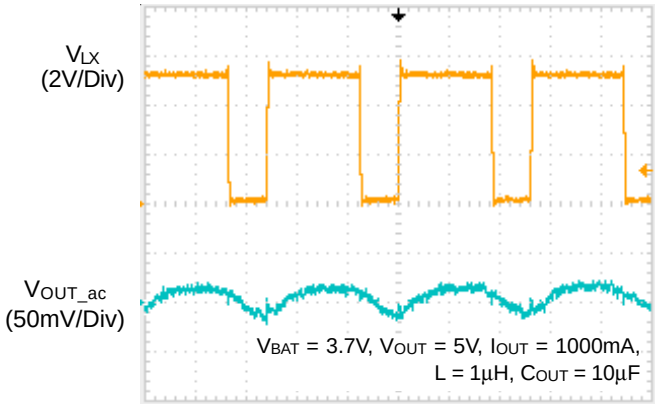
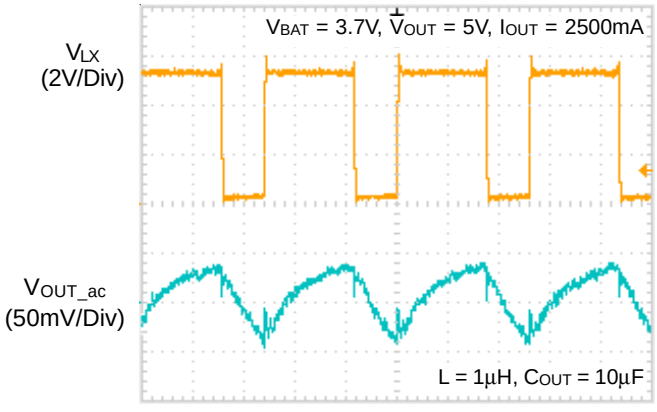


Steady State



Application Information

MCU Functional Block Diagram

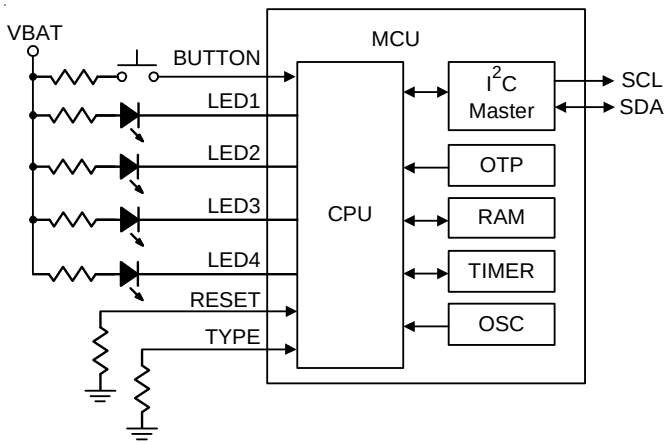


Figure 1. MCU Hardware Block Diagram

The kernel of MCU is a high performance and low power CPU, the program code is store in a One Time Programmable (OTP) memory. The MCU control the charge and discharge scenario, battery type selection, button detection, LED SOC look up and LED flash.

I²C Master

MCU is via I²C interface to control the switch charger, ADC, Adapter Detection, DCP controller and Load Switch what the IPs in the RT9485. I²C master can transport the I²C physical layer protocol byte by byte.

TYPE

The TYPE pin is use for select the 4.2V battery type or 4.35V. Battery type will be set to 4.2V when TYPE pin is pull low, otherwise battery type is set to 4.35V.

BUTTON

The button pin detects the button is press or not. It will trigger the interrupt to MCU when button pressed.

LED

There are four LED pins for LED driver. Its IO structure is open-drain. The LED flash sequence is defined by firmware program for increase the application flexibility.

TIMER

There are three types timer for firmware usage. They are RTC, TIMER and WDT respectively. The RTC and TIMER include interrupt function to trigger MCU. The WDT can reset MCU when system is crash.

Power Bank Function Overview

Operation Mode

There are four main operation modes in the power bank operation state machine. They are Power on, Relax, CHG and DCHG respectively.

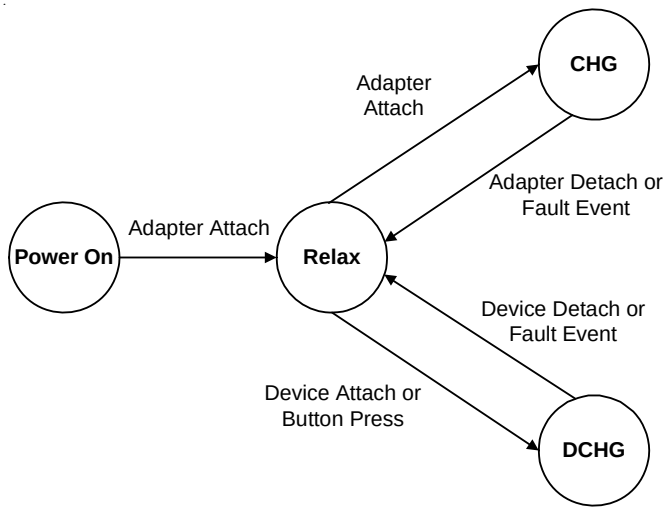


Figure 2. Power Bank Operation State Machine

Power ON

Once the RT9485 is power on, firmware will complete all initial setting and system check then keep in the power on stage. The discharge is not available when device connect to power bank before button press or adapter connection. It can prevent wrong operation during power bank assembly.

Relax

The state is enter relax mode if there is no adapter and device connect. For saving the power consumption there are only adapter and device detect function will be enabled in the relax mode. Besides, MCU will periodical wake by RTC and to monitor the whole system status.

CHG

The charge state will be started if adapter attach and battery status is suitable for charge. The basic condition to cause stop charging is the temperature of battery over the safety range 0 to 50°C.

The total sink current form adapter will follow the specification of BC1.2. JEITA is also implemented for make safe battery charging and lengthen the battery life.

The power of adapter is also bypass to USBOUT port, it can make device and battery charging at the same time.

DCHG

There are two event trigger discharge state, device attach and button press. The firmware will check the battery voltage and temperature then stop discharge when battery low or over safe temperature range –20 to 60°C. The USBOUT output over/short current is also protected.

LED SOC Look Up

Power bank LED number is judge by battery voltage and defined threshold. There are four thresholds to indicate 0%, 25%, 50%, 75% battery capacity. MCU to measure the battery voltage by ADC and look up the voltage is under which one LED level. MCU is also measure the current and temperature of battery and do the compensation. It can prevent the abnormal LED number drop or jump.

LED Flash

LED display has charge and discharge mode. The following table shows LED flash behavior for charging and discharging mode.

Table 1. LED Flash Table in The Charging Mode

Charge Mode				
SOC	**LED1**	**LED2**	**LED3**	**LED4**
0 to 25%	Flash	OFF	OFF	OFF
25 to 50%	ON	Flash	OFF	OFF
50 to 75%	ON	ON	Flash	OFF
75-Full Charge	ON	ON	ON	Flash
Full Charge	ON	ON	ON	ON

Table 2. LED Flash Table in The Discharging Mode

Discharge Mode				
SOC	**LED1**	**LED2**	**LED3**	**LED4**
Under Voltage	Flash 5sec	OFF	OFF	OFF
0 to 25%	Flash	OFF	OFF	OFF
25 to 50%	Flash	Flash	OFF	OFF
50 to 75%	Flash	Flash	Flash	OFF
75- Full Charge	Flash	Flash	Flash	Flash

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a VQFN-32L 4x4 package, the thermal resistance, θ_{JA}, is 27.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (27.8°C/W) = 3.59W for a VQFN-32L 4x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

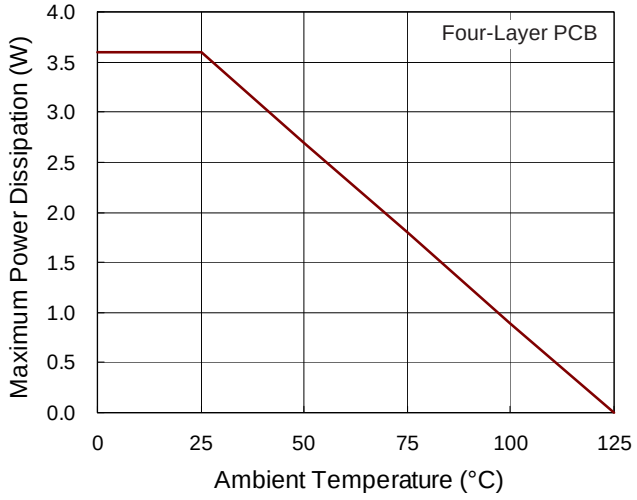


Figure 3. Derating Curve of Maximum Power Dissipation

Layout Considerations

Some PCB layout guidelines for optimal performance of RT9485 list as following. Following figure shows the real PCB layout considerations and it is based on the real component size whose unit is millimeter (mm).

- Place the input and output capacitors as close to the input and output pins as possible.
- Keep the main power traces as wide and short as possible.
- The output inductor and boot capacitor should be placed close to the chip and LX pins.
- The battery voltage sensing point should be placed after the output capacitor.
- To optimize current sense accuracy, connect the traces to RSENSE with Kelvin sense connection by ISENSN and ISENSP.
- LX node is with high frequency voltage swing and should be kept small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.
- Add Snubber in LX : 2Ω resister 0805 package and 1nF capacitor.

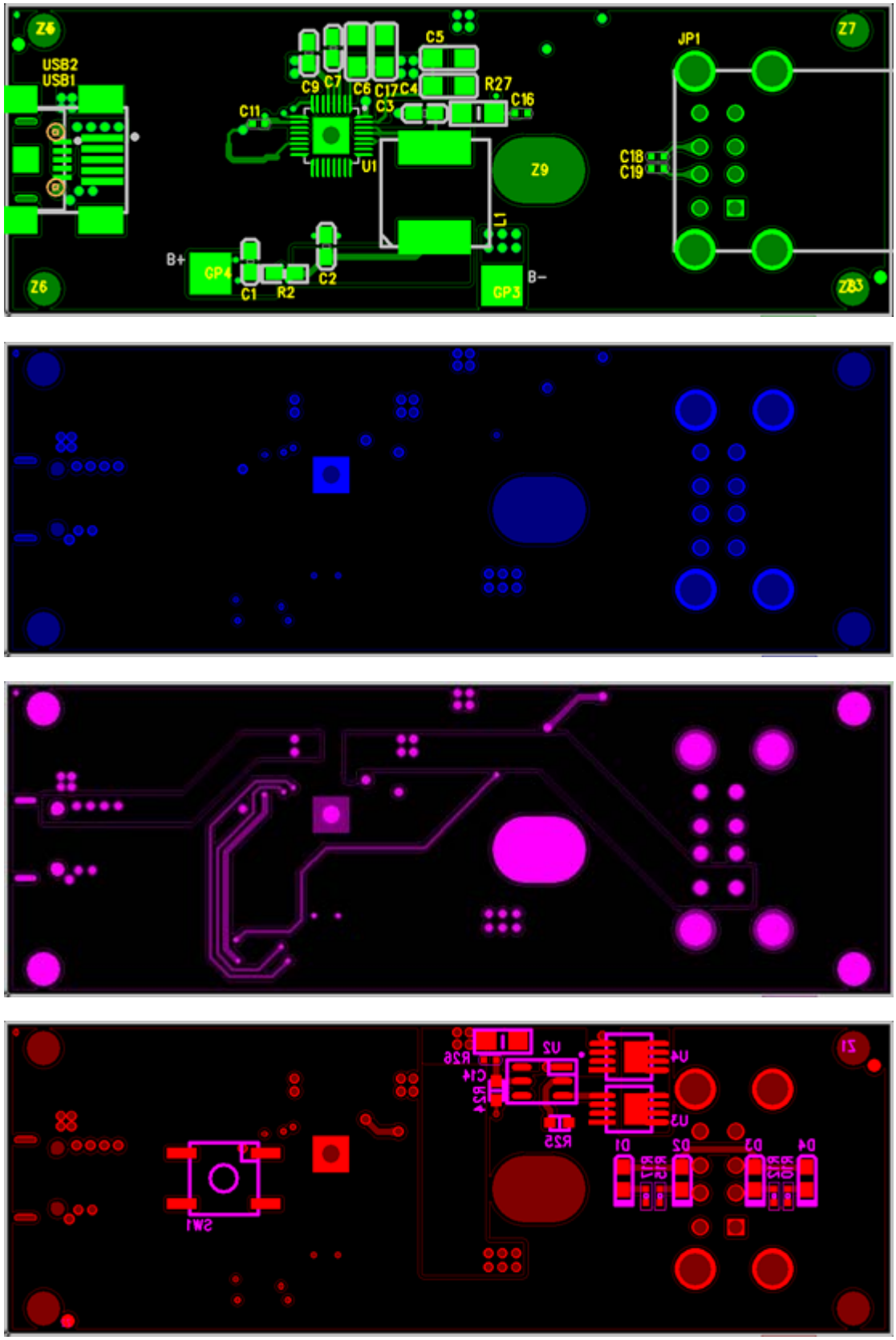
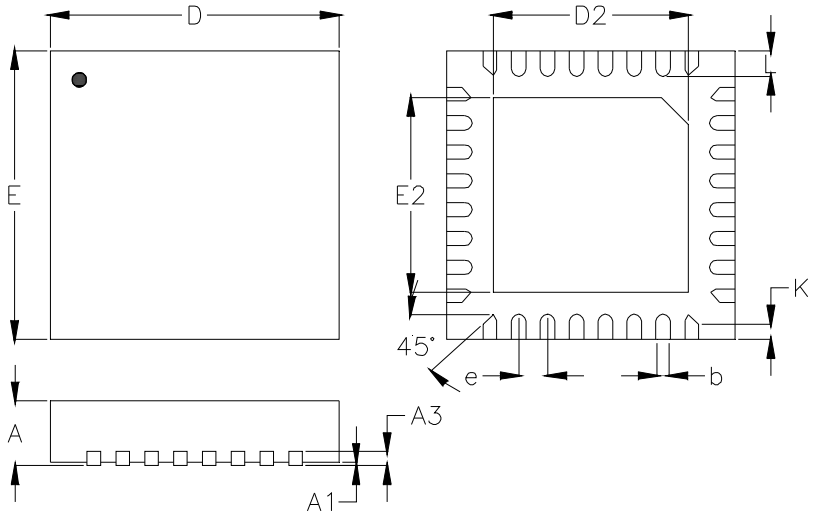
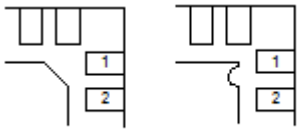


Figure 4. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	3.950	4.050	0.156	0.159
D2	2.650	2.750	0.104	0.108
E	3.950	4.050	0.156	0.159
E2	2.650	2.750	0.104	0.108
e	0.400		0.016	
L	0.300	0.400	0.012	0.016
K	0.200		0.008	

V-Type 32L QFN 4x4 Package

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