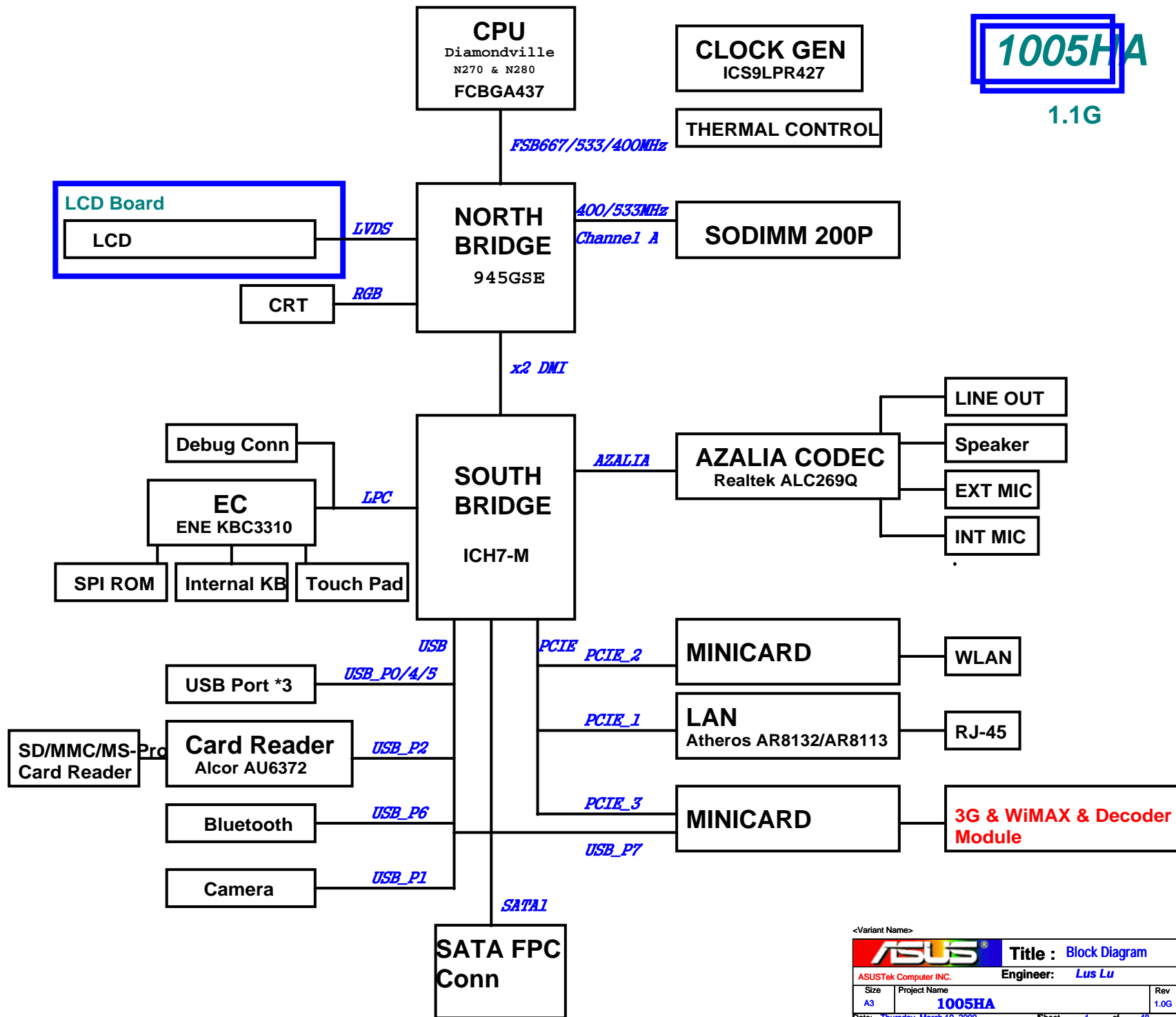


01\_Block Diagram  
02\_System Setting  
03\_Power Sequence  
04\_Clock Gen\_ICS9LPR434  
05\_Diamondville\_BUS  
06\_Diamondville\_PWR  
07\_NB-945GMS(HOST)  
08\_NB-945GMS(DMI)  
09\_NB-945GMS(GRAPHIC)  
10\_NB-945GMS(DDR2)  
11\_NB-945GMS(PWR)  
12\_NB-945GMS(PWR2)  
13\_NB-945GMS(GND)  
14\_SB-ICH7M(PWR)  
15\_SB-ICH7M(1)  
16\_SB-ICH7M(2)  
17\_SB-ICH7M(3)  
18\_DDR2 SODIMM  
19\_DDR2\_Termination  
20\_Onboard VGA  
21\_LCD Conn\_LID  
22\_Blank  
23\_Mini WiFi+ BT  
24\_LAN\_Atheros AR8113  
25\_RJ45  
26\_Flash Conn  
27\_USB Port  
28\_Camera Conn  
29\_Card Reader\_AU6372A51  
30\_Codec\_ALC269  
31\_Audio\_AMP\_Jack  
32\_EC\_ENE KB3310  
33\_EC  
34\_Switch\_SPI ROM\_Debug Conn  
35\_Thermal Sensor\_FAN  
36\_KB\_Touch Pad  
37\_LED\_THERMTRIP  
38\_Discharge  
39\_PWR Jack  
40\_Srew Hole  
41\_EMI  
42\_POWER FLOW  
43\_Vcore  
44\_Power System  
45\_Power\_+1.8V & VTTDDR  
46\_Power\_VCCP  
47\_Power\_+1.5VS & +2.5VS  
48\_Power\_Charger  
49\_EC Pin Define  
49\_History



EEE PC 701 PCB version

GPI37	GPI38	GPI39	PCB version
0	0	0	
0	0	0	
0	0	1	
0	0	1	
0	1	0	
0	1	0	
0	1	1	
0	1	1	
1	0	0	
1	0	0	
1	0	1	
1	0	1	
1	1	0	
1	1	0	
1	1	1	
1	1	1	

USB

USB 0	NC
USB 1	USB Conn
USB 2	USB Conn
USB 3	USB Conn
USB 4	Card Reader
USB 5	Minicard
USB 6	Bluetooth
USB 7	Camera


PCIE

PCIE 1	NC
PCIE 2	LAN
PCIE 3	Minicard
PCIE 4	SSD

Azalia

ACZ_SDIN0	CODEC
ACZ_SDIN1	NC
ACZ_SDIN2	NC

<Variant Name>

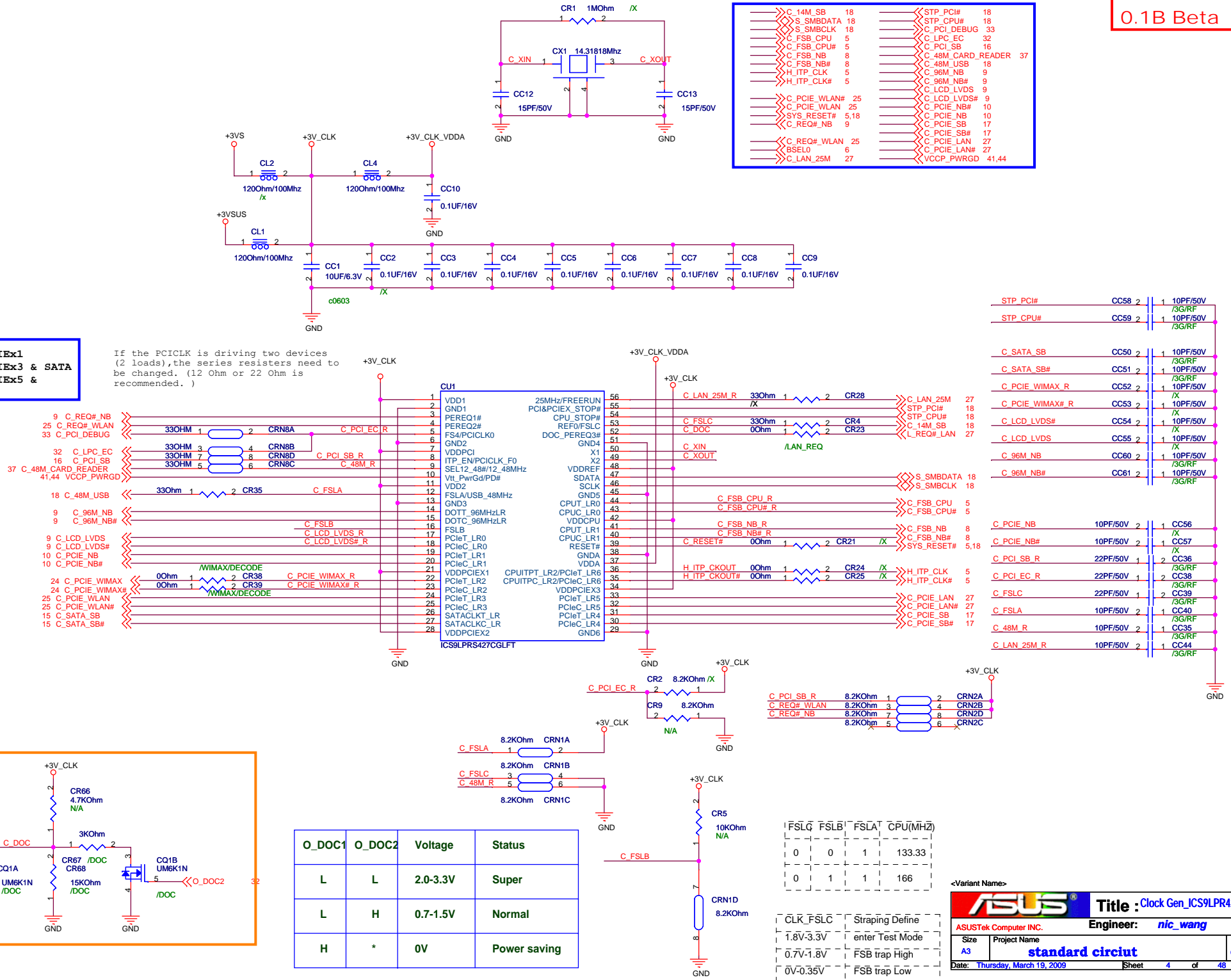
		Title : System Setting	
ASUSTek Computer INC.		Engineer: Satan_He	
Size	Project Name	Rev	
A3	1005HA	1.0G	
Date: Thursday, March 19, 2009		Sheet	2 of 48

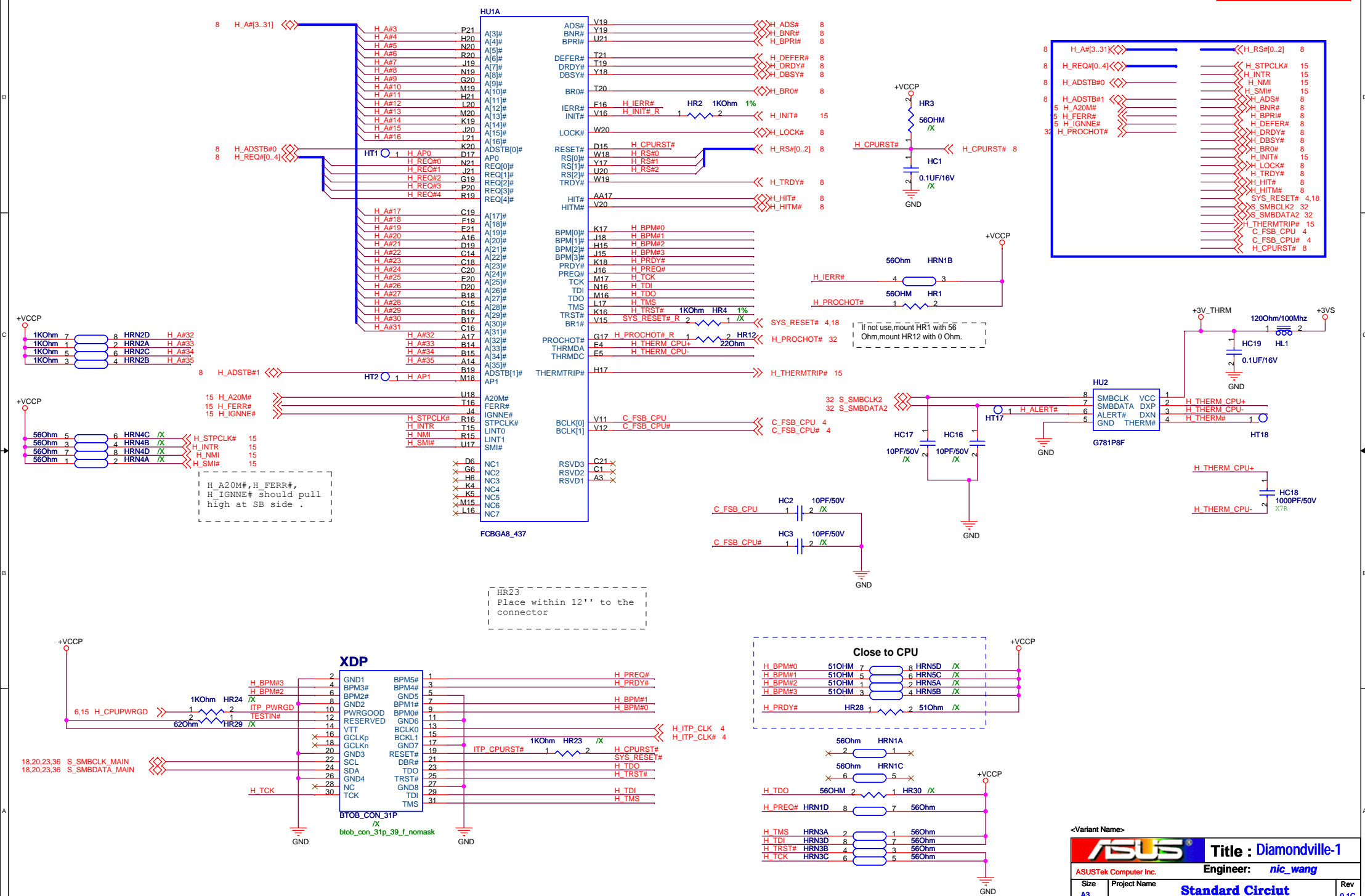


1:Disable  
0:Enable

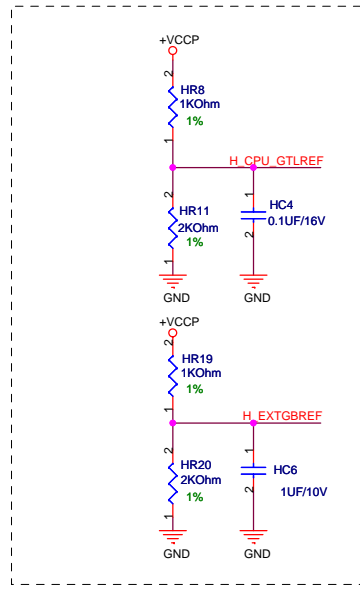
PEREQ1:PCIEx0 & PCIEx1  
PEREQ2:PCIEx2 & PCIEx3 & SATA  
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

If the PCICLK is driving two devices (2 loads), the series resistors need to be changed. (12 Ohm or 22 Ohm is recommended.)

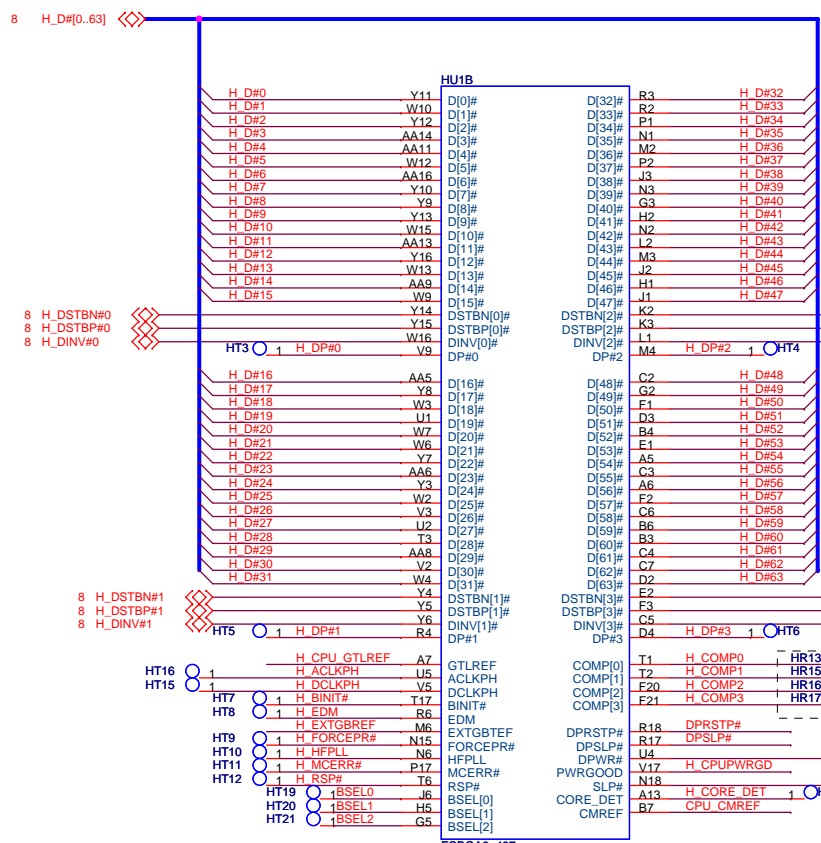


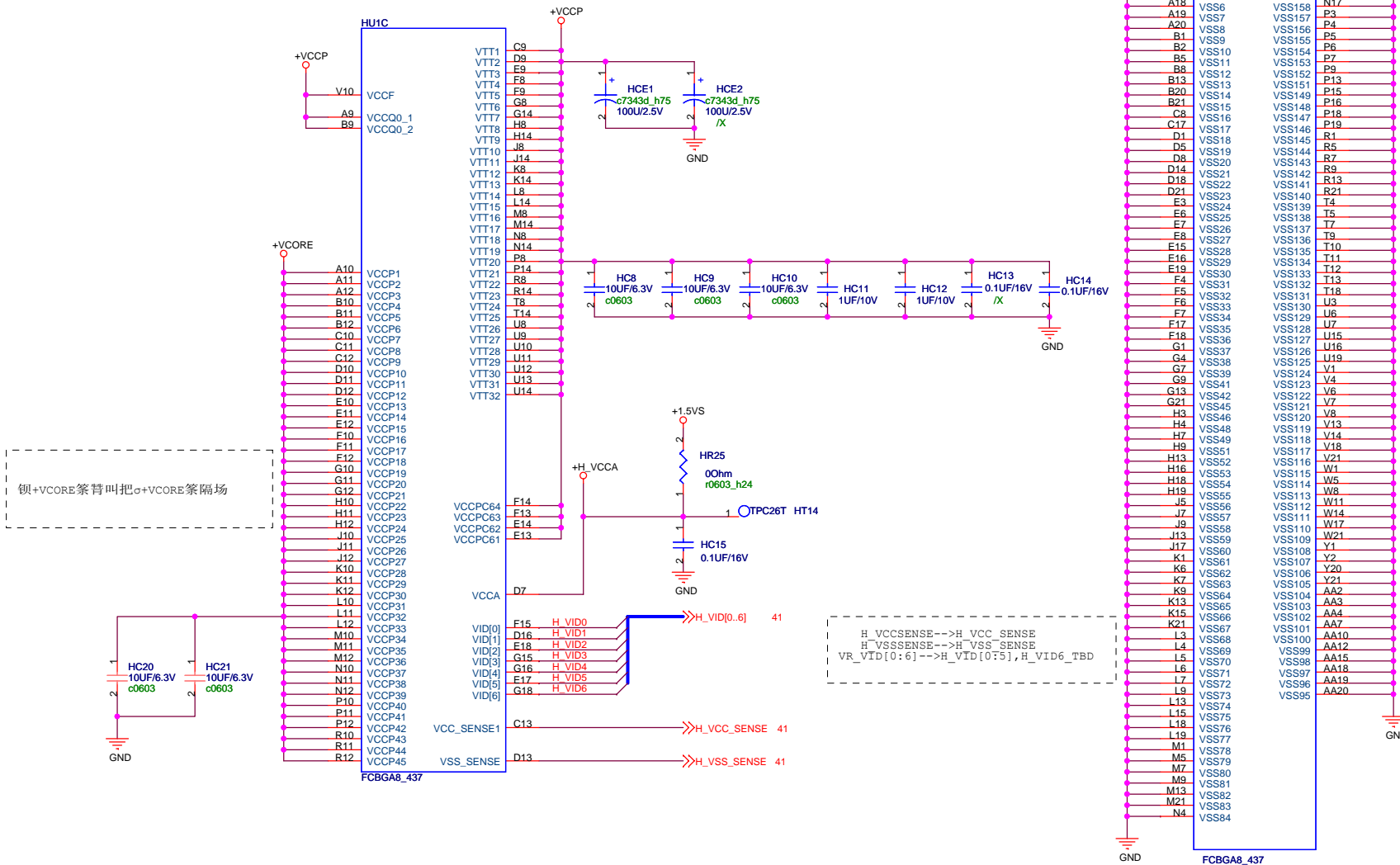


Place within 0.5'' to processor pin

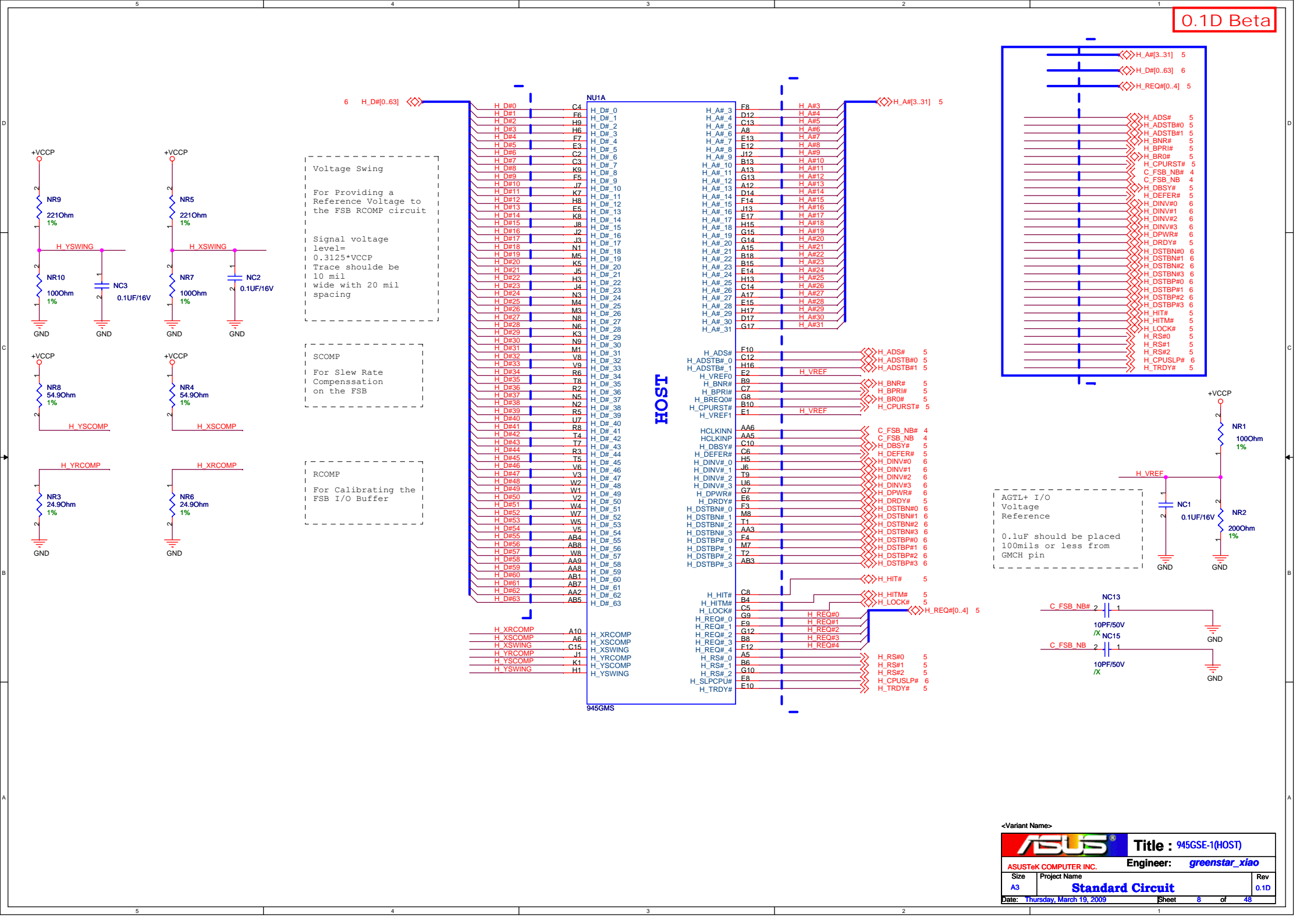


BSEL0	BSEL1	BSEL2	FSB
0	X	X	400
1	X	X	533

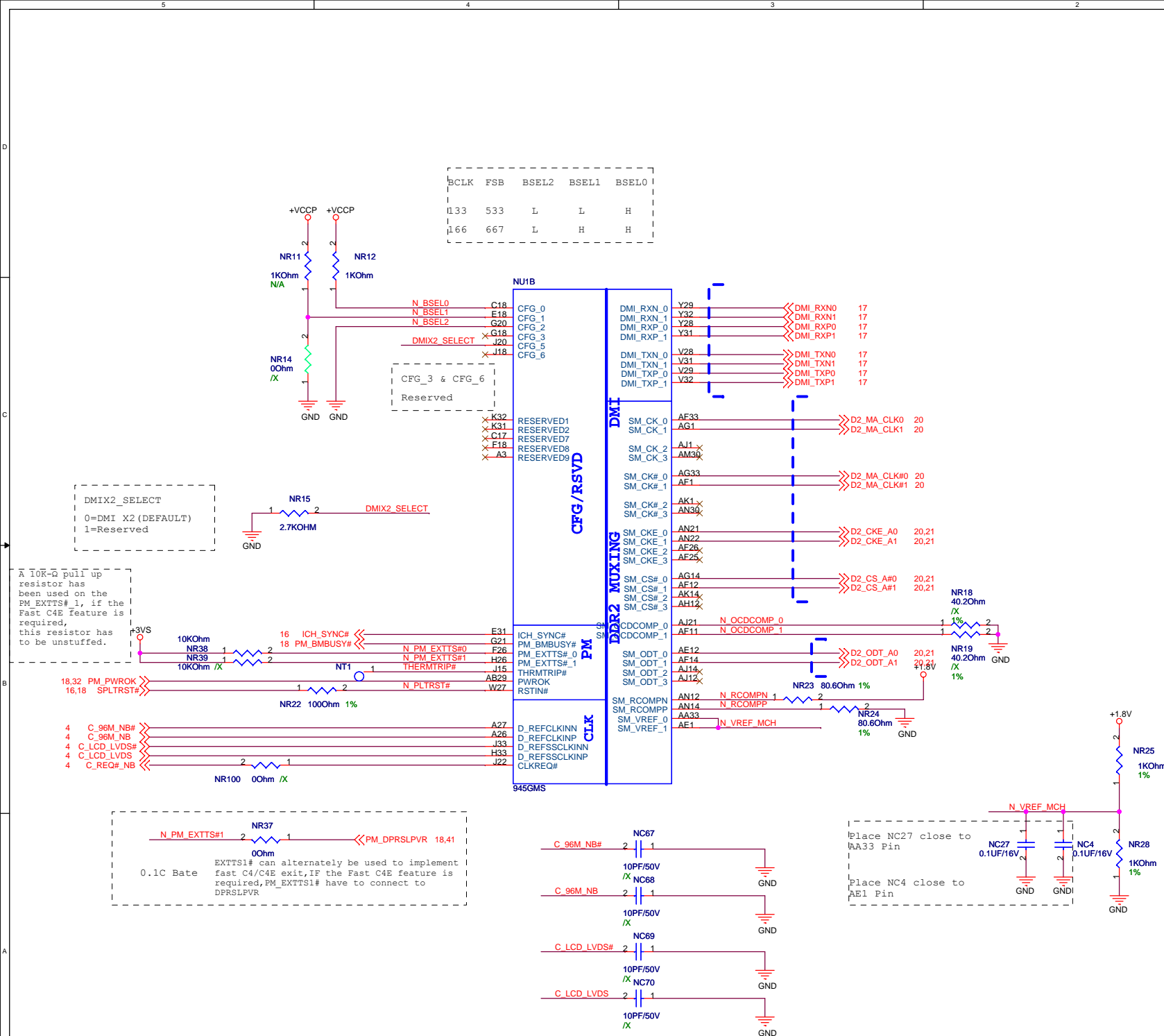
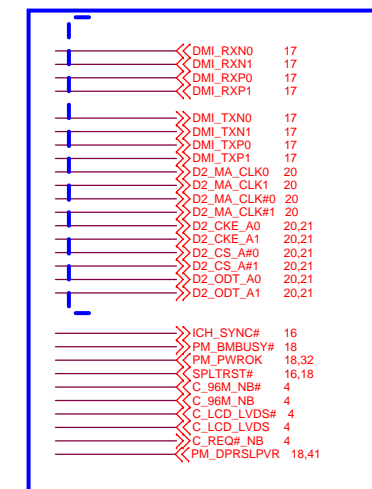


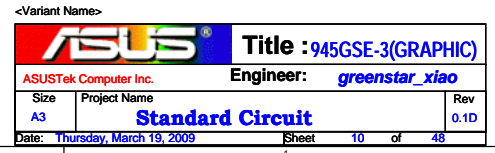
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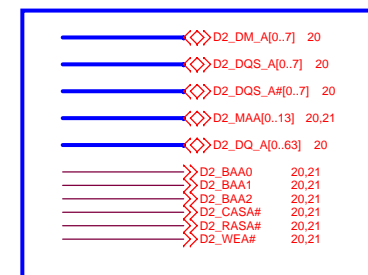
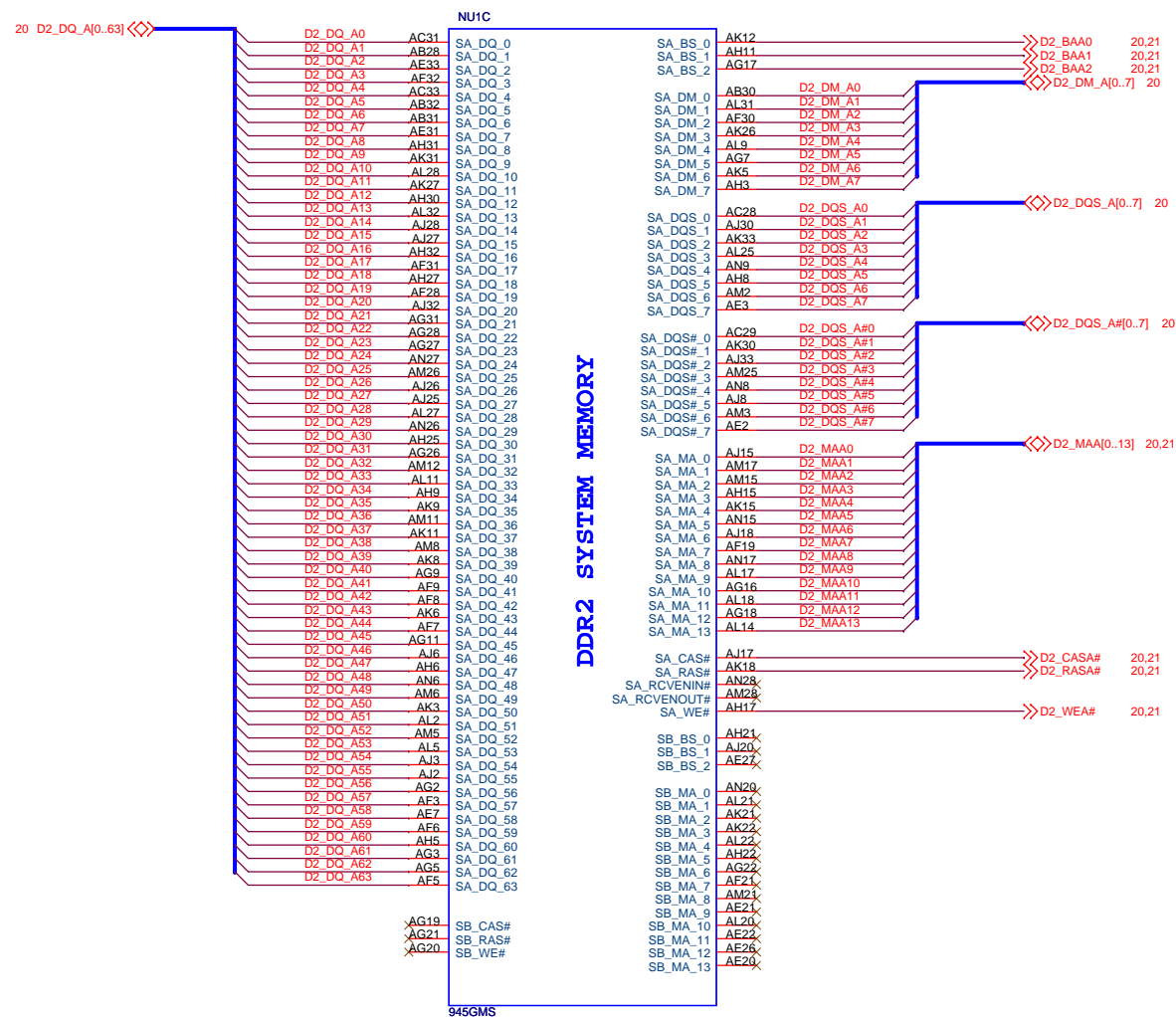
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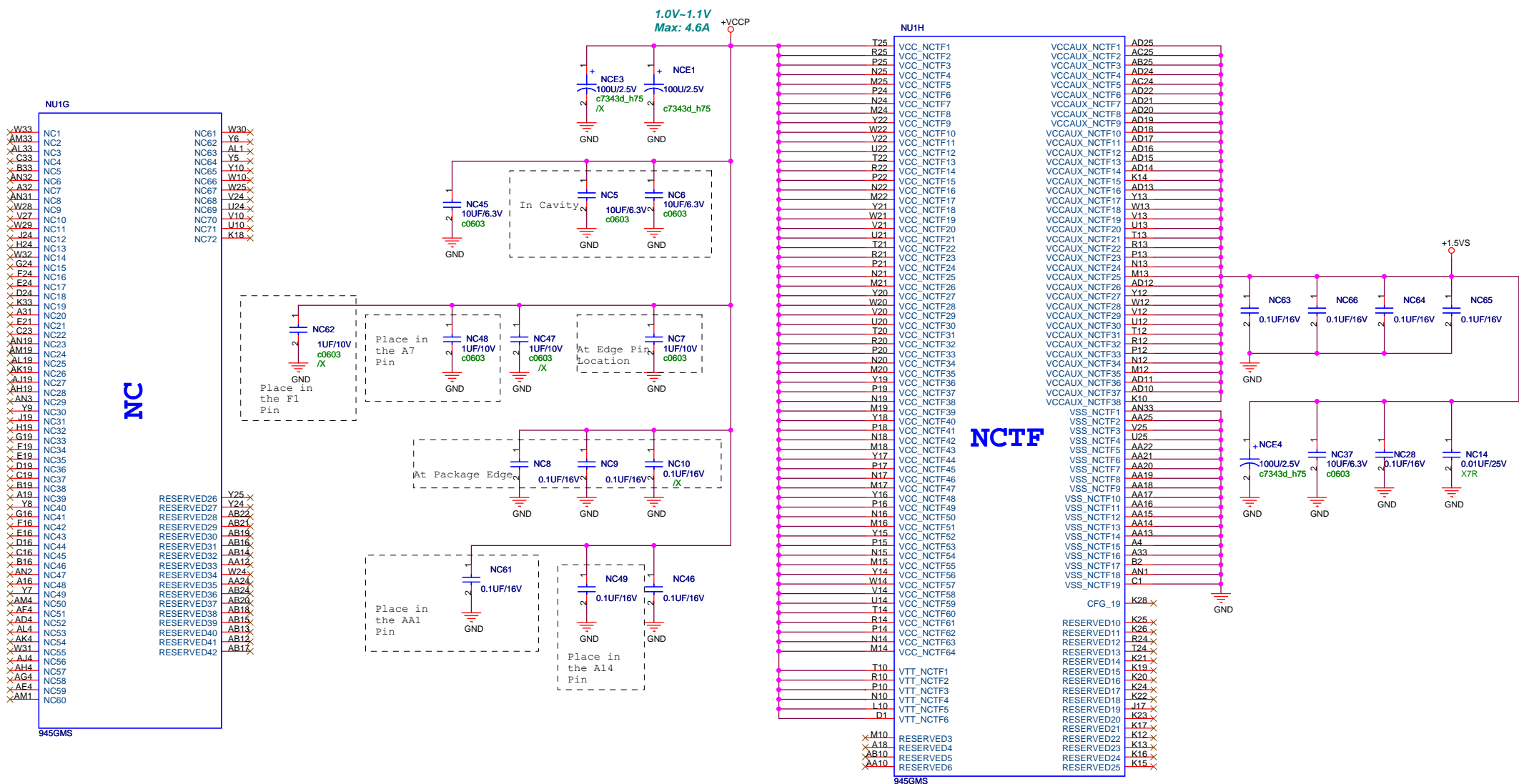










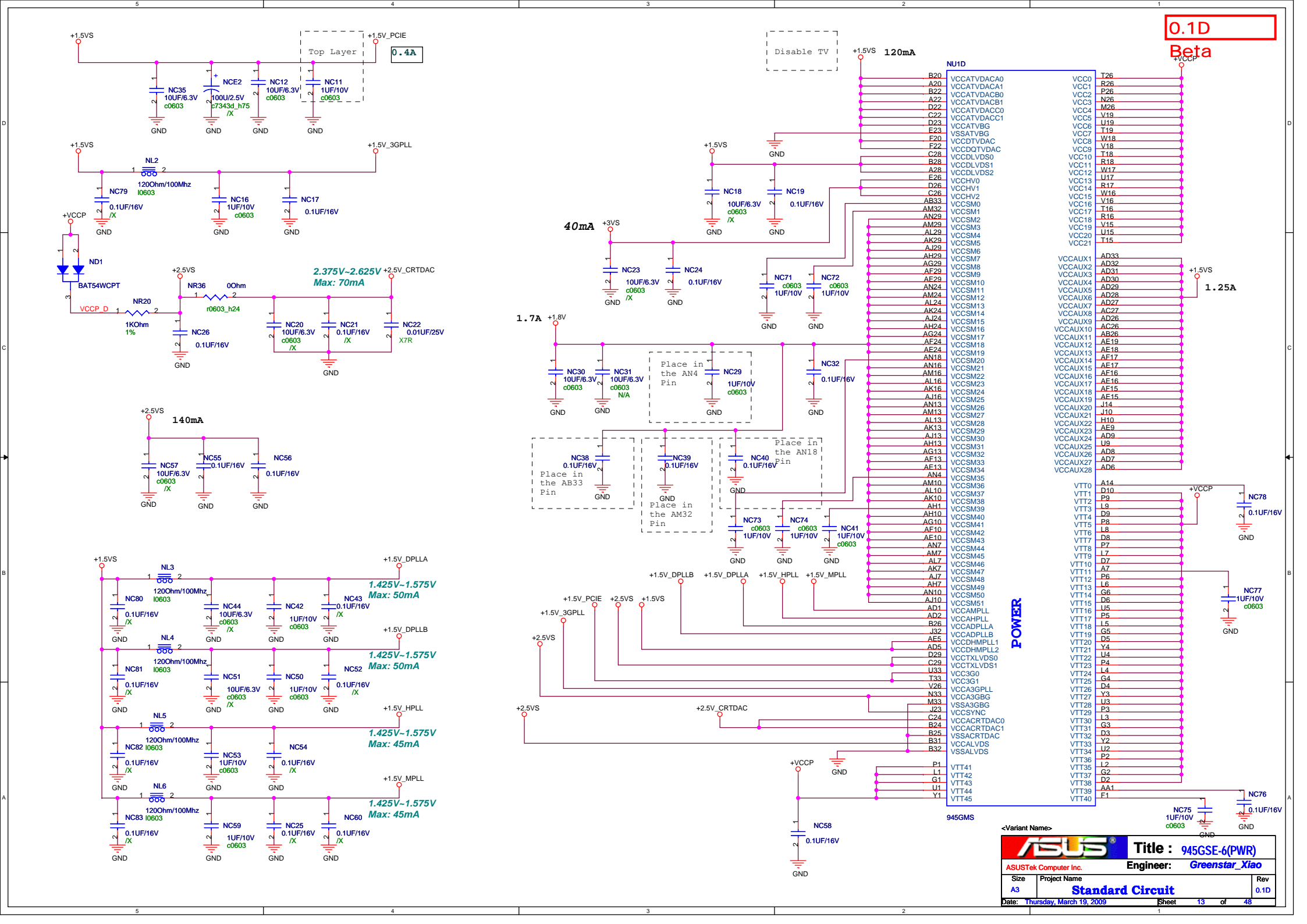


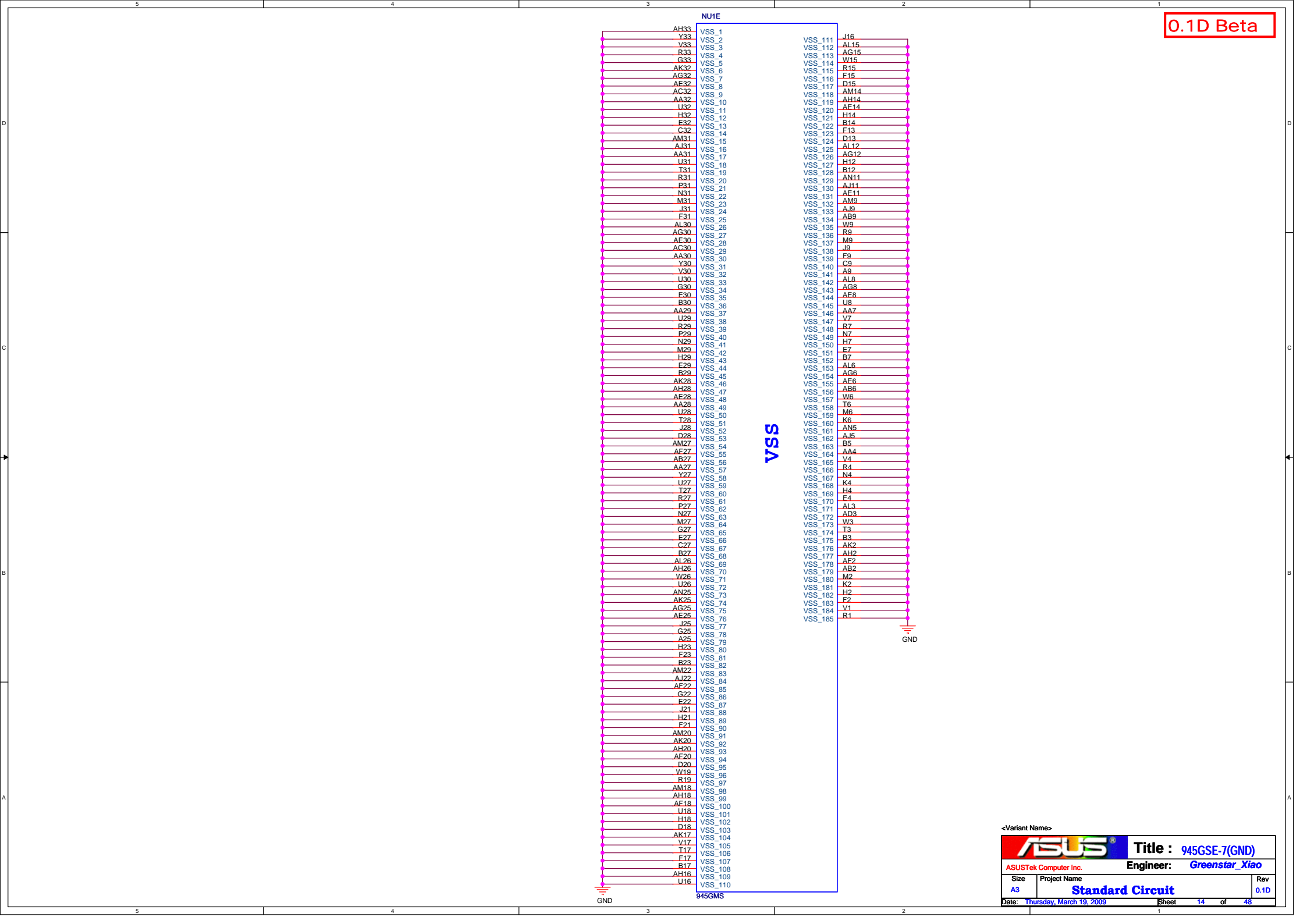
**<Variant Name>**



ASUSTek Computer Inc. Engineer: greenstar\_xiao


Size <b>A3</b>	Project Name <b>Standard Circuit</b>	Rev <b>0.1D</b>
Date: <b>Thursday, March 19, 2009</b>		Sheet <b>12</b> of <b>48</b>





0.1D Beta

<Variant Name>

**ASUSTek Computer Inc.**

**Title :** 945GSE-7(GND)

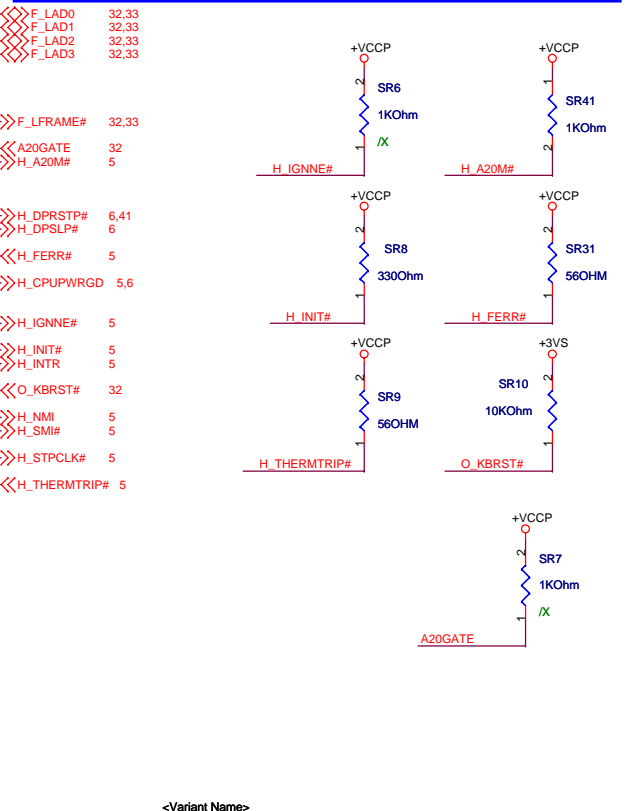
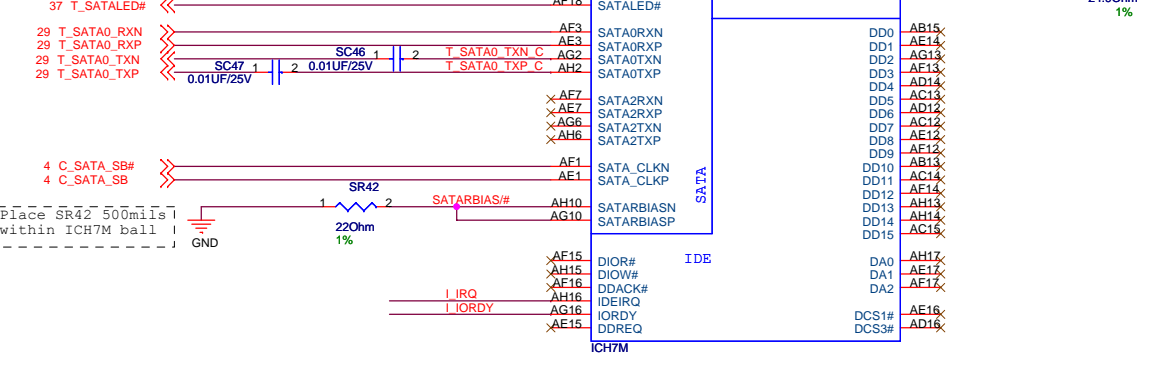
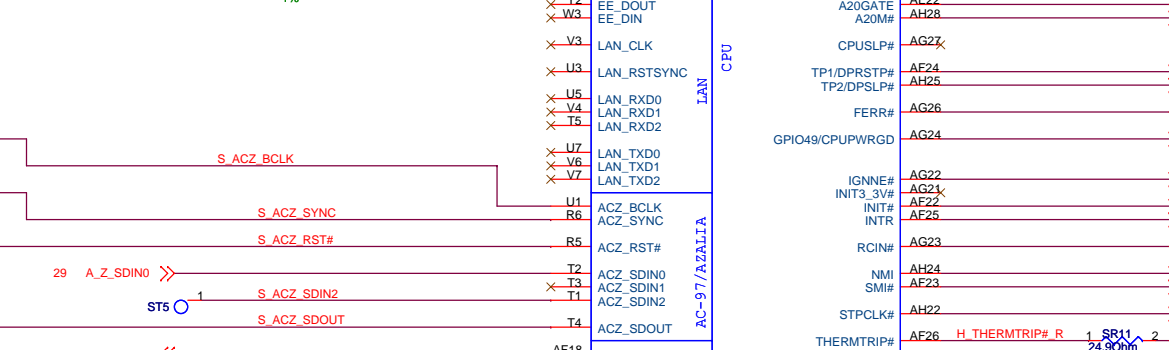
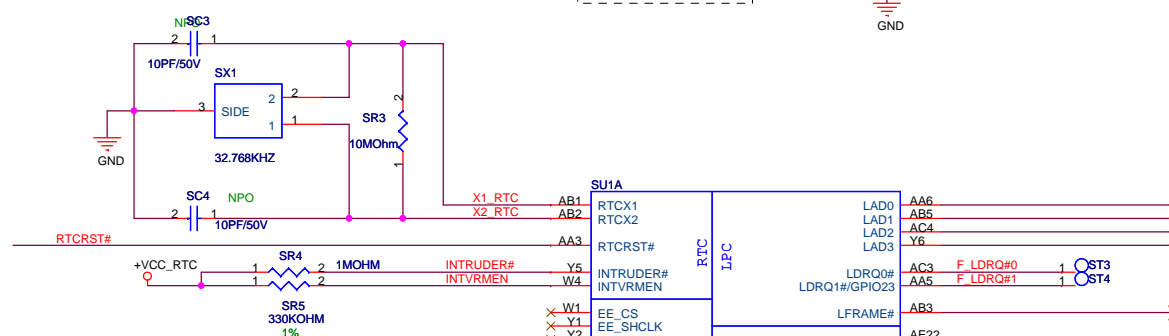
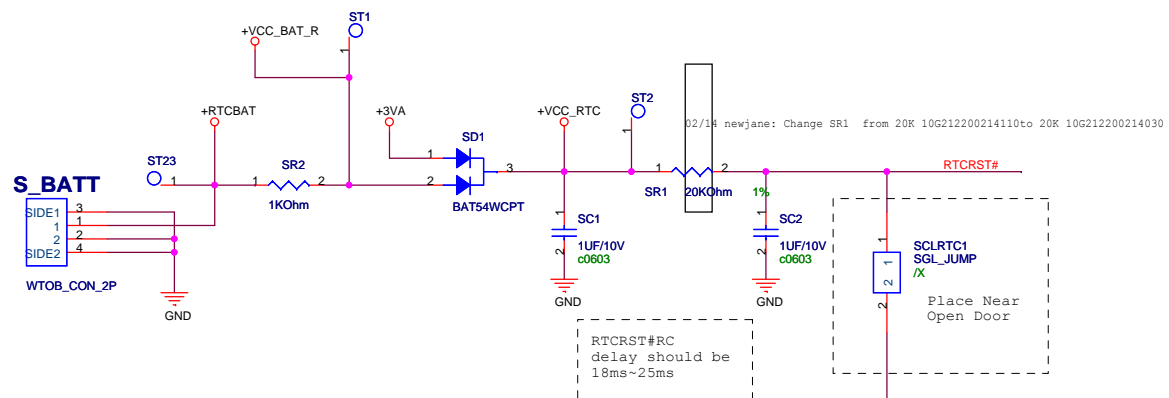
Size  
A3

Project Name  
**Standard Circuit**

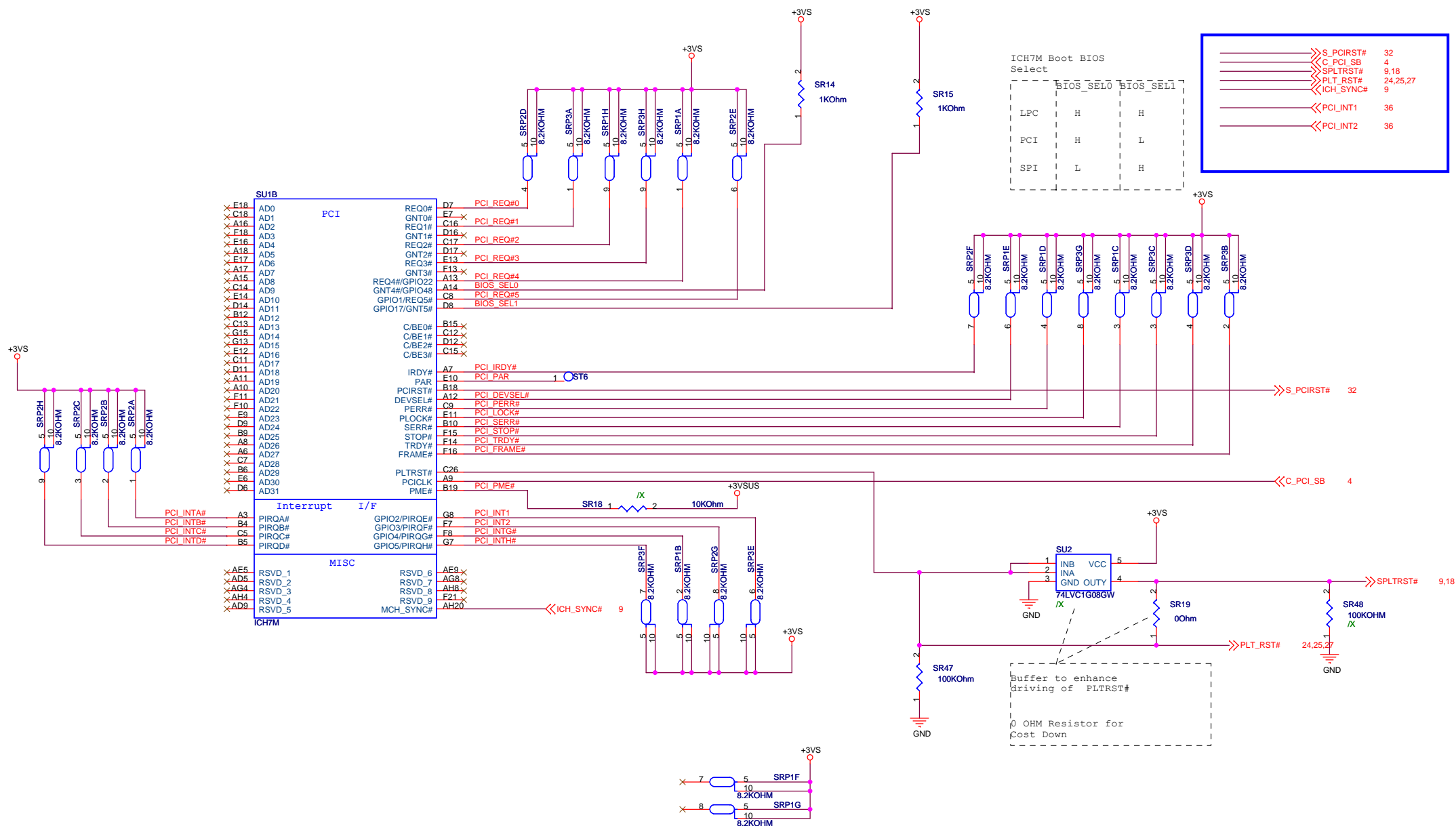
Rev  
0.1D

Date: Thursday, March 19, 2009

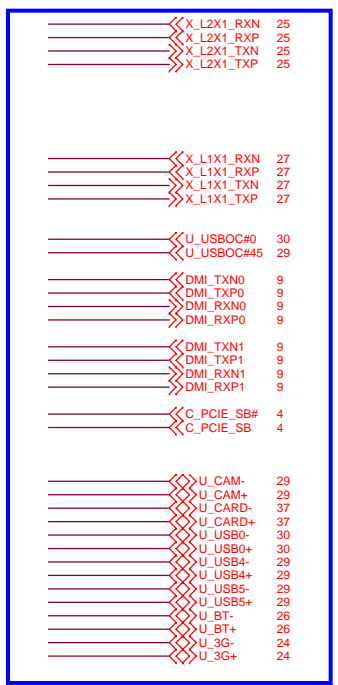
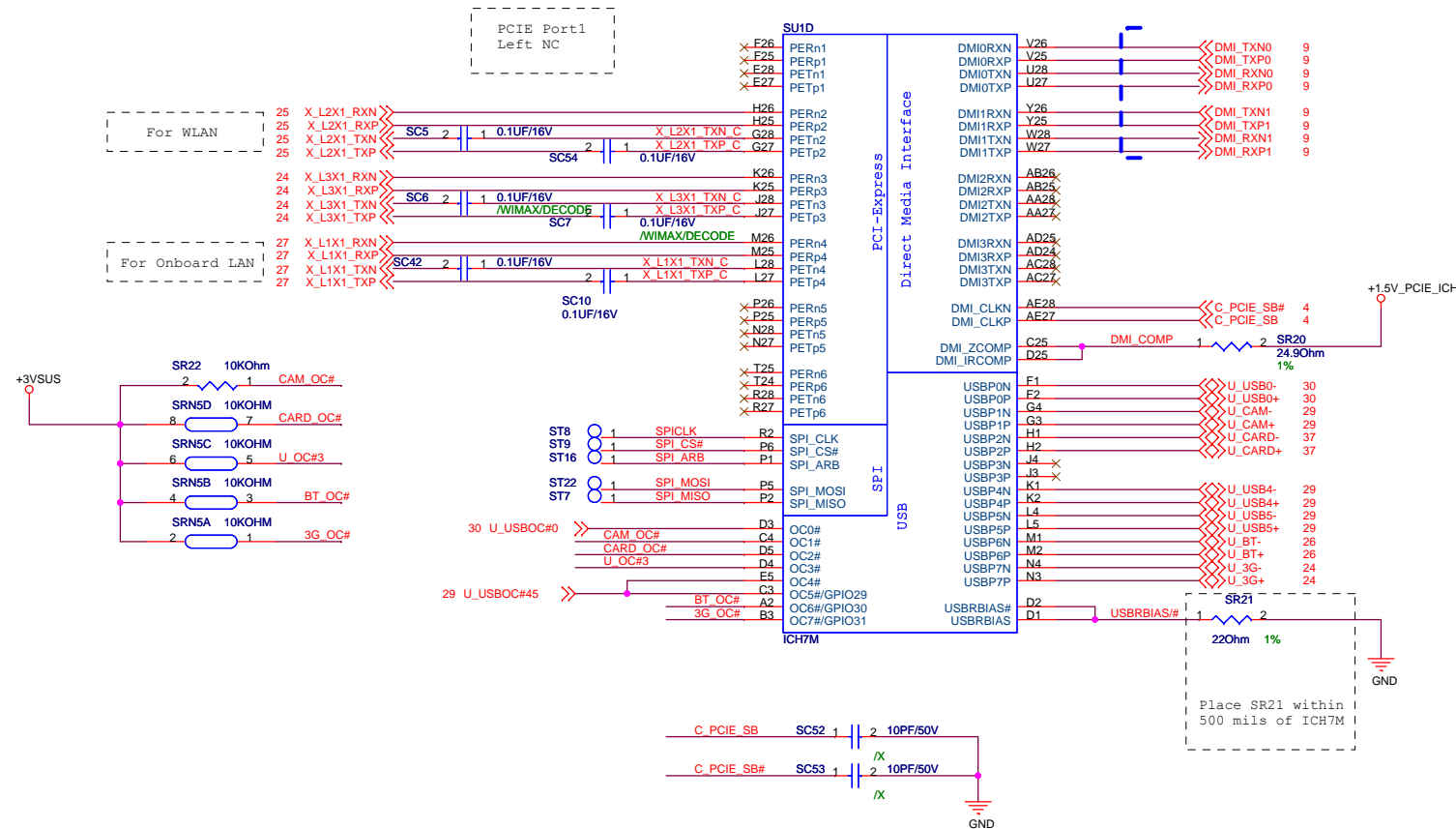
Sheet 14 of 48



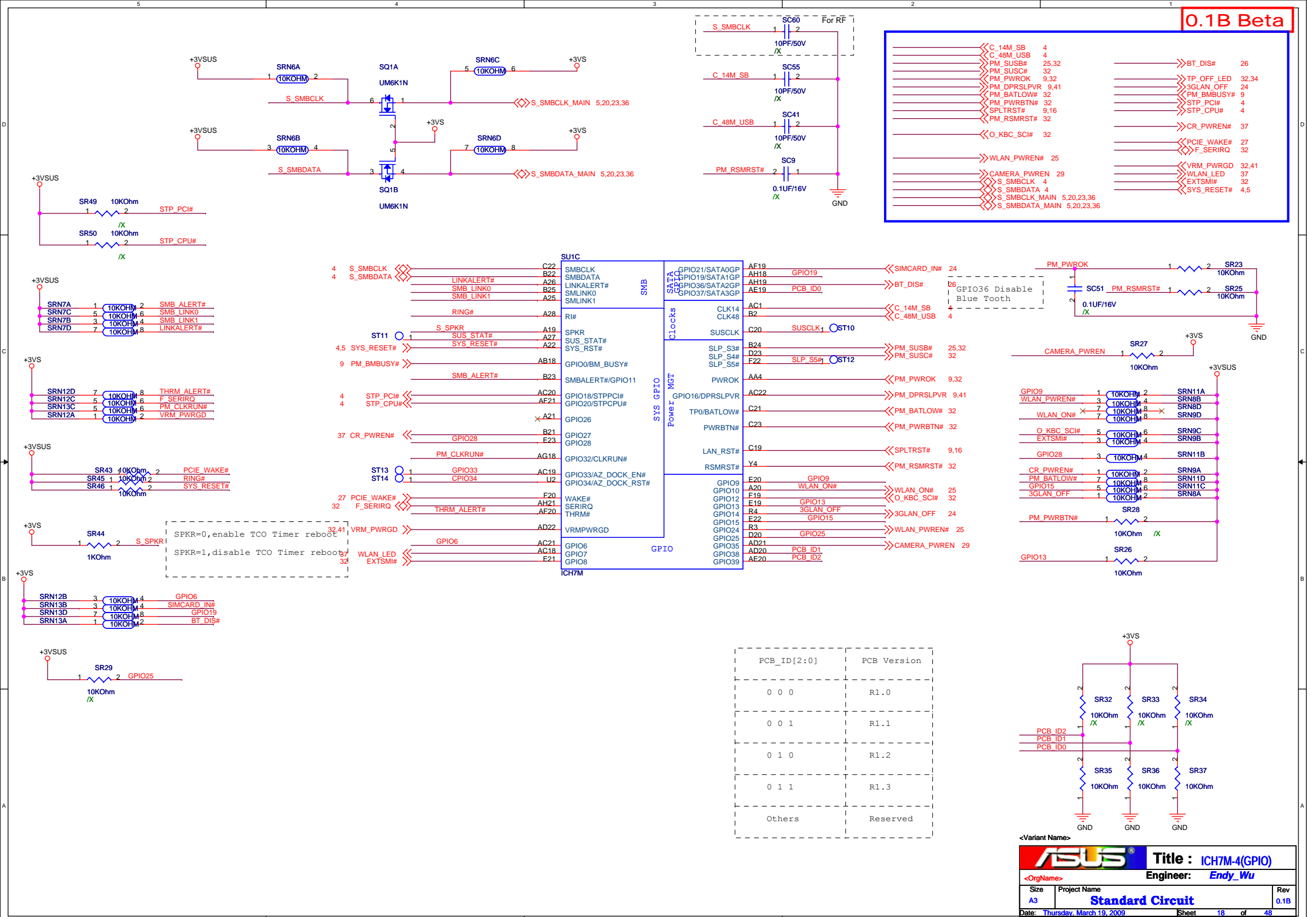
**<Variant Name>**



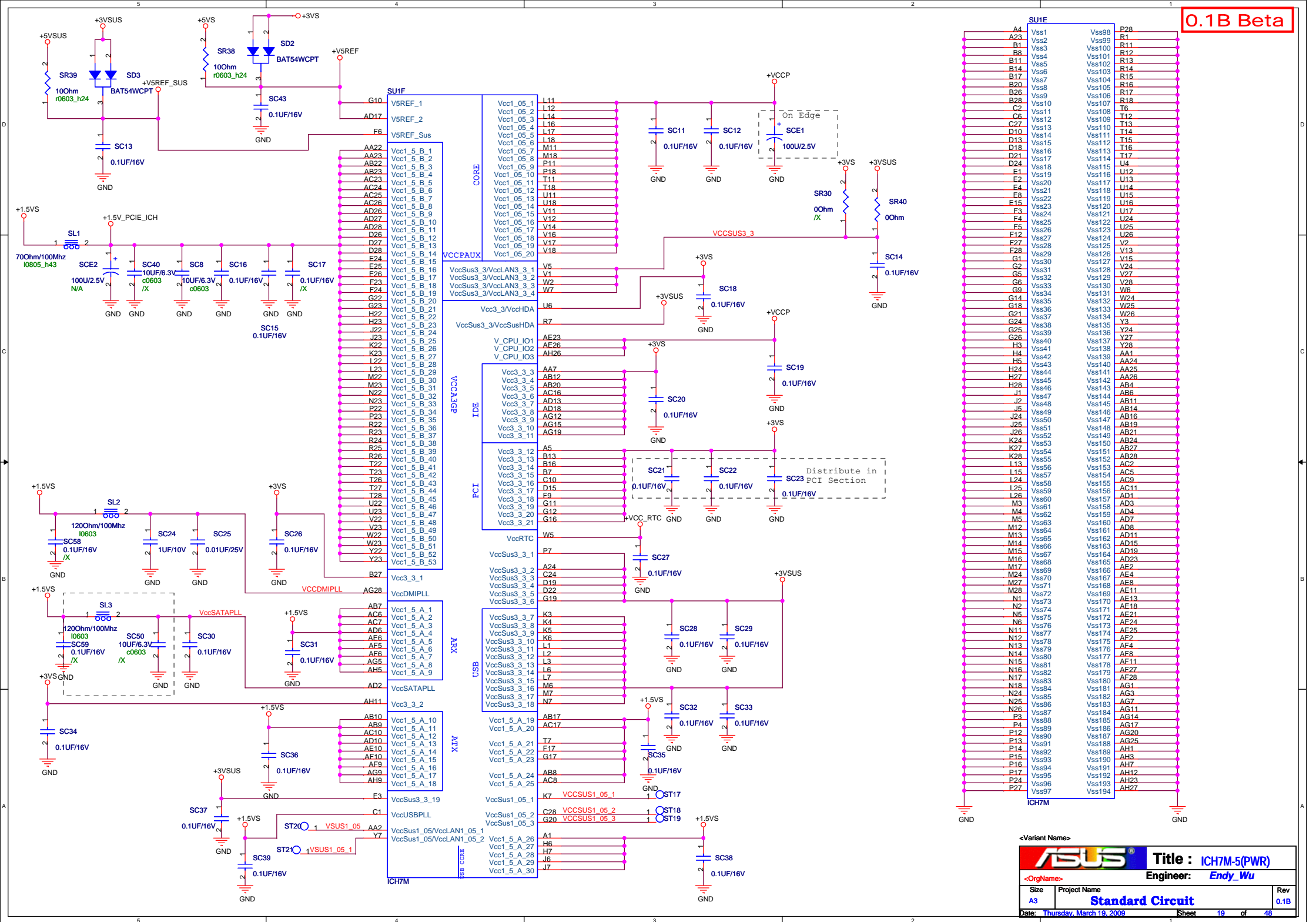


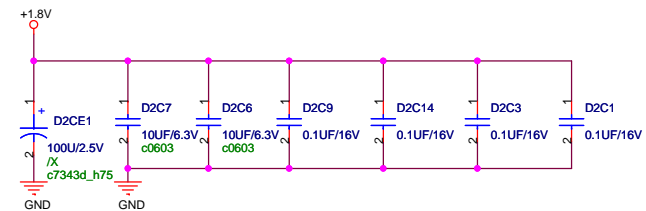
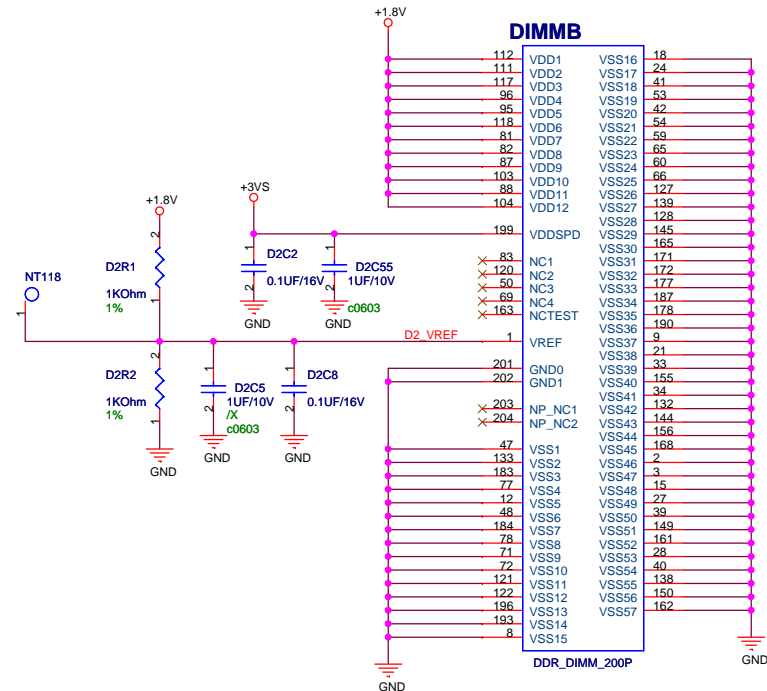
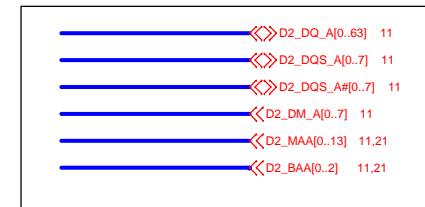
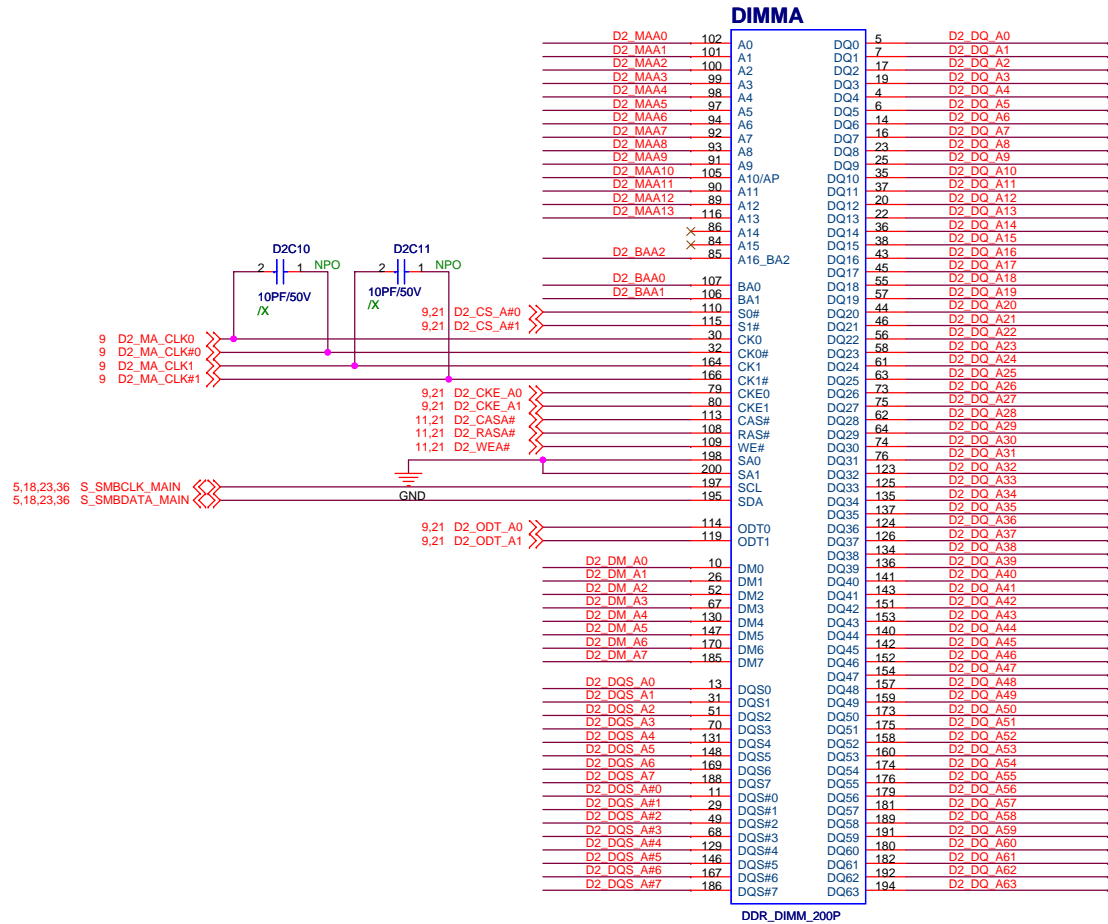


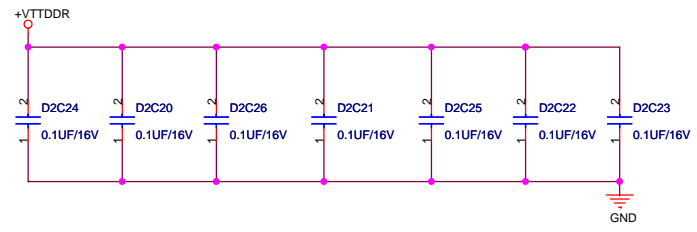
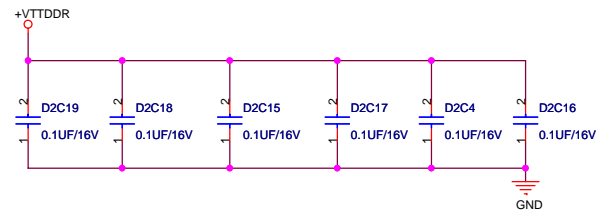
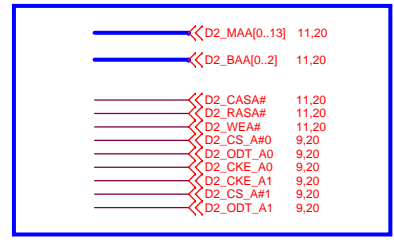
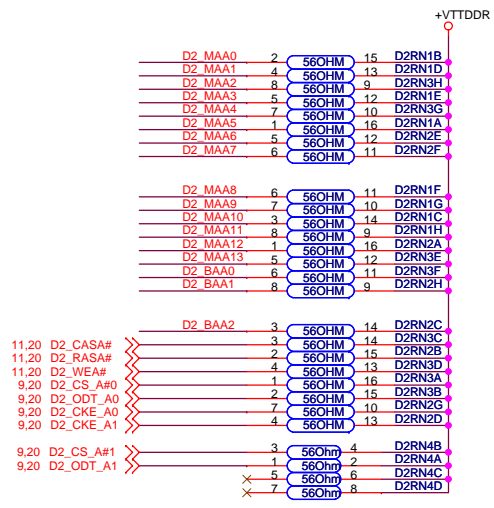
USB0	NC
USB1	Camera
USB2	Card Reader
USB3	USB CONN
USB4	USB CONN
USB5	USB CONN
USB6	Blue Tooth
USB7	3G Card

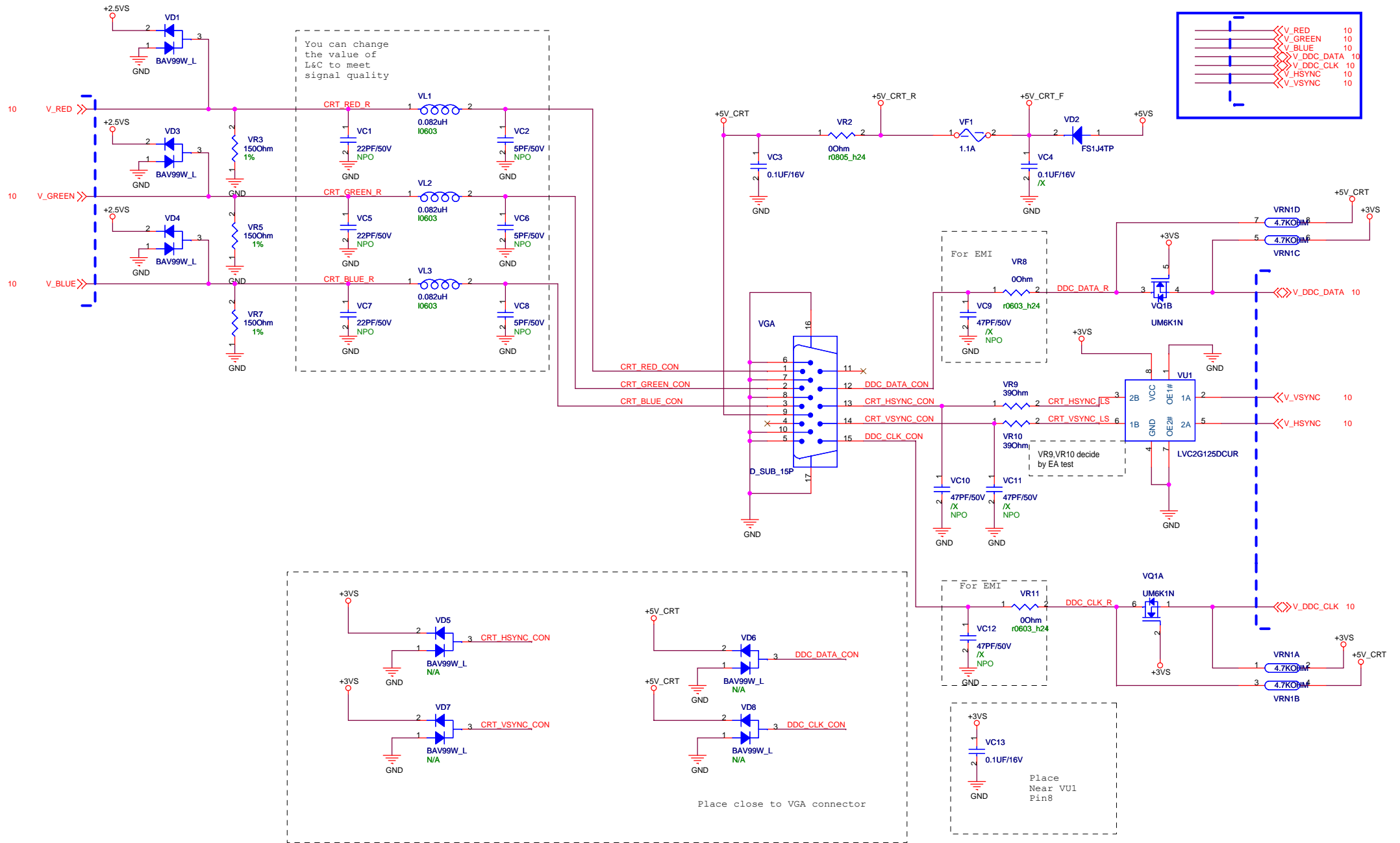


## 0.1B Beta

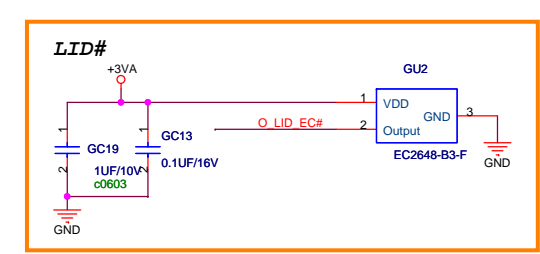
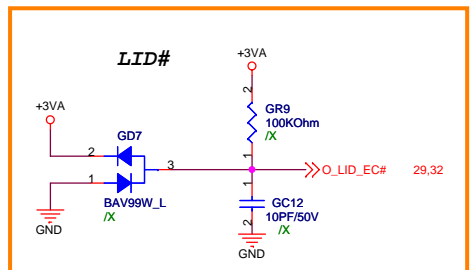
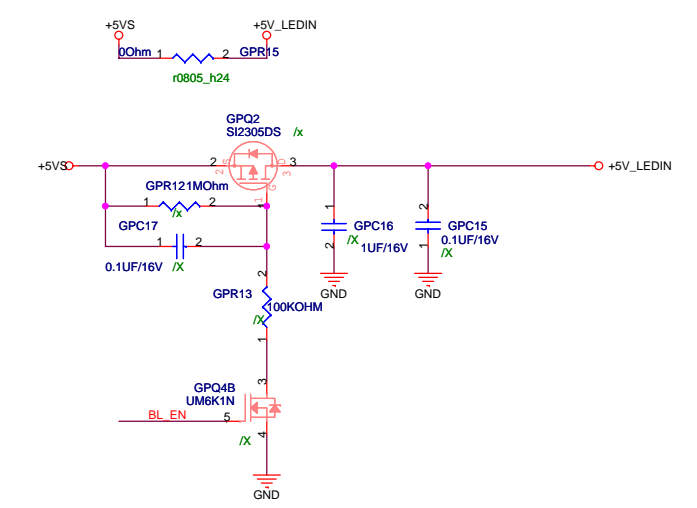
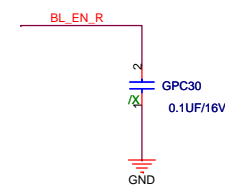
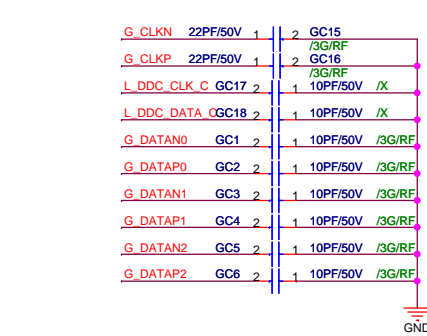
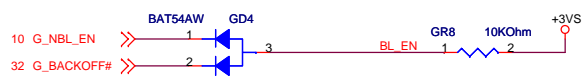
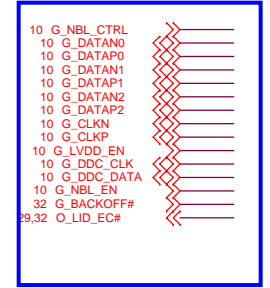
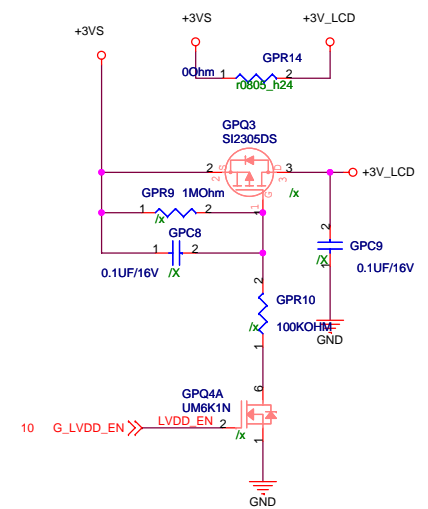
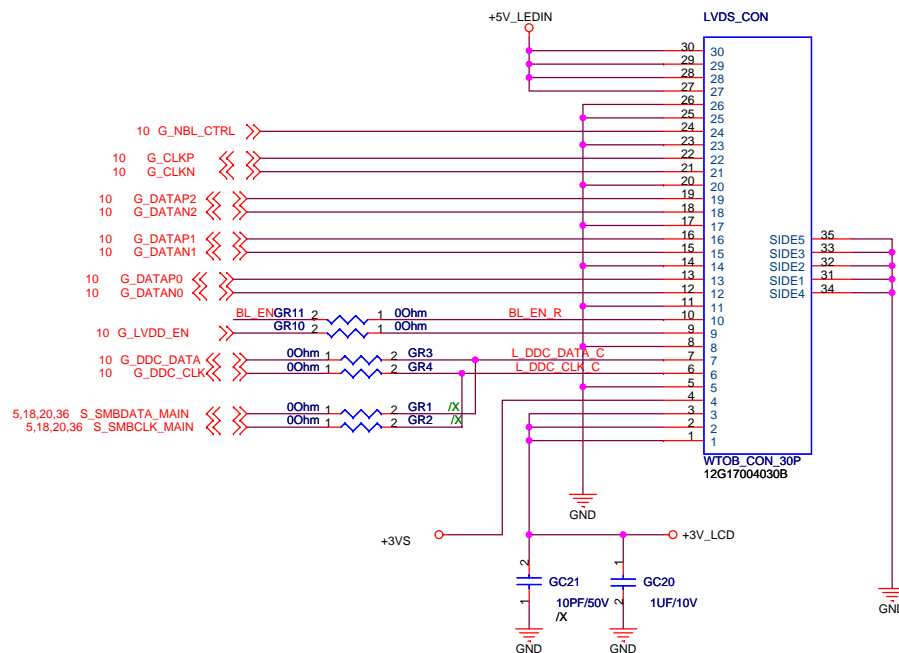




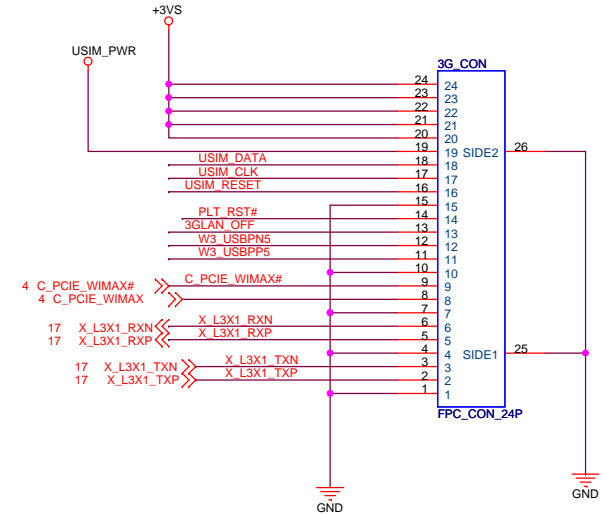
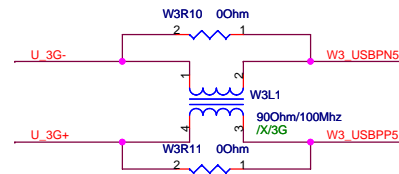
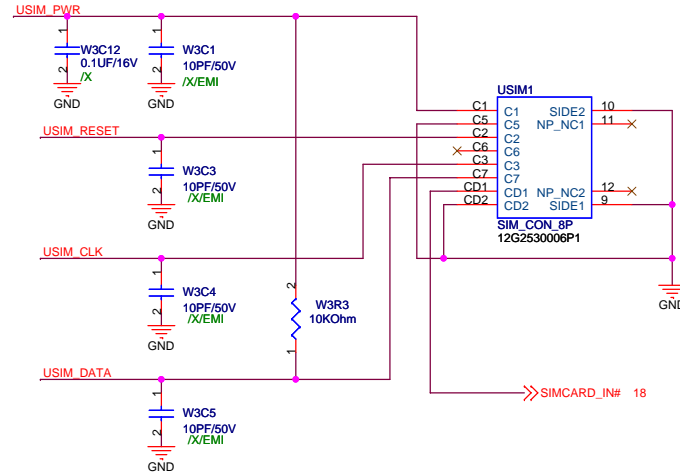




<Variant Name>

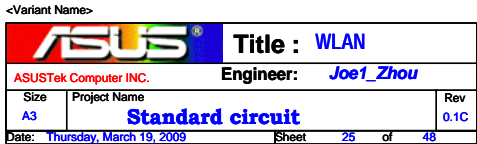


CAP Near SIM Socket



<Variant Name>



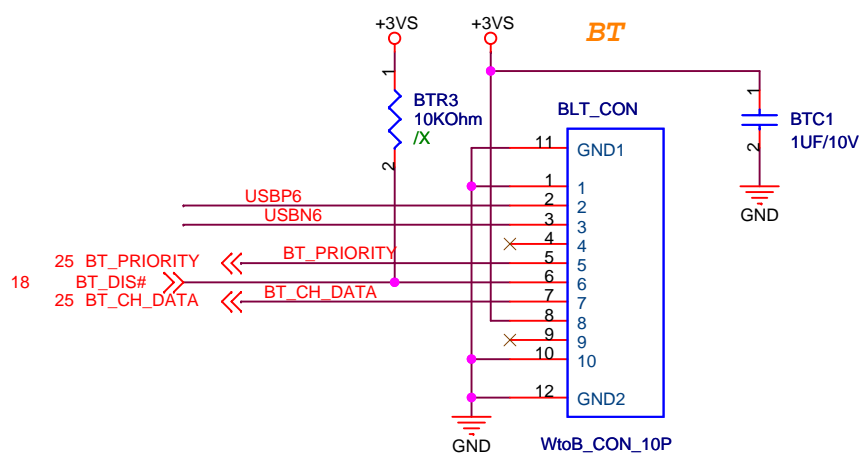
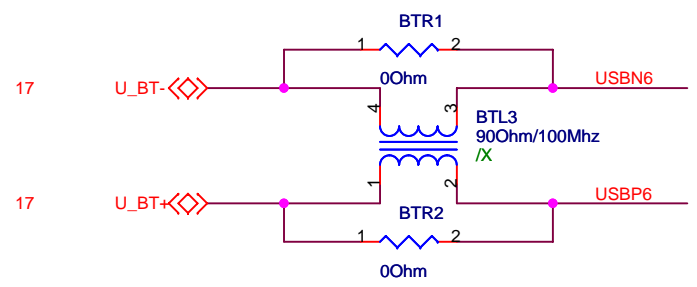


D


C

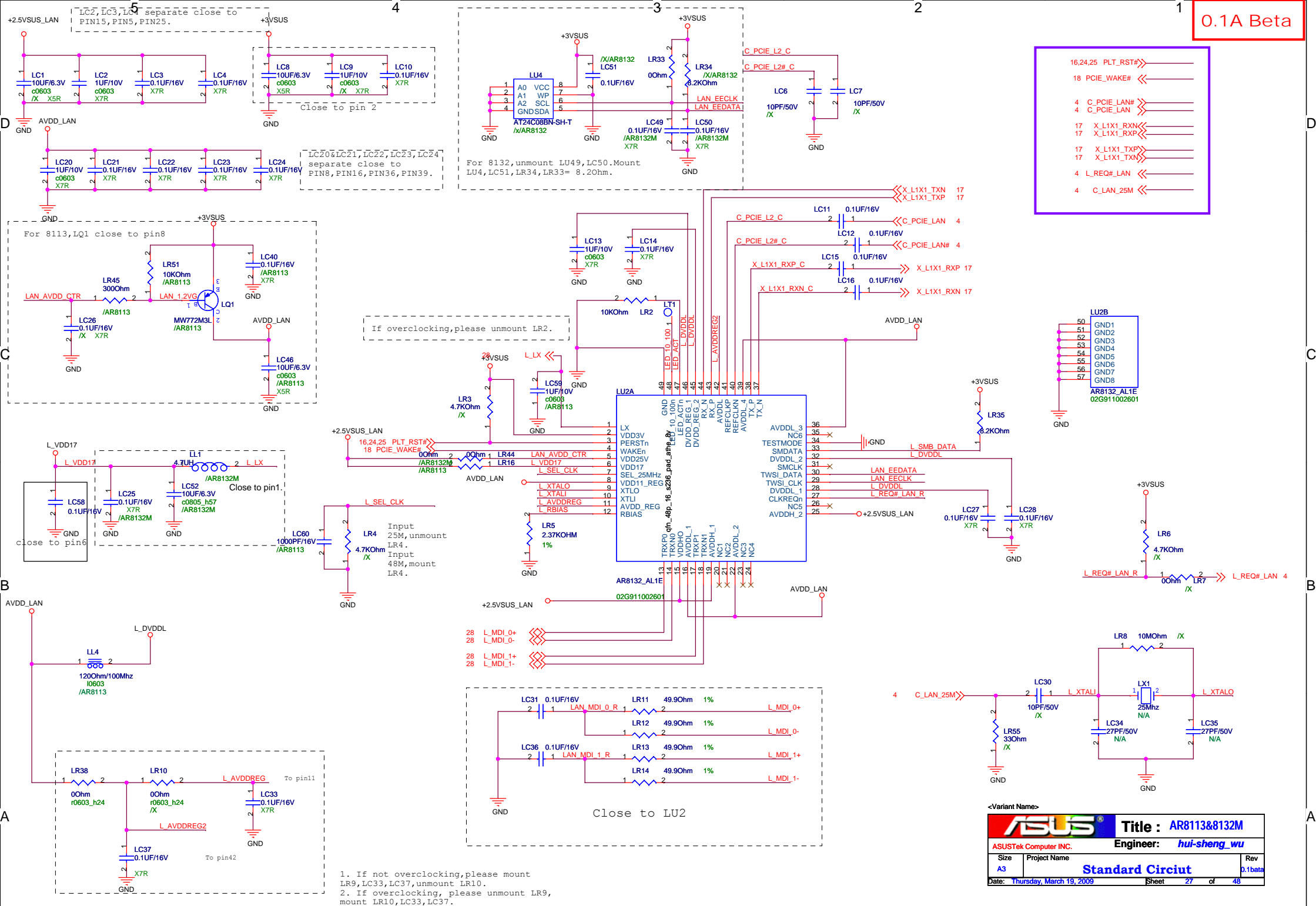
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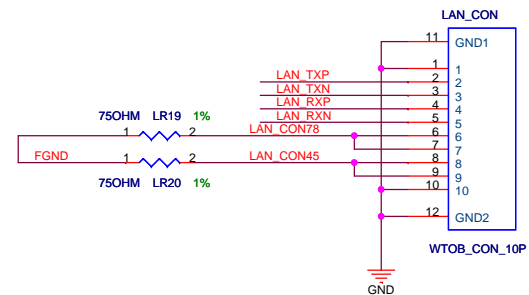
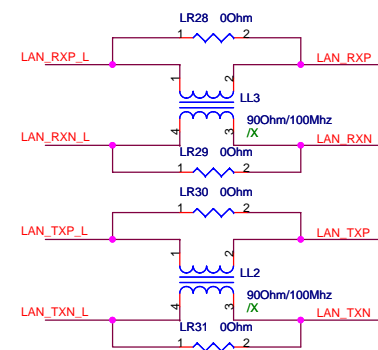
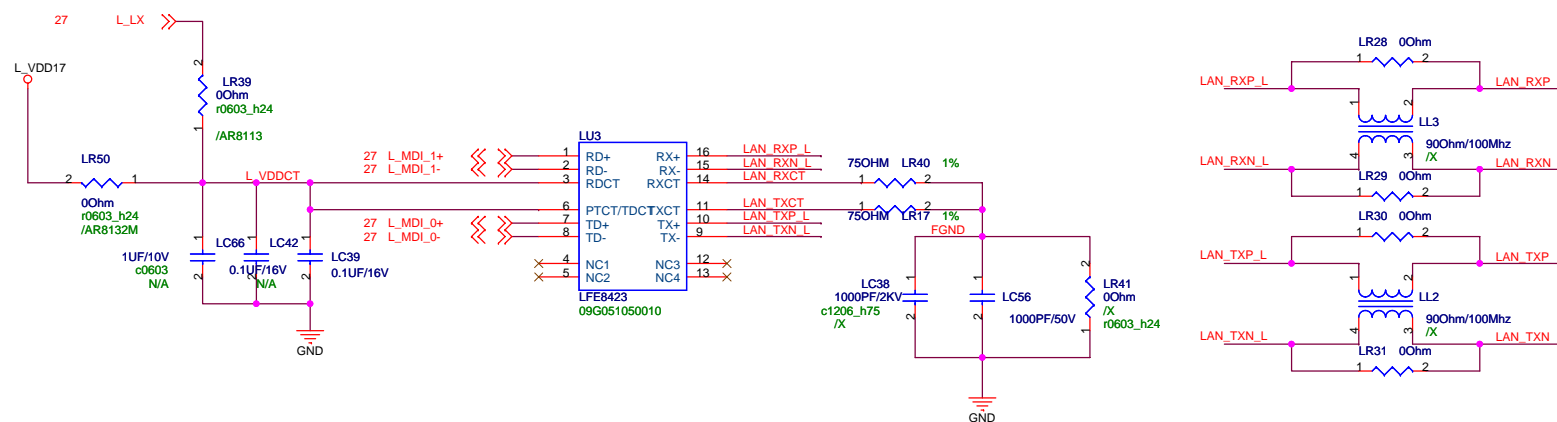
A

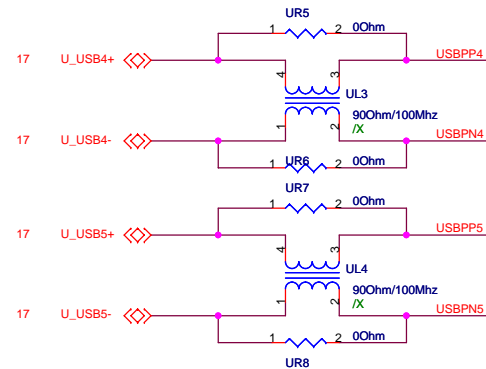
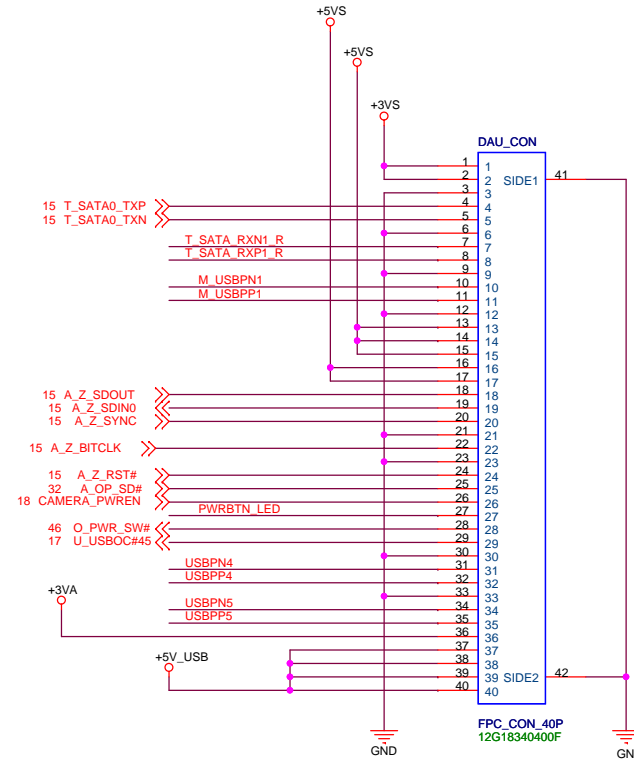
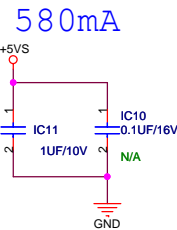
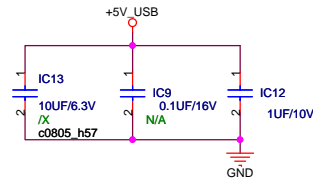
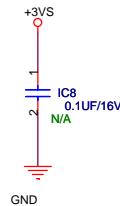
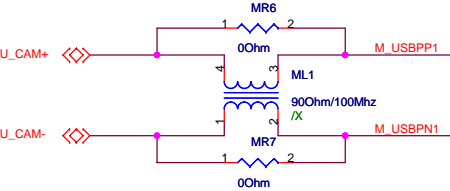
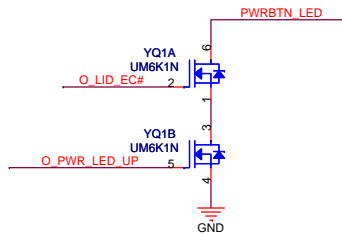
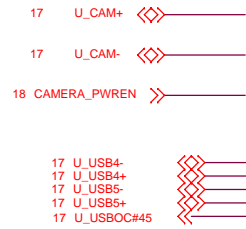


<Variant Name>

		<b>Title :</b> BLUETOOTH	
ASUSTek Computer INC.		<b>Engineer:</b> JOE1_ZHOU	
Size A4	Project Name <b>Standard Circiut</b>		Rev 0.1A
Date: Thursday, March 19, 2009		Sheet	26 of 48

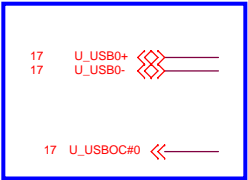
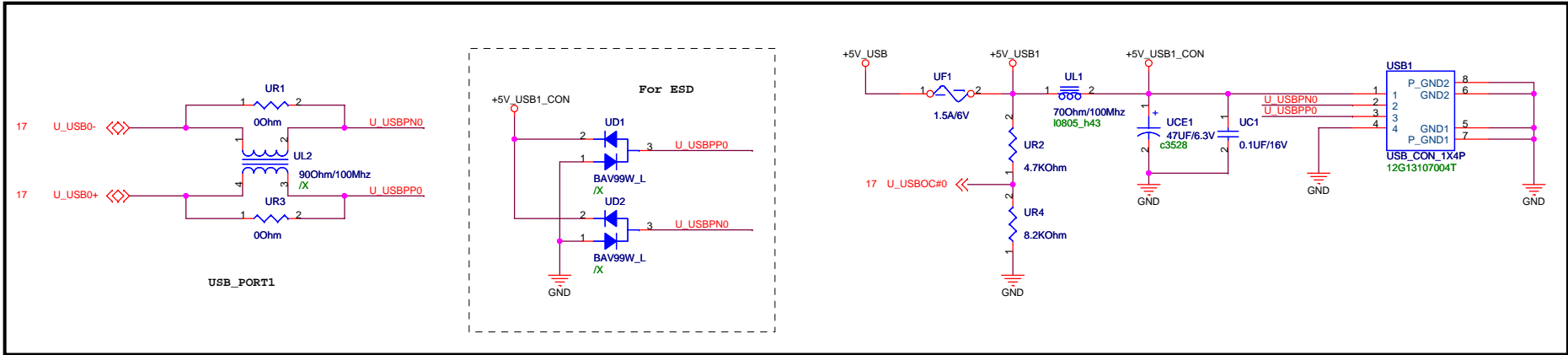







<Variant Name>

<b>ASUS</b>		<b>Title : SATA HDD</b>	
ASUSTek Computer INC.		Engineer: KingCa_Jin	
Size A3	Project Name <b>1000HN</b>		Rev 1.0
Date: Thursday, March 19, 2009		Sheet	29 of 48





<Variant Name>



**Title :** Camera CONN

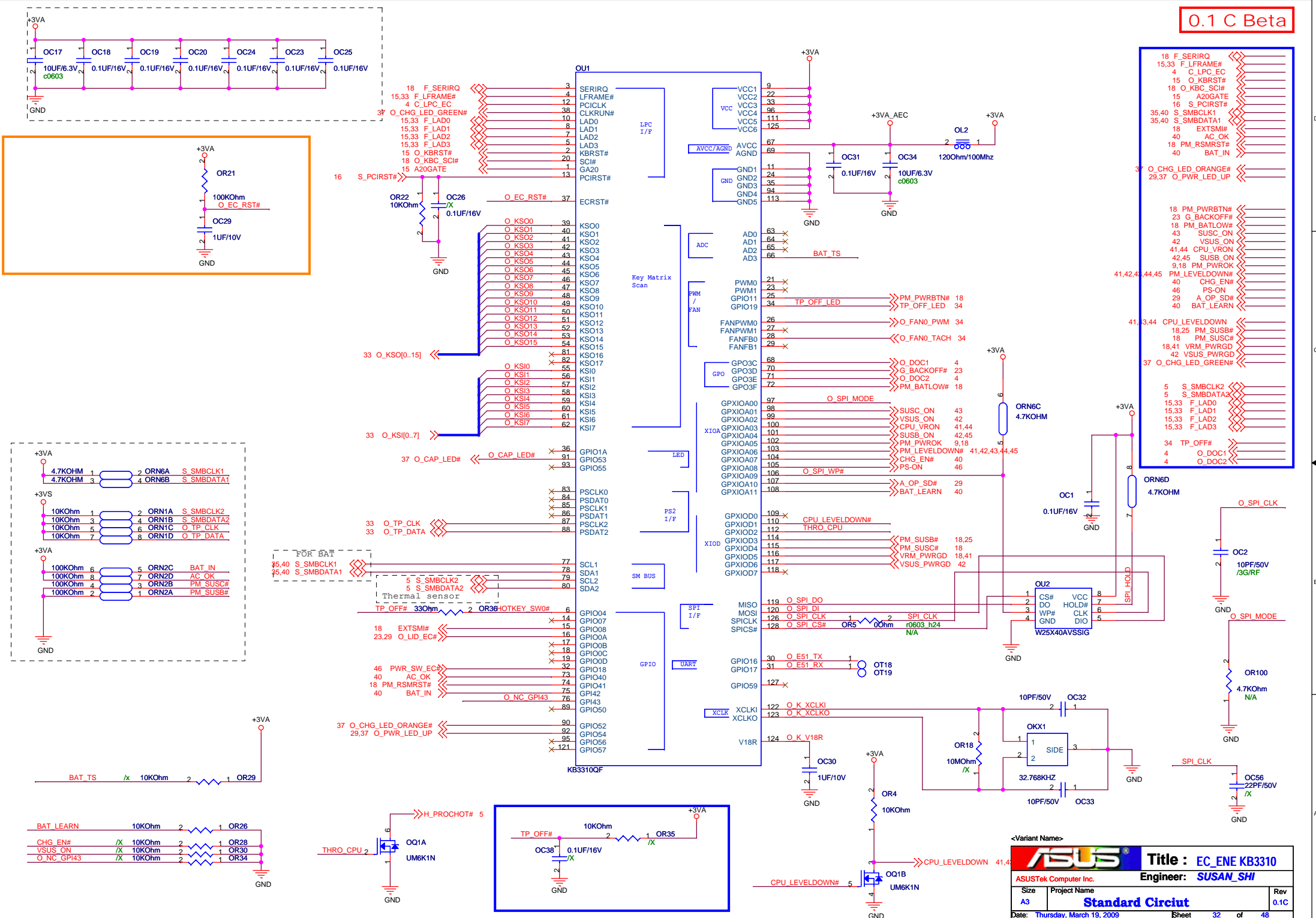
ASUSTEK COMPUTER INC

**Engineer:** KEN\_JIN

Size	Project Name	Rev
A3	<b>Standard Circiut</b>	0.1A

Date: Thursday, March 19, 2009

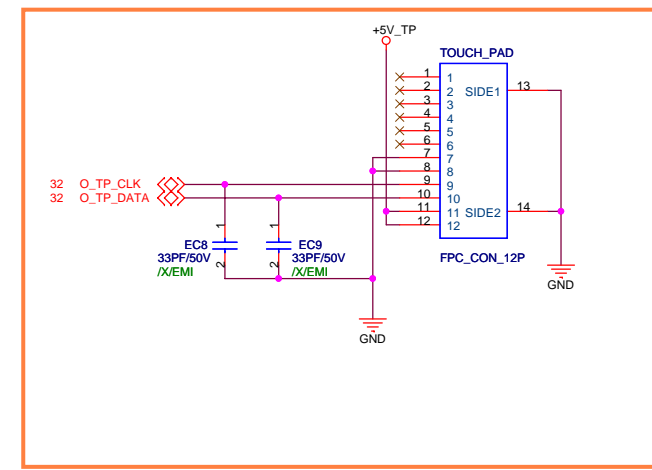
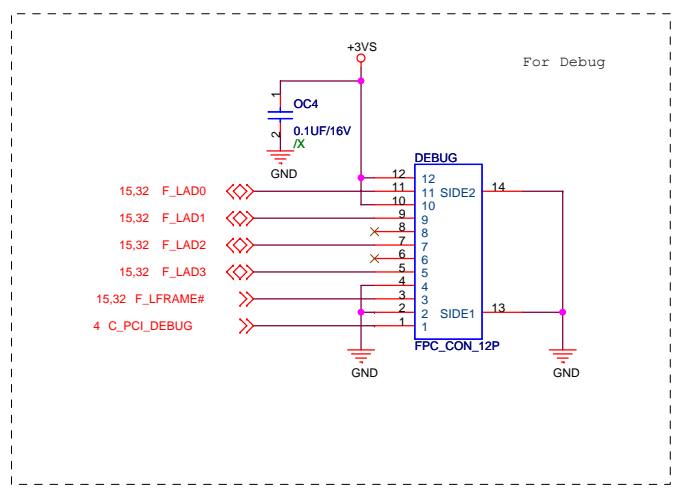
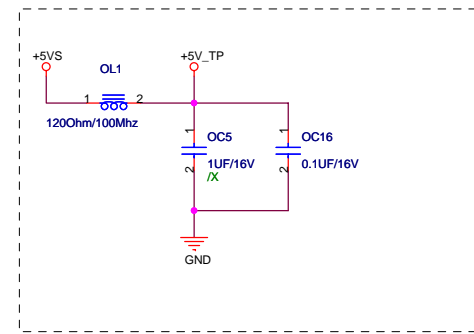
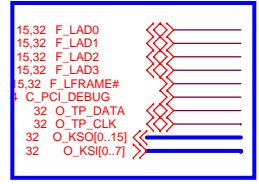
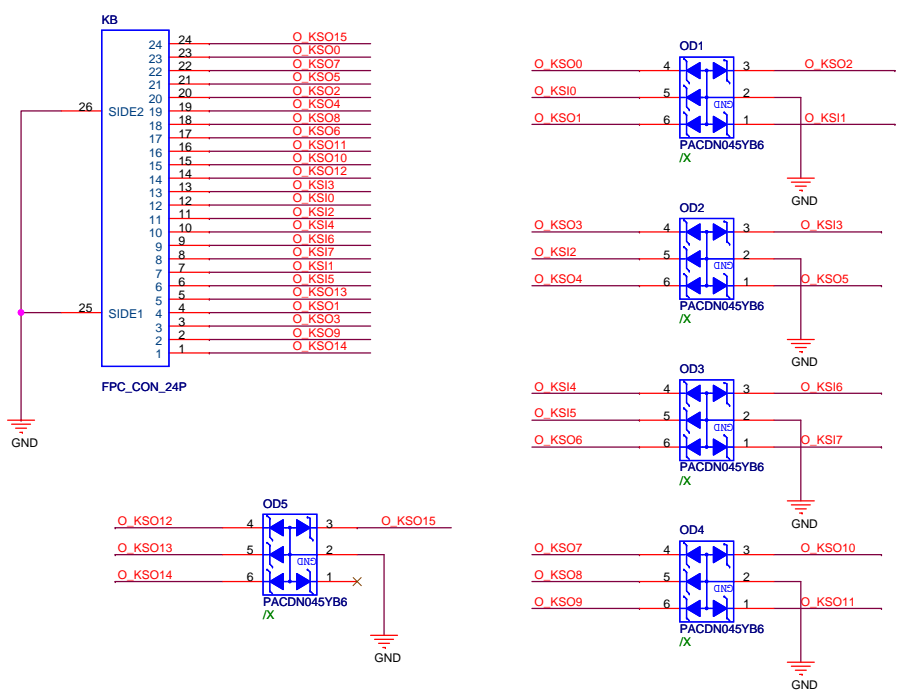
Sheet 31 of 48

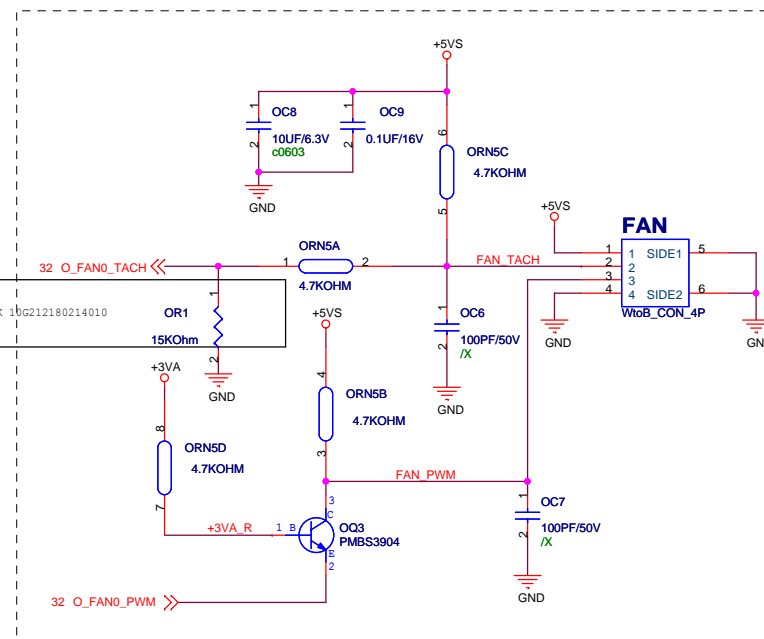
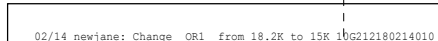




>>O\_KSO[0..15] 32  
<<O\_KSI[0..7] 32

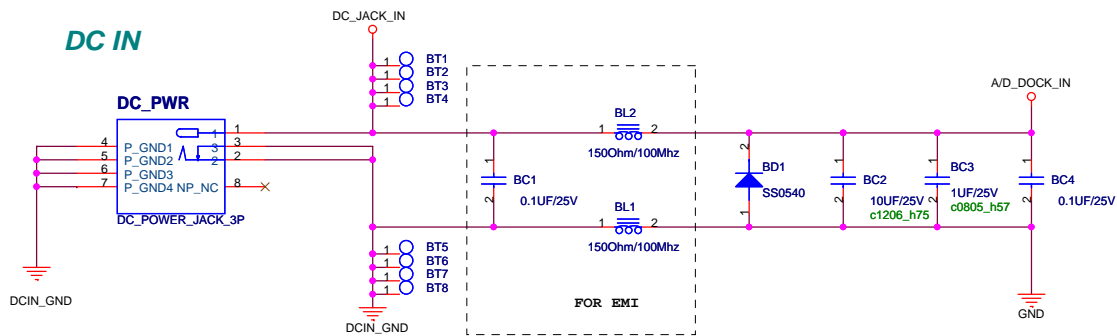
# For Keyboard Connector





The diagram illustrates the TP LED driver circuit. It features a +5VS supply connected to a resistor TPR1 (4.7KOhm) and a TP LED (BLUE). The TP LED is connected to a resistor TPR2 (10KOhm) and a TP LED G. The TP LED G is connected to a MOSFET TPG1A (UM6K1N) and a MOSFET TPG1B (UM6K1N). The MOSFETs are connected to a 32 TP\_OFF\_LED and a GND.

0.1B Beta

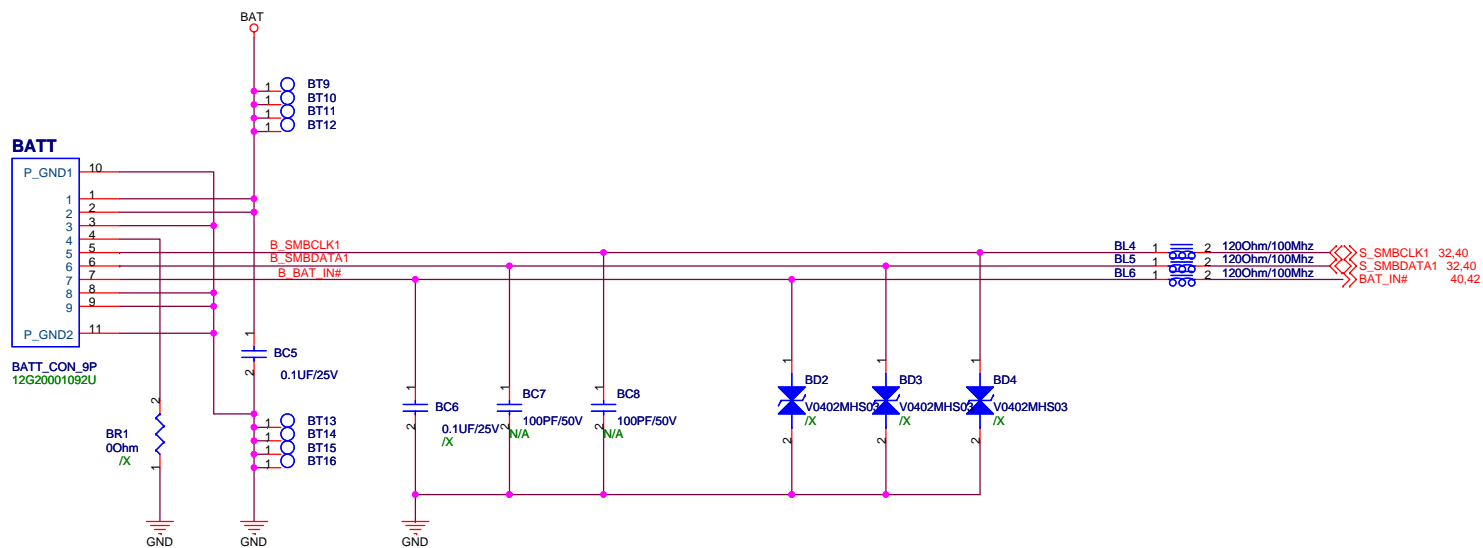


BAT\_IN# 40,42

S\_SMBCLK1 32,40

S\_SMBDATA1 32,40

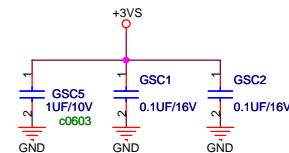
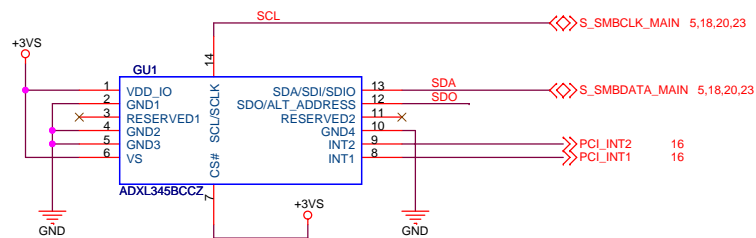
change from DIP to SMD



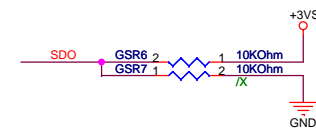
<Variant Name>

<b>ASUS</b>		Title : PWR Jack	
ASUSTEK COMPUTER INC		Engineer: KEN_JIN	
Size	Project Name	Rev	
A3	Standard Circiut	0.1B	
Date: Thursday, March 19, 2009		Sheet 35 of 48	

5,18,20,23 S\_SMBCLK\_MAIN  
5,18,20,23 S\_SMBDATA\_MAIN  
16 PCI\_INT2  
16 PCI\_INT1

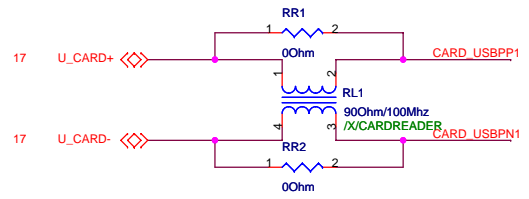


Install GSR6 being slave address "3A" for  
ADI/Freescale/ST G-sensors

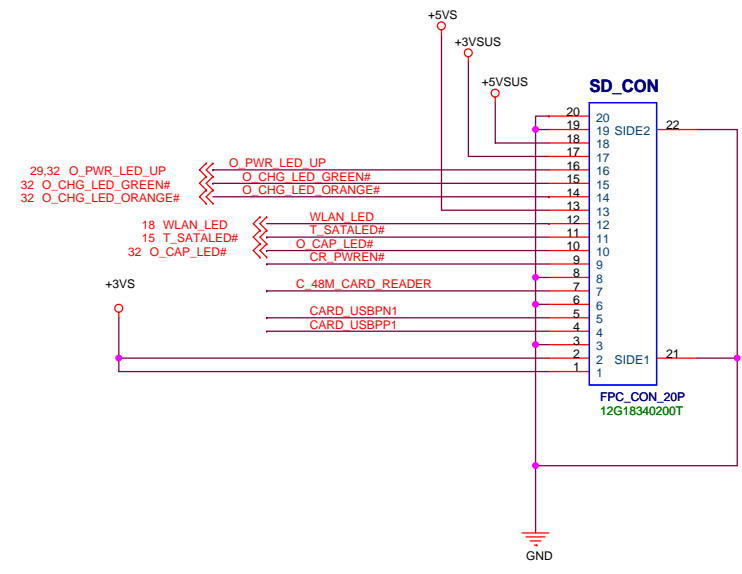


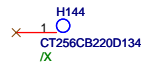
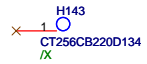
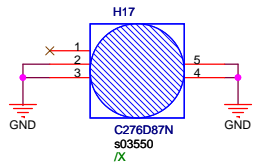
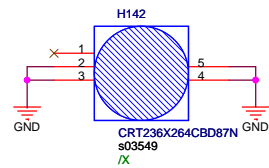
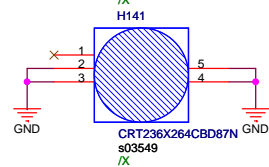
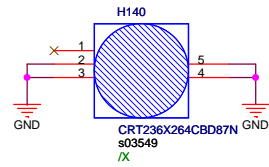
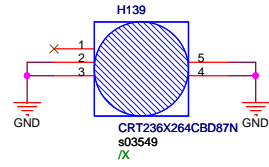
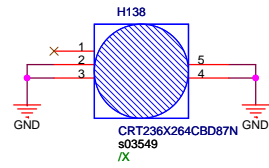
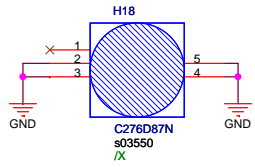
<Variant Name>

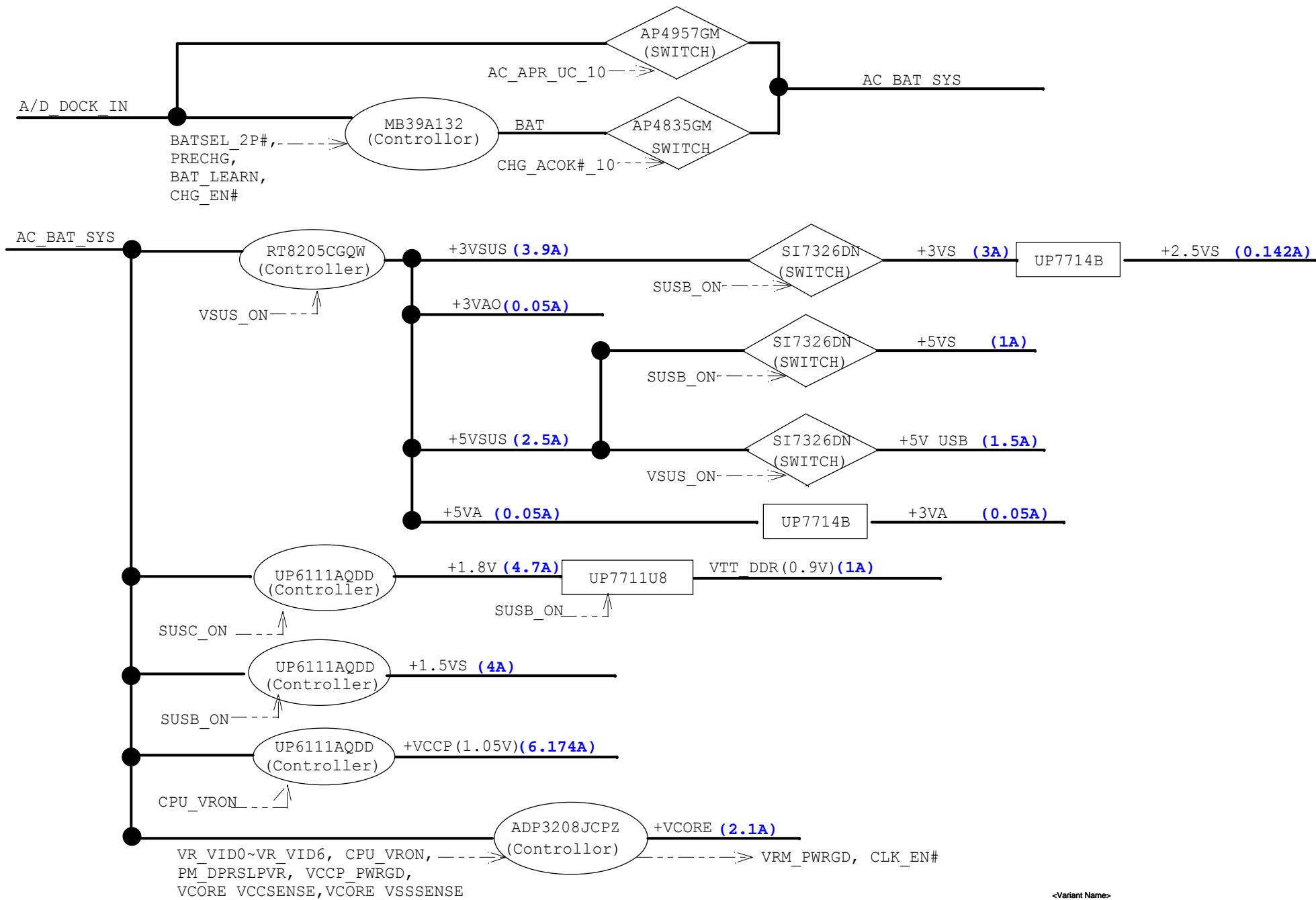
		Title : G_sensor	
ASUSTek Computer Inc.		Engineer: SUSAN_SHI	
Size A3	Project Name Standard Circiut		Rev 0.1A
Date: Thursday, March 19, 2009		Sheet 36 of 48	



4 C\_48M\_CARD\_READER  
17 U\_CARD+  
17 U\_CARD-  
18 CR\_PWREN#

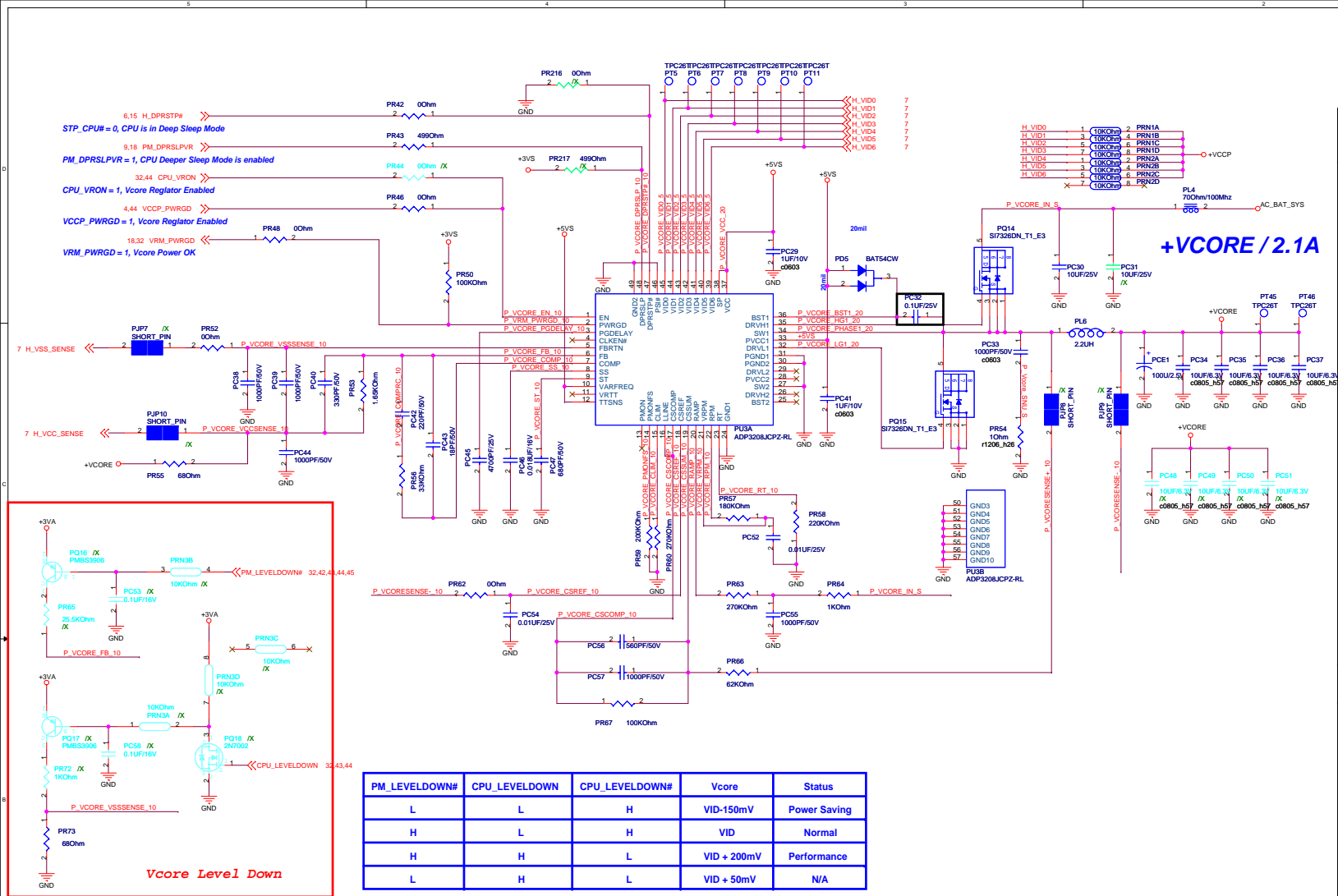












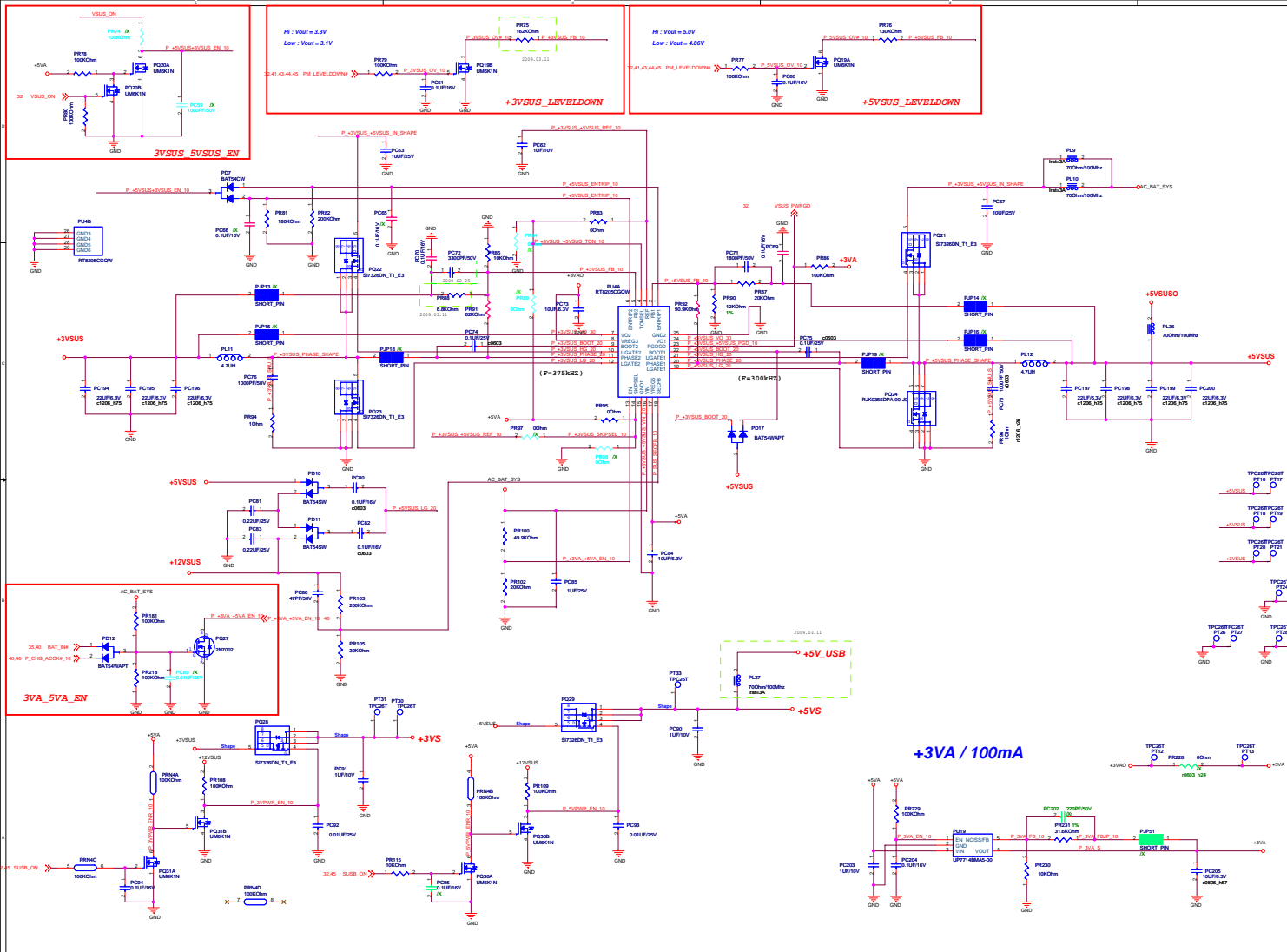
## Power Stage

- I/P Current:**  
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 0.32A$
- Ripple Current:**  
 $I_{rip} = 0.6A$   
 $I_{spec} = 2.5A$
- Dynamic:**  
 $I_{peak} = 2.1A$   
 $ESR / 1 \text{ pcs} = 18m\Omega$   
 $V = 38mV$
- Inductor Spec:**  
 $I_{sat} = 14A$   
 $I_{dc} = 8A$   
 $DCR = 18m\Omega$
- MOSFET Spec:**  
**H-side MOSFET: SI7326DN\_T1\_E3**  
 $R_{ds(ON)} = 22m\Omega$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 6.5A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 40A$  (Pause  $\leq 10\mu s$ )  
**L-side MOSFET: SI7326DN\_T1\_E3**  
 $R_{ds(ON)} = 22m\Omega$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 6.5A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 40A$  (Pause  $\leq 10\mu s$ )

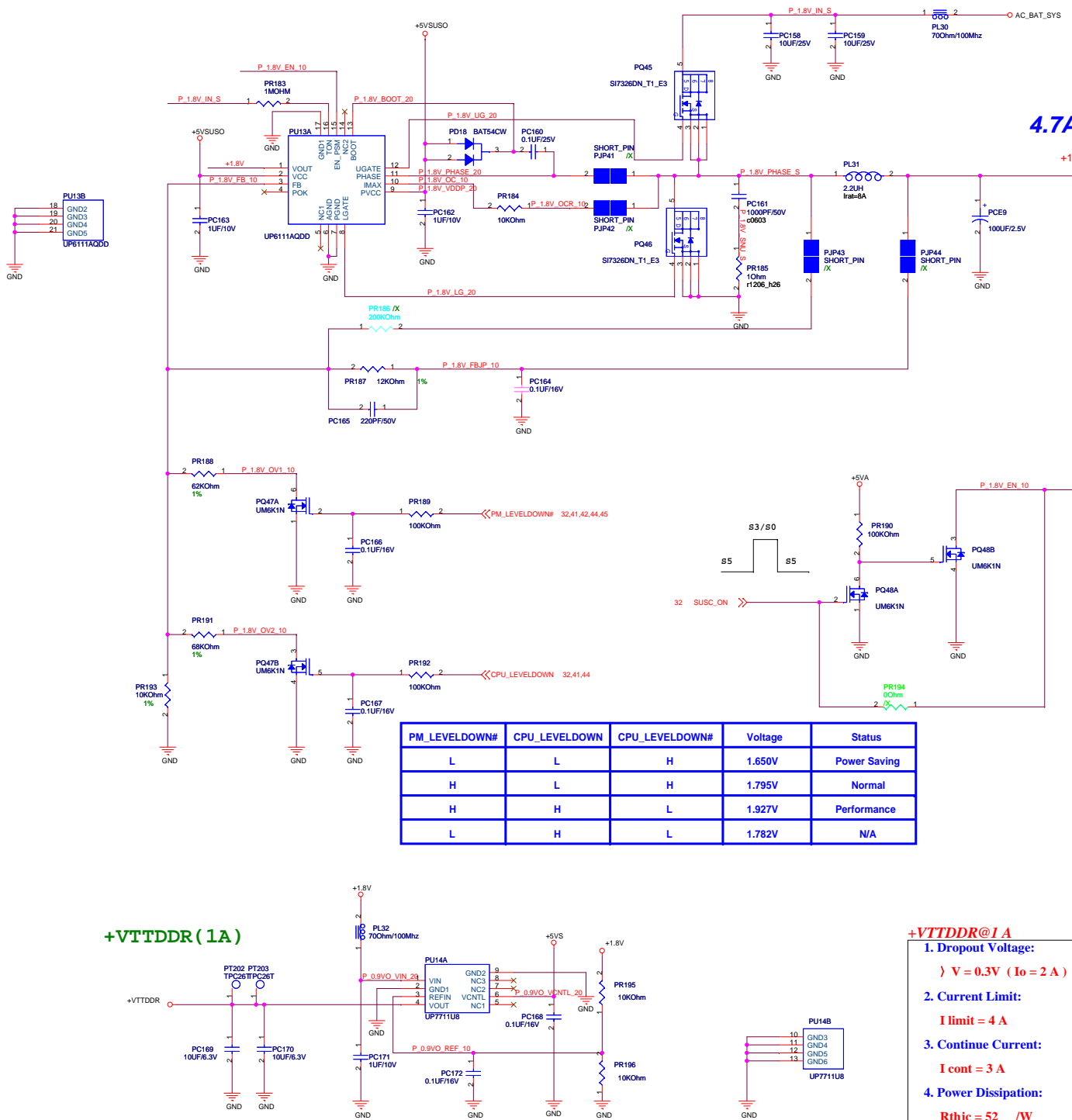
## Controller

- Voltage & Current:**  
 $V_{CORE} = 0.5 - 1.5V @ 2.1A$
- Frequency:**  
Set  $PR58 = 220K\Omega$   
 $F_{osc} = 322KHz$  for RPM  
Set  $PR57 = 180K\Omega$   
 $F_{osc} = 272KHz$  for CCM
- OCP:**  
Set  $PR60 = 270K\Omega$   
 $I_{ocp} = 9.3A$
- POR:**  
POR Hysteresis  $= 0.15V$   
 $V_{on} = 4.4 - 4.5V$   
 $V_{off} = 4.0 - 4.2V$
- UVP:**  
 $VID = 300mV$
- OVP:**  
 $VID = 200mV$
- Soft start time:**  
 $2.7ms$
- Phase selection:**  
 $SP = VCC$   
single phase
- Loadline:**  
 $30m\Omega$

<Variant Name>



Power stage		+3VSUS	+5VSUS
1. I/P Current:		I in = Vo/Io/( 0.8 * Vin ) =1.1A	I in = Vo/Io/( 0.8 * Vin ) =1.67A
2. Ripple Current:		I rip =1.36A I spec=2.5A Q1 pcs	I rip =2.07A I spec=2.5A Q1 pcs
3. Dynamic:		I peak=3A ESR / 1 pcs =18 mohm ) V =54mV	I peak=3A ESR / 1 pcs =18 mohm ) V =54mV
4. Inductor Spec:		I sat=10 A I dc =5.5 A DCR=37 mohm	I sat=10 A I dc =5.5 A DCR=37 mohm
5. MOSFET Spec:		H-side MOSFET: SI7326DN_T1_E3 Rds(ON)= 22 mohm (Vgs=4.5 V) I cont = 6.5 A (T =25 ) I peak = 40 A (Pause ≥10 us)	H-side MOSFET: SI7326DN_T1_E3 Rds(ON)= 22 mohm (Vgs=4.5 V) I cont = 6.5 A (T =25 ) I peak = 40 A (Pause ≥10 us)
L-side MOSFET: SI7326DN_T1_E3		Rds(ON)= 22 mohm (Vgs=4.5 V) I cont = 6.5 A (T =25 ) I peak = 40 A (Pause ≥10 us)	Rds(ON)= 10.7 mohm (Vgs=10 V) I cont = 30 A (T =25 ) I peak = 120 A (Pause ≥10 us)
Controller		+3VSUS	+5VSUS
1. Voltage & Current:		+3VSUS=3.3V@3A	+5VSUS=5V@2.5A
2. Frequency:		fosc=375KHz	fosc=300KHz
3. OCP:		Set PR1=180Kohm Iocp=8A	Set PR2=200Kohm Iocp=17A
4. POR:		V on =4.35-4.5 V V off =3.9-4.25 V	V on =4.35-4.5 V V off =3.9-4.25 V
5. UVP:		V uvp= 70% Vout	V uvp= 70% Vout
6. OVP:		V ovp=115%Vout	V ovp=115%Vout
7. Enable Voltage:		V rising = 1V V falling = 0.4 V	V rising = 1V V falling = 0.4 V
8. Soft start time:		Tss=2ms	Tss=2ms
9. Phase selection:		/X	/X
10. Inrush Current:		C total = 100 uF I inrush= 0.165 A	C total = 100 uF I inrush= 0.25 A
+3VA AEC / 100mA		1. Dropout Voltage: ) V = 0.21V (Io = 0.3A ) 2. OCP: I ocp=480mA 3. Short Circuit Current Limit: I sc= 320mA 4. Power Dissipation: Rthja =250 /W Pd = 0.4W	5. EN Voltage: V en = 2V V od = 6. Power OK Voltage: Vpokth = 92% *Vout Vpokhys = 8% 7. Inrush current: T ss = 400us C total =10uF I inrush 8. Feedback Voltage: VFB = 0.8 V



## Power stage

### 1. I/P Current:

$$I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.175A$$

### 2. Ripple Current:

$$I_{rip} = 1.88A$$

$$I_{spec} = 2.5A \odot 1$$

### 3. Dynamic:

$$I_{peak} = 4.7A$$

$$ESR / 1 \text{ pcs} = 18 \text{ mohm}$$

$$V = 84.6mV$$

### 4. Inductor Spec:

$$I_{sat} = 14A$$

$$I_{dc} = 8A$$

$$DCR = 18 \text{ mohm}$$

### 5. MOSFET Spec:

H-side MOSFET: SI7326DN\_T1\_E3

$$R_{ds(ON)} = 22 \text{ mohm} \quad (V_{gs} = 4.5V)$$

$$I_{cont} = 6.5A \quad (T = 25^\circ C)$$

$$I_{peak} = 40A \quad (\text{Pause} \geq 10 \mu s)$$

L-side MOSFET: SI7326DN\_T1\_E3

$$R_{ds(ON)} = 22 \text{ mohm} \quad (V_{gs} = 4.5V)$$

$$I_{cont} = 6.5A \quad (T = 25^\circ C)$$

$$I_{peak} = 40A \quad (\text{Pause} \geq 10 \mu s)$$

## Controller

### 1. Voltage & Current:

$$+1.8V @ 5.8A$$

### 2. Frequency:

$$PR183 = 1M \text{ ohm}$$

$$F_{osc} = 250KHz$$

### 3. OCP:

$$PR184 = 10K \text{ ohm} \rightarrow 9A$$

### 4. POR:

$$V_{ccrth} = 3.7 \sim 4.1V$$

$$V_{cclys} = 0.2V$$

### 5. UVP:

$$V_{out} = 70\%$$

### 6. OVP:

$$V_{out} = 115\%$$

### 7. Enable Voltage:

$$V = 2.9V$$

### 8. Soft start time:

$$T_{ss} = 1.2 \text{ ms}$$

### 9. Phase selection:

$$/X$$

### 10. Inrush Current:

$$C_{total} = 100 \mu F$$

$$I_{inrush} = 0.15A$$

### +VTDDR@1A

#### 1. Dropout Voltage:

$$V = 0.3V \quad (I_o = 2A)$$

#### 2. Current Limit:

$$I_{limit} = 4A$$

#### 3. Continue Current:

$$I_{cont} = 3A$$

#### 4. Power Dissipation:

$$R_{thjc} = 52^\circ C/W$$

$$P_d = 1.9W$$

#### 5. EN Voltage:

$$V_{en} = 1.4V$$

$$V_{sd} = 0.8V$$

#### 6. Supply Voltage:

$$V_{cc} = 5V$$

#### 7. Inrush current:

$$T_{ss} = 5 \text{ ms}$$

$$C_{total} = 10 \mu F$$

$$I_{inrush} = 1.8 \text{ mA}$$

<Variant Name>

ASUSTek Computer INC.

Title : +1.8V & +VTDDR

Engineer: Joy Zhou

Size Project Name 100SHA

Date: Thursday, March 19, 2009 Sheet 43 of 48







Ver	Description	Date
1.0G	change UF1 to the same as 1005hn's	2009.0122.2027
	change lvds conn P/N to 12G170190201 change CPU P/N from 01G012290000 to 01G012520100  P4:橄 CC50 ..CC57 盤箬臂ꠤ clock gen pin 狼 P23:橄 GC21 P29: 奔IL2	2009.0203.1555
	update NB symbol 癸clock gen cm WIFI 场だ 酚1005HN 秊ㄟ 穰	2009.0205.1555
	P4: C_PCIE_LAN_R C_PCIE_LAN#_R H_ITP_CKOUT H_ITP_CKOUT# add 10pf for RF P23: cancel BL_EN, G_LVDD_EN, G_NBL_CTRL EMI cap	2009.0205.2120
	ADD LR55  02/14 newjane: Change PR227 to 5% 10G212105004031 02/14 newjane: Change OR1 from 18.2K to 18K 10G212180214010 02/14 newjane: Change HR1 from 68ohm to 56 ohm 02/14 newjane: Change SR1 from 20K 10G212200214110to 20K 10G212200214030 02/14 newjane: ChangeHC18 from 11G23211021115 to 11G232110214030 02/14 newjane: ChangeHC6 GC20 HC11 HC12 from 11G233310531360 to11G233210516320 02/14 newjane: /X LC41 02/14 newjane: SD RC1 RC7 RC12 from 11G232310431360to11G232110411320 02/14 xiao-jie SR4 PR227 from 10G212105004031 to 10G212100414030 02/14 xiao-jie aAR8 AR5 from 10G212200214110 to 10G212200214030 02/14 xiao-jie AR7 P/N toPR105 P/N	2009.0210.1513

