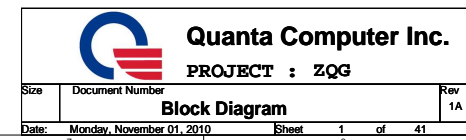
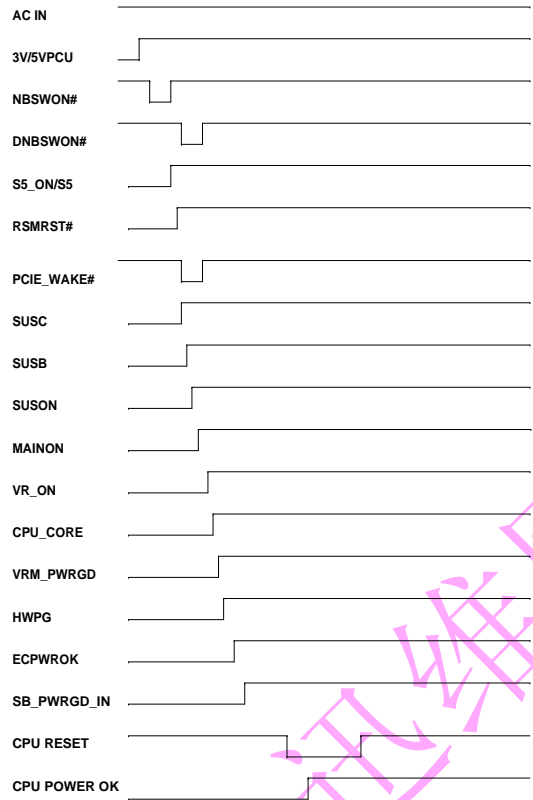


ZQG SYSTEM DIAGRAM



[illegible]

Power Sequence

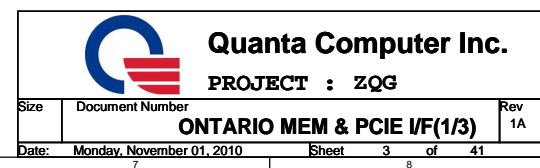


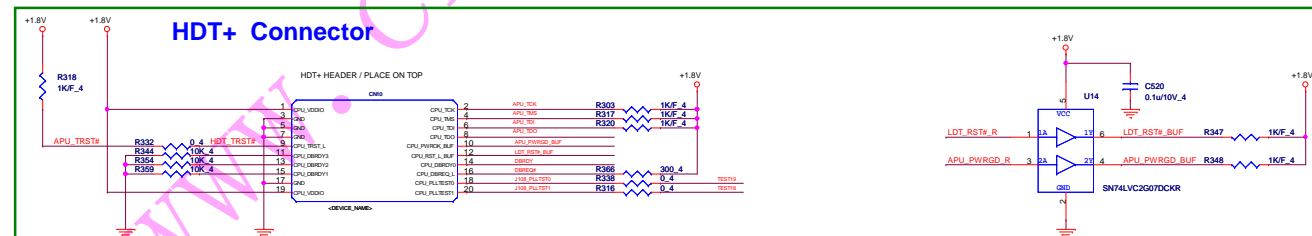
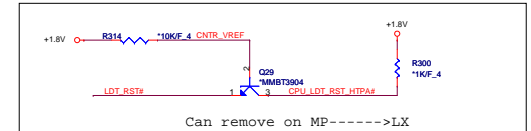
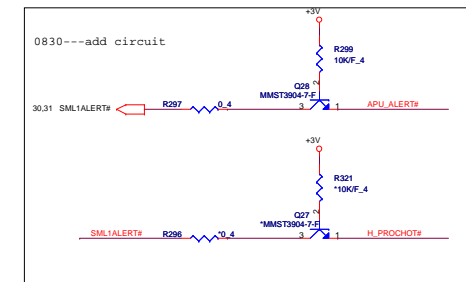
Hudson M1 SM BUS

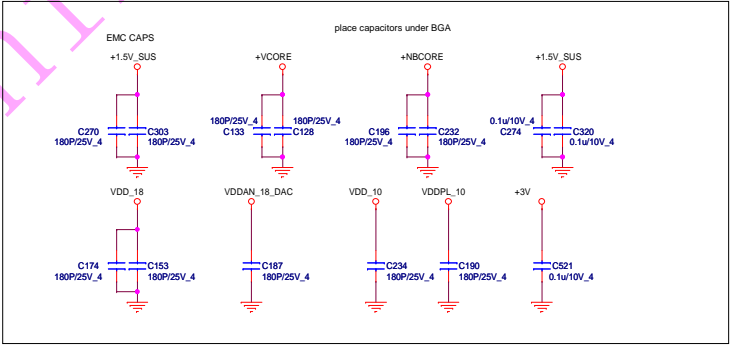
SB820 SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD22 AE22	DDR / RFID
SB_SMBCLK1 SB_SMBDATA1 (+3V_S5)	F5 F4	not used
SB_SCLK2 SB_SDATA2 (+3V_S5)	D25 F23	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used

KBC(EC) SM BUS

KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	110 111	Battery
MBCLK_THRM MBDATA_THRM (+3VPCU)	115 116	Thermal

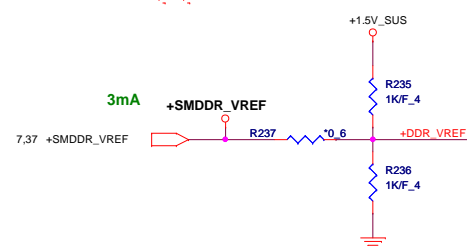
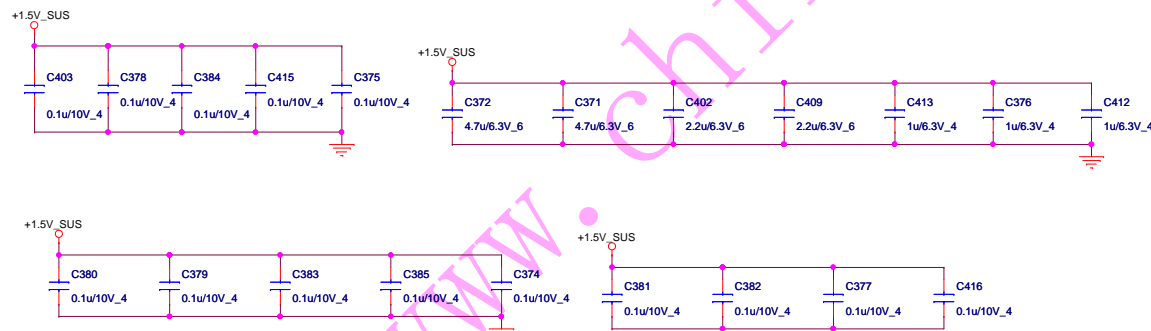
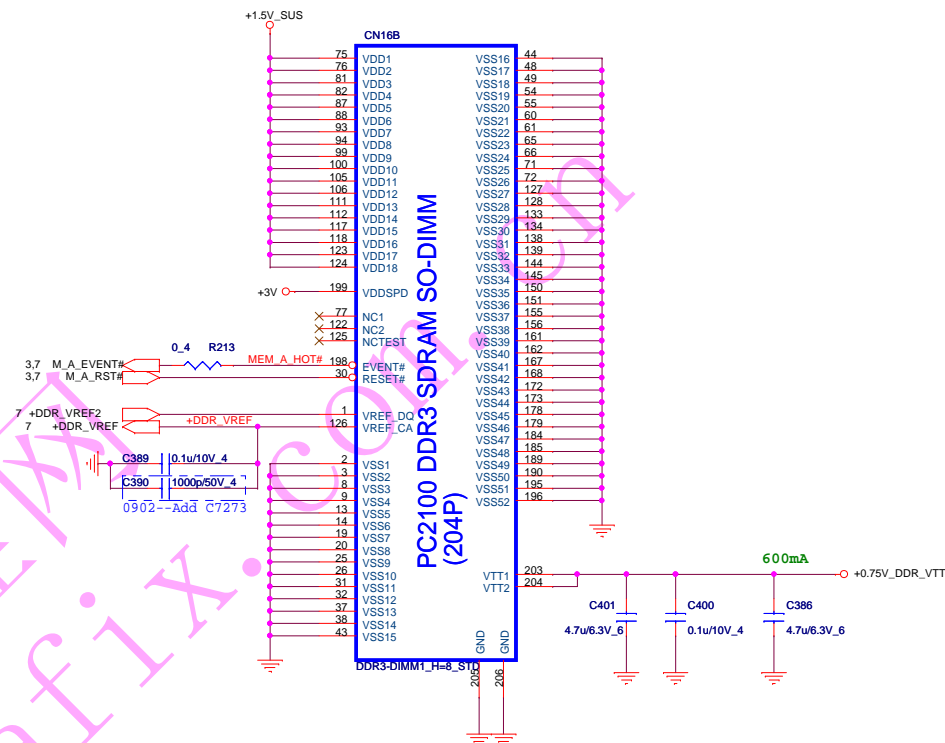
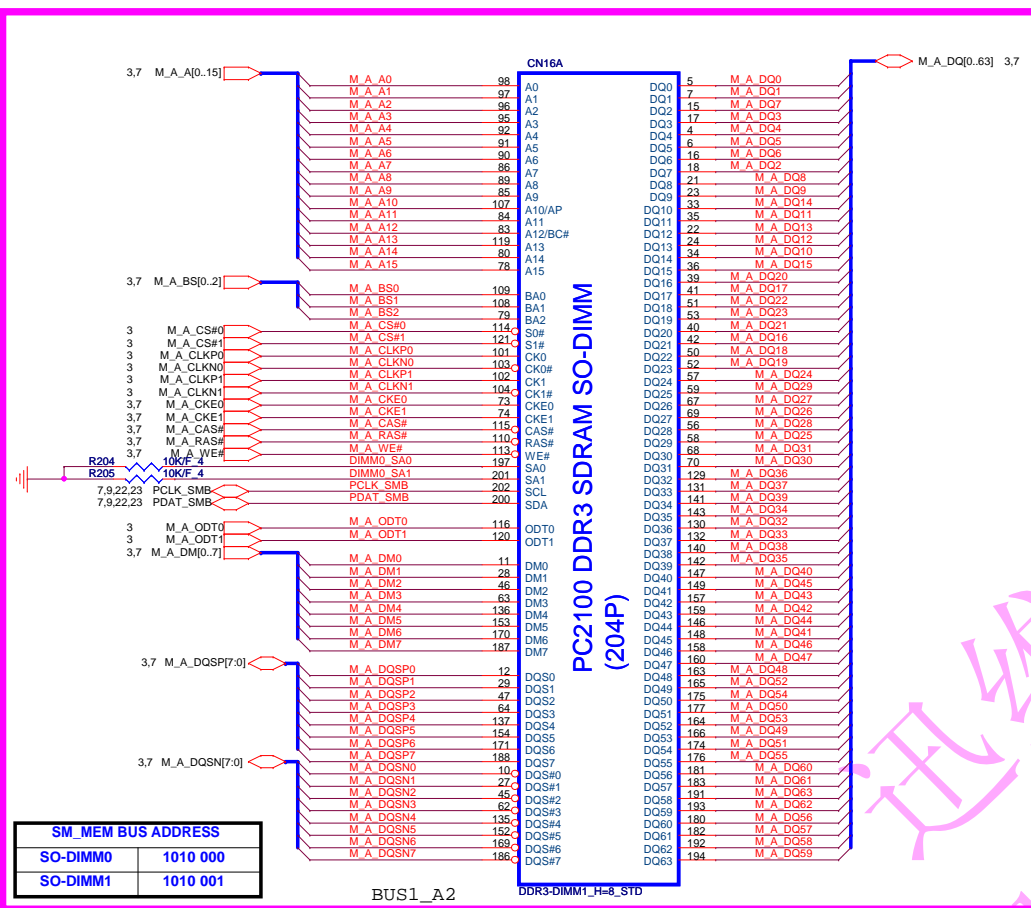


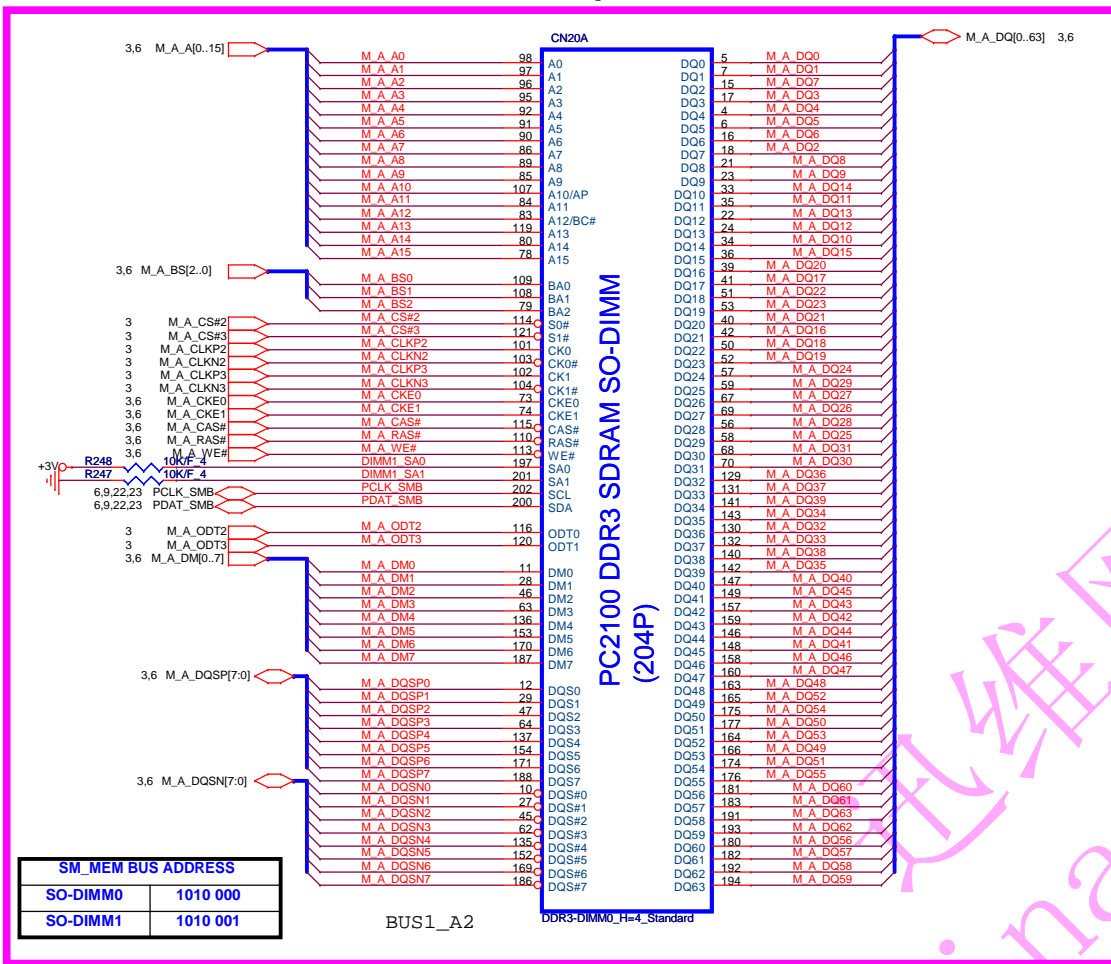


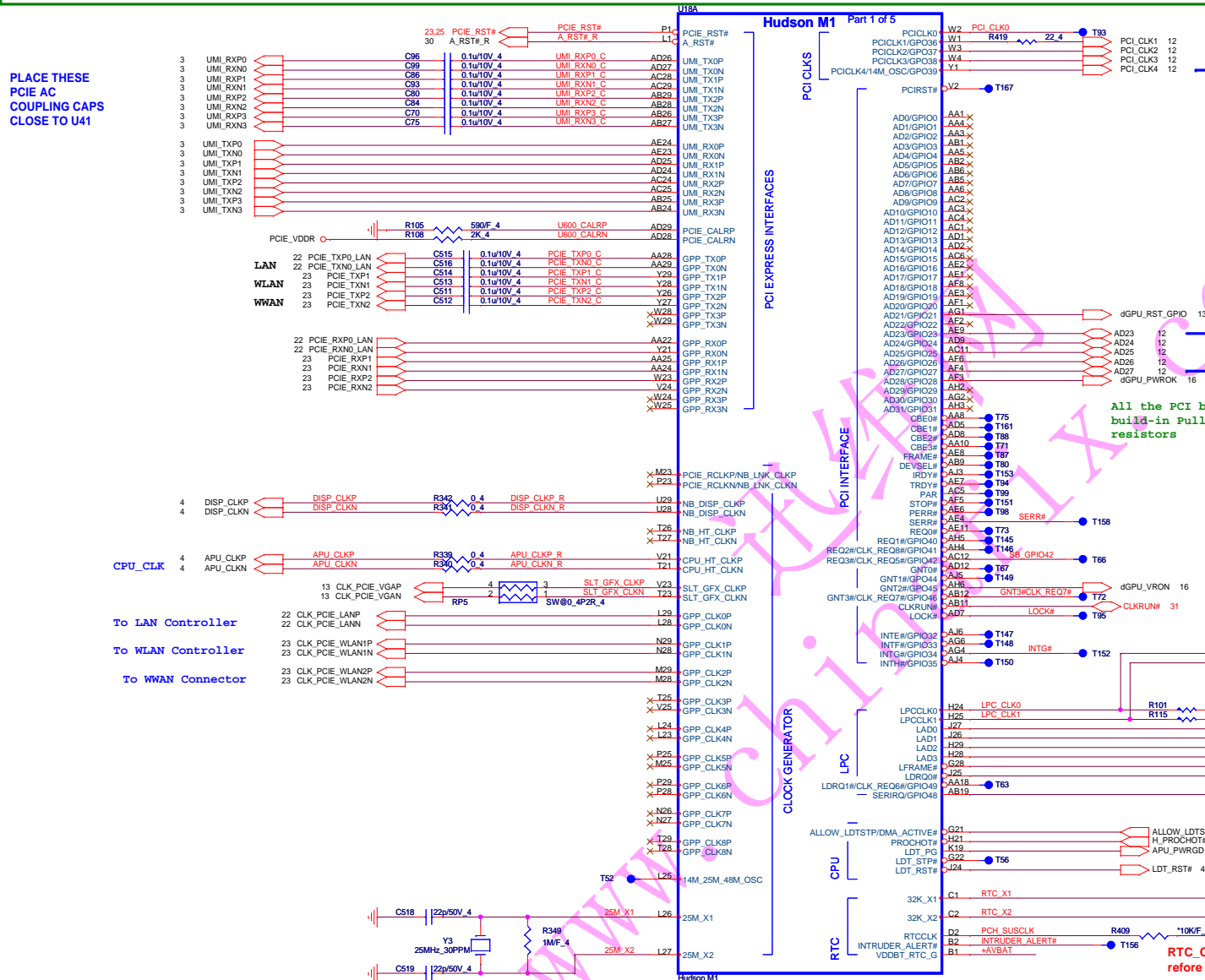
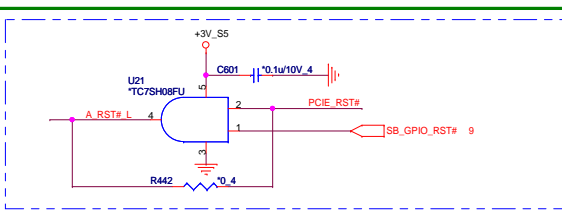


0830--P/N and footprint are follow ZR7B

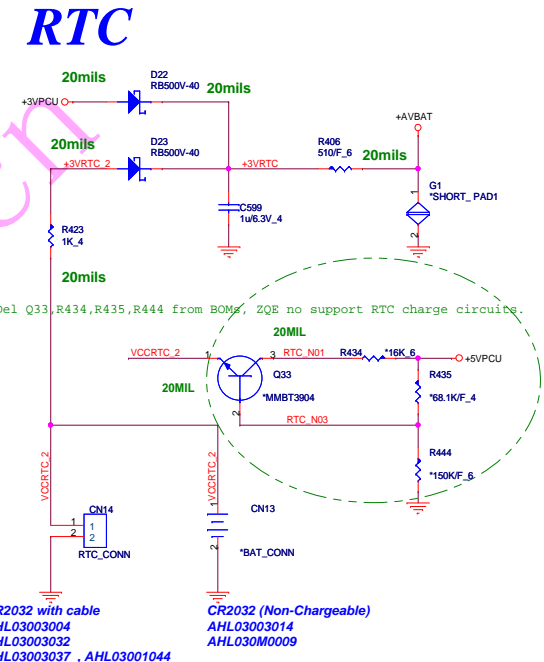
+1.5V_SUS 3,5,7,30,37,39
 +0.75V_DDR_VTT 7,37
 +3V 4,5,7,9,10,11,12,16,17,20,21,23,25,26,29,30,31,33,34,35,36,37,38,39,40





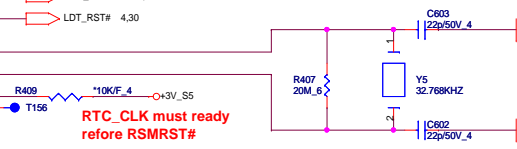


INTRUDER_ALERT# Left not connected (Southbridge
has 50-kohm internal pull-up to VBAT).



CR2032 with cable
AHL03003004
AHL03003032
AHL03003037 , AHL03001044

CR2032 (Non-Chargeable)
AHL03003014
AHL030M0009

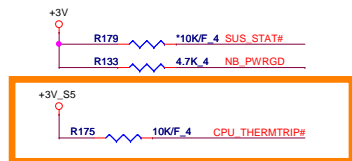


PCH_SUSCLK

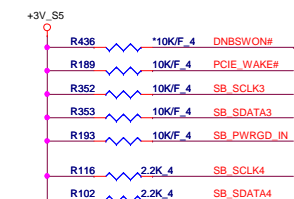
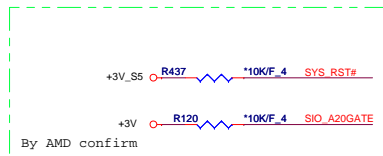
+3V_SCL0/SDATA0 is 3V tolerance
AMD datasheet define it

R125 2.2K 4 PCLK SMB
R131 2.2K 4 PDAT SMB

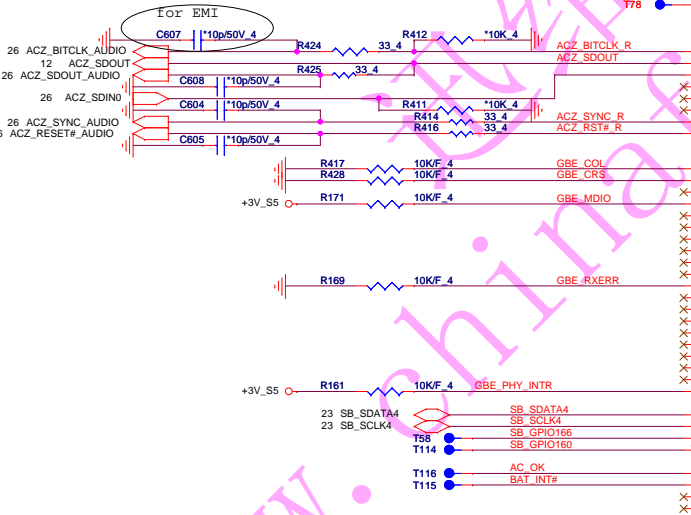
Clock gen/Robson/TV
tuner
/DDR3/DDR3
thermal/Accelerometer



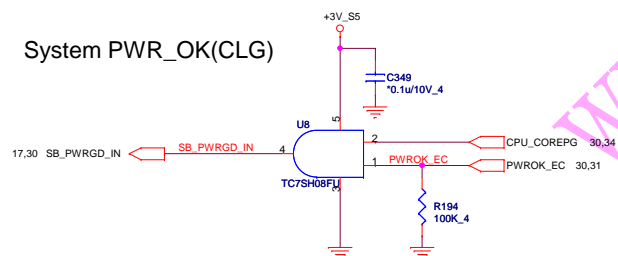
SB/ PWR_GOOD / VDDIO_33_5



To Azalia
HD audio
interface
is 3.3V5
voltage



System PWR_OK(CLG)



U18D

Hudson M1
Part 4 of 5

ACPI/WAKE UP EVENTS

USB 1.1 USB MISC

USB 2.0

GPIO

USB OC

HD AUDIO

GBE LAN

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USB 2.0

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USB OC

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SATA PORT 0,1,2,3
can support AHCI
mode

PLACE SATA AC COUPLING
CAPS CLOSE TO HUDSON M1

SATA HDD

SATA ODD

PLACE SATA_CAL RES
VERY CLOSE TO BALL
OF HUDSON M1

XTLVDVDD_SATA-- SATA
crystal power
PLVDVDD_SATA--
SATA PLL
POWER

AVDD_SATA

29 SATA_LED#

C575

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T162

U188

Hudson M1
Part 2 of 5

SERIAL ATA

HW MONITOR

SPI ROM

Hudson M1

Hudson M1

Hudson M1

Hudson M1

Hudson M1

Hudson M1

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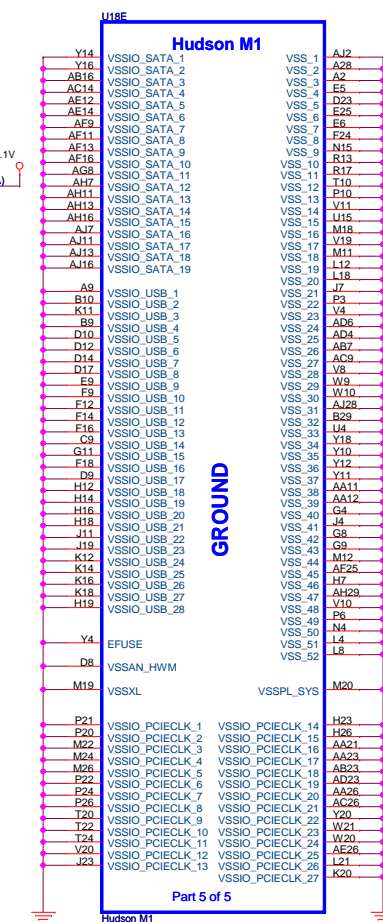
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PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

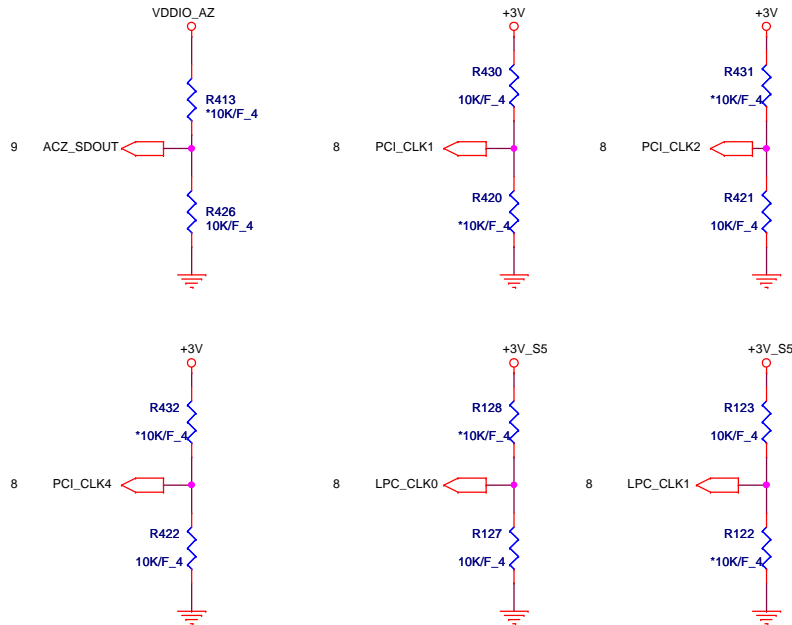




OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

internal have pull
Hi 10K , confirm AMD
ward this pull Hi
not need



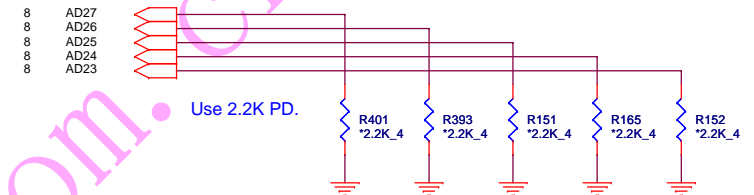
PCI_CLK4 CPU/NB HT Clock Selection
0 V - Reserved.
3.3 V - Required setting for integrated clock mode.
This strap is not used if the strap CLKGEN is
configured for external clock generator mode.

REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM (Default)	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM L,L = FWH ROM	

DEBUG STRAPS

HUDSON-M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





Quanta Computer Inc.


PROJECT : ZQG


Size	Document Number	Rev
	HUDSON STRAPS/PWRGD(5/5)	1A
Date:	Monday, November 01, 2010	Sheet 12 of 41

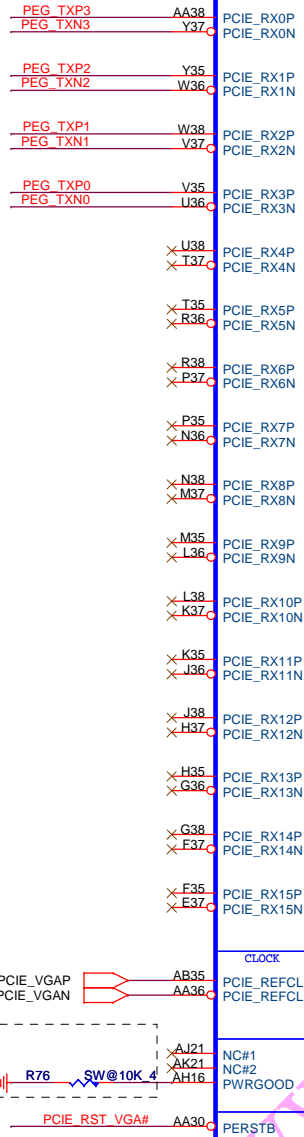
U15A

3 PEG_TXP[3..0]  PEG_TXP[3..0]

3 PEG_TXN[3..0]  PEG_TXN[3..0]

3 PEG_RXP[3..0]  PEG_RXP[3..0]

3 PEG_RXN[3..0]  PEG_RXN[3..0]

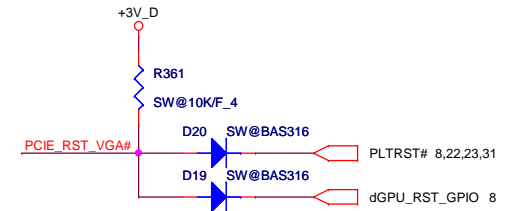
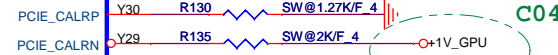


For Madison and Park
the PWRGOOD ball must
be connected to ground

PCI
EXPRESS
INTERFACE

CALIBRATION

PCIE_CALRP
PCIE_CALRN



Quanta Computer Inc.

PROJECT : ZQG

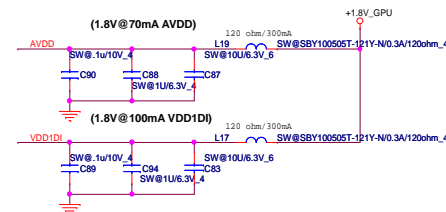
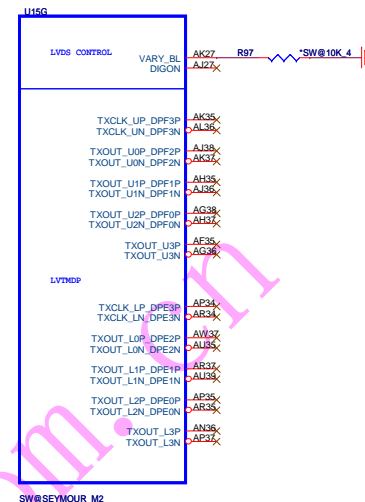
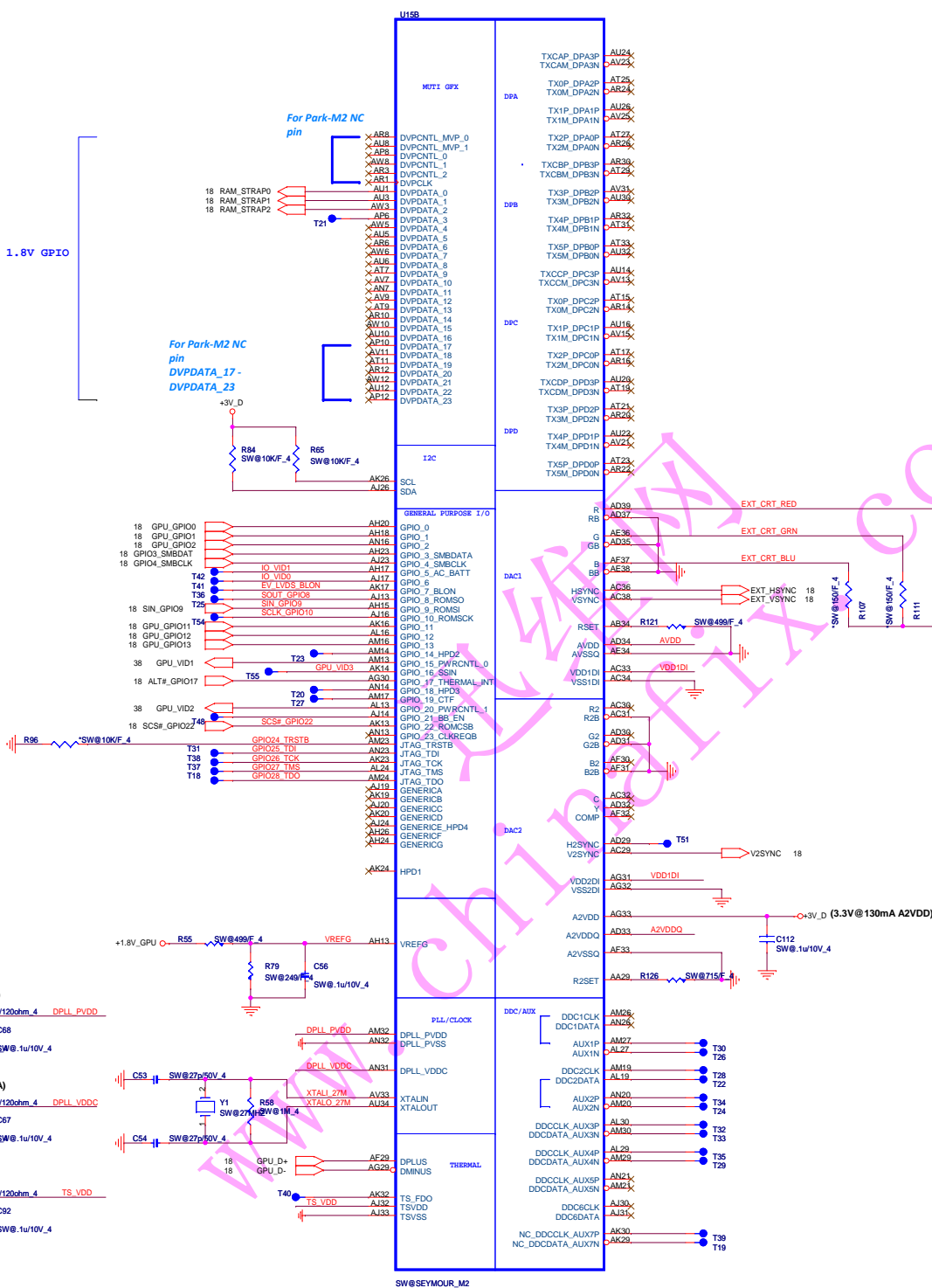
Size	Document Number	Rev
	SeymourPCIE 1/6	1A
Date:	Monday, November 01, 2010	Sheet 13 of 41

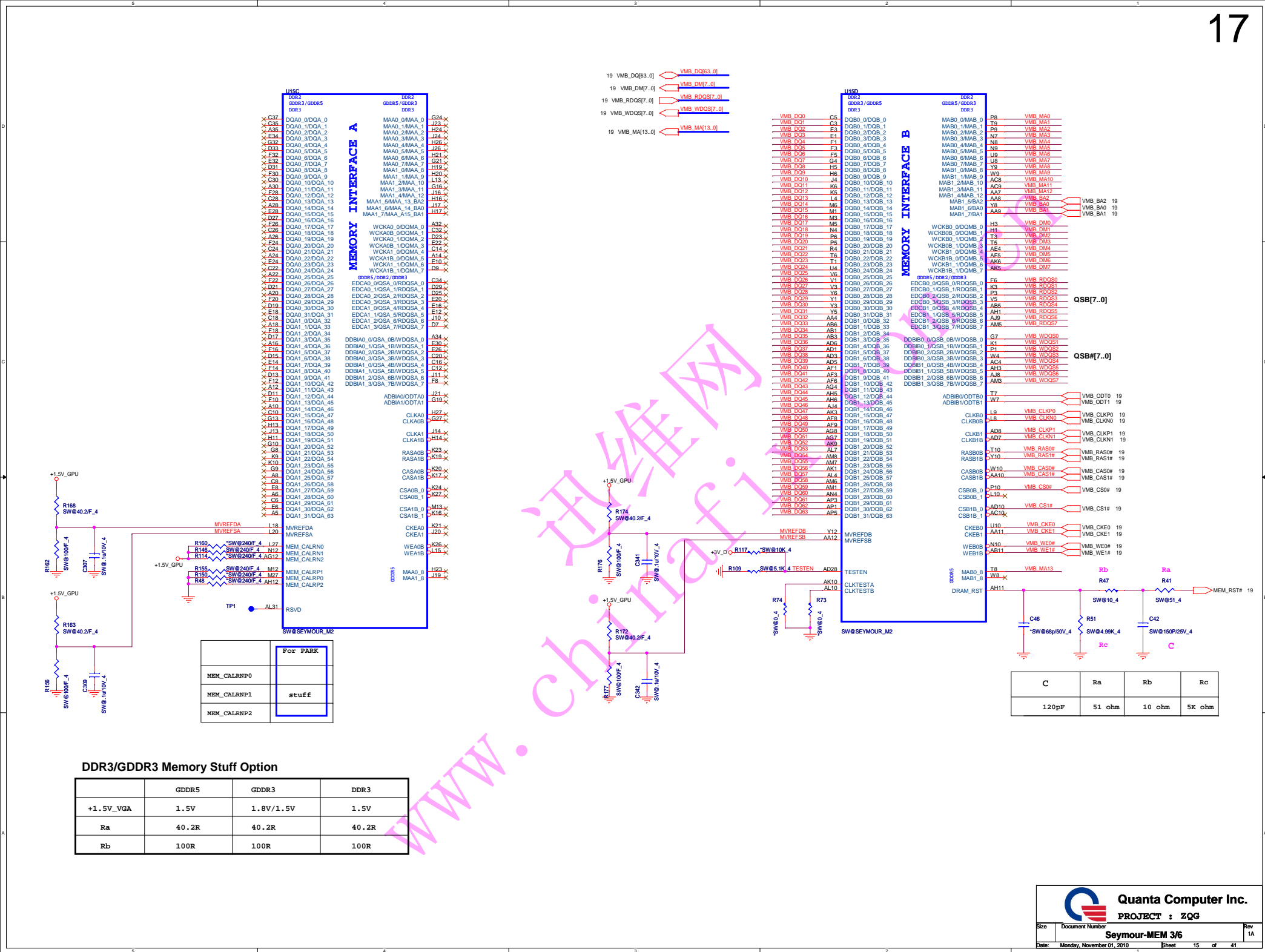
GPU Power-on sequence

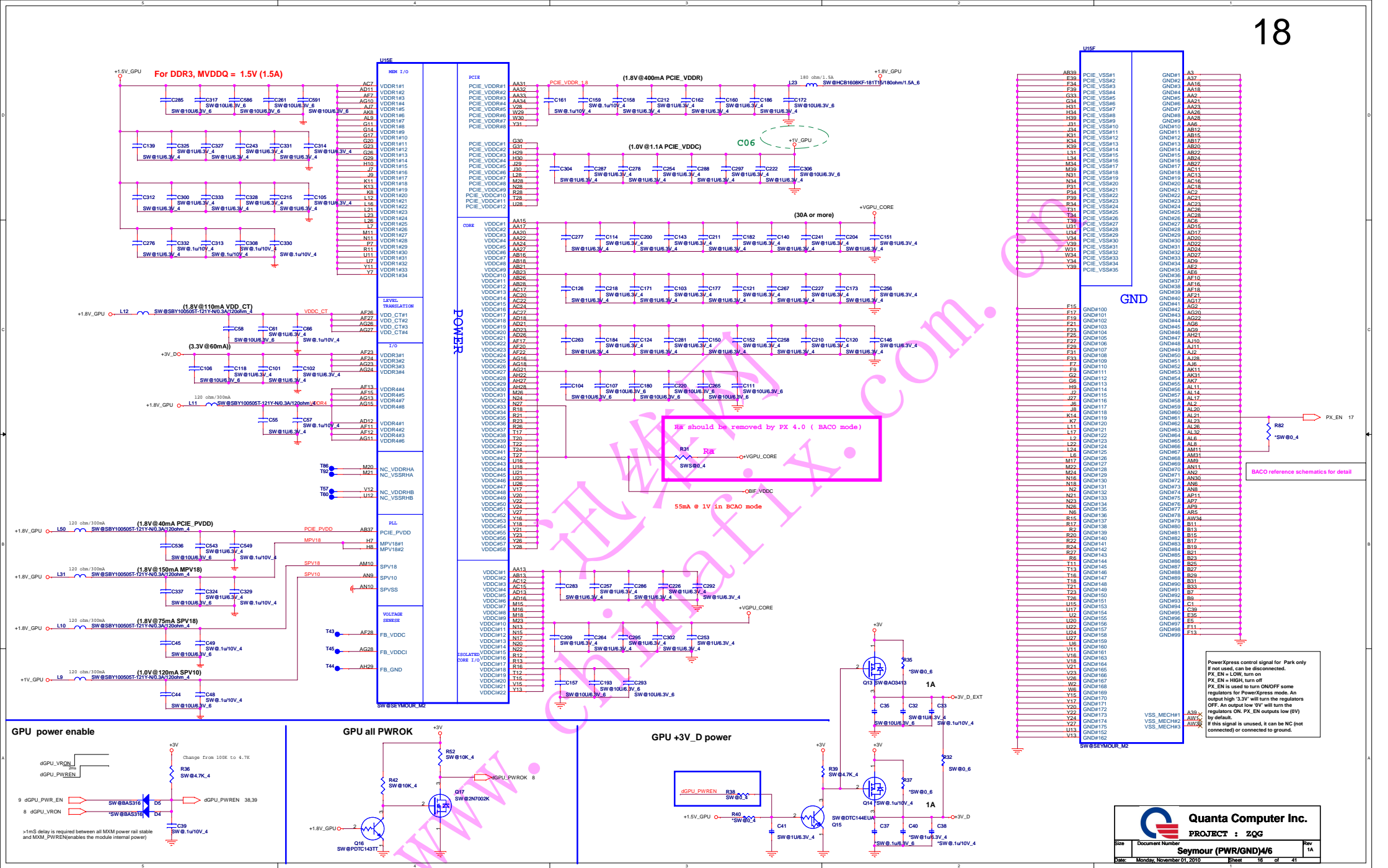
```
1 => +3V_D
2 => +VGPU_CORE
3 => +1V
4 => +1.5V_GPU
5 => +1.8V_GPU
6 => dGPU_PWROK
```

1.8V GPIO

3.3V GPIO

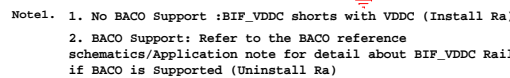




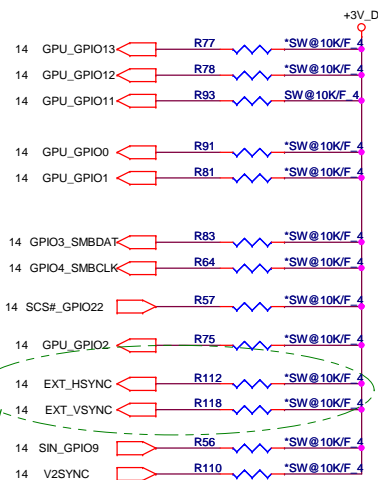




BACO MODE : Board ID / BACO part / Del Ra



PIN STRAPS



C08 : to slove the HDMI issue , remove R112,R118 from BOMs

Memory Aperture size

GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

C02 : to slove the Power DVD issue , setting size to 256MB

ROM Table

EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

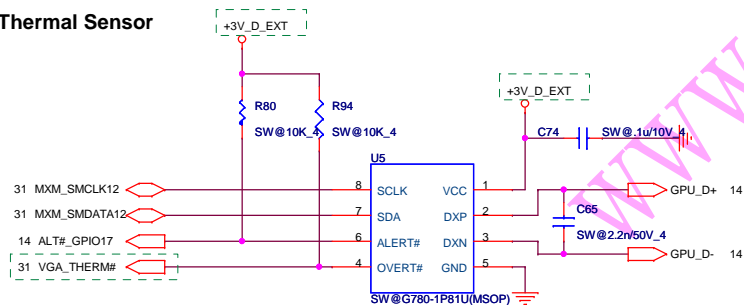
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	00	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

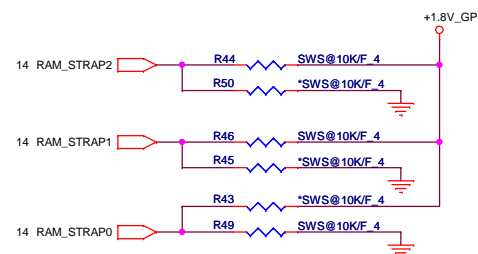
DDR3 Memory Aperture size

Vendor	Vendor P/N	STN B/S P/N	Total Memory Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	ZQE/G
Hynix	H5TQ1G63DFR-11C	AKD5LZWTW05 (64M*16)	1GB (900 Mhz)	1	1	0	V
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB (800 Mhz)	1	0	0	V
	H5TQ2G63BFR-12C	AKD5MGGTW03 (128M*16)	2GB	1	1	1	V
Samsung	K4W1G1646G-BC11	AKD5EGGT503 (64M*16)	1GB	0	1	0	
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB (800 Mhz)	0	0	0	V
	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1	

Thermal Sensor

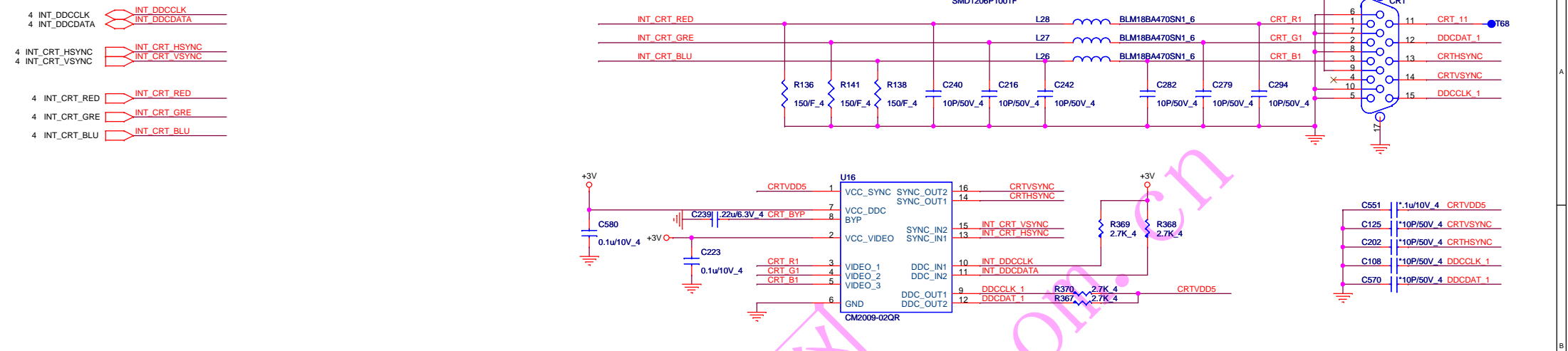


Address ID: 98H

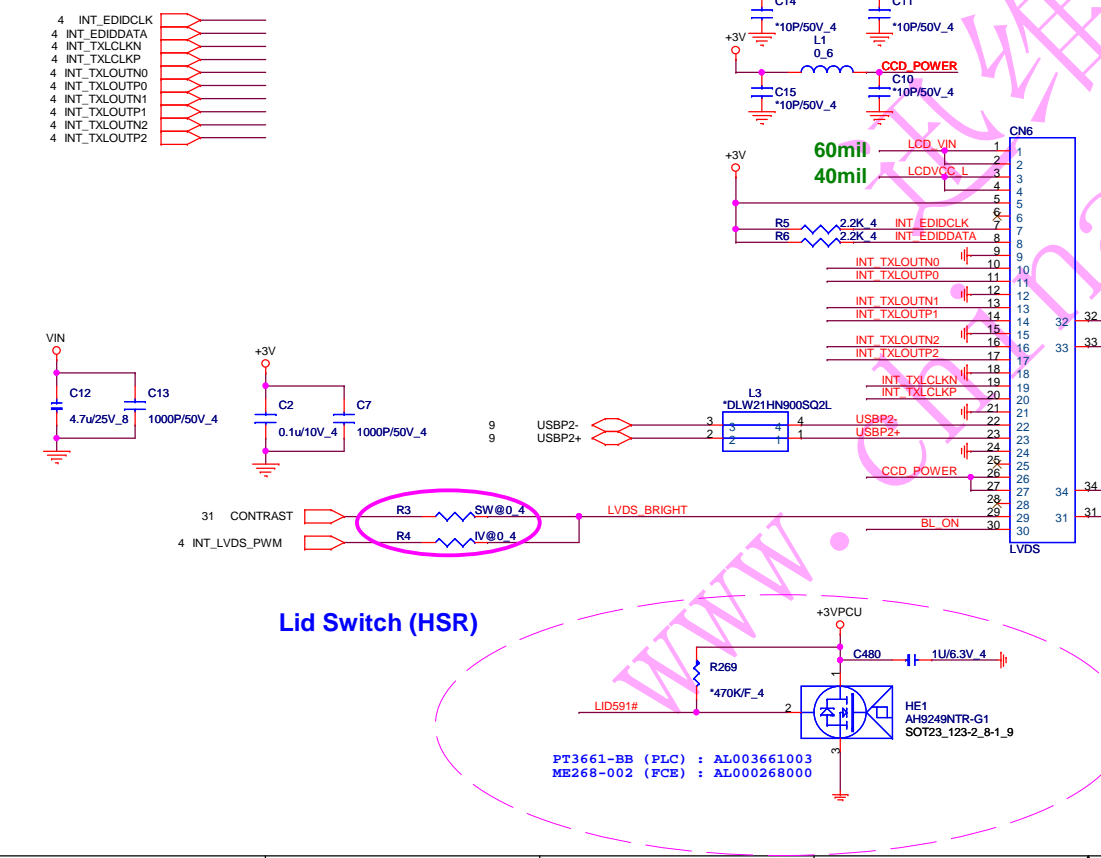
RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

CRT

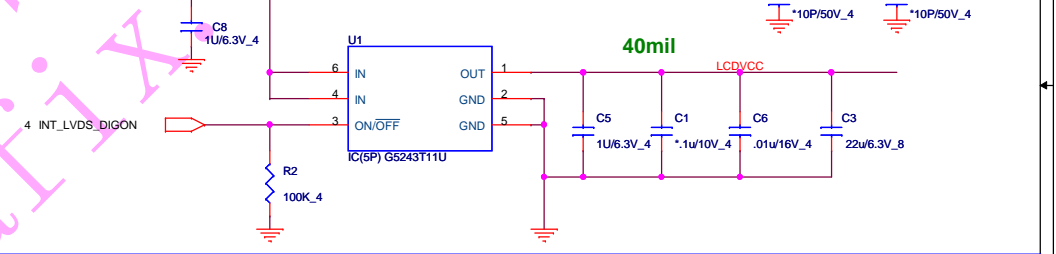
OPTION SIGNAL FROM NB to LVDS/CRT for UMA



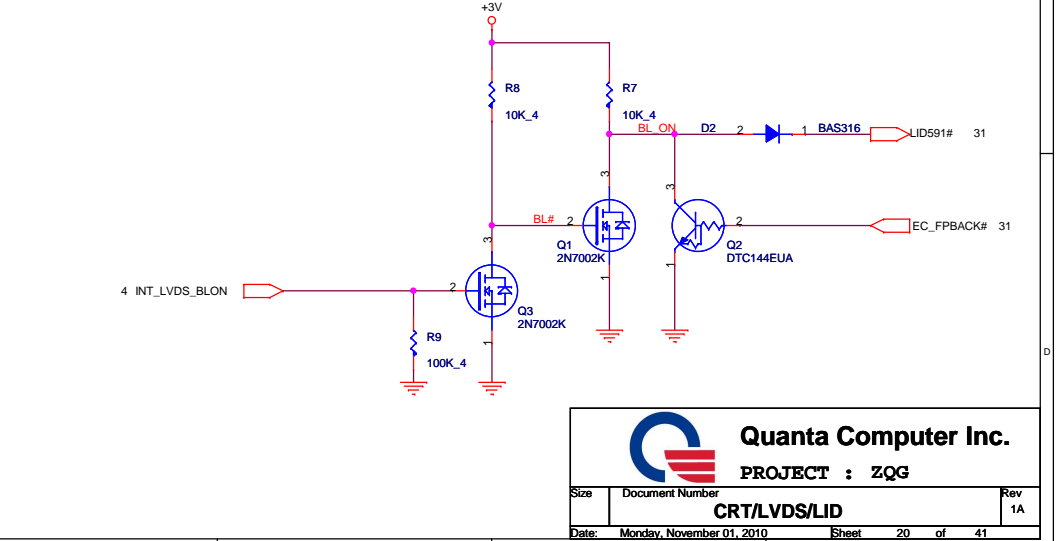
LVDS(LDS)



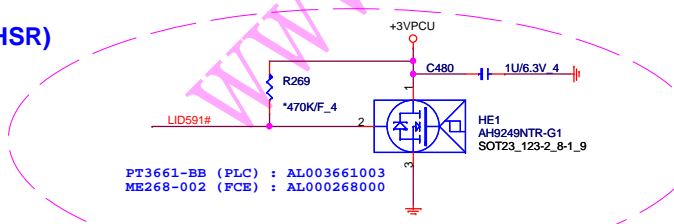
LCD PW(LDS)



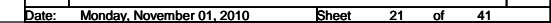
Backlight Control(LDS)



Lid Switch (HSR)



23

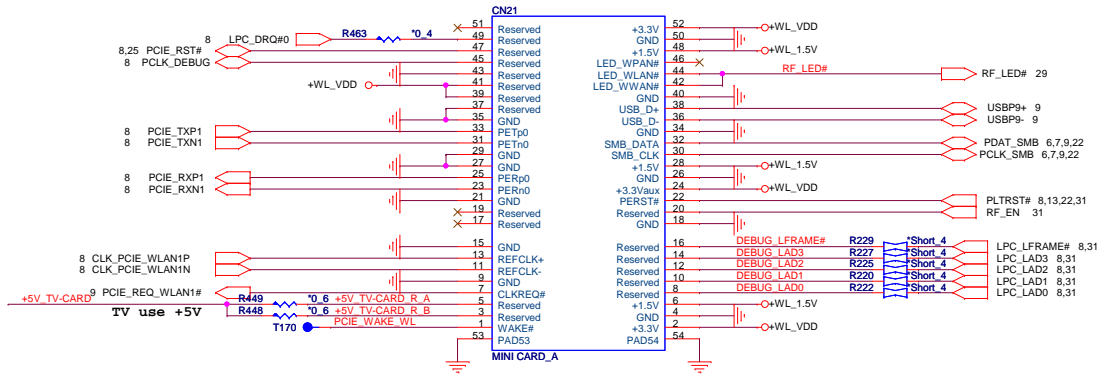


[illegible]

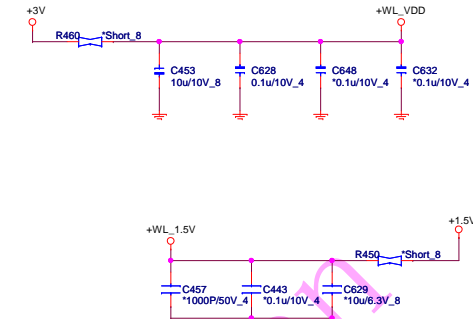
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)



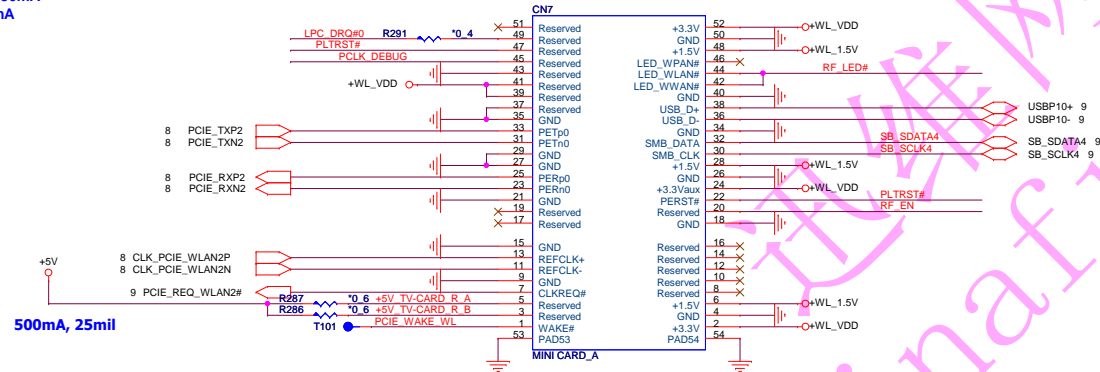
Debug



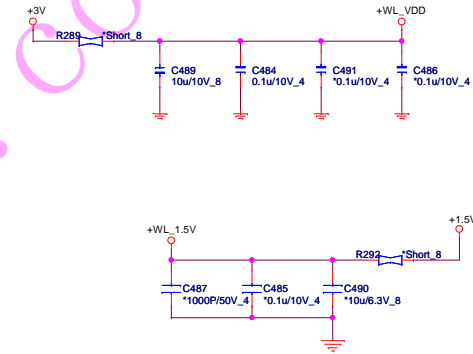
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

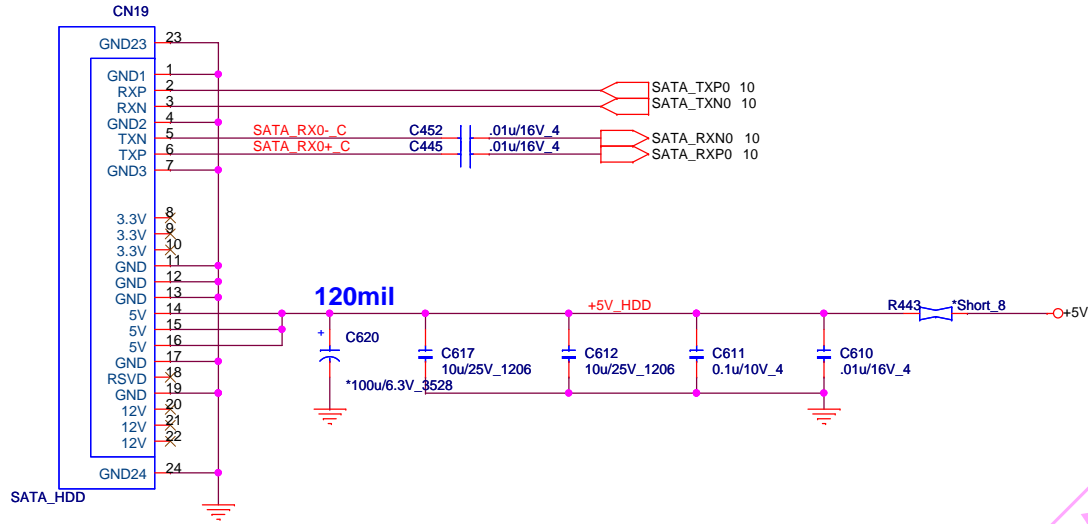
Check LED signal. (active high or low)



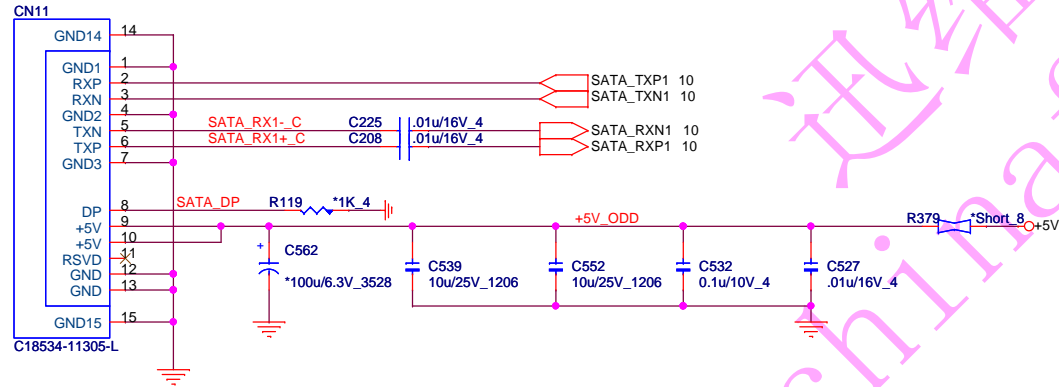
500mA, 25mil



SATA HDD



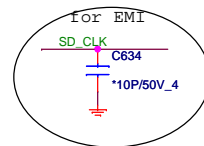
SATA ODD



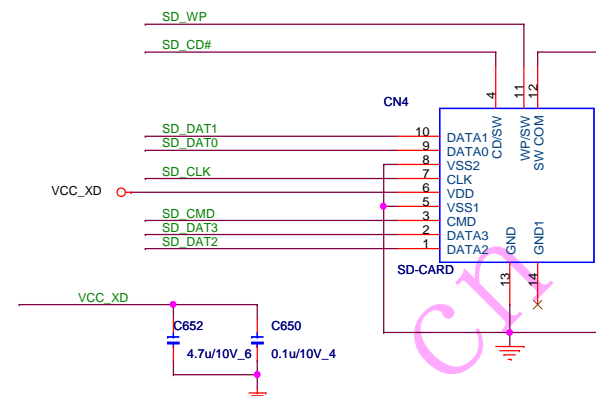
CARD READER Controller

2 IN 1 CARD READER (MMC)

30

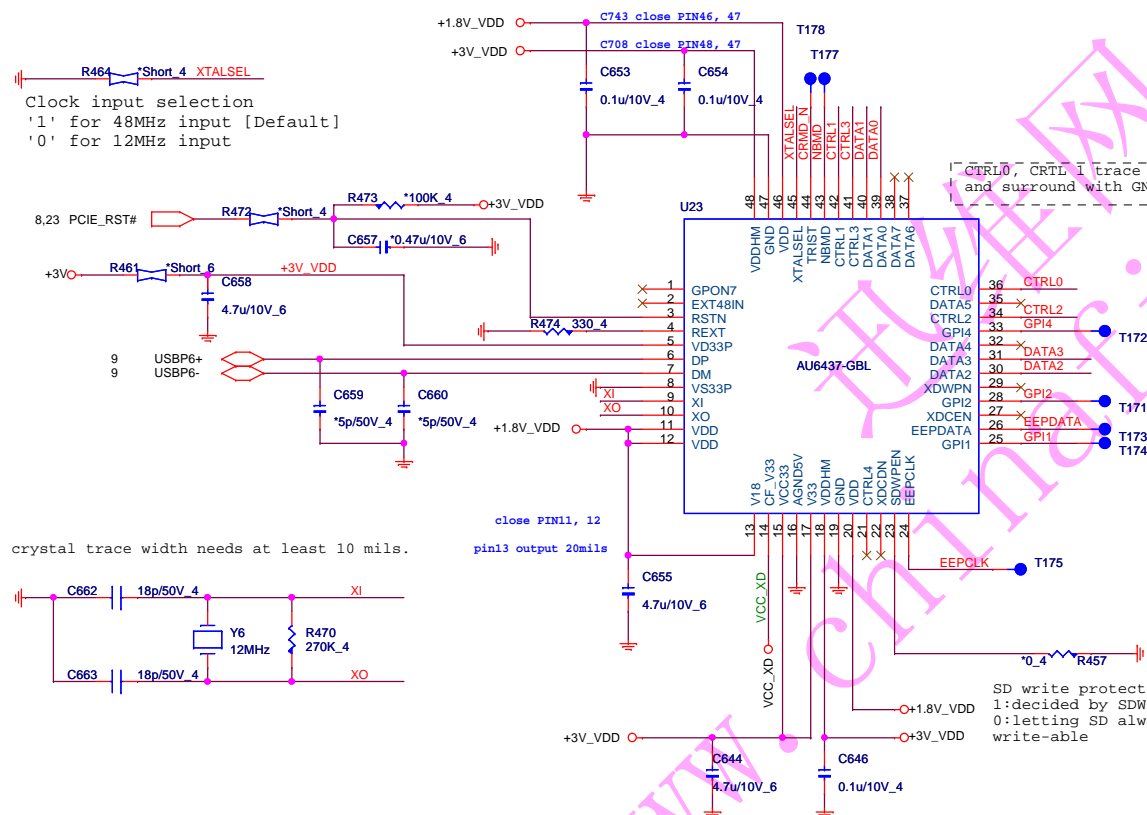


Main	DFHS11FR011
Second	DFHS11FR033

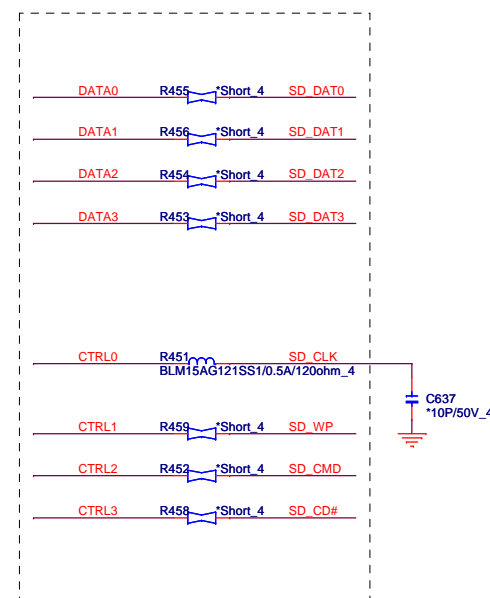


Close to CNxx pin 14 & pin23
4.7u CAP close to pin23

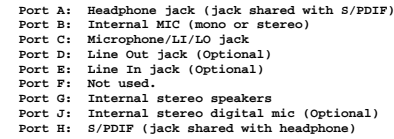
5/10 change Card Redaer conn
footpirnt sdcard-sdsn09-08-xa-11p-smt



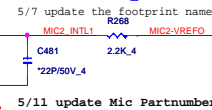
CTRL0, CTRL1 trace length shorter,
and surround with GND.



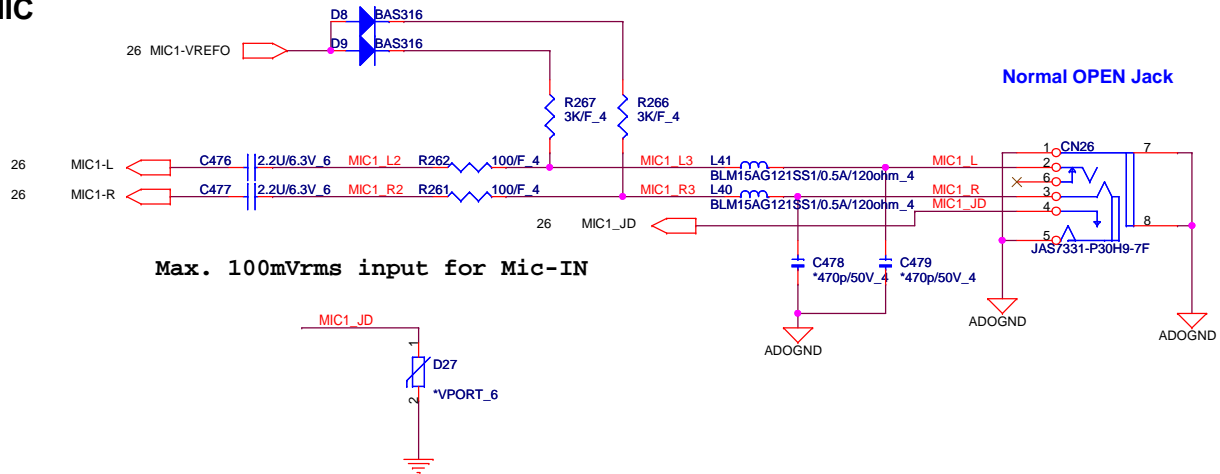
Codec(ADO)



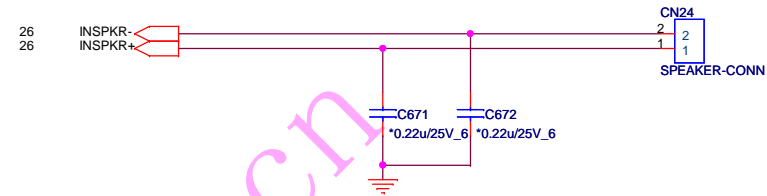
1. The VDD_{IO} and VAUX_{3.3} pins should be connected to same power supply domain as HDA bus controller so that the HDA controller and codec bus interface will power-up at the same time. This will avoid bus leakage issues if using HDA controller with bus pull-up strap options. See other FET option on this page if these supplies are not on same domain as HDA controller.
2. To support Wake-on-Jack, the codec VAUX_{3.3} pin must be powered from a Standby supply.
3. C309, C310, C311 are optional.
Do not install unless needed for EMI/SI.



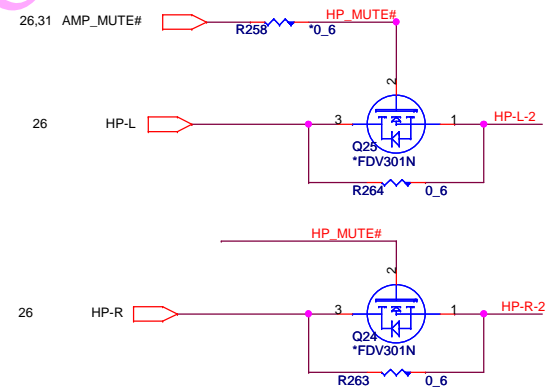
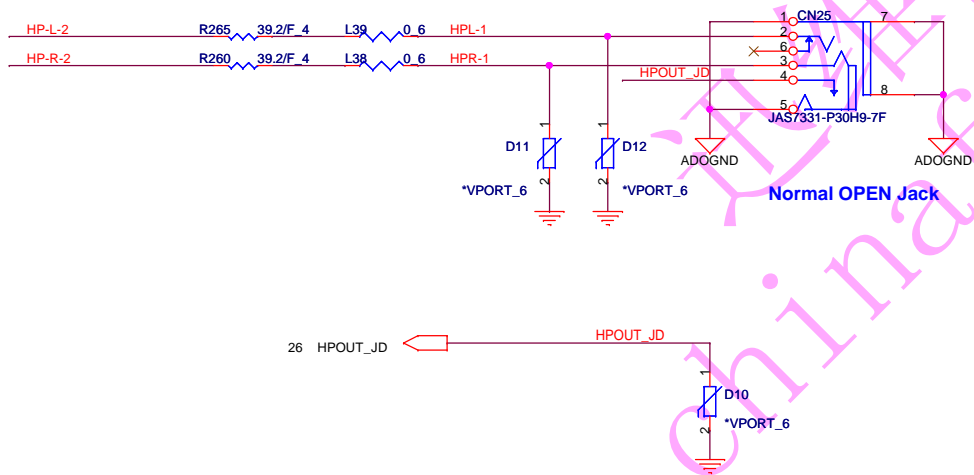
MIC



Internal Speaker



HP

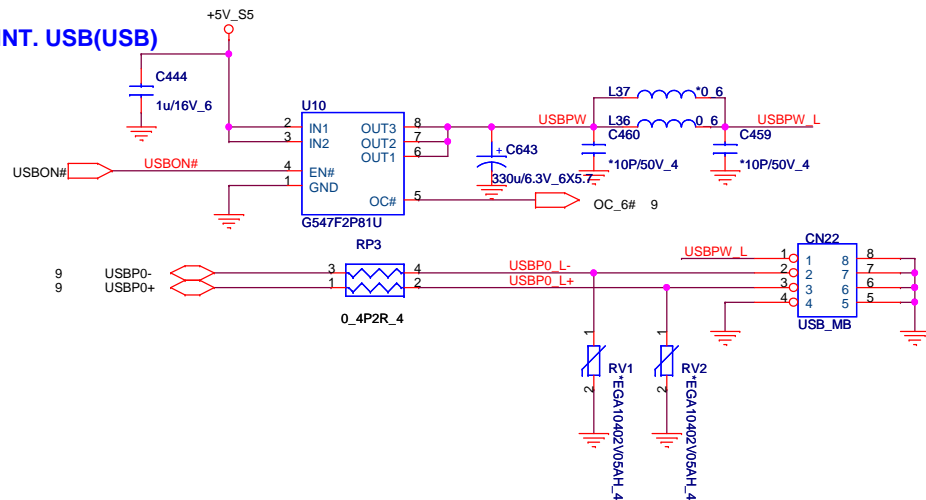


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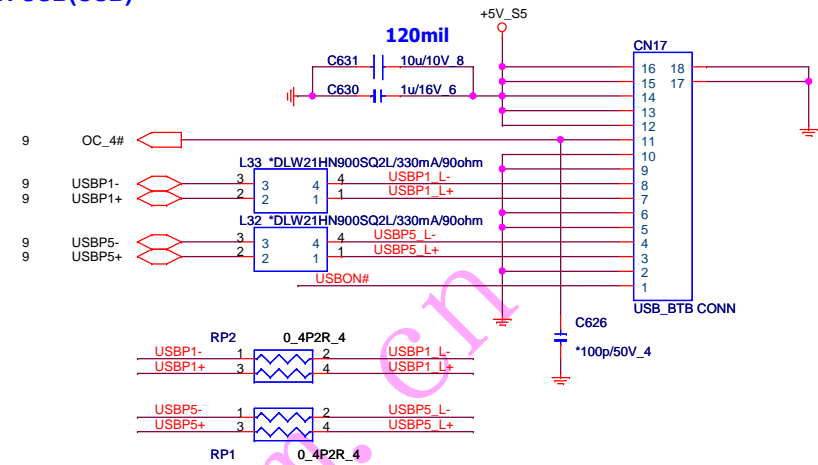
PROJECT : ZQG

Size	Document Number	Rev
	AUDIO JACK CONN	1A
Date:	Monday, November 01, 2010	Sheet 27 of 41

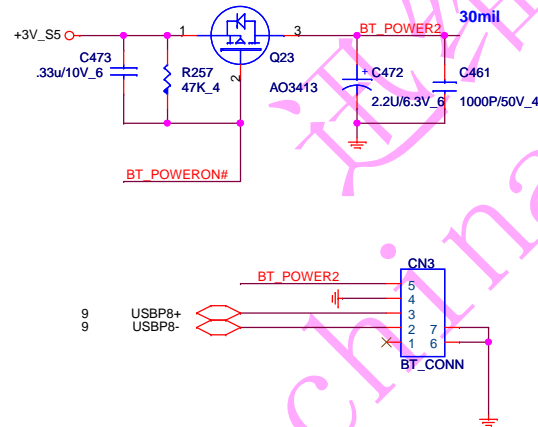
INT. USB(USB)



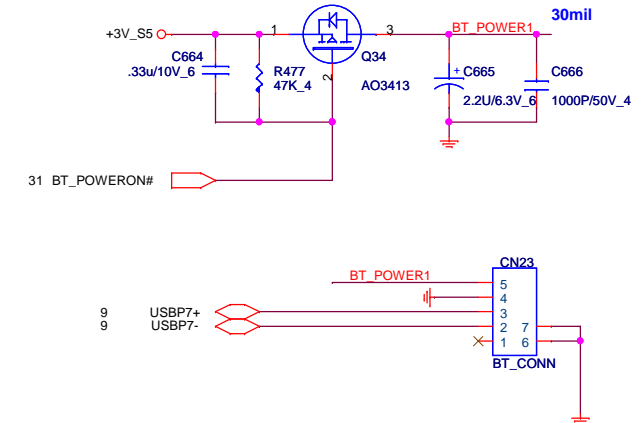
EXT. USB(USB)



BLUETOOTH V2.1 CONN(BTM)



BLUETOOTH V3.0 CONN(BTM)



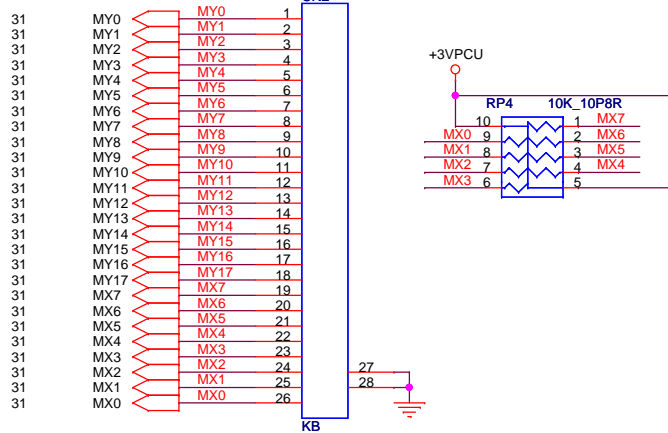
Quanta Computer Inc.

PROJECT : ZQG

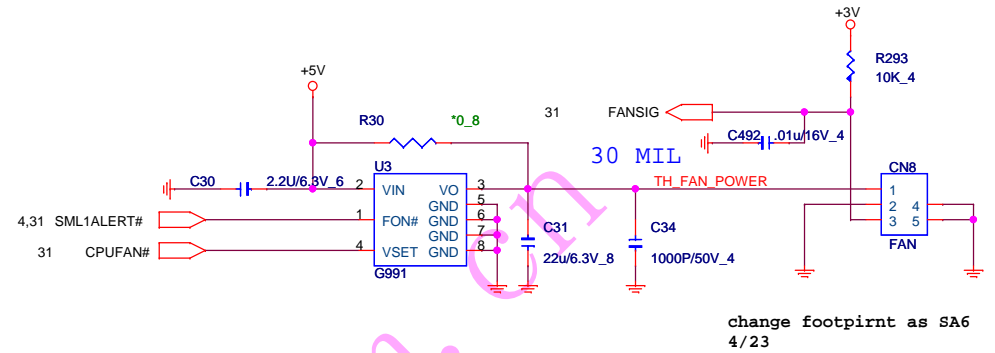
Size	Document Number	Rev
	USB/BT	1A

Date: Monday, November 01, 2010 Sheet 28 of 41

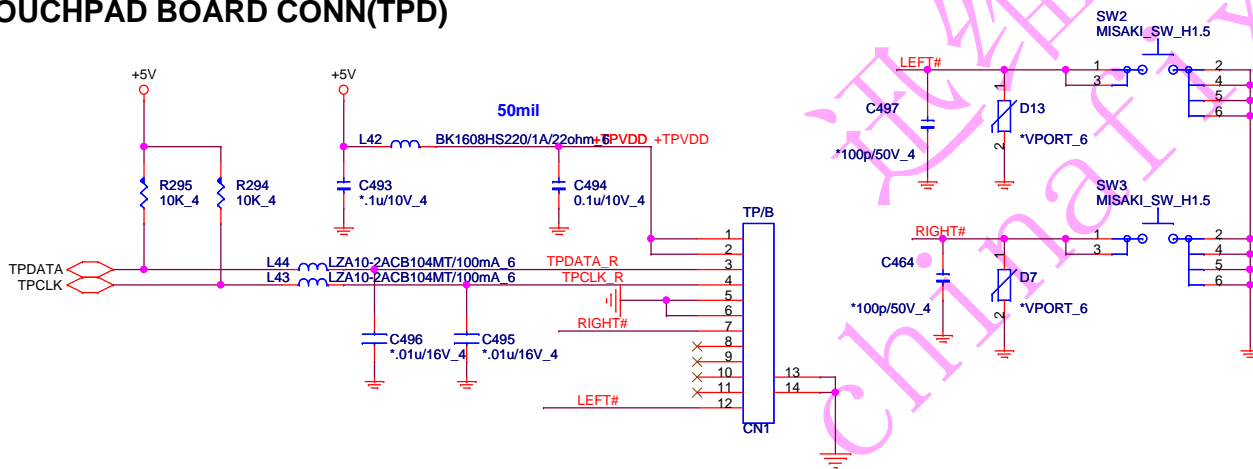
K/B(KBC)



CPU FAN(THM)

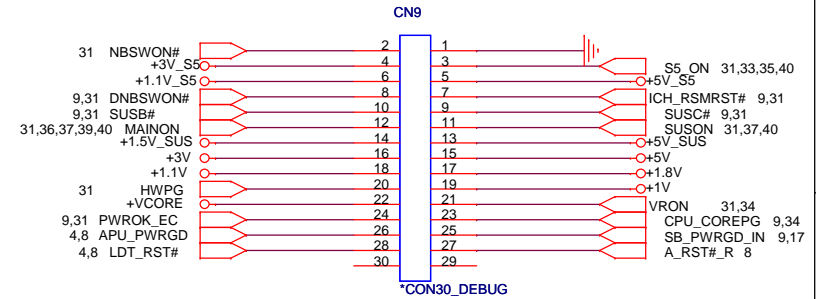


TOUCHPAD BOARD CONN(TPD)



Power Sequence

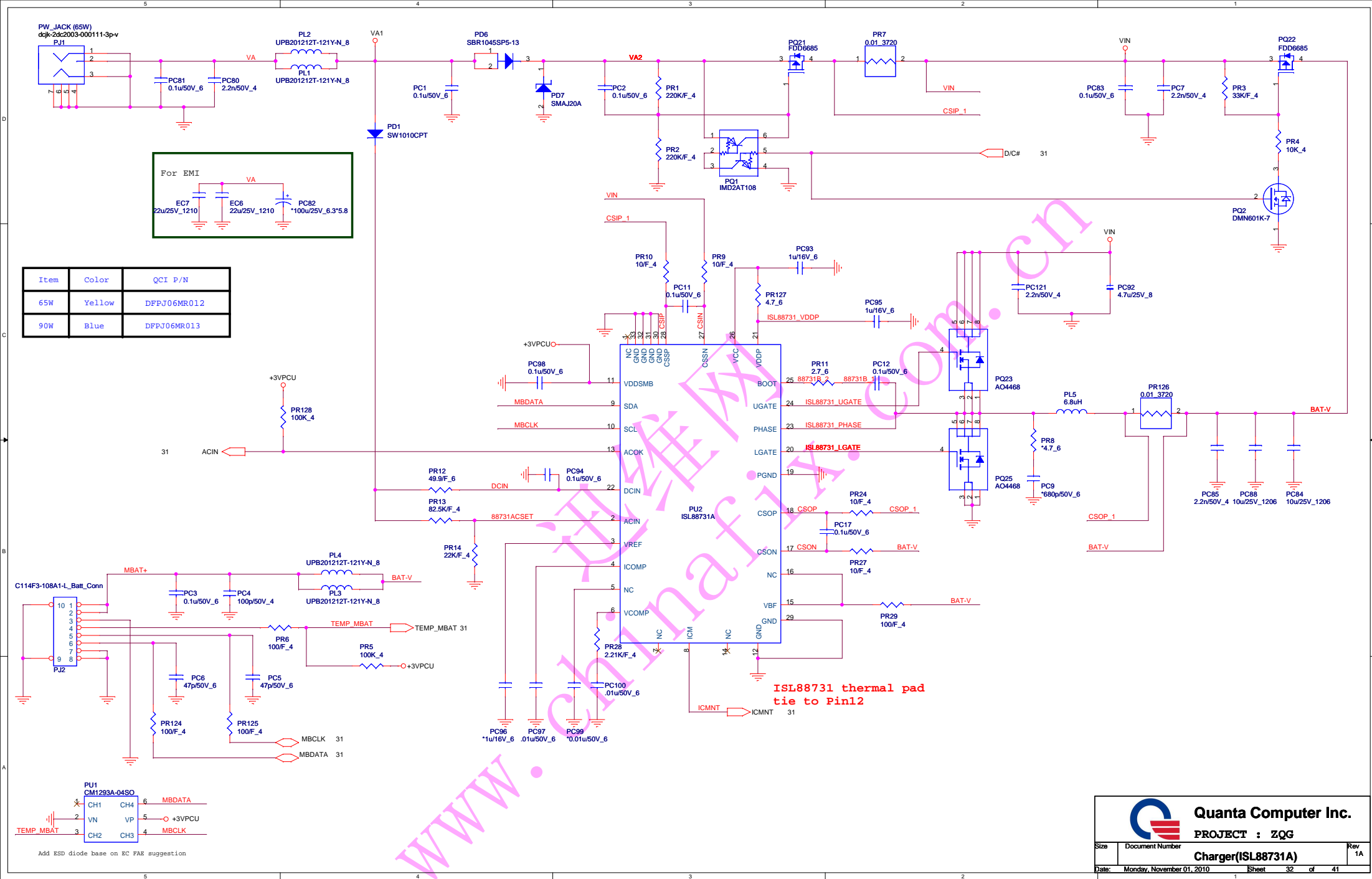
0903--Add Connecotr

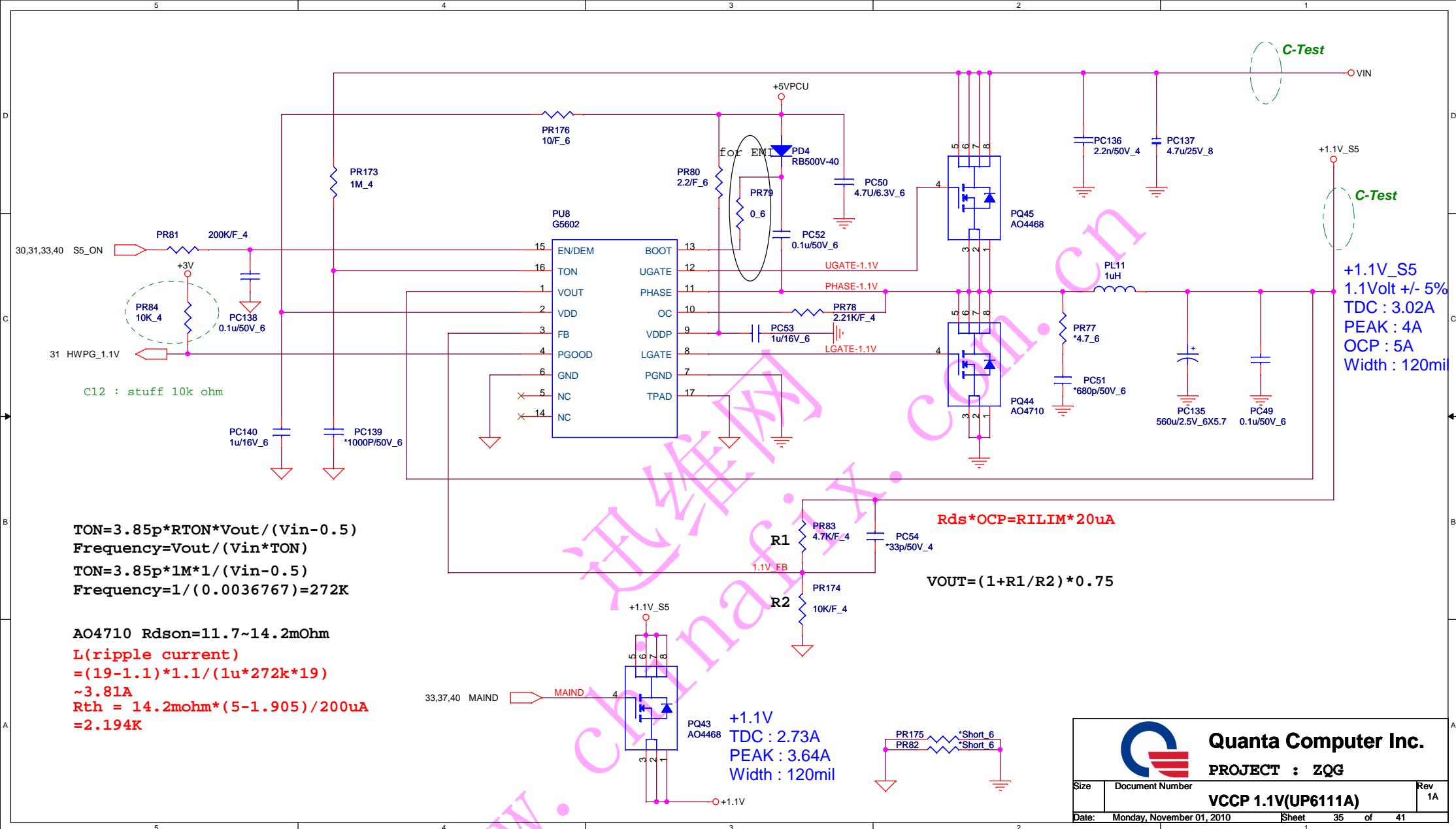


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PROJECT : ZQG

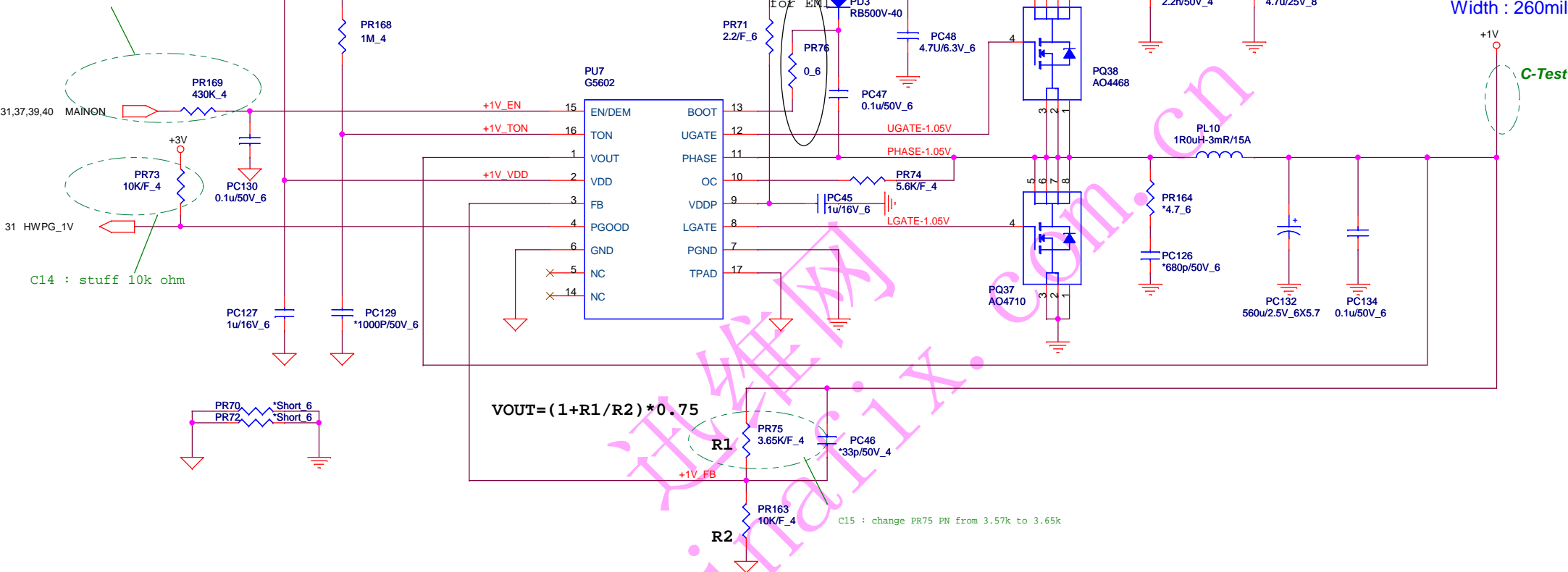
Size	Document Number	Rev
	30 -- KB/TP/FAN	1A
Date:	Monday, November 01, 2010	Sheet 30 of 41





C13

change PR169 PN from 0ohm to 430kohm for timing issue

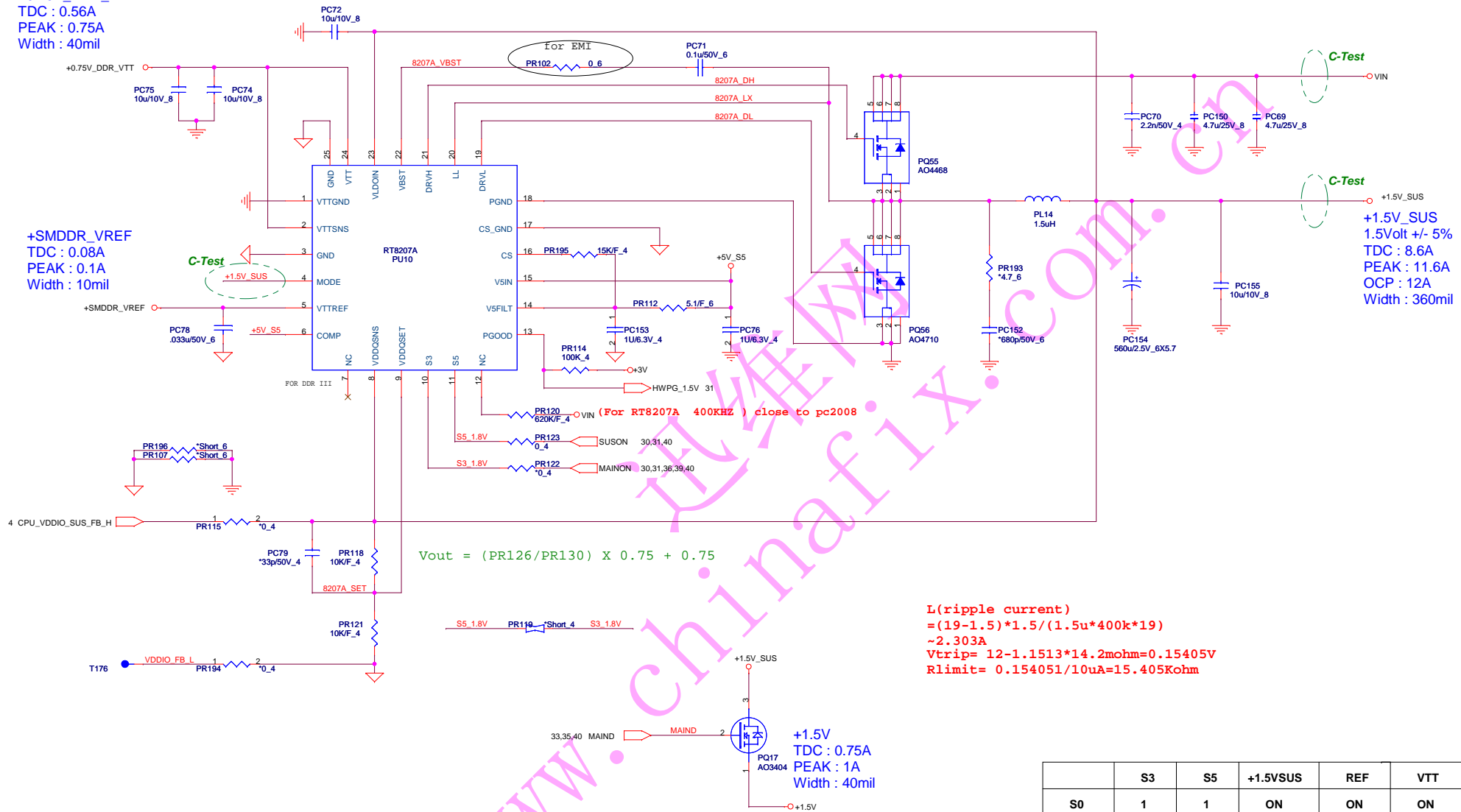


$$\begin{aligned} \text{TON} &= 3.85\text{p} \cdot \text{RTON} \cdot \text{Vout} / (\text{Vin} - 0.5) \\ \text{Frequency} &= \text{Vout} / (\text{Vin} \cdot \text{TON}) \\ \text{TON} &= 3.85\text{p} \cdot 1\text{M} \cdot 1 / (\text{Vin} - 0.5) \\ \text{Frequency} &= 1 / (0.0036767) = 272\text{K} \end{aligned}$$

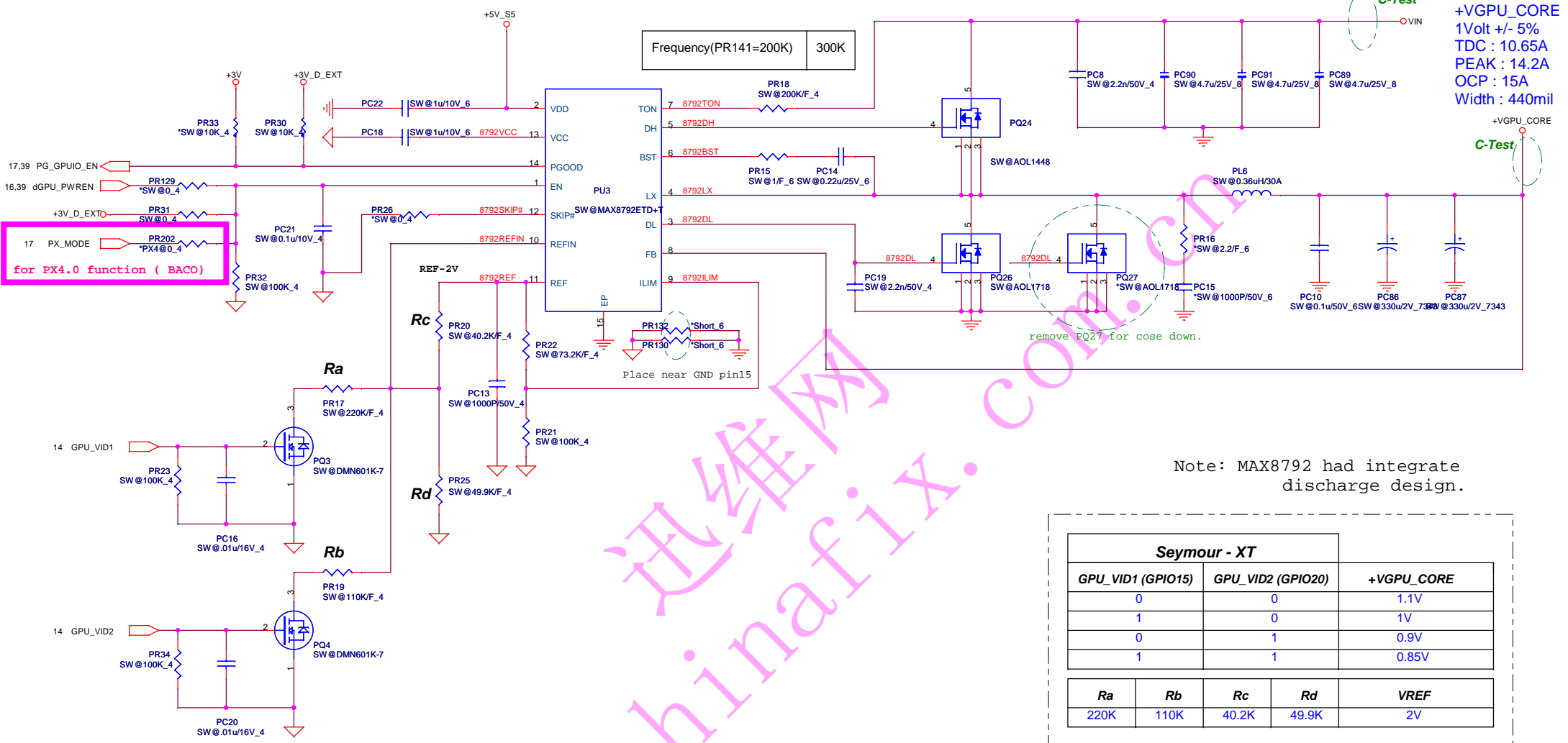
$$\begin{aligned} \text{AO4710 } R_{\text{dson}} &= 11.7 \sim 14.2\text{mOhm} \\ L(\text{ripple current}) &= (19 - 1) \cdot 1 / (1\text{u} \cdot 272\text{k} \cdot 19) \\ &\sim 3.483\text{A} \\ R_{\text{th}} &= 14.2\text{mohm} \cdot (10 - 1.741) / 20\text{uA} \\ &= 5.863\text{Kohm} \end{aligned}$$

+0.75V_DDR_VTT
TDC : 0.56A
PEAK : 0.75A
Width : 40mil

+SMDDR_VREF
TDC : 0.08A
PEAK : 0.1A
Width : 10mil



	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF




Note: MAX8792 had integrate discharge design.

Seymour - XT		
GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.1V
1	0	1V
0	1	0.9V
1	1	0.85V

Ra	Rb	Rc	Rd	VREF
220K	110K	40.2K	49.9K	2V

Ra --> 220K/F_4 (CS42202FB01) Rb --> 110K/F_4 (CS41102FB13)
Rc --> 40.2K/F_4 (CS34022FB15) Rd --> 49.9K/F_4 (CS34992FB10)

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PROJECT : ZQG

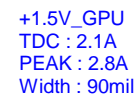
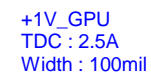
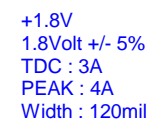
GPU CORE(MAX8792)

Size Document Number

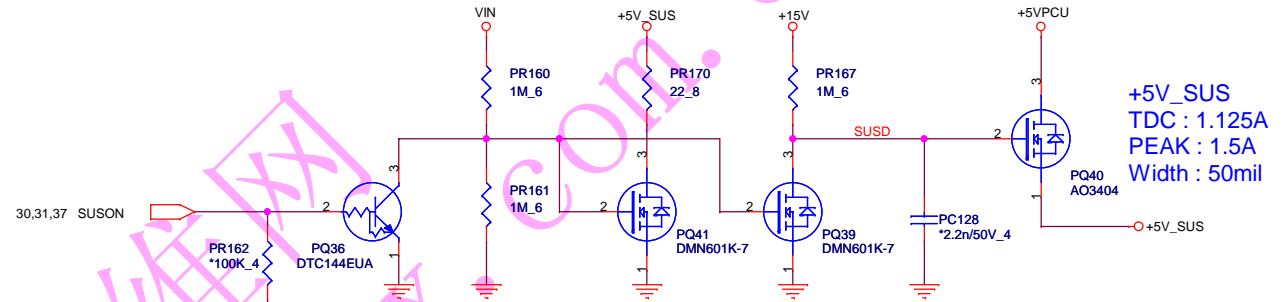
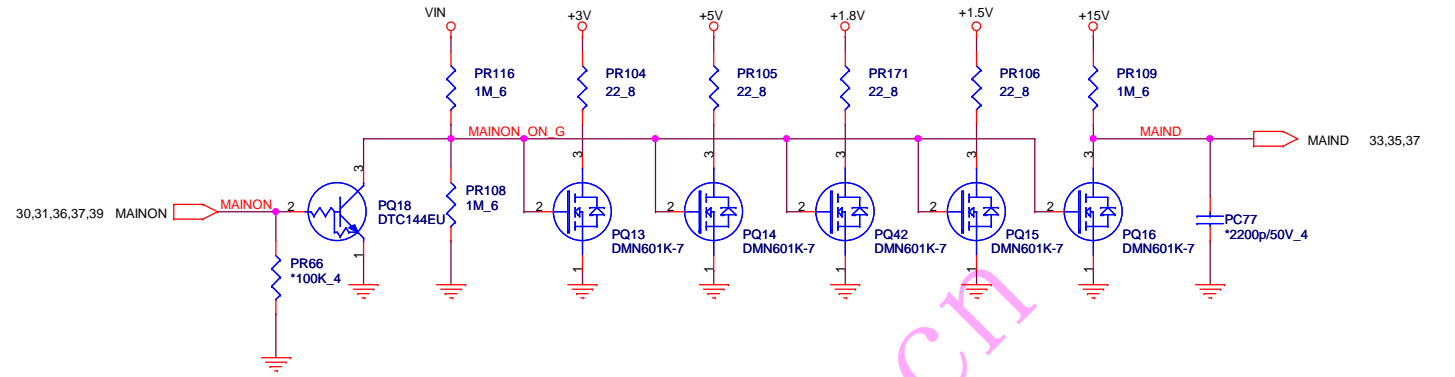
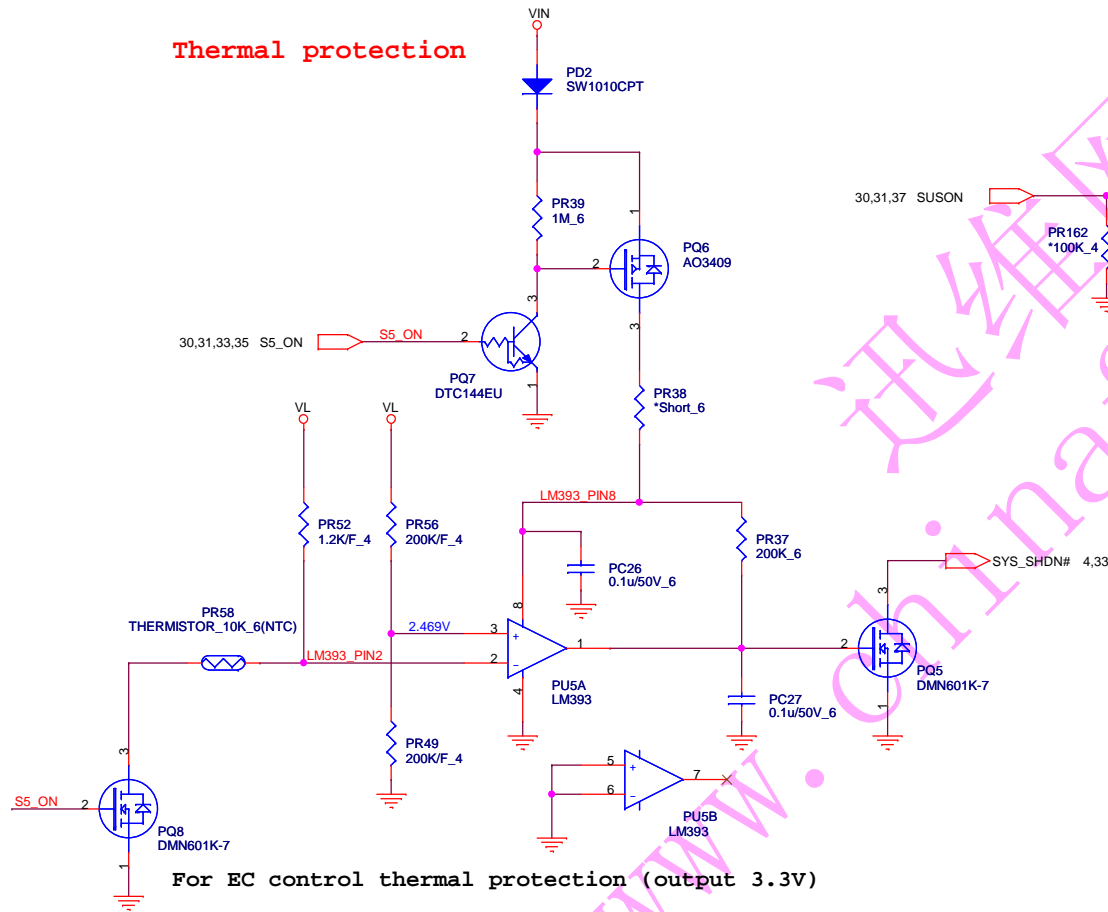
Date: Monday, November 01, 2010

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Rev 1A



Thermal protection




Quanta Computer Inc.

PROJECT : ZQG

Size	Document Number	Rev
		1A

Discharge /Thermal protection

Date: Monday, November 01, 2010 Sheet 40 of 41

MODEL	REV	CHANGE LIST	Model ZQE/G M/B BOARD		
			Page	From	To
ZQE/G M/B	3A	C01	1	1A	3A
		C02 PAGE18 : to slove the Power DVD issue , setting size to 256MB	2	1A	3A
		C03 PAGE39 : add PR210,PC157,PQ61,PR198,PR200,PR199,PQ60,PC156,PQ69 for GPU +1V power source .	3	1A	3A
		changed control net from HWPG_1V to PG_GPUIO_EN	4	1A	3A
		C04 PAGE13 : change the power source from +1V to +1V_GPU	5	1A	3A
		C05 PAGE14 : change the power source from +1V to +1V_GPU	6	1A	3A
		C06 PAGE16 : change the power source from +1V to +1V_GPU	7	1A	3A
		C07 PAGE17 : change the power source from +1V to +1V_GPU	8	1A	3A
		C08 PAGE18 : to solve the HDMI issue , remove R112,R118 from BOMs	9	1A	3A
		C09 PAGE21 : Del D26 to slove HDMI issue.	10	1A	3A
		C10 PAGE26 : net PCBEEP connects with U11 by 10k ohm for AC pulg in /out function.	11	1A	3A
		C11 PAGE31 : Both MXM_SMCLK12 / MXM_SMDATA12 should be pull up to +3V by 10k ohm.	12	1A	3A
		C12 PAGE35 : stuff 10k ohm	13	1A	3A
		C13 PAGE36 : change PR169 PN from 0 ohm to 430K ohm for timing issue.	14	1A	3A
		C14 PAGE36 : stuff 10k ohm	15	1A	3A
		C15 PAGE36 : change PR75 PN from 3.57k to 3.65k	16	1A	3A
		C16 PAGE38 : remove PQ27 for cose down.	17	1A	3A
		C17 PAGE38 : remove PQ27 for cose down.	18	1A	3A
		C18 PAGE5 : Add C674 to reduce CRT noise.	19	1A	3A
		C19 PAGE5 : del R100 , add L58 to reduce CRT noise.	20	1A	3A
			21	1A	3A
			22	1A	3A
			23	1A	3A
			24	1A	3A
			25	1A	3A
			26	1A	3A
			27	1A	3A
			28	1A	3A
			29	1A	3A
			30	1A	3A
			31	1A	3A
			32	1A	3A
			33	1A	3A
			34	1A	3A
			35	1A	3A
			36	1A	3A
			37	1A	3A
			38	1A	3A
			39	1A	3A
			40	1A	3A
			41	1A	3A
Note : 1. Remove Jumper : JP7,JP11,JP1,JP2,JP3,JP4,JP5,JP6,JP8,JP9,JP10,JP12,JP13,JP14,JP15,JP16,JP17,JP18			<div><div></div><div><div>Quanta Computer Inc.</div><div>PROJECT : ZQG</div><div>CHANGE LIST - 3A</div><div>Size Document Number Rev 1A</div><div>Date: Monday, November 01, 2010 Sheet 41 of 41</div></div></div>		
Quanta Computer Inc. ZQE/G		PROJECT: ZQE/G	PCBA NO.	REV: 3A	DOC. NO :
		APPROVED BY : Johnny O	CHECK BY : Darren Liao	DRAWING BY : Kenneth Huang	DATE :10/18/2010
		SHEET 1			