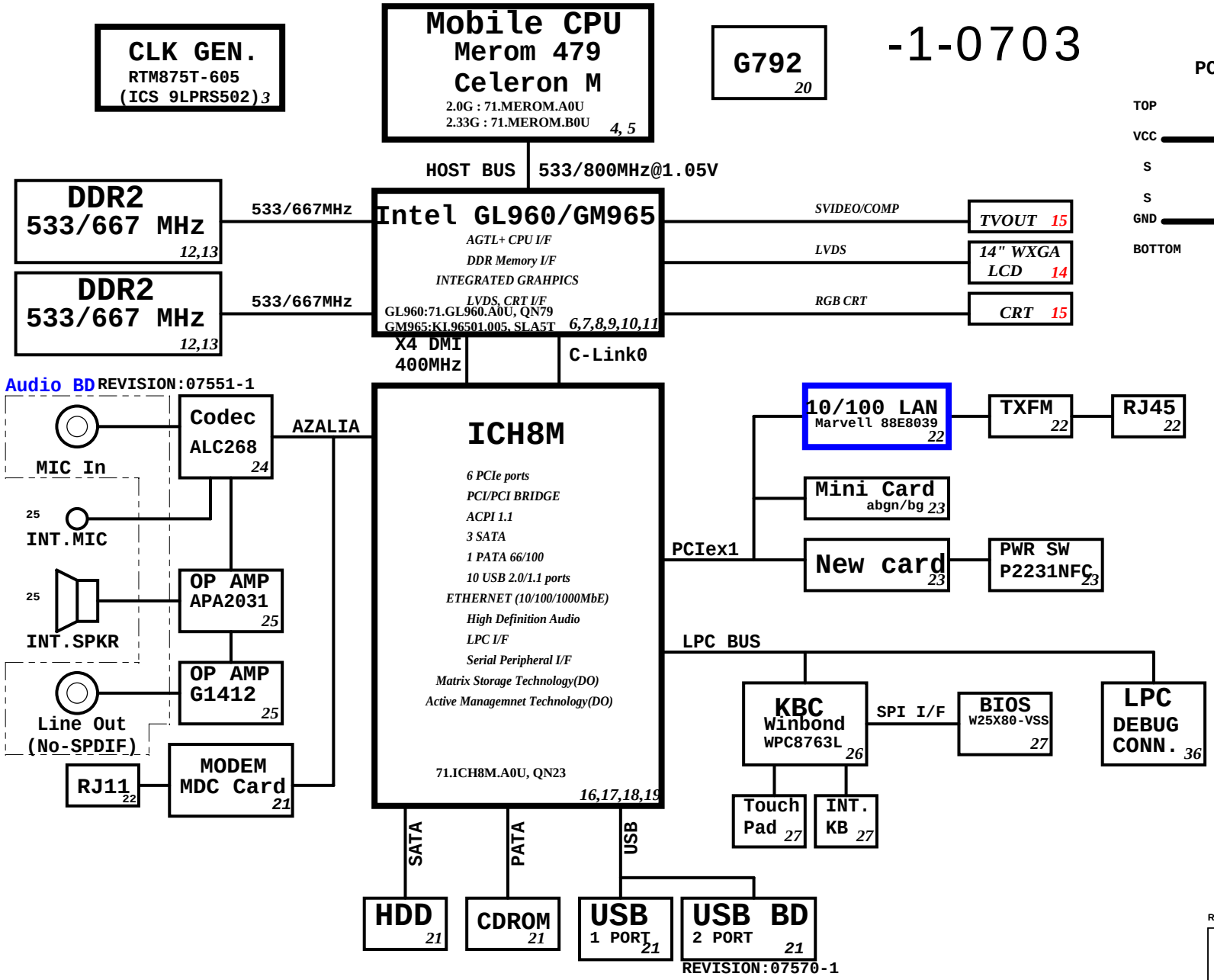
Volvi2 Block Diagram

Project code: 91.4X101.001
PCB P/N : 48.4X101.011
REVISION : 07220-1

-1-0703



PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC MAX8744 31	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(6A)

SYSTEM DC/DC TPS51124 32	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(8A) 1D8V_S3(12A)
TPS51100(G2997) 33	
1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3
APL5913 33	
1D8V_S3	1D25V_S0 (1.5A)
G909 28	
5V_AUX_S5	3D3V_AUX_S5 (100mA)
APL5915 33	
1D8V_S3	1D5V_S0 (1.5A)

CHARGER MAX8731 34	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC MAX8770 30	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

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Title: BLOCK DIAGRAM

Size: A3 | Document Number: Volvi2 | Rev: -1

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ICH8M Functional Strap Definitions

ICH8-M EDS 21762 2.0V1 page 16

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

PCIE Routing

LANE1	LAN Marvell
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	NC
4	USB3
5	NC
6	NC
7	MINICARD
8	CCD
9	NEW1

ICH8M Integrated Pull-up and Pull-down Resistors

ICH8-M EDS 21762 2.0V1

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K ?
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K ?
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Crestline Strapping Signals and Configuration

Crestline EDS 20954 1.0 page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode **1 = Low Power mode** (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO Card present** (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWORK in signal.

History

2007/05/02
1 Based on Tahoe to modify schematics.
==========
2007/05/14
1.Page 34:Replace "D25" with "BAS16-1-GP".
2.Page 27:Replace "R485" with "2K7R2j".
3.Page 27:DY:C379"
4.Page 27:Add "C682" D1u capacitor on "LID1.PIN1"
5.Page 27:Replace "R238" with "0R2".
6.Page 25:Replace "INTMIC1" & "SPKR1" with main source follow connector list.
7.Page 5:Add C115, C116, C141, C149, C169, C171 for Colay with TC25.
8.Page 10:Replace "L20" with "68.00217.141".
9.Page 10:Replace "L10" & "L23" with "68.00217.101"
==========

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Title: Reference
Size: A3 | Document Number: Volvi2 | Rev: -1
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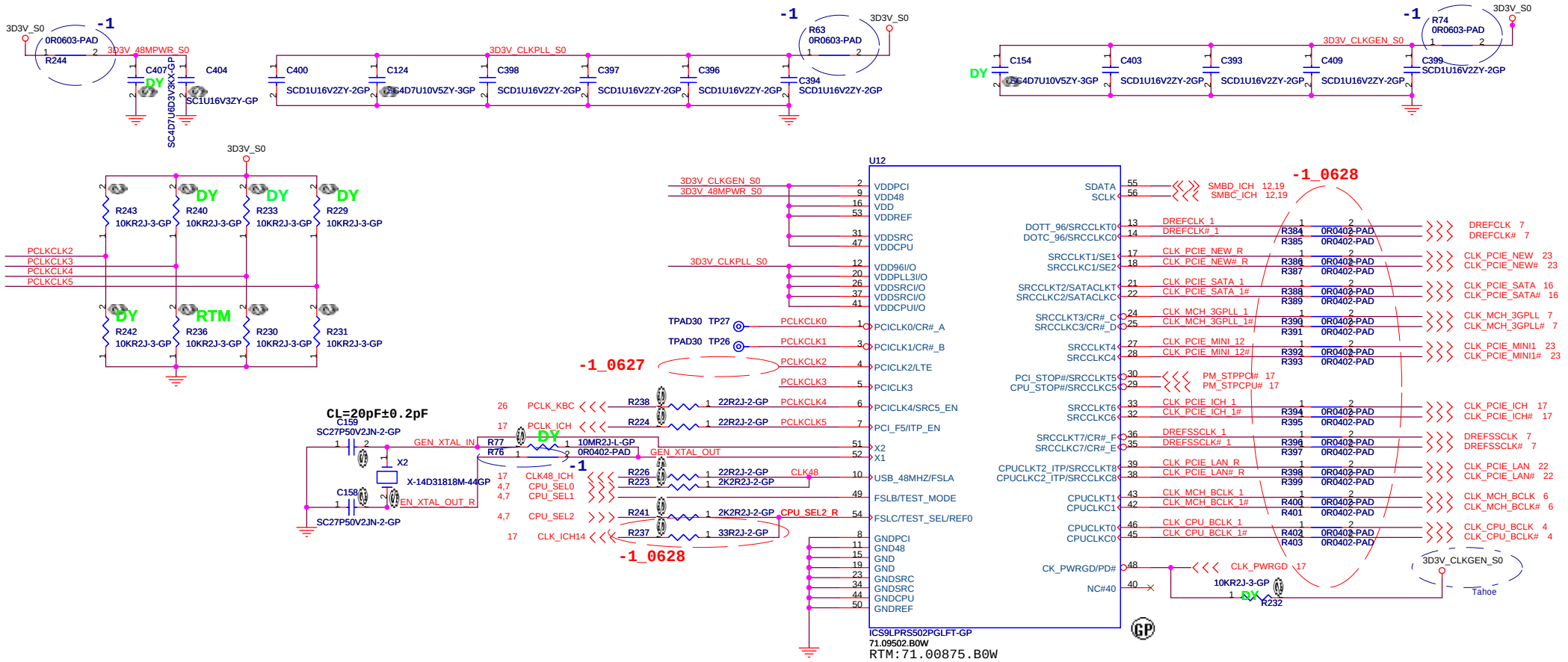

ICS9LPR502HGLFT-GP setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pai Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pai Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI4/SRC5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

RTM875T-605 setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pai Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pai Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/SRC-5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

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Title: Clock Generator

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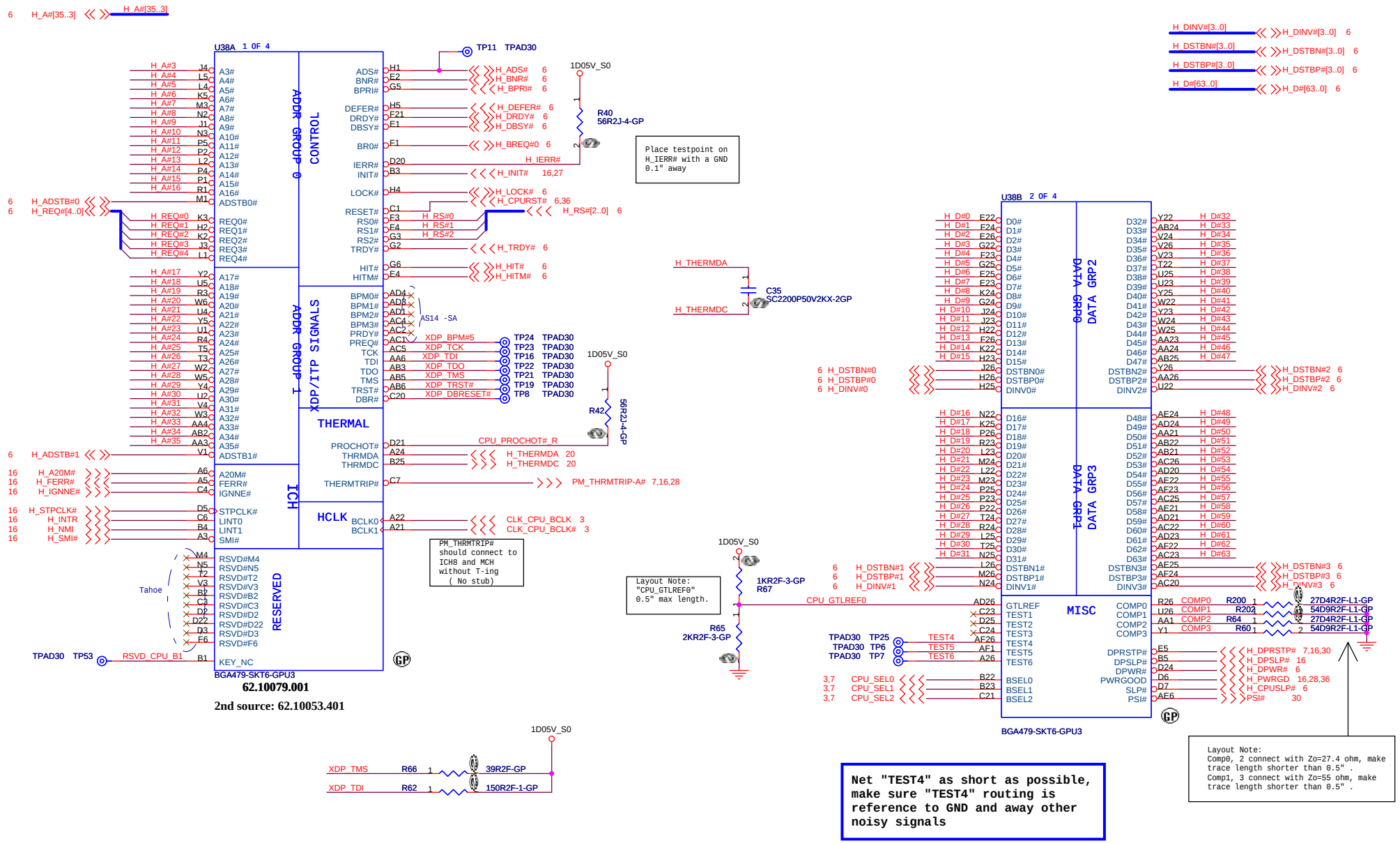

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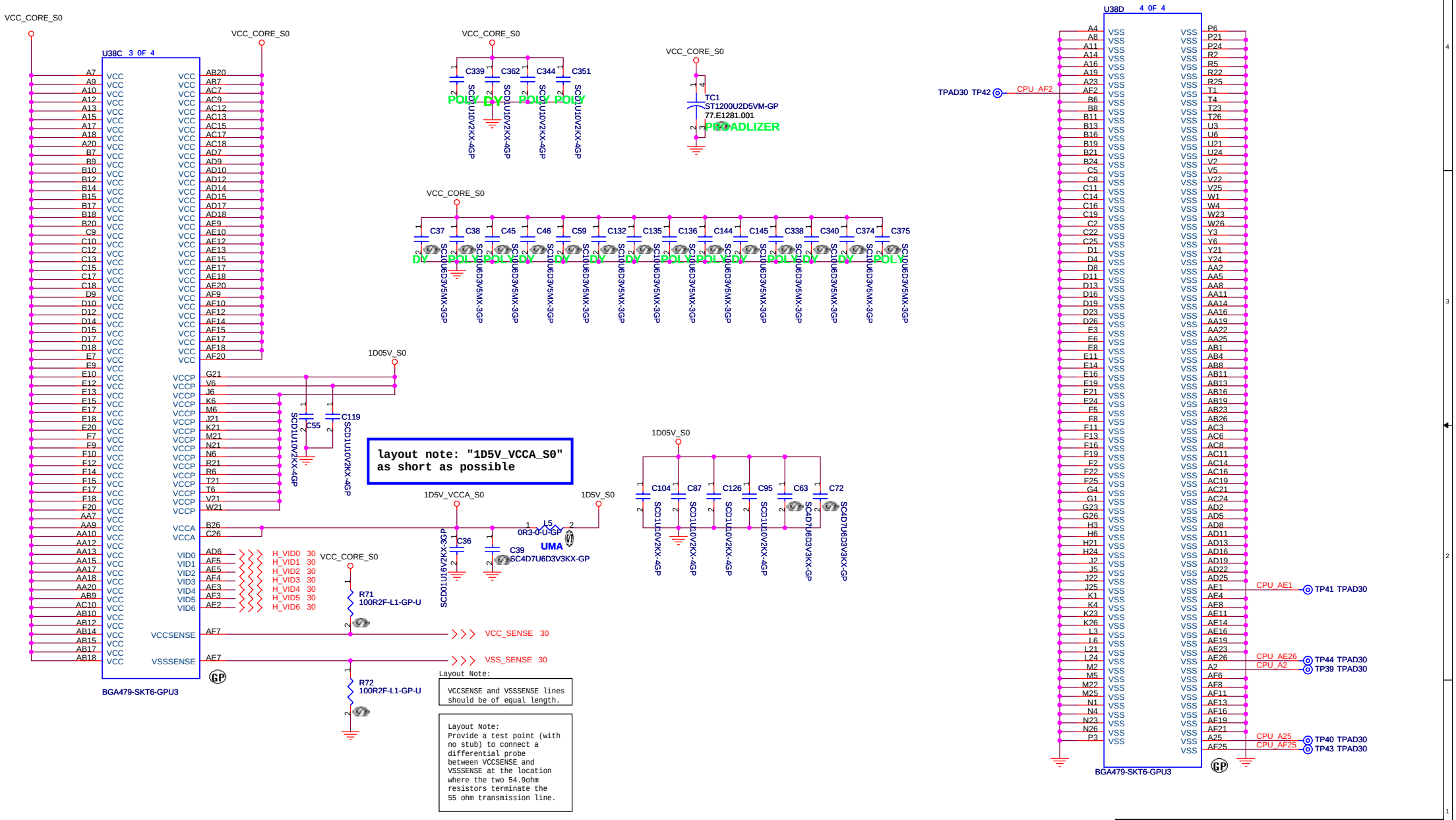
Title: *CPU (1 of 2)*

Size | Document Number: Volvi2 | Rev: SA

Date: Thursday, July 05, 2007 | Sheet 4 of 36



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Title	***CPU (2 of 2)***	
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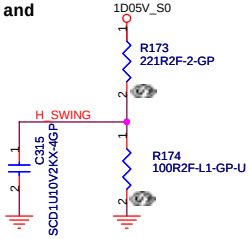
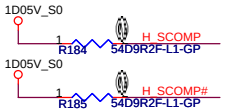
H_SWING routing Trace width and Spacing use 10 / 20 mil

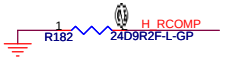
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil (MAX)

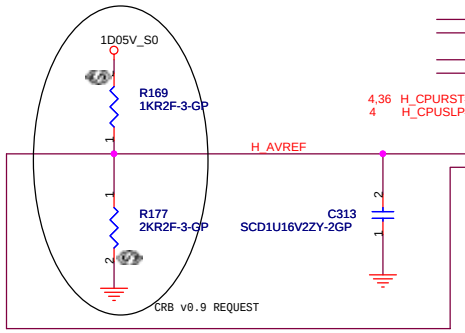


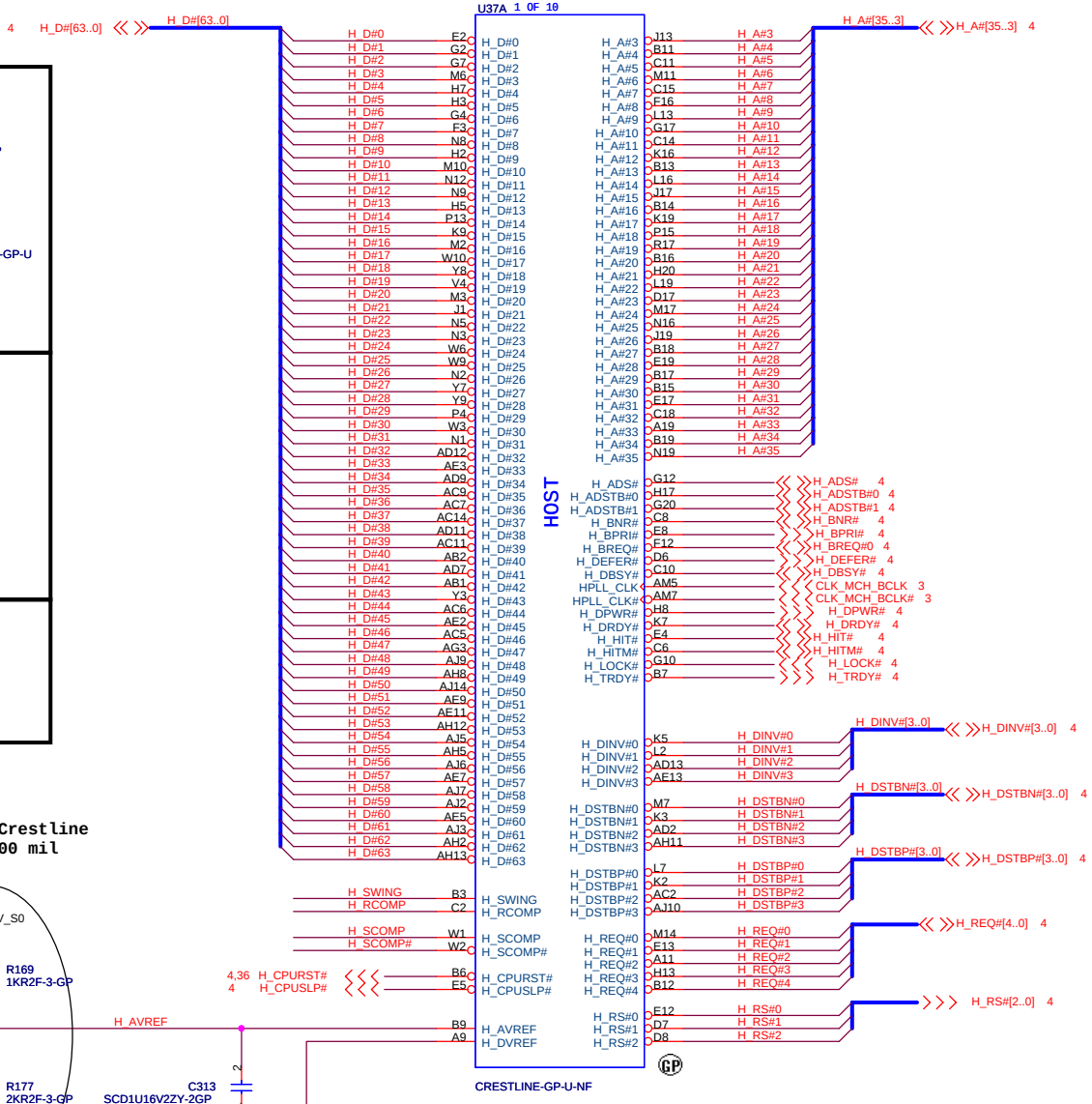
H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")

H_REF Decoupling Crestline close Crestline 100 mil





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Title	GMCH (1 of 6)	
Size	Document Number: Volvi2	Rev: SA
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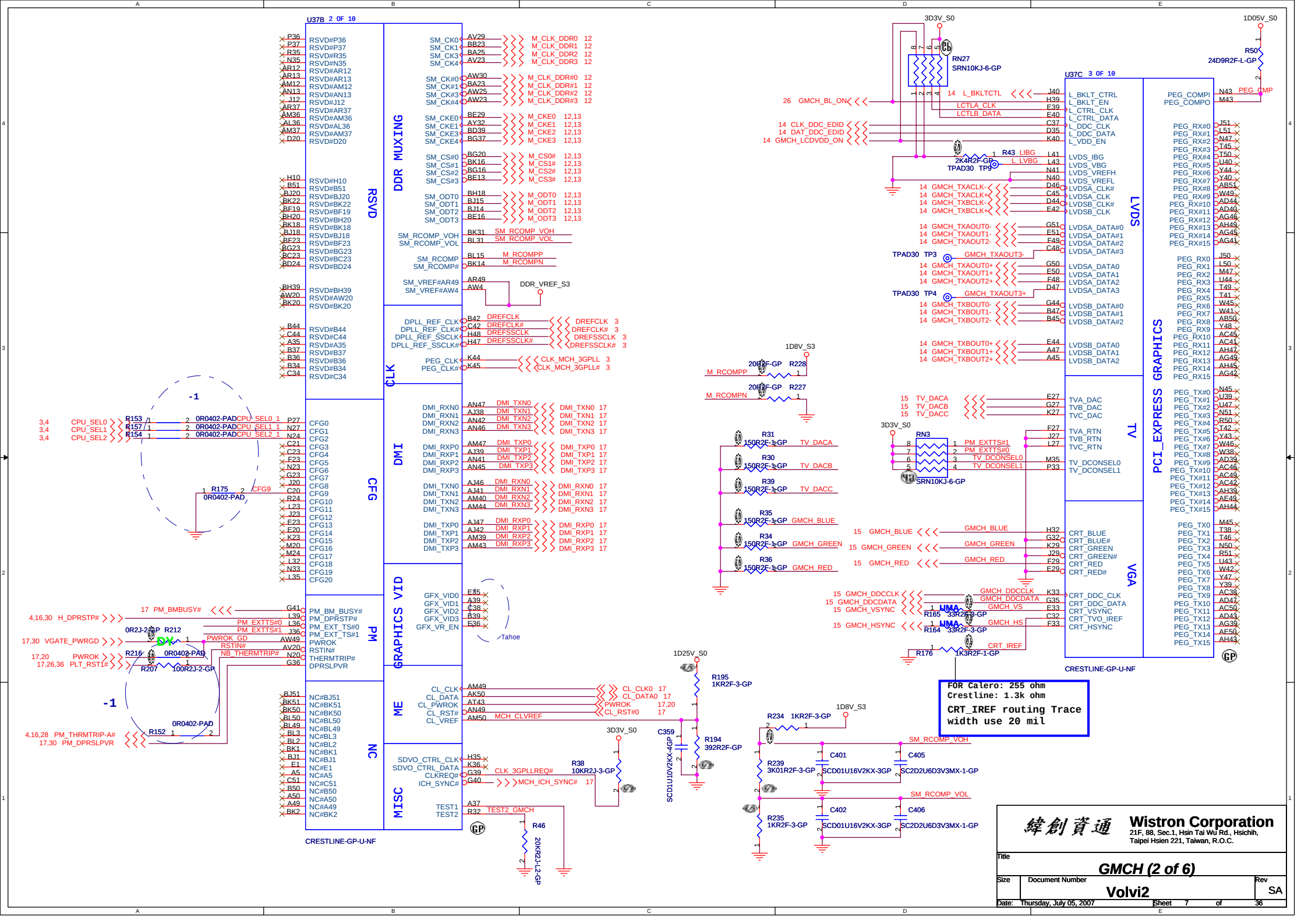
U37B 2 OF 10
RSVD
DDR MUXING
CLK
CFG
DMI
PM
GRAPHICS VID
ME
NC
MISC
CRESTLINE-GP-U-NF
U37C 3 OF 10
LVDS
TV
VGA
PCI_EXPRESS GRAPHICS
CRESTLINE-GP-U-NF
FOR Calero: 255 ohm
Crestline: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
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Title
GMCH (2 of 6)
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Title	***GMCH (3 of 6)***	
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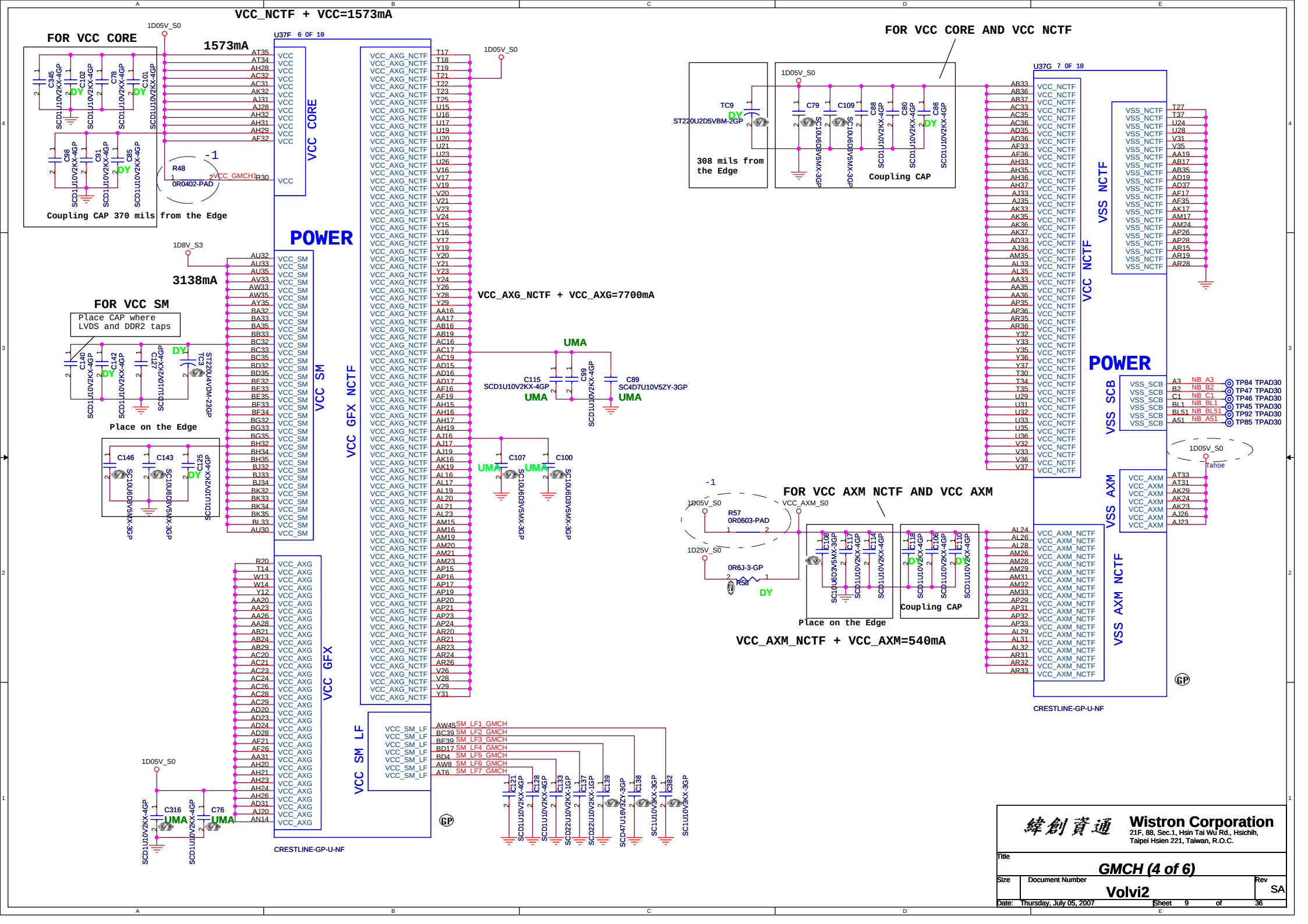
VCC_NCTF + VCC=1573mA
FOR VCC CORE
1D05V_S0
1573mA
U37F 6 OF 10
VCC CORE
Coupling CAP 370 mils from the Edge
R48
0R0402-PAD
VCC_GMCH1
POWER
1D8V_S3
3138mA
FOR VCC SM
Place CAP where LVDS and DDR2 taps
Place on the Edge
VCC SM
VCC GFX NCTF
VCC_AXG_NCTF + VCC_AXG=7700mA
UMA
VCC GFX
VCC SM LF
CRESTLINE-GP-U-NF
FOR VCC CORE AND VCC NCTF
308 mils from the Edge
Coupling CAP
U37G 7 OF 10
VCC NCTF
VSS NCTF
VSS SCB
VSS AXM
VSS AXM NCTF
FOR VCC AXM NCTF AND VCC AXM
R57
0R0603-PAD
R58
0R6J-3-GP
VCC_AXM_NCTF + VCC_AXM=540mA
Tahoe
CRESTLINE-GP-U-NF
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Title
GMCH (4 of 6)
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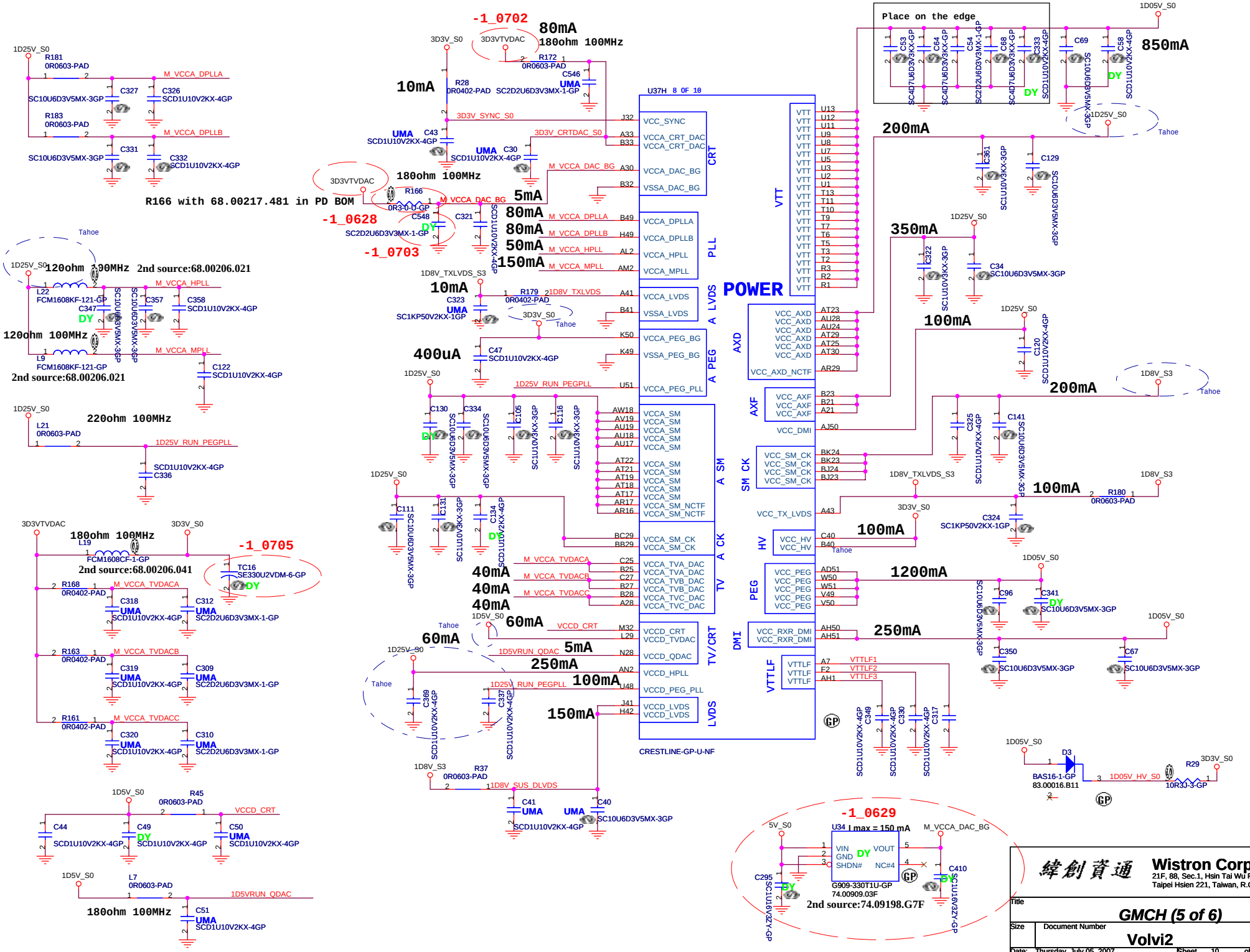
POWER
U37H 8 OF 10
CRESTLINE-GP-U-NF
Place on the edge
R166 with 68.00217.481 in PD BOM
-1_0702
-1_0628
-1_0703
-1_0705
-1_0629
2nd source:68.00206.021
2nd source:68.00206.041
2nd source:74.09198.G7F
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Title
GMCH (5 of 6)
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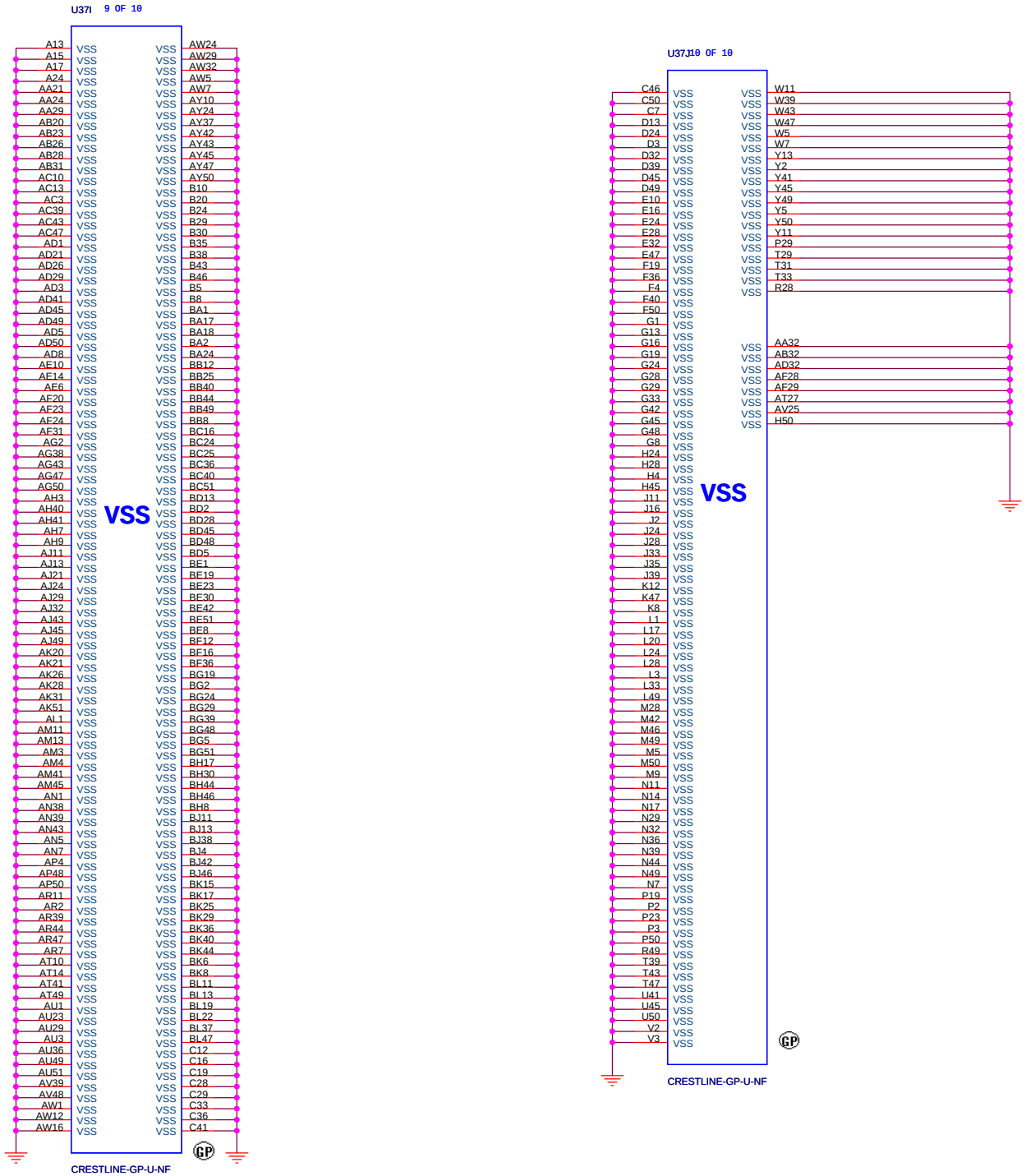

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Title	***GMCH (6 of 6)***
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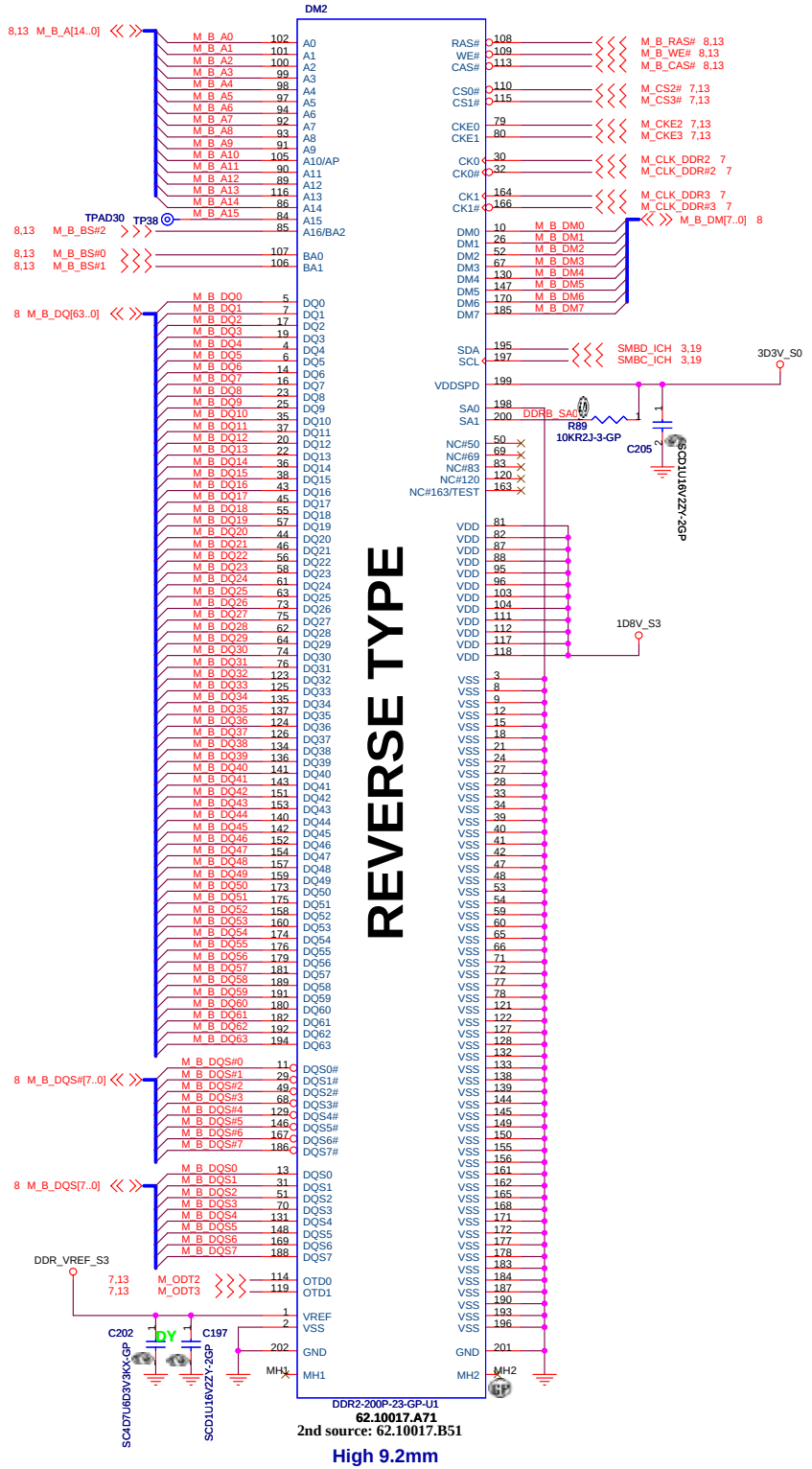

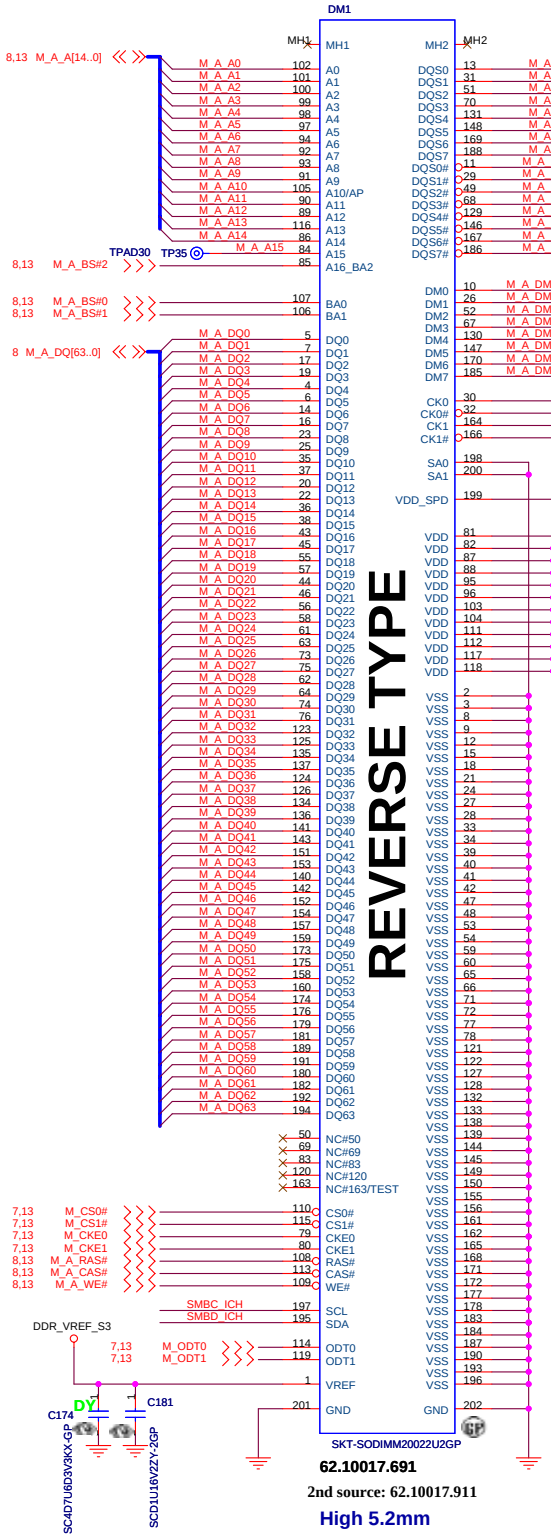

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Title	***DDR2 Socket***	
Size	Document Number **Volvi2**	Rev SA
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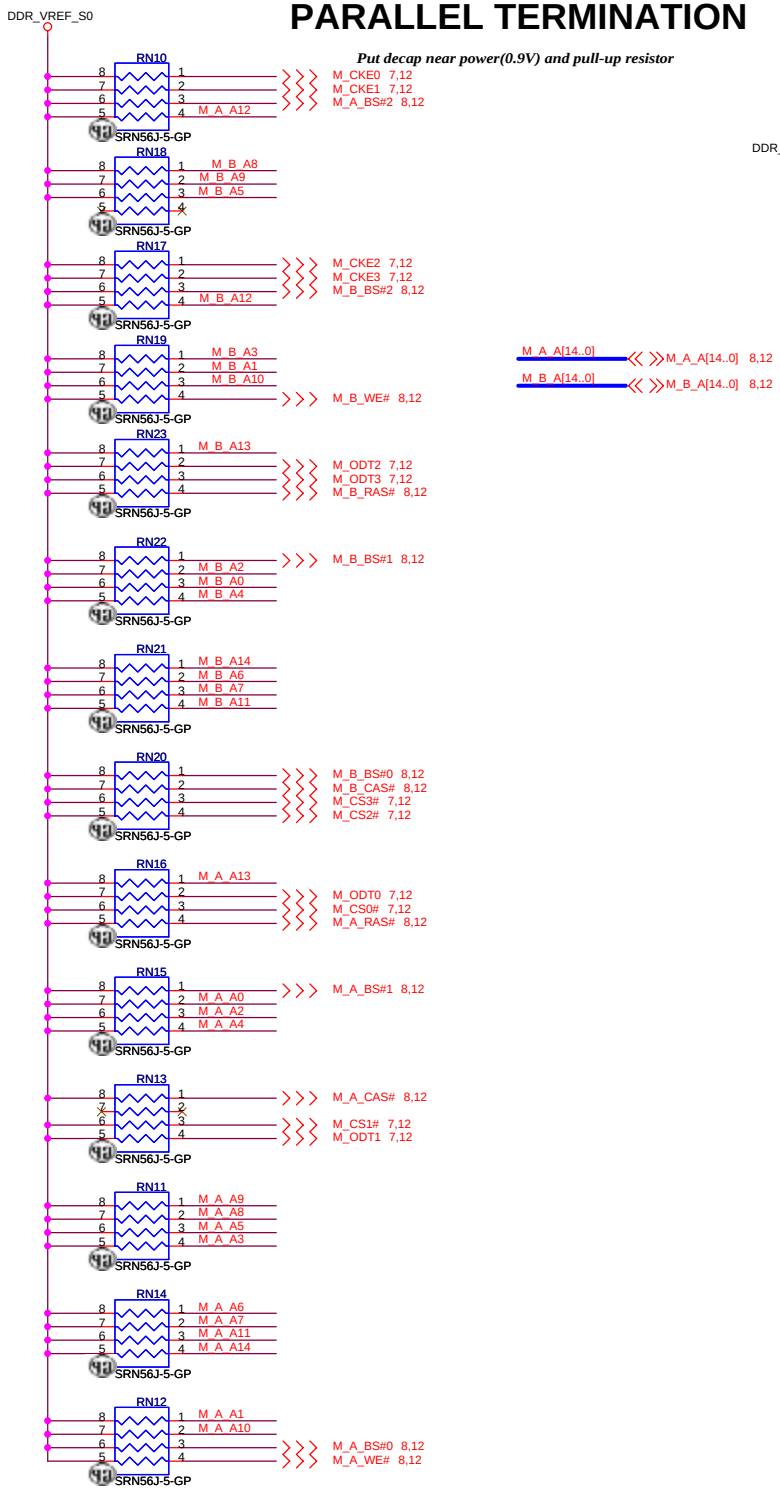
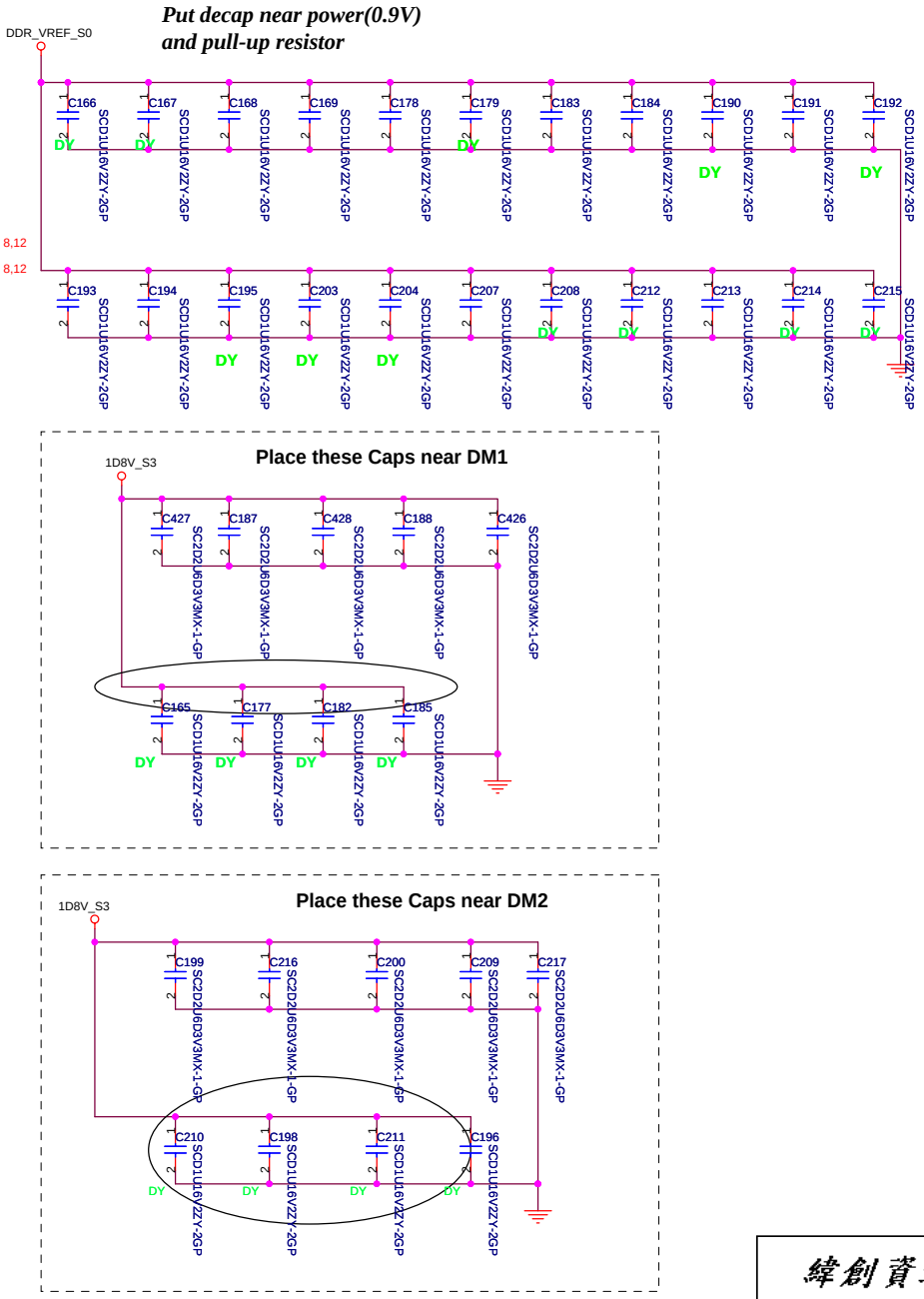
PARALLEL TERMINATION



M_A_A[14..0] — M_A_A[14..0] 8,12

M_B_A[14..0] — M_B_A[14..0] 8,12

Decoupling Capacitor



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Title	***DDR2 Termination Resistor***
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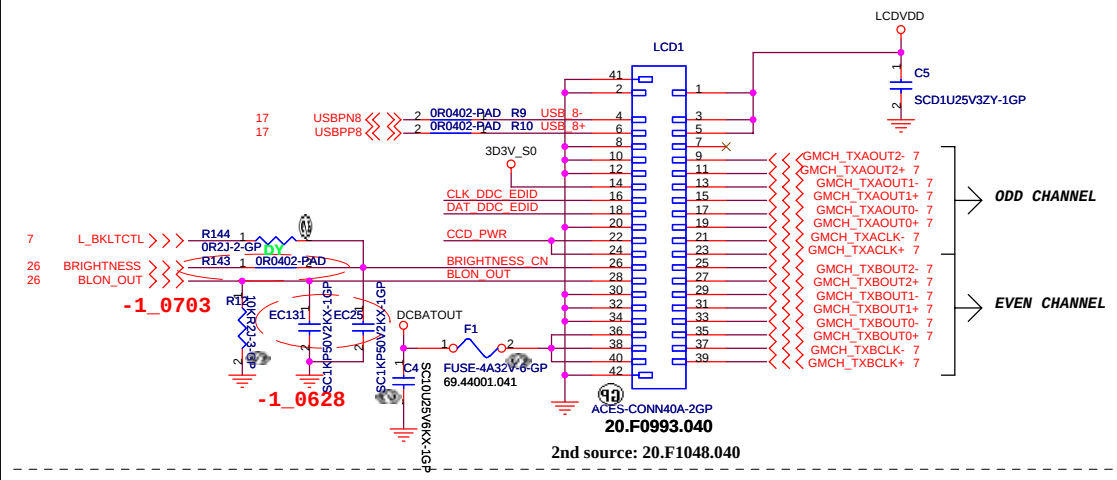
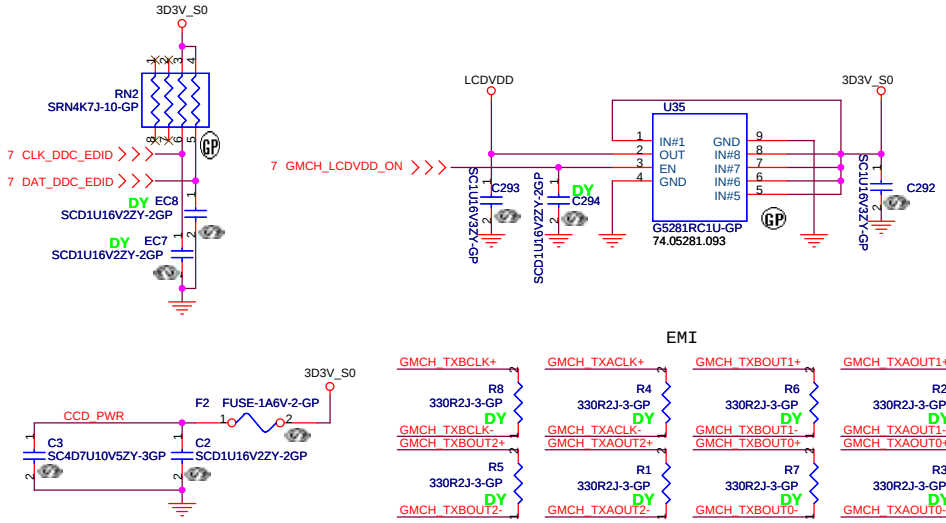
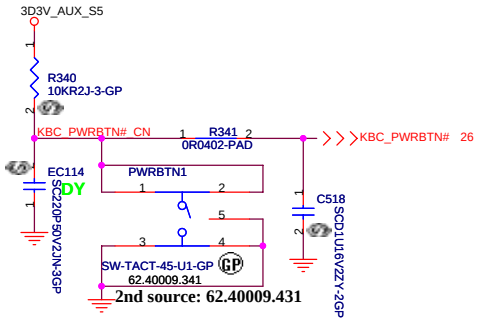
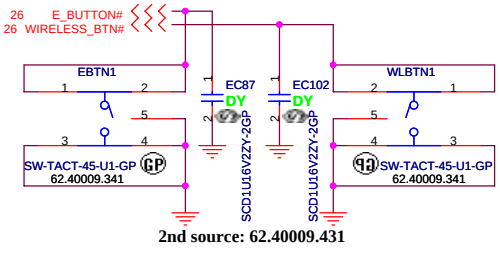
LCD/INVERTER CONN



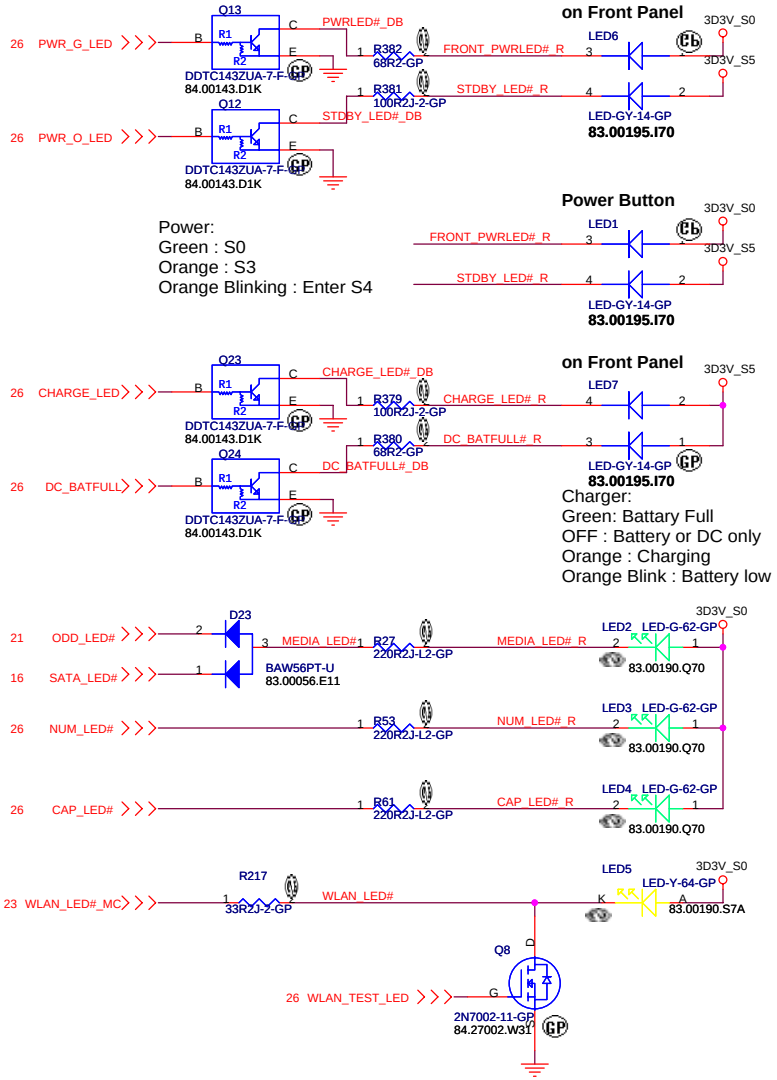


Buttons





LED



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Title	LCD CONN & LED & Buttons	
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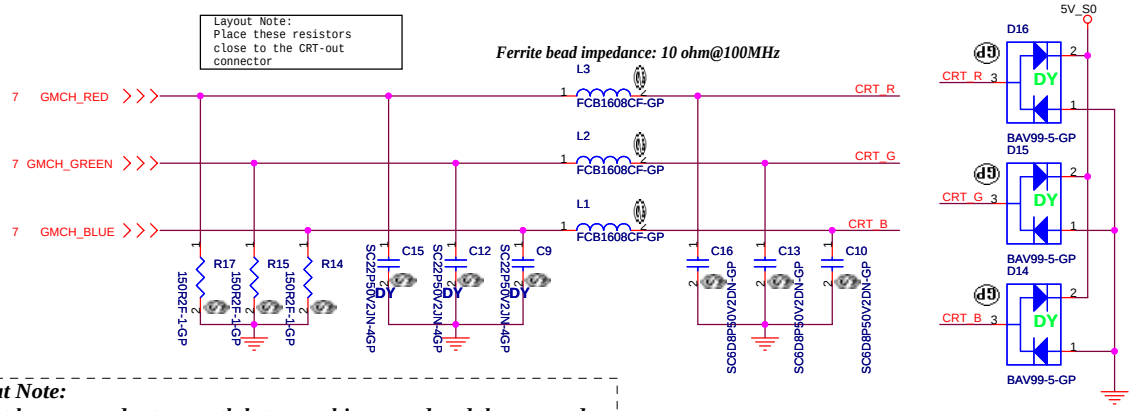
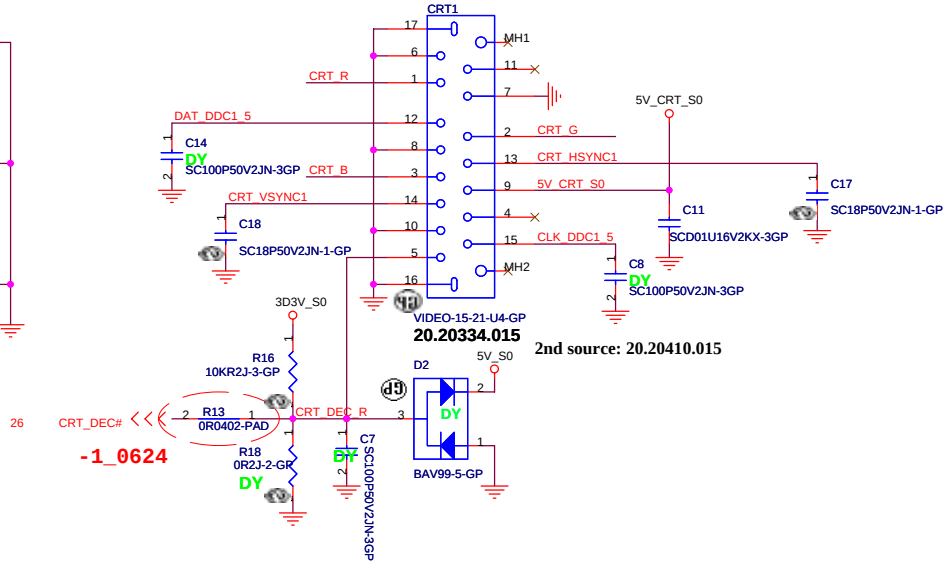
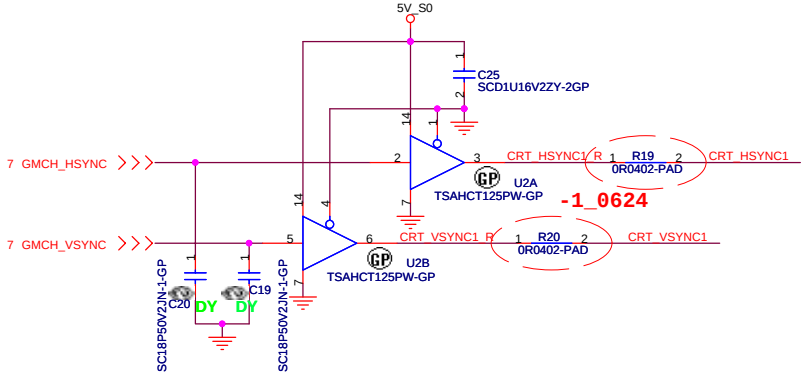
CRT I/F & CONNECTOR

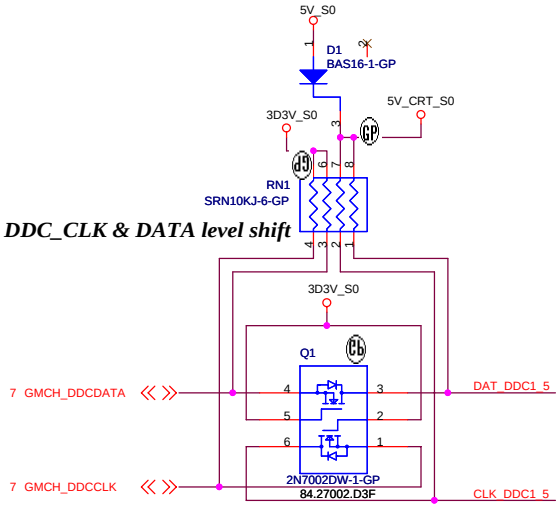




Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

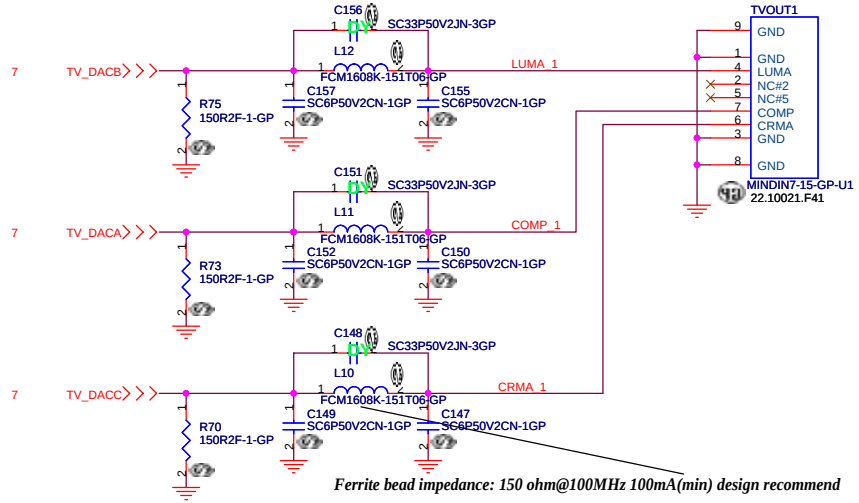
Hsync & Vsync level shift

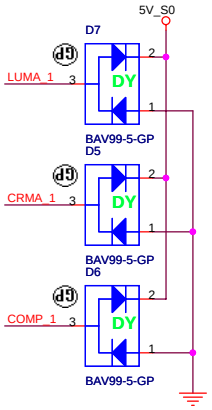




DDC_CLK & DATA level shift

TV CONN





緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*CRT/TV Connector*	
Size	Document Number Volvi2	Rev SA
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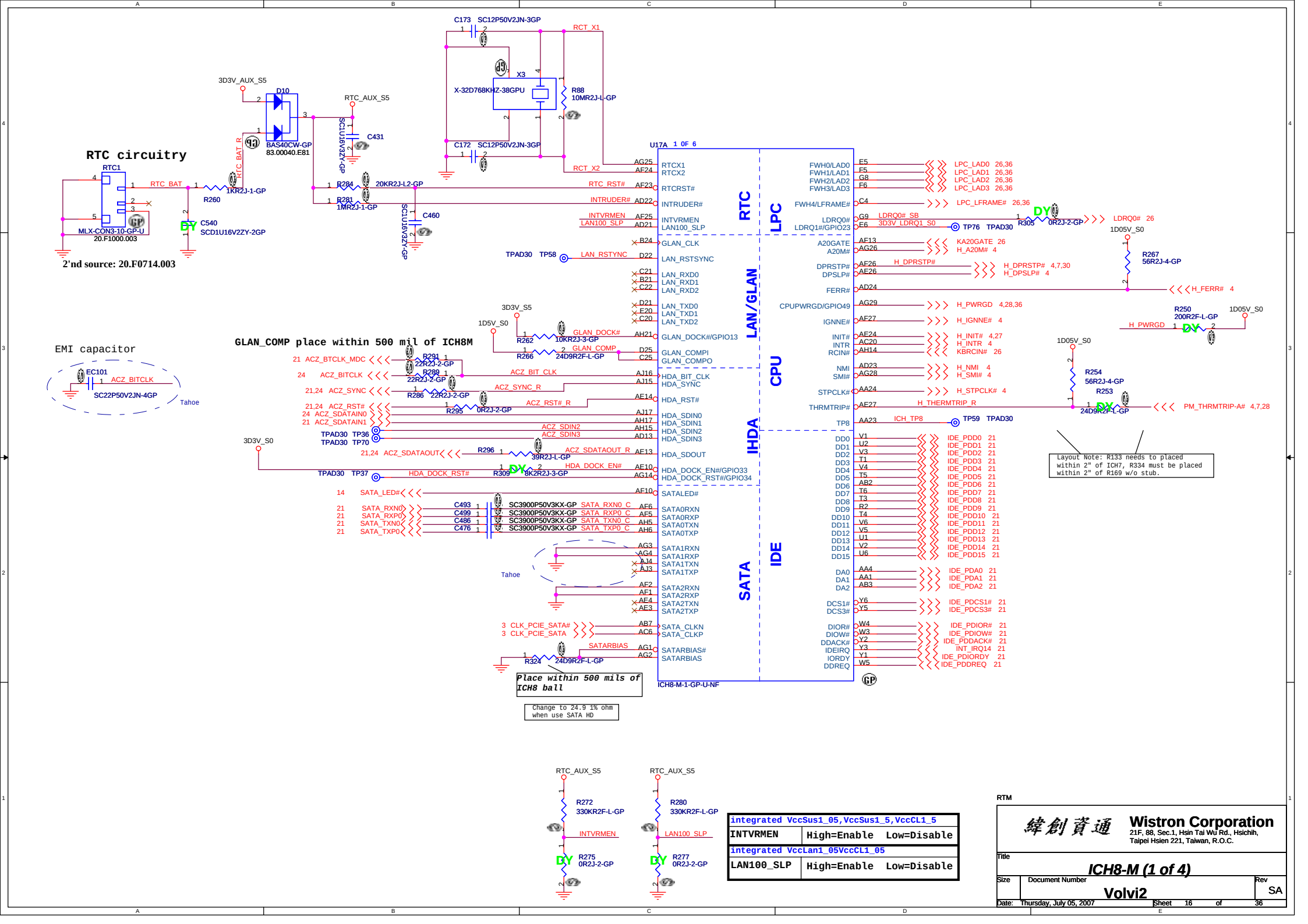
RTC circuitry
RTC1
MLX-CON3-10-GP-U
20.F1000.003
2'nd source: 20.F0714.003
RTC_BAT
R260
1KR2J-1-GP
RTC_BAT_R
3D3V_AUX_S5
D10
BAS40CW-GP
83.00040.E81
RTC_AUX_S5
SCU16V2ZY-GP
C431
R284
20KR2J-L2-GP
R281
1MR2J-1-GP
C540
SCD1U16V2ZY-2GP
C460
C173 SC12P50V2JN-3GP
C172 SC12P50V2JN-3GP
X3
X-32D768KHZ-38GPU
R88
10MR2J-L-GP
RCT_X1
RCT_X2
U17A 1 OF 6
RTC
LPC
LAN/GLAN
CPU
IHDA
SATA
IDE
ICH8-M-1-GP-U-NF
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
LPC_LAD0 26,36
LPC_LAD1 26,36
LPC_LAD2 26,36
LPC_LAD3 26,36
LPC_LFRAME# 26,36
LDRQ0# SB
3D3V_LDRQ1_S0
TP76 TPAD30
R305 0R2J-2-GP
LDRQ0# 26
KA20GATE 26
H_A20M# 4
H_DPRSTP# 4,7,30
H_DPSLP# 4
H_FERR# 4
H_PWRGD 4,28,36
H_IGNNE# 4
H_INIT# 4,27
H_INTR 4
KBRCIN# 26
H_NMI 4
H_SMI# 4
H_STPCLK# 4
H_THERMTRIP_R
PM_THRMTRIP-A# 4,7,28
ICH_TP8
TP59 TPAD30
IDE_PDD0 21
IDE_PDD1 21
IDE_PDD2 21
IDE_PDD3 21
IDE_PDD4 21
IDE_PDD5 21
IDE_PDD6 21
IDE_PDD7 21
IDE_PDD8 21
IDE_PDD9 21
IDE_PDD10 21
IDE_PDD11 21
IDE_PDD12 21
IDE_PDD13 21
IDE_PDD14 21
IDE_PDD15 21
IDE_PDA0 21
IDE_PDA1 21
IDE_PDA2 21
IDE_PDCS1# 21
IDE_PDCS3# 21
IDE_PDIOR# 21
IDE_PDIOW# 21
IDE_PDDACK# 21
INT_IRQ14 21
IDE_PDIORDY 21
IDE_PDDREQ 21
R267
56R2J-4-GP
R250
200R2F-L-GP
R254
56R2J-4-GP
R253
24D9R2F-L-GP
1D05V_S0
3D3V_S5
R262 10KR2J-3-GP
R266 24D9R2F-L-GP
GLAN_DOCK#
GLAN_COMP
GLAN_COMP place within 500 mil of ICH8M
EMI capacitor
EC101
SC22P50V2JN-4GP
ACZ_BITCLK
Tahoe
21 ACZ_BTCLK_MDC
24 ACZ_BITCLK
21,24 ACZ_SYNC
21,24 ACZ_RST#
24 ACZ_SDATAIN0
21 ACZ_SDATAIN1
R291 22R2J-2-GP
R289 22R2J-2-GP
R286 22R2J-2-GP
R295 0R2J-2-GP
ACZ_BIT_CLK
ACZ_SYNC_R
ACZ_RST#_R
ACZ_SDIN2
ACZ_SDIN3
TPAD30 TP36
TPAD30 TP70
21,24 ACZ_SDATAOUT
R296 39R2J-L-GP
ACZ_SDATAOUT_R
HDA_DOCK_EN#
HDA_DOCK_RST#
TPAD30 TP37
R309 8K2R2J-3-GP
3D3V_S0
14 SATA_LED#
21 SATA_RXN0
21 SATA_RXP0
21 SATA_TXN0
21 SATA_TXP0
C493 SC3900P50V3KX-GP SATA_RXN0_C
C499 SC3900P50V3KX-GP SATA_RXP0_C
C486 SC3900P50V3KX-GP SATA_TXN0_C
C476 SC3900P50V3KX-GP SATA_TXP0_C
3 CLK_PCIE_SATA#
3 CLK_PCIE_SATA
SATARBIAS
R324 24D9R2F-L-GP
Place within 500 mils of ICH8 ball
Change to 24.9 1% ohm when use SATA HD
Layout Note: R133 needs to placed within 2" of ICH7, R334 must be placed within 2" of R169 w/o stub.
RTC_AUX_S5
R272 330KR2F-L-GP
INTVRMEN
R275 0R2J-2-GP
R280 330KR2F-L-GP
LAN100_SLP
R277 0R2J-2-GP
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
RTM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8-M (1 of 4)
Size
Document Number
Volvi2
Rev
SA
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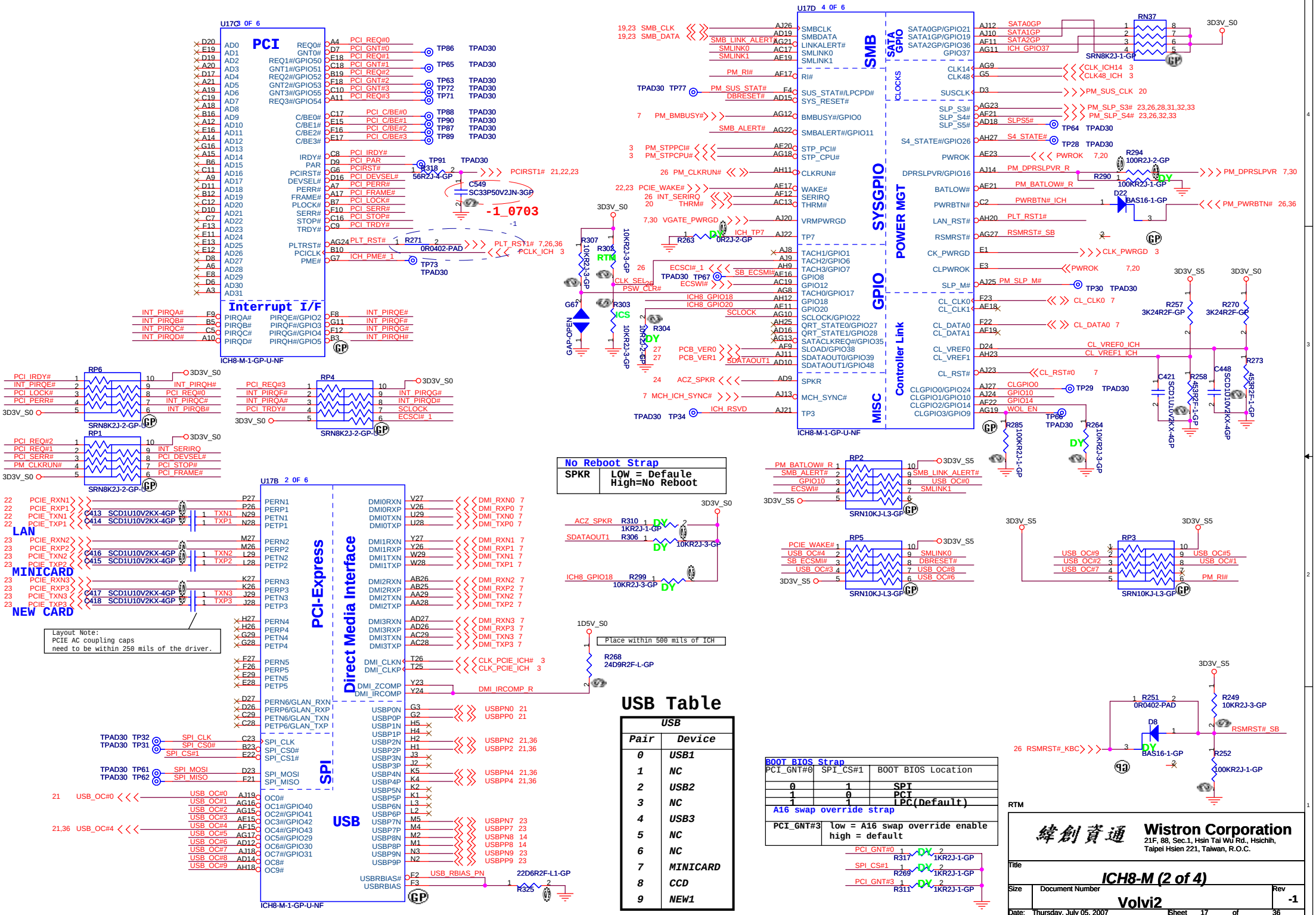
U17C 3 OF 6
PCI
Interrupt I/F
ICH8-M-1-GP-U-NF
U17D 4 OF 6
SMB
SATA GPIO
CLOCKS
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
ICH8-M-1-GP-U-NF
U17B 2 OF 6
PCI-Express
Direct Media Interface
SPI
USB
ICH8-M-1-GP-U-NF
LAN
MINICARD
NEW CARD
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Place within 500 mils of ICH
No Reboot Strap
SPKR LOW = Defaule
High=No Reboot
BOOT BIOS Strap
PCI_GNT#0 SPI_CS#1 BOOT BIOS Location
0 1 SPI
1 0 PCI
1 1 LPC(Default)
A16 swap override strap
PCI_GNT#3 low = A16 swap override enable
high = default
USB Table
USB
Pair Device
0 USB1
1 NC
2 USB2
3 NC
4 USB3
5 NC
6 NC
7 MINICARD
8 CCD
9 NEW1
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Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8-M (2 of 4)
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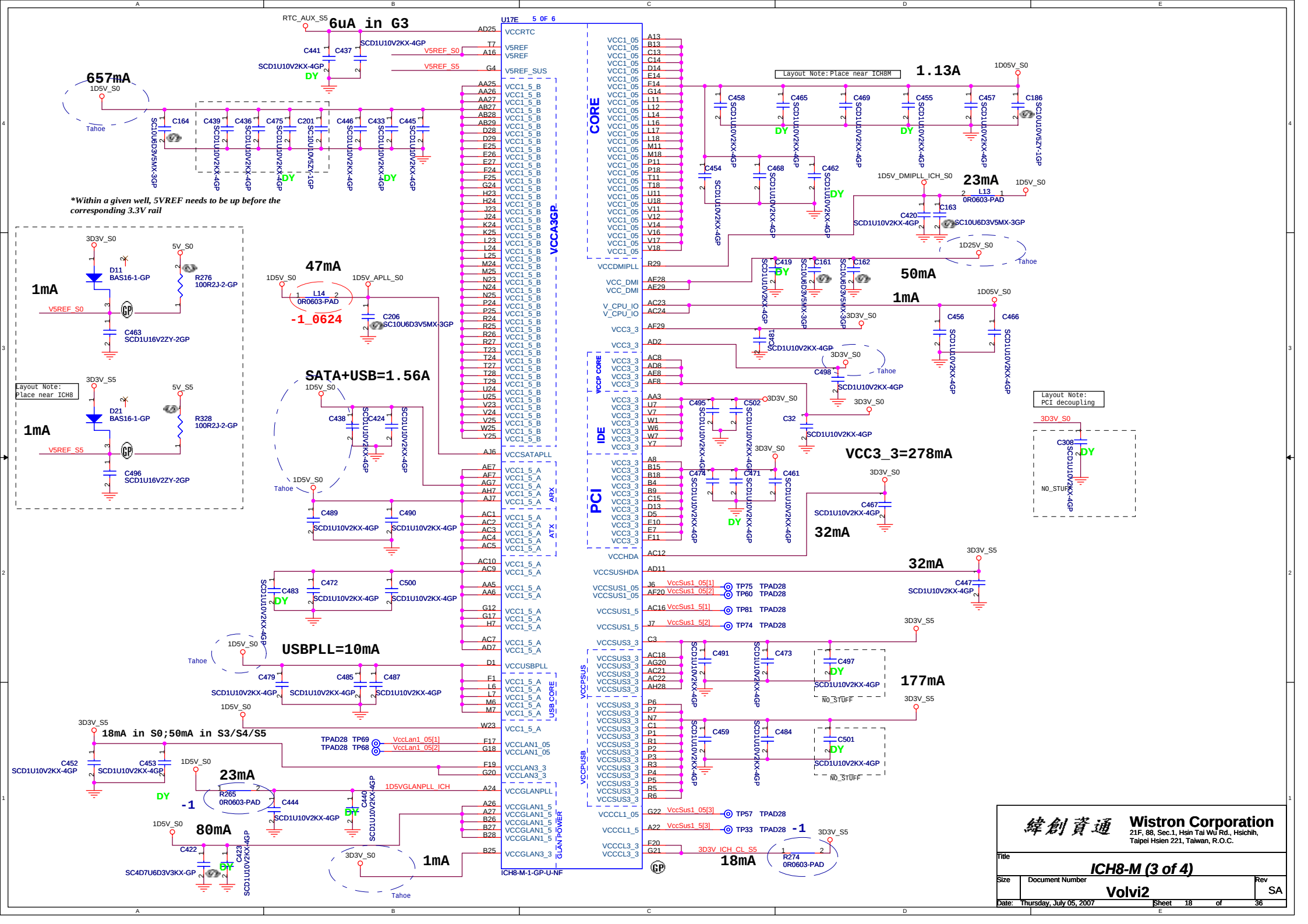
U17E 5 OF 6
ICH8-M-1-GP-U-NF
CORE
VCCA3GP
PCI
IDE
VCCP CORE
ARX
ATX
USB CORE
VCCPSUS
VCCPUSB
LAN POWER
6uA in G3
657mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
1mA
47mA
-1_0624
SATA+USB=1.56A
USBPLL=10mA
18mA in S0;50mA in S3/S4/S5
23mA
-1
80mA
1mA
1.13A
Layout Note:Place near ICH8M
23mA
50mA
1mA
VCC3_3=278mA
32mA
32mA
177mA
18mA
-1
Layout Note: Place near ICH8
Layout Note: PCI decoupling
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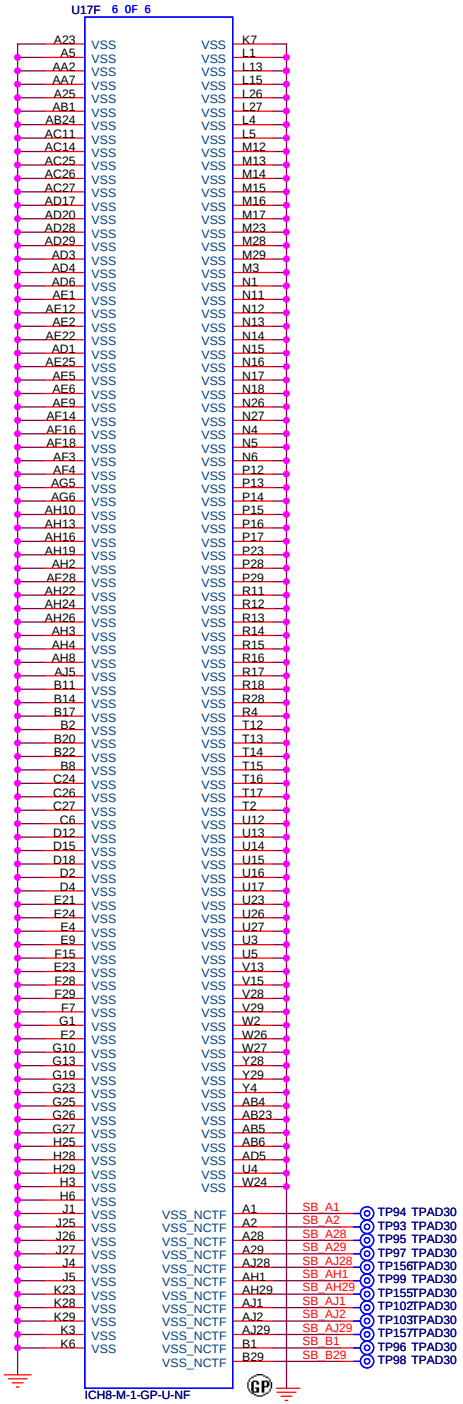

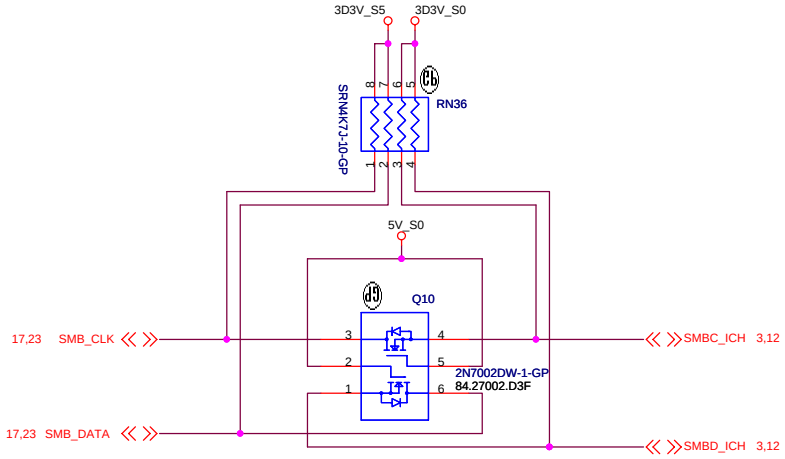

Q12 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

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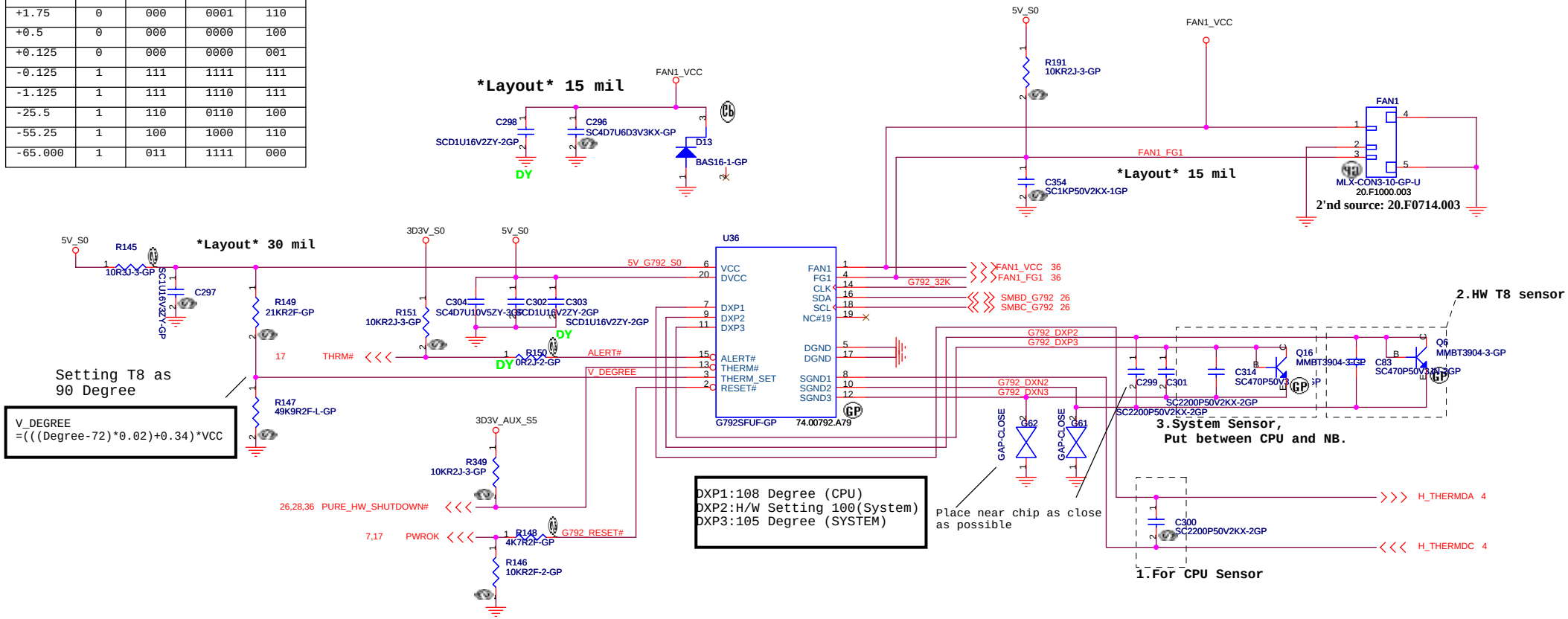
TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Controllor***

Size | Document Number: **Volvi2** | Rev: **-1**

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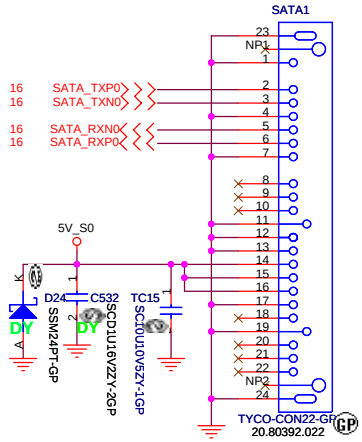
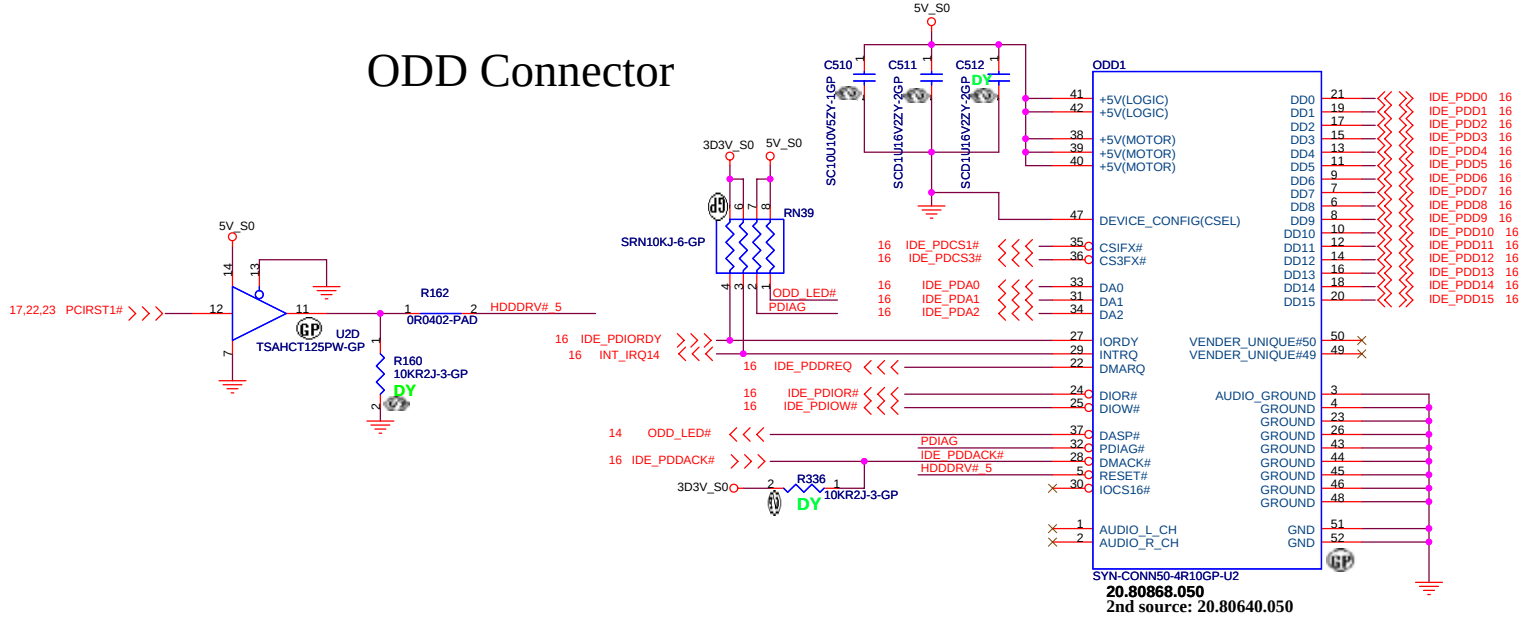
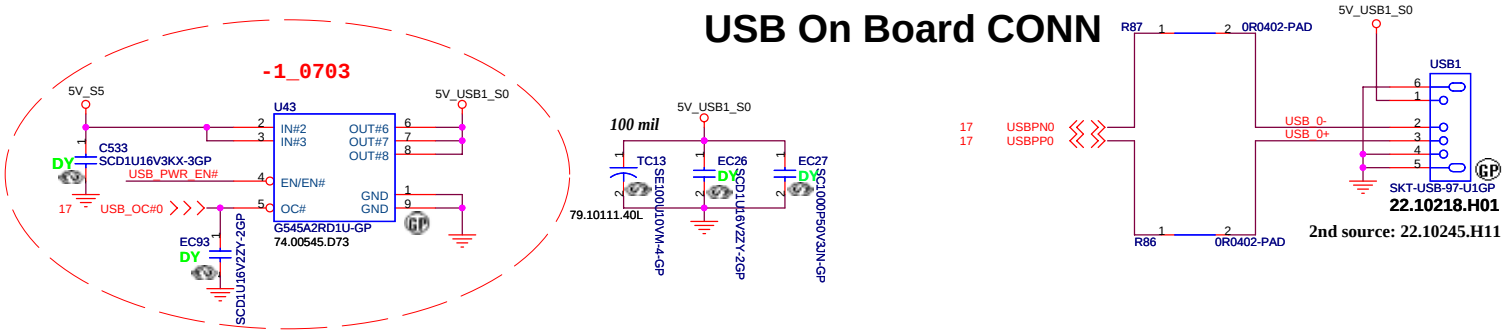
SATA HD Connector



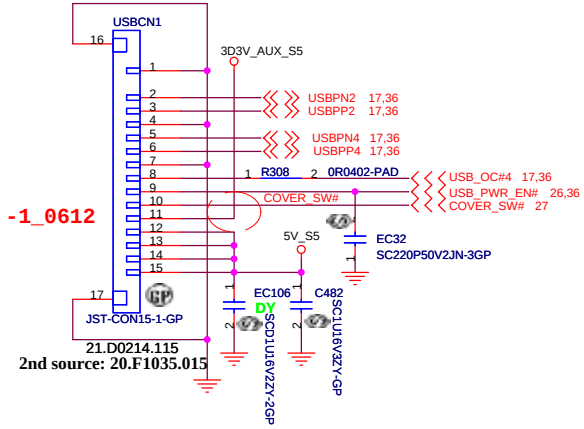
ODD Connector



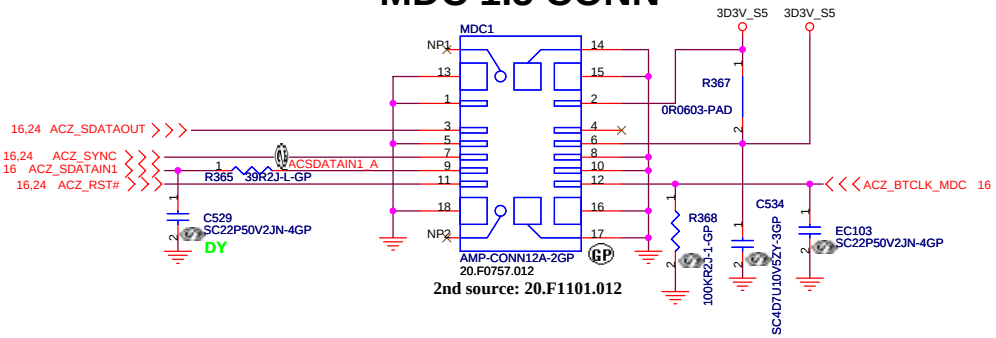
USB On Board CONN



USB ZIF CONN



MDC 1.5 CONN



RTM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
	HDD / CDROM / USB / MDC	
Size	Document Number	Rev
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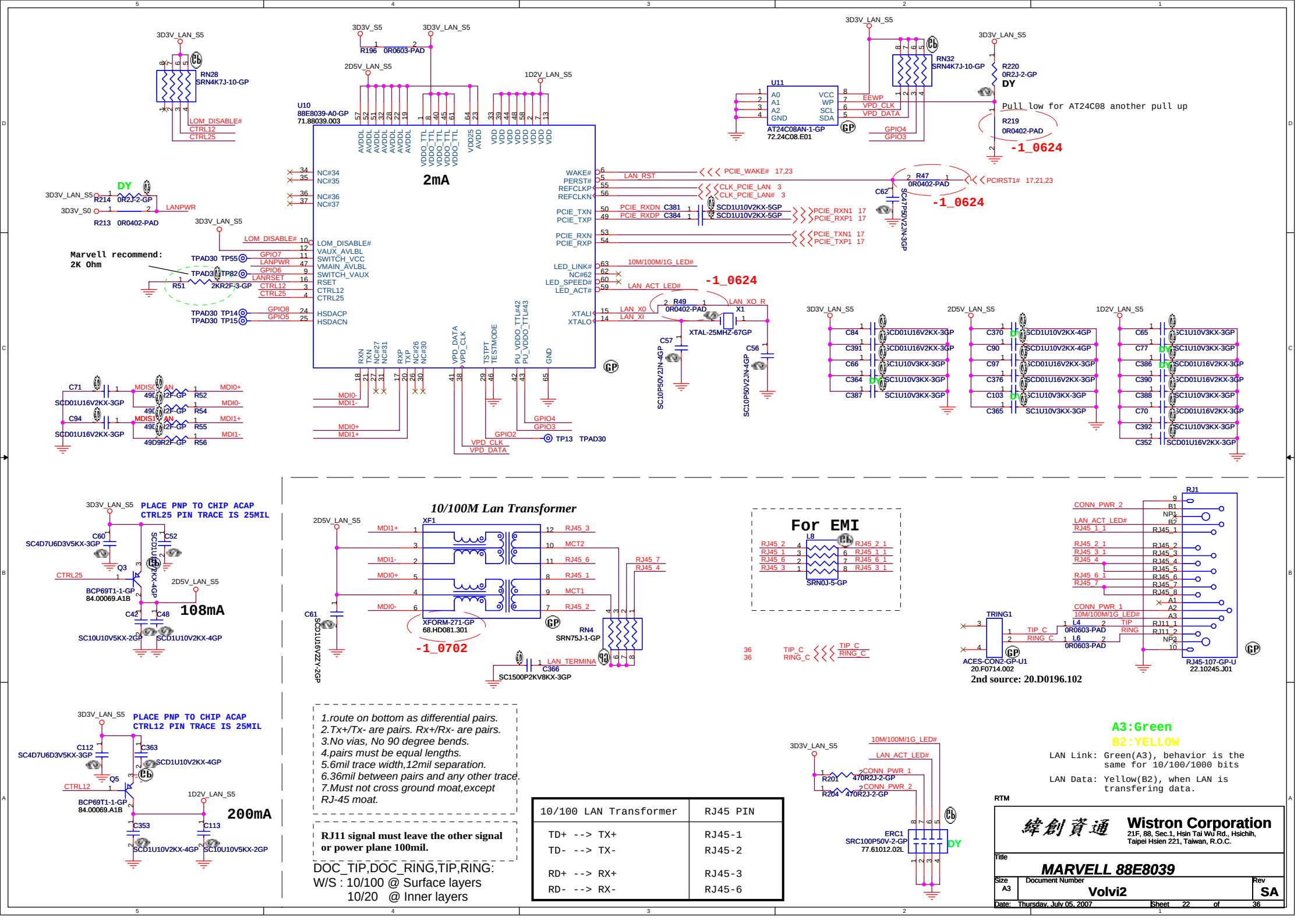
U10
88E8039-A0-GP
71.88039.003
2mA
U11
AT24C08AN-1-GP
72.24C08.E01
RN28
SRN4K7J-10-GP
RN32
SRN4K7J-10-GP
R220
0R2J-2-GP
DY
Pull low for AT24C08 another pull up
R219
0R0402-PAD
-1_0624
R47
0R0402-PAD
C62
SC47P50V2JN-3GP
R214
0R2J-2-GP
R213
0R0402-PAD
LANPWR
Marvell recommend:
2K Ohm
R51
2KR2F-3-GP
R49
0R0402-PAD
X1
XTAL-25MHZ-67GP
C57
SC10P50V2JN-4GP
C56
SC10P50V2JN-4GP
C71
SCD01U16V2KX-3GP
C94
SCD01U16V2KX-3GP
R52
49D9R2F-GP
R54
49D9R2F-GP
R55
49D9R2F-GP
R56
49D9R2F-GP
TP13
TPAD30
PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL
Q3
BCP69T1-1-GP
84.00069.A1B
108mA
C60
SC4D7U6D3V5KX-3GP
C52
SCD1U16V2KX-4GP
C42
SC10U10V5KX-2GP
C48
SCD1U10V2KX-4GP
10/100M Lan Transformer
XF1
XFORM-271-GP
68.HD081.301
-1_0702
C61
SCD1U16V2ZY-2GP
RN4
SRN75J-1-GP
C366
SC1500P2KV8KX-3GP
For EMI
L8
SRN0J-5-GP
TRING1
ACES-CON2-GP-U1
20.F0714.002
2nd source: 20.D0196.102
L4
0R0603-PAD
L6
0R0603-PAD
RJ1
RJ45-107-GP-U
22.10245.J01
PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL
Q5
BCP69T1-1-GP
84.00069.A1B
200mA
C112
SC4D7U6D3V5KX-3GP
C363
SCD1U10V2KX-4GP
C353
SCD1U10V2KX-4GP
C113
SC10U10V5KX-2GP
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.
RJ11 signal must leave the other signal or power plane 100mil.
DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers
10/100 LAN Transformer | RJ45 PIN
TD+ --> TX+ | RJ45-1
TD- --> TX- | RJ45-2
RD+ --> RX+ | RJ45-3
RD- --> RX- | RJ45-6
ERC1
SRC100P50V-2-GP
77.61012.02L
A3:Green
B2:YELLOW
LAN Link: Green(A3), behavior is the same for 10/100/1000 bits
LAN Data: Yellow(B2), when LAN is transfering data.
RTM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
MARVELL 88E8039
Size A3
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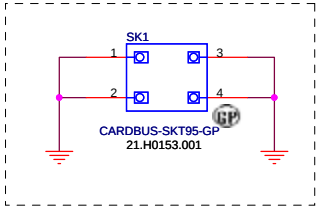
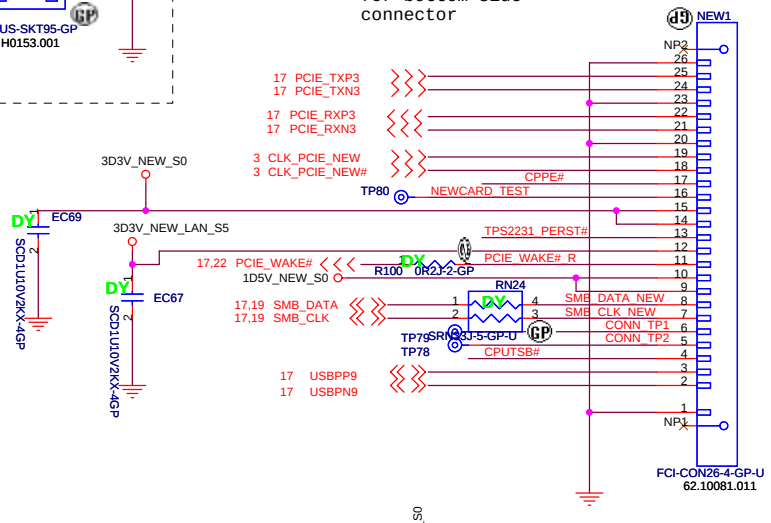
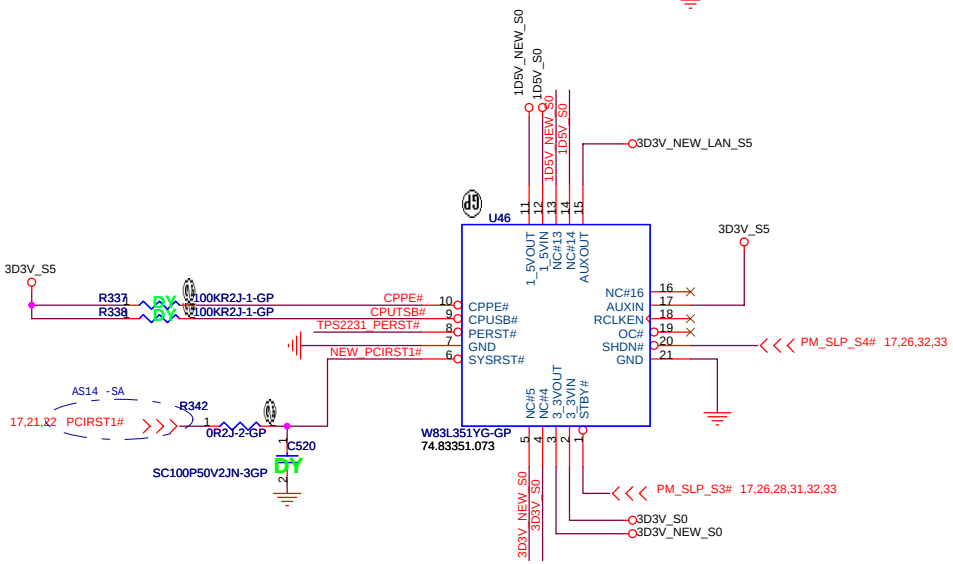
Mini Card Connector

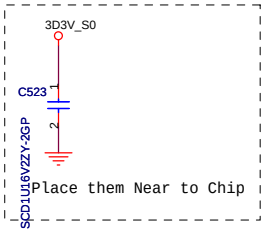


NEWCARD Connector

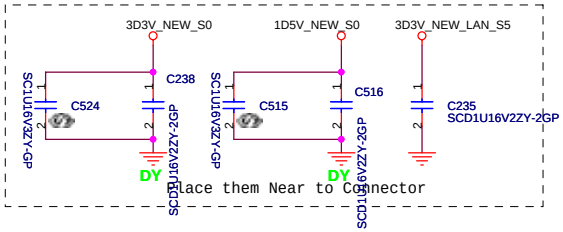
Reserve the symbol for bottom side connector



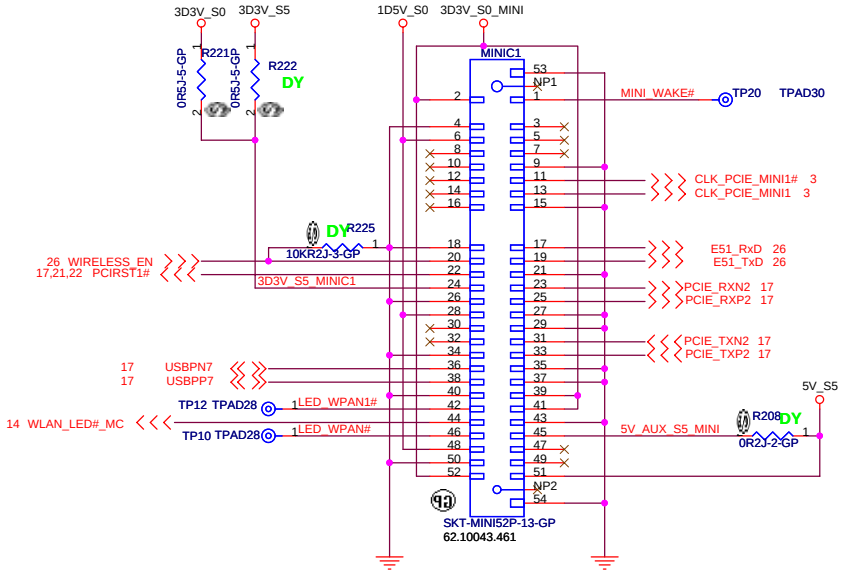


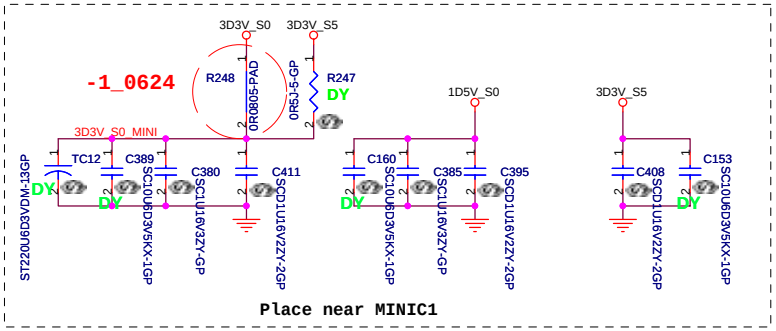


Place them Near to Chip



Place them Near to Connector





Place near MINIC1

RTM

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Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD / NEW CARD

Size: | Document Number: Volvi2 | Rev: SA

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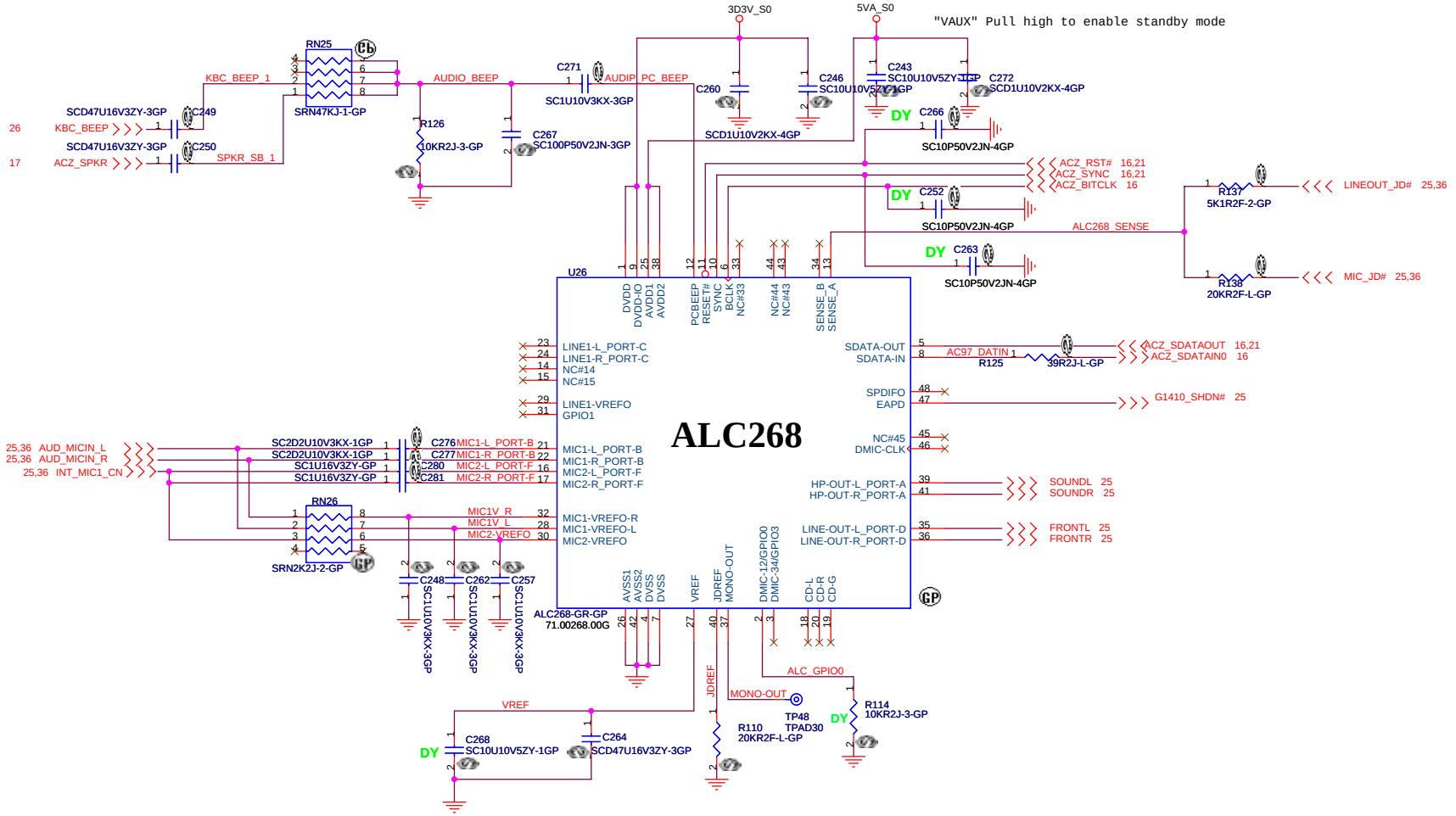
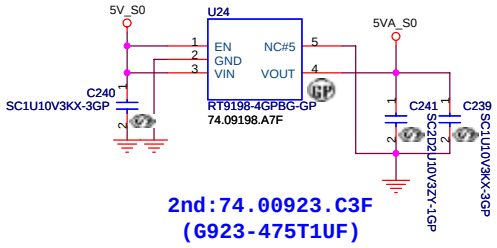


POWER GENERATE

Layout
20 mil



2nd:74.00923.C3F
(G923-475T1UF)

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Title	*AZALIA CODEC - ALC268*	
Size	Document Number **Volvi2**	Rev SA
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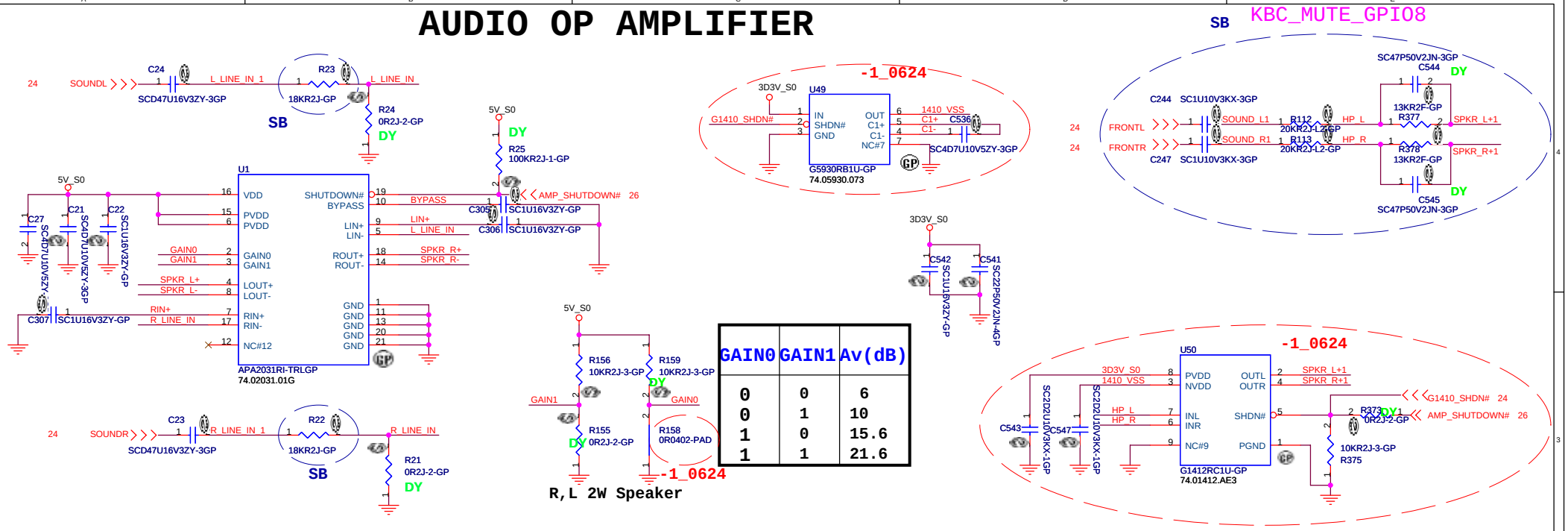
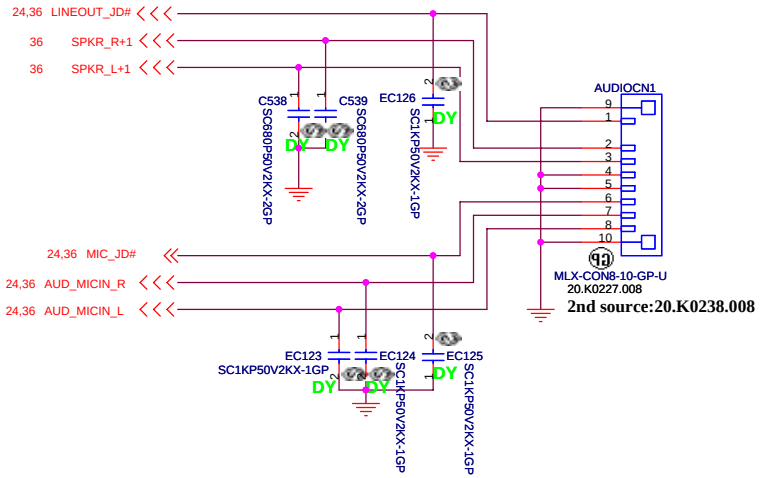
AUDIO OP AMPLIFIER

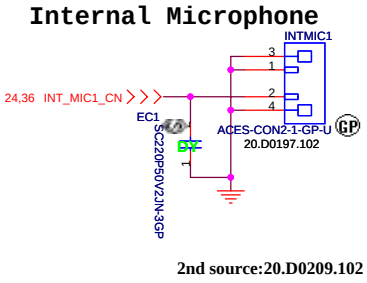


GAIN0	GAIN1	Av(dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6

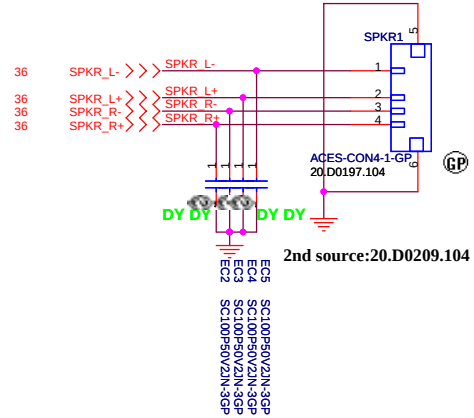
Audio Connector



Internal Microphone



Internal Speaker



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Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP AND JACK

Size | Document Number: Volvi2 | Rev: -1

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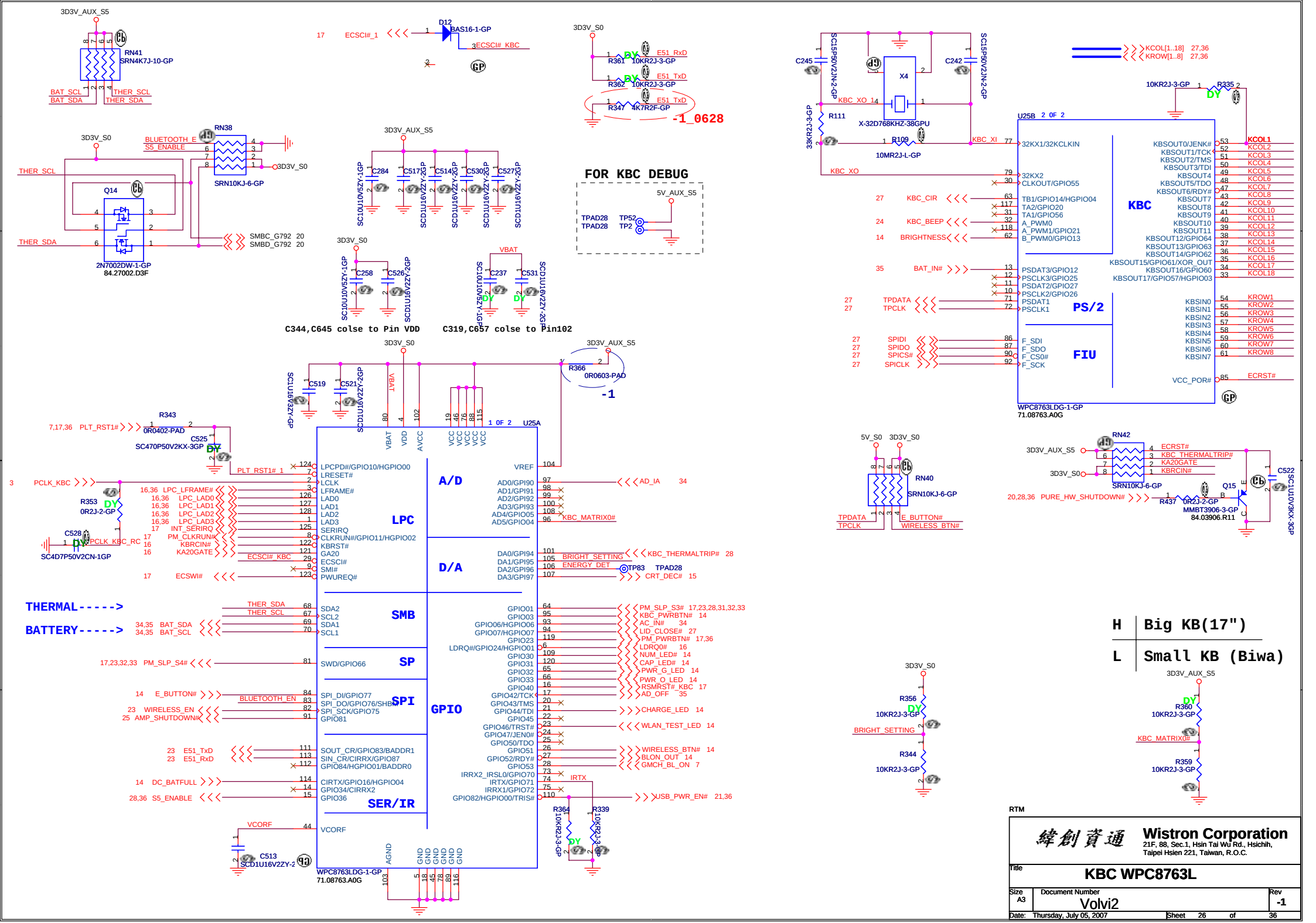
3D3V_AUX_S5
RN41
SRN4K7J-10-GP
BAT_SCL
BAT_SDA
THER_SCL
THER_SDA
17 ECSCI#_1
D12
BAS16-1-GP
ECSCI#_KBC
3D3V_S0
R361 10KR2J-3-GP
R362 10KR2J-3-GP
R347 4K7R2F-GP
E51_RxD
E51_TxD
-1_0628
RN38
BLUETOOTH_E
S5_ENABLE
SRN10KJ-6-GP
Q14
2N7002DW-1-GP
84.27002.D3F
SMBC_G792 20
SMBD_G792 20
C284
C517
C514
C530
C527
SC10U10V5ZY-1GP
SCD1U16V2ZY-2GP
FOR KBC DEBUG
5V_AUX_S5
TPAD28
TP52
TP2
C258
C526
C237
C531
VBAT
C344,C645 colse to Pin VDD
C319,C657 colse to Pin102
C519
C521
R366
0R0603-PAD
-1
R343
0R0402-PAD
7,17,36 PLT_RST1#
C525
SC470P50V2KX-3GP
PLT_RST1# 1
3 PCLK_KBC
R353
0R2J-2-GP
C528
SC4D7P50V2CN-1GP
PCLK_KBC_RC
16,36 LPC_LFRAME#
16,36 LPC_LAD0
16,36 LPC_LAD1
16,36 LPC_LAD2
16,36 LPC_LAD3
17 INT_SERIRQ
17 PM_CLKRUN#
16 KBRCIN#
16 KA20GATE
ECSCI#_KBC
17 ECSWI#
U25A
1 0F 2
LPC
A/D
D/A
SMB
SP
SPI
GPIO
SER/IR
LPCPD#/GPIO10/HGPIO00
LRESET#
LCLK
LFRAME#
LAD0
LAD1
LAD2
LAD3
SERIRQ
CLKRUN#/GPIO11/HGPIO02
KBRST#
GA20
ECSCI#
SMI#
PWUREQ#
VREF
AD0/GPI90
AD1/GPI91
AD2/GPI92
AD3/GPI93
AD4/GPIO05
AD5/GPIO04
AD_IA 34
KBC_MATRIX0#
DA0/GPI94
DA1/GPI95
DA2/GPI96
DA3/GPI97
BRIGHT_SETTING
ENERGY_DET
TP83 TPAD28
KBC_THERMALTRIP# 28
CRT_DEC# 15
THERMAL----->
BATTERY----->
THER_SDA
THER_SCL
34,35 BAT_SDA
34,35 BAT_SCL
17,23,32,33 PM_SLP_S4#
14 E_BUTTON#
BLUETOOTH_EN
23 WIRELESS_EN
25 AMP_SHUTDOWN#
23 E51_TxD
23 E51_RxD
14 DC_BATFULL
28,36 S5_ENABLE
SDA2
SCL2
SDA1
SCL1
SWD/GPIO66
SPI_DI/GPIO77
SPI_DO/GPIO76/SHBM
SPI_SCK/GPIO75
GPIO81
SOUT_CR/GPIO83/BADDR1
SIN_CR/CIRRX/GPIO87
GPIO84/HGPIO01/BADDR0
CIRTX/GPIO16/HGPIO04
GPIO34/CIRRX2
GPIO36
VCORF
C513
SCD1U16V2ZY-2
WPC8763LDG-1-GP
71.08763.A0G
GPIO01
GPIO03
GPIO06/HGPIO06
GPIO07/HGPIO07
GPIO23
LDRQ#/GPIO24/HGPIO01
GPIO30
GPIO31
GPIO32
GPIO33
GPIO40
GPIO42/TCK
GPIO43/TMS
GPIO44/TDI
GPIO45
GPIO46/TRST#
GPIO47/JEN0#
GPIO50/TDO
GPIO51
GPIO52/RDY#
GPIO53
IRRX2_IRSL0/GPIO70
IRTX/GPIO71
IRRX1/GPIO72
GPIO82/HGPIO00/TRIS#
PM_SLP_S3# 17,23,28,31,32,33
KBC_PWRBTN# 14
AC_IN# 34
LID_CLOSE# 27
PM_PWRBTN# 17,36
LDRQ0# 16
NUM_LED# 14
CAP_LED# 14
PWR_G_LED 14
PWR_O_LED 14
RSMRST#_KBC 17
AD_OFF 35
CHARGE_LED 14
WLAN_TEST_LED 14
WIRELESS_BTN# 14
BLON_OUT 14
GMCH_BL_ON 7
IRTX
USB_PWR_EN# 21,36
R364
R339
10KR2J-3-GP
C245
C242
SC15P50V2JN-2-GP
X4
X-32D768KHZ-38GPU
KBC_XO 14
KBC_XI
R111
33KR2J-3-GP
R109
10MR2J-L-GP
KCOL[1..18] 27,36
KROW[1..8] 27,36
R335
U25B 2 0F 2
KBC
PS/2
FIU
32KX1/32KCLKIN
32KX2
CLKOUT/GPIO55
TB1/GPIO14/HGPIO04
TA2/GPIO20
TA1/GPIO56
A_PWM0
A_PWM1/GPIO21
B_PWM0/GPIO13
PSDAT3/GPIO12
PSCLK3/GPIO25
PSDAT2/GPIO27
PSCLK2/GPIO26
PSDAT1
PSCLK1
F_SDI
F_SDO
F_CS0#
F_SCK
VCC_POR#
KBSOUT0/JENK#
KBSOUT1/TCK
KBSOUT2/TMS
KBSOUT3/TDI
KBSOUT4
KBSOUT5/TDO
KBSOUT6/RDY#
KBSOUT7
KBSOUT8
KBSOUT9
KBSOUT10
KBSOUT11
KBSOUT12/GPIO64
KBSOUT13/GPIO63
KBSOUT14/GPIO62
KBSOUT15/GPIO61/XOR_OUT
KBSOUT16/GPIO60
KBSOUT17/GPIO57/HGPIO03
KBSIN0
KBSIN1
KBSIN2
KBSIN3
KBSIN4
KBSIN5
KBSIN6
KBSIN7
KCOL1
KCOL2
KCOL3
KCOL4
KCOL5
KCOL6
KCOL7
KCOL8
KCOL9
KCOL10
KCOL11
KCOL12
KCOL13
KCOL14
KCOL15
KCOL16
KCOL17
KCOL18
KROW1
KROW2
KROW3
KROW4
KROW5
KROW6
KROW7
KROW8
ECRST#
27 KBC_CIR
24 KBC_BEEP
14 BRIGHTNESS
35 BAT_IN#
27 TPDATA
27 TPCLK
27 SPIDI
27 SPIDO
27 SPICS#
27 SPICLK
WPC8763LDG-1-GP
71.08763.A0G
5V_S0
RN40
SRN10KJ-6-GP
TPDATA
TPCLK
E_BUTTON#
WIRELESS_BTN#
RN42
ECRST#
KBC_THERMALTRIP#
KA20GATE
KBRCIN#
SRN10KJ-6-GP
20,28,36 PURE_HW_SHUTDOWN#
R437 0R2J-2-GP
Q15
MMBT3906-3-GP
84.03906.R11
C522
SC1U10V3KX-3GP
R356
10KR2J-3-GP
BRIGHT_SETTING
R344
10KR2J-3-GP
R360
10KR2J-3-GP
KBC_MATRIX0#
R359
10KR2J-3-GP
H Big KB(17")
L Small KB (Biwa)
RTM
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC WPC8763L
Size A3
Document Number
Volvi2
Rev -1
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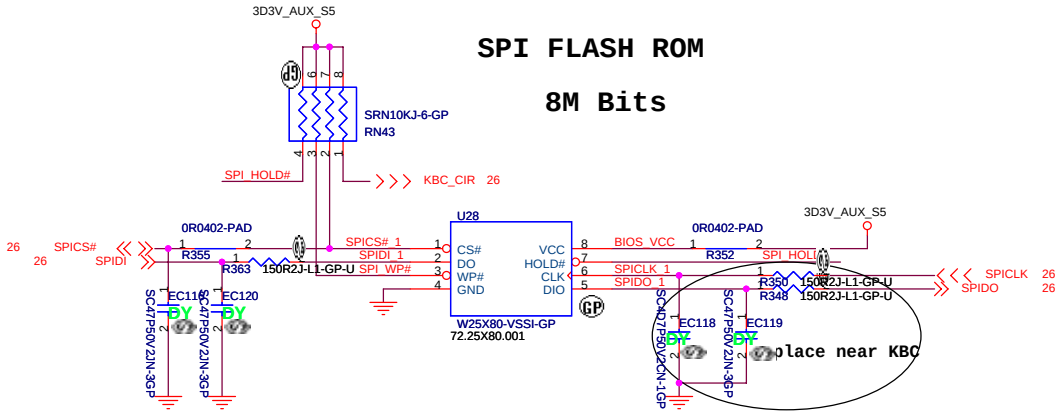

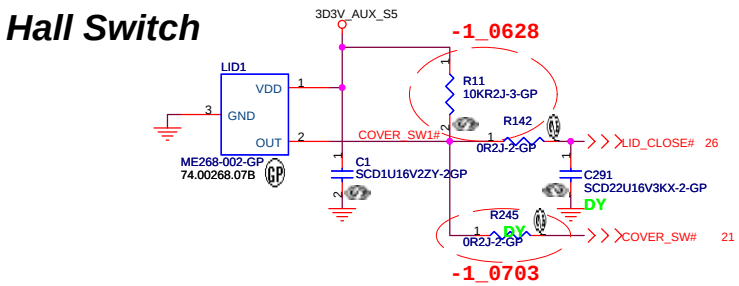

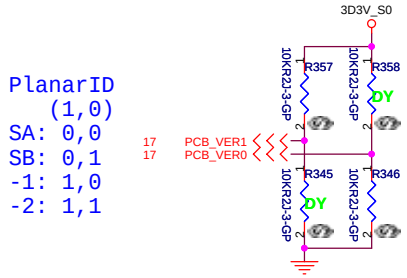

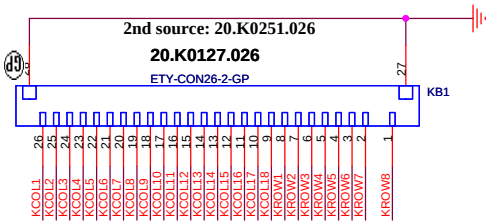

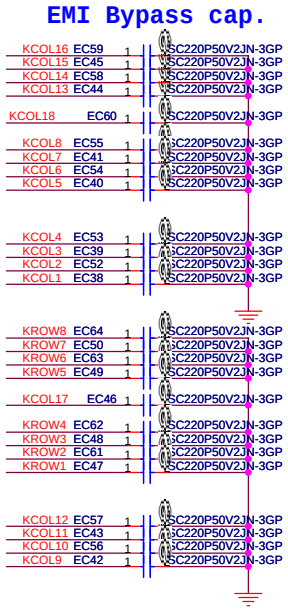

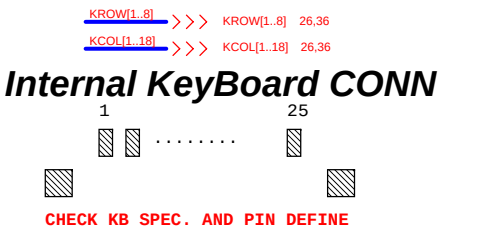

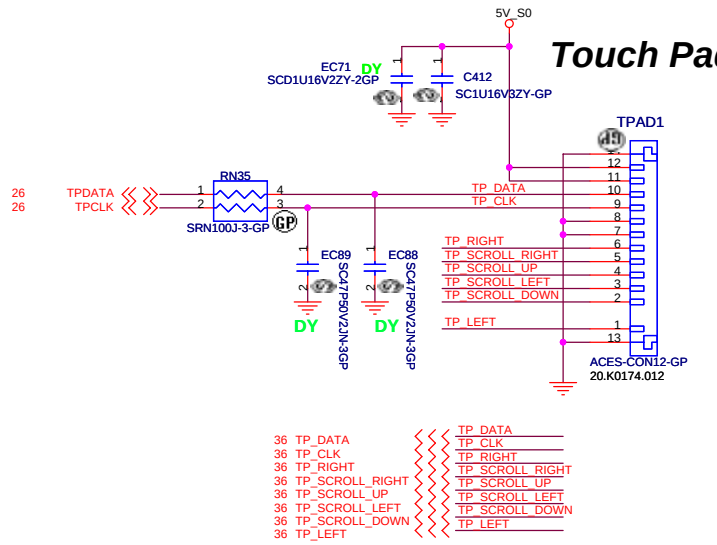

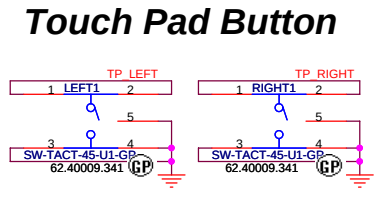

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Title	BUTTONs / KB / TOUCHPAD / BIOS	
Size	Document Number: Volvi2	Rev: -1
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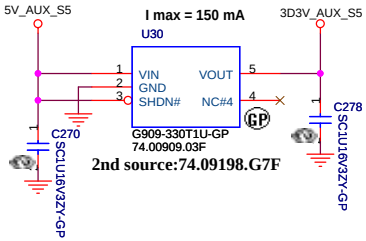
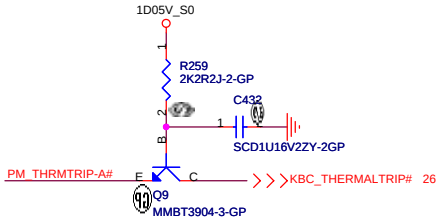
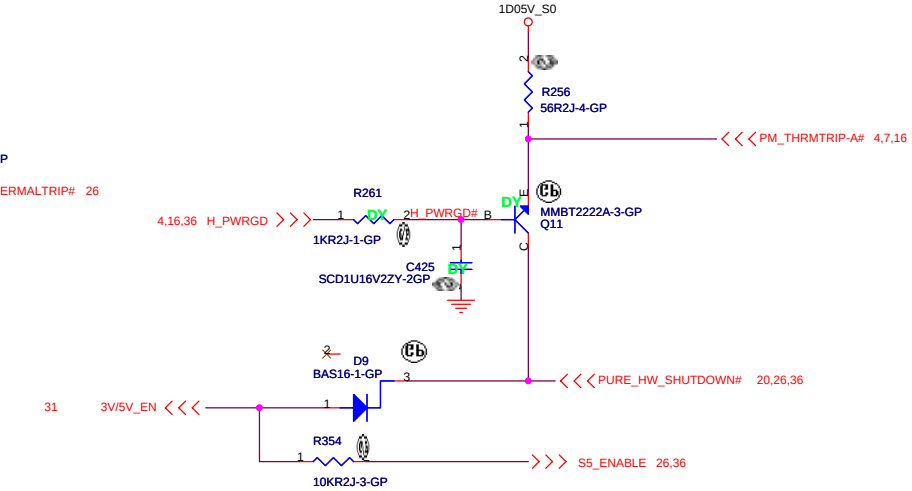
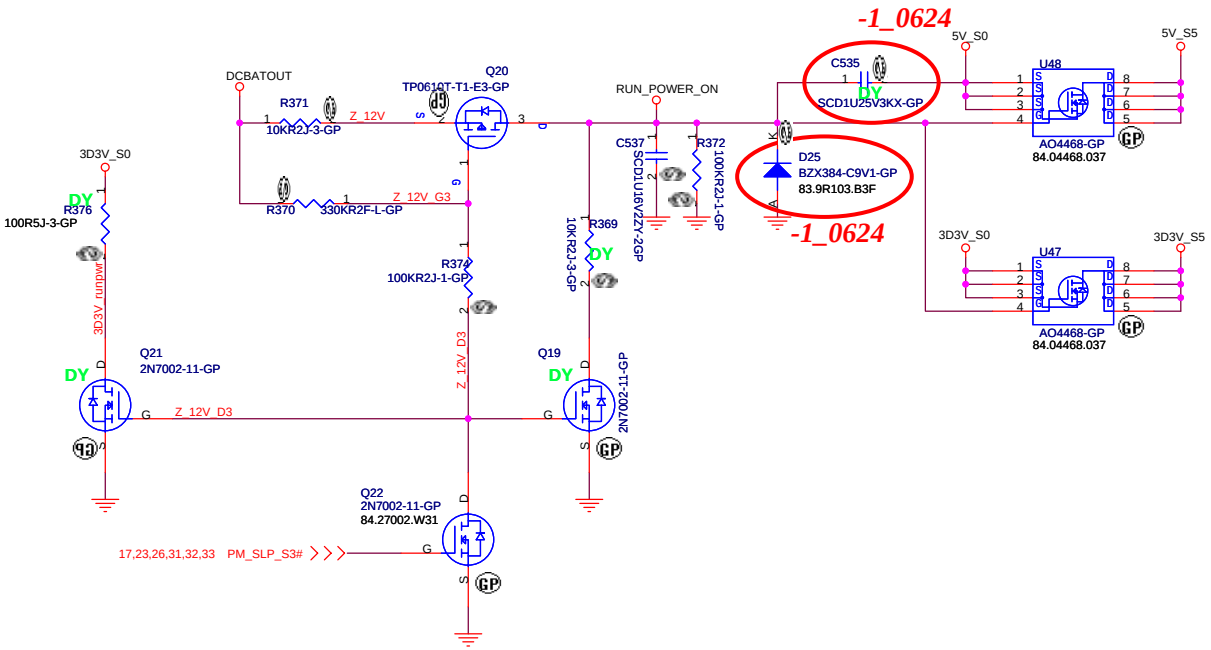
Aux Power 3D3V_AUX_S5







Run Power



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Title	RUN POWER and 3D3V_AUX_S5	
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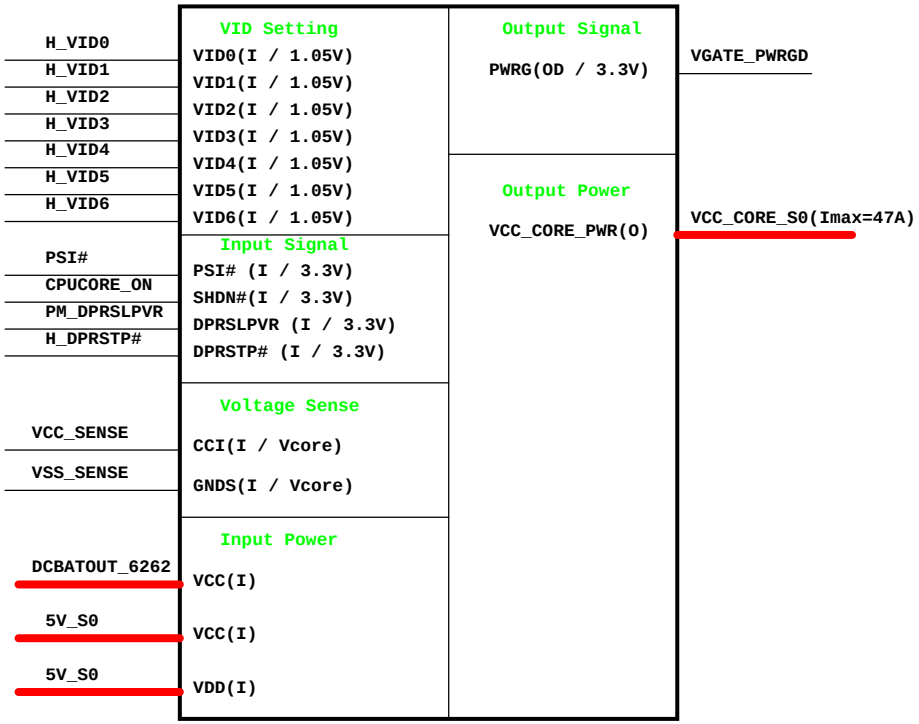
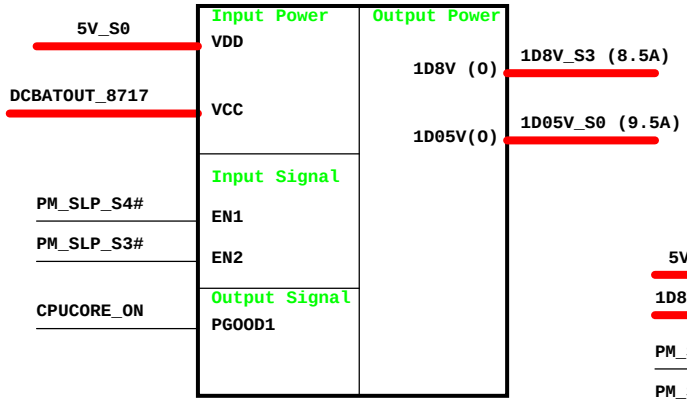
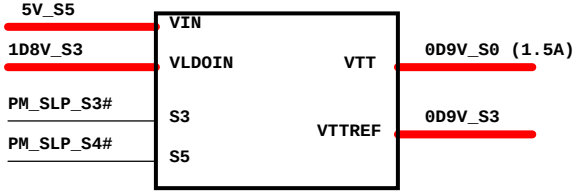
CPU_CORE
MAX8770



TPS51124
1D8V/1D05V

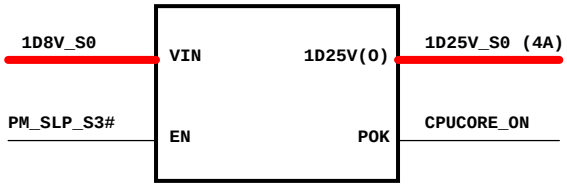


0D9V_S0



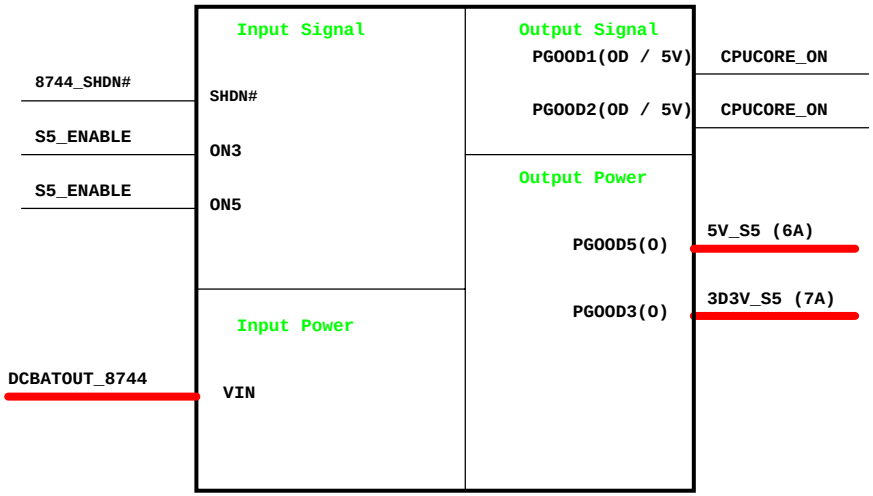
TPS51100

1D25V_S0

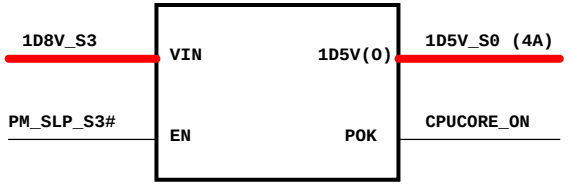


APL5913

MAX8744
5V/3D3V

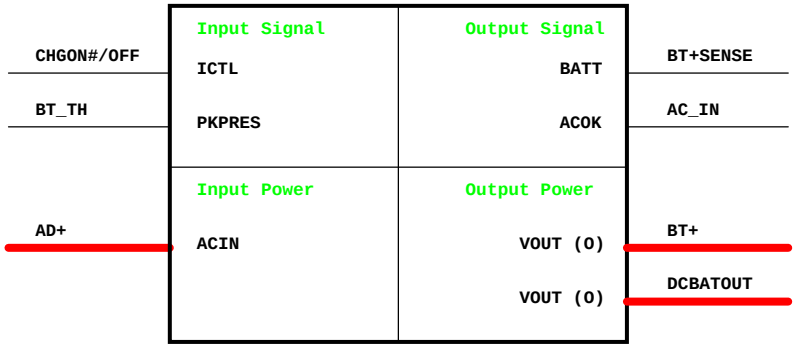


1D5V_S0



APL5915

Charger MAX8731



RTM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Power Block Diagram	
Size A3	Document Number Volvi2	Rev SA
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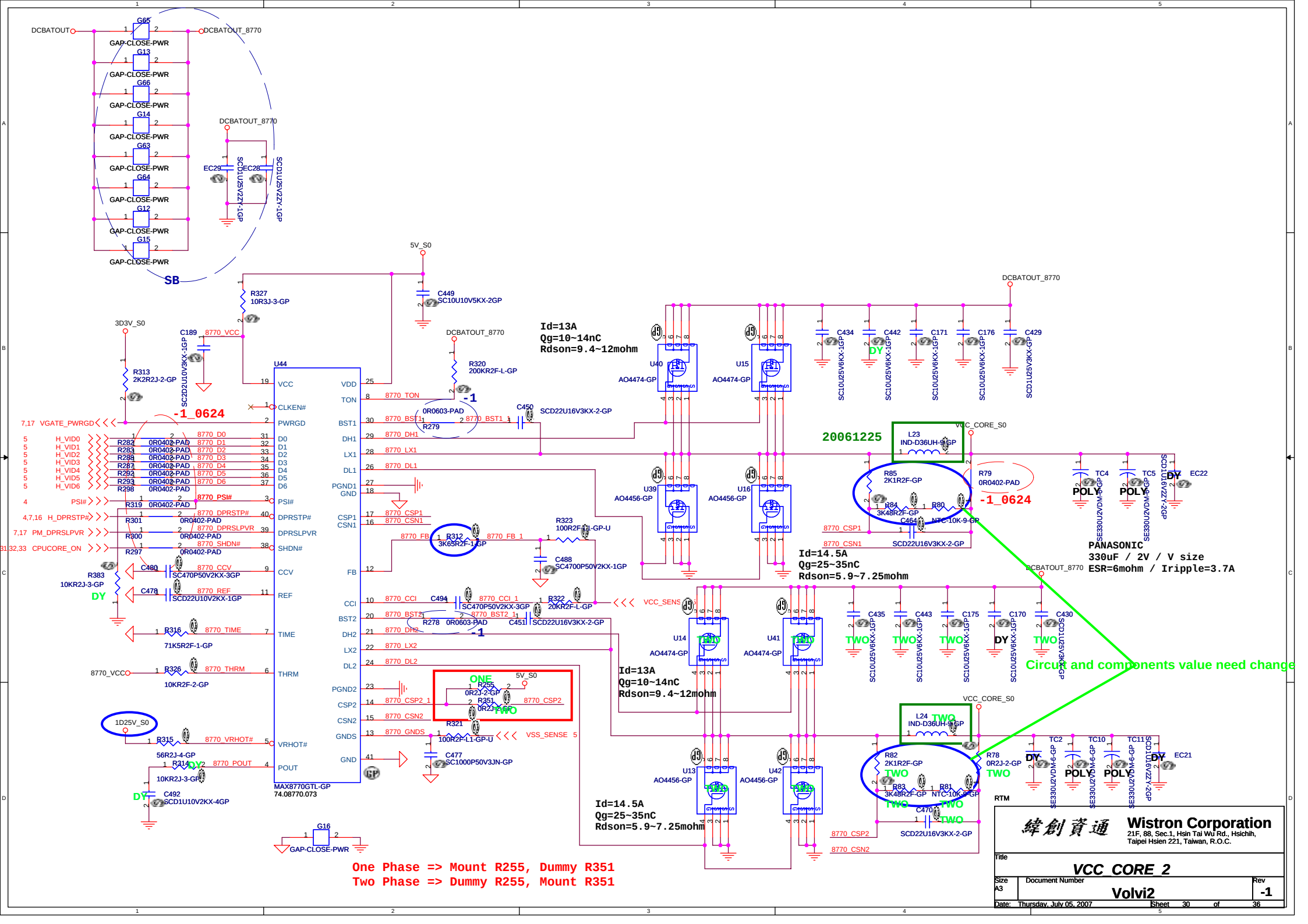
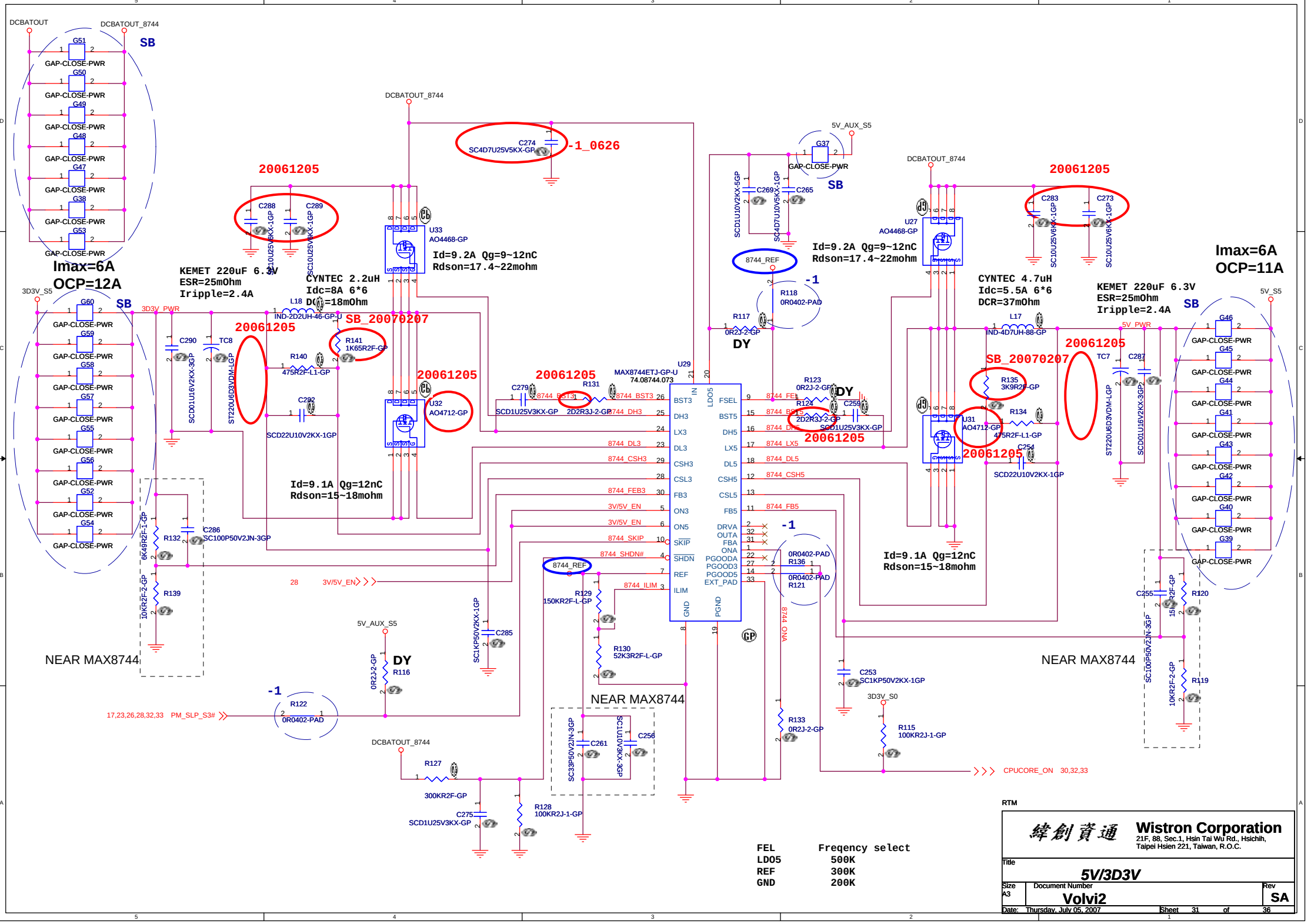
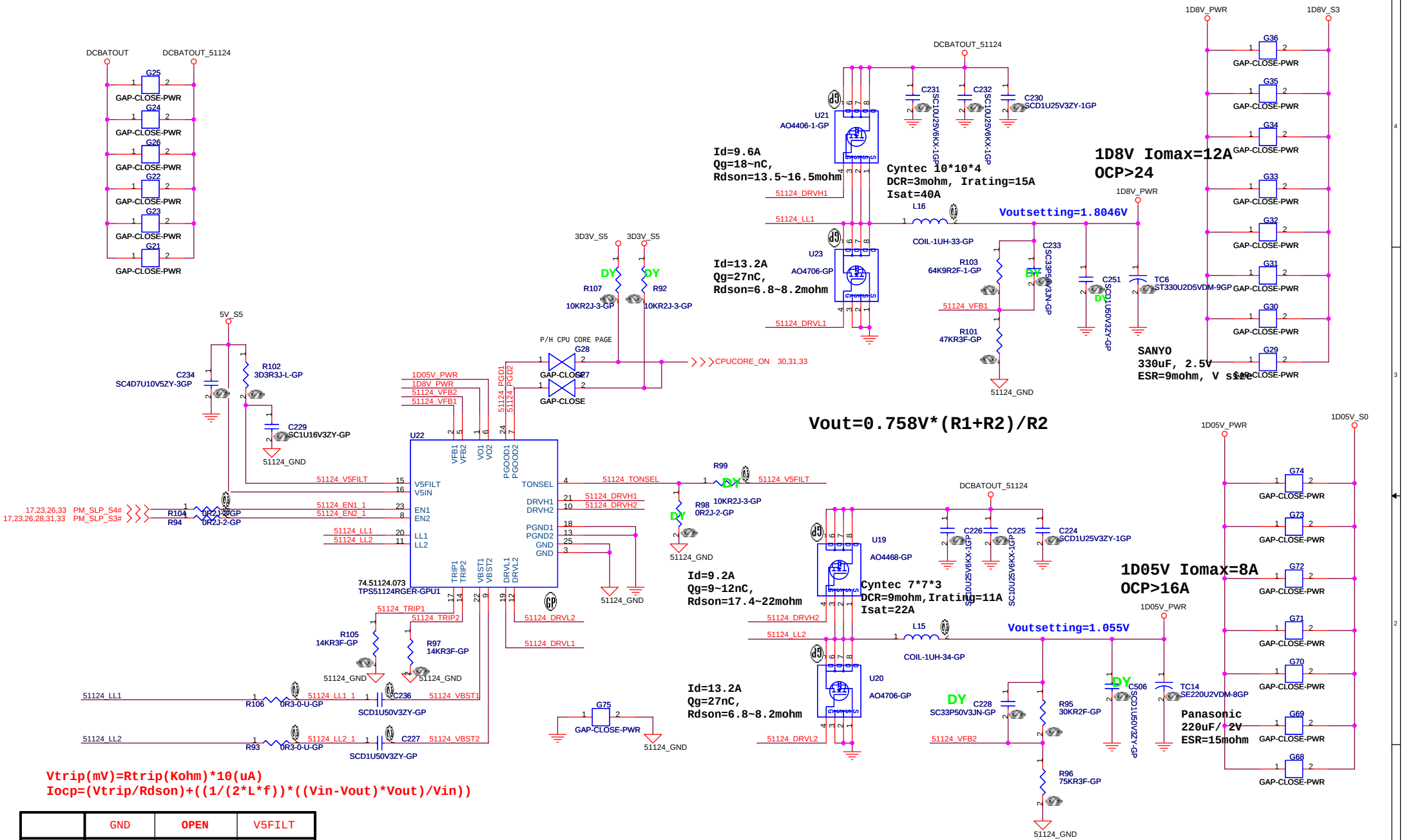

DCBATOUT
DCBATOUT_8770
G65
G13
G66
G14
G63
G64
G12
G15
GAP-CLOSE-PWR
SB
EC29
EC28
SCD1U25V2ZY-1GP
5V_S0
3D3V_S0
R327
10R3J-3-GP
C449
SC10U10V5KX-2GP
C189
8770_VCC
SC2D2U10V3KX-1GP
R313
2K2R2J-2-GP
U44
MAX8770GTL-GP
74.08770.073
-1_0624
7,17 VGATE_PWRGD
5 H_VID0
5 H_VID1
5 H_VID2
5 H_VID3
5 H_VID4
5 H_VID5
5 H_VID6
4 PSI#
4,7,16 H_DPRSTP#
7,17 PM_DPRSLPVR
31,32,33 CPUCORE_ON
R282 0R0402-PAD
R283 0R0402-PAD
R286 0R0402-PAD
R287 0R0402-PAD
R292 0R0402-PAD
R293 0R0402-PAD
R298 0R0402-PAD
R319 0R0402-PAD
R301 0R0402-PAD
R300 0R0402-PAD
R297 0R0402-PAD
R383
10KR2J-3-GP
DY
C480
SC470P50V2KX-3GP
C479
SCD22U10V2KX-1GP
R316
71K5R2F-1-GP
R326
10KR2F-2-GP
1D25V_S0
R315
56R2J-4-GP
R314
10KR2J-3-GP
C492
SCD1U10V2KX-4GP
G16
GAP-CLOSE-PWR
VCC
CLKEN#
PWRGD
D0
D1
D2
D3
D4
D5
D6
PSI#
DPRSTP#
DPRSLPVR
SHDN#
CCV
REF
TIME
THRM
VRHOT#
POUT
VDD
TON
BST1
DH1
LX1
DL1
PGND1
GND
CSP1
CSN1
FB
CCI
BST2
DH2
LX2
DL2
PGND2
CSP2
CSN2
GNDS
GND
8770_D0
8770_D1
8770_D2
8770_D3
8770_D4
8770_D5
8770_D6
8770_PSI#
8770_DPRSTP#
8770_DPRSLPVR
8770_SHDN#
8770_CCV
8770_REF
8770_TIME
8770_THRM
8770_VRHOT#
8770_POUT
8770_TON
8770_BST1
8770_DH1
8770_LX1
8770_DL1
8770_CSP1
8770_CSN1
8770_FB
8770_CCI
8770_BST2
8770_DH2
8770_LX2
8770_DL2
8770_CSP2_1
8770_CSN2
8770_GNDS
R320
200KR2F-L-GP
-1
0R0603-PAD
R279
C450
SCD22U16V3KX-2-GP
R312
3K65R2F-1-GP
R323
100R2F-L1-GP-U
C488
SC4700P50V2KX-1GP
C494
SC470P50V2KX-3GP
8770_CCI_1
R322
20KR2F-L-GP
VCC_SENS 5
R278 0R0603-PAD
C451
SCD22U16V3KX-2-GP
8770_BST2_1
ONE
R255
0R2J-2-GP
R351
0R2J-2-GP
TWO
8770_CSP2
R321
100R2F-L1-GP-U
VSS_SENSE 5
C477
SC1000P50V3JN-GP
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
U40
U15
AO4474-GP
C434
C442
C171
C176
C429
SC10U25V6KX-1GP
SCD1U25V3KX-GP
U39
U16
AO4456-GP
20061225
L23
IND-D36UH-9GP
VCC_CORE_S0
R85
2K1R2F-GP
R79
0R0402-PAD
R84
3K48R2F-GP
R80
C464
NTC-10K-9-GP
8770_CSP1
8770_CSN1
SCD22U16V3KX-2-GP
TC4
TC5
EC22
POLY
SE330U2VDM-6-GP
SCD1U16V2ZY-2GP
PANASONIC
330uF / 2V / V size
ESR=6mohm / Iripple=3.7A
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
U14
U41
C435
C443
C175
C170
C430
TWO
Circuit and components value need change
L24
R82
2K1R2F-GP
R83
3K48R2F-GP
R81
NTC-10K-9-GP
C470
R78
0R2J-2-GP
TC2
TC10
TC11
EC21
U13
U42
RTM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VCC_CORE_2
Size
A3
Document Number
Volvi2
Rev
-1
Date: Thursday, July 05, 2007
Sheet 30 of 36
One Phase => Mount R255, Dummy R351
Two Phase => Dummy R255, Mount R351



FEL	Freqency select
LDO5	500K
REF	300K
GND	200K



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	**300k/CH1** **360k/CH2**	360k/CH1 420k/CH2

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Title: ***TPS51124 1D8V 1D05V***

Size: A3 | Document Number: **Volvi2** | Rev: **SA**

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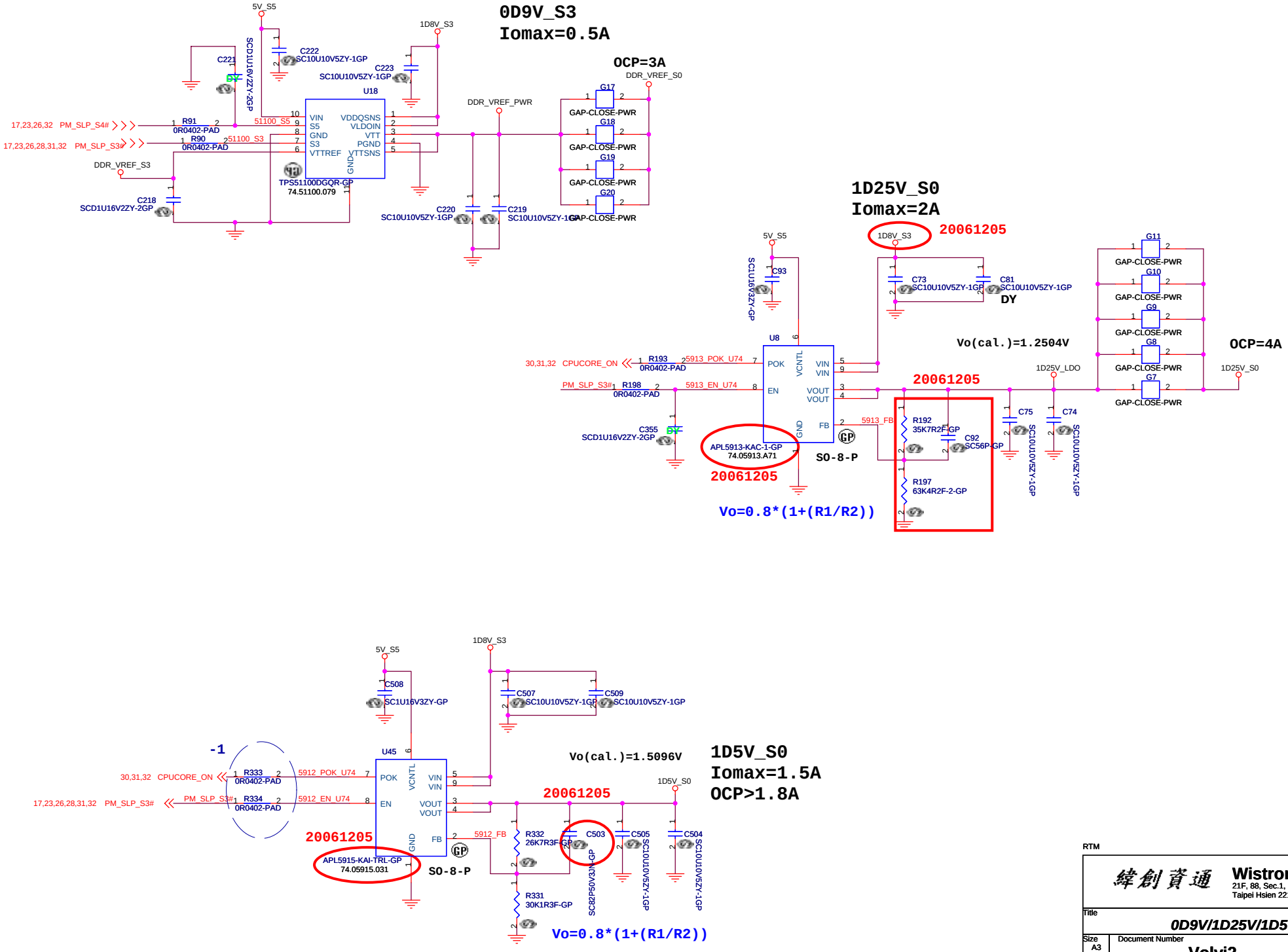

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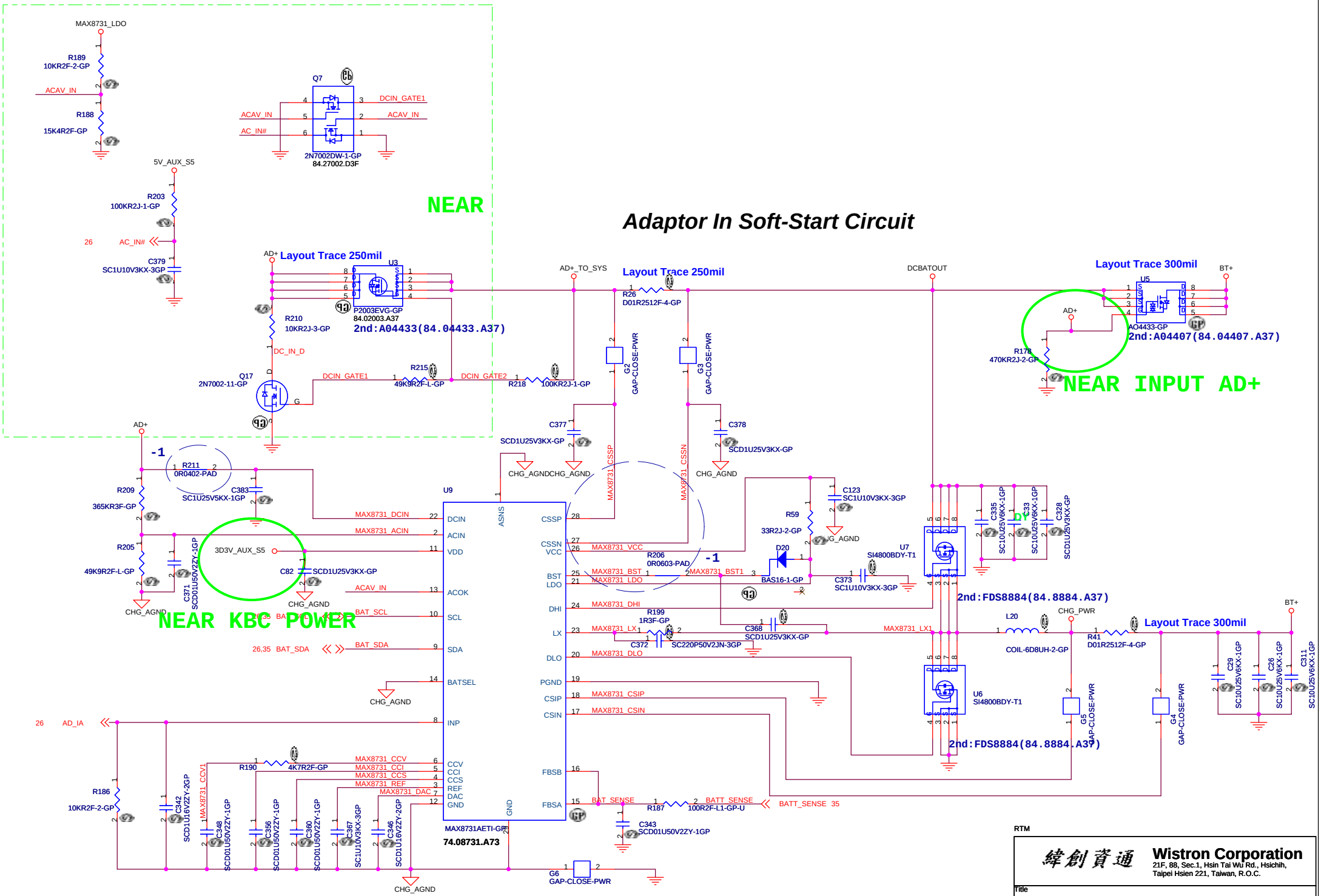
Title: 0D9V/1D25V/1D5V

Size: A3 | Document Number: Volvi2 | Rev: SB

Date: Thursday, July 05, 2007 | Sheet 33 of 36



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Title: CHARGER MAX8731

Size: A3 | Document Number: Volvi960 | Rev: SA

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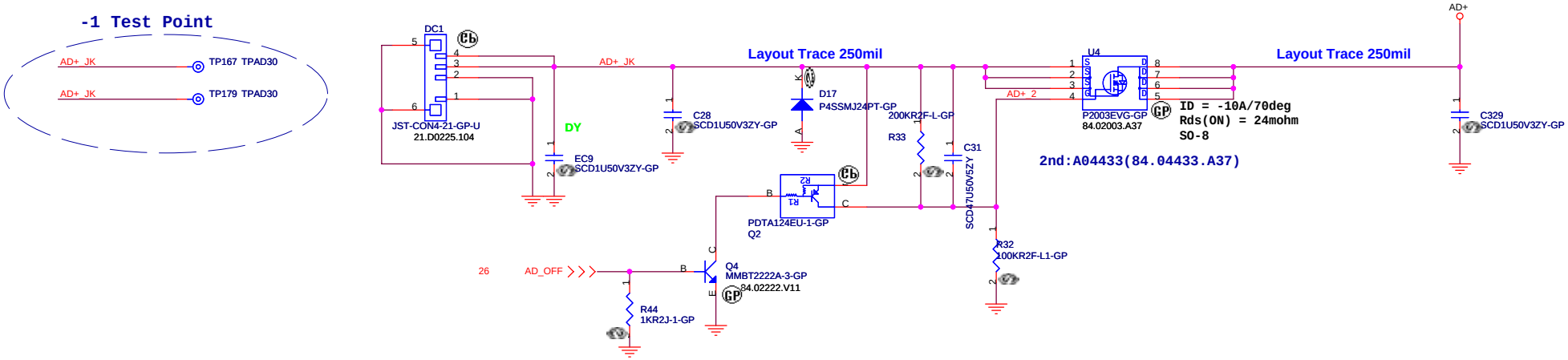
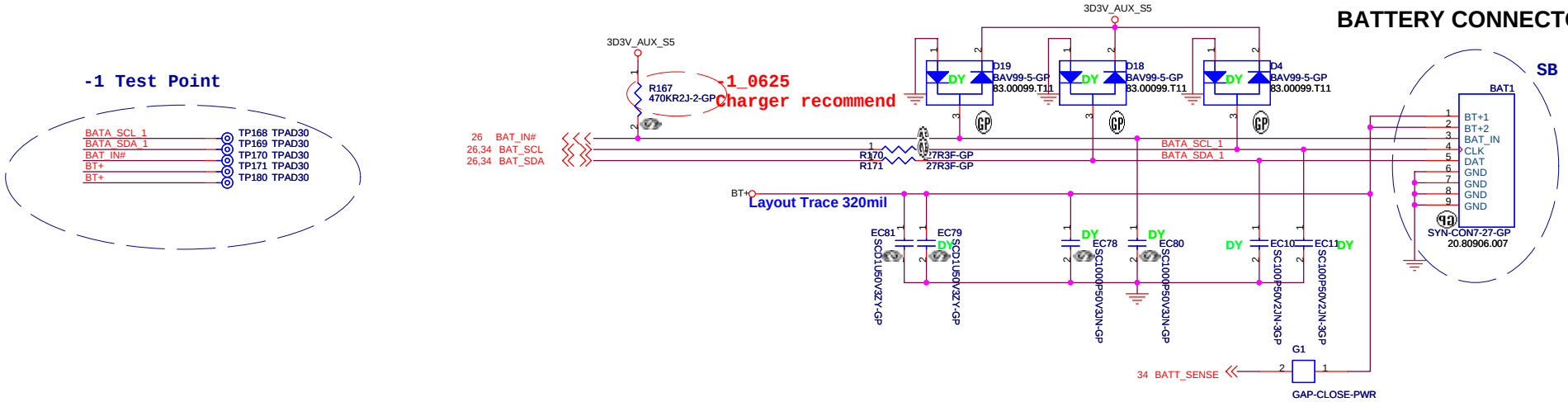
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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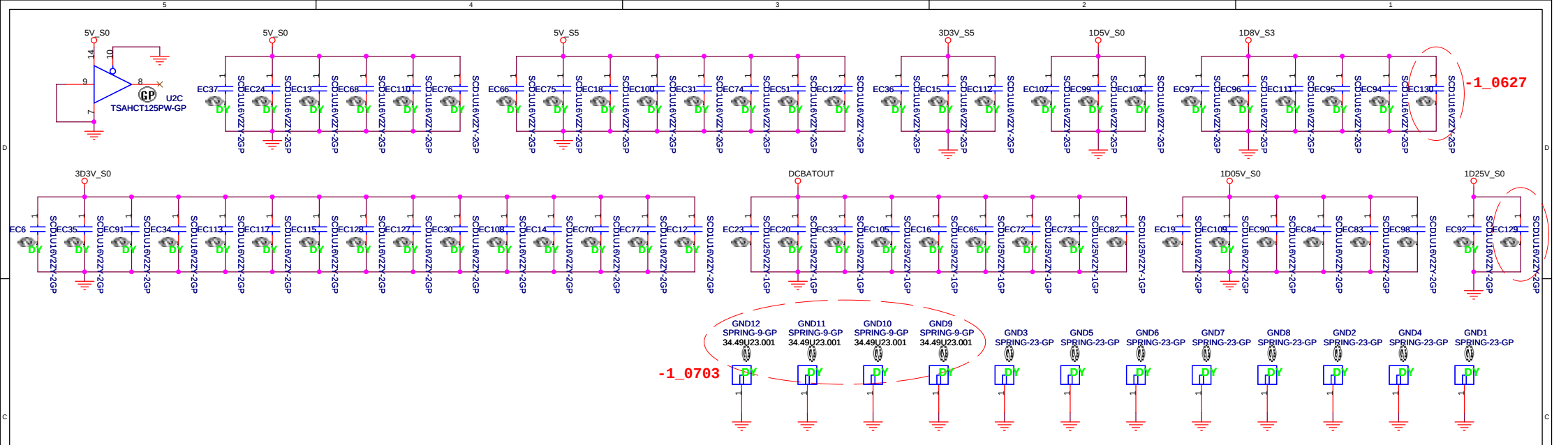
Title	**AD/BATT CONN**
Size A3	Document Number **Volvi2** Rev **-1**
Date: Thursday, July 05, 2007	Sheet 35 of 36



FAN CONN

20	FAN1_VCC	FAN1_VCC	TP172 TPAD30
20	FAN1_FG1	FAN1_FG1	TP100 TPAD30
20,26,28	PURE_HW_SHUTDOWN#	PURE_HW_SHUTDOWN#	TP101 TPAD30

USB ZIF CONN

Test Point

5V_S5		TP176 TPAD30
5V_S5		TP175 TPAD30
17,21 USBPN2	USBPN2	TP104 TPAD30
17,21 USBPP2	USBPP2	TP105 TPAD30
17,21 USBPN4	USBPN4	TP106 TPAD30
17,21 USBPP4	USBPP4	TP107 TPAD30
17,21 USB_OC#4	USB_OC#4	TP108 TPAD30
21,26 USB_PWR_EN#	USB_PWR_EN#	TP109 TPAD30

Internal Microphone

24,25 INT_MIC1_CN	INT_MIC1_CN	TP110 TPAD30

Audio Connector

24,25 LINEOUT_JD#	LINEOUT_JD#	TP111 TPAD30
25 SPKR_R+1	SPKR_R+1	TP150 TPAD30
25 SPKR_L+1	SPKR_L+1	TP151 TPAD30
24,25 MIC_JD#	MIC_JD#	TP152 TPAD30
24,25 AUD_MICIN_R	AUD_MICIN_R	TP153 TPAD30
24,25 AUD_MICIN_L	AUD_MICIN_L	TP154 TPAD30

Internal Speaker

25 SPKR_L-	SPKR_L-	TP112 TPAD30
25 SPKR_L+	SPKR_L+	TP113 TPAD30
25 SPKR_R-	SPKR_R-	TP114 TPAD30
25 SPKR_R+	SPKR_R+	TP115 TPAD30

Internal KeyBoard CONN

26,27 KROW[1..8]	KROW[1..8]	
26,27 KCOL[1..18]	KCOL[1..18]	

Test Point

KCOL1	TP116 TPAD30
KCOL2	TP117 TPAD30
KCOL3	TP118 TPAD30
KCOL4	TP119 TPAD30
KCOL5	TP120 TPAD30
KCOL6	TP121 TPAD30
KCOL7	TP122 TPAD30
KCOL8	TP123 TPAD30
KCOL9	TP124 TPAD30
KCOL10	TP125 TPAD30
KCOL11	TP126 TPAD30
KCOL12	TP127 TPAD30
KCOL13	TP128 TPAD30
KCOL14	TP129 TPAD30
KCOL15	TP130 TPAD30
KCOL16	TP131 TPAD30
KCOL17	TP132 TPAD30
KCOL18	TP133 TPAD30
KROW1	TP134 TPAD30
KROW2	TP135 TPAD30
KROW3	TP136 TPAD30
KROW4	TP137 TPAD30
KROW5	TP138 TPAD30
KROW6	TP139 TPAD30
KROW7	TP140 TPAD30
KROW8	TP141 TPAD30

TRING CONN

Test Point

22 TIP_C	TIP_C	TP174 TPAD30
22 RING_C	RING_C	TP173 TPAD30

Touch Pad CONN

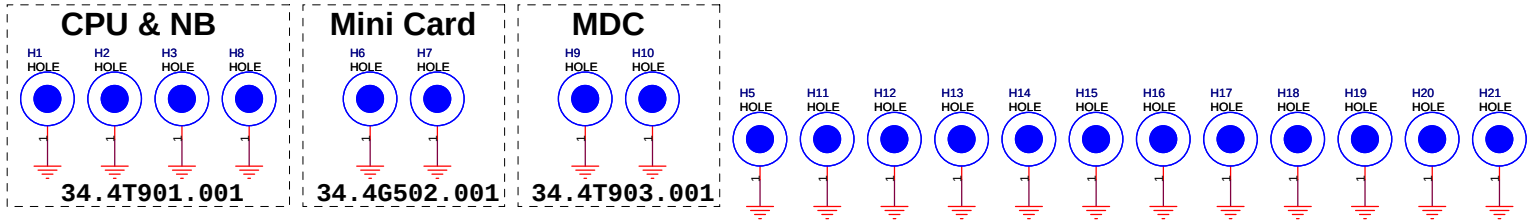
Test Point near TPAD1

5V_S0		TP177 TPAD30
27 TP_DATA	TP_DATA	TP142 TPAD30
27 TP_CLK	TP_CLK	TP143 TPAD30
27 TP_RIGHT	TP_RIGHT	TP144 TPAD30
27 TP_SCROLL_RIGHT	TP_SCROLL_RIGHT	TP145 TPAD30
27 TP_SCROLL_UP	TP_SCROLL_UP	TP146 TPAD30
27 TP_SCROLL_LEFT	TP_SCROLL_LEFT	TP147 TPAD30
27 TP_SCROLL_DOWN	TP_SCROLL_DOWN	TP148 TPAD30
27 TP_LEFT	TP_LEFT	TP149 TPAD30

Check test point

3D3V_S0	TP178 TPAD30
3D3V_AUX_S5	TP1 TPAD30
3D3V_S5	TP54 TPAD30
5V_S5	TP51 TPAD30
17,26 PM_PWRBTN#	TP50 TPAD30
4,16,28 H_PWRGD	TP56 TPAD30
26,28 S5_ENABLE	TP49 TPAD30
4,6 H_CPURST#	TP5 TPAD30

STAND OFF ON BOTTOM



Test Point放在Dimm Door打開可量測處

RTM

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *EMI/Spring/Boss*

Size | Document Number: Volvi2 | Rev: -1

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