Biwa Block Diagram

Project code: 91.4H001.001
PCB P/N : 55.4H001.XXX
REVISION : 06237-2(GCE, Hannstar)

-2-0226

CLK GEN.
ICS 9LPR502
(RTM875T-605) 3

Mobile CPU
Merom 479
2G/2.33G
2.0G : B0, QLYV
2.2G : B0, QLFS
4, 5

G792 20

HOST BUS 800MHz@1.05V

DDR2 533/667 MHz 12,13
533/667MHz

DDR2 533/667 MHz 12,13
533/667MHz

Crestline
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
71.CREST.M02, B0, QN12
6,7,8,9,10,11

SVIDEO/COMP → TVOUT 15
LVDS → 14" WXGA LCD 14
RGB CRT → CRT 15

X4 DMI
400M Byte/s
C-Link0

ICH8M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 1.1
3 SATA
1 PATA 66/100
10 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
71.0ICH8.A0U, B1, QN23
16,17,18,19

Line In 30
Mic In 30
INT.MIC
INT.SPKR 30
Line Out (No-SPDIF) 30

Codec ALC268 29
AZALIA

OP AMP APA2031 30
G1412 30
MODEM MDC Card 22
RJ11 24

PCI BUS

TI 7412 CardBus 1394 CardReader 25,26
PCMCIA I/F
PWR SW TPS2211 27
PCMCIA SLOT Support TypeII 27
1394 CONN 26
MS/MS Pro/xD/ MMC/SD/SDIO 6 in 1 27

LAN Giga LAN BCM5787MKMLG 23
TXFM 24
RJ45 24

New card 28
PWR SW P2231NFC 28

PCIex1
Mini Card Kedron a/b/g/n 28
C Link1

LPC BUS

SATA
PATA

HDD 21
USB 4 PORT 22
CCD 14
CDROM 21
MINI USB Blue-tooth 22
Finger PT 22

Super I/O Winbond PC87381 33
FIR 32

KBC Winbond WPC8763L 31
SPI I/F
BIOS W25X80-VSSI-G 33
Touch Pad 32
INT. KB 32

LPC DEBUG CONN. 33

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

CPU DC/DC MAX8770 36	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

SYSTEM DC/DC ISL6236 37	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(5A) 3D3V_S5(5A) 5V_AUX_S5

SYSTEM DC/DC MAX8717 38	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(13A) 1D8V_S3(10A)

G971 39	
1D8V_S3	1D5V_S0 (4A)

APL5913 39	
1D8V_S3	1D25V_S0 (1.5A)

G2997F6U 39	
1D8V_S3	DDR_VREF_S0 (1.2A) DDR_VREF_S3

G909 34	
5V_AUX_S5	3D3V_AUX_S5 (100mA)

MAXIM CHARGER ISL6255 40	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 19V 4.0A UP+5V 5V 100mA

55.4H001.S03G

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Title: BLOCK DIAGRAM
Size: A3 | Document Number: Biwa | Rev: -2
Date: Thursday, March 01, 2007 | Sheet 1 of 42

ICH8M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	USB3
3	USB4
4	MINIC1
5	BT
6	CCD
7	Finger
8	NEW
9	NC

ICH8M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K (?)
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K (?)
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Crestline Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode **1 = Low Power mode** (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO Card present** (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWORK in signal.

History

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2007/02/16
1.Page 33: Add SIO 87381 for FIR Issue.
2.Page 31, change KBC from 8768L to 8763L.
3.Page 33, del U33(LPC golden Finger).
4.Page 24/32, change ERC1/ERC2 due to 77.61021.02L is Obsoleted Part !
5.Page 37, del TC22/TC19.
6.Page 38, del TC1/TC4.
============================================================
2007/02/09
1.Page 14:Modify "Q14" "BTBTN1" "WLBTN1" symbol.
2.Page 36, 37, 38: Replace 0ohm with 0ohm pad.
============================================================
2007/02/08a
1.Page 14:Modify R428 to“FRONT_PWRLED#_1”and RN58 pin7 to“STBY_LED#_2”due to LED brightness issue.
2.Page 38:Replace "TC26" with "77.C1561.01L".
============================================================
2007/02/08
1.Page 10:Replace "R244" with "0603-PAD".
2.Page 36:Replace open power gap with close power gap.
3.Page 38:Add capacitor "TC26" for acoustic noise
============================================================
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55.4H001.S03G

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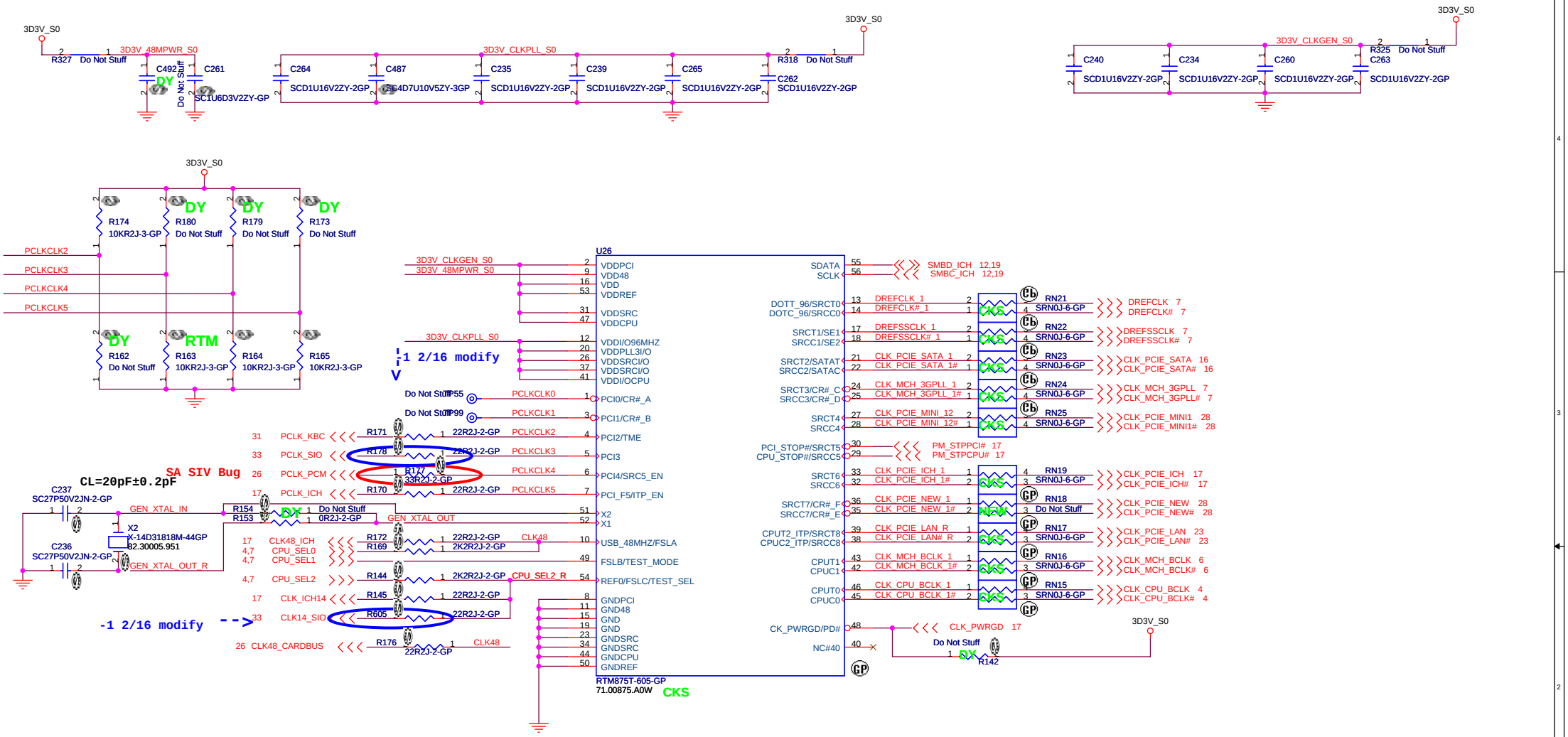
Title: **Reference**

Size	Document Number	Rev
A3	Biwa	-2

Date: Thursday, March 01, 2007 Sheet 2 of 42



ICS9LPR502HGLFT-GP setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI4/SRC5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

RTM875T-605 setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/SRC-5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

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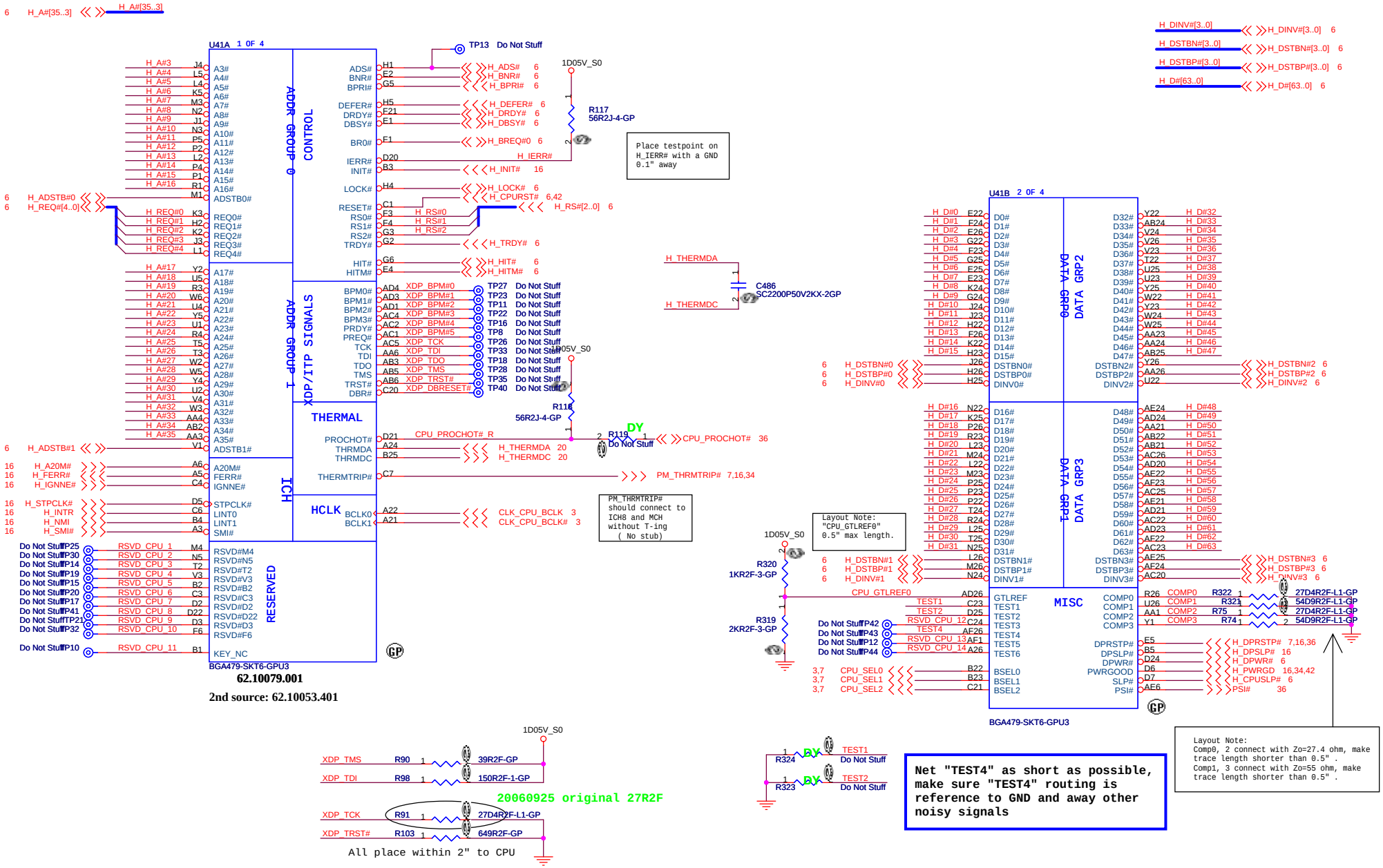
Title: **Clock Generator**

Size | Document Number: Biwa | Rev: -2

Date: Thursday, March 01, 2007 | Sheet 3 of 42



62.10079.001

2nd source: 62.10053.401

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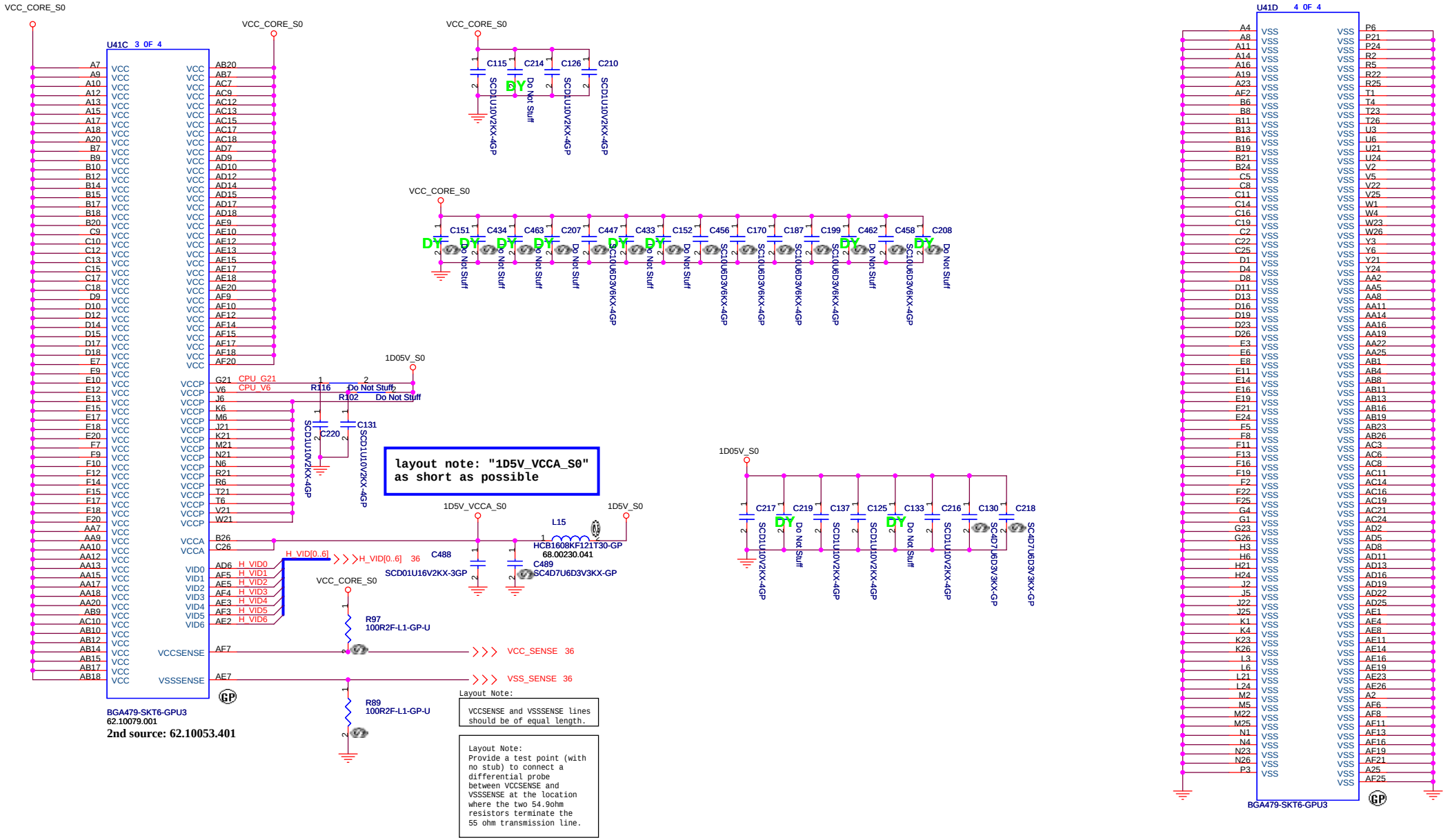
Title: **CPU (1 of 2)**

Size | Document Number: **Biwa** | Rev: SA

Date: Thursday, March 01, 2007 | Sheet 4 of 42



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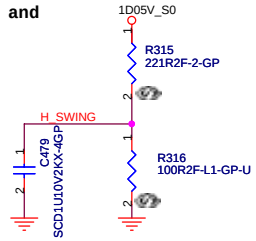
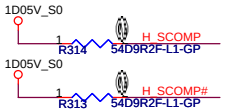
Title	***CPU (2 of 2)***	
Size	Document Number: **Biwa**	Rev: SA
Date: Thursday, March 01, 2007	Sheet 5 of 42	

H_SWING routing Trace width and Spacing use 10 / 20 mil

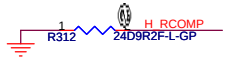
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil (MAX)

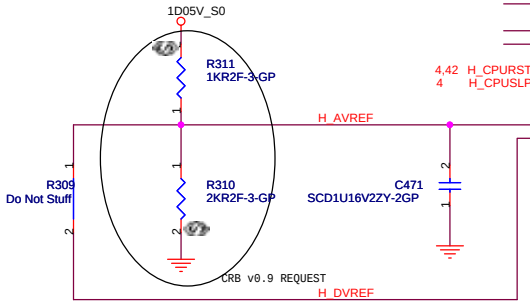


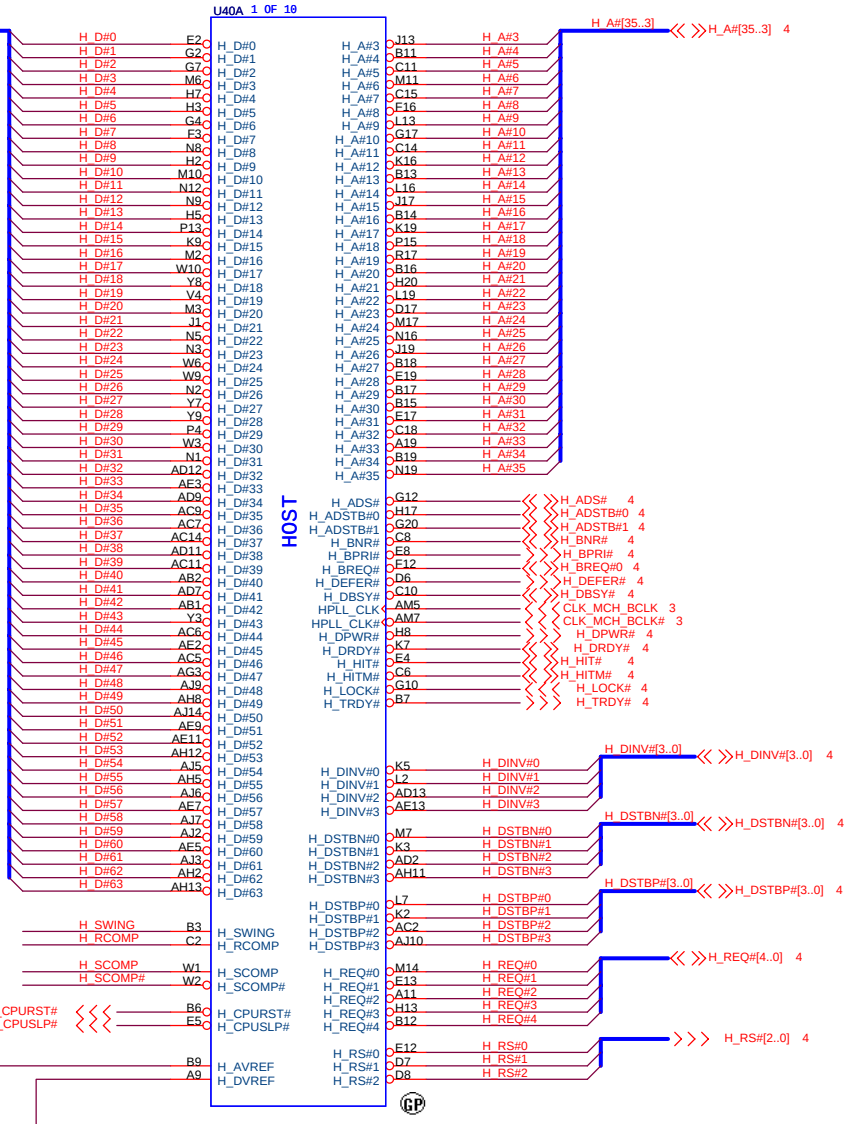
H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")

H_REF Decoupling Crestline close Crestline 100 mil





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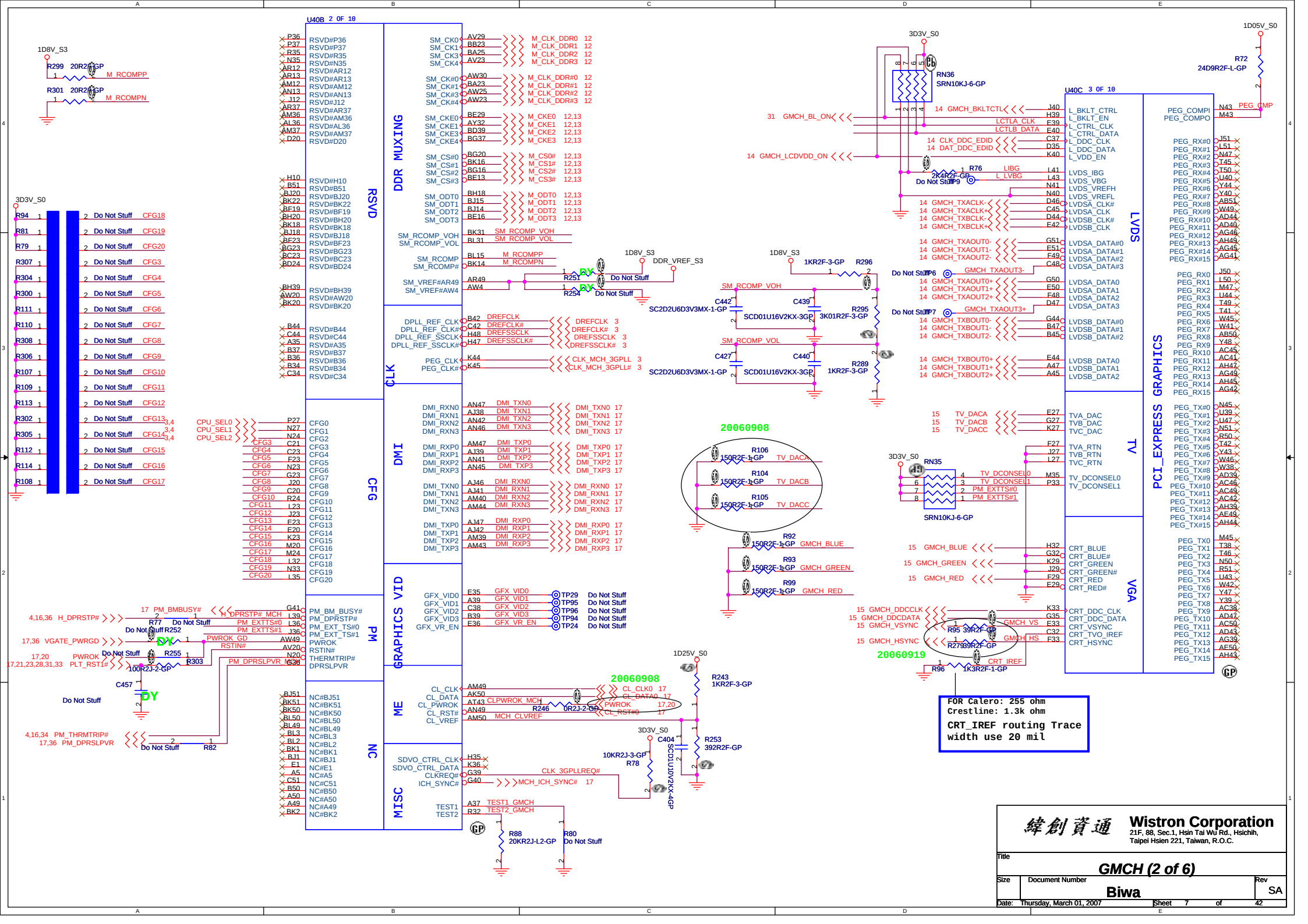
Title	***GMCH (1 of 6)***	
Size	Document Number **Biwa**	Rev SA
Date: Thursday, March 01, 2007	Sheet 6 of 42	


U40B 2 OF 10
RSVD
DDR MUXING
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
U40C 3 OF 10
LVDS
TV
VGA
PCI_EXPRESS GRAPHICS
1D8V_S3
3D3V_S0
1D05V_S0
1D25V_S0
DDR_VREF_S3
SC2D2U6D3V3MX-1-GP
SCD01U16V2KX-3GP
SCD1U10V2KX-4GP
SRN10KJ-6-GP
RN36
SRN10KJ-6-GP
RN35
20060908
20060919
FOR Calero: 255 ohm
Crestline: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
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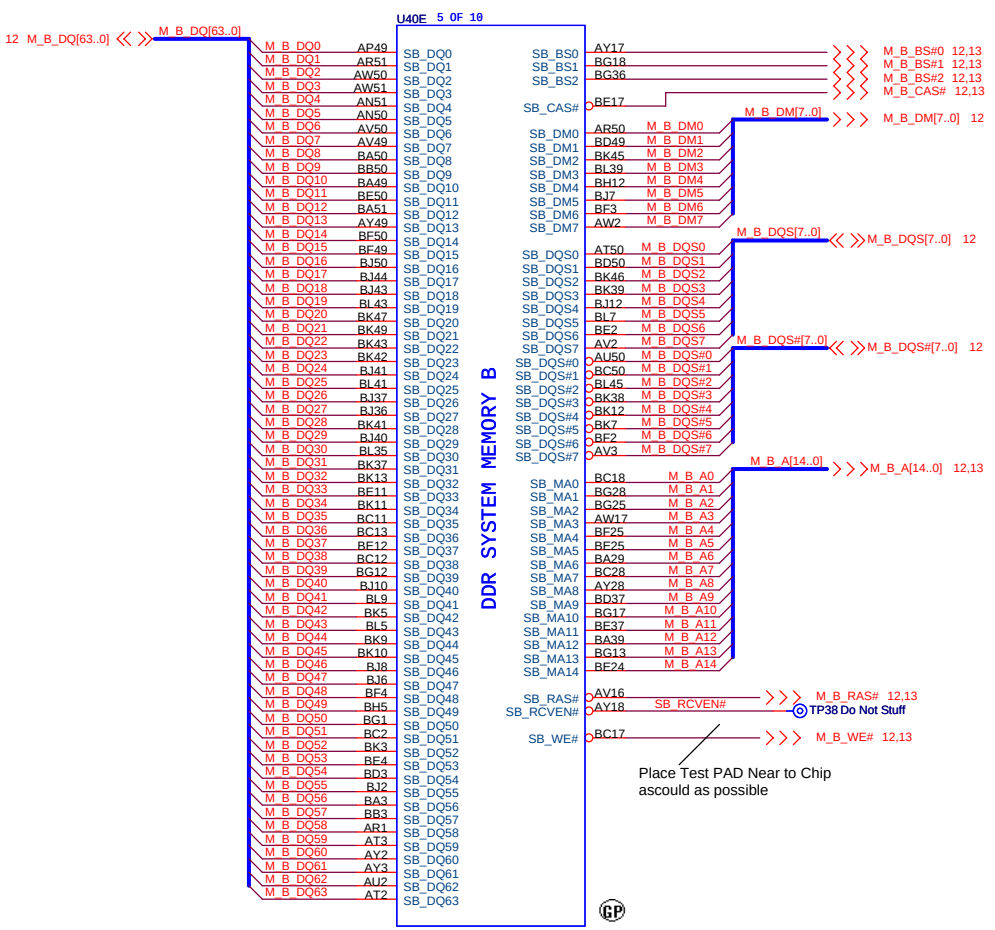
Title
GMCH (2 of 6)
Size
Document Number
Biwa
Rev
SA
Date: Thursday, March 01, 2007
Sheet 7 of 42



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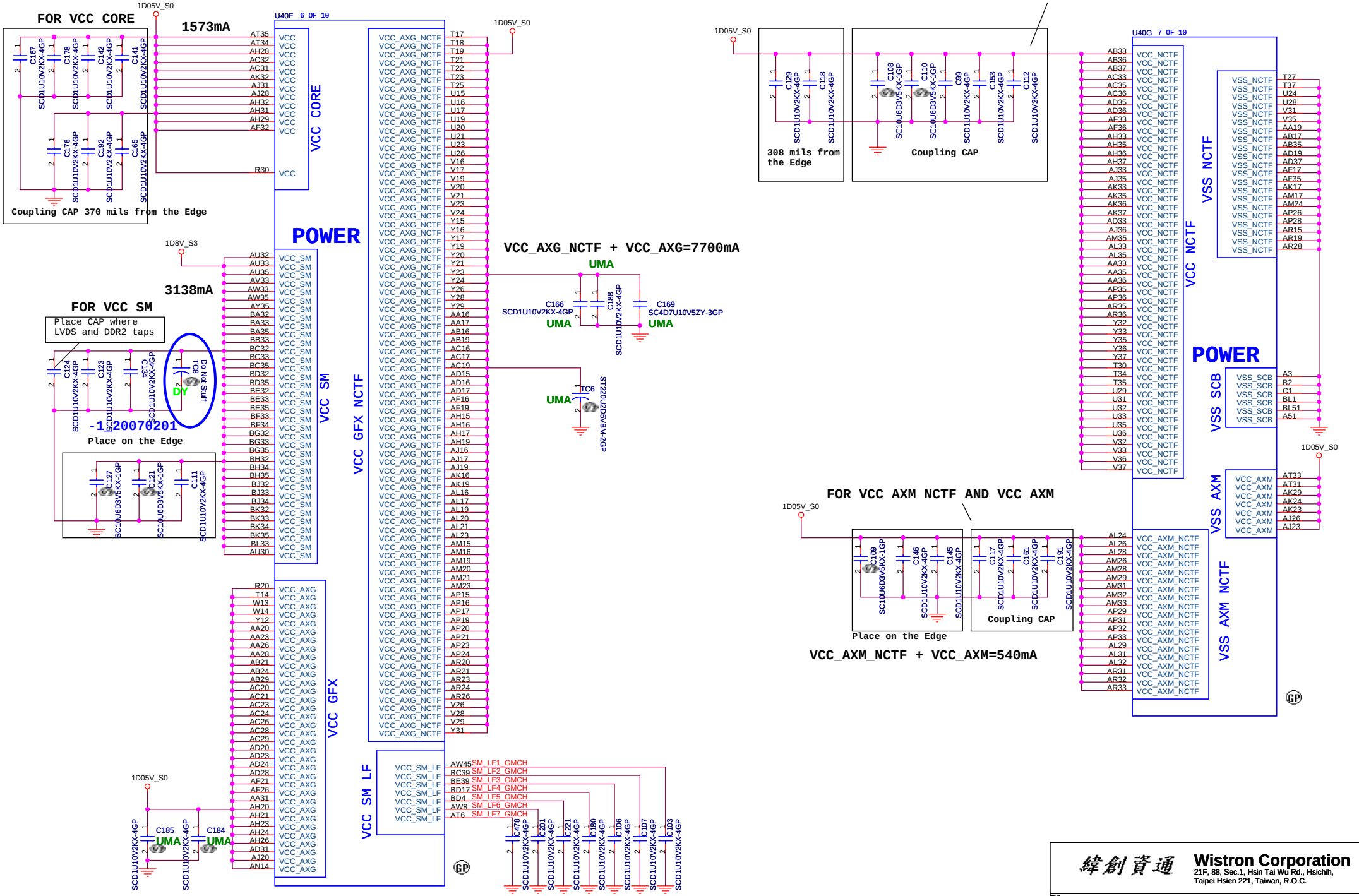
Size	Document Number: **Biwa**	Rev: SA
Date: Thursday, March 01, 2007	Sheet 8 of 42	



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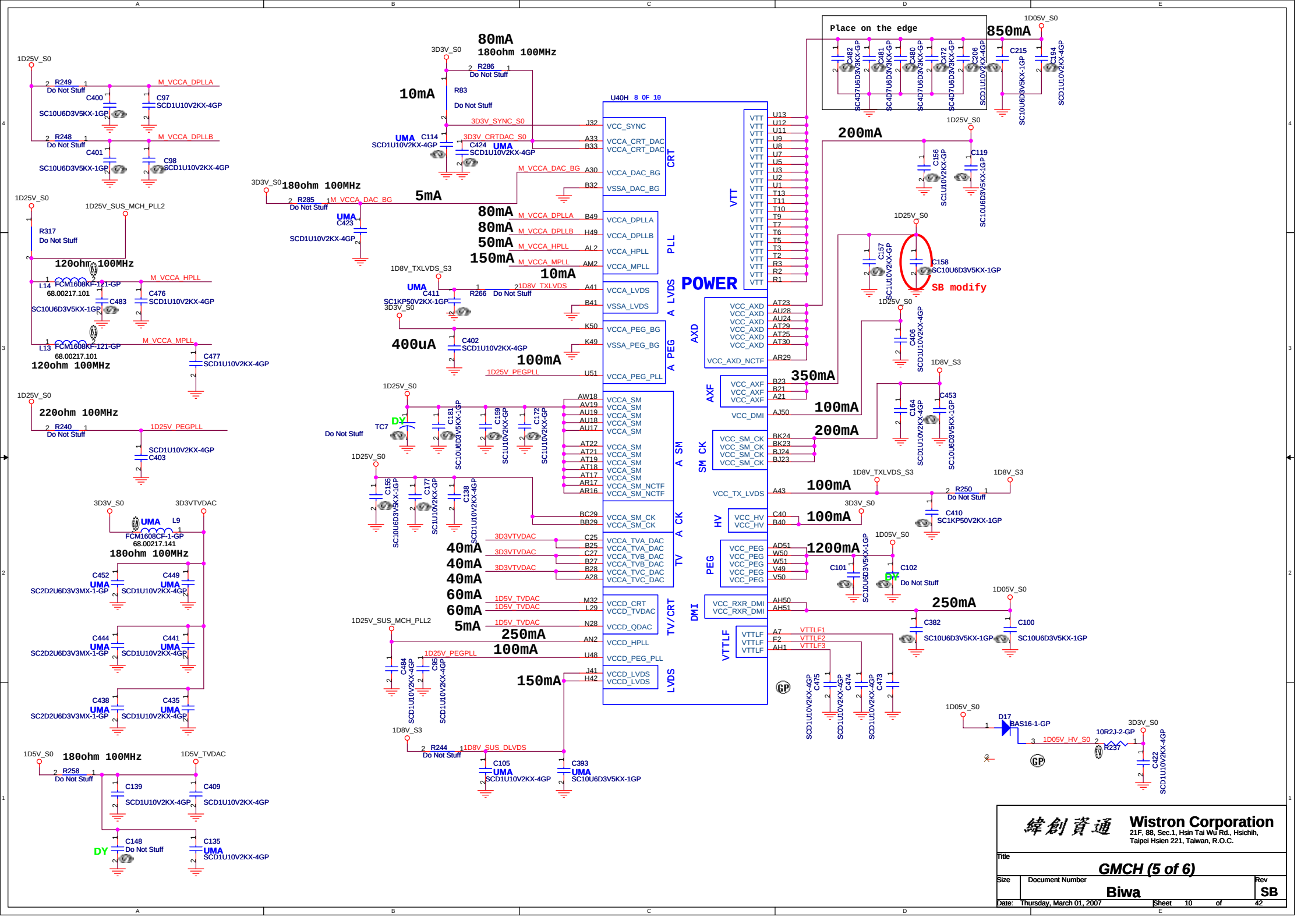
Size	Document Number **Biwa**	Rev -1
Date: Thursday, March 01, 2007	Sheet 9 of 42	


Place on the edge
850mA
200mA
SB modify
80mA
180ohm 100MHz
10mA
5mA
400uA
100mA
150mA
50mA
60mA
40mA
250mA
350mA
1200mA
U40H 8 OF 10
POWER
CRT
PLL
LVDS
SDVO
SM CK
TV
TV/CRT
DMI
VTTLF
AXD
AXF
PEG
HV
VTT
GP
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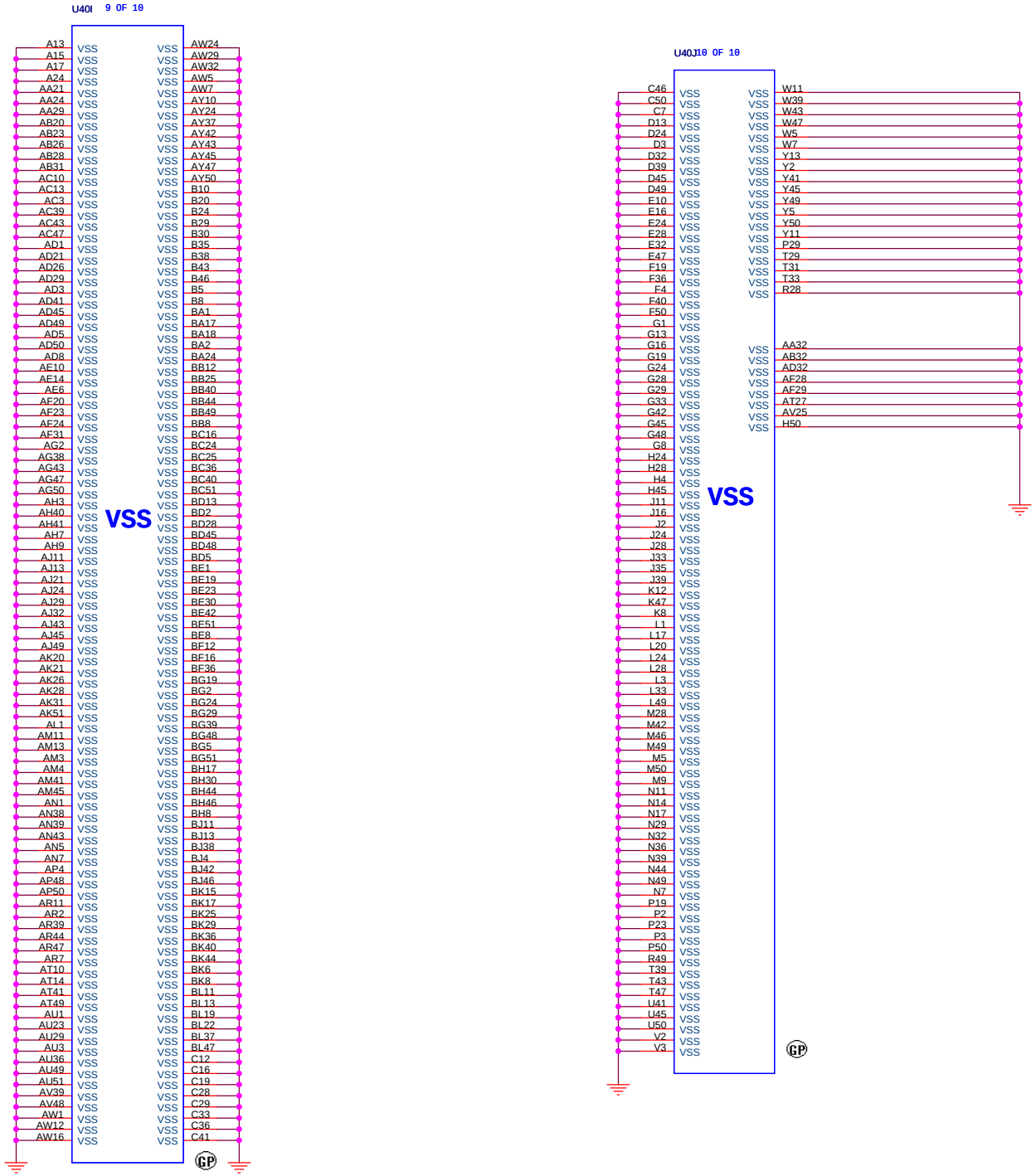
GMCH (5 of 6)
Biwa
SB
Thursday, March 01, 2007
Sheet 10 of 42



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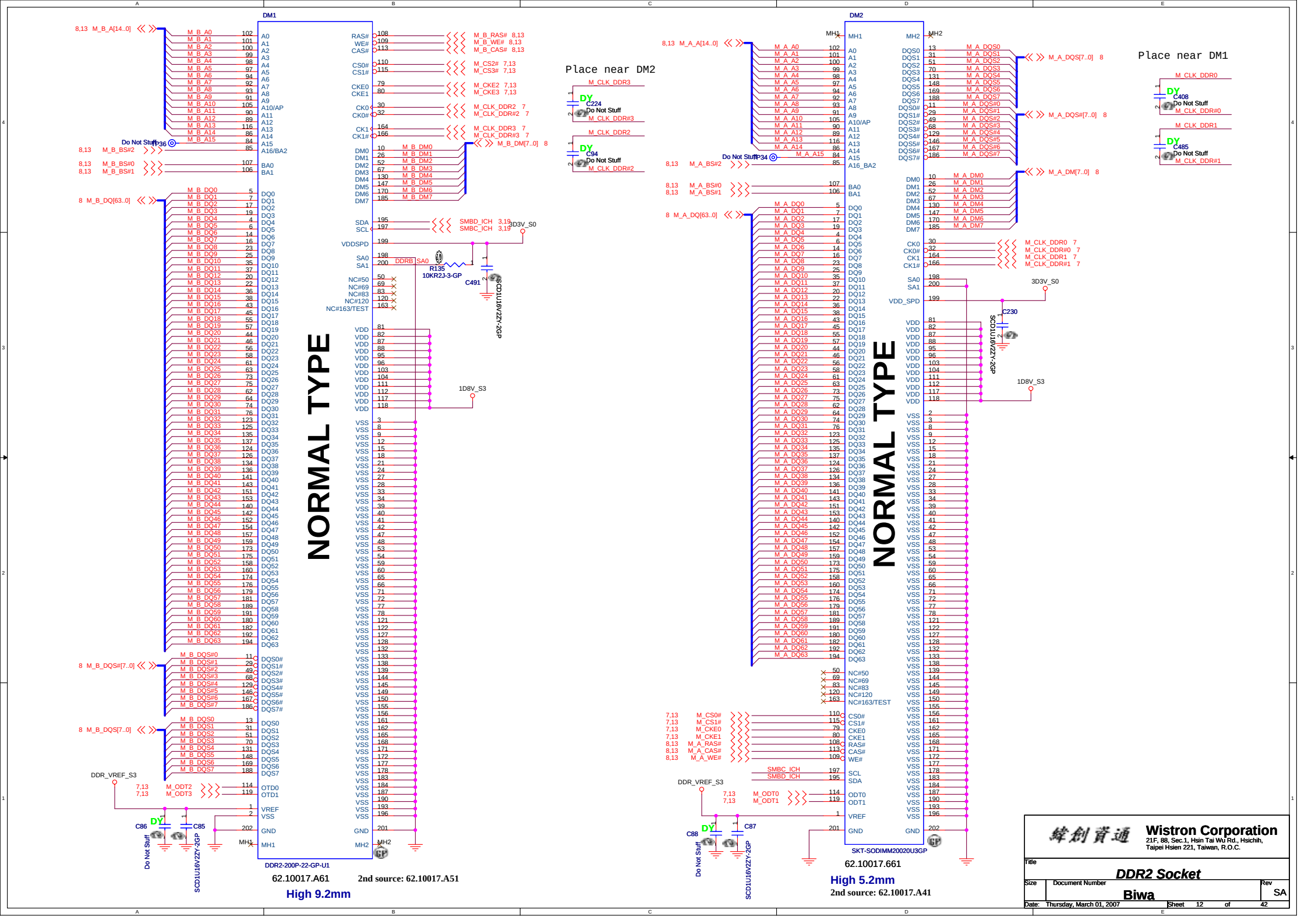
Title	***GMCH (6 of 6)***	
Size	Document Number **Biwa**	Rev SA
Date: Thursday, March 01, 2007	Sheet 11 of 42	


DM1
NORMAL TYPE
DDR2-200P-22-GP-U1
62.10017.A61
2nd source: 62.10017.A51
High 9.2mm
Place near DM2
Place near DM1
DM2
NORMAL TYPE
SKT-SODIMM20020U3GP
62.10017.661
High 5.2mm
2nd source: 62.10017.A41
Do Not Stuff
R135
10KR2J-3-GP
C491
C224
C94
C408
C485
C230
C86
C85
C88
C87
SCD1U16V2ZY-2GP
3D3V_S0
1D8V_S3
DDR_VREF_S3
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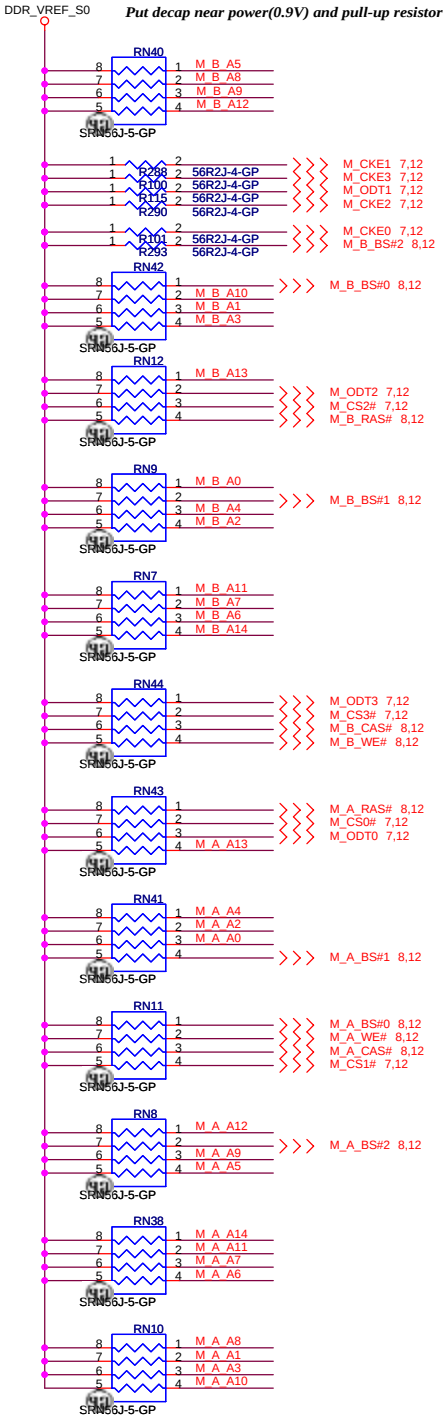
Title
DDR2 Socket
Size
Document Number
Biwa
Rev
SA
Date: Thursday, March 01, 2007
Sheet 12 of 42

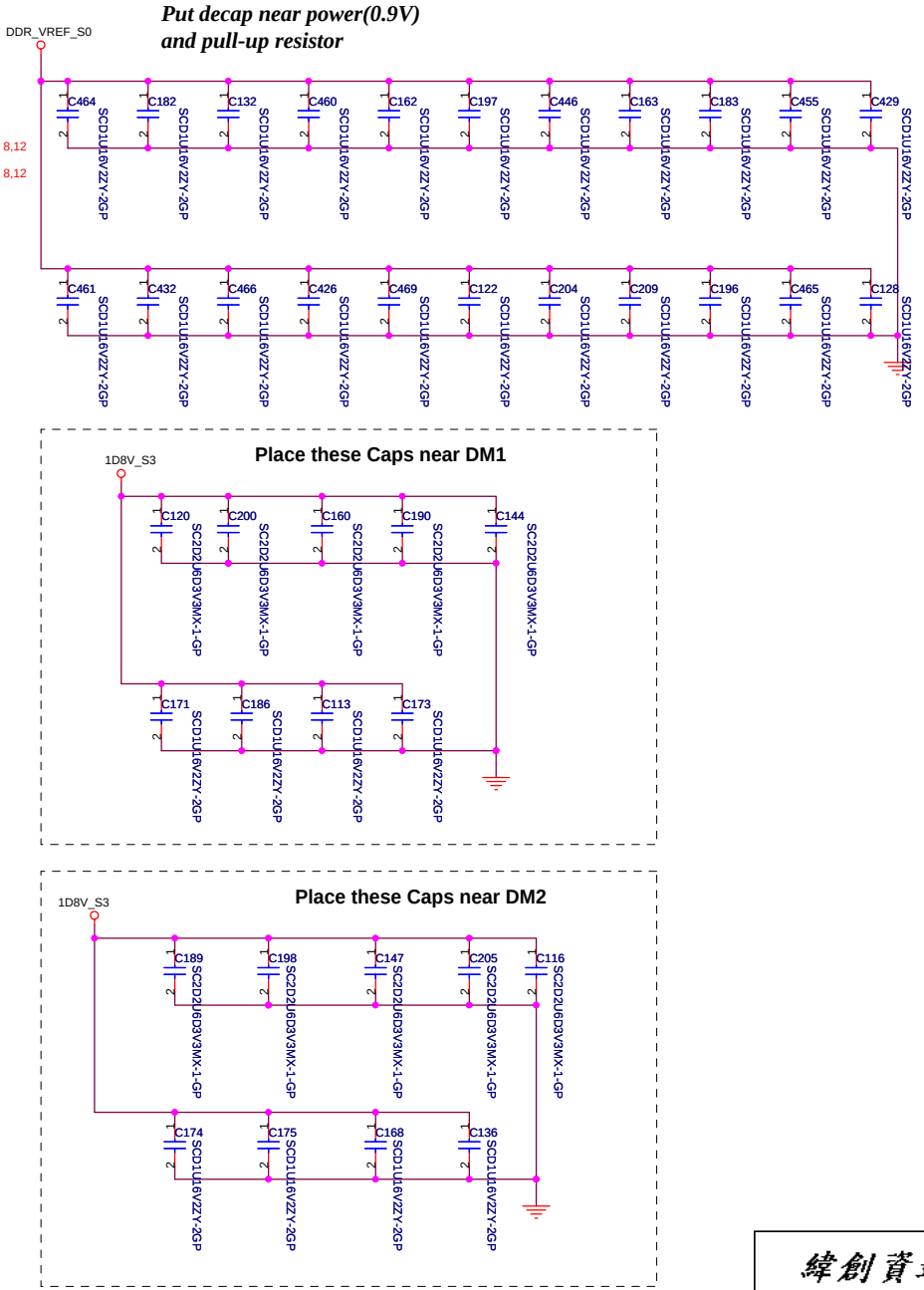
PARALLEL TERMINATION



M_A_A[14..0] <<>> M_A_A[14..0] 8,12

M_B_A[14..0] <<>> M_B_A[14..0] 8,12

Decoupling Capacitor



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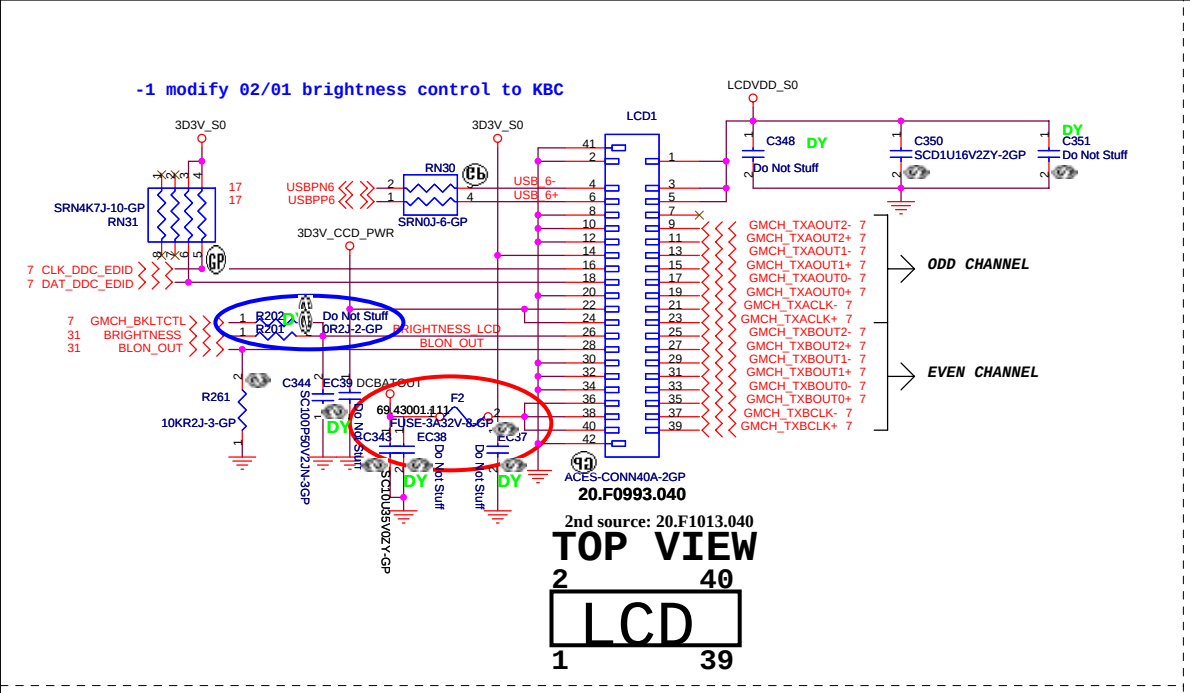
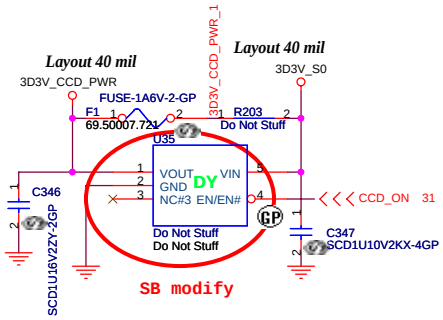
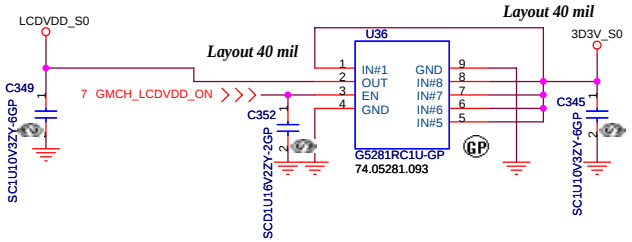
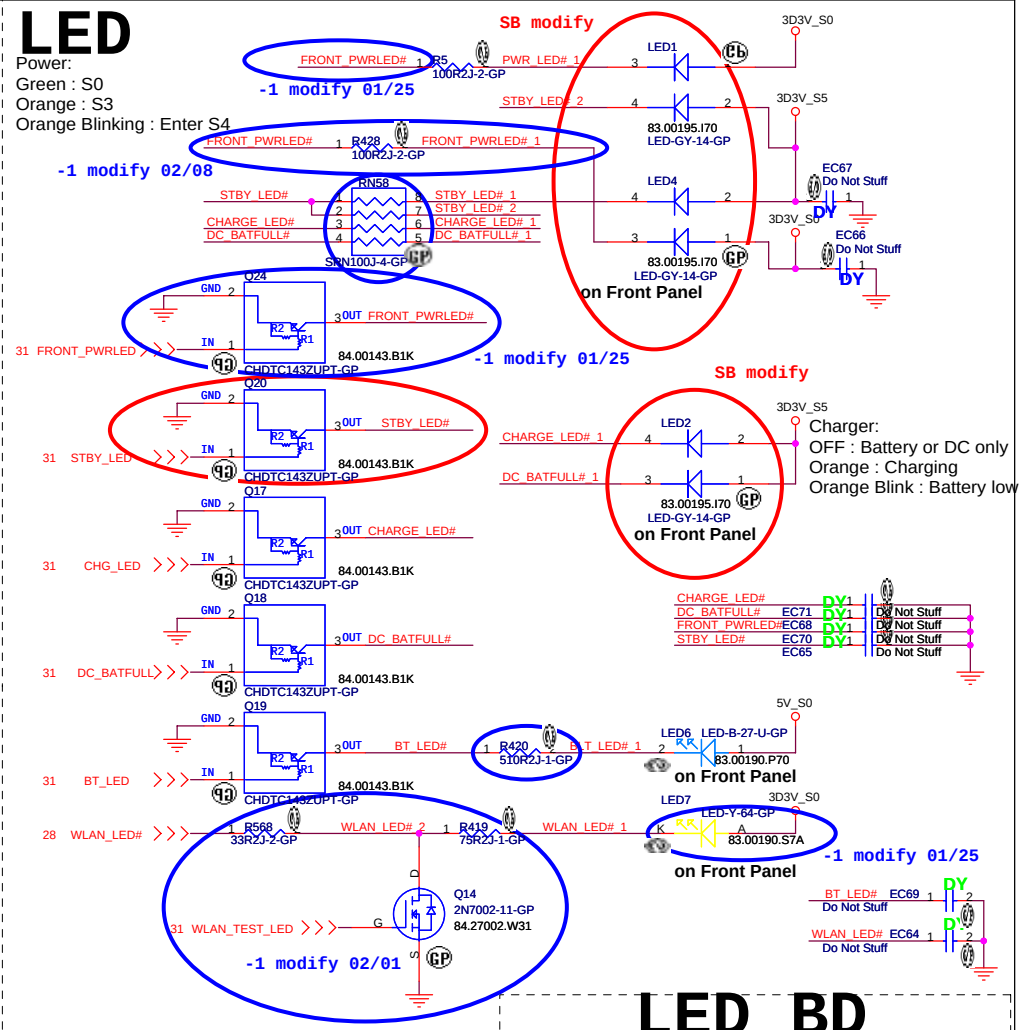
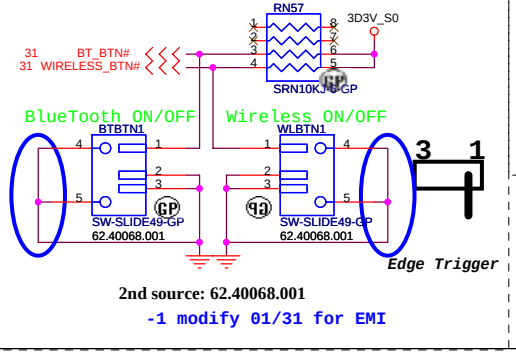
Title: DDR2 Termination Resistor		
Size	Document Number: Biwa	Rev: SB
Date: Thursday, March 01, 2007	Sheet 13 of 42	

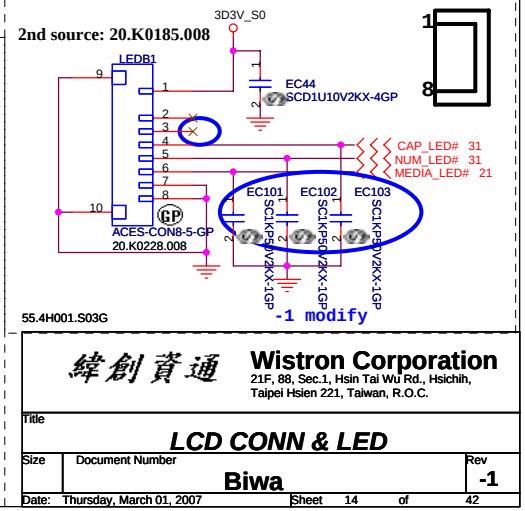












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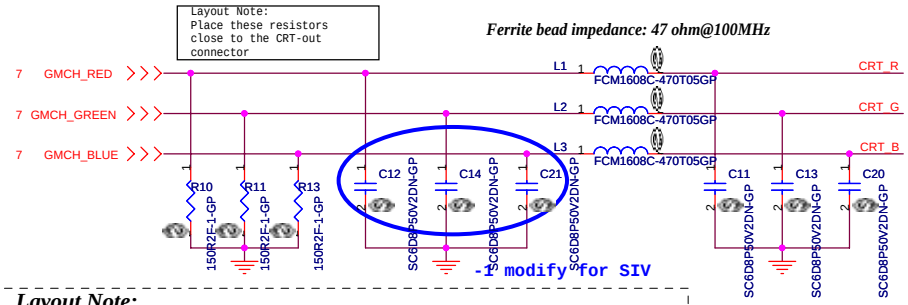
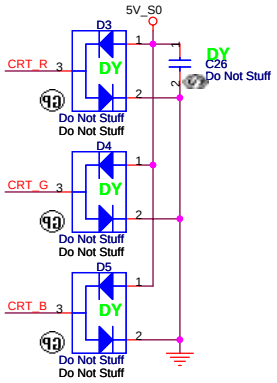
Title: LCD CONN & LED

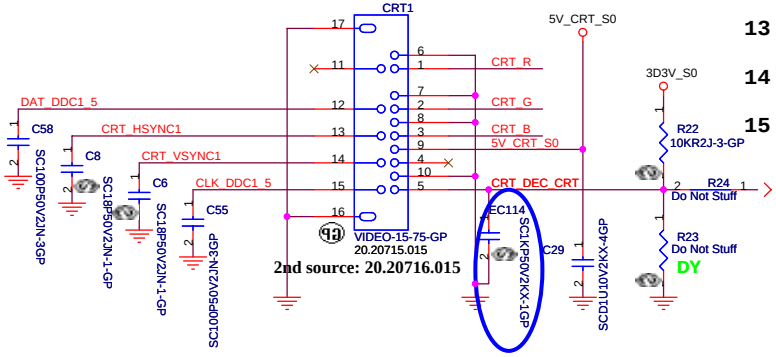
Size	Document Number	Rev
	Biwa	-1

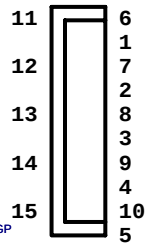
Date: Thursday, March 01, 2007 Sheet 14 of 42

CRT I/F & CONNECTOR



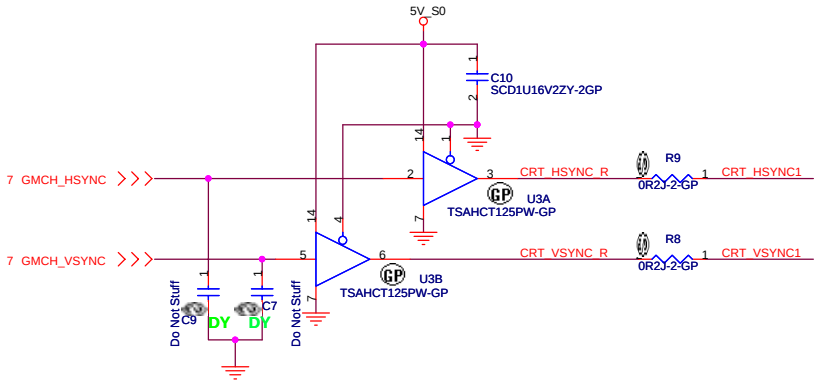




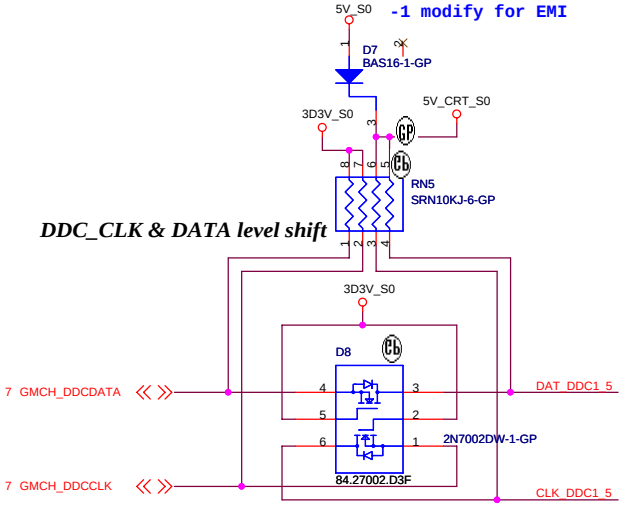


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

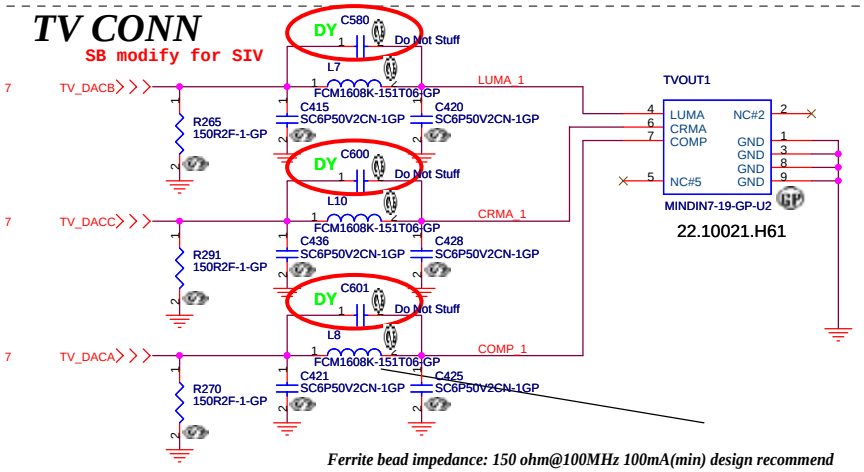


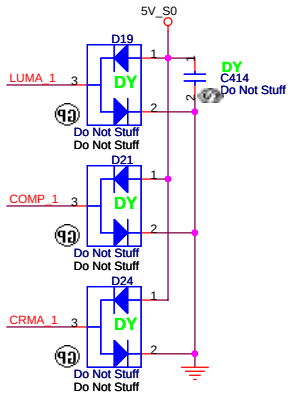
DDC_CLK & DATA level shift



TV CONN

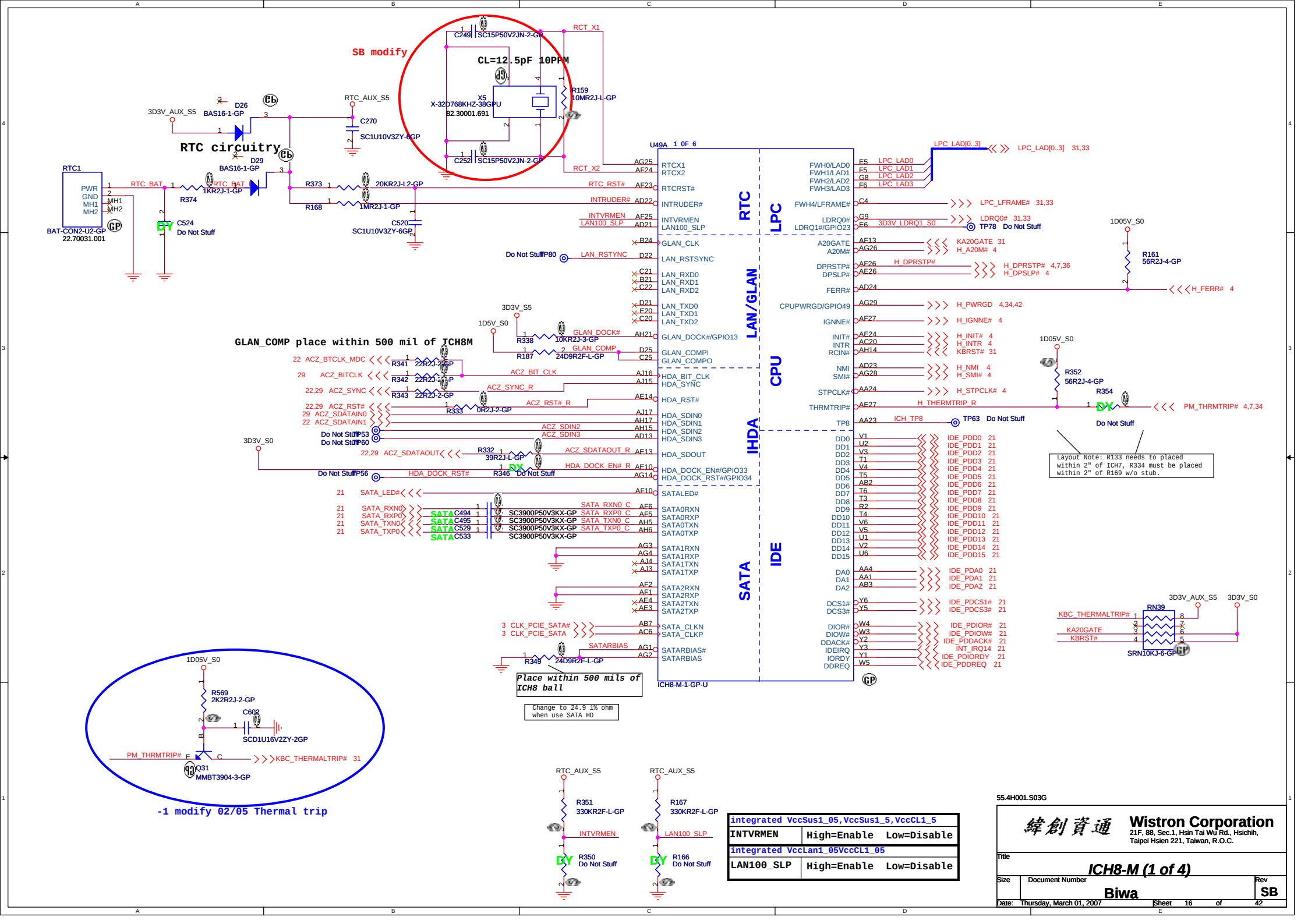
SB modify for SIV

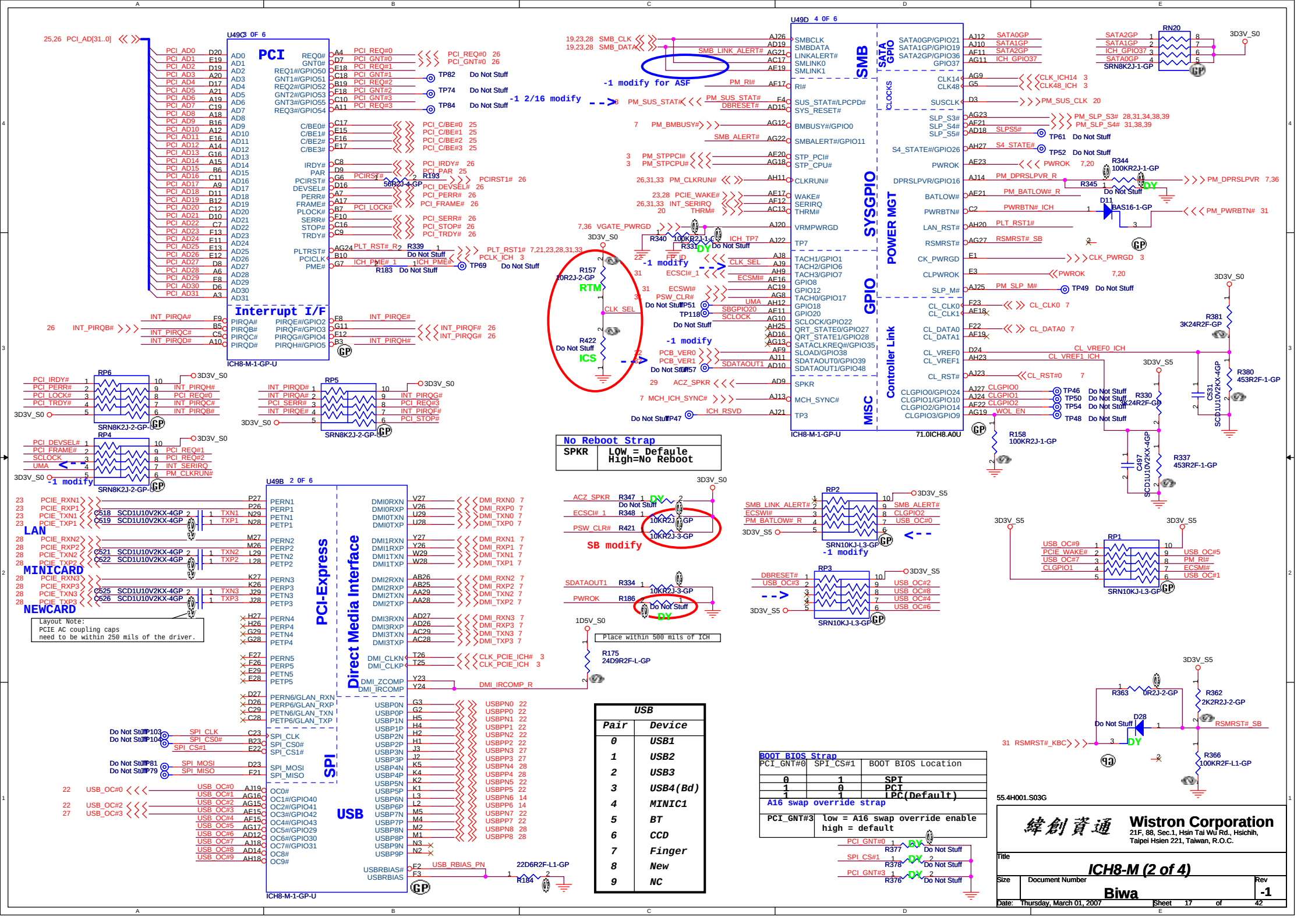


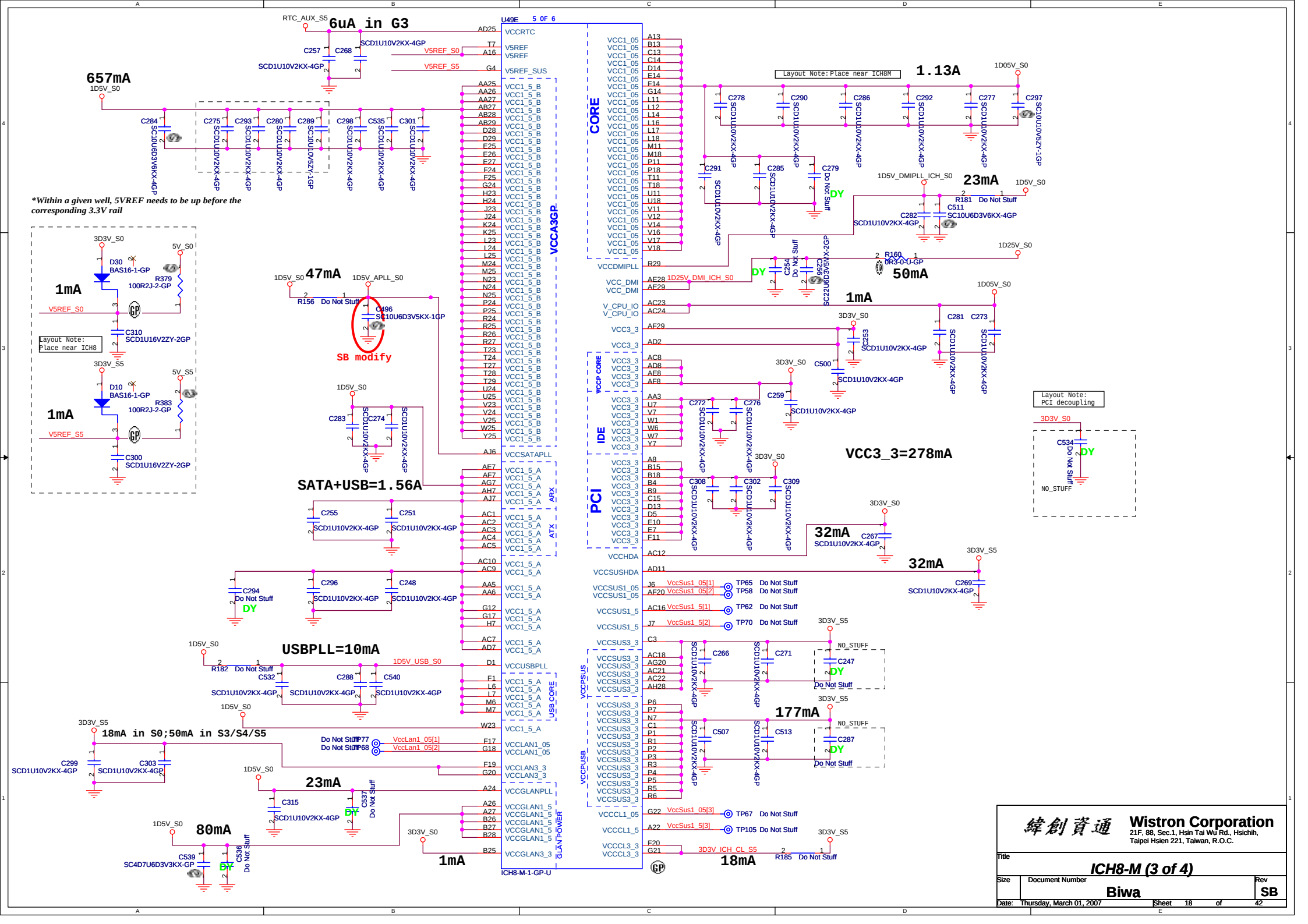


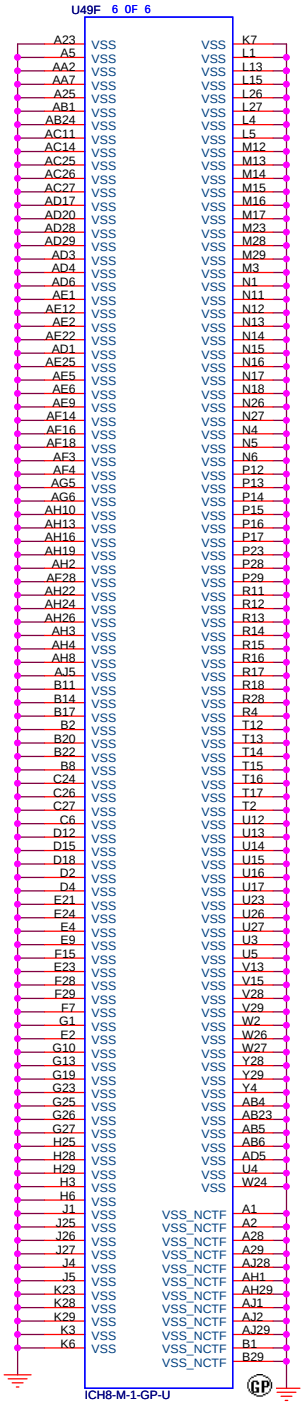
Ferrite bead impedance: 150 ohm@100MHz 100mA(min) design recommend

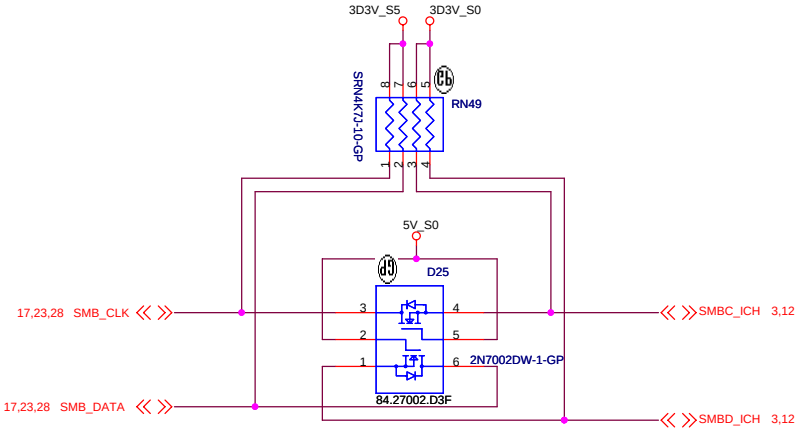
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CRT/TV Connector***	
Size	Document Number: **Biwa**	Rev: **-1**
Date: Thursday, March 01, 2007	Sheet 15 of 42	


SB modify
CL=12.5pF 10PPM
RTC circuitry
GLAN_COMP place within 500 mil of ICH8M
Place within 500 mils of ICH8 ball
Change to 24.9 1% ohm when use SATA HD
Layout Note: R133 needs to placed within 2" of ICH7, R334 must be placed within 2" of R169 w/o stub.
-1 modify 02/05 Thermal trip
U49A 1 OF 6
ICH8-M-1-GP-U
RTC
LPC
LAN/GLAN
CPU
IHDA
SATA
IDE
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
55.4H001.S03G
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8-M (1 of 4)
Size
Document Number
Biwa
Rev
SB
Date: Thursday, March 01, 2007
Sheet 16 of 42


PCI
Interrupt I/F
ICH8-M-1-GP-U
SMB
GPIO
SYSGPIO
POWER MGT
Controller Link
MISC
SATA GPIO
CLOCKS
ICH8-M-1-GP-U
71.0ICH8.A0U
PCI-Express
Direct Media Interface
SPI
USB
LAN
MINICARD
NEWCARD
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
-1 modify for ASF
-1 2/16 modify
-1 modify
SB modify
RTM
ICS
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
Place within 500 mils of ICH
USB
Pair
Device
0
USB1
1
USB2
2
USB3
3
USB4(Bd)
4
MINIC1
5
BT
6
CCD
7
Finger
8
New
9
NC
BOOT BIOS Strap
PCI_GNT#0
SPI_CS#1
BOOT BIOS Location
SPI
PCI
LPC(Default)
A16 swap override strap
PCI_GNT#3
low = A16 swap override enable
high = default
55.4H001.S03G
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8-M (2 of 4)
Size
Document Number
Biwa
Rev
-1
Date: Thursday, March 01, 2007
Sheet 17 of 42


6uA in G3
657mA
1.13A
23mA
47mA
1mA
50mA
SB modify
SATA+USB=1.56A
USBPLL=10mA
18mA in S0;50mA in S3/S4/S5
23mA
80mA
1mA
VCC3_3=278mA
32mA
32mA
177mA
18mA
1mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near ICH8M
Layout Note: Place near ICH8
Layout Note: PCI decoupling
U49E 5 OF 6
ICH8-M-1-GP-U
CORE
VCCA3GP
PCI
IDE
USB CORE
GLAN POWER
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH8-M (3 of 4)
Biwa
SB
Thursday, March 01, 2007
Sheet 18 of 42





D55 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

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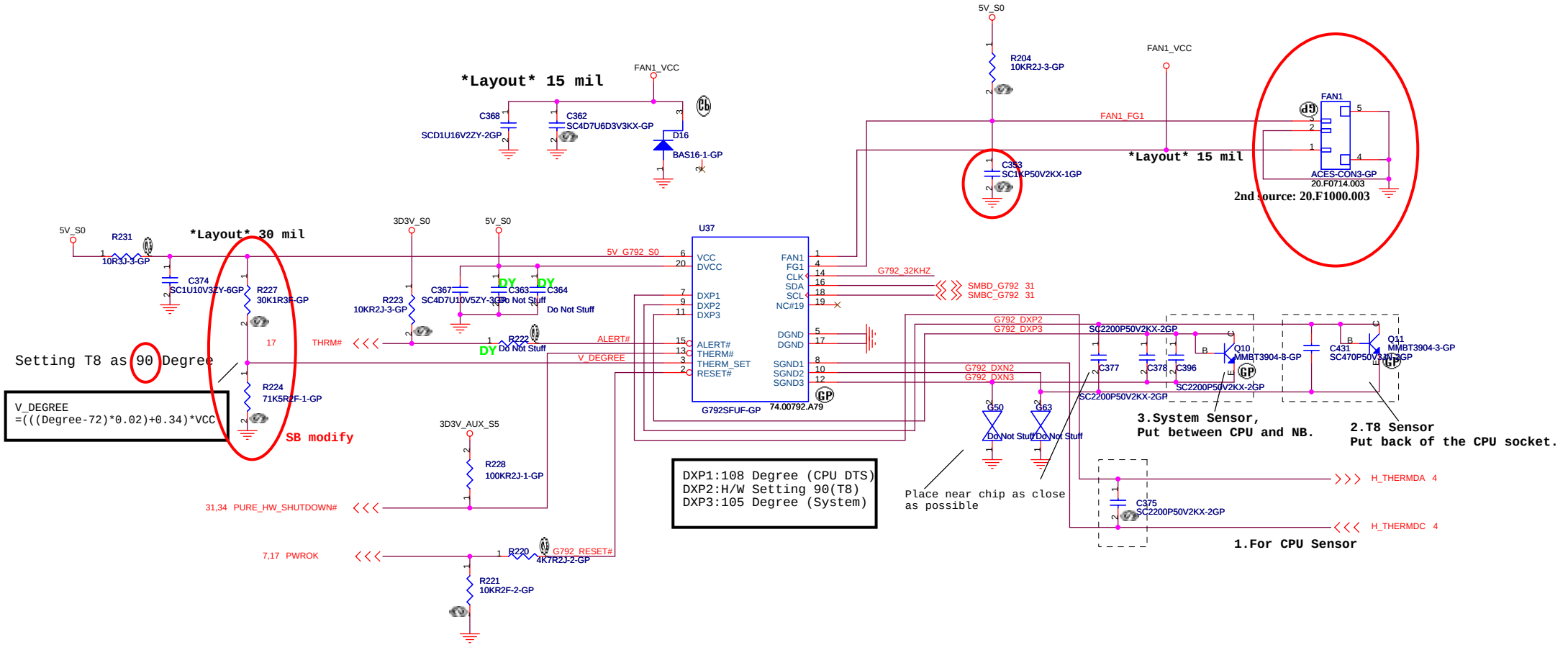
Title	*ICH8-M (4 of 4)*	
Size	Document Number: **Biwa**	Rev: SA
Date: Thursday, March 01, 2007	Sheet 19 of 42	



TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

Biwa Thermal Table 1106

		T6	T7
Sencor 0	CPU DTS	100	102
Sencor 1	CPU G792 Analog	110	113
Sencor 2	System G792	85	87
Sencor 3	T8		
Sencor 4	ADIA status		

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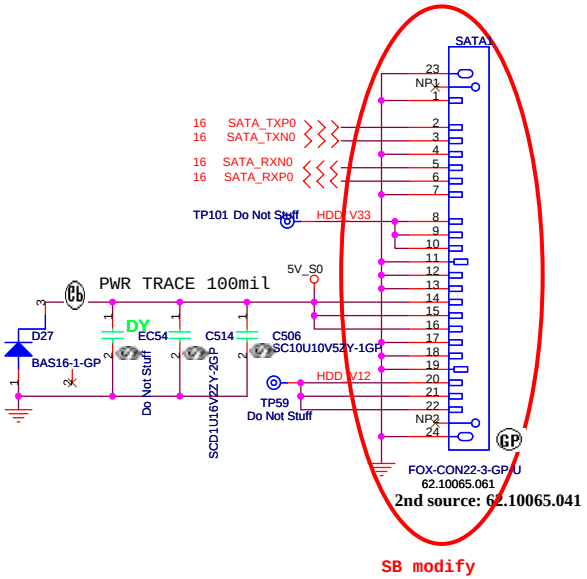
Title: Thermal/Fan Controllor

Size | Document Number: Biwa | Rev: SB

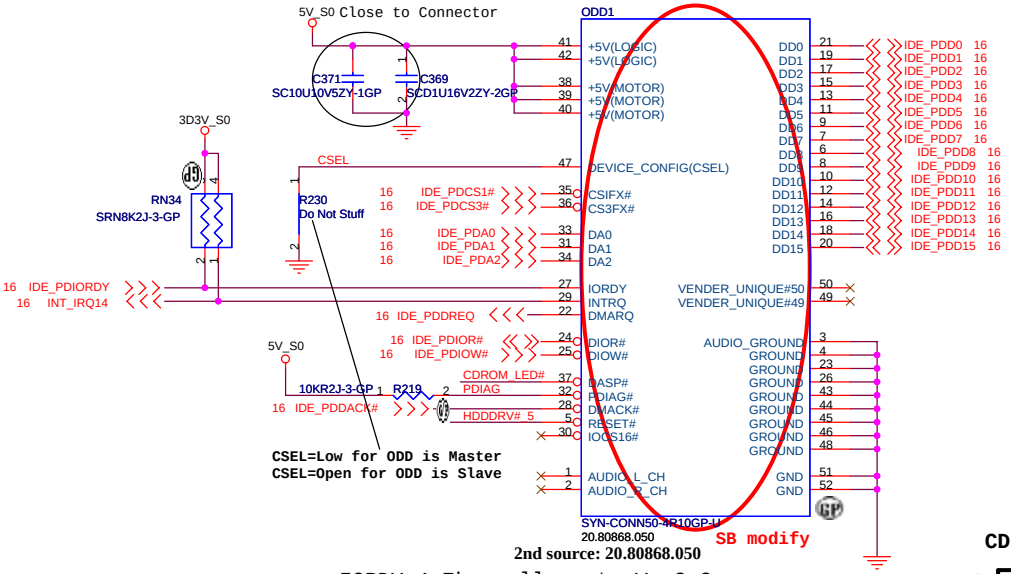
Date: Thursday, March 01, 2007 | Sheet 20 of 42

SATA Connector



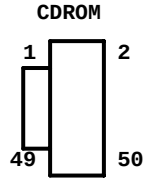
SB modify

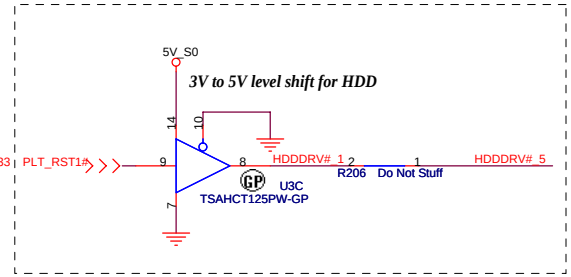
ODD Connector

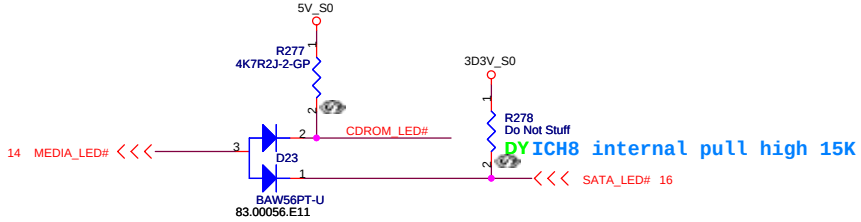


SB modify

IORDY 4.7k pull-up to Vcc3_3
IDEIRQ 8.2k to 10k pull-up to Vcc3_3







ICH8 internal pull high 15K

55.4H001.S03G

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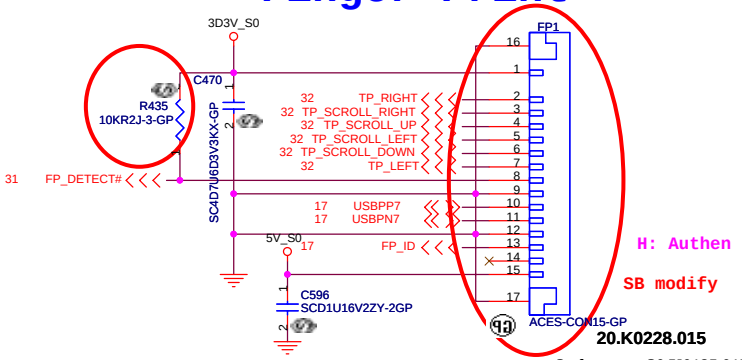
Title: HDD and CDROM

Size	Document Number	Rev
	Biwa	SB

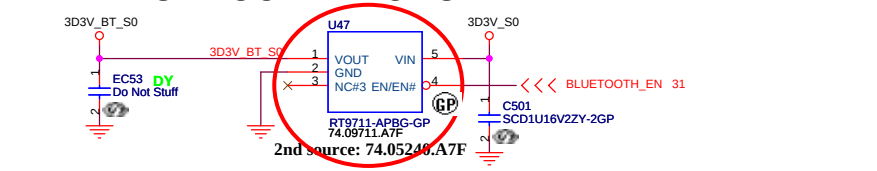
Date: Thursday, March 01, 2007 Sheet 21 of 42

Finger Print



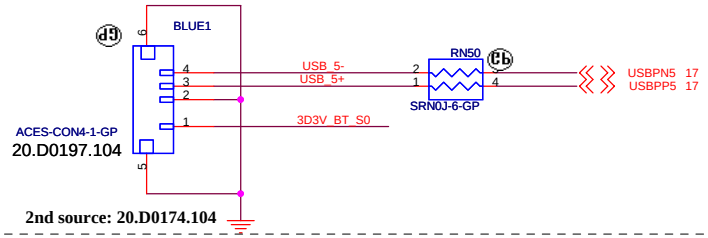
2nd source: 20.K0185.015

BLUETOOTH MODULE



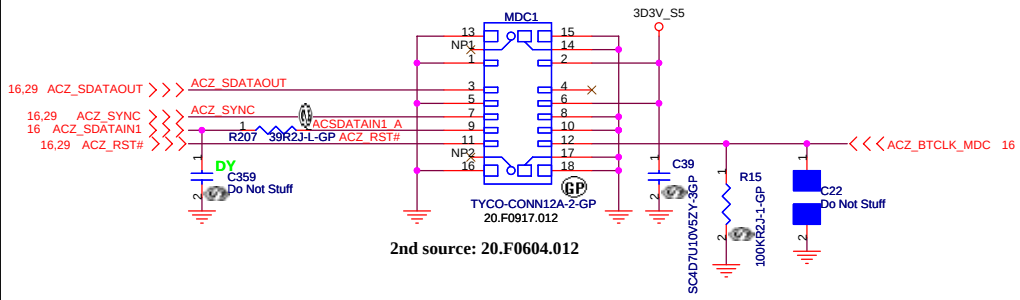
2nd source: 74.05240.A7F

EC21 put near BLUE1 / all USB put one choke near connector by EMI request

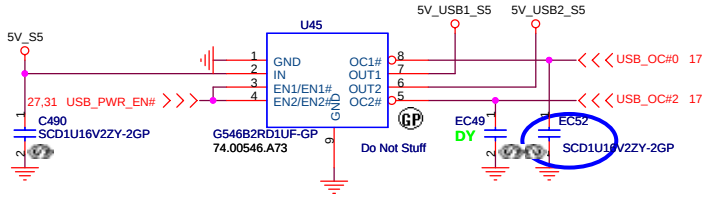


2nd source: 20.D0174.104

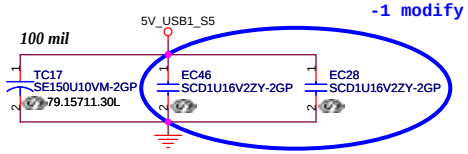
MDC 1.5 CONN

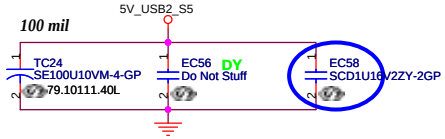


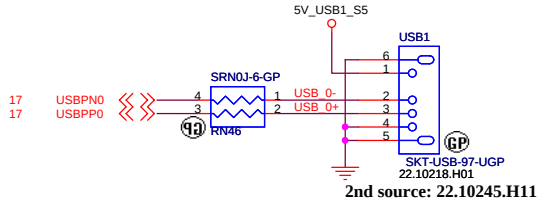
2nd source: 20.F0604.012



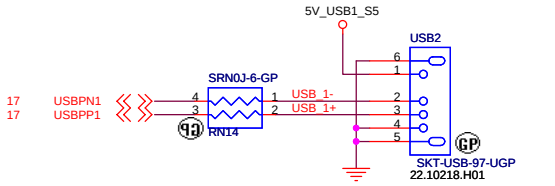
-1 modify for EMC



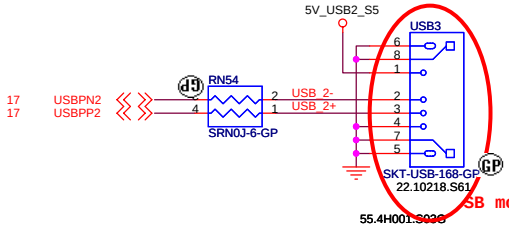




2nd source: 22.10245.H11



2nd source: 22.10245.H11



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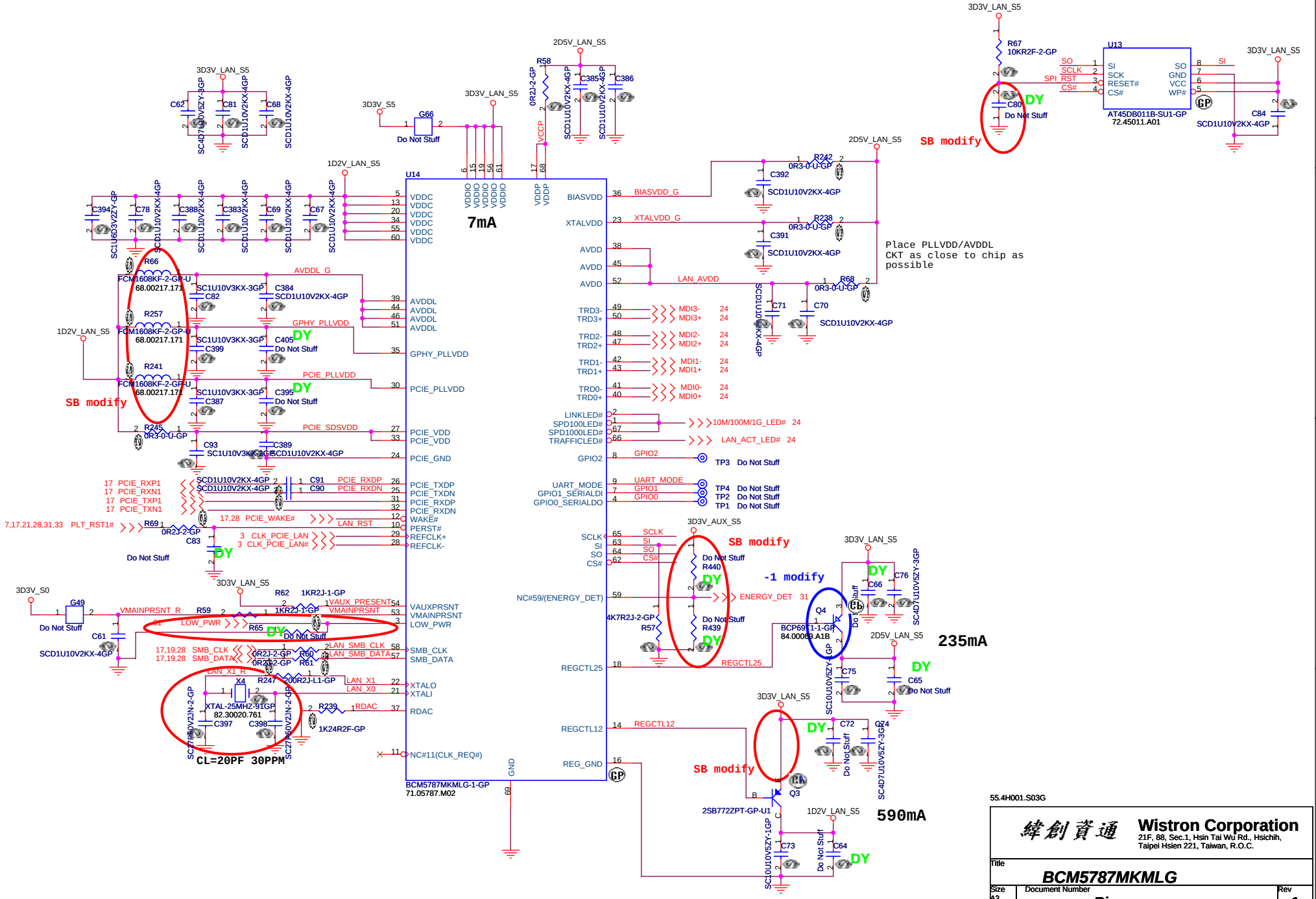
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB / MDC / BLUETOOTH / FP

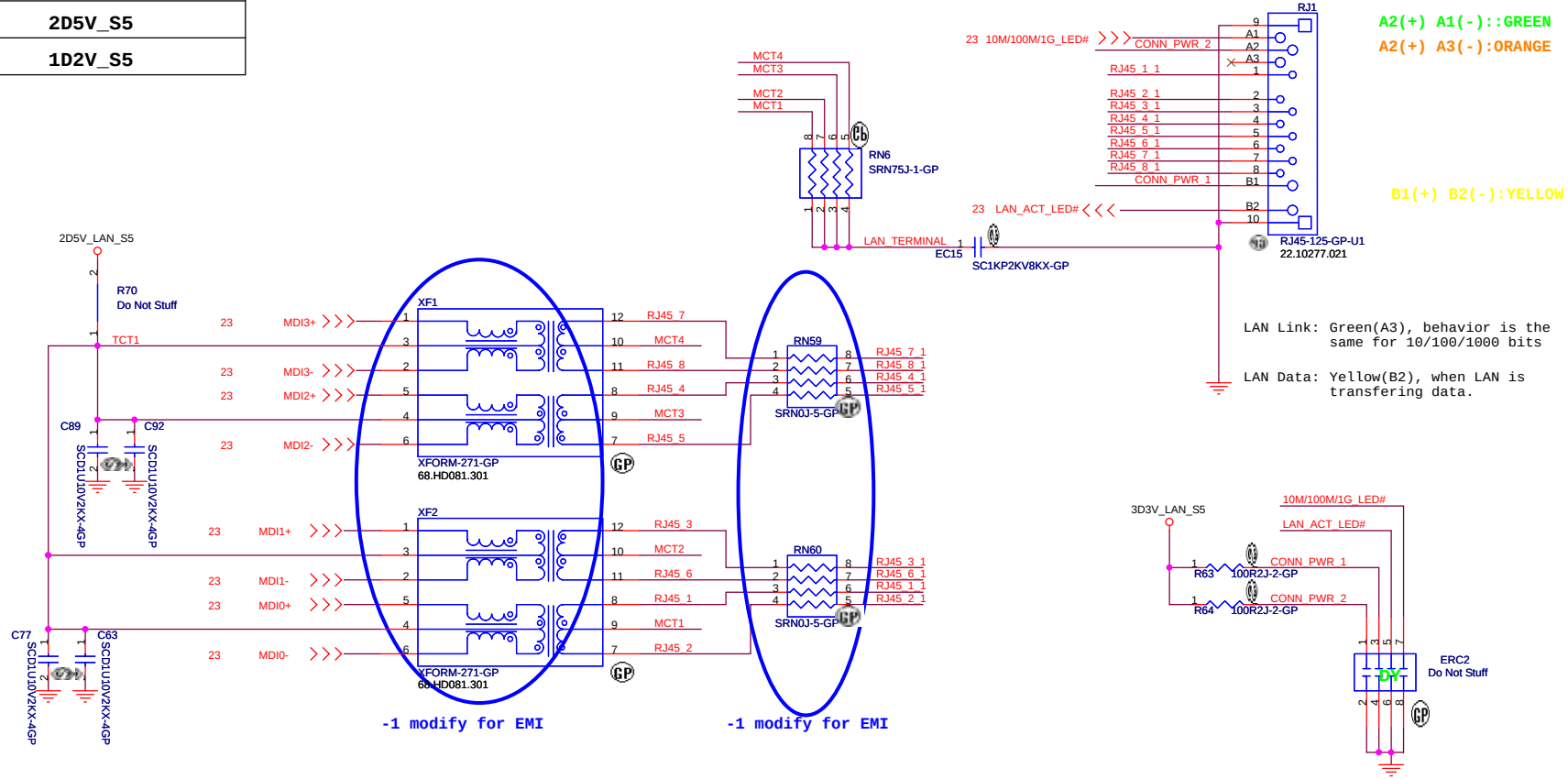
Size | Document Number: Biwa | Rev: -1

Date: Thursday, March 01, 2007 | Sheet 22 of 42


U14
BCM5787MKMLG-1-GP
71.05787.M02
7mA
235mA
590mA
SB modify
DY
Do Not Stuff
Place PLLVDD/AVDDL
CKT as close to chip as
possible
CL=20PF 30PPM
-1 modify
U13
AT45DB011B-SU1-GP
72.45011.A01
Q3
2SB772ZPT-GP-U1
Q4
BCP69T1-1-GP
84.00069.A1B
55.4H001.S03G
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5787MKMLG
Size A3
Document Number
Biwa
Rev -1
Date: Thursday, March 01, 2007
Sheet 23 of 42

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

LAN Connector



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

55.4H001.S03G

緯創資通 **Wistron Corporation**
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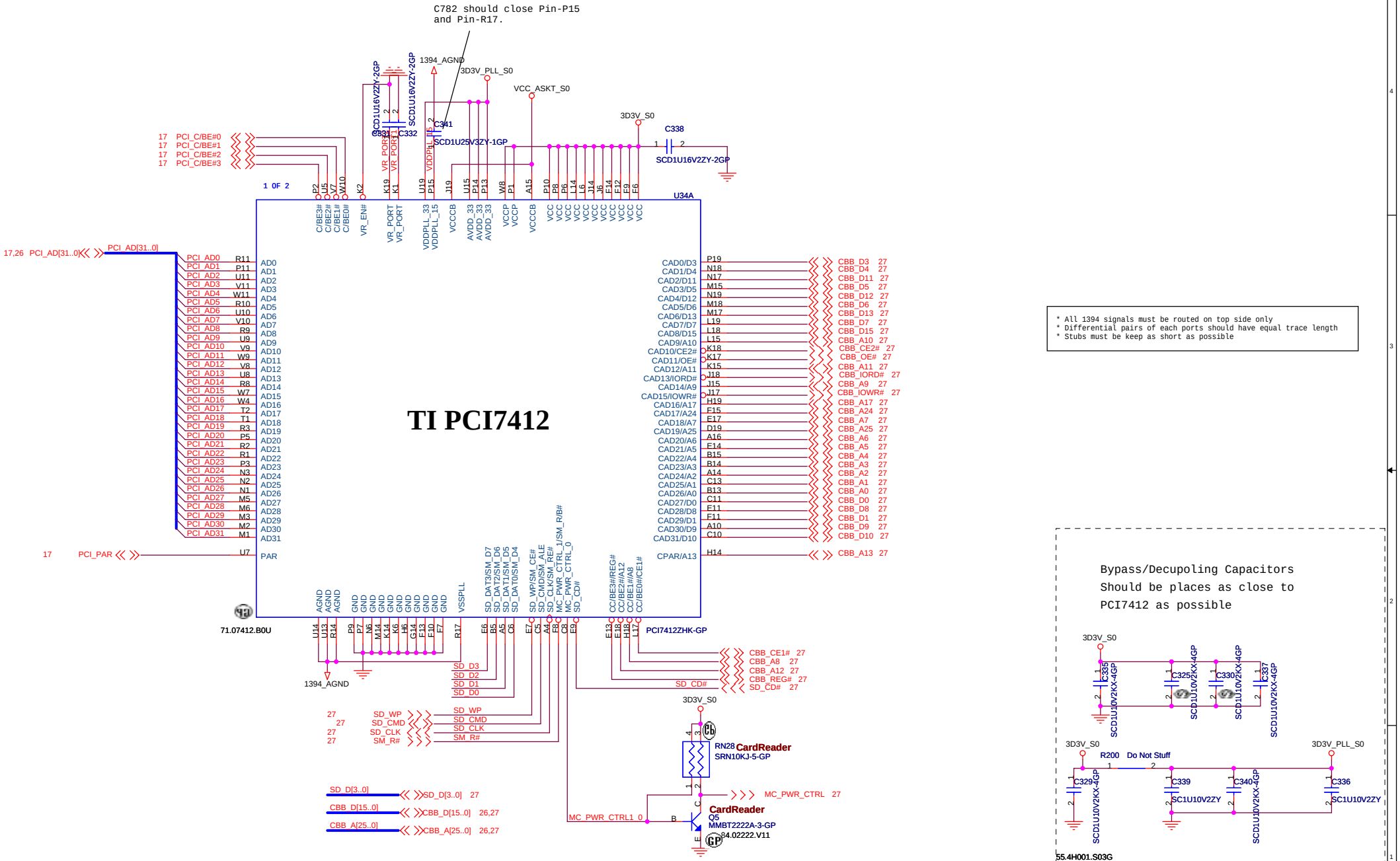
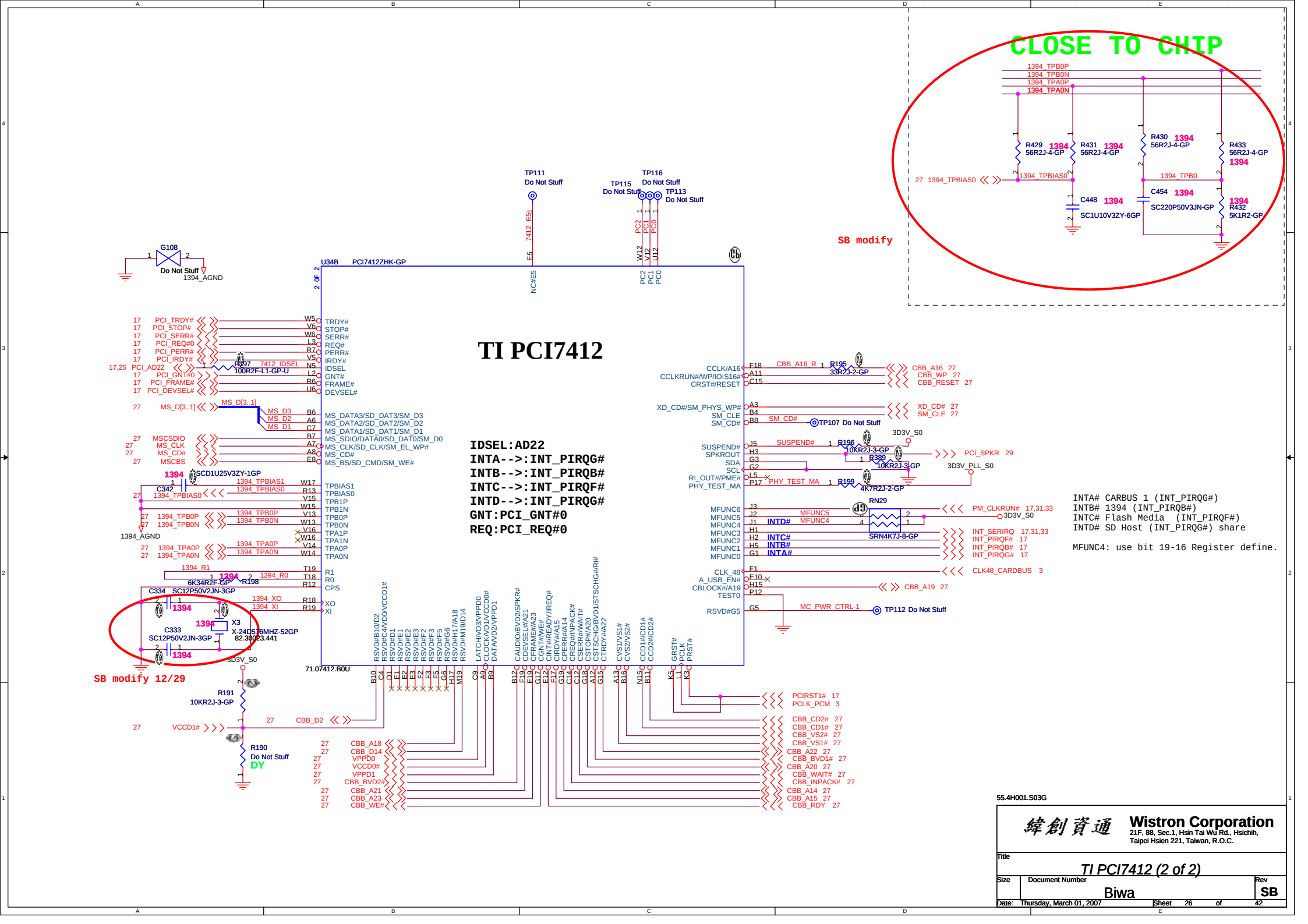
Title: **LAN Connector**

Size	Document Number	Rev
A3	Biwa	-1

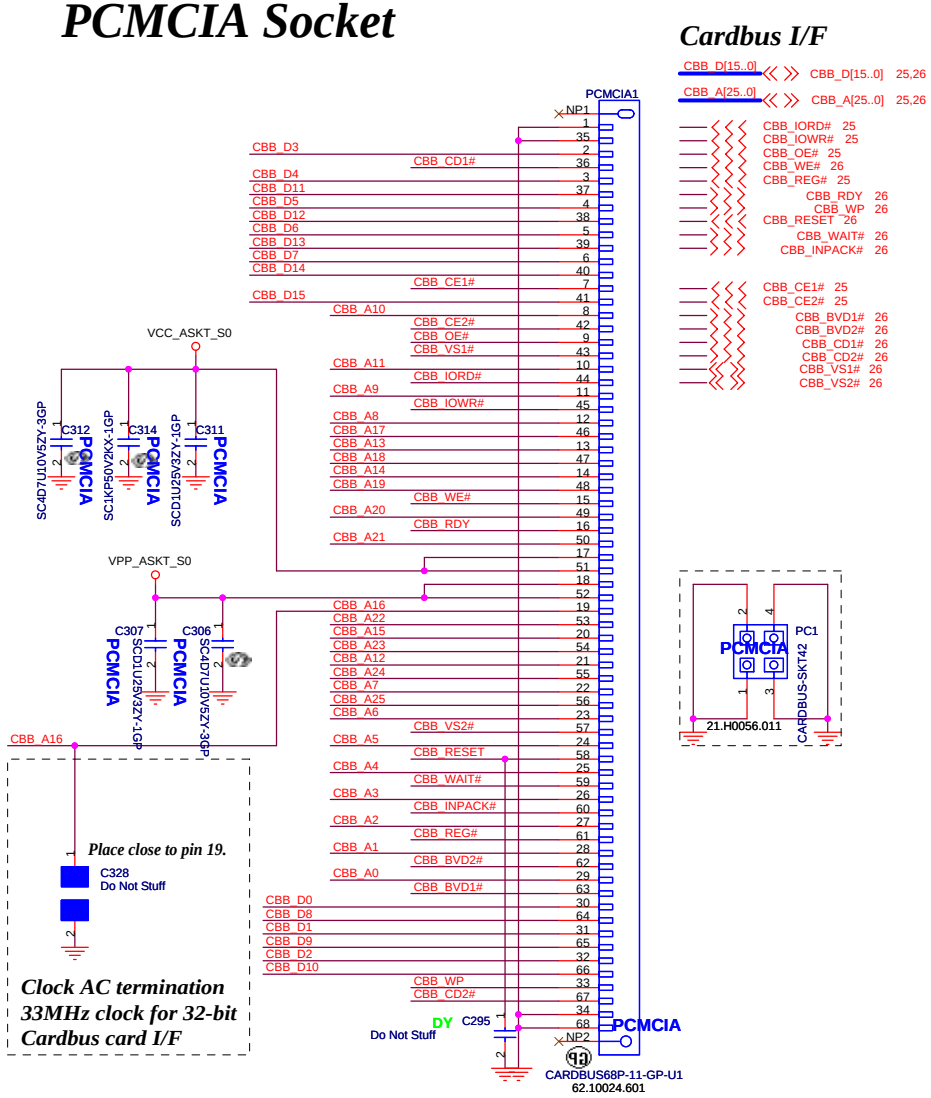
Date: Thursday, March 01, 2007 Sheet 24 of 42

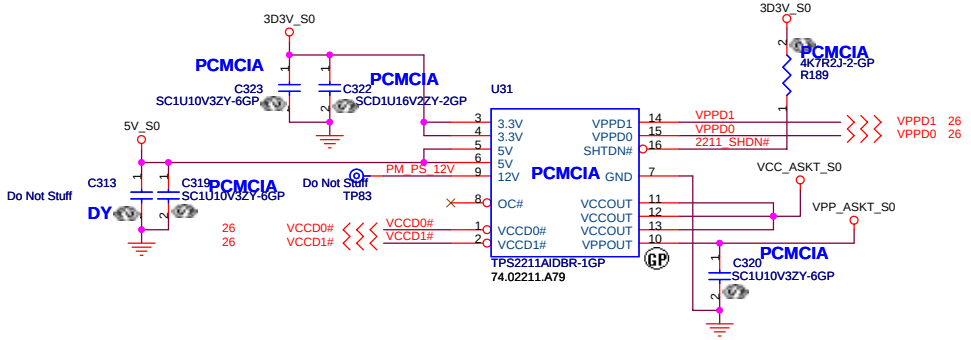


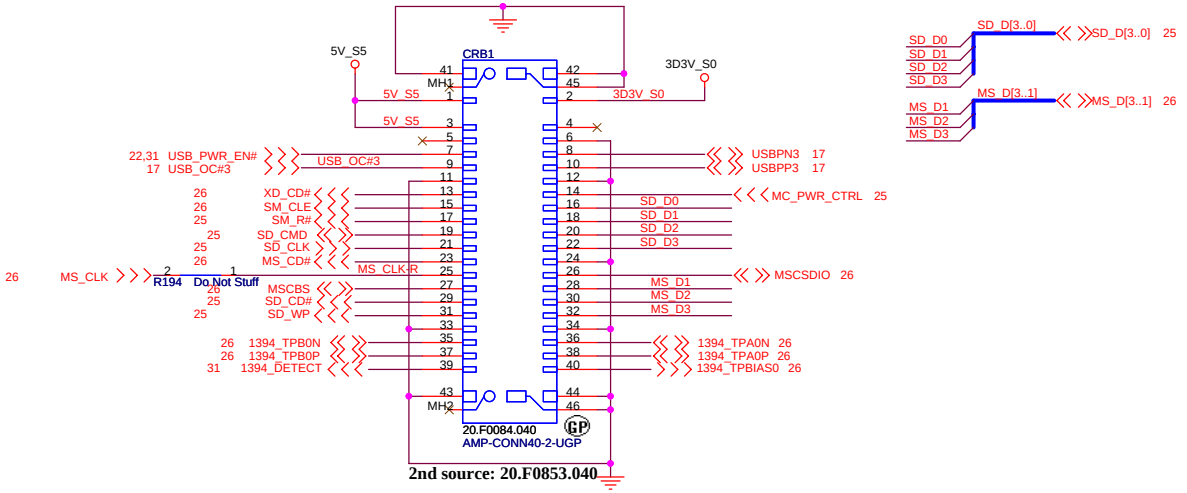
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	TI PCI7412 (1 of 2)
Size	Document Number: Biwa
Rev	SA
Date:	Thursday, March 01, 2007
Sheet	25 of 42


CLOSE TO CHIP
SB modify
TI PCI7412
U34B PCI7412ZHK-GP
IDSEL:AD22
INTA-->:INT_PIRQG#
INTB-->:INT_PIRQB#
INTC-->:INT_PIRQF#
INTD-->:INT_PIRQG#
GNT:PCI_GNT#0
REQ:PCI_REQ#0
INTA# CARBUS 1 (INT_PIRQG#)
INTB# 1394 (INT_PIRQB#)
INTC# Flash Media (INT_PIRQF#)
INTD# SD Host (INT_PIRQG#) share
MFUNC4: use bit 19-16 Register define.
SB modify 12/29
55.4H001.S03G
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TI PCI7412 (2 of 2)
Size
Document Number
Biwa
Rev
SB
Date: Thursday, March 01, 2007
Sheet 26 of 42

PCMCIA Socket







XD
MS / MS PRO
SD / SD IO / MMC

55.4H001.S03G

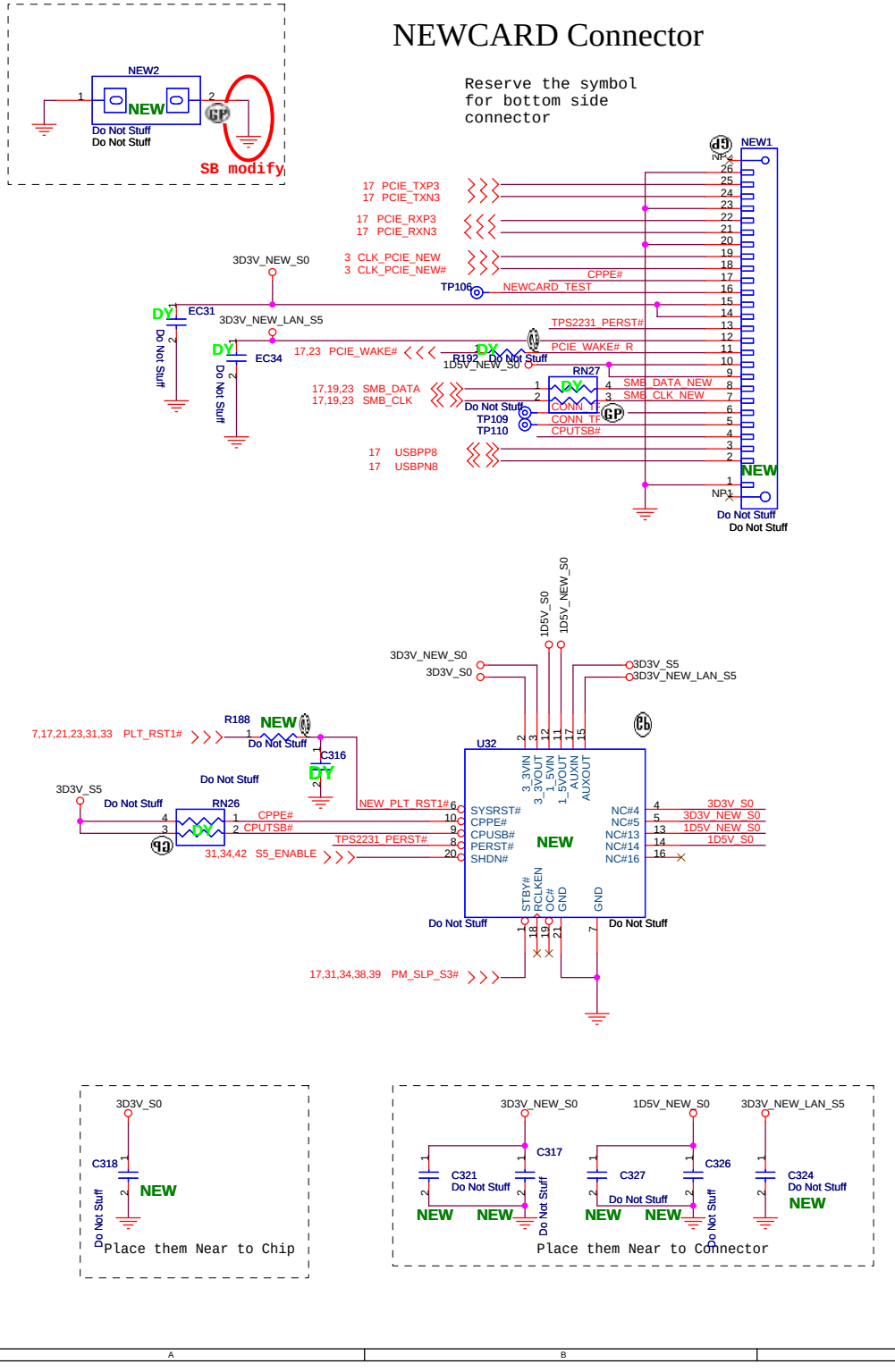
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *PCMCIA / CARD READER BD*

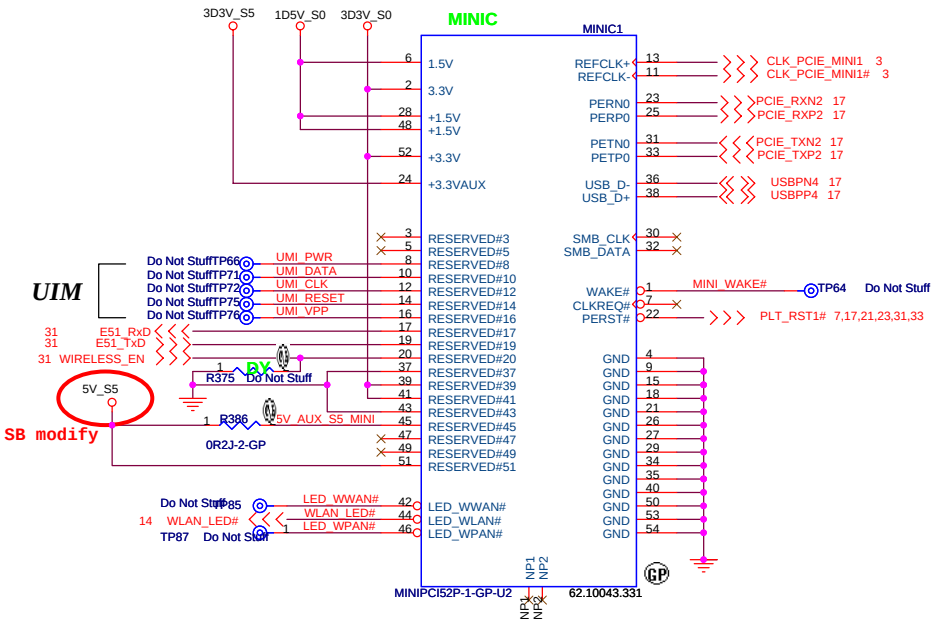
Size	Document Number	Rev
	Biwa	SA

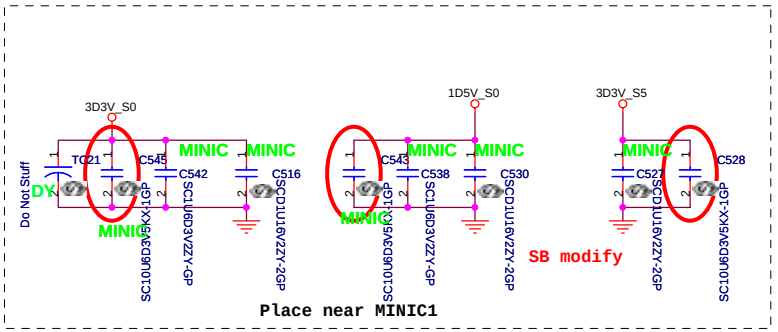
Date: Thursday, March 01, 2007 Sheet 27 of 42

NEWCARD Connector



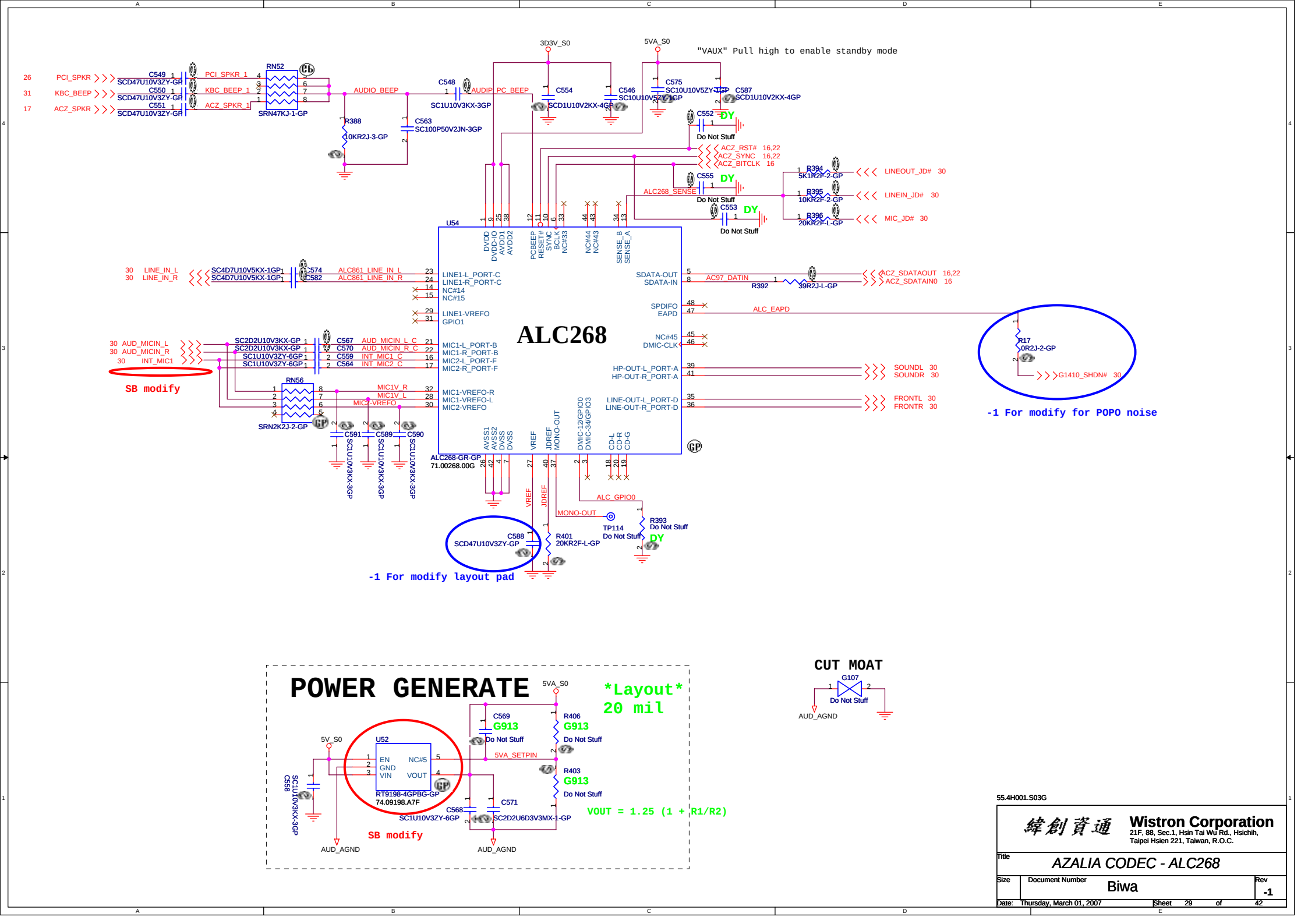
Mini Card Connector





55.4H001.S03G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD / NEW CARD		
Size	Document Number: Biwa	Rev: SB
Date: Thursday, March 01, 2007	Sheet 28 of 42	



55.4H001.S03G

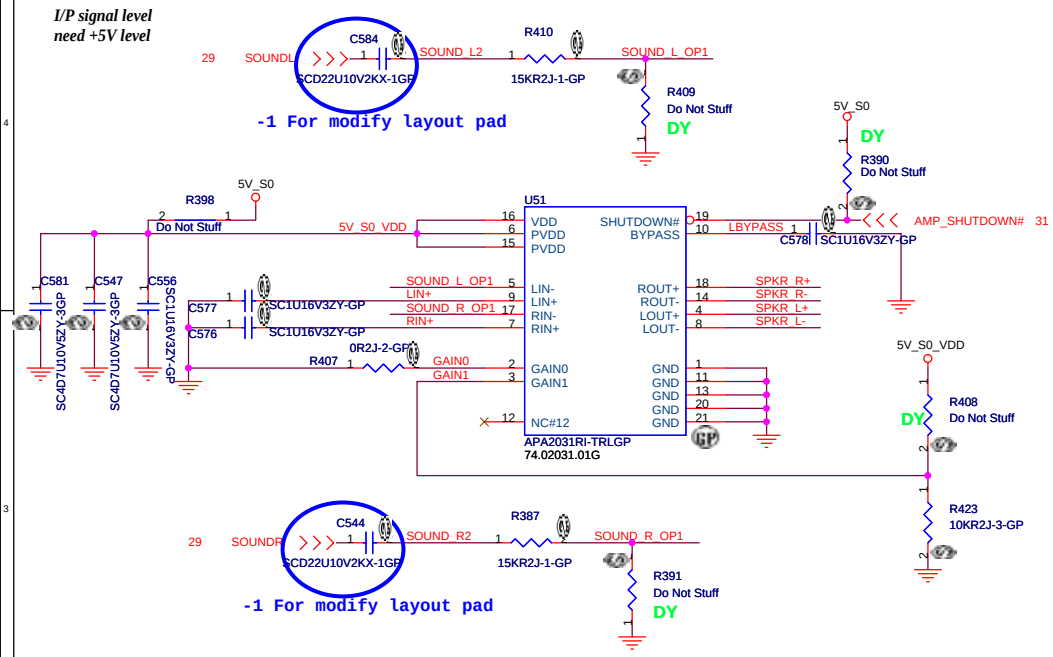
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

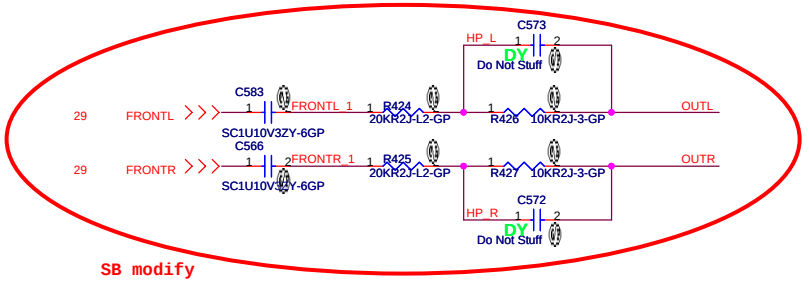
Title: AZALIA CODEC - ALC268

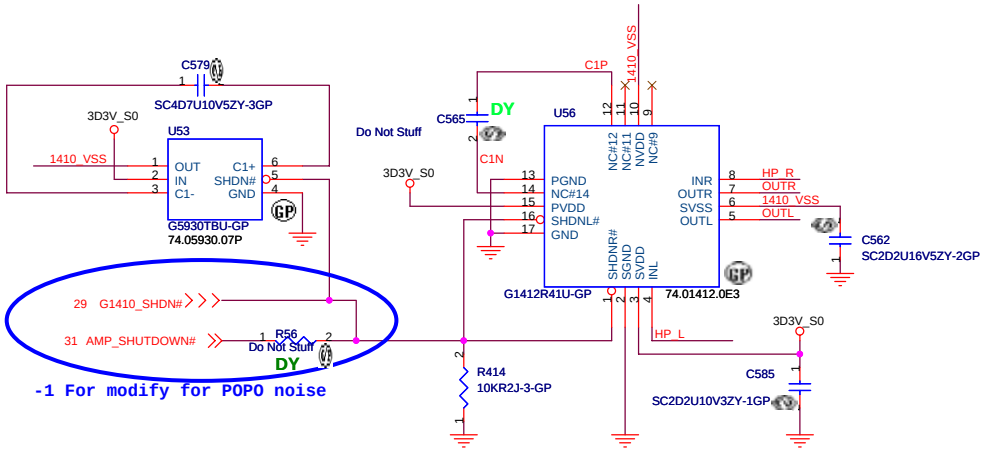
Size | Document Number: Biwa | Rev: -1

Date: Thursday, March 01, 2007 | Sheet 29 of 42

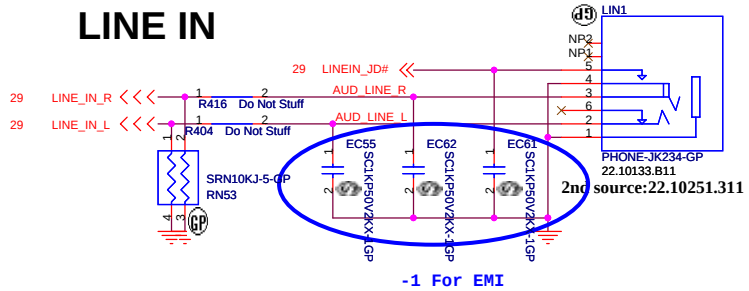
AUDIO OP AMPLIFIER



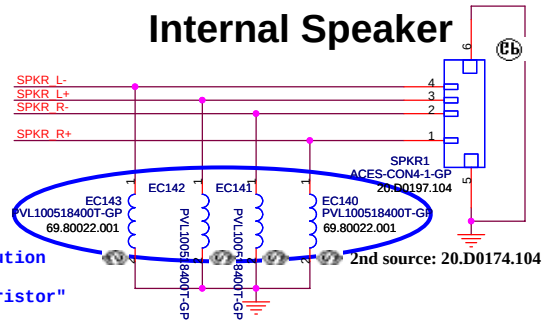




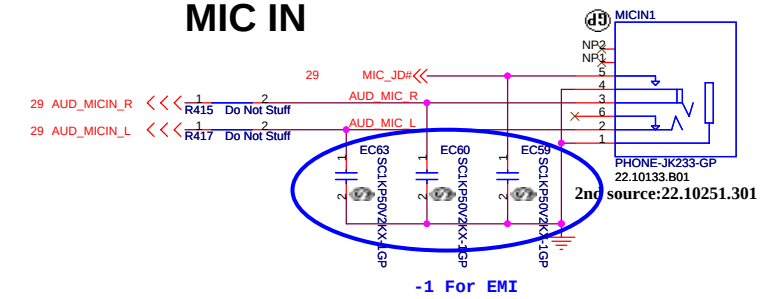
LINE IN



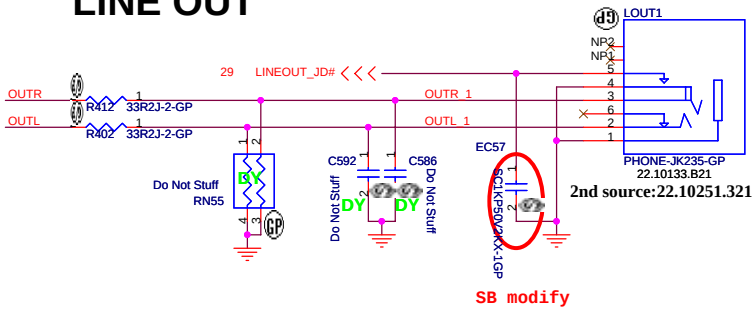
Internal Speaker



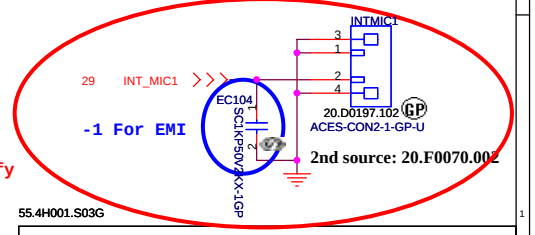
MIC IN



LINE OUT



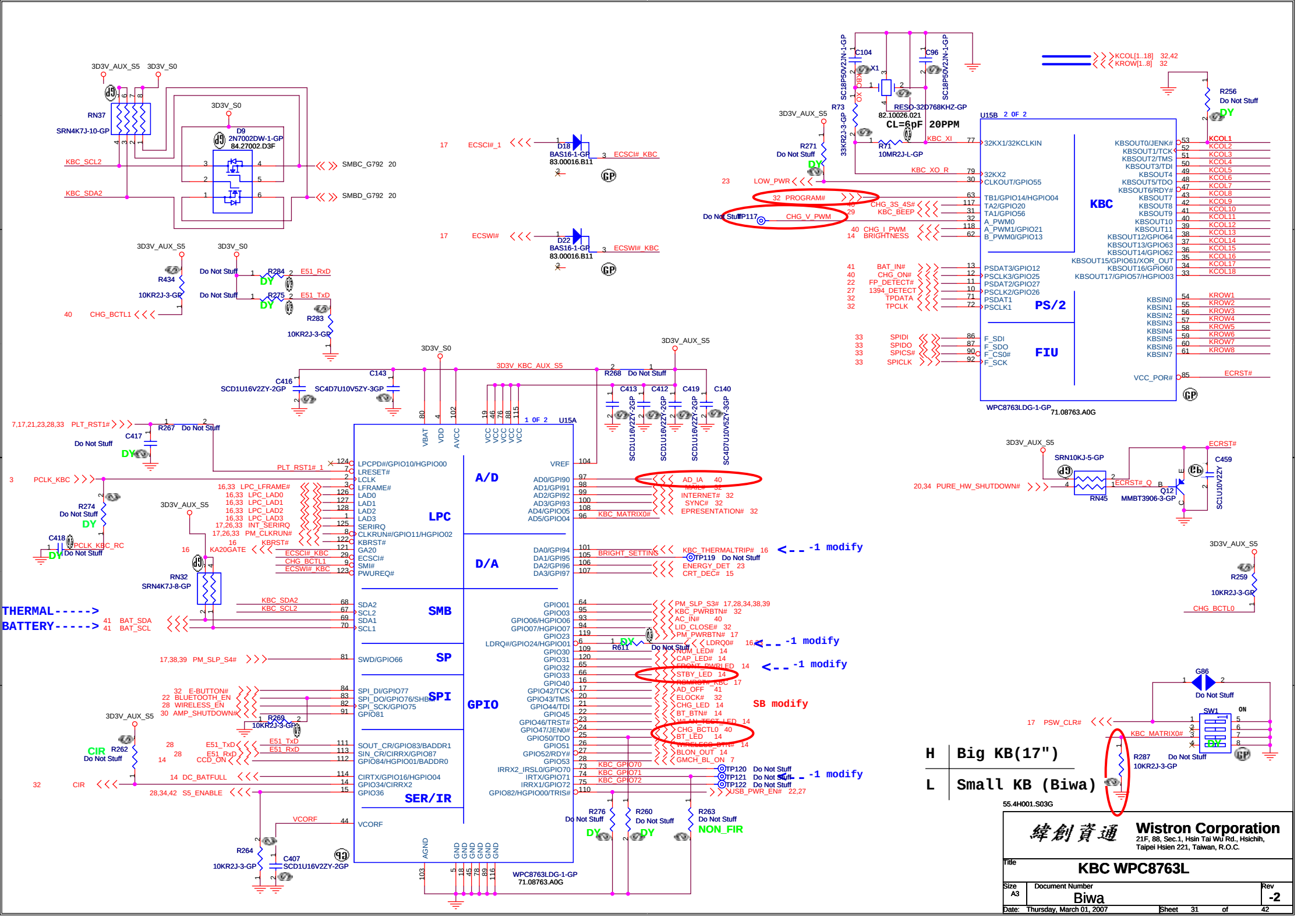
Internal Microphone

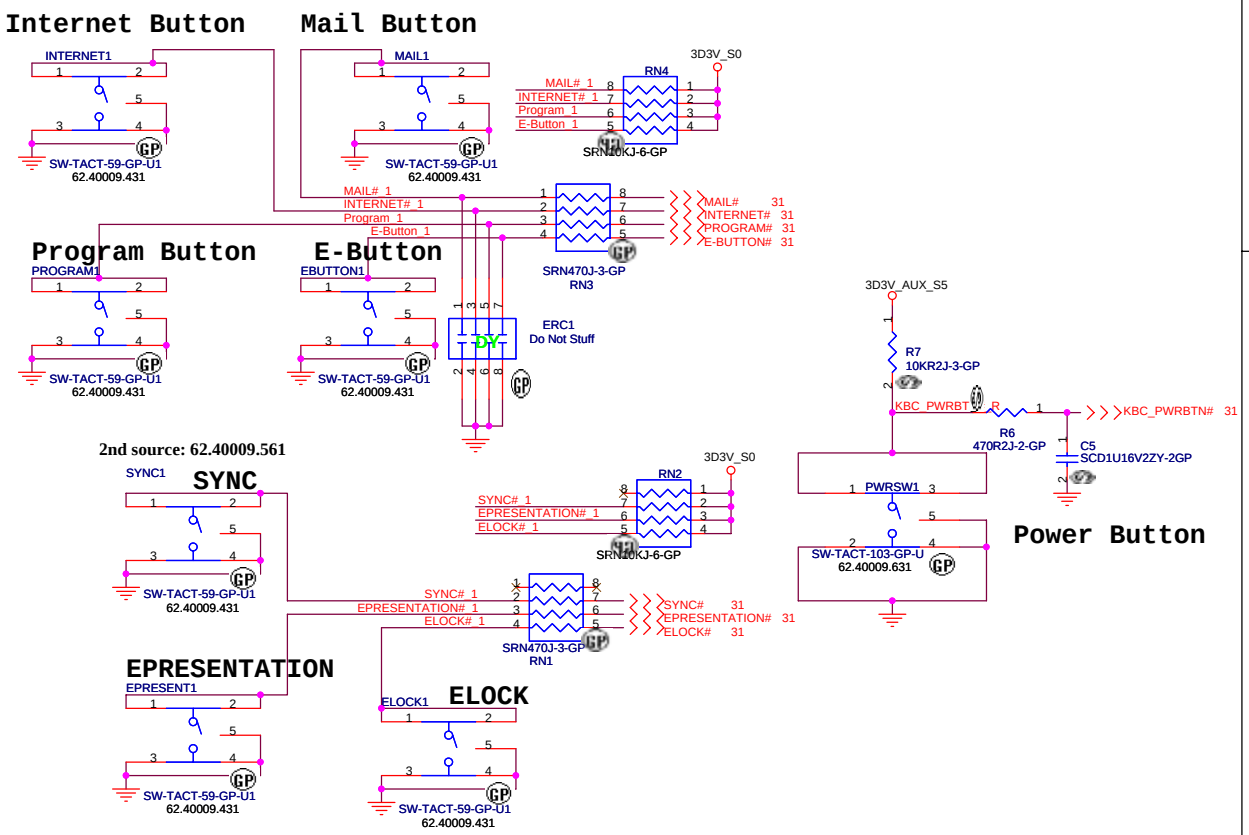


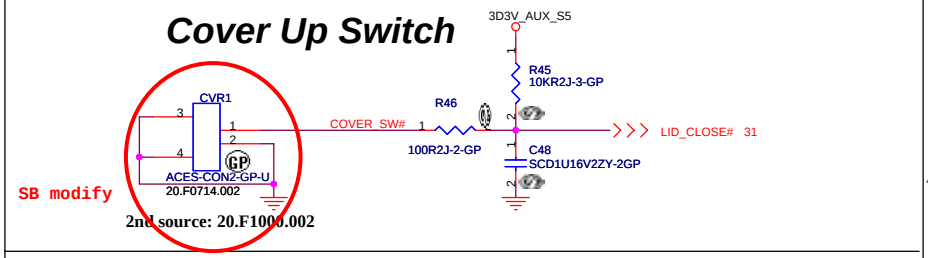
55.4H001.S03G

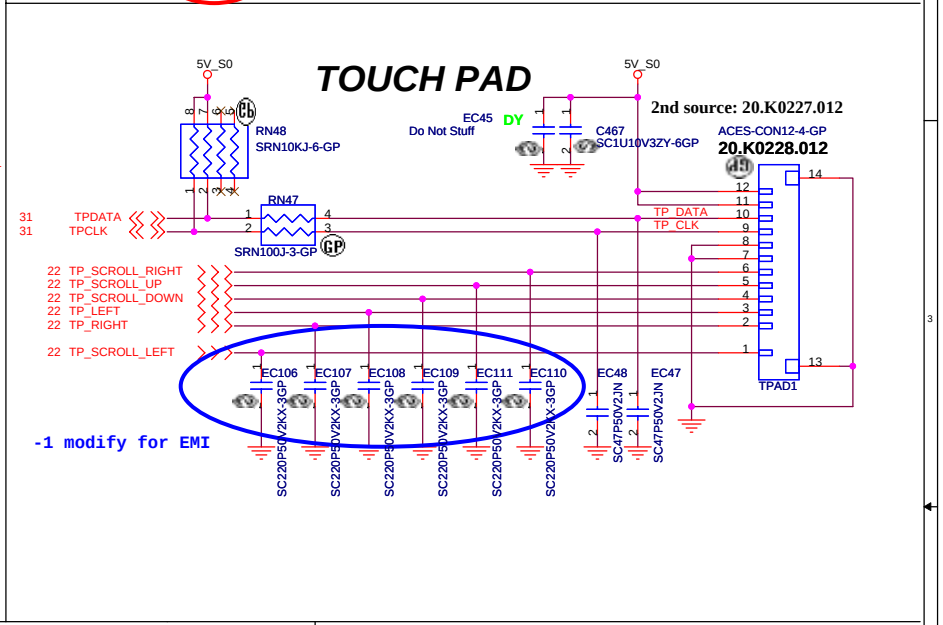
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

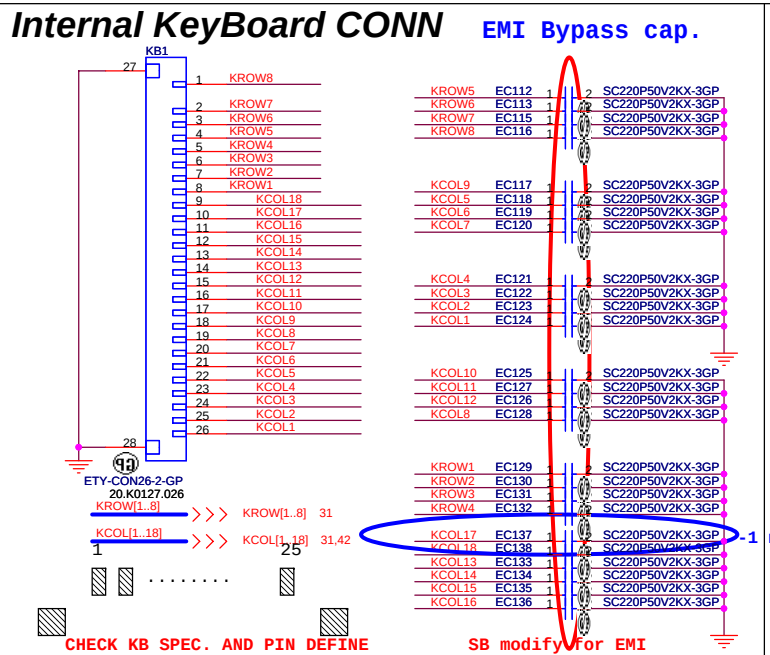
Title	AUDIO AMP AND JACK	
Size: A3	Document Number: Biwa	Rev: -2
Date: Thursday, March 01, 2007	Sheet 30 of 42	

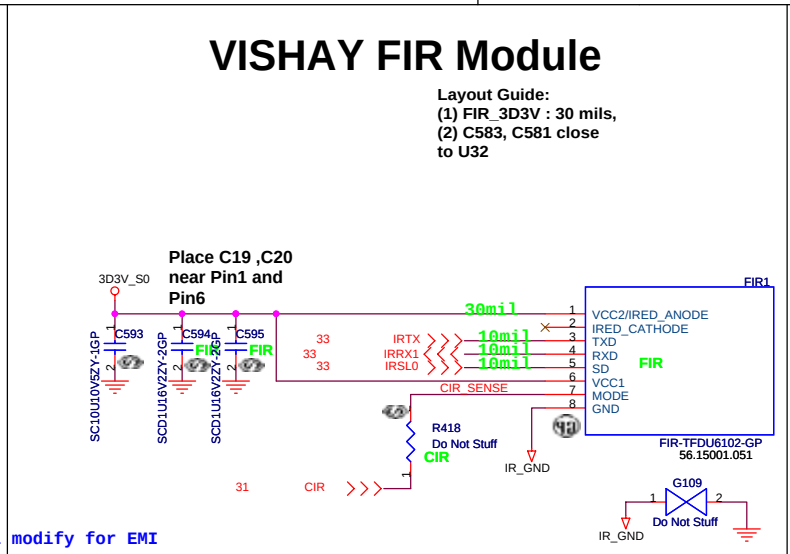

3D3V_AUX_S5
3D3V_S0
RN37
SRN4K7J-10-GP
D9
2N7002DW-1-GP
84.27002.D3F
KBC_SCL2
KBC_SDA2
SMBC_G792 20
SMBD_G792 20
17 ECSCI#_1
D18
BAS16-1-GP
83.00016.B11
ECSCI# KBC
17 ECSWI#
D22
BAS16-1-GP
83.00016.B11
ECSWI# KBC
R434
10KR2J-3-GP
40 CHG_BCTL1
Do Not Stuff
R284
E51_RxD
R275
E51_TxD
R283
10KR2J-3-GP
C104
C96
X1
RESO-32D768KHZ-GP
82.10026.021
CL=6pF 20PPM
SC18P50V2JN-1-GP
33KR2J-3-GP
R73
R271
Do Not Stuff
R71
10MR2J-L-GP
KBC_XI
KBC_XO_R
23 LOW_PWR
32 PROGRAM#
Do Not Stuff P117
CHG_V_PWM
40 CHG_3S_4S#
29 KBC_BEEP
40 CHG_I_PWM
14 BRIGHTNESS
U15B 2 0F 2
32KX1/32KCLKIN
32KX2
CLKOUT/GPIO55
TB1/GPIO14/HGPIO04
TA2/GPIO20
TA1/GPIO56
A_PWM0
A_PWM1/GPIO21
B_PWM0/GPIO13
KBC
41 BAT_IN#
40 CHG_ON#
22 FP_DETECT#
27 1394_DETECT
32 TPDATA
32 TPCLK
PSDAT3/GPIO12
PSCLK3/GPIO25
PSDAT2/GPIO27
PSCLK2/GPIO26
PSDAT1
PSCLK1
PS/2
33 SPIDI
33 SPIDO
33 SPICS#
33 SPICLK
F_SDI
F_SDO
F_CS0#
F_SCK
FIU
KBSOUT0/JENK#
KBSOUT1/TCK
KBSOUT2/TMS
KBSOUT3/TDI
KBSOUT4
KBSOUT5/TDO
KBSOUT6/RDY#
KBSOUT7
KBSOUT8
KBSOUT9
KBSOUT10
KBSOUT11
KBSOUT12/GPIO64
KBSOUT13/GPIO63
KBSOUT14/GPIO62
KBSOUT15/GPIO61/XOR_OUT
KBSOUT16/GPIO60
KBSOUT17/GPIO57/HGPIO03
KCOL1
KCOL2
KCOL3
KCOL4
KCOL5
KCOL6
KCOL7
KCOL8
KCOL9
KCOL10
KCOL11
KCOL12
KCOL13
KCOL14
KCOL15
KCOL16
KCOL17
KCOL18
KSBIN0
KSBIN1
KSBIN2
KSBIN3
KSBIN4
KSBIN5
KSBIN6
KSBIN7
KROW1
KROW2
KROW3
KROW4
KROW5
KROW6
KROW7
KROW8
VCC_POR#
ECRST#
WPC8763LDG-1-GP
71.08763.A0G
KCOL[1..18] 32,42
KROW[1..8] 32
R256
Do Not Stuff
3D3V_AUX_S5
SRN10KJ-5-GP
RN45
ECRST# Q
Q12
MMBT3906-3-GP
C459
SC1U10V2ZY
20,34 PURE_HW_SHUTDOWN#
3D3V_S0
3D3V_KBC_AUX_S5
C416
SCD1U16V2ZY-2GP
C143
SC4D7U10V5ZY-3GP
R268
Do Not Stuff
C413
C412
C419
C140
SCD1U16V2ZY-2GP
SC4D7U10V5ZY-3GP
U15A
VBAT
VDD
AVCC
VCC
VREF
7,17,21,23,28,33 PLT_RST1#
C417
R267
Do Not Stuff
PLT_RST1# 1
3 PCLK_KBC
R274
Do Not Stuff
C418
PCLK_KBC_RC
Do Not Stuff
LPCPD#/GPIO10/HGPIO00
LRESET#
LCLK
LFRAME#
LAD0
LAD1
LAD2
LAD3
SERIRQ
CLKRUN#/GPIO11/HGPIO02
KBRST#
GA20
ECSCI#
SMI#
PWUREQ#
LPC
16,33 LPC_LFRAME#
16,33 LPC_LAD0
16,33 LPC_LAD1
16,33 LPC_LAD2
16,33 LPC_LAD3
17,26,33 INT_SERIRQ
17,26,33 PM_CLKRUN#
16 KBRST#
16 KA20GATE
ECSCI# KBC
CHG_BCTL1
ECSWI# KBC
A/D
AD0/GPI90
AD1/GPI91
AD2/GPI92
AD3/GPI93
AD4/GPIO05
AD5/GPIO04
AD_IA 40
MAIL# 32
INTERNET# 32
SYNC# 32
EPRESENTATION# 32
KBC_MATRIX0#
D/A
DA0/GPI94
DA1/GPI95
DA2/GPI96
DA3/GPI97
BRIGHT_SETTING
TP119 Do Not Stuff
KBC_THERMALTRIP# 16
ENERGY_DET 23
CRT_DEC# 15
<--- -1 modify
RN32
SRN4K7J-8-GP
THERMAL----->
BATTERY----->
41 BAT_SDA
41 BAT_SCL
KBC_SDA2
KBC_SCL2
SMB
SDA2
SCL2
SDA1
SCL1
17,38,39 PM_SLP_S4#
SWD/GPIO66
SP
SPI_DI/GPIO77
SPI_DO/GPIO76/SHBM#
SPI_SCK/GPIO75
GPIO81
SPI
32 E-BUTTON#
22 BLUETOOTH_EN
28 WIRELESS_EN
30 AMP_SHUTDOWN#
R269
10KR2J-3-GP
GPIO01
GPIO03
GPIO06/HGPIO06
GPIO07/HGPIO07
GPIO23
LDRQ#/GPIO24/HGPIO01
GPIO30
GPIO31
GPIO32
GPIO33
GPIO40
GPIO42/TCK
GPIO43/TMS
GPIO44/TDI
GPIO45
GPIO46/TRST#
GPIO47/JEN0#
GPIO50/TDO
GPIO51
GPIO52/RDY#
GPIO53
IRRX2_IRSL0/GPIO70
IRTX/GPIO71
IRRX1/GPIO72
GPIO82/HGPIO00/TRIS#
PM_SLP_S3# 17,28,34,38,39
KBC_PWRBTN# 32
AC_IN# 40
LID_CLOSE# 32
PM_PWRBTN# 17
LDRQ0# 16
R611
Do Not Stuff
NUM_LED# 14
CAP_LED# 14
FRONT_PWRLED 14
STBY_LED 14
RSMRST#_KBC 17
AD_OFF 41
ELOCK# 32
CHG_LED 14
BT_BTN# 14
WLAN_TEST_LED 14
CHG_BCTL0 40
BT_LED 14
WIRELESS_BTN# 14
BLON_OUT 14
GMCH_BL_ON 7
KBC_GPIO70
KBC_GPIO71
KBC_GPIO72
TP120 Do Not Stuff
TP121 Do Not Stuff
TP122 Do Not Stuff
USB_PWR_EN# 22,27
<--- -1 modify
<--- -1 modify
SB modify
<--- -1 modify
R259
10KR2J-3-GP
CHG_BCTL0
CIR
R262
Do Not Stuff
32 CIR
28 E51_TxD
28 E51_RxD
14 CCD_ON
14 DC_BATFULL
28,34,42 S5_ENABLE
SOUT_CR/GPIO83/BADDR1
SIN_CR/CIRRX/GPIO87
GPIO84/HGPIO01/BADDR0
CIRTX/GPIO16/HGPIO04
GPIO34/CIRRX2
GPIO36
SER/IR
VCORF
R264
10KR2J-3-GP
C407
SCD1U16V2ZY-2GP
R276
Do Not Stuff
R260
Do Not Stuff
R263
Do Not Stuff
NON_FIR
AGND
GND
WPC8763LDG-1-GP
71.08763.A0G
G86
Do Not Stuff
SW1
ON
17 PSW_CLR#
KBC_MATRIX0#
R287
Do Not Stuff
10KR2J-3-GP
H Big KB(17")
L Small KB (Biwa)
55.4H001.S03G
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC WPC8763L
Size A3
Document Number
Biwa
Rev -2
Date: Thursday, March 01, 2007
Sheet 31 of 42

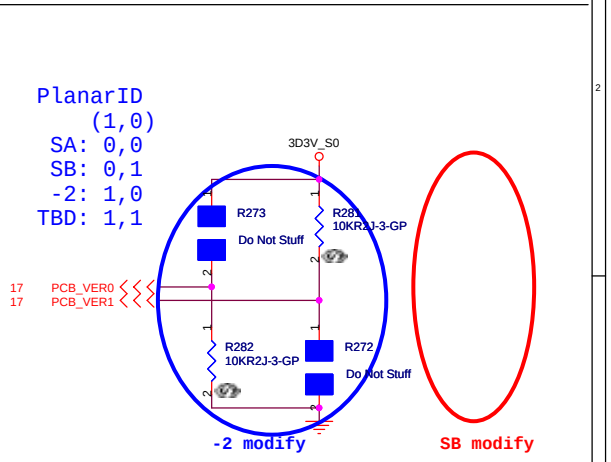






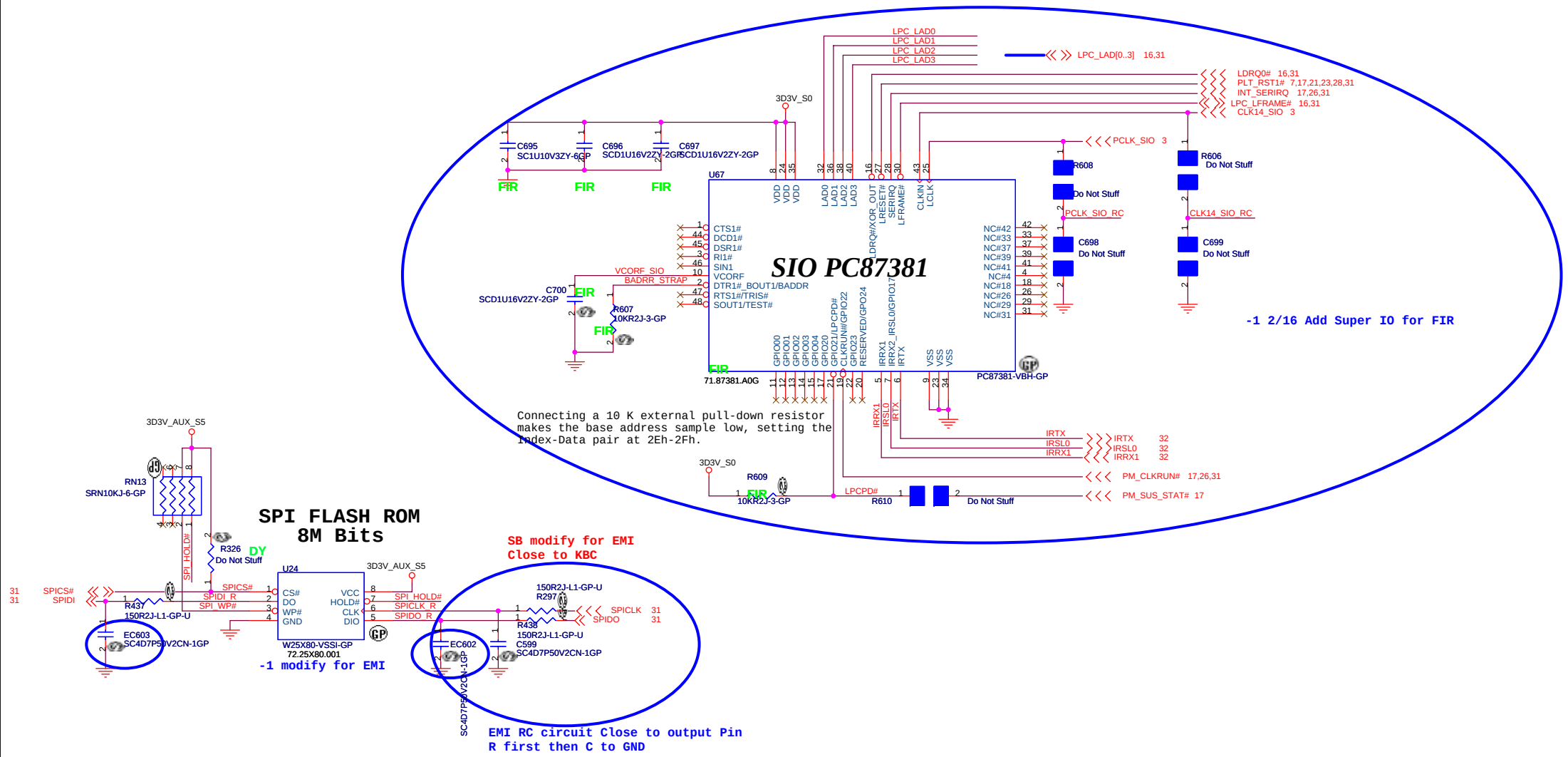






55.4H001.S03G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: *BUTTONs / KB / TOUCHPAD / FIR*		
Size	Document Number: Biwa	Rev: -2
Date: Thursday, March 01, 2007	Sheet 32 of 42	



55.4H001.S03G

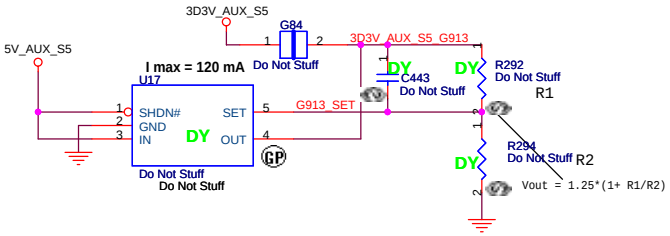
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

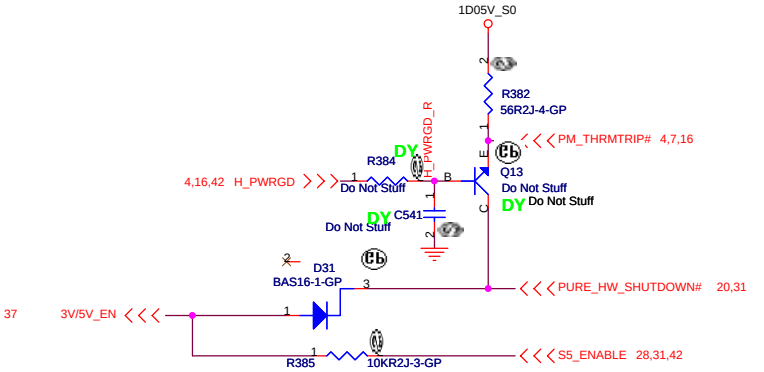
Title: BIOS & Super IO

Size	Document Number	Rev
A3	Biwa	-2

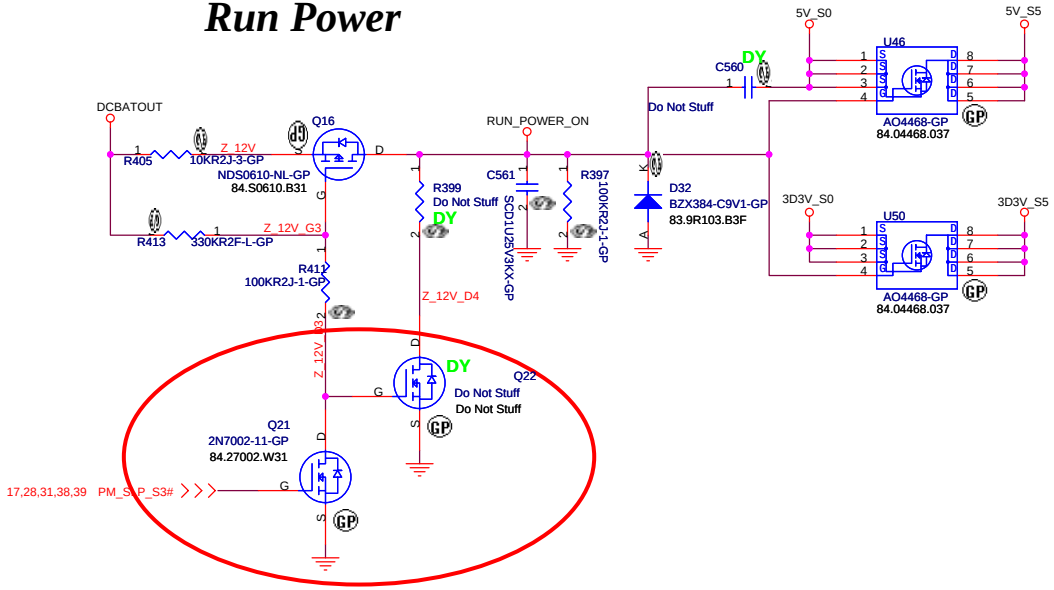
Date: Thursday, March 01, 2007 Sheet 33 of 42

Aux Power 3D3V_AUX_S5

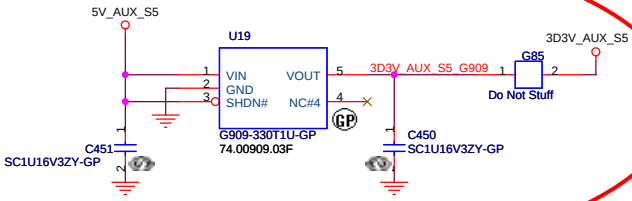




Run Power



Aux Power 3D3V_AUX_S5

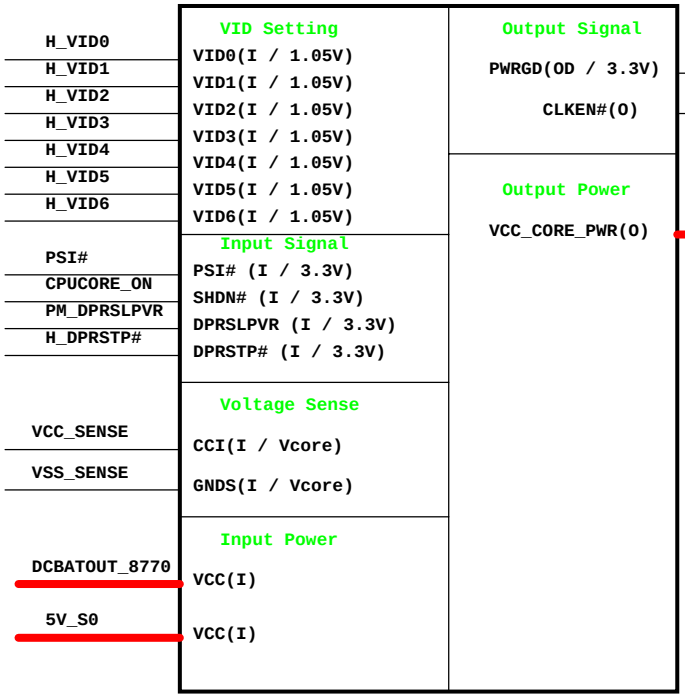


SB modify

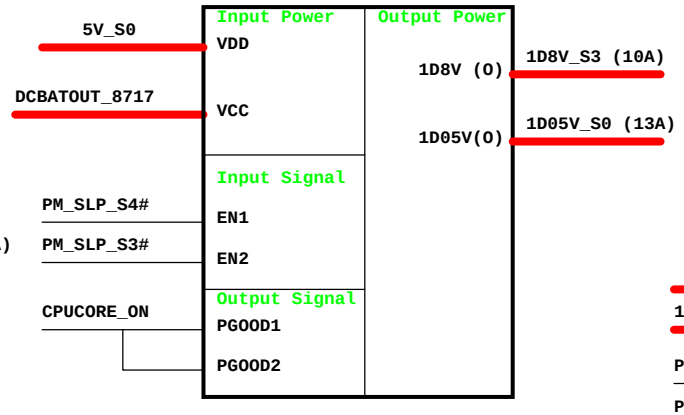
55.4H001.S03G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RUN POWER and 3D3V_AUX_S5		
Size	Document Number: Biwa	Rev: -1
Date: Thursday, March 01, 2007	Sheet 34 of 42	

CPU_CORE
MAXIM MAX8770



MAX8717
1D8V/1D05V



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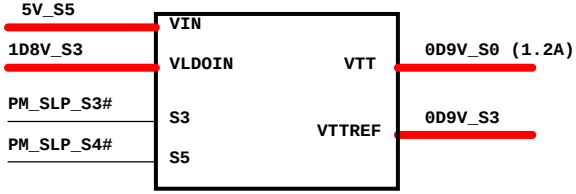
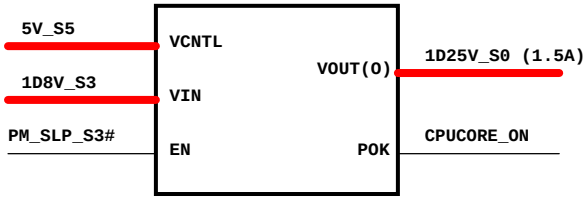


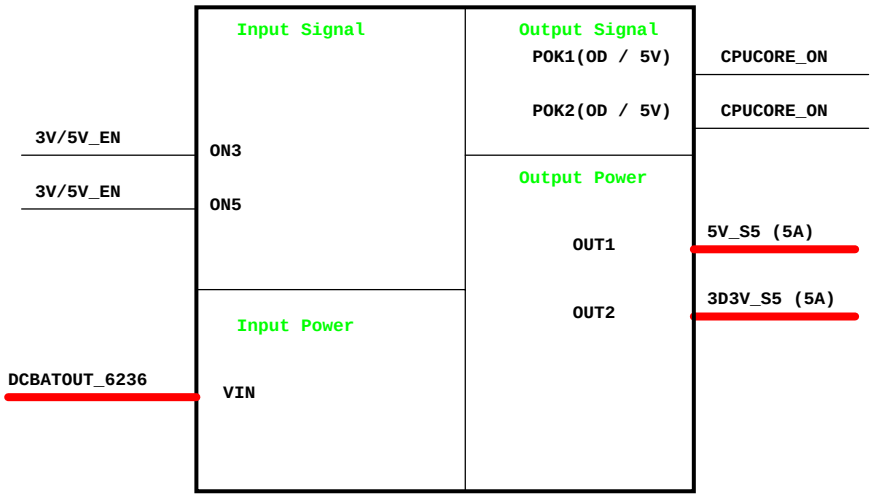
TPS51100

1D25V_S0

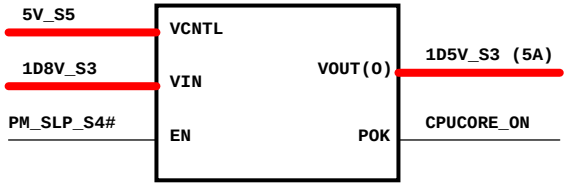


APL5915

ISL6236
5V/3D3V

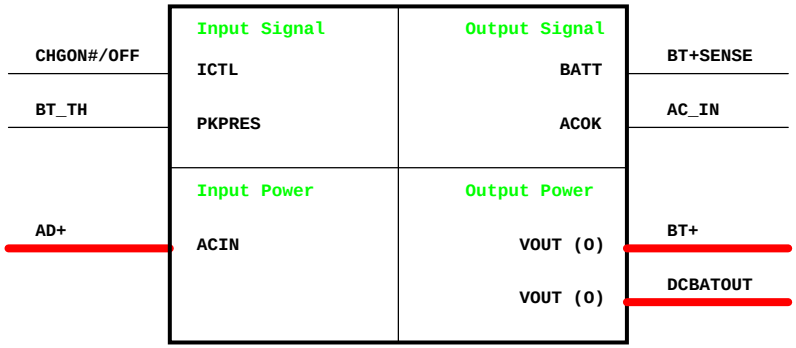


1D5V_S3



APL5912

Charger ISL6255



55.4H001.S03G

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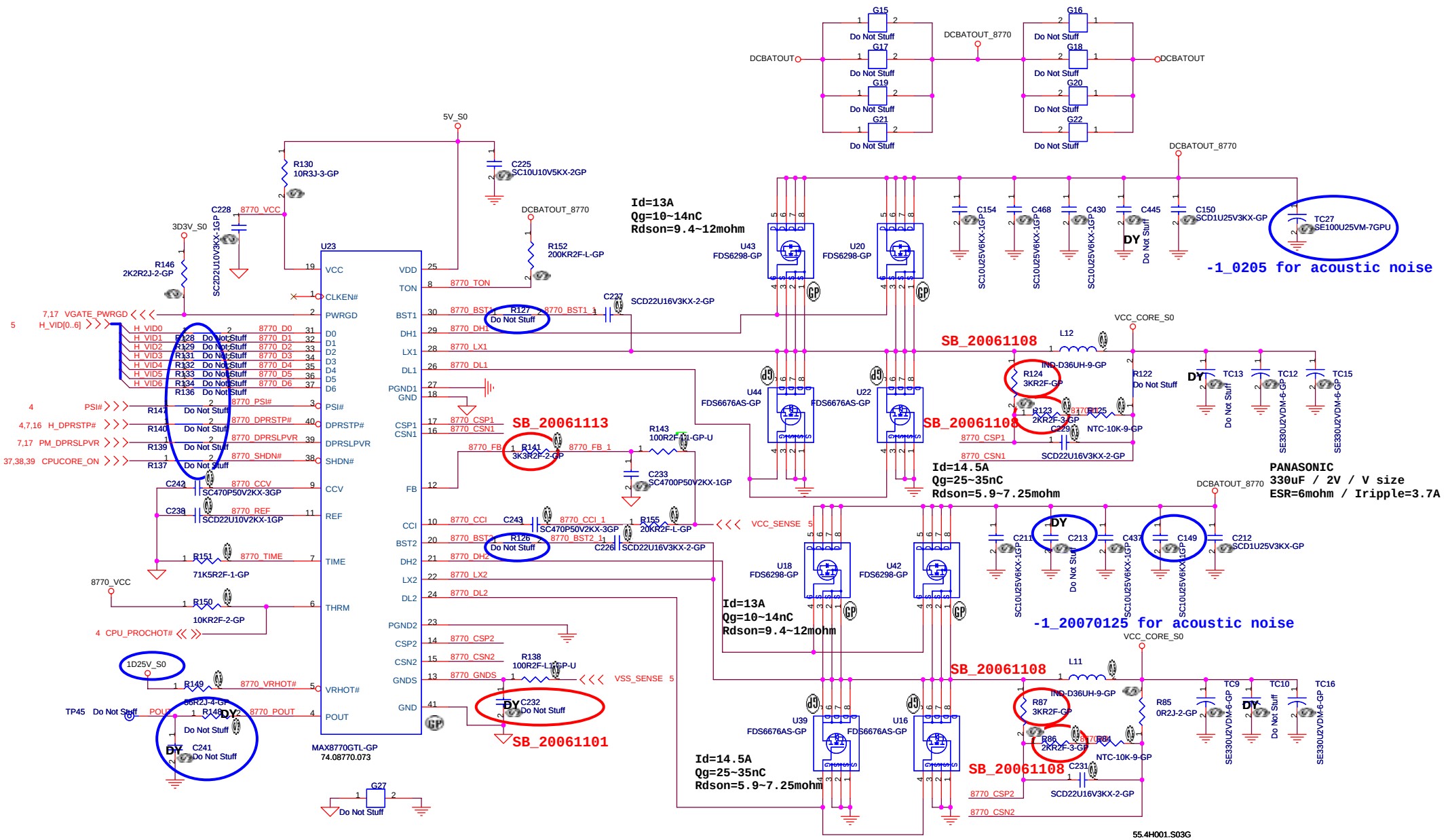
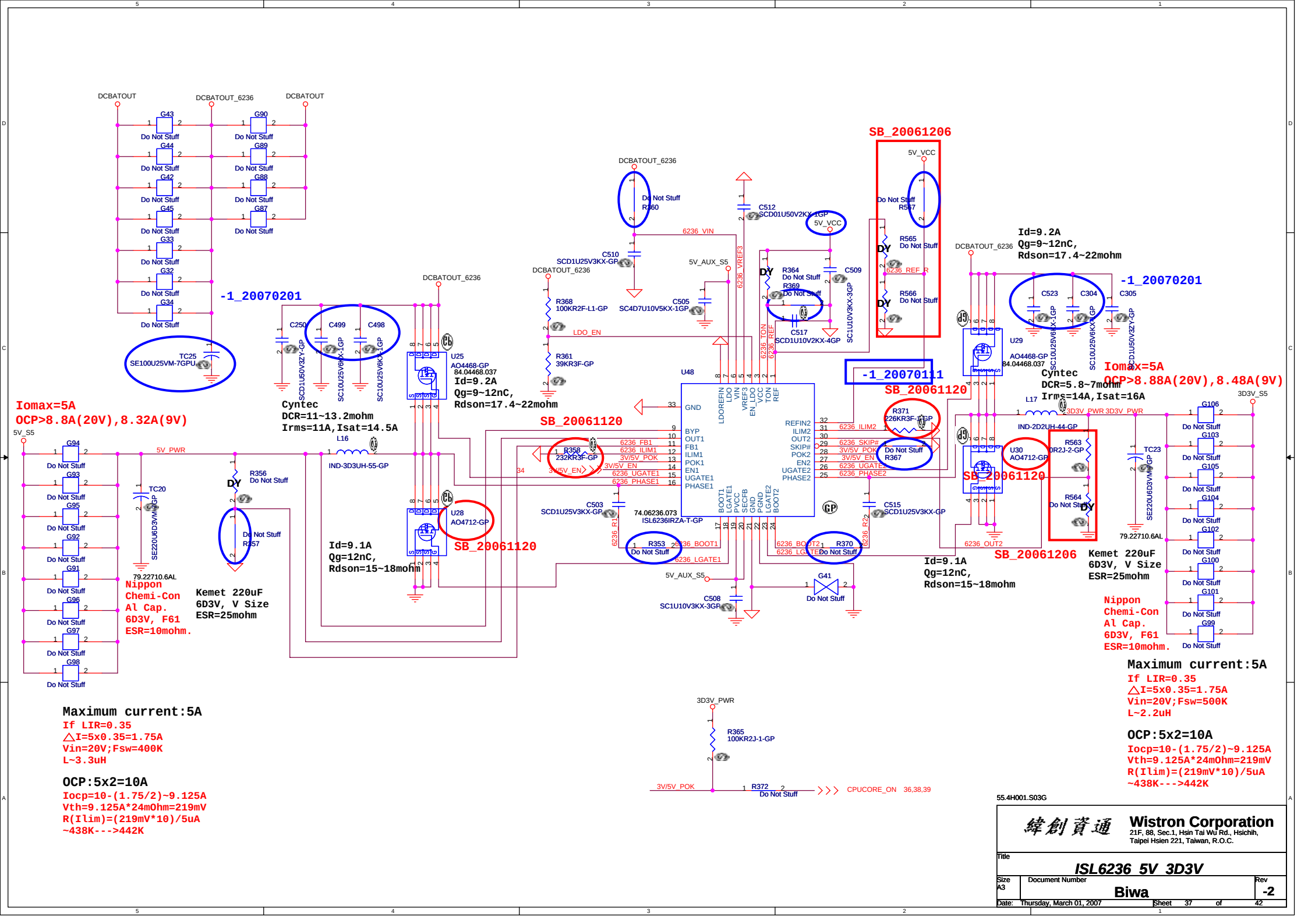
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

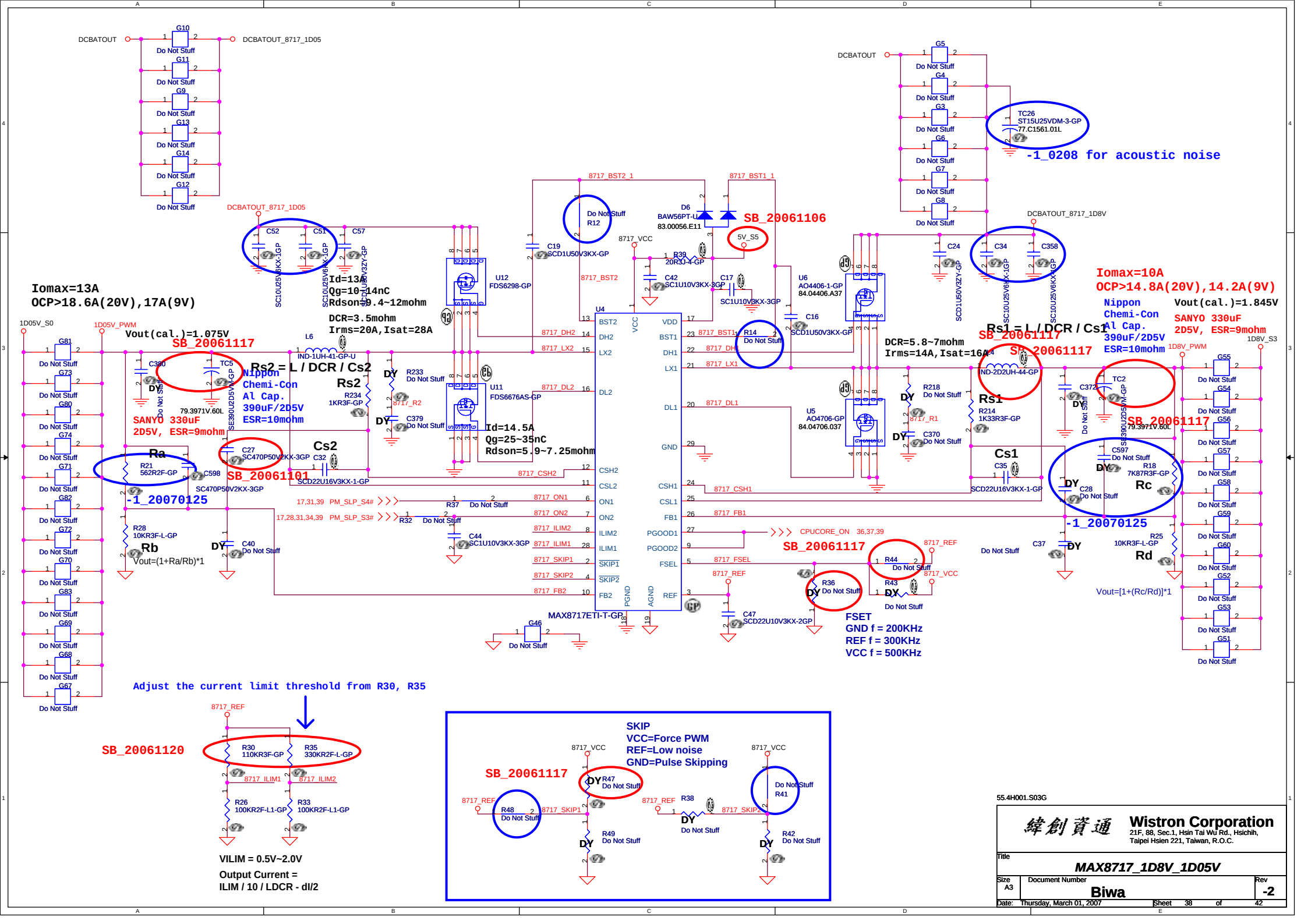
Title: Power Block Diagram

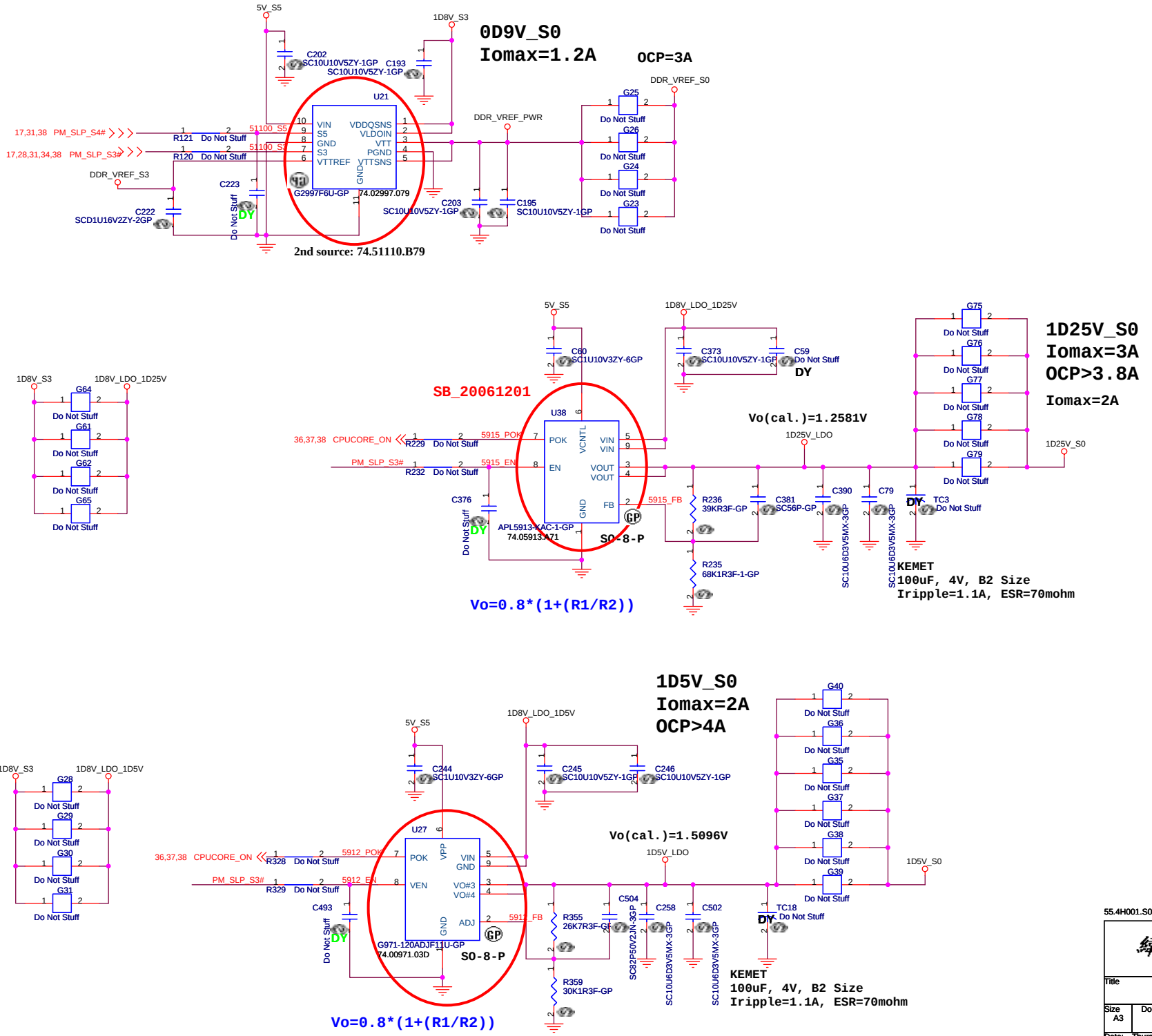
Size	Document Number	Rev
A3	Biwa	SA

Date: Thursday, March 01, 2007 Sheet 35 of 42


DCBATOUT
DCBATOUT_8770
DCBATOUT
G15
G16
G17
G18
G19
G20
G21
G22
Do Not Stuff
5V_S0
3D3V_S0
1D25V_S0
8770_VCC
U23
MAX8770GTL-GP
74.08770.073
VCC
CLKEN#
PWRGD
D0
D1
D2
D3
D4
D5
D6
PSI#
DPRSTP#
DPRSLPVR
SHDN#
CCV
REF
TIME
THRM
VRHOT#
POUT
VDD
TON
BST1
DH1
LX1
DL1
PGND1
GND
CSP1
CSN1
FB
CCI
BST2
DH2
LX2
DL2
PGND2
CSP2
CSN2
GNDS
GND
R130 10R3J-3-GP
C225 SC10U10V5KX-2GP
C228 8770_VCC
SC2D2U10V3KX-1GP
R146 2K2R2J-2-GP
R152 200KR2F-L-GP
R127 Do Not Stuff
C227 SCD22U16V3KX-2-GP
R128 Do Not Stuff
R129 Do Not Stuff
R131 Do Not Stuff
R132 Do Not Stuff
R133 Do Not Stuff
R134 Do Not Stuff
R136 Do Not Stuff
R147 Do Not Stuff
R140 Do Not Stuff
R139 Do Not Stuff
R137 Do Not Stuff
C242 SC470P50V2KX-3GP
C238 SCD22U10V2KX-1GP
R151 71K5R2F-1-GP
R150 10KR2F-2-GP
R149 56R2J-4-GP
R148 Do Not Stuff
C241 Do Not Stuff
TP45 Do Not Stuff
R141 3K3R2F-2-GP
SB_20061113
R143 100R2F-L1-GP-U
C233 SC4700P50V2KX-1GP
C243 SC470P50V2KX-3GP
R126 Do Not Stuff
C226 SCD22U16V3KX-2-GP
R155 20KR2F-L-GP
R138 100R2F-L1-GP-U
C232 Do Not Stuff
SB_20061101
G27 Do Not Stuff
VCC_SENSE
VSS_SENSE
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
U43 FDS6298-GP
U20 FDS6298-GP
U44 FDS6676AS-GP
U22 FDS6676AS-GP
C154 SC10U25V6KX-1GP
C468 SC10U25V6KX-1GP
C430 SC10U25V6KX-1GP
C445 Do Not Stuff
C150 SCD1U25V3KX-GP
TC27 SE100U25VM-7GPU
-1_0205 for acoustic noise
SB_20061108
L12 IND-D36UH-9-GP
R124 3KR2F-GP
R123 2KR2F-3-GP
R122 Do Not Stuff
R125 NTC-10K-9-GP
C229 SCD22U16V3KX-2-GP
TC13 Do Not Stuff
TC12 SE330U2VDM-6-GP
TC15 SE330U2VDM-6-GP
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
PANASONIC
330uF / 2V / V size
ESR=6mohm / Iripple=3.7A
U18 FDS6298-GP
U42 FDS6298-GP
C211 SC10U25V6KX-1GP
C213 Do Not Stuff
C437 SC10U25V6KX-1GP
C149 SC10U25V6KX-1GP
C212 SCD1U25V3KX-GP
-1_20070125 for acoustic noise
L11 IND-D36UH-9-GP
R87 3KR2F-GP
R86 2KR2F-3-GP
R84 NTC-10K-9-GP
C231 SCD22U16V3KX-2-GP
R85 0R2J-2-GP
TC9 SE330U2VDM-6-GP
TC10 Do Not Stuff
TC16 SE330U2VDM-6-GP
U39 FDS6676AS-GP
U16 FDS6676AS-GP
55.4H001.S03G
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VCC_CORE
Size A3
Document Number
Biwa
Rev -1
Date: Thursday, March 01, 2007
Sheet 36 of 42


DCBATOUT
DCBATOUT_6236
G43
G44
G42
G45
G33
G32
G34
G90
G89
G88
G87
Do Not Stuff
-1_20070201
TC25
SE100U25VM-7GPU
C250
C499
C498
SCD1U50V3ZY-GP
SC10U25V6KX-1GP
U25
AO4468-GP
84.04468.037
Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm
Cyntec
DCR=11~13.2mohm
Irms=11A,Isat=14.5A
Iomax=5A
OCP>8.8A(20V),8.32A(9V)
SB_20061120
5V_S5
G94
G93
G95
G92
G91
G96
G97
G98
5V_PWR
TC20
SE220U6D3VM-GP
79.22710.6AL
Nippon
Chemi-Con
Al Cap.
6D3V, F61
ESR=10mohm.
R356
DY
R357
L16
IND-3D3UH-55-GP
U28
AO4712-GP
Id=9.1A
Qg=12nC,
Rdson=15~18mohm
Kemet 220uF
6D3V, V Size
ESR=25mohm
Maximum current:5A
If LIR=0.35
△I=5x0.35=1.75A
Vin=20V;Fsw=400K
L~3.3uH
OCP:5x2=10A
Iocp=10-(1.75/2)~9.125A
Vth=9.125A*24mOhm=219mV
R(Ilim)=(219mV*10)/5uA
~438K--->442K
R360
C512
SCD01U50V2KX-1GP
5V_VCC
6236_VIN
C510
SCD1U25V3KX-GP
5V_AUX_S5
C505
SC4D7U10V5KX-1GP
R368
100KR2F-L1-GP
LDO_EN
R361
39KR3F-GP
R364
R369
C509
C517
SCD1U10V2KX-4GP
SC1U10V3KX-3GP
6236_TON
6236_REF
6236_VREF3
U48
GND
BYP
OUT1
FB1
ILIM1
POK1
EN1
UGATE1
PHASE1
LDOREFIN
LDO
VIN
VREF3
EN_LDO
VCC
TON
REF
REFIN2
ILIM2
OUT2
SKIP#
POK2
EN2
UGATE2
PHASE2
BOOT1
LGATE1
PVCC
SECFB
GND
PGND
LGATE2
BOOT2
6236_FB1
6236_ILIM1
3V/5V_POK
3V/5V_EN
6236_UGATE1
6236_PHASE1
6236_BOOT1
6236_LGATE1
6236_ILIM2
6236_SKIP#
6236_UGATE2
6236_PHASE2
6236_BOOT2
6236_LGATE2
R358
232KR3F-GP
R353
C503
SCD1U25V3KX-GP
74.06236.073
ISL6236IRZA-T-GP
R371
226KR3F-GP
R367
C515
R370
C508
SC1U10V3KX-3GP
G41
SB_20061206
-1_20070111
R565
R566
R567
Do Not Stuff
6236_REF_R
Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm
C523
C304
C305
SC10U25V6KX-1GP
SCD1U50V3ZY-GP
U29
AO4468-GP
84.04468.037
Cyntec
DCR=5.8~7mohm
Irms=14A,Isat=16A
Iomax=5A
OCP>8.88A(20V),8.48A(9V)
3D3V_S5
L17
3D3V_PWR
IND-2D2UH-44-GP
U30
AO4712-GP
R563
0R2J-2-GP
R564
TC23
SE220U6D3VM-GP
G106
G103
G105
G104
G102
G100
G101
G99
Id=9.1A
Qg=12nC,
Rdson=15~18mohm
Kemet 220uF
6D3V, V Size
ESR=25mohm
Nippon
Chemi-Con
Al Cap.
6D3V, F61
ESR=10mohm.
Maximum current:5A
If LIR=0.35
△I=5x0.35=1.75A
Vin=20V;Fsw=500K
L~2.2uH
OCP:5x2=10A
Iocp=10-(1.75/2)~9.125A
Vth=9.125A*24mOhm=219mV
R(Ilim)=(219mV*10)/5uA
~438K--->442K
3D3V_PWR
R365
100KR2J-1-GP
3V/5V_POK
R372
CPUCORE_ON 36,38,39
55.4H001.S03G
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6236 5V 3D3V
Size
A3
Document Number
Biwa
Rev
-2
Date: Thursday, March 01, 2007
Sheet 37 of 42


DCBATOUT
DCBATOUT_8717_1D05
DCBATOUT_8717_1D8V
Do Not Stuff
Iomax=13A
OCP>18.6A(20V),17A(9V)
Vout(cal.)=1.075V
SB_20061117
Rs2 = L / DCR / Cs2
Nippon Chemi-Con Al Cap. 390uF/2D5V ESR=10mohm
SANYO 330uF 2D5V, ESR=9mohm
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
DCR=3.5mohm
Irms=20A,Isat=28A
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
SB_20061101
-1_20070125
Ra
Rb
Rc
Rd
Cs1
Cs2
Rs1
Vout=(1+Ra/Rb)*1
Vout=[1+(Rc/Rd)]*1
SB_20061106
-1_0208 for acoustic noise
Iomax=10A
OCP>14.8A(20V),14.2A(9V)
Vout(cal.)=1.845V
DCR=5.8~7mohm
Irms=14A,Isat=16A
Rs1 = L / DCR / Cs1
MAX8717ETI-T-GP
FSET
GND f = 200KHz
REF f = 300KHz
VCC f = 500KHz
Adjust the current limit threshold from R30, R35
SB_20061120
VILIM = 0.5V~2.0V
Output Current =
ILIM / 10 / LDCR - dI/2
SKIP
VCC=Force PWM
REF=Low noise
GND=Pulse Skipping
SB_20061117
55.4H001.S03G
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
MAX8717_1D8V_1D05V
Size A3
Document Number
Biwa
Rev -2
Date: Thursday, March 01, 2007
Sheet 38 of 42



55.4H001.S03G

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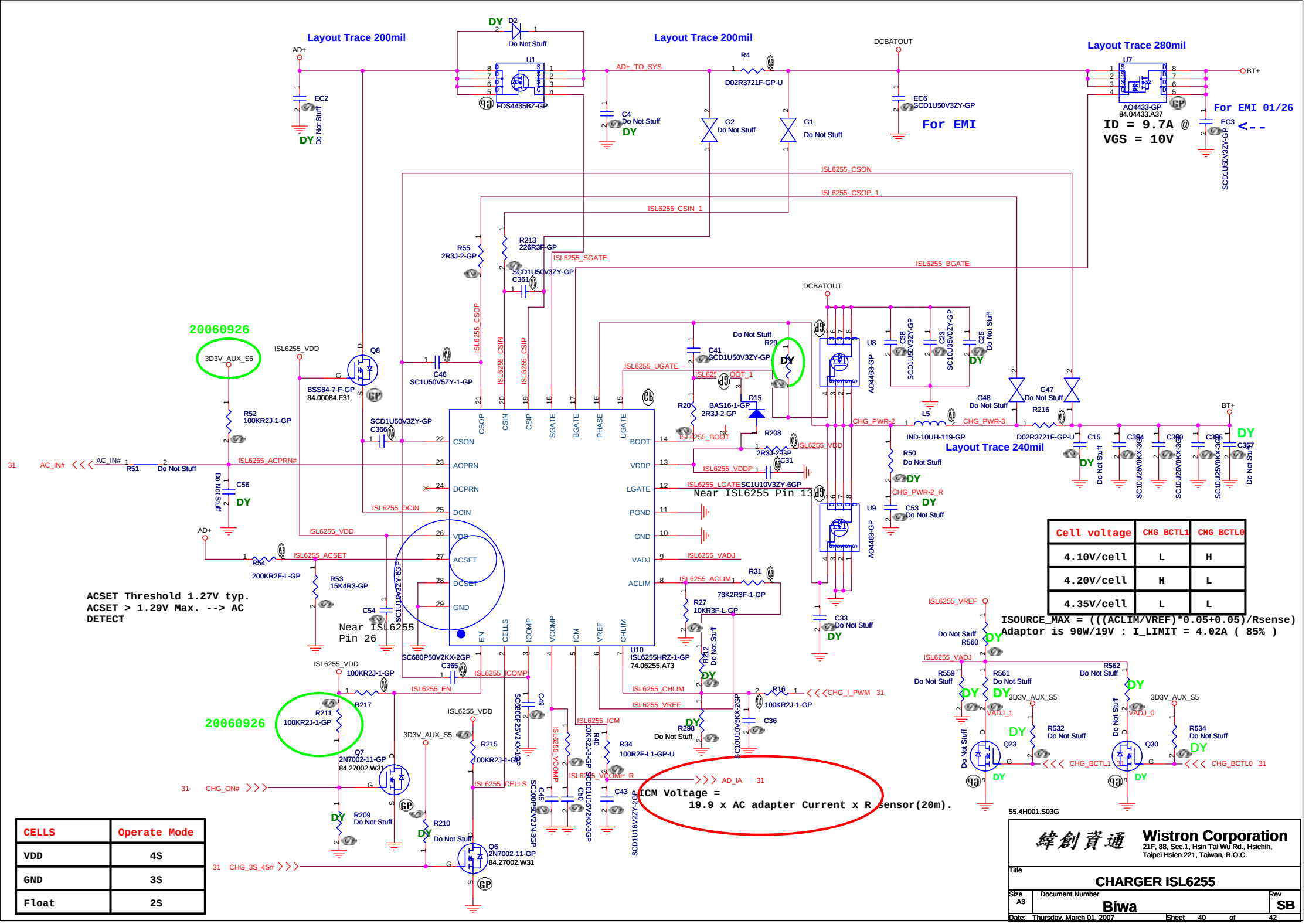
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D25V/1D5V/0D9V

Size	Document Number	Rev
A3	Biwa	SB

Date: Thursday, March 01, 2007 Sheet 39 of 42



Cell voltage	CHG_BCTL1	CHG_BCTL0
4.10V/cell	L	H
4.20V/cell	H	L
4.35V/cell	L	L

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

55.4H001.S03G

Wistron Corporation
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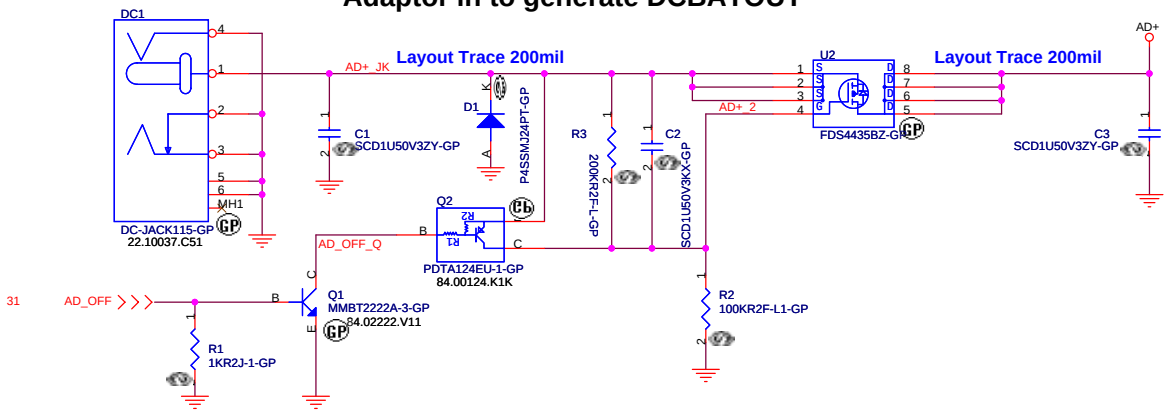
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER ISL6255

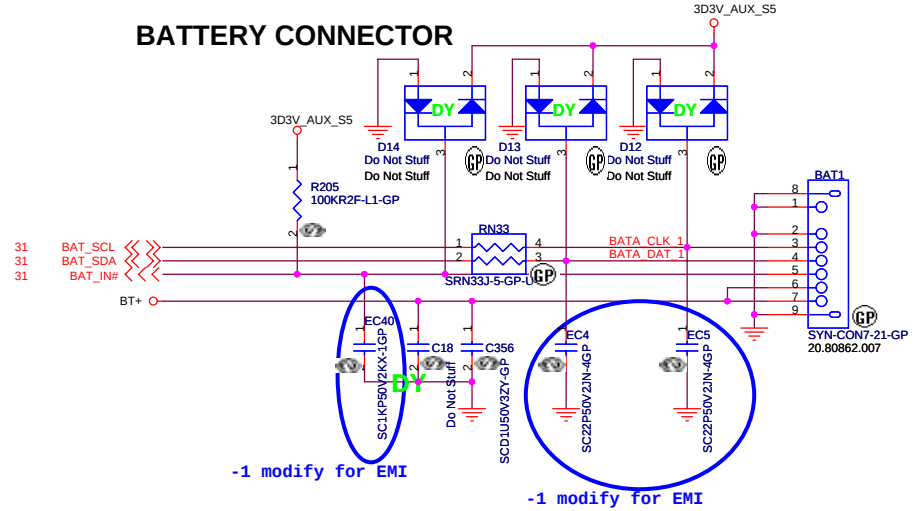
Size	Document Number	Rev
A3	Biwa	SB

Date: Thursday, March 01, 2007 Sheet 40 of 42

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



55.4H001.S03G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size A3	Document Number Biwa	Rev -1
Date: Thursday, March 01, 2007	Sheet 41 of 42	

EMI Capacitor

DCBATOUT
EC22 SCD1U25V3ZY-1GP
EC19 SCD1U25V3ZY-1GP
EC17 SCD1U25V3ZY-1GP
EC8 SCD1U25V3ZY-1GP
EC1 SCD1U25V3ZY-1GP

1D5V_S0
EC21 DY Do Not Stuff
EC26 DY Do Not Stuff

5V_AUX_S5
EC33 DY Do Not Stuff
EC30 DY Do Not Stuff

3D3V_S5
EC13 DY Do Not Stuff
EC32 DY Do Not Stuff
EC14 DY Do Not Stuff

5V_S5
EC11 SCD1U10V2KX-4GP
EC29 DY Do Not Stuff

5V_S0
EC35 DY Do Not Stuff
EC50 DY Do Not Stuff
EC36 DY Do Not Stuff
EC16 DY Do Not Stuff

1D05V_S0
EC24 DY Do Not Stuff
EC51 DY Do Not Stuff
EC20 DY Do Not Stuff
EC18 DY Do Not Stuff

3D3V_S0
EC42 DY Do Not Stuff
EC10 DY Do Not Stuff
EC25 DY Do Not Stuff
EC12 DY Do Not Stuff

2006/12/04
SB for EMI

DCBATOUT
EC7 SCD1U25V3ZY-1GP
EC41 SCD1U25V3ZY-1GP
EC9 SCD1U25V3ZY-1GP
EC43 SCD1U25V3ZY-1GP
EC27 SCD1U25V3ZY-1GP
EC23 SCD1U25V3ZY-1GP

5V_S0
EC72 DY Do Not Stuff
EC73 DY Do Not Stuff
EC74 DY Do Not Stuff

3D3V_S0
EC75 DY Do Not Stuff
EC77 DY Do Not Stuff
EC76 DY Do Not Stuff
EC78 DY Do Not Stuff
EC80 DY Do Not Stuff
EC79 DY Do Not Stuff
EC81 DY Do Not Stuff

1D05V_S0
EC82 DY Do Not Stuff
EC83 DY Do Not Stuff
EC84 DY Do Not Stuff

VCC_CORE_S0
EC85 DY Do Not Stuff
EC87 DY Do Not Stuff
EC86 DY Do Not Stuff
EC88 DY Do Not Stuff

1D8V_S3
EC92 DY Do Not Stuff
EC91 DY Do Not Stuff
EC93 DY Do Not Stuff
EC90 DY Do Not Stuff
EC89 DY Do Not Stuff

5V_USB2_S5
EC97 DY Do Not Stuff
EC96 DY Do Not Stuff
EC98 DY Do Not Stuff
EC95 DY Do Not Stuff
EC94 DY Do Not Stuff

DCBATOUT
EC99 SCD1U25V3ZY-1GP
EC100 SCD1U25V3ZY-1GP

3D3V_AUX_S5
EC105 SCD1U10V2KX-4GP

BT+
EC139 SCD1U10V2KX-4GP

-1_20070115

TOP

CARD READER BD
H9 HOLE
H8 HOLE
34.42Y01.011

CPU
K1 DY Do Not Stuff
Do Not Stuff

Near H8
K2 DY Do Not Stuff
Do Not Stuff

-1_0131 for thermal

BOTTOM

CPU Thermal Module
H18 HOLE
H21 HOLE
H19 HOLE
H22 HOLE
H20 HOLE
34.42Y01.011

MDC
H15 HOLE
H16 HOLE
34.42Y01.011

SB
34.42Y01.011

MINI CARD
H26 HOLE
H25 HOLE
34.4G502.001

CPU
K4 DY Do Not Stuff
Do Not Stuff

PCMCIA
K5 DY Do Not Stuff Do Not Stuff
K10 DY Do Not Stuff Do Not Stuff
K6 DY Do Not Stuff Do Not Stuff
K9 DY Do Not Stuff Do Not Stuff

Near H8
K8 DY Do Not Stuff
Do Not Stuff

Near H15
K7 DY Do Not Stuff
Do Not Stuff

Near CCD
K3 DY Do Not Stuff
Do Not Stuff

Between NB & DIMM
K11 SPRING-23-GP
34.39S07.001
K12 SPRING-23-GP
34.39S07.001

Between NB & DIMM
K13 SPRING-35-GP
34.41P18.001
K14 SPRING-35-GP
34.41P18.001

-1_20070206

H2 Do Not Stuff
H4 Do Not Stuff
H3 Do Not Stuff
H11 Do Not Stuff
H5 Do Not Stuff
H6 Do Not Stuff
H12 Do Not Stuff
H10 Do Not Stuff
H1 Do Not Stuff
H7 Do Not Stuff
H13 Do Not Stuff

GP8 Do Not Stuff
GP7 Do Not Stuff
GP5 Do Not Stuff
GP11 Do Not Stuff
GP2 Do Not Stuff
GP3 Do Not Stuff
GP1 Do Not Stuff
GP12 Do Not Stuff

Unused gate

5V_S0
U3D TSAHCT125PW-GP

KBC JTAG Test Pad

31,32	KCOL1	KCOL1	TP88	Do Not Stuff
31,32	KCOL2	KCOL2	TP91	Do Not Stuff
31,32	KCOL3	KCOL3	TP92	Do Not Stuff
31,32	KCOL4	KCOL4	TP90	Do Not Stuff
31,32	KCOL6	KCOL6	TP89	Do Not Stuff
31,32	KCOL7	KCOL7	TP93	Do Not Stuff

DFX Test Point

3D3V_AUX_S5		TP97	Do Not Stuff
3D3V_S5		TP102	Do Not Stuff
5V_S5		TP100	Do Not Stuff
4,16,34	H_PWRGD	TP31	Do Not Stuff
28,31,34	S5_ENABLE	TP86	Do Not Stuff
4,6	H_CPURST#	TP39	Do Not Stuff

Test Point放在Dimm Door打開可量測處

55.4H001.S03G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss
Size: Document Number: Biwa
Rev: -1
Date: Thursday, March 01, 2007
Sheet 42 of 42