1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

X362 MLB SCHEMATIC

LAST_MODIFICATION=Tue Aug 30 11:06:16 2016

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
9	0006939272	ENGINEERING RELEASED	2016-08-30

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00515	1	SCHEM,MLB,X362	SCH	CRITICAL	
820-00239	1	PCBF,MLB,X362	PCB	CRITICAL	

?

DRAWING TITLE: SCHEM,MLB,X362

Apple Inc.

DRAWING NUMBER: 051-00515 SIZE: D

REVISION: 9.0.0

BRANCH: dvt-fab09-0

PAGE: 1 OF 145

SHEET: 1 OF 119

BOM Groups

BOM GROUP	BOM OPTIONS
X362_COMMON	ALTERNATE,COMMON,X362_COMMON1,X362_COMMON2,X362_COMMON3,X362_PROGPARTS
X362_COMMON1	SE:PROD,BOARD_ID:8,T208_PROG:REV5,TBTTHRM_SNS,S3XCLK:INT
X362_COMMON2	EDP_ENABLE,XDP:YES,PCH_CLK:GRNCLK,TBT_DBG,SAMCONN,SKIP_5V3V3:AUDIBLE,SOC_BOOT:SPI
X362_COMMON3	CPUTHRM:ALRT,TBTTHRM:ALRT,LOADRC:NO,CUMULUS_IPD,S3_STATE:YES,VCCPLLOC:S3
X362_PROGPARTS	BOOTROM_PROG,SMC_PROG,AR_LT_PROG,AR_RT_PROG,WIFI_PROG,BTROM_PROG
X362_DEVEL:ENG	ALTERNATE,DBGLED,USBC_DBG,XDP_CONN:YES,WIFI_DBG,S3X_DBG,DEBUG_BUTTON,LOADISNS
X362_DEVEL:DVT	ALTERNATE,USBC_DBG,XDP_CONN:YES,WIFI_DBG
X362_DEVEL:PVT	ALTERNATE

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00266	1	CPU,SKLU,SR2JK,PRQ,2.9,28W,1.05,B1356	U0500	CRITICAL	CPU_SKL23:2.9G
337S00267	1	CPU,SKLU,SR2JJ,PRQ,3.1,28W,1.1,B1356	U0500	CRITICAL	CPU_SKL23:3.1G
337S00268	1	CPU,SKLU,SR2JH,PRQ,3.3,28W,1.1,B1356	U0500	CRITICAL	CPU_SKL23:3.3G
998-04195	1	INTERPOSER,VTT ADAPTER,SKL-U,BGA1356	U0500	CRITICAL	CPU_SOCKET
338S00254	2	IC,TBT,ALPINE RIDGE,QSTY,PRQ,C1,CSP337	U2800,UB000	CRITICAL	
353S00961	4	IC,CD3215,ACE,C00,USB PWR SW,BLNK,BGA96	U3100,U3200,UB300,UB400	CRITICAL	
338S00276	1	IC,CNTLR,S3X,B1,FCBGA900	U8600	CRITICAL	
333S00055	1	IC,LPDDR3-1600,4GBIT,25NM,A,276B	POP8600	CRITICAL	POP_4GBIT
333S00056	1	IC,LPDDR3-1600,8GBIT,25NM,A,276B	POP8600	CRITICAL	POP_8GBIT
343S00147	1	IC,SLG4AP41172,PAK3,STQFN20	U3620	CRITICAL	
338S00221	1	IC,PMU,SN650839,7X7MM,BGA168	U7800	CRITICAL	
353S01016	1	IC,ISL9239HIZ,PMU,TUBA,WCSP40,2.1X3.3MM	U7000	CRITICAL	
338S00227	1	IC,PMU,PICCOLO,D2231A0,OTP-AK,WLCSP96	U9300	CRITICAL	

Programmables (All Builds)

EFI ROM

341S00698	1	IC,EFI ROM (V0193) DVT,X362	U6100	CRITICAL	BOOTROM_PROG

SMC ROM

341S00700	1	IC,SMC-B1,EXT (V2.37F6) PVT,X362	U5000	CRITICAL	SMC_PROG

TBT ROMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S00717	1	T29,AR1 (VTBD) PVT,X362	U2890	CRITICAL	AR_LT_PROG
341S00718	1	T29,AR2 (VTBD) PVT,X362	UB090	CRITICAL	AR_RT_PROG

WIFI/BT ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S00715	1	IC,BT ROM (V32) PVT,X362/X363	U3750	CRITICAL	BTROM_PROG
341S00716	1	WIFI ROM (P108) PVT,WW1,X362/X363	U3710	CRITICAL	WIFI_PROG

Variable BOM Groups
Development/Base BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00055	1	COMMON PARTS,MLB,X362	BASE	CRITICAL	BASE_BOM
985-00070	1	DEV,MLB,X362	DEVEL	CRITICAL	DEVEL_BOM

Main DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00069	4	IC,SDRAM,LPDDR3-2133,16GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	8G_MICRON_2133
333S00070	4	IC,SDRAM,LPDDR3-2133,32GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	16G_MICRON_2133
333S00068	4	IC,SDRAM,LPDDR3-2133,16GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	8G_SAMSUNG_2133
333S00050	4	IC,SDRAM,LPDDR3-2133,32GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	16G_SAMSUNG_2133

Main DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM_8G_MICRON_2133	8G_MICRON_2133,RAMCFG4_L,RAMCFG3_L,RAMCFG2_L,RAMCFG1_L
RAM_16G_MICRON_2133	16G_MICRON_2133,RAMCFG4_L,RAMCFG3_L,RAMCFG1_L
RAM_8G_SAMSUNG_2133	8G_SAMSUNG_2133,RAMCFG4_L,RAMCFG3_L,RAMCFG2_L,RAMCFG0_L
RAM_16G_SAMSUNG_2133	16G_SAMSUNG_2133,RAMCFG4_L,RAMCFG3_L,RAMCFG0_L

NAND Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00124	4	NAND,1ZNM,64GB,TOGG,HPN,128G,LGA60	U9100,U9120,U9200,U9220	CRITICAL	NAND_SDISK_256GB
335S00125	4	NAND,1ZNM,128GB,TOGG,HPN,128G,LGA60	U9100,U9120,U9200,U9220	CRITICAL	NAND_SDISK_512GB
335S00126	4	NAND,1ZNM,256GB,TOGG,HPN,128G,LGA60	U9100,U9120,U9200,U9220	CRITICAL	NAND_SDISK_1TB
335S00261	4	NAND,TGDDR2,128GX4,15NM,HP,USHD,T2,LGA60	U9100,U9120,U9200,U9220	CRITICAL	NAND_TSHBA_256GB
335S00262	4	NAND,TGDDR2,128GX8,15NM,HP,USHD,T2,LGA60	U9100,U9120,U9200,U9220	CRITICAL	NAND_TSHBA_512GB
335S00263	4	NAND,TGDDR2,128GX16,15NM,HP,UHD,T2,LGA60	U9100,U9120,U9200,U9220	CRITICAL	NAND_TSHBA_1TB

NAND Straps

BOM GROUP	BOM OPTIONS
SAND_256G	ALTERNATE,NAND_SDISK_256GB,POP_4GBIT,CAPACITY1,CAPACITY0
SAND_512G	ALTERNATE,NAND_SDISK_512GB,POP_4GBIT,CAPACITY2
SAND_1T	ALTERNATE,NAND_SDISK_1TB,POP_8GBIT,CAPACITY2,CAPACITY0
TOSH_256G	ALTERNATE,NAND_TSHBA_256GB,POP_4GBIT,CAPACITY1,CAPACITY0
TOSH_512G	ALTERNATE,NAND_TSHBA_512GB,POP_4GBIT,CAPACITY2
TOSH_1T	ALTERNATE,NAND_TSHBA_1TB,POP_8GBIT,CAPACITY2,CAPACITY0

CPU DRAM CFG Chart

DIE REV	CFG 4
A	0
B	1

SPEED	CFG 3
2133	0
1866	1

CAPACITY	CFG 2
8GB	0
16GB	1

VENDOR	CFG 1	CFG 0
HYNIX	0	0
MICRON	0	1
SAMSUNG	1	0
N/A	1	1

Strategic Silicon

PART#	STRATEGIC VALUE	COMMENT
337S00266	08	CPU
337S00267	08	CPU
337S00268	08	CPU
333S00050	07	MEMORY
333S00068	07	MEMORY
333S00069	07	MEMORY
333S00070	07	MEMORY
335S00124	02	NAND
335S00125	02	NAND
335S00126	02	NAND
335S00261	02	NAND
335S00262	02	NAND
335S00263	02	NAND
333S00025	02	S3X DRAM
333S00026	02	S3X DRAM
333S00055	02	S3X DRAM
333S00056	02	S3X DRAM
333S00107	02	S3X DRAM
333S00108	02	S3X DRAM
998-06736	02	S3X CONTROLLER

PART#	STRATEGIC VALUE	COMMENT
338S00227	02	PICCOLO
343S00135	10	T208
343S00136	10	T208
343S00137	10	T208
343S00138	10	T208
338S00193	09	BERKELIUM
353S3978	02	MOJAVE
338S00147	02	SECURE ELEMENT
338S00254	08	ALPINE RIDGE
353S00961	09	ACE
338S00142	09	CLIFDEN
353S00685	07	AUDIO AMP
353S4316	08	BAYSIDE
338S00221	08	BANJO
353S01016	09	TUBA
339S00056	05	ICEBOCK
343S00147	08	PAK
359S00006	08	GREEN CLOCK
353S00795	09	DEBUG MUX

SYNC_MASTER=SHART_J44 SYNC_DATE=11/27/2012

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D

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BRANCH dvt-fab09-0

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00055	COMMON PARTS,MLB,X362	X362_COMMON
985-00070	DEV,MLB,X362	X362_DEVEL:DVT
639-01870	MLB,2.9G,SAM-8G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,SAND_256G
639-01871	MLB,2.9G,SAM-16G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,SAND_256G
639-01872	MLB,2.9G,MIC-8G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,SAND_256G
639-01873	MLB,2.9G,MIC-16G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,SAND_256G
639-01984	MLB,2.9G,SAM-8G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,SAND_512G
639-01985	MLB,2.9G,SAM-16G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,SAND_512G
639-01986	MLB,2.9G,MIC-8G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,SAND_512G
639-01987	MLB,2.9G,MIC-16G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,SAND_512G
639-02517	MLB,2.9G,SAM-8G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,SAND_1T
639-02518	MLB,2.9G,SAM-16G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,SAND_1T
639-02519	MLB,2.9G,MIC-8G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,SAND_1T
639-02520	MLB,2.9G,MIC-16G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,SAND_1T
639-01874	MLB,3.1G,SAM-8G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,SAND_256G
639-01875	MLB,3.1G,SAM-16G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,SAND_256G
639-01876	MLB,3.1G,MIC-8G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,SAND_256G
639-01877	MLB,3.1G,MIC-16G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,SAND_256G
639-01883	MLB,3.1G,SAM-8G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,SAND_512G
639-01884	MLB,3.1G,SAM-16G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,SAND_512G
639-01885	MLB,3.1G,MIC-8G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,SAND_512G
639-01886	MLB,3.1G,MIC-16G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,SAND_512G
639-01887	MLB,3.1G,SAM-8G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,SAND_1T
639-01888	MLB,3.1G,SAM-16G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,SAND_1T
639-01889	MLB,3.1G,MIC-8G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,SAND_1T
639-01890	MLB,3.1G,MIC-16G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,SAND_1T
639-02221	MLB,3.3G,SAM-8G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,SAND_256G
639-02222	MLB,3.3G,SAM-16G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,SAND_256G
639-02223	MLB,3.3G,MIC-8G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,SAND_256G
639-02224	MLB,3.3G,MIC-16G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,SAND_256G
639-01891	MLB,3.3G,SAM-8G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,SAND_512G
639-01892	MLB,3.3G,SAM-16G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,SAND_512G
639-01893	MLB,3.3G,MIC-8G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,SAND_512G
639-01894	MLB,3.3G,MIC-16G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,SAND_512G
639-01895	MLB,3.3G,SAM-8G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,SAND_1T
639-01896	MLB,3.3G,SAM-16G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,SAND_1T
639-01897	MLB,3.3G,MIC-8G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,SAND_1T
639-01898	MLB,3.3G,MIC-16G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,SAND_1T

BOM NUMBER	BOM NAME	BOM OPTIONS
639-01988	MLB,NO CPU,X362	BASE_BOM,DEVEL_BOM,RAM_16G_SAMSUNG_2133,SAND_512G
639-01989	MLB,CPU SOCKET,X362	BASE_BOM,DEVEL_BOM,CPU_SOCKET,RAM_16G_SAMSUNG_2133,SAND_512G
639-02521	MLB,2.9G,SAM-8G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,TOSH_256G
639-02522	MLB,2.9G,SAM-16G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,TOSH_256G
639-02523	MLB,2.9G,MIC-8G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,TOSH_256G
639-02524	MLB,2.9G,MIC-16G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,TOSH_256G
639-02525	MLB,2.9G,SAM-8G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,TOSH_512G
639-02526	MLB,2.9G,SAM-16G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,TOSH_512G
639-02527	MLB,2.9G,MIC-8G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,TOSH_512G
639-02528	MLB,2.9G,MIC-16G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,TOSH_512G
639-02529	MLB,2.9G,SAM-8G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,TOSH_1T
639-02530	MLB,2.9G,SAM-16G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,TOSH_1T
639-02531	MLB,2.9G,MIC-8G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,TOSH_1T
639-02532	MLB,2.9G,MIC-16G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,TOSH_1T
639-02533	MLB,3.1G,SAM-8G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,TOSH_256G
639-02534	MLB,3.1G,SAM-16G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,TOSH_256G
639-02535	MLB,3.1G,MIC-8G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,TOSH_256G
639-02536	MLB,3.1G,MIC-16G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,TOSH_256G
639-02537	MLB,3.1G,SAM-8G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,TOSH_512G
639-02538	MLB,3.1G,SAM-16G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,TOSH_512G
639-02539	MLB,3.1G,MIC-8G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,TOSH_512G
639-02540	MLB,3.1G,MIC-16G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,TOSH_512G
639-02541	MLB,3.1G,SAM-8G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,TOSH_1T
639-02542	MLB,3.1G,SAM-16G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,TOSH_1T
639-02543	MLB,3.1G,MIC-8G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,TOSH_1T
639-02544	MLB,3.1G,MIC-16G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,TOSH_1T
639-02545	MLB,3.3G,SAM-8G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,TOSH_256G
639-02546	MLB,3.3G,SAM-16G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,TOSH_256G
639-02547	MLB,3.3G,MIC-8G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,TOSH_256G
639-02548	MLB,3.3G,MIC-16G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,TOSH_256G
639-02549	MLB,3.3G,SAM-8G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,TOSH_512G
639-02550	MLB,3.3G,SAM-16G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,TOSH_512G
639-02551	MLB,3.3G,MIC-8G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,TOSH_512G
639-02552	MLB,3.3G,MIC-16G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,TOSH_512G
639-02553	MLB,3.3G,SAM-8G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,TOSH_1T
639-02554	MLB,3.3G,SAM-16G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,TOSH_1T
639-02555	MLB,3.3G,MIC-8G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,TOSH_1T
639-02556	MLB,3.3G,MIC-16G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,TOSH_1T

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
152S00367	152S00266		ALL		Text note to be updated
152S00368	152S00269		ALL		Text note to be updated
152S00370	152S00270		ALL		Text note to be updated
353S4068	353S4070		ALL		Text note to be updated
353S00772	353S4070		ALL		Text note to be updated
138S00086	138S0884		ALL		Text note to be updated
107S0248	107S0250		ALL		TFT alt to Cyntec
152S00434	152S1829		ALL		Text note to be updated
371S00019	371S0463		ALL		Rohm alt to Rohm
353S00107	353S3239	ANY	ALL		Onsemi alt to Intersil
353S00231	353S3987		ALL		NXP alt to TI
333S00025	333S00055	POP_4GBIT	ALL		MICRON SSD POP ALT for HYNIX
333S00026	333S00056	POP_8GBIT	ALL		MICRON SSD POP ALT for HYNIX
333S00107	333S00055	POP_4GBIT	ALL		HYNIX SSD POP REPLACEMENT for HYNIX
333S00108	333S00056	POP_8GBIT	ALL		HYNIX SSD POP REPLACEMENT for HYNIX

138S0701	138S0689		ALL		Text note to be updated
138S00012	138S0771		ALL		Text note to be updated
138S0772	138S00013		ALL		Text note to be updated
152S00401	152S0529		ALL		Text note to be updated
152S00344	152S1683		ALL		Text note to be updated
152S00331	152S00283		ALL		Text note to be updated
152S2034	152S00190		ALL		Text note to be updated
197S0613	197S0612		ALL		Text note to be updated
311S00121	311S0398		ALL		Text note to be updated
371S0713	371S0558		ALL		Text note to be updated
371S00074	371S0602		ALL		Text note to be updated

SYNC_MASTER:J29_JADE SYNC_DATE:04/07/2016

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D

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BRANCH dvt-fab09-0

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BOARD MECHANICALS

Shield Cans - BOTTOM SIDE

ALPINE RIDGE - LIO (U2800) - 806-06077

SH0418 SM
SHLD-FENCE-ALPINE-X379

LPDDR3 (U2300 ~ U2600) - 806-06167

SH0415 SM
SHLD-FENCE-X379

NAND - BOTTOM SOUTH (U9120) - 806-05945

SH0417 SM
SHLD-FENCE-NAND-BOT-SOUTH-X379

S3X (U8600) - 806-06023

SH0414 SM
SHLD-FENCE-S3X-X379

NAND - BOTTOM NORTH (U9200) - 806-06265

SH0419 SM
SHLD-FENCE-MLB-NAND-BTM-NORTH-X379

ALPINE RIDGE - RIO (UB000) - 806-06077

SH0420 SM
SHLD-FENCE-ALPINE-X379

Shield Cans - TOP SIDE

T208 (U3900) - 806-06264

SH0412 SM
SHLD-FENCE-M8-X379

DIPLEXERS - 806-06266

SH0411 SM
SHLD-MLB-DIPLEXER-X379

NAND - TOP SOUTH (U9100) - 806-06262

SH0416 SM
SHLD-FENCE-MLB-NAND-TOP-SOUTH-X379

NAND - TOP NORTH (9220) - 806-06258

SH0413 SM
SHLD-FENCE-MLB-NAND-NORTH-X379

POGO PINS

LIO and RIO -2X (870-5071)

SH0471 POGO-2.00D-2.95H-SM SM
SH0472 POGO-2.00D-2.95H-SM SM

AROUND THE FAN AND CENTER - 8X (870-01518)

SH0463 POGO-2.30D-4.0H-SM SM
SH0464 POGO-2.30D-4.0H-SM SM
SH0465 POGO-2.30D-4.0H-SM SM
SH0466 POGO-2.30D-4.0H-SM SM
SH0467 POGO-2.30D-4.0H-SM SM
SH0468 POGO-2.30D-4.0H-SM SM
SH0469 POGO-2.30D-4.0H-SM SM
SH0470 POGO-2.30D-4.0H-SM SM

Cowling Bosses - BOTTOM SIDE

DFR TOUCH CONN (J4402) - 860-00414

SH0425 6.25X3.85R-1.75ID-1.938H-SM

USB-C CONN - LIO (J3300) - 860-00392

SH0445 3.40D1.75ID-1.12H-SM
SH0446 3.40D1.75ID-1.12H-SM

DFR DISPLAY CONN (J4401) - 860-00412

SH0426 3.40D1.75ID-1.7H-SM
SH0427 3.40D1.75ID-1.7H-SM

IPD CONN (J4501) - 860-00412

SH0428 3.40D1.75ID-1.7H-SM
SH0429 3.40D1.75ID-1.7H-SM

KBD CONN (J4500) - 860-00412

SH0430 3.40D1.75ID-1.7H-SM
SH0431 3.40D1.75ID-1.7H-SM

USB-C CONN - RIO (JB500) - 860-00392

SH0447 3.40D1.75ID-1.12H-SM
SH0448 3.40D1.75ID-1.12H-SM

AUDIO JACK CONN (J6600) - 860-00399

SH0432 3.3X1.8R-1.4ID-1.64H-SM

MESA CONN (J4900) - 860-00399

SH0433 3.3X1.8R-1.4ID-1.64H-SM

LIFEBOAT CONN (J9600) - 860-00413

SH0473 3.40D1.75ID-1.57H-SM
SH0474 3.40D1.75ID-1.57H-SM

Shield CAN Alignment Slots 14X - 998-04440 (1.2mm X 0.4mm)

SH0449 TH-NSP SL-1.2X0.4-1.5X0.7
SH0450 TH-NSP SL-1.2X0.4-1.5X0.7
SH0451 TH-NSP SL-1.2X0.4-1.5X0.7
SH0452 TH-NSP SL-1.2X0.4-1.5X0.7
SH0453 TH-NSP SL-1.2X0.4-1.5X0.7
SH0454 TH-NSP SL-1.2X0.4-1.5X0.7
SH0455 TH-NSP SL-1.2X0.4-1.5X0.7
SH0457 TH-NSP SL-1.2X0.4-1.5X0.7
SH0458 TH-NSP SL-1.2X0.4-1.5X0.7
SH0459 TH-NSP SL-1.2X0.4-1.5X0.7
SH0460 TH-NSP SL-1.2X0.4-1.5X0.7
SH0461 TH-NSP SL-1.2X0.4-1.5X0.7

Thermal Stage Mounting Holes

Plated Through Hole - 3.15mm - APN 998-0845

SH0490 3P9R3P15

Plated Through Hole - 3.6mm - APN 998-03850

SH0491 4.0R3.6-NSP
SH0492 4.0R3.6-NSP
SH0493 4.0R3.6-NSP

TOP Rubber Mount Standoffs - 12X - (860-00430)

SH0400 2.80D1.2ID-1.435H-SM
SH0401 2.80D1.2ID-1.435H-SM
SH0402 2.80D1.2ID-1.435H-SM
SH0403 2.80D1.2ID-1.435H-SM
SH0404 2.80D1.2ID-1.435H-SM
SH0405 2.80D1.2ID-1.435H-SM
SH0406 2.80D1.2ID-1.435H-SM
SH0407 2.80D1.2ID-1.435H-SM
SH0408 2.80D1.2ID-1.435H-SM
SH0409 2.80D1.2ID-1.435H-SM
SH0410 2.80D1.2ID-1.435H-SM
SH0436 2.80D1.2ID-1.435H-SM

Bottom Rubber Mount Standoffs - 1X - (860-00476)

SH0437 2.80D1.2ID-3.25H-SM

Cowling Bosses - TOP SIDE

eDP CONN (J8500) - 860-00415

SH0421 3.40D1.75ID-0.844H-SM
SH0422 3.40D1.75ID-0.844H-SM

BOM_COST_GROUP=MECHANICALS

SYNC_MASTER=LDUNN_J44 SYNC_DATE=01/13/2013

PAGE TITLE: PD Parts

Apple Inc.

DRAWING NUMBER: 051-00515 SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
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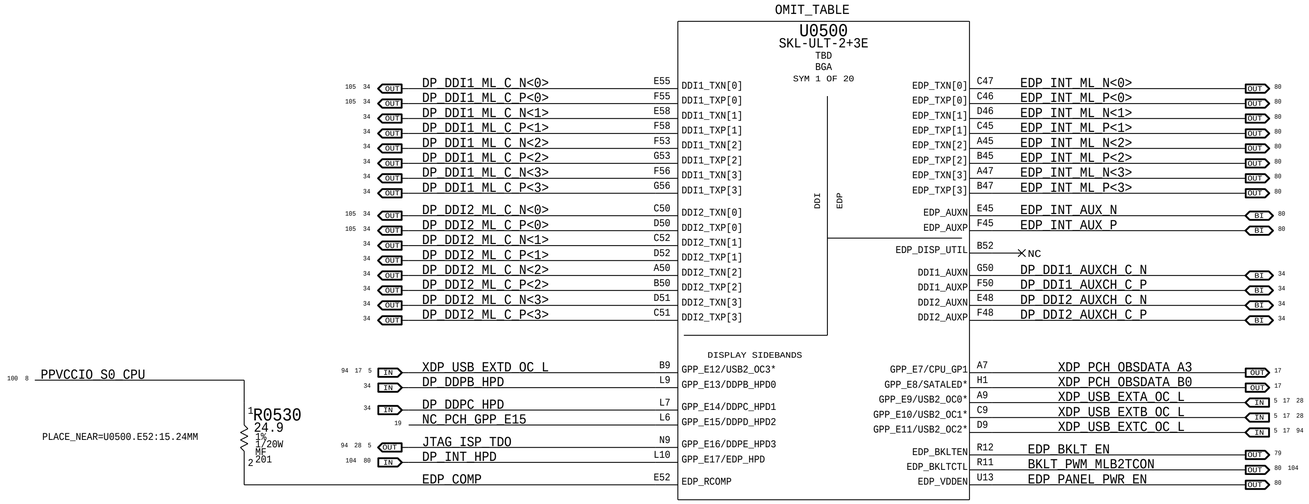

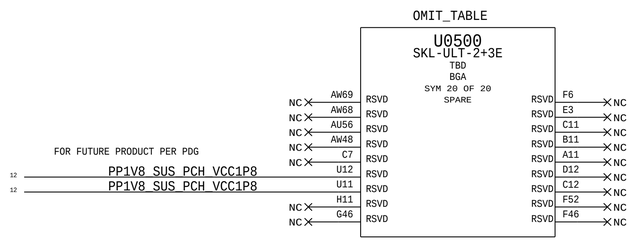

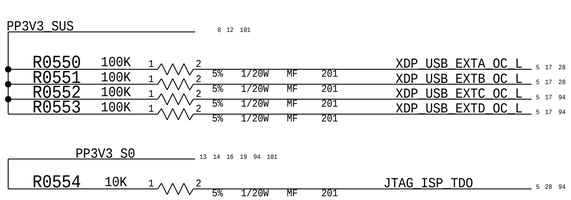

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DESIGN: X502/DEV_MLB_U
LAST CHANGE: Tue Apr 28 20:32:21 2015

PAGE TITLE
CPU GFX

Apple Inc.

DRAWING NUMBER	051-00515
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
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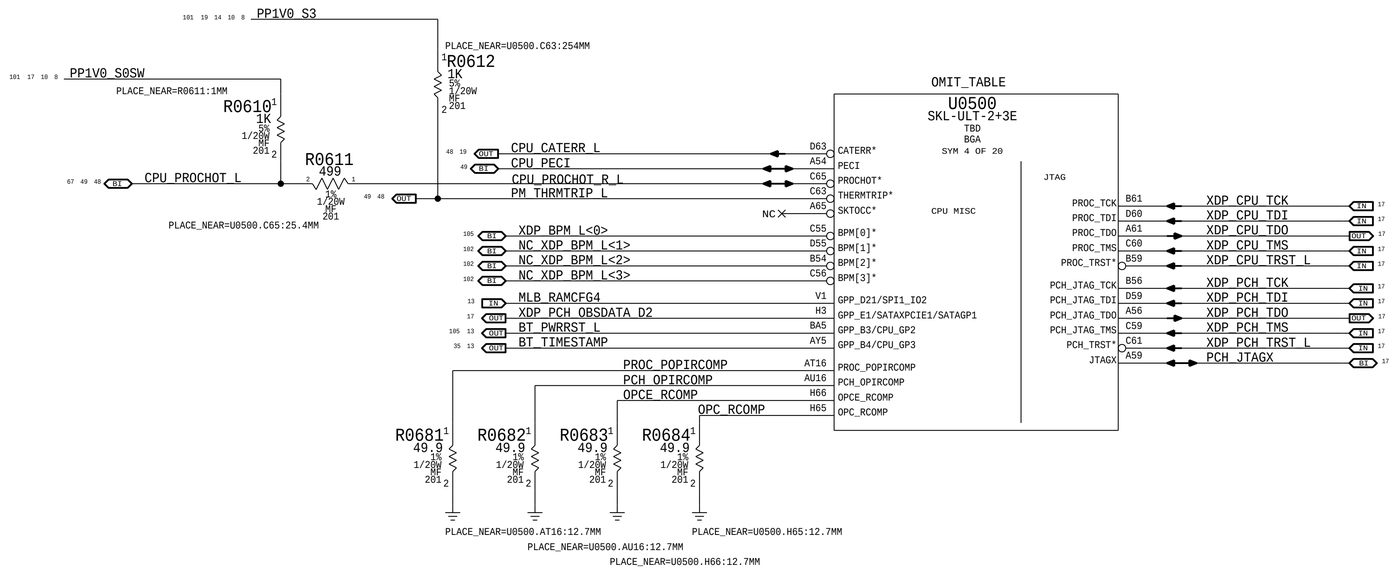

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LAST CHANGE: Mon Apr 27 22:56:39 2015

PAGE TITLE
CPU MISC/JTAG/CFG/RSVD

Apple Inc.

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OMIT_TABLE

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SKL-ULT-2+3E
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LPDDR3 NON-INTERLEAVED0

MEM_A_DQ<0>	AL71	DDR0_DQ[0]	DDR0_CKP[0]	AT53	MEM_A_CLK_P<0>
MEM_A_DQ<1>	AL68	DDR0_DQ[1]	DDR0_CKN[0]	AU53	MEM_A_CLK_N<0>
MEM_A_DQ<2>	AN68	DDR0_DQ[2]	DDR0_CKP[1]	AT55	MEM_A_CLK_P<1>
MEM_A_DQ<3>	AN69	DDR0_DQ[3]	DDR0_CKN[1]	AU55	MEM_A_CLK_N<1>
MEM_A_DQ<4>	AL70	DDR0_DQ[4]			
MEM_A_DQ<5>	AL69	DDR0_DQ[5]	DDR0_CKE[0]	BA56	MEM_A_CKE<0>
MEM_A_DQ<6>	AN70	DDR0_DQ[6]	DDR0_CKE[1]	BB56	MEM_A_CKE<1>
MEM_A_DQ<7>	AN71	DDR0_DQ[7]	DDR0_CKE[2]	AW56	MEM_A_CKE<2>
MEM_A_DQ<8>	AR70	DDR0_DQ[8]	DDR0_CKE[3]	AY56	MEM_A_CKE<3>
MEM_A_DQ<9>	AR68	DDR0_DQ[9]			
MEM_A_DQ<10>	AU71	DDR0_DQ[10]	DDR0_CS[0]*	AU45	MEM_A_CS_L<0>
MEM_A_DQ<11>	AU68	DDR0_DQ[11]	DDR0_CS[1]*	AU43	MEM_A_CS_L<1>
MEM_A_DQ<12>	AR71	DDR0_DQ[12]			
MEM_A_DQ<13>	AR69	DDR0_DQ[13]	DDR0_ODT[0]	AT45	MEM_A_ODT<0>
MEM_A_DQ<14>	AU70	DDR0_DQ[14]	DDR0_ODT[1]	AT43	NC
MEM_A_DQ<15>	AU69	DDR0_DQ[15]			
MEM_A_DQ<16>	AF65	DDR0_DQ[16]	DDR0_CAA[0]	BA51	MEM_A_CAA<0>
MEM_A_DQ<17>	AF64	DDR0_DQ[17]	DDR0_CAA[1]	BB54	MEM_A_CAA<1>
MEM_A_DQ<18>	AK65	DDR0_DQ[18]	DDR0_CAA[2]	BA52	MEM_A_CAA<2>
MEM_A_DQ<19>	AK64	DDR0_DQ[19]	DDR0_CAA[3]	AY52	MEM_A_CAA<3>
MEM_A_DQ<20>	AF66	DDR0_DQ[20]	DDR0_CAA[4]	AW52	MEM_A_CAA<4>
MEM_A_DQ<21>	AF67	DDR0_DQ[21]	DDR0_CAA[5]	AY55	MEM_A_CAA<5>
MEM_A_DQ<22>	AK67	DDR0_DQ[22]	DDR0_CAA[6]	AW54	MEM_A_CAA<6>
MEM_A_DQ<23>	AK66	DDR0_DQ[23]	DDR0_CAA[7]	BA54	MEM_A_CAA<7>
MEM_A_DQ<24>	AF70	DDR0_DQ[24]	DDR0_CAA[8]	BA55	MEM_A_CAA<8>
MEM_A_DQ<25>	AF68	DDR0_DQ[25]	DDR0_CAA[9]	AY54	MEM_A_CAA<9>
MEM_A_DQ<26>	AH71	DDR0_DQ[26]			
MEM_A_DQ<27>	AH68	DDR0_DQ[27]	DDR0_CAB[0]	AU46	MEM_A_CAB<0>
MEM_A_DQ<28>	AF71	DDR0_DQ[28]	DDR0_CAB[1]	AU48	MEM_A_CAB<1>
MEM_A_DQ<29>	AF69	DDR0_DQ[29]	DDR0_CAB[2]	AT46	MEM_A_CAB<2>
MEM_A_DQ<30>	AH70	DDR0_DQ[30]	DDR0_CAB[3]	AU50	MEM_A_CAB<3>
MEM_A_DQ<31>	AH69	DDR0_DQ[31]	DDR0_CAB[4]	AU52	MEM_A_CAB<4>
MEM_A_DQ<32>	BB65	DDR0_DQ[32]	DDR0_CAB[5]	AY51	MEM_A_CAB<5>
MEM_A_DQ<33>	AW65	DDR0_DQ[33]	DDR0_CAB[6]	AT48	MEM_A_CAB<6>
MEM_A_DQ<34>	AW63	DDR0_DQ[34]	DDR0_CAB[7]	AT50	MEM_A_CAB<7>
MEM_A_DQ<35>	AY63	DDR0_DQ[35]	DDR0_CAB[8]	BB50	MEM_A_CAB<8>
MEM_A_DQ<36>	BA65	DDR0_DQ[36]	DDR0_CAB[9]	AY50	MEM_A_CAB<9>
MEM_A_DQ<37>	AY65	DDR0_DQ[37]			
MEM_A_DQ<38>	BA63	DDR0_DQ[38]	DDR0_DQSN[0]	AM70	MEM_A_DQS_N<0>
MEM_A_DQ<39>	BB63	DDR0_DQ[39]	DDR0_DQSN[1]	AT69	MEM_A_DQS_N<1>
MEM_A_DQ<40>	BA61	DDR0_DQ[40]	DDR0_DQSN[2]	AH66	MEM_A_DQS_N<2>
MEM_A_DQ<41>	AW61	DDR0_DQ[41]	DDR0_DQSN[3]	AG69	MEM_A_DQS_N<3>
MEM_A_DQ<42>	BB59	DDR0_DQ[42]	DDR0_DQSN[4]	BA64	MEM_A_DQS_N<4>
MEM_A_DQ<43>	AW59	DDR0_DQ[43]	DDR0_DQSN[5]	AY60	MEM_A_DQS_N<5>
MEM_A_DQ<44>	BB61	DDR0_DQ[44]	DDR0_DQSN[6]	AR66	MEM_A_DQS_N<6>
MEM_A_DQ<45>	AY61	DDR0_DQ[45]	DDR0_DQSN[7]	AR61	MEM_A_DQS_N<7>
MEM_A_DQ<46>	BA59	DDR0_DQ[46]			
MEM_A_DQ<47>	AY59	DDR0_DQ[47]	DDR0_DQSP[0]	AM69	MEM_A_DQS_P<0>
MEM_A_DQ<48>	AT66	DDR0_DQ[48]	DDR0_DQSP[1]	AT70	MEM_A_DQS_P<1>
MEM_A_DQ<49>	AU66	DDR0_DQ[49]	DDR0_DQSP[2]	AH65	MEM_A_DQS_P<2>
MEM_A_DQ<50>	AP65	DDR0_DQ[50]	DDR0_DQSP[3]	AG70	MEM_A_DQS_P<3>
MEM_A_DQ<51>	AN65	DDR0_DQ[51]	DDR0_DQSP[4]	AY64	MEM_A_DQS_P<4>
MEM_A_DQ<52>	AN66	DDR0_DQ[52]	DDR0_DQSP[5]	BA60	MEM_A_DQS_P<5>
MEM_A_DQ<53>	AP66	DDR0_DQ[53]	DDR0_DQSP[6]	AR65	MEM_A_DQS_P<6>
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MEM_A_DQ<56>	AT61	DDR0_DQ[56]	DDR0_ALERT*	AW50	
MEM_A_DQ<57>	AU61	DDR0_DQ[57]	DDR0_PAR	AT52	NC
MEM_A_DQ<58>	AP60	DDR0_DQ[58]	DDR0_MA[3]	BA50	NC
MEM_A_DQ<59>	AN60	DDR0_DQ[59]	DDR0_MA[4]	BB52	NC
MEM_A_DQ<60>	AN61	DDR0_DQ[60]			
MEM_A_DQ<61>	AP61	DDR0_DQ[61]	DDR_VREF_CA	AY67	CPU_DIMM_VREFCA
MEM_A_DQ<62>	AT60	DDR0_DQ[62]	DDR0_VREF_DQ	AY68	CPU_DIMMA_VREFDQ
MEM_A_DQ<63>	AU60	DDR0_DQ[63]	DDR1_VREF_DQ	BA67	CPU_DIMMB_VREFDQ
			DDR_VTT_CNTL	AW67	PM_MEMVTT_EN

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
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LPDDR3 NON-INTERLEAVED

MEM_B_DQ<0>	AY39	DDR1_DQ[0]	DDR1_CKP[0]	AP45	MEM_B_CLK_P<0>
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MEM_B_DQ<2>	AY37	DDR1_DQ[2]	DDR1_CKP[1]	AP46	MEM_B_CLK_P<1>
MEM_B_DQ<3>	AW37	DDR1_DQ[3]	DDR1_CKN[1]	AN46	MEM_B_CLK_N<1>
MEM_B_DQ<4>	BB39	DDR1_DQ[4]			
MEM_B_DQ<5>	BA39	DDR1_DQ[5]	DDR1_CKE[0]	AN56	MEM_B_CKE<0>
MEM_B_DQ<6>	BA37	DDR1_DQ[6]	DDR1_CKE[1]	AP55	MEM_B_CKE<1>
MEM_B_DQ<7>	BB37	DDR1_DQ[7]	DDR1_CKE[2]	AN55	MEM_B_CKE<2>
MEM_B_DQ<8>	AY35	DDR1_DQ[8]	DDR1_CKE[3]	AP53	MEM_B_CKE<3>
MEM_B_DQ<9>	AW35	DDR1_DQ[9]			
MEM_B_DQ<10>	AY33	DDR1_DQ[10]	DDR1_CS[0]*	BB42	MEM_B_CS_L<0>
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MEM_B_DQ<22>	AP37	DDR1_DQ[22]	DDR1_CAA[6]	AN50	MEM_B_CAA<6>
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MEM_B_DQ<25>	AU33	DDR1_DQ[25]	DDR1_CAA[9]	AN52	MEM_B_CAA<9>
MEM_B_DQ<26>	AU30	DDR1_DQ[26]			
MEM_B_DQ<27>	AT30	DDR1_DQ[27]	DDR1_CAB[0]	BA43	MEM_B_CAB<0>
MEM_B_DQ<28>	AR33	DDR1_DQ[28]	DDR1_CAB[1]	AY43	MEM_B_CAB<1>
MEM_B_DQ<29>	AP33	DDR1_DQ[29]	DDR1_CAB[2]	AY44	MEM_B_CAB<2>
MEM_B_DQ<30>	AR30	DDR1_DQ[30]	DDR1_CAB[3]	AW44	MEM_B_CAB<3>
MEM_B_DQ<31>	AP30	DDR1_DQ[31]	DDR1_CAB[4]	BB44	MEM_B_CAB<4>
MEM_B_DQ<32>	AY31	DDR1_DQ[32]	DDR1_CAB[5]	AY47	MEM_B_CAB<5>
MEM_B_DQ<33>	AW31	DDR1_DQ[33]	DDR1_CAB[6]	BA44	MEM_B_CAB<6>
MEM_B_DQ<34>	AY29	DDR1_DQ[34]	DDR1_CAB[7]	AW46	MEM_B_CAB<7>
MEM_B_DQ<35>	AW29	DDR1_DQ[35]	DDR1_CAB[8]	AY46	MEM_B_CAB<8>
MEM_B_DQ<36>	BB31	DDR1_DQ[36]	DDR1_CAB[9]	BA46	MEM_B_CAB<9>
MEM_B_DQ<37>	BA31	DDR1_DQ[37]			
MEM_B_DQ<38>	BA29	DDR1_DQ[38]	DDR1_DQSN[0]	BA38	MEM_B_DQS_N<0>
MEM_B_DQ<39>	BB29	DDR1_DQ[39]	DDR1_DQSN[1]	AY34	MEM_B_DQS_N<1>
MEM_B_DQ<40>	AY27	DDR1_DQ[40]	DDR1_DQSN[2]	AT38	MEM_B_DQS_N<2>
MEM_B_DQ<41>	AW27	DDR1_DQ[41]	DDR1_DQSN[3]	AT32	MEM_B_DQS_N<3>
MEM_B_DQ<42>	AY25	DDR1_DQ[42]	DDR1_DQSN[4]	BA30	MEM_B_DQS_N<4>
MEM_B_DQ<43>	AW25	DDR1_DQ[43]	DDR1_DQSN[5]	AY26	MEM_B_DQS_N<5>
MEM_B_DQ<44>	BB27	DDR1_DQ[44]	DDR1_DQSN[6]	AR25	MEM_B_DQS_N<6>
MEM_B_DQ<45>	BA27	DDR1_DQ[45]	DDR1_DQSN[7]	AR22	MEM_B_DQS_N<7>
MEM_B_DQ<46>	BA25	DDR1_DQ[46]			
MEM_B_DQ<47>	BB25	DDR1_DQ[47]	DDR1_DQSP[0]	AY38	MEM_B_DQS_P<0>
MEM_B_DQ<48>	AU27	DDR1_DQ[48]	DDR1_DQSP[1]	BA34	MEM_B_DQS_P<1>
MEM_B_DQ<49>	AT27	DDR1_DQ[49]	DDR1_DQSP[2]	AR38	MEM_B_DQS_P<2>
MEM_B_DQ<50>	AT25	DDR1_DQ[50]	DDR1_DQSP[3]	AR32	MEM_B_DQS_P<3>
MEM_B_DQ<51>	AU25	DDR1_DQ[51]	DDR1_DQSP[4]	AY30	MEM_B_DQS_P<4>
MEM_B_DQ<52>	AP27	DDR1_DQ[52]	DDR1_DQSP[5]	BA26	MEM_B_DQS_P<5>
MEM_B_DQ<53>	AN27	DDR1_DQ[53]	DDR1_DQSP[6]	AR27	MEM_B_DQS_P<6>
MEM_B_DQ<54>	AN25	DDR1_DQ[54]	DDR1_DQSP[7]	AR21	MEM_B_DQS_P<7>
MEM_B_DQ<55>	AP25	DDR1_DQ[55]			
MEM_B_DQ<56>	AT22	DDR1_DQ[56]	DDR1_ALERT*	AN43	
MEM_B_DQ<57>	AU22	DDR1_DQ[57]	DDR1_PAR	AP43	NC
MEM_B_DQ<58>	AU21	DDR1_DQ[58]	DDR1_MA[3]	BB46	NC
MEM_B_DQ<59>	AT21	DDR1_DQ[59]	DDR1_MA[4]	BA47	NC
MEM_B_DQ<60>	AN22	DDR1_DQ[60]			
MEM_B_DQ<61>	AP22	DDR1_DQ[61]	DRAM_RESET*	AT13	NC
MEM_B_DQ<62>	AP21	DDR1_DQ[62]	DDR_RCOMP[0]	AR18	CPU_DDR_RCOMP<0>
MEM_B_DQ<63>	AN21	DDR1_DQ[63]	DDR_RCOMP[1]	AT18	CPU_DDR_RCOMP<1>
			DDR_RCOMP[2]	AU18	CPU_DDR_RCOMP<2>

R0700 162 1% 1/20W MF 201 — PLACE_NEAR=U0500.AU18:6MM
R0701 80.6 1% 1/20W MF 201 — PLACE_NEAR=U0500.AT18:6MM
R0702 200 1% 1/20W MF 201 — PLACE_NEAR=U0500.AR18:6MM

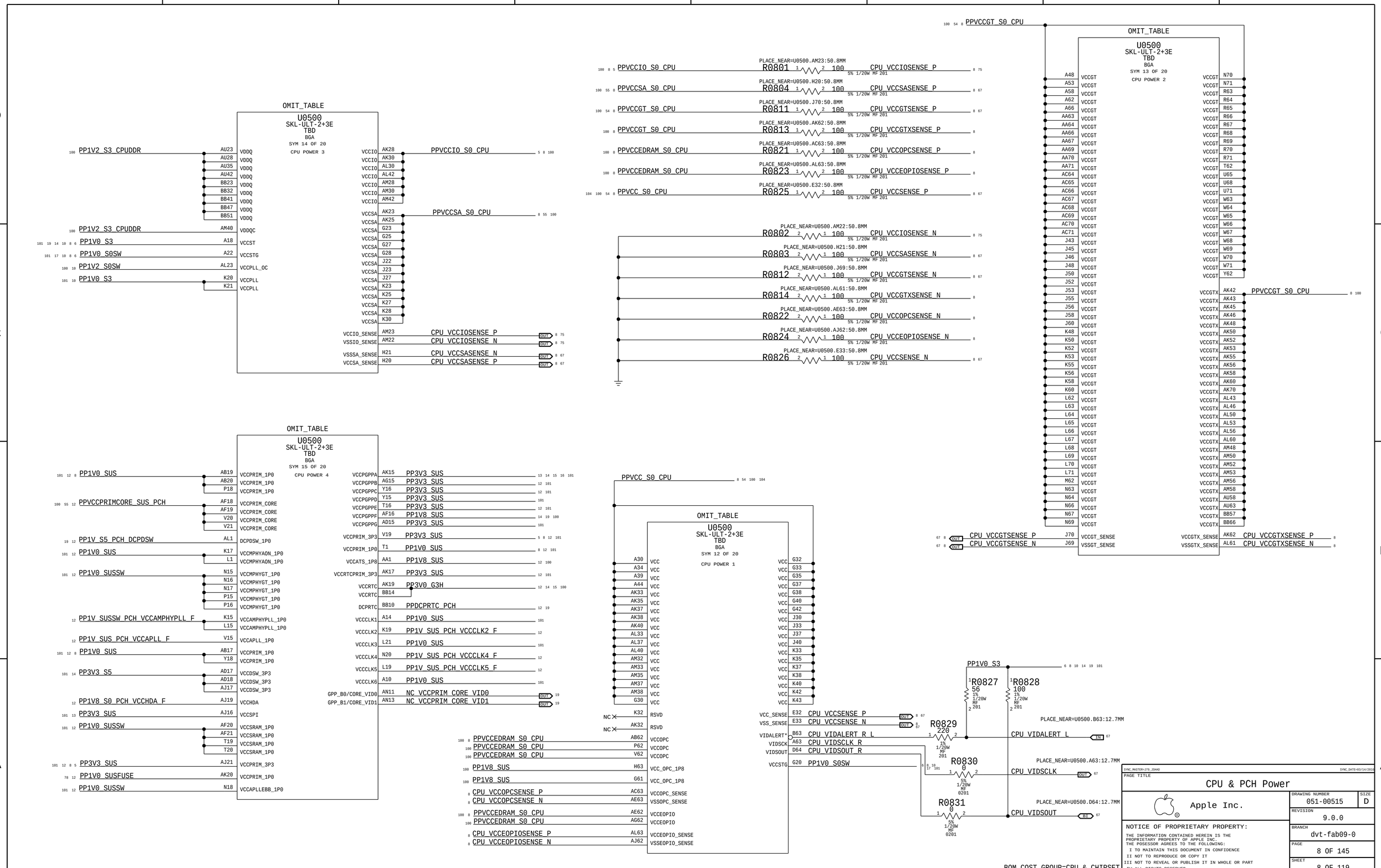
BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J52_MLB SYNC_DATE=05/12/2015

PAGE TITLE: CPU LPDDR3 Interface

Apple Inc.

DRAWING NUMBER: 051-00515 SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 7 OF 145
SHEET: 7 OF 119



OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 16 OF 20
GND1

102 NC_CPU_NCTFVSS_A5	A5 VSS	VSS AL65	
	A67 VSS	VSS AL66	
102 NC_CPU_NCTFVSS_A70	A70 VSS	VSS AM13	
	AA2 VSS	VSS AM21	
	AA4 VSS	VSS AM25	
	AA65 VSS	VSS AM27	
	AA68 VSS	VSS AM43	
	AB15 VSS	VSS AM45	
	AB16 VSS	VSS AM46	
	AB18 VSS	VSS AM55	
	AB21 VSS	VSS AM60	
	AB8 VSS	VSS AM61	
	AD13 VSS	VSS AM68	
	AD16 VSS	VSS AM71	
	AD19 VSS	VSS AM8	
	AD20 VSS	VSS AN20	
	AD21 VSS	VSS AN23	
	AD62 VSS	VSS AN28	
	AD8 VSS	VSS AN30	
	AE64 VSS	VSS AN32	
	AE65 VSS	VSS AN33	
	AE66 VSS	VSS AN35	
	AE67 VSS	VSS AN37	
	AE68 VSS	VSS AN38	
	AE69 VSS	VSS AN40	
	AF1 VSS	VSS AN42	
	AF10 VSS	VSS AN58	
	AF15 VSS	VSS AN63	
	AF17 VSS	VSS AP10	
	AF2 VSS	VSS AP18	
	AF4 VSS	VSS AP20	
	AF63 VSS	VSS AP23	
	AG16 VSS	VSS AP28	
	AG17 VSS	VSS AP32	
	AG18 VSS	VSS AP35	
	AG19 VSS	VSS AP38	
	AG20 VSS	VSS AP42	
	AG21 VSS	VSS AP58	
	AG71 VSS	VSS AP63	
	AH13 VSS	VSS AP68	
	AH6 VSS	VSS AP70	
	AH63 VSS	VSS AR11	
	AH64 VSS	VSS AR15	
	AH67 VSS	VSS AR16	
	AJ15 VSS	VSS AR20	
	AJ18 VSS	VSS AR23	
	AJ20 VSS	VSS AR28	
	AJ4 VSS	VSS AR35	
	AK11 VSS	VSS AR42	
	AK16 VSS	VSS AR43	
	AK18 VSS	VSS AR45	
	AK21 VSS	VSS AR46	
	AK22 VSS	VSS AR48	
	AK27 VSS	VSS AR5	
	AK63 VSS	VSS AR50	
	AK68 VSS	VSS AR52	
	AK69 VSS	VSS AR53	
	AK8 VSS	VSS AR55	
	AL2 VSS	VSS AR58	
	AL28 VSS	VSS AR63	
	AL32 VSS	VSS AR8	
	AL35 VSS	VSS AT2	
	AL38 VSS	VSS AT20	
	AL4 VSS	VSS AT23	
	AL45 VSS	VSS AT28	
	AL48 VSS	VSS AT35	
	AL52 VSS	VSS AT4	
	AL55 VSS	VSS AT42	
	AL58 VSS	VSS AT56	
	AL64 VSS	VSS AT58	

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 17 OF 20
GND2

	AT63 VSS	VSS BA49	
	AT68 VSS	VSS BA53	
	AT71 VSS	VSS BA57	
	AU10 VSS	VSS BA6	
	AU15 VSS	VSS BA62	
	AU20 VSS	VSS BA66	
	AU32 VSS	VSS BA71	NC_CPU_NCTFVSS_BA71 102
	AU38 VSS	VSS BB18	
102 NC_CPU_NCTFVSS_AV1	AV1 VSS	VSS BB26	
	AV68 VSS	VSS BB30	
	AV69 VSS	VSS BB34	
	AV70 VSS	VSS BB38	
	AV71 VSS	VSS BB43	
	AW10 VSS	VSS BB55	
	AW12 VSS	VSS BB6	
	AW14 VSS	VSS BB60	
	AW16 VSS	VSS BB64	
	AW18 VSS	VSS BB67	
	AW21 VSS	VSS BB70	NC_CPU_NCTFVSS_BB70 102
	AW23 VSS	VSS C1	NC_CPU_NCTFVSS_C1 102
	AW26 VSS	VSS C25	
	AW28 VSS	VSS C5	
	AW30 VSS	VSS D10	
	AW32 VSS	VSS D11	
	AW34 VSS	VSS D14	
	AW36 VSS	VSS D18	
	AW38 VSS	VSS D22	
	AW41 VSS	VSS D25	
	AW43 VSS	VSS D26	
	AW45 VSS	VSS D30	
	AW47 VSS	VSS D34	
	AW49 VSS	VSS D39	
	AW51 VSS	VSS D44	
	AW53 VSS	VSS D45	
	AW55 VSS	VSS D47	
	AW57 VSS	VSS D48	
	AW6 VSS	VSS D53	
	AW60 VSS	VSS D58	
	AW62 VSS	VSS D6	
	AW64 VSS	VSS D62	
	AW66 VSS	VSS D66	
	AW8 VSS	VSS D69	
	AY66 VSS	VSS E11	
	B10 VSS	VSS E15	
	B14 VSS	VSS E18	
	B18 VSS	VSS E21	
	B22 VSS	VSS E46	
	B30 VSS	VSS E50	
	B34 VSS	VSS E53	
	B39 VSS	VSS E56	
	B44 VSS	VSS E6	
	B48 VSS	VSS E65	
	B53 VSS	VSS E71	
	B58 VSS	VSS F1	
	B62 VSS	VSS F13	
	B66 VSS	VSS F2	
102 NC_CPU_NCTFVSS_B71	B71 VSS	VSS F22	
102 NC_CPU_NCTFVSS_BA1	BA1 VSS	VSS F23	
	BA10 VSS	VSS F27	
	BA14 VSS	VSS F28	
	BA18 VSS	VSS F32	
	BA2 VSS	VSS F33	
	BA23 VSS	VSS F35	
	BA28 VSS	VSS F37	
	BA32 VSS	VSS F38	
	BA36 VSS	VSS F4	
	F68 VSS	VSS F40	
	BA45 VSS	VSS F42	
		VSS BA41	

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 18 OF 20
GND 3

F8 VSS	VSS L18	
G10 VSS	VSS L2	
G22 VSS	VSS L20	
G43 VSS	VSS L4	
G45 VSS	VSS L8	
G48 VSS	VSS N10	
G5 VSS	VSS N13	
G52 VSS	VSS N19	
G55 VSS	VSS N21	
G58 VSS	VSS N6	
G6 VSS	VSS N65	
G60 VSS	VSS N68	
G63 VSS	VSS P17	
G66 VSS	VSS P19	
H15 VSS	VSS P20	
H18 VSS	VSS P21	
H71 VSS	VSS R13	
J11 VSS	VSS R6	
J13 VSS	VSS T15	
J25 VSS	VSS T17	
J28 VSS	VSS T18	
J32 VSS	VSS T2	
J35 VSS	VSS T21	
J38 VSS	VSS T4	
J42 VSS	VSS U10	
J8 VSS	VSS U63	
K16 VSS	VSS U64	
K18 VSS	VSS U66	
K22 VSS	VSS U67	
K61 VSS	VSS U69	
K63 VSS	VSS U70	
K64 VSS	VSS V16	
K65 VSS	VSS V17	
K66 VSS	VSS V18	
K67 VSS	VSS W13	
K68 VSS	VSS W6	
K70 VSS	VSS W9	
K71 VSS	VSS Y17	
L11 VSS	VSS Y19	
L16 VSS	VSS Y20	
L17 VSS	VSS Y21	

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J79_ALFRED SYNC_DATE=05/12/2015

PAGE TITLE

CPU & PCH Grounds

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

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BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J79_JSHAO SYNC_DATE=08/28/2015

PAGE TITLE

CPU Core Decoupling

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

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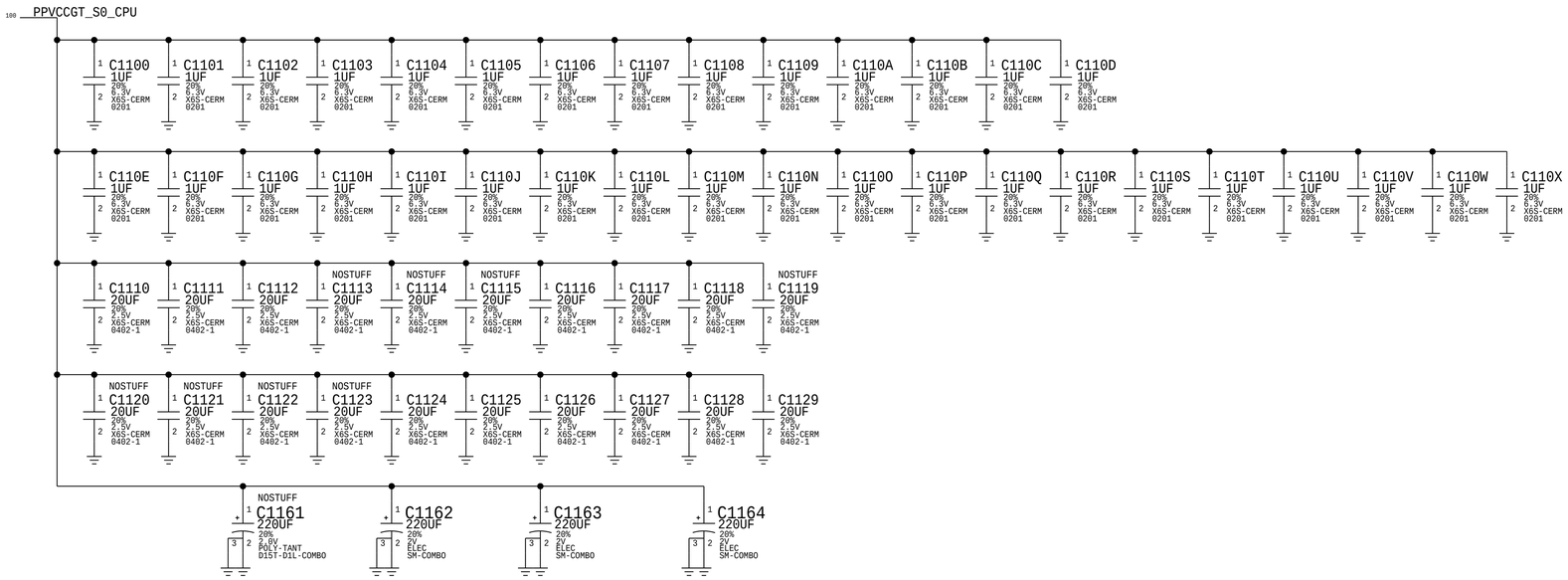

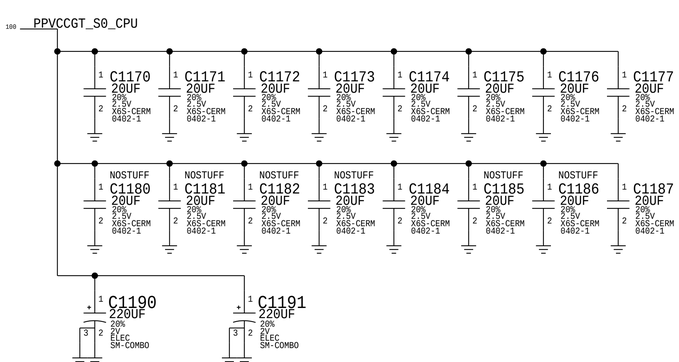

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PAGE TITLE
CPU GT Decoupling

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

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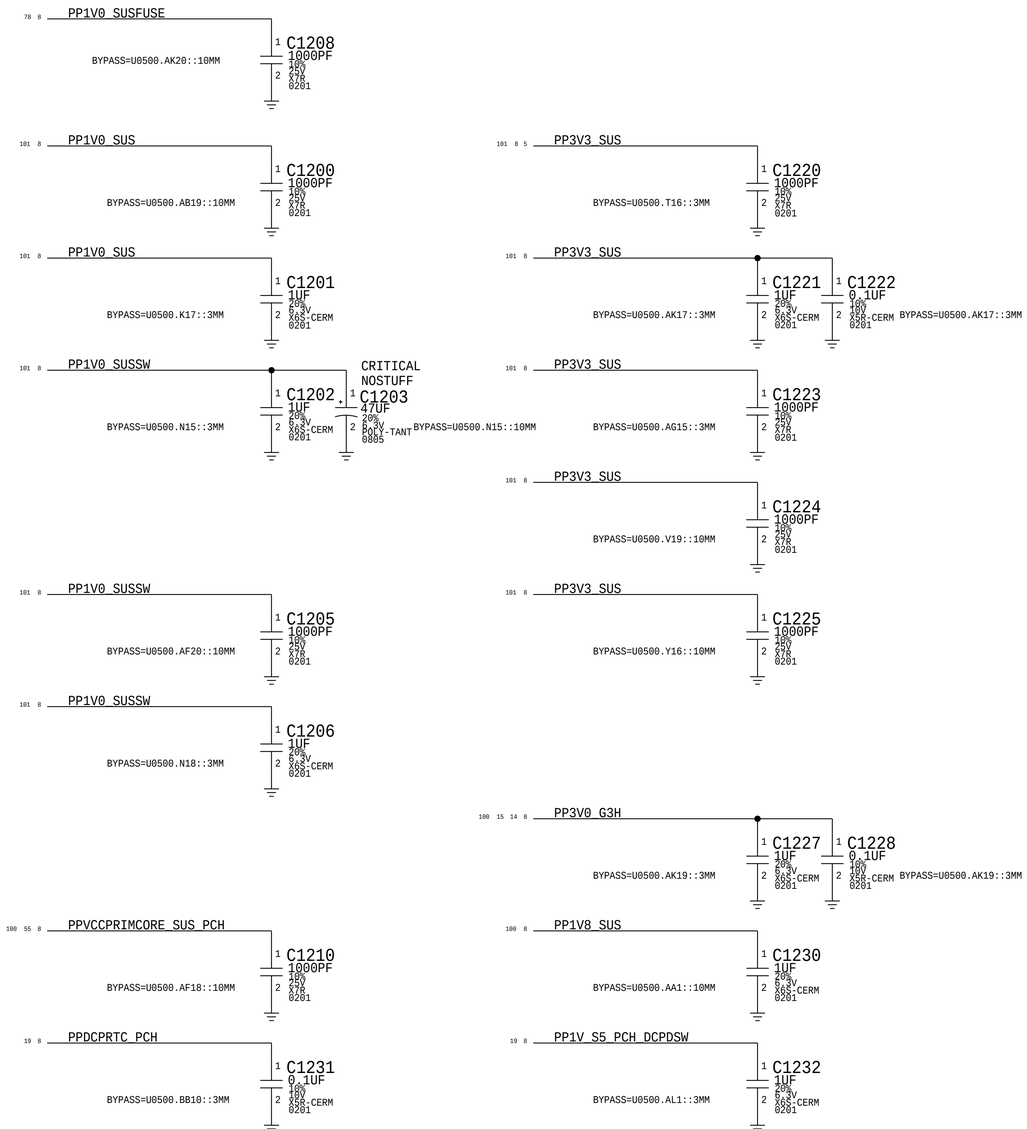
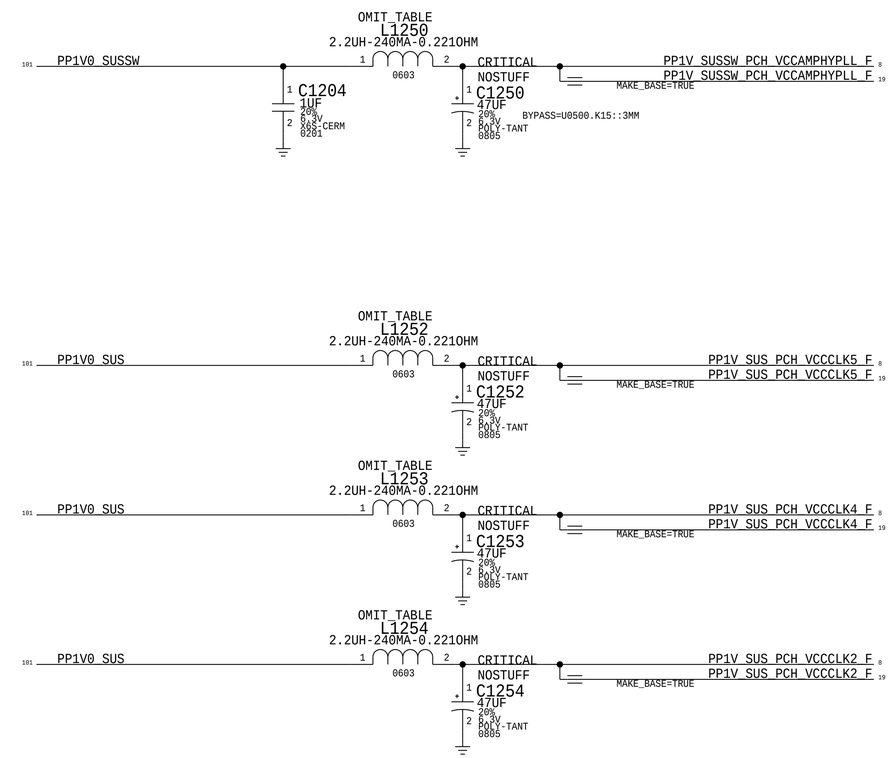
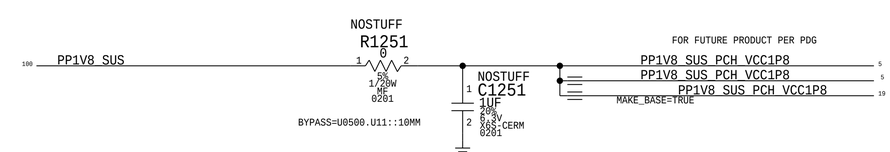


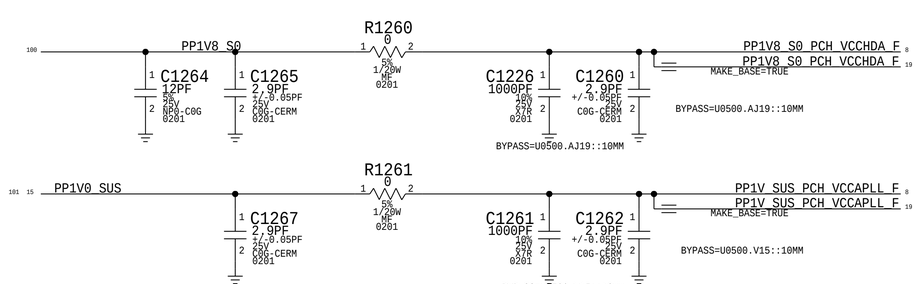
FILTER PLACEHOLDERS ONLY

RAIL SIDE PCH SIDE



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	4	RES,MF,1A MAX,0OHM,5%,0603	L1250,L1252,L1253,L1254		





BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
PCH Decoupling

Apple Inc.

DRAWING NUMBER 051-00515
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
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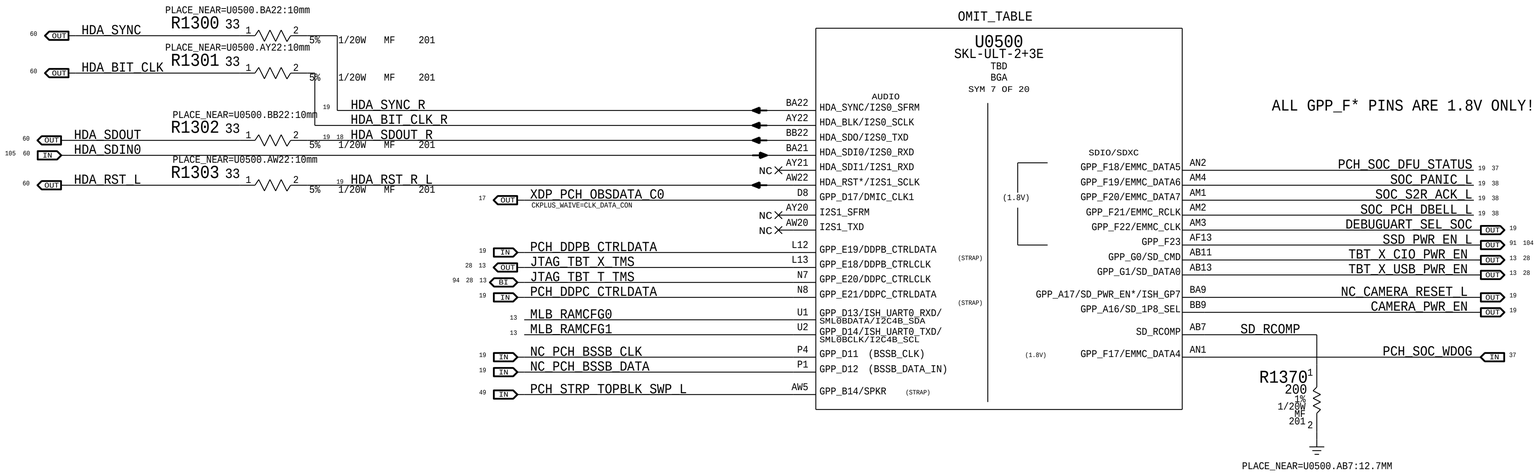
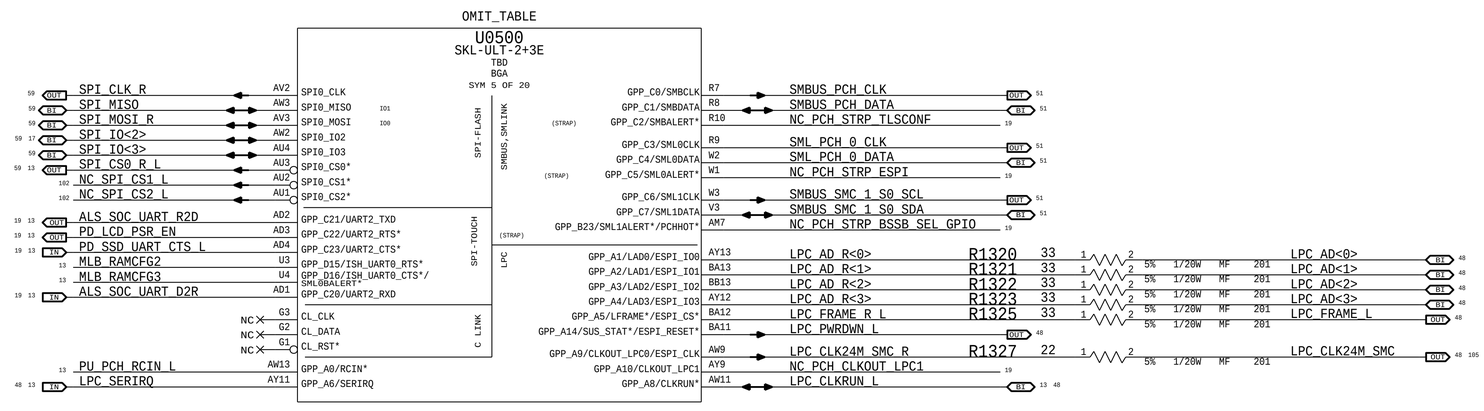
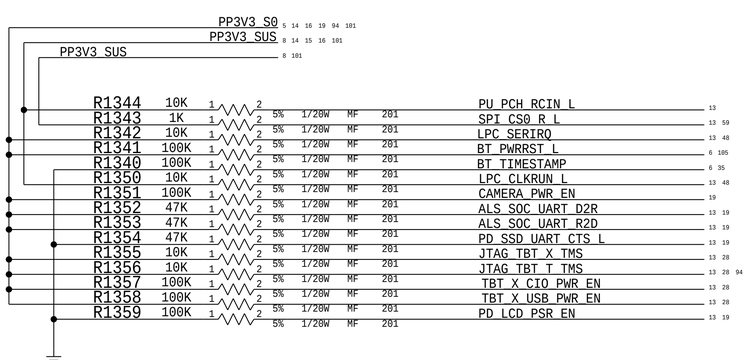
SHEET 12 OF 119

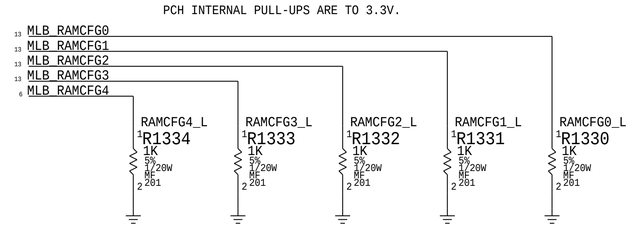






MEMORY CONFIGURATION STRAPS.

PCH INTERNAL PULL-UPS ARE TO 3.3V.



BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG4_L,RAMCFG3_L,RAMCFG2_L,RAMCFG1_L,RAMCFG0_L

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB
LAST CHANGE: Tue Feb 2 13:18:21 2016

PAGE TITLE
PCH Audio/LPC/SPI/SMBus

Apple Inc.

DRAWING NUMBER 051-00515
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
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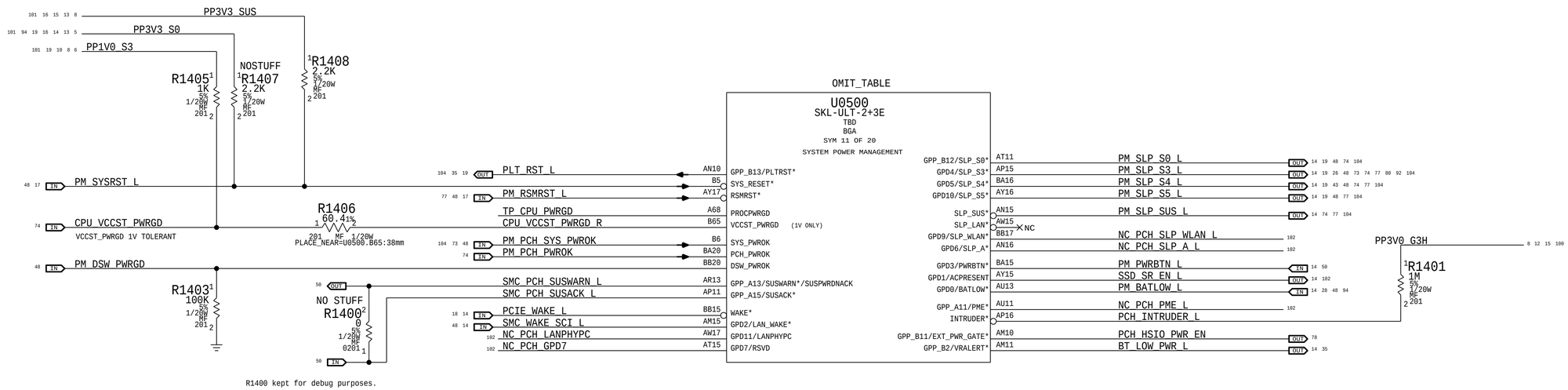
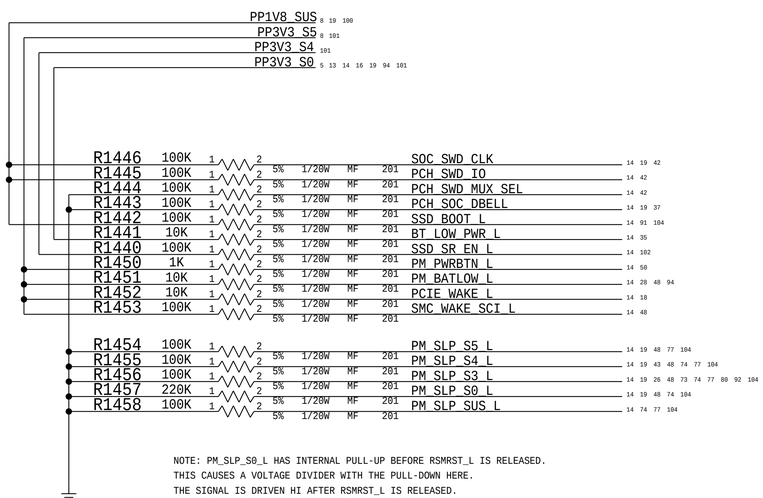
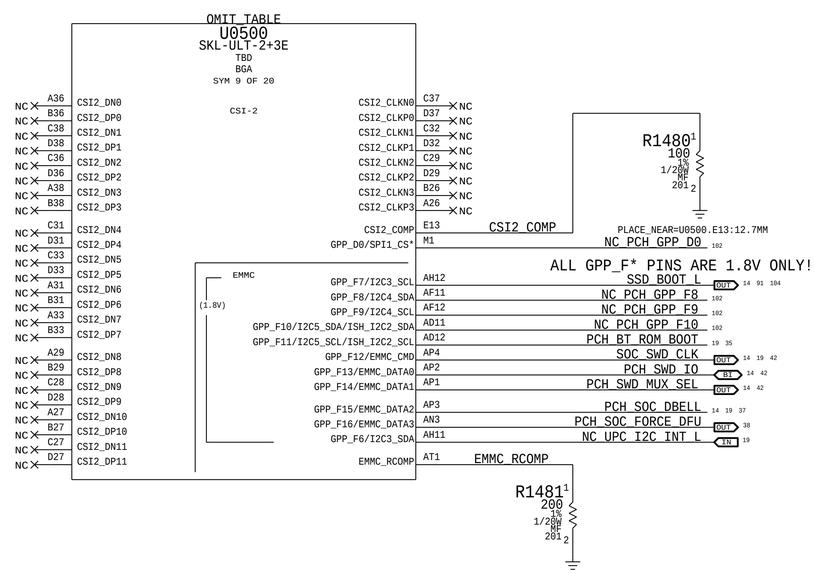
PCH Reset Button



R1400 kept for debug purposes.



NOTE: PM_SLP_S0_L HAS INTERNAL PULL-UP BEFORE RSMRST_L IS RELEASED.
THIS CAUSES A VOLTAGE DIVIDER WITH THE PULL-DOWN HERE.
THE SIGNAL IS DRIVEN HI AFTER RSMRST_L IS RELEASED.



BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB
LAST CHANGE: Tue May 3 17:45:28 2016

PAGE TITLE
PCH Power Management

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
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PCIe Port Assignments:

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U0500
SKL-ULT-2+3E
TBD
BGA
SYM 8 OF 20

SSD LANE 0
- PCIE SSD D2R N<0> — H13 PCIE1_RXN/USB3_5_RXN
- PCIE SSD D2R P<0> — G13 PCIE1_RXP/USB3_5_RXP
- PCIE SSD R2D C N<0> — B17 PCIE1_TXN/USB3_5_TXN
- PCIE SSD R2D C P<0> — A17 PCIE1_TXP/USB3_5_TXP

SSD LANE 1
- PCIE SSD D2R N<1> — G11 PCIE2_RXN/USB3_6_RXN
- PCIE SSD D2R P<1> — F11 PCIE2_RXP/USB3_6_RXP
- PCIE SSD R2D C N<1> — D16 PCIE2_TXN/USB3_6_TXN
- PCIE SSD R2D C P<1> — C16 PCIE2_TXP/USB3_6_TXP

SSD LANE 2
- PCIE SSD D2R N<2> — H16 PCIE3_RXN
- PCIE SSD D2R P<2> — G16 PCIE3_RXP
- PCIE SSD R2D C N<2> — D17 PCIE3_TXN
- PCIE SSD R2D C P<2> — C17 PCIE3_TXP

SSD LANE 3
- PCIE SSD D2R N<3> — G15 PCIE4_RXN
- PCIE SSD D2R P<3> — F15 PCIE4_RXP
- PCIE SSD R2D C N<3> — B19 PCIE4_TXN
- PCIE SSD R2D C P<3> — A19 PCIE4_TXP

Thunderbolt X lane 0
- PCIE TBT X D2R N<0> — F16 PCIE5_RXN
- PCIE TBT X D2R P<0> — E16 PCIE5_RXP
- PCIE TBT X R2D C N<0> — C19 PCIE5_TXN
- PCIE TBT X R2D C P<0> — D19 PCIE5_TXP

Thunderbolt X lane 1
- PCIE TBT X D2R N<1> — G18 PCIE6_RXN
- PCIE TBT X D2R P<1> — F18 PCIE6_RXP
- PCIE TBT X R2D C N<1> — D20 PCIE6_TXN
- PCIE TBT X R2D C P<1> — C20 PCIE6_TXP

Thunderbolt X lane 2
- PCIE TBT X D2R N<2> — F20 PCIE7_RXN/SATA0_RXN
- PCIE TBT X D2R P<2> — E20 PCIE7_RXP/SATA0_RXP
- PCIE TBT X R2D C N<2> — B21 PCIE7_TXN/SATA0_TXN
- PCIE TBT X R2D C P<2> — A21 PCIE7_TXP/SATA0_TXP

Thunderbolt X lane 3
- PCIE TBT X D2R N<3> — G21 PCIE8_RXN/SATA1A_RXN
- PCIE TBT X D2R P<3> — F21 PCIE8_RXP/SATA1A_RXP
- PCIE TBT X R2D C N<3> — D21 PCIE8_TXN/SATA1A_TXN
- PCIE TBT X R2D C P<3> — C21 PCIE8_TXP/SATA1A_TXP

AirPort
- PCIE AP D2R N — E22 PCIE9_RXN
- PCIE AP D2R P — E23 PCIE9_RXP
- PCIE AP R2D C N — B23 PCIE9_TXN
- PCIE AP R2D C P — A23 PCIE9_TXP

CAMERA
- NC PCIE CAMERA D2R N — F25 PCIE10_RXN
- NC PCIE CAMERA D2R P — E25 PCIE10_RXP
- NC PCIE CAMERA R2D C N — D23 PCIE10_TXN
- NC PCIE CAMERA R2D C P — C23 PCIE10_TXP

PLACE_NEAR=U0500.F5:12.7mm
R1504 100 1% 1/20W MF 201

- PCH PCIE RCOMP N — F5 PCIE_RCOMPN
- PCH PCIE RCOMP P — E5 PCIE_RCOMPP
- XDP CPU PRDY L — D56 PROC_PRDY*
- XDP CPU PREQ L — D61 PROC_PREQ*
- SMC RUNTIME SCI L — BB11 GPP_A7/PIRQA*

Thunderbolt T lane 0
- PCIE TBT T D2R N<0> — E28 PCIE11_RXN/SATA1B_RXN
- PCIE TBT T D2R P<0> — E27 PCIE11_RXP/SATA1B_RXP
- PCIE TBT T R2D C N<0> — D24 PCIE11_TXN/SATA1B_TXN
- PCIE TBT T R2D C P<0> — C24 PCIE11_TXP/SATA1B_TXP

Thunderbolt T lane 1
- PCIE TBT T D2R N<1> — E30 PCIE12_RXN/SATA2_RXN
- PCIE TBT T D2R P<1> — F30 PCIE12_RXP/SATA2_RXP
- PCIE TBT T R2D C N<1> — A25 PCIE12_TXN/SATA2_TXN
- PCIE TBT T R2D C P<1> — B25 PCIE12_TXP/SATA2_TXP

SSIC/USB3
- USB3_1_RXN — H8 USB3 EXTA D2R N
- USB3_1_RXP — G8 USB3 EXTA D2R P
- USB3_1_TXN — C13 USB3 EXTA R2D C N
- USB3_1_TXP — D13 USB3 EXTA R2D C P

EXT A (SS,DCI)

- USB3_2_RXN/SSIC_RXN — J6 NC USB3 EXTB D2R N
- USB3_2_RXP/SSIC_RXP — H6 NC USB3 EXTB D2R P
- USB3_2_TXN/SSIC_TXN — B13 NC USB3 EXTB R2D C N
- USB3_2_TXP/SSIC_TXP — A13 NC USB3 EXTB R2D C P

EXT B (SS)

- USB3_3_RXN — J10 TP USB3 03 D2RN
- USB3_3_RXP — H10 TP USB3 03 D2RP
- USB3_3_TXN — B15 TP USB3 03 R2DN
- USB3_3_TXP — A15 TP USB3 03 R2DP
- USB3_4_RXN — E10 NC USB3 04 D2RN
- USB3_4_RXP — F10 NC USB3 04 D2RP
- USB3_4_TXN — C15 NC USB3 04 R2DN
- USB3_4_TXP — D15 NC USB3 04 R2DP

USB2
- USB2N_1 — AB9 NC USB EXTA N
- USB2P_1 — AB10 NC USB EXTA P

EXT A (LS/FS/HS)

- USB2N_2 — AD6 NC USB EXTB N
- USB2P_2 — AD7 NC USB EXTB P

EXT B (LS/FS/HS)

- USB2N_3 — AH3 USB CAMERA DFR N
- USB2P_3 — AJ3 USB CAMERA DFR P
- USB2N_4 — AD9 TP USB TESTERN
- USB2P_4 — AD10 TP USB TESTERP
- USB2N_5 — AJ1 NC USB2 05N
- USB2P_5 — AJ2 NC USB2 05P
- USB2N_6 — AF6 USB UPC PCH XA N
- USB2P_6 — AF7 USB UPC PCH XA P
- USB2N_7 — AH1 USB UPC PCH TA N
- USB2P_7 — AH2 USB UPC PCH TA P
- USB2N_8 — AF8 USB UPC PCH XB N
- USB2P_8 — AF9 USB UPC PCH XB P
- USB2N_9 — AG1 USB UPC PCH TB N
- USB2P_9 — AG2 USB UPC PCH TB P
- USB2N_10 — AH7 NC USB2 10N
- USB2P_10 — AH8 NC USB2 10P
- USB2_COMP — AB6 PCH USB2 COMP
- USB2_ID — AG3
- USB2_VBUSSENSE — AG4 PCH USB2 VBUSSENSE

GROUNDED PER SKYLAKE MOW 2015WW10.

R1501 113 1% 1/20W MF 201
PLACE_NEAR=U0500.AB6:12.7MM

R1503 1K 5% 1/20W MF 201
PLACE_NEAR=U0500.AG4:12.7MM

PCIE/USB3/SATA
- GPP_E3/CPU_GP0 — A6 XDP PCH OBSFN C1
- GPP_E4/DEVSLP0 — J1 XDP JTAG ISP TCK
- GPP_E5/DEVSLP1 — J2 XDP JTAG ISP TDI
- GPP_E6/DEVSLP2 — J3 XDP PCH OBSDATA A2
- GPP_D22/SPI1_IO3 — V2 NC SPKR ID0
- GPP_D23/I2S_MCLK — J5 XDP PCH OBSDATA D0 (CKPLUS_WAIVE=CLK_DATA_CON)
- GPP_E0/SATAXPCIE0/SATAGP0 — H2 XDP PCH OBSDATA D1
- GPP_D18/DMIC_DATA1 — C8 XDP PCH OBSDATA C1
- GPP_D19/DMIC_CLK0 — H5 XDP PCH OBSDATA C2 (CKPLUS_WAIVE=CLK_DATA_CON)
- GPP_D20/DMIC_DATA0 — D7 XDP PCH OBSDATA C3
- GPP_E2/SATAXPCIE2/SATAGP2 — G4 XDP PCH OBSDATA D3

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 10 OF 20

CLOCK SIGNALS

ANY CLKREQ CAN MAP TO ANY CLK.
ANY CLKREQ OR CLK CAN MAP TO ANY PCIE PORT.
UNUSED CLKREQS AND CLKS SHOULD BE DISABLED.
PER SKYLAKE PDG, SKYLAKE PCH EDS.

- PCIE CLK100M SSD N — D42 CLKOUT_PCIE_N0
- PCIE CLK100M SSD P — C42 CLKOUT_PCIE_P0
- SSD CLKREQ L R — AR10 GPP_B5/SRCCLKREQ0*
- PCIE CLK100M TBT X N — B42 CLKOUT_PCIE_N1
- PCIE CLK100M TBT X P — A42 CLKOUT_PCIE_P1
- TBT X CLKREQ L R — AT7 GPP_B6/SRCCLKREQ1*
- PCIE CLK100M TBT T N — D41 CLKOUT_PCIE_N2
- PCIE CLK100M TBT T P — C41 CLKOUT_PCIE_P2
- TBT T CLKREQ L R — AT8 GPP_B7/SRCCLKREQ2*
- PCIE CLK100M AP N — D40 CLKOUT_PCIE_N3
- PCIE CLK100M AP P — C40 CLKOUT_PCIE_P3
- AP CLKREQ L R — AT10 GPP_B8/SRCCLKREQ3*
- NC PCIE CLK100M CAMERA N — B40 CLKOUT_PCIE_N4
- NC PCIE CLK100M CAMERA P — A40 CLKOUT_PCIE_P4
- NC PCH CLKREQ4 L — AU8 GPP_B9/SRCCLKREQ4*
- NC PCIE CLK100M5N — E40 CLKOUT_PCIE_N5
- NC PCIE CLK100M5P — E38 CLKOUT_PCIE_P5
- NC PCH CLKREQ5 L — AU7 GPP_B10/SRCCLKREQ5*
- CLKOUT_ITPXDP_N — F43 NC ITPXDP CLK100M N
- CLKOUT_ITPXDP_P — E43 NC ITPXDP CLK100M P
- GPD8/SUSCLK — BA17 PM CLK32K SUSCLK R
- XTAL24_IN — E37 PCH CLK24M XTALIN
- XTAL24_OUT — E35 NC PCH CLK24M XTALOUT
- XCLK_BIASREF — E42 PCH DIFFCLK BIASREF
- RTCX1 — AM18 SYSCLK CLK32K PCH
- RTCX2 — AM20 NC PCH CLK32K RTCX2
- SRTCRST* — AN18 PCH SRTCRST L
- RTCRST* — AM16 RTC RESET L

PP1V0 SUS
PLACE_NEAR=U0500.E42:2.54mm
R1520 2.7K 1% 1/20W MF 201

PP3V0 G3H
R1530 20K 1% 1/20W MF 201
R1531 20K 1% 1/20W MF 201
C1530 1UF 20% 6.3V X6S-CERM 0201
C1531 1UF 20% 6.3V X6S-CERM 0201

PP3V3 SUS
R1550 100K 5% 1/20W MF 201 — SMC RUNTIME SCI L

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB
LAST CHANGE: Thu Jun 18 20:05:18 2015

PAGE TITLE
PCH PCIE/USB/CLKS

Apple Inc.

DRAWING NUMBER 051-00515 | SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 15 OF 145
SHEET 15 OF 119

ALL GPP_F* PINS ARE 1.8V ONLY!

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 6 OF 20

		LPSS		ISH		
19 16 OUT	PU_AUD_SPI_CS_L	AN8	GPP_B15/GSPI0_CS*		GPP_D5/ISH_I2C0_SDA	M4	MLB_BOARD_ID0 16
19 16 OUT	PD_AUD_SPI_CLK	AP7	GPP_B16/GSPI0_CLK		GPP_D6/ISH_I2C0_SCL	N3	MLB_BOARD_ID1 16
19 16 IN	PD_AUD_SPI_MISO	AP8	GPP_B17/GSPI0_MISO		GPP_D7/ISH_I2C1_SDA	N1	MLB_BOARD_ID2 16
19 16 OUT	PU_AUD_SPI_MOSI	AR7	GPP_B18/GSPI0_MOSI	(STRAP)	GPP_D8/ISH_I2C1_SCL	N2	MLB_BOARD_ID3 16
43 16 OUT	TPAD_SPI_CS_L	AM5	GPP_B19/GSPI1_CS*		GPP_D1/SPI1_CLK	M2	NC_PCH_GPP_D1 102
43 16 OUT	TPAD_SPI_CLK	AN7	GPP_B20/GSPI1_CLK		GPP_D2/SPI1_MISO	M3	NC_SPKR_ID1 19
43 16 IN	TPAD_SPI_MISO	AP5	GPP_B21/GSPI1_MISO		GPP_D3/SPI1_MOSI	J4	NC_PCH_GPP_D3 102
43 16 OUT	TPAD_SPI_MOSI	AN5	GPP_B22/GSPI1_MOSI	(STRAP)	GPP_D4/FLASHTRIG	B7	NC_PCH_GPP_D4 102
35 16 IN	PCH_BT_UART_D2R	AB1	GPP_C8/UART0_RXD	(1.8V)	GPP_F4/I2C2_SDA	AH9	NC_I2C_UPC_SDA BI 19
35 16 OUT	PCH_BT_UART_R2D	AB2	GPP_C9/UART0_TXD	(1.8V)	GPP_F5/I2C2_SCL	AH10	NC_I2C_UPC_SCL OUT 19
35 16 OUT	PCH_BT_UART_RTS_L	W4	GPP_C10/UART0_RTS*		GPP_G6/SD_CLK	W8	AP_RESET_L OUT 19 35 36
35 16 IN	PCH_BT_UART_CTS_L	AB3	GPP_C11/UART0_CTS*		GPP_D9	P2	MLB_BOARD_ID4 16
18 16 OUT	AP_S0IX_WAKE_SEL	U7	GPP_C16/I2C0_SDA		GPP_D10	P3	NC_MLB_DEV_L IN 19
18 16 IN	AP_S0IX_WAKE_L	U6	GPP_C17/I2C0_SCL		GPP_G7/SD_WP	W7	PD_AP_DEV_WAKE OUT 16 19
28 16 IN	TBT_X_CIO_PLUG_EVENT_L	U8	GPP_C18/I2C1_SDA		GPP_G2/SD_DATA1	AB12	TBT_T_CIO_PWR_EN OUT 84
94 16 IN	TBT_T_CIO_PLUG_EVENT_L	U9	GPP_C19/I2C1_SCL		GPP_G3/SD_DATA2	W12	TBT_T_USB_PWR_EN OUT 84
19 16 IN	PCH_SSD_SOC_UART_D2R	AC1	GPP_C12/UART1_RXD/ISH_UART1_RXD		GPP_G4/SD_DATA3	W11	TBT_X_PCI_RESET_L OUT 19
19 16 OUT	PCH_SSD_SOC_UART_R2D	AC2	GPP_C13/UART1_TXD/ISH_UART1_TXD		GPP_G5/SD_CD*	W10	TBT_T_PCI_RESET_L OUT 19
19 16 OUT	PU_SOC_UART_RTS_L	AC3	GPP_C14/UART1_RTS*/ISH_UART1_RTS*		GPP_A18/ISH_GP0	AY8	SPIROM_USE_MLB OUT 16 59
19 16 IN	PD_SOC_UART_CTS_L	AB4	GPP_C15/UART1_CTS*/ISH_UART1_CTS*		GPP_A19/ISH_GP1	BA8	LCD_IRQ_L OUT 16 80 104
104 91 19 IN	SSD_RESET_L	N11	GPP_E22		GPP_A20/ISH_GP2	BB7	DDI1_MUX_SEL IN 28
94 28 16 OUT	TBT_POC_RESET	N12	GPP_E23		GPP_A21/ISH_GP3	BA7	DDI2_MUX_SEL IN 28
19	BT_I2S_CLK_1V8	AK6	GPP_F0/I2S2_SCLK		GPP_A22/ISH_GP4	AY7	TPAD_SPI_IF_EN OUT 16 43
19	BT_I2S_SYNC_1V8	AK7	GPP_F1/I2S2_SFRM		GPP_A23/ISH_GP5	AW7	TPAD_SPI_INT_L IN 16 43
19	BT_I2S_R2D_1V8	AK9	GPP_F2/I2S2_TXD	(1.8V)	SX_EXIT_HOLDOFF*/GPP_A12/BM_BUSY*/ISH_GP6	AP13	AUD_PWR_EN OUT 16 61
19	BT_I2S_D2R_1V8	AK10	GPP_F3/I2S2_RXD				

PP3V3_S0 5 13 14 19 94 101

PP3V3_SUS 8 13 14 15 101

R1643	47K	5%	1/20W	MF	201		PCH_SSD_SOC_UART_D2R	16 19
R1642	47K	5%	1/20W	MF	201		PCH_SSD_SOC_UART_R2D	16 19
R1641	47K	5%	1/20W	MF	201		PU_SOC_UART_RTS_L	16 19
R1640	47K	5%	1/20W	MF	201		PD_SOC_UART_CTS_L	16 19
R1650	100K	5%	1/20W	MF	201		SPIROM_USE_MLB	16 59
R1652	100K	5%	1/20W	MF	201		AUD_PWR_EN	16 61
R1653	47K	5%	1/20W	MF	201		PU_AUD_SPI_CS_L	16 19
R1654	47K	5%	1/20W	MF	201		PD_AUD_SPI_CLK	16 19
R1655	47K	5%	1/20W	MF	201		PD_AUD_SPI_MISO	16 19
R1656	1K	5%	1/20W	MF	201		PU_AUD_SPI_MOSI	16 19
R1657	47K	5%	1/20W	MF	201		TPAD_SPI_CS_L	16 43
R1658	47K	5%	1/20W	MF	201		TPAD_SPI_CLK	16 43
R1659	47K	5%	1/20W	MF	201		TPAD_SPI_MISO	16 43
R1660	150K	5%	1/20W	MF	201		TPAD_SPI_MOSI	16 43
R1674	100K	5%	1/20W	MF	201		TPAD_SPI_INT_L	16 43
R1676	10K	5%	1/20W	MF	201	NOSTUFF		
R1673	100K	5%	1/20W	MF	201	NOSTUFF	TPAD_SPI_IF_EN	16 43
R1675	100K	5%	1/20W	MF	201	NOSTUFF		
R1661	47K	5%	1/20W	MF	201		PCH_BT_UART_D2R	16 35
R1662	47K	5%	1/20W	MF	201		PCH_BT_UART_R2D	16 35
R1663	47K	5%	1/20W	MF	201		PCH_BT_UART_RTS_L	16 35
R1664	47K	5%	1/20W	MF	201		PCH_BT_UART_CTS_L	16 35
R1665	100K	5%	1/20W	MF	201		AP_S0IX_WAKE_SEL	16 18
R1666	100K	5%	1/20W	MF	201		AP_S0IX_WAKE_L	16 18
R1667	100K	5%	1/20W	MF	201		PD_AP_DEV_WAKE	16 19
R1669	100K	5%	1/20W	MF	201		LCD_IRQ_L DRIVEN PUSH PULL FROM SWITCHED RAIL.	16 80 104
R1668	100K	5%	1/20W	MF	201		TBT_X_CIO_PLUG_EVENT_L	16 28
R1671	100K	5%	1/20W	MF	201		TBT_T_CIO_PLUG_EVENT_L	16 94
R1672	100K	5%	1/20W	MF	201		TBT_POC_RESET	16 28 94

MLB ID STRAPS.

PCH INTERNAL PULL-UPS ARE TO VCCGPPD = 3.3V.

16 MLB_BOARD_ID0
16 MLB_BOARD_ID1
16 MLB_BOARD_ID2
16 MLB_BOARD_ID3
16 MLB_BOARD_ID4

OMIT_TABLE R1694	OMIT_TABLE R1693	OMIT_TABLE R1692	OMIT_TABLE R1691	OMIT_TABLE R1690
1K 5% 1/20W MF 201	1K 5% 1/20W MF 201	1K 5% 1/20W MF 201	1K 5% 1/20W MF 201	1K 5% 1/20W MF 201

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	CODE
117S0006	0	RES,MF,1/20W/1K OHM,5,0201,SMD		BOARD_ID:0	<11111>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1690	BOARD_ID:1	<11110>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691	BOARD_ID:2	<11101>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691,R1690	BOARD_ID:3	<11100>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692	BOARD_ID:4	<11011>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1690	BOARD_ID:5	<11010>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691	BOARD_ID:6	<11001>
117S0006	3	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691,R1690	BOARD_ID:7	<11000>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693	BOARD_ID:8	<10111>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1690	BOARD_ID:9	<10110>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691	BOARD_ID:10	<10101>
117S0006	3	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691,R1690	BOARD_ID:11	<10100>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1694	BOARD_ID:16	<01111>

BOM_COST_GROUP=CPU & CHIPSET

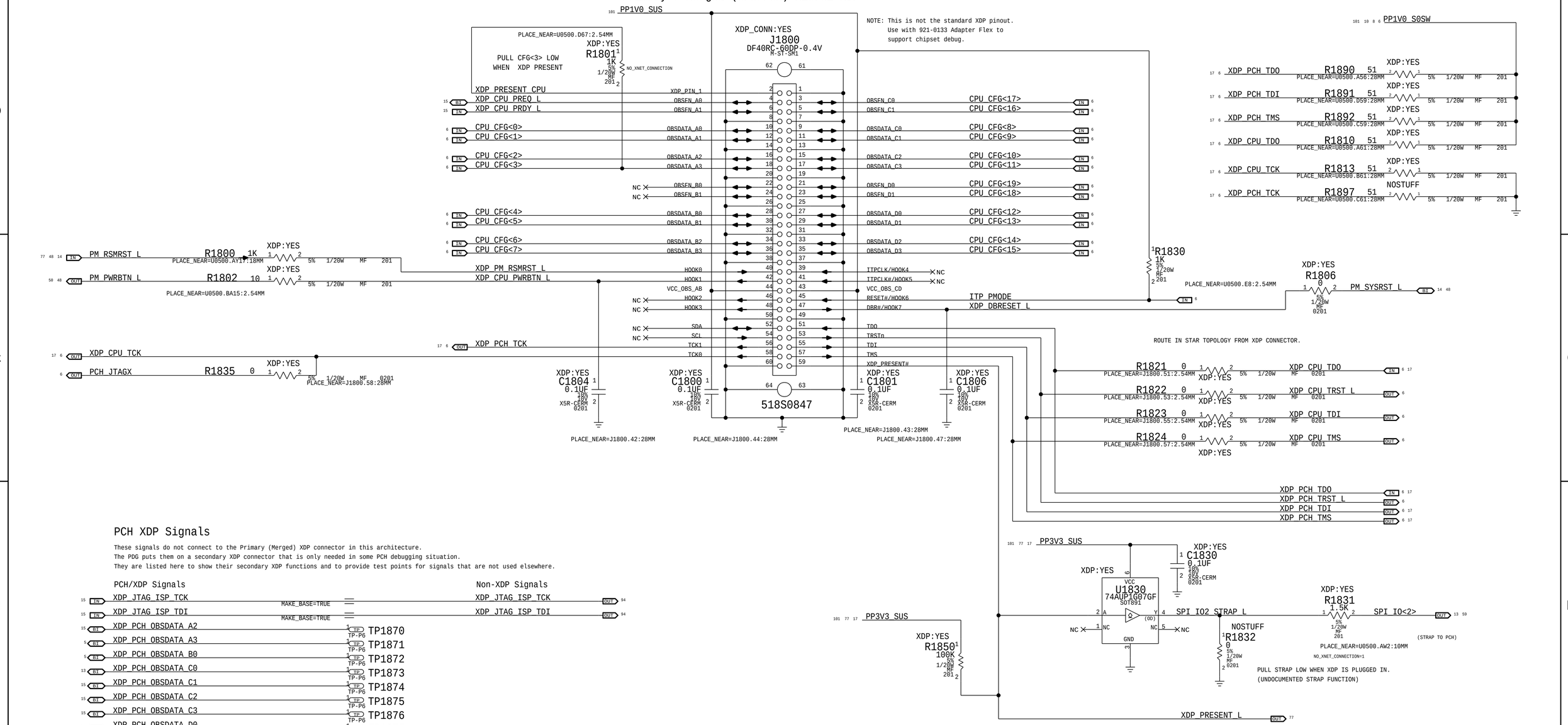
DESIGN: X502/MLB
LAST CHANGE: Wed Oct 28 12:50:22 2015

PAGE TITLE
PCH SPI/UART/GPIO

Apple Inc.

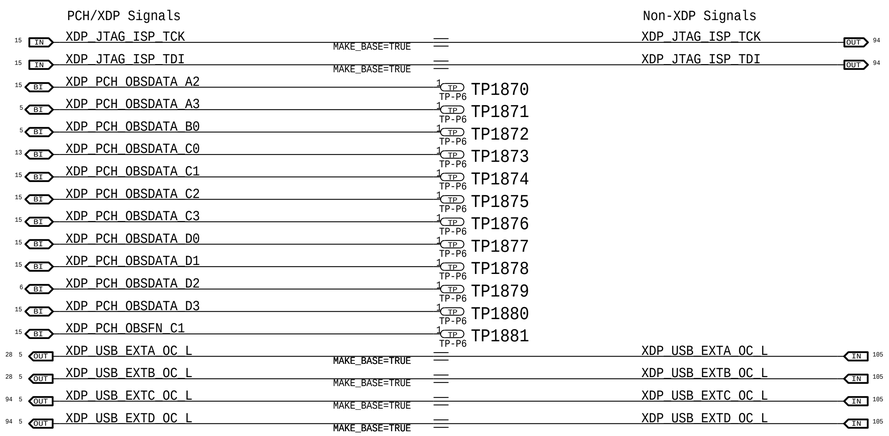
DRAWING NUMBER 051-00515 SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 16 OF 145
SHEET 16 OF 119

Primary / Merged (CPU/PCH) Micro2-XDP



PCH XDP Signals

These signals do not connect to the Primary (Merged) XDP connector in this architecture.
The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation.
They are listed here to show their secondary XDP functions and to provide test points for signals that are not used elsewhere.



Unused GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

BOM_COST_GROUP=DEBUG

DESIGN: X502/MLB
LAST CHANGE: Thu Oct 22 19:53:09 2015

PAGE TITLE
CPU/PCH Merged XDP

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
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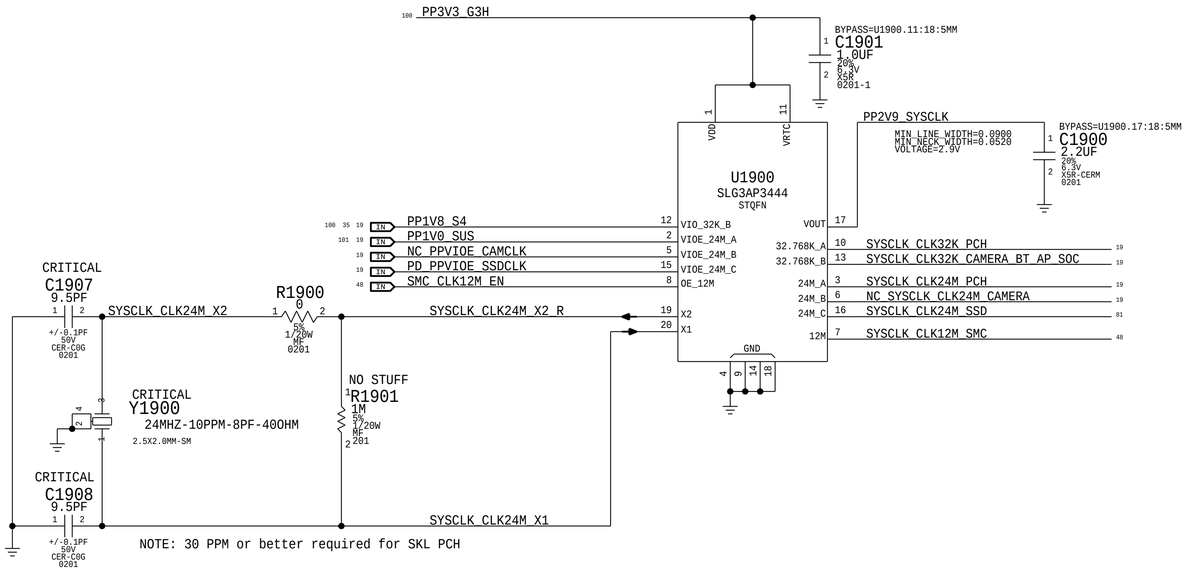
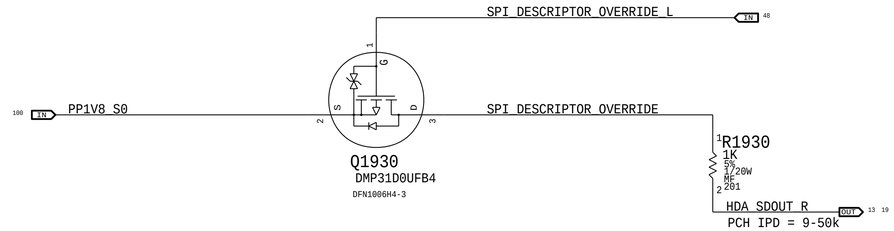
System 32kHz / 12MHz / 24MHz Clock Generator

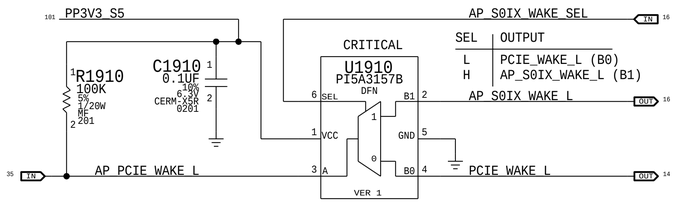


PCH ME Disable Strap



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
***** Circuit does not support HDA voltage >3.3V.

PCIe Wake Muxing



SEL	OUTPUT
L	PCIE_WAKE_L (B0)
H	AP_S0IX_WAKE_L (B1)

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
Chipset Support 1

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
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Platform Reset Connections

Unbuffered

PLT_RST_L → R2000 100K → TBT_X_PCI_RESET_L (MAKE_BASE=TRUE) → TBT_X_PCI_RESET_L
R2001 100K → TBT_T_PCI_RESET_L (MAKE_BASE=TRUE) → TBT_T_PCI_RESET_L
R2002 100K → AP_RESET_L
R2003 100K → SSD_RESET_L
R2004 100K → SMC_LRESET_L

PCIE CLKREQS

PP3V3_S0

R2080	47K	SSD_CLKREQ_L	R2084 1K	SSD_CLKREQ_L_R (MAKE_BASE=TRUE)
R2081	47K	TBT_X_CLKREQ_L	R2085 1K	TBT_X_CLKREQ_L_R (MAKE_BASE=TRUE)
R2082	47K	TBT_T_CLKREQ_L	R2086 1K	TBT_T_CLKREQ_L_R (MAKE_BASE=TRUE)
R2083	47K	AP_CLKREQ_L	R2087 1K	AP_CLKREQ_L_R (MAKE_BASE=TRUE)

ENABLE DDPB DDPC INTERFACES

PP3V3_S0
R2050 2.2K PCH_DDPB_CTRLDATA
R2051 2.2K PCH_DDPC_CTRLDATA

CATERR PU

PP1V0_S3
R2059 51 CPU_CATERR_L

WIFI GPIO PD

R2058 100K PCH_BT_ROM_BOOT

T208 PCH GPIO PUs/PDs & ALIASES

PP1V8_SUS

R2054	100K	SOC_PANIC_L	
R2055	100K	SOC_S2R_ACK_L	
R2056	100K	SOC_PCH_DBELL_L	SOC_PCH_DBELL_L (MAKE_BASE=TRUE)
		PCH_SOC_DBELL	PCH_SOC_DBELL (MAKE_BASE=TRUE)
		SOC_SWD_CLK	SOC_SWD_CLK (MAKE_BASE=TRUE)
R2053	100K	PCH_SOC_DFU_STATUS	
		SOC_TO_STOCKHOLM_EN	

NOSTUFF C2050 100PF 5% 25V C0G 0201

Desense Decoupling Caps on HDA Lines

HDA_SYNC_R — NOSTUFF C2020 3.0PF ±0.1PF 25V NP0-C0G 0201
HDA_SDOUT_R — NOSTUFF C2021 3.0PF ±0.1PF 25V NP0-C0G 0201
HDA_RST_R_L — NOSTUFF C2022 3.0PF ±0.1PF 25V NP0-C0G 0201

Power State Debug LEDs

(For development only)

PP3V3_S5

DBGLED R2090 20K	DBGLED_S5	DBGLED D2090 GRN-90MCD-5MA-2.85V 0402 (PLACE_SIDE=BOTTOM, SILK_PART=S5_ON)	PM_SLP_S5_L
DBGLED R2091 20K	DBGLED_S4	DBGLED D2091 GRN-90MCD-5MA-2.85V 0402 (PLACE_SIDE=BOTTOM, SILK_PART=STBY_ON)	PM_SLP_S4_L
DBGLED R2092 20K	DBGLED_S3	DBGLED D2092 GRN-90MCD-5MA-2.85V 0402 (PLACE_SIDE=BOTTOM, SILK_PART=S3_ON)	PM_SLP_S3_L
DBGLED R2093 20K	DBGLED_S0I3	DBGLED D2093 GRN-90MCD-5MA-2.85V 0402 (PLACE_SIDE=BOTTOM, SILK_PART=S0I3_ON)	
DBGLED R2095 20K	DBGLED_S0	DBGLED D2095 GRN-90MCD-5MA-2.85V 0402 (PLACE_SIDE=BOTTOM, SILK_PART=S0_ON)	PM_SLP_S0_L

DBGLED_S4_D, DBGLED_S3_D, DBGLED_S0I3_D, DBGLED_S0_D → DBGLED Q2090 / DBGLED Q2091 DMN5L06VK-7 SOT563 VER 3

GREENCLK VIOEs

NO_TEST=1, MAKE_BASE=TRUE: NC_PPVIOE_CAMCLK — NC_PPVIOE_CAMCLK
PP1V0_SUS
PP1V8_S4
MAKE_BASE=TRUE: PP1V8_SSD_COLD — NOSTUFF R2010 0 — PD_PPVIOE_SSDCLK
NOSTUFF C2002 0.1UF (BYPASS=U1900.15:18:5MM); C2001 0.1UF (BYPASS=U1900.12:18:5MM); C2000 0.1UF (BYPASS=U1900.02:18:5MM)

GREENCLK CLOCK OUT ALIASES

MAKE_BASE=TRUE: SYSCLK_CLK32K_PCH — SYSCLK_CLK32K_PCH
NC_PCH_CLK32K_RTCX2 (MAKE_BASE=TRUE, NO_TEST=1) — NC_PCH_CLK32K_RTCX2
SYSCLK_CLK24M_PCH — R2024 0 (PCH_CLK:GRNCLK) — PCH_CLK24M_XTALIN (PLACE_NEAR=U1900.3:5MM)
MAKE_BASE=TRUE: SYSCLK_CLK32K_CAMERA_BT_AP_SOC — NOSTUFF R2042 0 — SYSCLK_CLK32K_WIFIBT
R2043 0 — SOC_PMU_CLK_32K
SYSCLK_CLK32K_OSC_OUT — NOSTUFF R2044 0

x100 I2S Level Translator

PP1V8_S0: C2010 0.1UF; PP3V3_S0: C2011 0.1UF
U2010 NLSX5014MU_G (UQFN)

BT_I2S_SYNC_1V8	BT_I2S_SYNC_1V8 (MAKE_BASE=TRUE)	IOLV[1] / IOVCC[1]	BT_I2S_SYNC
BT_I2S_R2D_1V8	BT_I2S_R2D_1V8 (MAKE_BASE=TRUE)	IOLV[2] / IOVCC[2]	BT_I2S_R2D
BT_I2S_D2R_1V8	BT_I2S_D2R_1V8 (MAKE_BASE=TRUE)	IOLV[3] / IOVCC[3]	BT_I2S_D2R
BT_I2S_CLK_1V8	BT_I2S_CLK_1V8 (MAKE_BASE=TRUE)	IOLV[4] / IOVCC[4]	BT_I2S_CLK

EN, GND

BT/SSD DEBUG UART MUX

PP3V3_S0: C2060 0.1UF; PP1V8_S0
U2060 PI3USB102EZLE TQFN (CRITICAL)
PCH_SSD_SOC_UART_D2R (MAKE_BASE=TRUE) — PCH_SSD_SOC_UART_D2R — SSD_DBG_UART_D2R
PCH_SSD_SOC_UART_R2D (MAKE_BASE=TRUE) — PCH_SSD_SOC_UART_R2D — SSD_DBG_UART_R2D_R
R2060 100K, R2061 100K, R2062 100K, R2063 100K
R2066 100K — DEBUGUART_SEL_SOC
SOC_DBG_UART_D2R, SOC_DBG_UART_R2D
R2067 0 NO STUFF, R2068 0 NO STUFF

BOM_COST_GROUP=CPU & CHIPSET

Voltage Props

PP1V_SUS_PCH_VCCCLK2_F	VOLTAGE=1.0V
PP1V_SUS_PCH_VCCCLK4_F	VOLTAGE=1.0V
PP1V_SUS_PCH_VCCCLK5_F	VOLTAGE=1.0V
PP1V_S5_PCH_DCPDSW	VOLTAGE=1.0V
PP1V_SUS_PCH_VCCAPLL_F	VOLTAGE=1.0V
PP1V_SUSSW_PCH_VCCAMPHYPLL_F	VOLTAGE=1.8V
PP1V8_SUS_PCH_VCC1P8	VOLTAGE=1.0V
PP1V8_S0_PCH_VCCHDA_F	VOLTAGE=3.0V
PPDCPRTC_PCH	

NO TEST

NC_USB2_10N, NC_USB2_10P, NC_USB2_05N, NC_USB2_05P (NO_TEST=1)

Unused GPIOs with PUs/PDs

PD_AP_DEV_WAKE	PD_AP_DEV_WAKE (MAKE_BASE=TRUE)
PU_AUD_SPI_CS_L	PU_AUD_SPI_CS_L (MAKE_BASE=TRUE)
PD_AUD_SPI_CLK	PD_AUD_SPI_CLK (MAKE_BASE=TRUE)
PD_AUD_SPI_MISO	PD_AUD_SPI_MISO (MAKE_BASE=TRUE)
PU_AUD_SPI_MOSI	PU_AUD_SPI_MOSI (MAKE_BASE=TRUE)
PD_LCD_PSR_EN	PD_LCD_PSR_EN (MAKE_BASE=TRUE)
PD_SSD_UART_CTS_L	PD_SSD_UART_CTS_L (MAKE_BASE=TRUE)
PU_SOC_UART_RTS_L	PU_SOC_UART_RTS_L (MAKE_BASE=TRUE)
PD_SOC_UART_CTS_L	PD_SOC_UART_CTS_L (MAKE_BASE=TRUE)

SIGNAL ALIASES

PD_PPVIOE_SSDCLK	PD_PPVIOE_SSDCLK (MAKE_BASE=TRUE)
CAMERA_PWR_EN	CAMERA_PWR_EN (MAKE_BASE=TRUE)
ALS_SOC_UART_D2R	ALS_SOC_UART_D2R (MAKE_BASE=TRUE)
ALS_SOC_UART_R2D	ALS_SOC_UART_R2D (MAKE_BASE=TRUE)

NC SIGNAL ALIASES

NC_PCH_CLKREQ4_L	NC_PCH_CLKREQ4_L (MAKE_BASE=TRUE)
NC_PCIE_CLK100M5N	NC_PCIE_CLK100M5N (MAKE_BASE=TRUE, NO_TEST=1)
NC_PCIE_CLK100M5P	NC_PCIE_CLK100M5P (MAKE_BASE=TRUE, NO_TEST=1)
NC_PCH_CLKREQ5_L	NC_PCH_CLKREQ5_L (MAKE_BASE=TRUE, NO_TEST=1)
NC_SPKR_ID1	NC_SPKR_ID1 (MAKE_BASE=TRUE, NO_TEST=1)
NC_PCH_CLK24M_XTALOUT	NC_PCH_CLK24M_XTALOUT (MAKE_BASE=TRUE, NO_TEST=1)
NC_PCH_GPP_E15	NC_PCH_GPP_E15 (MAKE_BASE=TRUE, NO_TEST=1)
NC_PCH_BSSB_CLK	NC_PCH_BSSB_CLK (MAKE_BASE=TRUE, NO_TEST=1)
NC_PCH_BSSB_DATA	NC_PCH_BSSB_DATA (MAKE_BASE=TRUE, NO_TEST=1)
NC_ITPXDP_CLK100M_N	NC_ITPXDP_CLK100M_N (MAKE_BASE=TRUE, NO_TEST=1)
NC_ITPXDP_CLK100M_P	NC_ITPXDP_CLK100M_P (MAKE_BASE=TRUE, NO_TEST=1)
NC_UPC_I2C_INT_L	NC_UPC_I2C_INT_L (MAKE_BASE=TRUE, NO_TEST=1)
NC_SPKR_ID0	NC_SPKR_ID0 (MAKE_BASE=TRUE, NO_TEST=1)
NC_USB3_04_D2RN	NC_USB3_04_D2RN (MAKE_BASE=TRUE, NO_TEST=1)
NC_USB3_04_D2RP	NC_USB3_04_D2RP (MAKE_BASE=TRUE, NO_TEST=1)
NC_USB3_04_R2DN	NC_USB3_04_R2DN (MAKE_BASE=TRUE, NO_TEST=1)
NC_USB3_04_R2DP	NC_USB3_04_R2DP (MAKE_BASE=TRUE, NO_TEST=1)
NC_I2C_UPC_SDA	NC_I2C_UPC_SDA (MAKE_BASE=TRUE, NO_TEST=1)
NC_I2C_UPC_SCL	NC_I2C_UPC_SCL (MAKE_BASE=TRUE, NO_TEST=1)
NC_MLB_DEV_L	NC_MLB_DEV_L (MAKE_BASE=TRUE, NO_TEST=1)
NC_SYSCLK_CLK24M_CAMERA	NC_SYSCLK_CLK24M_CAMERA (NO_TEST=1)
NC_PCH_STRP_TLSCONF	NC_PCH_STRP_TLSCONF (MAKE_BASE=TRUE, NO_TEST=1)
NC_PCH_STRP_ESPI	NC_PCH_STRP_ESPI (MAKE_BASE=TRUE, NO_TEST=1)
NC_PCH_STRP_BSSB_SEL_GPIO	NC_PCH_STRP_BSSB_SEL_GPIO (MAKE_BASE=TRUE, NO_TEST=1)
NC_PCH_CLKOUT_LPC1	NC_PCH_CLKOUT_LPC1 (MAKE_BASE=TRUE, NO_TEST=1)
NC_VCCPRIM_CORE_VID0	NC_VCCPRIM_CORE_VID0 (MAKE_BASE=TRUE, NO_TEST=1)
NC_VCCPRIM_CORE_VID1	NC_VCCPRIM_CORE_VID1 (MAKE_BASE=TRUE, NO_TEST=1)
NC_CAMERA_RESET_L	NC_CAMERA_RESET_L (NO_TEST=1)

PAGE TITLE: Chipset Support 2

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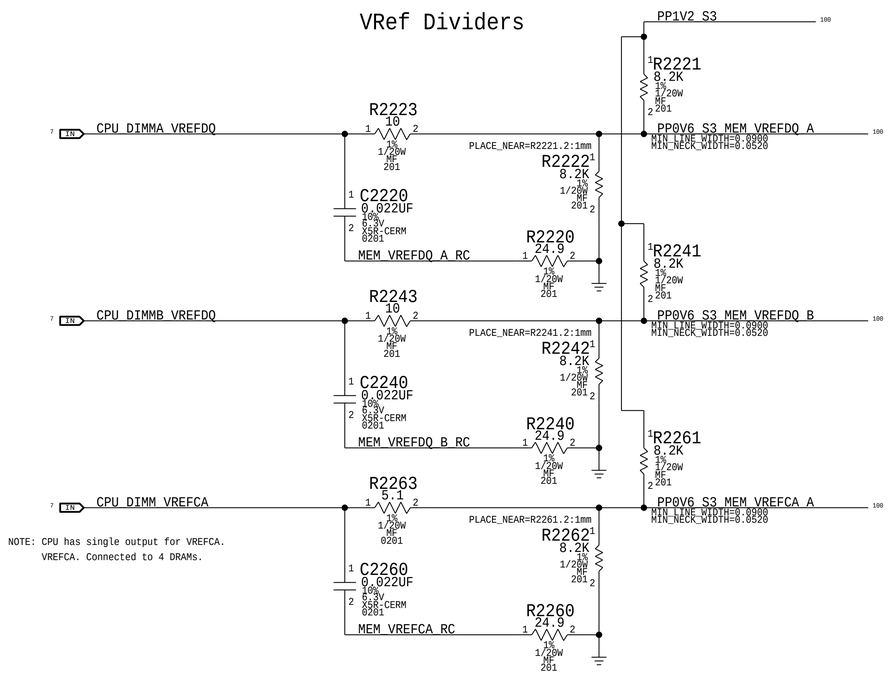
CPU-Based Margining

VRef Dividers



NOTE: CPU has single output for VREFCA.
VREFCA. Connected to 4 DRAMs.

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J52_MLB SYNC_DATE=05/12/2015

PAGE TITLE

LPDDR3 VREF Margining

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D

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BRANCH dvt-fab09-0

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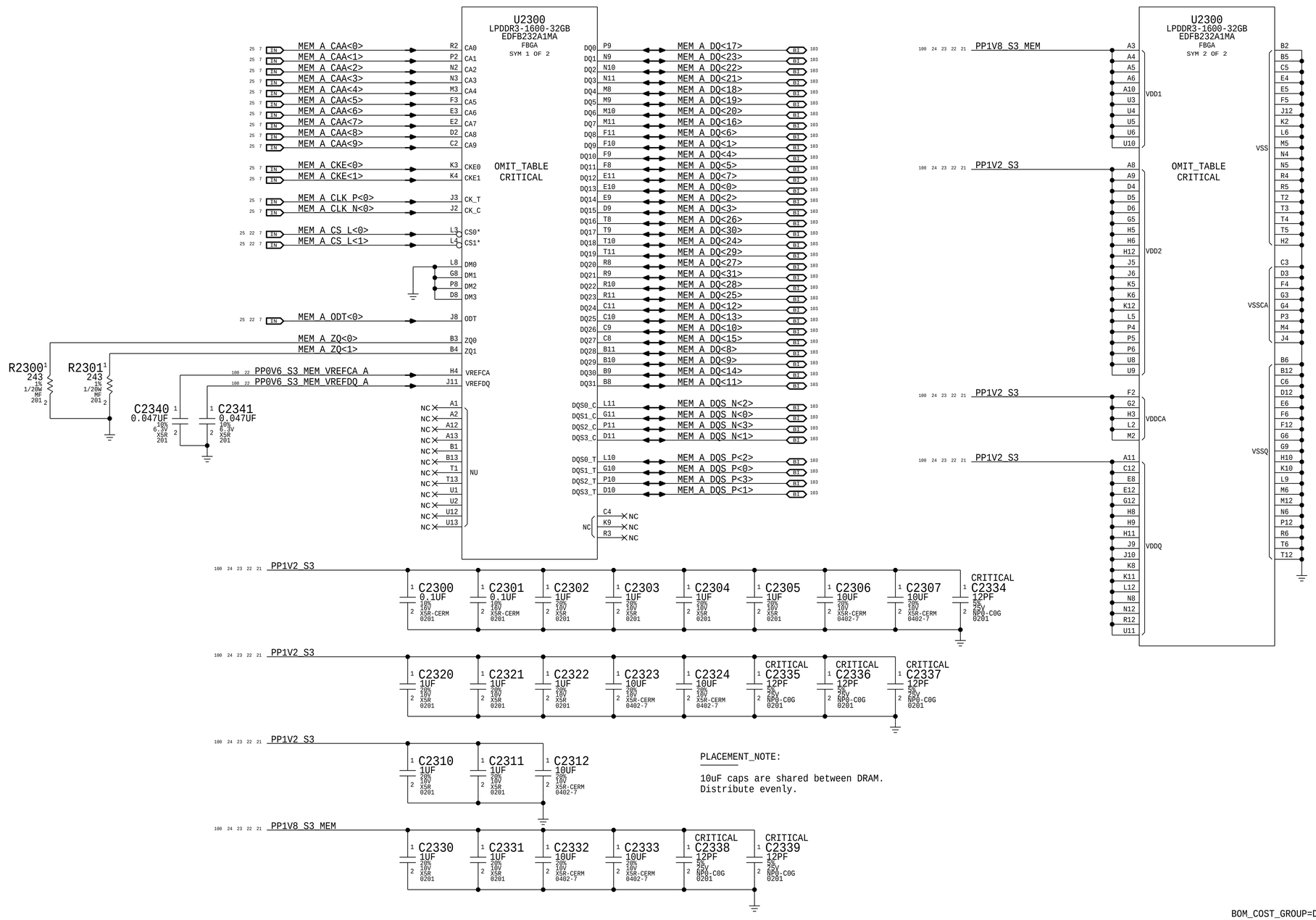
LPDDR3 CHANNEL A (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J52_MLB SYNC_DATE=05/12/2015

PAGE TITLE
LPDDR3 DRAM Channel A (00-31)

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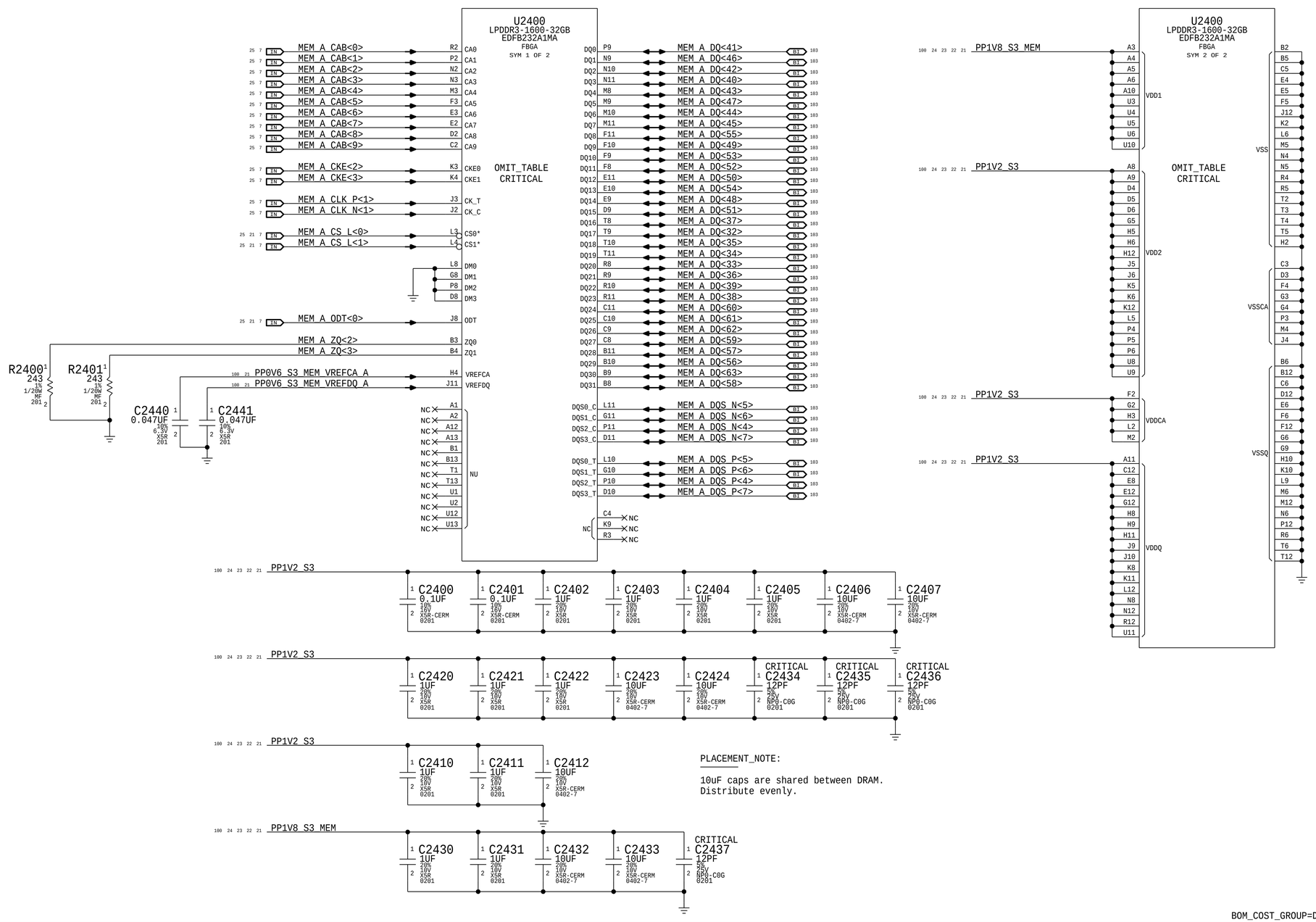
LPDDR3 CHANNEL A (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J52_MLB SYNC_DATE=05/12/2015

PAGE TITLE
LPDDR3 DRAM Channel A (32-63)

Apple Inc.

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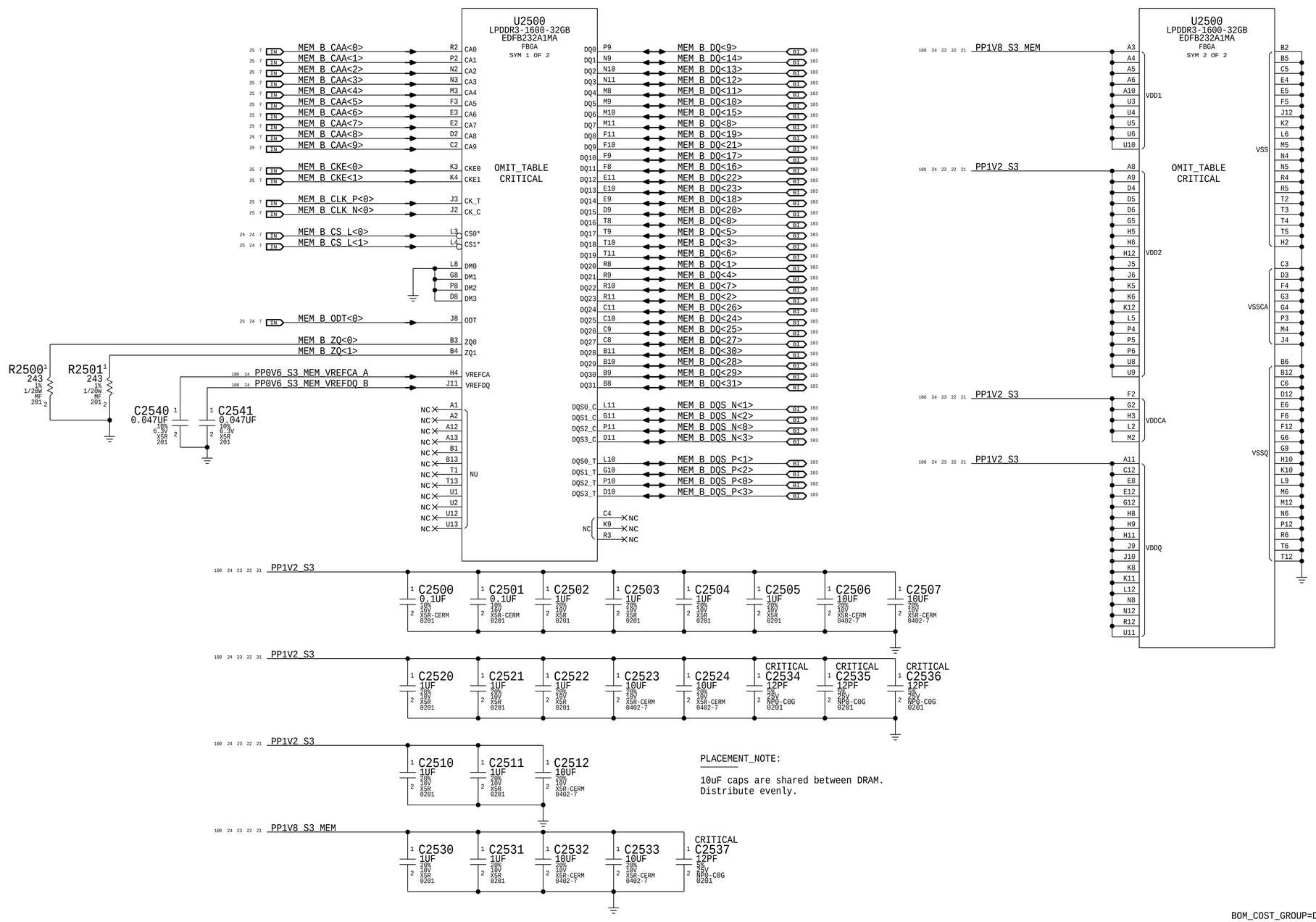
LPDDR3 CHANNEL B (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J52_MLB SYNC_DATE=05/12/2015

PAGE TITLE
LPDDR3 DRAM Channel B (00-31)

Apple Inc.

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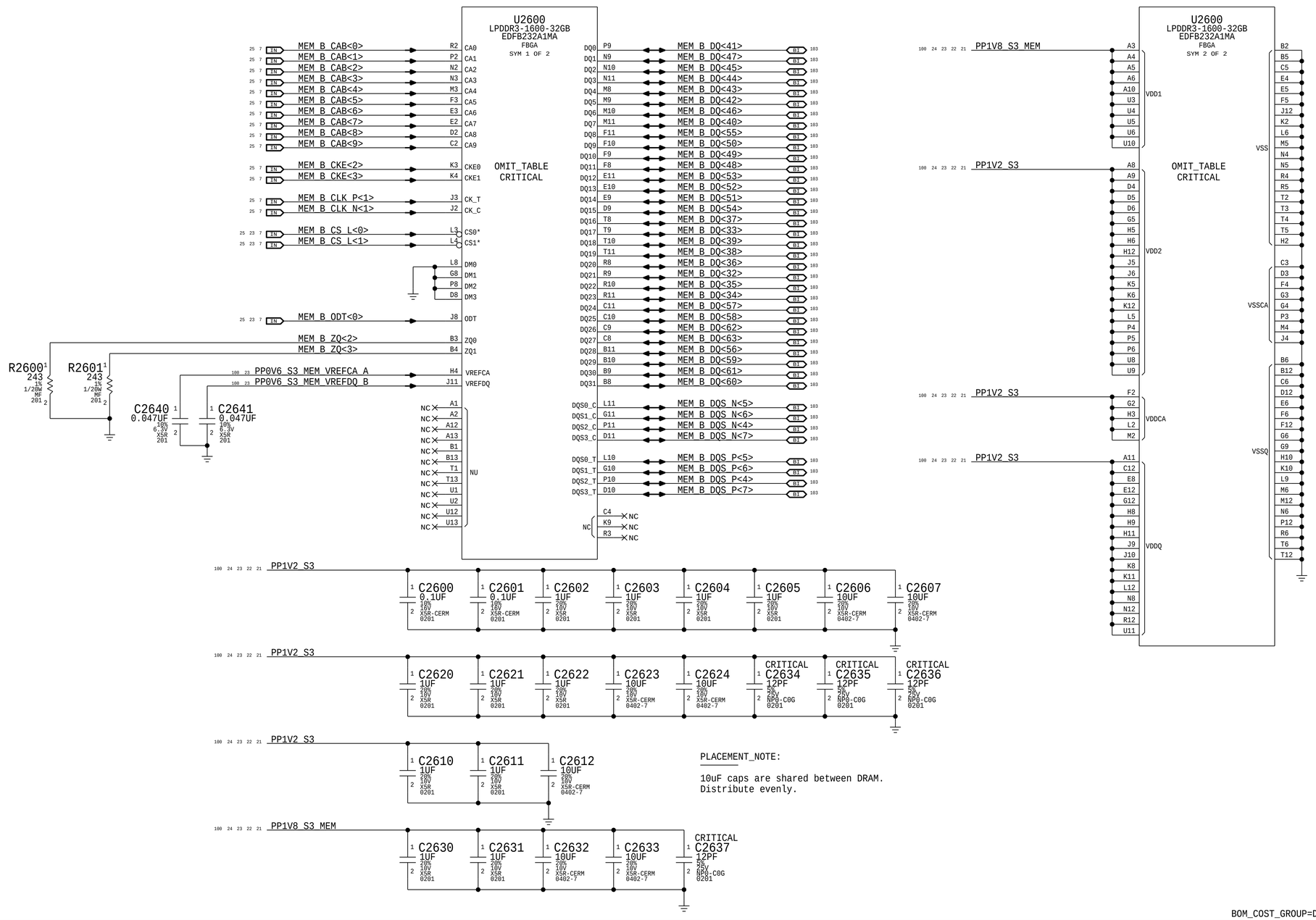
LPDDR3 CHANNEL B (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J52_MLB	SYNC_DATE=05/12/2015
PAGE TITLE: LPDDR3 DRAM Channel B (32-63)	
Apple Inc.	DRAWING NUMBER: 051-00515 — SIZE: D
	REVISION: 9.0.0
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Intel recommends 68 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK

PP0V6_S0_DDRVTT

MEM_A_CAA<9>	R2700	68	1% 1/20W 201 MF
MEM_A_CAA<8>	R2701	68	1% 1/20W 201 MF
MEM_A_CAA<6>	R2702	68	1% 1/20W 201 MF
MEM_A_CAA<7>	R2703	68	1% 1/20W 201 MF
MEM_A_CAA<5>	R2704	68	1% 1/20W 201 MF
MEM_A_CLK_P<0>	R2705	39	1% 1/20W 201 MF
MEM_A_CLK_N<0>	R2706	39	1% 1/20W 201 MF
MEM_A_CKE<1>	R2707	82	1% 1/20W 201 MF
MEM_A_CKE<0>	R2708	82	1% 1/20W 201 MF
MEM_A_CAA<4>	R2709	68	1% 1/20W 201 MF
MEM_A_CAA<3>	R2710	68	1% 1/20W 201 MF
MEM_A_CAA<2>	R2711	68	1% 1/20W 201 MF
MEM_A_CAA<1>	R2712	68	1% 1/20W 201 MF
MEM_A_CAA<0>	R2713	68	1% 1/20W 201 MF
MEM_A_CAB<9>	R2714	68	1% 1/20W 201 MF
MEM_A_CAB<8>	R2715	68	1% 1/20W 201 MF
MEM_A_CAB<6>	R2716	68	1% 1/20W 201 MF
MEM_A_CAB<7>	R2717	68	1% 1/20W 201 MF
MEM_A_CAB<5>	R2718	68	1% 1/20W 201 MF
MEM_A_CLK_P<1>	R2719	39	1% 1/20W 201 MF
MEM_A_CLK_N<1>	R2720	39	1% 1/20W 201 MF
MEM_A_CKE<2>	R2721	82	1% 1/20W 201 MF
MEM_A_CKE<3>	R2722	82	1% 1/20W 201 MF
MEM_A_CAB<4>	R2723	68	1% 1/20W 201 MF
MEM_A_CAB<2>	R2724	68	1% 1/20W 201 MF
MEM_A_CAB<3>	R2725	68	1% 1/20W 201 MF
MEM_A_CAB<1>	R2726	68	1% 1/20W 201 MF
MEM_A_CAB<0>	R2727	68	1% 1/20W 201 MF
MEM_A_CS_L<0>	R2728	82	1% 1/20W 201 MF
MEM_A_CS_L<1>	R2729	82	1% 1/20W 201 MF
MEM_A_ODT<0>	R2730	82	1% 1/20W 201 MF

C2700 0.47UF 20% 4V CERM-X5R-1 201
C2730 12PF 5% 25V NP0-C0G 0201
C2701 0.47UF 20% 4V CERM-X5R-1 201
C2702 0.47UF 20% 4V CERM-X5R-1 201
C2703 0.47UF 20% 4V CERM-X5R-1 201
C2704 0.47UF 20% 4V CERM-X5R-1 201
C2705 0.47UF 20% 4V CERM-X5R-1 201
C2706 0.47UF 20% 4V CERM-X5R-1 201
C2707 0.47UF 20% 4V CERM-X5R-1 201
C2708 0.47UF 20% 4V CERM-X5R-1 201
C2709 0.47UF 20% 4V CERM-X5R-1 201
CRITICAL
C2720 20UF 20% 6.3V CERM-X5R 0402
C2722 3.0PF ±0.1PF 25V NP0-C0G 0201

PP0V6_S0_DDRVTT

MEM_B_CAA<9>	R2740	68	1% 1/20W 201 MF
MEM_B_CAA<8>	R2741	68	1% 1/20W 201 MF
MEM_B_CAA<7>	R2742	68	1% 1/20W 201 MF
MEM_B_CAA<6>	R2743	68	1% 1/20W 201 MF
MEM_B_CAA<5>	R2744	68	1% 1/20W 201 MF
MEM_B_CLK_P<0>	R2745	39	1% 1/20W 201 MF
MEM_B_CLK_N<0>	R2746	39	1% 1/20W 201 MF
MEM_B_CKE<1>	R2747	82	1% 1/20W 201 MF
MEM_B_CKE<0>	R2748	82	1% 1/20W 201 MF
MEM_B_CAA<4>	R2749	68	1% 1/20W 201 MF
MEM_B_CAA<2>	R2750	68	1% 1/20W 201 MF
MEM_B_CAA<3>	R2751	68	1% 1/20W 201 MF
MEM_B_CAA<1>	R2752	68	1% 1/20W 201 MF
MEM_B_CAA<0>	R2753	68	1% 1/20W 201 MF
MEM_B_CAB<9>	R2754	68	1% 1/20W 201 MF
MEM_B_CAB<8>	R2755	68	1% 1/20W 201 MF
MEM_B_CAB<7>	R2756	68	1% 1/20W 201 MF
MEM_B_CAB<6>	R2757	68	1% 1/20W 201 MF
MEM_B_CAB<5>	R2758	68	1% 1/20W 201 MF
MEM_B_CLK_N<1>	R2759	39	1% 1/20W 201 MF
MEM_B_CLK_P<1>	R2760	39	1% 1/20W 201 MF
MEM_B_CKE<2>	R2761	82	1% 1/20W 201 MF
MEM_B_CKE<3>	R2762	82	1% 1/20W 201 MF
MEM_B_CAB<4>	R2763	68	1% 1/20W 201 MF
MEM_B_CAB<2>	R2764	68	1% 1/20W 201 MF
MEM_B_CAB<3>	R2765	68	1% 1/20W 201 MF
MEM_B_CAB<1>	R2766	68	1% 1/20W 201 MF
MEM_B_CAB<0>	R2767	68	1% 1/20W 201 MF
MEM_B_CS_L<0>	R2768	82	1% 1/20W 201 MF
MEM_B_CS_L<1>	R2769	82	1% 1/20W 201 MF
MEM_B_ODT<0>	R2770	82	1% 1/20W 201 MF

C2710 0.47UF 20% 4V CERM-X5R-1 201
C2731 12PF 5% 25V NP0-C0G 0201
C2711 0.47UF 20% 4V CERM-X5R-1 201
C2712 0.47UF 20% 4V CERM-X5R-1 201
C2713 0.47UF 20% 4V CERM-X5R-1 201
C2714 0.47UF 20% 4V CERM-X5R-1 201
C2715 0.47UF 20% 4V CERM-X5R-1 201
C2716 0.47UF 20% 4V CERM-X5R-1 201
C2717 0.47UF 20% 4V CERM-X5R-1 201
C2718 0.47UF 20% 4V CERM-X5R-1 201
C2719 0.47UF 20% 4V CERM-X5R-1 201
CRITICAL
C2740 20UF 20% 6.3V CERM-X5R 0402
C2742 3.0PF ±0.1PF 25V NP0-C0G 0201

BOM_COST_GROUP=DRAM

SYNC_MASTER=J52_MLB SYNC_DATE=05/12/2015

PAGE TITLE
LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D
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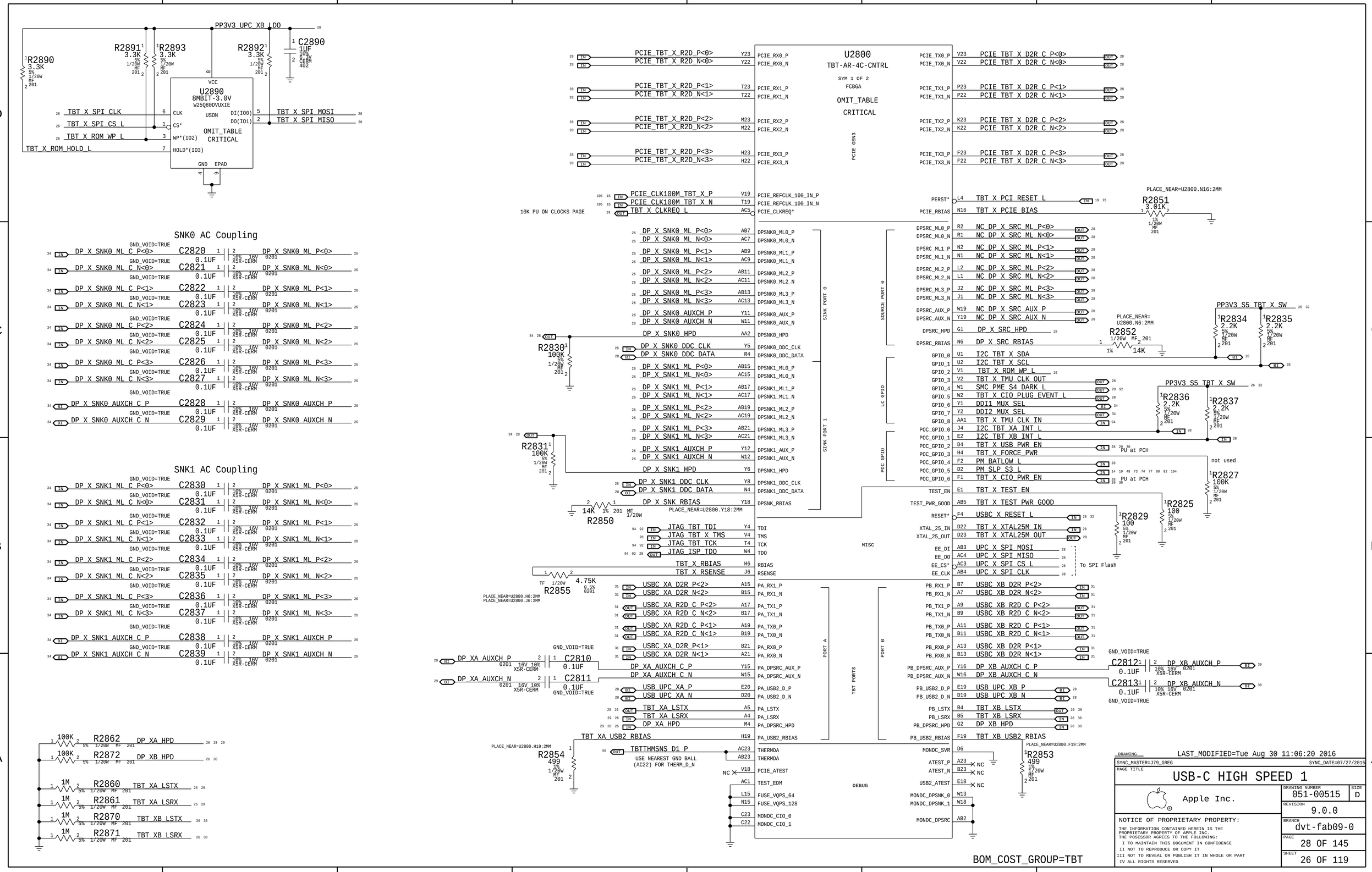

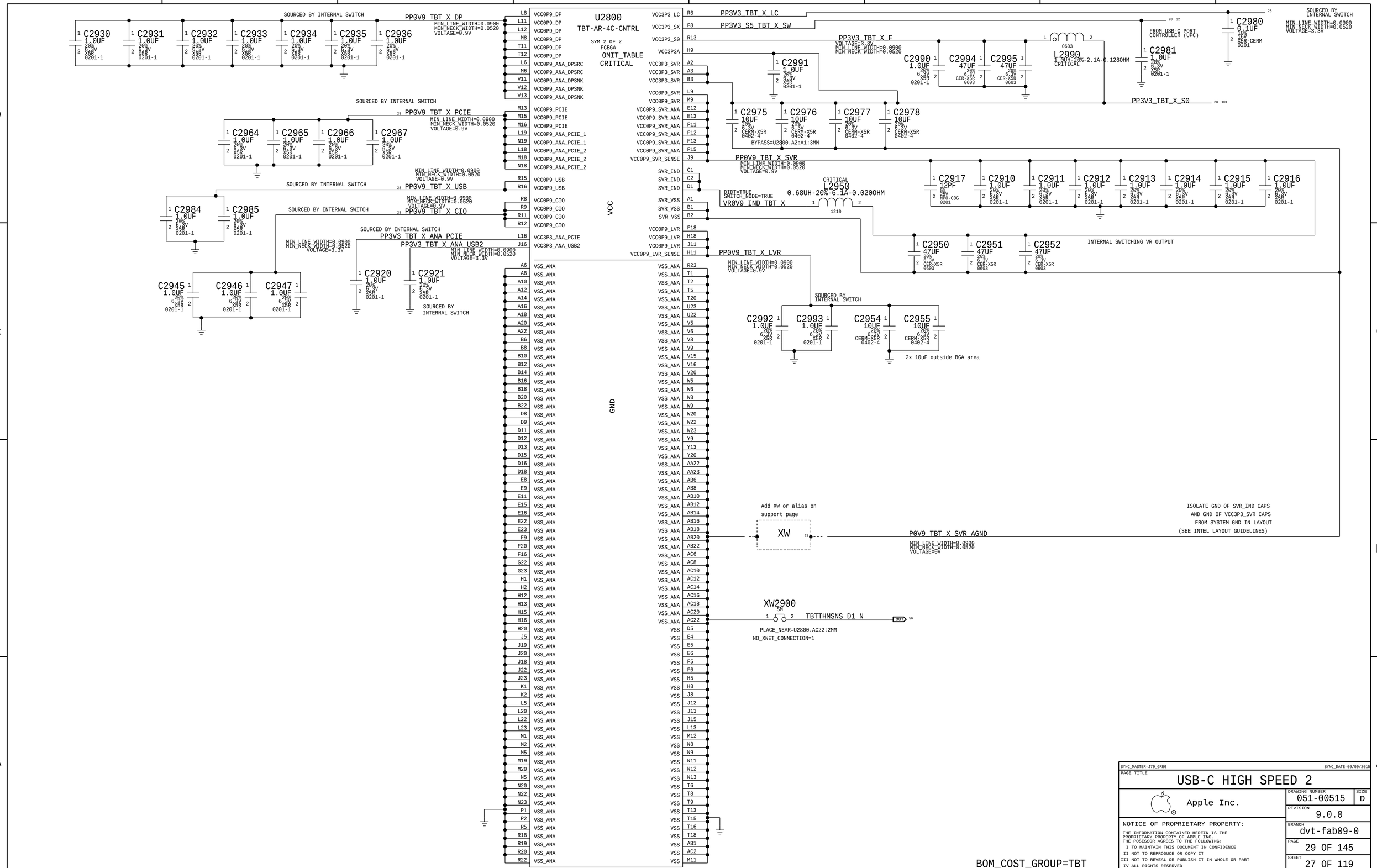

SYNC_MASTER=J79_GREG SYNC_DATE=09/09/2015

PAGE TITLE
USB-C HIGH SPEED 2

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D
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TMU CLKs

26 TBT_X_TMU_CLK_OUT — MAKE_BASE=TRUE — TBT_X_TMU_CLK_OUT
R3025 15 5% 1/20W MF 201 (PLACE_NEAR=U2800.V2:5mm)
TBT_T_TMU_CLK_IN — MAKE_BASE=TRUE — TBT_T_TMU_CLK_IN 92
R3024 100K 5% 1/20W MF 201

Ridge 0.9V SVR XW

27 P0V9_TBT_X_SVR_AGND — XW3000 SHORT-L6-SM (NO_XNET_CONNECTION=1)

DP SRC OPTIONS

IF DP SRC NOT USED

26 DP_X_SRC_HPD — R3040 1M 5% 1/20W MF 201

NC_DP_X_SRC_ML_P<0>	NC_DP_X_SRC_ML_P<0>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_X_SRC_ML_P<1>	NC_DP_X_SRC_ML_P<1>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_X_SRC_ML_P<2>	NC_DP_X_SRC_ML_P<2>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_X_SRC_ML_P<3>	NC_DP_X_SRC_ML_P<3>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_X_SRC_ML_N<0>	NC_DP_X_SRC_ML_N<0>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_X_SRC_ML_N<1>	NC_DP_X_SRC_ML_N<1>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_X_SRC_ML_N<2>	NC_DP_X_SRC_ML_N<2>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_X_SRC_ML_N<3>	NC_DP_X_SRC_ML_N<3>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_X_SRC_AUX_P	NC_DP_X_SRC_AUX_P	MAKE_BASE=TRUE NO_TEST=1
NC_DP_X_SRC_AUX_N	NC_DP_X_SRC_AUX_N	MAKE_BASE=TRUE NO_TEST=1

AR xtal

26 IN TBT_X_XTAL25M_OUT — R3007 0 5% 1/20W MF 201 — TBT_X_XTAL25M_OUT_R
R3006 1M 5% 1/20W MF 201 (NOSTUFF)
CRITICAL Y3000 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM
C3002 20PF 5% 25V C0G 0201
C3003 20PF 5% 25V C0G 0201
26 OUT TBT_X_XTAL25M_IN

X ACE-SMC I2C SERIES R'S

29 I2C_UPC_X_SDA2 — I2C_UPC_X_SDA2 (MAKE_BASE=TRUE) — 30 I2C_UPC_X_SDA2 — 26 I2C_UPC_X_SDA2
R3041 33 5% 1/20W MF 201 (PLACE_NEAR=U5000:5mm)
SMBUS_SMC_4_G3H_SDA — SMBUS_SMC_4_G3H_SDA 51

29 I2C_UPC_X_SCL2 — I2C_UPC_X_SCL2 (MAKE_BASE=TRUE) — 30 I2C_UPC_X_SCL2 — 28 I2C_UPC_X_SCL2
R3042 33 5% 1/20W MF 201 (PLACE_NEAR=U5000:5mm)
SMBUS_SMC_4_G3H_SCL — SMBUS_SMC_4_G3H_SCL 51

ACE A/B RPD STRAPPING

29 USBC_XA_CC1	USBC_XA_CC1 (MAKE_BASE=TRUE)	29 31 104
29 USBC_XA_CC2	USBC_XA_CC2 (MAKE_BASE=TRUE)	29 31 104
30 USBC_XB_CC1	USBC_XB_CC1 (MAKE_BASE=TRUE)	30 31 104
30 USBC_XB_CC2	USBC_XB_CC2	30 31 104

ACE PDs

33 28 UPC_X_5V_EN — R3032 100K 5% 1/20W MF 201

ACE Debug Support

29 UPC_XA_DBG_UART_TX — R3089 1 (OMIT NOSTUFF NONE NONE NONE 402) 2 — 29 UPC_XA_DBG_UART_RX
30 UPC_XB_DBG_UART_TX — R3088 1 (OMIT NOSTUFF NONE NONE NONE 402) 2 — 30 UPC_XB_DBG_UART_RX

USB2 AR PDs

26 USB_UPC_XA_P — R3020 0 5% 1/20W MF 201
26 USB_UPC_XA_N — R3021 0 5% 1/20W MF 201
26 USB_UPC_XB_P — R3022 0 5% 1/20W MF 201
26 USB_UPC_XB_N — R3023 0 5% 1/20W MF 201

GND ALIASES

29 GND, 30 GND, 96 95 30 29 GND, 29 GND, 29 GND, 29 GND
29 GND, 30 GND, 30 GND, 29 GND, 30 GND, 29 GND

NC ALIASES / NO TEST

30 IN NC_UPC_XB_I2C_ADDR (NO_TEST=1)

SIGNAL ALIASES

29 UPC_X_5V_EN	UPC_X_5V_EN (MAKE_BASE=TRUE)	28 33
30 UPC_X_5V_EN		
30 29 26 TBT_X_CIO_PWR_EN	TBT_X_CIO_PWR_EN (MAKE_BASE=TRUE)	13
30 29 26 TBT_X_USB_PWR_EN	TBT_X_USB_PWR_EN (MAKE_BASE=TRUE)	13
26 PM_BATLOW_L	PM_BATLOW_L (MAKE_BASE=TRUE)	14 48 94
92 26 SMC_PME_S4_DARK_L	SMC_PME_S4_DARK_L (MAKE_BASE=TRUE)	48 49 50
96 95 30 29 SMC_PME_S4_DARK_L		
28 26 UPC_X_SPI_CLK	UPC_X_SPI_CLK (MAKE_BASE=TRUE)	
28 26 UPC_X_SPI_CS_L	UPC_X_SPI_CS_L (MAKE_BASE=TRUE)	
28 26 UPC_X_SPI_MOSI	UPC_X_SPI_MOSI (MAKE_BASE=TRUE)	
28 26 UPC_X_SPI_MISO	UPC_X_SPI_MISO (MAKE_BASE=TRUE)	
94 92 UPC_T_SPI_CLK	UPC_T_SPI_CLK (MAKE_BASE=TRUE)	
94 92 UPC_T_SPI_CS_L	UPC_T_SPI_CS_L (MAKE_BASE=TRUE)	
94 92 UPC_T_SPI_MOSI	UPC_T_SPI_MOSI (MAKE_BASE=TRUE)	
94 92 UPC_T_SPI_MISO	UPC_T_SPI_MISO (MAKE_BASE=TRUE)	
94 92 26 JTAG_ISP_TDO	JTAG_ISP_TDO (MAKE_BASE=TRUE)	5 94
30 29 28 TBT_POC_RESET	TBT_POC_RESET (MAKE_BASE=TRUE)	16 94
106 34 DDI1_MUX_SEL	DDI1_MUX_SEL (MAKE_BASE=TRUE)	16
106 34 DDI2_MUX_SEL	DDI2_MUX_SEL (MAKE_BASE=TRUE)	16
16 TBT_X_CIO_PLUG_EVENT_L	TBT_X_CIO_PLUG_EVENT_L (MAKE_BASE=TRUE)	26 28
29 XDP_USB_EXTA_OC_L	XDP_USB_EXTA_OC_L (MAKE_BASE=TRUE)	5 17
30 XDP_USB_EXTB_OC_L	XDP_USB_EXTB_OC_L (MAKE_BASE=TRUE)	5 17
13 JTAG_TBT_X_TMS	JTAG_TBT_X_TMS (MAKE_BASE=TRUE)	26
94 13 JTAG_TBT_T_TMS	JTAG_TBT_T_TMS (MAKE_BASE=TRUE)	92 94
30 SMC_DEBUGPRT_TX_L	SMC_DEBUGPRT_TX_L (MAKE_BASE=TRUE)	48 49 104
30 SMC_DEBUGPRT_RX_L	SMC_DEBUGPRT_RX_L (MAKE_BASE=TRUE)	48 49 104
29 NC_USBC_XA_RESET_L	NC_USBC_XA_RESET_L (MAKE_BASE=TRUE)	102
15 USB_UPC_PCH_XA_N	USB_UPC_PCH_XA_N (MAKE_BASE=TRUE)	
29 USB_UPC_PCH_XA_N		
15 USB_UPC_PCH_XA_P	USB_UPC_PCH_XA_P (MAKE_BASE=TRUE)	
29 USB_UPC_PCH_XA_P		
15 USB_UPC_PCH_XB_N	USB_UPC_PCH_XB_N (MAKE_BASE=TRUE)	
30 USB_UPC_PCH_XB_N		
15 USB_UPC_PCH_XB_P	USB_UPC_PCH_XB_P (MAKE_BASE=TRUE)	
30 USB_UPC_PCH_XB_P		

POWER ALIASES

29 PP3V3_UPC_XA_LDO	PP3V3_UPC_XA_LDO (MAKE_BASE=TRUE)	29
29 PP3V3_UPC_XA_LDO		
29 PP3V3_UPC_XA_LDO		
26 PP3V3_UPC_XB_LDO	PP3V3_UPC_XB_LDO (MAKE_BASE=TRUE)	30
30 PP3V3_UPC_XB_LDO		
30 PP3V3_UPC_XB_LDO		
30 PP3V3_UPC_XB_LDO		
29 26 PP20V_USBC_XA_VBUS	PP20V_USBC_XA_VBUS (MAKE_BASE=TRUE)	31
30 26 PP20V_USBC_XB_VBUS	PP20V_USBC_XB_VBUS (MAKE_BASE=TRUE)	31
29 PP5V_S4_X_USBC	PP5V_S4_X_USBC (MAKE_BASE=TRUE) MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 VOLTAGE=5V	
30 PP5V_S4_X_USBC		
33 PP5V_S4_X_USBC		
101 27 PP3V3_TBT_X_S0	PP3V3_TBT_X_S0 (MAKE_BASE=TRUE) MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 VOLTAGE=3.3V	

AR/ACE SPI BUS SERIES R'S

26 TBT_X_SPI_CLK	R3094 100	TBT_X_SPI_CLK_DBG	28	USBC DEBUG CONN
	R3095 15	UPC_XB_SPI_CLK	IN 30	Ace
26 TBT_X_SPI_CS_L	R3096 15	UPC_XB_SPI_CS_L	IN 30	Ace
26 TBT_X_SPI_MOSI	R3097 15	UPC_XB_SPI_MOSI	IN 30	Ace
26 TBT_X_SPI_MISO	R3098 15	UPC_XB_SPI_MISO	OUT 30	Ace
ROM	R3090 15	UPC_X_SPI_CLK	IN 26 28	AR
	R3091 15	UPC_X_SPI_CS_L	IN 26 28	AR
	R3092 15	UPC_X_SPI_MOSI	IN 26 28	AR
	R3093 15	UPC_X_SPI_MISO	OUT 26 28	AR

TBT to ACE

TBT — Alpine Ridge U2800 (MASTER)

Pri ACE — U3100 (Write: 0x70 Read: 0x71)

Sec ACE — U3200 (Write: 0x7E Read: 0x7F)

MAKE_BASE=TRUE 26 28	I2C_TBT_X_SCL	I2C_TBT_X_SCL 29
MAKE_BASE=TRUE 26 28	I2C_TBT_X_SDA	I2C_TBT_X_SDA 29
MAKE_BASE=TRUE 26 28	I2C_TBT_XA_INT_L	I2C_TBT_XA_INT_L 29
MAKE_BASE=TRUE 26 28	I2C_TBT_XB_INT_L	I2C_TBT_XB_INT_L 30

RIDGE DEBUG CONN

J3001 505070-1220 M-ST-SM (USBC_DBG)

28 26 TBT_X_CIO_PLUG_EVENT_L	1	2	TBT_X_PCI_RESET_L 19 26
34 26 DP_X_SNK0_HPD	3	4	USBC_X_RESET_L 26 32
34 26 DP_X_SNK1_HPD	5	6	PP3V3_S5_TBT_X_SW 27 32
29 26 DP_XA_HPD	7	8	PP0V9_TBT_X_PCIE 27
30 29 28 TBT_POC_RESET	9	10	PP0V9_TBT_X_USB 27
27 PP3V3_TBT_X_LC	11	12	PP0V9_TBT_X_CIO 27
	15	16	

ACE DEBUG CONN

J3000 505070-1220 M-ST-SM (USBC_DBG)

28 26 I2C_TBT_XB_INT_L	1	2	I2C_TBT_XA_INT_L 26 28
28 I2C_UPC_X_SCL2	3	4	I2C_TBT_X_SDA 26 28
28 I2C_UPC_X_SDA2	5	6	I2C_TBT_X_SCL 26 28
94 51 48 SMC_USBC_INT_L	7	8	I2C_UPC_XA_DBG_CTL_SDA 29
28 TBT_X_SPI_CLK_DBG	9	10	I2C_UPC_XA_DBG_CTL_SCL 29
30 29 UPC_XA_UART_TX	11	12	UPC_XA_UART_RX 29 30
	15	16	

Ridge PCIE Caps

D2R

26 IN PCIE_TBT_X_D2R_C_P<0>	C3050 0.22UF (0201 X5R 6.3V 20% GND_VOID=TRUE)	PCIE_TBT_X_D2R_P<0>	OUT 15 105
26 IN PCIE_TBT_X_D2R_C_N<0>	C3051 0.22UF (0201 X5R 6.3V 20% GND_VOID=TRUE)	PCIE_TBT_X_D2R_N<0>	OUT 15 105
26 IN PCIE_TBT_X_D2R_C_P<1>	C3052 0.22UF (0201 X5R 6.3V 20% GND_VOID=TRUE)	PCIE_TBT_X_D2R_P<1>	OUT 15
26 IN PCIE_TBT_X_D2R_C_N<1>	C3053 0.22UF (0201 X5R 6.3V 20% GND_VOID=TRUE)	PCIE_TBT_X_D2R_N<1>	OUT 15
26 IN PCIE_TBT_X_D2R_C_P<2>	C3054 0.22UF (0201 X5R 6.3V 20% GND_VOID=TRUE)	PCIE_TBT_X_D2R_P<2>	OUT 15
26 IN PCIE_TBT_X_D2R_C_N<2>	C3055 0.22UF (0201 X5R 6.3V 20% GND_VOID=TRUE)	PCIE_TBT_X_D2R_N<2>	OUT 15
26 IN PCIE_TBT_X_D2R_C_P<3>	C3056 0.22UF (0201 X5R 6.3V 20% GND_VOID=TRUE)	PCIE_TBT_X_D2R_P<3>	OUT 15
26 IN PCIE_TBT_X_D2R_C_N<3>	C3057 0.22UF (0201 X5R 6.3V 20% GND_VOID=TRUE)	PCIE_TBT_X_D2R_N<3>	OUT 15

R2D

15 IN PCIE_TBT_X_R2D_C_P<0>	C3040 0.22UF (0201 X5R 6.3V 20% GND_VOID=TRUE)	PCIE_TBT_X_R2D_P<0>	OUT 26
15 IN PCIE_TBT_X_R2D_C_N<0>	C3041 0.22UF (0201 X5R 6.3V 20% GND_VOID=TRUE)	PCIE_TBT_X_R2D_N<0>	OUT 26
15 IN PCIE_TBT_X_R2D_C_P<1>	C3042 0.22UF (0201 X5R 6.3V 20% GND_VOID=TRUE)	PCIE_TBT_X_R2D_P<1>	OUT 26
15 IN PCIE_TBT_X_R2D_C_N<1>	C3043 0.22UF (0201 X5R 6.3V 20% GND_VOID=TRUE)	PCIE_TBT_X_R2D_N<1>	OUT 26
15 IN PCIE_TBT_X_R2D_C_P<2>	C3044 0.22UF (0201 X5R 6.3V 20% GND_VOID=TRUE)	PCIE_TBT_X_R2D_P<2>	OUT 26
15 IN PCIE_TBT_X_R2D_C_N<2>	C3045 0.22UF (0201 X5R 6.3V 20% GND_VOID=TRUE)	PCIE_TBT_X_R2D_N<2>	OUT 26
15 IN PCIE_TBT_X_R2D_C_P<3>	C3046 0.22UF (0201 X5R 6.3V 20% GND_VOID=TRUE)	PCIE_TBT_X_R2D_P<3>	OUT 26
15 IN PCIE_TBT_X_R2D_C_N<3>	C3047 0.22UF (0201 X5R 6.3V 20% GND_VOID=TRUE)	PCIE_TBT_X_R2D_N<3>	OUT 26

Ridge PDs

26 DP_X_SNK0_DDC_CLK (MAKE_BASE=TRUE)	R3067 100K 5% 1/20W MF 201	DP_X_SNK0_DDC_CLK
26 DP_X_SNK0_DDC_DATA (MAKE_BASE=TRUE)	R3068 100K 5% 1/20W MF 201	DP_X_SNK0_DDC_DATA
26 DP_X_SNK1_DDC_CLK (MAKE_BASE=TRUE)	R3069 100K 5% 1/20W MF 201	DP_X_SNK1_DDC_CLK
26 DP_X_SNK1_DDC_DATA (MAKE_BASE=TRUE)	R3070 100K 5% 1/20W MF 201	DP_X_SNK1_DDC_DATA

FUSES FOR UPC

PLACE_NEAR=Q3100:5MM
CRITICAL 0603 F3000 6AMP-32V-0.00950HM
29 28 PP20V_USBC_XA_VBUS — 1 — 2 — PP20V_USBC_XA_VBUS_F 29

PLACE_NEAR=Q3200:5MM
CRITICAL 0603 740S0135 F3001 6AMP-32V-0.00950HM
30 28 PP20V_USBC_XB_VBUS — 1 — 2 — PP20V_USBC_XB_VBUS_F 30

DCI ALIASES

DCI PCH USB3

15 IN USB3_EXTA_R2D_C_P	C3020 0.1UF (10% 16V X5R-CERM 0201)	USB3_EXTA_D2R_P (MAKE_BASE=TRUE)	IN 29
15 OUT USB3_EXTA_D2R_N		USB3_EXTA_D2R_N (MAKE_BASE=TRUE)	IN 29
15 IN USB3_EXTA_R2D_C_N	C3021 0.1UF (10% 16V X5R-CERM 0201)	USB3_EXTA_R2D_P (MAKE_BASE=TRUE)	OUT 29
		USB3_EXTA_R2D_N	OUT 29

DCI Ace

BOM_COST_GROUP=TBT

PAGE TITLE	USB-C Support
Apple Inc.	DRAWING NUMBER 051-00515 SIZE D
	REVISION 9.0.0
	BRANCH dvt-fab09-0
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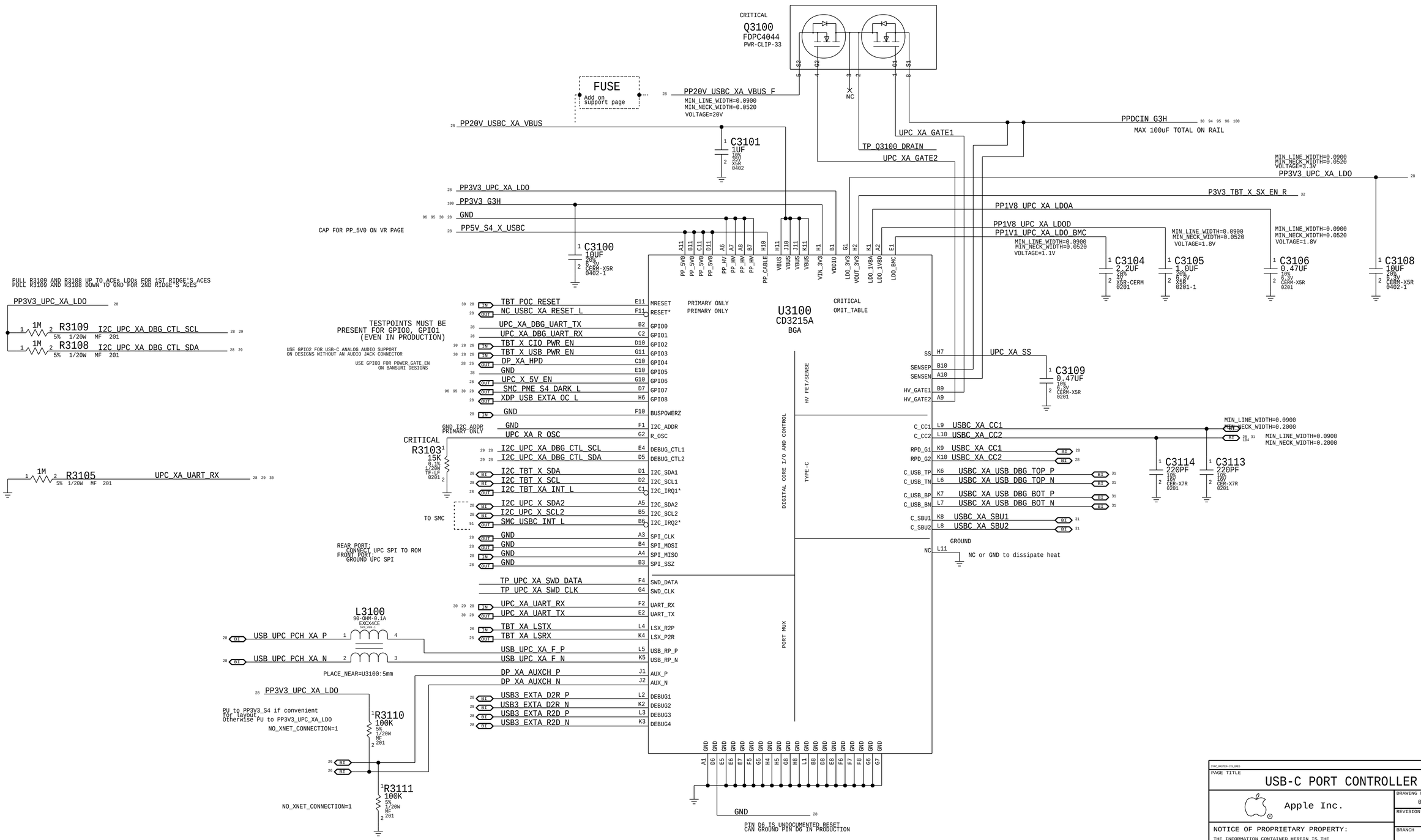
	SHEET 28 OF 119

PRIMARY ACE USB-C PORT CONTROLLER (UPC)



BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C PORT CONTROLLER A

Apple Inc.

DRAWING NUMBER	051-00515
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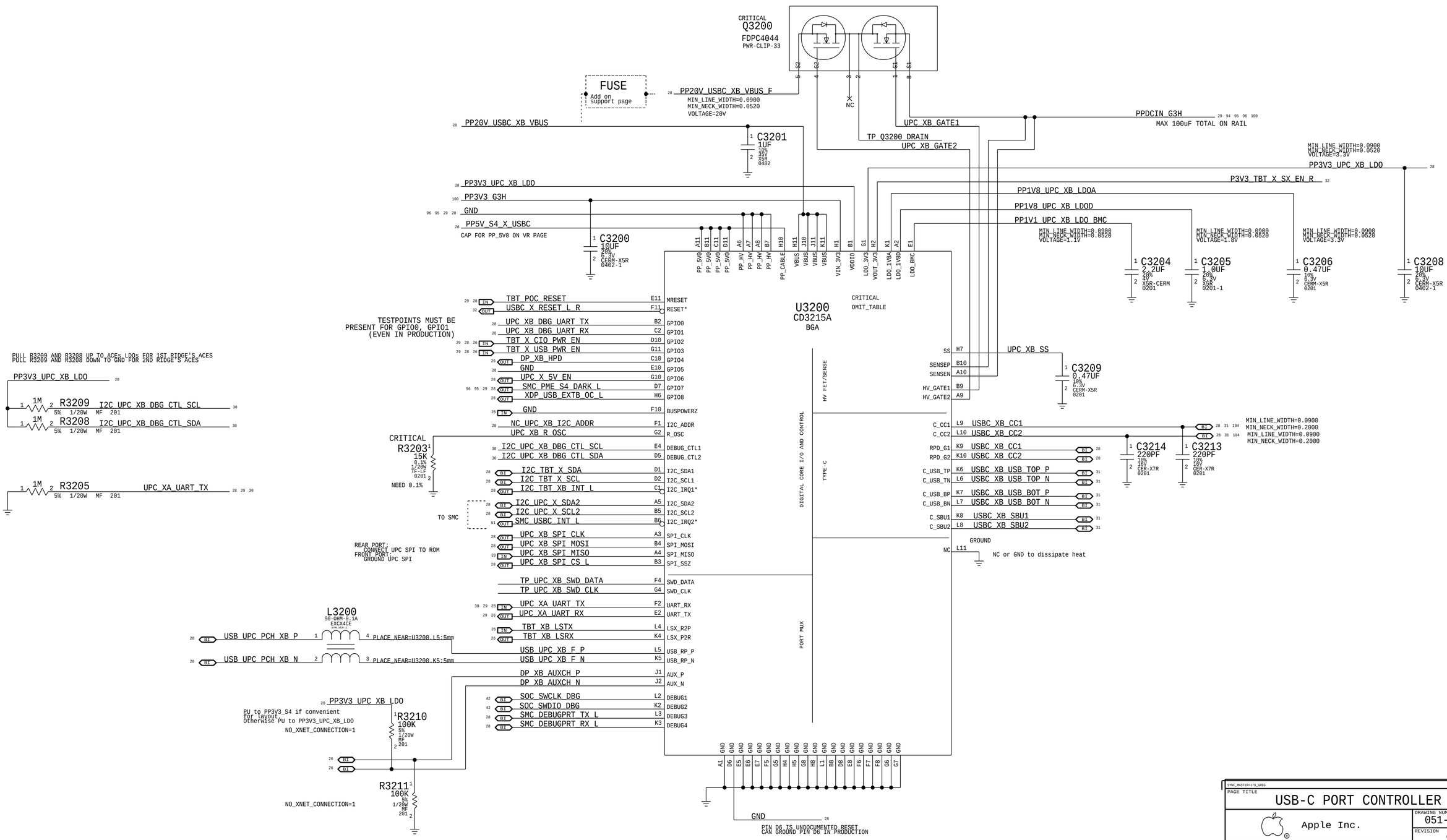
SECONDARY ACE USB-C PORT CONTROLLER (UPC)



BOM_COST_GROUP=USB-C

SYNC_MASTER=J79_GREG SYNC_DATE=02/28/2018

PAGE TITLE
USB-C PORT CONTROLLER B

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D
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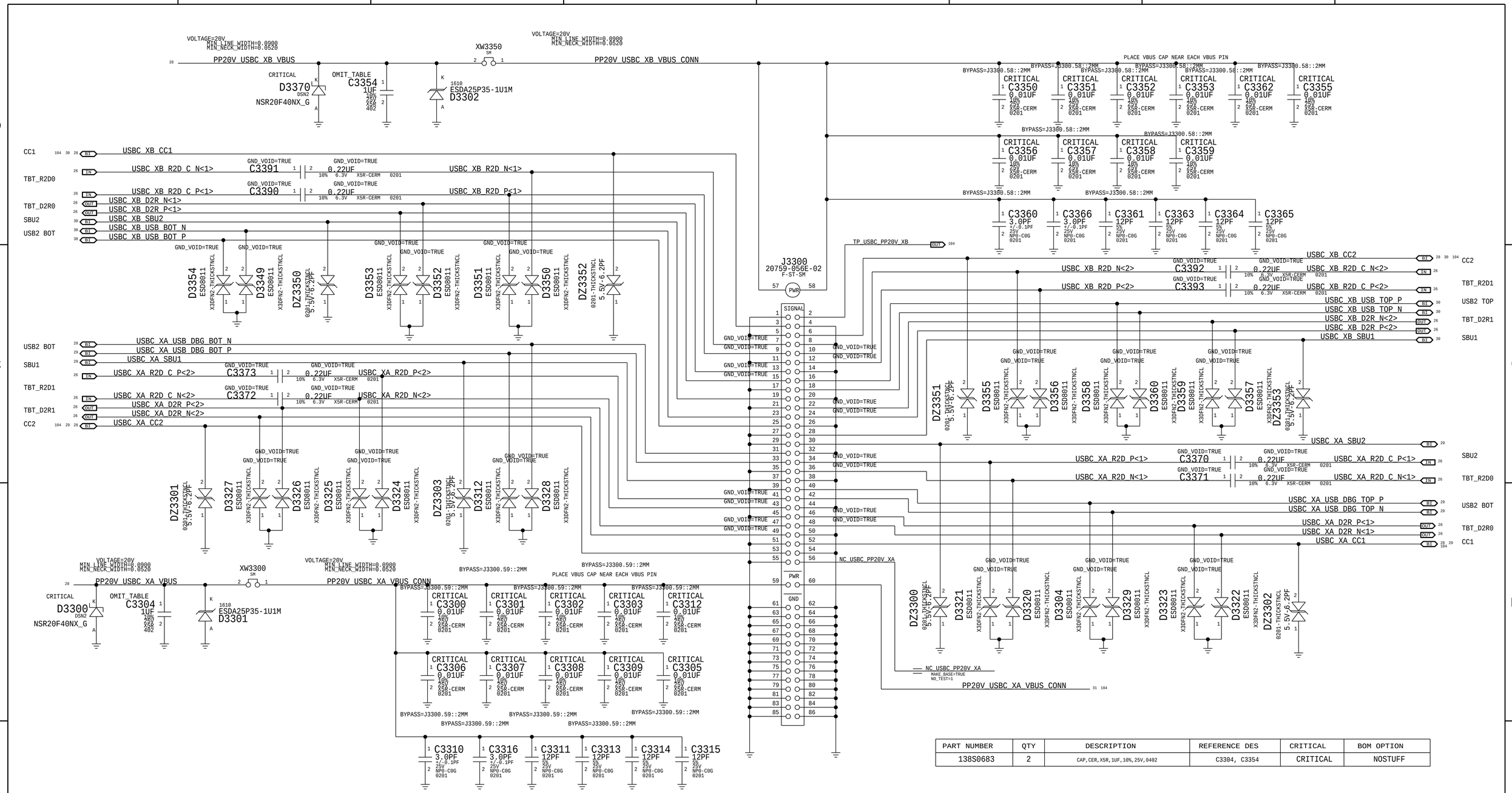

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0683	2	CAP,CER,X5R,1UF,10%,25V,0402	C3304, C3354	CRITICAL	NOSTUFF

LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE
USB-C CONNECTOR A

Apple Inc.

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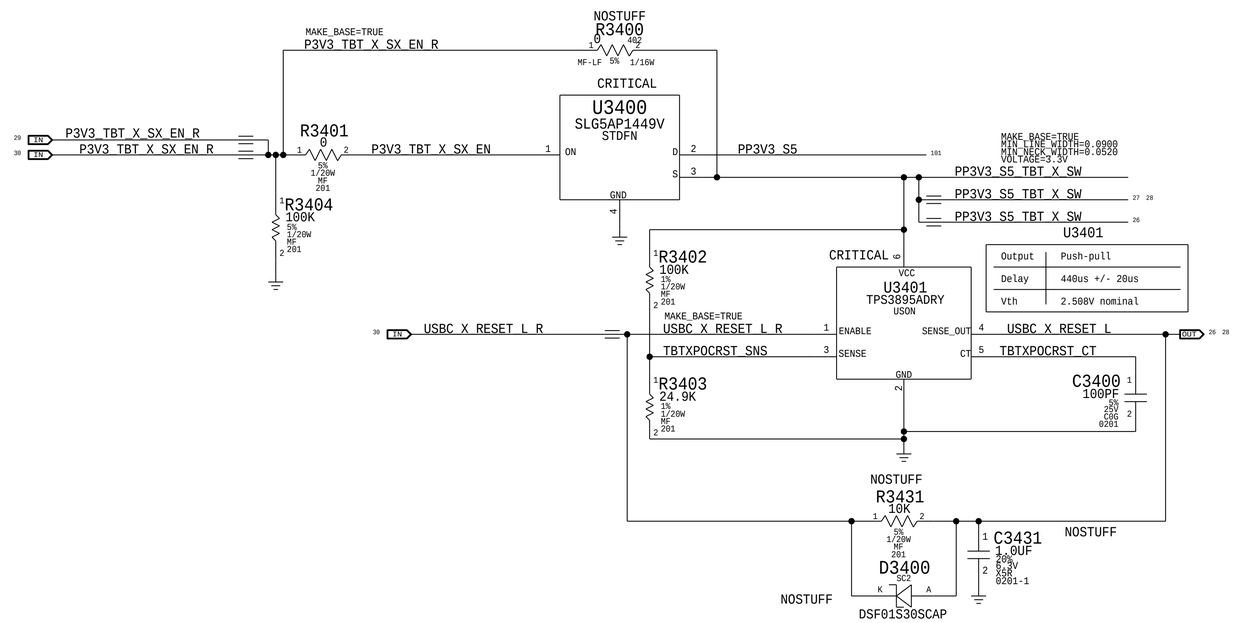
TBT X "POC" Power-up Reset



BOM_COST_GROUP=USB-C

DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17:12:24 2015
SYNC_MASTER=J79_GREG SYNC_DATE=03/24/2016

PAGE TITLE
USB-C CONNECTOR B

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D
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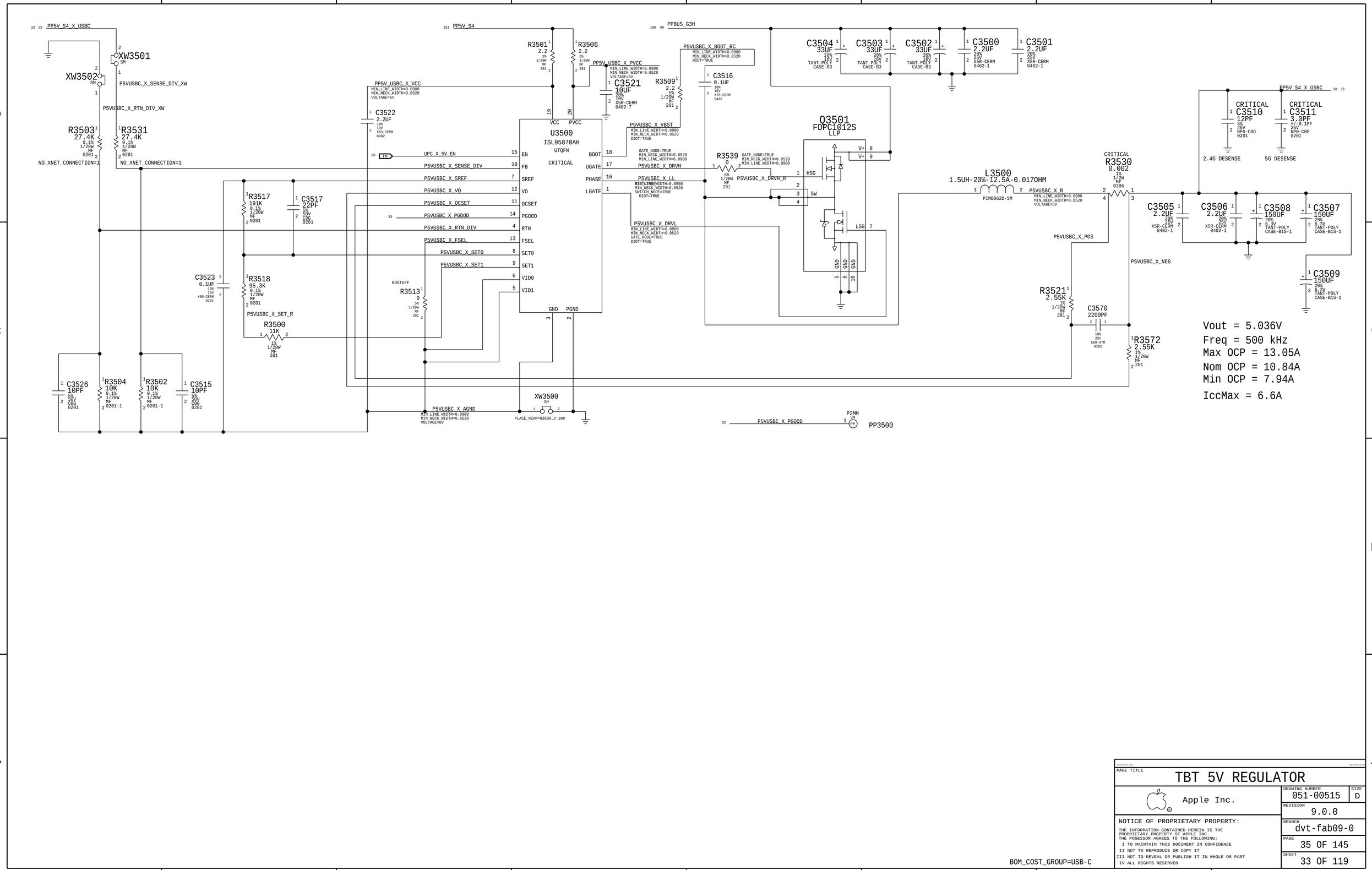

PAGE TITLE

TBT 5V REGULATOR

Apple Inc.

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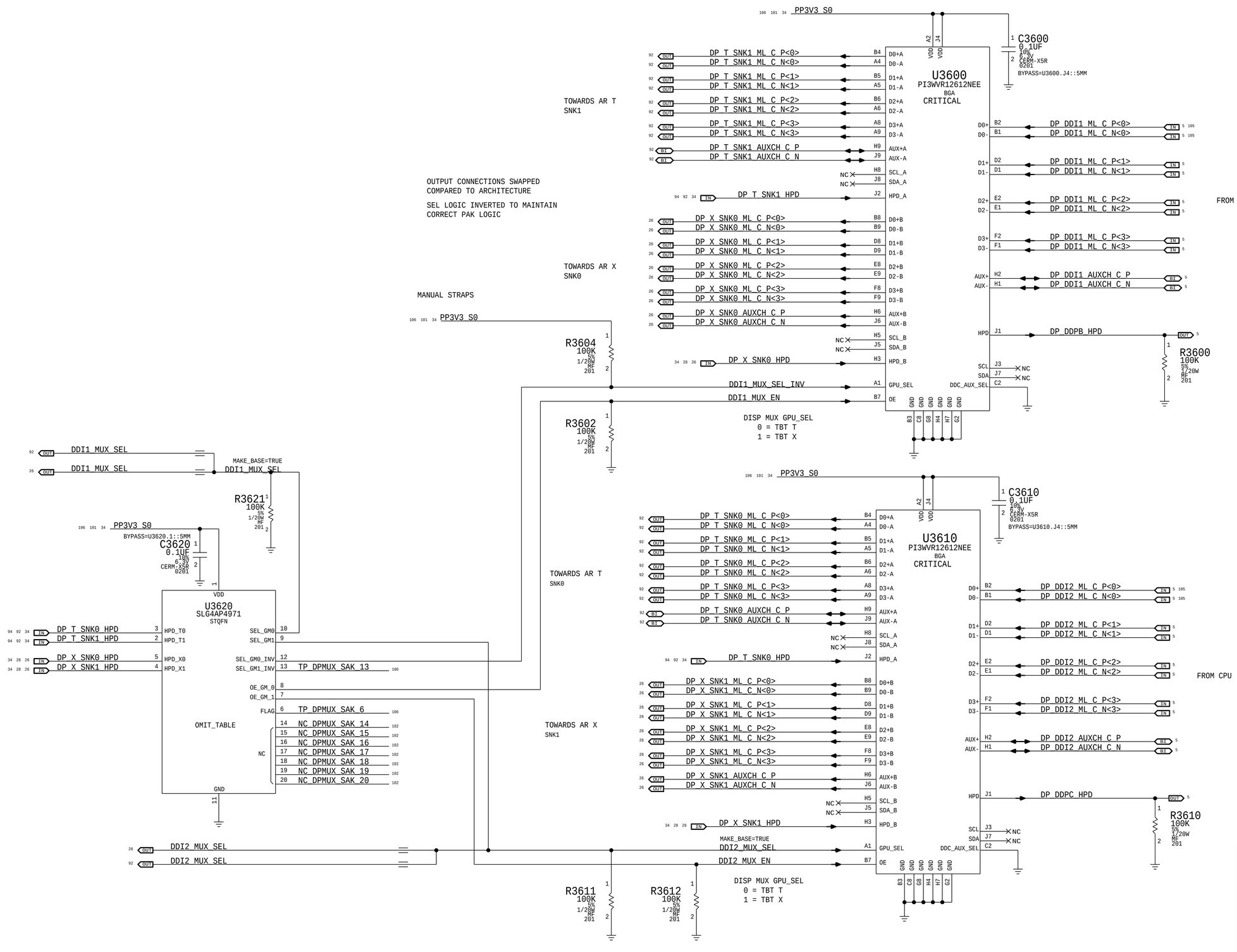

PAGE TITLE

Display Mux

Apple Inc.

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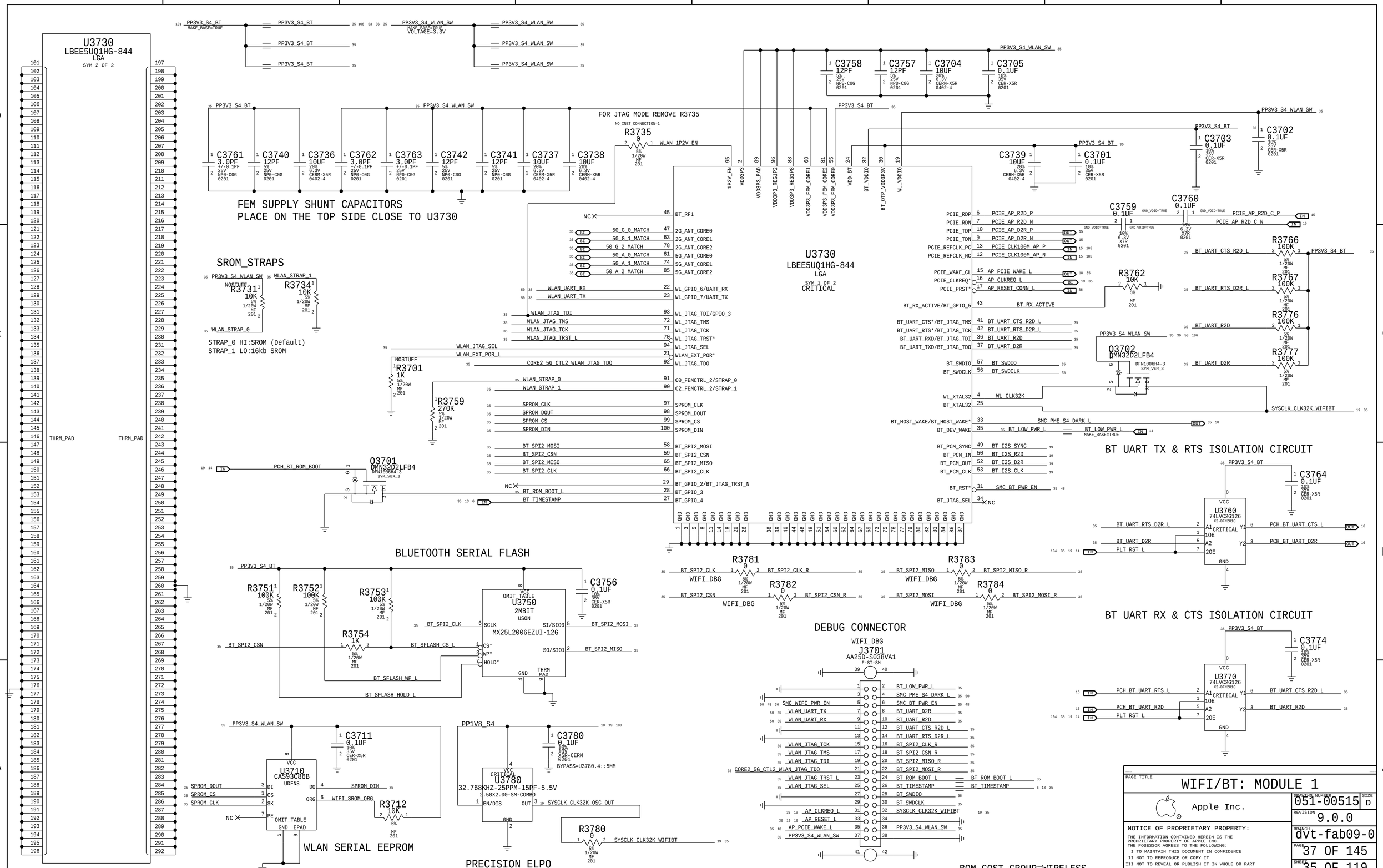
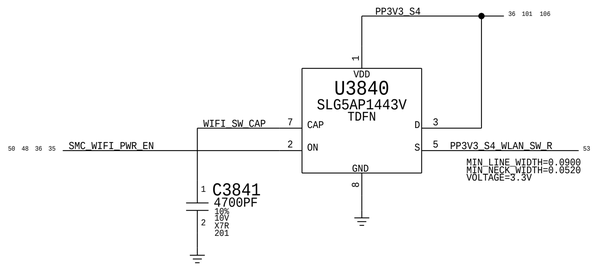
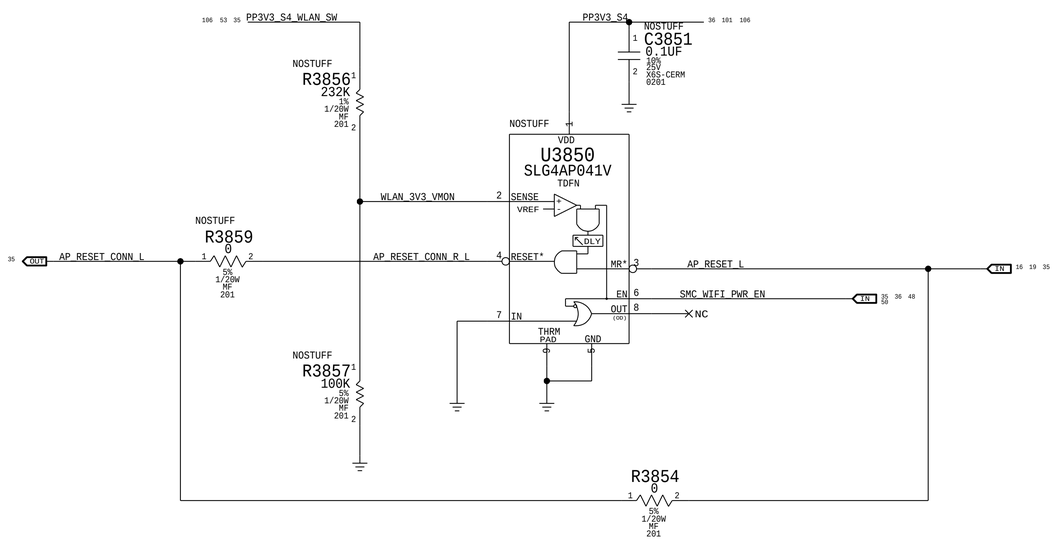


WLAN Power Switch

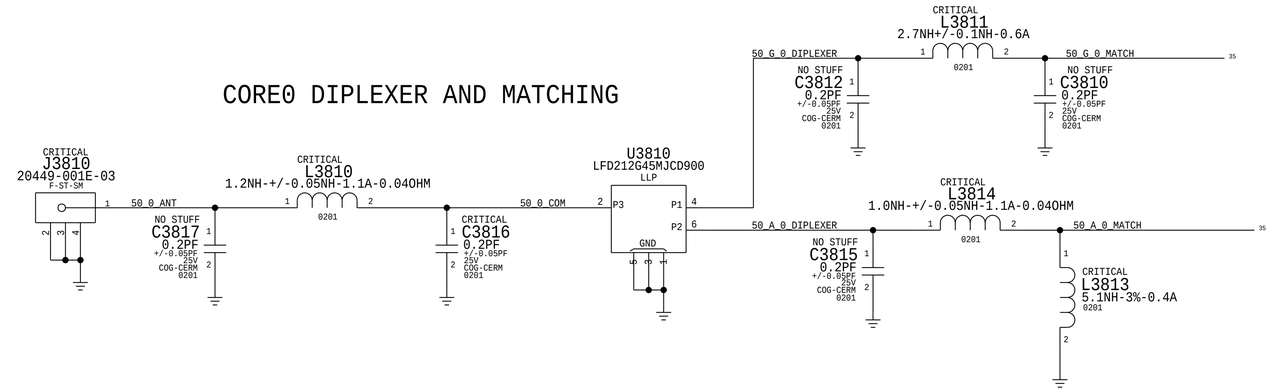


Supervisor & CLKREQ# Isolation

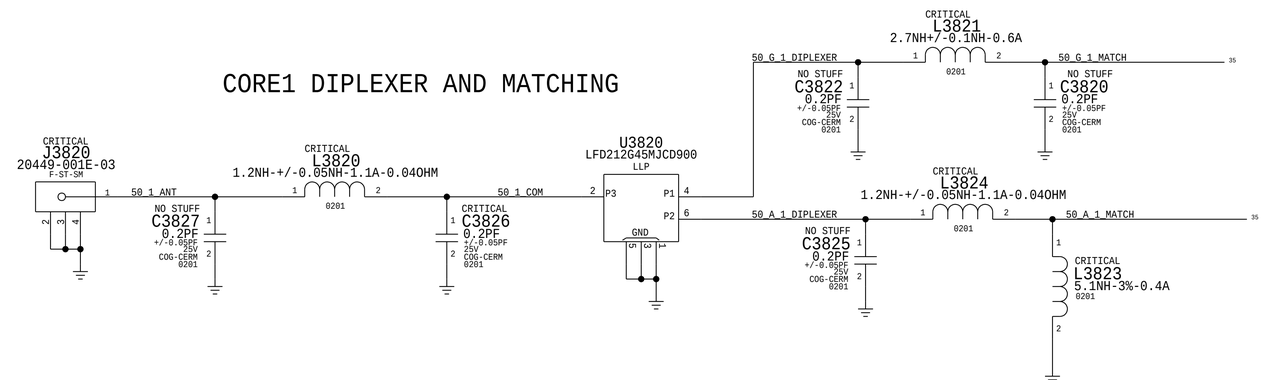
Delay = 130ms +/- 20%



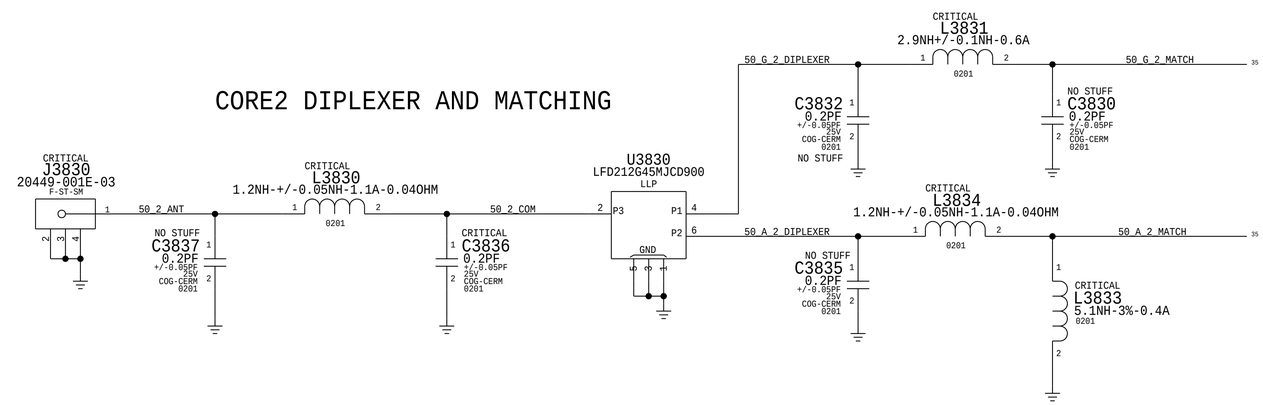
CORE0 DIPLEXER AND MATCHING



CORE1 DIPLEXER AND MATCHING



CORE2 DIPLEXER AND MATCHING



BOM_COST_GROUP=WIRELESS

SYNC_MASTER=J79_METE SYNC_DATE=03/02/2016

PAGE TITLE

WIFI/BT: MODULE 2

Apple Inc.

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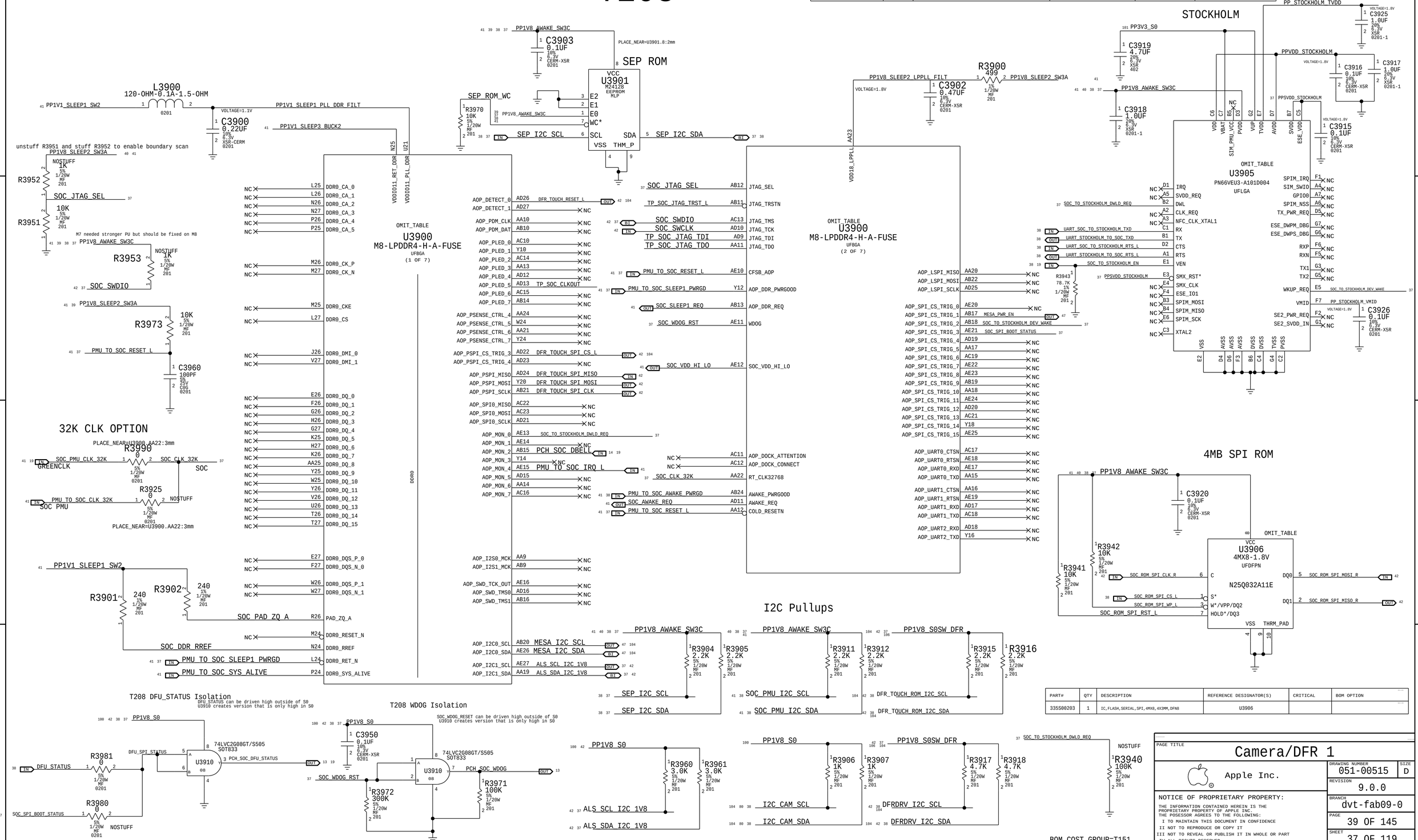
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S00135	1	IC,M8+512MB 20NM DDR,A12,S,SCK,BGA700	U3900	CRITICAL	

T208

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00147	1	IC,RTM2,DEV,PN549A1,P61D0	U3905	CRITICAL	SE:DEV
338S00097	1	IC,RTM2,MP,PN549A1,P61D0	U3905	CRITICAL	SE:PROD



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00203	1	IC,FLASH,SERIAL,SPI,4MX8,4X3MM,DFN8	U3906		

PAGE TITLE: Camera/DFR 1

Apple Inc.

DRAWING NUMBER: 051-00515 SIZE: D

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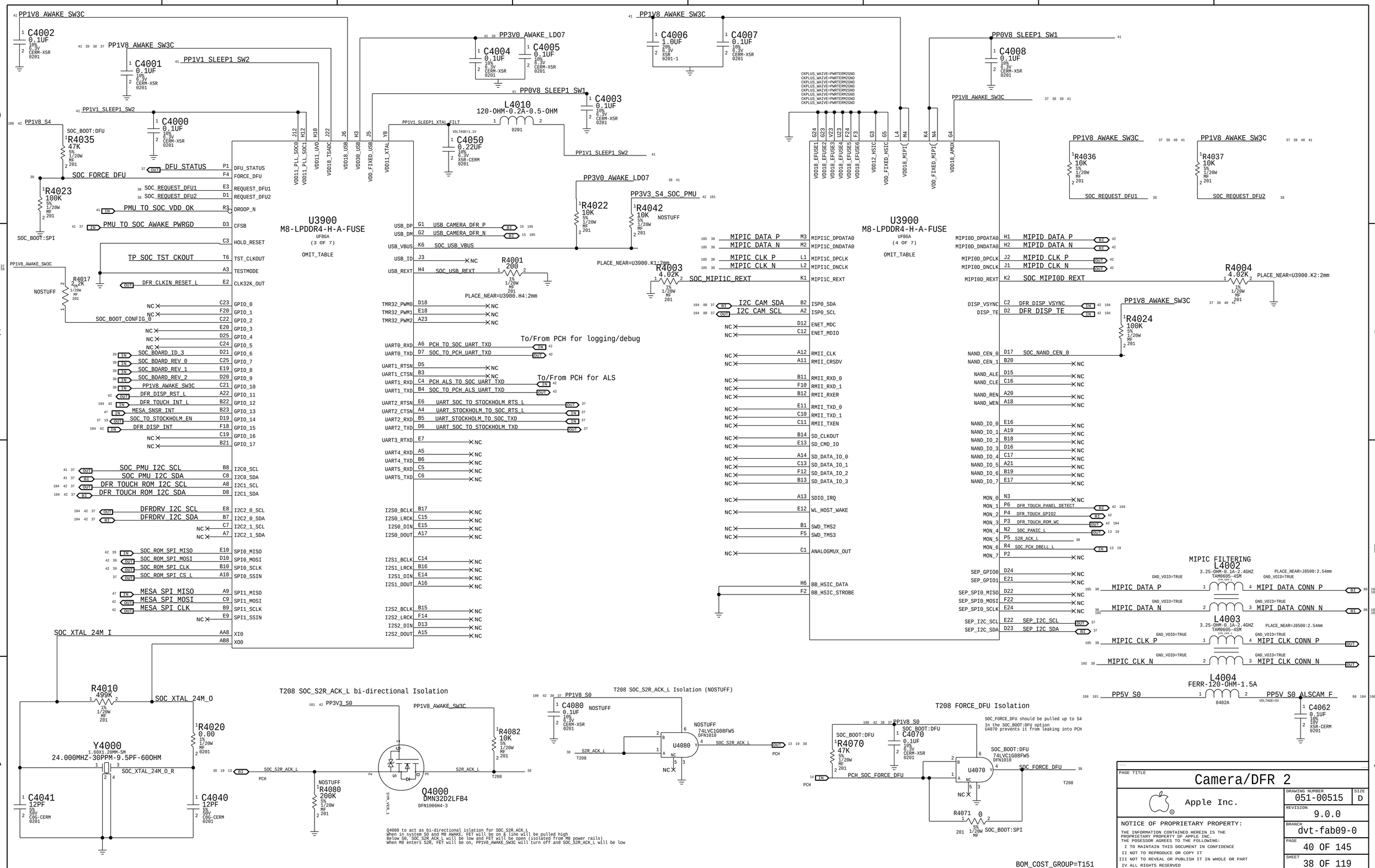
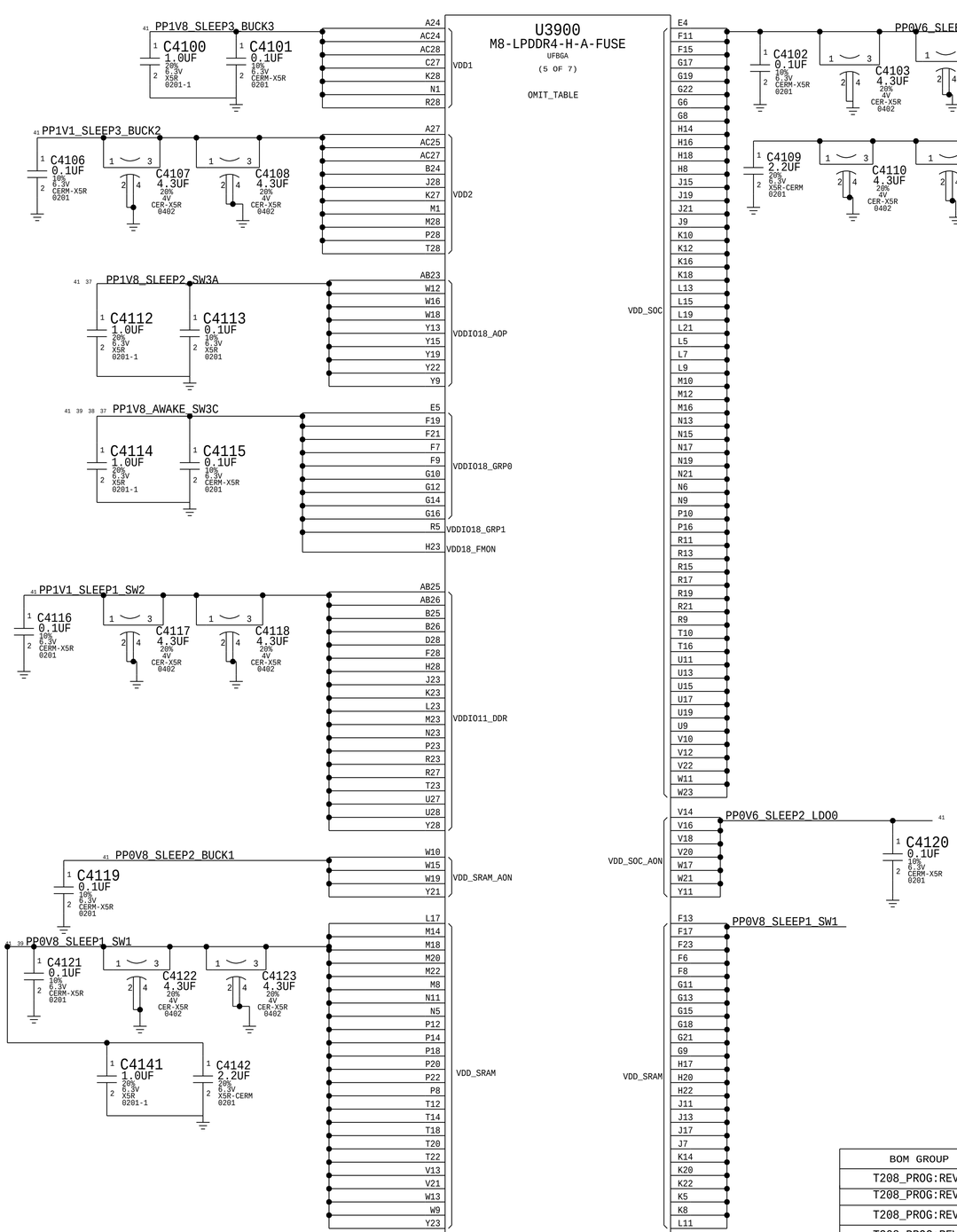
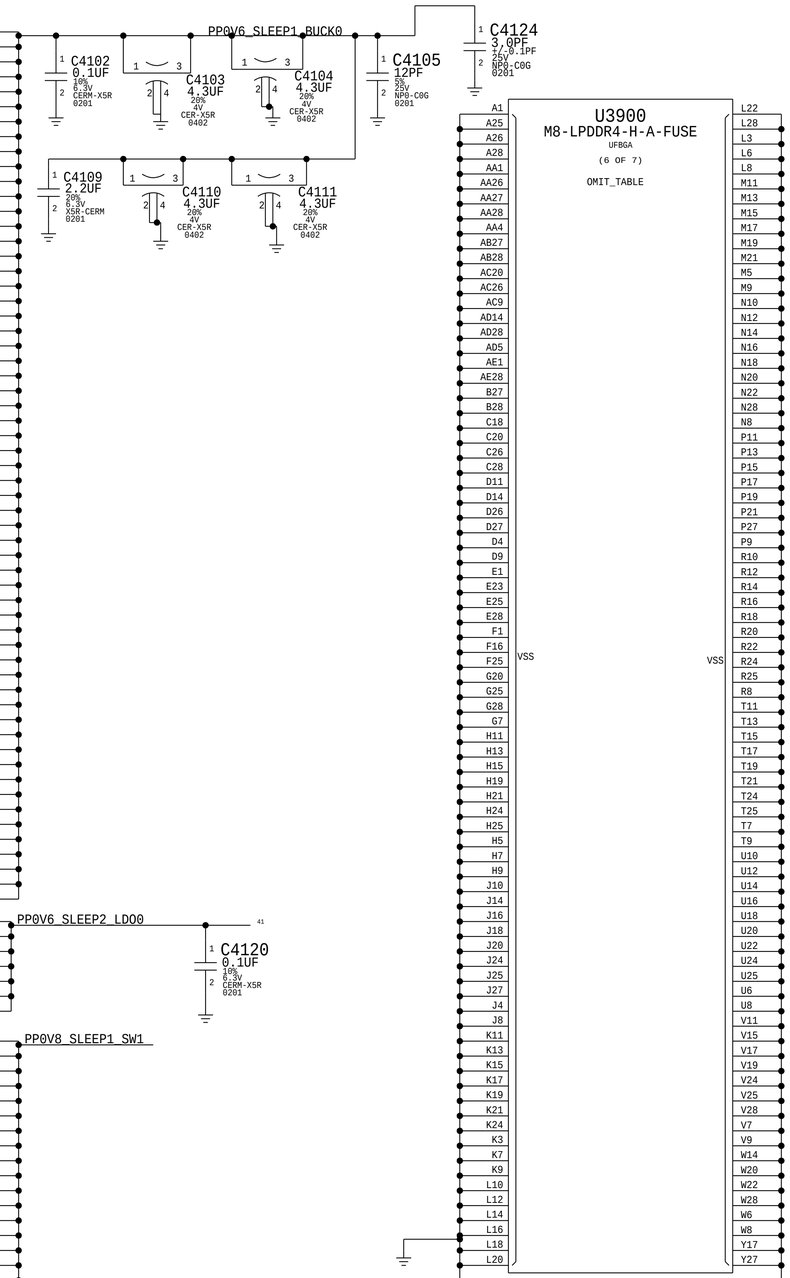
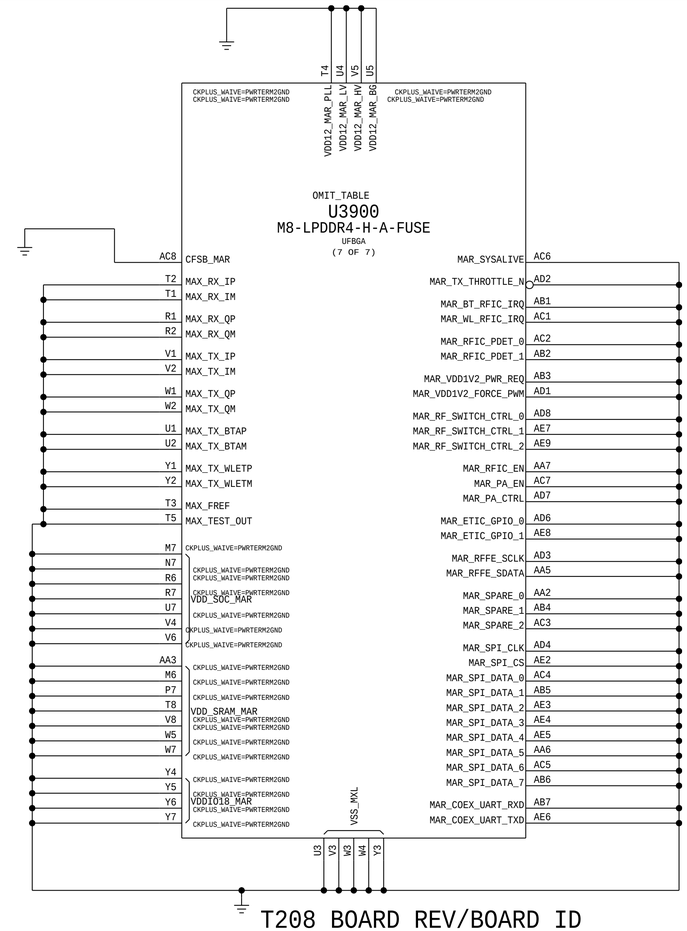




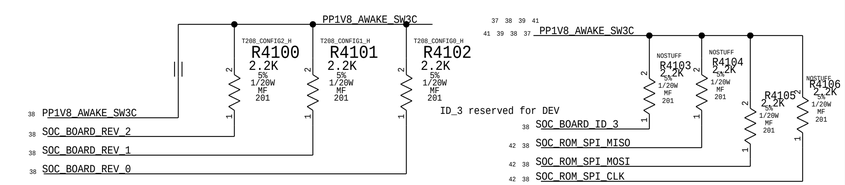




T208 BOARD REV/BOARD ID

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ
4. DISABLE PD AND ENABLE PU



BOARD REV[3:0]	MODE
1111	T208_Rev0 (X362 P0)
1110	T208_Rev1 (X363 P0)
1101	T208_Rev2 (X362 P1)
1100	T208_Rev3 (X362 P2)
1011	T208_Rev4 (X363 P2/X362 localEVT)
1010	T208_Rev5 (X363 EVT/X362 EVT1)

BOARD ID[3:0]	MODE
1XXX	T202 DEV
0010	T208

BOM GROUP	BOM OPTIONS
T208_PROG:REV0	T208_CONFIG2_H,T208_CONFIG1_H,T208_CONFIG0_H
T208_PROG:REV1	T208_CONFIG2_H,T208_CONFIG1_H
T208_PROG:REV2	T208_CONFIG2_H,T208_CONFIG0_H
T208_PROG:REV3	T208_CONFIG2_H
T208_PROG:REV4	T208_CONFIG1_H, T208_CONFIG0_H
T208_PROG:REV5	T208_CONFIG1_H

BOM_COST_GROUP=T151

PAGE TITLE: Camera/DFR 3

Apple Inc.

DRAWING NUMBER: 051-00515 SIZE: D

REVISION: 9.0.0

BRANCH: dvt-fab09-0

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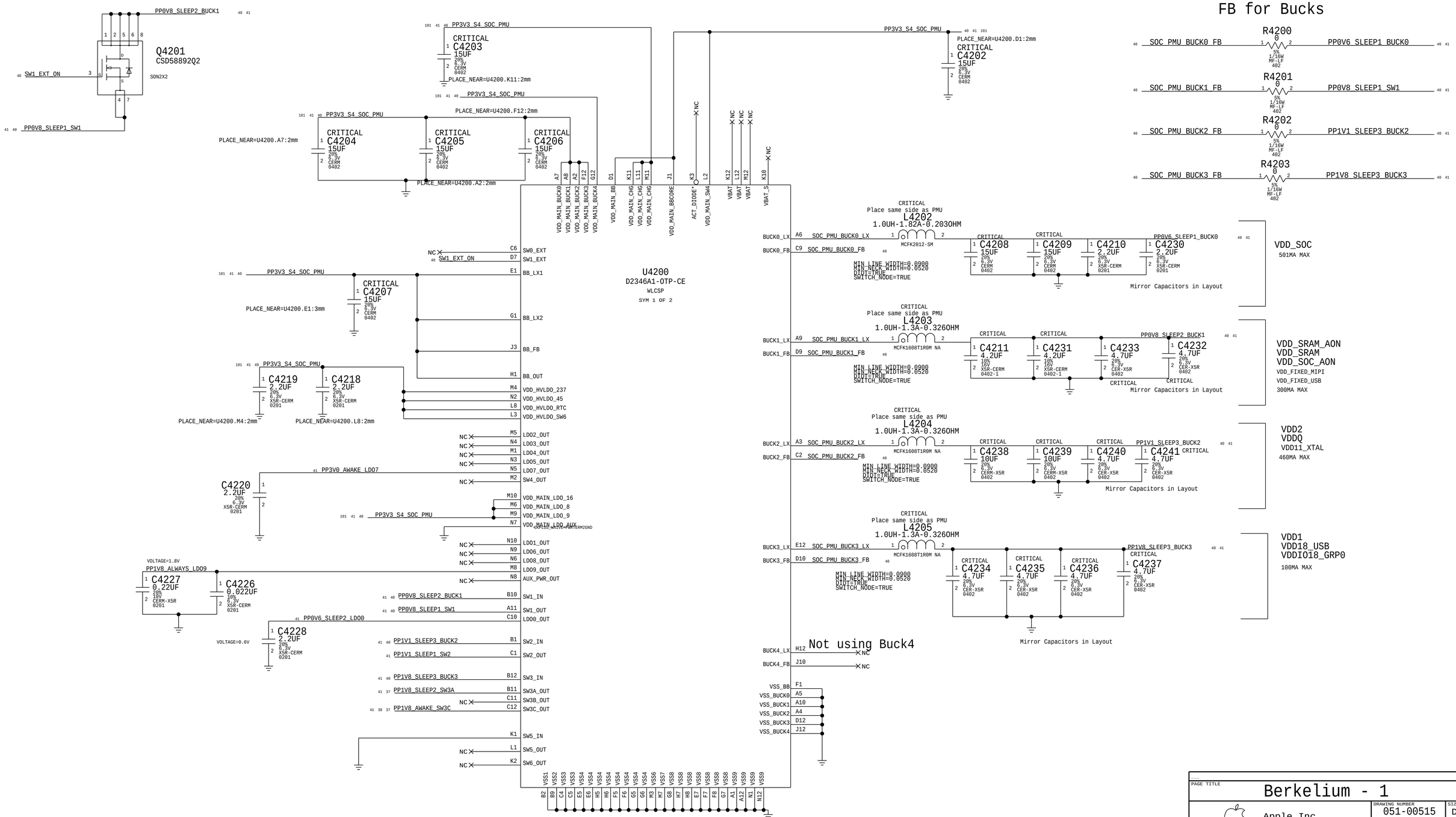
Berkelium



BOM_COST_GROUP=T151

PAGE TITLE	Berkelium - 1
	Apple Inc.
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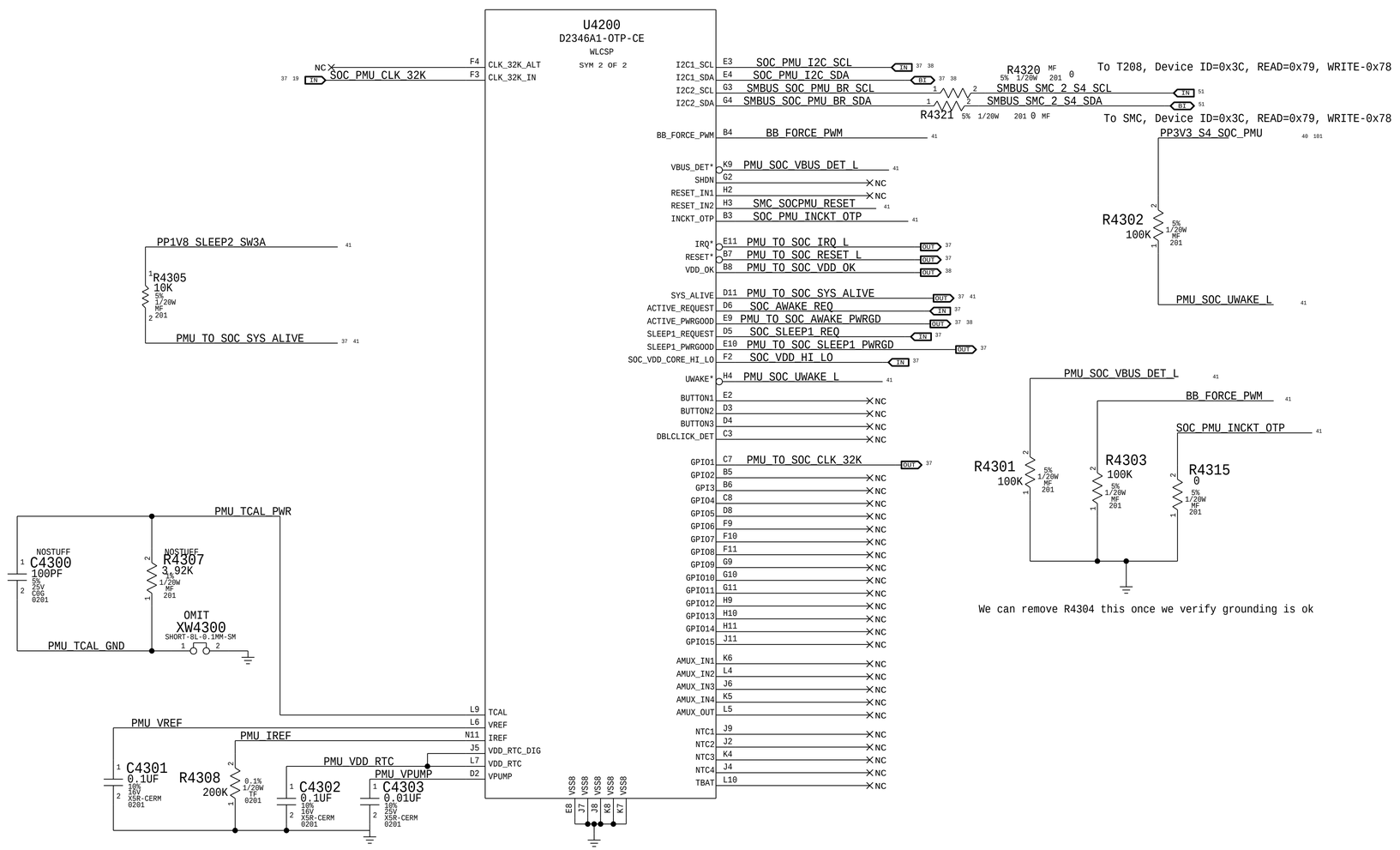
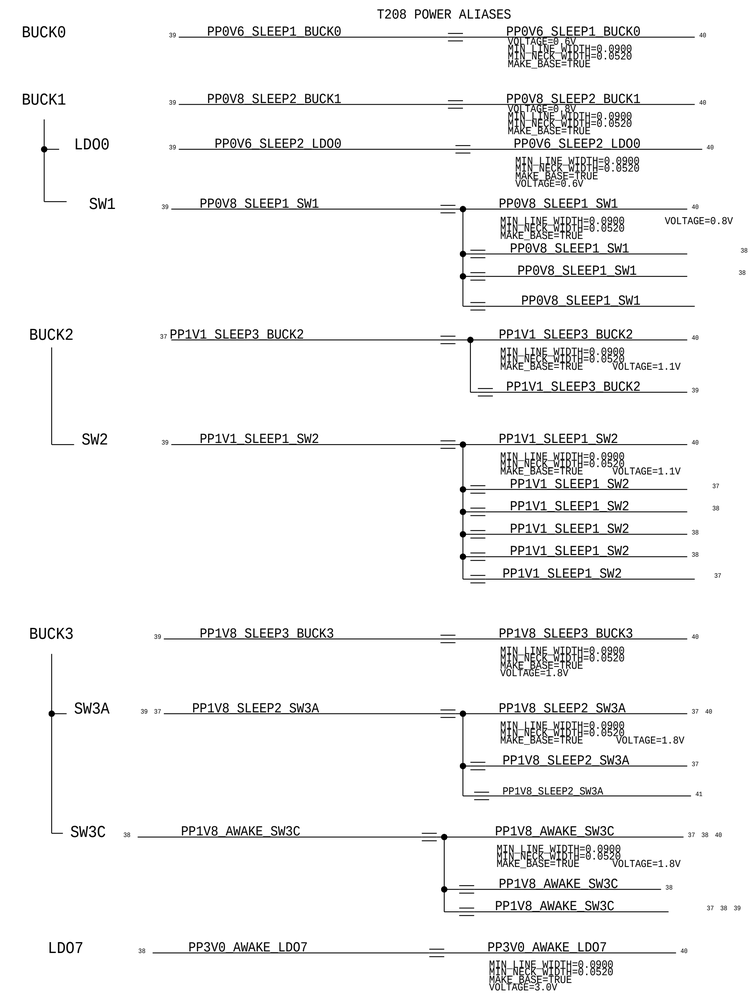
Berkelium - 2





Signal Aliases

SMC_SOCPMU_RESET — SMC_SOCPMU_RESET (MAKE_BASE=TRUE)

BOM_COST_GROUP=T151

PAGE TITLE	Berkelium - 2
	Apple Inc.
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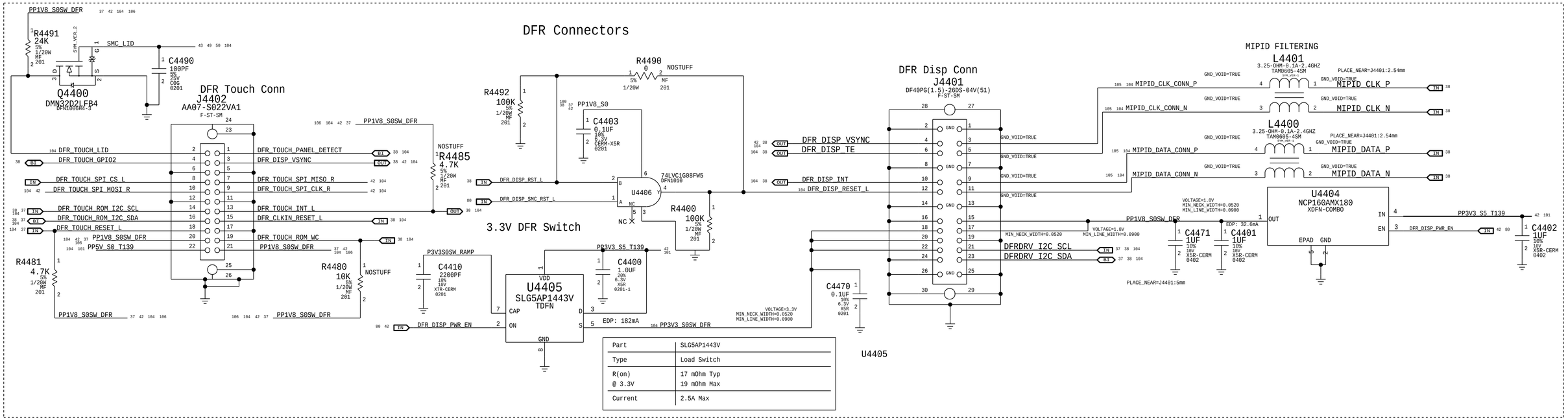
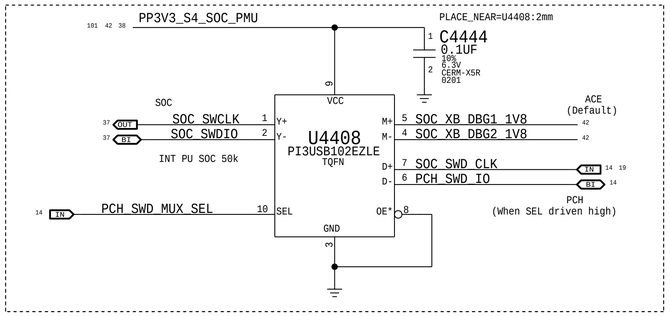
T208 Support



Part	SLG5AP1443V
Type	Load Switch
R(on) @ 3.3V	17 mOhm Typ 19 mOhm Max
Current	2.5A Max

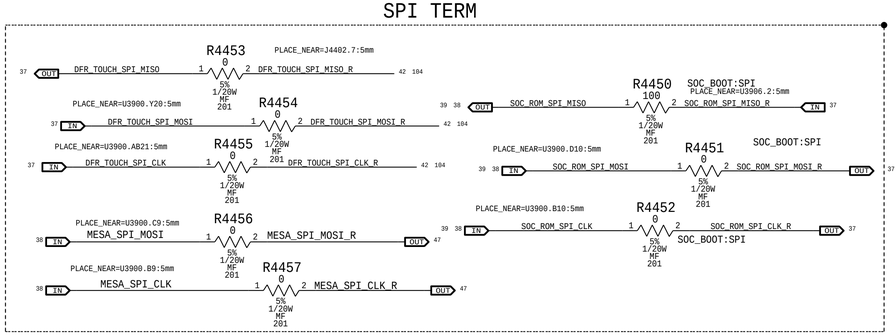
SWD DEBUG MUX



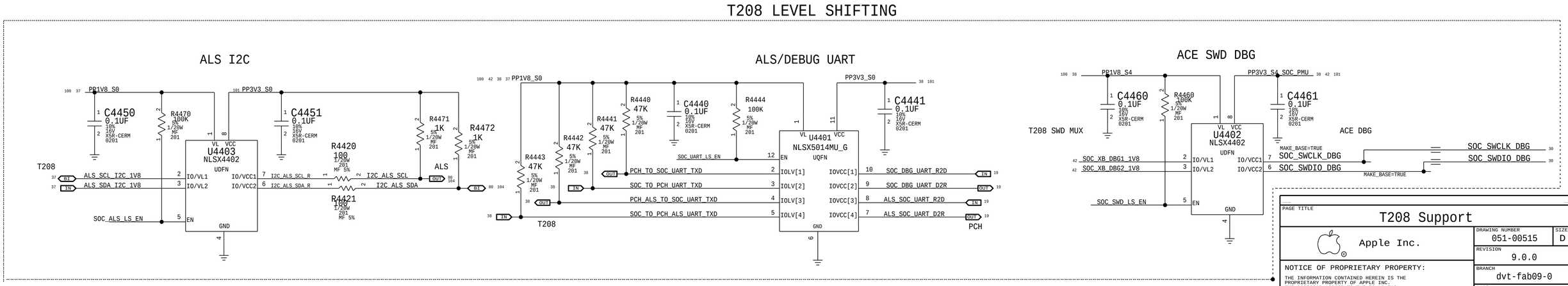
T208 I2C Mapping

Bus	Device	7-bit Address	8-bit Address Read	8-bit Address Write
AP0	PMU	0011110 (0x3C)	0x79	0x78
AP1	Touch EEPROM	1010000 (0x50)	0xA1	0xA0
AP2_0	Tesla	1010100 (0x4C)	0x99	0x98
AOP0	Mesa EEPROM	101000x (0x50/0x51)	0xA1/A3	0xA0/A2
AOP1	ALS	0111001 (0x39)	0x73	0x72
SEP	M34128 EEPROM	1010001 (0x51)	0xA3	0xA2

SPI TERM



T208 LEVEL SHIFTING



BOM_COST_GROUP=T151

PAGE TITLE	T208 Support
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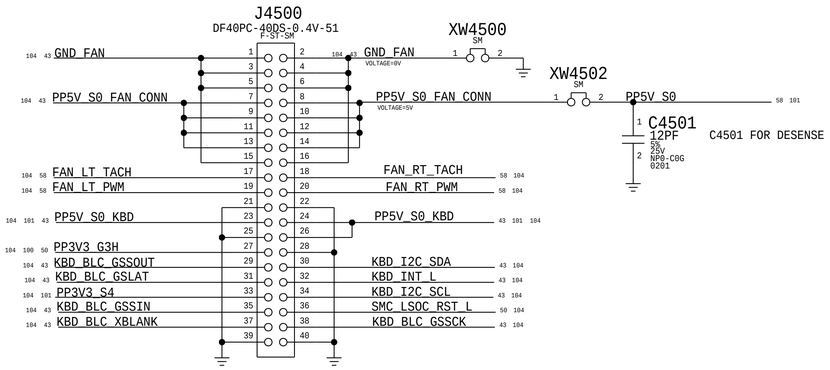
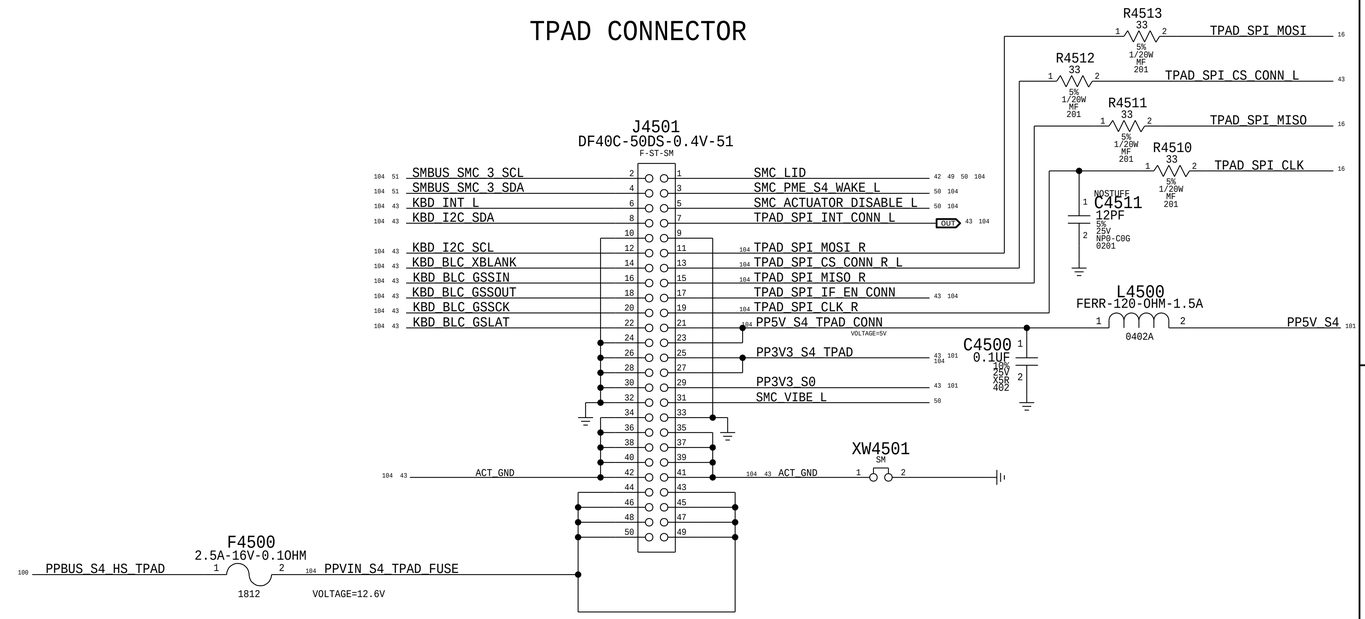
KBD CONNECTOR



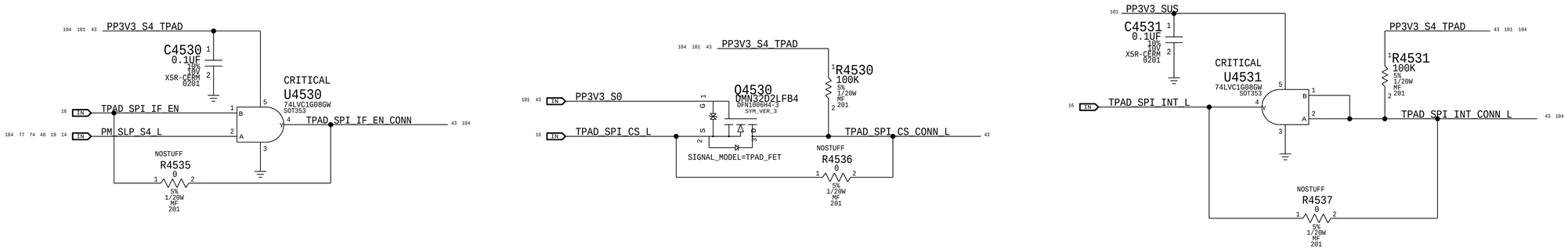
516S00177 (RCPT, 0.3A per pin)
MATE WITH PLUG 516S00054

TPAD CONNECTOR



516S00187, MATE WITH 516S00188

TRACKPAD ISOLATION



BOM_COST_GROUP=KEYBOARD

SYNC_MASTER=J79_GAREN	SYNC_DATE=11/21/2015
PAGE TITLE	Connectors&ESD
Apple Inc.	DRAWING NUMBER 051-00515 / SIZE D
	REVISION 9.0.0
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SYNC_MASTER=J79_DAYU SYNC_DATE=05/26/2015

PAGE TITLE

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SYNC_MASTER=J79_DAYU SYNC_DATE=05/26/2015

PAGE TITLE

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SYNC_MASTER=J79_DAYU SYNC_DATE=05/12/2015

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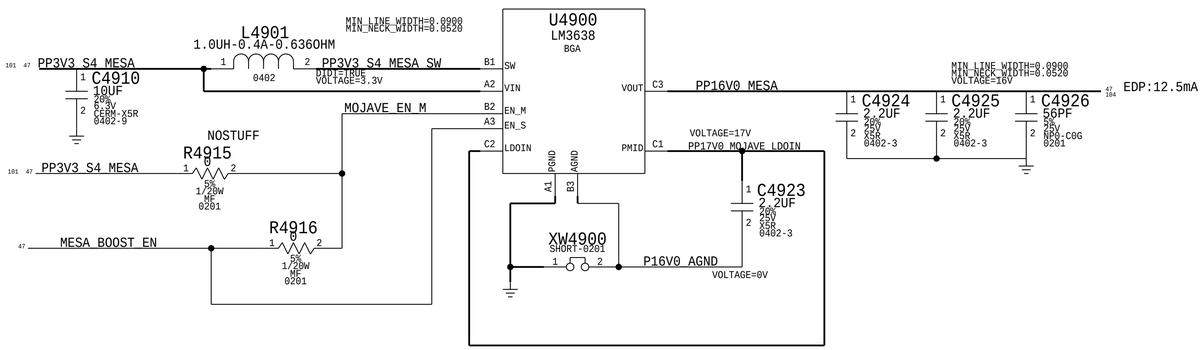
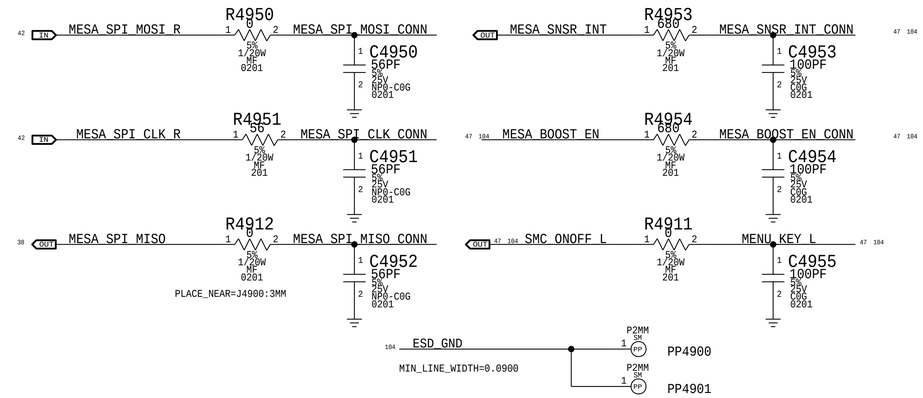
ISOLATE FROM OTHER COMPONENTS/NETS AS MUCH AS POSSIBLE

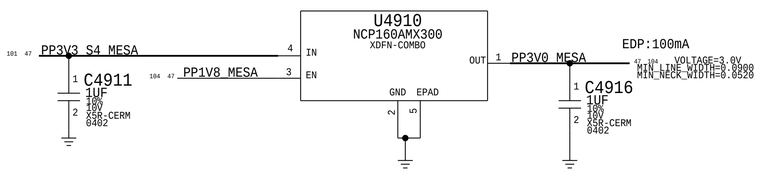
MOJAVE 16V BOOST

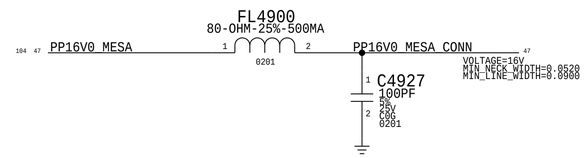




3.0V MESA

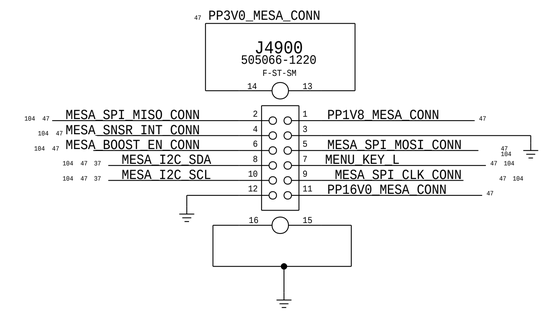
Option to feed LDO from 5V in case of dropout issue





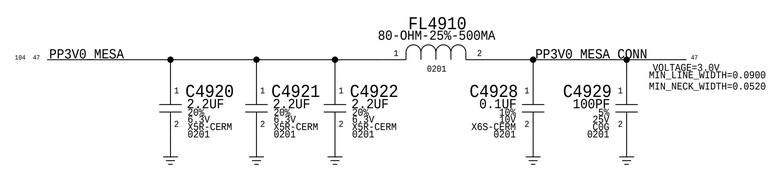
MESA FLEX CONNECTOR

Proto1 Connector for X434/X435 Support
PLUG (516S00115) - X434/ X435 Jumper
Recptacle (516S00203) - X362/X363 MLB

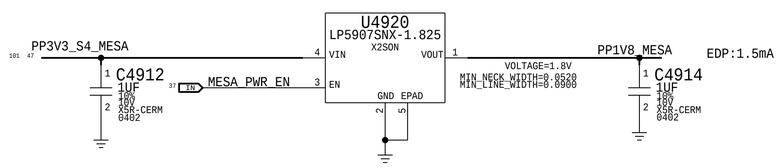


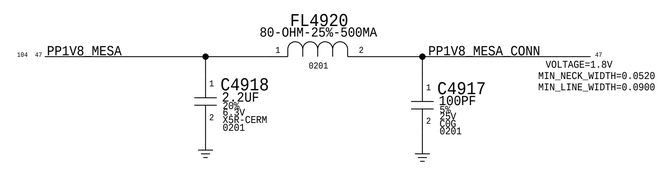
Mesa Power Sequencing Requirements

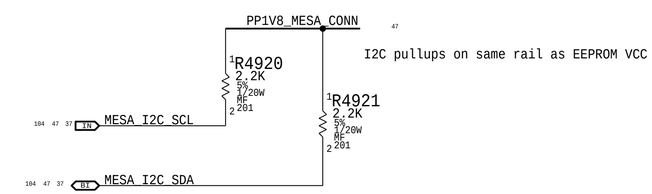
Power On: 1V8 -> 3V3 -> 16V0



1.8V MESA







I2C pullups on same rail as EEPROM VCC

BOM_COST_GROUP=T151

PAGE TITLE	MESA
Apple Inc.	DRAWING NUMBER 051-00515 SIZE D
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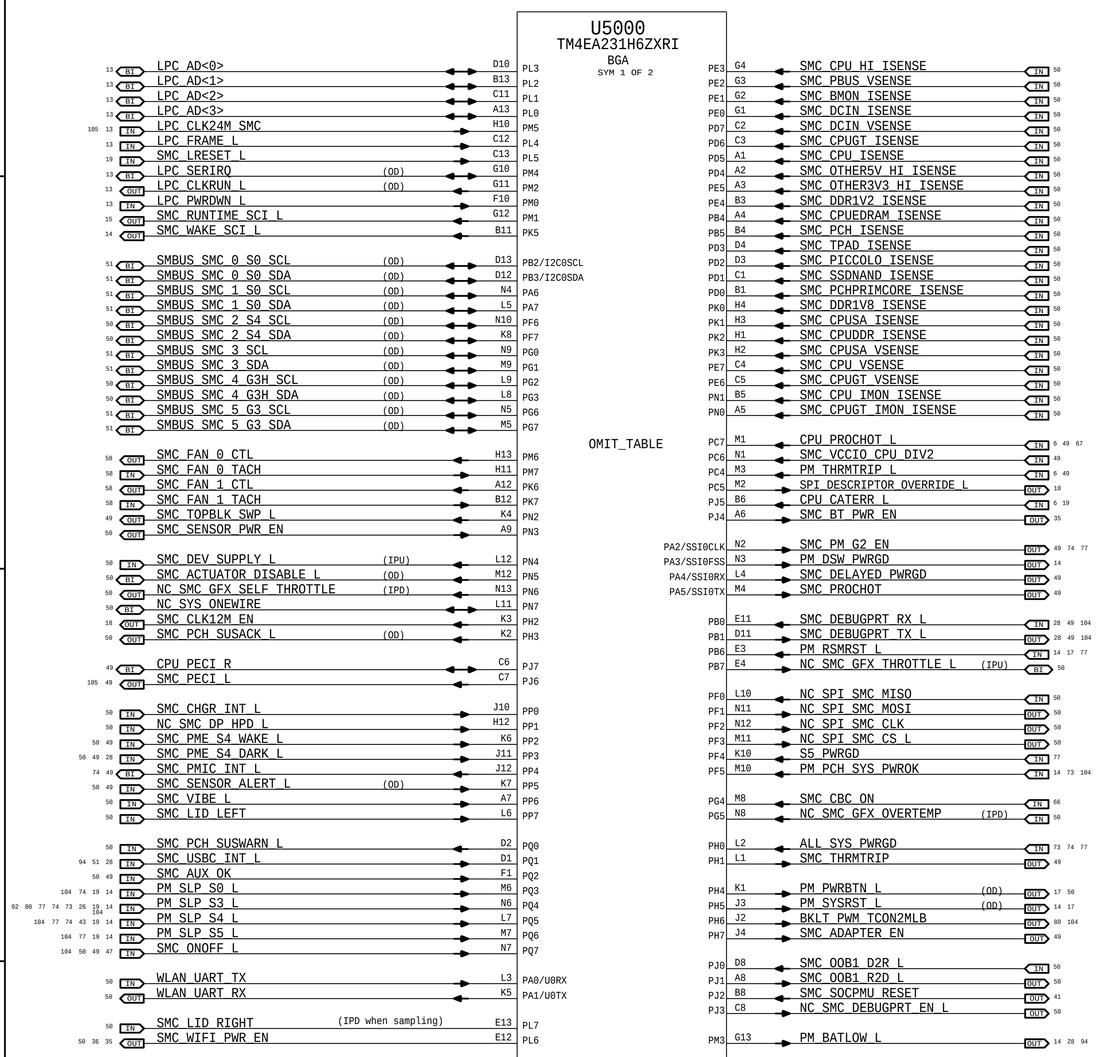

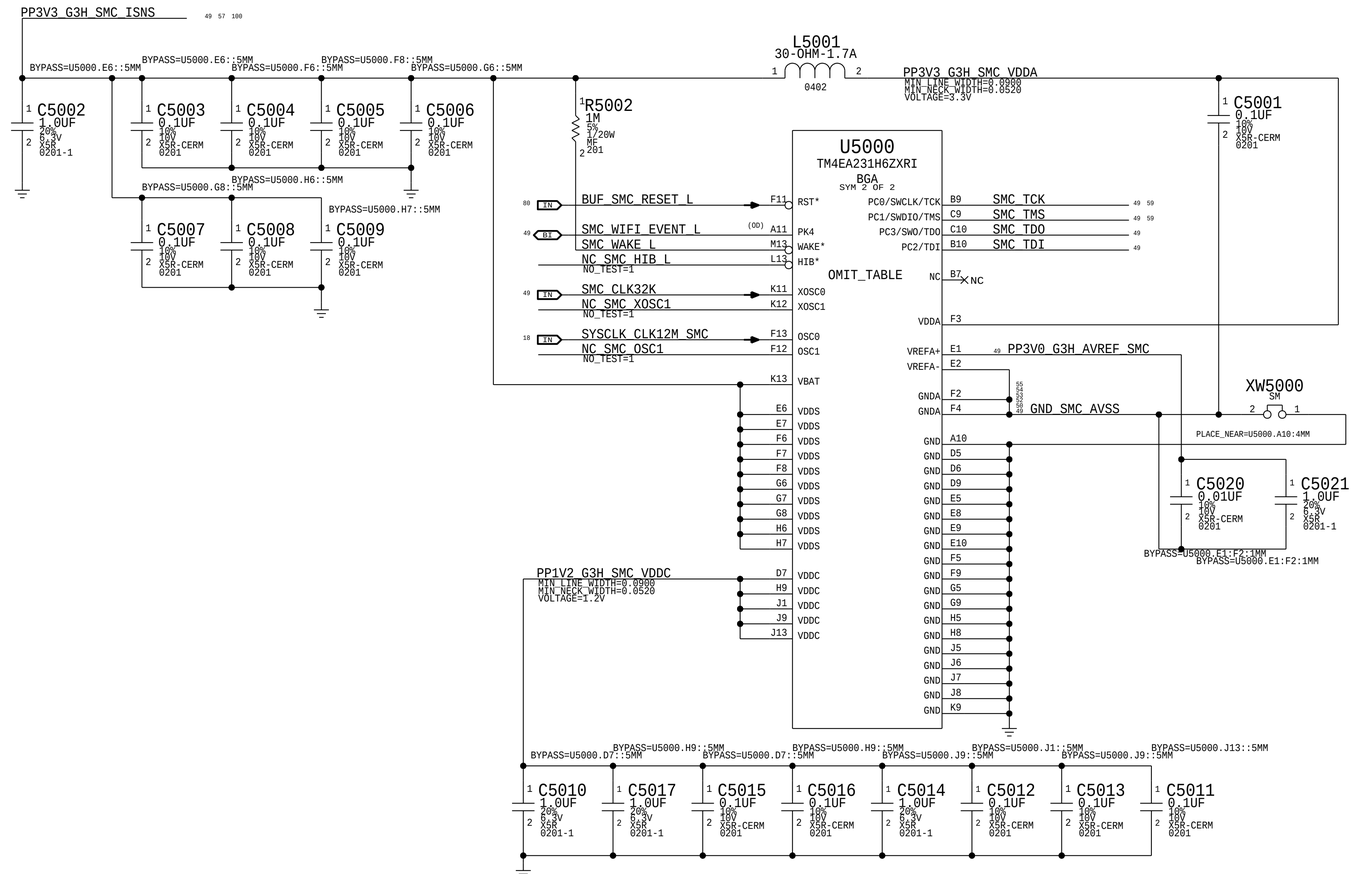

NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

PAGE TITLE
SMC

Apple Inc.

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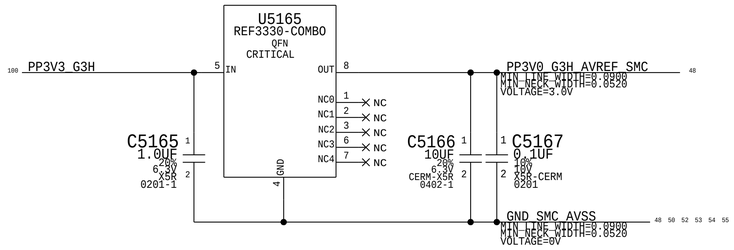
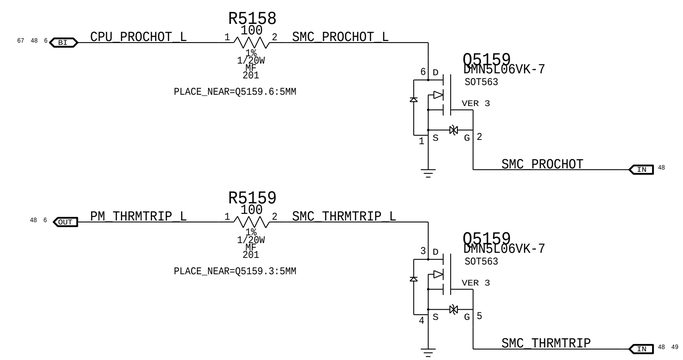
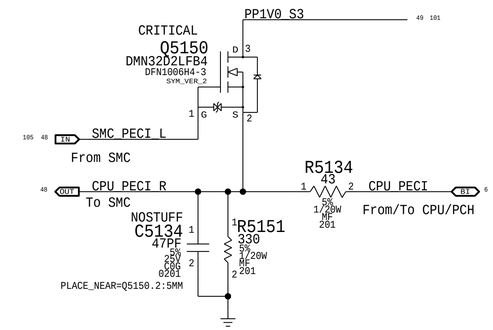
SMC AVREF Supply



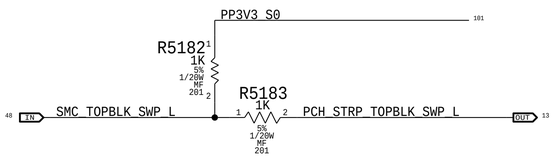
PROCHOT/THRMTRIP Support

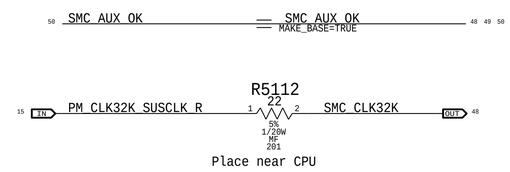


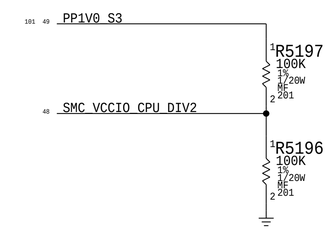
PECI Support

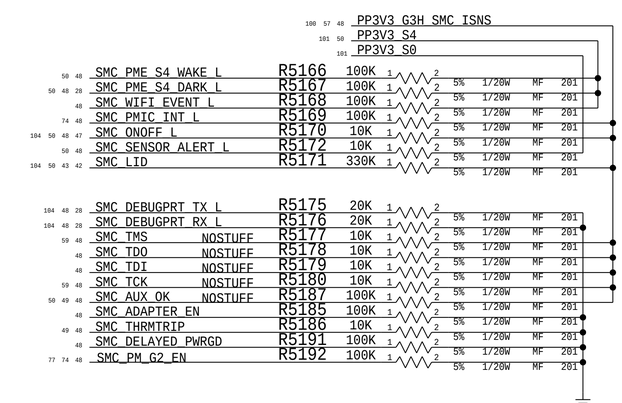


Top-Block Swap









BOM_COST_GROUP=SMC

SYNC_MASTER=J79_JACK SYNC_DATE=04/14/2016

PAGE TITLE

SMC Shared Support

Apple Inc.

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SMC12 ADC Assignments

SMC_CPU_HI_ISENSE	MAKE_BASE=TRUE	SMC_CPU_HI_ISENSE	52
SMC_PBUS_VSENSE	MAKE_BASE=TRUE	SMC_PBUS_VSENSE	52
SMC_BMON_ISENSE	MAKE_BASE=TRUE	SMC_BMON_ISENSE	52
SMC_DCIN_ISENSE	MAKE_BASE=TRUE	SMC_DCIN_ISENSE	52
SMC_DCIN_VSENSE	MAKE_BASE=TRUE	SMC_DCIN_VSENSE	52
SMC_CPUGT_ISENSE	MAKE_BASE=TRUE	SMC_CPUGT_ISENSE	55
SMC_CPU_ISENSE	MAKE_BASE=TRUE	SMC_CPU_ISENSE	53
SMC_OTHER5V_HI_ISENSE	MAKE_BASE=TRUE	SMC_OTHER5V_HI_ISENSE	52
SMC_OTHER3V3_HI_ISENSE	MAKE_BASE=TRUE	SMC_OTHER3V3_HI_ISENSE	52
SMC_DDR1V2_ISENSE	MAKE_BASE=TRUE	SMC_DDR1V2_ISENSE	53
SMC_CPUEDRAM_ISENSE	MAKE_BASE=TRUE	SMC_CPUEDRAM_ISENSE	55
SMC_PCH_ISENSE	MAKE_BASE=TRUE	SMC_PCH_ISENSE	53
SMC_TPAD_ISENSE	MAKE_BASE=TRUE	SMC_TPAD_ISENSE	52
SMC_PICCOLO_ISENSE	MAKE_BASE=TRUE	SMC_PICCOLO_ISENSE	55
SMC_SSDNAND_ISENSE	MAKE_BASE=TRUE	SMC_SSDNAND_ISENSE	55
SMC_PCHPRIMCORE_ISENSE	MAKE_BASE=TRUE	SMC_PCHPRIMCORE_ISENSE	55
SMC_DDR1V8_ISENSE	MAKE_BASE=TRUE	SMC_DDR1V8_ISENSE	55
SMC_CPUSA_ISENSE	MAKE_BASE=TRUE	SMC_CPUSA_ISENSE	55
SMC_CPUDDR_ISENSE	MAKE_BASE=TRUE	SMC_CPUDDR_ISENSE	53
SMC_CPUSA_VSENSE	MAKE_BASE=TRUE	SMC_CPUSA_VSENSE	55
SMC_CPU_VSENSE	MAKE_BASE=TRUE	SMC_CPU_VSENSE	54
SMC_CPUGT_VSENSE	MAKE_BASE=TRUE	SMC_CPUGT_VSENSE	54
SMC_CPU_IMON_ISENSE	MAKE_BASE=TRUE	SMC_CPU_IMON_ISENSE	54
SMC_CPUGT_IMON_ISENSE	MAKE_BASE=TRUE	SMC_CPUGT_IMON_ISENSE	54

SMC12 Pin Assignments

NC_SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE	NC_SMC_GFX_THROTTLE_L	NO_TEST=1	
NC_SMC_GFX_OVERTEMP	MAKE_BASE=TRUE	NC_SMC_GFX_OVERTEMP	NO_TEST=1	
NC_SMC_GFX_SELF_THROTTLE	MAKE_BASE=TRUE	NC_SMC_GFX_SELF_THROTTLE	NO_TEST=1	
NC_SMC_DP_HPD_L	MAKE_BASE=TRUE	NC_SMC_DP_HPD_L	NO_TEST=1	
NC_SYS_ONEWIRE	MAKE_BASE=TRUE	NC_SYS_ONEWIRE	NO_TEST=1	
NC_SMC_DEBUGPRT_EN_L	MAKE_BASE=TRUE	NC_SMC_DEBUGPRT_EN_L	NO_TEST=1	
SMC_LID_RIGHT	MAKE_BASE=TRUE	SMC_LID_RIGHT		50
NC_SPI_SMC_MISO		NC_SPI_SMC_MISO	NO_TEST=1	TRUE
NC_SPI_SMC_MOSI		NC_SPI_SMC_MOSI	NO_TEST=1	TRUE
NC_SPI_SMC_CLK		NC_SPI_SMC_CLK	NO_TEST=1	TRUE
NC_SPI_SMC_CS_L		NC_SPI_SMC_CS_L	NO_TEST=1	TRUE
SMC_VIBE_L	MAKE_BASE=TRUE	SMC_VIBE_L		43
SMC_PCH_SUSWARN_L	MAKE_BASE=TRUE	SMC_PCH_SUSWARN_L		14
SMC_PCH_SUSACK_L	MAKE_BASE=TRUE	SMC_PCH_SUSACK_L		14
SMC_SENSOR_PWR_EN	MAKE_BASE=TRUE	SMC_SENSOR_PWR_EN		78
		SMC_SENSOR_PWR_EN		52
WLAN_UART_RX	MAKE_BASE=TRUE	WLAN_UART_RX		35
WLAN_UART_TX	MAKE_BASE=TRUE	WLAN_UART_TX		35
SMC_AUX_OK	MAKE_BASE=TRUE	SMC_AUX_OK		49
PM_PWRBTN_L	MAKE_BASE=TRUE	PM_PWRBTN_L		14
SMC_AUX_OK	MAKE_BASE=TRUE	SMC_AUX_OK		52
SMBUS_SMC_4_G3H_SCL	MAKE_BASE=TRUE	SMBUS_SMC_4_G3H_SCL		48
SMBUS_SMC_4_G3H_SDA	MAKE_BASE=TRUE	SMBUS_SMC_4_G3H_SDA		48
SMBUS_SMC_2_S4_SCL	MAKE_BASE=TRUE	SMBUS_SMC_2_S4_SCL		48
SMBUS_SMC_2_S4_SDA	MAKE_BASE=TRUE	SMBUS_SMC_2_S4_SDA		48
SMC_OOB1_D2R_L	MAKE_BASE=TRUE	SMC_OOB1_D2R_L		88
SMC_OOB1_R2D_L	MAKE_BASE=TRUE	SMC_OOB1_R2D_L		88
SMC_ACTUATOR_DISABLE_L	MAKE_BASE=TRUE	SMC_ACTUATOR_DISABLE_L		43 104
SMC_CHGR_INT_L	MAKE_BASE=TRUE	SMC_CHGR_INT_L		66

Debug Power "Buttons"

DEBUG_BUTTON
PLACE_SIDE=TOP
SILK_PART=PWR_BTN
CRITICAL
R5226
SOX-152HNT
SM

SMC_ONOFF_L — OUT 47 48 49 50 104

PLACE_SIDE=BOTTOM
SILK_PART=PWR_BTN
CRITICAL
R5225
SOX-152HNT
SM

DEBUG_BUTTON

Debug RESET "Buttons"

DEBUG_BUTTON
PLACE_SIDE=BOTTOM
SILK_PART=RESET_BTN
CRITICAL
SW5227
SOX-152HNT
SM

SMC_RESET_L — OUT 50 59 66 80 104

Hall Effect Pads - Left

J5250
AMR-MLB-X502
SM

HALL_SENSOR_LEFT
PP3V3_G3H — 50 100
OMIT_TABLE

NOSTUFF
C5250
1000PF
10%
16V
X7R-1
0201

Hall Effect Pads - Right

J5260
AMR-MLB-X502
SM

HALL_SENSOR_RIGHT
PP3V3_G3H — 50 100
OMIT_TABLE

NOSTUFF
C5260
1000PF
10%
16V
X7R-1
0201

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
677-04255	2	SUBASSY (T&R) PCBA,HES INTERPOSER,X502	J5250, J5260	CRITICAL	

Specify one of these BOM GROUPs.

BOM GROUP	BOM OPTIONS
CPUTHRM:BOTH	CPUTHRM_THRM:SMC,CPUTHRM_ALRT:SMC
CPUTHRM:THRM	CPUTHRM_THRM:SMC,CPUTHRM_ALRT:PU
CPUTHRM:ALRT	CPUTHRM_ALRT:SMC
CPUTHRM:NONE	CPUTHRM_ALRT:PU

Specify one of these BOM GROUPs.

BOM GROUP	BOM OPTIONS
TBTTHRM:BOTH	TBTTHRM_THRM:SMC,TBTTHRM_ALRT:SMC
TBTTHRM:THRM	TBTTHRM_THRM:SMC,TBTTHRM_ALRT:PU
TBTTHRM:ALRT	TBTTHRM_THRM:PU,TBTTHRM_ALRT:SMC
TBTTHRM:NONE	TBTTHRM_THRM:PU,TBTTHRM_ALRT:PU

Requires EMC1412-1 or EMC1412-2 instead of EMC1412-A, new APN needs to be created.

Thermal Alerts

SMC_CPUHI_COMP_ALERT_L	R5217	100	
CPUTHMSNS_THM_L	R5216	100	CPUTHRM_THRM:SMC
CPUTHMSNS_ALERT_L	R5214	100	CPUTHRM_ALRT:SMC
TBTTHMSNS_THM_L	R5220	100	TBTTHRM_THRM:SMC
TBTTHMSNS_ALERT_L	R5210	100	TBTTHRM_ALRT:SMC
TBTTHMSNS_THM_T_L	R5221	100	TBTTHRM_THRM:SMC
TBTTHMSNS_ALERT_T_L	R5211	100	TBTTHRM_ALRT:SMC

5% 1/20W MF 201

SMC_SENSOR_ALERT_L — OUT 48 49

PP3V3_G3H — 43 100 104
BYPASS=U5256.5::5MM

R5258
100K
5%
1/20W
MF
201

C5256
0.1UF
10%
10V
X5R-CERM
0201

SN74LVC1G02
SOT553-5

SMC_LSOC_RST_L — IN 104 43
SMC_ONOFF_L — IN 104 50 49 48 47
SMC_4FINGERS_RST — OUT 66

U5256
CRITICAL

S4 SMC Wake Sources

SMC_PME_S4_WAKE_L — IN 104 43 — SMC_PME_S4_WAKE_L MAKE_BASE=TRUE — OUT 48 49

SMC_PME_S4_DARK_L — 35 — SMC_PME_S4_DARK_L MAKE_BASE=TRUE — OUT 20 48 49

PP3V3_S4 — 101 49

R5273
10K

WLAN_UART_RX — 50 48
WLAN_UART_TX — 50 48

R5274
100K

5% 1/20W MF 201

SMC_LID_LEFT_R — R5256 0 — SMC_LID_LEFT — OUT 48

PP3V3_G3H — 100 50
BYPASS=U5255.6::5MM

C5255
0.1UF
10%
10V
X5R-CERM
0201

NOSTUFF
R5257
0
5%
1/20W
MF
0201

U5255
74LVC1G32
SOT891

HALL_SENSOR_LEFT — 50
R5251
10K

HALL_SENSOR_RIGHT — 50
R5261
10K

SMC_LID_R — R5255 10K — SMC_LID — OUT 42 43 49 104

CRITICAL

NC

SMC_LID_RIGHT — 50

SMC_WIFI_PWR_EN — 48 36 35 — R5295 10K
SMC_SENSOR_PWR_EN — 50 48 — R5294 10K

5% 1/20W MF 201

SMC_DEV_SUPPLY_L — 48 — R5259 0 — TP_SMC_DEV_SUPPLY_L — 104

5% 1/20W MF 0201

SMC_RESET_L — 50 59 66 80 104

NOSTUFF
C5270
1000PF
10%
10V
X7R-CERM
0201

GND_SMC_AVSS — 48 49 52 53 54 55

BOM_COST_GROUP=SMC

PAGE TITLE
PAGE_TITLE=SMC Project Support

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SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
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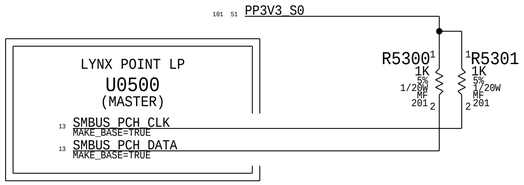
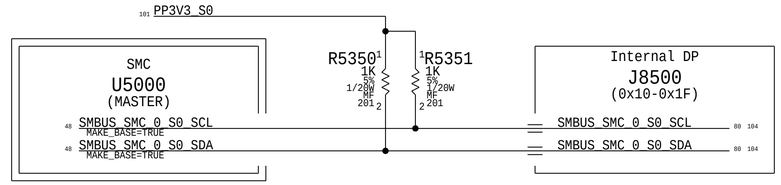
SHEET 50 OF 119

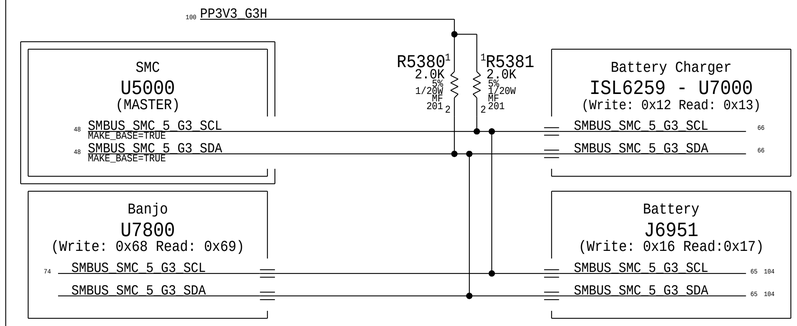
LYNX POINT LP S0 "SMBus 0" Connections



SMC SMBus "0" S0 Connections

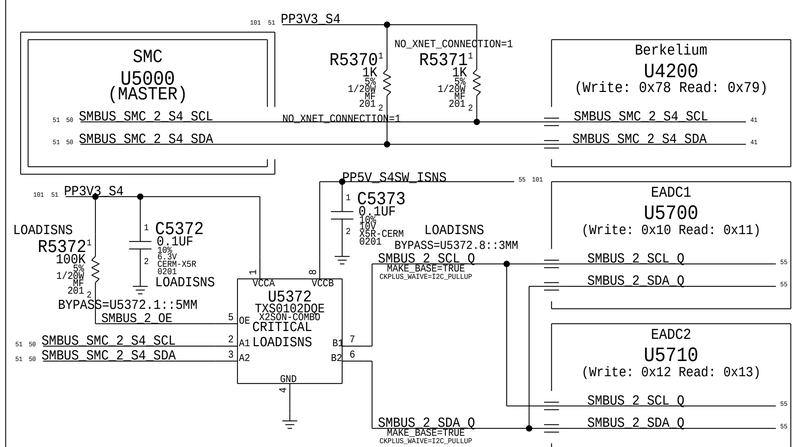


SMC SMBus "5" G3H Connections

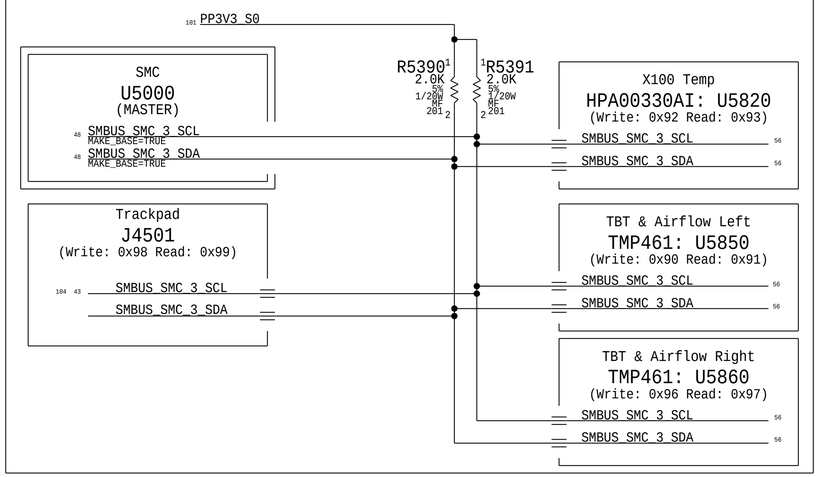


ACE I2C Interrupt

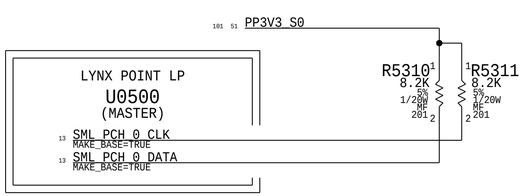
SMC SMBus "2" S4 Connections



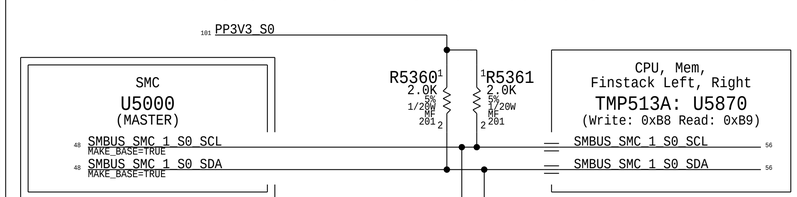
SMC SMBus "3" S0 Connections



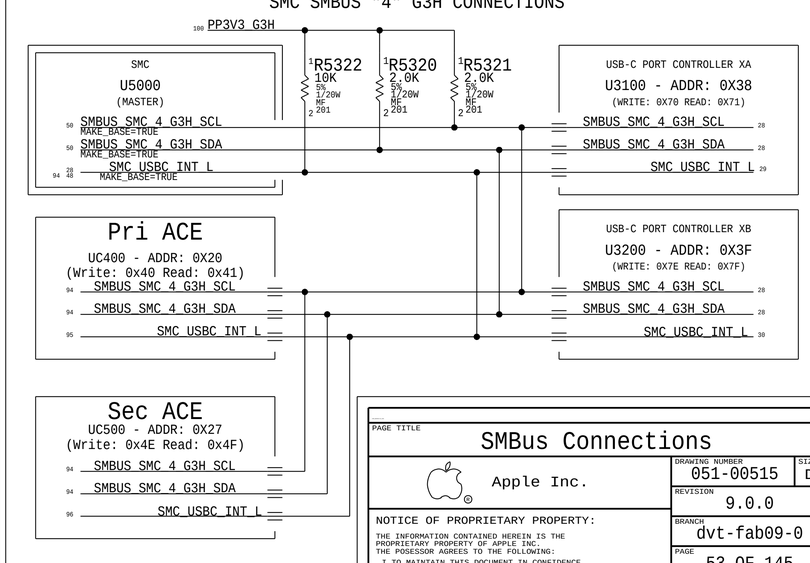
LYNX POINT LP S0 "SMLink 0" Connections



SMC SMBus "1" S0 Connections



SMC SMBUS "4" G3H CONNECTIONS



LYNX POINT LP S0 "SMLink 1" Connections

SMLink 1 is slave port to access PCH.

BOM_COST_GROUP=SMC

PAGE TITLE: SMBus Connections

Apple Inc.

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REVISION: 9.0.0
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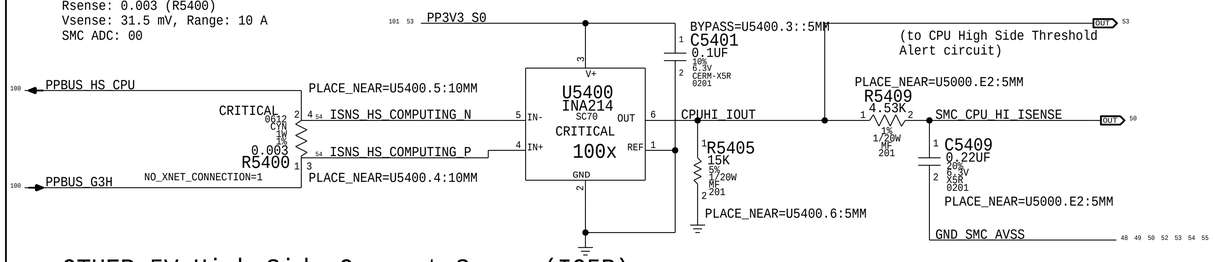
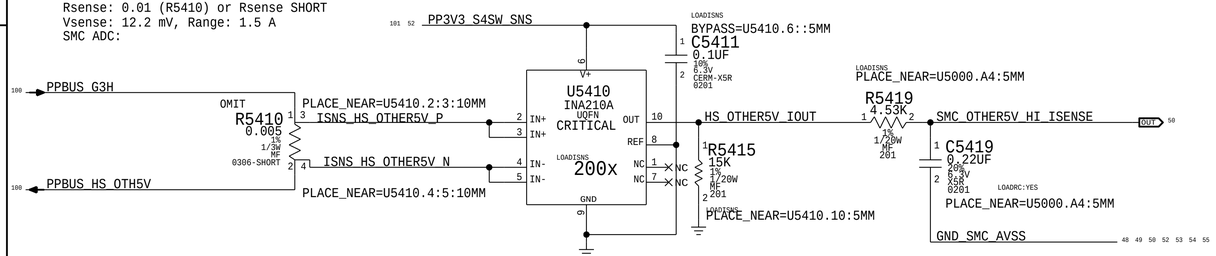
CPU High Side Current Sense (IC0R)

Gain: 100x, EDP: 10.5 A
Rsense: 0.003 (R5400)
Vsense: 31.5 mV, Range: 10 A
SMC ADC: 00



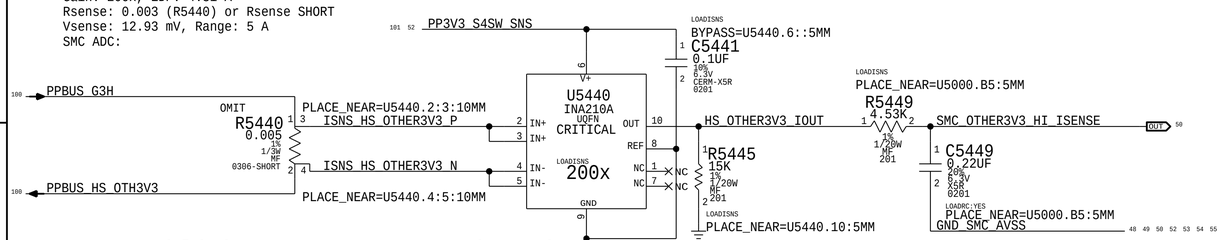
OTHER 5V High Side Current Sense (IO5R)

Gain: 200x, EDP: 1.22 A
Rsense: 0.01 (R5410) or Rsense SHORT
Vsense: 12.2 mV, Range: 1.5 A
SMC ADC:



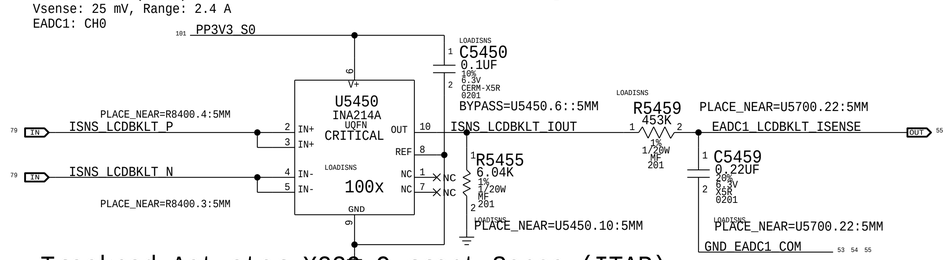
OTHER 3.3V High Side Current Sense (IO3R)

Gain: 200x, EDP: 4.31 A
Rsense: 0.003 (R5440) or Rsense SHORT
Vsense: 12.93 mV, Range: 5 A
SMC ADC:



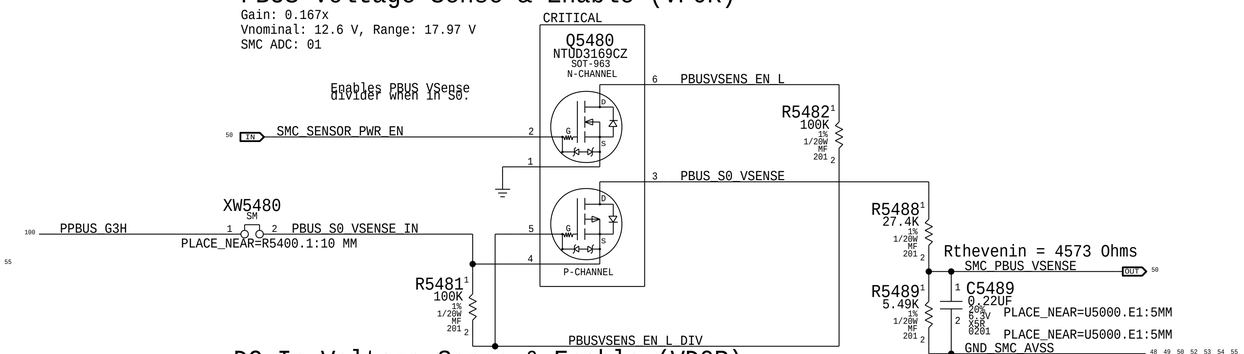
LCD Backlight Current Sense (IBLR)

Gain: 100x. EDP: 1 A
Rsense: 0.025 (R8400)
Vsense: 25 mV, Range: 2.4 A
EADC1: CH0



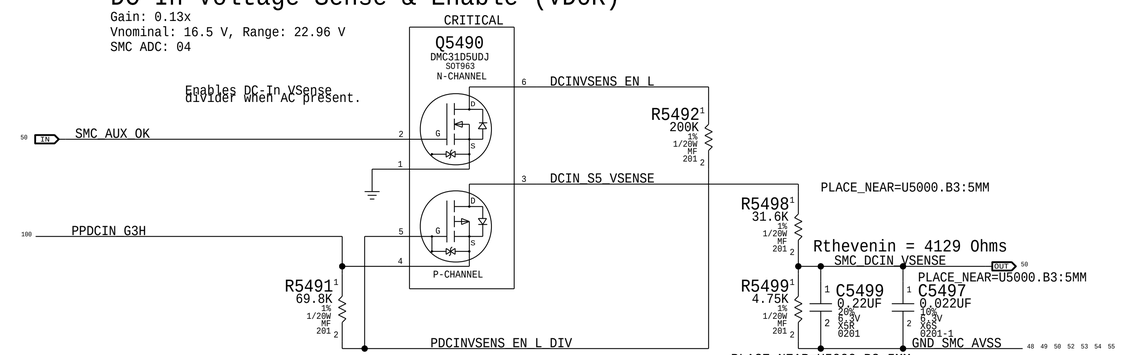
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
Vnominal: 12.6 V, Range: 17.97 V
SMC ADC: 01



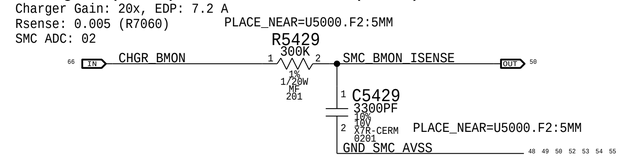
DC In Voltage Sense & Enable (VD0R)

Gain: 0.13x
Vnominal: 16.5 V, Range: 22.96 V
SMC ADC: 04



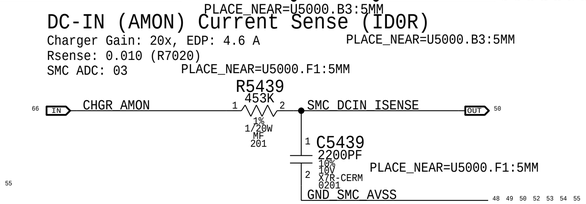
Charger (BMON) Current Sense (IPBR)

Charger Gain: 20x, EDP: 7.2 A
Rsense: 0.005 (R7060)
SMC ADC: 02



DC-IN (AMON) Current Sense (ID0R)

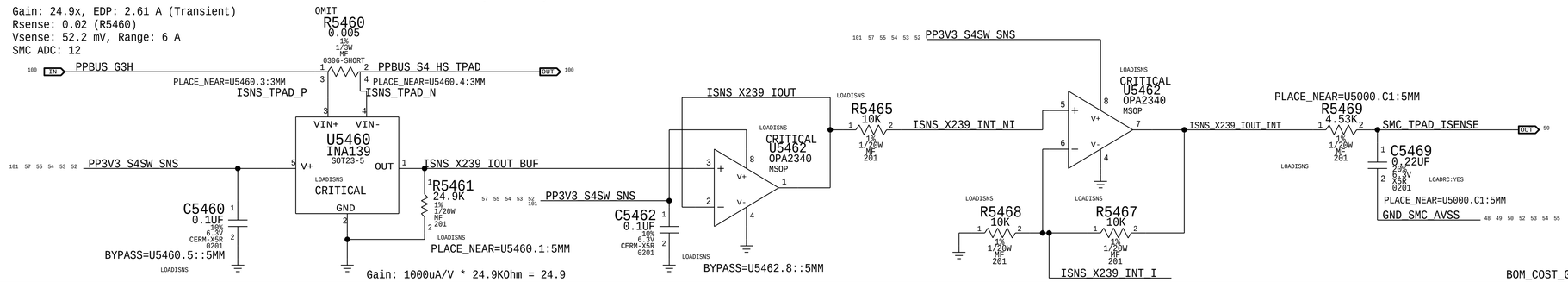
Charger Gain: 20x, EDP: 4.6 A
Rsense: 0.010 (R7020)
SMC ADC: 03



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5419,C5449		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5469		LOADRC:NO

Trackpad Actuator X239 Current Sense (ITAR)

Gain: 24.9x, EDP: 2.61 A (Transient)
Rsense: 0.02 (R5460)
Vsense: 52.2 mV, Range: 6 A
SMC ADC: 12



BOM_COST_GROUP=SENSORS

PAGE TITLE
Power Sensors: High Side

Apple Inc.

DRAWING NUMBER	051-00515
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
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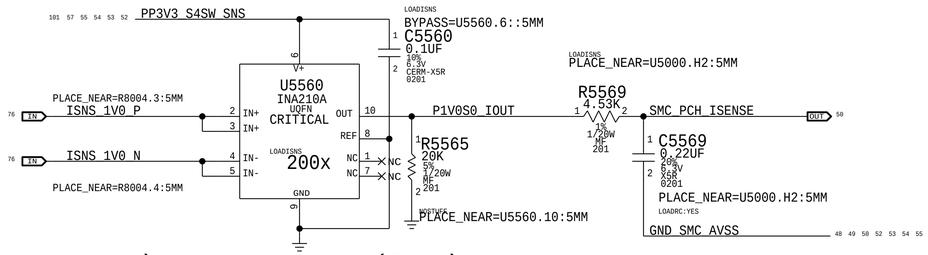
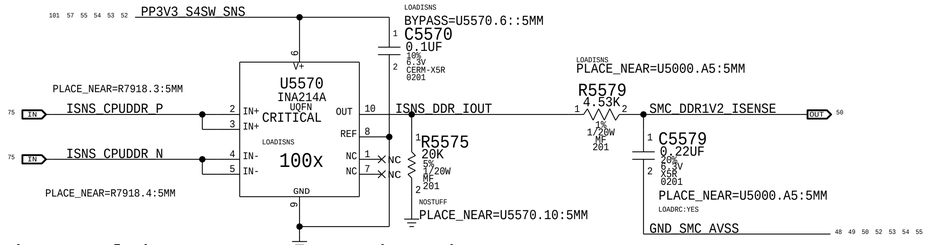
PCH 1.0V Current Sense (IS1C)

Gain: 200x, EDP: 3.29 A
Rsense: 0.003 (R8004) or Rsense SHORT
Vsense: 9.87 mV, Range: 5 A
SMC ADC: 11



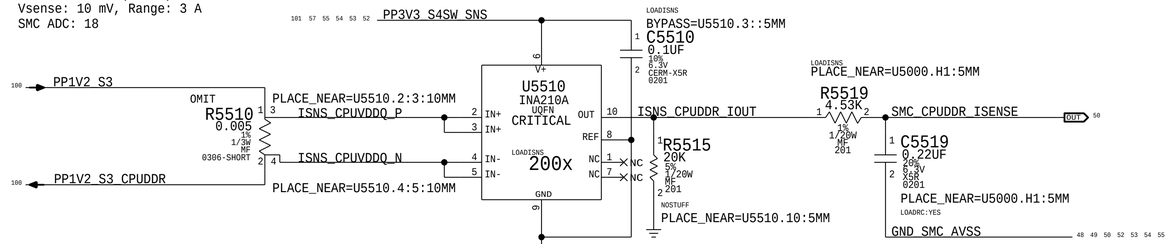
DDR 1.2V S3 (CPU & Memory) Current Sense (IM0C)

Gain: 100x, EDP: 8.21 A
Rsense: 0.003 (R7918) or XWTBD
Vsense: 24.63 mV, Range: 10 A
SMC ADC: 09



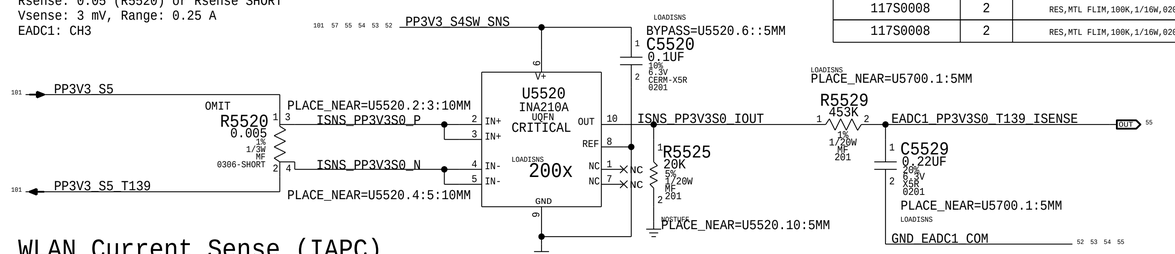
CPU DDR 1.2V S3 (CPU Only) Current Sense (IMCC)

Gain: 200x, EDP: 2 A
Rsense: 0.005 (R5510) or Rsense SHORT
Vsense: 10 mV, Range: 3 A
SMC ADC: 18



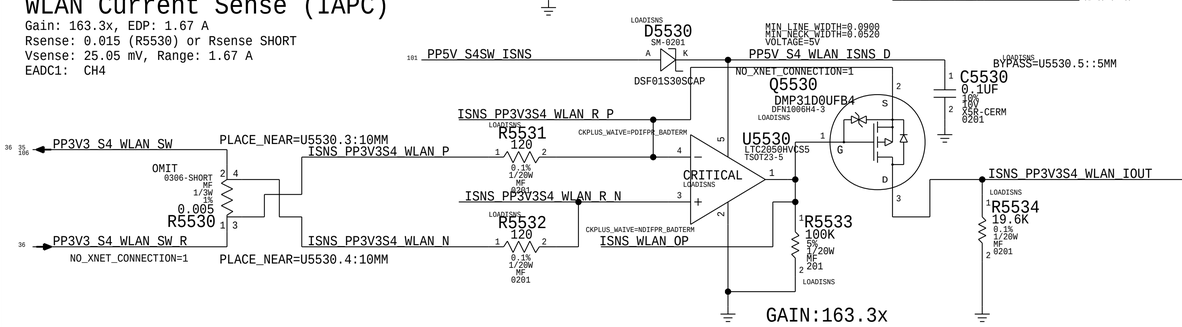
T139 Current Sense (IF3C)

Gain: 200x, EDP: 0.06 A
Rsense: 0.05 (R5520) or Rsense SHORT
Vsense: 3 mV, Range: 0.25 A
EADC1: CH3



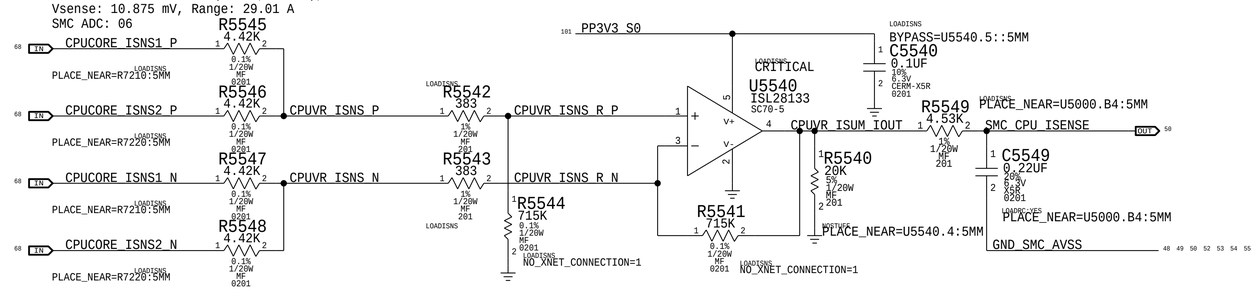
WLAN Current Sense (IAPC)

Gain: 163.3x, EDP: 1.67 A
Rsense: 0.015 (R5530) or Rsense SHORT
Vsense: 25.05 mV, Range: 1.67 A
EADC1: CH4



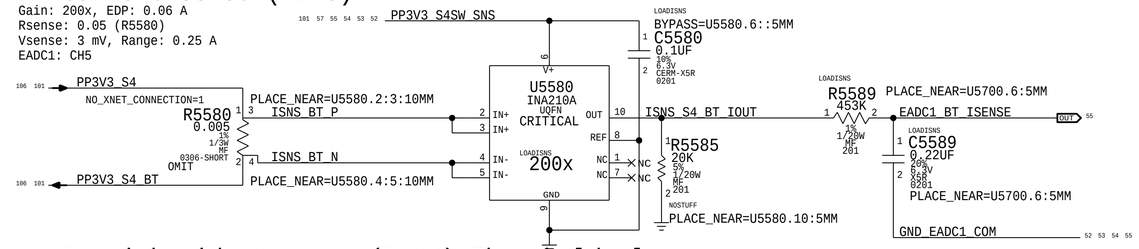
CPU Fixed Current Sense (ICAC)

Gain: 275.74x, EDP: 29 A
Rsense: 2x of 0.00075 (R7310, R7320), Rsum: 0.000375
Vsense: 10.875 mV, Range: 29.01 A
SMC ADC: 06



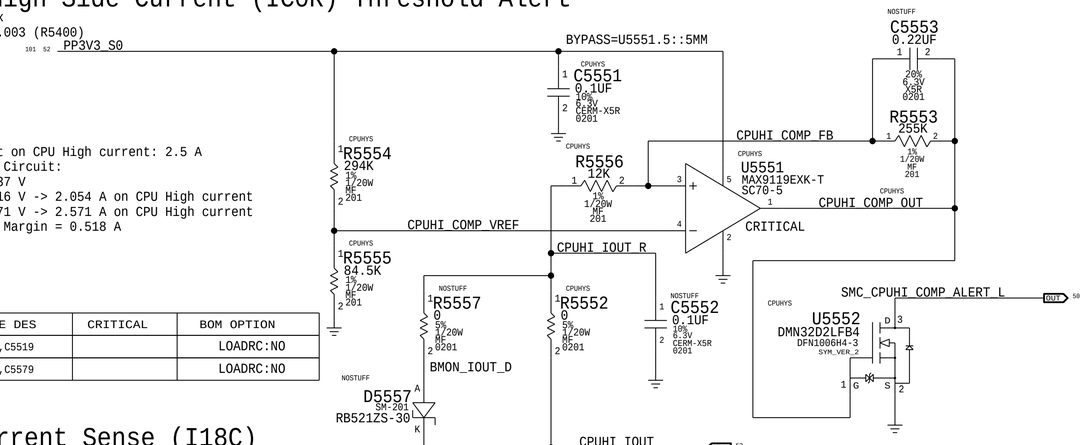
BT Current Sense (IBTC)

Gain: 200x, EDP: 0.06 A
Rsense: 0.05 (R5580)
Vsense: 3 mV, Range: 0.25 A
EADC1: CH5



CPU High Side Current (IC0R) Threshold Alert

Gain: 100x
Rsense: 0.003 (R5400)

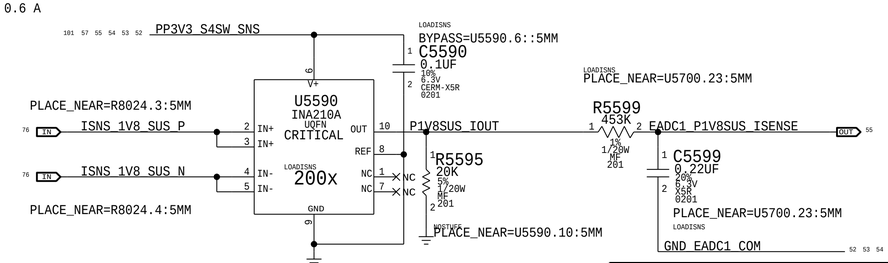


Trip Target on CPU High current: 2.5 A
Hysteresis Circuit:
Vref = 0.737 V
Vth = 0.616 V -> 2.054 A on CPU High current
Vtl = 0.771 V -> 2.571 A on CPU High current
Hysteresis Margin = 0.518 A

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5569,C5519		LOADRC:NO
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5549,C5579		LOADRC:NO

1.8V Current Sense (I18C)

Gain: 200x, EDP: 0.7 A
Rsense: 0.025 (R8024) or Rsense SHORT
Vsense: 17.5 mV, Range: 0.6 A
SMC ADC: 16



BOM_COST_GROUP=SENSORS

PAGE TITLE	Power Sensors: Load Side
	Apple Inc.
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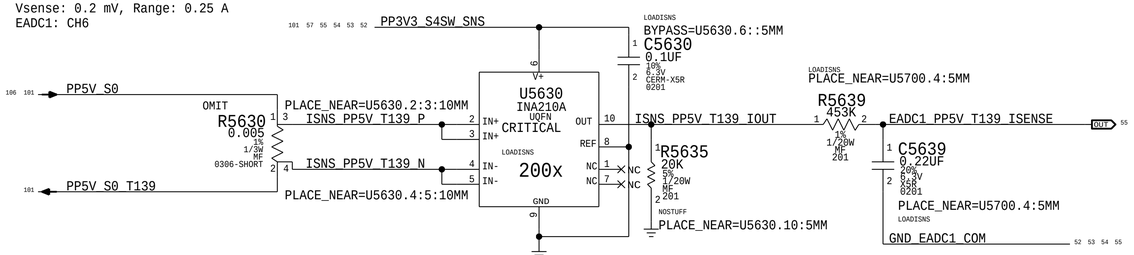
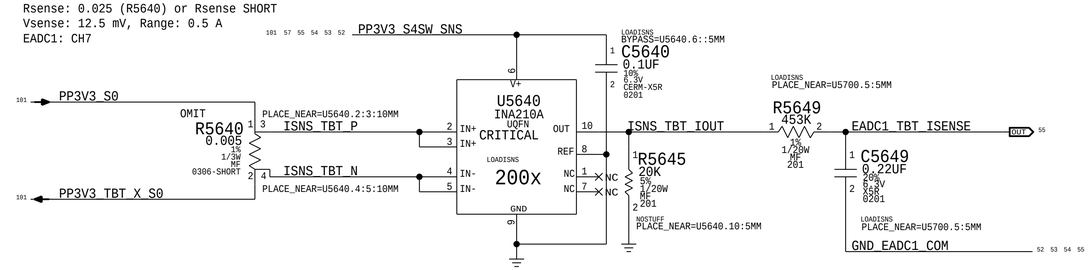
T139 5V Current Sense (IF5C)

Gain: 200x, EDP: 0.004 A
Rsense: 0.05 (R5630) or Rsense SHORT
Vsense: 0.2 mV, Range: 0.25 A
EADC1: CH6



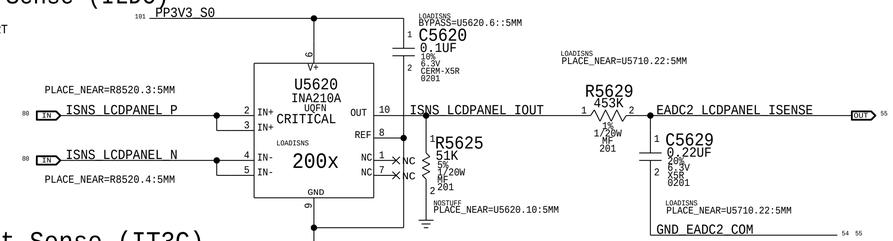
Thunderbolt TBT Current Left (IULC)

Gain: 200x. EDP: 0.5 A
Rsense: 0.025 (R5640) or Rsense SHORT
Vsense: 12.5 mV, Range: 0.5 A
EADC1: CH7



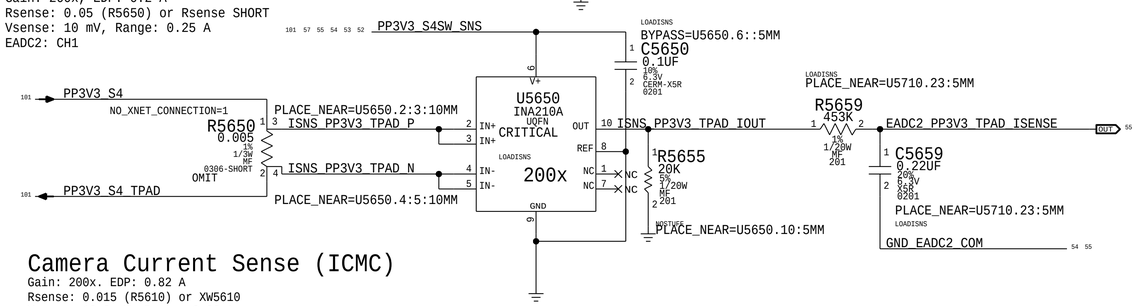
LCD Panel Current Sense (ILDC)

Gain: 200x. EDP: 1 A
RSENSE: 0.01 (R8520) or Rsense SHORT
Vsense: 5 mV, Range: 1.25 A
EADC2: CH0



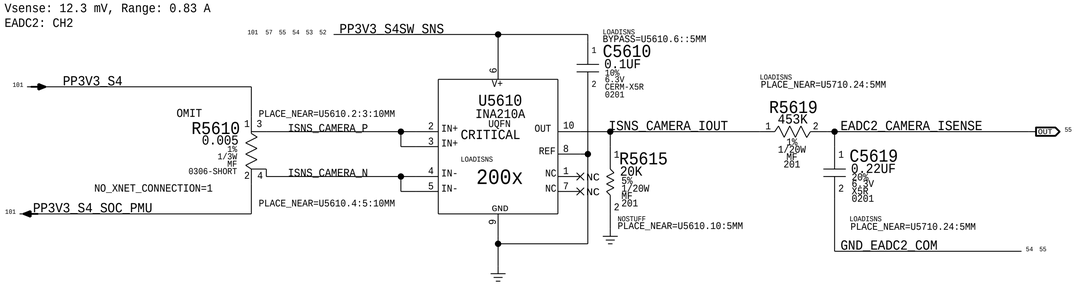
Trackpad 3V Current Sense (IT3C)

Gain: 200x, EDP: 0.2 A
Rsense: 0.05 (R5650) or Rsense SHORT
Vsense: 10 mV, Range: 0.25 A
EADC2: CH1

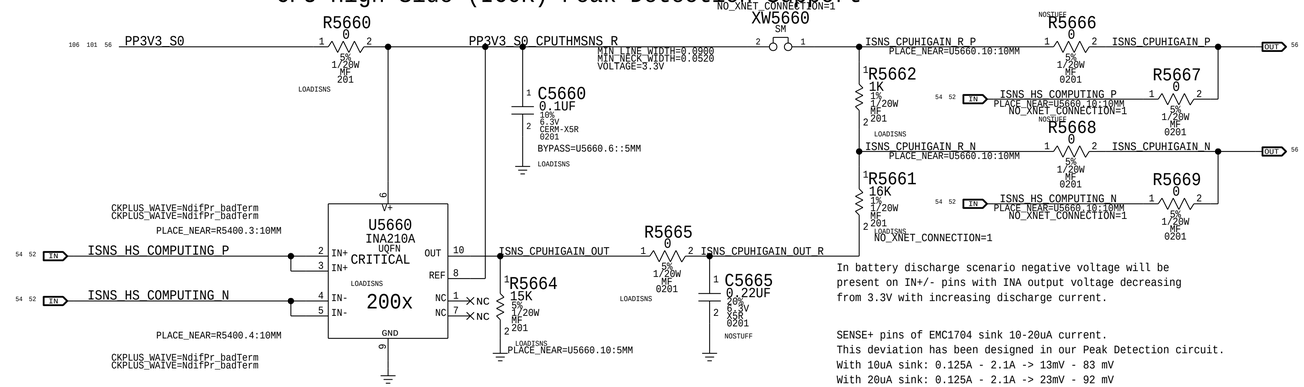


Camera Current Sense (ICMC)

Gain: 200x. EDP: 0.82 A
Rsense: 0.015 (R5610) or XW5610
Vsense: 12.3 mV, Range: 0.83 A
EADC2: CH2



CPU High Side (IC0R) Peak Detection Support

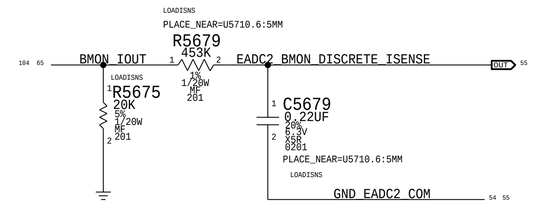


In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

SENSE+ pins of EMC1704 sink 10-20uA current.
This deviation has been designed in our Peak Detection circuit.
With 10uA sink: 0.125A - 2.1A -> 13mV - 83 mV
With 20uA sink: 0.125A - 2.1A -> 23mV - 92 mV

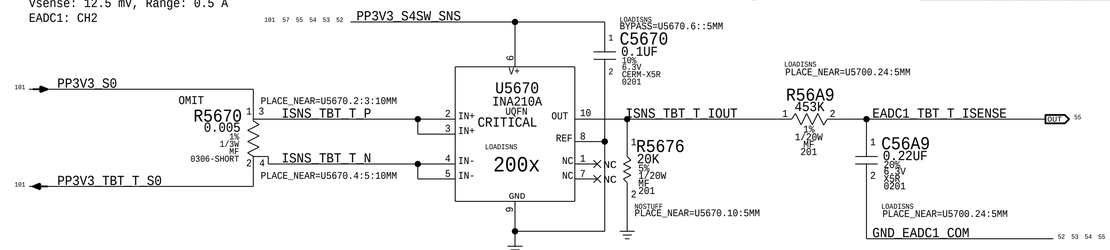
Battery Discrete Current Sense (IB0L)

Gain: 2940x. EDP: 8 A
Rsense: 0.003 (R501//R502)
Vsense: 24 mV, Range: 0.28 A
EADC2: CH5



Thunderbolt TBT Current Right (IURC)

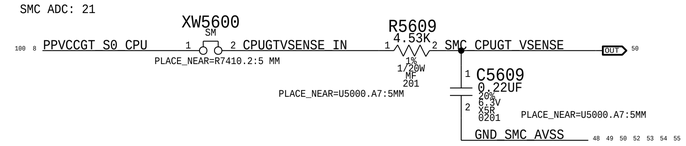
Gain: 200x. EDP: 0.5 A
Rsense: 0.025 (R5670) or Rsense SHORT
Vsense: 12.5 mV, Range: 0.5 A
EADC1: CH2



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5608, C5699		LOADRC:NO

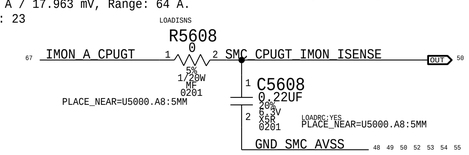
CPU GT Voltage Sense (VCGC)

SMC ADC: 21



CPU GT IMON Current Sense (ICGM)

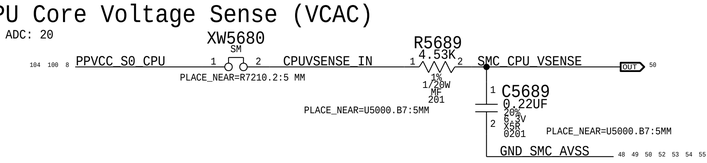
Gain: 1 A / 17.963 mV, Range: 64 A.
SMC ADC: 23



With R7154 (Ri) set to 294 Ohm,
R7410 (Rsen) set to 0.75 mOhm,
R7194 set to 84.5 kOhm,
Num Phases (N) is 3, and Io (ICCmax) is 64A,
then 1A of Io gives 17.963mV at the Vimon.

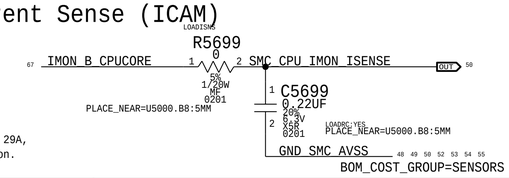
CPU Core Voltage Sense (VCAC)

SMC ADC: 20



CPU Core IMON Current Sense (ICAM)

Gain: 1 A / 34.223 mV, Range: 29 A.
SMC ADC: 22



With R7150 (Ri) set to 226 Ohm,
R7210 (Rsen) set to 0.75 mOhm,
R7160 set to 82.5 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 29A,
then 1A of Io gives 34.223mV at the Vimon.

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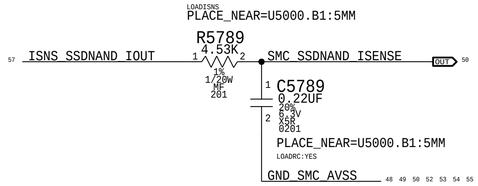
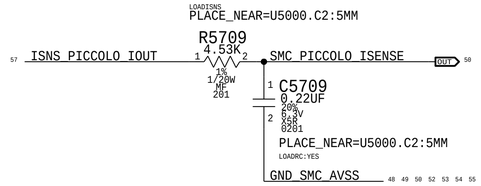
NAND Current Sense (IHNC)

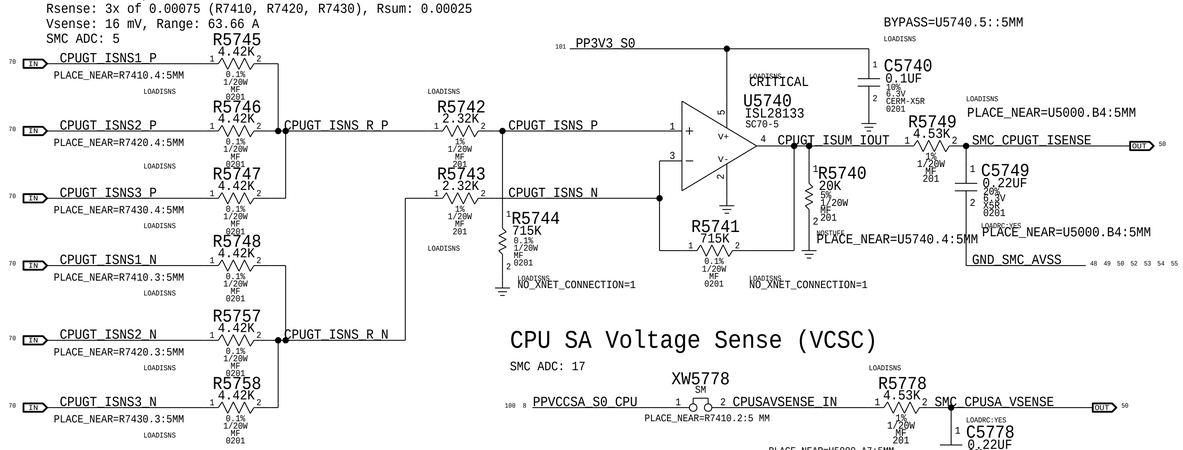


PICCOLO Current Sense (IHCC)



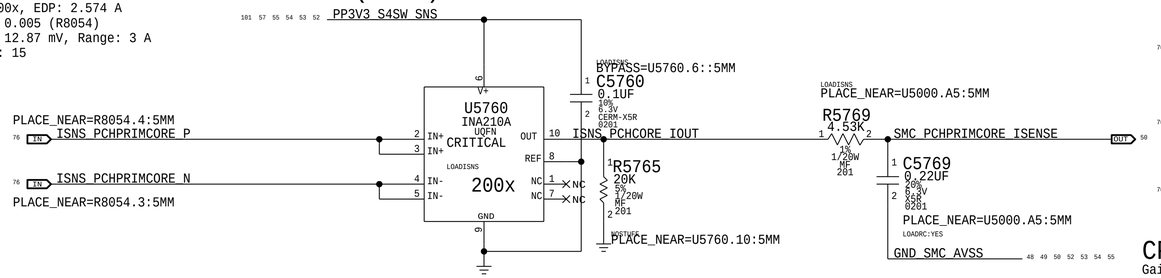
CPU GT+GTX Current Sense (ICGC)

Gain: 188.49x, EDP: 64 A
Rsense: 3x of 0.00075 (R7410, R7420, R7430), Rsum: 0.00025
Vsense: 16 mV, Range: 63.66 A
SMC ADC: 5



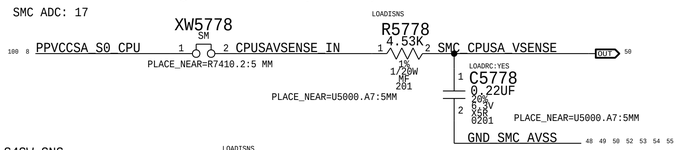
PCH PrimeCore Current Sense (ISCC)

Gain: 200x, EDP: 2.574 A
Rsense: 0.005 (R8054)
Vsense: 12.87 mV, Range: 3 A
SMC ADC: 15



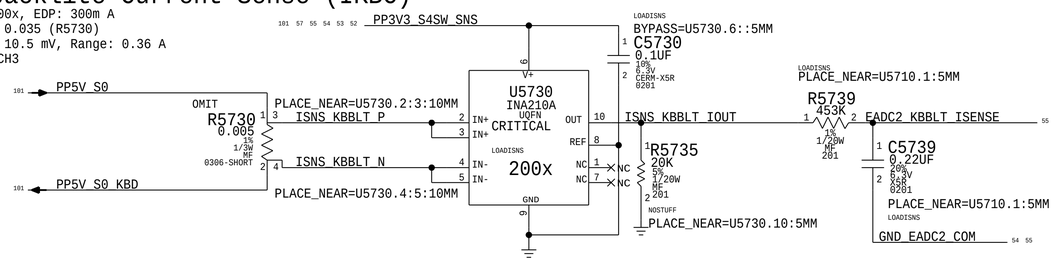
CPU SA Voltage Sense (VCSC)

SMC ADC: 17



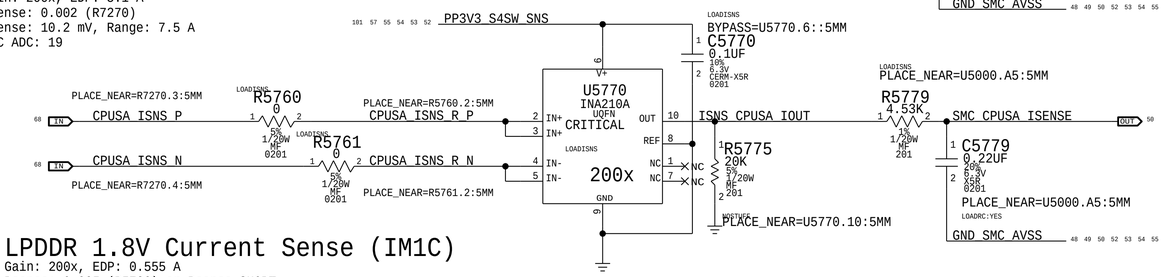
KB backlite Current Sense (IKBC)

Gain: 200x, EDP: 300m A
Rsense: 0.035 (R5730)
Vsense: 10.5 mV, Range: 0.36 A
EADC2: CH3



CPU SA Current Sense (ICSC)

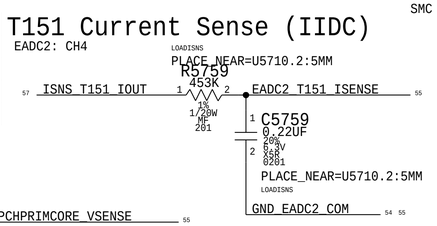
Gain: 200x, EDP: 5.1 A
Rsense: 0.002 (R7270)
Vsense: 10.2 mV, Range: 7.5 A
SMC ADC: 19



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5769,C5778		LOADRC:NO
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5749,C5779		LOADRC:NO
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5729,C5799		LOADRC:NO
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5709,C5789		LOADRC:NO

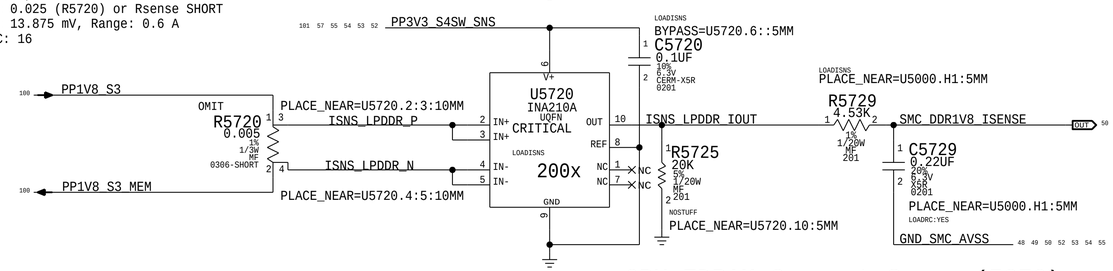
T151 Current Sense (IIDC)

EADC2: CH4



LPDDR 1.8V Current Sense (IM1C)

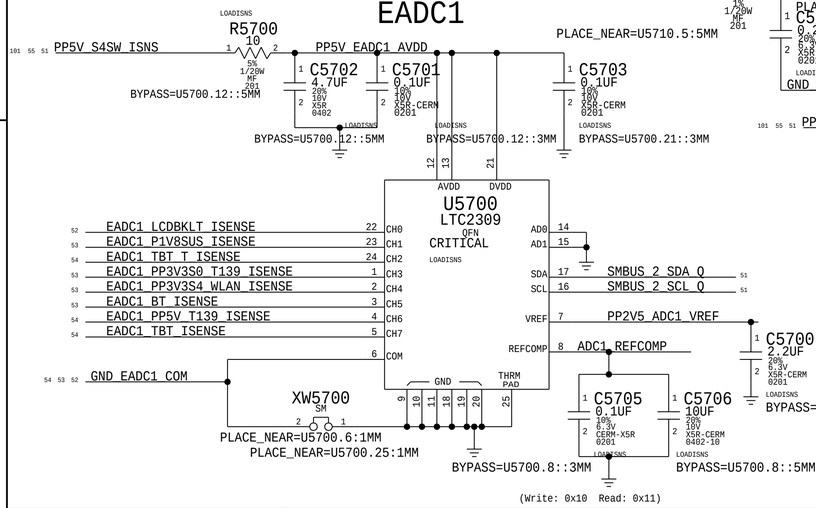
Gain: 200x, EDP: 0.555 A
Rsense: 0.025 (R5720) or Rsense SHORT
Vsense: 13.875 mV, Range: 0.6 A
SMC ADC: 16



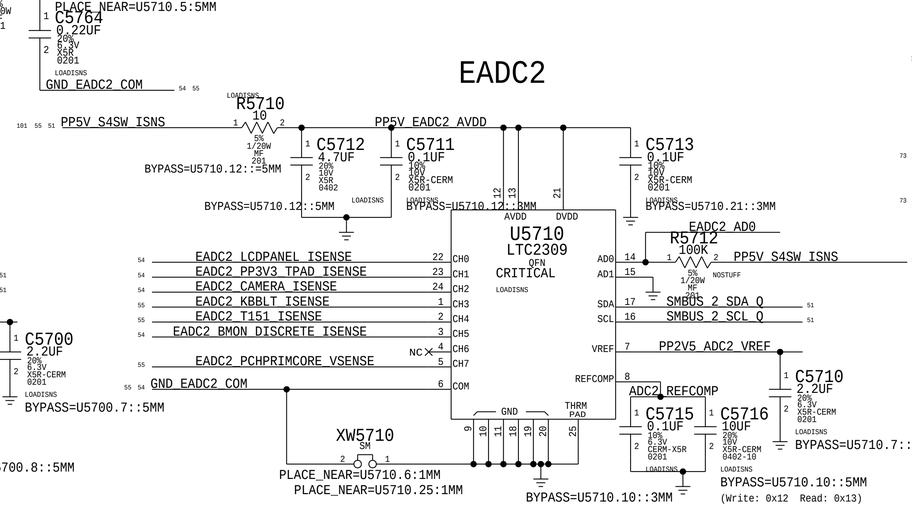
PCH PrimeCore Voltage Sense (VSCC)

EADC2: CH7

EADC1

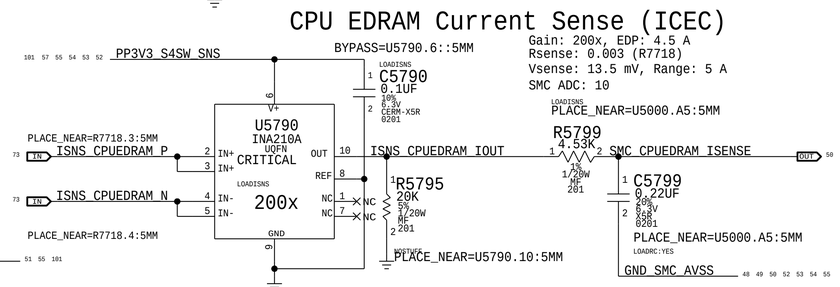


EADC2



CPU EDRAM Current Sense (ICEC)

Gain: 200x, EDP: 4.5 A
Rsense: 0.003 (R7718)
Vsense: 13.5 mV, Range: 5 A
SMC ADC: 10



BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors: Extended 2

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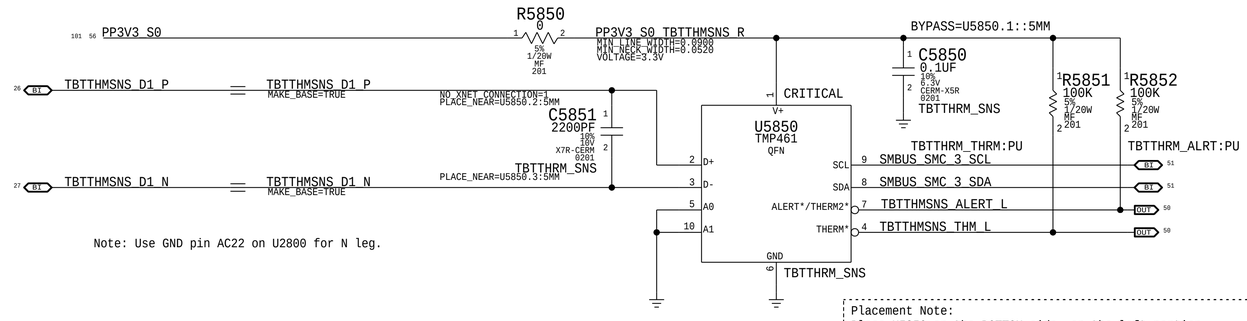
Thermal Sensor A: Thunderbolt Die, Airflow Left

I2C Write: 0xD8, I2C Read: 0xD9

Thermal Diode: TBT Die (TBT1)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.



U5850 I2C Address: TMP461 is 0x90/0x91.

Note: Use GND pin AC22 on U2800 for N leg.

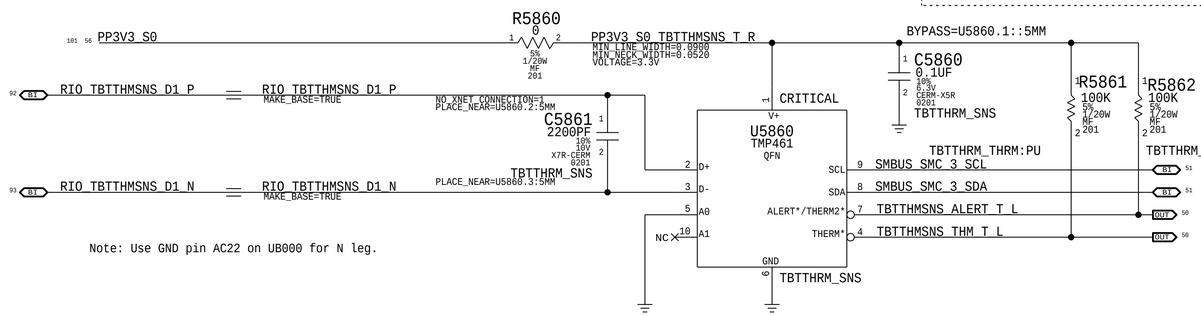
Placement Note:
Place U5850 on the BOTTOM side, on the left portion of the board, 1" to the right of USB connector.

Thermal Sensor C: Thunderbolt Die, Air Flow Right

I2C Write: 0xB8, I2C Read: 0xB9

Thermal Diode: TBT Die (TBT2)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.

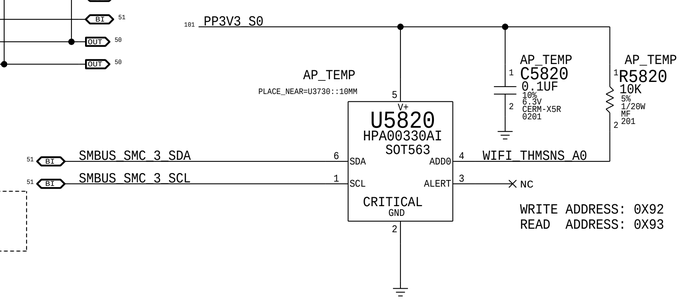


Note: Use GND pin AC22 on UB000 for N leg.

U5860 I2C Address: TMP461 is 0x96/0x97.

Placement Note:
Place U5860 on the BOTTOM side, on the right portion of the board, 1" to the left of USB connector.

X100 PROXIMITY



WRITE ADDRESS: 0X92
READ ADDRESS: 0X93

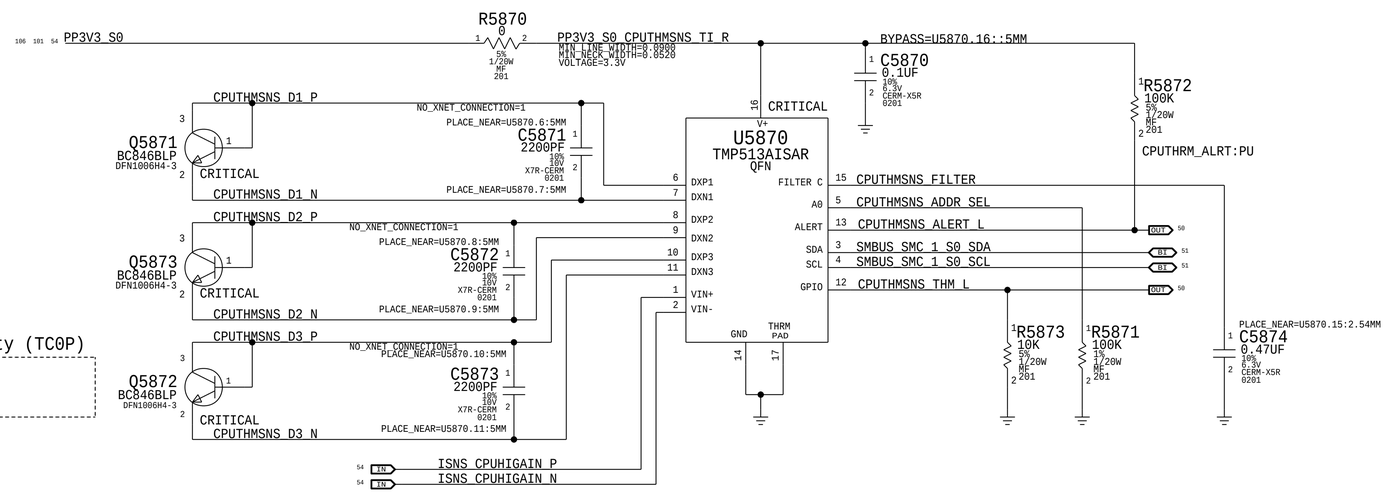
Placement note:
PLACE U5820 ON BOTTOM NEAR X100

Thermal Sensor B & CPU High Peak Detection: CPU Proximity, Memory Proximity, Fin Stack Left, Fin Stack Right

I2C Write: 0xB8, I2C Read: 0xB9

Thermal Diode: Fin Stack Left (Th2H)

Placement Note:
Place Q5871, Airflow thermal indicator, above the X100, on the TOP side.



Thermal Diode: CPU Proximity (TC0P)

Placement Note:
Place Q5873 under the CPU, on the BOTTOM side.

Thermal Diode: Memory Proximity (TM0P)

Placement Note:
Place Q5872 between two rows of Memory devices, between channel A and B, on the BOTTOM side.

Thermal Sensor: Fin Stack Right (Th1H)

Placement Note:
Place U5870 at corner near right Fan, on the TOP side.

BOM_COST_GROUP=SENSORS

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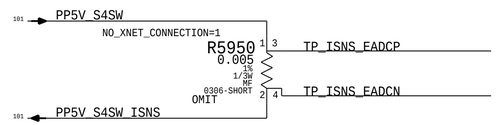
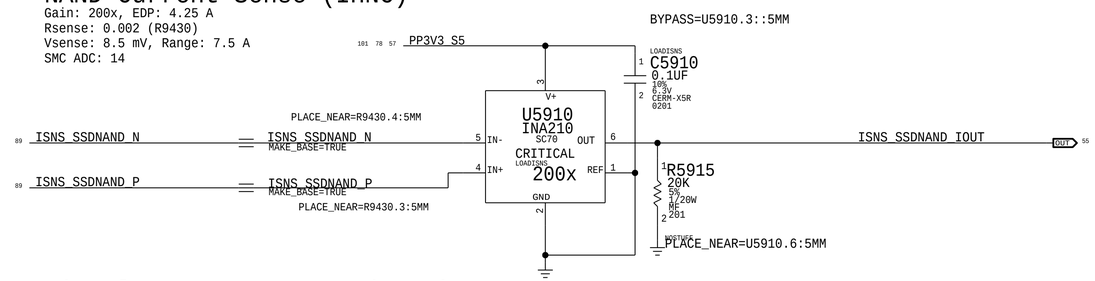
EADC Current Sense (IADC)

Gain: 200x, EDP: 200m A
Rsense: 0.050 (R5950) or Rsense SHORT
Vsense: 10 mV, Range: 0.25 A
EADC2: CH7



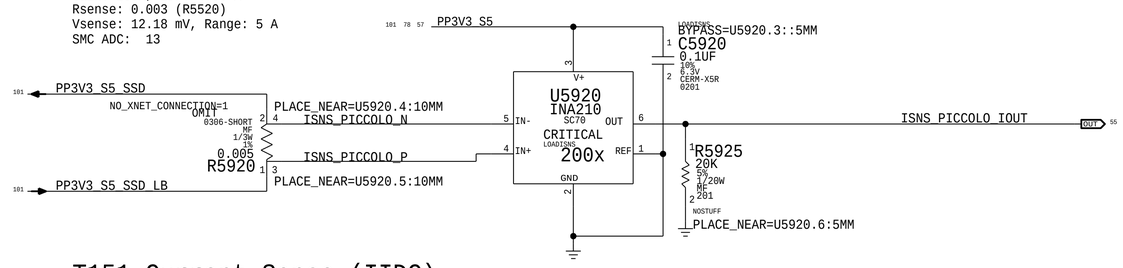
NAND Current Sense (IHNC)

Gain: 200x, EDP: 4.25 A
Rsense: 0.002 (R9430)
Vsense: 8.5 mV, Range: 7.5 A
SMC ADC: 14



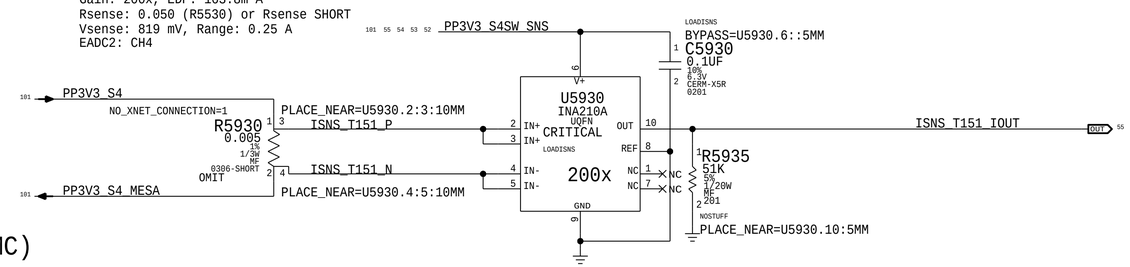
Piccolo Current Sense (IHCC)

Gain: 200x, EDP: 4.06 A
Rsense: 0.003 (R5520)
Vsense: 12.18 mV, Range: 5 A
SMC ADC: 13



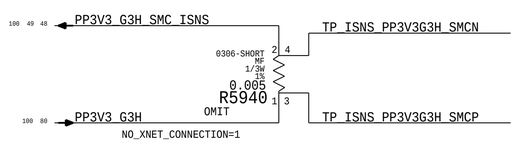
T151 Current Sense (IIDC)

Gain: 200x, EDP: 163.8m A
Rsense: 0.050 (R5530) or Rsense SHORT
Vsense: 819 mV, Range: 0.25 A
EADC2: CH4



SMC Current Sense (ISMC)

Gain: 391.67x, EDP: 0.2 A
Rsense: 0.05 (R5940) or Rsense SHORT
Vsense: 10 mV, Range: 0.21A
EADC2: CH6



BOM_COST_GROUP=SENSORS

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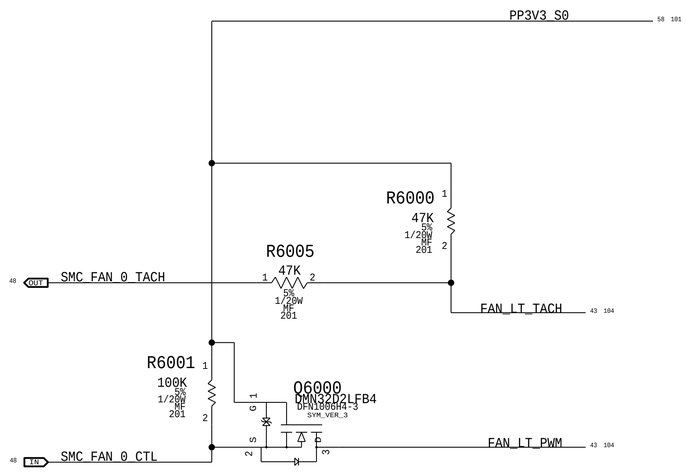
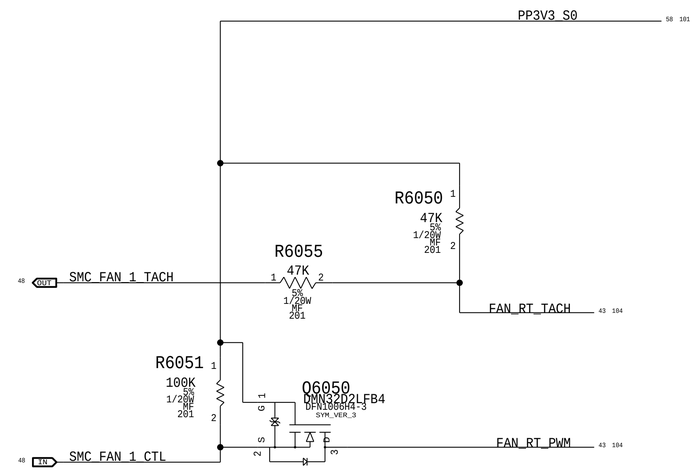
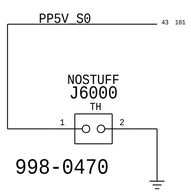
FAN CONTROL





FOR DEBUG FAN POWER



BOM_COST_GROUP=FAN

SYNC_MASTER=J70_JACK SYNC_DATE=08/21/2015

PAGE TITLE

Fans

Apple Inc.

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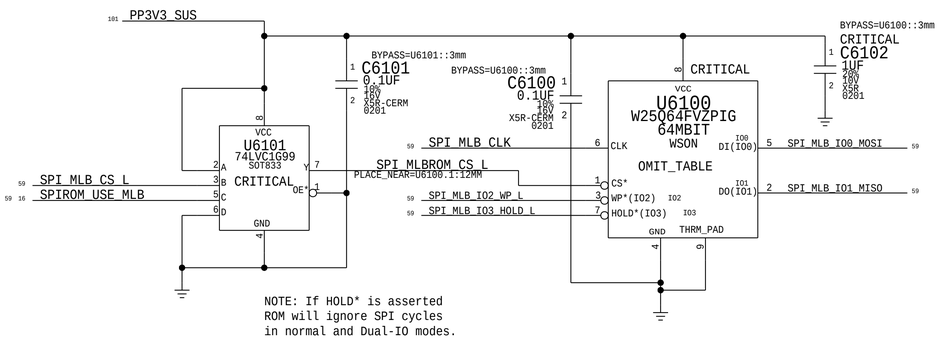
SPI ROM

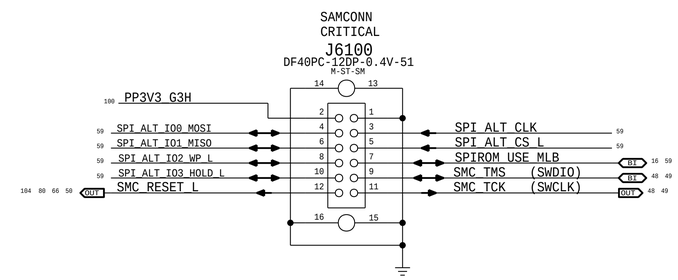
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



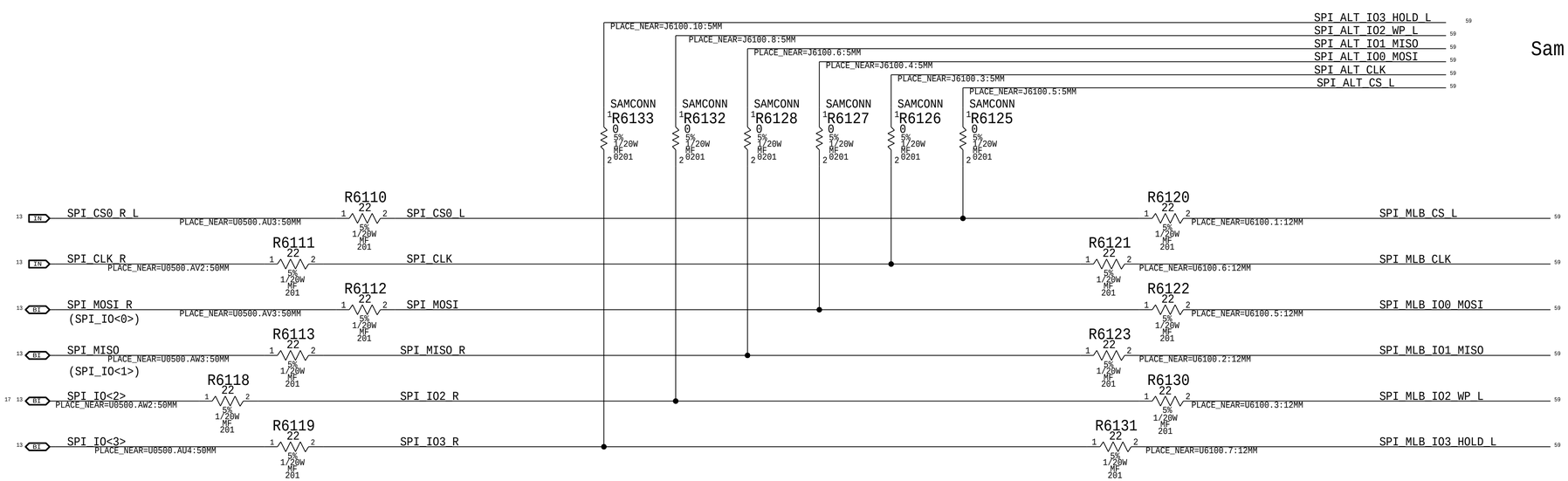
NOTE: If HOLD* is asserted
ROM will ignore SPI cycles
in normal and Dual-IO modes.

Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE)
in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

SPI+SWD SAM Connector



SPI Bus Series Termination (Modified per PDG)



BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J52_MLB SYNC_DATE=05/12/2015

PAGE TITLE
SPI Debug Connector

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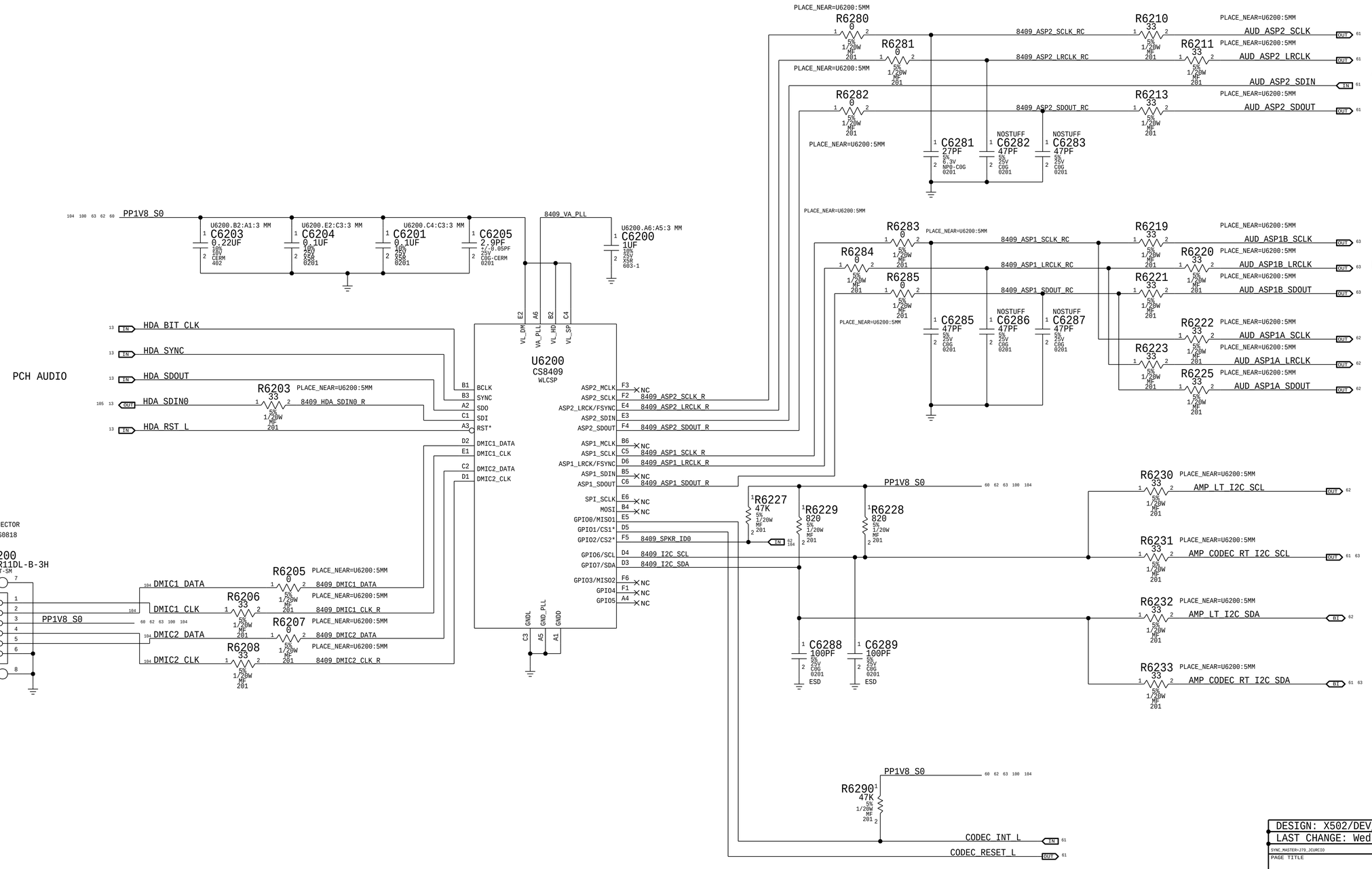

DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17:12:24 2015

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HDA Bridge

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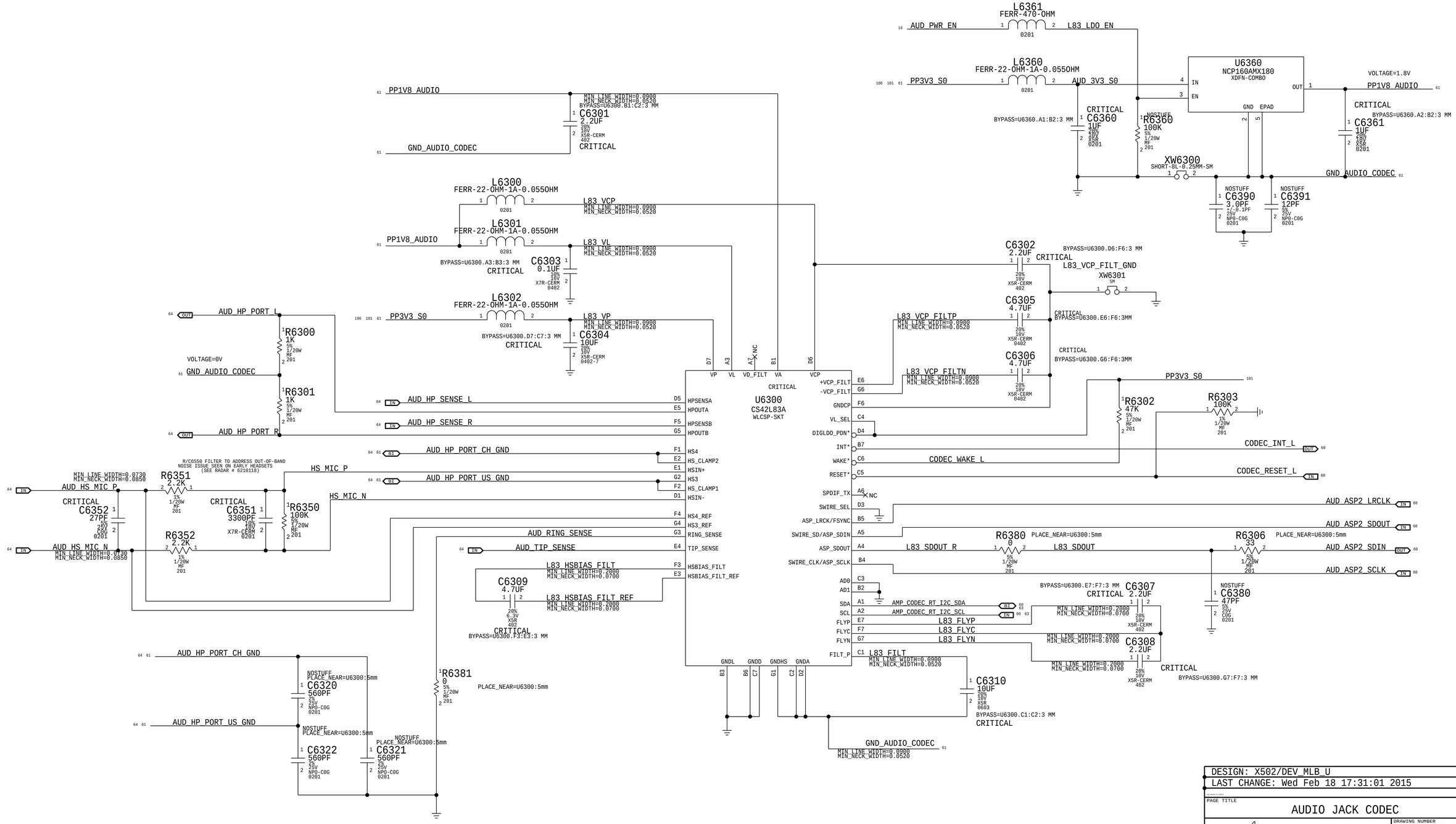
AUDIO JACK CODEC I2C ADDRESS

AD1	AD0	ADDRESS
GND	GND	0x90 <--
GND	1.8V	0x92
1.8V	GND	0x94
1.8V	1.8V	0x96



BOM_COST_GROUP=AUDIO

DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17:31:01 2015

PAGE TITLE
AUDIO JACK CODEC

Apple Inc.

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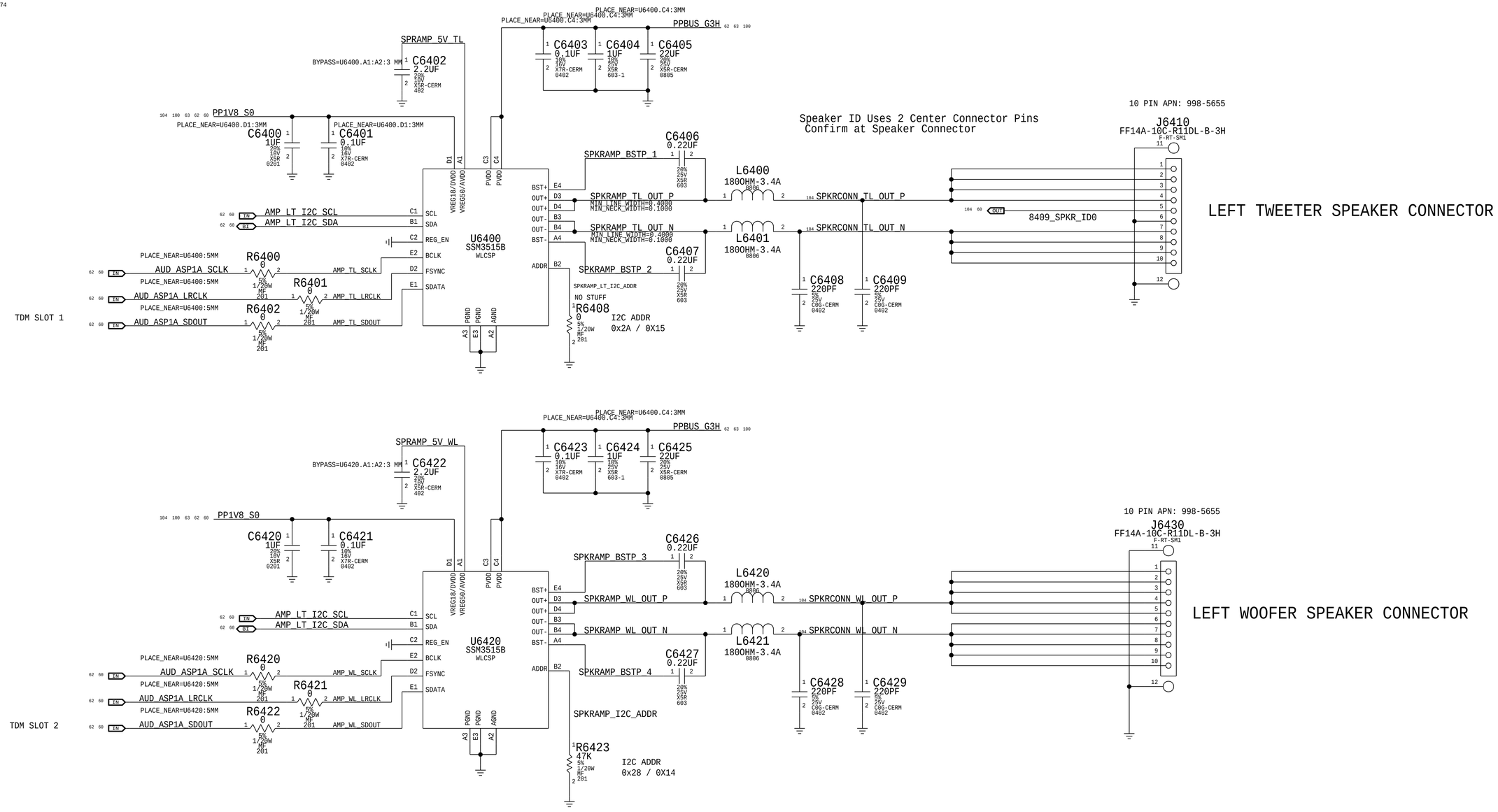
2X MONO SPEAKER AMPLIFIERS
APN: 353S4074
GAIN = TBD



BOM_COST_GROUP=AUDIO

DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17:12:24 2015

PAGE TITLE
Left Speaker Amps & Conn

Apple Inc.

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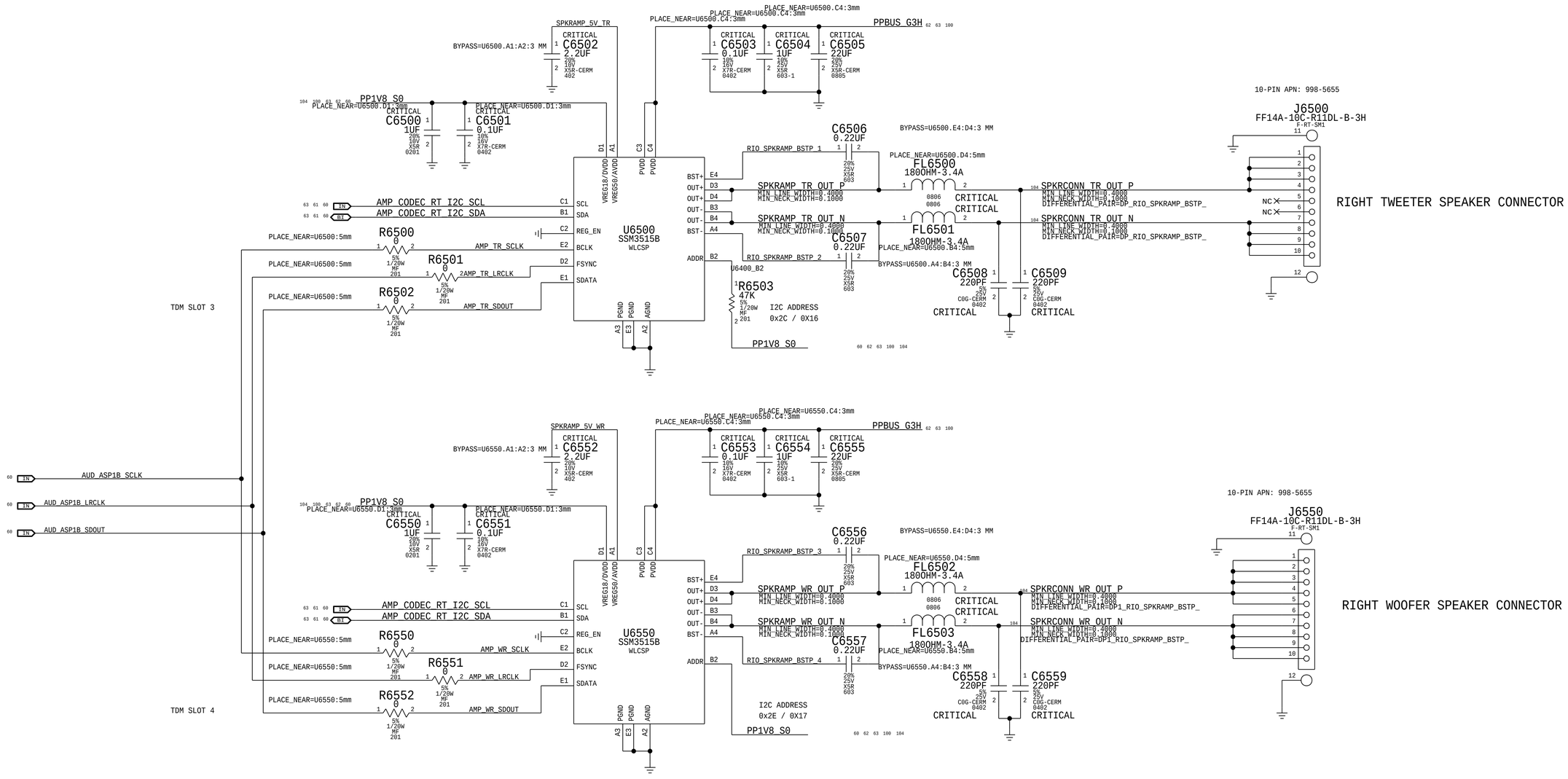
2X MONO SPEAKER AMPLIFIERS
APN: 353S4073
GAIN = TBD



DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17:12:24 2015

PAGE TITLE
Right Speaker Amps & Conn

Apple Inc.

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CODEC OUTPUT SIGNAL PATHS

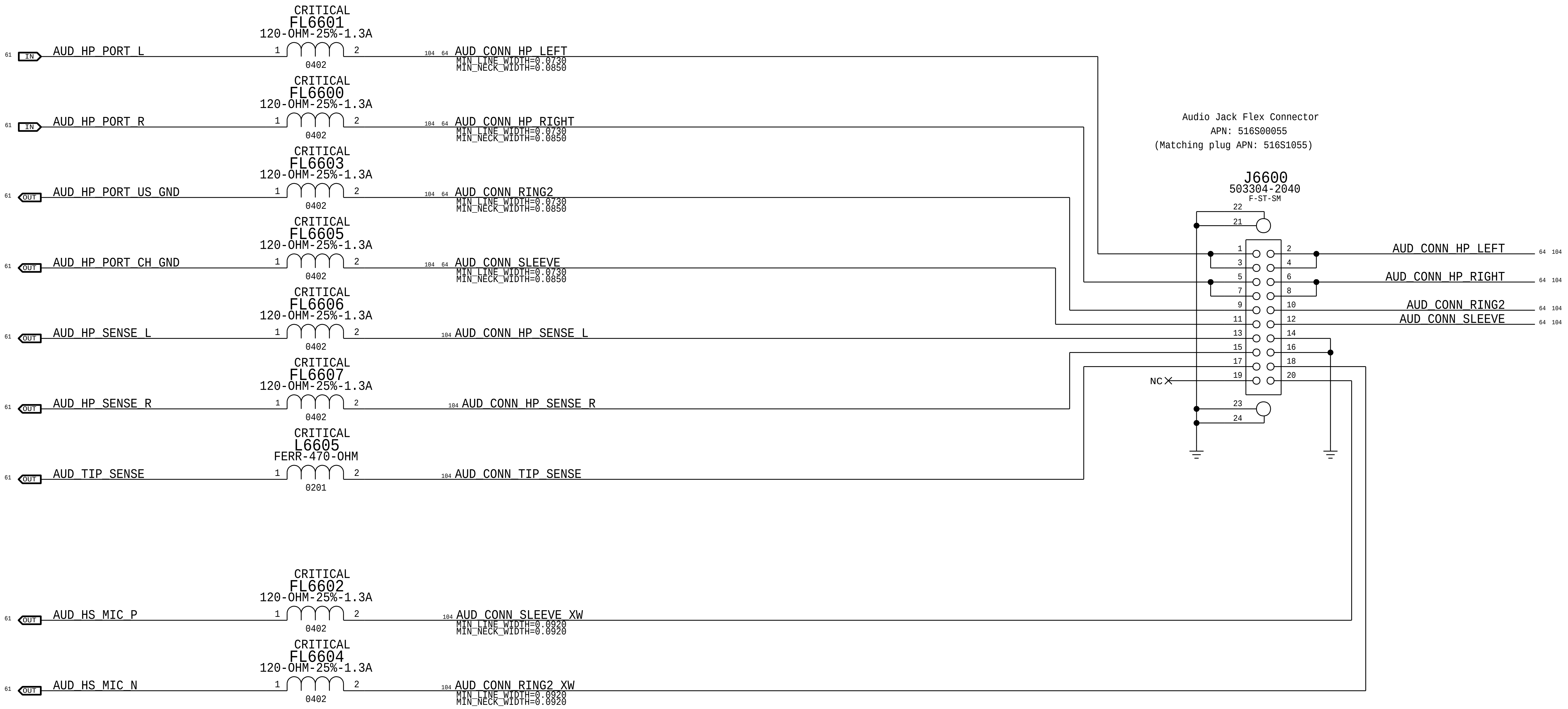
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

[redacted]

[redacted]	GPIO2	INPUT	HIGH = FG, LOW = MERRY
[redacted]	GPIO3	INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4	OUTPUT	HIGH = DFETs OPEN

CODEC INPUT SIGNAL PATHS

[redacted]	[redacted]	[redacted]	VREF
DMIC	[redacted]	[redacted]	3.3V
DMIC	[redacted]	[redacted]	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V



BOM_COST_GROUP=AUDIO

DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17:12:24 2015
SYNC_MASTER=J79_JCURCIO
SYNC_DATE=12/18/2015

PAGE TITLE
AUDIO JACK CONNECTOR

Apple Inc.

DRAWING NUMBER 051-00515
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 66 OF 145
SHEET 64 OF 119

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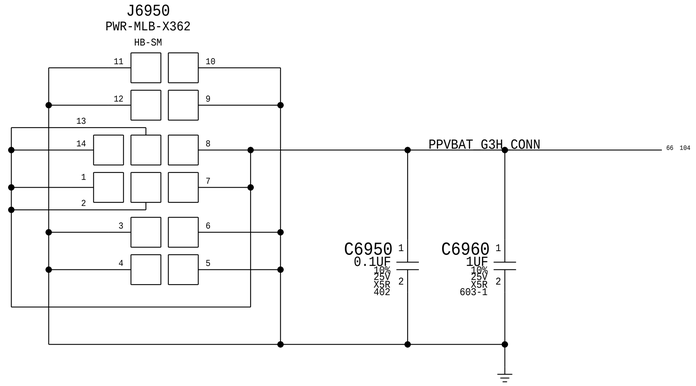
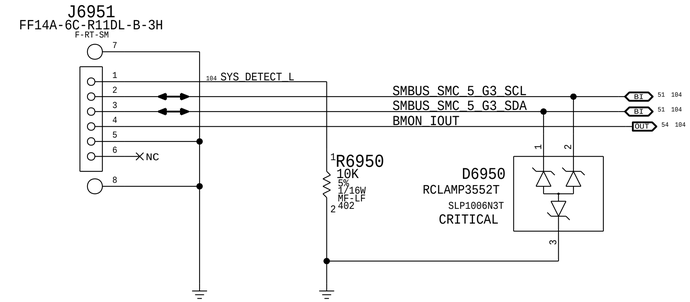
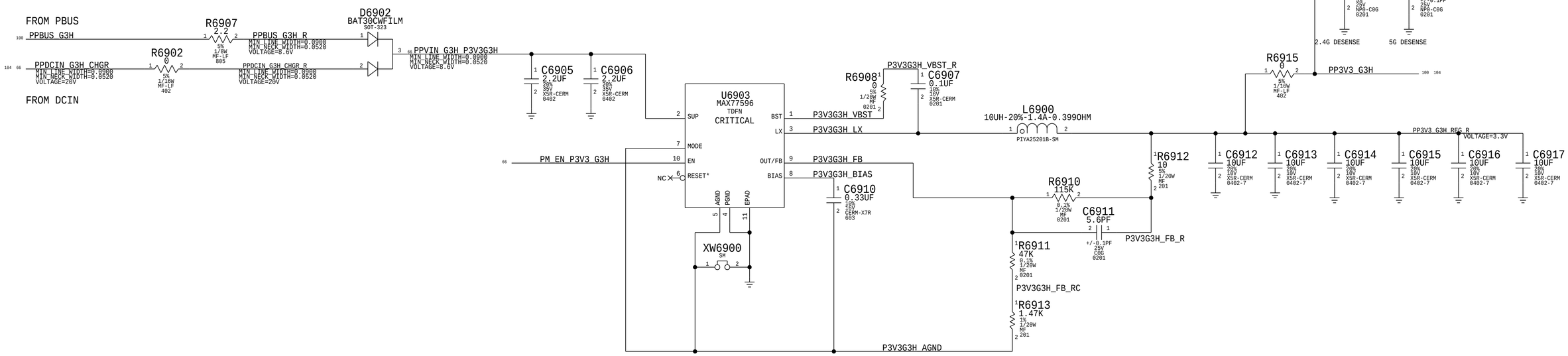
J79 Battery Hotbar Flex Pads





BMU POWER FLEX HOTBAR'd TO THE MLB:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-00566	1	PCBA,FLEX,BMU PWR,X362	J6950	CRITICAL	

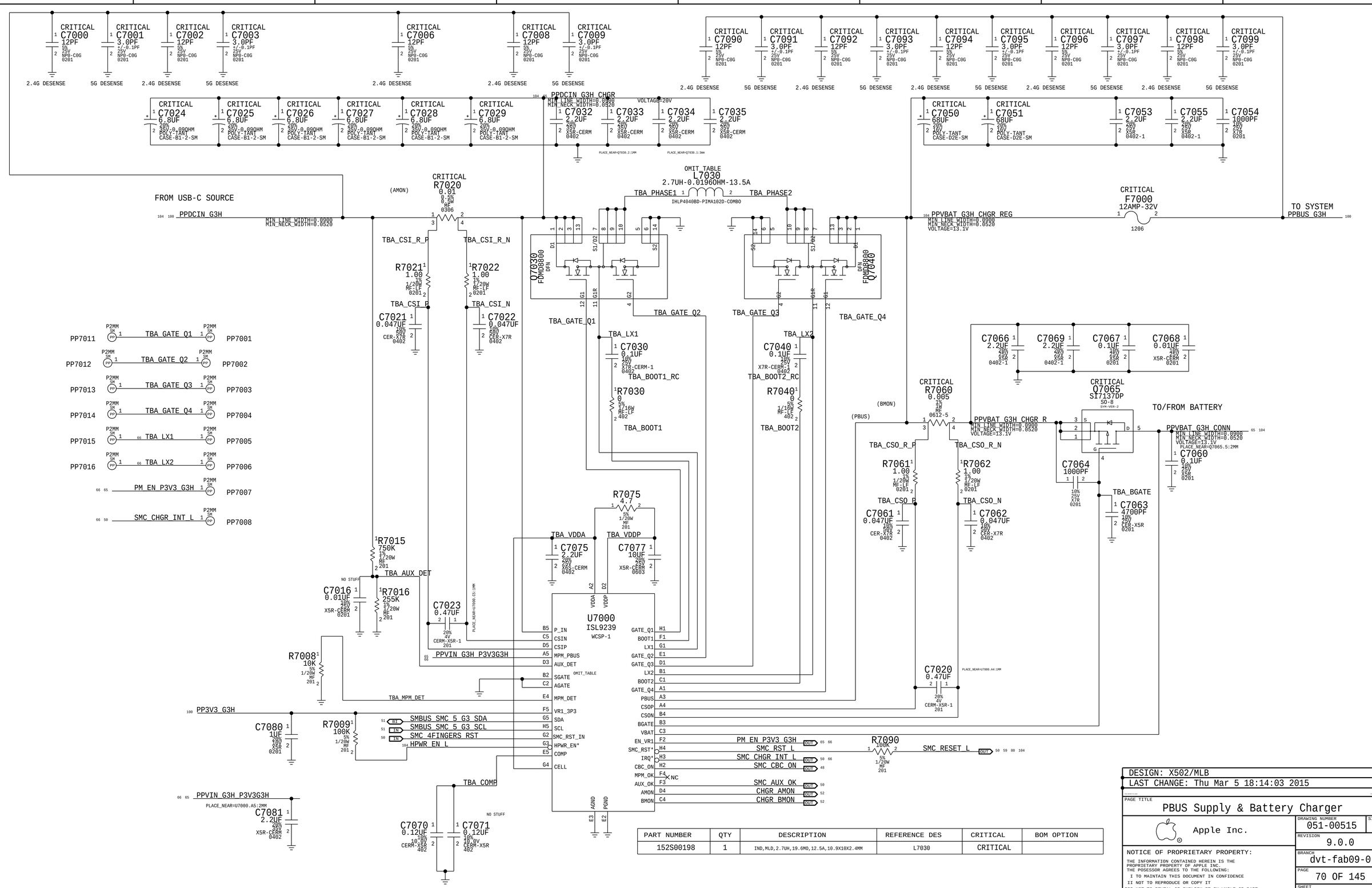


BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER 051-00515
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 69 OF 145
SHEET 65 OF 119



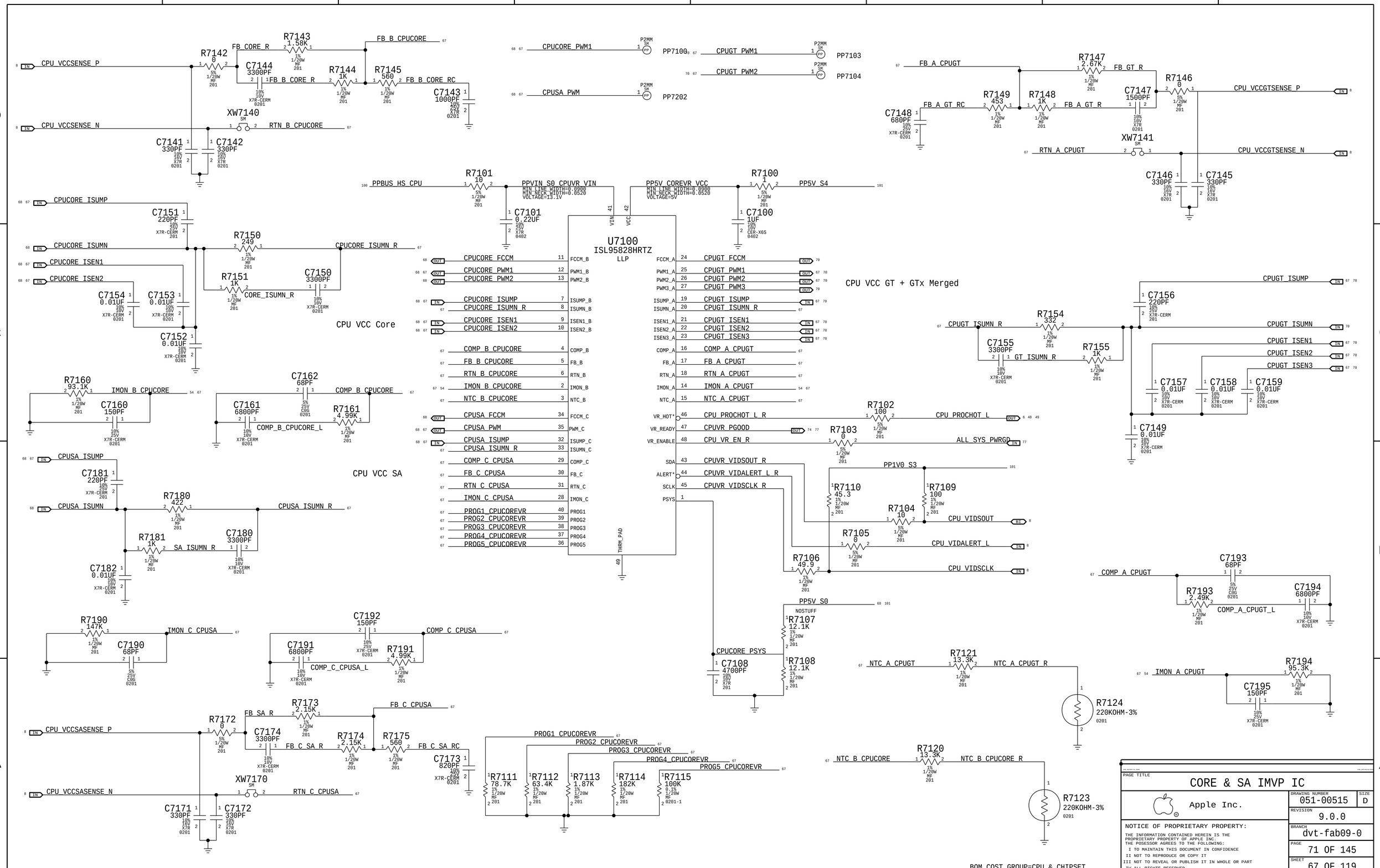
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00198	1	IND,MLD,2.7UH,19.6MΩ,12.5A,10.9X10X2.4MM	L7030	CRITICAL	

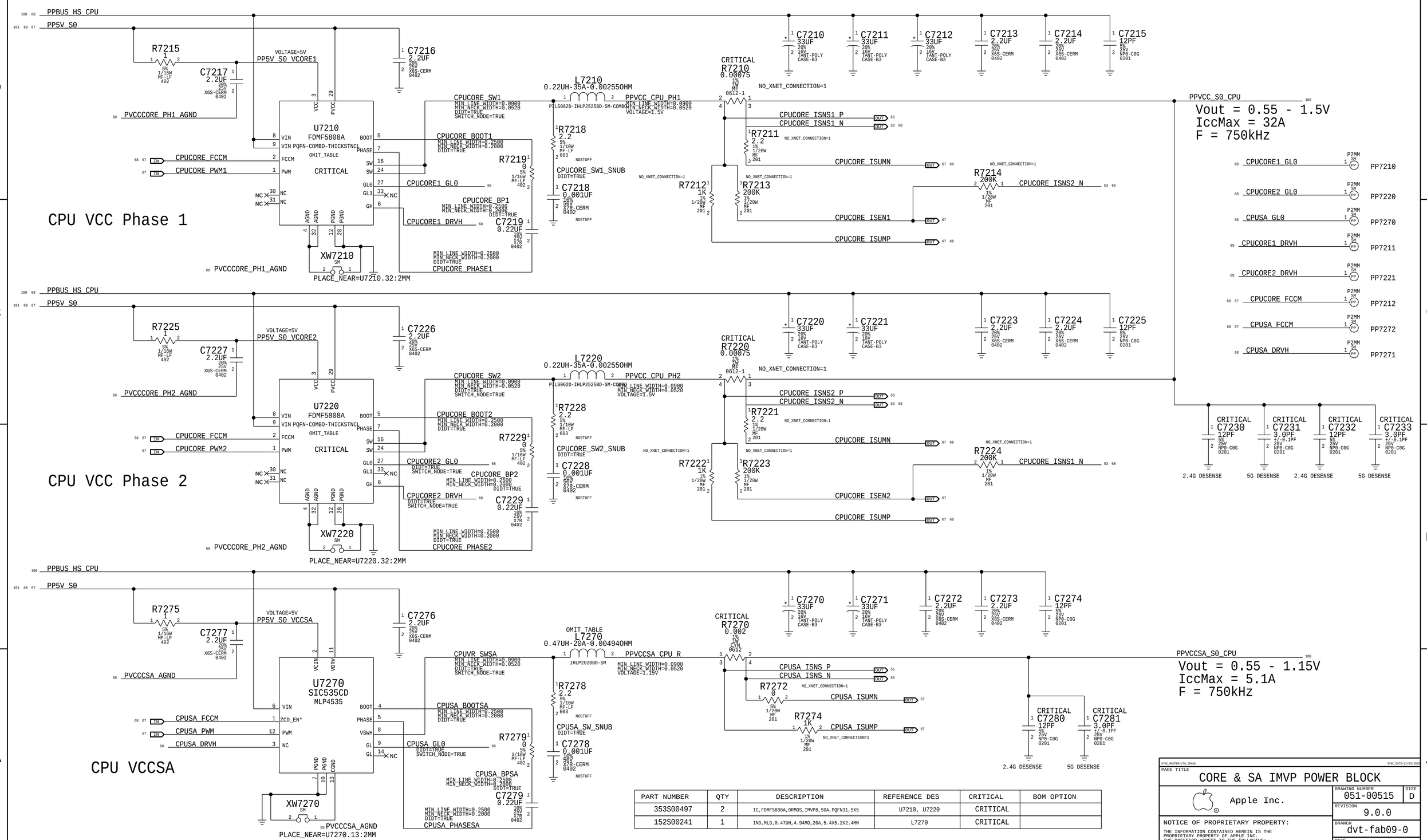
DESIGN: X502/MLB
LAST CHANGE: Thu Mar 5 18:14:03 2015

PAGE TITLE
PBUS Supply & Battery Charger

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 70 OF 145
SHEET 66 OF 119





PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00497	2	IC,FDMF5808A,DRMOS,IMVP8,50A,PQFN31,5X5	U7210, U7220	CRITICAL	
152S00241	1	IND,MLD,0.47UH,4.94MO,20A,5.4X5.2X2.4MM	L7270	CRITICAL	

PAGE TITLE
CORE & SA IMVP POWER BLOCK

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 72 OF 145
SHEET 68 OF 119

SYNC_MASTER=J79_SILUCHEN SYNC_DATE=04/02/2015

PAGE TITLE

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Apple Inc.

DRAWING NUMBER 051-00515

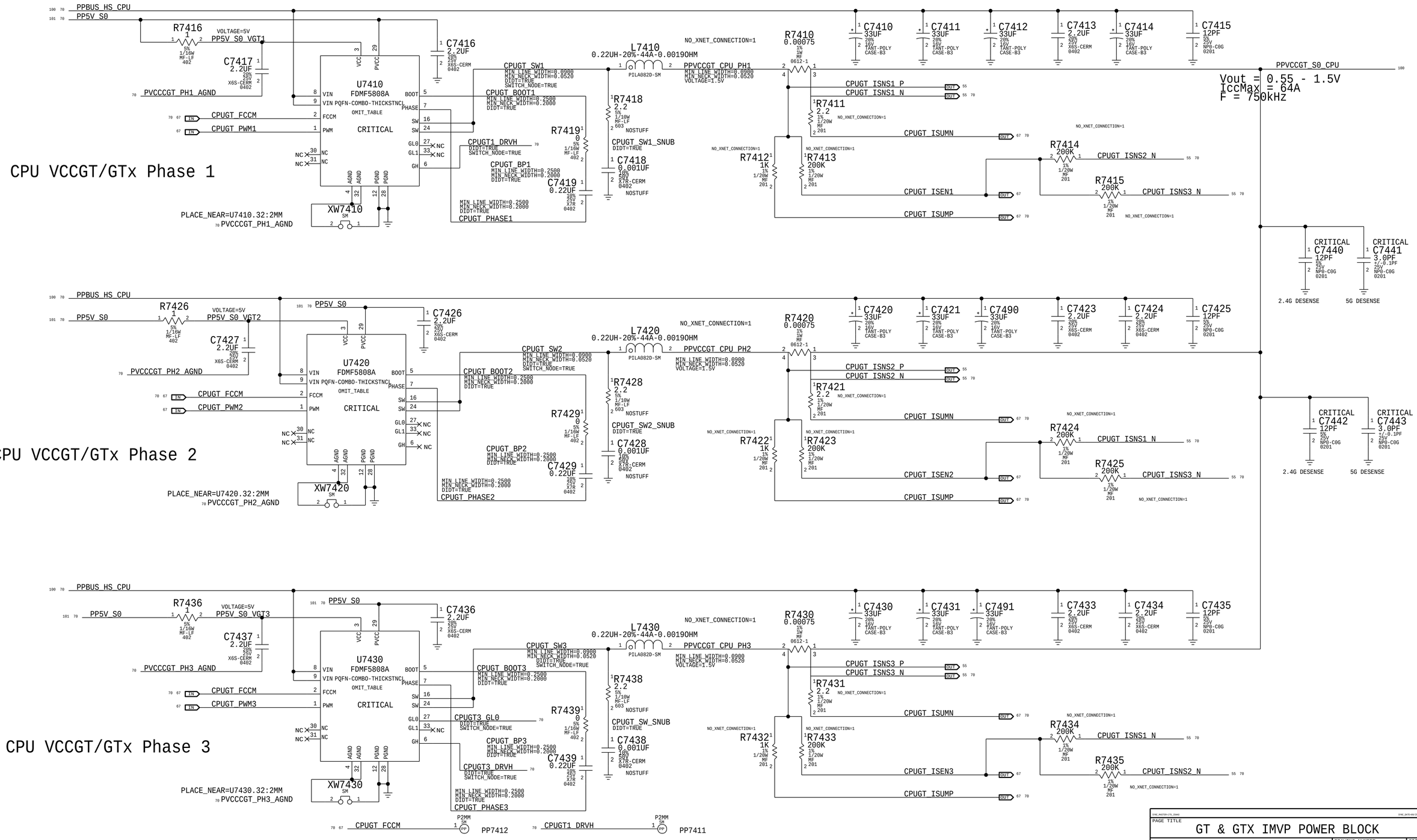
SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 73 OF 145

SHEET 69 OF 119



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00497	3	IC,FDMF808A,DRMOS,IMVP8,50A,PQFN31,5X5	U7410, U7420, U7430	CRITICAL	

PAGE TITLE
GT & GTX IMVP POWER BLOCK

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 74 OF 145
SHEET 70 OF 119

SYNC_MASTER=J79_SILUCHEN SYNC_DATE=03/27/2015

PAGE TITLE

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Apple Inc.

DRAWING NUMBER 051-00515

SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

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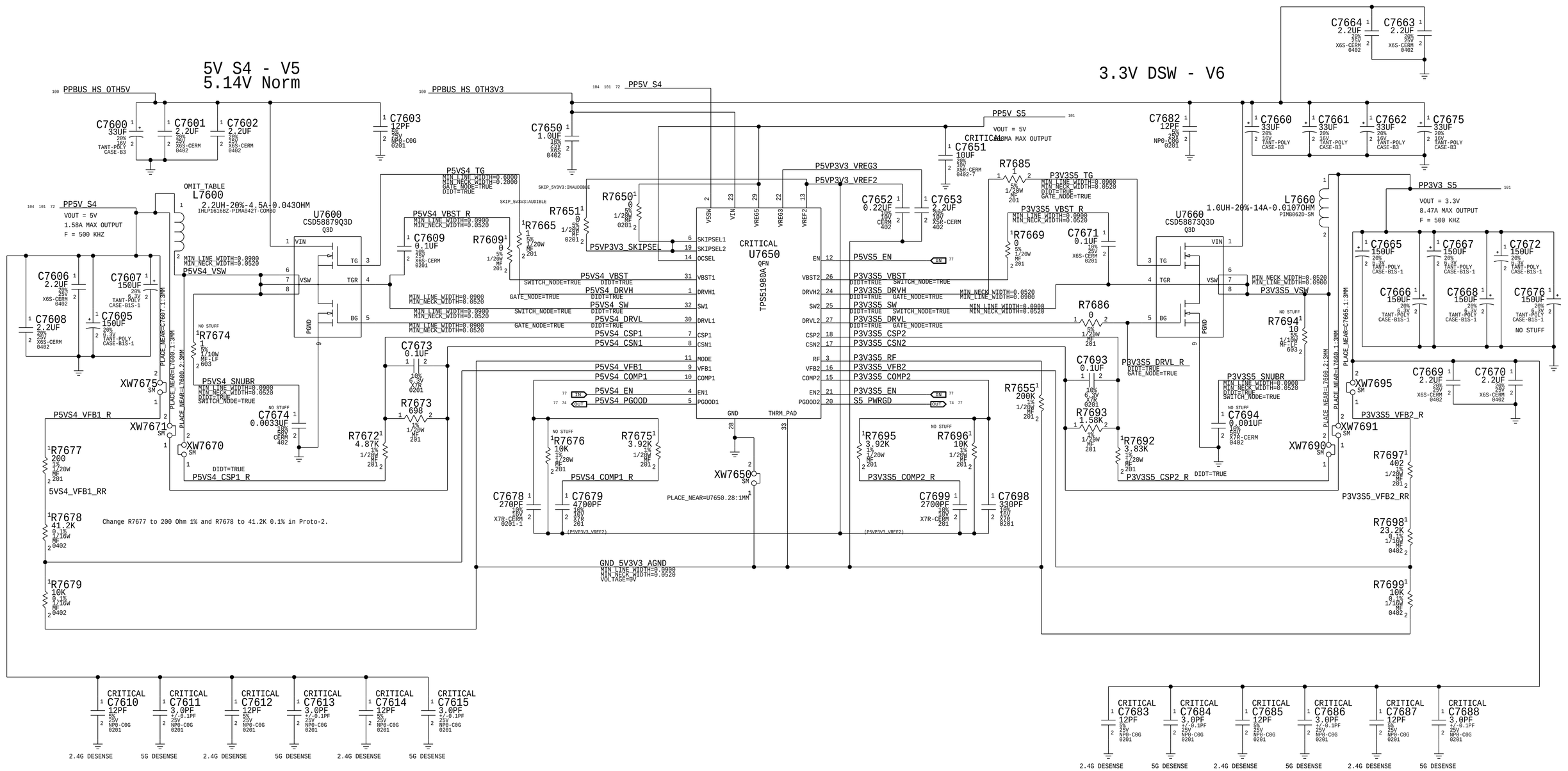
SHEET 71 OF 119



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00182	1	IND,PWR,2.2UH,20%,4.5A,43MOHM,4X4MM	L7600	CRITICAL	

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
Power - 5V 3.3V Supply

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
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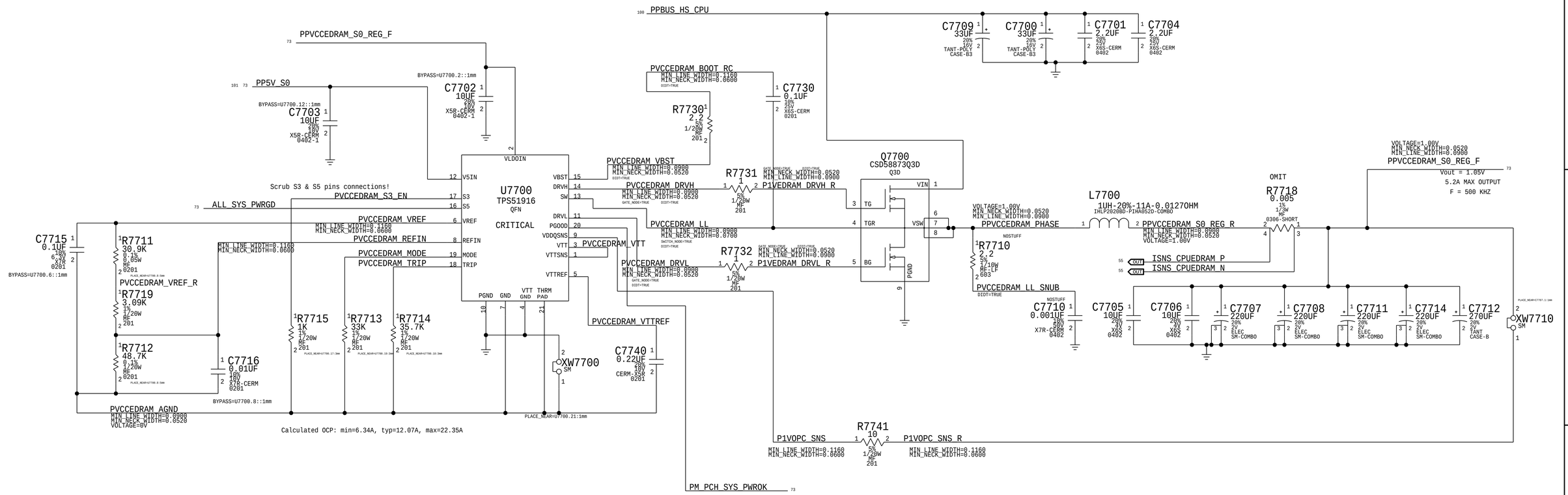
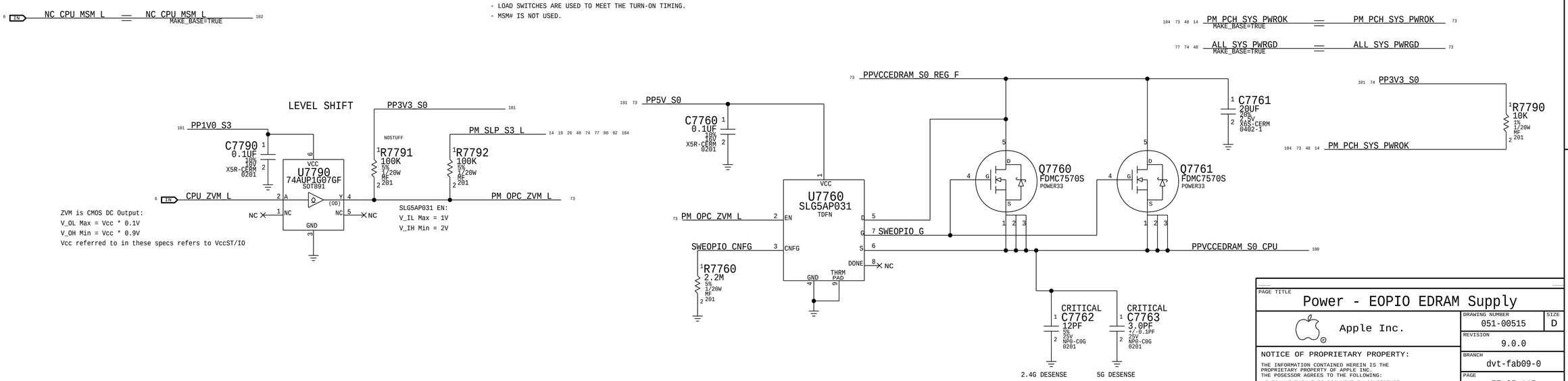
1V EDRAM & EOPIO



THE FOLLOWING SHORTCUTS ARE USED:
- OPC (EDRAM) IS POWERED FROM ONE VR.
- LOAD SWITCHES ARE USED TO MEET THE TURN-ON TIMING.
- MSM# IS NOT USED.



BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
Power - EOPIO EDRAM Supply

Apple Inc.

DRAWING NUMBER 051-00515
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
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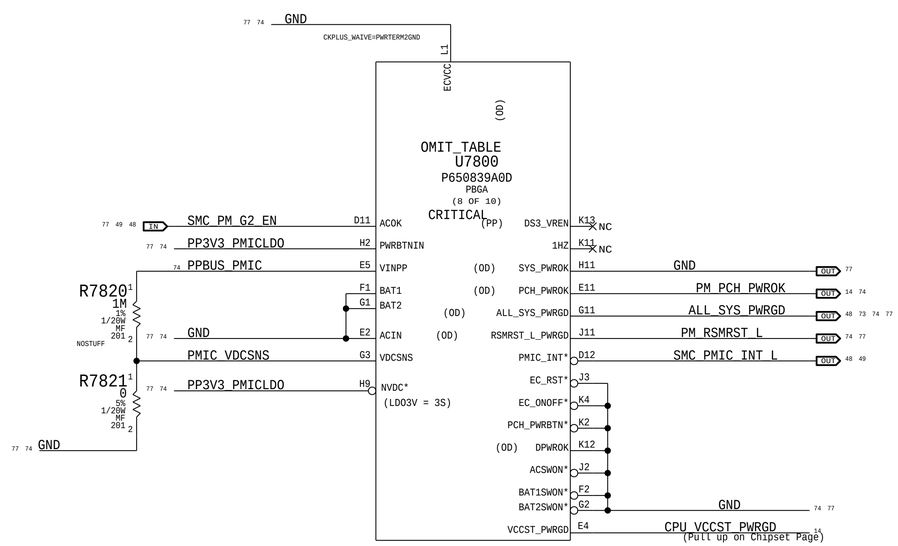
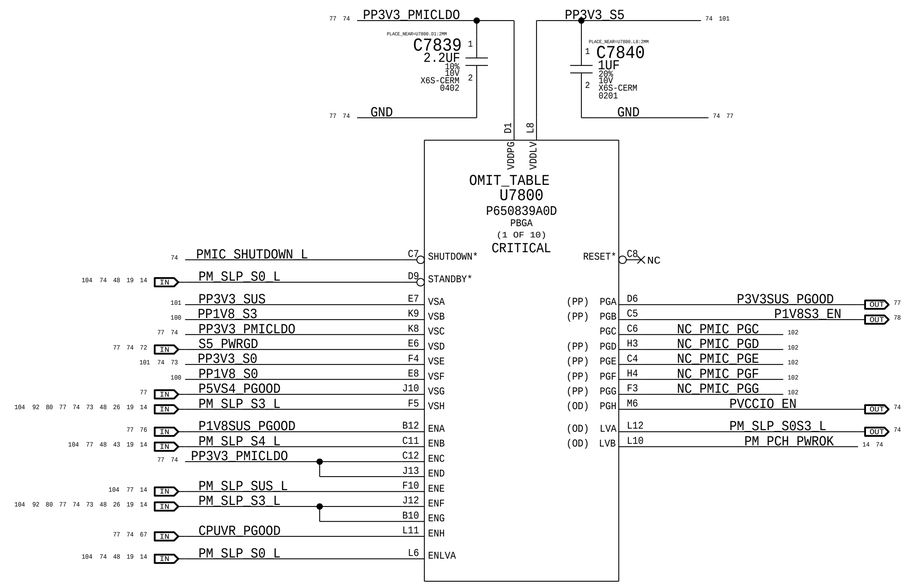
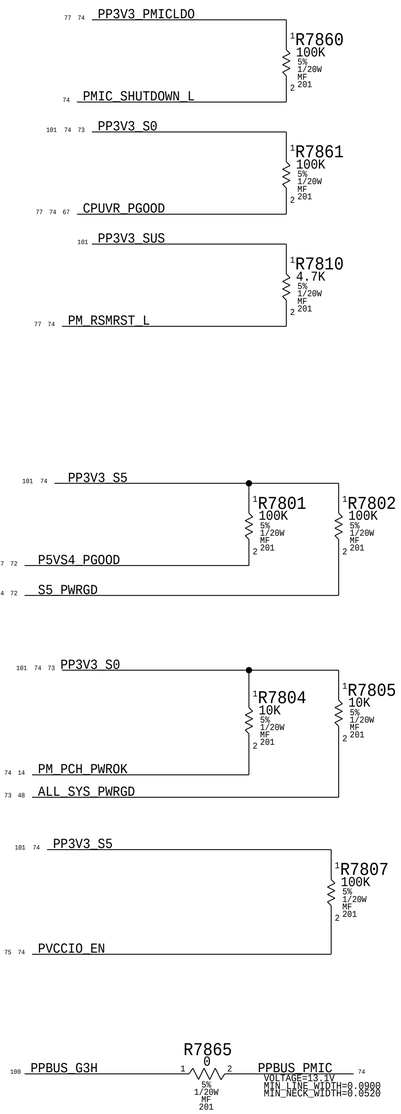
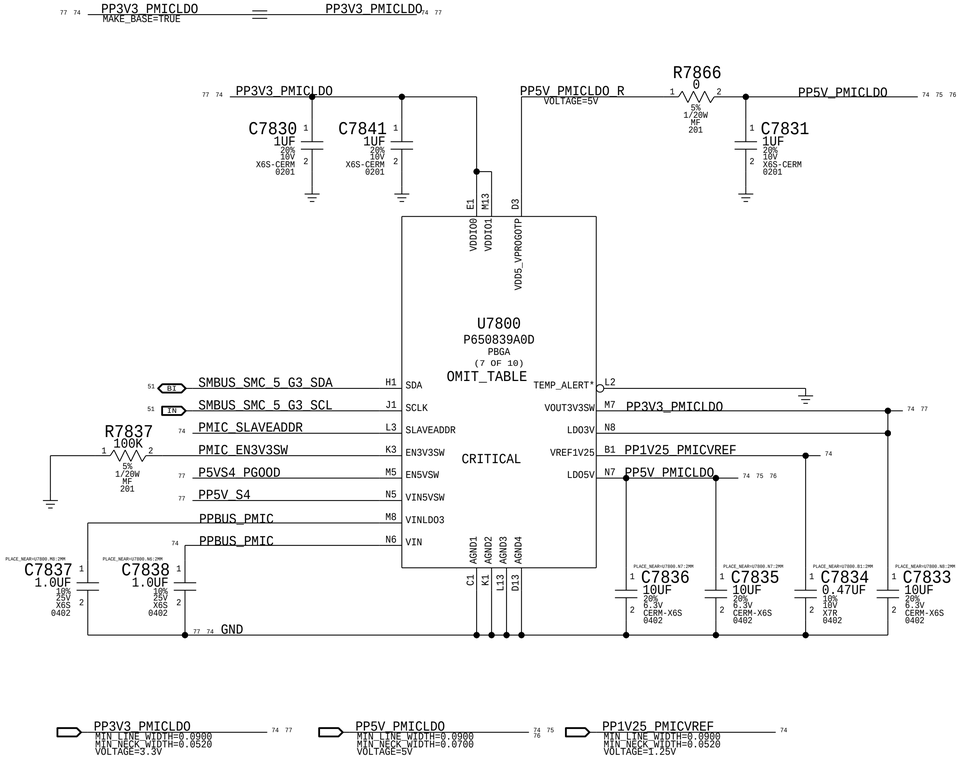
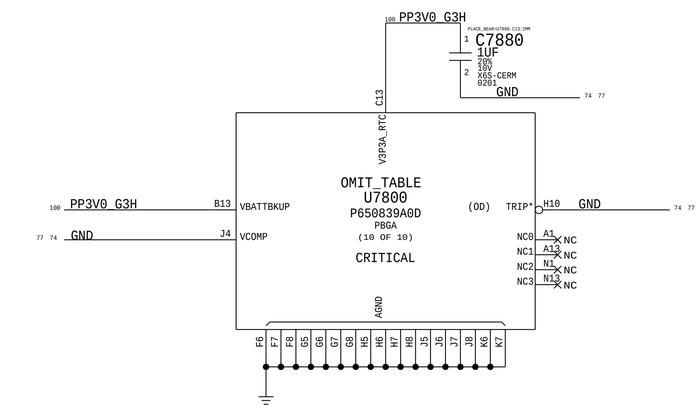
BANJO - PMIC Control

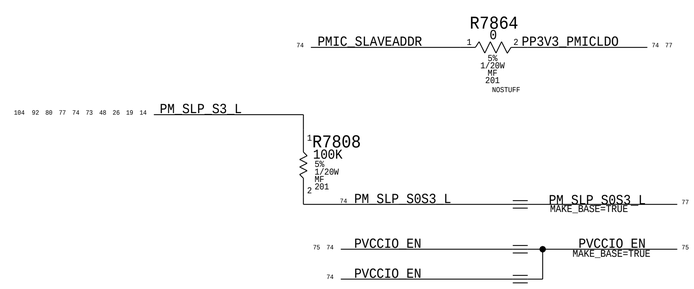












BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE	PMIC-1 & Power Control
Apple Inc.	DRAWING NUMBER 051-00515 SIZE D
	REVISION 9.0.0
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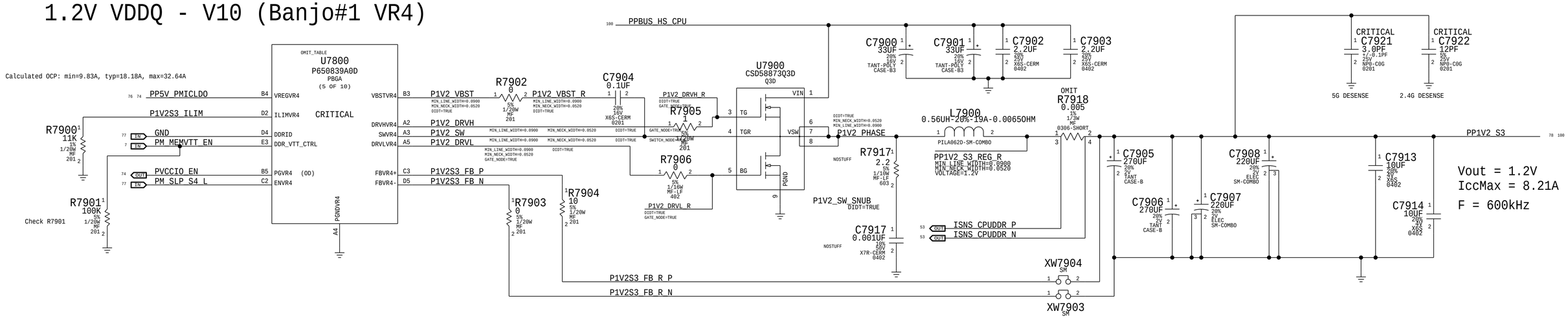
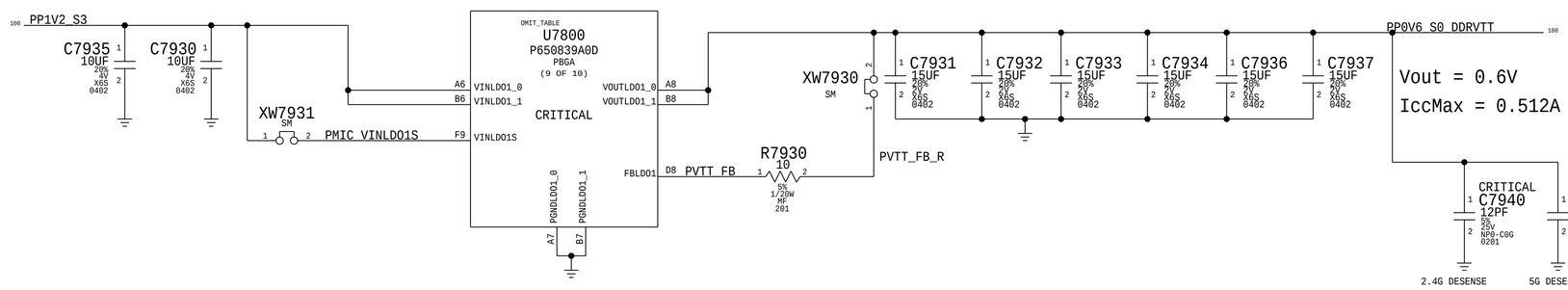
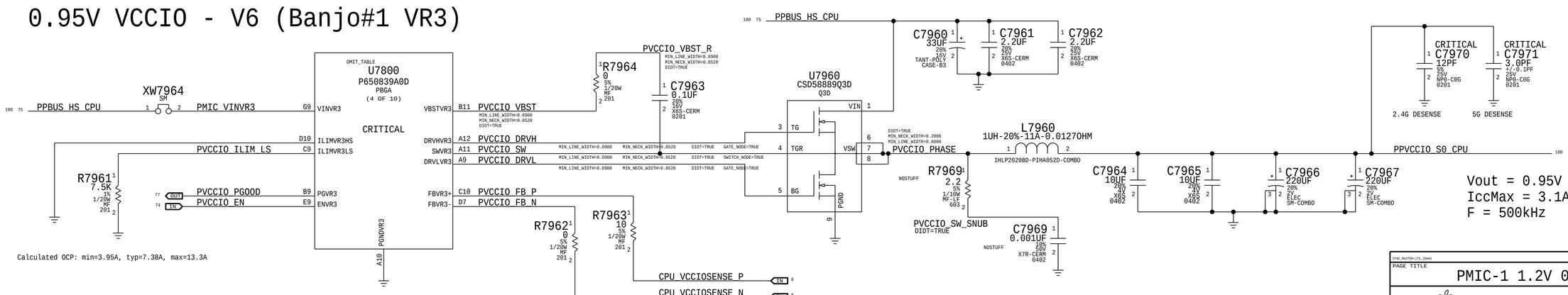
1.2V VDDQ - V10 (Banjo#1 VR4)



0.6V VTT - V13 (Banjo#1 LDO1)



0.95V VCCIO - V6 (Banjo#1 VR3)



BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
PMIC-1 1.2V 0.6V VCCIO

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 79 OF 145
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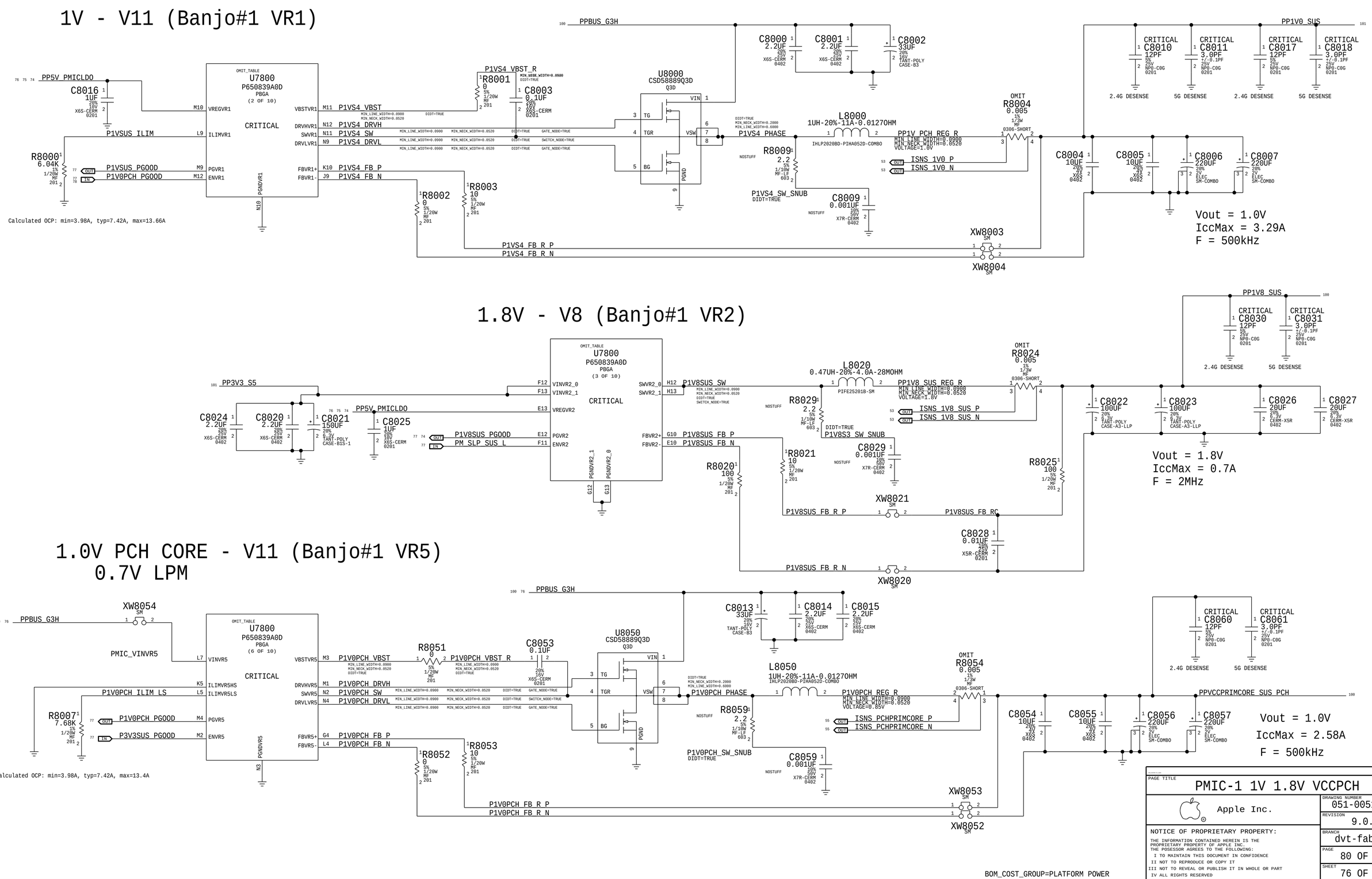

PAGE TITLE
PMIC-1 1V 1.8V VCCPCH

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
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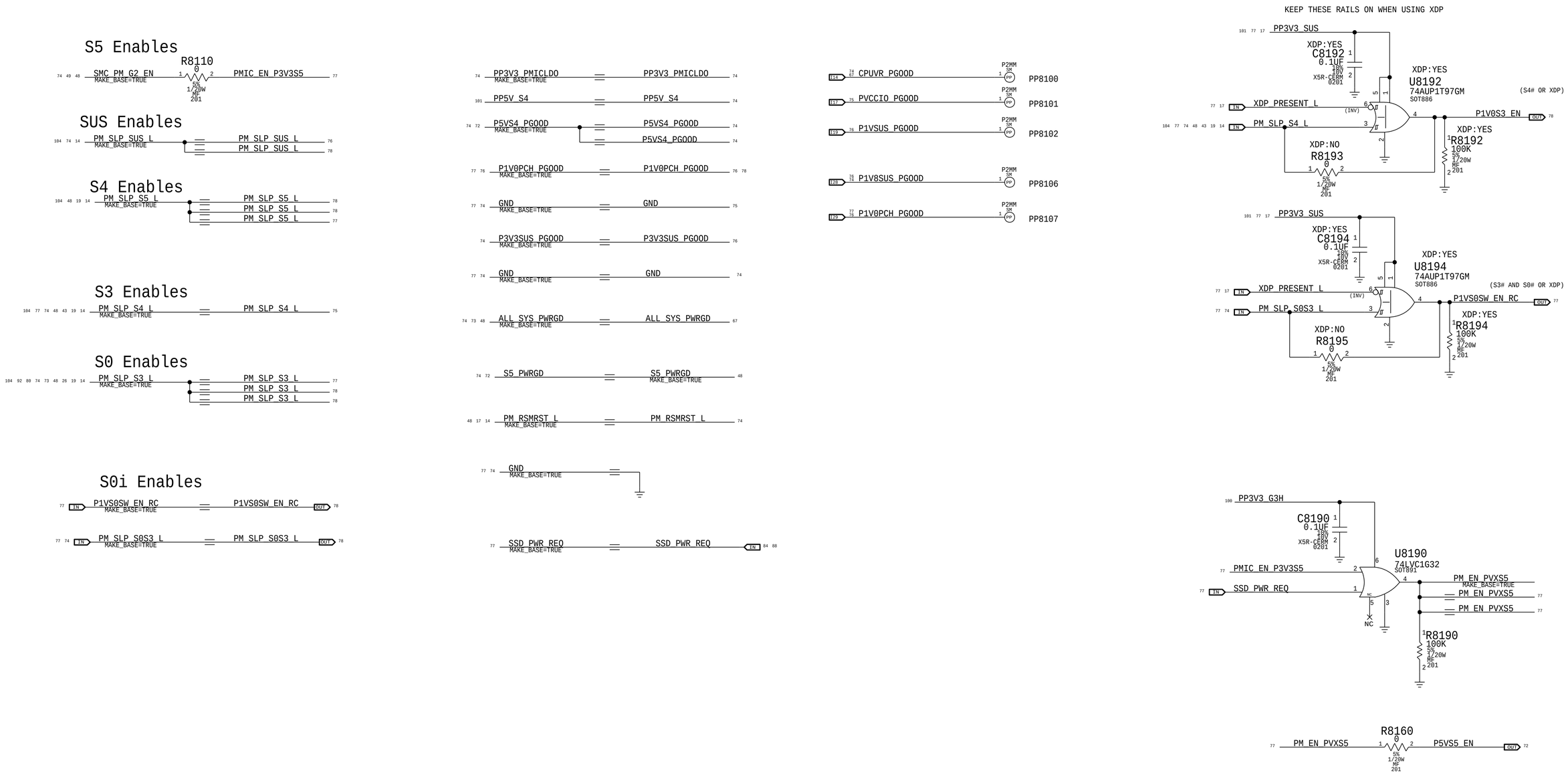

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE

PMIC-1 Aliases & TPs

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

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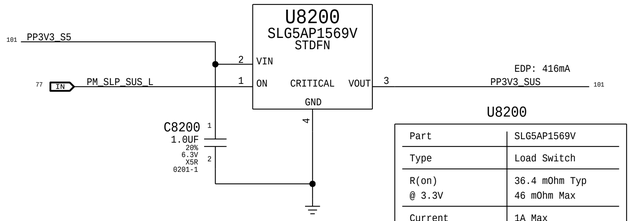
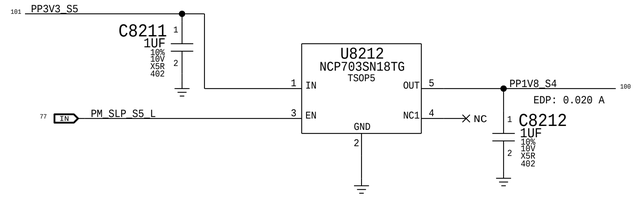
3.3V SUS Switch



U8200

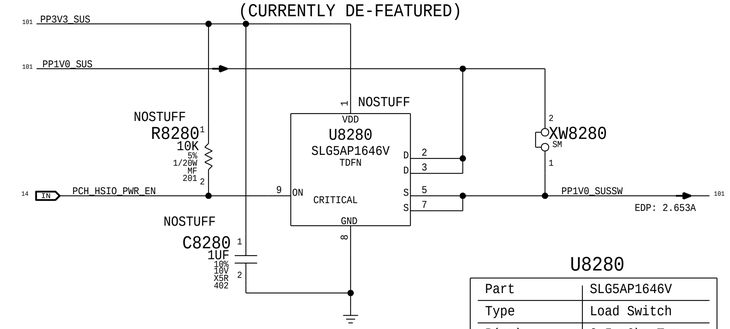
Part	SLG5AP1569V
Type	Load Switch
R(on) @ 3.3V	36.4 mOhm Typ 46 mOhm Max
Current	1A Max

1.8V S4 LDO



1.0V SUS SW Switch

(CURRENTLY DE-FEATURED)

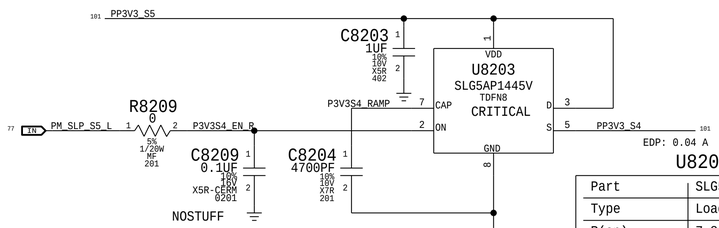


HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

U8280

Part	SLG5AP1646V
Type	Load Switch
R(on) @ 4V Vgs	8.5 mOhm Typ 9.8 mOhm Max
Current	6A Max

3.3V S4 Switch



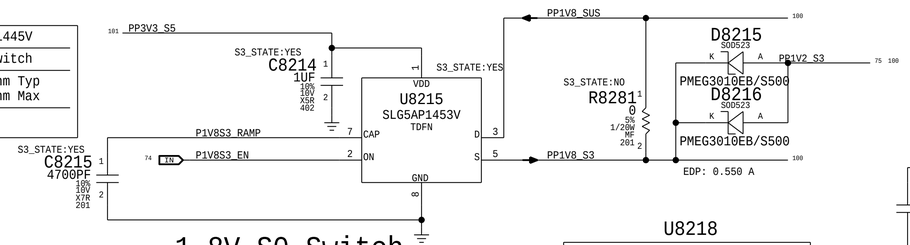
U8203

Part	SLG5AP1445V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ TBD mOhm Max
Current	4A Max

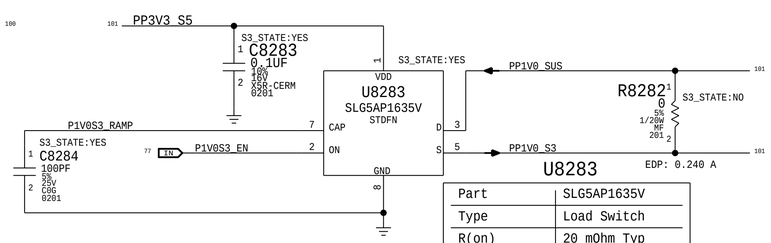
U8215

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

1.8V S3 Switch



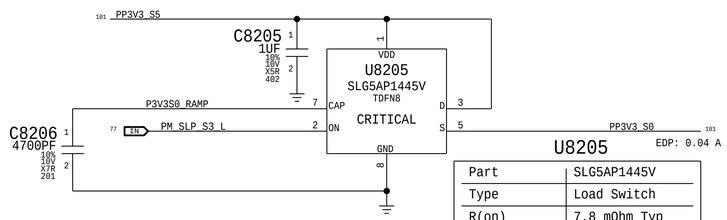
1.0V S3 Switch



U8283

Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 mOhm Typ 28 mOhm Max
Current	2.5A Max
Ton Total	39us max @ 1V

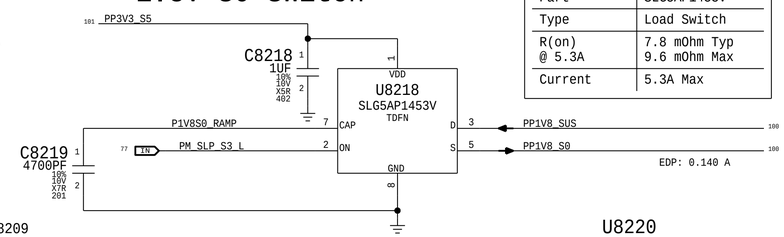
3.3V S0 Switch



U8205

Part	SLG5AP1445V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ TBD mOhm Max
Current	4A Max

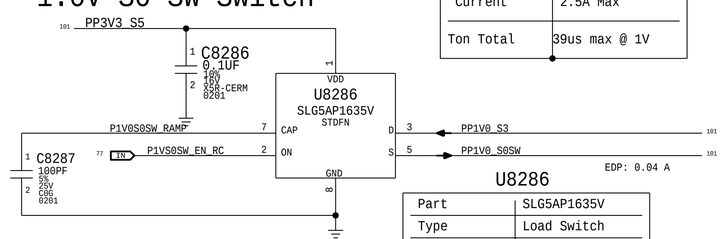
1.8V S0 Switch



U8218

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

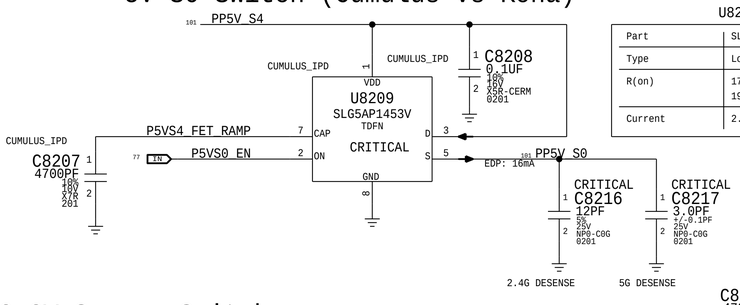
1.0V S0 SW Switch



U8286

Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 mOhm Typ 28 mOhm Max
Current	2.5A Max
Ton Total	39us max @ 1V

5V S0 Switch (Cumulus vs Kona)



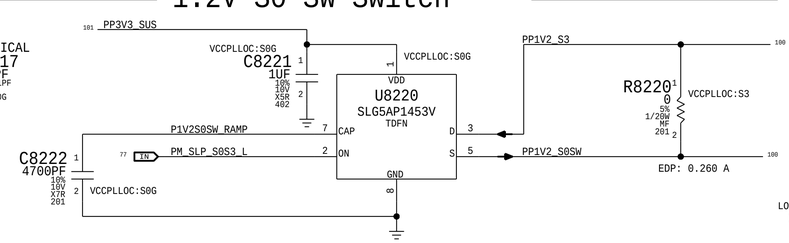
U8209

Part	SLG5AP1443V
Type	Load Switch
R(on)	17 mOhm Typ 19 mOhm Max
Current	2.5A

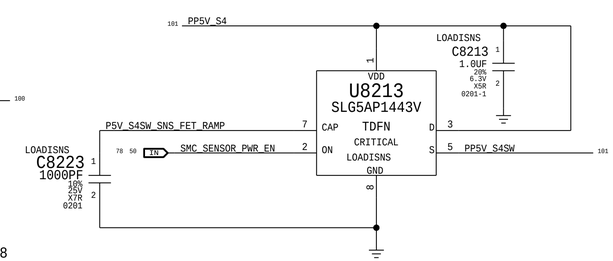
U8220

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

1.2V S0 SW Switch



5V Sensor Switch

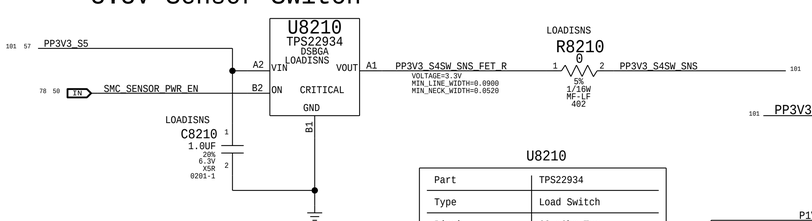


U8213

Part	SLG5AP1443V
Type	Load Switch
R(on)	17 mOhm Typ 19 mOhm Max
Current	2.5A

BOM_COST_GROUP=PLATFORM POWER

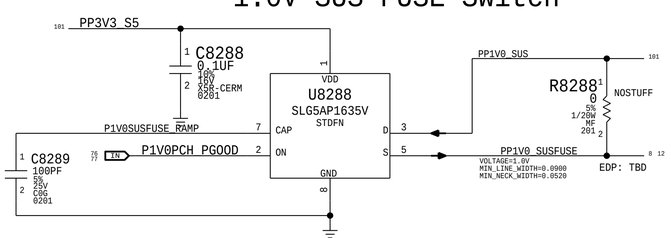
3.3V Sensor Switch



U8210

Part	TPS22934
Type	Load Switch
R(on) @ 3.6V	63 mOhm Typ 77 mOhm Max
Current	1A Max

1.0V SUS FUSE Switch



U8288

Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 mOhm Typ 28 mOhm Max
Current	2.5A Max
Ton Total	39us max @ 1V
R(discharge)	300 Ohm Max

PAGE TITLE

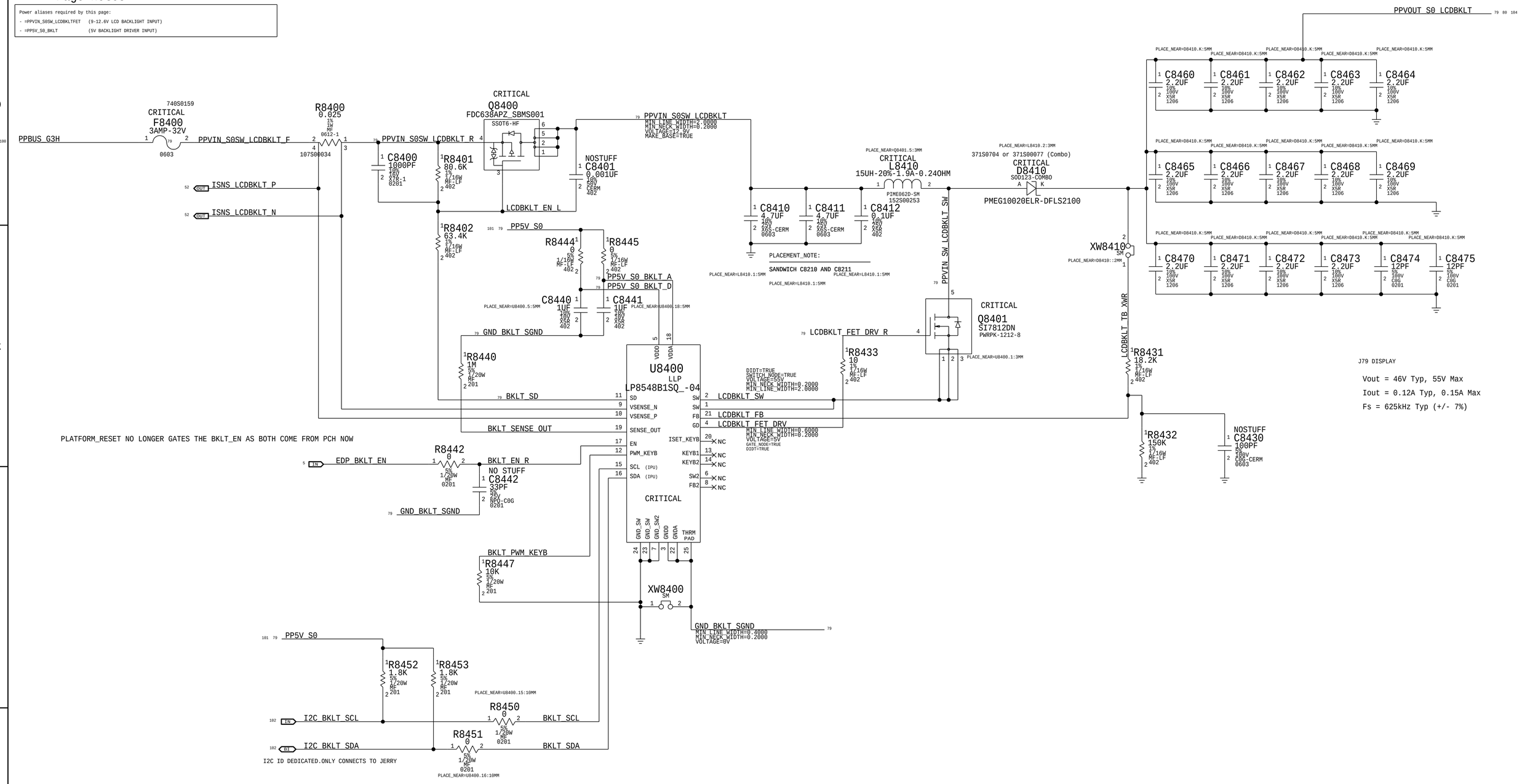
Power FETs

Apple Inc.

DRAWING NUMBER	051-00515
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	82 OF 145
SHEET	78 OF 119

Page Notes

Power aliases required by this page:
- =PPVIN_S0SW_LCDBKLTFET (9-12.6V LCD BACKLIGHT INPUT)
- =PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)



LINE WIDTHS

- PP5V_S0_BKLT_A — MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=5V
- PP5V_S0_BKLT_D — MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=5V
- BKLT_SD — MIN_LINE_WIDTH=0.4500, MIN_NECK_WIDTH=0.2000

PBUS LINE WIDTHS

- PPVIN_S0SW_LCDBKLT_F — MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=12.9V
- PPVIN_S0SW_LCDBKLT_R — MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=12.9V
- PPVIN_S0SW_LCDBKLT — MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=12.9V

LCD BKLT LINE WIDTHS

- LCDBKLT_FET_DRV_R — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.2000, VOLTAGE=5V, GATE_NODE=TRUE, DIDT=TRUE
- PPVIN_SW_LCDBKLT_SW — MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=55V, SWITCH_NODE=TRUE, DIDT=TRUE
- PPVOUT_S0_LCDBKLT — MIN_LINE_WIDTH=0.5000, MIN_NECK_WIDTH=0.1500, VOLTAGE=55V

BOM_COST_GROUP=DISPLAY

PAGE TITLE: LCD Backlight Driver

Apple Inc.

DRAWING NUMBER	051-00515
SIZE	D
REVISION	9.0.0
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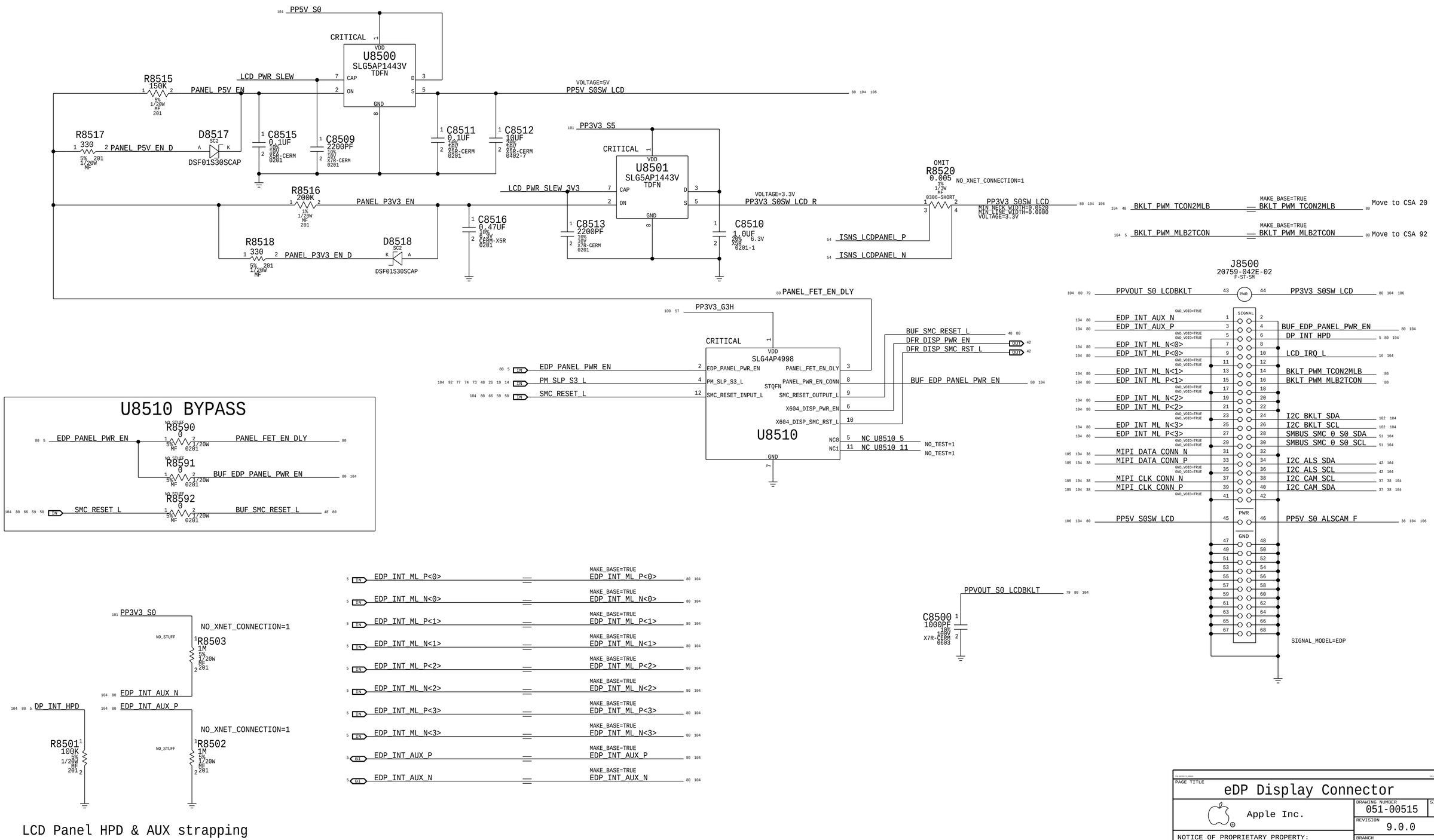
LCD PANEL INTERFACE (eDP) + Camera (MIPI)



LCD Panel HPD & AUX strapping

BOM_COST_GROUP=DISPLAY

PAGE TITLE
eDP Display Connector

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D
REVISION 9.0.0
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NAND LANDINGS

CONFIG	LANDING1 R8601	LANDING0 R8600
00 - 2	NOSTUFF	NOSTUFF
01 - 4	NOSTUFF	ASSEMBLE
10 - 8	ASSEMBLE	NOSTUFF
11 - RESERVED	ASSEMBLE	ASSEMBLE

OPERATION MODE (ODT, CLK FREQ, ETC)

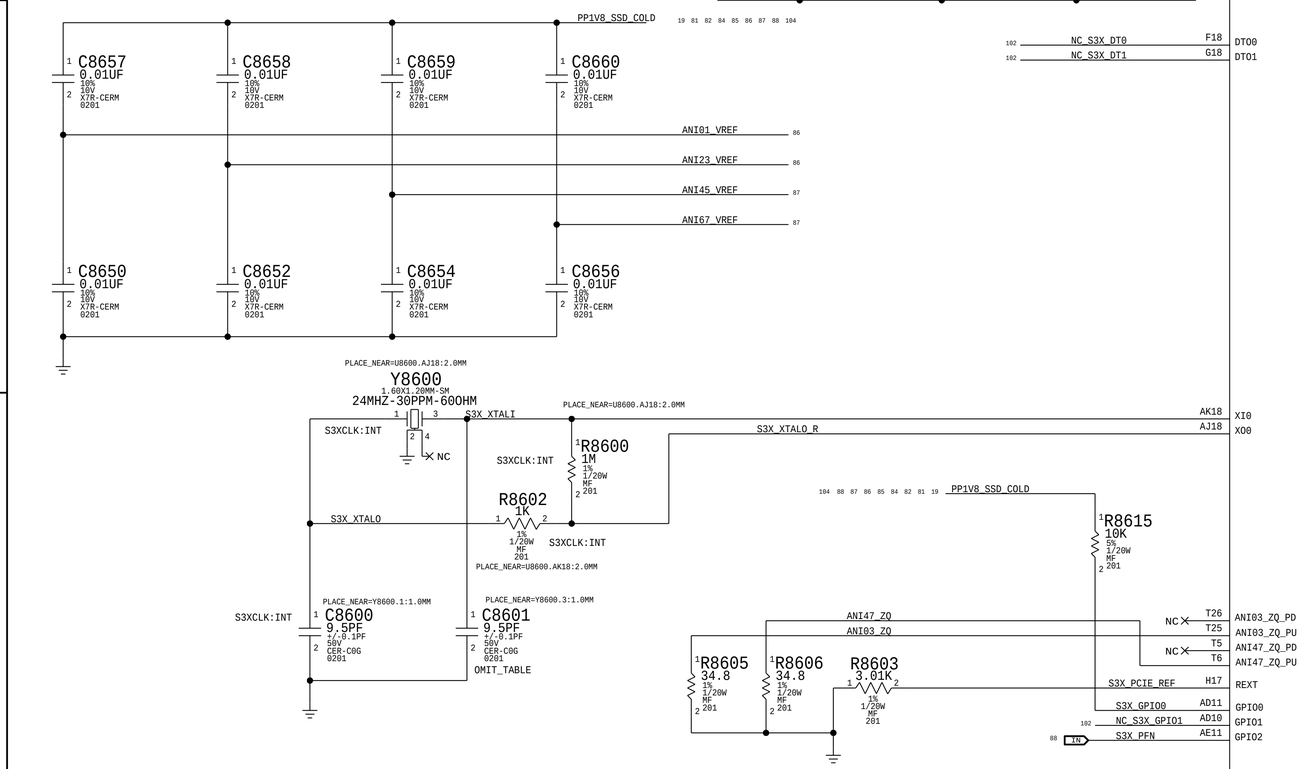
CONFIG	OP_MODE2 R8614	OP_MODE1 R8615	OP_MODE0 R8680
000 - TEABERRY	NOSTUFF	NOSTUFF	NOSTUFF
001 - XB58 GS	NOSTUFF	NOSTUFF	ASSEMBLE
010 - RESERVED	NOSTUFF	ASSEMBLE	NOSTUFF
011 - RESERVED	NOSTUFF	ASSEMBLE	ASSEMBLE
100 - RESERVED	ASSEMBLE	NOSTUFF	NOSTUFF
101 - RESERVED	ASSEMBLE	NOSTUFF	ASSEMBLE
110 - RESERVED	ASSEMBLE	ASSEMBLE	NOSTUFF
111 - RESERVED	ASSEMBLE	ASSEMBLE	ASSEMBLE

NAND CONFIGURATION

CONFIG	ROMBOOT2 R8617	ROMBOOT1 R8618	ROMBOOT0 R8616
000 - MLC SD/TOS 1Y/1Z(W/ HARD RESET)	NOSTUFF	NOSTUFF	NOSTUFF
001 - MLC SD/TOS 1Y/1Z (W/O HARD RESET)	NOSTUFF	NOSTUFF	ASSEMBLE
010 - RESERVED	NOSTUFF	ASSEMBLE	NOSTUFF
011 - MLC HYNIX 3D-V2	NOSTUFF	ASSEMBLE	ASSEMBLE
100 - RESERVED	ASSEMBLE	NOSTUFF	NOSTUFF
101 - RESERVED	ASSEMBLE	NOSTUFF	ASSEMBLE
110 - RESERVED	ASSEMBLE	ASSEMBLE	NOSTUFF
111 - RESERVED	ASSEMBLE	ASSEMBLE	ASSEMBLE

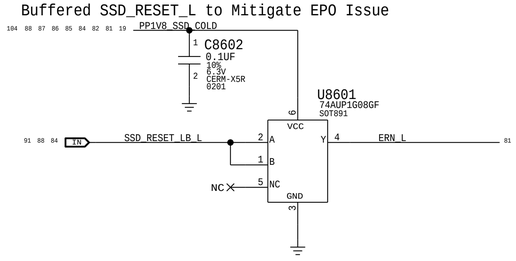
PRODUCT CAPACITY

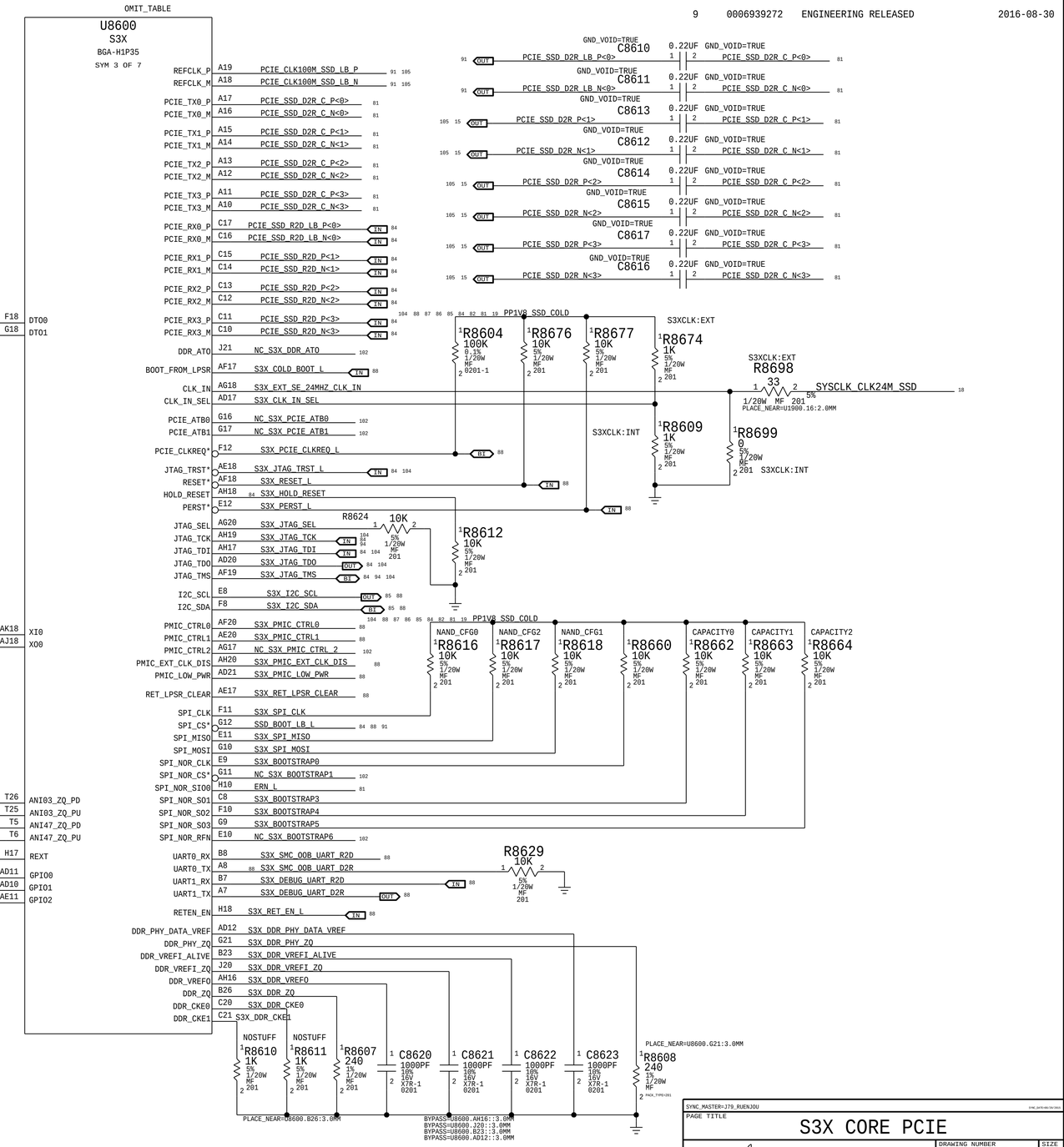
CONFIG	CAPACITY2 R8664	CAPACITY1 R8663	CAPACITY0 R8662
000 - 32GB	NOSTUFF	NOSTUFF	NOSTUFF
001 - 64GB	NOSTUFF	NOSTUFF	ASSEMBLE
010 - 128GB	NOSTUFF	ASSEMBLE	NOSTUFF
011 - 256GB	NOSTUFF	ASSEMBLE	ASSEMBLE
100 - 512GB	ASSEMBLE	NOSTUFF	NOSTUFF
101 - 1024GB	ASSEMBLE	NOSTUFF	ASSEMBLE
110 - 2048GB	ASSEMBLE	ASSEMBLE	NOSTUFF
111 - RESERVED	ASSEMBLE	ASSEMBLE	ASSEMBLE



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
131S00077	1	CAP,9.5PF,50V,0201	C8601	CRITICAL	S3XCLK:INT
117S0002	1	RES,MF,0 OHM,1/20W,0201	C8601	CRITICAL	S3XCLK:EXT

Buffered SSD_RESET_L to Mitigate EPO Issue





BOM_COST_GROUP=SSD

SYNC_MASTER=J79_RUENJOU

PAGE TITLE

S3X CORE PCIE

Apple Inc.

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BRANCH dvt-fab09-0

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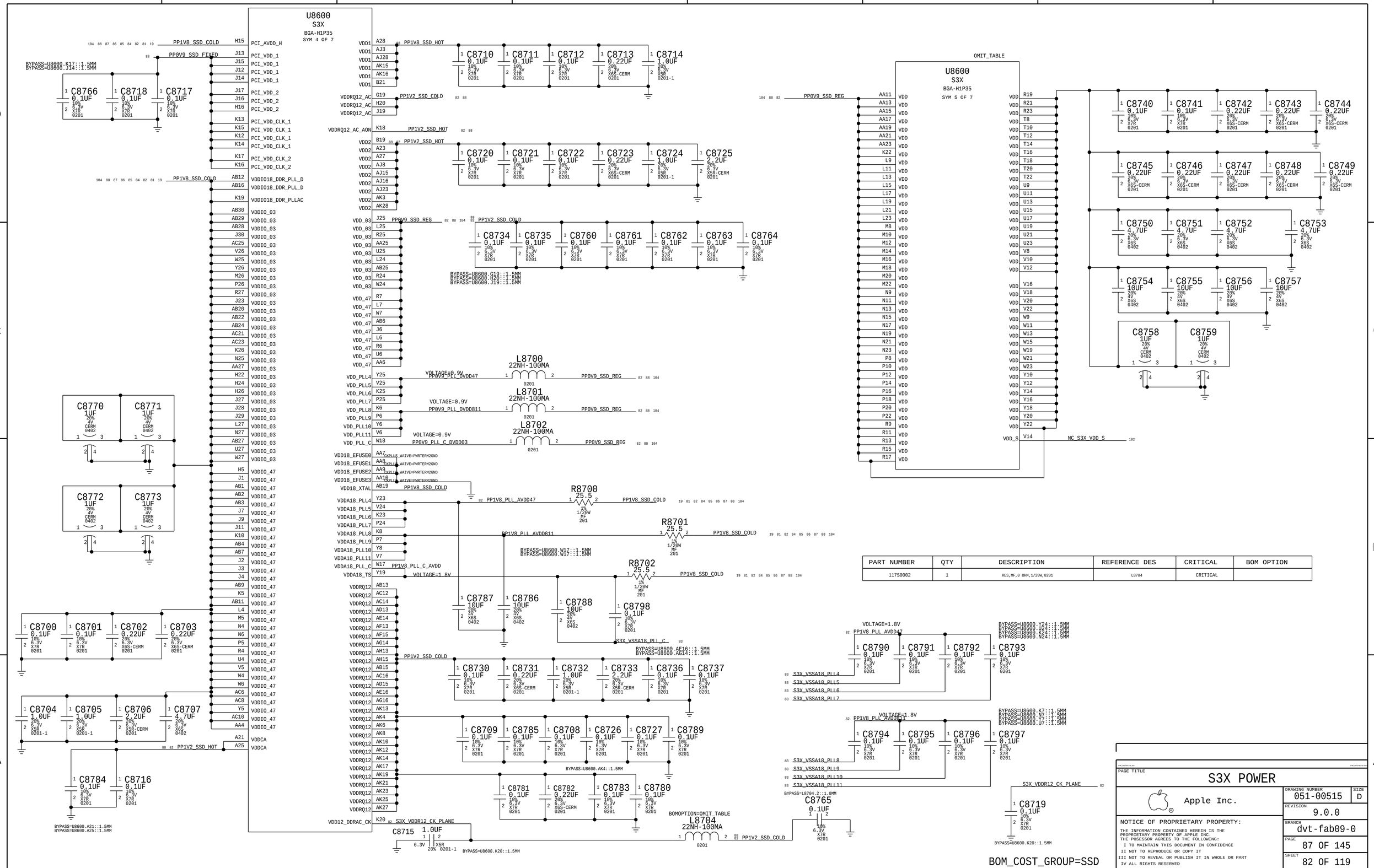

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	1	RES,MF,0 OHM,1/20W,0201	L8704	CRITICAL	

PAGE TITLE

S3X POWER

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D

REVISION 9.0.0

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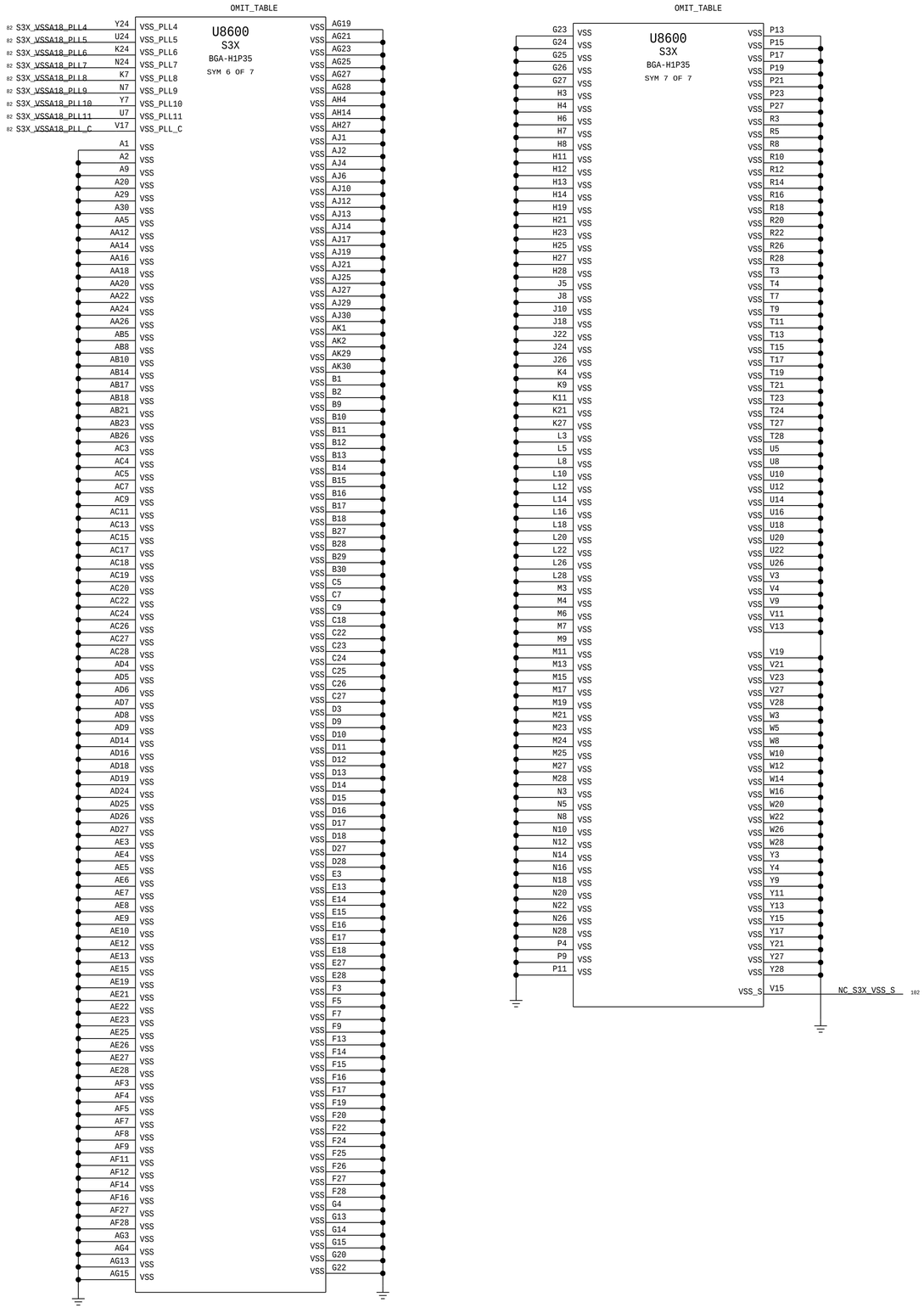

BOM_COST_GROUP=SSD

SYNC_MASTER=J79_RIO SYNC_DATE=06/18/2015

PAGE TITLE

PAGE_TITLE=S3X GND

Apple Inc.

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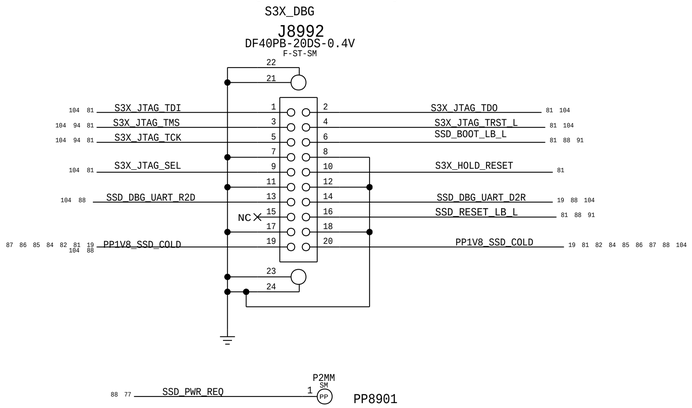
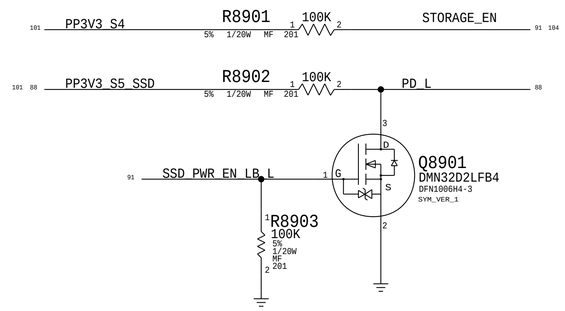
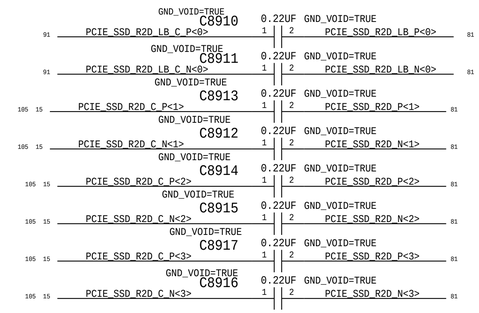
JTAG (DEBUG 1)







BOM_COST_GROUP=SSD

PAGE TITLE
Connector

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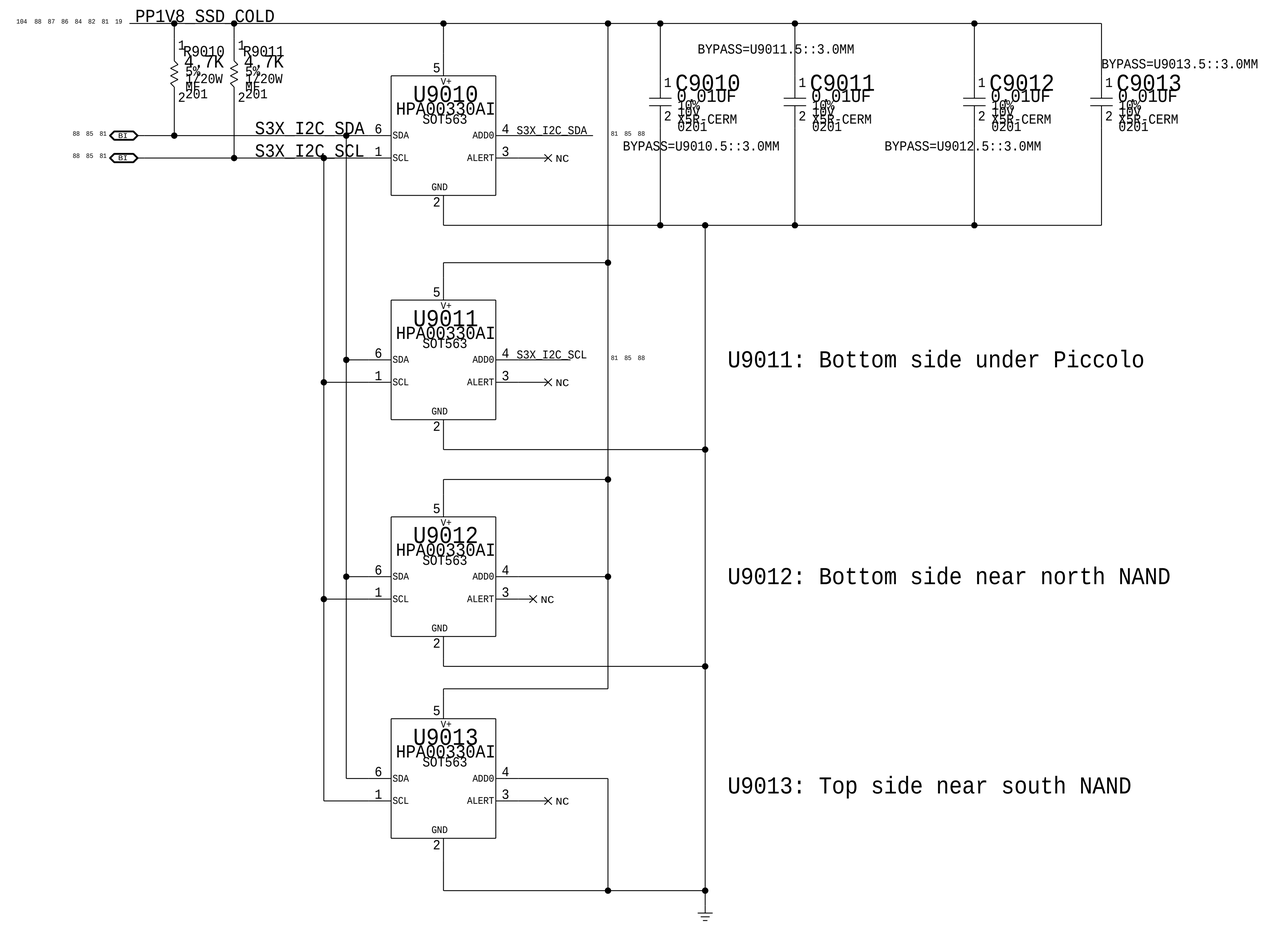
DEVICE 2-WIRE ADDRESS ADD0	PIN CONNECTION
1001000	GND
1001001	V+
1001010	SDA
1001011	SCL

U9010: Top side under S3X



U9011: Bottom side under Piccolo

U9012: Bottom side near north NAND

U9013: Top side near south NAND

BOM_COST_GROUP=SSD

SYNC_MASTER=J70_RUEN30U SYNC_DATE=09/12/2015

PAGE TITLE
NAND VR, I2C ROM, TEMP SENSORS

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D

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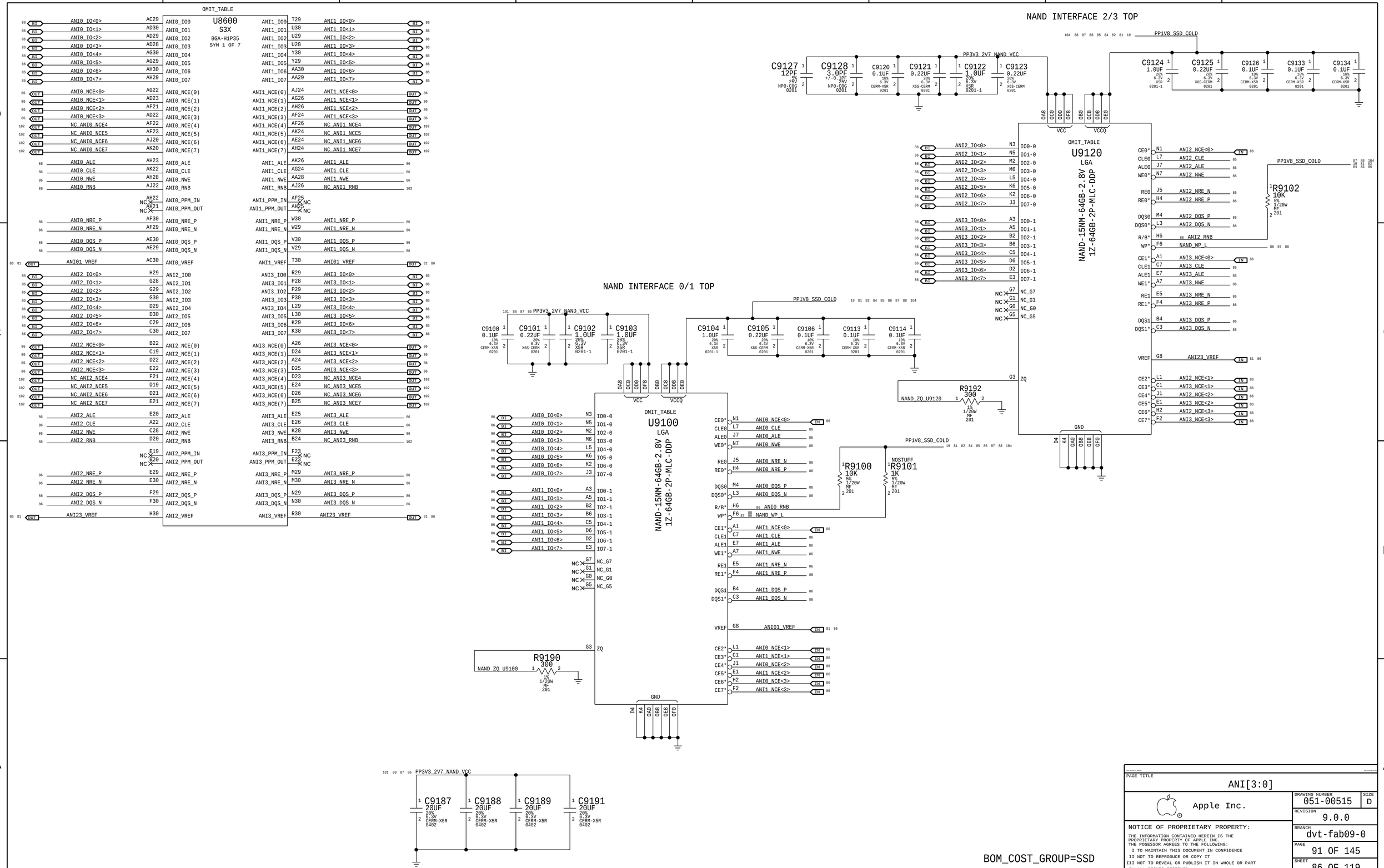

PAGE TITLE
ANI[3:0]

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D
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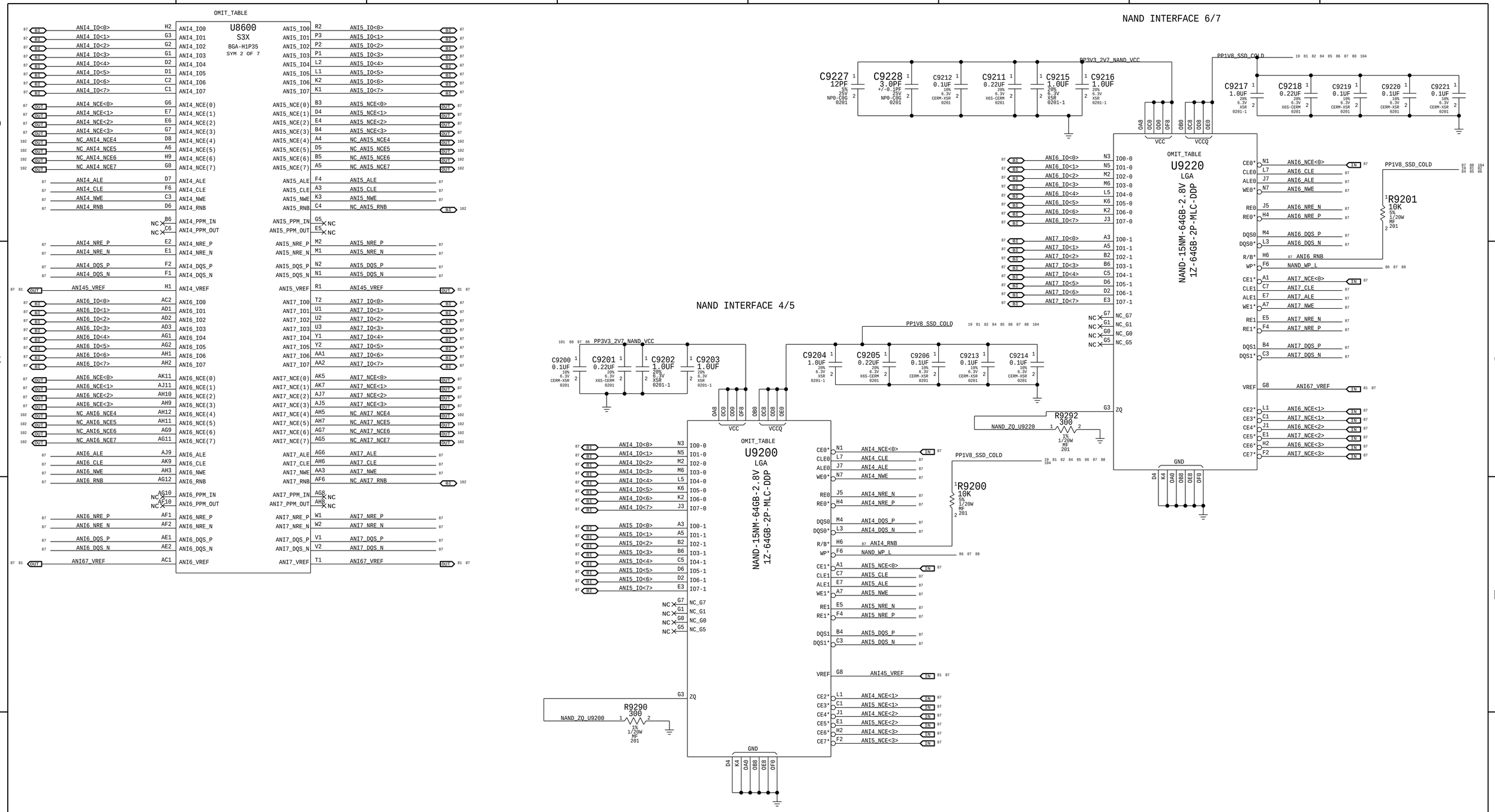
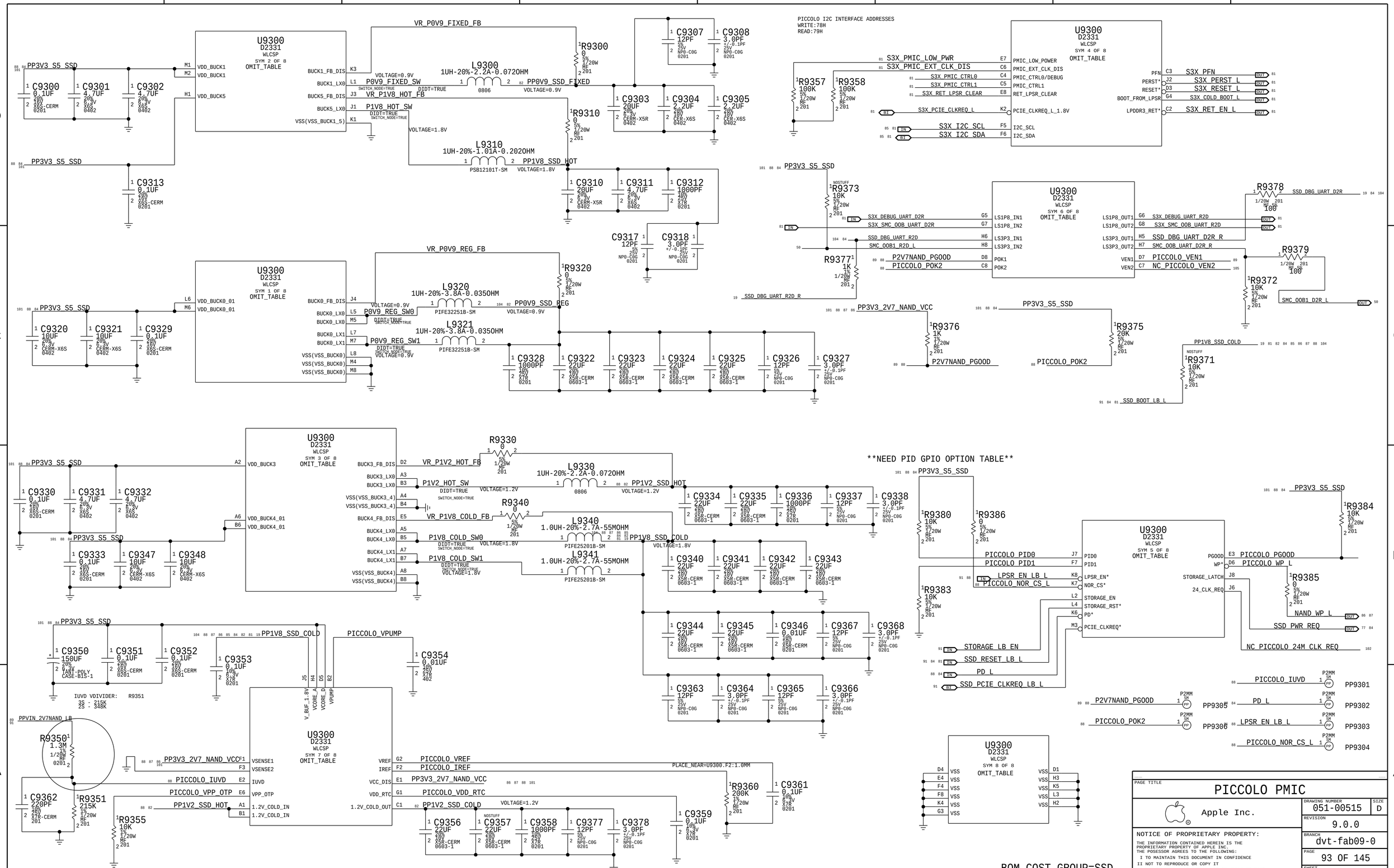


PAGE TITLE	ANI[7:4]
Apple Inc.	DRAWING NUMBER 051-00515
	SIZE D
	REVISION 9.0.0
	BRANCH dvt-fab09-0
	PAGE 92 OF 145
	SHEET 87 OF 119



PAGE TITLE: PICCOLO PMIC

Apple Inc.

DRAWING NUMBER: 051-00515 SIZE: D

REVISION: 9.0.0

BRANCH: dvt-fab09-0

PAGE: 93 OF 145

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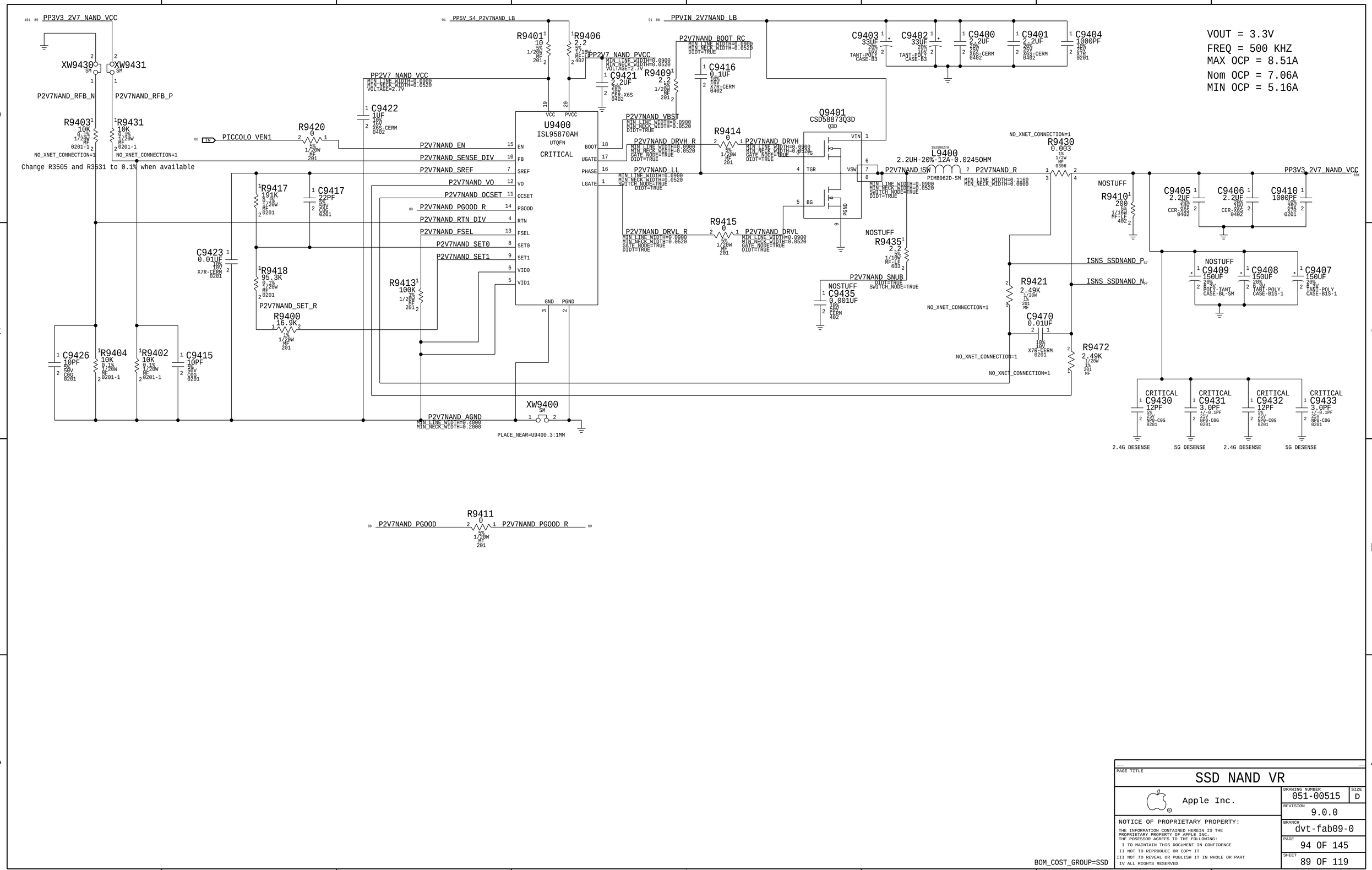

PAGE TITLE

SSD NAND VR

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D

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BRANCH dvt-fab09-0

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SYNC_MASTER=J14 SYNC_DATE=10/23/2012

PAGE TITLE

Empty

Apple Inc.

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REVISION 9.0.0

BRANCH dvt-fab09-0

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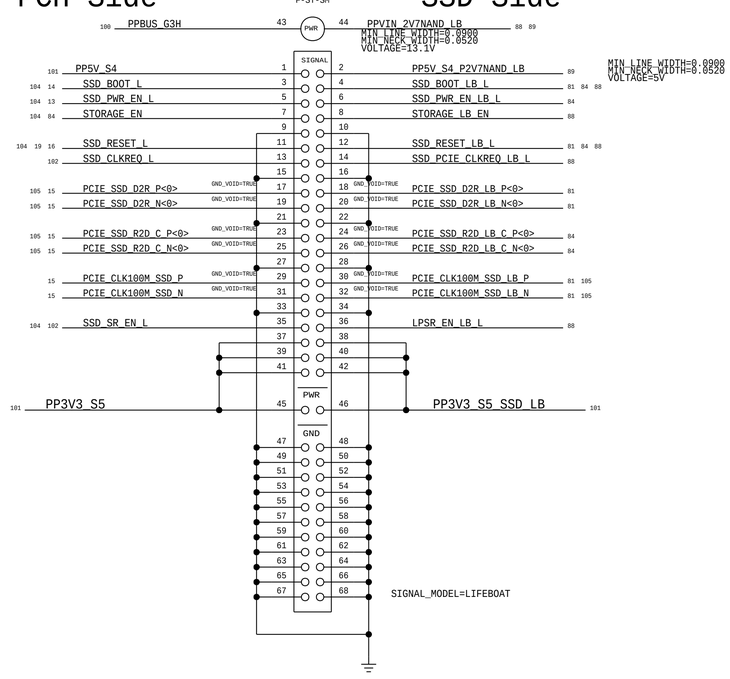
LIFEBOAT

J9600
20759-042E-02
F-ST-SM



BOM_COST_GROUP=SSD

SYNC_MASTER=J79_RUENJOU SYNC_DATE=09/09/2015

PAGE TITLE
LIFEBOAT

Apple Inc.

DRAWING NUMBER 051-00515
SIZE D
REVISION 9.0.0
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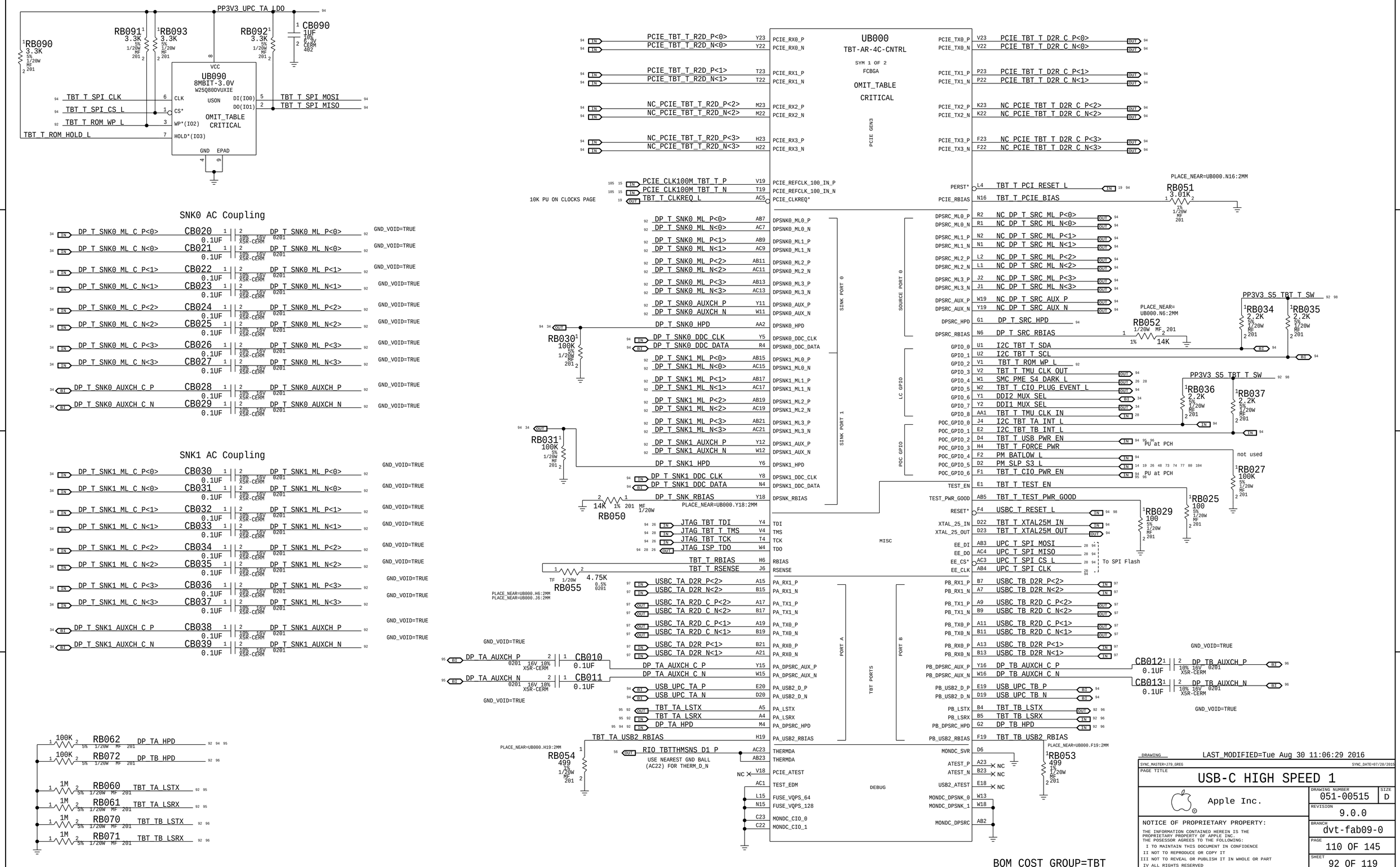
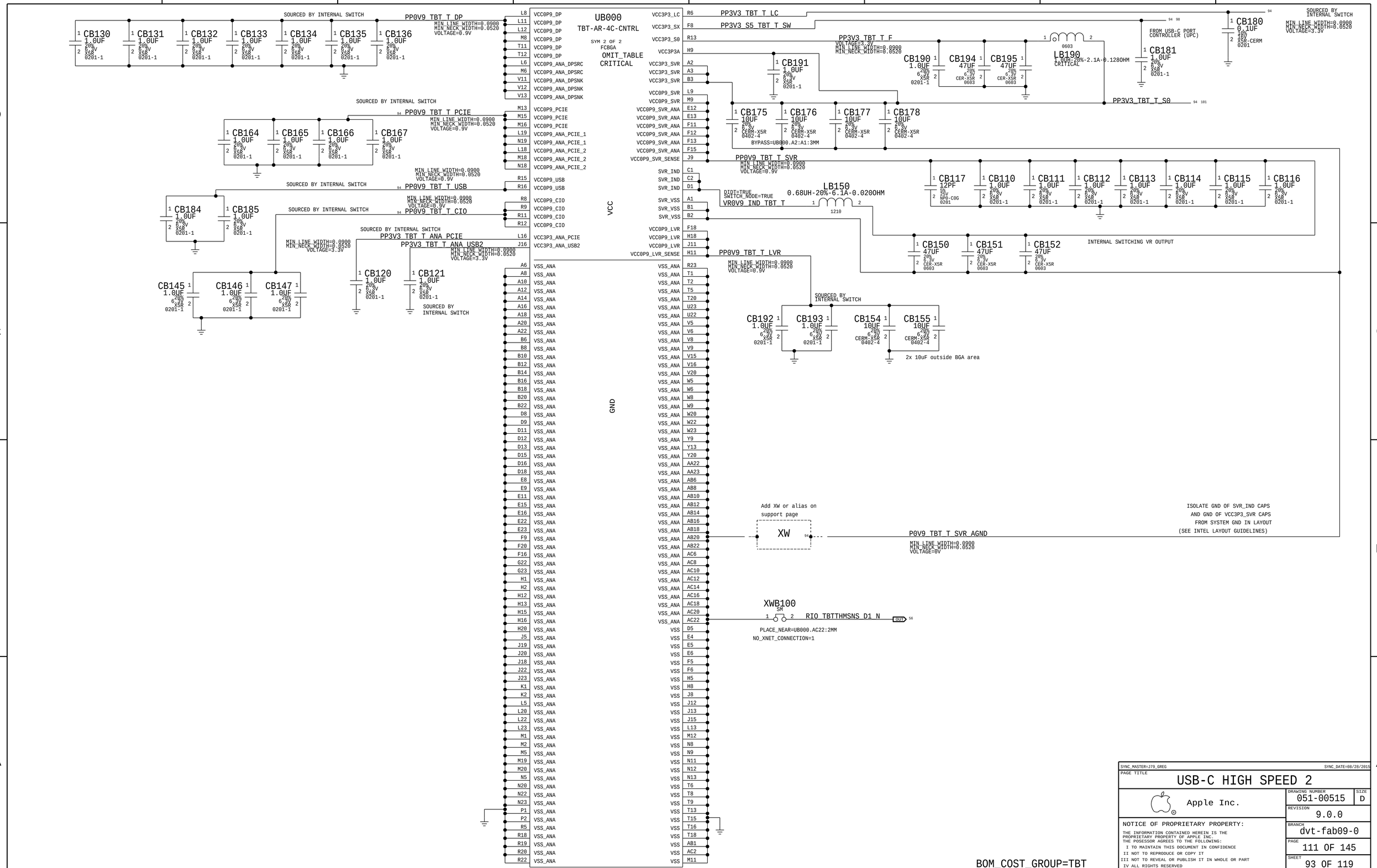




TMU CLKs

TBT_T_TMU_CLK_OUT (MAKE_BASE=TRUE) → TBT_T_TMU_CLK_OUT
RB225 15 5% 1/20W MF 201 (PLACE_NEAR=UB000.V2:5mm)
TBT_X_TMU_CLK_IN (MAKE_BASE=TRUE) → TBT_X_TMU_CLK_IN
RB224 100K 5% 1/20W MF 201

Ridge 0.9V SVR XW

P0V9_TBT_T_SVR_AGND
NO_XNET_CONNECTION=1
XWB200 SHORT-L6-SM

DP SRC OPTIONS

IF DP SRC NOT USED

DP_T_SRC_HPD
RB240 1M 5% 1/20W MF 201

NC_DP_T_SRC_ML_P<0>	NC_DP_T_SRC_ML_P<0>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_T_SRC_ML_P<1>	NC_DP_T_SRC_ML_P<1>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_T_SRC_ML_P<2>	NC_DP_T_SRC_ML_P<2>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_T_SRC_ML_P<3>	NC_DP_T_SRC_ML_P<3>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_T_SRC_ML_N<0>	NC_DP_T_SRC_ML_N<0>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_T_SRC_ML_N<1>	NC_DP_T_SRC_ML_N<1>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_T_SRC_ML_N<2>	NC_DP_T_SRC_ML_N<2>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_T_SRC_ML_N<3>	NC_DP_T_SRC_ML_N<3>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_T_SRC_AUX_P	NC_DP_T_SRC_AUX_P	MAKE_BASE=TRUE NO_TEST=1
NC_DP_T_SRC_AUX_N	NC_DP_T_SRC_AUX_N	MAKE_BASE=TRUE NO_TEST=1

AR xtal

TBT_T_XTAL25M_OUT → RB207 0 5% 1/20W MF 201 → TBT_T_XTAL25M_OUT_R
NOSTUFF RB206 1M 5% 1/20W MF 201
CRITICAL YB200 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM
CB202 20PF 5% 25V C0G 0201
CB203 20PF 5% 25V C0G 0201
TBT_T_XTAL25M_IN

T RIDGE DEBUG CONN

USBC_DBG JB201 505070-1220 M-ST-SM — Place on bottom

TBT_T_CIO_PLUG_EVENT_L	13–1	14–2	TBT_T_PCI_RESET_L
DP_T_SNK0_HPD	3	4	USBC_T_RESET_L
DP_T_SNK1_HPD	5	6	PP3V3_S5_TBT_T_SW
DP_TA_HPD	7	8	PP0V9_TBT_T_PCIE
TBT_POC_RESET	9	10	PP0V9_TBT_T_USB
PP3V3_TBT_T_LC	11	12	PP0V9_TBT_T_CIO
	15	16	

RIDGE JTAG ISOLATION

PLACE_NEAR=U0500.J1:10mm
JTAG_TBT_TCK → RB243 15 5% 1/20W MF 201 → XDP_JTAG_ISP_TCK
JTAG_TBT_TDI → RB244 15 5% 1/20W MF 201 → XDP_JTAG_ISP_TDI
TBT_DBG
RB246 100K 5% 1/20W MF 201
RB245 100K 5% 1/20W MF 201
TBT_DBG
PLACE_NEAR=U0500.J2:10mm

Ridge PWR ENs

PP3V3_S0
TBT_T_CIO_PWR_EN → RB271 100K 5% 1/20W MF 201
TBT_T_USB_PWR_EN → RB272 100K 5% 1/20W MF 201

Ridge PDs

DP_T_SNK0_DDC_CLK (MAKE_BASE=TRUE)	RB267	100K
DP_T_SNK0_DDC_DATA (MAKE_BASE=TRUE)	RB268	100K
DP_T_SNK1_DDC_CLK (MAKE_BASE=TRUE)	RB269	100K
DP_T_SNK1_DDC_DATA (MAKE_BASE=TRUE)	RB270	100K

ACE A/B RPD STRAPPING

USBC_TA_CC1	USBC_TA_CC1	MAKE_BASE=TRUE
USBC_TA_CC2	USBC_TA_CC2	MAKE_BASE=TRUE
USBC_TB_CC1	USBC_TB_CC1	MAKE_BASE=TRUE
USBC_TB_CC2	USBC_TB_CC2	MAKE_BASE=TRUE

ACE FET DCIN Bypass Caps

PPDCIN_G3H
CB211 0.1UF 10% 35V CER-X5R 0201
CB212 0.1UF 10% 35V CER-X5R 0201
CB213 0.1UF 10% 35V CER-X5R 0201
CB214 0.1UF 10% 35V CER-X5R 0201

ACE PDs

UPC_TA_DBG3	RB260	100K
UPC_TA_DBG4	RB261	100K
UPC_TB_DBG3	RB262	100K
UPC_TB_DBG4	RB263	100K
UPC_TA_DBG1	RB264	100K
UPC_TA_DBG2	RB265	100K
UPC_T_5V_EN	RB232	100K

FUSES FOR UPC

PP20V_USBC_TA_VBUS → FB200 (0603, CRITICAL, PLACE_NEAR=QB300:5MM) 6AMP-32V-0.00950HM → PP20V_USBC_TA_VBUS_F
PP20V_USBC_TB_VBUS → FB201 (0603, CRITICAL, PLACE_NEAR=QB400:5MM) 6AMP-32V-0.00950HM → PP20V_USBC_TB_VBUS_F

T ACEs DEBUG CONN

USBC_DBG JB200 505070-1220 M-ST-SM — Place on bottom

I2C_TBT_TB_INT_L	13–1	14–2	I2C_TBT_TA_INT_L
I2C_UPC_T_SCL2	3	4	I2C_TBT_T_SDA
I2C_UPC_T_SDA2	5	6	I2C_TBT_T_SCL
SMC_USBC_INT_L	7	8	TBT_T_CIO_PWR_EN
TBT_T_SPI_CLK_DBG	9	10	TBT_T_USB_PWR_EN
UPC_TA_UART_TX	11	12	UPC_TA_UART_RX
	15	16	

T ACE-SMC I2C SERIES R'S

I2C_UPC_T_SDA2	RB241 (PLACE_NEAR=U5000:5mm) 33	SMBUS_SMC_4_G3H_SDA	SMBUS_SMC_4_G3H_SDA
I2C_UPC_T_SDA2 (MAKE_BASE=TRUE)			
I2C_UPC_T_SDA2			
I2C_UPC_T_SCL2	RB242 (PLACE_NEAR=U5000:5mm) 33	SMBUS_SMC_4_G3H_SCL	SMBUS_SMC_4_G3H_SCL
I2C_UPC_T_SCL2 (MAKE_BASE=TRUE)			
I2C_UPC_T_SCL2			

USB2 AR PDs

USB_UPC_TA_P	RB220	0
USB_UPC_TA_N	RB221	0
USB_UPC_TB_P	RB222	0
USB_UPC_TB_N	RB223	0

ACE Debug Support

UPC_TA_DBG_UART_TX	RB289 (OMIT, NOSTUFF)	UPC_TA_DBG_UART_RX
UPC_TB_DBG_UART_TX	RB288 (OMIT, NOSTUFF)	UPC_TB_DBG_UART_RX

GND ALIASES

GND

NC/NO TEST

NO_TEST=1
NC_UPC_TB_I2C_ADDR

SIGNAL ALIASES

TBT_T_CIO_PWR_EN	TBT_T_CIO_PWR_EN (MAKE_BASE=TRUE)
TBT_T_USB_PWR_EN	TBT_T_USB_PWR_EN (MAKE_BASE=TRUE)
PM_BATLOW_L	PM_BATLOW_L (MAKE_BASE=TRUE)
UPC_T_5V_EN	UPC_T_5V_EN (MAKE_BASE=TRUE)
UPC_T_5V_EN	
JTAG_ISP_TDO	JTAG_ISP_TDO (MAKE_BASE=TRUE)
TBT_POC_RESET	TBT_POC_RESET (MAKE_BASE=TRUE)
TBT_T_CIO_PLUG_EVENT_L	TBT_T_CIO_PLUG_EVENT_L (MAKE_BASE=TRUE)
XDP_USB_EXTC_OC_L	XDP_USB_EXTC_OC_L (MAKE_BASE=TRUE)
XDP_USB_EXTD_OC_L	XDP_USB_EXTD_OC_L (MAKE_BASE=TRUE)
JTAG_TBT_T_TMS	JTAG_TBT_T_TMS (MAKE_BASE=TRUE)
S3X_JTAG_TCK	S3X_JTAG_TCK (MAKE_BASE=TRUE)
S3X_JTAG_TMS	S3X_JTAG_TMS (MAKE_BASE=TRUE)
NC_USBC_TB_RESET_L	NC_USBC_TB_RESET_L (MAKE_BASE=TRUE)
USB_UPC_PCH_TA_N	USB_UPC_PCH_TA_N (MAKE_BASE=TRUE)
USB_UPC_PCH_TA_N	
USB_UPC_PCH_TA_P	USB_UPC_PCH_TA_P (MAKE_BASE=TRUE)
USB_UPC_PCH_TA_P	
USB_UPC_PCH_TB_N	USB_UPC_PCH_TB_N (MAKE_BASE=TRUE)
USB_UPC_PCH_TB_N	
USB_UPC_PCH_TB_P	USB_UPC_PCH_TB_P (MAKE_BASE=TRUE)
USB_UPC_PCH_TB_P	

POWER ALIASES

PP3V3_UPC_TA_LDO	PP3V3_UPC_TA_LDO (MAKE_BASE=TRUE)
PP3V3_UPC_TA_LDO	
PP3V3_UPC_TA_LDO	
PP3V3_UPC_TB_LDO	PP3V3_UPC_TB_LDO (MAKE_BASE=TRUE)
PP3V3_UPC_TB_LDO	
PP20V_USBC_TA_VBUS	PP20V_USBC_TA_VBUS (MAKE_BASE=TRUE)
PP20V_USBC_TB_VBUS	PP20V_USBC_TB_VBUS (MAKE_BASE=TRUE)
PP5V_S4_T_USBC	PP5V_S4_T_USBC (MAKE_BASE=TRUE; MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 VOLTAGE=5V)
PP5V_S4_T_USBC	
PP5V_S4_T_USBC	
PP3V3_TBT_T_S0	PP3V3_TBT_T_S0 (MAKE_BASE=TRUE; MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 VOLTAGE=3.3V)

AR/ACE SPI BUS SERIES R'S

	RB290 100	TBT_T_SPI_CLK_DBG	
TBT_T_SPI_CLK	RB280 15	UPC_TA_SPI_CLK	Ace
TBT_T_SPI_CS_L	RB281 15	UPC_TA_SPI_CS_L	Ace
TBT_T_SPI_MOSI	RB282 15	UPC_TA_SPI_MOSI	Ace
TBT_T_SPI_MISO	RB283 15	UPC_TA_SPI_MISO	Ace
ROM	RB284 15	UPC_T_SPI_CLK	AR
	RB285 15	UPC_T_SPI_CS_L	AR
	RB286 15	UPC_T_SPI_MOSI	AR
	RB287 15	UPC_T_SPI_MISO	AR

TBT to ACE

TBT — Alpine Ridge U2800 (MASTER)

I2C_TBT_T_SCL (MAKE_BASE=TRUE)	I2C_TBT_T_SCL
I2C_TBT_T_SDA (MAKE_BASE=TRUE)	I2C_TBT_T_SDA
I2C_TBT_TA_INT_L (MAKE_BASE=TRUE)	I2C_TBT_TA_INT_L
I2C_TBT_TB_INT_L (MAKE_BASE=TRUE)	I2C_TBT_TB_INT_L

Pri ACE — U3100 (Write: 0x70 Read: 0x71)

I2C_TBT_T_SCL	I2C_TBT_T_SCL
I2C_TBT_T_SDA	I2C_TBT_T_SDA
I2C_TBT_TA_INT_L	I2C_TBT_TA_INT_L

Sec ACE — U3200 (Write: 0x7E Read: 0x7F)

I2C_TBT_T_SCL	I2C_TBT_T_SCL
I2C_TBT_T_SDA	I2C_TBT_T_SDA
I2C_TBT_TB_INT_L	I2C_TBT_TB_INT_L

Ridge PCIE Caps D2R

PCIE_TBT_T_D2R_C_P<0>	CB250 0.22UF (GND_VOID=TRUE)	PCIE_TBT_T_D2R_P<0>	
PCIE_TBT_T_D2R_C_N<0>	CB251 0.22UF (GND_VOID=TRUE)	PCIE_TBT_T_D2R_N<0>	
PCIE_TBT_T_D2R_C_P<1>	CB252 0.22UF (GND_VOID=TRUE)	PCIE_TBT_T_D2R_P<1>	
PCIE_TBT_T_D2R_C_N<1>	CB253 0.22UF	PCIE_TBT_T_D2R_N<1>	
NC_PCIE_TBT_T_D2R_C_P<2> (MAKE_BASE=TRUE NO_TEST=1)		NC_PCIE_TBT_T_D2R_C_P<2>	
NC_PCIE_TBT_T_D2R_C_N<2> (MAKE_BASE=TRUE NO_TEST=1)		NC_PCIE_TBT_T_D2R_C_N<2>	
NC_PCIE_TBT_T_D2R_C_P<3> (MAKE_BASE=TRUE NO_TEST=1)		NC_PCIE_TBT_T_D2R_C_P<3>	
NC_PCIE_TBT_T_D2R_C_N<3> (MAKE_BASE=TRUE NO_TEST=1)		NC_PCIE_TBT_T_D2R_C_N<3>	

R2D

PCIE_TBT_T_R2D_C_P<0>	CB240 0.22UF (GND_VOID=TRUE)	PCIE_TBT_T_R2D_P<0>	
PCIE_TBT_T_R2D_C_N<0>	CB241 0.22UF (GND_VOID=TRUE)	PCIE_TBT_T_R2D_N<0>	
PCIE_TBT_T_R2D_C_P<1>	CB242 0.22UF (GND_VOID=TRUE)	PCIE_TBT_T_R2D_P<1>	
PCIE_TBT_T_R2D_C_N<1>	CB243 0.22UF	PCIE_TBT_T_R2D_N<1>	
NC_PCIE_TBT_T_R2D_P<2> (MAKE_BASE=TRUE NO_TEST=1)		NC_PCIE_TBT_T_R2D_P<2>	
NC_PCIE_TBT_T_R2D_N<2> (MAKE_BASE=TRUE NO_TEST=1)		NC_PCIE_TBT_T_R2D_N<2>	
NC_PCIE_TBT_T_R2D_P<3> (MAKE_BASE=TRUE NO_TEST=1)		NC_PCIE_TBT_T_R2D_P<3>	
NC_PCIE_TBT_T_R2D_N<3> (MAKE_BASE=TRUE NO_TEST=1)		NC_PCIE_TBT_T_R2D_N<3>	

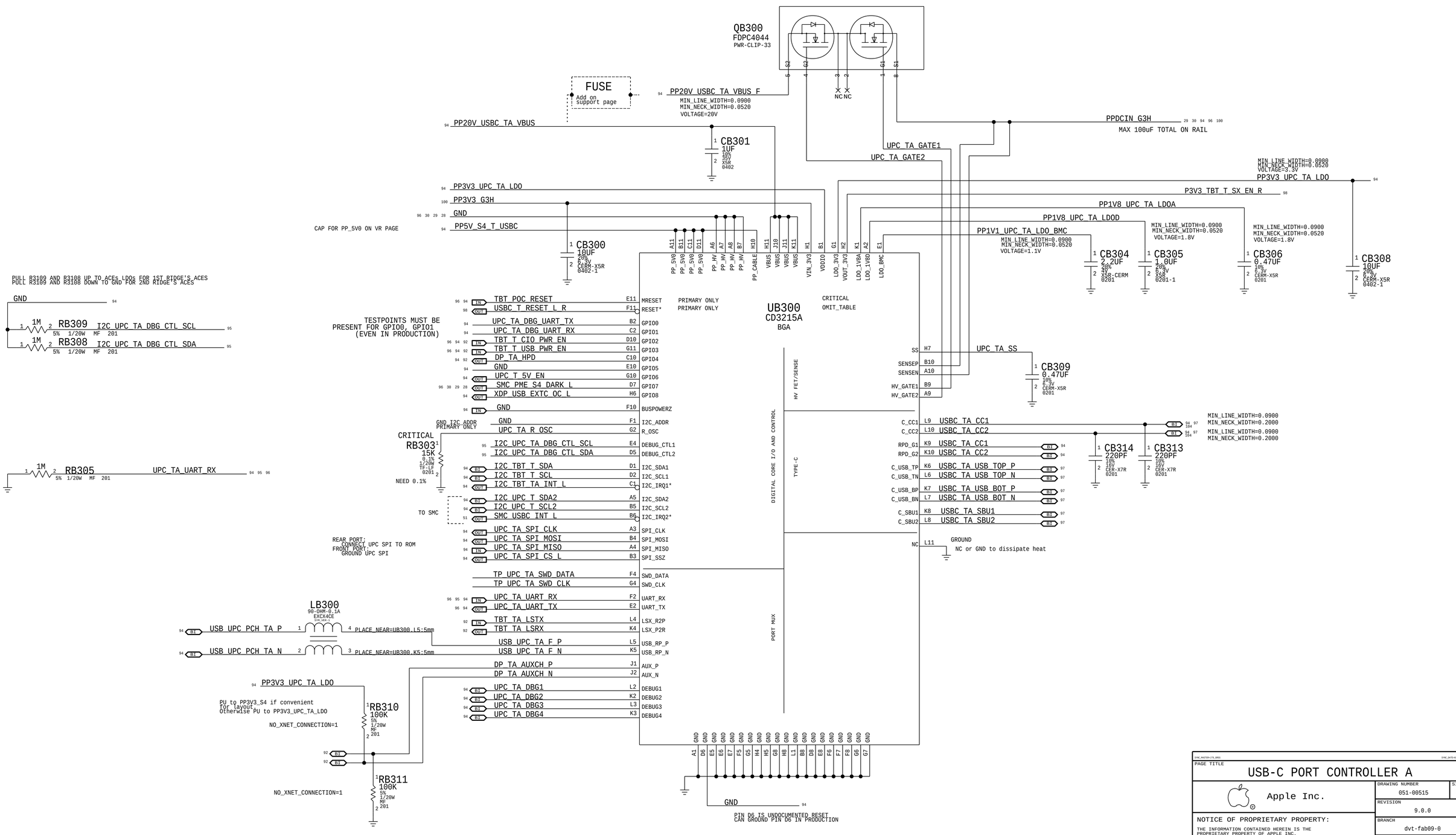
BOM_COST_GROUP=TBT

PAGE TITLE: USB-C Support

Apple Inc.

DRAWING NUMBER	051-00515
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	112 OF 145
SHEET	94 OF 119

PRIMARY ACE USB-C PORT CONTROLLER (UPC)



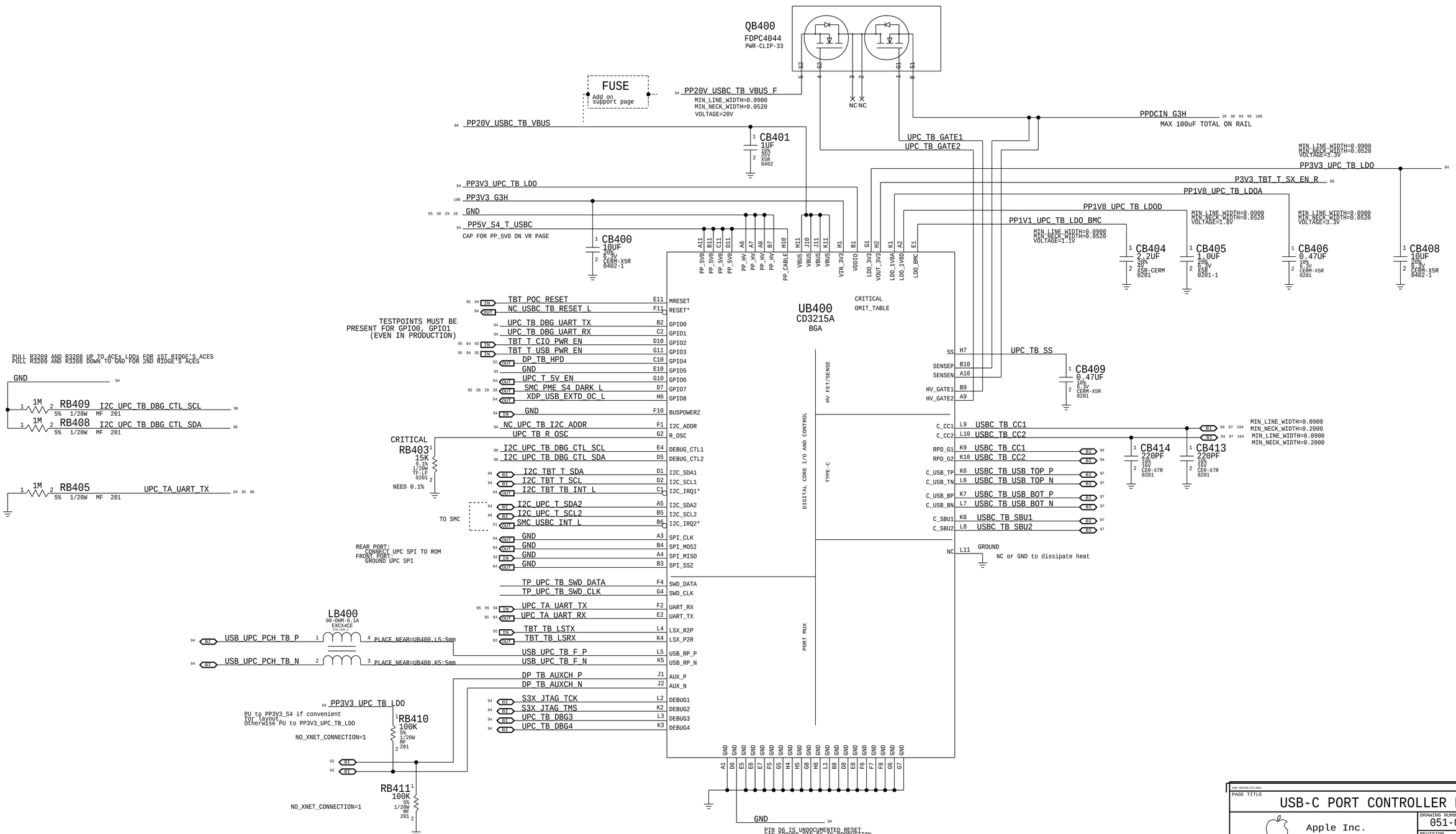
PAGE TITLE

USB-C PORT CONTROLLER A

Apple Inc.

DRAWING NUMBER	051-00515
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	113 OF 145
SHEET	95 OF 119

SECONDARY ACE USB-C PORT CONTROLLER (UPC)



BOM_COST_GROUP=USB-C

PAGE TITLE	USB-C PORT CONTROLLER B
Apple Inc.	DRAWING NUMBER 051-00515 SIZE D
	REVISION 9.0.0
	BRANCH dvt-fab09-0
	PAGE 114 OF 145
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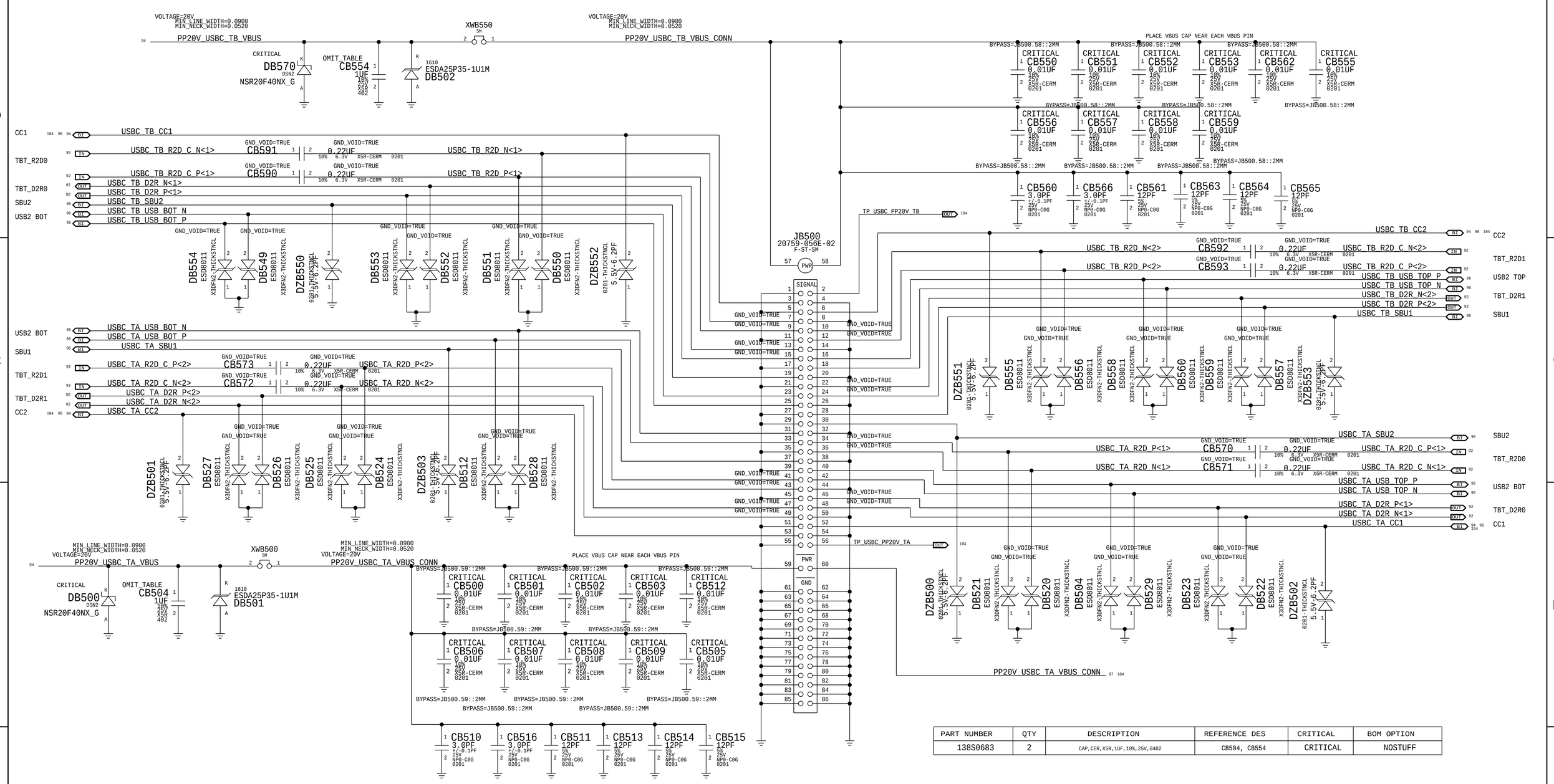

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0683	2	CAP,CER,X5R,1UF,10%,25V,0402	CB504, CB554	CRITICAL	NOSTUFF

BOM_COST_GROUP=USB-C

LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE
USB-C CONNECTOR A

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
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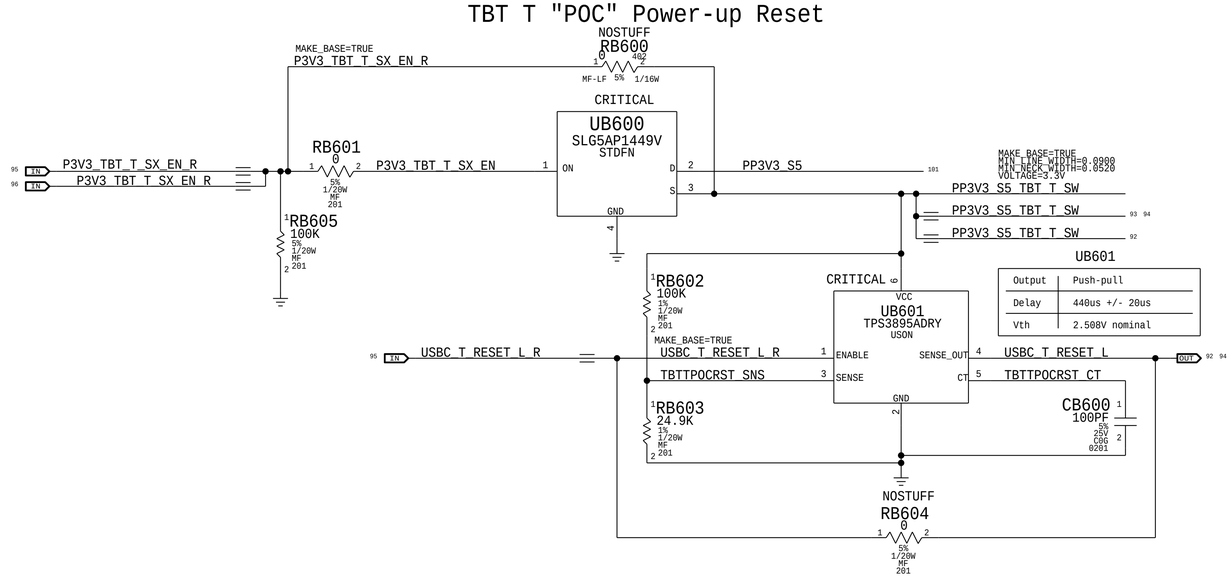
TBT T "POC" Power-up Reset



UB601

Output	Push-pull
Delay	440us +/- 20us
Vth	2.508V nominal

BOM_COST_GROUP=USB-C

DESIGN: j130/dev_mlb_u
LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE
USB-C CONNECTOR B

Apple Inc.

DRAWING NUMBER 051-00515
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 116 OF 145
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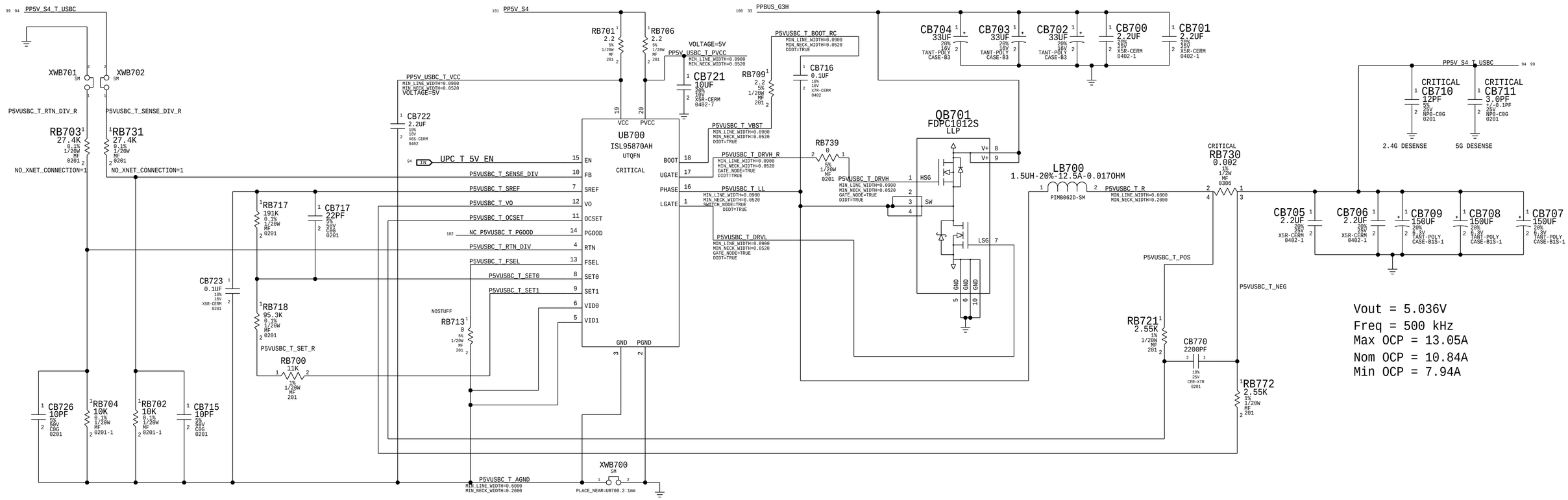

BOM_COST_GROUP=USB-C

PAGE TITLE

TBT 5V REGULATOR

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

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PBUS Rails

66 PPBUS_G3H
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=13.1V
- MAKE_BASE=TRUE

PPBUS_G3H: 52, 52, 52, 79, 52, 52, 74, 65, 76, 33 99, 76, 62 63, 91

52 PPBUS_HS_CPU
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=13.1V
- MAKE_BASE=TRUE

PPBUS_HS_CPU: 68, 68, 70, 75, 73, 75, 67

52 PPBUS_HS_OTH5V
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=13.1V
- MAKE_BASE=TRUE

PPBUS_HS_OTH5V: 72

52 PPBUS_HS_OTH3V3
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=13.1V
- MAKE_BASE=TRUE

PPBUS_HS_OTH3V3: 72

52 PPBUS_S4_HS_TPAD
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=13.1V
- MAKE_BASE=TRUE

PPBUS_S4_HS_TPAD: 43

96 95 94 30 29 PPDCIN_G3H
52 PPDCIN_G3H
- MAKE_BASE=TRUE
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=20V

PPDCIN_G3H: 66 104

3V3 G3H Rails

104 65 PP3V3_G3H
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=3.3V
- MAKE_BASE=TRUE

PP3V3_G3H: 59, 57 80, 50 100, 66, 43 50 104, 51, 49, 18, 51, 29, 30, 106, 77, 95, 96, 50 100

57 49 48 PP3V3_G3H_SMC_ISNS
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=3.3V
- MAKE_BASE=TRUE

RTC Rails

74 PP3V0_G3H
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=3.0V
- MAKE_BASE=TRUE

PP3V0_G3H: 8 12 14 15, 74

IMVP Rails

68 PPVCC_S0_CPU
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=1.5V
- MAKE_BASE=TRUE

PPVCC_S0_CPU: 8 54 104, 10

68 PPVCCSA_S0_CPU
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=1.5V
- MAKE_BASE=TRUE

PPVCCSA_S0_CPU: 8 55, 10

70 PPVCCGT_S0_CPU
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=1.5V
- MAKE_BASE=TRUE

PPVCCGT_S0_CPU: 8 54, 11, 8, 11

CPU VCCIO Rails

75 PPVCCIO_S0_CPU
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=0.95V
- MAKE_BASE=TRUE

PPVCCIO_S0_CPU: 5 8, 10

CPU EDRAM Rails

73 PPVCCEDRAM_S0_CPU
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=1.05V
- MAKE_BASE=TRUE

PPVCCEDRAM_S0_CPU: 8, 8, 8, 10, 8, 8, 10

PCH Prime Core Rails

76 PPVCCPRIMCORE_SUS_PCH
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=1.0V
- MAKE_BASE=TRUE

PPVCCPRIMCORE_SUS_PCH: 8 12 55

1V2 Rails

78 75 PP1V2_S3
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=1.2V
- MAKE_BASE=TRUE

PP1V2_S3: 21 22 23 24, 75, 20, 21 22 23 24, 21 22 23 24, 53, 78

53 PP1V2_S3_CPUDDR
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=1.2V
- MAKE_BASE=TRUE

PP1V2_S3_CPUDDR: 8, 8, 10, 10

78 PP1V2_S0SW
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=1.2V
- MAKE_BASE=TRUE

PP1V2_S0SW: 8 10

0V6 Rails

75 PP0V6_S0_DDRVTT
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=0.6V
- MAKE_BASE=TRUE

PP0V6_S0_DDRVTT: 25, 25

20 PP0V6_S3_MEM_VREFDQ_A
- MAKE_BASE=TRUE
- VOLTAGE=0.6V

PP0V6_S3_MEM_VREFDQ_A: 21 22

100 20 PP0V6_S3_MEM_VREFCA_A
- MAKE_BASE=TRUE
- VOLTAGE=0.6V

PP0V6_S3_MEM_VREFCA_A: 21 22

20 PP0V6_S3_MEM_VREFDQ_B
- MAKE_BASE=TRUE
- VOLTAGE=0.6V

PP0V6_S3_MEM_VREFDQ_B: 23 24

100 20 PP0V6_S3_MEM_VREFCA_A
- MAKE_BASE=TRUE
- VOLTAGE=0.6V

PP0V6_S3_MEM_VREFCA_A: 23 24

1V8 Rails

76 PP1V8_SUS
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=1.8V
- MAKE_BASE=TRUE

PP1V8_SUS: 8 14 19, 8 12, 78, 78, 8, 8, 12

78 PP1V8_S4
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=1.8V
- MAKE_BASE=TRUE

PP1V8_S4: 38 42, 18 19 35

78 PP1V8_S3
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=1.8V
- MAKE_BASE=TRUE

PP1V8_S3: 55, 74

55 PP1V8_S3_MEM
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=1.8V
- MAKE_BASE=TRUE

PP1V8_S3_MEM: 21 22 23 24

78 PP1V8_S0
- MIN_LINE_WIDTH=0.0900
- MIN_NECK_WIDTH=0.0520
- VOLTAGE=3.3V
- MAKE_BASE=TRUE

PP1V8_S0: 106, 12, 60 62 63 104, 19 106, 37 38 42, 74, 18, 37 42, 37, 19

PAGE TITLE

Power Aliases - 1

Apple Inc.

DRAWING NUMBER: 051-00515 | SIZE: D

REVISION: 9.0.0

BRANCH: dvt-fab09-0

PAGE: 120 OF 145

SHEET: 100 OF 119

1V0 Rails

```
76 PP1V0_SUS ═══ PP1V0_SUS
                 MIN_LINE_WIDTH=0.0900
                 MIN_NECK_WIDTH=0.0520
                 VOLTAGE=1.0V
                 MAKE_BASE=TRUE
                 ├═ PP1V0_SUS   8 12
                 ├═ PP1V0_SUS   8 12
                 ├═ PP1V0_SUS   12 15
                 ├═ PP1V0_SUS   8
                 ├═ PP1V0_SUS   12
                 ├═ PP1V0_SUS   8
                 ├═ PP1V0_SUS   12
                 ├═ PP1V0_SUS   12
                 ├═ PP1V0_SUS   8
                 ├═ PP1V0_SUS   17
                 ├═ PP1V0_SUS   78
                 ├═ PP1V0_SUS   78
                 ├═ PP1V0_SUS   18 19
                 └═ PP1V0_SUS   78

78 PP1V0_SUSSW ═══ PP1V0_SUSSW
                   MIN_LINE_WIDTH=0.0900
                   MIN_NECK_WIDTH=0.0520
                   VOLTAGE=1V
                   MAKE_BASE=TRUE
                   ├═ PP1V0_SUSSW   8 12
                   ├═ PP1V0_SUSSW   12
                   ├═ PP1V0_SUSSW   8 12
                   └═ PP1V0_SUSSW   8 12

78 PP1V0_S3 ═══ PP1V0_S3
                MIN_LINE_WIDTH=0.0900
                MIN_NECK_WIDTH=0.0520
                VOLTAGE=1V
                MAKE_BASE=TRUE
                ├═ PP1V0_S3   6 8 10 14 19
                ├═ PP1V0_S3   67
                ├═ PP1V0_S3   8 10
                ├═ PP1V0_S3   78
                ├═ PP1V0_S3   49
                └═ PP1V0_S3   73

78 PP1V0_S0SW ═══ PP1V0_S0SW
                  MIN_LINE_WIDTH=0.0900
                  MIN_NECK_WIDTH=0.0520
                  VOLTAGE=1V
                  MAKE_BASE=TRUE
                  └═ PP1V0_S0SW   6 8 10 17
```

5V Rails

```
72 PP5V_S5 ═══ PP5V_S5
               MIN_LINE_WIDTH=0.0900
               MIN_NECK_WIDTH=0.0520
               VOLTAGE=5V
               MAKE_BASE=TRUE

104 72 PP5V_S4 ═══ PP5V_S4
                   MIN_LINE_WIDTH=0.0900
                   MIN_NECK_WIDTH=0.0520
                   VOLTAGE=5V
                   MAKE_BASE=TRUE
                   ├═ PP5V_S4   43
                   ├═ PP5V_S4   67
                   ├═ PP5V_S4   78
                   ├═ PP5V_S4   33
                   ├═ PP5V_S4   99
                   ├═ PP5V_S4   91
                   ├═ PP5V_S4   78
                   └═ PP5V_S4   77

78 PP5V_S4SW ═══ PP5V_S4SW
                 MIN_LINE_WIDTH=0.0900
                 MIN_NECK_WIDTH=0.0520
                 VOLTAGE=5V
                 MAKE_BASE=TRUE
                 └═ PP5V_S4SW   57

57 PP5V_S4SW_ISNS ═══ PP5V_S4SW_ISNS
                      MIN_LINE_WIDTH=0.0900
                      MIN_NECK_WIDTH=0.0520
                      VOLTAGE=5V
                      MAKE_BASE=TRUE
                      ├═ PP5V_S4SW_ISNS   51 55
                      └═ PP5V_S4SW_ISNS   53

78 PP5V_S0 ═══ PP5V_S0
               MIN_LINE_WIDTH=0.0900
               MIN_NECK_WIDTH=0.0520
               VOLTAGE=5V
               MAKE_BASE=TRUE
               38 106
               ├═ PP5V_S0   54 106
               ├═ PP5V_S0   67 68
               ├═ PP5V_S0   79
               ├═ PP5V_S0   43 58
               ├═ PP5V_S0   55
               ├═ PP5V_S0   80
               ├═ PP5V_S0   73
               └═ PP5V_S0   70

55 PP5V_S0_KBD ═══ PP5V_S0_KBD
                   MIN_LINE_WIDTH=0.0900
                   MIN_NECK_WIDTH=0.0520
                   VOLTAGE=5V
                   MAKE_BASE=TRUE
                   └═ PP5V_S0_KBD   43 104
```

3V3 Rails

```
72 PP3V3_S5 ═══ PP3V3_S5
                MIN_LINE_WIDTH=0.0900
                MIN_NECK_WIDTH=0.0520
                VOLTAGE=3.3V
                MAKE_BASE=TRUE
                ├═ PP3V3_S5   8 14
                ├═ PP3V3_S5   78
                ├═ PP3V3_S5   78
                ├═ PP3V3_S5   78
                ├═ PP3V3_S5   74
                ├═ PP3V3_S5   19
                ├═ PP3V3_S5   57 78
                ├═ PP3V3_S5   76
                ├═ PP3V3_S5   18
                ├═ PP3V3_S5   78
                ├═ PP3V3_S5   78
                ├═ PP3V3_S5   78
                ├═ PP3V3_S5   53
                ├═ PP3V3_S5   91
                ├═ PP3V3_S5   80
                ├═ PP3V3_S5   78
                ├═ PP3V3_S5   78
                ├═ PP3V3_S5   78
                ├═ PP3V3_S5   32
                └═ PP3V3_S5   98

78 PP3V3_SUS ═══ PP3V3_SUS
                 MIN_LINE_WIDTH=0.0900
                 MIN_NECK_WIDTH=0.0520
                 VOLTAGE=3.3V
                 MAKE_BASE=TRUE
                 ├═ PP3V3_SUS   59
                 ├═ PP3V3_SUS   5 8 12
                 ├═ PP3V3_SUS   8 13
                 ├═ PP3V3_SUS   8 12
                 ├═ PP3V3_SUS   8 13 14 15 16
                 ├═ PP3V3_SUS   8 12
                 ├═ PP3V3_SUS   8 12
                 ├═ PP3V3_SUS   8
                 ├═ PP3V3_SUS   8 12
                 ├═ PP3V3_SUS   8
                 ├═ PP3V3_SUS   78
                 ├═ PP3V3_SUS   74
                 ├═ PP3V3_SUS   17 77
                 ├═ PP3V3_SUS   78
                 ├═ PP3V3_SUS   74
                 └═ PP3V3_SUS   43

78 PP3V3_S4 ═══ PP3V3_S4
                MIN_LINE_WIDTH=0.0900
                MIN_NECK_WIDTH=0.0520
                VOLTAGE=3.3V
                MAKE_BASE=TRUE
                106
                ├═ PP3V3_S4   53 106
                ├═ PP3V3_S4   36 106
                ├═ PP3V3_S4   54
                ├═ PP3V3_S4   43 104
                ├═ PP3V3_S4   51
                ├═ PP3V3_S4   14
                ├═ PP3V3_S4   84
                ├═ PP3V3_S4   54
                ├═ PP3V3_S4   57
                └═ PP3V3_S4   49 50

54 PP3V3_TBT_X_S0 ═══ PP3V3_TBT_X_S0   27 28

54 PP3V3_TBT_T_S0 ═══ PP3V3_TBT_T_S0   93 94

106 53 PP3V3_S4_BT ═══ PP3V3_S4_BT   35
                       MIN_LINE_WIDTH=0.0900
                       MIN_NECK_WIDTH=0.0520
                       VOLTAGE=2.9V
                       MAKE_BASE=TRUE

54 PP3V3_S4_TPAD ═══ PP3V3_S4_TPAD
                     MIN_LINE_WIDTH=0.0900
                     MIN_NECK_WIDTH=0.0520
                     VOLTAGE=3.3V
                     MAKE_BASE=TRUE
                     ├═ PP3V3_S4_TPAD   43 104
                     └═ PP3V3_S4_TPAD   104

78 PP3V3_S4SW_SNS ═══ PP3V3_S4SW_SNS
                      MIN_LINE_WIDTH=0.0900
                      MIN_NECK_WIDTH=0.0520
                      VOLTAGE=3.3V
                      MAKE_BASE=TRUE
                      ├═ PP3V3_S4SW_SNS   52
                      └═ PP3V3_S4SW_SNS   52 53 54 55 57

91 PP3V3_S5_SSD_LB ═══ PP3V3_S5_SSD_LB
                       MIN_LINE_WIDTH=0.0900   MAKE_BASE=TRUE
                       MIN_NECK_WIDTH=0.0520   VOLTAGE=3.3V
                       └═ PP3V3_S5_SSD_LB   57

57 PP3V3_S5_SSD ═══ PP3V3_S5_SSD
                    MIN_LINE_WIDTH=0.0900   MAKE_BASE=TRUE
                    MIN_NECK_WIDTH=0.0520   VOLTAGE=3.3V
                    └═ PP3V3_S5_SSD   84 88

57 PP3V3_S4_MESA ═══ PP3V3_S4_MESA
                     MIN_LINE_WIDTH=0.0900   VOLTAGE=3.3V
                     MIN_NECK_WIDTH=0.0520   MAKE_BASE=TRUE
                     └═ PP3V3_S4_MESA   47

89 PP3V3_2V7_NAND_VCC ═══ PP3V3_2V7_NAND_VCC   86 87 88
                          MIN_LINE_WIDTH=0.0900   VOLTAGE=2.7V
                          MIN_NECK_WIDTH=0.0520   MAKE_BASE=TRUE

78 PP3V3_S0 ═══ PP3V3_S0
                MIN_LINE_WIDTH=0.0900
                MIN_NECK_WIDTH=0.0520
                VOLTAGE=3.3V
                MAKE_BASE=TRUE
                61
                ├═ PP3V3_S0   55
                ├═ PP3V3_S0   58
                ├═ PP3V3_S0   54 56 106
                ├═ PP3V3_S0   73 74
                ├═ PP3V3_S0   5 13 14 16 19 94
                ├═ PP3V3_S0   19
                ├═ PP3V3_S0   38 42
                ├═ PP3V3_S0   51
                ├═ PP3V3_S0   51
                ├═ PP3V3_S0   51
                ├═ PP3V3_S0   51
                ├═ PP3V3_S0   54
                ├═ PP3V3_S0   52 53
                ├═ PP3V3_S0   53
                ├═ PP3V3_S0   34 106
                ├═ PP3V3_S0   37
                ├═ PP3V3_S0   56
                ├═ PP3V3_S0   56
                ├═ PP3V3_S0   49
                ├═ PP3V3_S0   80
                ├═ PP3V3_S0   49
                ├═ PP3V3_S0   19
                ├═ PP3V3_S0   73
                ├═ PP3V3_S0   42
                ├═ PP3V3_S0   54
                ├═ PP3V3_S0   54
                ├═ PP3V3_S0   52
                ├═ PP3V3_S0   61 106
                └═ PP3V3_S0   43
```

T208 Rails

```
53 PP3V3_S5_T139 ═══ PP3V3_S5_T139
                     MIN_LINE_WIDTH=0.0900
                     MIN_NECK_WIDTH=0.0520
                     VOLTAGE=3.3V
                     MAKE_BASE=TRUE
                     └═ PP3V3_S5_T139   42

54 PP3V3_S4_SOC_PMU ═══ PP3V3_S4_SOC_PMU
                        MIN_LINE_WIDTH=0.0900
                        MIN_NECK_WIDTH=0.0520
                        VOLTAGE=3.3V
                        MAKE_BASE=TRUE
                        ├═ PP3V3_S4_SOC_PMU   38 42
                        └═ PP3V3_S4_SOC_PMU   40 41

54 PP5V_S0_T139 ═══ PP5V_S0_T139
                    MIN_LINE_WIDTH=0.0900
                    MIN_NECK_WIDTH=0.0520
                    VOLTAGE=5V
                    MAKE_BASE=TRUE
                    └═ PP5V_S0_T139   42 104
```

```
GND
MIN_LINE_WIDTH=0.0900   VOLTAGE=0V
MIN_NECK_WIDTH=0.0700
```

Digital Ground

```
GND
MIN_NECK_WIDTH=0.0700
MIN_LINE_WIDTH=0.0900
```

PAGE TITLE

Power Aliases - 2

Apple Inc.

DRAWING NUMBER	051-00515
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
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SHEET	101 OF 119

UNUSED TP ALIASES

83	NC_S3X_VSS_S	MAKE_BASE=TRUE NO_TEST=1	NC_S3X_VSS_S	
82	NC_S3X_VDD_S	MAKE_BASE=TRUE NO_TEST=1	NC_S3X_VDD_S	
81	NC_S3X_PMIC_CTRL_2	MAKE_BASE=TRUE NO_TEST=1	NC_S3X_PMIC_CTRL_2	
81	NC_S3X_PCIE_ATB1	MAKE_BASE=TRUE NO_TEST=1	NC_S3X_PCIE_ATB1	
81	NC_S3X_PCIE_ATB0	MAKE_BASE=TRUE NO_TEST=1	NC_S3X_PCIE_ATB0	
81	NC_S3X_DT1	MAKE_BASE=TRUE NO_TEST=1	NC_S3X_DT1	
81	NC_S3X_DT0	MAKE_BASE=TRUE NO_TEST=1	NC_S3X_DT0	
81	NC_S3X_DDR_ATO	MAKE_BASE=TRUE NO_TEST=1	NC_S3X_DDR_ATO	
74	NC_PMIC_PGG	MAKE_BASE=TRUE NO_TEST=1	NC_PMIC_PGG	
74	NC_PMIC_PGF	MAKE_BASE=TRUE NO_TEST=1	NC_PMIC_PGF	
74	NC_PMIC_PGE	MAKE_BASE=TRUE NO_TEST=1	NC_PMIC_PGE	
74	NC_PMIC_PGD	MAKE_BASE=TRUE NO_TEST=1	NC_PMIC_PGD	
74	NC_PMIC_PGC	MAKE_BASE=TRUE NO_TEST=1	NC_PMIC_PGC	
88	NC_PICCOLO_24M_CLK_REQ	MAKE_BASE=TRUE NO_TEST=1	NC_PICCOLO_24M_CLK_REQ	
14	NC_PCH_SLP_A_L	MAKE_BASE=TRUE NO_TEST=1	NC_PCH_SLP_A_L	
14	NC_PCH_PME_L	MAKE_BASE=TRUE NO_TEST=1	NC_PCH_PME_L	
14	NC_PCH_LANPHYPC	MAKE_BASE=TRUE NO_TEST=1	NC_PCH_LANPHYPC	
14	NC_PCH_GPP_F9	MAKE_BASE=TRUE NO_TEST=1	NC_PCH_GPP_F9	
14	NC_PCH_GPP_F8	MAKE_BASE=TRUE NO_TEST=1	NC_PCH_GPP_F8	
14	NC_PCH_GPP_F10	MAKE_BASE=TRUE NO_TEST=1	NC_PCH_GPP_F10	
16	NC_PCH_GPP_D4	MAKE_BASE=TRUE NO_TEST=1	NC_PCH_GPP_D4	
16	NC_PCH_GPP_D3	MAKE_BASE=TRUE NO_TEST=1	NC_PCH_GPP_D3	
16	NC_PCH_GPP_D1	MAKE_BASE=TRUE NO_TEST=1	NC_PCH_GPP_D1	
14	NC_PCH_GPP_D0	MAKE_BASE=TRUE NO_TEST=1	NC_PCH_GPP_D0	
14	NC_PCH_GPD7	MAKE_BASE=TRUE NO_TEST=1	NC_PCH_GPD7	
90	NC_P5VUSBC_T_PGOOD	MAKE_BASE=TRUE NO_TEST=1	NC_P5VUSBC_T_PGOOD	
34	NC_DPMUX_SAK_20	MAKE_BASE=TRUE NO_TEST=1	NC_DPMUX_SAK_20	
34	NC_DPMUX_SAK_19	MAKE_BASE=TRUE NO_TEST=1	NC_DPMUX_SAK_19	
34	NC_DPMUX_SAK_18	MAKE_BASE=TRUE NO_TEST=1	NC_DPMUX_SAK_18	
34	NC_DPMUX_SAK_17	MAKE_BASE=TRUE NO_TEST=1	NC_DPMUX_SAK_17	
34	NC_DPMUX_SAK_16	MAKE_BASE=TRUE NO_TEST=1	NC_DPMUX_SAK_16	
34	NC_DPMUX_SAK_15	MAKE_BASE=TRUE NO_TEST=1	NC_DPMUX_SAK_15	
34	NC_DPMUX_SAK_14	MAKE_BASE=TRUE NO_TEST=1	NC_DPMUX_SAK_14	

UNUSED TP ALIASES

6	NC_CPU_RSVD_BB69	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_RSVD_BB69	
6	NC_CPU_RSVD_BB68	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_RSVD_BB68	
6	NC_CPU_RSVD_BA70	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_RSVD_BA70	
6	NC_CPU_RSVD_BA68	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_RSVD_BA68	
6	NC_CPU_RSVD_AW71	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_RSVD_AW71	
6	NC_CPU_RSVD_AW70	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_RSVD_AW70	
6	NC_CPU_RSVD_AK13	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_RSVD_AK13	
6	NC_CPU_RSVD_AK12	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_RSVD_AK12	
9	NC_CPU_NCTFVSS_C1	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_NCTFVSS_C1	
9	NC_CPU_NCTFVSS_BB70	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_NCTFVSS_BB70	
9	NC_CPU_NCTFVSS_BA71	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_NCTFVSS_BA71	
9	NC_CPU_NCTFVSS_BA1	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_NCTFVSS_BA1	
9	NC_CPU_NCTFVSS_B71	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_NCTFVSS_B71	
9	NC_CPU_NCTFVSS_AV1	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_NCTFVSS_AV1	
9	NC_CPU_NCTFVSS_A70	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_NCTFVSS_A70	
9	NC_CPU_NCTFVSS_A5	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_NCTFVSS_A5	
6	NC_CPU_BB5	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_BB5	
6	NC_CPU_BB3	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_BB3	
6	NC_CPU_AY4	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_AY4	
6	NC_CPU_AU5	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_AU5	
6	NC_CPU_AT5	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_AT5	
73	NC_CPU_MSM_L	MAKE_BASE=TRUE NO_TEST=1	NC_CPU_MSM_L	
28	NC_USBC_XA_RESET_L	MAKE_BASE=TRUE NO_TEST=1	NC_USBC_XA_RESET_L	
94	NC_USBC_TB_RESET_L	MAKE_BASE=TRUE NO_TEST=1	NC_USBC_TB_RESET_L	

UNUSED SIGNALS

14	NC_PCH_SLP_WLAN_L	TRUE	NC_PCH_SLP_WLAN_L	105	
102 13	NC_SPI_CS1_L	TRUE	NC_SPI_CS1_L	102 105	
102 13	NC_SPI_CS2_L	TRUE	NC_SPI_CS2_L	102 105	
102 13	NC_SPI_CS1_L	TRUE	NC_SPI_CS1_L	102 105	
102 13	NC_SPI_CS2_L	TRUE	NC_SPI_CS2_L	102 105	
15	NC_PCIE_CAMERA_D2R_N		NC_PCIE_CAMERA_D2R_N	105	TRUE
15	NC_PCIE_CAMERA_D2R_P		NC_PCIE_CAMERA_D2R_P	105	TRUE
15	NC_PCIE_CAMERA_R2D_C_N		NC_PCIE_CAMERA_R2D_C_N	105	TRUE
15	NC_PCIE_CAMERA_R2D_C_P		NC_PCIE_CAMERA_R2D_C_P	105	TRUE
15	NC_PCIE_CLK100M_CAMERA_N		NC_PCIE_CLK100M_CAMERA_N	105	TRUE
15	NC_PCIE_CLK100M_CAMERA_P		NC_PCIE_CLK100M_CAMERA_P	105	TRUE
15	NC_USB_EXTA_N		NC_USB_EXTA_N		TRUE
15	NC_USB_EXTA_P	NO_TEST=1 NO_TEST=1	NC_USB_EXTA_P		TRUE
15	NC_USB_EXTB_N		NC_USB_EXTB_N		TRUE
15	NC_USB_EXTB_P	NO_TEST=1 NO_TEST=1	NC_USB_EXTB_P		TRUE
6	NC_XDP_BPM_L<1>		NC_XDP_BPM_L<1>		TRUE
6	NC_XDP_BPM_L<2>	NO_TEST=1	NC_XDP_BPM_L<2>		TRUE
6	NC_XDP_BPM_L<3>	NO_TEST=1 NO_TEST=1	NC_XDP_BPM_L<3>		TRUE
15	NC_USB3_EXTB_D2R_N		NC_USB3_EXTB_D2R_N		TRUE
15	NC_USB3_EXTB_D2R_P	NO_TEST=1	NC_USB3_EXTB_D2R_P		TRUE
15	NC_USB3_EXTB_R2D_C_N	NO_TEST=1	NC_USB3_EXTB_R2D_C_N		TRUE
15	NC_USB3_EXTB_R2D_C_P	NO_TEST=1 NO_TEST=1	NC_USB3_EXTB_R2D_C_P		TRUE

UNUSED SIGNAL ALIAS

86	NC_ANI0_NCE4	MAKE_BASE=TRUE NO_TEST=1	NC_ANI0_NCE4	
86	NC_ANI0_NCE5	MAKE_BASE=TRUE NO_TEST=1	NC_ANI0_NCE5	
86	NC_ANI0_NCE6	MAKE_BASE=TRUE NO_TEST=1	NC_ANI0_NCE6	
86	NC_ANI0_NCE7	MAKE_BASE=TRUE NO_TEST=1	NC_ANI0_NCE7	
86	NC_ANI1_NCE4	MAKE_BASE=TRUE NO_TEST=1	NC_ANI1_NCE4	
86	NC_ANI1_NCE5	MAKE_BASE=TRUE NO_TEST=1	NC_ANI1_NCE5	
86	NC_ANI1_NCE6	MAKE_BASE=TRUE NO_TEST=1	NC_ANI1_NCE6	
86	NC_ANI1_NCE7	MAKE_BASE=TRUE NO_TEST=1	NC_ANI1_NCE7	
86	NC_ANI2_NCE4	MAKE_BASE=TRUE NO_TEST=1	NC_ANI2_NCE4	
86	NC_ANI2_NCE5	MAKE_BASE=TRUE NO_TEST=1	NC_ANI2_NCE5	
86	NC_ANI2_NCE6	MAKE_BASE=TRUE NO_TEST=1	NC_ANI2_NCE6	
86	NC_ANI2_NCE7	MAKE_BASE=TRUE NO_TEST=1	NC_ANI2_NCE7	
86	NC_ANI3_NCE4	MAKE_BASE=TRUE NO_TEST=1	NC_ANI3_NCE4	
86	NC_ANI3_NCE5	MAKE_BASE=TRUE NO_TEST=1	NC_ANI3_NCE5	
86	NC_ANI3_NCE6	MAKE_BASE=TRUE NO_TEST=1	NC_ANI3_NCE6	
86	NC_ANI3_NCE7	MAKE_BASE=TRUE NO_TEST=1	NC_ANI3_NCE7	
87	NC_ANI4_NCE4	MAKE_BASE=TRUE NO_TEST=1	NC_ANI4_NCE4	
87	NC_ANI4_NCE5	MAKE_BASE=TRUE NO_TEST=1	NC_ANI4_NCE5	
87	NC_ANI4_NCE6	MAKE_BASE=TRUE NO_TEST=1	NC_ANI4_NCE6	
87	NC_ANI4_NCE7	MAKE_BASE=TRUE NO_TEST=1	NC_ANI4_NCE7	
87	NC_ANI5_NCE4	MAKE_BASE=TRUE NO_TEST=1	NC_ANI5_NCE4	
87	NC_ANI5_NCE5	MAKE_BASE=TRUE NO_TEST=1	NC_ANI5_NCE5	
87	NC_ANI5_NCE6	MAKE_BASE=TRUE NO_TEST=1	NC_ANI5_NCE6	
87	NC_ANI5_NCE7	MAKE_BASE=TRUE NO_TEST=1	NC_ANI5_NCE7	
87	NC_ANI6_NCE4	MAKE_BASE=TRUE NO_TEST=1	NC_ANI6_NCE4	
87	NC_ANI6_NCE5	MAKE_BASE=TRUE NO_TEST=1	NC_ANI6_NCE5	
87	NC_ANI6_NCE6	MAKE_BASE=TRUE NO_TEST=1	NC_ANI6_NCE6	
87	NC_ANI6_NCE7	MAKE_BASE=TRUE NO_TEST=1	NC_ANI6_NCE7	
87	NC_ANI7_NCE4	MAKE_BASE=TRUE NO_TEST=1	NC_ANI7_NCE4	
87	NC_ANI7_NCE5	MAKE_BASE=TRUE NO_TEST=1	NC_ANI7_NCE5	
87	NC_ANI7_NCE6	MAKE_BASE=TRUE NO_TEST=1	NC_ANI7_NCE6	
87	NC_ANI7_NCE7	MAKE_BASE=TRUE NO_TEST=1	NC_ANI7_NCE7	
86	NC_ANI1_RNB	MAKE_BASE=TRUE NO_TEST=1	NC_ANI1_RNB	
86	NC_ANI3_RNB	MAKE_BASE=TRUE NO_TEST=1	NC_ANI3_RNB	
87	NC_ANI5_RNB	MAKE_BASE=TRUE NO_TEST=1	NC_ANI5_RNB	
87	NC_ANI7_RNB	MAKE_BASE=TRUE NO_TEST=1	NC_ANI7_RNB	
81	NC_S3X_GPIO1	MAKE_BASE=TRUE NO_TEST=1	NC_S3X_GPIO1	
81	NC_S3X_BOOTSTRAP6	MAKE_BASE=TRUE NO_TEST=1	NC_S3X_BOOTSTRAP6	
81	NC_S3X_BOOTSTRAP1	MAKE_BASE=TRUE NO_TEST=1	NC_S3X_BOOTSTRAP1	

S3X Aliasing

10	SSD_CLKREQ_L	MAKE_BASE=TRUE	SSD_CLKREQ_L	91
14	SSD_SR_EN_L	MAKE_BASE=TRUE	SSD_SR_EN_L	91 104

EPD PANEL

79	I2C_BKLT_SCL	MAKE_BASE TRUE	I2C_BKLT_SCL	80 104
79	I2C_BKLT_SDA	TRUE	I2C_BKLT_SDA	80 104

SYNC_MASTER=SHART_J44 SYNC_DATE=11/19/2012

PAGE TITLE

Signal Aliases

Apple Inc.

DRAWING NUMBER 051-00515 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

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Memory Bit & Byte Swizzle

MAKE_BASE=TRUE

7	MEM_A_DQ<0>	MEM_A_DQ<0>	21
7	MEM_A_DQ<1>	MEM_A_DQ<1>	21
7	MEM_A_DQ<2>	MEM_A_DQ<2>	21
7	MEM_A_DQ<3>	MEM_A_DQ<3>	21
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7	MEM_A_DQ<62>	MEM_A_DQ<62>	22
7	MEM_A_DQ<63>	MEM_A_DQ<63>	22

MAKE_BASE=TRUE

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7	MEM_B_DQ<1>	MEM_B_DQ<1>	23
7	MEM_B_DQ<2>	MEM_B_DQ<2>	23
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7	MEM_B_DQ<60>	MEM_B_DQ<60>	24
7	MEM_B_DQ<61>	MEM_B_DQ<61>	24
7	MEM_B_DQ<62>	MEM_B_DQ<62>	24
7	MEM_B_DQ<63>	MEM_B_DQ<63>	24

MAKE_BASE=TRUE

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7	MEM_A_DQS_N<0>	MEM_A_DQS_N<0>	21
7	MEM_A_DQS_P<1>	MEM_A_DQS_P<1>	21
7	MEM_A_DQS_N<1>	MEM_A_DQS_N<1>	21
7	MEM_A_DQS_P<2>	MEM_A_DQS_P<2>	21
7	MEM_A_DQS_N<2>	MEM_A_DQS_N<2>	21
7	MEM_A_DQS_P<3>	MEM_A_DQS_P<3>	21
7	MEM_A_DQS_N<3>	MEM_A_DQS_N<3>	21
7	MEM_A_DQS_P<4>	MEM_A_DQS_P<4>	22
7	MEM_A_DQS_N<4>	MEM_A_DQS_N<4>	22
7	MEM_A_DQS_P<5>	MEM_A_DQS_P<5>	22
7	MEM_A_DQS_N<5>	MEM_A_DQS_N<5>	22
7	MEM_A_DQS_P<6>	MEM_A_DQS_P<6>	22
7	MEM_A_DQS_N<6>	MEM_A_DQS_N<6>	22
7	MEM_A_DQS_P<7>	MEM_A_DQS_P<7>	22
7	MEM_A_DQS_N<7>	MEM_A_DQS_N<7>	22

MAKE_BASE=TRUE

7	MEM_B_DQS_P<0>	MEM_B_DQS_P<0>	23
7	MEM_B_DQS_N<0>	MEM_B_DQS_N<0>	23
7	MEM_B_DQS_P<1>	MEM_B_DQS_P<1>	23
7	MEM_B_DQS_N<1>	MEM_B_DQS_N<1>	23
7	MEM_B_DQS_P<2>	MEM_B_DQS_P<2>	23
7	MEM_B_DQS_N<2>	MEM_B_DQS_N<2>	23
7	MEM_B_DQS_P<3>	MEM_B_DQS_P<3>	23
7	MEM_B_DQS_N<3>	MEM_B_DQS_N<3>	23
7	MEM_B_DQS_P<4>	MEM_B_DQS_P<4>	24
7	MEM_B_DQS_N<4>	MEM_B_DQS_N<4>	24
7	MEM_B_DQS_P<5>	MEM_B_DQS_P<5>	24
7	MEM_B_DQS_N<5>	MEM_B_DQS_N<5>	24
7	MEM_B_DQS_P<6>	MEM_B_DQS_P<6>	24
7	MEM_B_DQS_N<6>	MEM_B_DQS_N<6>	24
7	MEM_B_DQS_P<7>	MEM_B_DQS_P<7>	24
7	MEM_B_DQS_N<7>	MEM_B_DQS_N<7>	24

SYNC_MASTER=AHARTMAN_J52 SYNC_DATE=10/29/2013

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LPDDR3 Bit & Byte Swizzle

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Functional Test Points

J4401 - DFR Display Connector

104 42 38	DFR_DISP_VSYNC	FUNC_TEST=TRUE	
42 38	DFR_DISP_TE	FUNC_TEST=TRUE	
42 38	DFR_DISP_INT	FUNC_TEST=TRUE	
42	DFR_DISP_RESET_L	FUNC_TEST=TRUE	3 TPs
42	PP3V3_S0SW_DFR	FUNC_TEST=TRUE	
105 42	MIPID_CLK_CONN_P	FUNC_TEST=TRUE	
105 42	MIPID_CLK_CONN_N	FUNC_TEST=TRUE	
105 42	MIPID_DATA_CONN_P	FUNC_TEST=TRUE	
105 42	MIPID_DATA_CONN_N	FUNC_TEST=TRUE	
106 104 42 37	PP1V8_S0SW_DFR	FUNC_TEST=TRUE	2 TPs
42 38 37	DFRDRV_I2C_SCL	FUNC_TEST=TRUE	
42 38 37	DFRDRV_I2C_SDA	FUNC_TEST=TRUE	
	GND	FUNC_TEST=TRUE	
	6 TPs		

J4402 - DFR Touch Connector

104 42	DFR_TOUCH_LID	FUNC_TEST=TRUE	
104 42	DFR_TOUCH_LID	FUNC_TEST=TRUE	
42 37	DFR_TOUCH_SPI_CS_L	FUNC_TEST=TRUE	
42	DFR_TOUCH_SPI_MOSI_R	FUNC_TEST=TRUE	
42 38 37	DFR_TOUCH_ROM_I2C_SCL	FUNC_TEST=TRUE	
42 38 37	DFR_TOUCH_ROM_I2C_SDA	FUNC_TEST=TRUE	
42 37	DFR_TOUCH_RESET_L	FUNC_TEST=TRUE	
106 104 42 37	PP1V8_S0SW_DFR	FUNC_TEST=TRUE	2 TPs
101 42	PP5V_S0_T139	FUNC_TEST=TRUE	1 TPs
42 38	DFR_TOUCH_PANEL_DETECT	FUNC_TEST=TRUE	
104 42 38	DFR_DISP_VSYNC	FUNC_TEST=TRUE	
42	DFR_TOUCH_SPI_MISO_R	FUNC_TEST=TRUE	
42	DFR_TOUCH_SPI_CLK_R	FUNC_TEST=TRUE	
42 38	DFR_TOUCH_INT_L	FUNC_TEST=TRUE	
42 38	DFR_CLKIN_RESET_L	FUNC_TEST=TRUE	
42 38	DFR_TOUCH_ROM_WC	FUNC_TEST=TRUE	
106 104 42 37	PP1V8_S0SW_DFR	FUNC_TEST=TRUE	
	GND	FUNC_TEST=TRUE	
	6 TPs		

J4500 - Keyboard Connector

43	PP5V_S0_FAN_CONN	FUNC_TEST=TRUE	8 TPs
43	GND_FAN	FUNC_TEST=TRUE	8 TPs
58 43	FAN_LT_TACH	FUNC_TEST=TRUE	
58 43	FAN_LT_PWM	FUNC_TEST=TRUE	
58 43	FAN_RT_TACH	FUNC_TEST=TRUE	
58 43	FAN_RT_PWM	FUNC_TEST=TRUE	
101 43	PP5V_S0_KBD	FUNC_TEST=TRUE	3 TPs
100 50 43	PP3V3_G3H	FUNC_TEST=TRUE	1 TPs
104 43	KBD_BLC_GSSOUT	FUNC_TEST=TRUE	
104 43	KBD_BLC_GSLAT	FUNC_TEST=TRUE	
101 43	PP3V3_S4	FUNC_TEST=TRUE	
104 43	KBD_BLC_GSSIN	FUNC_TEST=TRUE	
104 43	KBD_BLC_XBLANK	FUNC_TEST=TRUE	
104 43	KBD_I2C_SDA	FUNC_TEST=TRUE	
104 43	KBD_INT_L	FUNC_TEST=TRUE	
104 43	KBD_I2C_SCL	FUNC_TEST=TRUE	
50 43	SMC_LSOC_RST_L	FUNC_TEST=TRUE	
104 43	KBD_BLC_GSSCK	FUNC_TEST=TRUE	
	GND	FUNC_TEST=TRUE	
	6 TPs		

J4501 - Trackpad Connector

104 43	KBD_I2C_SCL	FUNC_TEST=TRUE
104 43	KBD_I2C_SDA	FUNC_TEST=TRUE
104 43	KBD_INT_L	FUNC_TEST=TRUE
51 43	SMBUS_SMC_3_SDA	FUNC_TEST=TRUE
51 43	SMBUS_SMC_3_SCL	FUNC_TEST=TRUE
101 43	PP3V3_S4_TPAD	FUNC_TEST=TRUE
101	PP3V3_S4_TPAD	FUNC_TEST=TRUE
43	PP5V_S4_TPAD_CONN	FUNC_TEST=TRUE
43	ACT_GND	FUNC_TEST=TRUE
43	PPVIN_S4_TPAD_FUSE	FUNC_TEST=TRUE
43	TPAD_SPI_CLK_R	FUNC_TEST=TRUE
43	TPAD_SPI_IF_EN_CONN	FUNC_TEST=TRUE
43	TPAD_SPI_MISO_R	FUNC_TEST=TRUE
43	TPAD_SPI_CS_CONN_R_L	FUNC_TEST=TRUE
43	TPAD_SPI_MOSI_R	FUNC_TEST=TRUE
43	TPAD_SPI_INT_CONN_L	FUNC_TEST=TRUE
50 43	SMC_ACTUATOR_DISABLE_L	FUNC_TEST=TRUE
50 43	SMC_PME_S4_WAKE_L	FUNC_TEST=TRUE
49 43 42 50	SMC_LID	FUNC_TEST=TRUE
104 43	KBD_BLC_GSLAT	FUNC_TEST=TRUE
104 43	KBD_BLC_GSSCK	FUNC_TEST=TRUE
104 43	KBD_BLC_GSSOUT	FUNC_TEST=TRUE
104 43	KBD_BLC_GSSIN	FUNC_TEST=TRUE
104 43	KBD_BLC_XBLANK	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE
	6 TPs	

J4900 - Mesa Connector

47	PP3V0_MESA		2 TPs
	MESA_SPI_MISO_CONN	FUNC_TEST=TRUE	
47	MESA_SNSR_INT_CONN	FUNC_TEST=TRUE	
47	MESA_BOOST_EN_CONN	FUNC_TEST=TRUE	
47 37	MESA_I2C_SDA	FUNC_TEST=TRUE	
47 37	MESA_I2C_SCL	FUNC_TEST=TRUE	
47	ESD_GND	FUNC_TEST=TRUE	1 TPs
47	PP1V8_MESA	FUNC_TEST=TRUE	1 TPs
47	MESA_SPI_MOSI_CONN	FUNC_TEST=TRUE	
47	MENU_KEY_L	FUNC_TEST=TRUE	
47	MESA_SPI_CLK_CONN	FUNC_TEST=TRUE	
47	PP16V0_MESA	FUNC_TEST=TRUE	1 TPs
	GND	FUNC_TEST=TRUE	
	2 TPs		

J6200 - MIC Connector

60	DMIC1_DATA	FUNC_TEST=TRUE
60	DMIC1_CLK	FUNC_TEST=TRUE
	PP1V8_S0	FUNC_TEST=TRUE 1 TPs
60	DMIC2_DATA	FUNC_TEST=TRUE
60	DMIC2_CLK	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE
	2 TPs	

J6410 - Left Tweeter Connector

62	SPKRCONN_TL_OUT_P	FUNC_TEST=TRUE
62	SPKRCONN_TL_OUT_N	FUNC_TEST=TRUE
62 60	8409_SPKR_ID0	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE
	2 TPs	

J6430 - Left Woofer Connector

62	SPKRCONN_WL_OUT_P	FUNC_TEST=TRUE
62	SPKRCONN_WL_OUT_N	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE
	2 TPs	

J6500 - Right Tweeter Connector

63	SPKRCONN_TR_OUT_P	FUNC_TEST=TRUE
63	SPKRCONN_TR_OUT_N	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE
	2 TPs	

J6550 - Right Woofer Connector

63	SPKRCONN_WR_OUT_P	FUNC_TEST=TRUE
63	SPKRCONN_WR_OUT_N	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE
	2 TPs	

J6600 - Audio Jack Connector

104 64	AUD_CONN_HP_LEFT	FUNC_TEST=TRUE	
104 64	AUD_CONN_HP_RIGHT	FUNC_TEST=TRUE	
104 64	AUD_CONN_RING2	FUNC_TEST=TRUE	
104 64	AUD_CONN_SLEEVE	FUNC_TEST=TRUE	
64	AUD_CONN_HP_SENSE_L	FUNC_TEST=TRUE	
	AUD_CONN_HP_SENSE_R	FUNC_TEST=TRUE	
64	AUD_CONN_TIP_SENSE	FUNC_TEST=TRUE	
64	AUD_CONN_SLEEVE_XW	FUNC_TEST=TRUE	2 TPs
64	AUD_CONN_RING2_XW	FUNC_TEST=TRUE	1 TPs
104 64	AUD_CONN_HP_LEFT	FUNC_TEST=TRUE	1 TPs
104 64	AUD_CONN_HP_RIGHT	FUNC_TEST=TRUE	8 TPs
104 64	AUD_CONN_RING2	FUNC_TEST=TRUE	8 TPs
104 64	AUD_CONN_SLEEVE	FUNC_TEST=TRUE	
	GND	FUNC_TEST=TRUE	
	4 TPs		

J6950 - Battery Connector

66 65	PPVBAT_G3H_CONN	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE
	8 TPs	

J6951 - Battery Sense Connector

65	SYS_DETECT_L	FUNC_TEST=TRUE
65 51	SMBUS_SMC_5_G3_SCL	FUNC_TEST=TRUE
65 51	SMBUS_SMC_5_G3_SDA	FUNC_TEST=TRUE
65 54	BMON_IOUT	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE
	1 TPs	

J8500 - eDP Connector

80 79	PPVOUT_S0_LCDBKLT	FUNC_TEST=TRUE	
80 38 37	I2C_CAM_SDA	FUNC_TEST=TRUE	
80 38 37	I2C_CAM_SCL	FUNC_TEST=TRUE	
80 42	I2C_ALS_SCL	FUNC_TEST=TRUE	
80 42	I2C_ALS_SDA	FUNC_TEST=TRUE	
80 51	SMBUS_SMC_0_S0_SCL	FUNC_TEST=TRUE	
80 51	SMBUS_SMC_0_S0_SDA	FUNC_TEST=TRUE	
102 80	I2C_BKLT_SCL	FUNC_TEST=TRUE	
102 80	I2C_BKLT_SDA	FUNC_TEST=TRUE	
80 5	BKLT_PWM_MLB2TCON	FUNC_TEST=TRUE	
80 48	BKLT_PWM_TCON2MLB	FUNC_TEST=TRUE	
80 16	LCD_IRQ_L	FUNC_TEST=TRUE	
80 5	DP_INT_HPD	FUNC_TEST=TRUE	
80	BUF_EDP_PANEL_PWR_EN	FUNC_TEST=TRUE	
106 80	PP3V3_S0SW_LCD	FUNC_TEST=TRUE	7 TPs
106 80	PP5V_S0SW_LCD	FUNC_TEST=TRUE	1 TPs
106 80 38	PP5V_S0_ALSCAM_F	FUNC_TEST=TRUE	
105 80 38	MIPI_CLK_CONN_P	FUNC_TEST=TRUE	
105 80 38	MIPI_CLK_CONN_N	FUNC_TEST=TRUE	
105 80 38	MIPI_DATA_CONN_P	FUNC_TEST=TRUE	
105 80 38	MIPI_DATA_CONN_N	FUNC_TEST=TRUE	
80	EDP_INT_ML_P<3>	FUNC_TEST=TRUE	
80	EDP_INT_ML_N<3>	FUNC_TEST=TRUE	
80	EDP_INT_ML_P<2>	FUNC_TEST=TRUE	
80	EDP_INT_ML_N<2>	FUNC_TEST=TRUE	
80	EDP_INT_ML_P<1>	FUNC_TEST=TRUE	
80	EDP_INT_ML_N<1>	FUNC_TEST=TRUE	
80	EDP_INT_ML_P<0>	FUNC_TEST=TRUE	
80	EDP_INT_ML_N<0>	FUNC_TEST=TRUE	
80	EDP_INT_AUX_P	FUNC_TEST=TRUE	
80	EDP_INT_AUX_N	FUNC_TEST=TRUE	
	GND	FUNC_TEST=TRUE	
	8 TPs		

Probe Block Grid - WiPass and NAND Rack

15	TP_USB_TESTERN	FUNC_TEST=TRUE
15	TP_USB_TESTERP	FUNC_TEST=TRUE
15	TP_USB3_03_D2RN	FUNC_TEST=TRUE
15	TP_USB3_03_D2RP	FUNC_TEST=TRUE
15	TP_USB3_03_R2DN	FUNC_TEST=TRUE
15	TP_USB3_03_R2DP	FUNC_TEST=TRUE
	SMC_DEBUGPRT_RX_L	FUNC_TEST=TRUE
49 48 28	SMC_DEBUGPRT_TX_L	FUNC_TEST=TRUE
91 19 16	SSD_RESET_L	FUNC_TEST=TRUE
91 84	STORAGE_EN	FUNC_TEST=TRUE
102 91	SSD_SR_EN_L	FUNC_TEST=TRUE
91 14	SSD_BOOT_L	FUNC_TEST=TRUE
88 84	SSD_DBG_UART_R2D	FUNC_TEST=TRUE
88 84 19	SSD_DBG_UART_D2R	FUNC_TEST=TRUE
	SSD_PWR_EN_L	FUNC_TEST=TRUE
84 81	S3X_JTAG_SEL	FUNC_TEST=TRUE
94 84 81	S3X_JTAG_TCK	FUNC_TEST=TRUE
84 81	S3X_JTAG_TDI	FUNC_TEST=TRUE
84 81	S3X_JTAG_TDO	FUNC_TEST=TRUE
94 84 81	S3X_JTAG_TMS	FUNC_TEST=TRUE
84 81	S3X_JTAG_TRST_L	FUNC_TEST=TRUE
88 87 86 85 84 82 81 19	PP1V8_SSD_COLD	FUNC_TEST=TRUE
	PPDCIN_G3H_CHGR	FUNC_TEST=TRUE
66	PPVBAT_G3H_CHGR_REG	FUNC_TEST=TRUE
100 54 8	PPVCC_S0_CPU	FUNC_TEST=TRUE 4 TPs
88 82	PP0V9_SSD_REG	FUNC_TEST=TRUE 4 TPs
50 49 48 47	SMC_ONOFF_L	FUNC_TEST=TRUE
50	TP_SMC_DEV_SUPPLY_L	FUNC_TEST=TRUE
73 48 14	PM_PCH_SYS_PWROK	FUNC_TEST=TRUE
101 72	PP5V_S4	FUNC_TEST=TRUE
100 66	PPDCIN_G3H	FUNC_TEST=TRUE
104 92 80 77 74 73 48 26 19 14	PM_SLP_S3_L	FUNC_TEST=TRUE
35 19 14	PLT_RST_L	FUNC_TEST=TRUE
100 65	PP3V3_G3H	FUNC_TEST=TRUE
66	HPWR_EN_L	FUNC_TEST=TRUE
80 66 59 50	SMC_RESET_L	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE
	3 TPs; 1x for USB2 pair, 1x for USB3 R2D, 1x for USB3 D2R	

Debug LEDs

77 48 19 14	PM_SLP_S5_L	FUNC_TEST=TRUE
8 TPs 77 74 48 43 19 14	PM_SLP_S4_L	FUNC_TEST=TRUE
104 92 80 77 74 73 48 26 19 14	PM_SLP_S3_L	FUNC_TEST=TRUE
74 48 19 14	PM_SLP_S0_L	FUNC_TEST=TRUE
	PM_SLP_SUS_L	FUNC_TEST=TRUE

J3300 - Left USB-C Connector

31	PP20V_USBC_XA_VBUS_CONN	FUNC_TEST=TRUE
	4 TPs	
31	PP20V_USBC_XB_VBUS_CONN	FUNC_TEST=TRUE
	4 TPs	
31 29 28	USBC_XA_CC1	FUNC_TEST=TRUE
31 29 28	USBC_XA_CC2	FUNC_TEST=TRUE
31 30 28	USBC_XB_CC1	FUNC_TEST=TRUE
31 30 28	USBC_XB_CC2	FUNC_TEST=TRUE
31	TP_USBC_PP20V_XB	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE
	4 TPs	

JB500 - Right USB-C Connector

97	PP20V_USBC_TA_VBUS_CONN	FUNC_TEST=TRUE
	4 TPs	
97	PP20V_USBC_TB_VBUS_CONN	FUNC_TEST=TRUE
	4 TPs	
97 95 94	USBC_TA_CC1	FUNC_TEST=TRUE
97 95 94	USBC_TA_CC2	FUNC_TEST=TRUE
97 96 94	USBC_TB_CC1	FUNC_TEST=TRUE
97 96 94	USBC_TB_CC2	FUNC_TEST=TRUE
97	TP_USBC_PP20V_TB	FUNC_TEST=TRUE
97	TP_USBC_PP20V_TA	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE
	4 TPs	

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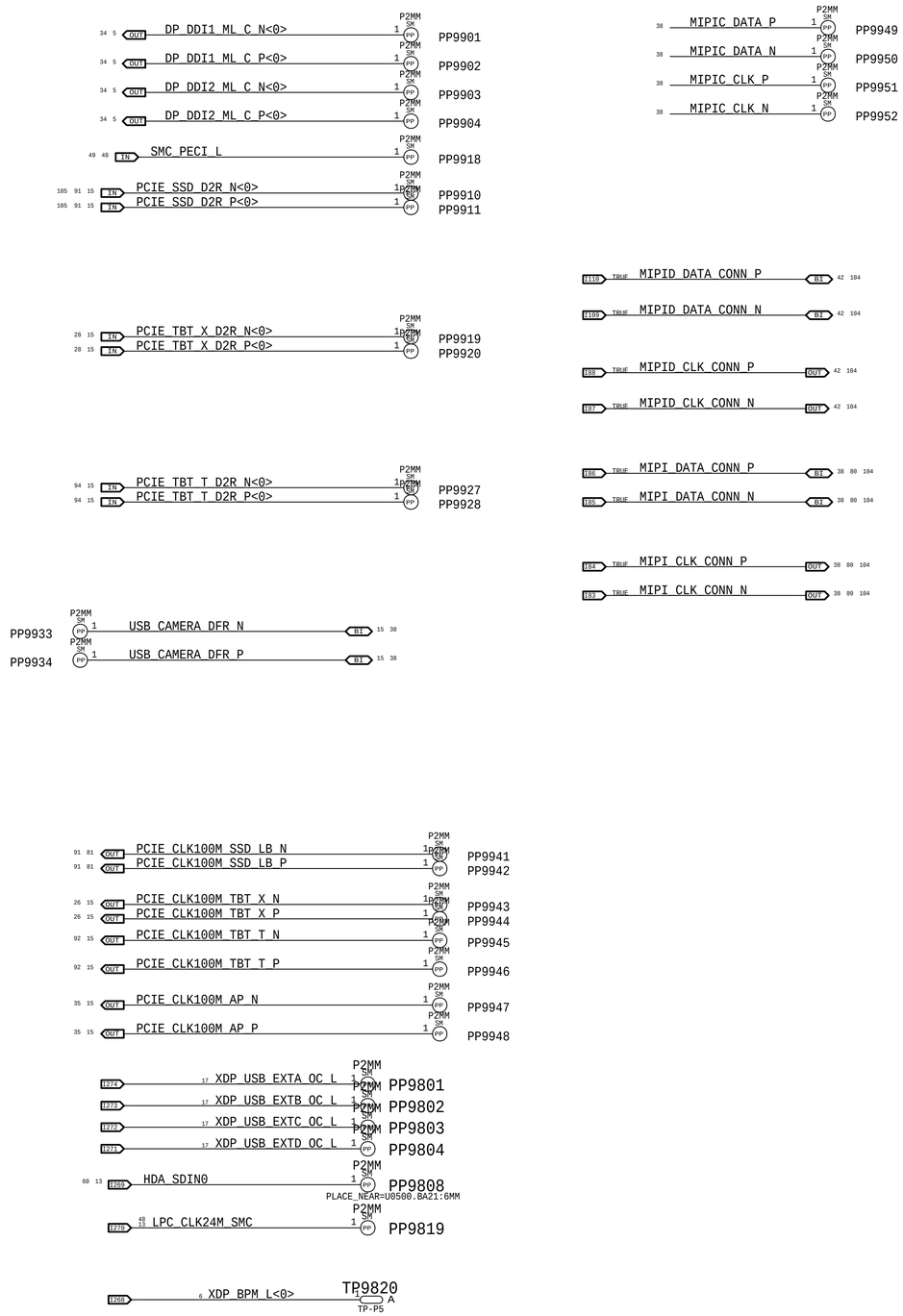

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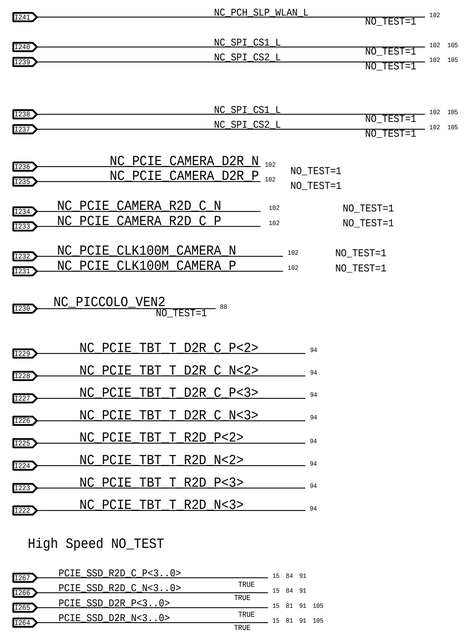

Unused nets with offpage

(Nets with offpages not used on this project)

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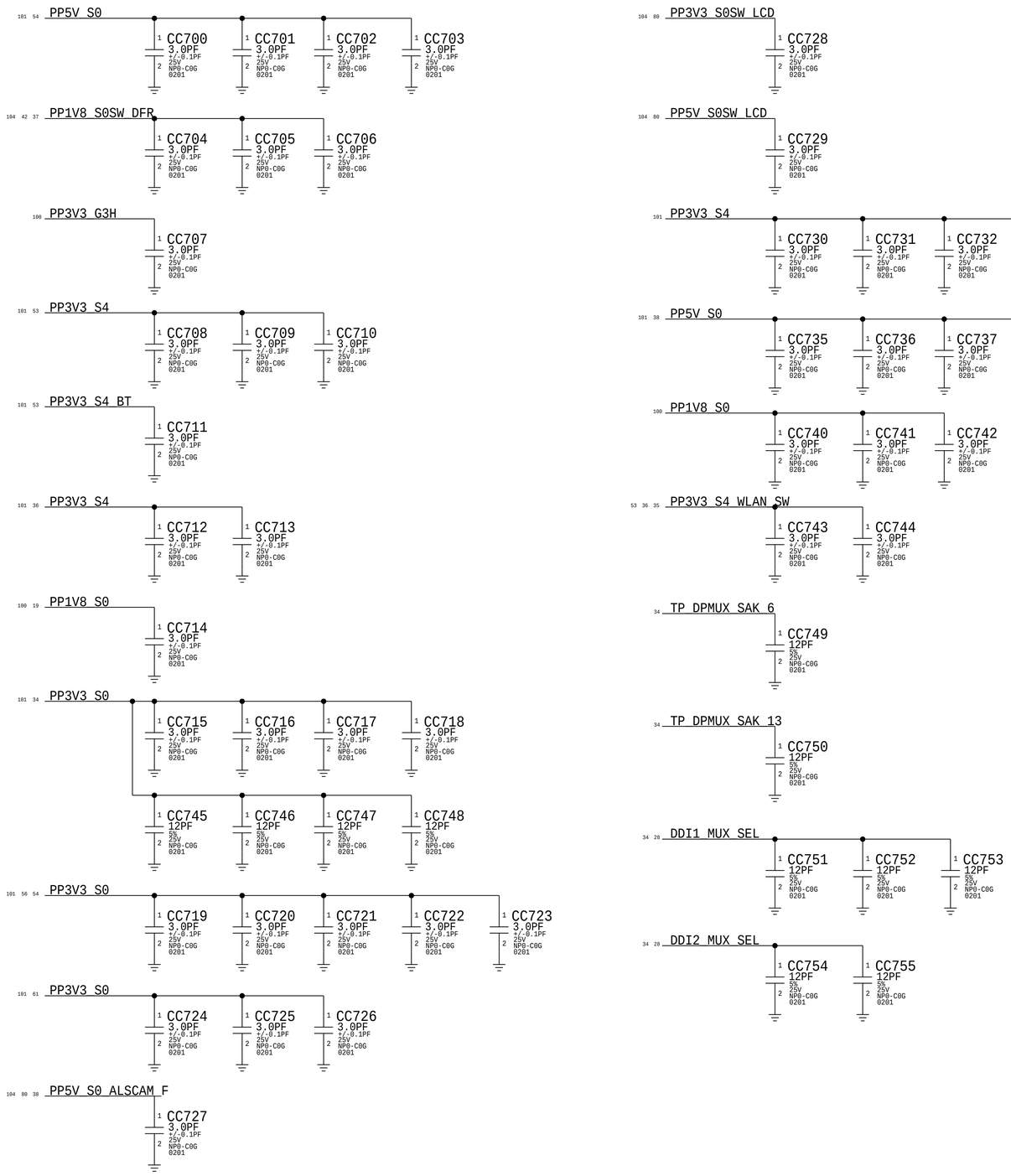

BOM_COST_GROUP=WIRELESS

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Desense Capacitors

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J79 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

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PCB Rule Definitions

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_08MIL	*	0.203 MM	?
CPU_12MIL	*	0.305 MM	?
CPU_18MIL	*	0.457 MM	?
CPU_25MIL	*	0.635 MM	?

CPU Signal Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING

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CPU Constraints

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
PCH_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_12MIL	*	0.305 MM	?
PCH_15MIL	*	0.381 MM	?
PCH_18MIL	*	0.457 MM	?
PCH_20MIL	*	0.508 MM	?

PCH Net Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_75D	*	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF
MEM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=4x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=6x_DIELECTRIC	?
MEM_CMD2CMD	*	=6x_DIELECTRIC	?
MEM_CMD2CTL	*	=6x_DIELECTRIC	?
MEM_CTL2CTL	*	=6x_DIELECTRIC	?
MEM_CLK2CLK	*	=12x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=16x_DIELECTRIC	?
MEM_2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_2PWR	*	=4x_DIELECTRIC	?
MEM_2GND	*	=4x_DIELECTRIC	?
MEM_2OTHER	*	=12x_DIELECTRIC	?
MEM_12MIL	*	0.305 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=10x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=10x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=10x_DIELECTRIC	?
MEM_CMD2CTL	TOP,BOTTOM	=10x_DIELECTRIC	?
MEM_CTL2CTL	TOP,BOTTOM	=10x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=16x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=16x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=20x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF_B	*	=1.5x_DIELECTRIC	?
MEM_DQS2OWNDATA_B	*	=1.5x_DIELECTRIC	?
MEM_CMD2CMD_B	*	=1.5x_DIELECTRIC	?
MEM_CMD2CTL_B	*	=1.5x_DIELECTRIC	?
MEM_CTL2CTL_B	*	=1.5x_DIELECTRIC	?
MEM_CLK2CLK_B	*	=1.5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2OTHERMEM_B	*	=1.5x_DIELECTRIC	?
MEM_2OTHERMEM_B	*	=1.5x_DIELECTRIC	?
MEM_2OTHER_B	*	=1.5x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	*	BGA_MEM	MEM_2OTHER_B
MEM_*_DQS_*	*	BGA_MEM	MEM_2OTHER_B
MEM_CMD	*	BGA_MEM	MEM_2OTHER_B
MEM_CTL	*	BGA_MEM	MEM_2OTHER_B
MEM_CLK	*	BGA_MEM	MEM_2OTHER_B
MEM_*	MEM_*	BGA_MEM	MEM_2OTHERMEM_B

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	=SAME	BGA_MEM	MEM_DATA2SELF_B

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	MEM_*	BGA_MEM	MEM_DATA2OTHERMEM_B

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTL	*	MEM_CMD2CTL
MEM_CTL	MEM_CTL	*	MEM_CTL2CTL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	BGA_MEM	MEM_CMD2CMD_B
MEM_CMD	MEM_CTL	BGA_MEM	MEM_CMD2CTL_B
MEM_CTL	MEM_CTL	BGA_MEM	MEM_CTL2CTL_B
MEM_CLK	MEM_CLK	BGA_MEM	MEM_CLK2CLK_B

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DQBYTE_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DQBYTE_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DQBYTE_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DQBYTE_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DQBYTE_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DQBYTE_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DQBYTE_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DQBYTE_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DQBYTE_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DQBYTE_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DQBYTE_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DQBYTE_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DQBYTE_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DQBYTE_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DQBYTE_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DQBYTE_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DQBYTE_0	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_A_DQS_1	MEM_A_DQBYTE_1	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_A_DQS_2	MEM_A_DQBYTE_2	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_A_DQS_3	MEM_A_DQBYTE_3	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_A_DQS_4	MEM_A_DQBYTE_4	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_A_DQS_5	MEM_A_DQBYTE_5	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_A_DQS_6	MEM_A_DQBYTE_6	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_A_DQS_7	MEM_A_DQBYTE_7	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_B_DQS_0	MEM_B_DQBYTE_0	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_B_DQS_1	MEM_B_DQBYTE_1	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_B_DQS_2	MEM_B_DQBYTE_2	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_B_DQS_3	MEM_B_DQBYTE_3	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_B_DQS_4	MEM_B_DQBYTE_4	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_B_DQS_5	MEM_B_DQBYTE_5	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_B_DQS_6	MEM_B_DQBYTE_6	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_B_DQS_7	MEM_B_DQBYTE_7	BGA_MEM	MEM_DQS2OWNDATA_B

Memory Net Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	BGA_MEM	MEM_80D
MEM_40S	BGA_MEM	MEM_45S

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/02/2013

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Memory Constraints

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Thunderbolt, DP, HDMI Constraints

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt & DisplayPort Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3X_DIELECTRIC	?
TBTDP_TXRX	*	=6X_DIELECTRIC	?
TBTDP_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	*	*	TBTDP_2OTHER
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_TX	*_RX	*	TBTDP_TXRX
TBTDP_RX	*_TX	*	TBTDP_TXRX

DisplayPort & HDMI Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?
HDMICLK_2DPHDMI	*	=4x_DIELECTRIC	?
HDMIDATA_2SAME	*	=3x_DIELECTRIC	?
HDMIDATA_2OTHER	*	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICLK_2DPHDMI	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMIDATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
HDMIDATA_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDMI_DATA	*	*	HDMIDATA_2OTHER
HDMI_DATA	=SAME	*	HDMIDATA_2SAME
HDMI_DATA	TBTDP_TX	*	HDMIDATA_2SAME
HDMI_DATA	TBTDP_RX	*	TBTDP_TXRX
HDMI_CLK	*	*	HDMICLK_2OTHER
HDMI_CLK	HDMI_DATA	*	HDMICLK_2DPHDMI
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DPHDMI
HDMI_CLK	TBTDP_TX	*	HDMICLK_2DPHDMI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	*	*	DP_2OTHER
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	HDMI_DATA	*	DP_2SAME
DISPLAYPORT	TBTDP_TX	*	DP_2SAME
DISPLAYPORT	TBTDP_RX	*	TBTDP_TXRX

Thunderbolt, DP, HDMI Net Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING

SYNC_MASTER=J79_JACK SYNC_DATE=05/19/2015

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TBT DP HDMI Constraints

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PCI Express Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=3X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER
PCIE_TX	*_RX	*	PCIE_TXRX
PCIE_RX	*_TX	*	PCIE_TXRX

PCI Express Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING

SYNC_MASTER=J79_JACK SYNC_DATE=05/19/2015

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PCIe Constraints

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USB 2 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?

USB 3 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	*	*	USB3_2OTHER
USB3_*	=SAME	*	USB3_2SAME
USB3_TX	*_RX	*	USB3_TXRX
USB3_RX	*_TX	*	USB3_TXRX

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_25M	*	=5x_DIELECTRIC	?

SATA Interface Constraints (Not Used)

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	*	*	SATA_2OTHER
SATA_*	=SAME	*	SATA_2SAME
SATA_TX	*_RX	*	SATA_TXRX
SATA_RX	*_TX	*	SATA_TXRX

USB Constraints

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING

SMC SMBus & Charger Net Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/02/2013

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SMC Constraints

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
THERM_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
DIG_AUDIO	*	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	0.1 MM	0.1 MM
ANL_AUDIO	*	=1TO1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
ANL_AUDIO_WIDE	*	=1TO1_DIFFPAIR	0.3 MM	0.3 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.070 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.100 MM	500 MIL		
CPU_27P4S	BOTTOM			0.230 MM	100 MIL		
USB3_85D	TOP			0.100 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

DP, SATA, HDMI, PCIE CONSTRAINT RELAXATIONS

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_85D	BGA	P65_BGA
PCIE_85D	BGA	P65_BGA
CLK_PCIE_85D	BGA	P65_BGA
HDMI_85D	BGA	P65_BGA

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SENSE_45S	*	SENSE_45S
THERM_45S	*	THERM_45S
DIG_AUDIO	*	DIG_AUDIO
ANL_AUDIO	*	ANL_AUDIO

J79 Specific Net Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING

J79 Specific Net Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING

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Change List:
<RDAR://COMPONENT/XXXXXX> J79 HW EE SCHEMATIC | PROTO 0

Kismet:
AFP://KISMET.APPLE.COM/KISMET-PROJECTS/J79

Useful Wiki Links:
Schematic Conventions - https://hmts.ecs.apple.com/wiki/index.php/User:Wferry/SchConventions
Schematic Design Wiki - https://hmts.ecs.apple.com/wiki/index.php/Schematic_Design

MobileMac HW Radar:
<rdar://component/XXXXXX> MobileMac HW | Task
<rdar://component/XXXXXX> MobileMac HW | Schematic
<rdar://component/XXXXXX> MobileMac HW | New Bugs
<rdar://component/XXXXXX> MobileMac HW | Layout
<rdar://component/XXXXXX> MobileMac HW | Investigation
<rdar://component/XXXXXX> MobileMac HW | Architecture

Other Info:
Page Allocations - <rdar://problem/19817053> 2015 Schematic Page Allocations

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Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S00033	107S00034		ALL	
138S0738	138S1101		ALL	Samsung alt to Murata
138S0846	138S0811		ALL	Samsung alt to Murata
152S00359	152S00253		ALL	Chilisin alt to Cyntec
371S0704	371S00077		ALL	NXP alt to Diodes
376S1053	376S0604		ALL	Diodes alt to Fairchild
376S1106	376S0678		ALL	Fairchild alt to Vishay
740S00027	740S0159		ALL	Bourns alt to Little Fuse
107S0249	107S0251		ALL	
107S00015	107S00011		ALL	
107S00071	107S00053		ALL	
128S0364	128S0264		ALL	Kemet w/ Panasonic
128S0325	128S0397		ALL	
128S00009	128S00007		ALL	
128S00029	128S00007		ALL	
128S00070	128S00007		ALL	
128S00010	128S00011		ALL	
128S00031	128S00011		ALL	
128S00026	128S00011		ALL	
132S00064	132S0409		ALL	
138S0614	138S0578		ALL	
138S0703	138S0648		ALL	
138S00032	138S0831		ALL	
138S00049	138S0831		ALL	
138S0863	138S0853		ALL	
138S0775	138S0860		ALL	
138S00084	138S00060		ALL	
152S00369	152S00268		ALL	Cyntec w/ NEC
155S00188	155S0275		ALL	Murata w/ Taiyo
155S0694	155S0387		ALL	
155S0660	155S0513		ALL	
155S00018	155S0664		ALL	Murata w/ Taiyo
155S00007	155S0667		ALL	

BLC

155S0914	155S0897		ALL	
155S00190	155S0897		ALL	
311S00004	311S0370		ALL	
311S00013	311S0508		ALL	NXP w/ Diodes
353S00107	353S3239		ALL	
353S00525	353S4471		ALL	
372S0186	372S0185		ALL	
376S00014	376S0761		ALL	
376S00086	376S0761		ALL	
376S1080	376S0820		ALL	
376S00074	376S0855		ALL	
376S1089	376S1128		ALL	
740S0144	740S0118		ALL	
740S00028	740S0118		ALL	
740S00003	740S0135		ALL	
998-04070	998-04071		ALL	Hynix alt to SS

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S00046	197S00036		ALL	Epson w/ TXC
197S00047	197S00036		ALL	Kyocera w/ TXC
197S00048	197S00036		ALL	Murata w/ TXC
197S00053	197S00050		ALL	Kyocera w/ TXC
197S00054	197S00050		ALL	NDK w/ TXC
197S00055	197S00050		ALL	Murata w/ TXC
311S0596	311S0593		ALL	NXP w/ Diodes
107S0276	107S00020		ALL	Cyntec w/ TFT
107S00021	107S0284		ALL	TFT w/ Yageo
152S00343	152S1682		ALL	NXP w/ Diodes
107S00087	107S00029		ALL	TFT w/ Yageo
128S00058	128S00018		ALL	NEC w/ Rohm
138S0706	138S0739		ALL	NEC w/ Vishay
138S0945	138S0739		ALL	NEC w/ Rohm
152S00358	152S00208		ALL	Murata w/ Chillisin
152S00400	152S00361		ALL	Murata w/ Cyntec
152S1872	152S00361		ALL	Murata w/ Cyntec
155S00034	155S0706		ALL	Taiyo w/ Murata

353S00711	353S2073		ALL	On Semi w/ TI

740S00019	740S00007		ALL	Bourns w/ Polytronics
155S00189	155S0342		ALL	Murata w/ Taiyo
138S0714	138S0713		ALL	Murata w/ Samsung
138S0715	138S0732		ALL	Murata w/ Samsung
107S00086	107S00056		ALL	TFT w/ Cyntec
138S0875	138S0678		ALL	Taiyo w/ Mur&SS
138S0786	138S0705		ALL	Murata w/ Samsung
152S2052	152S1954		ALL	Taiyo w/ Cyntec
152S2015	152S1958		ALL	Taiyo w/ Cyntec
138S0789	138S0941		ALL	Murata w/ SS
107S00101	107S00005		ALL	Cyntec w/ Yageo
107S00102	107S00017		ALL	Cyntec w/ Yageo
107S00100	107S00057		ALL	Cyntec w/ TFT
107S00103	107S00058		ALL	Cyntec w/ Yageo
107S00104	107S00061		ALL	Cyntec w/ Yageo
107S00105	107S00062		ALL	Cyntec w/ Yageo
152S00403	152S00322		ALL	Murata w/ Chillisin

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00104	138S0978		ALL	Murata w/ Taiyo
311S00072	311S0657		ALL	NXP w/ On Semi
311S00090	311S00028		ALL	On Semi w/ TI
353S00854	353S4342		ALL	TI w/ ST
377S0077	377S0183		ALL	Infineon w/ ST

138S0700	138S0641		ALL	Murata w/ SS&Taiyo
152S00363	152S00048		ALL	Cyntec w/ Vishay
155S0659	155S0382		ALL	Murata w/ TDK
376S00146	376S1061		ALL	NXP w/ Diodes

128S00062	128S00067		ALL	
128S00069	128S00067		ALL	
132S00012	132S0401		ALL	
138S0660	138S0684		ALL	
138S1103	138S0719		ALL	
138S00097	138S0750		ALL	
138S00111	138S00036		ALL	
155S00203	155S0894		ALL	
197S00082	197S00081		ALL	
311S00060	311S0273		ALL	
311S00118	311S0489		ALL	
311S0271	311S00008		ALL	
311S00104	311S00091		ALL	
311S0437	311S00112		ALL	
335S00213	335S0888		ALL	
343S00136	343S00135		ALL	
343S00137	343S00135		ALL	
343S00138	343S00135		ALL	
353S00880	353S3452		ALL	
353S00878	353S00599		ALL	
353S00879	353S00754		ALL	
353S00750	353S00877		ALL	
371S00089	371S00085		ALL	
377S0178	377S00031		ALL	

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