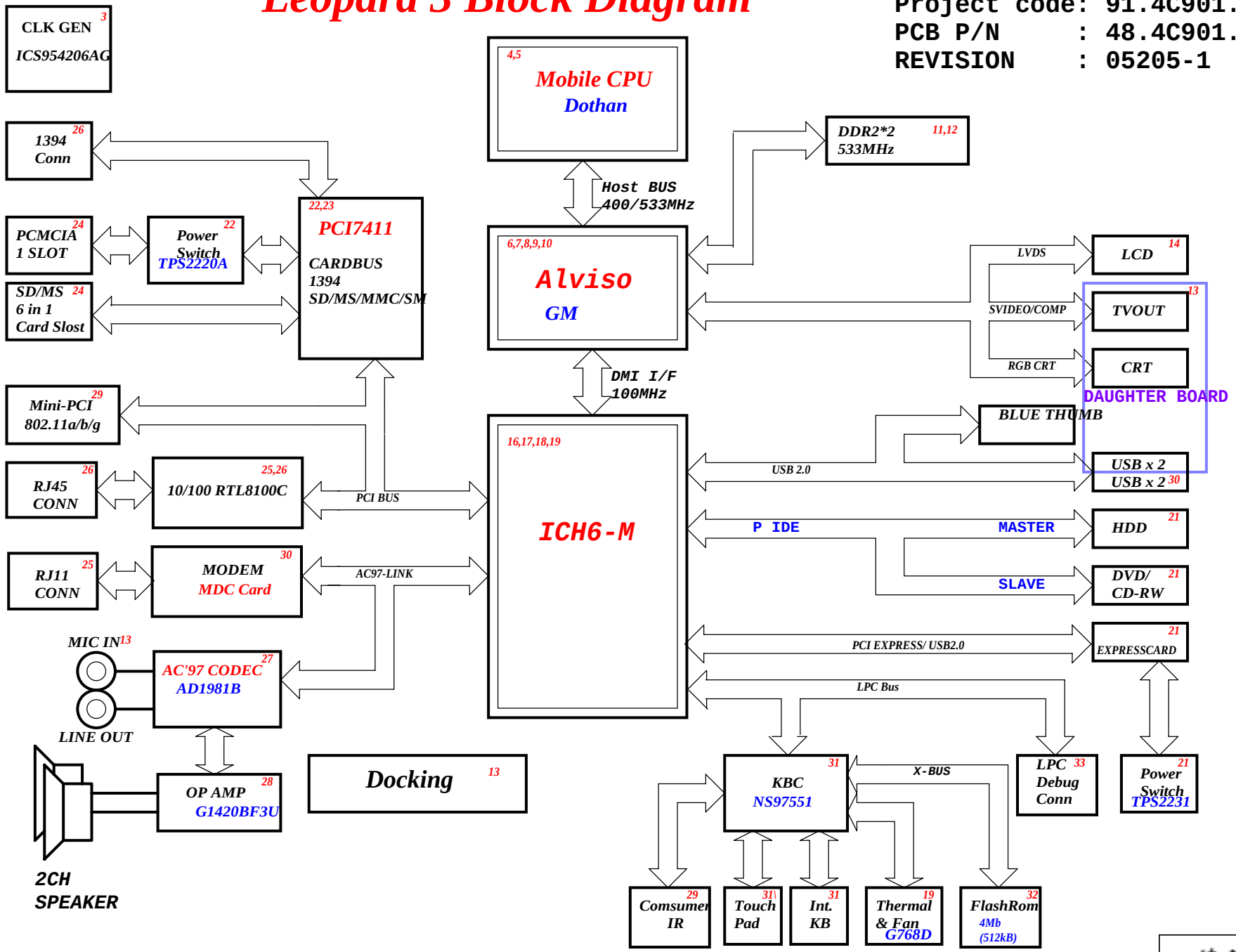
Leopard 3 Block Diagram

Project code: 91.4C901.001
PCB P/N : 48.4C901.001
REVISION : 05205-1



SYSTEM DC/DC 36 MAX1999	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S5

SYSTEM DC/DC 37 TPS5130	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_S0 1D8V_S3

MAXIM CHARGER 34 MAX1909	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC 35 MAX1907	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

Size	Document Number	Rev
A3	Leopard 3	-1

Date: Tuesday, July 19, 2005 Sheet 1 of 41

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

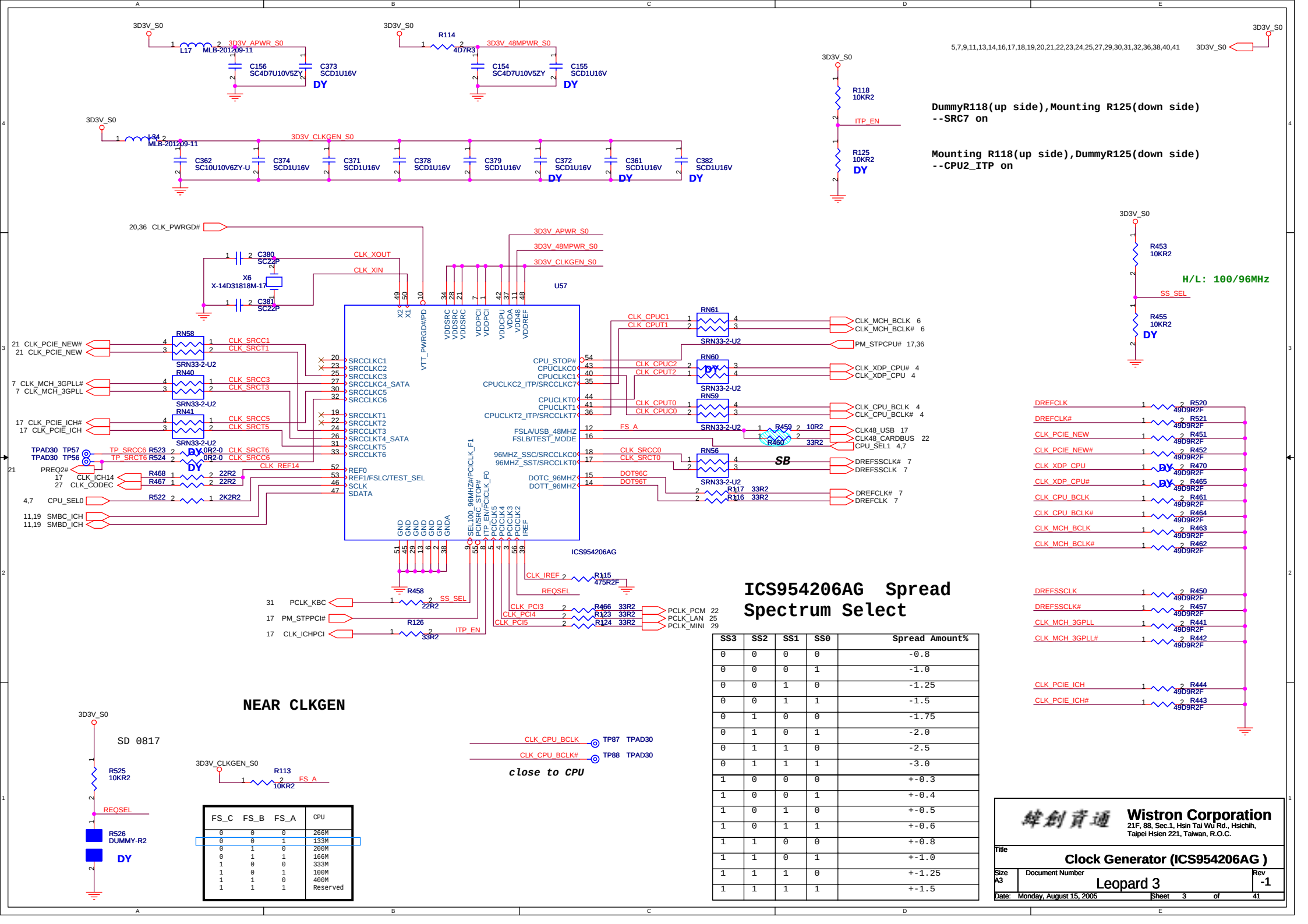
Power name description

5V_S0= 5 Voltage power up on system work(S0 state)
5V_S3= 5 Voltage suspend to RAM(S3 state)
5V_S5= 5 Voltage soft off(S5 state)
3D3V_S0= 3.3 Voltage power up on system work(S0 state)
3D3V_S3= 3.3 Voltage suspend to RAM(S3 state)
3D3V_S5= 3.3 Voltage soft off(S5 state)
LVDDR_1D8V= 1.8 Voltage power up on system work(S0 state)
1D8V_S3= 1.8Voltage suspend to RAM(S3 state)
2D5V_S0= 2.5 Voltage power up on system work(S0 state)

VCC_CORE_S0= CPU VID Voltage power up on system work(S0 state)
1D5V_VCCA_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S5= 1.5 Voltage soft off(S5 state)
DDR_VREF_S3= 0.9 Voltage suspend to RAM(S3 state)
0D9V_S0= 1.25 Voltage power up on system work(S0 state)
1D2_VGA_S0= 1.2 Voltage power up on system work(S0 state) for VGA
1D05V_S0= 1.05 Voltage power up on system work(S0 state)
CORE_GMCH_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power
VCCP_GMCH_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power

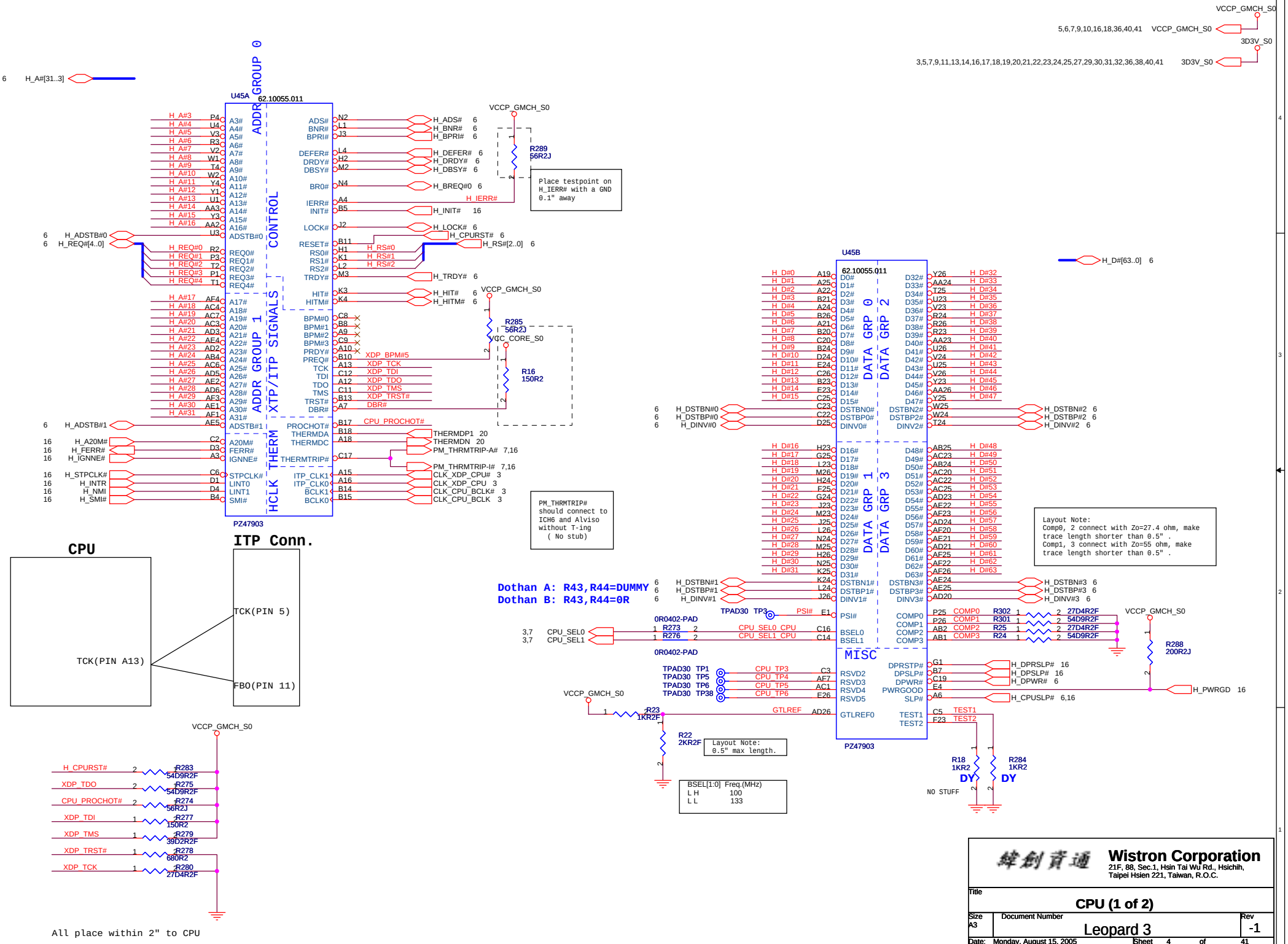
PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD21	P_INTE#	REQ0#/GNT0#
Cardbus Controller TI7411	AD22	(CARBUS)P_INTG# (1394)P_INTF# (CARD READER)P_INTG#	REQ1#/GNT1#
LAN	AD23	P_INTE#	REQ2#/GNT2#
Blue Thumb	AD24		



FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved

SS3	SS2	SS1	SS0	Spread Amount%
0	0	0	0	-0.8
0	0	0	1	-1.0
0	0	1	0	-1.25
0	0	1	1	-1.5
0	1	0	0	-1.75
0	1	0	1	-2.0
0	1	1	0	-2.5
0	1	1	1	-3.0
1	0	0	0	+-0.3
1	0	0	1	+-0.4
1	0	1	0	+-0.5
1	0	1	1	+-0.6
1	1	0	0	+-0.8
1	1	0	1	+-1.0
1	1	1	0	+-1.25
1	1	1	1	+-1.5


VCCP_GMCH_S0
5,6,7,9,10,16,18,36,40,41 VCCP_GMCH_S0
3D3V_S0
3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41 3D3V_S0
6 H_A#[31..3]
U45A 62.10055.011
ADDR GROUP 0
ADDR GROUP 1
XTP/ITP SIGNALS
CONTROL
HCLK THERM
PZ47903
H_ADS# 6
H_BNR# 6
H_BPRI# 6
H_DEFER# 6
H_DRDY# 6
H_DBSY# 6
H_BREQ#0 6
H_IERR#
H_INIT# 16
H_LOCK# 6
H_CPURST# 6
H_RS#[2..0] 6
H_TRDY# 6
H_HIT# 6
H_HITM# 6
R289 56R2J
Place testpoint on H_IERR# with a GND 0.1" away
6 H_ADSTB#0
6 H_REQ#[4..0]
6 H_ADSTB#1
16 H_A20M#
16 H_FERR#
16 H_IGNNE#
16 H_STPCLK#
16 H_INTR
16 H_NMI
16 H_SMI#
XDP_BPM#5
XDP_TCK
XDP_TDI
XDP_TDO
XDP_TMS
XDP_TRST#
DBR#
CPU_PROCHOT#
THERMDP1 20
THERMDN 20
PM_THRMTRIP-A# 7,16
PM_THRMTRIP-I# 7,16
CLK_XDP_CPU# 3
CLK_XDP_CPU 3
CLK_CPU_BCLK# 3
CLK_CPU_BCLK 3
R285 56R2J
VCC_CORE_S0
R16 150R2
PM_THRMTRIP# should connect to ICH6 and Alviso without T-ing (No stub)
CPU
TCK(PIN A13)
ITP Conn.
TCK(PIN 5)
FBO(PIN 11)
VCCP_GMCH_S0
H_CPURST# R283 54D9R2F
XDP_TDO R275 54D9R2F
CPU_PROCHOT# R274 56R2J
XDP_TDI R277 150R2
XDP_TMS R279 39D2R2F
XDP_TRST# R278 680R2
XDP_TCK R280 27D4R2F
All place within 2" to CPU
U45B
62.10055.011
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
PZ47903
H_D#[63..0] 6
6 H_DSTBN#0
6 H_DSTBP#0
6 H_DINV#0
H_DSTBN#2 6
H_DSTBP#2 6
H_DINV#2 6
6 H_DSTBN#1
6 H_DSTBP#1
6 H_DINV#1
H_DSTBN#3 6
H_DSTBP#3 6
H_DINV#3 6
Dothan A: R43,R44=DUMMY
Dothan B: R43,R44=0R
TPAD30 TP3
PSI#
0R0402-PAD
3,7 CPU_SEL0
3,7 CPU_SEL1
R273
R276
CPU_SEL0_CPU
CPU_SEL1_CPU
TPAD30 TP1
TPAD30 TP5
TPAD30 TP6
TPAD30 TP38
CPU_TP3
CPU_TP4
CPU_TP5
CPU_TP6
VCCP_GMCH_S0
R23 1KR2F
GTLREF
R22 2KR2F
Layout Note: 0.5" max length.
BSEL[1:0] Freq.(MHz)
L H 100
L L 133
P25 COMP0 R302 27D4R2F
P26 COMP1 R301 54D9R2F
AB2 COMP2 R25 27D4R2F
AB1 COMP3 R24 54D9R2F
R288 200R2J
H_DPRSLP# 16
H_DPSLP# 16
H_DPWR# 6
H_PWRGD 16
H_CPUSLP# 6,16
TEST1
TEST2
R18 1KR2 DY
R284 1KR2 DY
NO STUFF
Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" .
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
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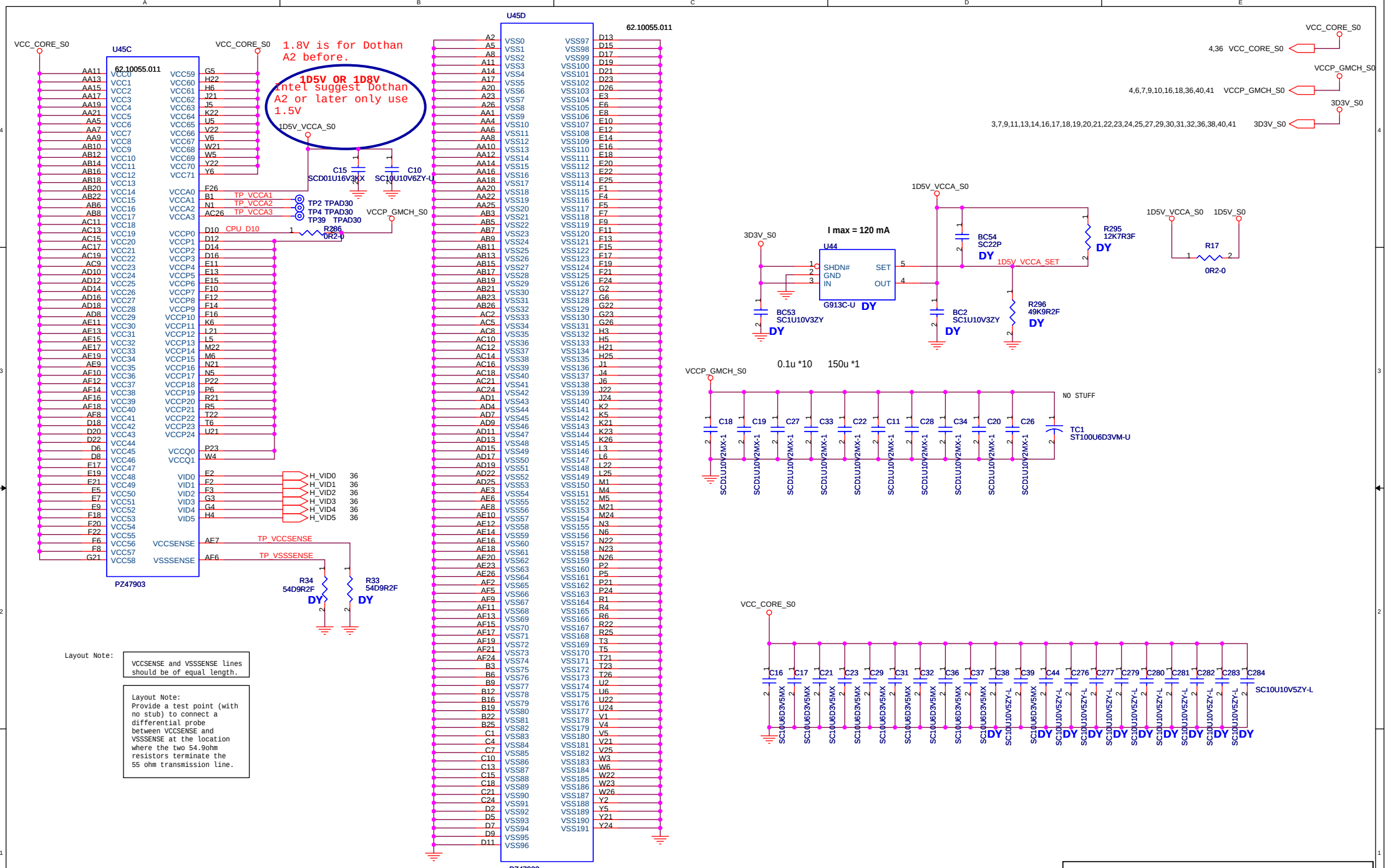
Title
CPU (1 of 2)
Size A3
Document Number
Leopard 3
Rev -1
Date: Monday, August 15, 2005
Sheet 4 of 41



Layout Note:

VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

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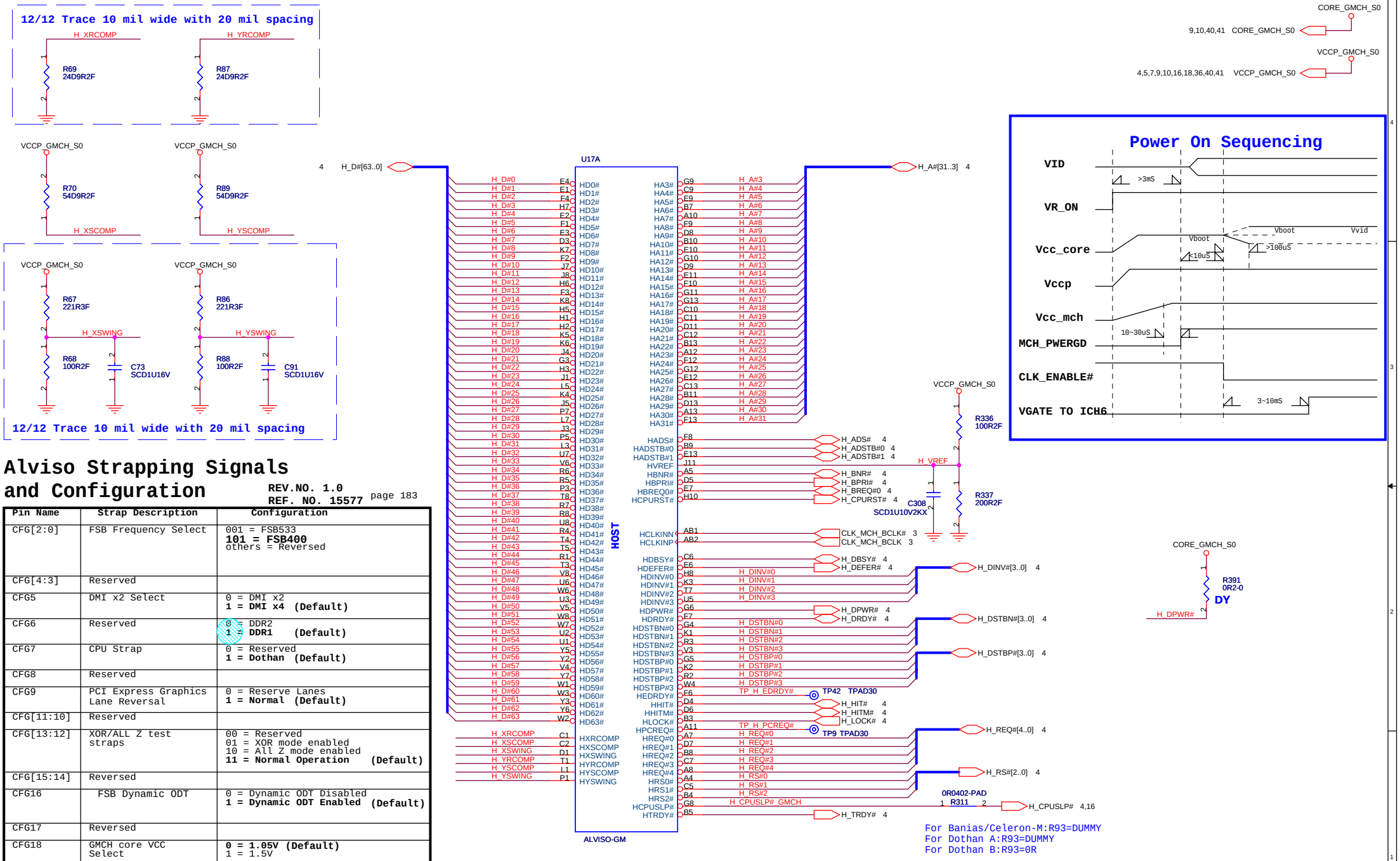
Title	CPU (2 of 2)	
Size A3	Document Number Leopard 3	Rev -1
Date: Monday, August 15, 2005	Sheet 5 of 41	



Alviso Strapping Signals and Configuration

REV.NO. 1.0
REF. NO. 15577 page 183

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 **101 = FSB400** others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	Reserved	0 = DDR2 **1 = DDR1 (Default)**
CFG7	CPU Strap	0 = Reserved **1 = Dothan (Default)**
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes **1 = Normal (Default)**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation (Default)**
CFG[15:14]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Reversed	
CFG18	GMCH core VCC Select	**0 = 1.05V (Default)** 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V (Default)** 1 = 1.2V
CFG20	Reversed	
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO device present(Default)** 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

ALVISO-GM:71.0GMCH.08U
ALVISO-PM:71.0GMCH.0BU
ALVISO-GML:71.0GMCH.0JU

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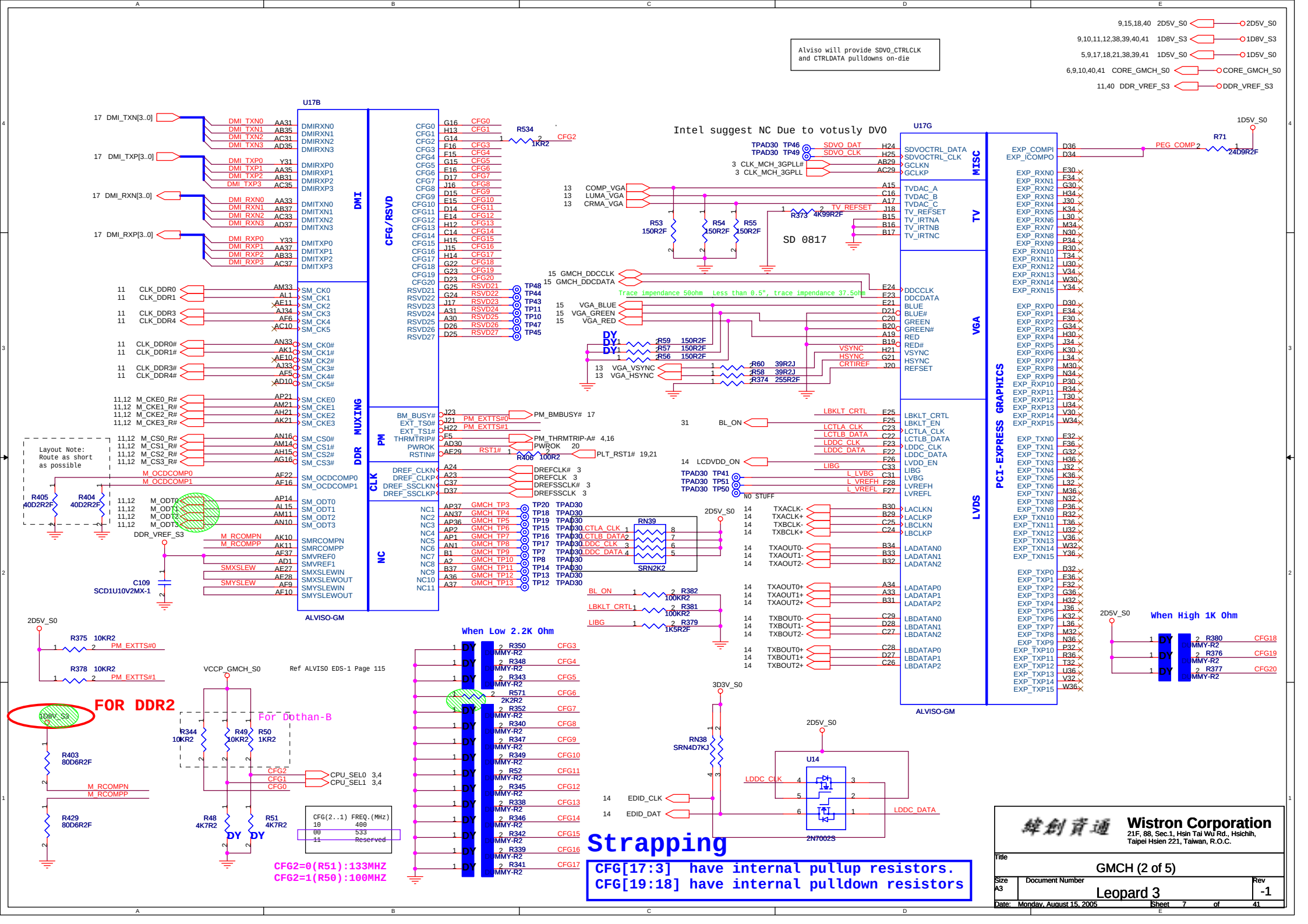
Title: GMCH (1 of 5)
Size: A3 | Document Number: Leopard 3 | Rev: -1
Date: Monday, August 15, 2005 | Sheet 6 of 41


Alviso will provide SDVO_CTRLCLK and CTRLDATA pulldowns on-die
Intel suggest NC Due to votusly DVO
U17B
U17G
DMI
CFG/RSVD
DDR MUXING
PM
CLK
NC
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
ALVISO-GM
SD 0817
Layout Note: Route as short as possible
Trace impendance 50ohm Less than 0.5", trace impendance 37.5ohm
FOR DDR2
For Dothan-B
Ref ALVISO EDS-1 Page 115
When Low 2.2K Ohm
When High 1K Ohm
CFG(2..1) FREQ.(MHz)
10 400
00 533
11 Reserved
CFG2=0(R51):133MHZ
CFG2=1(R50):100MHZ
Strapping
CFG[17:3] have internal pullup resistors.
CFG[19:18] have internal pulldown resistors
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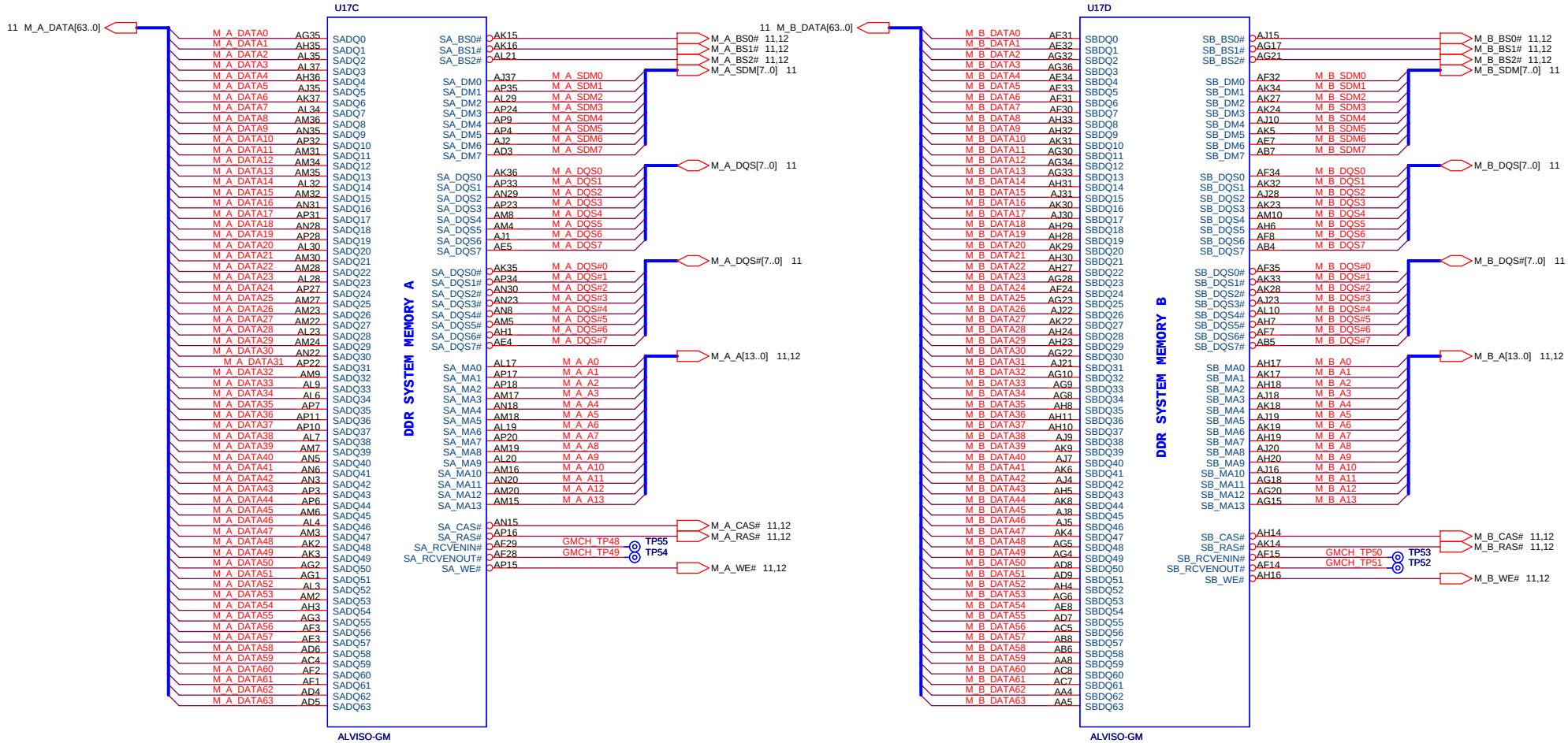
Title
GMCH (2 of 5)
Size A3
Document Number
Leopard 3
Rev -1
Date: Monday, August 15, 2005
Sheet 7 of 41



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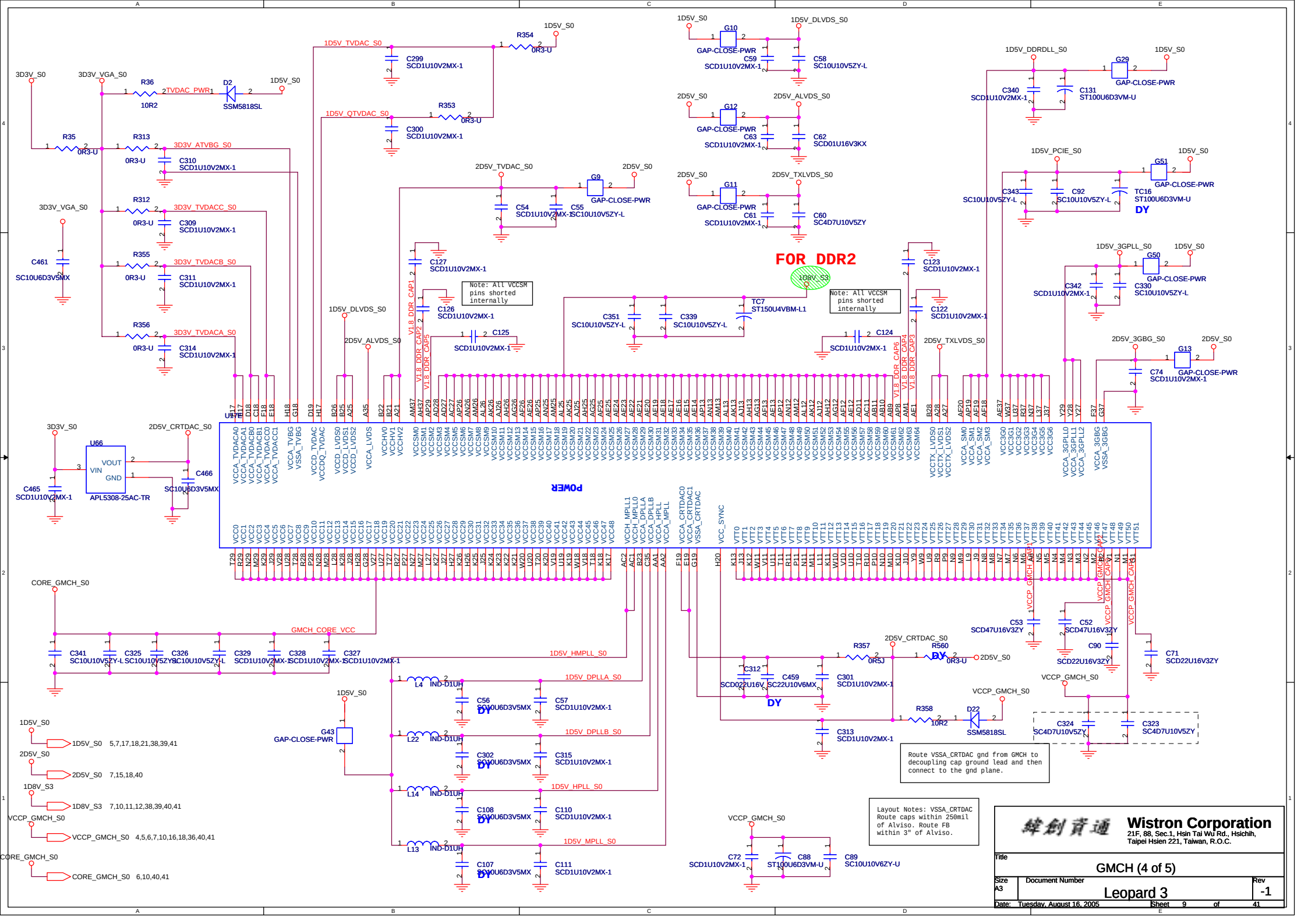
Title	GMCH (3 of 5)	
Size A3	Document Number Leopard 3	Rev -1
Date: Tuesday, July 12, 2005	Sheet 8 of 41	


FOR DDR2
POWER
Note: All VCCSM pins shorted internally
Note: All VCCSM pins shorted internally
Route VSSA_CRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.
Layout Notes: VSSA_CRTDAC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.
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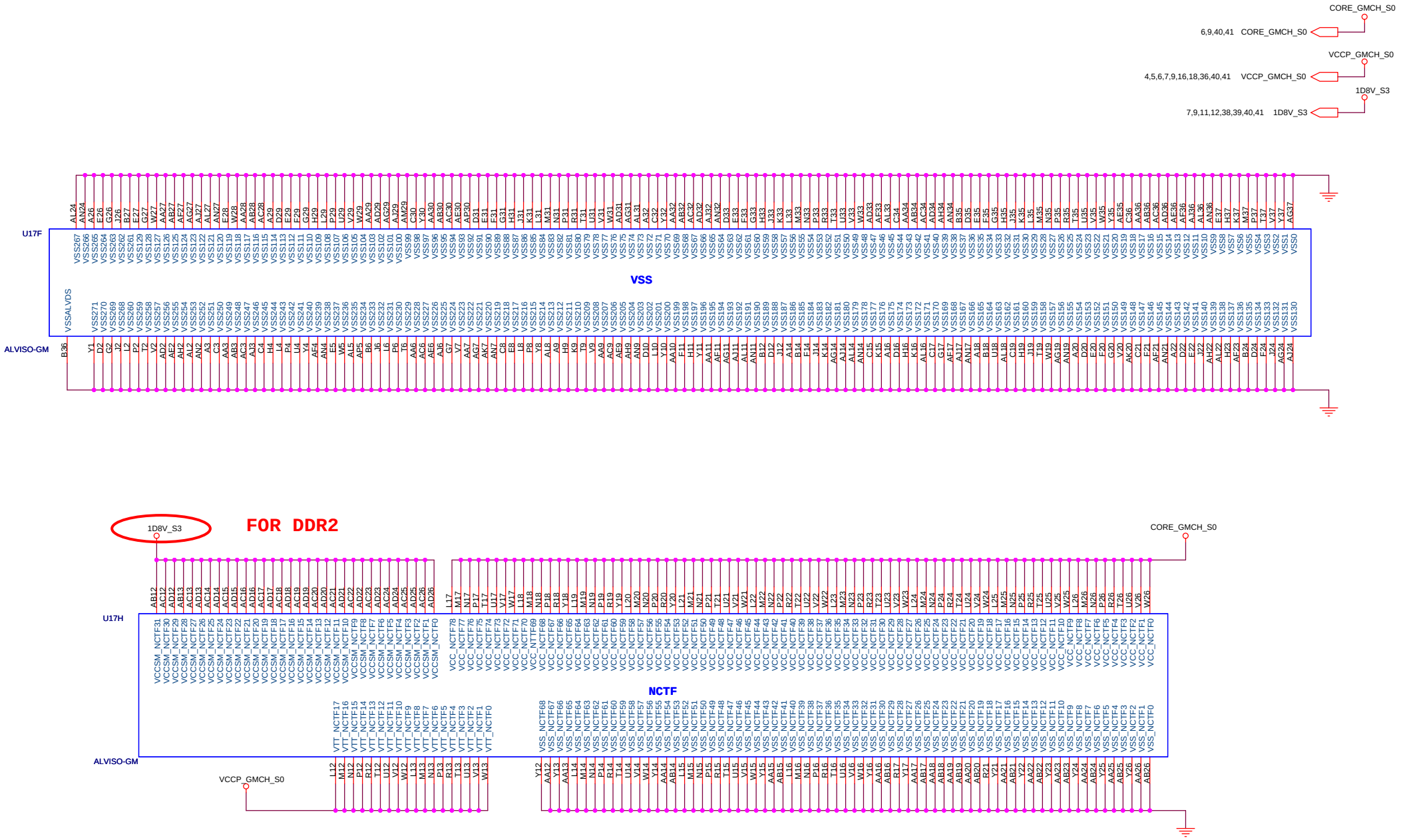
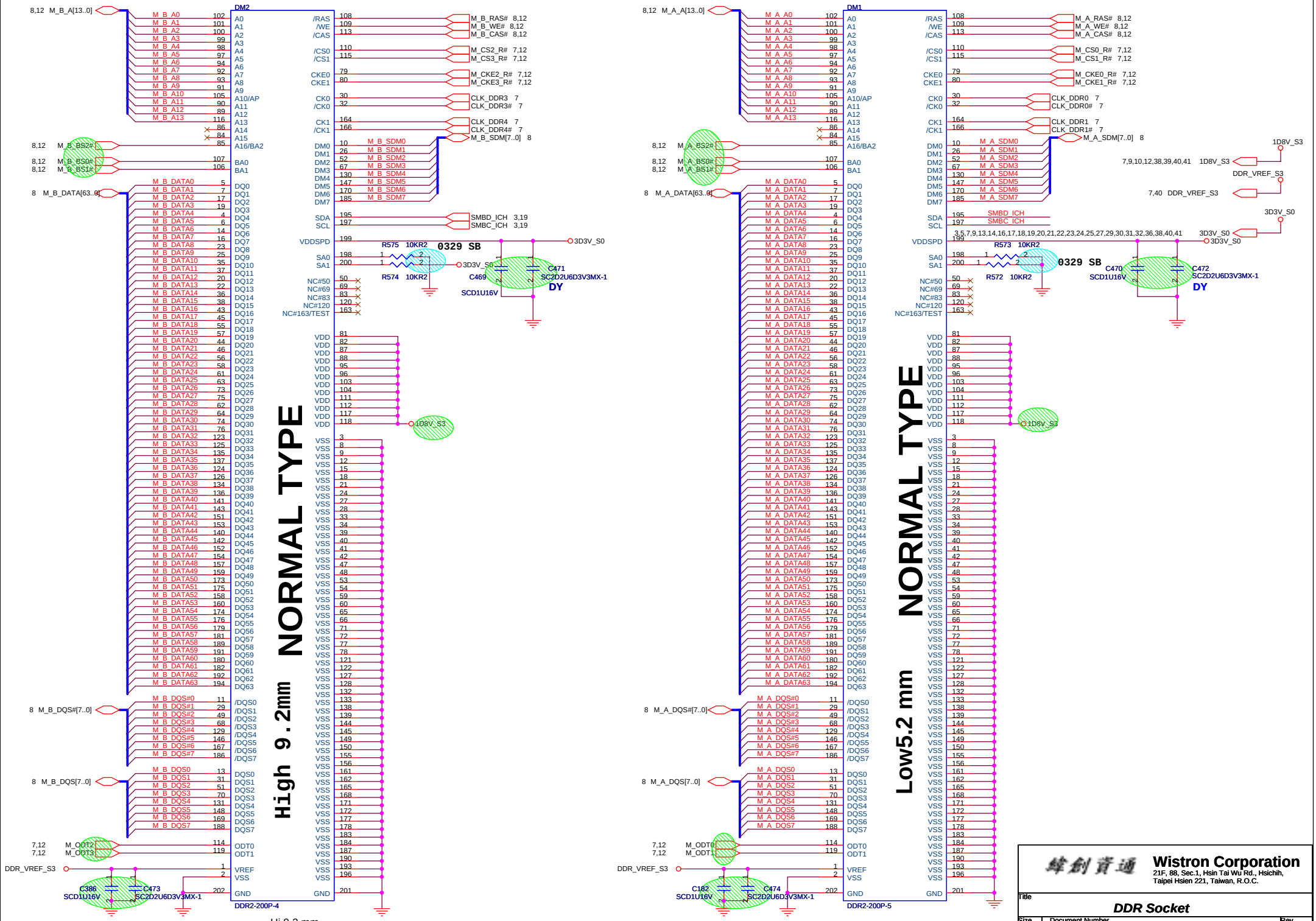
Title
GMCH (4 of 5)
Size A3
Document Number
Leopard 3
Rev -1
Date: Tuesday, August 16, 2005
Sheet 9 of 41



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	GMCH (5 of 5)	
Size A3	Document Number Leopard 3	Rev -1
Date: Tuesday, July 12, 2005	Sheet 10 of 41	



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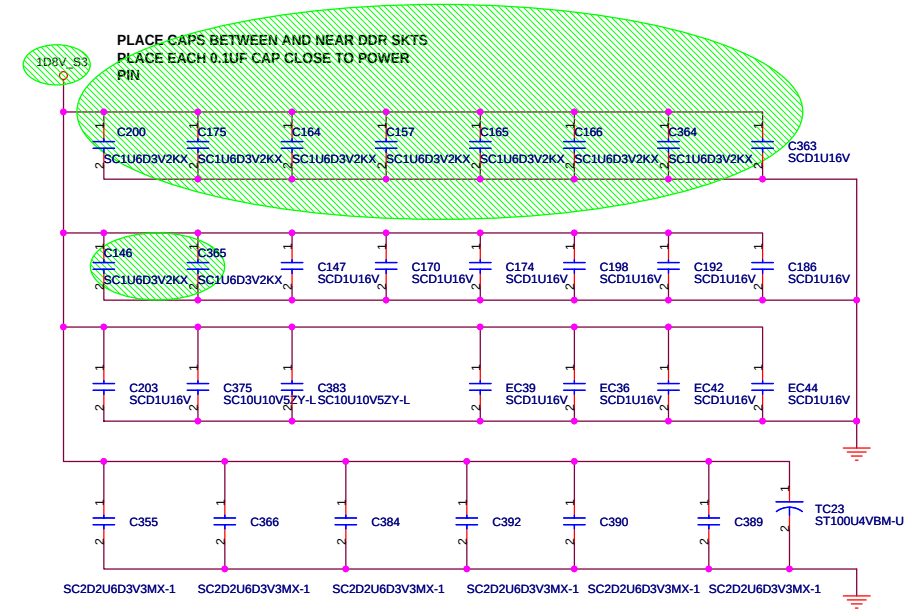
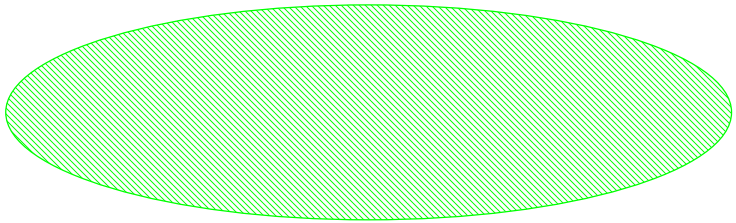
Title: DDR Socket

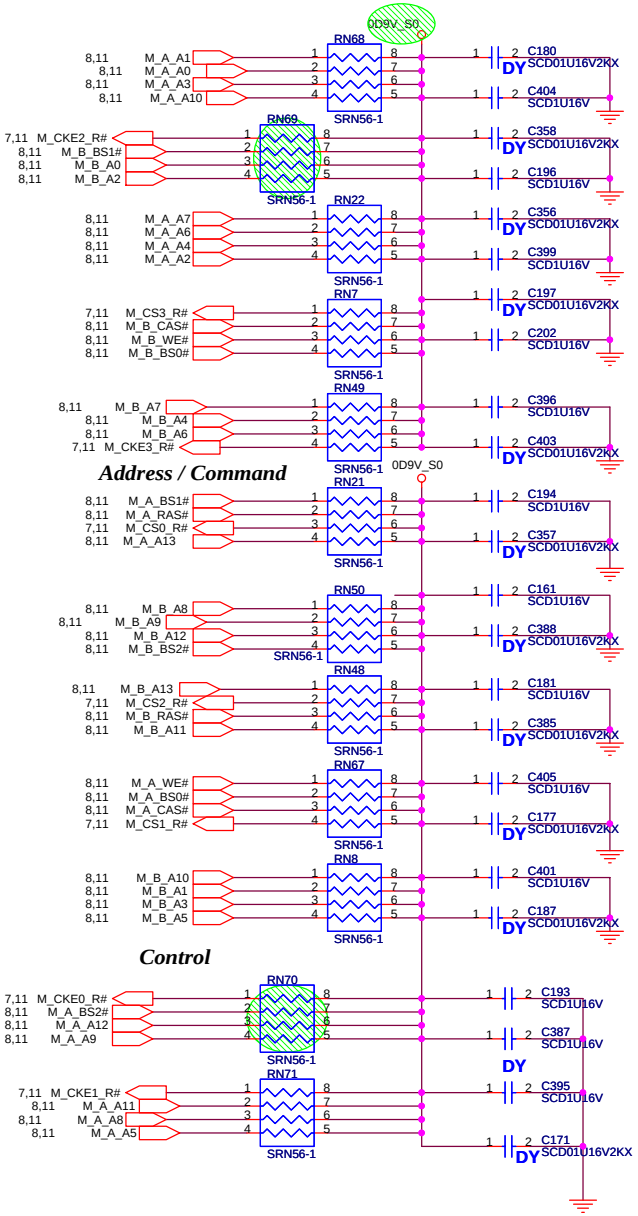
Size: Custom | Document Number: Leopard 3 | Rev: -1

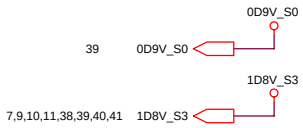
Date: Tuesday, August 16, 2005 | Sheet 11 of 41



For 1GB Memory







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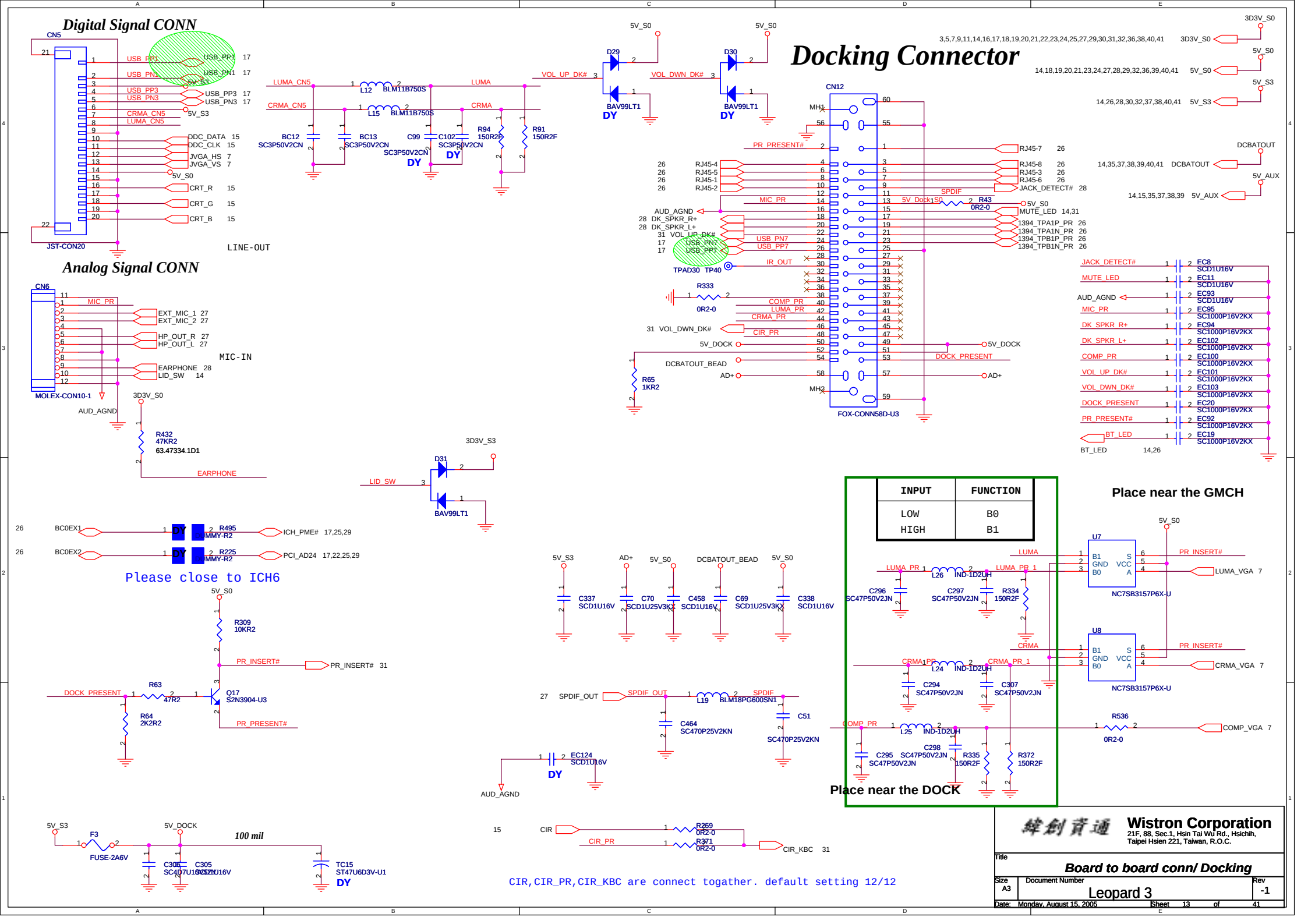
Title: ***DDR Serial/Terminator Resistor***

Size	Document Number	Rev
A3	Leopard 3	-1

Date: Thursday, August 18, 2005 Sheet 12 of 41


Digital Signal CONN
CN5
JST-CON20
USB_PP1 17
USB_PN1 17
USB_PP3 17
USB_PN3 17
CRMA_CN5
LUMA_CN5
5V_S3
DDC_DATA 15
DDC_CLK 15
JVGA_HS 7
JVGA_VS 7
5V_S0
CRT_R 15
CRT_G 15
CRT_B 15
LINE-OUT
Analog Signal CONN
CN6
MOLEX-CON10-1
MIC_PR
EXT_MIC_1 27
EXT_MIC_2 27
HP_OUT_R 27
HP_OUT_L 27
EARPHONE 28
LID_SW 14
MIC-IN
AUD_AGND
3D3V_S0
R432
47KR2
63.47334.1D1
EARPHONE
3D3V_S3
D31
LID_SW
BAV99LT1
26 BC0EX1
R495
DUMMY-R2
ICH_PME# 17,25,29
26 BC0EX2
R225
PCI_AD24 17,22,25,29
Please close to ICH6
5V_S0
R309
10KR2
PR_INSERT#
PR_INSERT# 31
DOCK_PRESENT
R63
47R2
Q17
S2N3904-U3
R64
2K2R2
PR_PRESENT#
5V_S3
F3
FUSE-2A6V
5V_DOCK
100 mil
C305
TC15
ST47U6D3V-U1
DY
LUMA_CN5
L12
BLM11B750S
LUMA
CRMA_CN5
L15
CRMA
BC12
SC3P50V2CN
BC13
C99
C102
R94
150R2F
R91
150R2F
VOL_UP_DK#
D29
BAV99LT1
VOL_DWN_DK#
D30
Docking Connector
CN12
FOX-CONN58D-U3
MH1
MH2
PR_PRESENT#
RJ45-4
RJ45-5
RJ45-1
RJ45-2
MIC_PR
AUD_AGND
DK_SPKR_R+
DK_SPKR_L+
VOL_UP_DK#
USB_PN7
USB_PP7
IR_OUT
TPAD30 TP40
R333
0R2-0
COMP_PR
LUMA_PR
CRMA_PR
CIR_PR
VOL_DWN_DK#
5V_DOCK
DCBATOUT_BEAD
AD+
R65
1KR2
RJ45-7 26
RJ45-8 26
RJ45-3 26
RJ45-6 26
JACK_DETECT# 28
SPDIF
5V_Dock1S0
R43
0R2-0
5V_S0
MUTE_LED 14,31
1394_TPA1P_PR 26
1394_TPA1N_PR 26
1394_TPB1P_PR 26
1394_TPB1N_PR 26
DOCK_PRESENT
3,5,7,9,11,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41
3D3V_S0
14,18,19,20,21,23,24,27,28,29,32,36,39,40,41
5V_S0
14,26,28,30,32,37,38,40,41
5V_S3
14,35,37,38,39,40,41
DCBATOUT
14,15,35,37,38,39
5V_AUX
JACK_DETECT#
MUTE_LED
AUD_AGND
MIC_PR
DK_SPKR_R+
DK_SPKR_L+
COMP_PR
VOL_UP_DK#
VOL_DWN_DK#
DOCK_PRESENT
PR_PRESENT#
BT_LED
EC8
SCD1U16V
EC11
SCD1U16V
EC93
SCD1U16V
EC95
SC1000P16V2KX
EC94
SC1000P16V2KX
EC102
SC1000P16V2KX
EC100
SC1000P16V2KX
EC101
SC1000P16V2KX
EC103
SC1000P16V2KX
EC20
SC1000P16V2KX
EC92
SC1000P16V2KX
EC19
SC1000P16V2KX
BT_LED 14,26
5V_S3
AD+
5V_S0
DCBATOUT_BEAD
C337
SCD1U16V
C70
SCD1U25V3KX
C458
SCD1U16V
C69
SCD1U25V3KX
C338
SCD1U16V
27 SPDIF_OUT
L19
BLM18PG600SN1
SPDIF
C464
SC470P25V2KN
C51
SC470P25V2KN
EC124
SCD1U16V
DY
AUD_AGND
15 CIR
R259
0R2-0
CIR_PR
R371
0R2-0
CIR_KBC 31
CIR,CIR_PR,CIR_KBC are connect togather. default setting 12/12
INPUT FUNCTION
LOW B0
HIGH B1
Place near the GMCH
U7
NC7SB3157P6X-U
U8
NC7SB3157P6X-U
LUMA
LUMA_PR
L26
IND-1D2UH
C296
SC47P50V2JN
C297
SC47P50V2JN
R334
150R2F
LUMA_VGA 7
CRMA
CRMA_PR
L24
C294
SC47P50V2JN
C307
SC47P50V2JN
CRMA_VGA 7
COMP_PR
L25
C298
SC47P50V2JN
C295
SC47P50V2JN
R335
150R2F
R372
150R2F
R536
0R2-0
COMP_VGA 7
Place near the DOCK
Wistron Corporation
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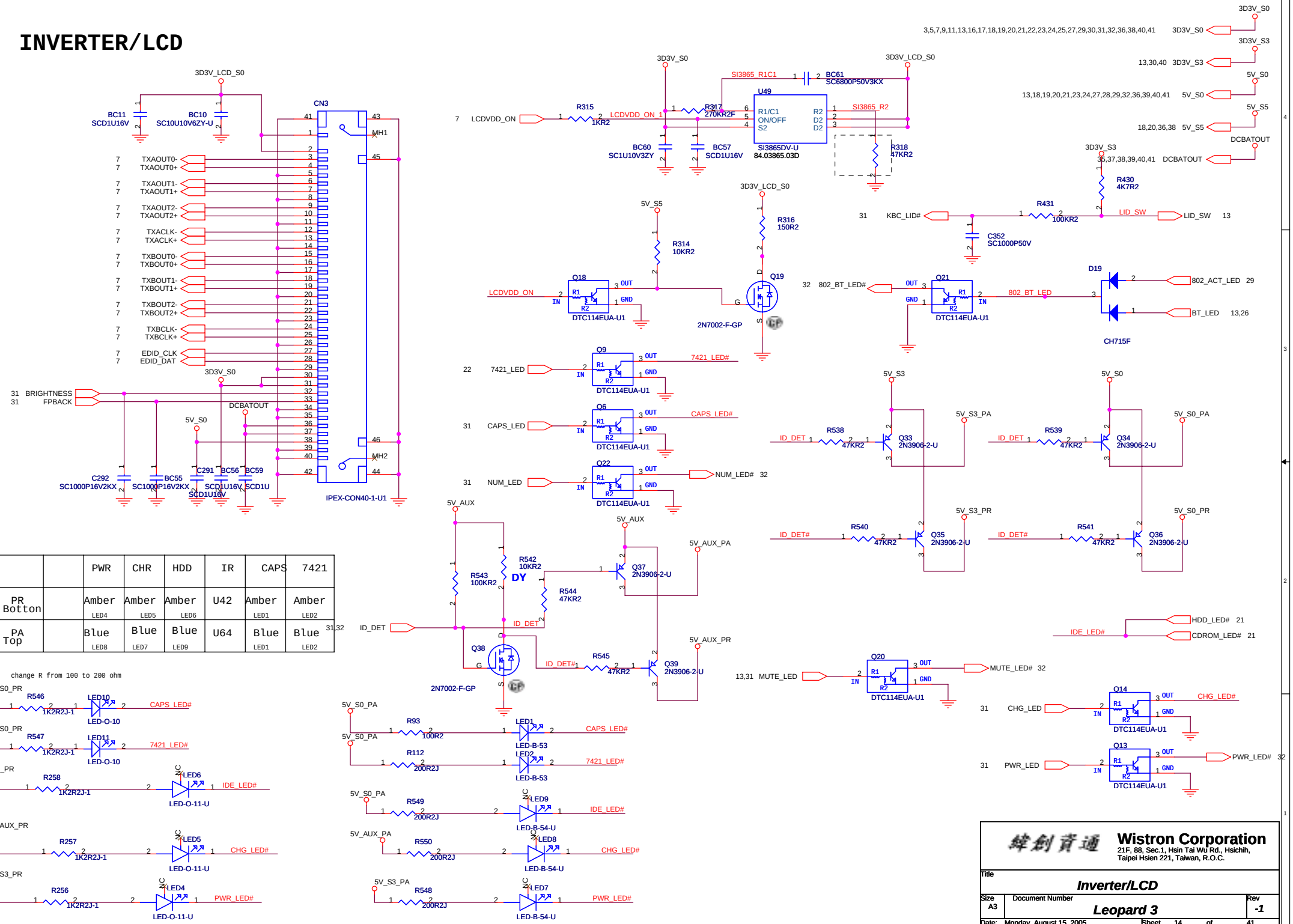
Taipei Hsien 221, Taiwan, R.O.C.
Title
Board to board conn/ Docking
Size A3
Document Number
Leopard 3
Rev -1
Date: Monday, August 15, 2005
Sheet 13 of 41

INVERTER/LCD



		PWR	CHR	HDD	IR	CAPS	7421
PR Botton		Amber LED4	Amber LED5	Amber LED6	U42	Amber LED1	Amber LED2
PA Top		Blue LED8	Blue LED7	Blue LED9	U64	Blue LED1	Blue LED2

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Title: Inverter/LCD

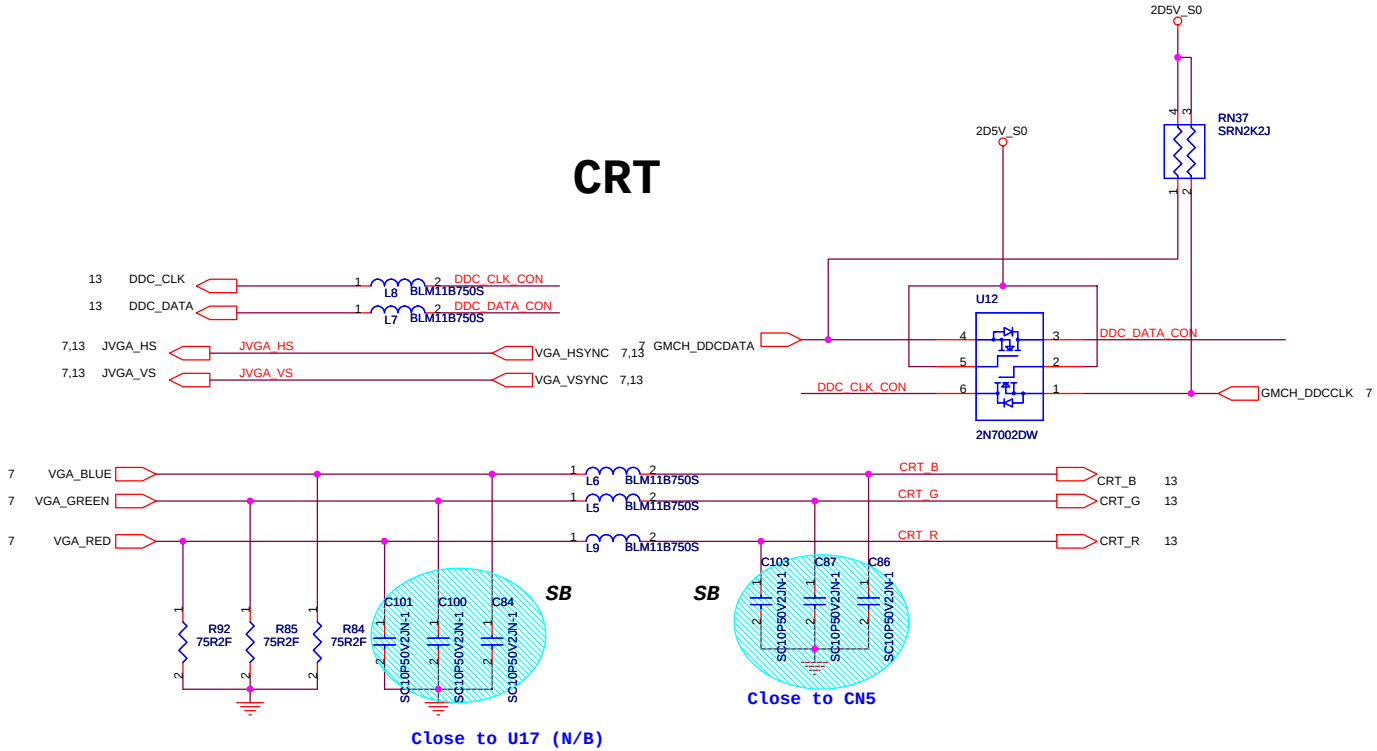
Size: A3 | Document Number: Leopard 3 | Rev: -1

Date: Monday, August 15, 2005 | Sheet 14 of 41

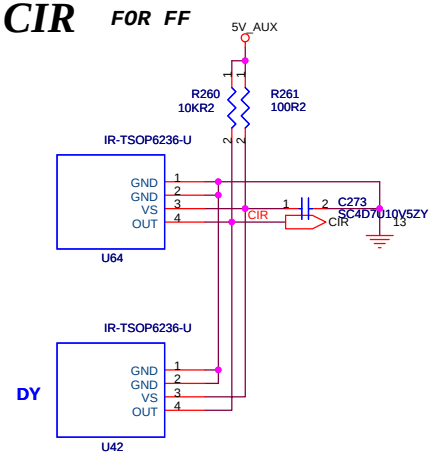
PA & PR diffent parts

	PA	PR
LED1	83.00190.Y70	83.00190.W70
LED2	83.00190.Y70	83.00190.W70
LED4	Dummy	83.00110.D70
LED5	Dummy	83.00110.D70
LED6	Dummy	83.00110.D70
LED7	83.00110.E70	Dummy
LED8	83.00110.E70	Dummy
LED9	83.00110.E70	Dummy
U64	56.15006.001	Dummy
U42	Dummy	56.15006.001
R256	63.20134.1D1	63.12234.1D1
R257	63.20134.1D1	63.12234.1D1
R258	63.20134.1D1	63.12234.1D1
R93	63.20134.1D1	63.12234.1D1
R112	63.20134.1D1	63.12234.1D1
CBUS1	21.H0088.001	21.H0088.001
R176	63.10334.1D1	Dummy
R177	Dummy	63.10334.1D1

CRT



CIR FOR FF



Wistron Corporation
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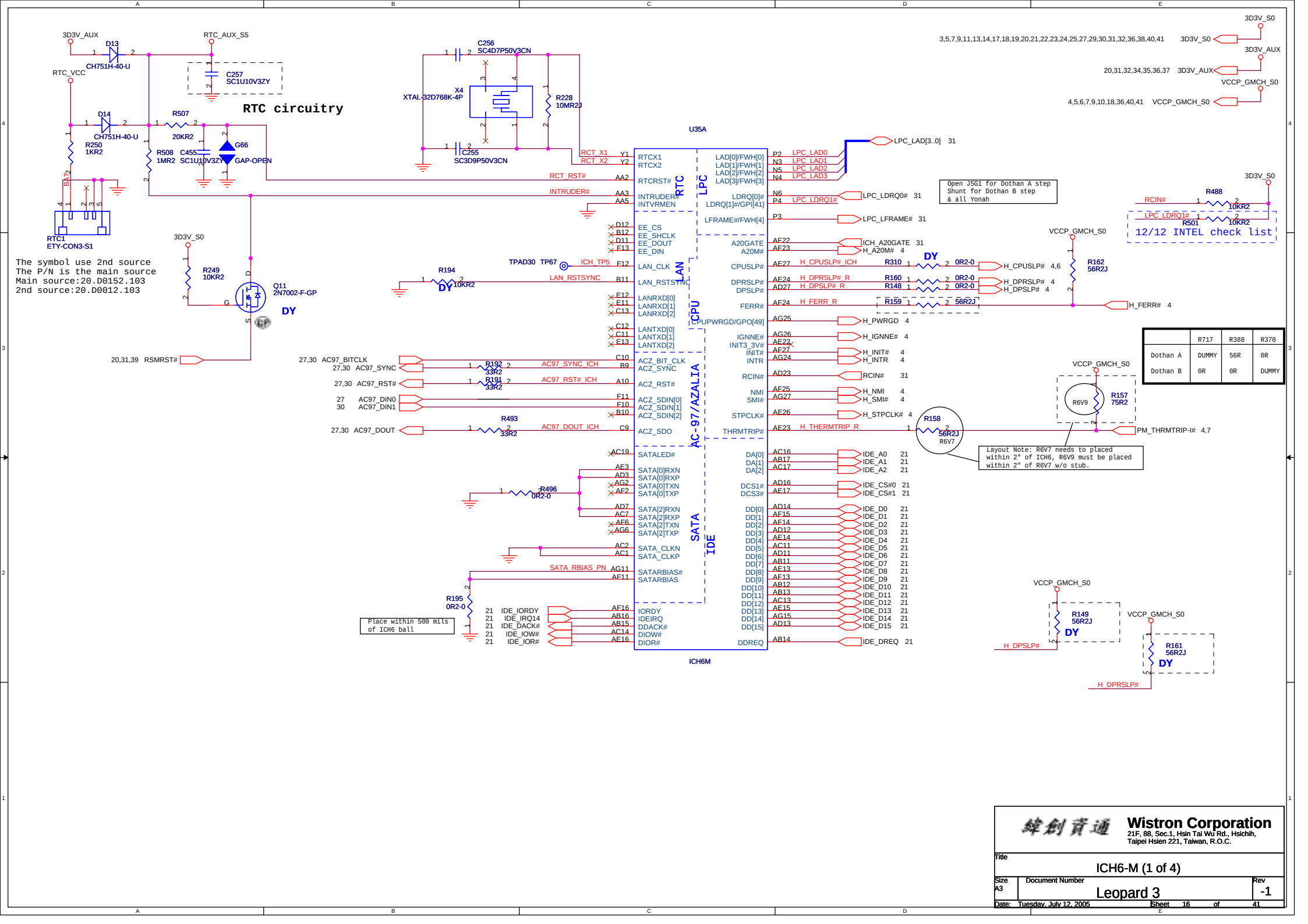
Taipei Hsien 221, Taiwan, R.O.C.

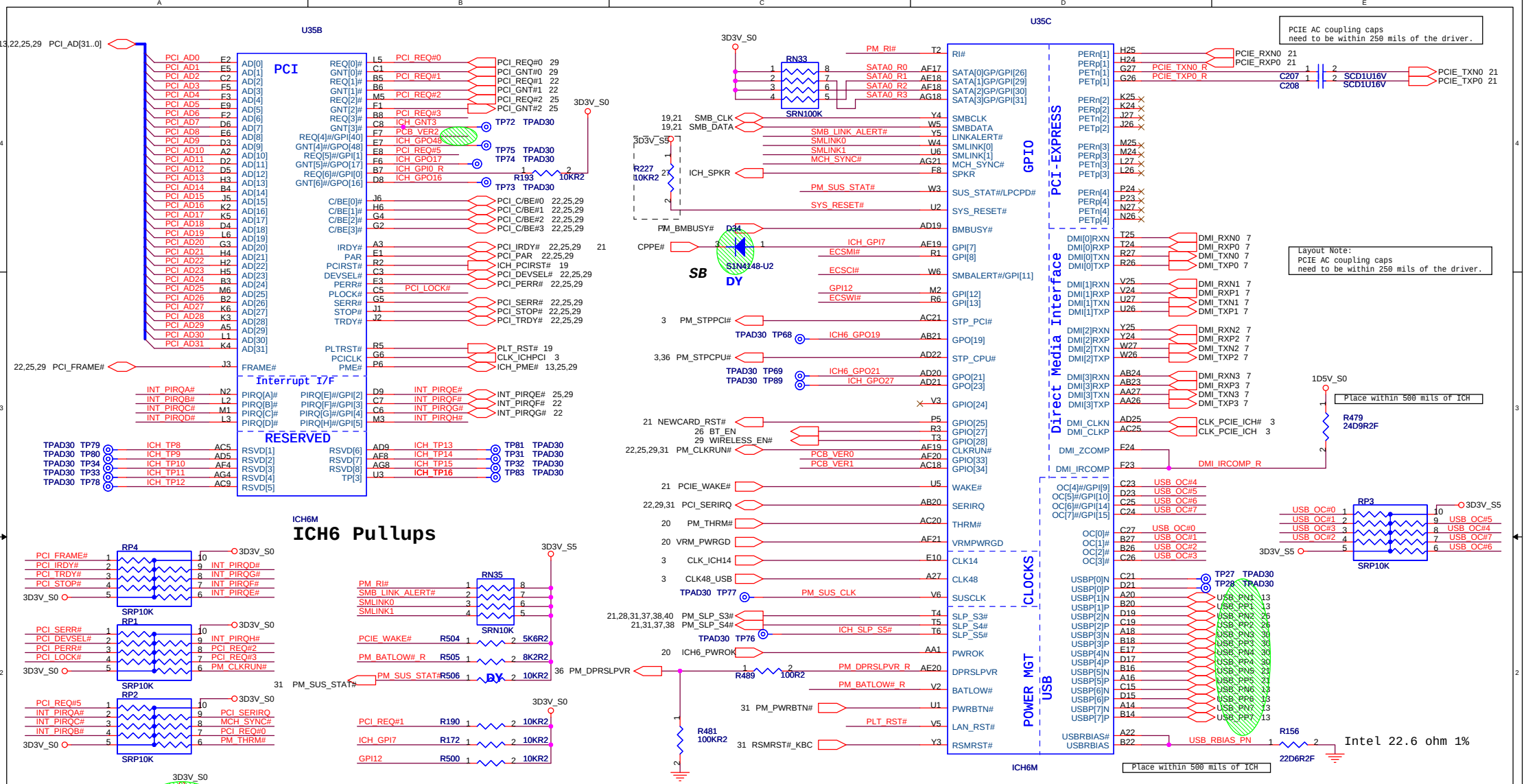
Title: CRT/ CIR

Size: A3 | Document Number: Leopard 3 | Rev: -1

Date: Monday, August 15, 2005 | Sheet 15 of 41



	R717	R388	R370
Dothan A	DUMMY	56R	0R
Dothan B	0R	0R	DUMMY



PUMA Board Version Setting

Ver.	PCB_VER0	PCB_VER1	PCB_VER2
SA	0	0	0
SB	0	1	0
SC	1	0	0
-1	1	1	0
-2	0	0	1

ICH6-M Strapping Options

REF	FUNCTION	DEFAULT	OPTIONAL OVERRIDE
R7F9	No Reboot	NO_STUFF	STUFF
R7F8	A16 Swap Override	NO_STUFF	STUFF
R7F7	Boot BIOS	NO_STUFF	STUFF

1D5V_S0 — 1D5V_S0 5,7,9,18,21,38,39,41
3D3V_S5 — 3D3V_S5 18,19,21,25,29,31,35,37,39,40
3D3V_S0 — 3D3V_S0 3,5,7,9,11,13,14,16,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41

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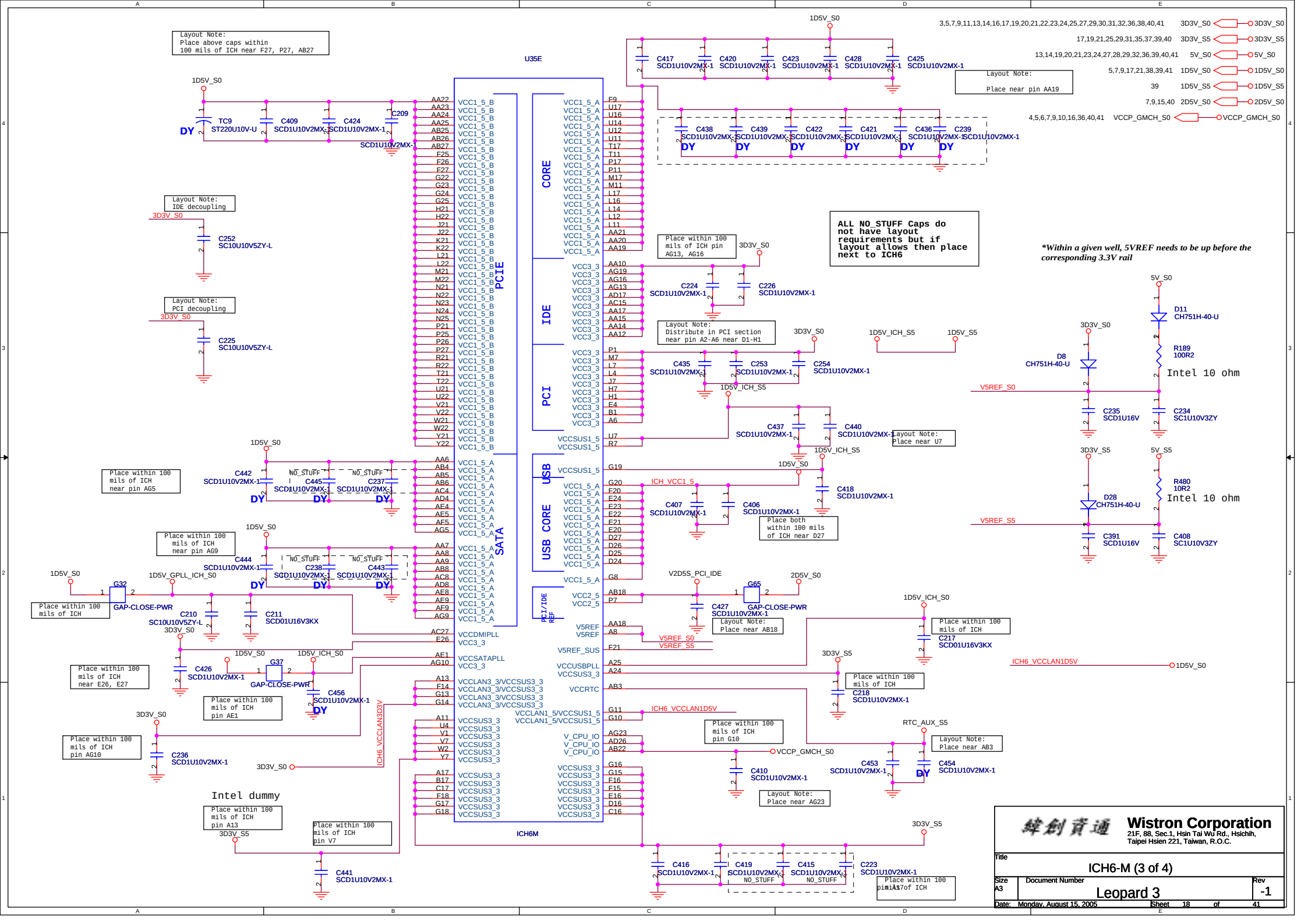
Title: ICH6-M (2 of 4)
Size: A3 | Document Number: Leopard 3 | Rev: -1
Date: Monday, August 15, 2005 | Sheet 17 of 41


U35E
ICH6M
PCIE
IDE
PCI
CORE
USB
USB CORE
SATA
PCI/IDE REF
Layout Note: Place above caps within 100 mils of ICH near F27, P27, AB27
Layout Note: IDE decoupling
Layout Note: PCI decoupling
Place within 100 mils of ICH pin AG13, AG16
Layout Note: Distribute in PCI section near pin A2-A6 near D1-H1
Place within 100 mils of ICH near pin AG5
Place within 100 mils of ICH near pin AG9
Place within 100 mils of ICH
Place within 100 mils of ICH near E26, E27
Place within 100 mils of ICH pin AE1
Place within 100 mils of ICH pin AG10
Place within 100 mils of ICH pin A13
Place within 100 mils of ICH pin V7
Place within 100 mils of ICH pin G10
Place within 100 mils of ICH pin A17
Layout Note: Place near U7
Place both within 100 mils of ICH near D27
Layout Note: Place near AB18
Layout Note: Place near AB3
Layout Note: Place near AG23
Layout Note: Place near pin AA19
ALL NO_STUFF Caps do not have layout requirements but if layout allows then place next to ICH6
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Intel 10 ohm
Intel 10 ohm
Intel dummy
1D5V_S0
3D3V_S0
3D3V_S5
5V_S0
5V_S5
1D5V_ICH_S5
1D5V_S5
1D5V_ICH_S0
1D5V_GPLL_ICH_S0
V2D5S_PCI_IDE
2D5V_S0
RTC_AUX_S5
VCCP_GMCH_S0
ICH_VCC1_5
ICH6_VCCLAN1D5V
V5REF_S0
V5REF_S5
ICH6_VCCLAN3D3V
GAP-CLOSE-PWR
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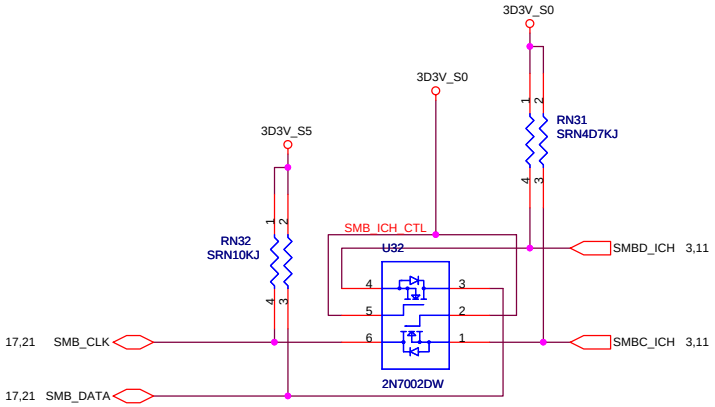
Title
ICH6-M (3 of 4)
Size A3
Document Number
Leopard 3
Rev -1
Date: Monday, August 15, 2005
Sheet 18 of 41

SMBUS(ICH6 ---> SODIMM,CLKGEN)



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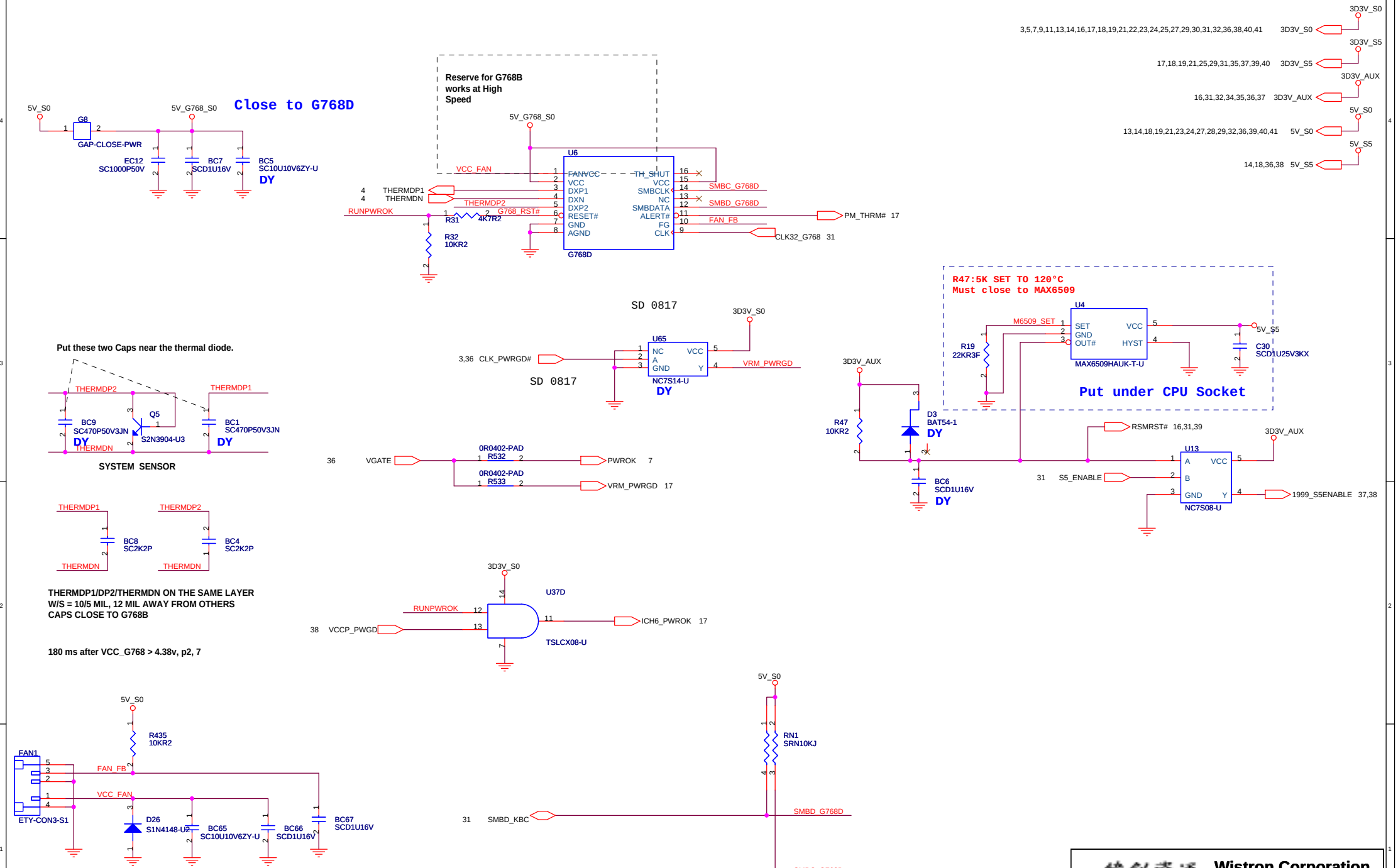
Title	ICH6-M (4 of 4)	
Size A3	Document Number Leopard 3	Rev -1
Date: Monday, August 15, 2005	Sheet 19 of 41	



The symbol use 2nd source
The P/N is the main source
Main source:20.D0152.103
2nd source:20.D0012.103

Wistron Corporation
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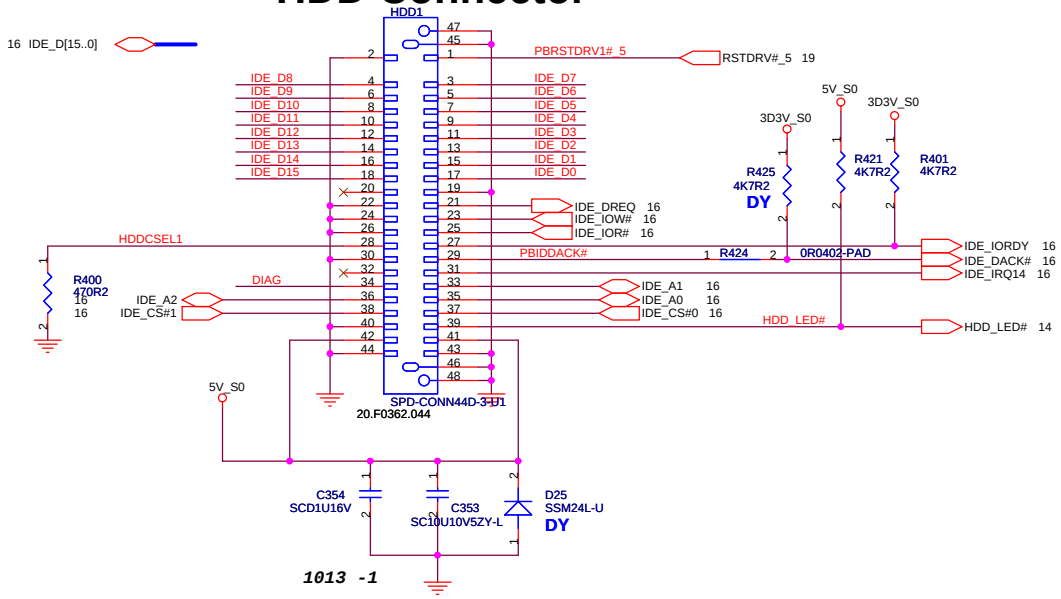
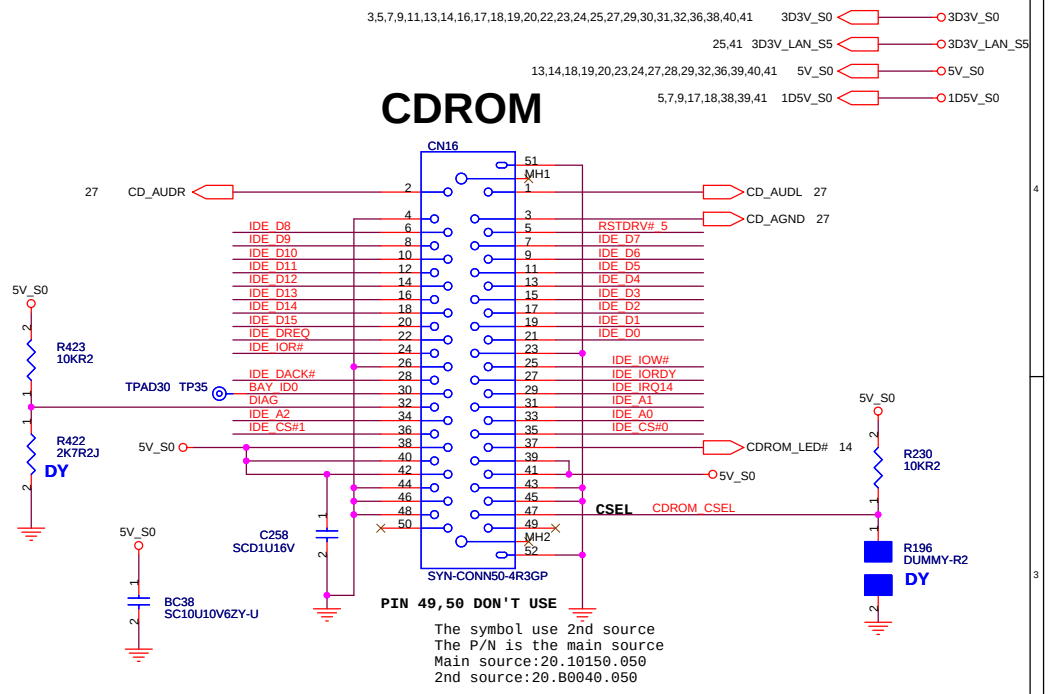
Title	G768D	
Size A3	Document Number Leopard 3	Rev -1
Date: Monday, August 15, 2005	Sheet 20 of 41	

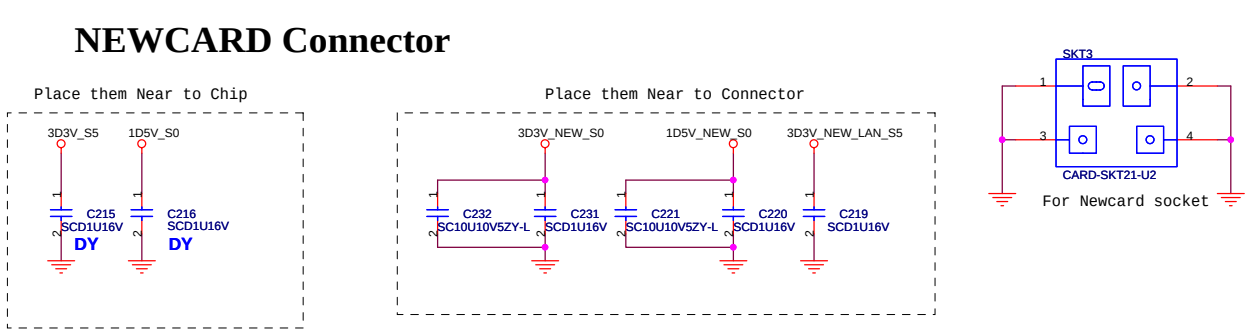
HDD Connector

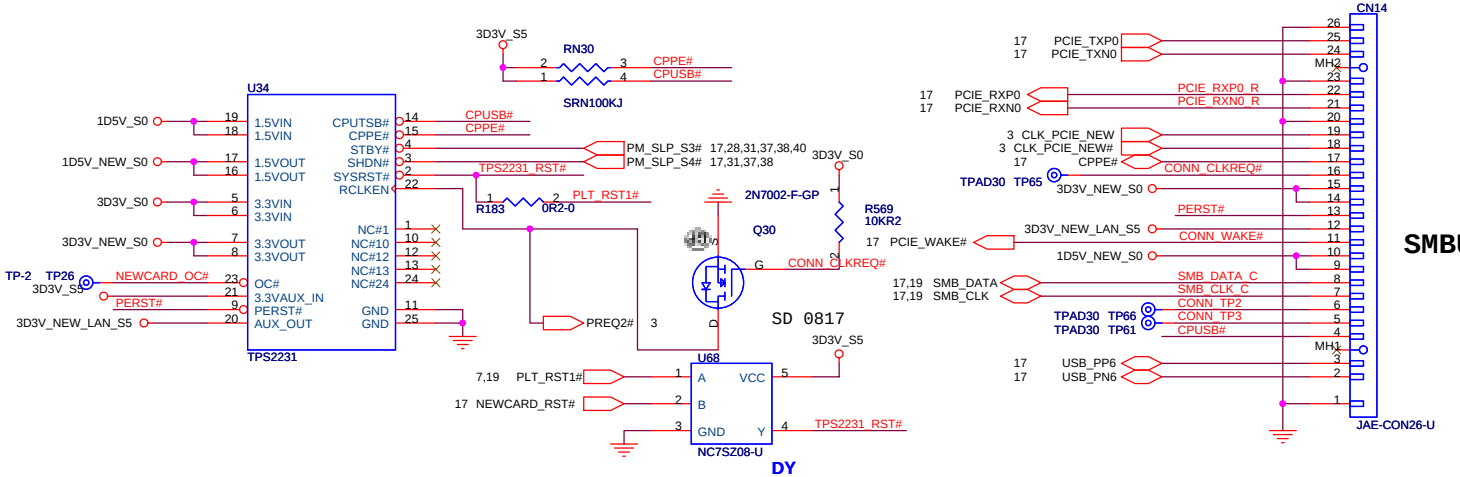


CDROM



NEWCARD Connector





SMBUS(ICH6--NEWCARD,LAN)

Wistron Corporation
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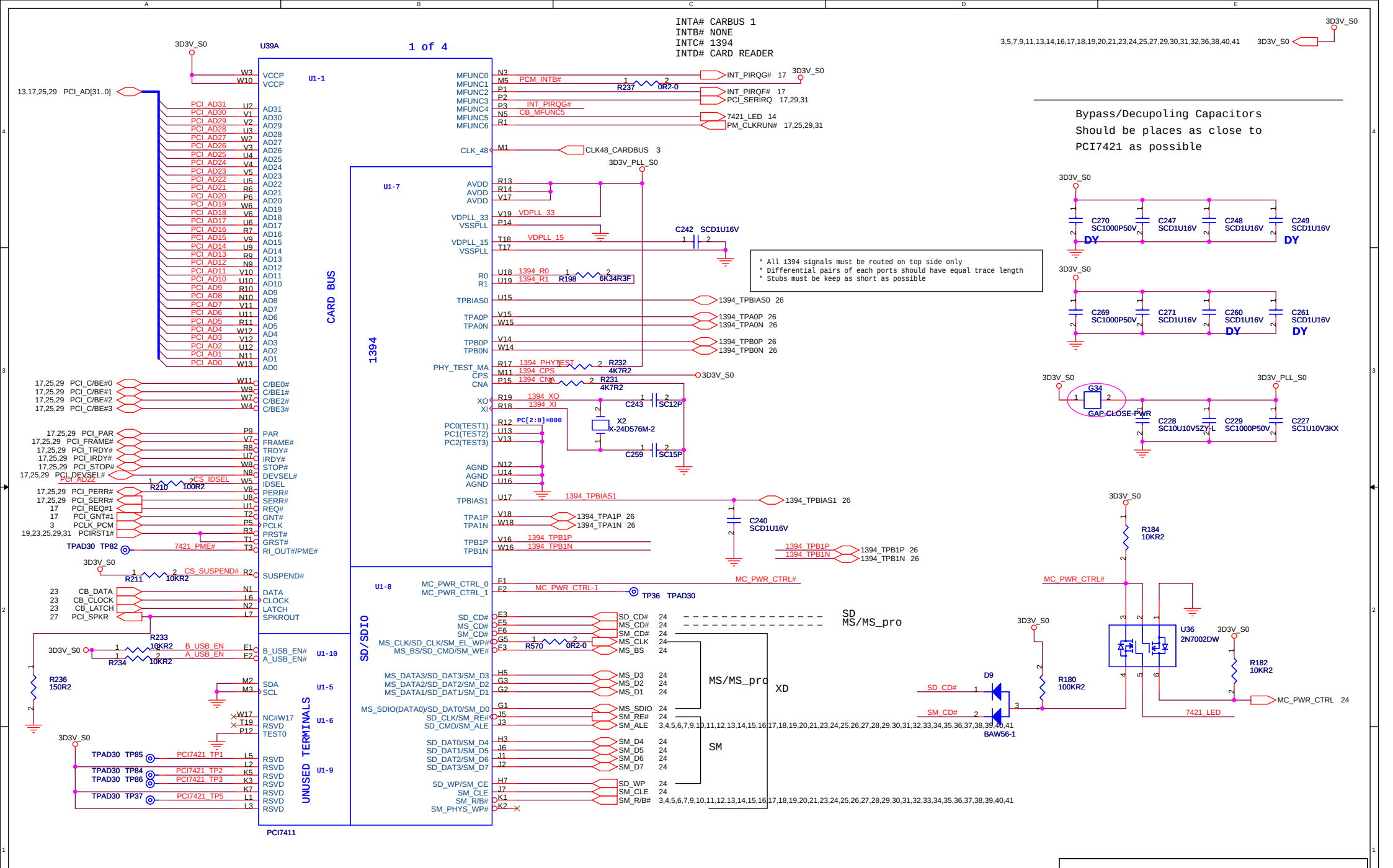
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD / CDROM/NEWCARD

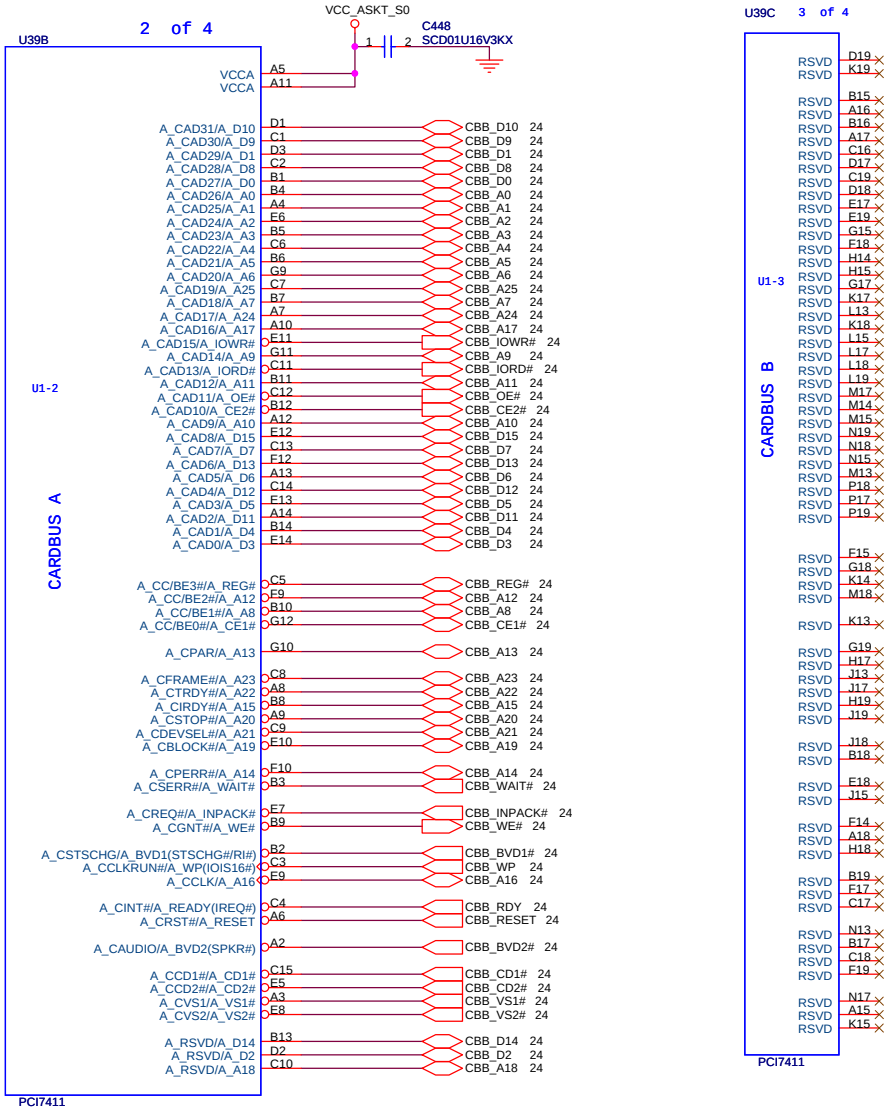
Size	Document Number	Rev
A3	Leopard 3	-1

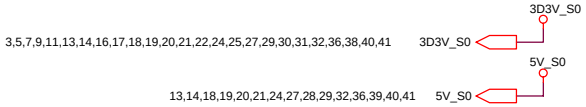
Date: Tuesday, July 12, 2005 Sheet 21 of 41



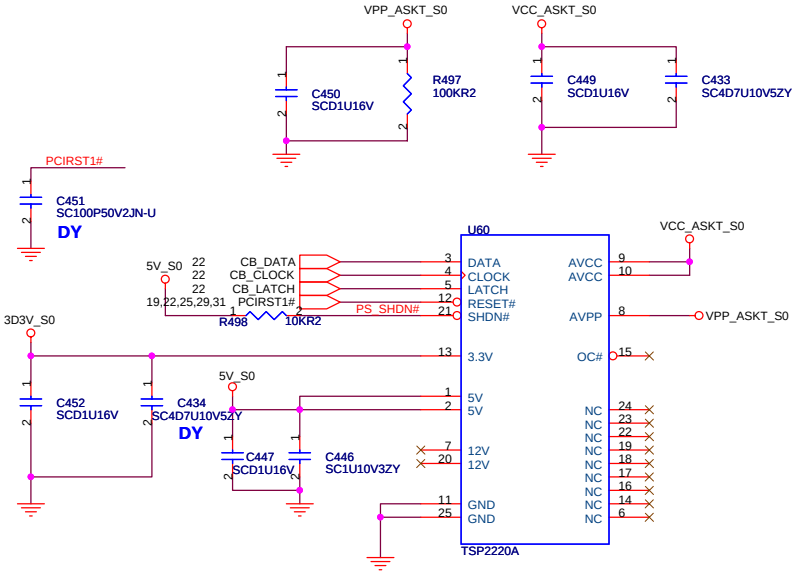
7411:71.07411.00U
7421:71.07421.00U

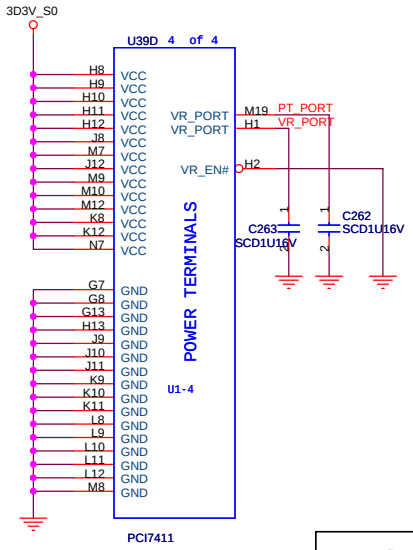
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	TI SNC1Q21 (1 of 2)	
Size A3	Document Number Leopard 3	Rev -1
Date: Monday, August 15, 2005	Sheet 22 of 41	





Power switch





緯創資通 Wistron Corporation
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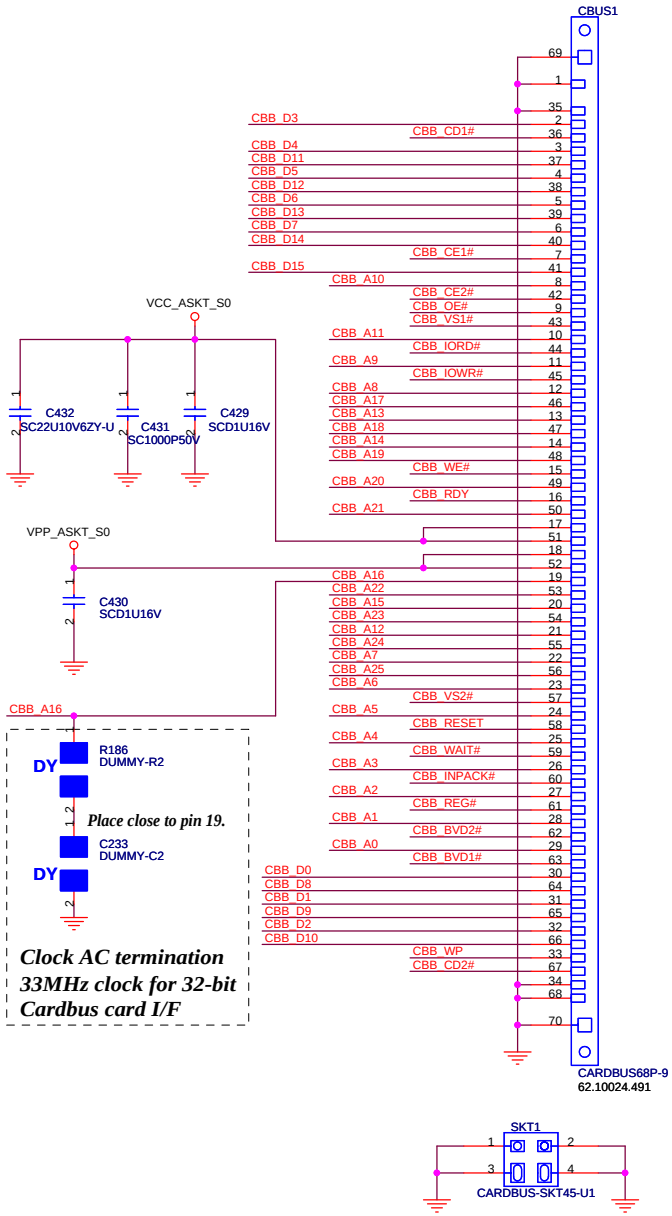
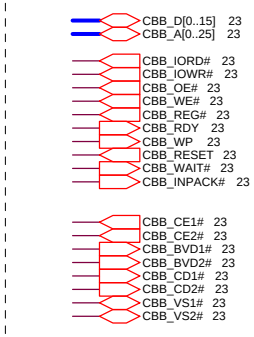
Taipei Hsien 221, Taiwan, R.O.C.

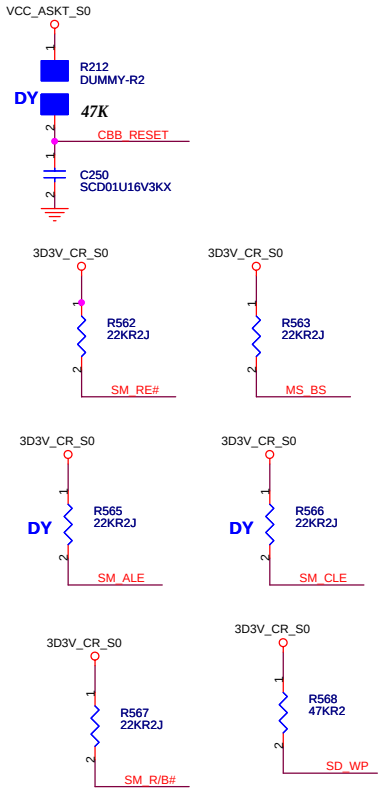
Title	TI PCI7411 GHK (2 of 2)	
Size A3	Document Number Leopard 3	Rev -1
Date: Tuesday, July 12, 2005	Sheet 23 of 41	

PCMCIA Socket

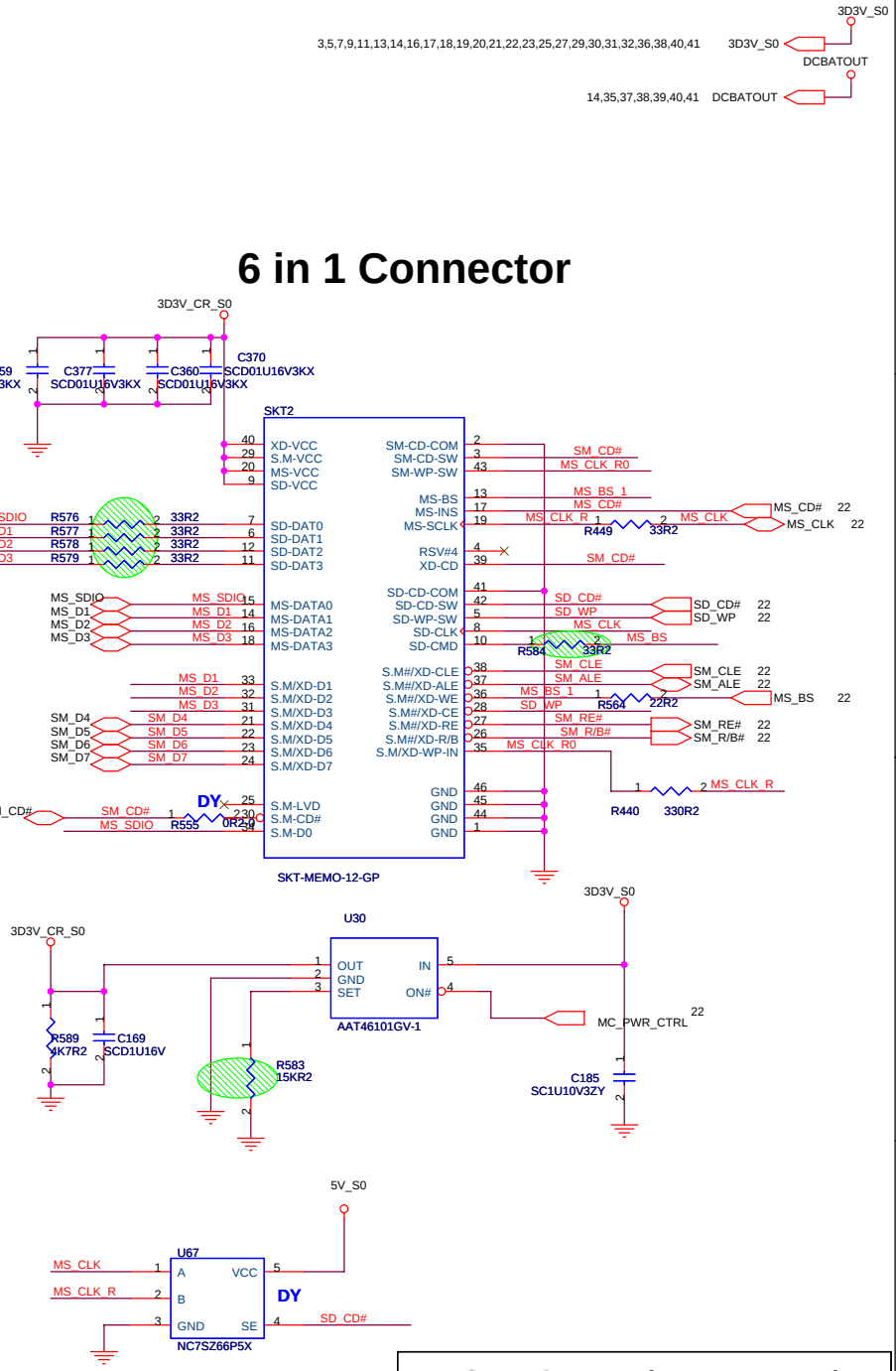


Cardbus I/F





6 in 1 Connector



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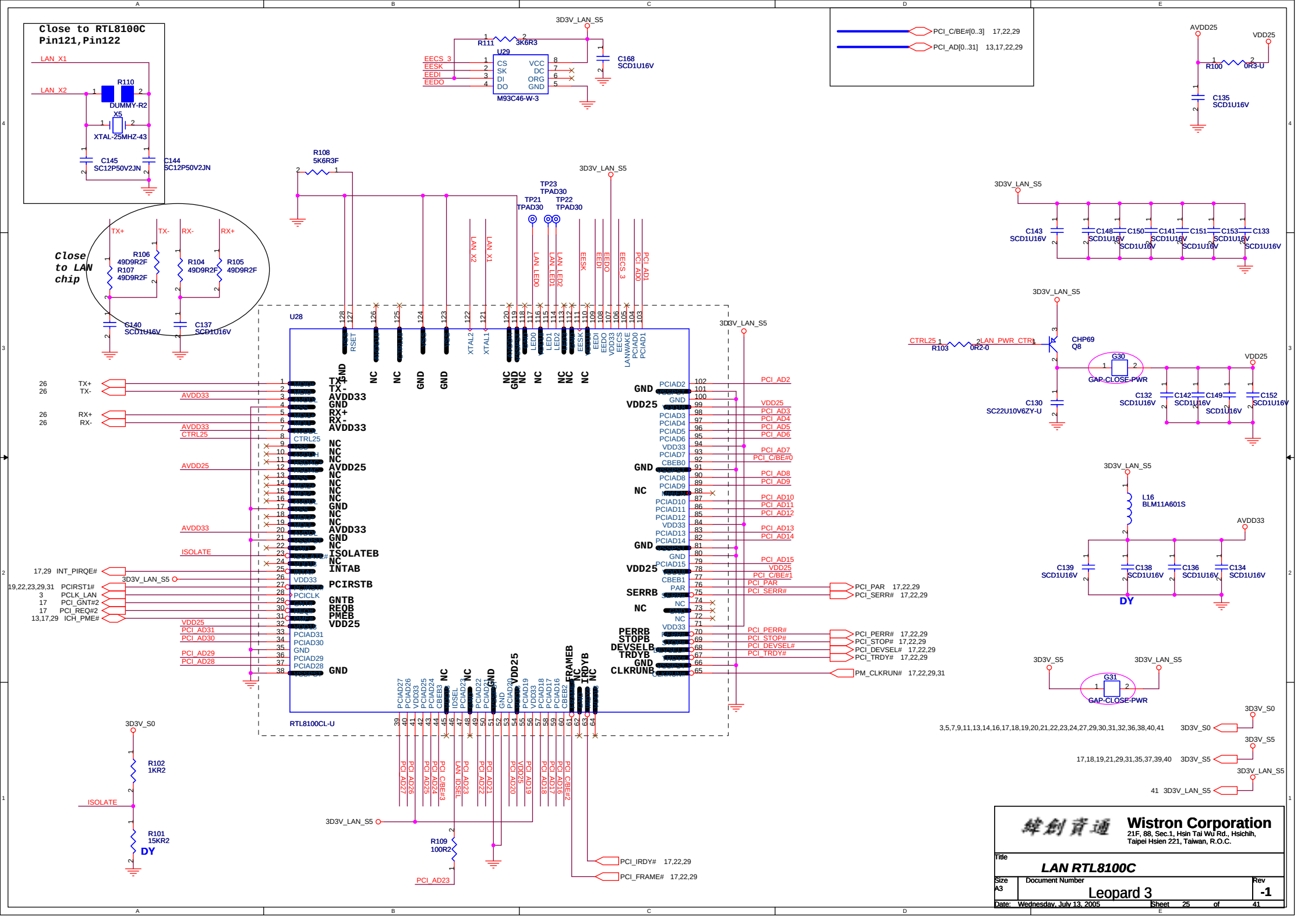
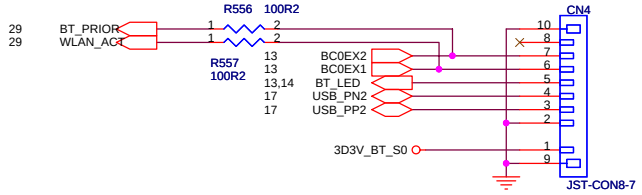
Title	PCMCIA SLOT/ CARDBUS SKT	
Size A3	Document Number Leopard 3	Rev -1
Date: Tuesday, July 12, 2005	Sheet 24 of 41	


Close to RTL8100C Pin121,Pin122
LAN_X1
LAN_X2
R110
DUMMY-R2
X5
XTAL-25MHZ-43
C145 SC12P50V2JN
C144 SC12P50V2JN
Close to LAN chip
TX+
TX-
RX-
RX+
R106 49D9R2F
R107 49D9R2F
R104 49D9R2F
R105 49D9R2F
C140 SCD1U16V
C137 SCD1U16V
R108 5K6R3F
3D3V_LAN_S5
R111 3K6R3
U29
M93C46-W-3
EECS_3
EESK
EEDI
EEDO
C168 SCD1U16V
TP23 TPAD30
TP21 TPAD30
TP22 TPAD30
U28
RTL8100CL-U
PCI_C/BE#[0..3] 17,22,29
PCI_AD[0..31] 13,17,22,29
AVDD25
VDD25
R100 0R3-U
C135 SCD1U16V
C143 SCD1U16V
C148 SCD1U16V
C150 SCD1U16V
C141 SCD1U16V
C151 SCD1U16V
C153 SCD1U16V
C133 SCD1U16V
CTRL25
R103 0R2-0
LAN_PWR_CTRL
CHP69
Q8
G30
GAP-CLOSE-PWR
C130 SC22U10V6ZY-U
C132 SCD1U16V
C142 SCD1U16V
C149 SCD1U16V
C152 SCD1U16V
L16 BLM11A601S
AVDD33
C139 SCD1U16V
C138 SCD1U16V
C136 SCD1U16V
C134 SCD1U16V
DY
3D3V_S5
G31
GAP-CLOSE-PWR
3D3V_S0
R102 1KR2
ISOLATE
R101 15KR2
DY
R109 100R2
PCI_AD23
PCI_IRDY# 17,22,29
PCI_FRAME# 17,22,29
PCI_PAR 17,22,29
PCI_SERR# 17,22,29
PCI_PERR# 17,22,29
PCI_STOP# 17,22,29
PCI_DEVSEL# 17,22,29
PCI_TRDY# 17,22,29
PM_CLKRUN# 17,22,29,31
17,29 INT_PIRQE#
19,22,23,29,31 PCIRST1#
3 PCLK_LAN
17 PCI_GNT#2
17 PCI_REQ#2
13,17,29 ICH_PME#
3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,27,29,30,31,32,36,38,40,41 3D3V_S0
17,18,19,21,29,31,35,37,39,40 3D3V_S5
41 3D3V_LAN_S5
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
LAN RTL8100C
Size A3
Document Number
Leopard 3
Rev -1
Date: Wednesday, July 13, 2005
Sheet 25 of 41

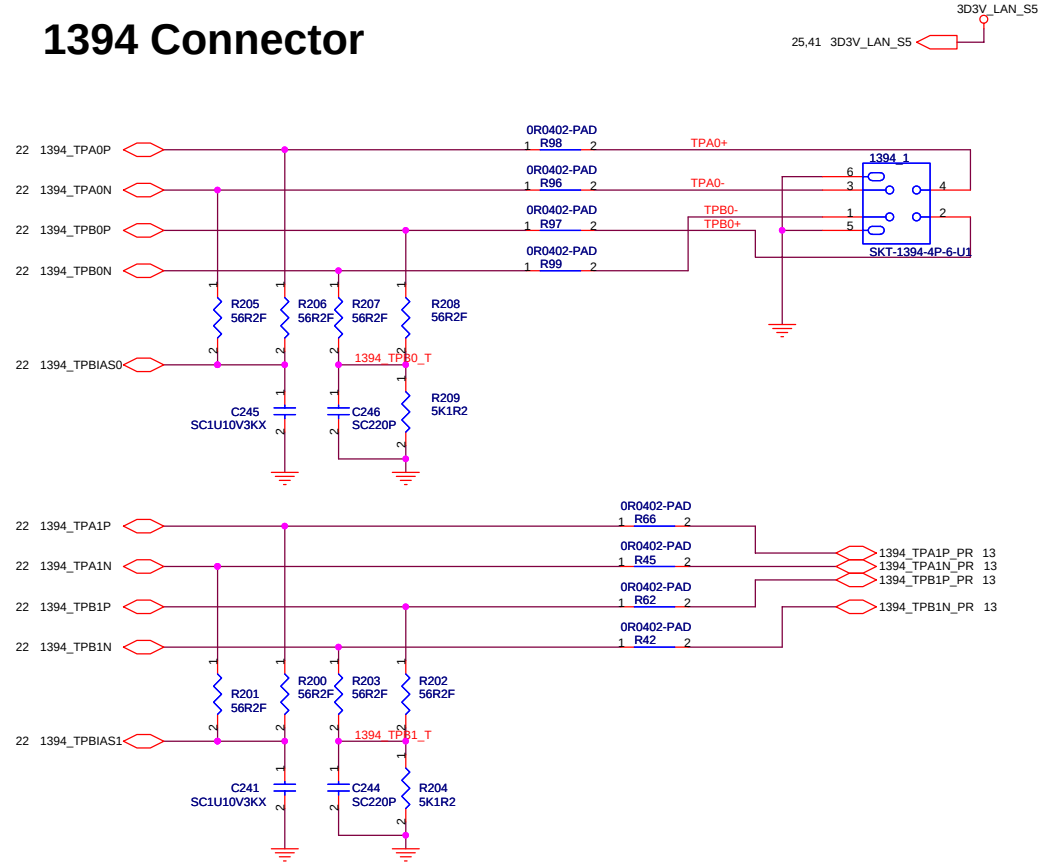
Blue thumb

Place on bottom side



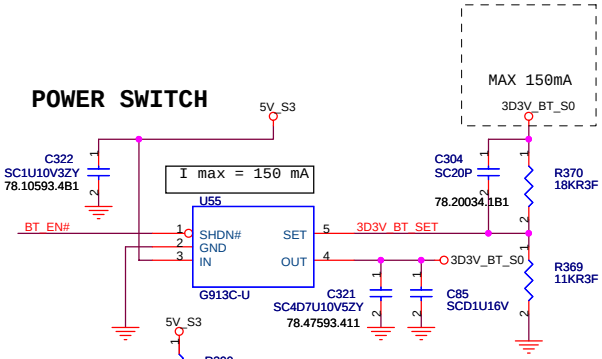
BC0EX2 connect to PCI_AD22 on main board.
BC0EX1 connect to ICH_PME# on main board.

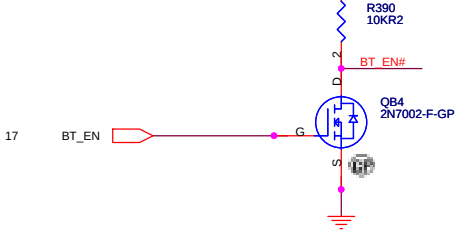
1394 Connector

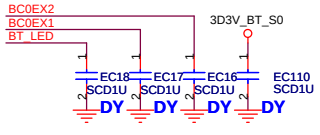


These components near to chip side.

POWER SWITCH



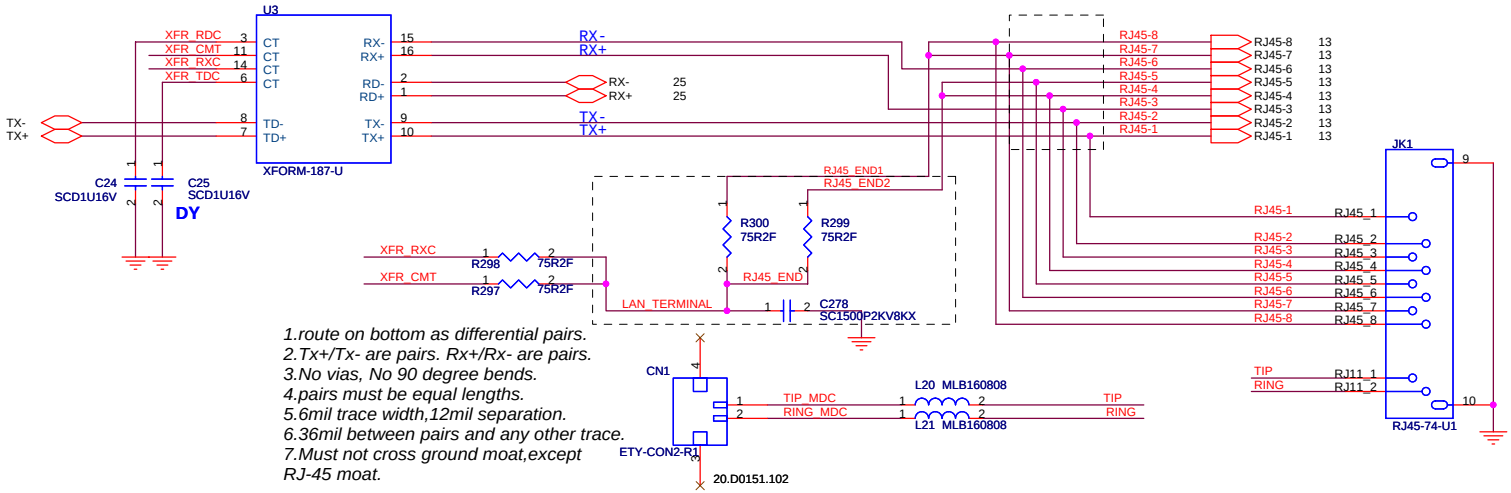




Close to CN20

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

10/100M Lan Transformer



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

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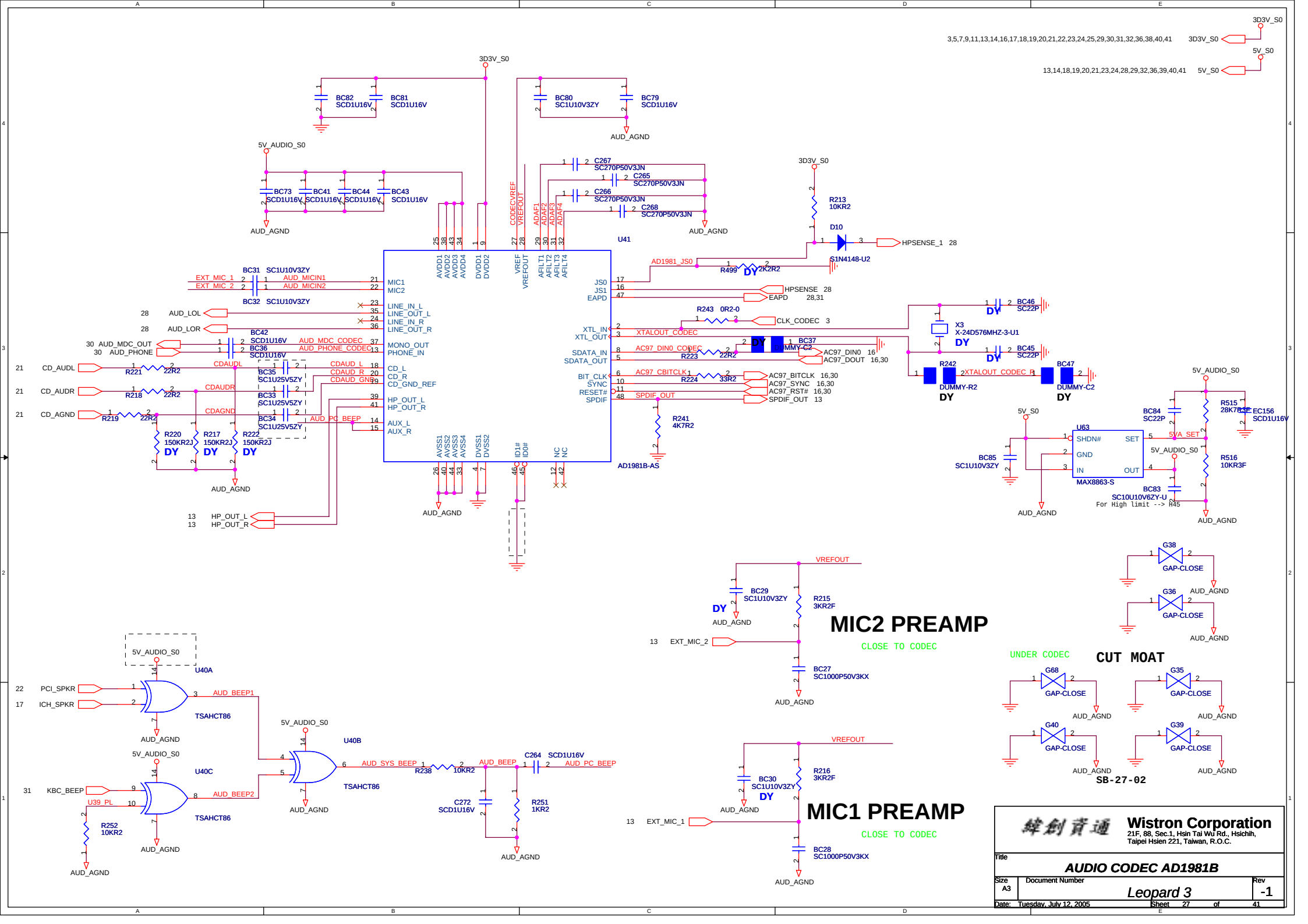
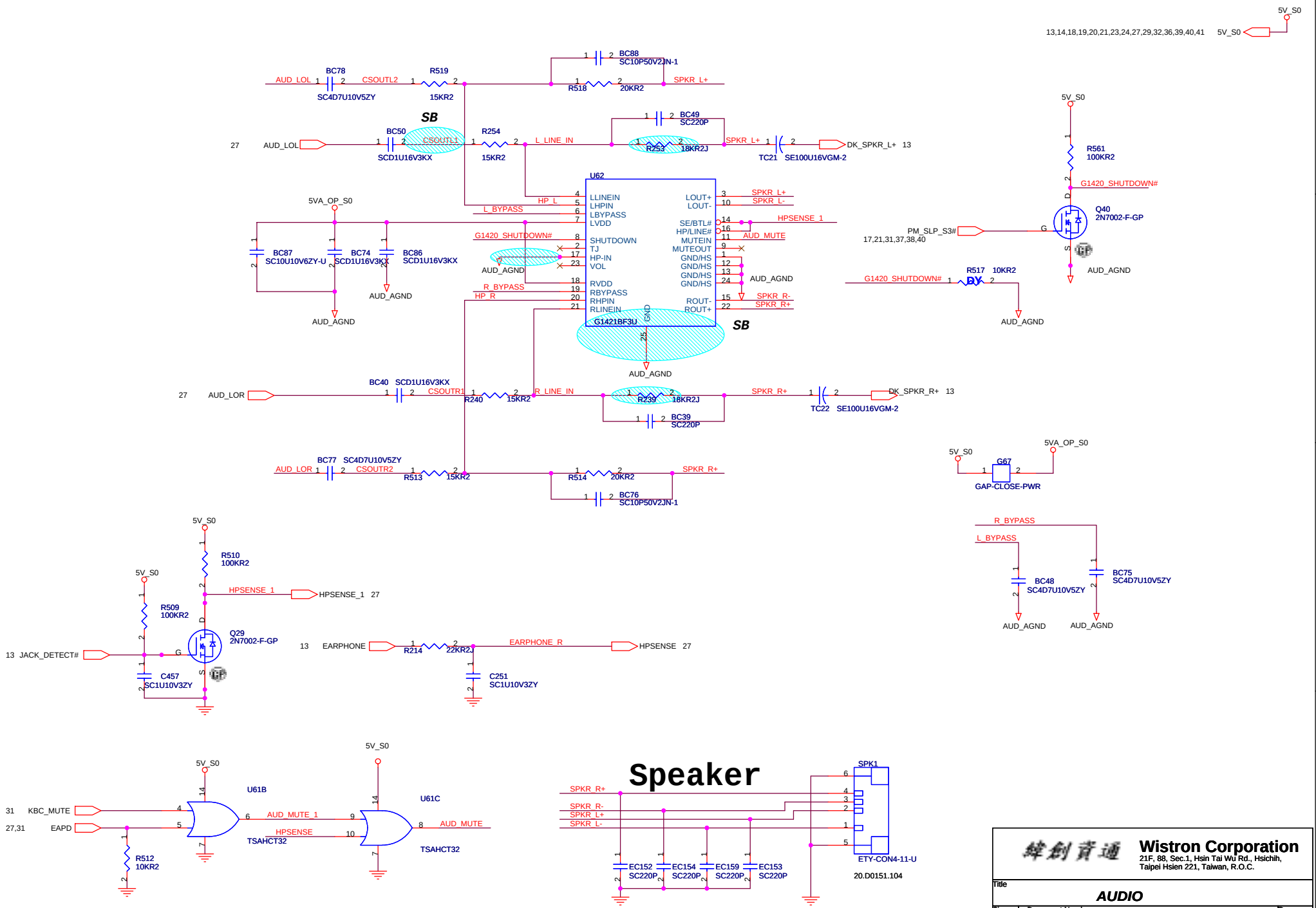
Title: *LAN / 1394 Connector*

Size: A3 | Document Number: Leopard 3 | Rev: -1

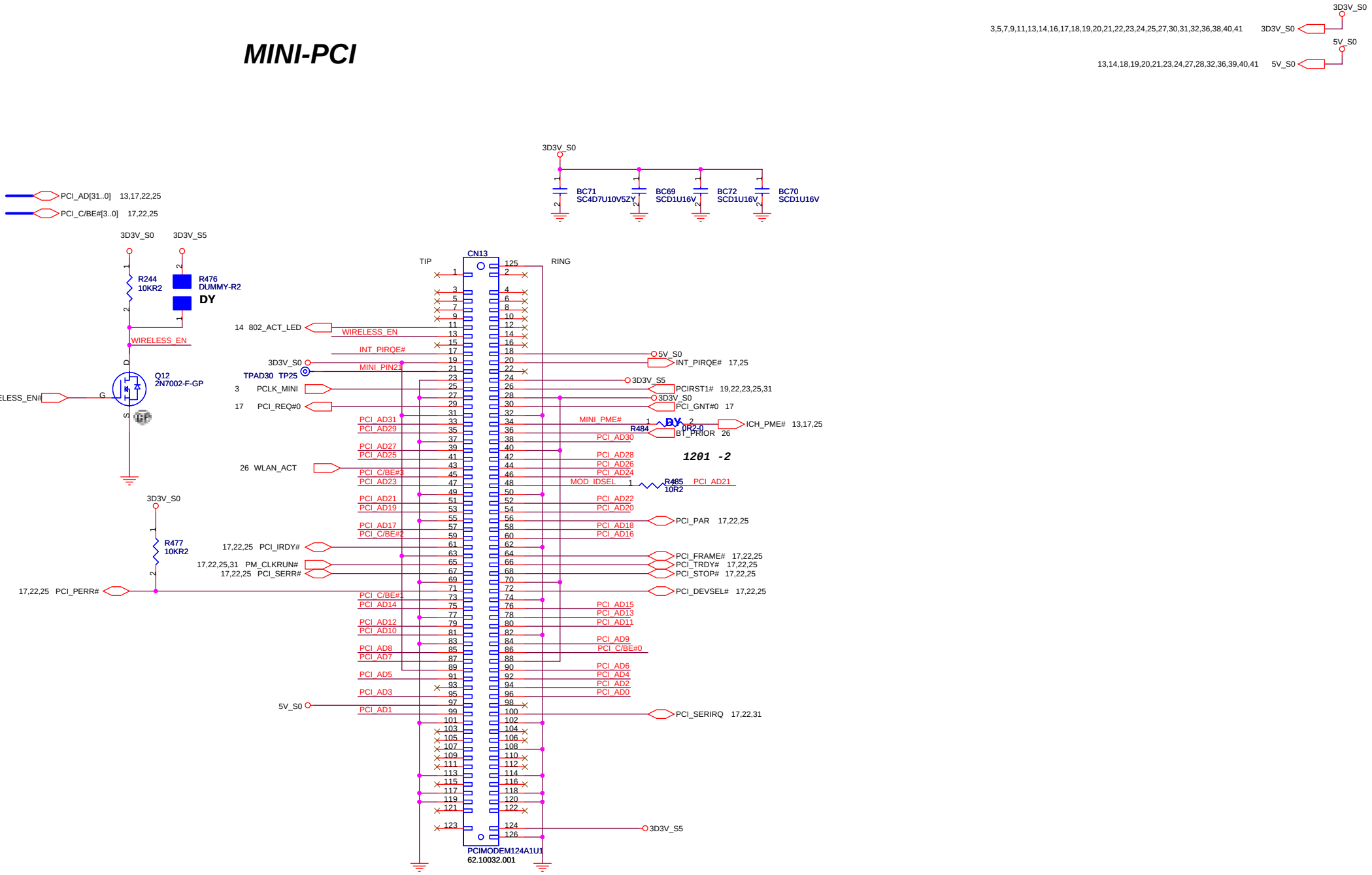
Date: Monday, August 15, 2005 | Sheet 26 of 41


3D3V_S0
5V_S0
3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,29,30,31,32,36,38,40,41
13,14,18,19,20,21,23,24,28,29,32,36,39,40,41
5V_AUDIO_S0
AUD_AGND
U41
AD1981B-AS
MIC1
MIC2
LINE_IN_L
LINE_OUT_L
LINE_IN_R
LINE_OUT_R
MONO_OUT
PHONE_IN
CD_L
CD_R
CD_GND_REF
HP_OUT_L
HP_OUT_R
AUX_L
AUX_R
JS0
JS1
EAPD
XTL_IN
XTL_OUT
SDATA_IN
SDATA_OUT
BIT_CLK
SYNC
RESET#
SPDIF
CODECVREF
VREFOUT
ADAF1
ADAF2
ADAF3
ADAF4
AFILT1
AFILT2
AFILT3
AFILT4
AVDD1
AVDD2
AVDD3
AVDD4
DVDD1
DVDD2
VREF
AVSS1
AVSS2
AVSS3
AVSS4
DVSS1
DVSS2
ID1#
ID0#
NC
EXT_MIC_1
EXT_MIC_2
AUD_MICIN1
AUD_MICIN2
AUD_LOL
AUD_LOR
AUD_MDC_OUT
AUD_PHONE
AUD_MDC_CODEC
AUD_PHONE_CODEC
CD_AUDL
CD_AUDR
CD_AGND
CDAUDL
CDAUDR
CDAGND
CDAUD_L
CDAUD_R
CDAUD_GND
AUD_PC_BEEP
HP_OUT_L
HP_OUT_R
HPSENSE_1
HPSENSE
EAPD
AD1981_JS0
CLK_CODEC
XTALOUT_CODEC
AC97_DIN0_CODEC
AC97_DIN0
AC97_DOUT
AC97_CBITCLK
AC97_BITCLK
AC97_SYNC
AC97_RST#
SPDIF_OUT
BC82 SCD1U16V
BC81 SCD1U16V
BC80 SC1U10V3ZY
BC79 SCD1U16V
BC73 SCD1U16V
BC41 SCD1U16V
BC44 SCD1U16V
BC43 SCD1U16V
C267 SC270P50V3JN
C265 SC270P50V3JN
C266 SC270P50V3JN
C268 SC270P50V3JN
R213 10KR2
D10
S1N4148-U2
R499 2K2R2
DY
BC31 SC1U10V3ZY
BC32 SC1U10V3ZY
BC42 SCD1U16V
BC36 SCD1U16V
R221 22R2
R218 22R2
R219 22R2
BC35 SC1U25V5ZY
BC33 SC1U25V5ZY
BC34 SC1U25V5ZY
R220 150KR2J
R217 150KR2J
R222 150KR2J
R243 0R2-0
BC37 DUMMY-C2
R223 22R2
R224 33R2
R241 4K7R2
BC46 SC22P
X3 X-24D576MHZ-3-U1
BC45 SC22P
R242 DUMMY-R2
BC47 DUMMY-C2
U63
SHDN#
GND
IN
SET
OUT
MAX8863-S
BC84 SC22P
BC85 SC1U10V3ZY
BC83 SC10U10V6ZY-U
For High limit --> H45
R515 28K7R3F
EC156 SCD1U16V
R516 10KR3F
5VA_SET
U40A
U40B
U40C
U39_PL
PCI_SPKR
ICH_SPKR
KBC_BEEP
TSAHCT86
AUD_BEEP1
AUD_BEEP2
AUD_SYS_BEEP
AUD_BEEP
R238 10KR2
C264 SCD1U16V
C272 SCD1U16V
R251 1KR2
R252 10KR2
MIC2 PREAMP
CLOSE TO CODEC
BC29 SC1U10V3ZY
R215 3KR2F
BC27 SC1000P50V3KX
MIC1 PREAMP
BC30 SC1U10V3ZY
R216 3KR2F
BC28 SC1000P50V3KX
UNDER CODEC
CUT MOAT
G38 GAP-CLOSE
G36 GAP-CLOSE
G68 GAP-CLOSE
G35 GAP-CLOSE
G40 GAP-CLOSE
G39 GAP-CLOSE
SB-27-02
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC AD1981B
Size A3
Document Number
Leopard 3
Rev -1
Date: Tuesday, July 12, 2005
Sheet 27 of 41



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AUDIO***	
Size A3	Document Number Leopard 3	Rev -1
Date: Monday, August 15, 2005	Sheet 28 of 41	

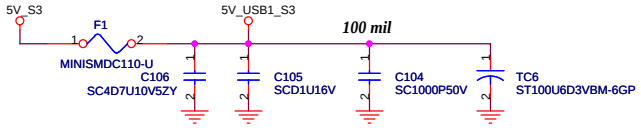
MINI-PCI

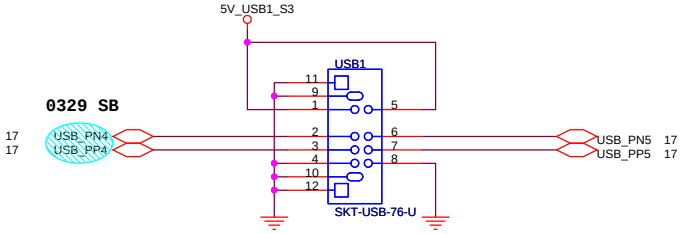


The symbol use 2nd source
The P/N is the main source
Main source:62.10032.001
2nd source:62.10032.031

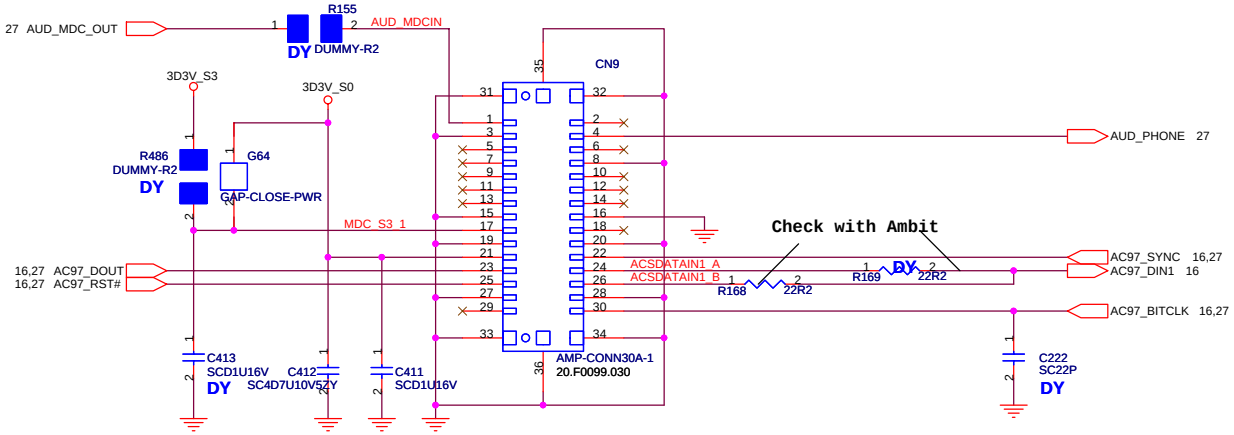
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI-PCI***	
Size A3	Document Number Leopard 3	Rev -1
Date: Tuesday, July 12, 2005	Sheet 29 of 41	

USB POWER

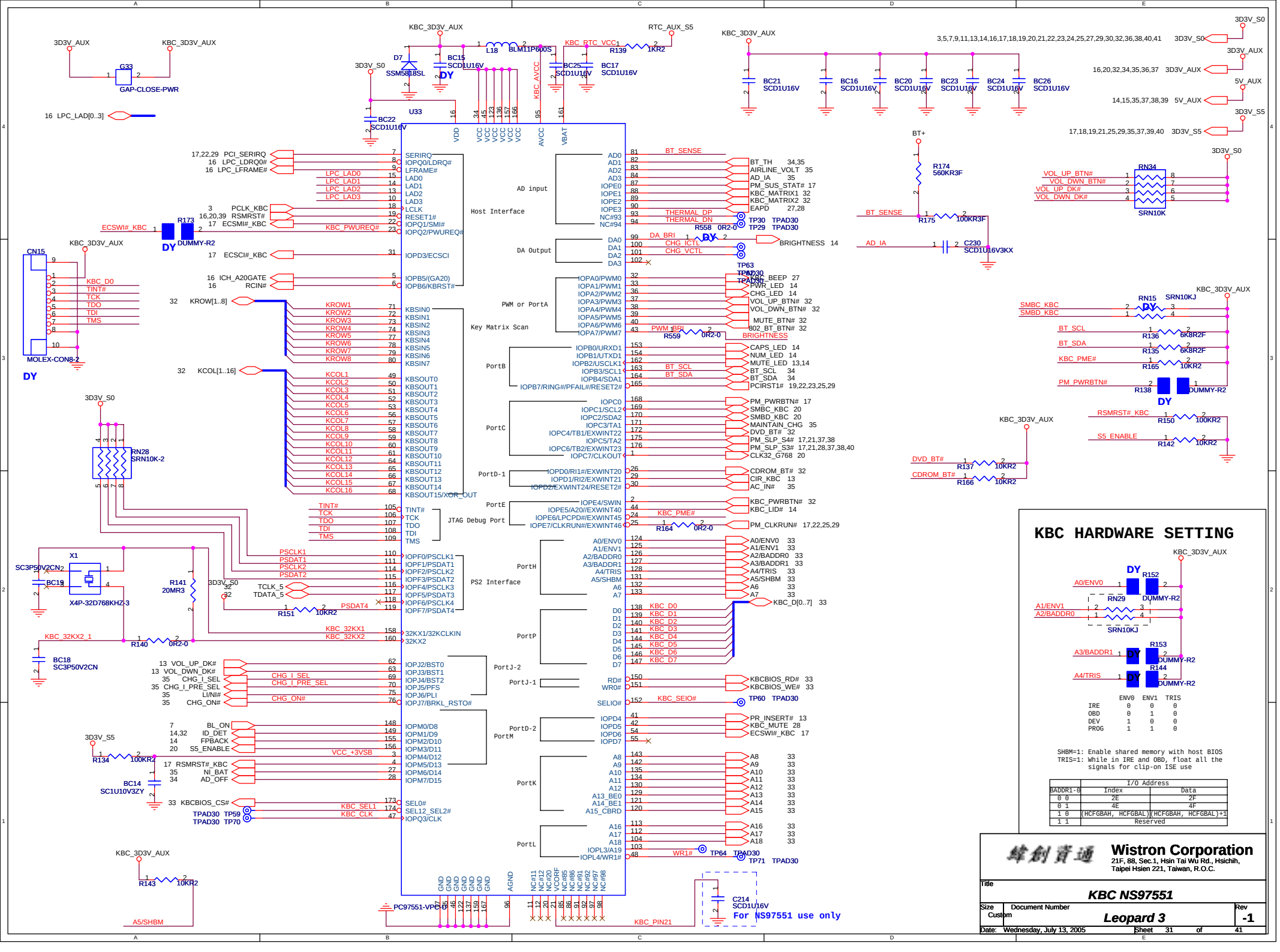




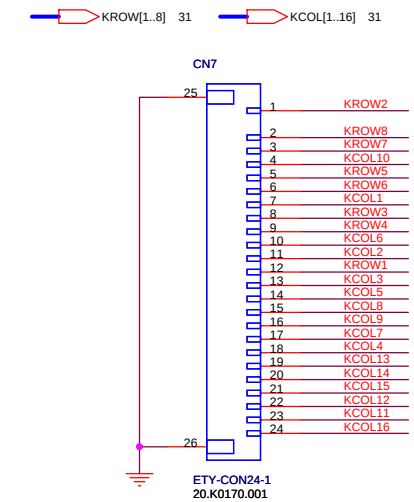
MDC Connector

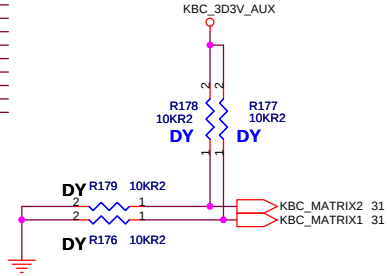


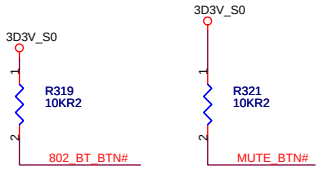
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***USB / MDC CONN.***	
Size A3	Document Number Leopard 3	Rev -1
Date: Tuesday, July 12, 2005	Sheet 30 of 41	


KBC HARDWARE SETTING
A0/ENV0 DY R152 DUMMY-R2
A1/ENV1 RN29 SRN10KJ
A2/BADDR0
A3/BADDR1 DY R153 DUMMY-R2
A4/TRIS DY R144 DUMMY-R2
ENV0 ENV1 TRIS
IRE 0 0 0
OBD 0 1 0
DEV 1 0 0
PROG 1 1 0
SHBM=1: Enable shared memory with host BIOS
TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use
I/O Address
BADDR1-0 Index Data
0 0 2E 2F
0 1 4E 4F
1 0 (HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1
1 1 Reserved
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC NS97551
Size Custom
Document Number
Leopard 3
Rev -1
Date: Wednesday, July 13, 2005
Sheet 31 of 41
For NS97551 use only
U33
PC97551-VPC-0
Host Interface
AD input
DA Output
PWM or PortA
Key Matrix Scan
PortB
PortC
PortD-1
PortE
JTAG Debug Port
PortH
PS2 Interface
PortP
PortJ-2
PortJ-1
PortD-2
PortM
PortK
PortL
CN15 MOLEX-CON8-2
X1 X4P-32D768KHZ-3
G33 GAP-CLOSE-PWR
D7 SSM5818SL
L18 BLM11P600S
R139 1KR2
R174 560KR3F
R175 100KR3F
C230 SCD1U16V3KX
RN34 SRN10K
RN15 SRN10KJ
RN28 SRN10K-2
R173 DUMMY-R2
R138 DUMMY-R2
R150 100KR2
R142 10KR2
R136 6K8R2F
R135 6K8R2F
R165 10KR2
R137 10KR2
R166 10KR2
R141 20MR3
R151 10KR2
R140 0R2-0
R134 100KR2
R143 10KR2
R559 0R2-0
R558 0R2-0
R164 0R2-0
C214 SCD1U16V

INTERNAL KEYBOARD CONNECTOR





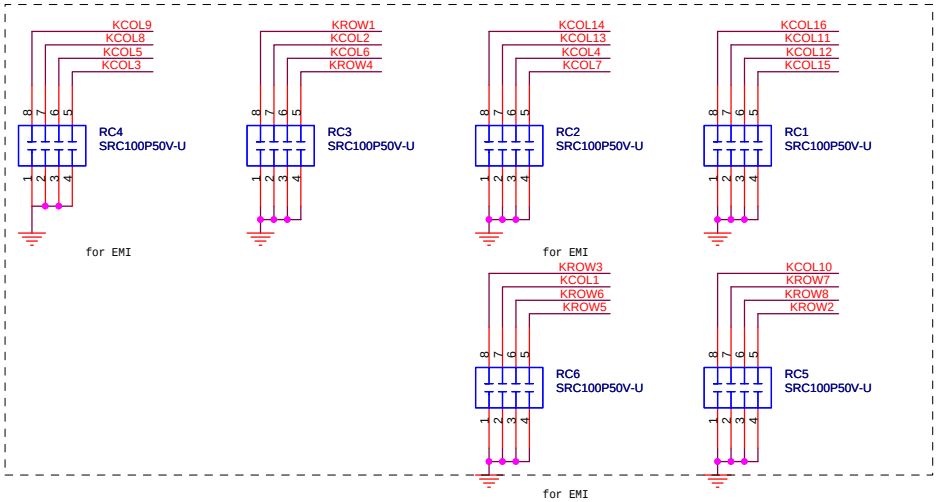


the matrix table for PCB

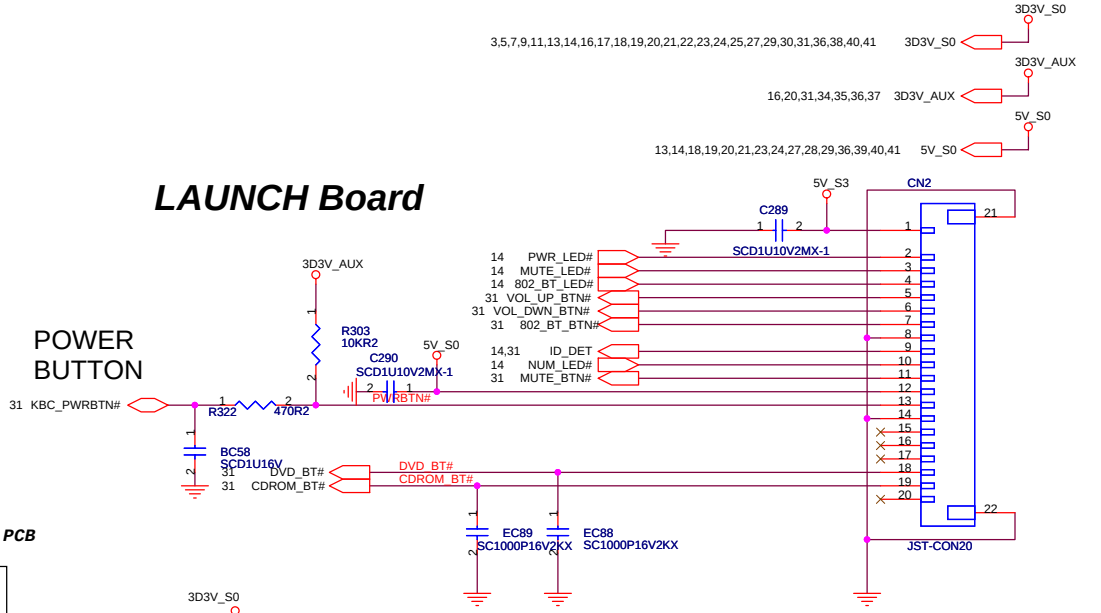
KBC_MATRIX2,KBC_MATRIX1

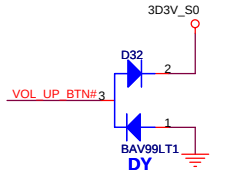
	PA	PR
FF	00	01
DF	10	11

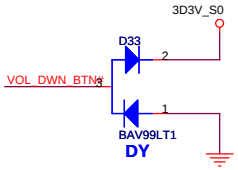
	NONE Quick Play	Quick Play
MATRIXID1#	0	1

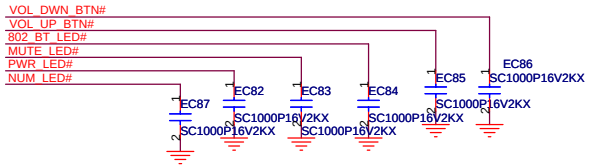


LAUNCH Board

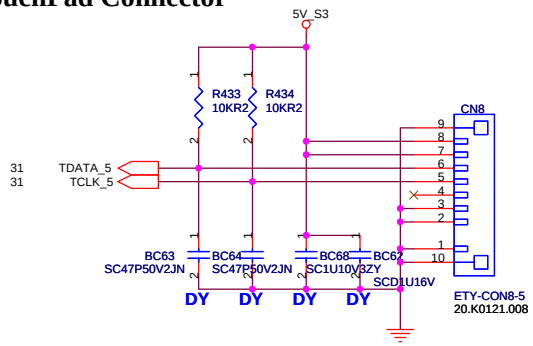




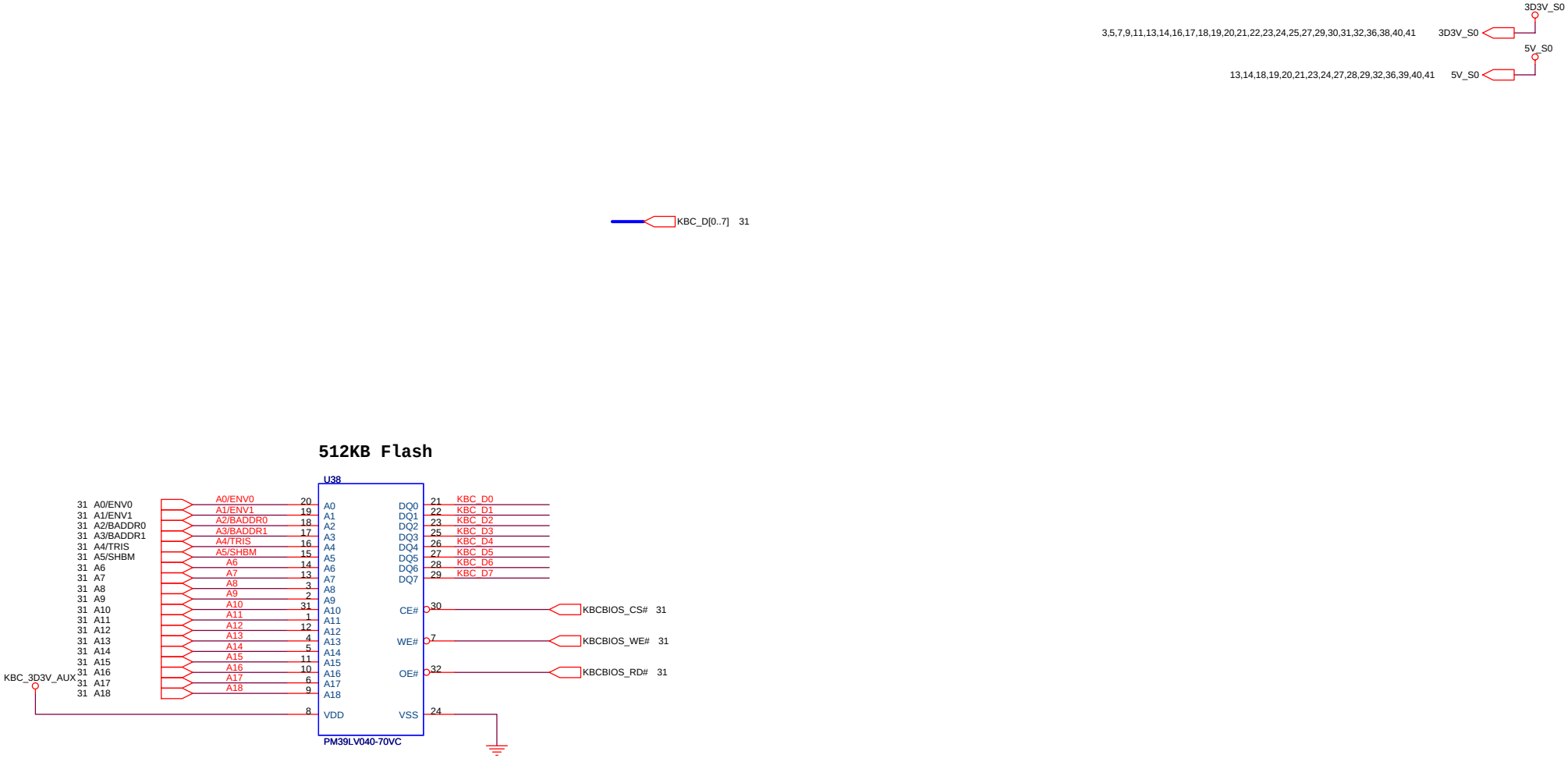




TouchPad Connector

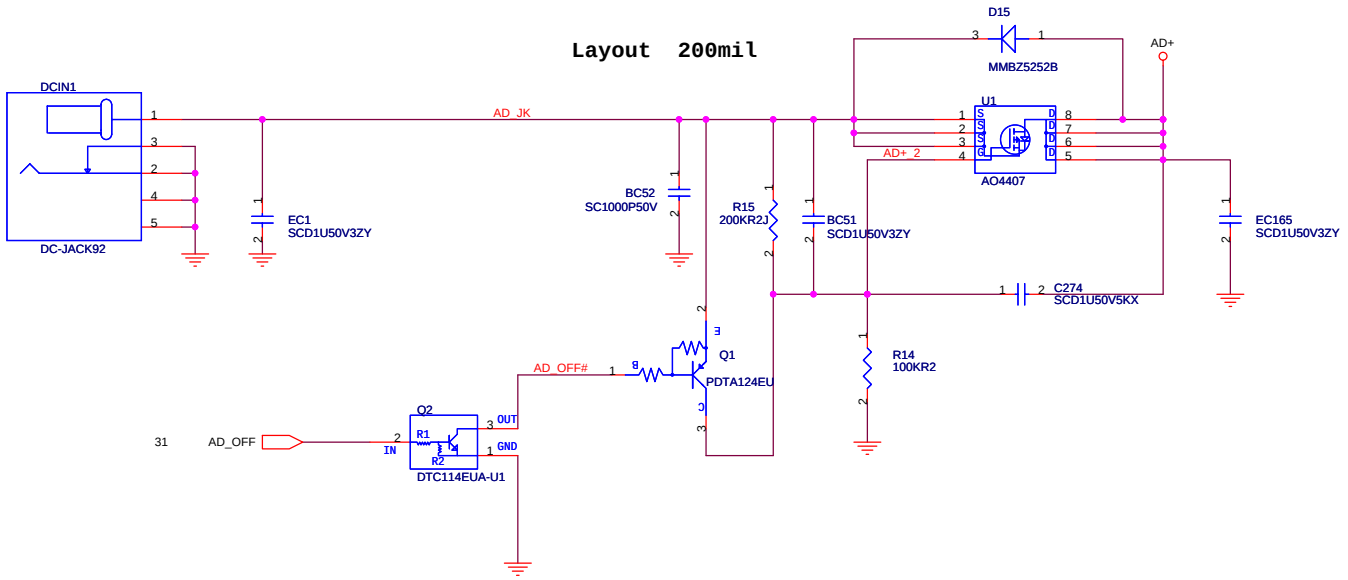


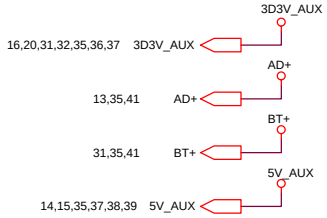
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***KEYBOARD/TOUCH PAD/Launch key***
Size A3	Document Number ***Leopard 3*** Rev **-1**
Date: Tuesday, July 12, 2005	Sheet 32 of 41

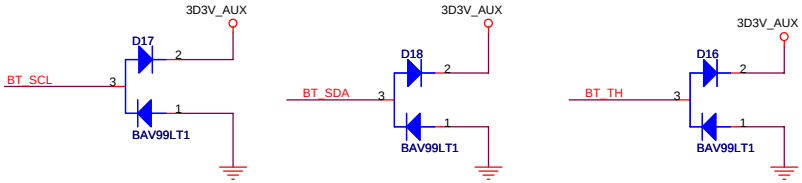


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BIOS/GF***	
Size A3	Document Number ***Leopard 3***	Rev **-1**
Date: Tuesday, July 12, 2005	Sheet 33 of 41	

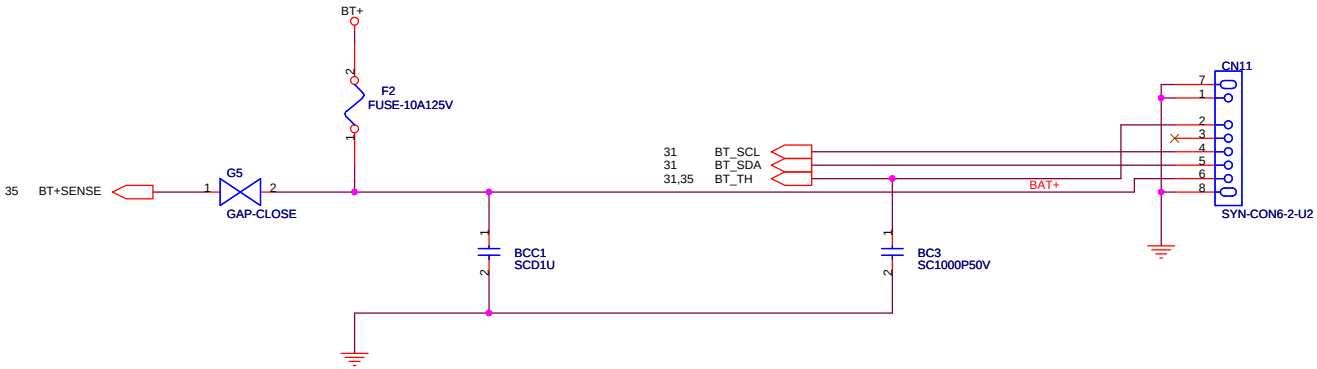
Adaptor in to generate DCBATOUT



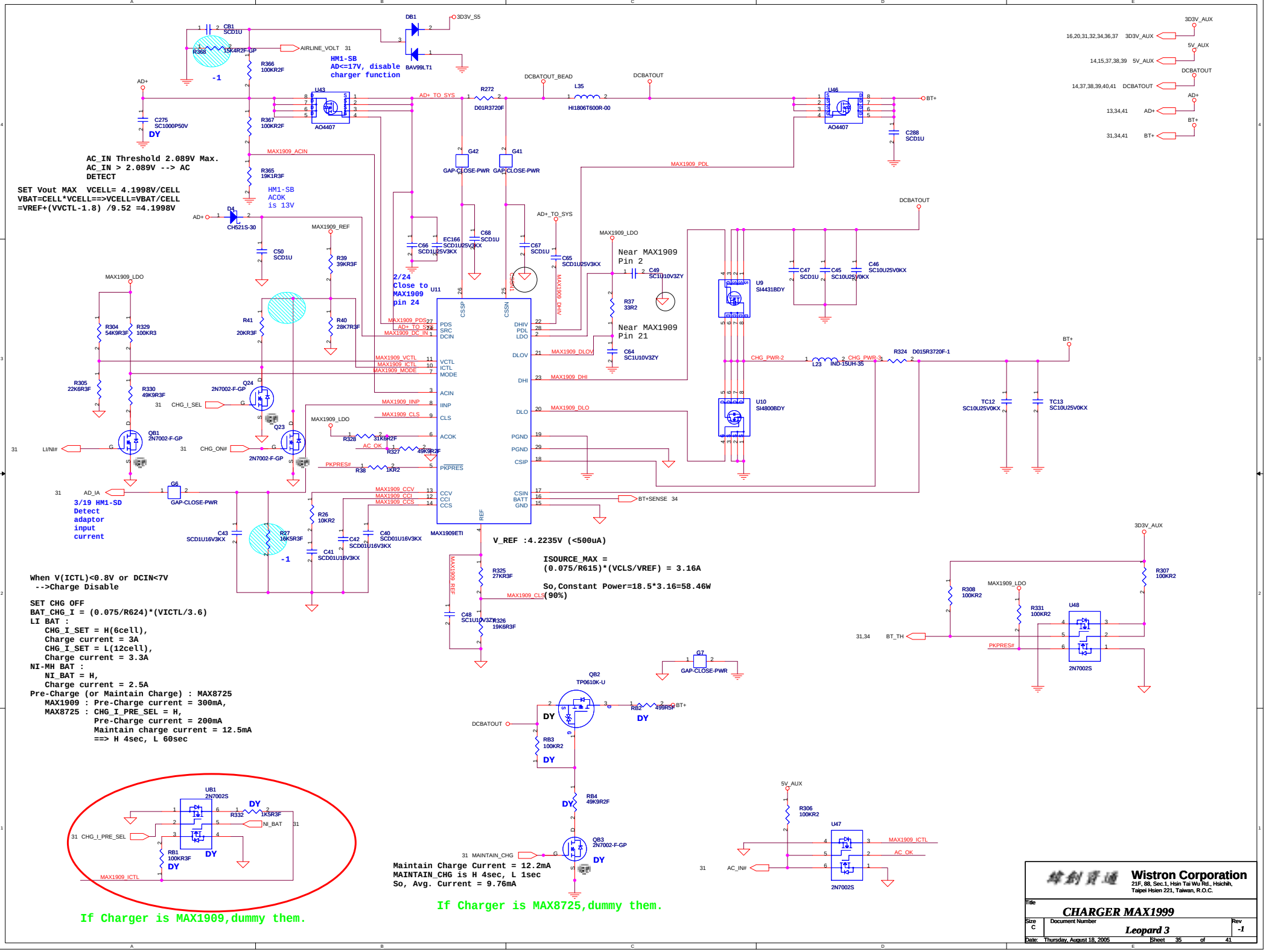




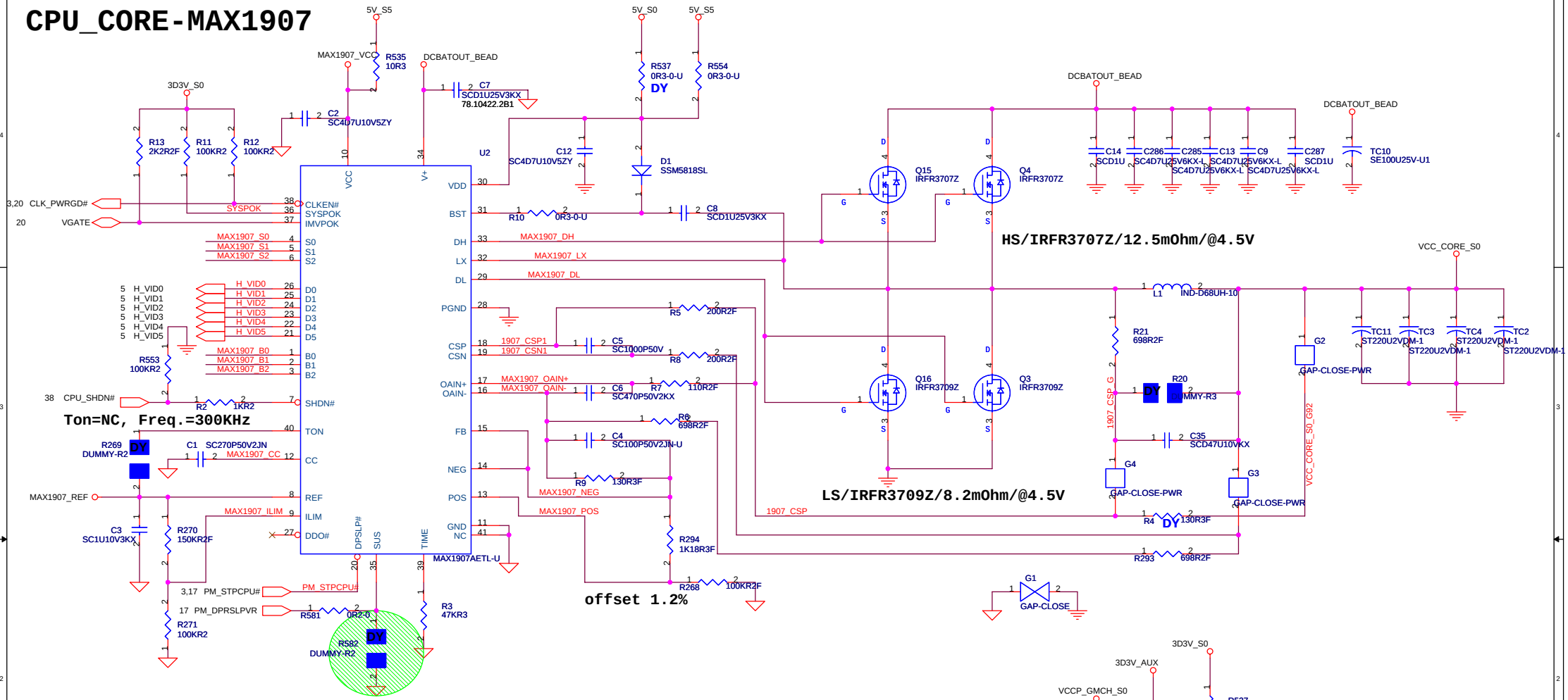
BATTERY CONNECTOR



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Adaptor/ Bettery conn.***	
Size A3	Document Number Leopard 3	Rev -1
Date: Tuesday, July 12, 2005	Sheet 34 of 41	


AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
SET Vout MAX VCELL= 4.1998V/CELL
VBAT=CELL*VCELL==>VCELL=VBAT/CELL
=VREF+(VVCTL-1.8) /9.52 =4.1998V
HM1-SB AD<=17V, disable charger function
HM1-SB ACOK is 13V
2/24 Close to MAX1909 pin 24
Near MAX1909 Pin 2
Near MAX1909 Pin 21
3/19 HM1-SD Detect adaptor input current
V_REF :4.2235V (<500uA)
ISOURCE_MAX = (0.075/R615)*(VCLS/VREF) = 3.16A
So,Constant Power=18.5*3.16=58.46W (90%)
When V(ICTL)<0.8V or DCIN<7V
-->Charge Disable
SET CHG OFF
BAT_CHG_I = (0.075/R624)*(VICTL/3.6)
LI BAT :
CHG_I_SET = H(6cell),
Charge current = 3A
CHG_I_SET = L(12cell),
Charge current = 3.3A
NI-MH BAT :
NI_BAT = H,
Charge current = 2.5A
Pre-Charge (or Maintain Charge) : MAX8725
MAX1909 : Pre-Charge current = 300mA,
MAX8725 : CHG_I_PRE_SEL = H,
Pre-Charge current = 200mA
Maintain charge current = 12.5mA
==> H 4sec, L 60sec
Maintain Charge Current = 12.2mA
MAINTAIN_CHG is H 4sec, L 1sec
So, Avg. Current = 9.76mA
If Charger is MAX1909,dummy them.
If Charger is MAX8725,dummy them.
MAX1909ETI
U11
U43
AO4407
U46
AO4407
U9
SI4431BDY
U10
SI4800BDY
U48
2N7002S
U47
2N7002S
UB1
2N7002S
QB2
TP0610K-U
QB3
2N7002-F-GP
QB1
2N7002-F-GP
Q24
2N7002-F-GP
Q23
2N7002-F-GP
DB1
BAV99LT1
D4
CH521S-30
L35
HI1806T600R-00
L23
IND-15UH-35
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CHARGER MAX1999
Size C
Document Number
Leopard 3
Rev -1
Date: Thursday, August 18, 2005
Sheet 35 of 41

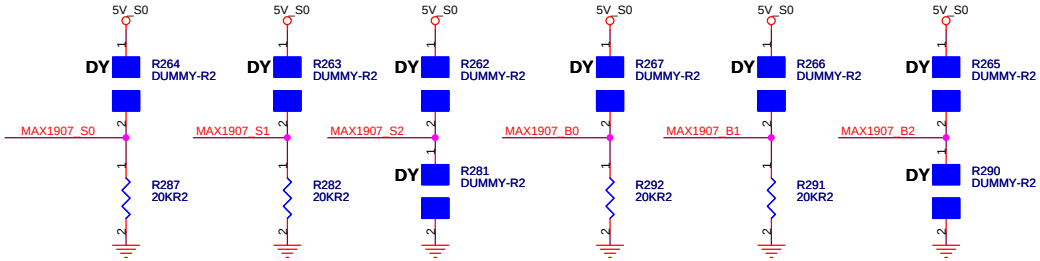
CPU_CORE-MAX1907



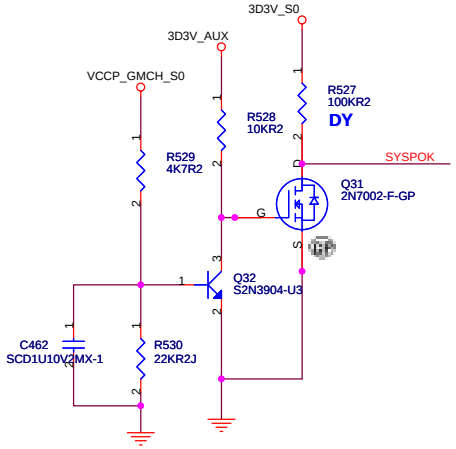
OCP=30A, Vally current = 27.5A,
Vilim=550mV(55mVp-p*10)

Deeper Sleep Voltage : 0.940V
, S0=L, S1=L, S2=Open,

Boot-up Voltage : 1.2V
, B0=L, B1=L, B2=Open



VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940



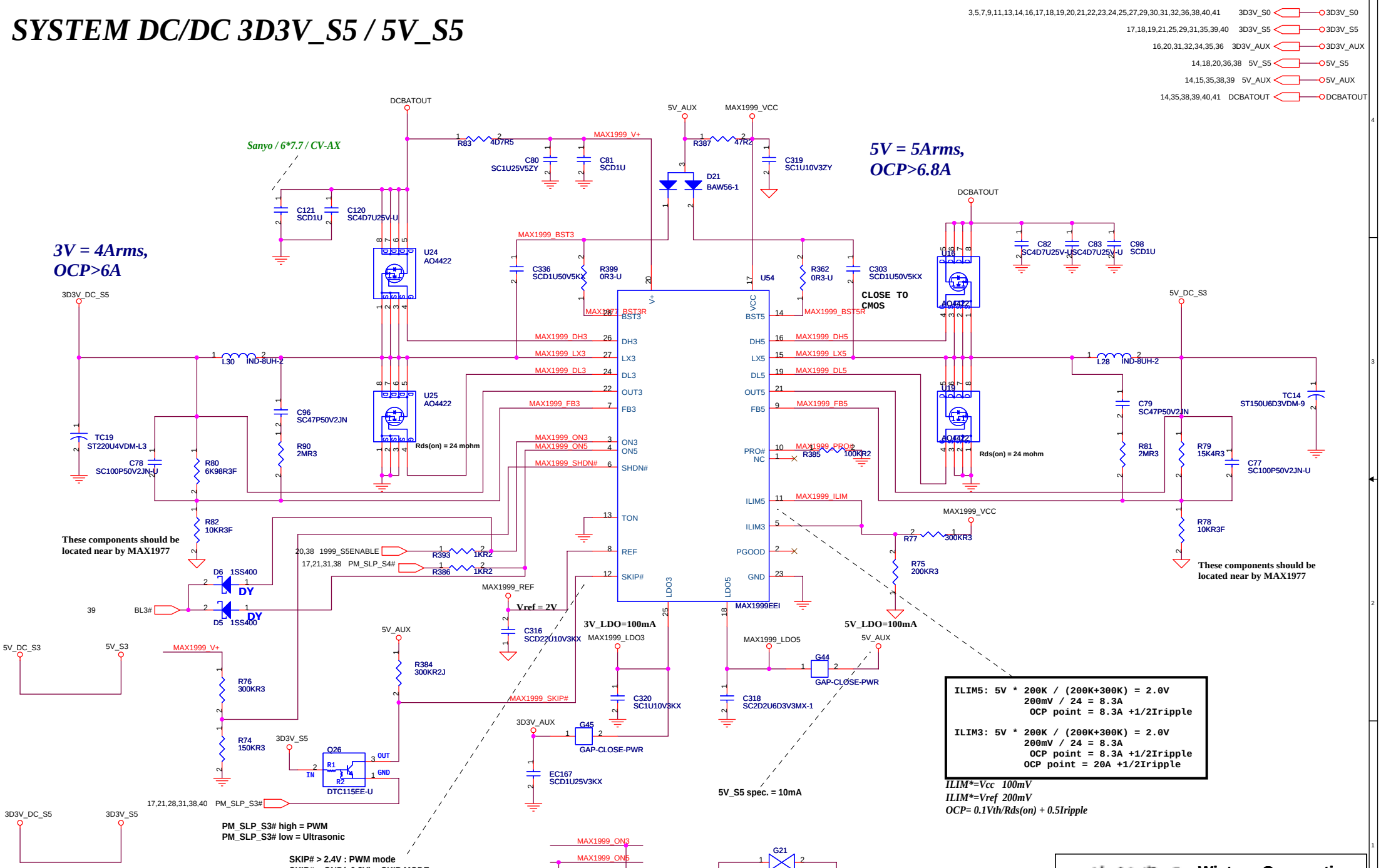
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IMVP IV-CPU POWER-MAX1907

Size: A3 | Document Number: Leopard 3 | Rev: -1

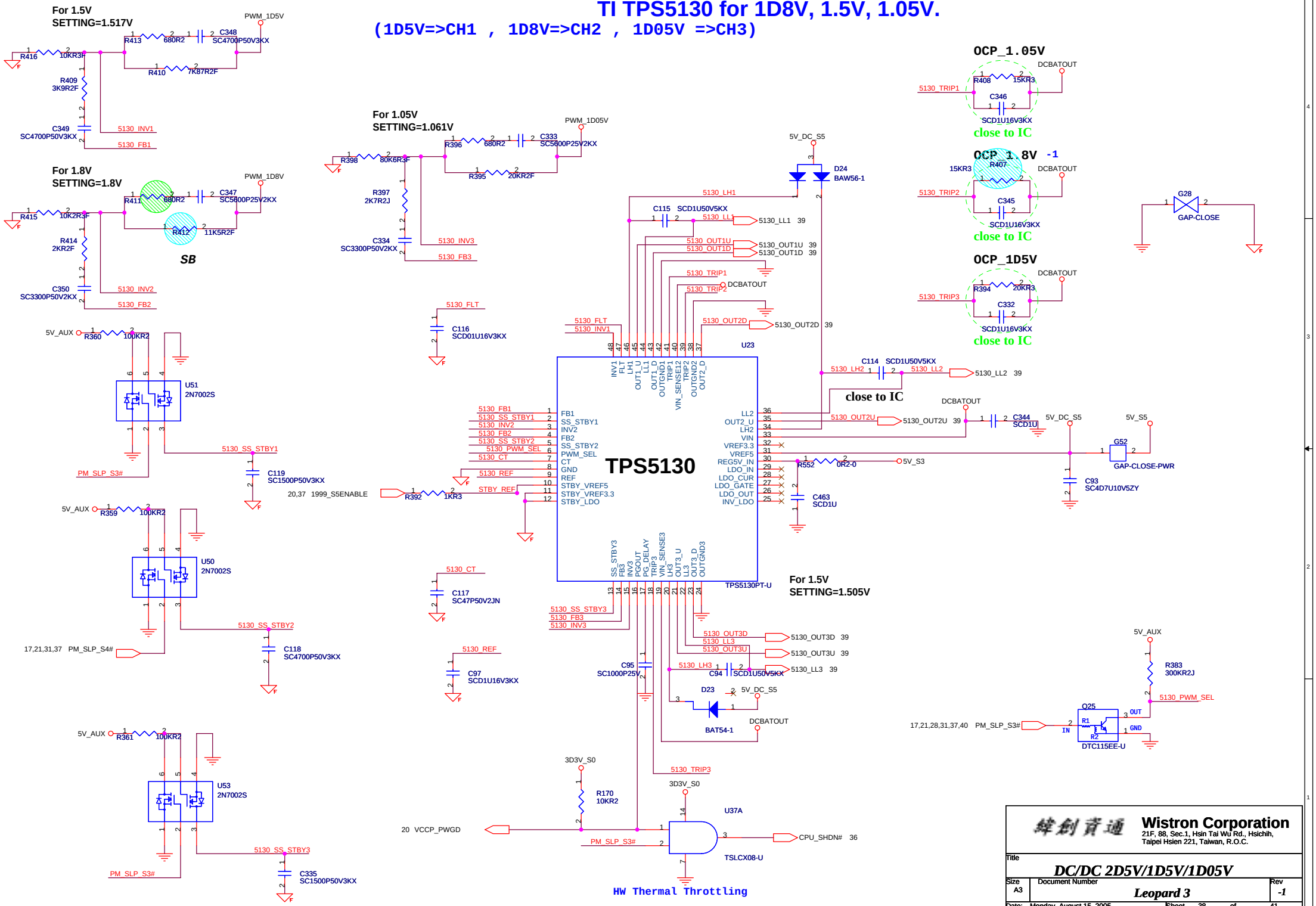
Date: Thursday, August 18, 2005 | Sheet 36 of 41

SYSTEM DC/DC 3D3V_S5 / 5V_S5



TI TPS5130 for 1D8V, 1.5V, 1.05V.

(1D5V=>CH1 , 1D8V=>CH2 , 1D05V =>CH3)



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*DC/DC 2D5V/1D5V/1D05V*
Size A3	Document Number *Leopard 3* Rev -1
Date: Monday, August 15, 2005	Sheet 38 of 41

TI TPS5130 for 2.5V, 1.5V, 1.05V

(1D5V=>CH1 , 2D5V=>CH2 , 1D05V =>CH3)

14,35,37,38,40,41 DCBATOUT — DCBATOUT
17,18,19,21,25,29,31,35,37,40 3D3V_S5 — 3D3V_S5
14,15,35,37,38 5V_AUX — 5V_AUX
18 1D5V_S5 — 1D5V_S5
7,9,10,11,12,38,40,41 1D8V_S3 — 1D8V_S3
13,14,18,19,20,21,23,24,27,28,29,32,36,40,41 5V_S0 — 5V_S0
12 0D9V_S0 — 0D9V_S0

1D5V/5A
OCP=10A

DCBATOUT
C128 SCD1U
C129 SC4D7U25V6KX-L
U27 SI4800BDY
38 5130_OUT1U — 5130_OUT1U
38 5130_LL1 — 5130_LL1
L31 IND-4D7UH-56
PWM_1D5V
U26 IRF7807Z
Rds(on)=16mOhm
TC18 ST220U2VDM-1
38 5130_OUT1D — 5130_OUT1D

PWM_1D5V — 1D5V_S0
PWM_1D05V — 1D5V_S0

1.5V_S5 (For ICH6)

3D3V_S5
U59 G9131-15T73UF-GP
VIN, VOUT, GND
1D5V_S5
C414 SC10U10V6ZY-U
Imax=300mA

PWM_1D8V — 1D8V_S3

Power budget:0D9V/2.2Apeak (For DDR2_VTT)

DCBATOUT
C112 SCD1U
C113 SC4D7U25V6KX-L
U22 SI4800BDY
38 5130_OUT2U — 5130_OUT2U
38 5130_LL2 — 5130_LL2
L29 IND-4D7UH-56
PWM_1D8V
U21 IRF7807Z
Rds(on)=16mOhm
TC17 ST330U3VDM-1-GP
38 5130_OUT2D — 5130_OUT2D

0D9V / 1A

0D9V_S0
TC8 SE220U16VM-U
C460 SC10U10V5ZY-L
TC20 ST150U4VBM-L17
DY

U58 APL5331KAC-TR
VOUT, NC, NC, NC, VIN, VREF, VCNTL, GND, GND
1D8V_S3
C367 SC10U10V5ZY-L
5V_S0
C376 SCD1U10V2MX-1
R446 1KR2F
APL533_VREF1
R133 0R2-0
DDR_VREF_1 40
C368 SCD1U10V2MX-1
R447 1KR2F
R446,R447 for 1G Memory

L3# circuit

DCBATOUT
C75 SCD1U
C76 SC4D7U25V6KX-L
U18 SI4800BDY
38 5130_OUT3U — 5130_OUT3U
38 5130_LL3 — 5130_LL3
L27 IND-4D7UH-56
PWM_1D05V
U15 IRF7807Z
Rds(on)=16mOhm
R73 1KR2
DY
TC5 ST220U4VDM-10
38 5130_OUT3D — 5130_OUT3D

1D05V/5A
OCP=10A

DCBATOUT
R363 1MR2F
HTH
L3# at 8.13V
R364 6K04R2F
HTH
R323 174KR2F

5V_AUX
C293 SCD1U10V2MX-1
U52 G680LT1
HTH, GND, LTH, VCC, RESET#/RESET
37 BL3#
D20 BAT54-1
RSMRST# 16,20,31

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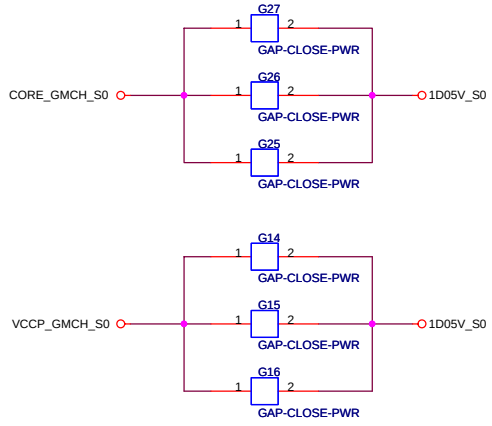
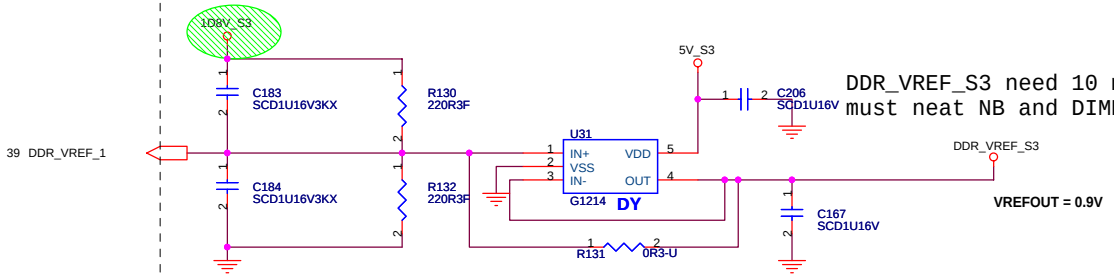
Taipei Hsien 221, Taiwan, R.O.C.

Title: 39.DC/DC 1D8V/1D5V/1D05V-2
Size: A3
Document Number: Leopard 3
Rev: -1
Date: Thursday, August 18, 2005
Sheet 39 of 41

FOR GMCH Power



3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,41 3D3V_S0 — 3D3V_S0
13,14,30 3D3V_S3 — 3D3V_S3
17,18,19,21,25,29,31,35,37,39 3D3V_S5 — 3D3V_S5
13,14,18,19,20,21,23,24,27,28,29,32,36,39,41 5V_S0 — 5V_S0
13,14,26,28,30,32,37,38,41 5V_S3 — 5V_S3
14,18,20,36,38 5V_S5 — 5V_S5
7,9,15,18 2D5V_S0 — 2D5V_S0
7,9,10,11,12,38,39,41 1D8V_S3 — 1D8V_S3
7,11 DDR_VREF_S3 — DDR_VREF_S3
14,35,37,38,39,41 DCBATOUT — DCBATOUT
38,39,41 1D05V_S0 — 1D05V_S0
4,5,6,7,9,10,16,18,36,41 VCCP_GMCH_S0 — VCCP_GMCH_S0
6,9,10,41 CORE_GMCH_S0 — CORE_GMCH_S0

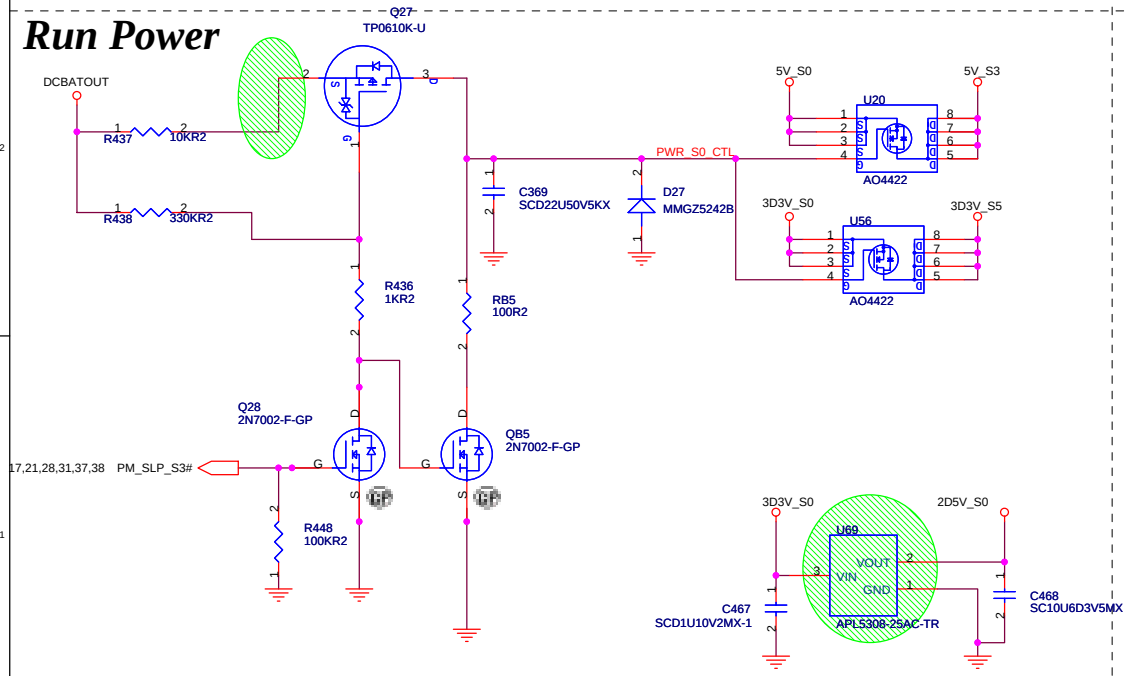


DDR_VREF_S3 need 10 mil and must neat NB and DIMM

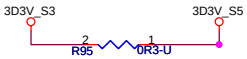
VREFOUT = 0.9V

FOR DDR 2 Power

Run Power



Suspend Power



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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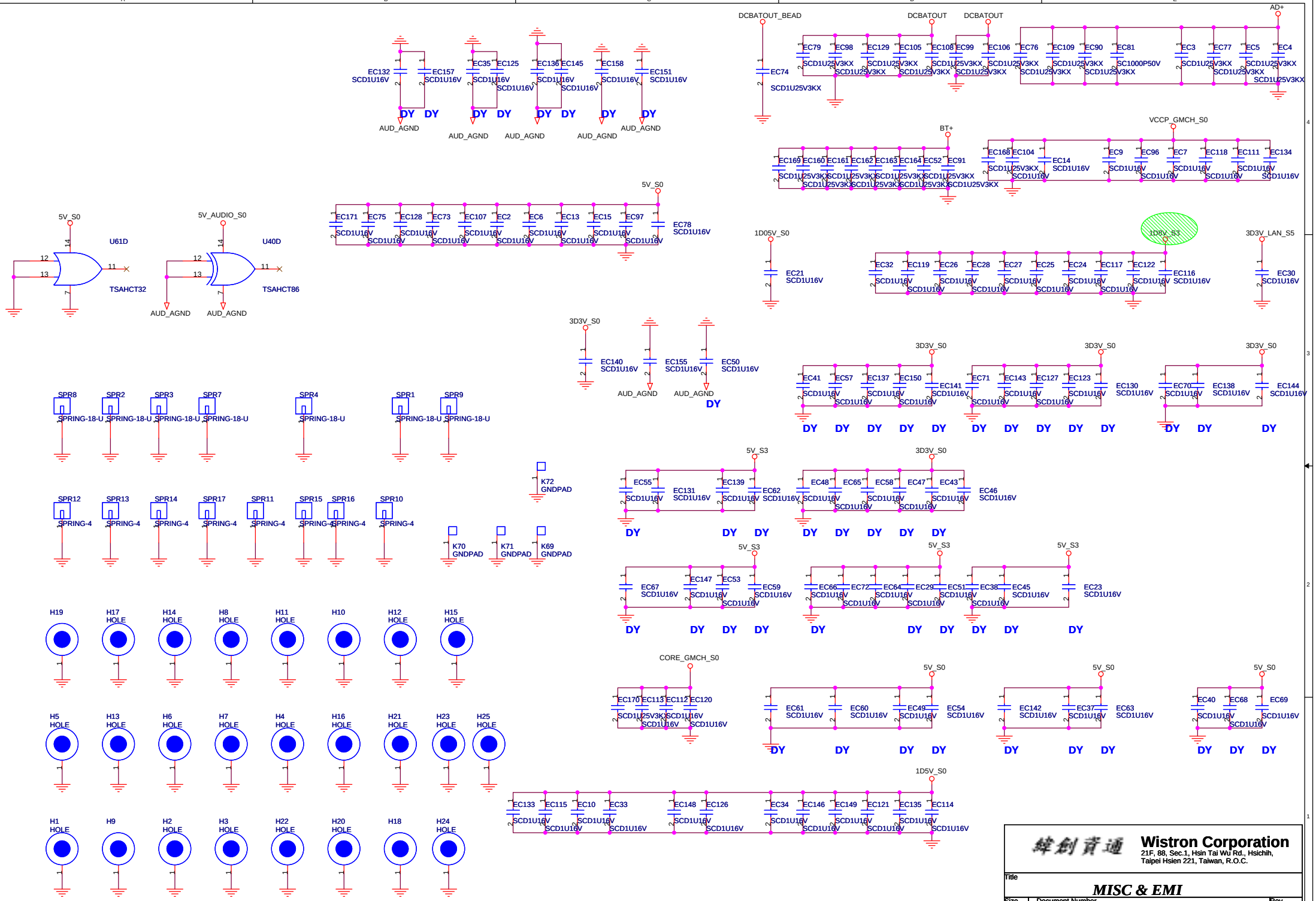
Size: A3 | Document Number: Leopard 3 | Rev: -1

Date: Tuesday, July 12, 2005 | Sheet 40 of 41


DCBATOUT_BEAD
DCBATOUT
DCBATOUT
AD+
EC74 SCD1U25V3KX
EC79 EC98 EC129 EC105 EC108 EC99 EC106 EC76 EC109 EC90 EC81 EC3 EC77 EC5 EC4
SCD1U25V3KX
SC1000P50V
EC132 SCD1U16V EC157 SCD1U16V
EC35 EC125 SCD1U16V
EC136 EC145 SCD1U16V
EC158 SCD1U16V EC151 SCD1U16V
DY
AUD_AGND
BT+
EC169 EC160 EC161 EC162 EC163 EC164 EC52 EC91
VCCP_GMCH_S0
EC168 EC104 EC14 SCD1U16V
EC9 EC96 EC7 EC118 EC111 EC134
5V_S0
EC171 EC75 EC128 EC73 EC107 EC2 EC6 EC13 EC15 EC97 EC78 SCD1U16V
5V_S0
U61D
TSAHCT32
5V_AUDIO_S0
U40D
TSAHCT86
AUD_AGND
1D05V_S0
EC21 SCD1U16V
1D8V_S3
EC32 EC119 EC26 EC28 EC27 EC25 EC24 EC117 EC122 EC116 SCD1U16V
3D3V_LAN_S5
EC30 SCD1U16V
3D3V_S0
EC140 SCD1U16V
EC155 SCD1U16V
EC50 SCD1U16V
AUD_AGND
DY
3D3V_S0
EC41 EC57 EC137 EC150 EC141 SCD1U16V
EC71 EC143 EC127 EC123 EC130 SCD1U16V
EC70 EC138 EC144 SCD1U16V
SPR8 SPR2 SPR3 SPR7 SPR4 SPR1 SPR9
SPRING-18-U
SPR12 SPR13 SPR14 SPR17 SPR11 SPR15 SPR16 SPR10
SPRING-4
K72 GNDPAD
K70 GNDPAD
K71 GNDPAD
K69 GNDPAD
5V_S3
EC55 EC131 SCD1U16V EC139 EC62 SCD1U16V
3D3V_S0
EC48 EC65 EC58 EC47 EC43 EC46 SCD1U16V
EC67 SCD1U16V EC147 EC53 EC59 SCD1U16V
EC66 EC72 EC64 EC29 EC51 SCD1U16V
EC38 EC45 SCD1U16V EC23 SCD1U16V
H19 H17 HOLE H14 HOLE H8 HOLE H11 HOLE H10 H12 HOLE H15 HOLE
H5 HOLE H13 HOLE H6 HOLE H7 HOLE H4 HOLE H16 HOLE H21 HOLE H23 HOLE H25 HOLE
H1 HOLE H9 H2 HOLE H3 HOLE H22 HOLE H20 HOLE H18 H24 HOLE
CORE_GMCH_S0
EC170 EC113 EC112 EC120 SCD1U25V3KX SCD1U16V
5V_S0
EC61 SCD1U16V EC60 SCD1U16V EC49 SCD1U16V EC54 SCD1U16V
EC142 SCD1U16V EC37 SCD1U16V EC63 SCD1U16V
EC40 EC68 SCD1U16V EC69 SCD1U16V
1D5V_S0
EC133 EC115 EC10 EC33 EC148 EC126 EC34 EC146 EC149 EC121 EC135 EC114 SCD1U16V
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
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Sheet 41 of 41