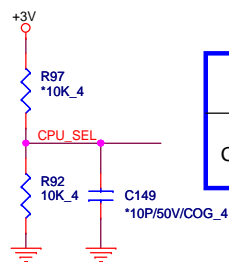
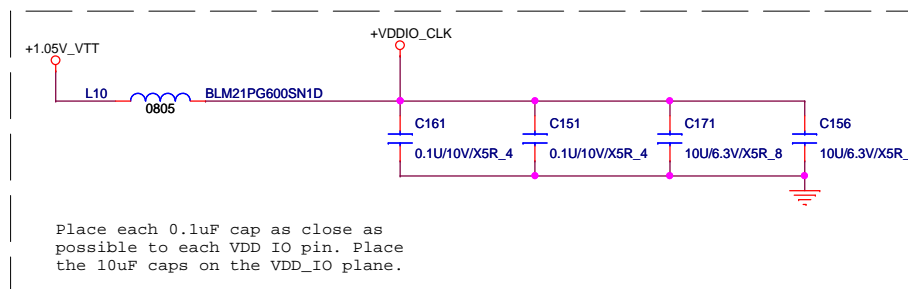
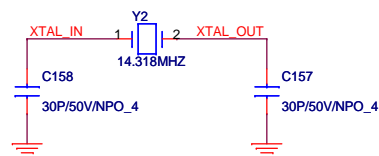
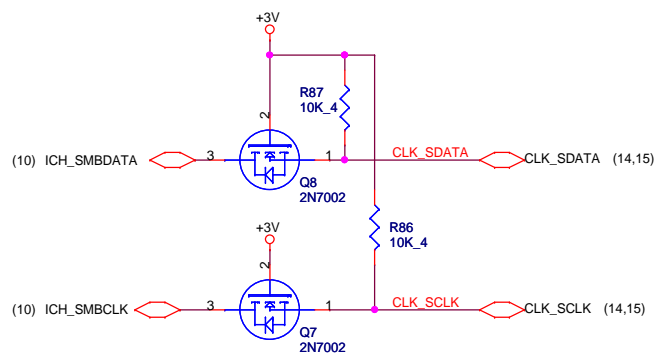
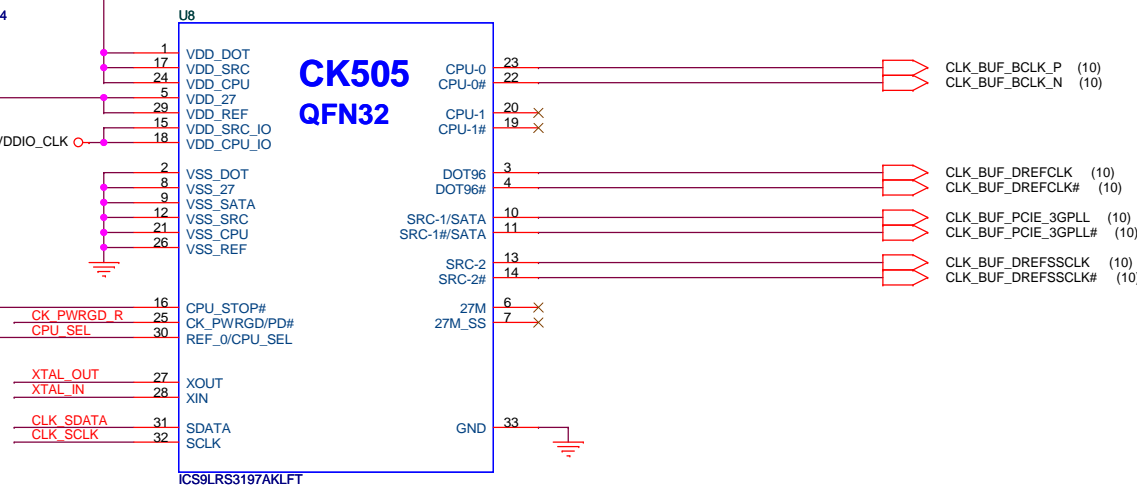
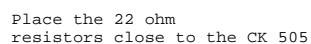


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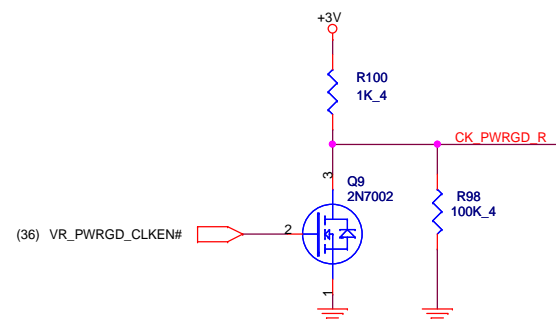
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3	CLOCK GENERATOR
4-7	Auburndale CPU
8-13	Ibex Peak-M
14-15	DDRIII SO-DIMM
16-22	Discreate VGA (M92-XT)
23	LCD + Camera Conn.
24	HDMI Conn.
25	CRT Conn.
26	Audio Codec ALC269
27	RTL8111DL
28	SATA HDD & ODD
29	USB x 2 & ESATA
30	USB X2/SIM_CARD/LEDs/RF
31	MINI-Card (UWB & WWAN)
32	MINI-Card (WLAN)
33	ONFI
34	Express Card
35	K/B & T/P
36	BLUETOOTH
37	FAN & Thermal
38	G-Sensor
39	B To B Conn.
40	iTPM & RFID EEPROM
41	KBC IT8502E
42	HOLD & SKEW
43	Discharge
44	Charger
45	DDR3 (TPS5116REGR)
46	1.05V_VTT & 1.05_PCH (RT8204)
47	3V/5V (MAX17101)
48	CPU (MAX17082)
49	DIS_GFX_VCC (MAX8792)
50	DIS_1.8V_RUN (OZ8116LN)
51	Power Block Dianram
52	XDP
53	Revision & Schematic Value Description
54	BOM Matrix Table

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	23,32,43,44,45,46,47,48,49,50	MAIN POWER		S0-S5
+3VRTC	+3.0V~+3.3V	9,12,41	RTC		S0-S5
3VPCU	+3.3V	9,23,27,30,32,35,39,41,43,44,47	ITE8052 POWER	3V5V_EN	S0-S5
5VPCU	+5V	14,43,44,45,46,47,49,50	DC/DC POWER IC SOURCE	3V5V_EN	S0-S5
+15V	+15V	23,38,43,45,46,47	LARGE POWER	3V5V_EN	S0-S5
LANVCC	+3.3V	27,43	LAN POWER	LAN_ON	
5V_S5	+5V	12,29,30,43	PCH SUS POWER	S5_ON	S0-S3
3V_S5	+3.3V	8,9,10,11,12,43,52	Sys Management,PCH Resume Well, Intel HD Audio,USB,WLAN WiMAX POWER	S5_ON	S0-S3
5VSUS	+5V	23,39,43,48	SLP_S4# CTRLD POWER	SUSON	S0-S3
3VSUS	+3.3V	14,15,30,34,41,43,49	SLP_S4# CTRLD POWER	SUSON	S0-S3
1.5VSUS	+1.5V	4,6,14,15,43,45,46,49,50	SODIMM POWER	SUSON	S0-S3
0.75VSMDDR_VTERM	+0.75V	14,15,43,45	DDR3 SODIMM REFERENCE POWER	MAIN_ON	S0
+5V	+5V	12,18,23,24,25,26,28,35,37,41,43,44	SLP_S3# CTRLD POWER	MAIN_ON	S0
+3V	+3.3V	3,4,8,9,10,11,12,14,15,17,23,25,26,27,28,29,30,31,32,33,34,36,37,38,39,40,41,43,44,45,46,47,48,50,52	SLP_S3# CTRLD POWER	MAIN_ON	S0
+1.8V	+1.8V	6,12,17,18,21,22,33,43,50	LVDS,NVM POWER	MAIN_ON	S0
+1.5V	+1.5V	12,18,19,20,31,32,34,45,46	Mini PCIe,Express Card POWER	MAIN_ON	S0
+1.05V_VTT	+1.05V	4,6,11,12,43,46,48,52	AuBurndale VTT POWER	MAIN_ON	S0
+1.05V_PCH	+1.05V	3,10,12,43,46,52	PCH CORE POWER	1.05V_RUN_ON	S0
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,43,49	VGA CORE POWER	GFXVR_EN	S0
VCC_CORE		6,43,48	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	23	LCD Power	ENVDD	S0
+5V_ODD	+5V	28	ODD Power	MAIN_ON	S0
+5V_HDD	+5V	28	HDD Power	MAIN_ON	S0
BAT-V	+10V~+17V	44	MAIN BATTERY	CHG_PBATT	S0-S5



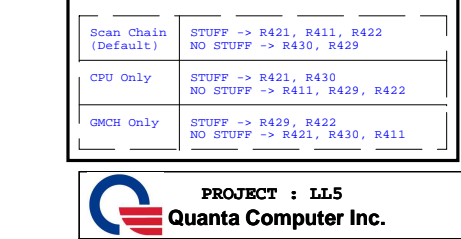
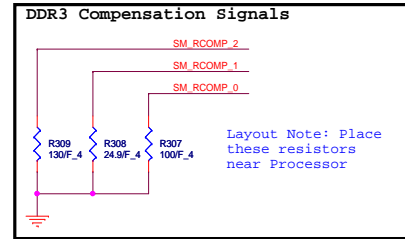
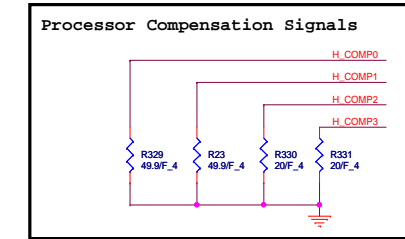
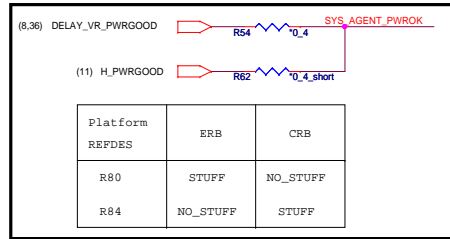
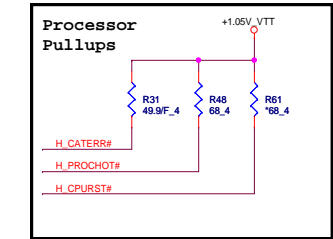
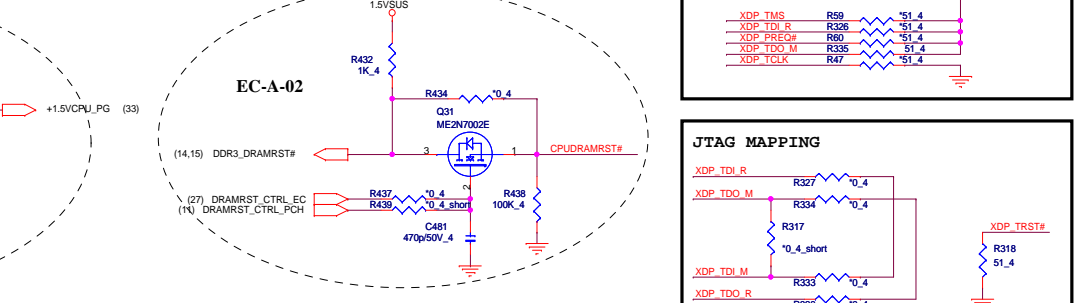
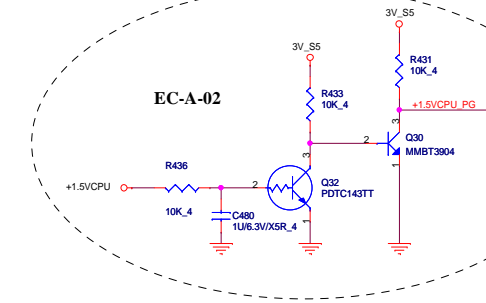
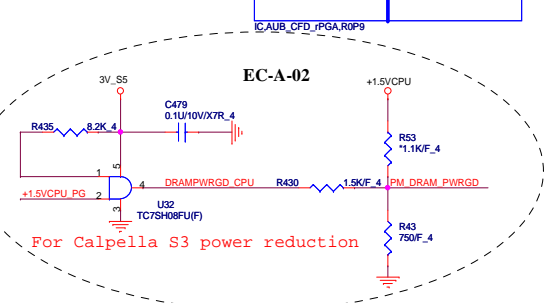
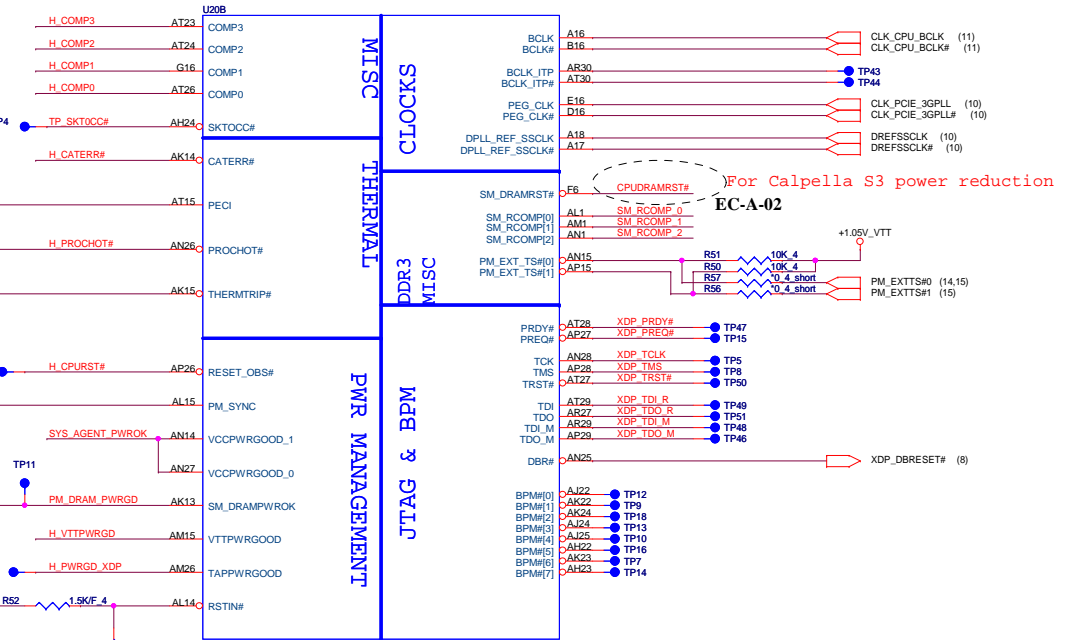
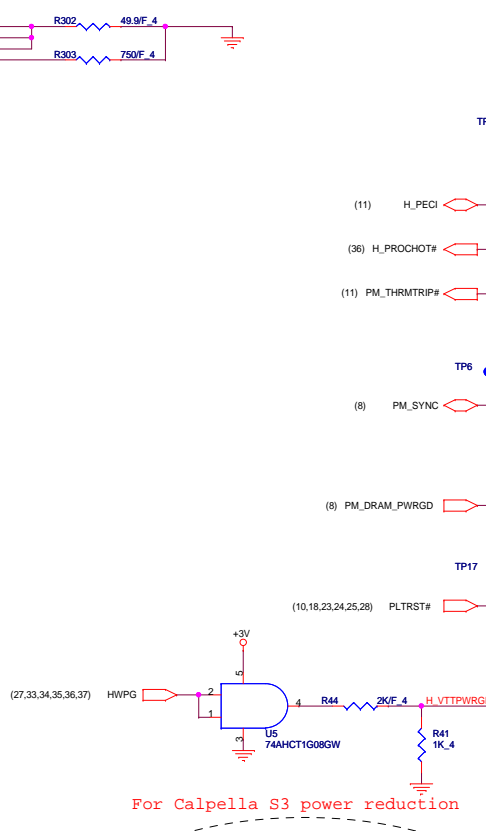
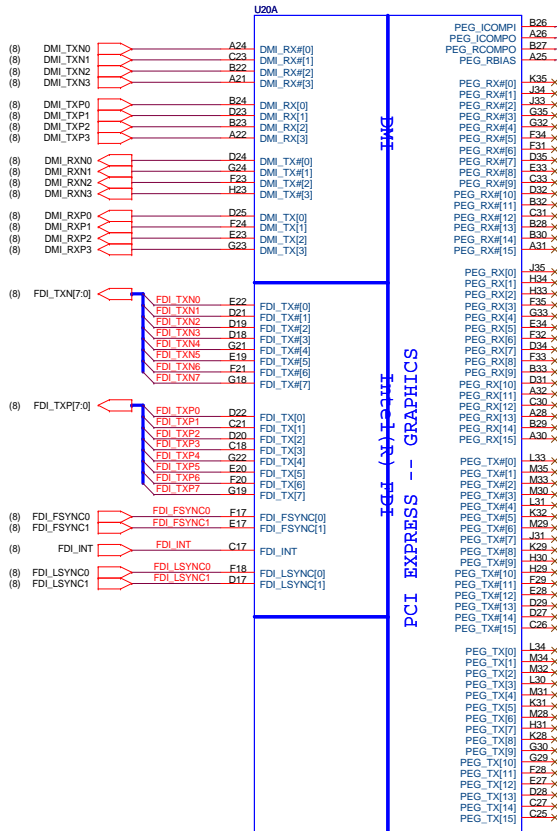
	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz



# AUBURNDALE PROCESSOR (DMI,PEG,FDI)

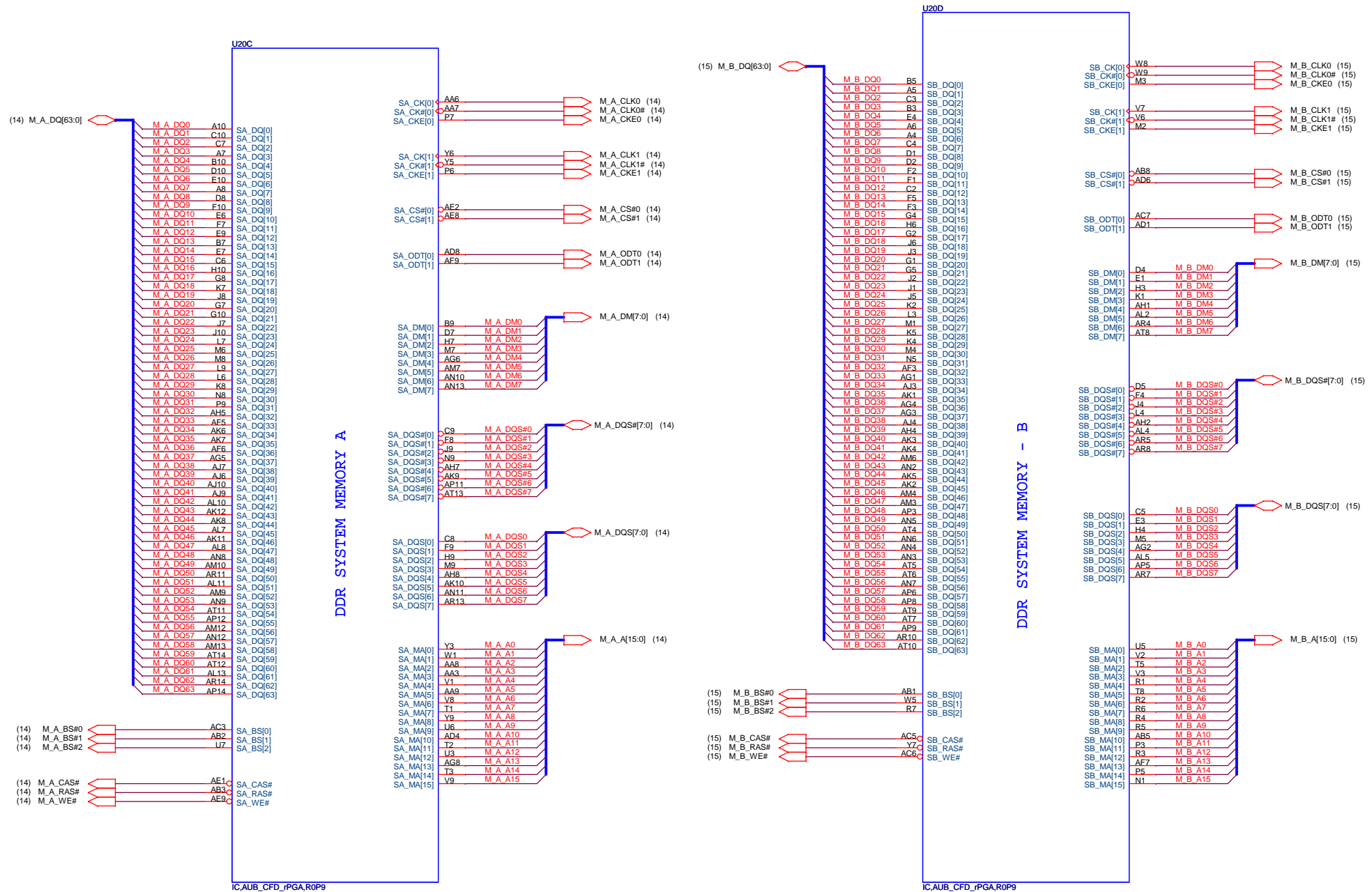
(3,6,8,9,10,11,12,14,15,16,17,19,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36)  
(3,6,8,9,10,11,12,18,30,31,34,36,37) +1.05V\_VTT  
(14,15,31,33) 1.5VSUS  
(9,16,18,27,28,29,31,32,35,37) 3VPCU

04



# AUBURNDALE PROCESSOR (DDR3)

05

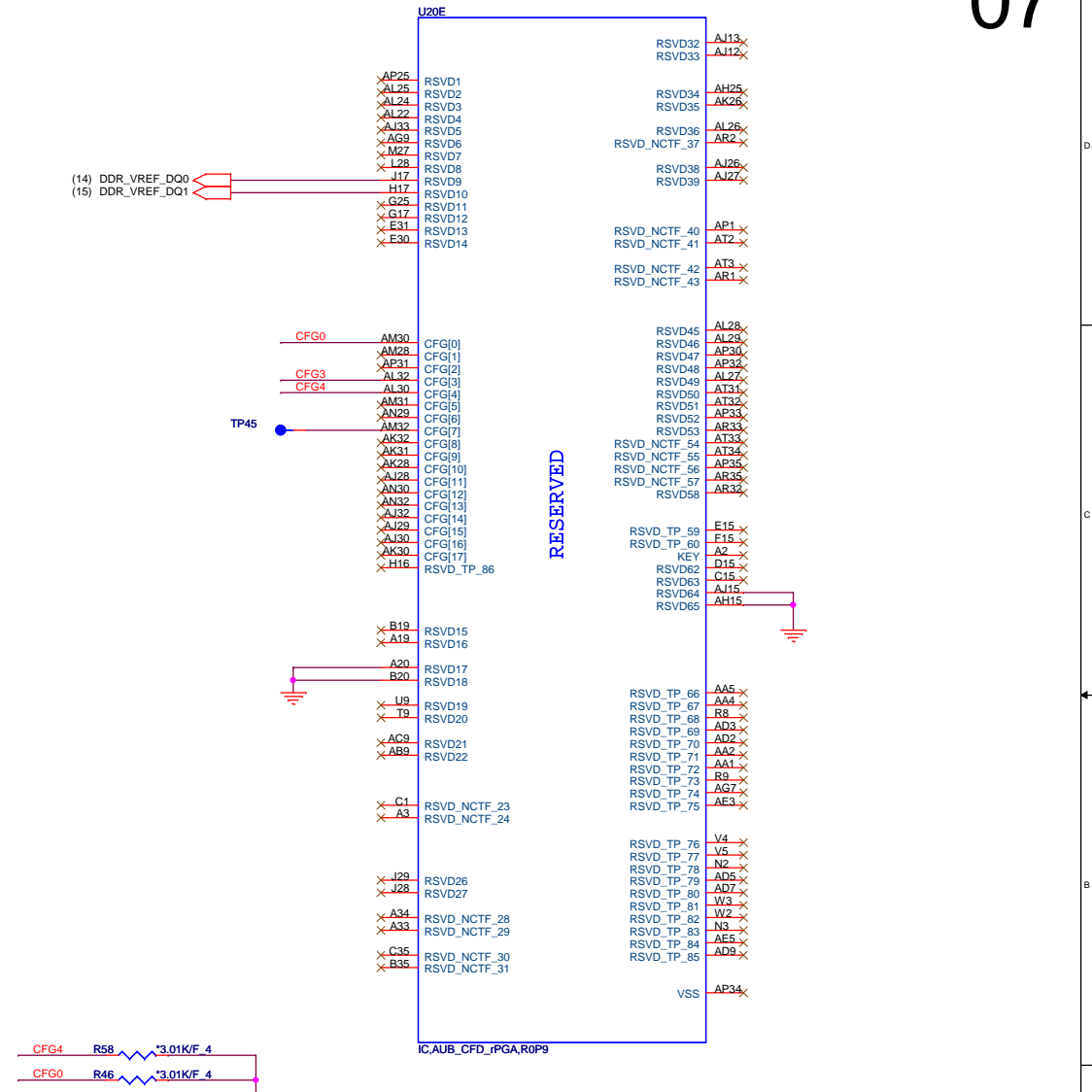
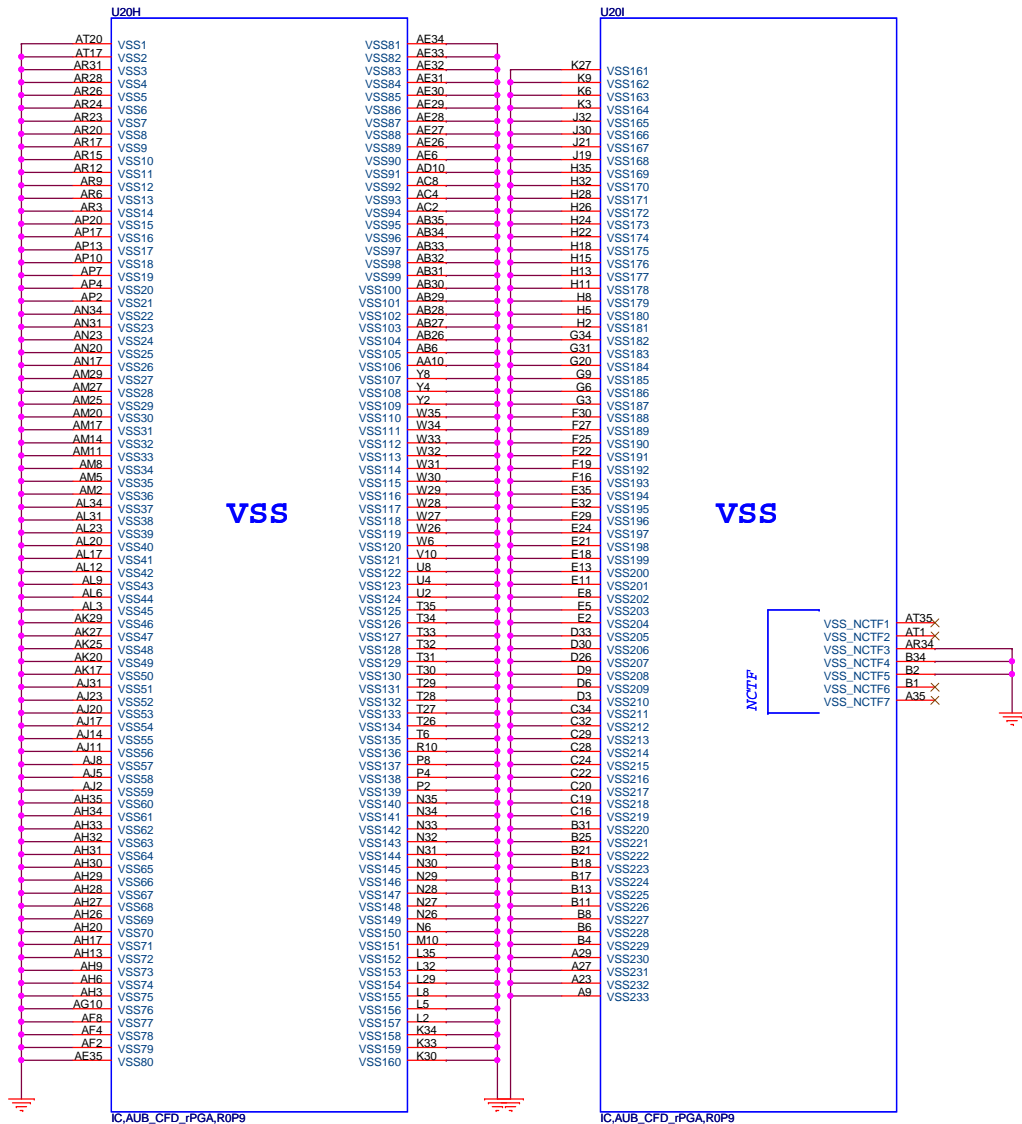




# AUBURNDALE PROCESSOR (GND)

# AUBURNDALE PROCESSOR( RESERVED, CFG)

07



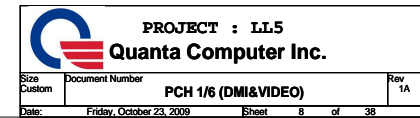
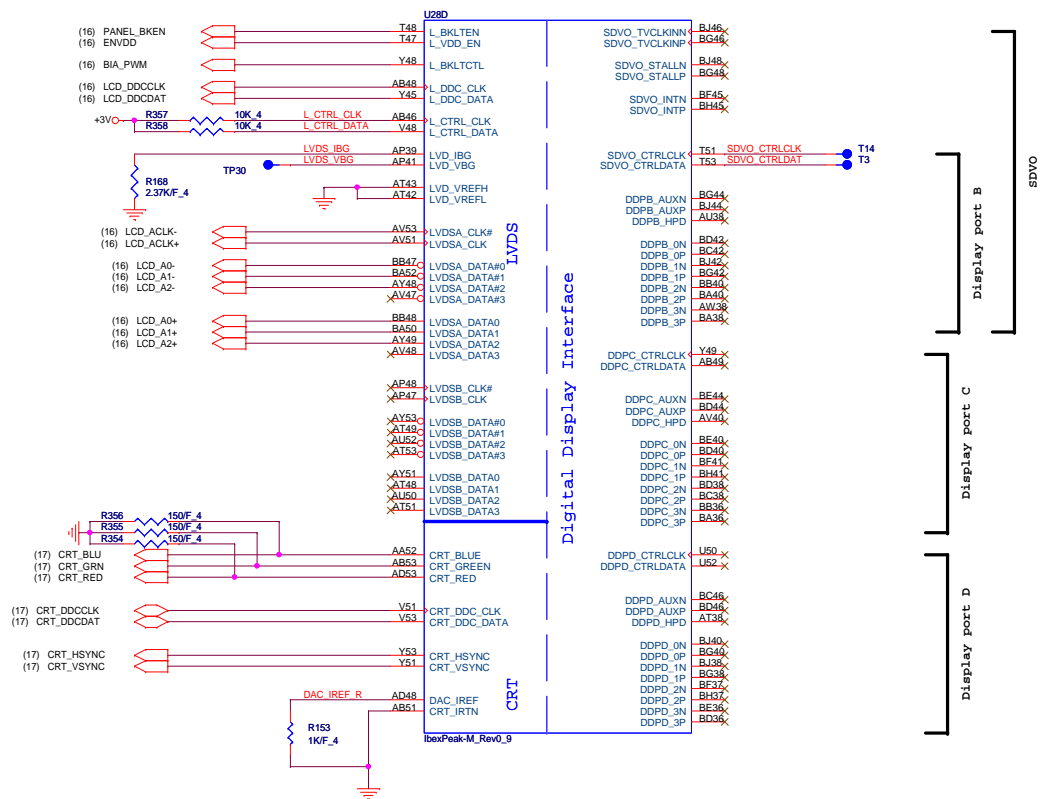
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

**PROJECT : LL5**  
**Quanta Computer Inc.**

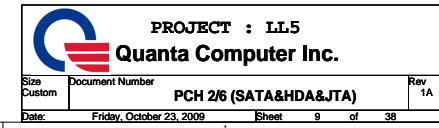
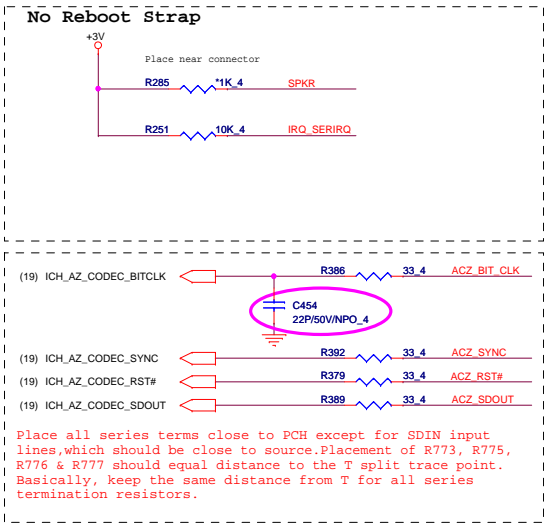
Size Custom	Document Number	Rev 1A
<b>PROCESSOR 4/4(GND)</b>		
Date: Friday, October 23, 2009	Sheet 7 of 38	



## IBEX PEAK-M (LVDS,DDI)





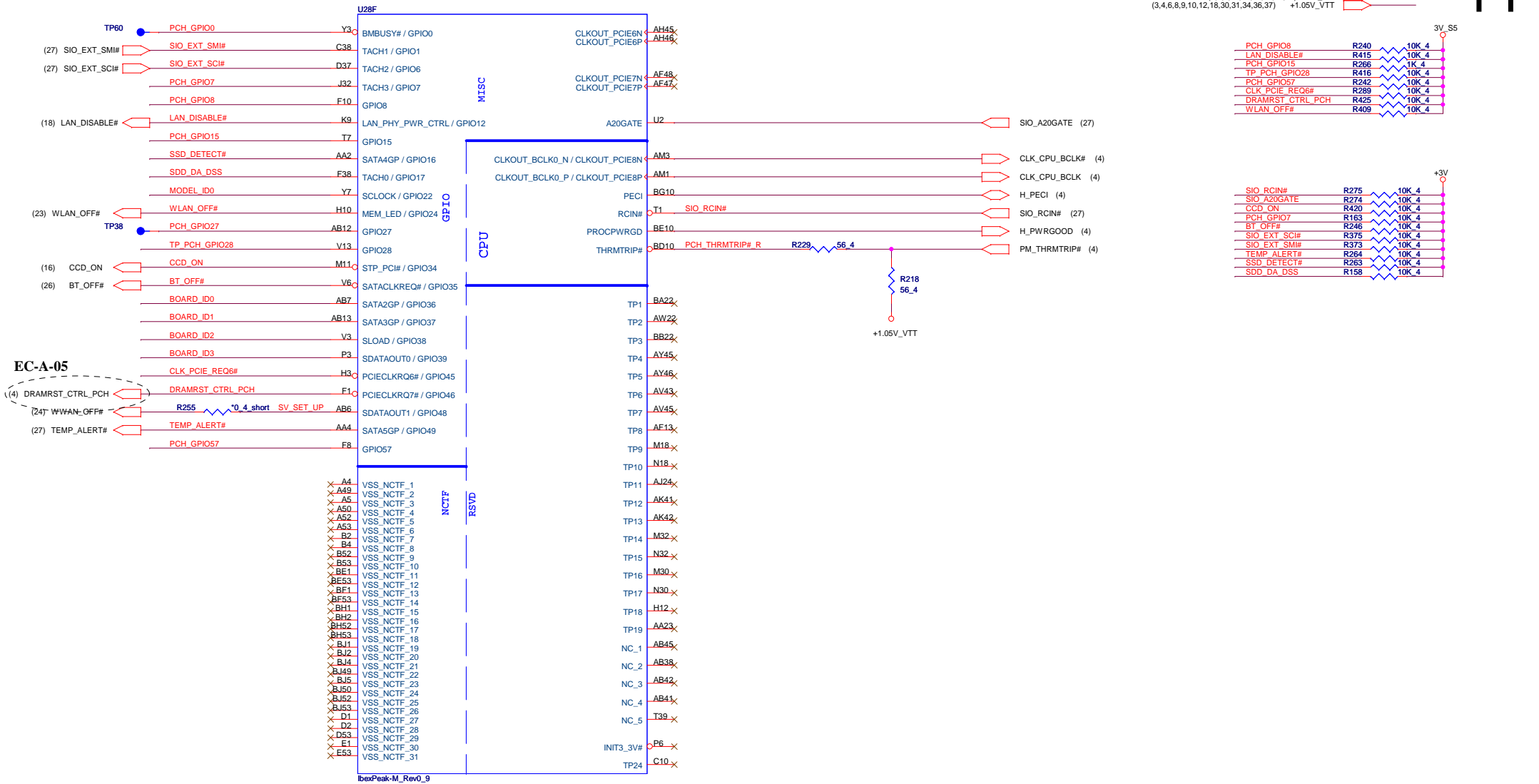




# IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)

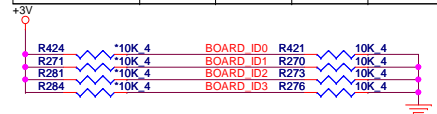
(3,4,6,8,9,10,12,14,15,16,17,19,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36) +3V  
(4,8,9,10,12,18,23,30,31) 3V\_S5  
(3,4,6,8,9,10,12,18,30,31,34,36,37) +1.05V\_VTT

11



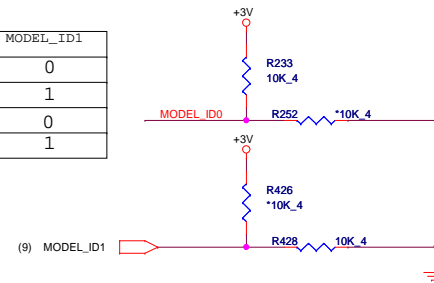
## Board ID

Board ID For Function	ID3 GPIO39	ID2 GPIO38	ID1 GPIO37	ID0 GPIO36
SDV	0	0	0	0
SIV	0	0	0	1
SIT	0	0	1	0
SVT	0	0	1	1
SOVP	0	1	0	0



## Model ID

Model ID	MODEL_ID0	MODEL_ID1
Default	0	0
LL3/LL3A	0	1
LL5/LL5A	1	0
	1	1

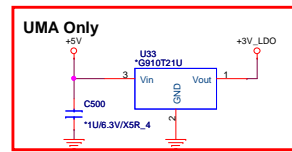


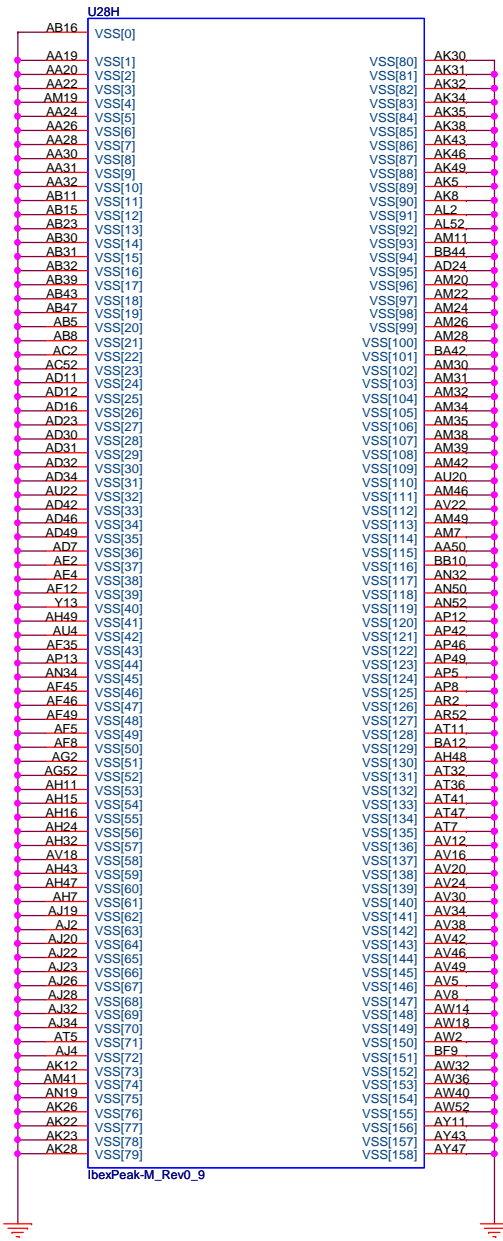
SV\_SET\_UP 1-X High = Strong (Default)

**PROJECT : LL5**  
**Quanta Computer Inc.**

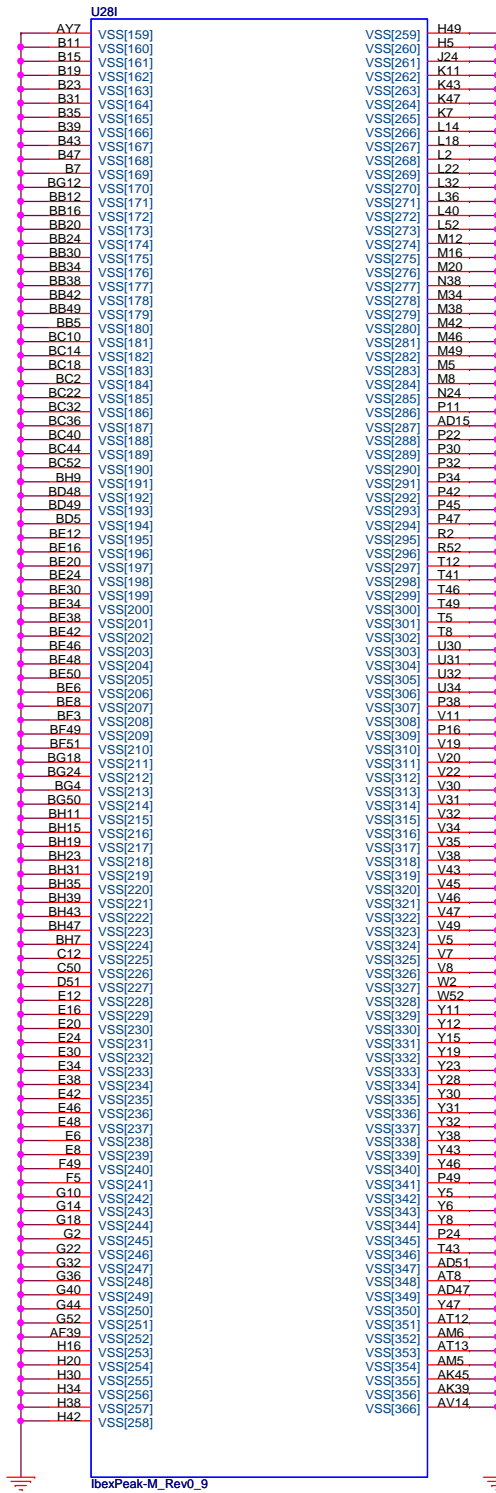
Size Custom Document Number **PCH 4/6 (GPIO)** Rev 1A

Date: Friday, October 23, 2009 Sheet 11 of 38

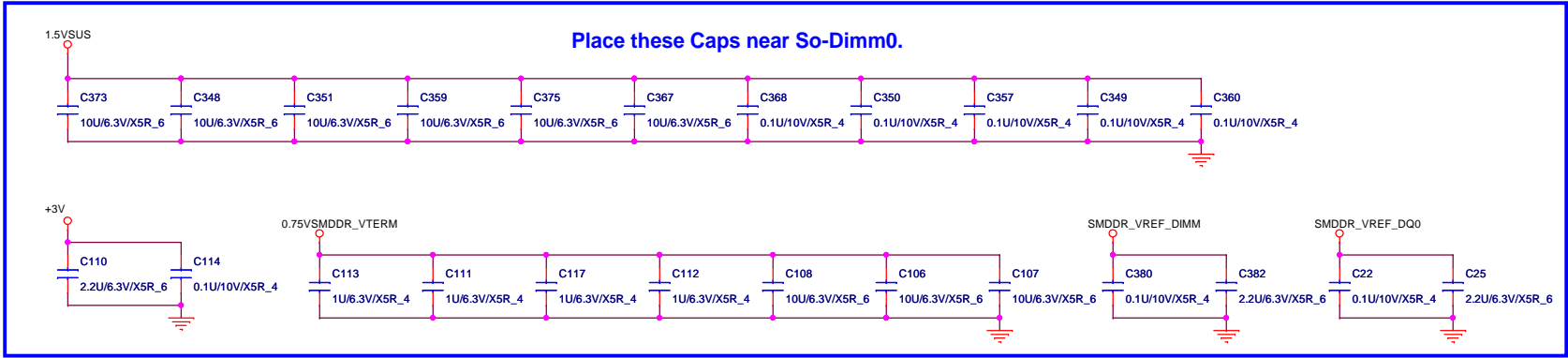
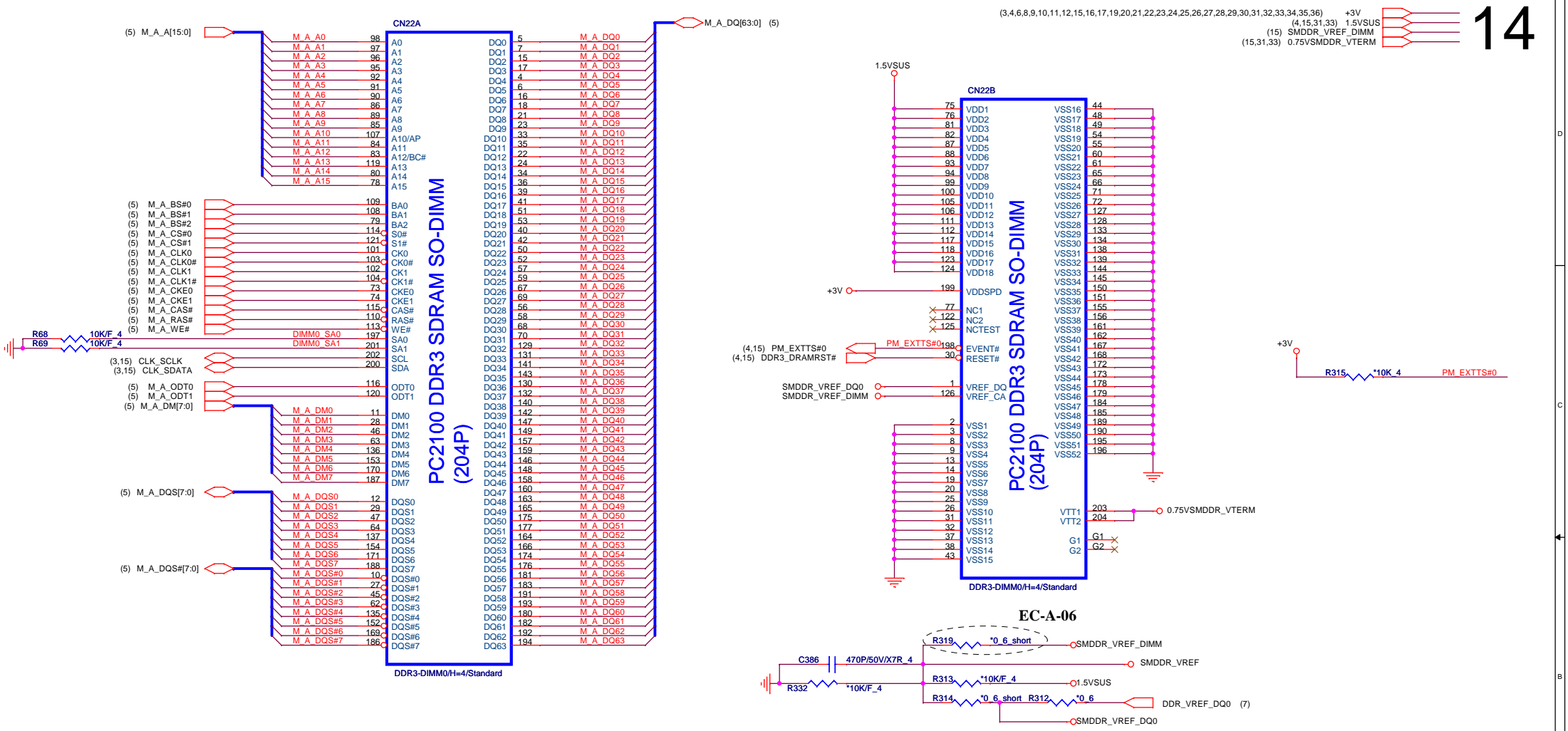




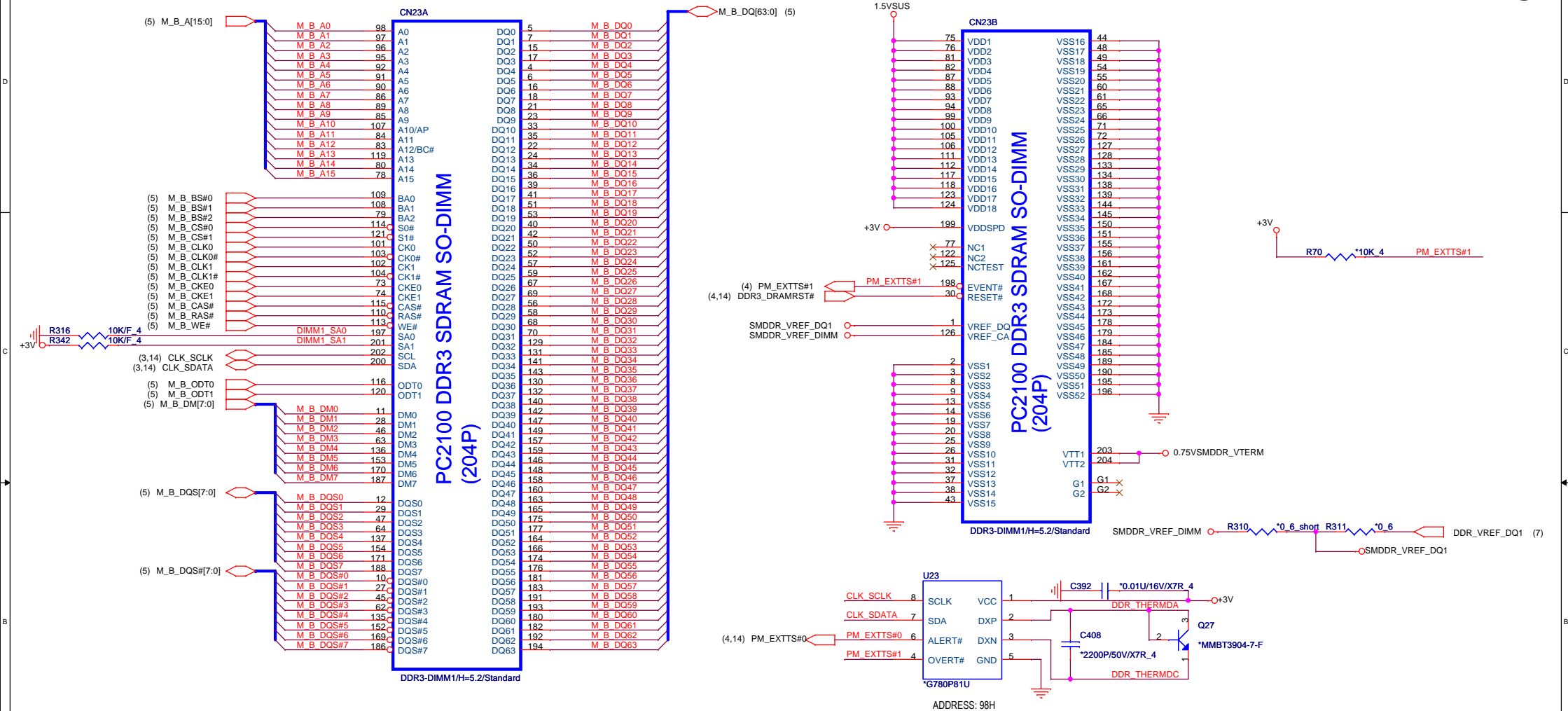
ibexPeak-M\_Rev0\_9



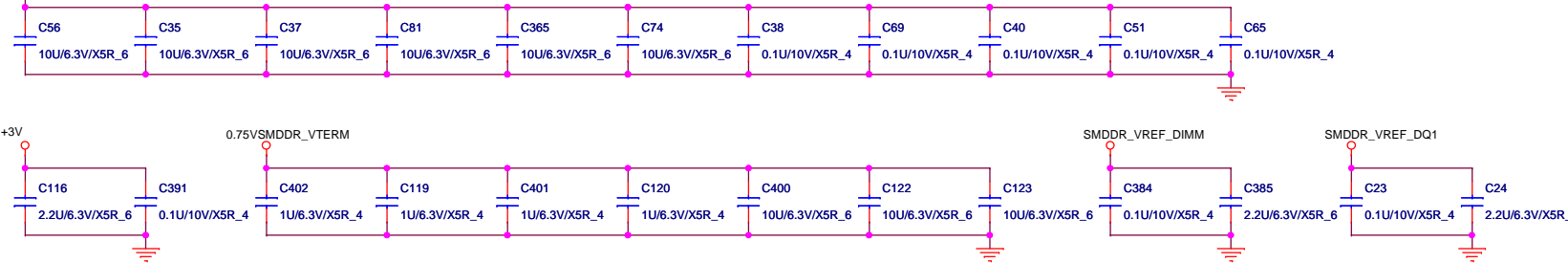
ibexPeak-M\_Rev0\_9



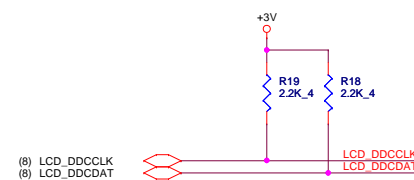
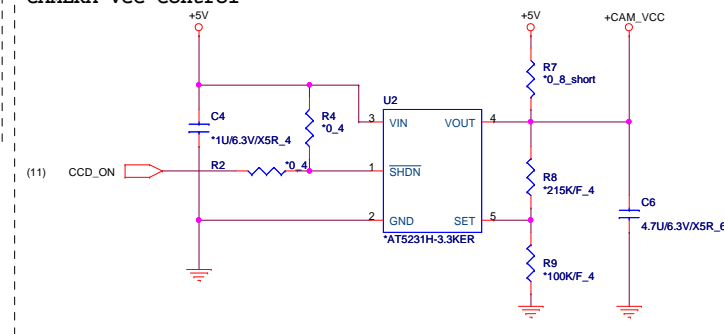
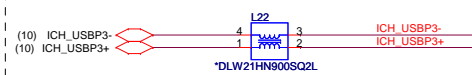
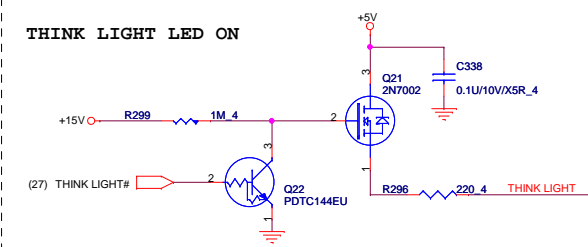
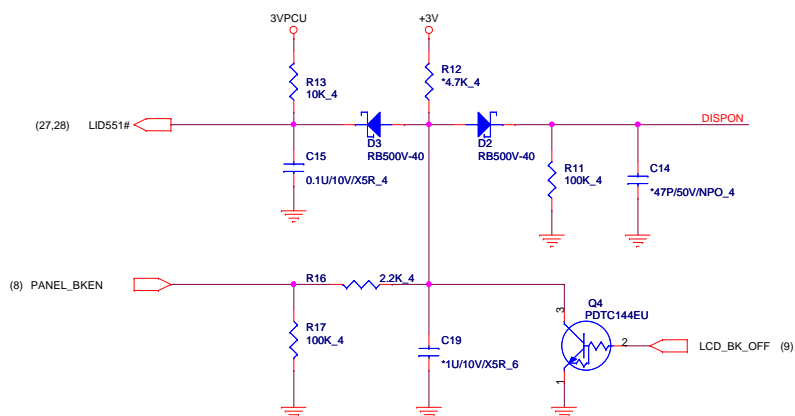
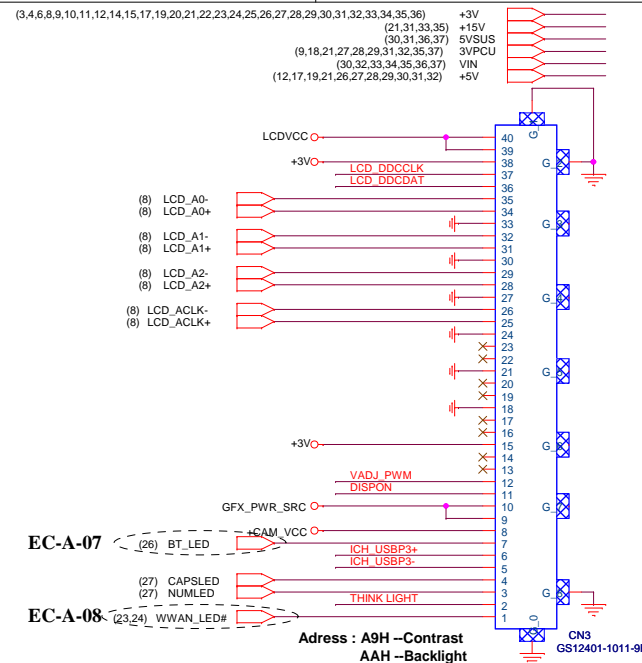


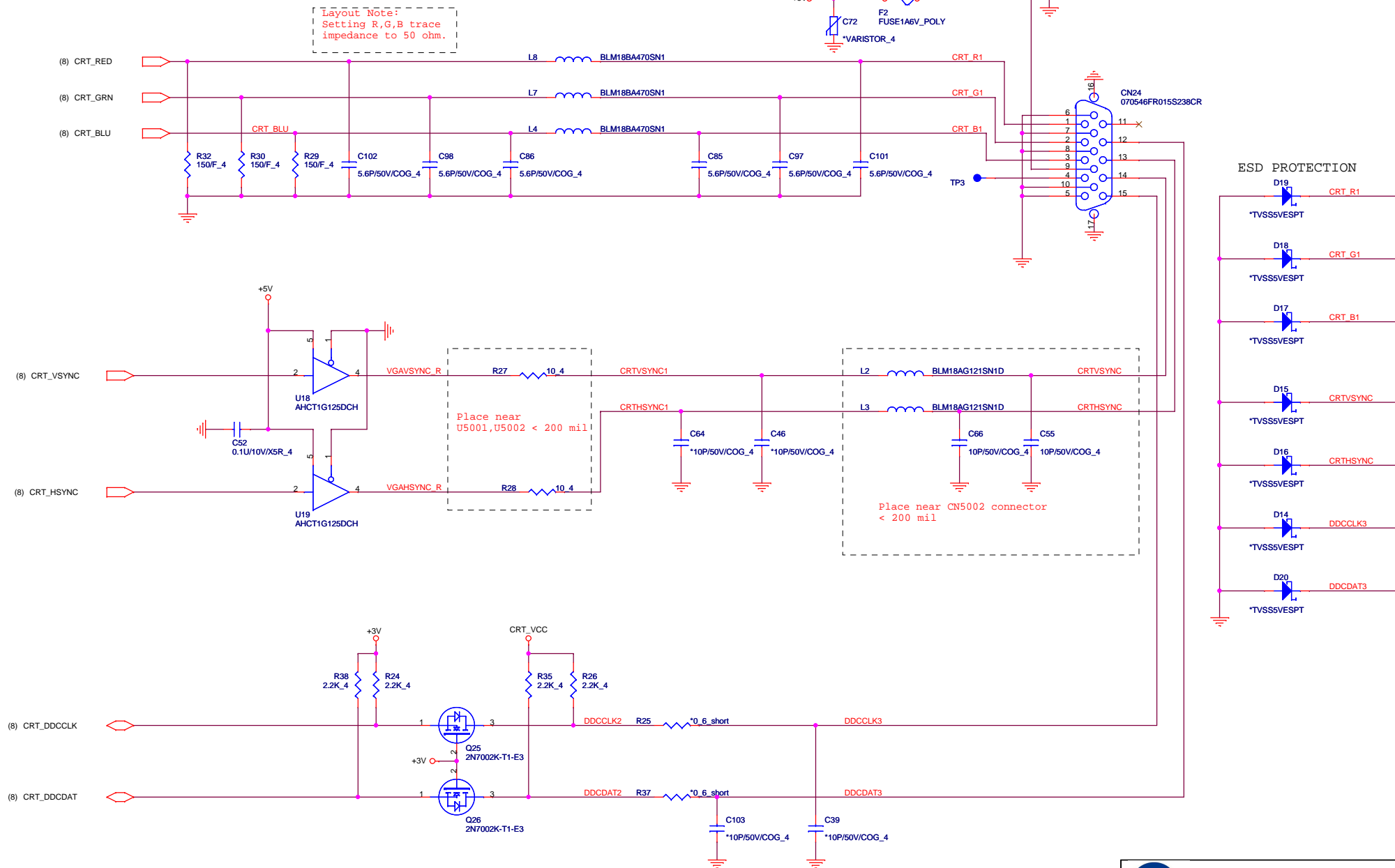


Place these Caps near So-Dimm1.

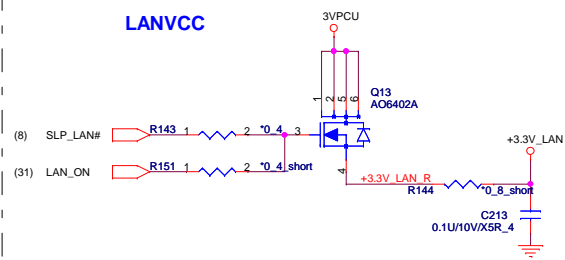




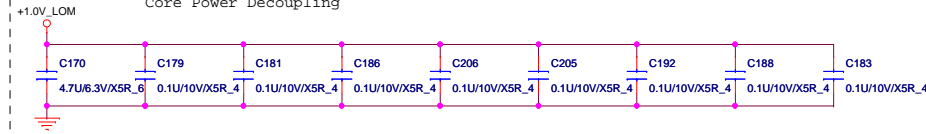




## LANVCC

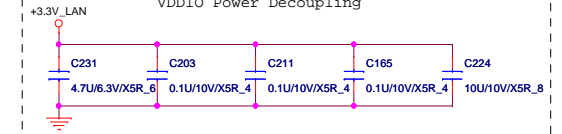


## Core Power Decoupling

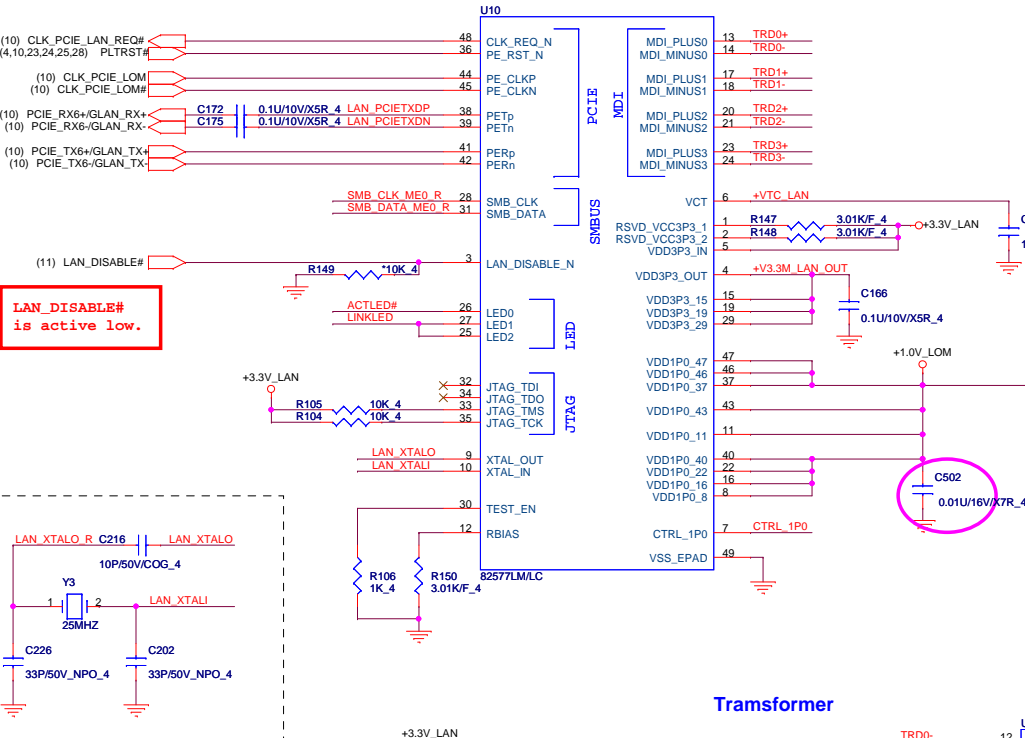
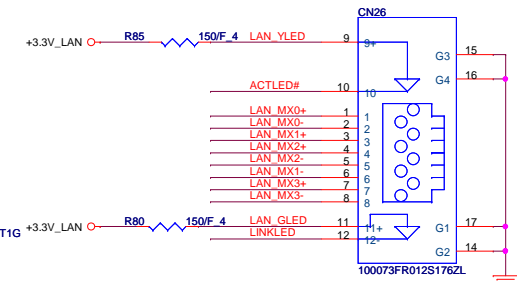


(4,8,9,10,11,12,23,30,31) 3V\_S5  
(3,4,6,8,9,10,11,12,30,31,34,36,37) +1.05V\_VTT

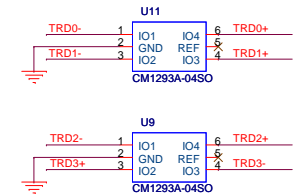
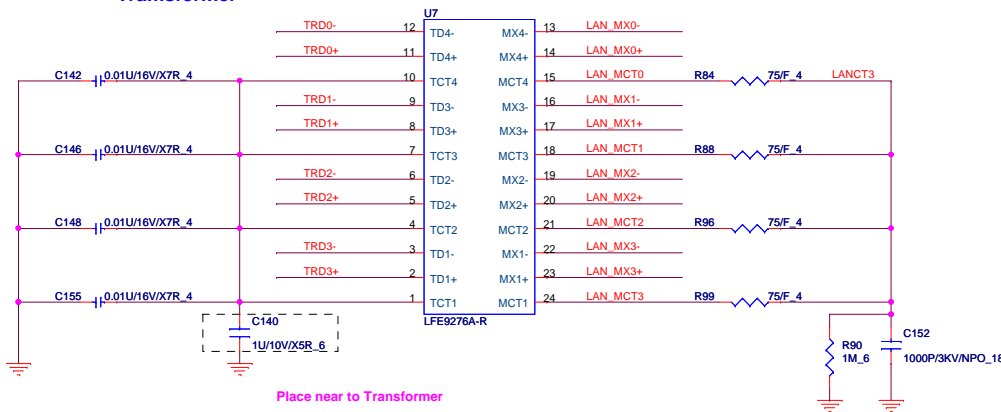
## VDDIO Power Decoupling

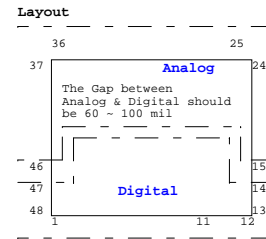


## RJ45 Connector



## Transformer





Sense_A	Sense_B	RES
Port_ A	Port_ E	39.2K
Port_ B	Port_ F	20K

The schematic diagram illustrates the microphone input circuitry. External microphones (EXT\_MIC\_L, EXT\_MIC\_R) are connected through resistors R182 and R159 (0.6 ohms) to the ADC inputs. A stereo microphone (CN13) is also connected, with its SENSE\_MIC signal going to MIC1\_VREF and its MIC\_JACK signal going to MIC1\_VREF. The circuit includes capacitors C225 and C252 (100pF/50V/NPO\_4) and inductors L17 and L16 (BLM188BD601SN1D\_0.2A). A dashed box highlights the 'Stereo MIC' section.

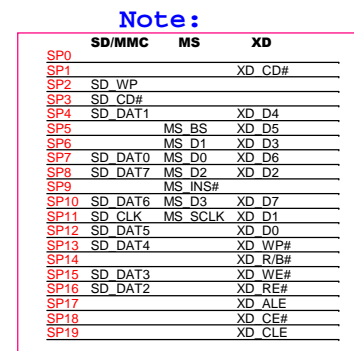
[illegible]

The diagram shows three resistors connected to a common ground. The first resistor is R258, connected to AGND. The second resistor is R156, connected to AGND. The third resistor is R443, connected to AGND. All three resistors are connected to a common ground symbol. The resistor R443 is circled in red.

ICH AZ CODEC RST#  
 ICH AZ CODEC SYNC  
 ICH AZ CODEC BITCLK  
 ICH AZ CODEC SDOUT

C306  
 \*22P/50V/NPO\_4  
 C298  
 \*10P/50V/COG\_4  
 C273  
 \*22P/50V/NPO\_4  
 C272  
 \*22P/50V/NPO\_4

Layout Note:  
 Place close to  
 Audio Codec.



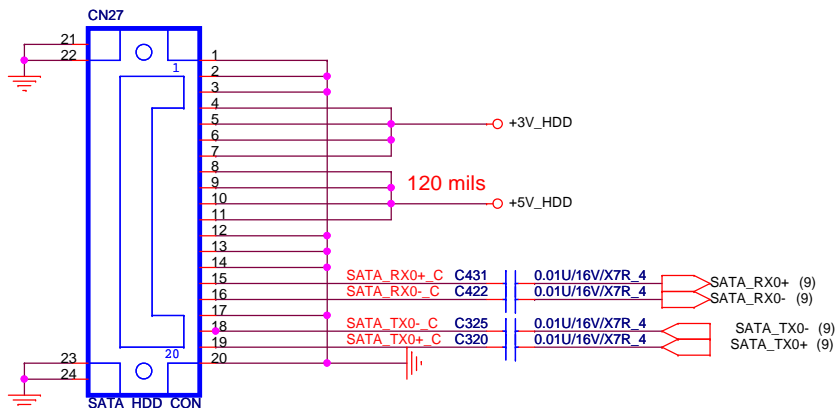
Timing diagram showing the relationship between SP signals and various data/control signals. The diagram illustrates that SP signals are sampled on the rising edge of the clock (indicated by blue zigzag lines). The signals shown are:

- SP7**: R124, R128, MS\_DATA0, SD\_DATA0, XD-D6
- SP6**: R127, R126, MS\_DATA1, XD-D3
- SP16**: R109, R110, SD\_DATA2, XD-RE#
- SP5**: R134, R139, MS\_BS, XD-D5
- SP15**: R108, R107, SD\_DAT3, XD\_WE
- SP11**: R118, R117, SD\_CLK, MS\_CLK, XD-D1
- SP10**: R122, R121, MS\_DATA3, XD-D7
- SP4**: R135, R137, XD-D4, SD\_DAT1

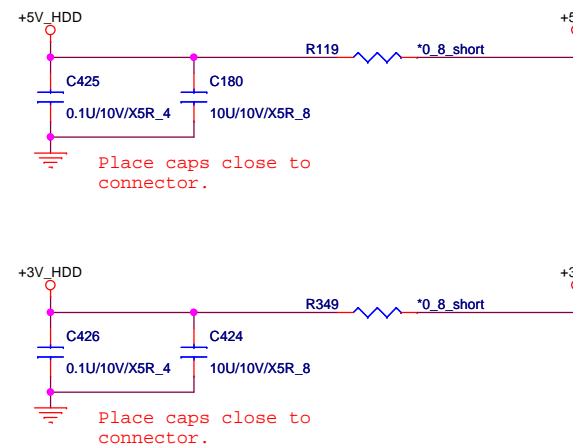
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# SATA-HDD CONNECTOR

21



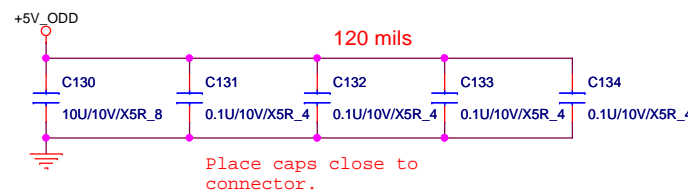
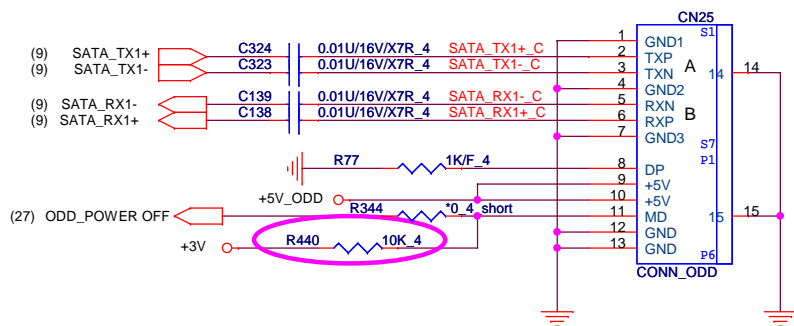
(3,4,6,8,9,10,11,12,14,15,16,17,19,20,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36)  
(12,16,17,19,26,27,28,29,30,31,32)



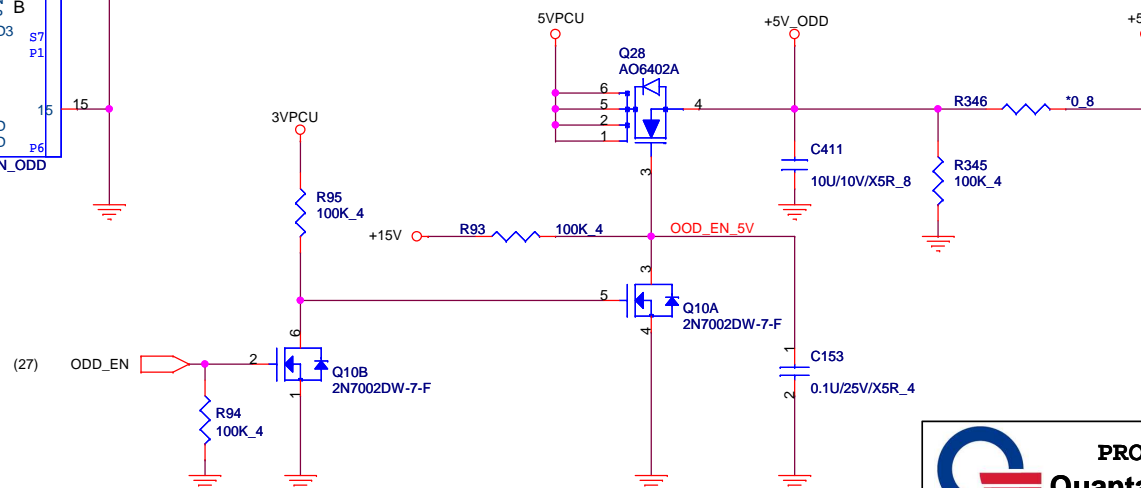
Place caps close to connector.

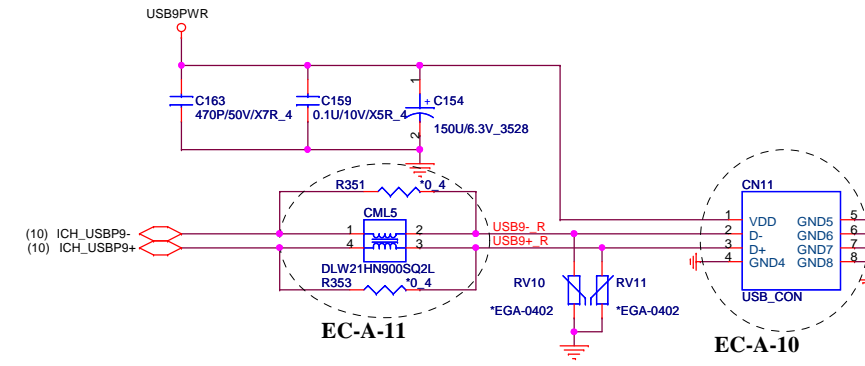
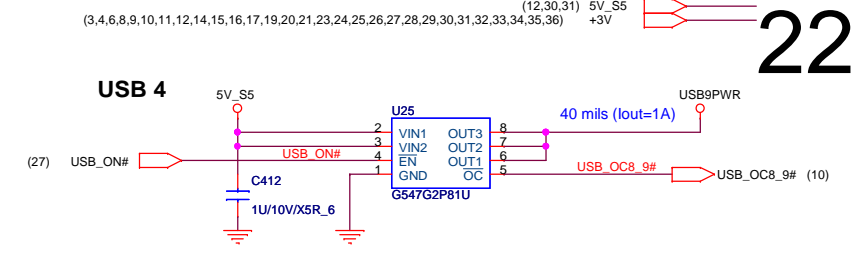
Place caps close to connector.

# SATA CD-ROM

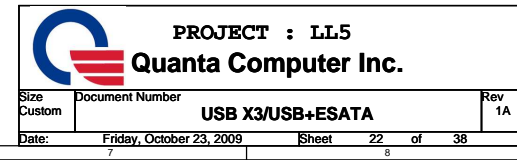


Place caps close to connector.





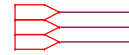
## USB + E-SATA



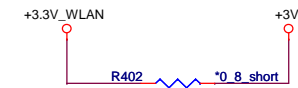
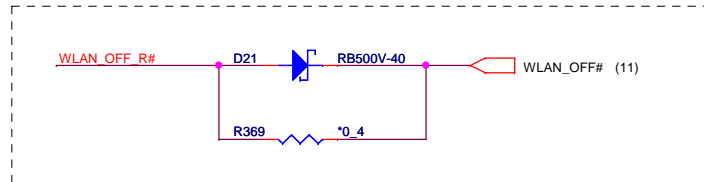
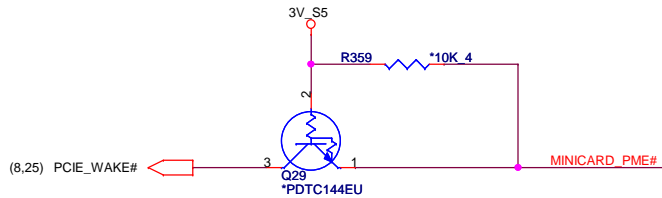
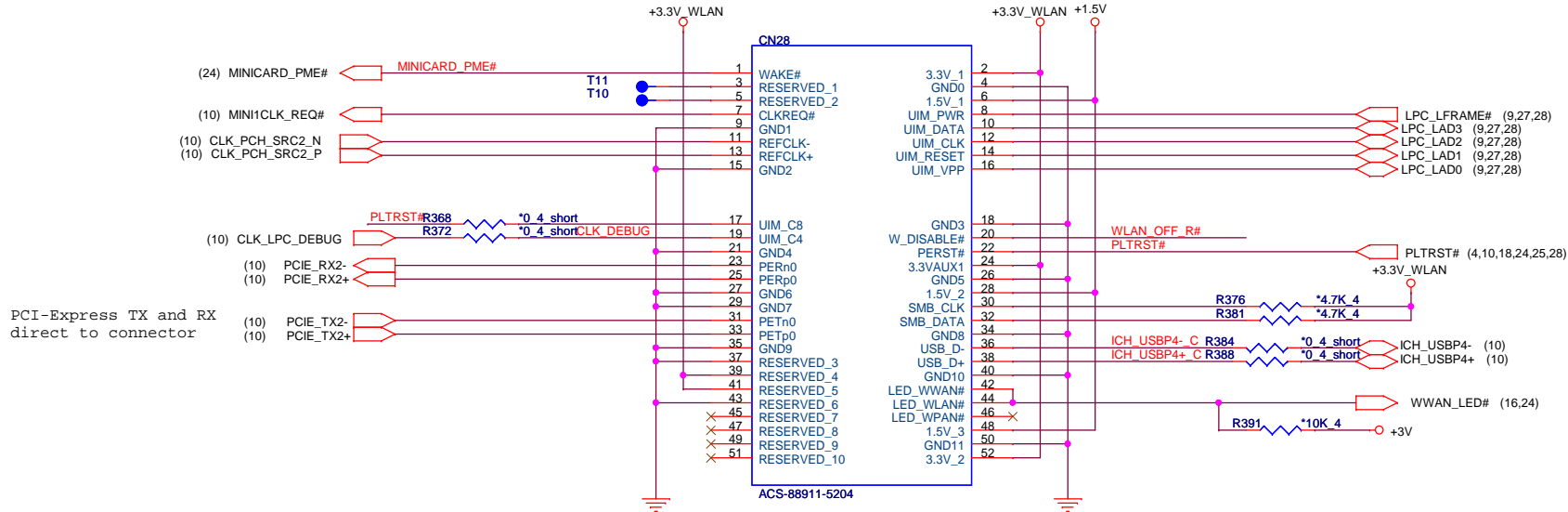


# MiniCard WLAN/WiMAX connector

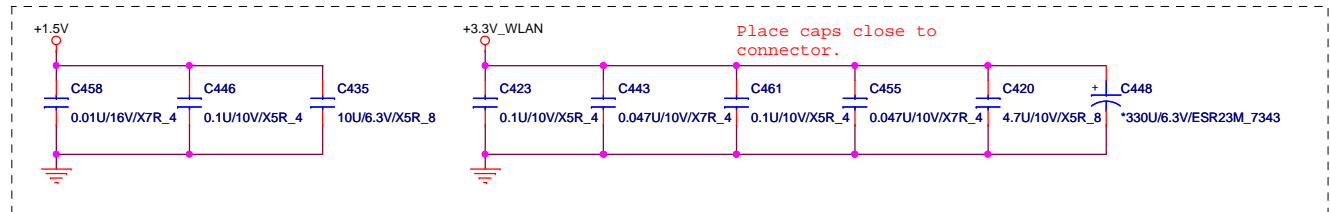
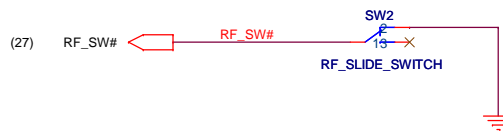
(3,4,6,8,9,10,11,12,14,15,16,17,19,20,21,22,24,25,26,27,28,29,30,31,32,33,34,35,36) +3V  
(3,24,25,33) +1.5V  
(16,30,32,33,34,35,36,37) VIN



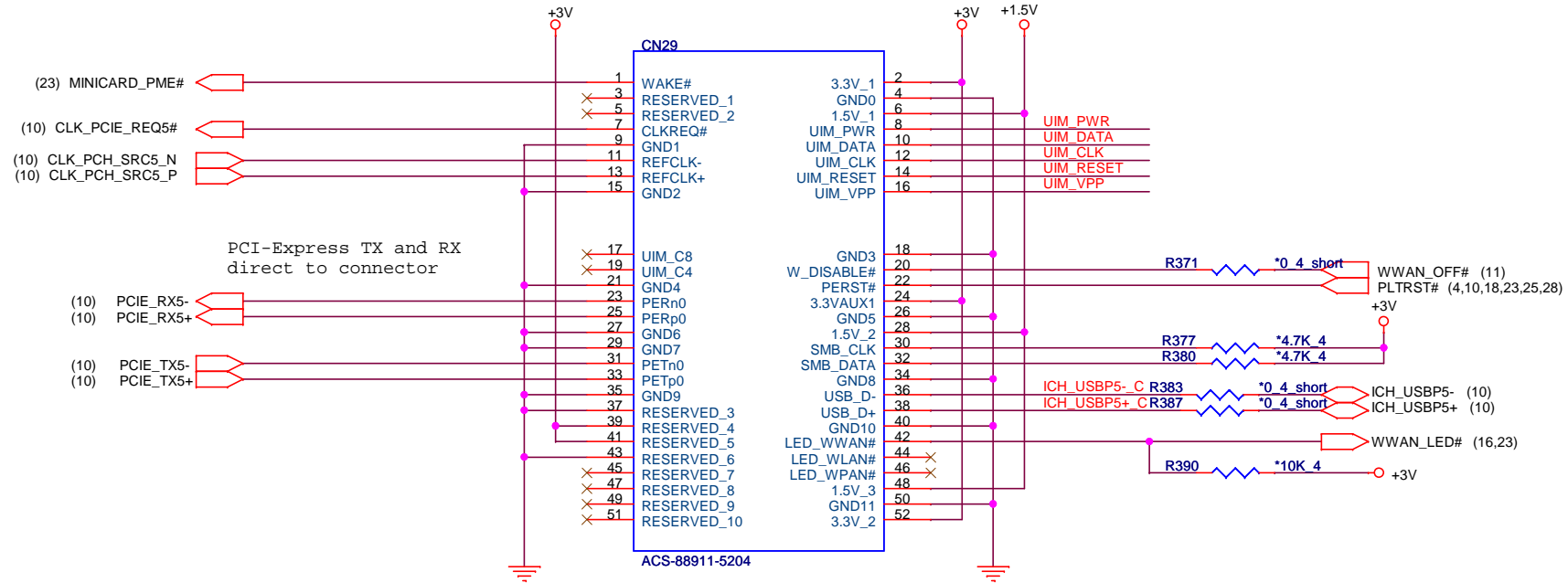
23



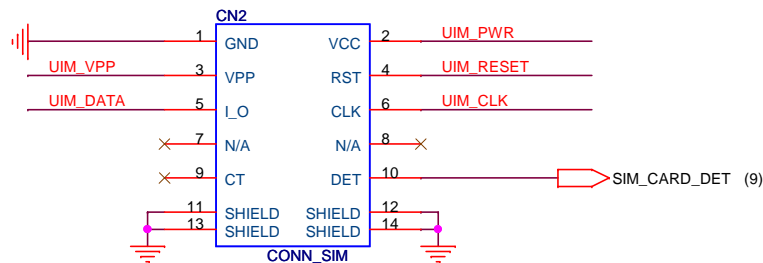
## RF ON/OFF SWITCH



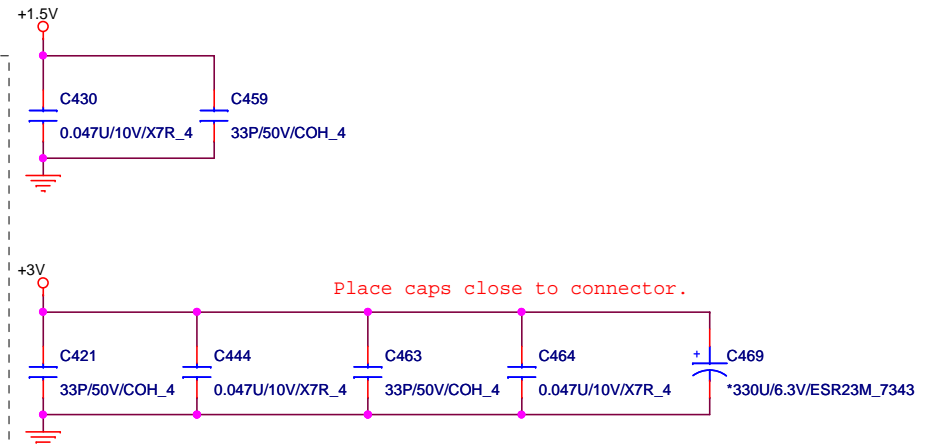
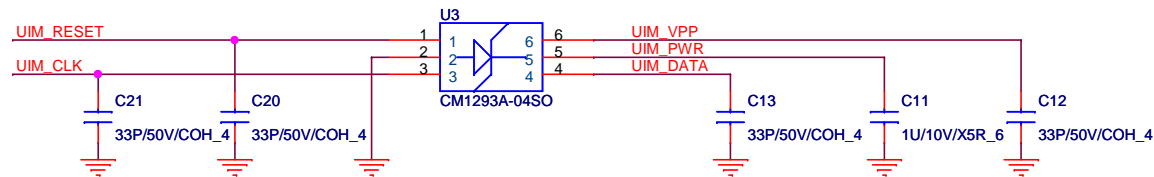
## MiniCard WWAN connector



## SIM Card CONN



**Layout Note:**  
UIM\_RESET, UIM\_CLK, UIM\_DATA routing as short as possible

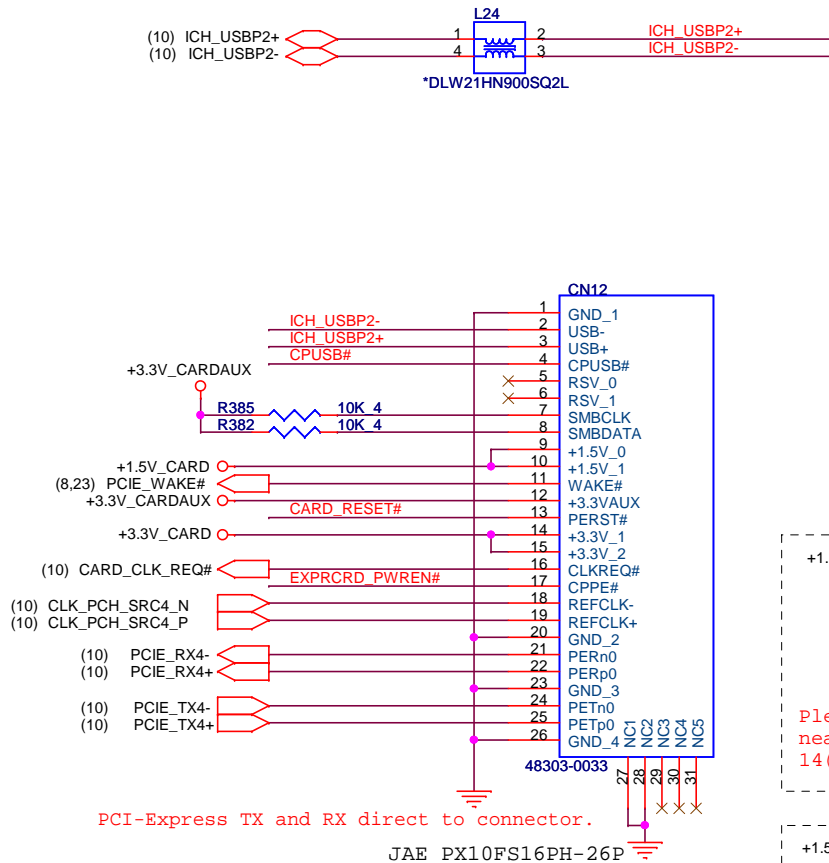


# Express Card

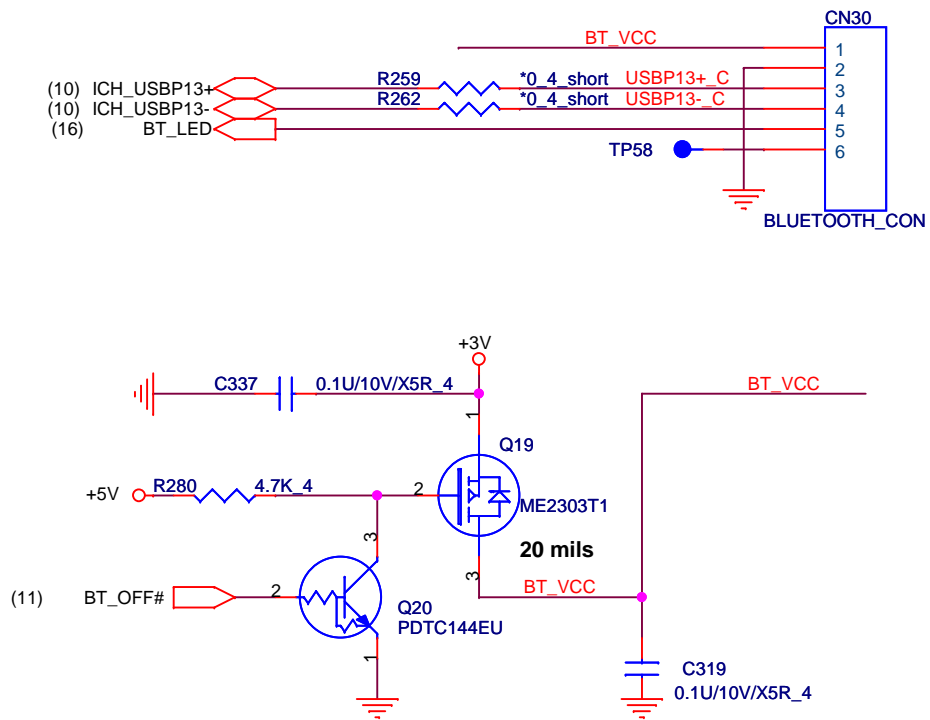
(3,4,6,8,9,10,11,12,14,15,16,17,19,20,21,22,23,24,26,27,28,29,30,31,32,33,34,35,36) +3V  
(3,23,24,33) +1.5V  
(27,31,37) 3VSUS

# 25

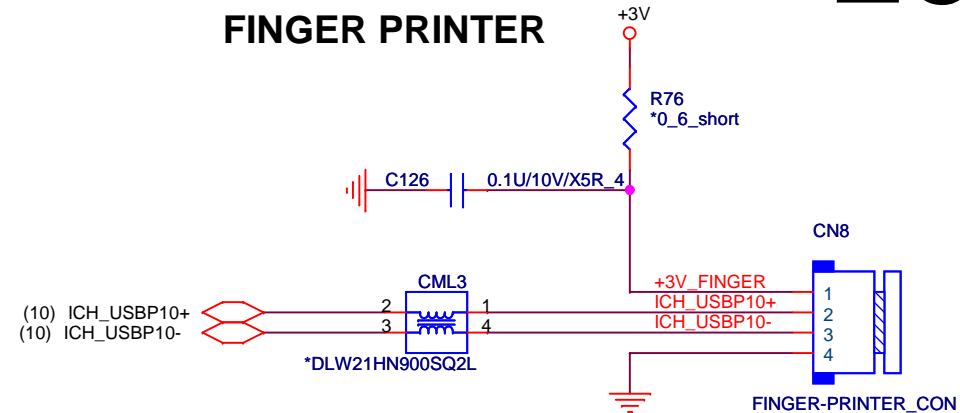
+1.5V\_CARD Max. 650mA, Average 500mA.  
+3.3V\_CARD Max. 1300mA, Average 1000mA.

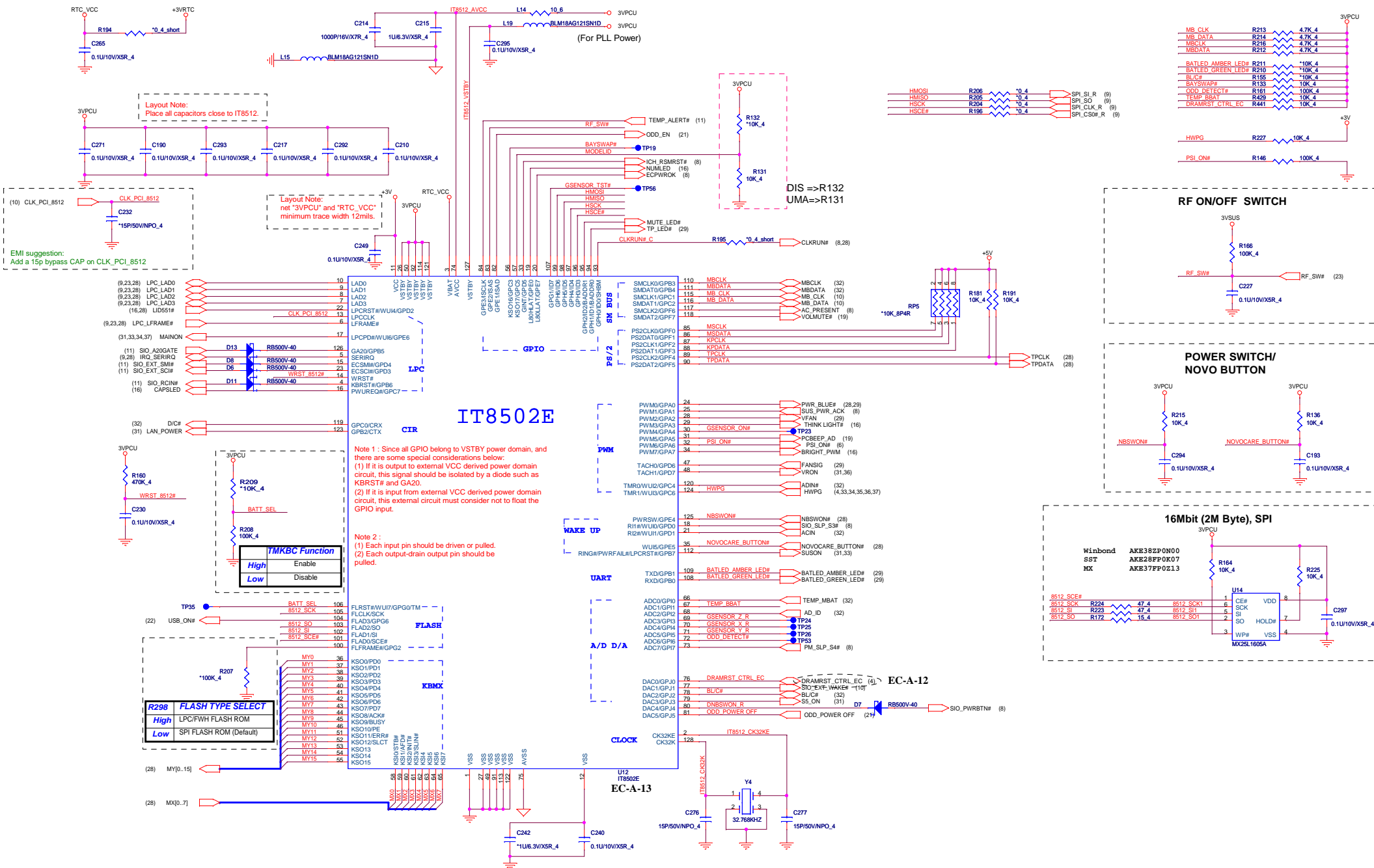


# BLUETOOTH

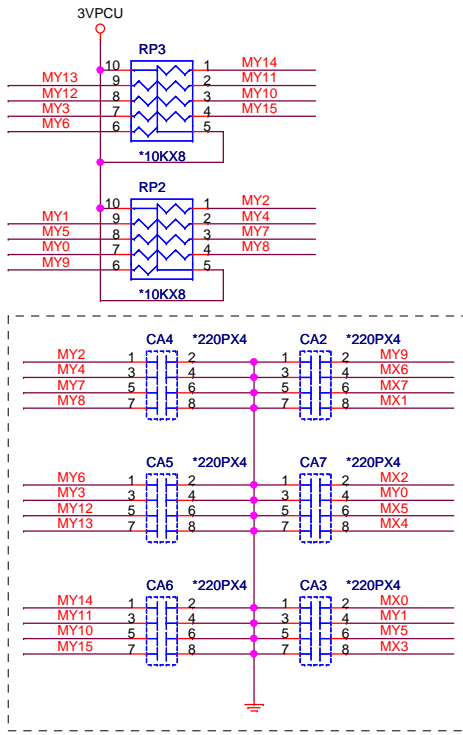
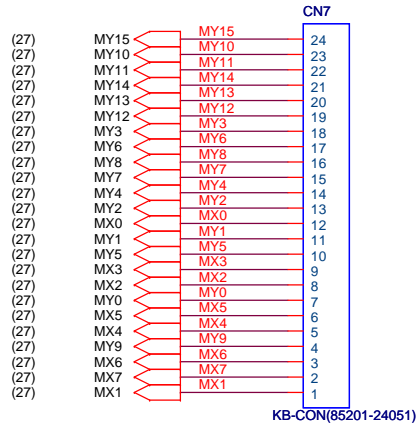


# FINGER PRINTER

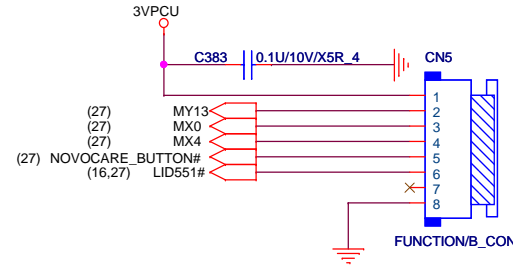




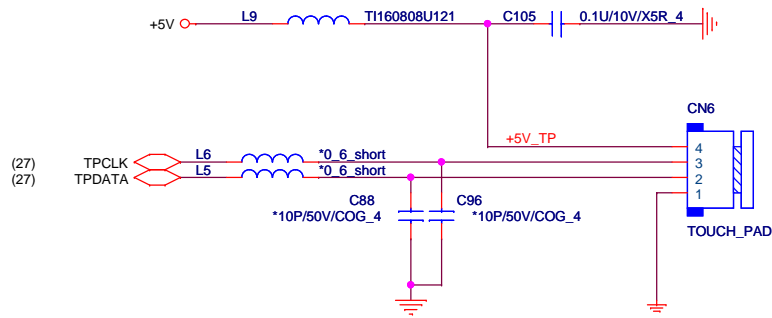
## KEYBOARD



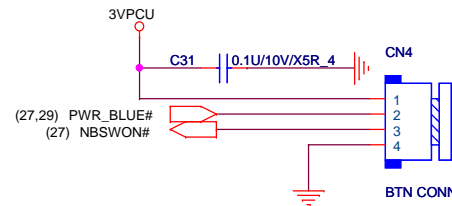
## FUNCTION BUTTON BOARD



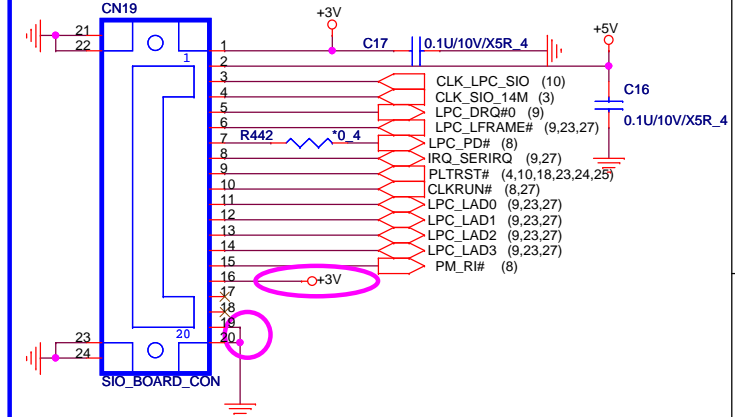
## TOUCH PAD



## POWER BUTTON BOARD



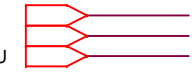
## SIO BOARD



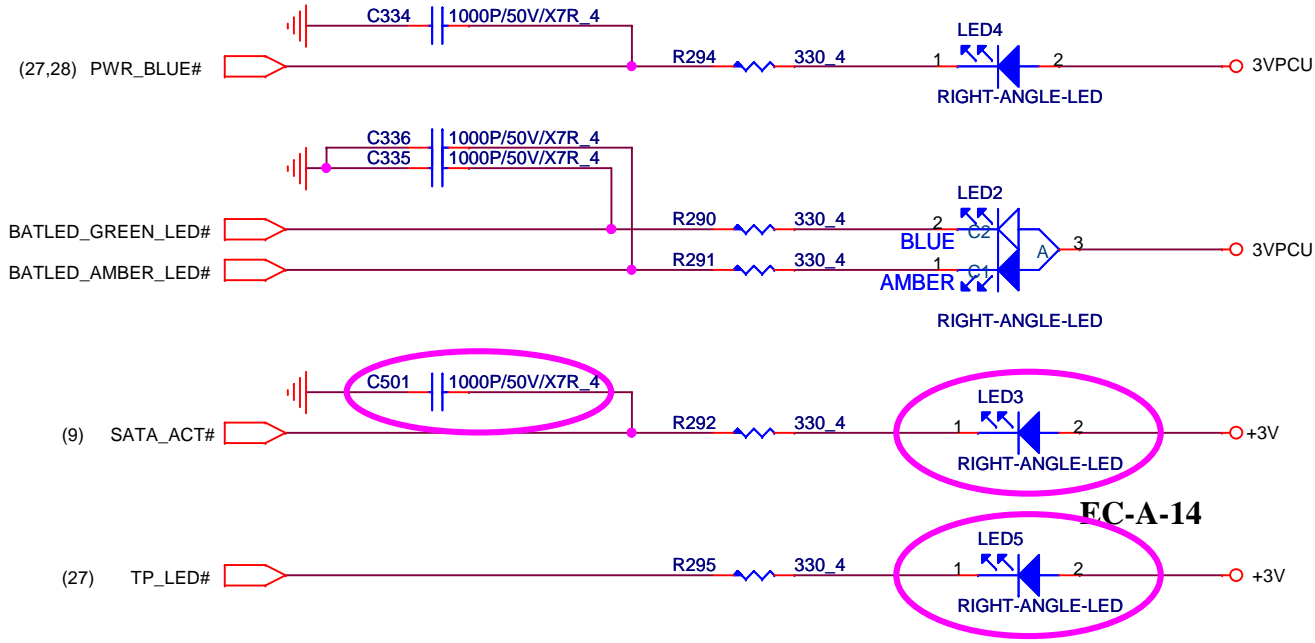
# LED

(3,4,6,8,9,10,11,12,14,15,16,17,19,20,21,22,23,24,25,26,27,28,30,31,32,33,34,35,36)  
(12,16,17,19,21,26,27,28,30,31,32)  
(9,16,18,21,27,28,31,32,35,37)

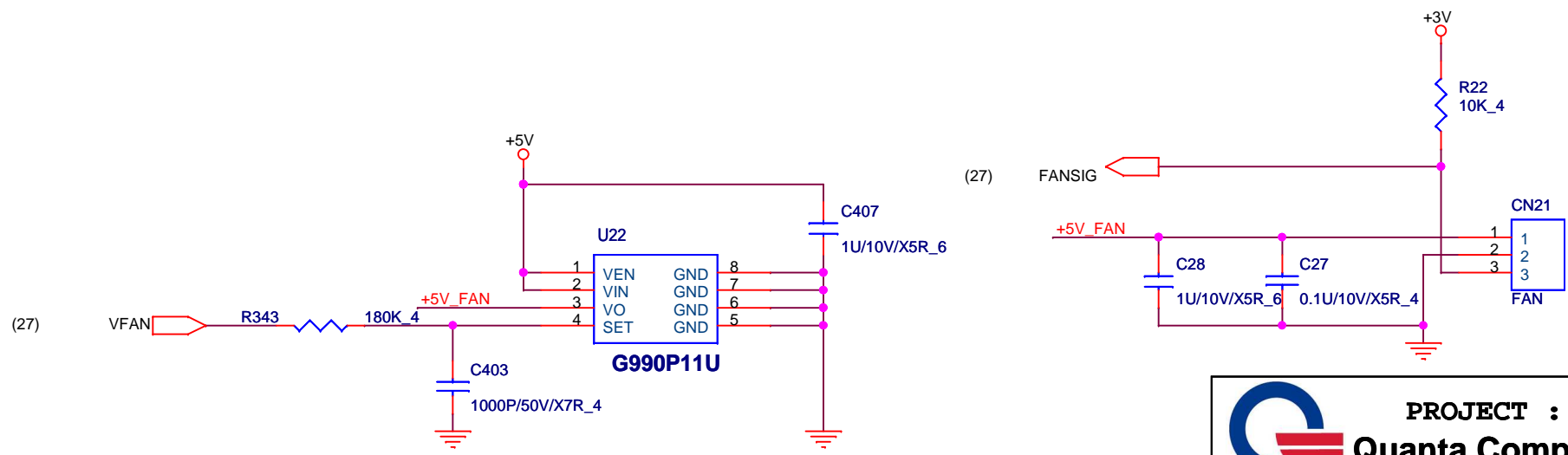
+3V  
+5V  
3VPCU




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# FAN CONTROL



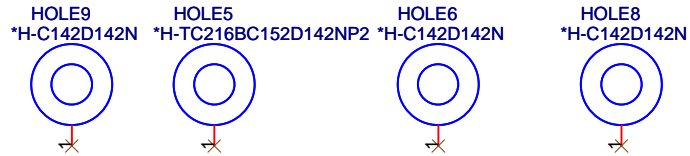


**PROJECT : LL5**  
**Quanta Computer Inc.**

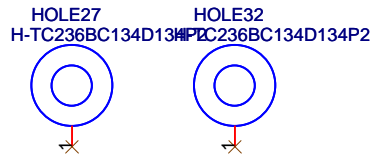
Size Custom	Document Number	Rev 1A
<b>LED/FAN</b>		
Date: Friday, October 23, 2009	Sheet 29 of 38	



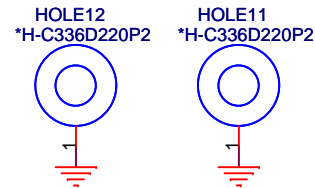
## Hole for CPU support



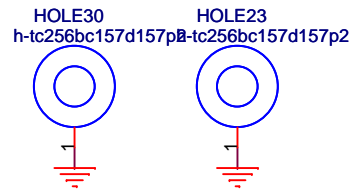
## Hole for PCH Thermal



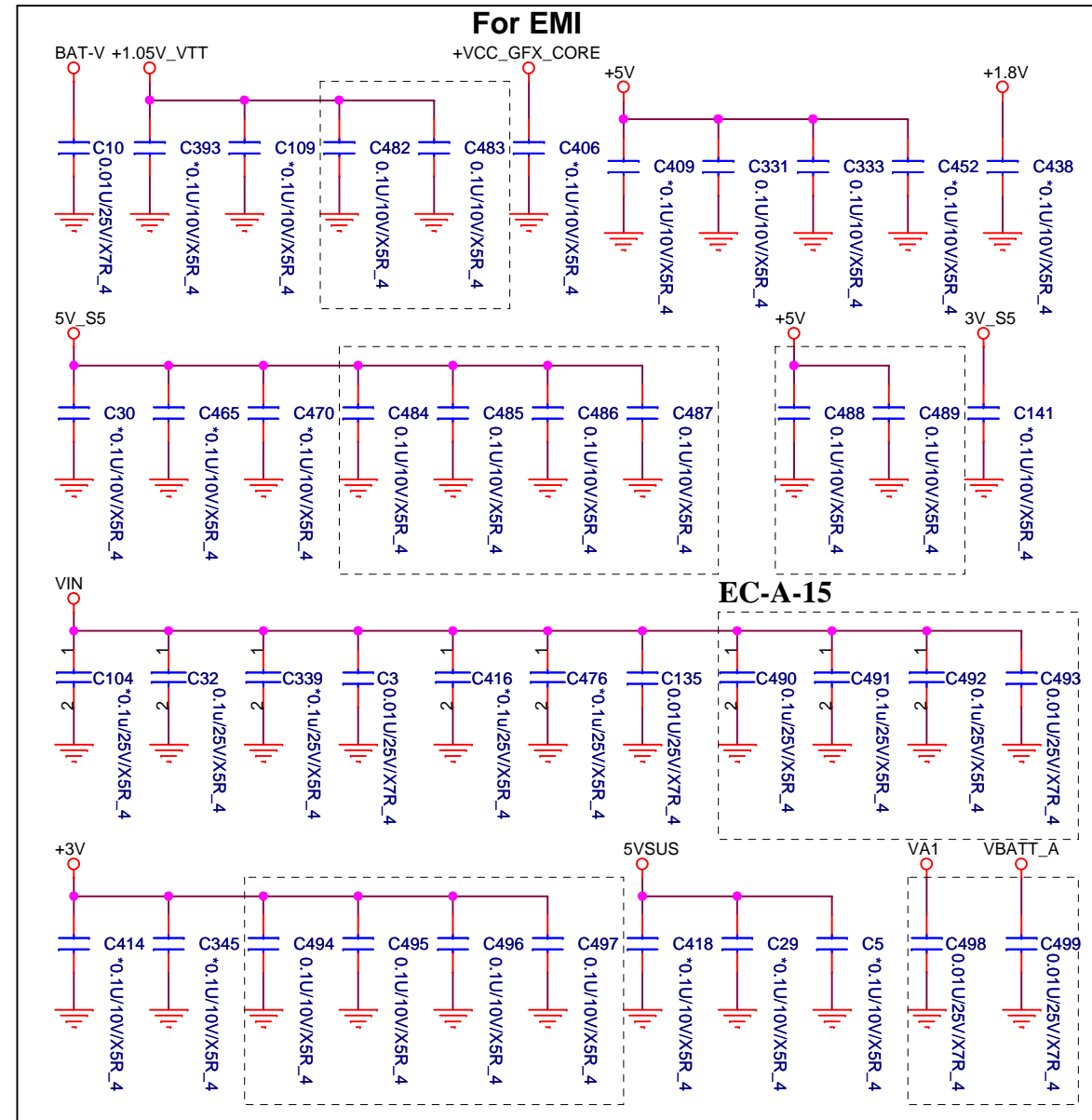
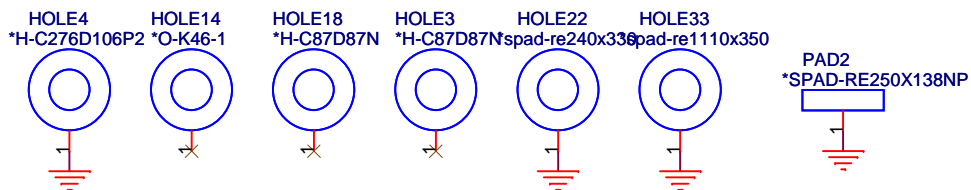
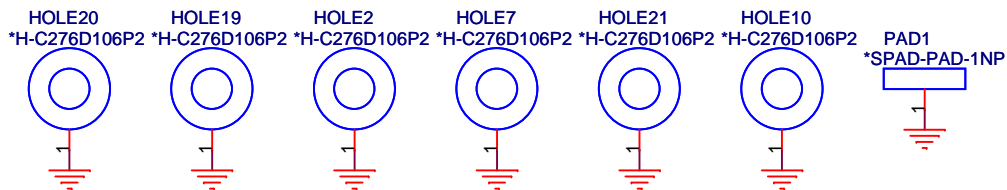
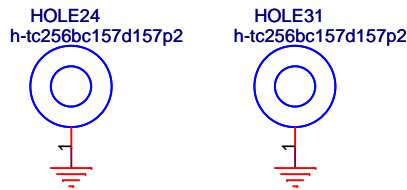
## Drink Hole



## MINI CARD nut (WLAN)



## MINI CARD nut (WWAN)



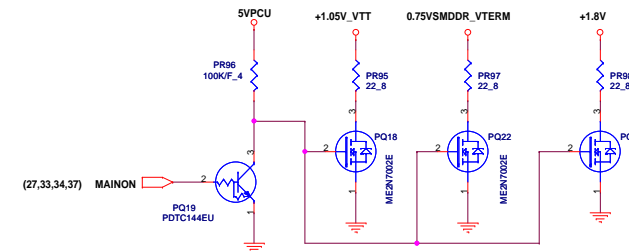
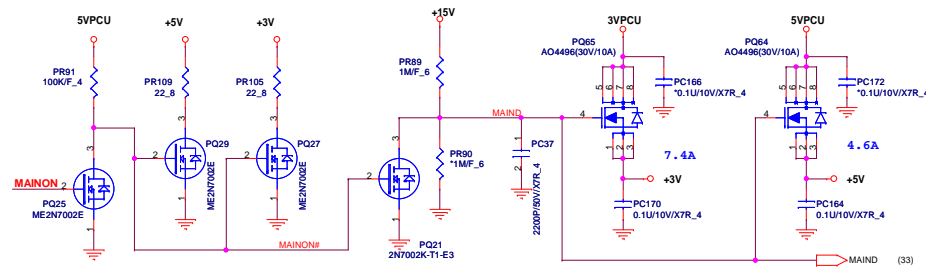
PROJECT : LL5

Quanta Computer Inc.

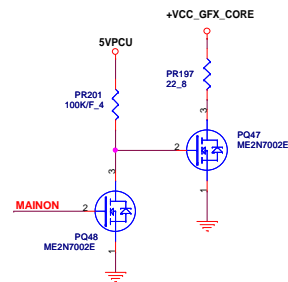
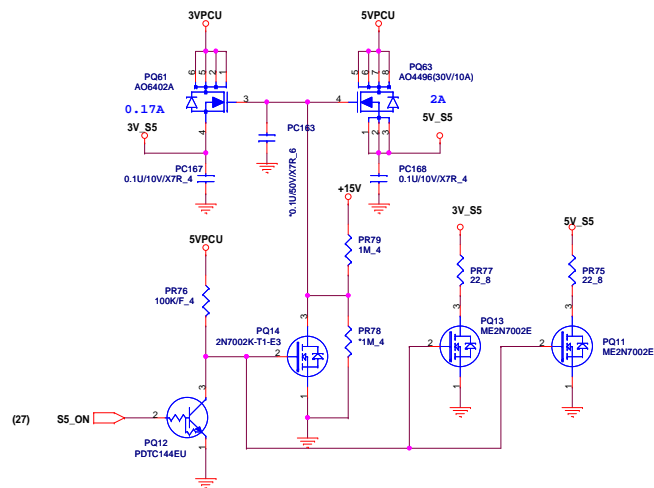
Size Custom	Document Number <b>HOLD &amp; SKEW</b>	Rev 1A
Date: Friday, October 23, 2009	Sheet 30 of 38	

## DISCHARGE

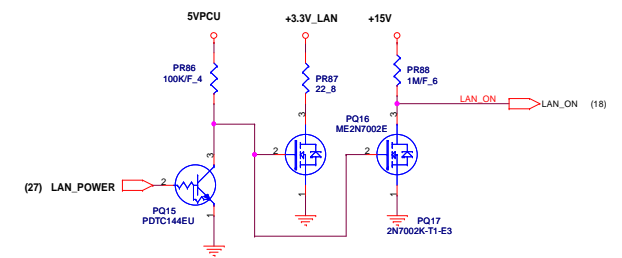
+3.3V, +5V



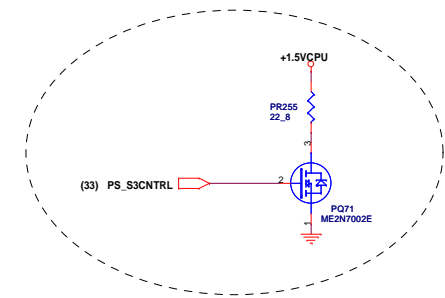
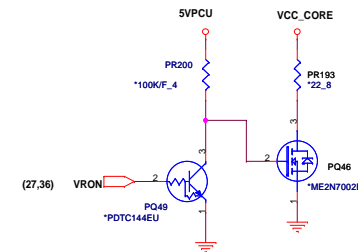
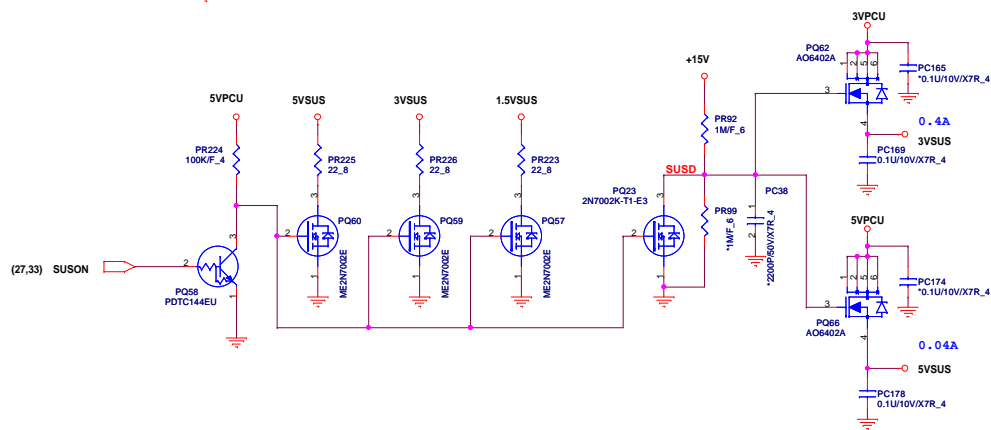
3V\_S5, 5V\_S5

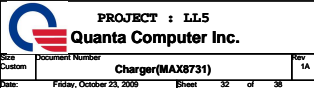


LANVCC



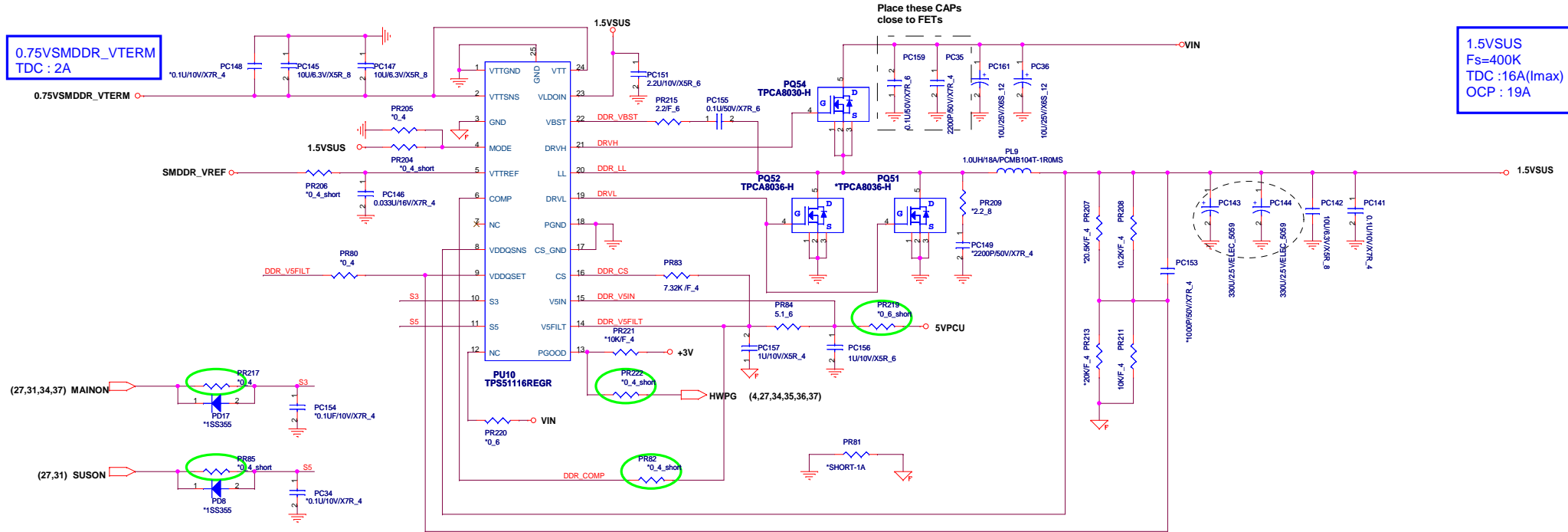
3VSUS, 5VSUS





0.75VSMDDR\_VTERM  
TDC : 2A

1.5VSUS  
Fs=400K  
TDC : 16A(I<sub>max</sub>)  
OCP : 19A



For S3 Power Saving

