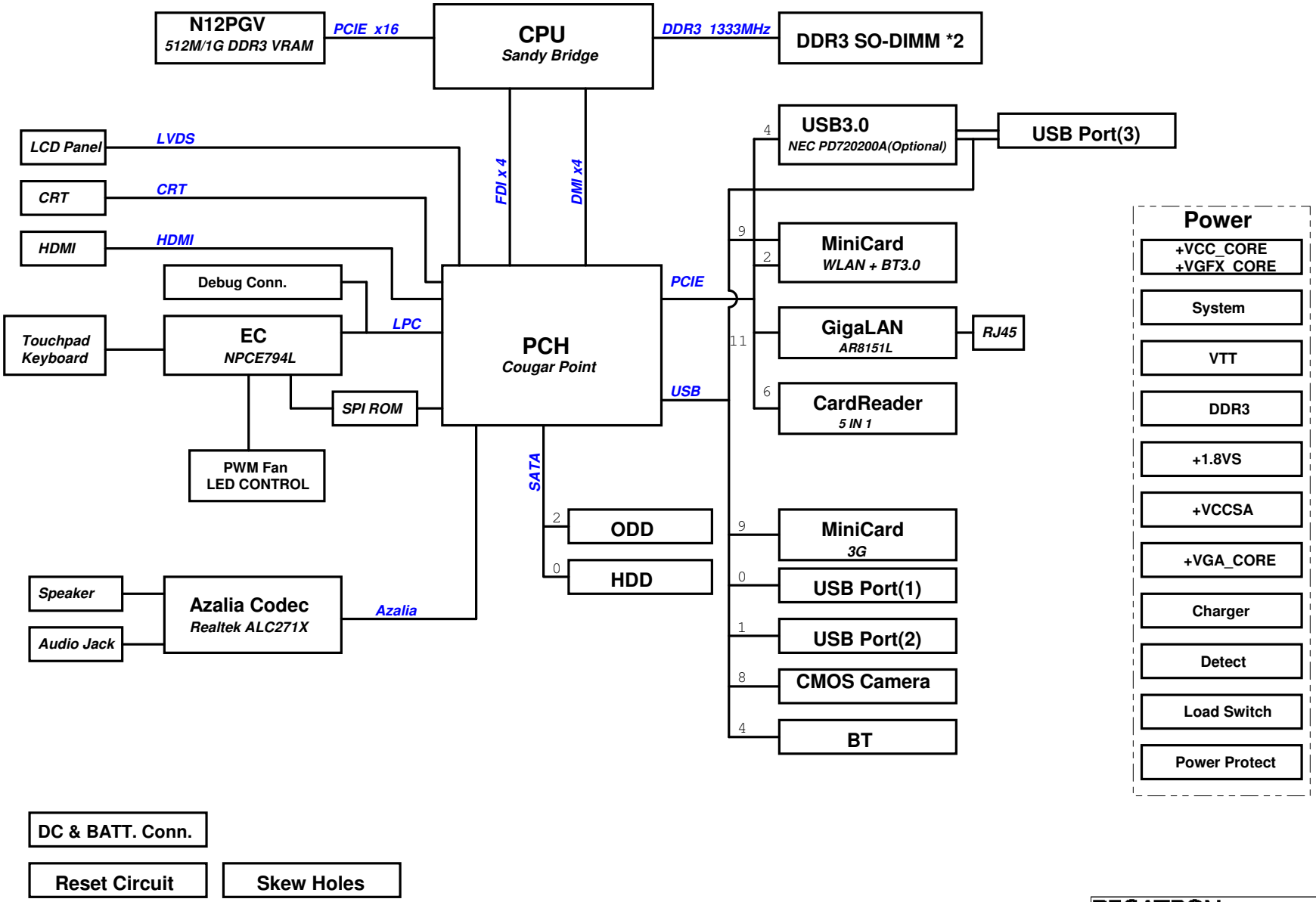
Huron River Platform Rev 2.1

BLOCK DIAGRAM



PEGATRON	Title : System Setting	
	Engineer: JAY TSAI	
Size: Custom	Project Name: EIH31	Rev: 1.3
Date: Sunday, February 06, 2011	Sheet 1 of 99	

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)
PlamRest Thermal Sensor (G781)	1001100x (98h)

PCIE 1	CardReader
PCIE 2	Minicard WLAN
PCIE 3	N/A
PCIE 4	USB3.0
PCIE 5	N/A
PCIE 6	GLAN
PCIE 7	N/A
PCIE 8	N/A

SATA0	SATA HDD
SATA1	N/A
SATA2	SATA ODD
SATA3	N/A
SATA4	N/A
SATA5	N/A

USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB Port (3)
USB 3	N/A
USB 4	Bluetooth
USB 5	N/A
USB 6	N/A
USB 7	N/A
USB 8	CMOS Camera
USB 9	WLAN
USB 10	SIM Card
USB 11	3G
USB 12	N/A
USB 13	N/A

PEGATRON Title : System Setting

Engineer: JAY TSAI

Size	Project Name	Rev
C	EIH31	1.3

Date: Tuesday, January 04, 2011 Sheet 2 of 99

+VCCP 4,6,25,26,27,30,32,55,82

U0301A

DMI

22 DMI_TXN0 B27 DMI_RX#[0]
22 DMI_TXN1 B25 DMI_RX#[1]
22 DMI_TXN2 A25 DMI_RX#[2]
22 DMI_TXN3 B24 DMI_RX#[3]

22 DMI_TXP0 B28 DMI_RX[0]
22 DMI_TXP1 B26 DMI_RX[1]
22 DMI_TXP2 A24 DMI_RX[2]
22 DMI_TXP3 B23 DMI_RX[3]

22 DMI_RXN0 G21 DMI_TX#[0]
22 DMI_RXN1 E22 DMI_TX#[1]
22 DMI_RXN2 F21 DMI_TX#[2]
22 DMI_RXN3 D21 DMI_TX#[3]

22 DMI_RXP0 G22 DMI_TX[0]
22 DMI_RXP1 D22 DMI_TX[1]
22 DMI_RXP2 F20 DMI_TX[2]
22 DMI_RXP3 C21 DMI_TX[3]

Intel(R) FDI

22 FDI_TXN[7:0]
FDI_TXN0 A21 FDI0_TX#[0]
FDI_TXN1 H19 FDI0_TX#[1]
FDI_TXN2 F19 FDI0_TX#[2]
FDI_TXN3 F18 FDI0_TX#[3]
FDI_TXN4 B21 FDI1_TX#[0]
FDI_TXN5 C20 FDI1_TX#[1]
FDI_TXN6 D18 FDI1_TX#[2]
FDI_TXN7 E17 FDI1_TX#[3]

22 FDI_TXP[7:0]
FDI_TXP0 A22 FDI0_TX[0]
FDI_TXP1 G19 FDI0_TX[1]
FDI_TXP2 E20 FDI0_TX[2]
FDI_TXP3 G18 FDI0_TX[3]
FDI_TXP4 B20 FDI1_TX[0]
FDI_TXP5 C19 FDI1_TX[1]
FDI_TXP6 D19 FDI1_TX[2]
FDI_TXP7 F17 FDI1_TX[3]

22 FDI_FSYNC0 J18 FDI0_FSYNC
22 FDI_FSYNC1 J17 FDI1_FSYNC

22 FDI_INT H20 FDI_INT

22 FDI_LSYNC0 J19 FDI0_LSYNC
22 FDI_LSYNC1 H17 FDI1_LSYNC

eDP

+VCCP
24.9Ohm 2 R0302 1 DP_COMP
A18 eDP_COMPIO
A17 eDP_ICOMPO
B16 eDP_HPD

EIH-D.G p83

C15 eDP_AUX
D15 eDP_AUX#

C17 eDP_TX[0]
F16 eDP_TX[1]
C16 eDP_TX[2]
G15 eDP_TX[3]

C18 eDP_TX#[0]
E16 eDP_TX#[1]
D16 eDP_TX#[2]
F15 eDP_TX#[3]

SOCKET989

PCI EXPRESS* - GRAPHICS

PEG_ICOMPI J22
PEG_ICOMPO J21
PEG_RCOMPO H22

+VCCP
PEG_COMP R0301 1 1% 2 24.9Ohm

PEG Compensation

Enable PCIE Lane Reversal
Need to PD CFG[2]

PCIENB_RXN[15:0] 70

PEG_RX#[0] K33 PCIENB_RXN15
PEG_RX#[1] M35 PCIENB_RXN14
PEG_RX#[2] L34 PCIENB_RXN13
PEG_RX#[3] J35 PCIENB_RXN12
PEG_RX#[4] J32 PCIENB_RXN11
PEG_RX#[5] H34 PCIENB_RXN10
PEG_RX#[6] H31 PCIENB_RXN9
PEG_RX#[7] G33 PCIENB_RXN8
PEG_RX#[8] G30 PCIENB_RXN7
PEG_RX#[9] F35 PCIENB_RXN6
PEG_RX#[10] E34 PCIENB_RXN5
PEG_RX#[11] E32 PCIENB_RXN4
PEG_RX#[12] D33 PCIENB_RXN3
PEG_RX#[13] D31 PCIENB_RXN2
PEG_RX#[14] B33 PCIENB_RXN1
PEG_RX#[15] C32 PCIENB_RXN0

PCIENB_RXP[15:0] 70

PEG_RX[0] J33 PCIENB_RXP15
PEG_RX[1] L35 PCIENB_RXP14
PEG_RX[2] K34 PCIENB_RXP13
PEG_RX[3] H35 PCIENB_RXP12
PEG_RX[4] H32 PCIENB_RXP11
PEG_RX[5] G34 PCIENB_RXP10
PEG_RX[6] G31 PCIENB_RXP9
PEG_RX[7] F33 PCIENB_RXP8
PEG_RX[8] F30 PCIENB_RXP7
PEG_RX[9] E35 PCIENB_RXP6
PEG_RX[10] E33 PCIENB_RXP5
PEG_RX[11] F32 PCIENB_RXP4
PEG_RX[12] D34 PCIENB_RXP3
PEG_RX[13] E31 PCIENB_RXP2
PEG_RX[14] C33 PCIENB_RXP1
PEG_RX[15] B32 PCIENB_RXP0

PCIEG_RXN[15:0] 70

PEG_TX#[0] M29 PCIENB_TXN0 CX0301 1 2 0.1UF/16V /DGPU PCIEG_RXN15
PEG_TX#[1] M32 PCIENB_TXN1 CX0302 1 2 0.1UF/16V /DGPU PCIEG_RXN14
PEG_TX#[2] M31 PCIENB_TXN2 CX0303 1 2 0.1UF/16V /DGPU PCIEG_RXN13
PEG_TX#[3] L32 PCIENB_TXN3 CX0304 1 2 0.1UF/16V /DGPU PCIEG_RXN12
PEG_TX#[4] L29 PCIENB_TXN4 CX0305 1 2 0.1UF/16V /DGPU PCIEG_RXN11
PEG_TX#[5] K31 PCIENB_TXN5 CX0306 1 2 0.1UF/16V /DGPU PCIEG_RXN10
PEG_TX#[6] K28 PCIENB_TXN6 CX0307 1 2 0.1UF/16V /DGPU PCIEG_RXN9
PEG_TX#[7] J30 PCIENB_TXN7 CX0308 1 2 0.1UF/16V /DGPU PCIEG_RXN8
PEG_TX#[8] J28 PCIENB_TXN8 CX302 1 2 0.1UF/16V /DGPU PCIEG_RXN7
PEG_TX#[9] H29 PCIENB_TXN9 CX303 1 2 0.1UF/16V /DGPU PCIEG_RXN6
PEG_TX#[10] G27 PCIENB_TXN10 CX304 1 2 0.1UF/16V /DGPU PCIEG_RXN5
PEG_TX#[11] F29 PCIENB_TXN11 CX305 1 2 0.1UF/16V /DGPU PCIEG_RXN4
PEG_TX#[12] E27 PCIENB_TXN12 CX306 1 2 0.1UF/16V /DGPU PCIEG_RXN3
PEG_TX#[13] D28 PCIENB_TXN13 CX307 1 2 0.1UF/16V /DGPU PCIEG_RXN2
PEG_TX#[14] F26 PCIENB_TXN14 CX308 1 2 0.1UF/16V /DGPU PCIEG_RXN1
PEG_TX#[15] E25 PCIENB_TXN15 CX309 1 2 0.1UF/16V /DGPU PCIEG_RXN0

PCIEG_RXP[15:0] 70

PEG_TX[0] M28 PCIENB_TXP0 CX0317 1 2 0.1UF/16V /DGPU PCIEG_RXP15
PEG_TX[1] M33 PCIENB_TXP1 CX0318 1 2 0.1UF/16V /DGPU PCIEG_RXP14
PEG_TX[2] M30 PCIENB_TXP2 CX0319 1 2 0.1UF/16V /DGPU PCIEG_RXP13
PEG_TX[3] L31 PCIENB_TXP3 CX0320 1 2 0.1UF/16V /DGPU PCIEG_RXP12
PEG_TX[4] L28 PCIENB_TXP4 CX0321 1 2 0.1UF/16V /DGPU PCIEG_RXP11
PEG_TX[5] K30 PCIENB_TXP5 CX0322 1 2 0.1UF/16V /DGPU PCIEG_RXP10
PEG_TX[6] K27 PCIENB_TXP6 CX0323 1 2 0.1UF/16V /DGPU PCIEG_RXP9
PEG_TX[7] J29 PCIENB_TXP7 CX0324 1 2 0.1UF/16V /DGPU PCIEG_RXP8
PEG_TX[8] J27 PCIENB_TXP8 CX318 1 2 0.1UF/16V /DGPU PCIEG_RXP7
PEG_TX[9] H28 PCIENB_TXP9 CX319 1 2 0.1UF/16V /DGPU PCIEG_RXP6
PEG_TX[10] G28 PCIENB_TXP10 CX320 1 2 0.1UF/16V /DGPU PCIEG_RXP5
PEG_TX[11] E28 PCIENB_TXP11 CX321 1 2 0.1UF/16V /DGPU PCIEG_RXP4
PEG_TX[12] F28 PCIENB_TXP12 CX322 1 2 0.1UF/16V /DGPU PCIEG_RXP3
PEG_TX[13] D27 PCIENB_TXP13 CX323 1 2 0.1UF/16V /DGPU PCIEG_RXP2
PEG_TX[14] E26 PCIENB_TXP14 CX324 1 2 0.1UF/16V /DGPU PCIEG_RXP1
PEG_TX[15] D25 PCIENB_TXP15 CX325 1 2 0.1UF/16V /DGPU PCIEG_RXP0

If Support PCIE Gen3, change AC Cap to 0.22uF

EIH31 : 1201-006D000 MOBILE rPGA CPU SOCKET 988B

PEGATRON	Title : CPU(1)_DMI,PEG,FDI,	
	Engineer: JAY TSAI	
Size: Custom	Project Name: EIH31	Rev: 1.0
Date: Friday, January 07, 2011	Sheet 3 of 99	

+1.5V_VCCDDQ — +1.5V_VCCDDQ 7
+3VS — +3VS 16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,59,91,92
+3VSUS — +3VSUS 22,24,27,28,30,59,81,82,84,92
+VCCP — +VCCP 3,6,25,26,27,30,32,55,82
+3V — +3V 24,52,53,55,59,91

U0301B

C26 will change to PROC_SELECT#

24 H_SNB_IVB# — C26 — SNB_IVB#
T0401 — TP_SKTOCC# R — AN34 — SKTOCC#
T0402 — TP_CATERR# R — AL33 — CATERR#
25 H_PECI — AN33 — PECI
+VCCP — 75Ohm — 1% R0404 — H_PROCHOT# — 44.2Ohm — 1% R0403 — H_PROCHOT# D — AL32 — PROCHOT#
25,32 H_THRMTRIP# — SP0401 R0402 — H_THRMTRIP# R — AN32 — THERMTRIP#

MISC
THERMAL

22 H_PM_SYNC — SP0402 — H_PM_SYNC R — AM34 — PM_SYNC
10KOhm R0408
25 H_CPUPWRGD — SP0403 — H CPUPWRGD R — AP33 — UNCOREPWRGOOD
22 PM_DRAM_PWRGD — 130Ohm — 1% R0409 — VDDPWRGOOD R — R1.3 — V8 — SM_DRAMPWROK
R0416 1.5KOhm
24,30,32,40,53,59,70 BUF_PLT_RST# — BUF_CPU_RST# — AR33 — RESET#
R0417 750Ohm

PWR MANAGEMENT

SOCKET989
12V013ASM000

CLOCKS

BCLK — A28 BCLK_CPU_P — 0Ohm RN0401A — CLK_EXP_P 21
BCLK# — A27 BCLK_CPU_N — 0Ohm RN0401B — CLK_EXP_N 21
R0429 1KOhm
DPLL_REF_SSCLK — A16 CLK_DP_P_R — 0Ohm RN0402A — CLK_DP_P 21
DPLL_REF_SSCLK# — A15 CLK_DP_N_R — 0Ohm RN0402B — CLK_DP_N 21
@@
R0430 1KOhm — +VCCP

EIH- D.G p83

DDR3 MISC

SM_DRAMRST# — R8 — CPUDRAMRST# 5
SM_RCOMP[0] — AK1 SM_RCOMP_0 — R0418 1% 140Ohm
SM_RCOMP[1] — A5 SM_RCOMP_1 — R0419 1% 25.5Ohm
SM_RCOMP[2] — A4 SM_RCOMP_2 — R0420 1% 200Ohm

Huron River platform Design Guide Update 440484
SM_RCOMP_1 use 26ohm 1%

JTAG & BPM

PRDY# — AP29 XDP_PRDY# — T0403
PREQ# — AP27 XDP_PREQ#
TCK — AR26 XDP_TCK
TMS — AR27 XDP_TMS
TRST# — AP30 XDP_TRST#
TDI — AR28 XDP_TDI
TDO — AP26 XDP_TDO
DBR# — AL35 H_DBR#
BPM#[0] — AT28 XDP_BPM#0 — T0411
BPM#[1] — AR29 XDP_BPM#1
BPM#[2] — AR30 XDP_BPM#2 — T0413
BPM#[3] — AT30 XDP_BPM#3 — T0414
BPM#[4] — AP32 XDP_BPM#4 — T0415
BPM#[5] — AR31 XDP_BPM#5 — T0416
BPM#[6] — AT31 XDP_BPM#6 — T0417
BPM#[7] — AR32 XDP_BPM#7 — T0418

+VCCP
XDP_BPM#1 — R0428 — 51Ohm @
XDP_PREQ# — R0421 — 51Ohm
XDP_TDI — R0422 — 51Ohm @
XDP_TDO — R0423 — 51Ohm
XDP_TMS — R0424 — 51Ohm @

H_DBR# — R0425 — 1KOhm @ — +3VS
XDP_TCK — R0426 — 51Ohm @
XDP_TRST# — R0427 — 51Ohm

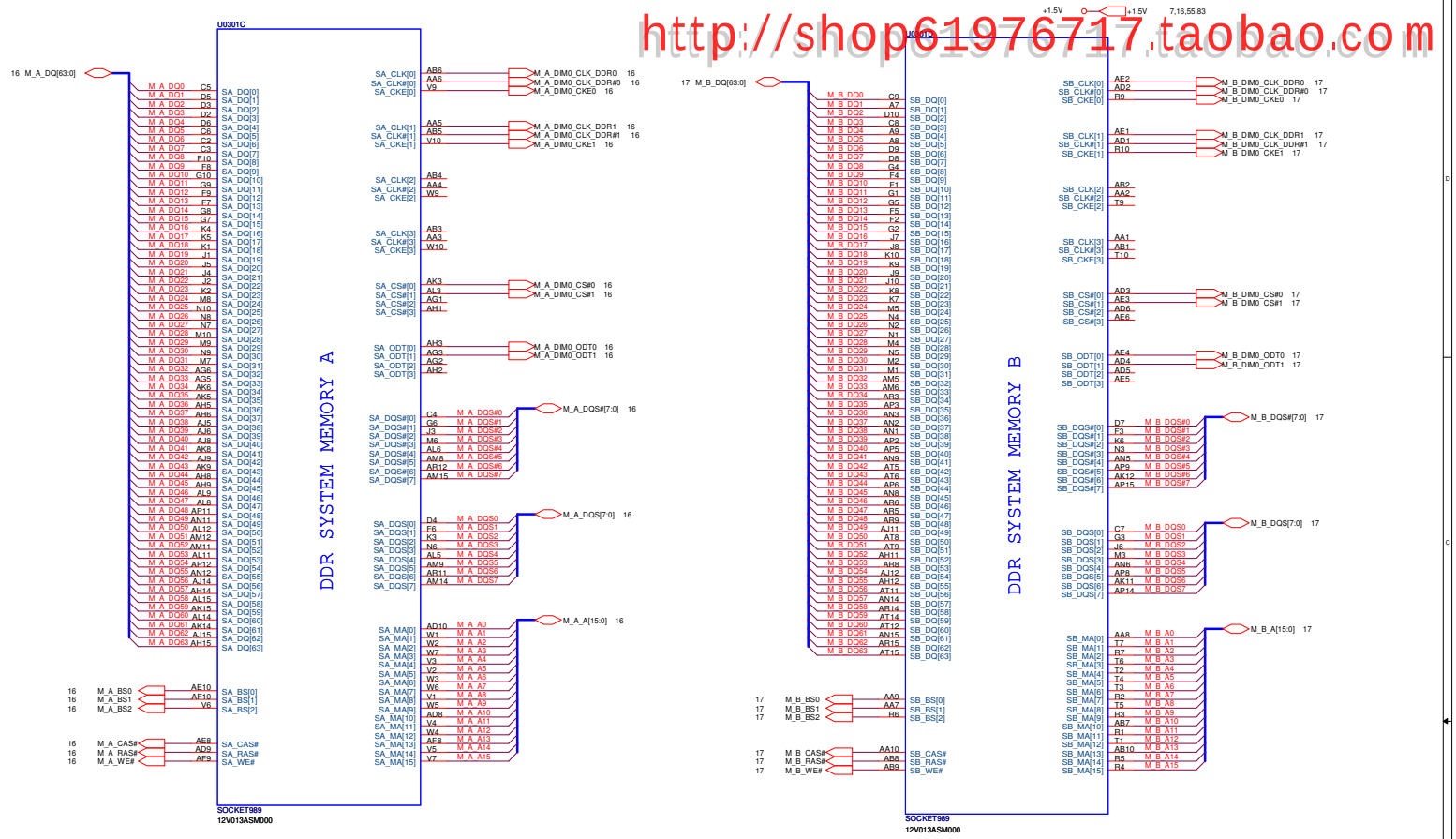
R1.3 Add VR_HOT#

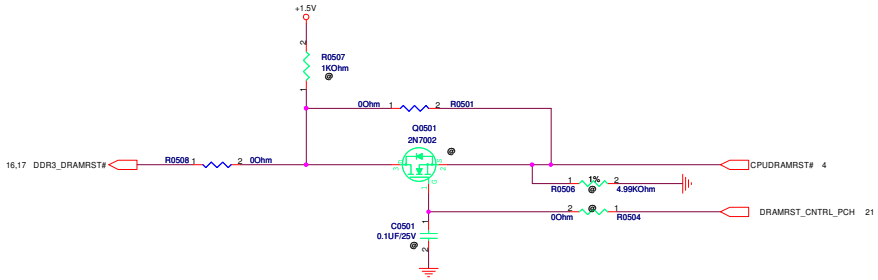
80 VR_HOT# — 0Ohm @ R0462 — H_PROCHOT#
Q0401 2N7002 — THRO_CPU — THRO_CPU 30

PM_SYS_PWRGD is the power good for +1.5V_VCCDDQ

+1.5V_VCCDDQ — R0449 200Ohm 1%
PM_DRAM_PWRGD — 0Ohm — R0451
R0450 1KOhm 1% @
1.57 Volt
R0452 1.1KOhm 1% @
C0405 0.22UF/10V @
+3VSUS — U0404 — Vcc=1.65~5.5 @
+3V — R0453 10KOhm @
Q0403 PMBS3904 @
C0404 0.22UF/10V @
R0455 47KOhm 1% @
R0454 24.3KOhm 1% @ — +1.5V_VCCDDQ

PEGATRON	Title : CPU(2)_CLK,MISC,JTA	
	Engineer: JAY TSAI	
Size: Custom	Project Name: EIH31	Rev: 1.0
Date: Friday, January 07, 2011	Sheet 4 of 99	





PEGATRON	Title : CPU(3) DDR3	
	Engineer: JAY TSAI	
Size: Custom	Project Name: EIH31	Rev: 1.0
Date: Friday, January 07, 2011	Sheet 5 of 99	

POWER

U0301F

SV-DC
0.8V ~ 1.35V

+VCC_CORE 1,4,25,28,27,30,32,55,82
+VCC_CORE 80

CORE SUPPLY

+VCC_CORE

AG35 VCC1, AG34 VCC2, AG33 VCC3, AG32 VCC4, AG31 VCC5, AG30 VCC6, AG29 VCC7, AG28 VCC8, AG27 VCC9, AG26 VCC10, AF35 VCC11, AF34 VCC12, AF33 VCC13, AF32 VCC14, AF31 VCC15, AF30 VCC16, AF29 VCC17, AF28 VCC18, AF27 VCC19, AF26 VCC20, AD35 VCC21, AD34 VCC22, AD33 VCC23, AD32 VCC24, AD31 VCC25, AD30 VCC26, AD29 VCC27, AD28 VCC28, AD27 VCC29, AD26 VCC30, AC35 VCC31, AC34 VCC32, AC33 VCC33, AC32 VCC34, AC31 VCC35, AC30 VCC36, AC29 VCC37, AC28 VCC38, AC27 VCC39, AC26 VCC40, AA35 VCC41, AA34 VCC42, AA33 VCC43, AA32 VCC44, AA31 VCC45, AA30 VCC46, AA29 VCC47, AA28 VCC48, AA27 VCC49, AA26 VCC50, Y35 VCC51, Y34 VCC52, Y33 VCC53, Y32 VCC54, Y31 VCC55, Y30 VCC56, Y29 VCC57, Y28 VCC58, Y27 VCC59, Y26 VCC60, V35 VCC61, V34 VCC62, V33 VCC63, V32 VCC64, V31 VCC65, V30 VCC66, V29 VCC67, V28 VCC68, V27 VCC69, V26 VCC70, U35 VCC71, U34 VCC72, U33 VCC73, U32 VCC74, U31 VCC75, U30 VCC76, U29 VCC77, U28 VCC78, U27 VCC79, U26 VCC80, R35 VCC81, R34 VCC82, R33 VCC83, R32 VCC84, R31 VCC85, R30 VCC86, R29 VCC87, R28 VCC88, R27 VCC89, R26 VCC90, P35 VCC91, P34 VCC92, P33 VCC93, P32 VCC94, P31 VCC95, P30 VCC96, P29 VCC97, P28 VCC98, P27 VCC99, P26 VCC100

PEG AND DDR

+VCCP

VCCIO1 AH13, VCCIO2 AH10, VCCIO3 AG10, VCCIO4 AC10, VCCIO5 Y10, VCCIO6 U10, VCCIO7 P10, VCCIO8 L10, VCCIO9 J14, VCCIO10 J13, VCCIO11 J12, VCCIO12 J11, VCCIO13 H14, VCCIO14 H12, VCCIO15 H11, VCCIO16 G14, VCCIO17 G13, VCCIO18 G12, VCCIO19 F14, VCCIO20 F13, VCCIO21 F12, VCCIO22 F11, VCCIO23 E14, VCCIO24 E12, VCCIO25 E11, VCCIO26 D14, VCCIO27 D13, VCCIO28 D12, VCCIO29 D11, VCCIO30 C14, VCCIO31 C13, VCCIO32 C12, VCCIO33 C11, VCCIO34 B14, VCCIO35 B12, VCCIO36 A14, VCCIO37 A13, VCCIO38 A12, VCCIO39 A11, VCCIO40 J23

+VCC_CORE

53A

C0632 22UF/6.3V, C0633 22UF/6.3V @, C0634 22UF/6.3V, C0638 22UF/6.3V, C0639 22UF/6.3V, C0645 22UF/6.3V, C0655 22UF/6.3V, C0658 22UF/6.3V, C0659 22UF/6.3V @, C0662 22UF/6.3V

C0640 10UF/6.3V @, C0657 10UF/6.3V, C0660 10UF/6.3V, C0661 10UF/6.3V, C0647 10UF/6.3V @, C0648 10UF/6.3V, C0649 10UF/6.3V, C0651 10UF/6.3V, C0652 10UF/6.3V, C0653 10UF/6.3V

C0637 10UF/6.3V, C0641 10UF/6.3V @, C0642 10UF/6.3V @, C0650 10UF/6.3V, C0656 10UF/6.3V, C0689 10UF/6.3V, C0690 22UF/6.3V @, C0691 22UF/6.3V @, C0692 22UF/6.3V @, C0693 22UF/6.3V @

ER1.16

CE0601 CE0602 A14 at Power side

SVID

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

+VCCP

Close to CPU R0611 75Ohm 1%
R0612 1% 44.2Ohm
VR_SVID_ALERT# 80

Close to VR R0605 54.9Ohm 1%
SP0601 R0402
VR_SVID_CLK 80

Close to CPU R0607 130Ohm 1%
SP0602 R0402
Close to VR R0608 130Ohm 1%
VR_SVID_DATA 80

8.5A

C0601 10UF/6.3V, C0602 10UF/6.3V, C0603 10UF/6.3V, C0604 10UF/6.3V, C0605 10UF/6.3V, C0606 10UF/6.3V, C0607 10UF/6.3V, C0608 10UF/6.3V, C0609 10UF/6.3V, C0687 10UF/6.3V

C0688 10UF/6.3V, C0610 10UF/6.3V, C0611 10UF/6.3V @, C0644 10UF/6.3V @, C0612 10UF/6.3V, C0613 10UF/6.3V, C0614 10UF/6.3V, C0615 10UF/6.3V, C0616 10UF/6.3V

C0617 22UF/6.3V @, C0618 22UF/6.3V @, C0619 22UF/6.3V @, C0620 22UF/6.3V @, C0621 22UF/6.3V @, C0622 22UF/6.3V @, C0623 22UF/6.3V @, C0624 22UF/6.3V @, C0625 22UF/6.3V @, CE0603 330UF/2V @

SENSE LINES

VCC_SENSE AJ35 VCC_SENSE_R SP0603 R0402 VCCSENSE VCCSENSE 80
VSS_SENSE AJ34 VSS_SENSE_R SP0604 R0402 VSSSENSE VSSSENSE 80

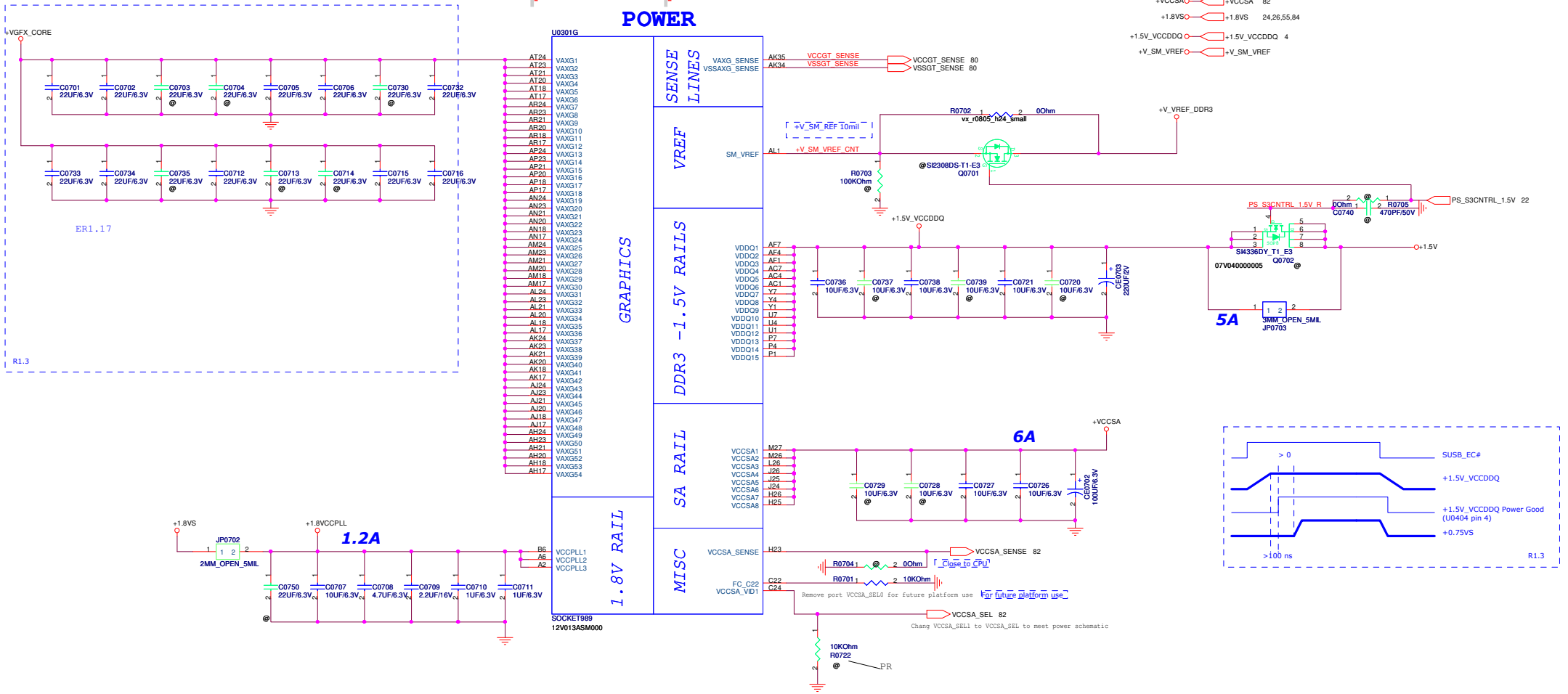
+VCC_CORE
R0602 100Ohm 1%
R0603 100Ohm 1%

VCCIO_SENSE B10 TP_VCCIO_SENSE T0601
VSSIO_SENSE A10 TP_VSSIO_SENSE T0602

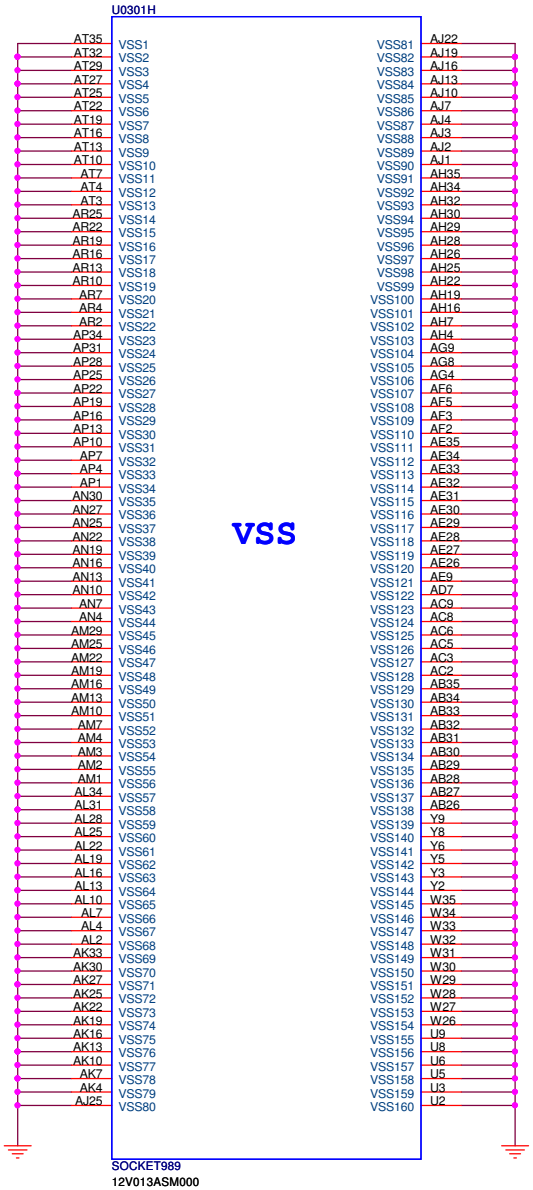
SOCKET989
12V013ASM000

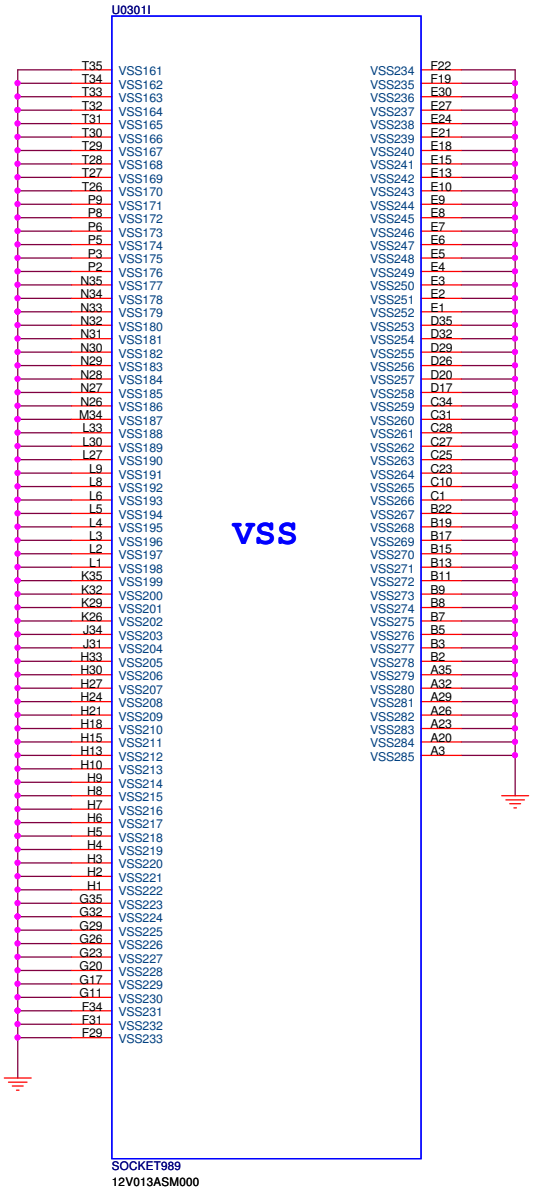
PEGATRON	Title : CPU(4)_PWR	
	Engineer: JAY TSAI	
Size: Custom	Project Name: EIH31	Rev: 1.0
Date: Thursday, January 13, 2011	Sheet 6 of 99	

POWER



PEGATRON	Title : CPU(5)_PWR	
	Engineer: JAY TSAI	
Size: Custom	Project Name: EIH31	Rev: 1.0
Date: Thursday, January 13, 2011	Sheet 7 of 99	





PEGATRON	Title : CPU(6)_CFG,RSVD,GN	
	Engineer: JAY TSAI	
Size: Custom	Project Name: EIH31	Rev: 1.0
Date: Tuesday, January 04, 2011	Sheet 8 of 99	

CFG strapping information:

CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x

- 1: (Default) Normal Operation, Lane # definition matches sockect pin map definition
- 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection

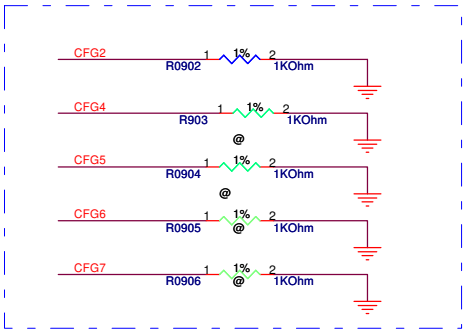
- 1: (Default) Disabled ; No Physical Display Port attached to Embedded DisplayPort
- 0: Enabled ; An external Display Port device is connected to the Embedded Display Port

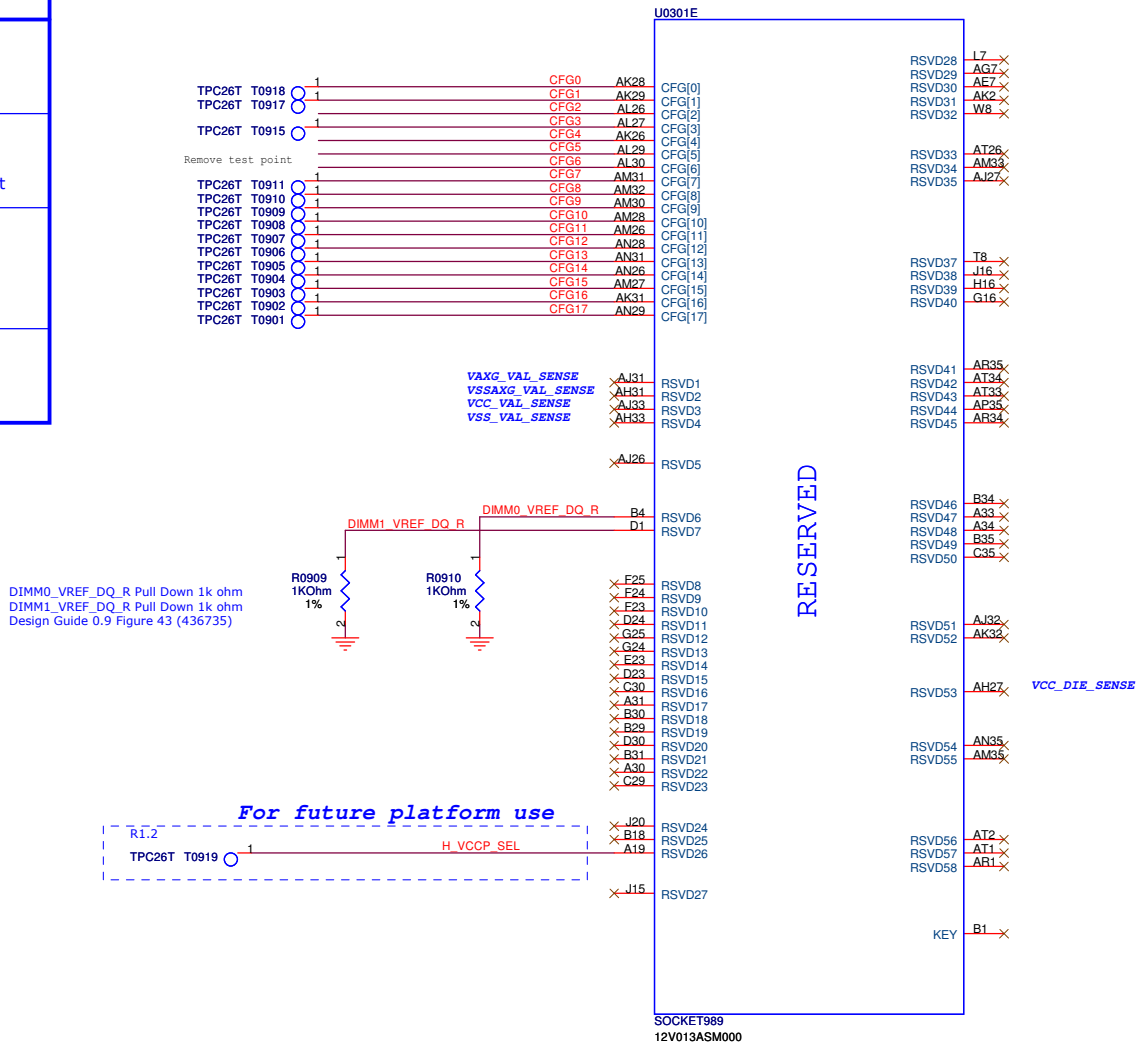
CFG[6:5]: PCI Express Port Bifurcation Straps

- 11 : (Default) x 1 6
- 10 : x 8 , x 8
- 01 : Reserved
- 00 : x 8 , x 4 , x 4

CFG[7]: PEG DEFER TRAINING

- 1: (Default) PEG Train immediately following xxRESETB de assertion
- 0: PEG Wait for BIOS training





PEGATRON	Title : CPU(7)_CFG,RSVD,GN	
	Engineer: JAY TSAI	
Size: Custom	Project Name: EIH31	Rev: 1.0
Date: Tuesday, January 04, 2011	Sheet 9 of 99	

PEGATRON	Title : NB(3)_****		
	Engineer: JAY TSAI		
Size: Custom	Project Name: EIH31		Rev: 1.3
Date: Tuesday, January 04, 2011	Sheet 10 of 99		

PEGATRON	Title : NB(4)_****		
	Engineer: JAY TSAI		
Size: Custom	Project Name: EIH31		Rev: 1.3
Date: Tuesday, January 04, 2011	Sheet 11 of 99		

PEGATRON	Title : NB(5)_****		
	Engineer: JAY TSAI		
Size: Custom	Project Name: EIH31		Rev: 1.3
Date: Tuesday, January 04, 2011	Sheet 12 of 99		

PEGATRON	Title : NB(6)_****		
	Engineer: JAY TSAI		
Size: Custom	Project Name: EIH31		Rev: 1.3
Date: Tuesday, January 04, 2011	Sheet 13 of 99		

PEGATRON	Title : NB(7)_****		
	Engineer: JAY TSAI		
Size A	Project Name EIH31		Rev 1.3
Date: Tuesday, January 04, 2011		Sheet 14 of 99	

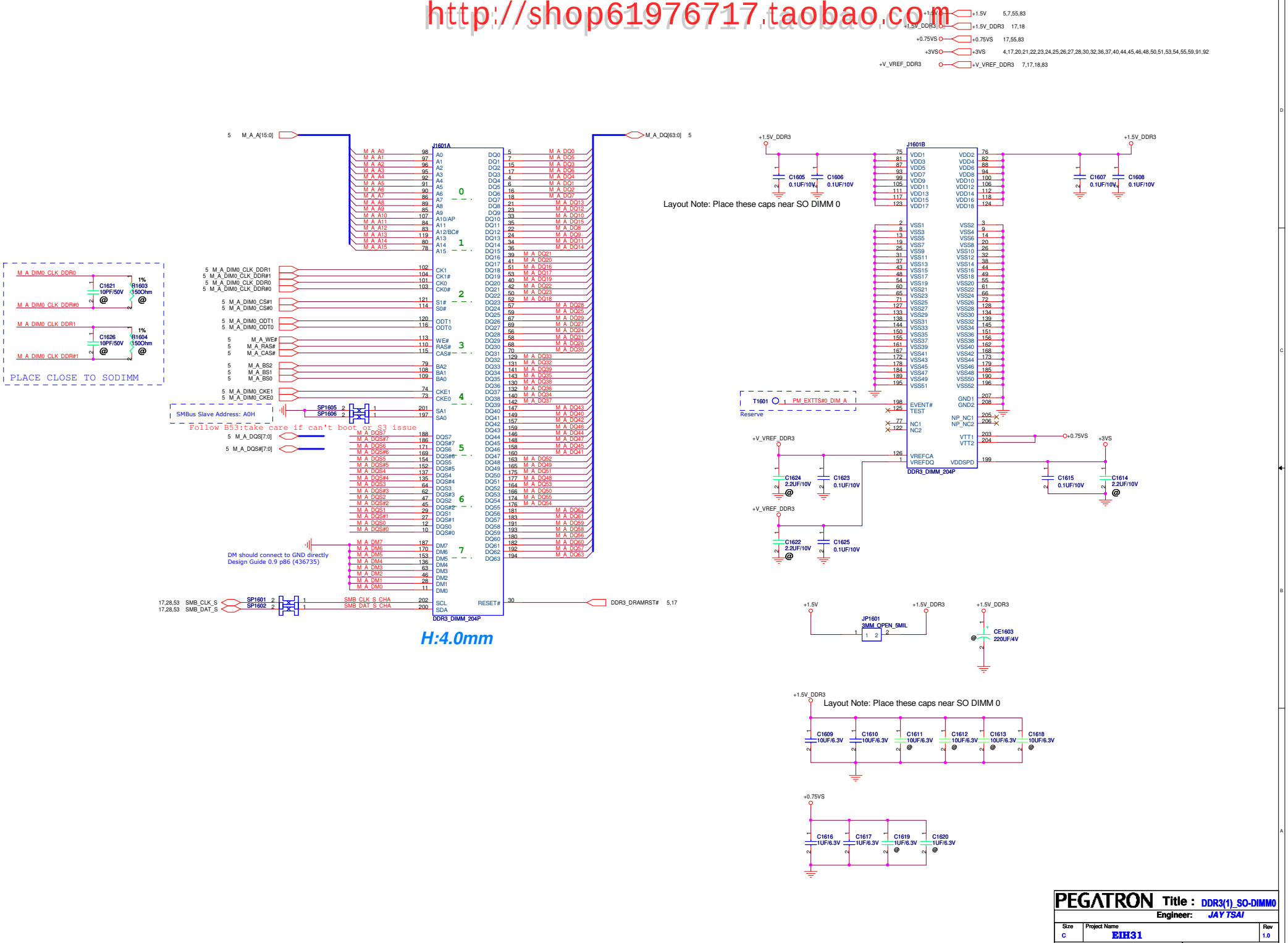
PEGATRON

Title : NB(8)_****

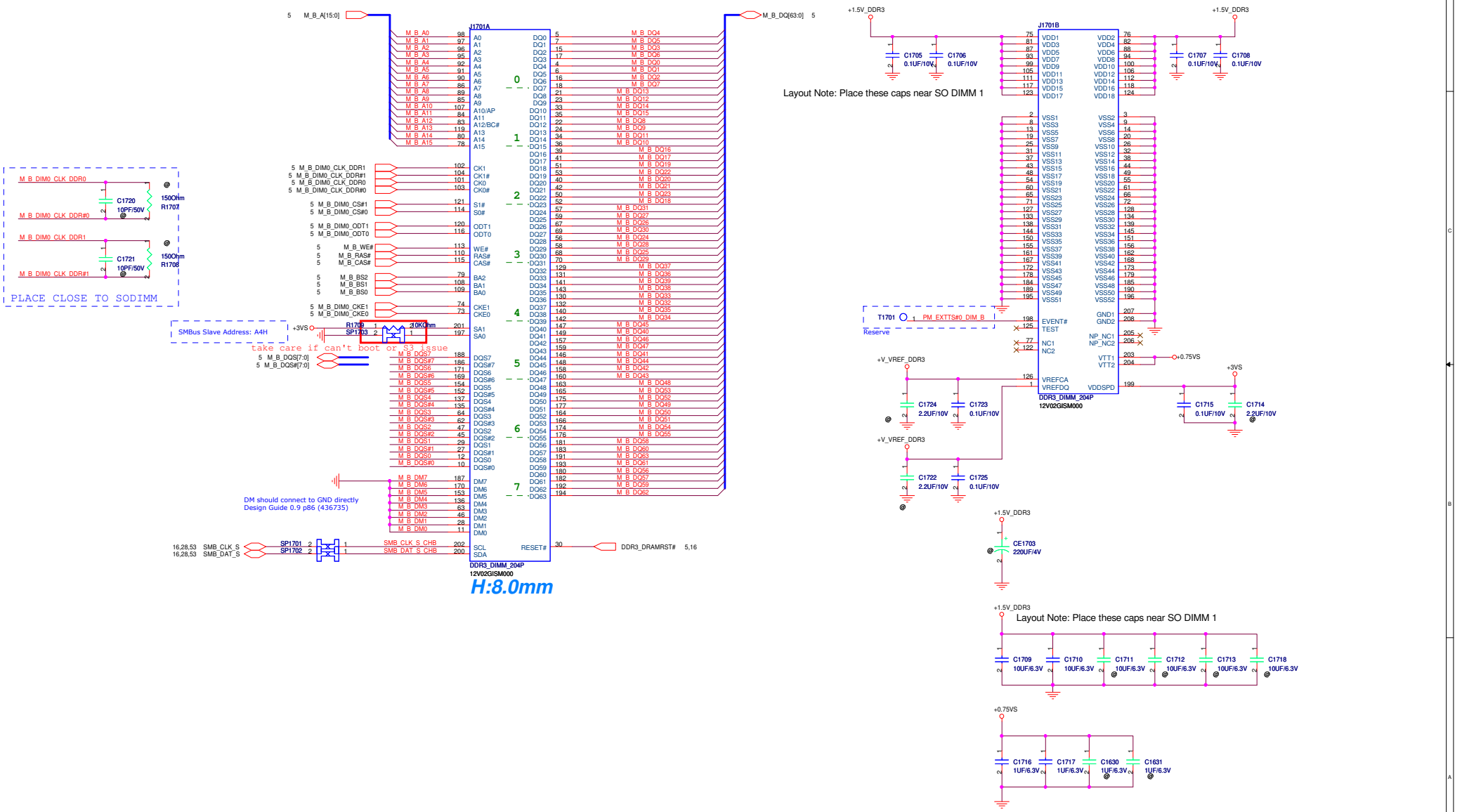
Engineer: JAY TSAI

Size	Project Name	Rev
A	EIH31	1.3

Date: Tuesday, January 04, 2011 Sheet 15 of 99



PEGATRON	Title : DDR3(1)_SO-DIMM0	
	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.0
Date: Thursday, January 13, 2011	Sheet 16 of 99	



PEGATRON	Title : DDR3(2)_SO-DIMM1	
	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.0
Date: Thursday, January 13, 2011	Sheet 17 of 99	

+1.5V_DDR3 +1.5V_DDR3 16,17

+V_VREF +V_VREF
+V_VREF_DDR3 +V_VREF_DDR3 7,16,17,83
+V_SM_VREF +V_SM_VREF

+3V +3V 4,24,52,53,55,59,91
+5VSUS +5VSUS 22,27,81,82,83,84,87,91
+5VA +5VA 59,81,88

DDR3 Vref

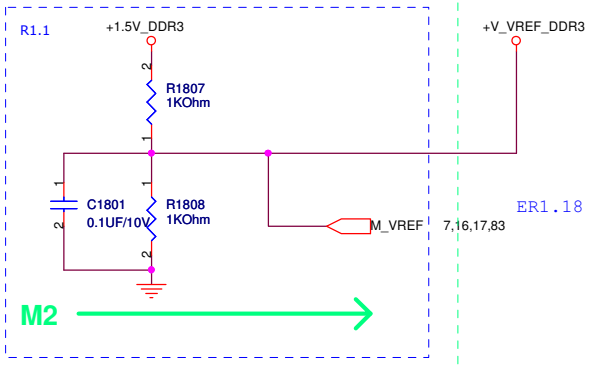
Default M1

R1.1

Power remove M_REF function.

M1: Fixed SO-DIMM VREF_DQ

M2: Programmable SO-DIMM VREFDQ on motherboard– New Requirement



PEGATRON	Title DDR3(3)_CA/DQ Voltage	
	Engineer: JAY TSAI	
Size B	Project Name EIH31	Rev 1.0
Date: Thursday, January 13, 2011	Sheet 18 of 99	

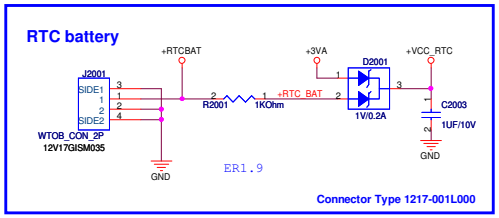
R1.4--2

PEGATRON Title : VID Controller

Engineer: JAY TSAI

Size	Project Name	Rev
C	EIH31	1.3

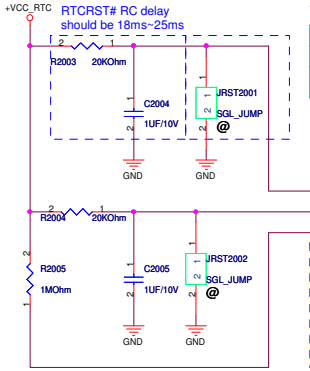
Date: Tuesday, January 04, 2011 Sheet 19 of 99



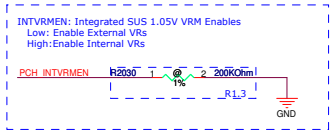
+VCC_RTC	+VCC_RTC	22,27
+RTCBAT	+RTCBAT	
+3VA	+3VA	27,30,55,56,59,81,93
+3VS	+3VS	4,16,17,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,59,91,92
+3VSUS_ORG	+3VSUS_ORG	21,22,24,25,27
+1.05VM_ORG	+1.05VM_ORG	27
+VTT_PCH_VCCIO	+VTT_PCH_VCCIO	26,27

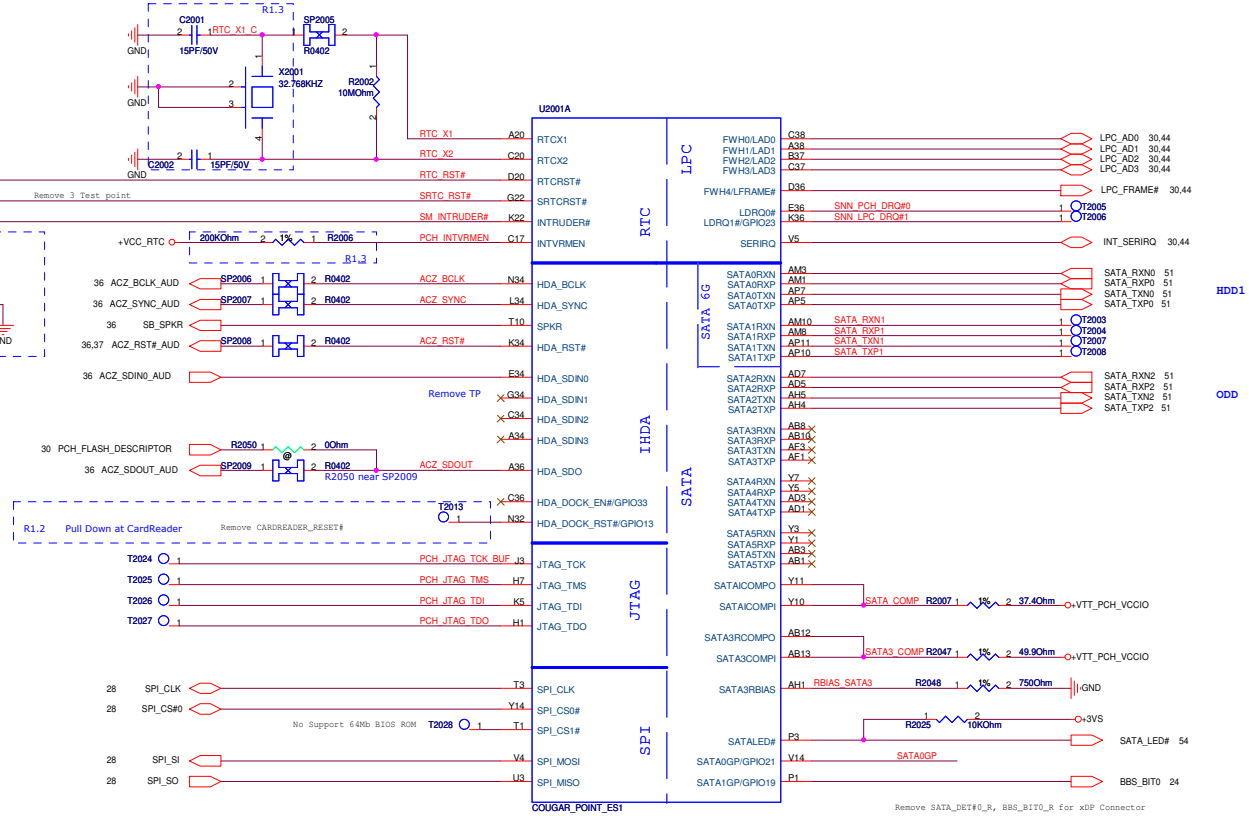
Request by CSC for CMOS clear function

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)



TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)





0200-00HU000 C.S 907552 A1 QMVY BGA942 INTEL/COUGAR POINT PCH

Remove xDP component

Strap information:

SB_SPKR: No reboot strap
Low: Disable (Default)
High:Enable

SB_SPKR — R2020 — 1KOhm — +3VS

ACZ_SDOUT:
1.Flash descriptor security:
Sampled Low: in effect.
Sampled High: override

2.ACZ_SDOUTwhich sample high on the rising edge of PWROK
Will also disable Intel ME.

ACZ_SDOUT — R2034 — 1KOhm — +3VSUS_ORG

ACZ_SYNC: On Die PLL VR voltage selector
Low: 1.8V (Default)
High: 1.5V
note : CRB has no strap
Hrron River Platform Schematic Design Checklist
(438390 page 48)

ACZ_SYNC — R2036 — 1KOhm — +3VSUS_ORG

VCCVRAM use +1.5VS in mobile

Pull High

INT_SERIRQ — R2026 — 10KOhm — +3VS

SATA0GP — R2027 — 10KOhm — +3VS

PEGATRON	Title : PCH(1)_SATA,IHDA,RTC,LPC	
	Engineer: JAY TSAI	
Size C	Project Name EIH31	Rev 1.3
Date: Thursday, January 13, 2011	Sheet 20 of 99	

+3VS 3,16,17,20,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,59,91,92
+VTT_PCH_ORG +VTT_PCH_ORG 22,26,27
+3VSUS_ORG +3VSUS_ORG 20,22,24,25,27

U2001B

PCI-E*

40 PCIE_RXN1_CR — BG34 PERn1
40 PCIE_RXP1_CR — BJ34 PERp1
40 PCIE_TXN1_CR — AV32 PETn1 — C2105 1 2 0.1UF/16V PCIE_TXN1_CR_C
40 PCIE_TXP1_CR — AU32 PETp1 — C2106 1 2 0.1UF/16V PCIE_TXP1_CR_C

53 PCIE_RXN2_WLAN — BE34 PERn2
53 PCIE_RXP2_WLAN — BE34 PERp2
53 PCIE_TXN2_WLAN — BB32 PETn2 — C2103 1 2 0.1UF/16V PCIE_TXN2_WLAN_C
53 PCIE_TXP2_WLAN — AY32 PETp2 — C2104 1 2 0.1UF/16V PCIE_TXP2_WLAN_C

BG36 PERn3
BJ36 PERp3
AV34 PETn3
AU34 PETp3

59 PCIE_RXN4_USB30 — BF36 PERn4
59 PCIE_RXP4_USB30 — BE36 PERp4
59 PCIE_TXN4_USB30 — AY34 PETn4 — C2111 1 2 0.1UF/16V /U30 PCIE_TXN4_USB30_C
59 PCIE_TXP4_USB30 — BB34 PETp4 — C2110 1 2 0.1UF/16V /U30 PCIE_TXP4_USB30_C

BG37 PERn5
BH37 PERp5
AY36 PETn5
BB36 PETp5

59 PCIE_RXN6_GLAN — BJ38 PERn6
59 PCIE_RXP6_GLAN — BG38 PERp6
59 PCIE_TXN6_GLAN — AU36 PETn6 — C2107 1 2 0.1UF/16V PCIE_TXN6_GLAN_C
59 PCIE_TXP6_GLAN — AV36 PETp6 — C2108 1 2 0.1UF/16V PCIE_TXP6_GLAN_C

BG40 PERn7
BJ40 PERp7
AY40 PETn7
BB40 PETp7

T2135 1 PCIE_RXN8 — BE38 PERn8
T2136 1 PCIE_RXP8 — BC38 PERp8
T2137 1 PCIE_TXN8 — AW38 PETn8
T2138 1 PCIE_TXP8 — AY38 PETp8

T2141 1 SNN_CLK_PCH_SRC0_N — Y40 CLKOUT_PCIE0N
T2142 1 SNN_CLK_PCH_SRC0_P — Y39 CLKOUT_PCIE0P
T2143 1 CLK_REQ0# — J2 PCIECLKRQ0#/GPIO73

40 CLK_PCIE_CR#_PCH — SP2104 1 2 R0402 CLK_PCH_SRC1_N — AB49 CLKOUT_PCIE1N
40 CLK_PCIE_CR_PCH — SP2105 1 2 R0402 CLK_PCH_SRC1_P — AB47 CLKOUT_PCIE1P
40 CLK_REQ1_CR# — SP2106 1 2 R0402 CLK_REQ1# — M1 PCIECLKRQ1#/GPIO18

53 CLK_PCIE_WLAN#_PCH — SP2101 1 2 R0402 CLK_PCH_SRC2_N — AA48 CLKOUT_PCIE2N
53 CLK_PCIE_WLAN_PCH — SP2102 1 2 R0402 CLK_PCH_SRC2_P — AA47 CLKOUT_PCIE2P
53 CLK_REQ2_WLAN# — SP2103 1 2 R0402 CLK_REQ2# — V10 PCIECLKRQ2#/GPIO20

T2144 1 CLK_PCH_SRC3_N — Y37 CLKOUT_PCIE3N
T2145 1 CLK_PCH_SRC3_P — Y36 CLKOUT_PCIE3P
T2146 1 CLK_REQ3# — A8 PCIECLKRQ3#/GPIO25

59 CLK_PCIE_USB#_PCH — SP2110 1 2 R0402 CLK_PCH_SRC4_N — Y43 CLKOUT_PCIE4N
59 CLK_PCIE_USB_PCH — SP2112 1 2 R0402 CLK_PCH_SRC4_P — Y45 CLKOUT_PCIE4P
59 CLK_REQ4_USB30# — CLK_REQ4_USB30# SP2113 1 2 R0402 CLK_REQ4# — L12 PCIECLKRQ4#/GPIO26
R1.1

V45 CLKOUT_PCIE5N
V46 CLKOUT_PCIE5P
CLK_REQ5# — L14 PCIECLKRQ5#/GPIO44

T2147 1 SNN_CLK_PCH_PEG_B_N — AB42 CLKOUT_PEG_B_N
T2148 1 SNN_CLK_PCH_PEG_B_P — AB40 CLKOUT_PEG_B_P
T2112 1 CLK_REQ_PEG_B# — E6 PEG_B_CLKRQ#/GPIO56

59 CLK_PCIE_LAN# — SP2107 1 2 R0402 CLK_PCH_SRC6_N — V40 CLKOUT_PCIE6N
59 CLK_PCIE_LAN — SP2108 1 2 R0402 CLK_PCH_SRC6_P — V42 CLKOUT_PCIE6P
59 CLK_REQ6_LAN# — SP2109 1 2 R0402 CLK_REQ6# — T13 PCIECLKRQ6#/GPIO45

V38 CLKOUT_PCIE7N
V37 CLKOUT_PCIE7P
CLK_REQ7# — K12 PCIECLKRQ7#/GPIO46

AK14 CLKOUT_ITPXDP_N
AK13 CLKOUT_ITPXDP_P
no xDP

COUGAR_POINT_ES1

SMBUS

SMBALERT#/GPIO11 — E12 — EXT_SCI# — EXT_SCI# 30
SMBCLK — H14 — SCL_3A — SCL_3A 28
SMBDATA — C9 — SDA_3A — SDA_3A 28

SML0ALERT#/GPIO60 — A12 — DRAMRST_CNTRL_PCH_R — R2101 2 1 0Ohm — DRAMRST_CNTRL_PCH 5
SML0CLK — C8 — SML0_CLK — 1 T2119
SML0DATA — G12 — SML0_DAT — 1 T2120

SML1ALERT#/PCHHOT#/GPIO74 — C13 — SML1ALERT# — 1 T2121
SML1CLK/GPIO58 — E14 — SML1_CLK — SML1_CLK 28
SML1DATA/GPIO75 — M16 — SML1_DAT — SML1_DAT 28
To EC

Controller Link

CL_CLK1 — M7 — 1 T2122
CL_DATA1 — T11 — 1 T2123
CL_RST1# — P10 — 1 T2124

CLOCKS

PEG_A_CLKRQ#/GPIO47 — M10 — CLK_REQ_PEG_A# — SP2114 1 2 R0402 — CLKREQ_PEG# 70

CLKOUT_PEG_A_N — AB37 — CLK_PCIE_PEG#_PCH_L — SP2115 1 2 R0402 — CLK_PCIE_PEG#_PCH 70
CLKOUT_PEG_A_P — AB38 — CLK_PCIE_PEG_PCH_L — SP2116 1 2 R0402 — CLK_PCIE_PEG_PCH 70

CLKOUT_DMI_N — AV22 — CLK_EXP_N 4
CLKOUT_DMI_P — AU22 — CLK_EXP_P 4

CLKOUT_DP_N — AM12 — CLK_DP_N 4
CLKOUT_DP_P — AM13 — CLK_DP_P 4

CLKIN_DMI_N — BF18 — CLK_BUF_EXP_N
CLKIN_DMI_P — BE18 — CLK_BUF_EXP_P

CLKIN_GND1_N — BJ30 — CLK_BUF_CPYCLK_N
CLKIN_GND1_P — BG30 — CLK_BUF_CPYCLK_P

CLKIN_DOT_96N — G24 — CLK_BUF_DOT96_N
CLKIN_DOT_96P — F24 — CLK_BUF_DOT96_P

CLKIN_SATA_N — AK7 — CLK_BUF_CKSSCD_N
CLKIN_SATA_P — AK5 — CLK_BUF_CKSSCD_P

REFCLK14IN — K45 — CLK_BUF_REF14 — R1.2

CLKIN_PCILOOPBACK — H45 — CLK_PCI_FB 24

XTAL25_IN — V47 — XTAL25_IN
XTAL25_OUT — V49 — XTAL25_OUT

XCLK_RCOMP — Y47 — XCLK_COMP — R2106 1 2 90.9Ohm — +VCCDIFFCLKN

FLEX CLOCKS

CLKOUTFLEX0/GPIO64 — K43 — DGPU_EDID_SELECT# — 1 T2140
CLKOUTFLEX1/GPIO65 — F47 — CLK_OUT1 — 1 T2139
CLKOUTFLEX2/GPIO66 — H47
CLKOUTFLEX3/GPIO67 — K49 — DGPU_PRSNT#

Remove CLK_USB48_CR, because CR is PCIE interface.

Remove test point

25-MHz is required in:
1. FCIM
2. BTM for PCH Display Clock generation in Integrated Graphics platforms

R2142 1MOhm 1 2 — R1.3 — R0402 SP2111 — XTAL25_OUT_C 1 2 — C2102 10PF/50V — GND
X2103 25MHZ 1 2 3 4 — C2101 10PF/50V — GND

CLK_BUF_CPYCLK_N — 3 — 10KOhm — 4 — RN2108B
CLK_BUF_CPYCLK_P — 1 — 10KOhm — 2 — RN2108A

CLK_BUF_EXP_N — 1 — 10KOhm — 2 — RN2109A
CLK_BUF_EXP_P — 3 — 10KOhm — 4 — RN2109B
CLK_BUF_DOT96_P — 1 — 10KOhm — 2 — RN2110A
CLK_BUF_DOT96_N — 3 — 10KOhm — 4 — RN2110B
CLK_BUF_CKSSCD_N — 3 — 10KOhm — 4 — RN2111B
CLK_BUF_CKSSCD_P — 1 — 10KOhm — 2 — RN2111A
CLK_BUF_REF14 — R2116 1 2 10KOhm — GND
R1.3
CLOCK TERMINATION for FCIM
Default power-on mode is ICC.

+3VSUS_ORG

EXT_SCI# — R2117 1 2 10KOhm
SCL_3A — 1 2.2KOhm 2 — RN2103A
SDA_3A — 3 2.2KOhm 4 — RN2103B
DRAMRST_CNTRL_PCH — R2120 1 2 1KOhm
SML0_CLK — 1 2.2KOhm 2 — RN2104A
SML0_DAT — 3 2.2KOhm 4 — RN2104B
SML1_CLK — 1 2.2KOhm 2 — RN2105A
SML1_DAT — 3 2.2KOhm 4 — RN2105B
SML1ALERT# — R2125 1 2 10KOhm

+3VS

No need DGPU_EDID_SELECT#

DGPU_PRSNT# — R2126 1 @ 2 10KOhm
DGPU_PRSNT# — R2134 1 2 10KOhm
GND

PCH CLKREQ Setting:
Not connected to device.

+3VSUS_ORG

CLK_REQ0# — R2143 1 2 10KOhm
CLK_REQ3# — 1 10KOhm 2 — RN2106A
CLK_REQ5# — 3 10KOhm 4 — RN2106B
CLK_REQ7# — 3 10KOhm 4 — RN2107B
CLK_REQ_PEG_B# — 1 10KOhm 2 — RN2107A

Connected to device.
Default : Clock free run. (PD 10K).
Reserver 10K PU for power saving purpose.

+3VS

CLK_REQ2_WLAN# — R2133 1 @ 2 10KOhm
CLK_REQ1_CR# — R2135 1 2 10KOhm

EIH

+3VSUS_ORG

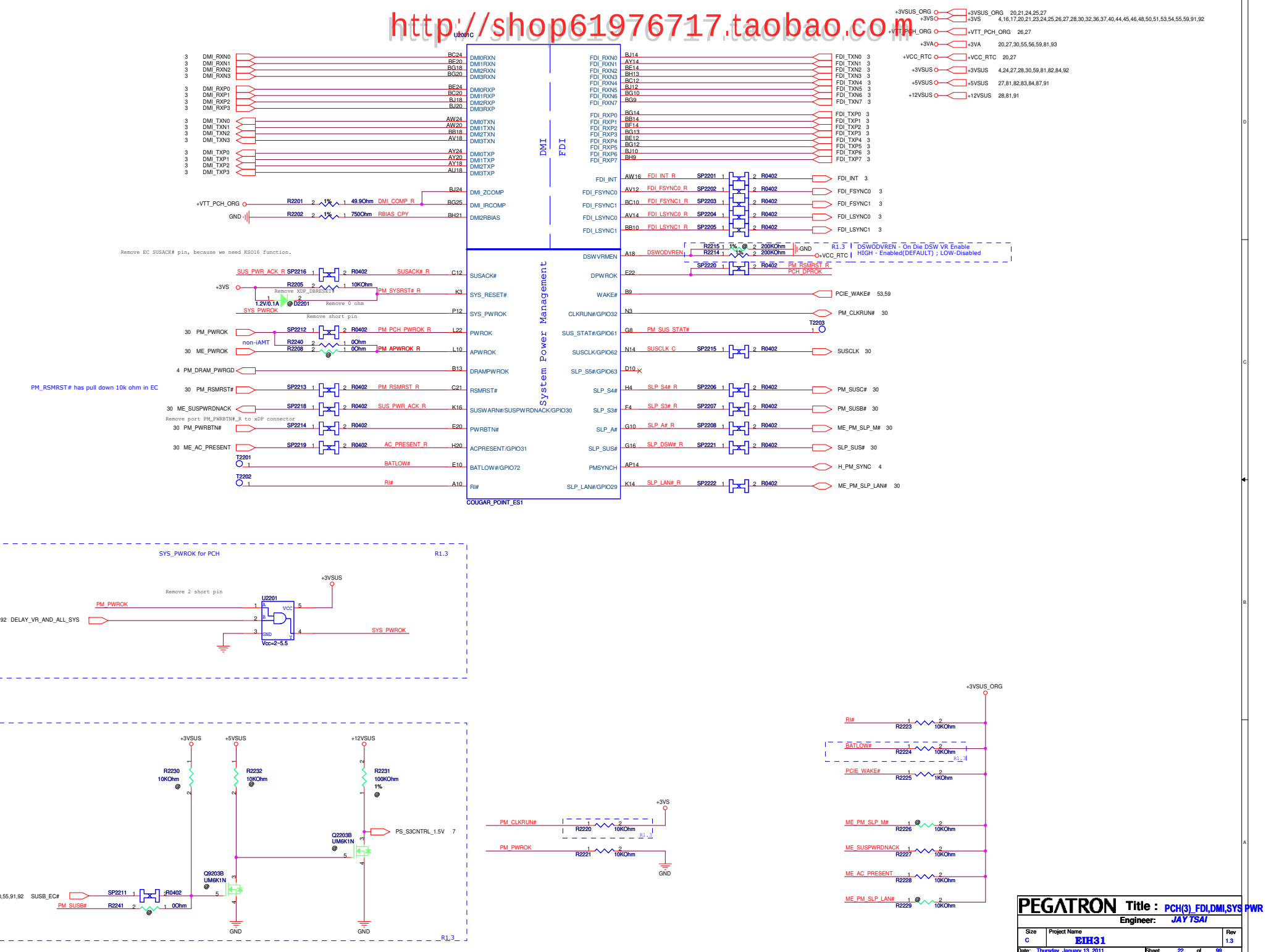
CLK_REQ6_LAN# — R2136 1 2 10KOhm
CLK_REQ4_USB30# — R2149 1 @ 2 10KOhm
CLKREQ_PEG# — R2140 1 2 10KOhm
R1.1
CLKREQ_PEG# — R2141 1 @ 2 10KOhm
CLK_REQ4_USB30# — R2150 1 2 10KOhm
CLK_REQ6_LAN# — R2137 1 @ 2 10KOhm
CLK_REQ2_WLAN# — R2138 1 2 10KOhm
CLK_REQ1_CR# — R2139 1 @ 2 10KOhm

check clk peg option
check clk free run

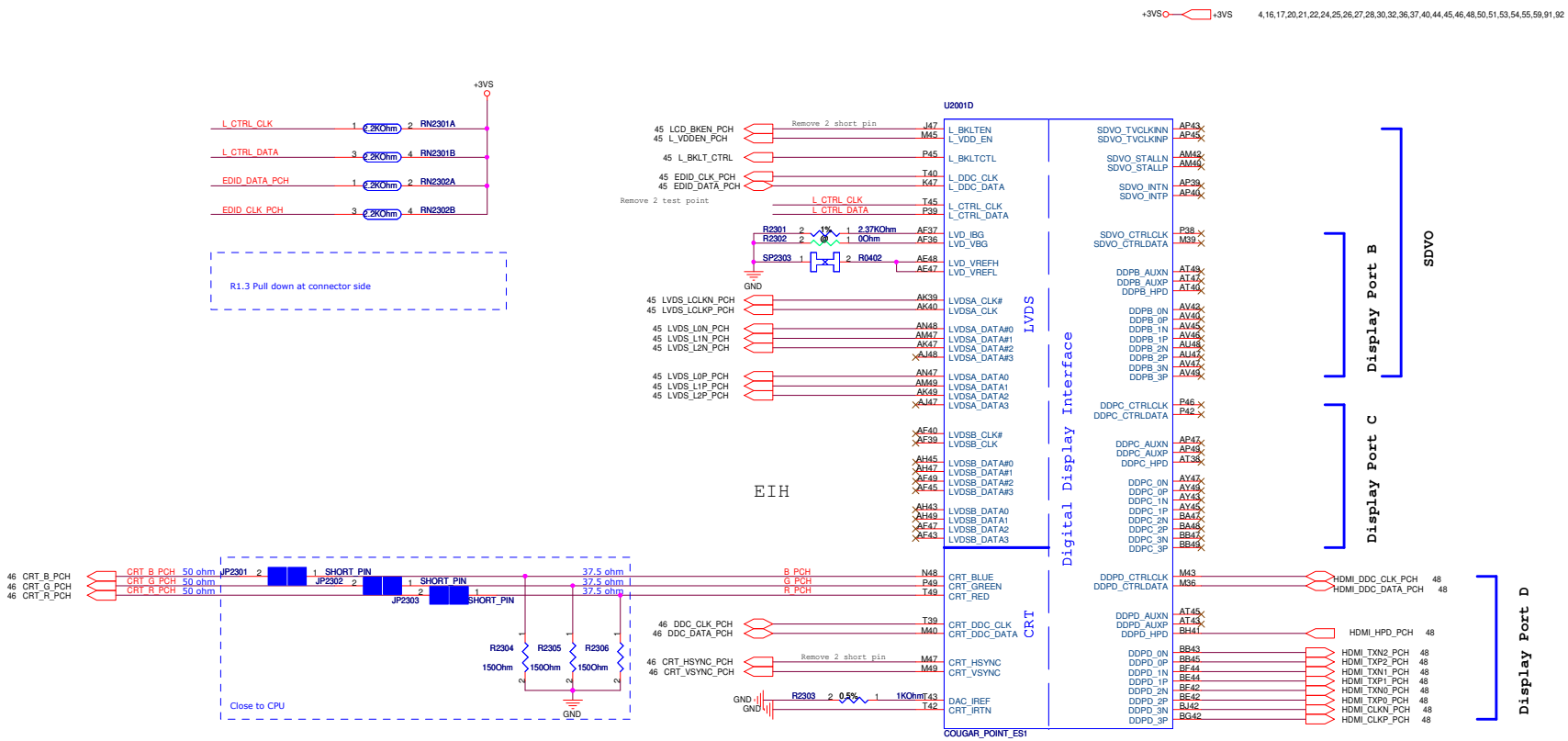
Remove New Card, change to Card Reader at Port 1.

GND

PEGATRON	Title : PCH(2)_PCIE,CLK,SMB,PEG	
	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, January 07, 2011	Sheet 21 of 99	



PEGATRON	Title : PCH(3)_FDI,DMI,SYS PWR	
	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Thursday, January 13, 2011	Sheet 22 of 99	



CRT Disable: (For discrete graphic)

1. NC:

CRT_RED,CRT_GREEN,CRT_BLUE

CRT_HSYCN,CRT_VSYNC

2. 1-kΩ ±0.5% pull-down to GND:

DAC_IREF

3. Connected to GND:

CRT_ITRN

4. Connect to +V3.3:

VCCADAC

DisPlay Port Disable: (For discrete graphic)

1. NC:

ALL

LVDS Disable: (For discrete graphic)

1. NC:

LVDSA_DATA [3:0], LVDSA_DATA# [3:0],

LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],

LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#

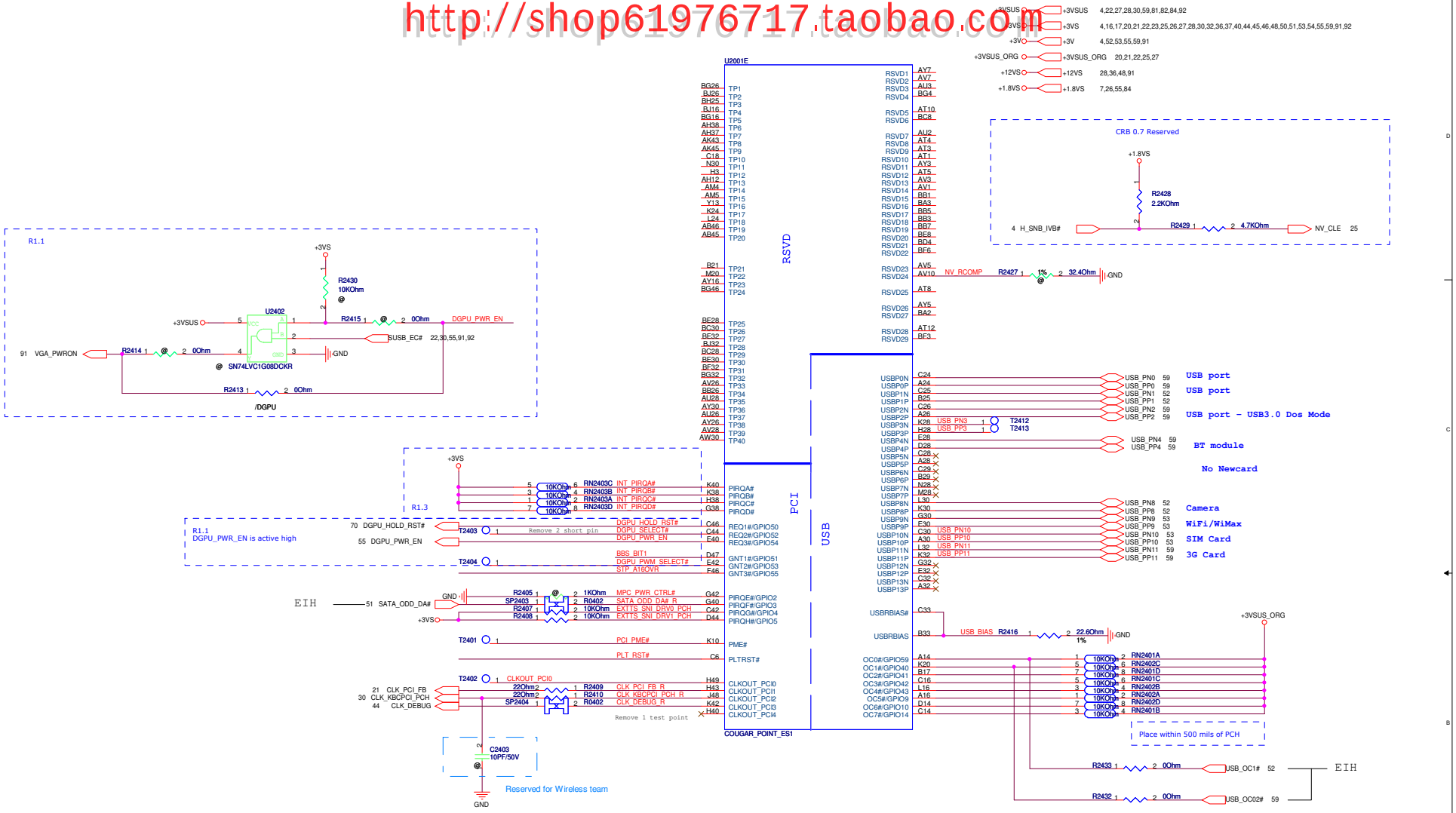
L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH

LVD_VREFL, LVD_IBG, LVD_VBG

2. Connected to GND:

VccALVDS,VccTX_LVDS

PEGATRON	Title : PCH(4)_DP,LVDS,CRT	
	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, January 07, 2011	Sheet 23 of 99	



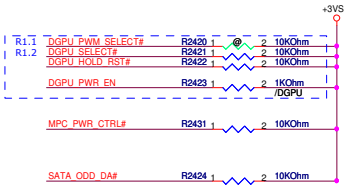
BBS_BIT0,BBS_BIT1 : Boot BIOS Strap

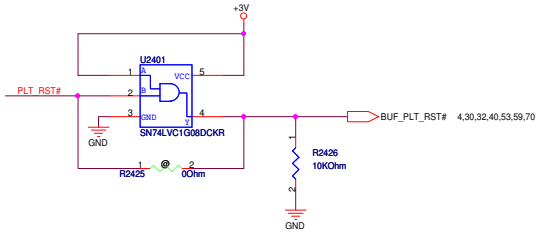
Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	Reserved
1	1	SPI **(PCH)**

Sampled on rising edge of PWROK.

STP_A16OVR:
A16 swap override Strap/
Top-Block swap override jumper

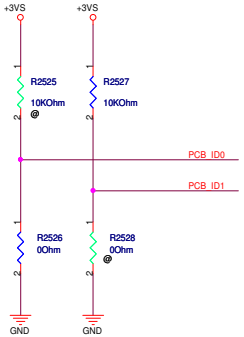
Low=Enabled A16 swap override/ Top-Block swap override
High=Default



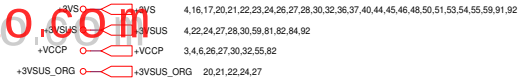


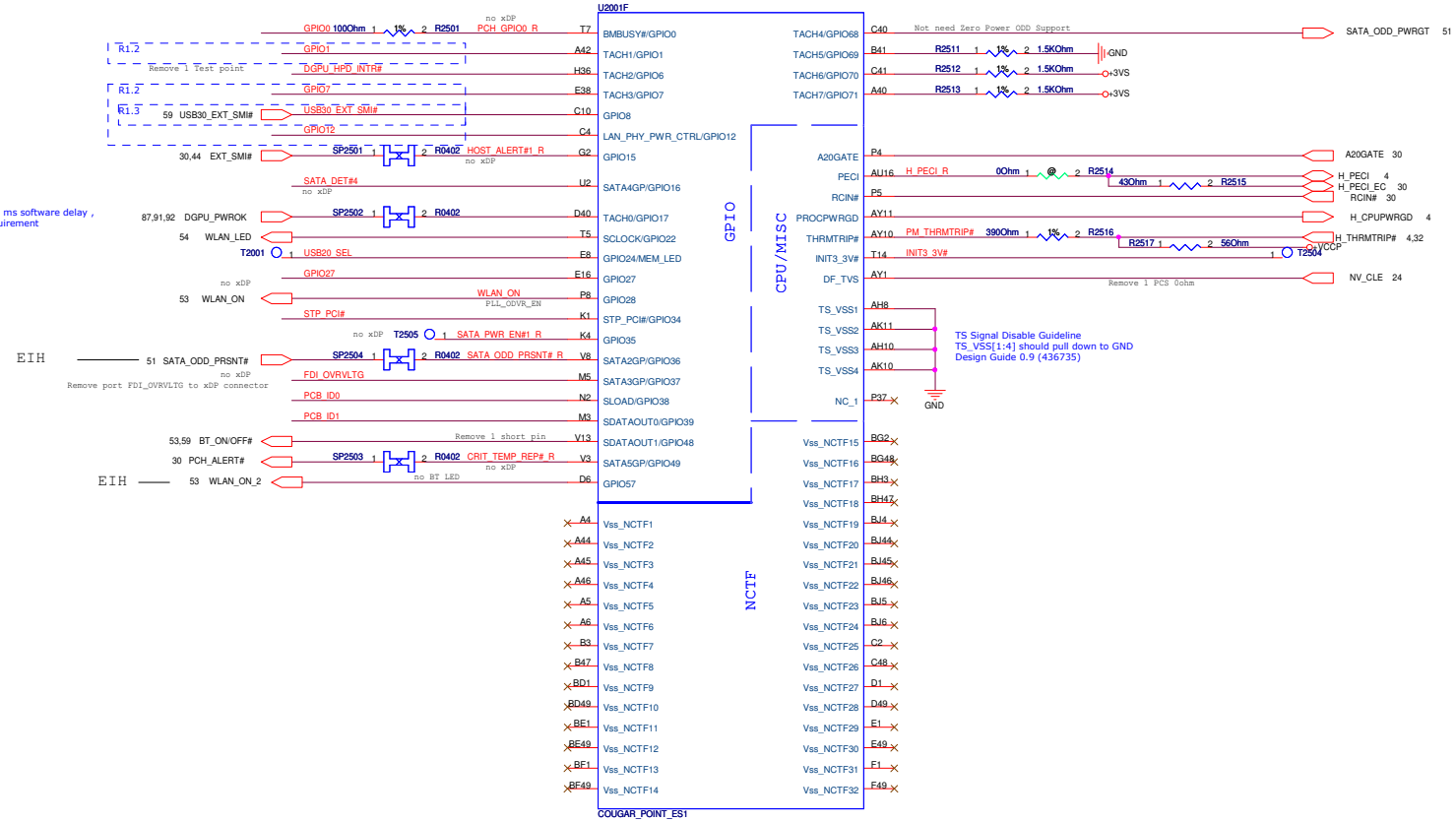
PEGATRON	Title : PCH(5)_PCI,NVRAM,USB	
	Engineer: JAY TSAI	
Size C	Project Name EIH31	Rev 1.3
Date: Friday, January 07, 2011	Sheet 24 of 99	

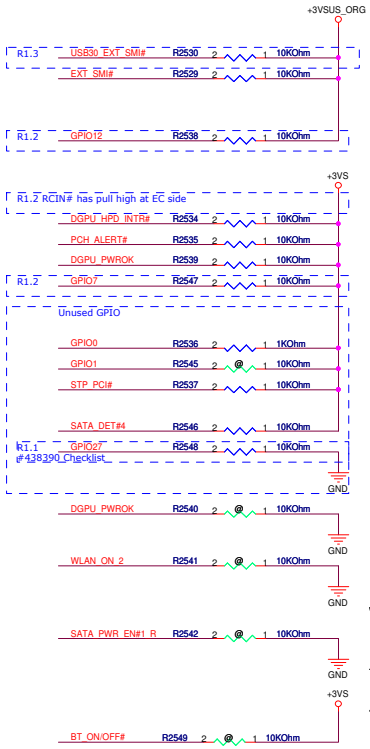
	PCB_ID1	PCB_ID0
SR	L	L
ER	L	H
PR	H	L
MP		



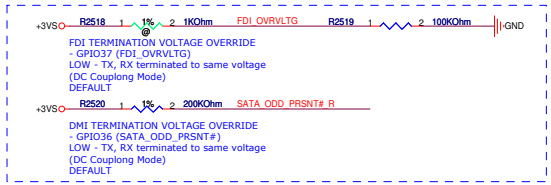
DGPU_PWROK has 100 ms software delay , no hardware delay requirement

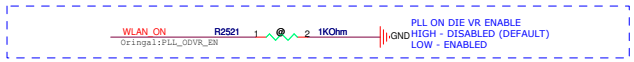




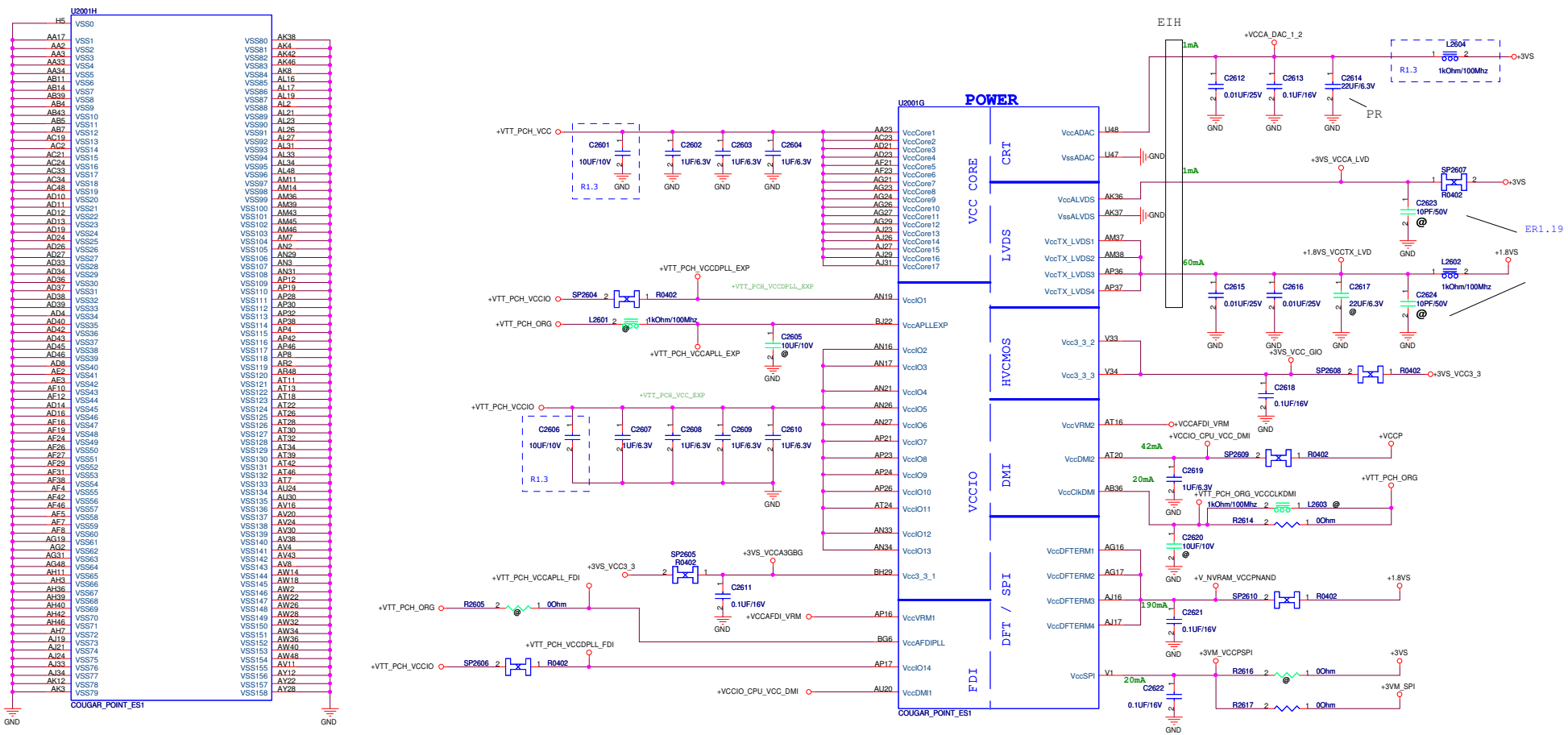


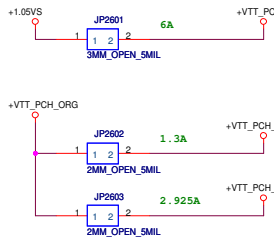
EIH

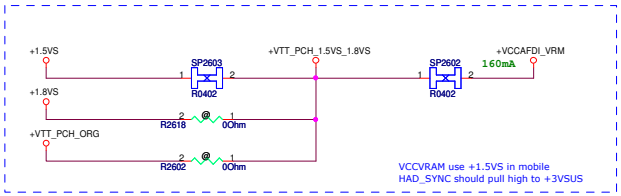




PEGATRON	Title : PCH(6)_CPU,GPIO,MISC	
	Engineer: JAY TSAI	
Size C	Project Name EIH31	Rev 1.3
Date: Thursday, January 13, 2011	Sheet 25 of 99	

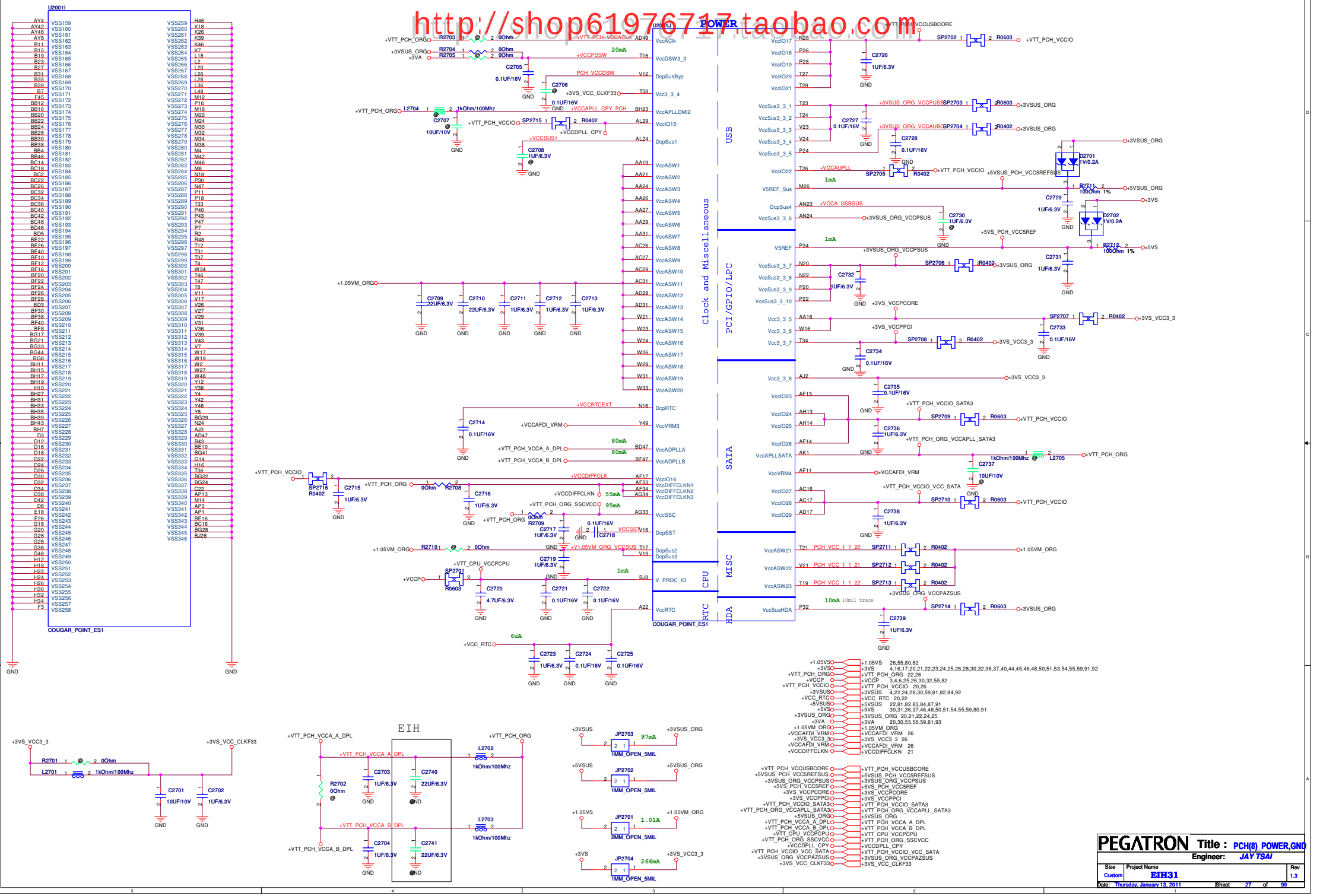




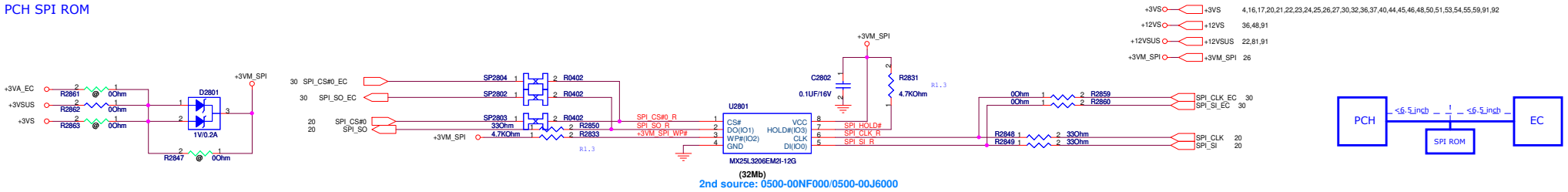


+VTT_PCH_VCC	+VTT_PCH_VCC	
+VTT_PCH_VCCIO	+VTT_PCH_VCCIO	20,27
+VTT_PCH_ORG	+VTT_PCH_ORG	22,27
+VCCP	+VCCP	3,4,6,25,27,30,32,55,82
+1.8VS	+1.8VS	7,24,55,84
+1.5VS	+1.5VS	53,55,91
+3VS	+3VS	4,16,17,20,21,22,23,24,25,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,59,91,92
+1.05VS	+1.05VS	27,55,80,82
+3VS_VCC3_3	+3VS_VCC3_3	27
+3VM_SPI	+3VM_SPI	28
+VCCAFDI_VRM	+VCCAFDI_VRM	27
+3VM_VCCPSPI	+3VM_VCCPSPI	
+VCCIO_CPU_VCC_DMI	+VCCIO_CPU_VCC_DMI	
+V_NVRAM_VCCPNAND	+V_NVRAM_VCCPNAND	
+1.8VS_VCCTX_LVD	+1.8VS_VCCTX_LVD	
+3VS_VCC_GIO	+3VS_VCC_GIO	
+VCCA_DAC_1_2	+VCCA_DAC_1_2	
+VTT_PCH_VCCDPLL_FDI	+VTT_PCH_VCCDPLL_FDI	
+VCCIO_CPU_VCC_DMI	+VCCIO_CPU_VCC_DMI	
+VTT_PCH_VCCAPLL_FDI	+VTT_PCH_VCCAPLL_FDI	
+3VS_VCCA3GBG	+3VS_VCCA3GBG	
+VTT_PCH_VCCDPLL_EXP	+VTT_PCH_VCCDPLL_EXP	
+VTT_PCH_VCCAPLL_EXP	+VTT_PCH_VCCAPLL_EXP	

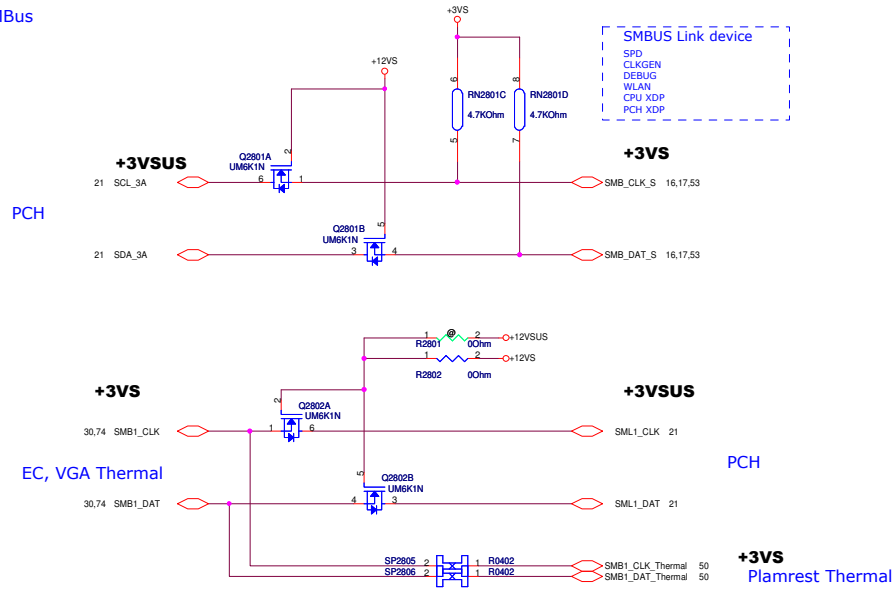
PEGATRON	Title : PCH(7)_POWER,GND		
	Engineer: JAY TSAI		
Size C	Project Name EIH31		Rev 1.3
Date: Thursday, January 13, 2011	Sheet 26 of 99		



PCH SPI ROM



PCH SMBus



remove MOS & pull-hige resitor, because there is the function at page 74

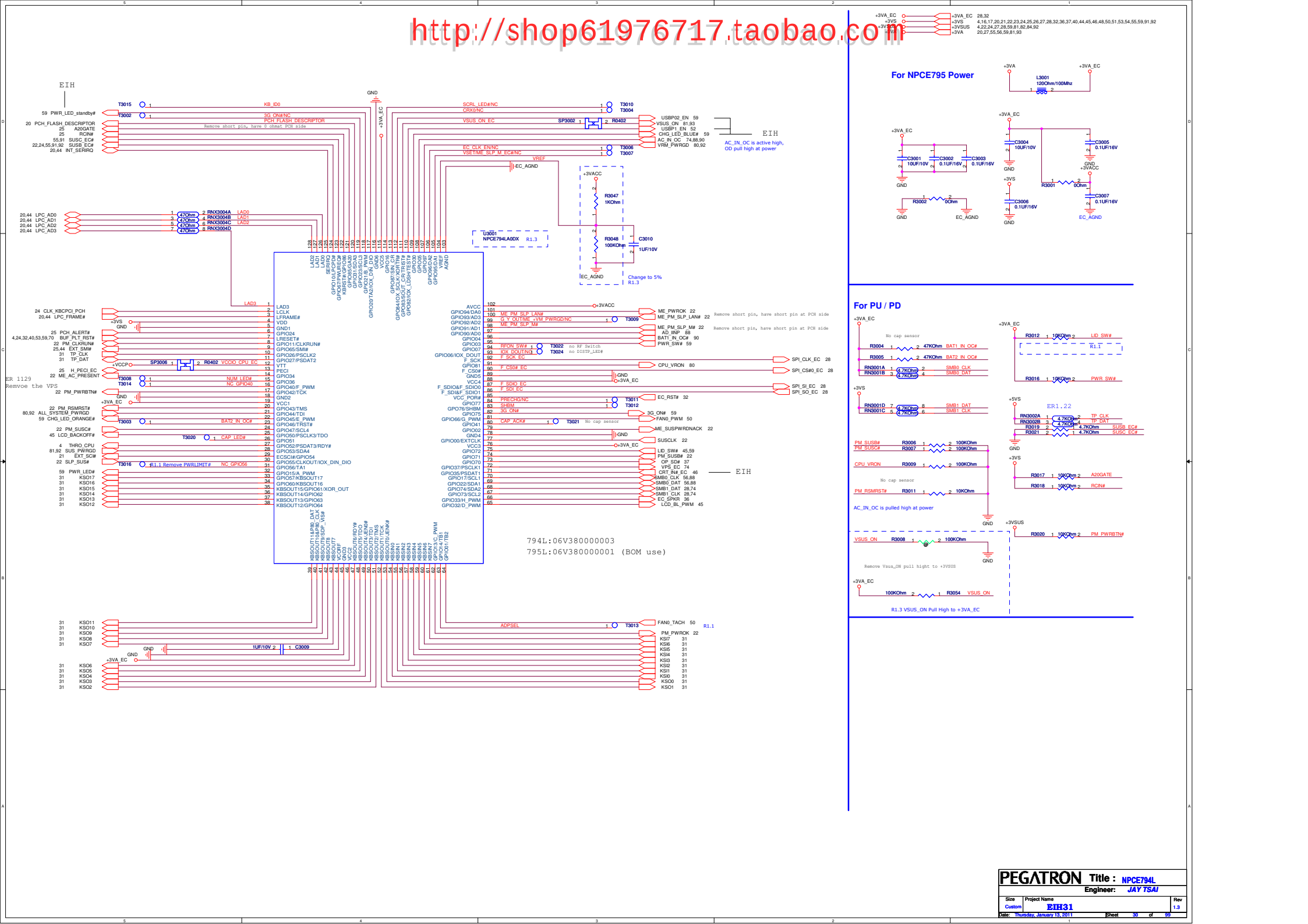
PEGATRON	Title : PCH(9)_SPI,SMB	
	Engineer: JAY TSAI	
Size C	Project Name EIH31	Rev 1.3
Date: Friday, January 07, 2011	Sheet 28 of 99	

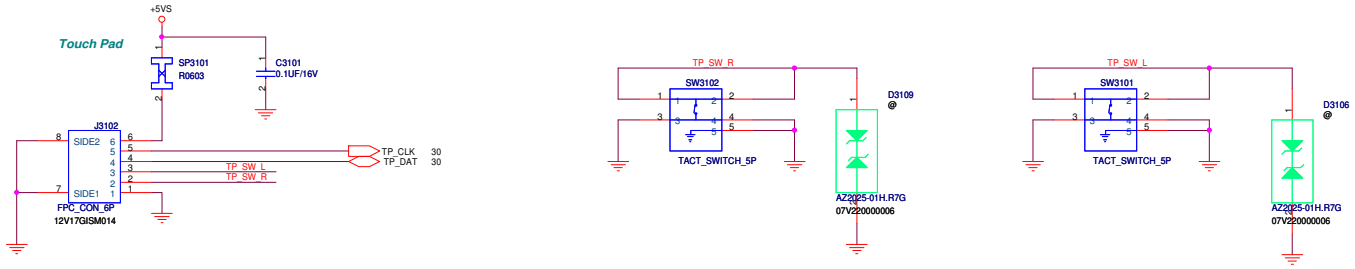
PEGATRON Title : CLK_ICS9LRS3197

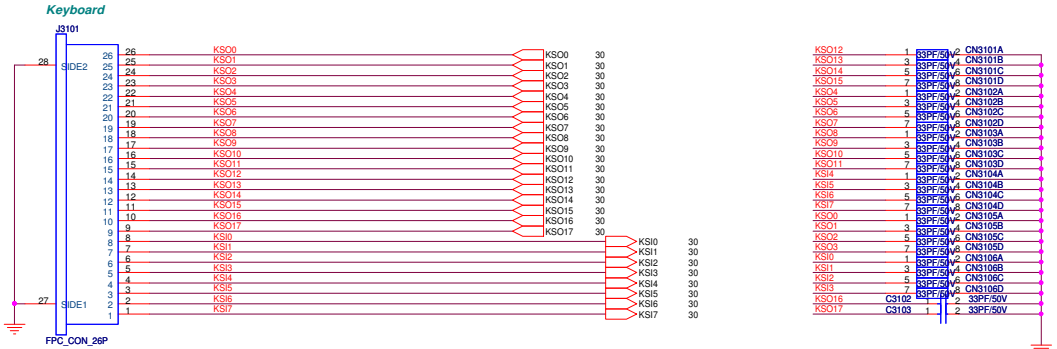
Engineer: JAY TSAI

Size	Project Name	Rev
C	EIH31	1.3

Date: Tuesday, January 04, 2011 Sheet 29 of 99





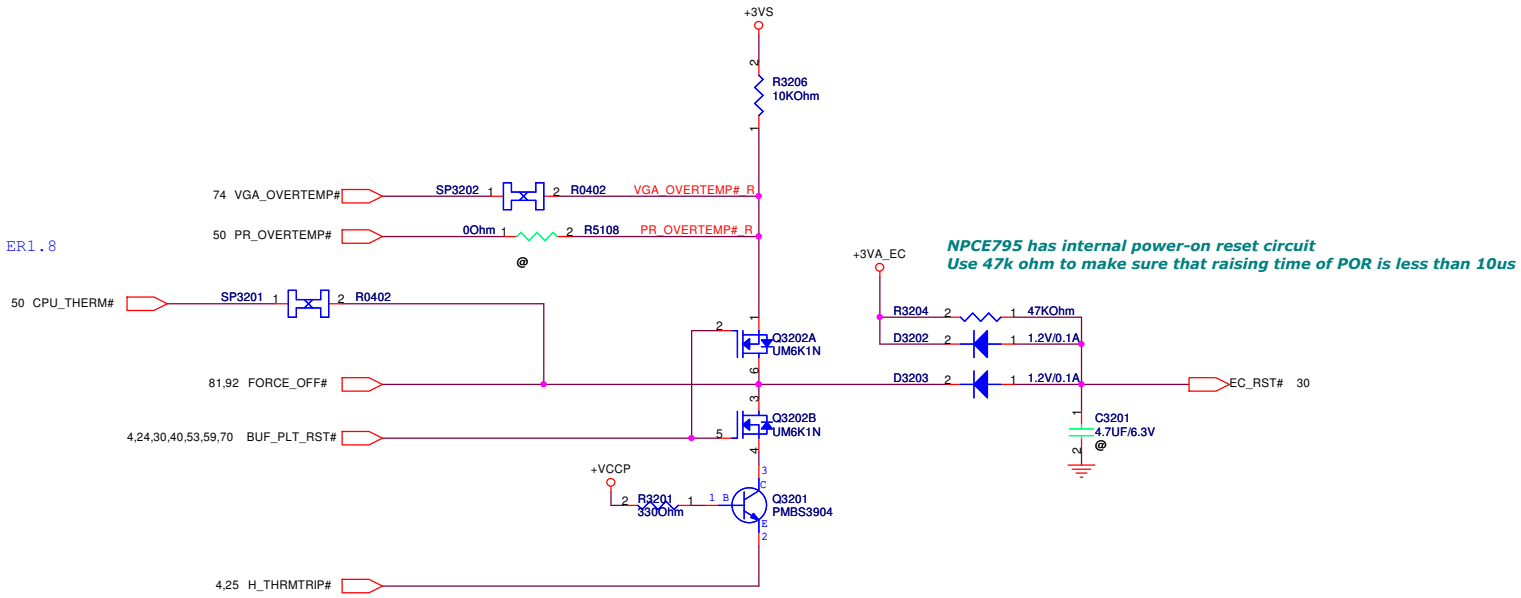


The pin define is checked to keyboard spec. R is KSO, C is KSI. The connector pin define is the same the KB.

PEGATRON	Title : EC_IT8512(2)KB, TP,FP	
	Engineer: JAY TSAI	
Size C	Project Name EIH31	Rev 1.3
Date: Thursday, January 13, 2011	Sheet 31 of 99	

+VCCP +VCCP 3,4,6,25,26,27,30,55,82
+3VA_EC +3VA_EC 28,30
+3VS +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,36,37,40,44,45,46,48,50,51,53,54,55,59,91,92

Thermal Policy



PEGATRON	Title : RST_Reset Circuit		
<OrgName>	Engineer: JAY TSAI		
Size: Custom	Project Name: EIH31		Rev: 1.0
Date: Thursday, January 13, 2011	Sheet 32 of 99		

PEGATRON	Title : MDC CONN		
<OrgName>	Engineer: JAY TSAI		
Size C	Project Name EIH31		Rev 1.3
Date: Tuesday, January 04, 2011	Sheet 35 of 99		

Audio Codec

DIGITAL ANALOG

Intel 1.01 Design Guide update #440484
R1.3 use dual mosfet

+12VS, SP3603 R0402, UM6K1N Q3604B, R3618 0Ohm, 20 ACZ_SDOUT_AUD
+12VS, SP3604 R0402, UM6K1N Q3604A, R3603 0Ohm, 20 ACZ_SYNC_AUD, ACZ_SYNC_AUD_R, ACZ_SDOUT_AUD_R

+5VS, +3VS, +5VS_AUDIO — +5VS 27,30,31,37,46,48,50,51,54,55,59,80,91; +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,32,37,40,44,45,46,48,50,51,53,54,55,59,91,92; +5VS_AUDIO 37

+5VS_AMP, SP3606 R0805, +5VS

H_SPKR+ 37, H_SPKR- 37, H_SPKL- 37, H_SPKL+ 37

R3610 0Ohm; C3634 10UF/10V @; C3628 0.1UF/16V @; C3615 10UF/10V; C3609 0.1UF/16V

Short 0 ohm: C3623 0.1UF/16V; C3620 10UF/10V; C3636 0.1UF/16V; C3638 10UF/10V @

+5VS, +5VS_AUDIO, L3603 80Ohm/100Mhz vx_l0805_h43_small Irat=2A, >30 mil or shape

37 EAPD, C3639 10UF/10V @, T3602

ER 1.8

SPDIF OUT

+3VS, +3VS_DVDD, L3602 120Ohm/100Mhz, C3616 10UF/10V, C3617 0.1UF/16V @, C3618 0.1UF/16V

U3601A ALC271X-VB3-GR 02V0J0000004

GND, SPDIFO, EAPD, PVDD2, SPK-OUT-R+, SPK-OUT-R-, PVSS2, SPK-OUT-L-, SPK-OUT-L+, PVDD1, AVDD2, AVSS2

DVDD, GPIO0/DMIC-DATA, GPIO1/DMIC-CLK, PD#, SDATA-OUT, BCLK, DVSS2, SDATA-IN, DVDD-IO, SYNC, RESET#, PCBEEP

T3603, T3604, 37 MUTE_AMP#, ACZ_SDOUT_AUD_R, 20 ACZ_BCLK_AUD, ACZ_BCLK_AUD, 20 ACZ_SDIN0_AUD, R3625 33Ohm, ACZ_SYNC_AUD_R, 20,37 ACZ_RST#_AUD, PC_BEEP, +3VS, C3633 0.1UF/16V

Check R3625 resistor value, ACZ_BCLK_AUD, C3629 22PF/50V

SenseA, LINE2-L(PORT-E-L), LINE2-R(PORT-E-R), MIC2-L(PORT-F-L), MIC2-R(PORT-F-R), Sense B, VREF, MONO-OUT, MIC1-L(PORT-B-L), MIC1-R(PORT-B-R), LINE1-L(PORT-C-L), LINE1-R(PORT-C-R)

CBP, CBN, CPVEE, HPOUT-R(PORT-I-R), HPOUT-L(PORT-I-L), MIC1-VREFO-L, MIC1-VREFO-R, MIC2-VREFO, LDO-CAP, VREF, AVSS1, AVDD1

C3626 2.2UF/10V, C3627 2.2UF/10V, GND_AUDIO, AC_HP_R, AC_HP_L, AUD_LDO_CAP, VREF_CODEC, +5VS_AUDIO, C3614 0.1UF/16V, C3632 10UF/10V, C3613 0.1UF/16V, C3611 2.2UF/10V

ER 1129
Change the PART & SYMBOL (8VIA)

HeadPhone Out

AC_HP_R 37, AC_HP_L 37, MIC1_VREFO 37, MIC_VREFO 37, MIC2_VREFO 37

EXT MIC Vref.
EXT MIC Vref.
COMBO MIC Vref.
INT MIC Vref.

MIC1_VREFO, MIC_VREFO, MIC2_VREFO, AUD_LDO_CAP
C3612 10UF/10V, C3624 10UF/10V @, C3619 10UF/10V, C3625 10UF/10V @
GND_AUDIO, GND_AUDIO, GND_AUDIO, GND_AUDIO

HP Jack Detect
EXT MIC Detect

37 HPOUT_JD#, 37 MIC1_JD#, R3619 39.2KOhm 1%, R3613 20KOhm 1%

INT MIC IN

AUD_LDO_CAP, R3628 4.7KOhm, R3629 1KOhm, 52 INT_MIC_AC_IN, C3630 1UF/10V, C3631 1UF/10V, INT_MIC_AC_IN_L, INT_MIC_AC_IN_R

C3635 2.2UF/10V, C3637 2.2UF/10V, EXT_MIC_AC_IN_R, EXT_MIC_AC_IN_L, R3630 1KOhm, R3631 1KOhm, EXT_MIC_R 37, EXT_MIC_L 37

EXT MIC IN

37 MIC2_L, 37 MIC2_R, 37 MIC2_JD#, R3620 20KOhm 1%, R3616 20KOhm 1%, GND_AUDIO

R3605 0Ohm, D3601 1V/0.2A, 20 SB_SPKR, 30 EC_SPKR, R3611 0Ohm, R3614 47KOhm, R3615 4.7KOhm, C3621 100PF/50V @, PC_BEEP_C, C3622 0.1UF/16V, PC_BEEP

ER1.2

U3601B ALC271X-VB3-GR 02V0J0000004
GND1, GND2, GND3, GND4, GND8, GND7, GND6, GND5

ER 1129
Change the PART & SYMBOL (8VIA)

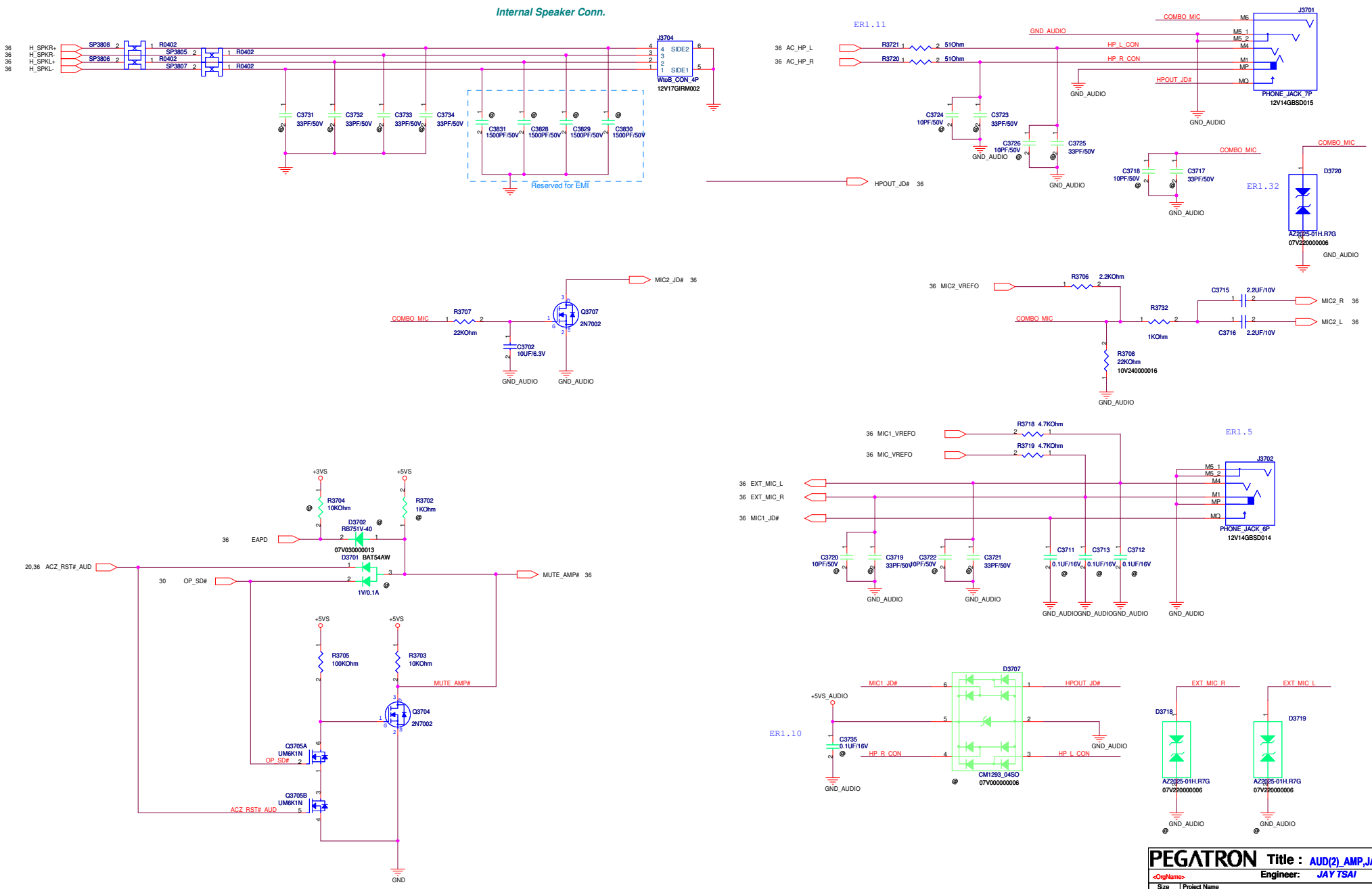
R3606 0Ohm, R3626 0Ohm @, GND_AUDIO
R3602 0Ohm, R3627 0Ohm @, GND_AUDIO

R3609 0Ohm @, R3608 0Ohm @, R3607 0Ohm @, R3604 0Ohm @, GND_AUDIO

add R3607&R3606&R3605 c3499 for EMI

PEGATRON	Title : AUD(1)_ALC269		
<OrgName>	Engineer: JAY TSAI		
Size C	Project Name EIH31		Rev 1.1
Date: Thursday, January 13, 2011	Sheet 36 of 99		

+5VS — +5VS 27,30,31,36,46,48,50,51,54,55,59,80,91
+3VS — +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,40,44,45,46,48,50,51,53,54,55,59,91,92
+5VS_AUDIO — +5VS_AUDIO 36



PEGATRON	Title : AUD(2)_AMP,JACK	
<OrgName>	Engineer: JAY TSAI	
Size C	Project Name EIH31	Rev 1.3
Date: Thursday, January 13, 2011	Sheet 37 of 99	

PEGATRON	Title : AUD(3)_FM2010		
<OrgName>	Engineer: JAY TSAI		
Size C	Project Name EIH31		Rev 1.3
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PEGATRON	Title : AUD(4)_****		
<OrgName>	Engineer: JAY TSAI		
Size: Custom	Project Name: EIH31		Rev: 1.3
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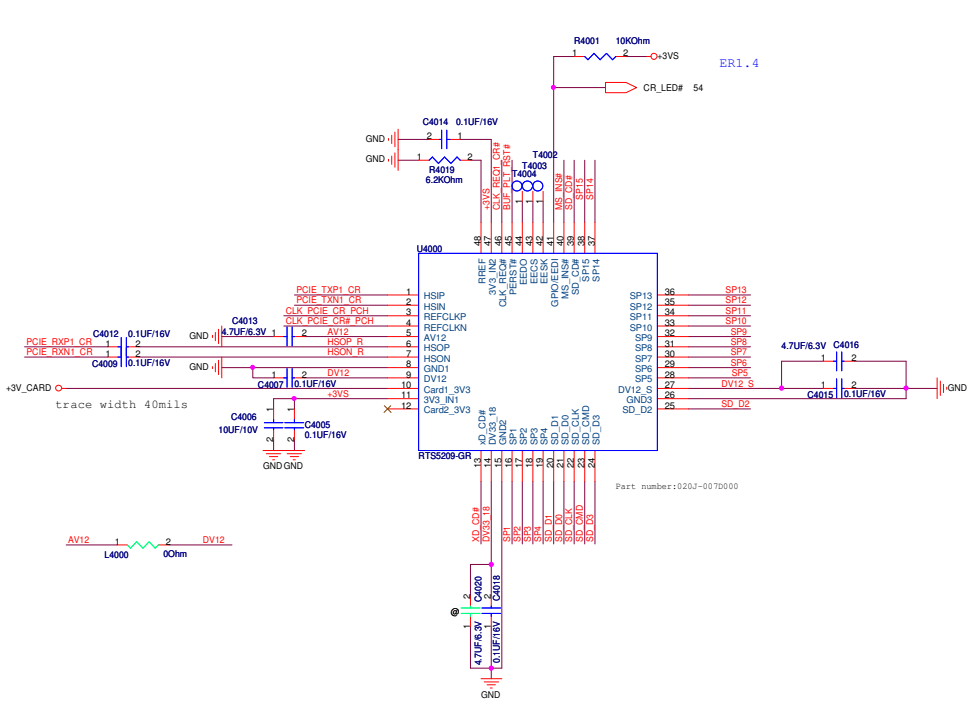
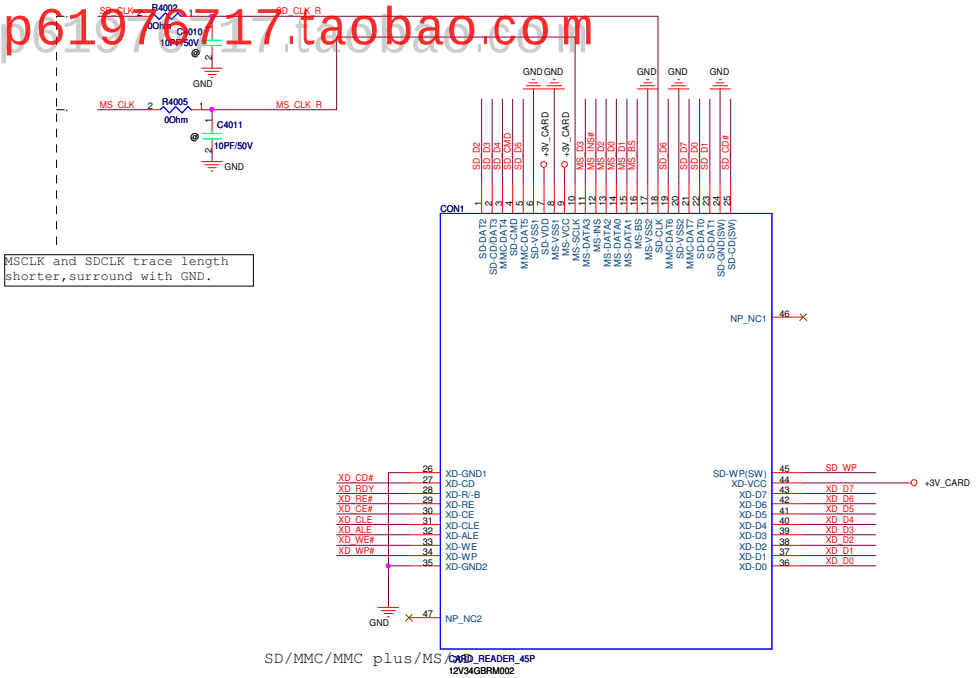
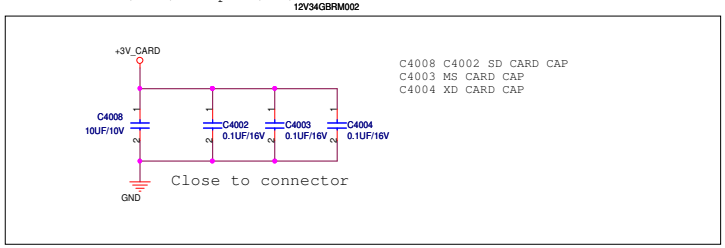
From System's PCIE interface





MSCLK and SDCLK trace length shorter,surround with GND.

SD/MMC/MMC plus/MS/XD



C4008 C4002 SD CARD CAP
C4003 MS CARD CAP
C4004 XD CARD CAP

Pin Name	Description
SP1	SD_D7/XD_RDY
SP2	SD_D6/XD_RE#
SP3	SD_D5/XD_CE#
SP4	SD_D4/XD_WE#
SP5	MS_BS/XD_CLE
SP6	MS_D5/XD_ALE
SP7	MS_D1/XD_WP#
SP8	MS_D4/XD_D0
SP9	MS_D0/XD_D1
SP10	MS_D2/XD_D2
SP11	MS_D6/XD_D3
SP12	MS_D3/XD_D4
SP13	MS_D7/XD_D5
SP14	MS_CLK/XD_D6
SP15	SD_WP/XD_D7

SP1	SD_D7	XD_RDY
SP2	SD_D6	XD_RE#
SP3	SD_D5	XD_CE#
SP4	SD_D4	XD_WE#
SP5	MS_BS	XD_CLE
SP6	MS_D5	XD_ALE
SP7	MS_D1	XD_WP#
SP8	MS_D4	XD_D0
SP9	MS_D0	XD_D1
SP10	MS_D2	XD_D2
SP11	MS_D6	XD_D3
SP12	MS_D3	XD_D4
SP13	MS_D7	XD_D5
SP14	MS_CLK	XD_D6
SP15	SD_WP	XD_D7

Share Pin

Remove Serial Flash

Reserve for BIOS boot function

When EECS switch to be D3-Delink sideband signal, Serial Flash function is disabled.

PEGATRON Title : RTS5209
<OrgName> Engineer:
Size C | Project Name EIH31 | Rev 0.1
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PEGATRON	Title : CB(2)_R5C833		
<OrgName>	Engineer: JAY TSAI		
Size C	Project Name EIH31		Rev 1.3
Date: Tuesday, January 04, 2011	Sheet 41 of 99		

4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,59,91,92

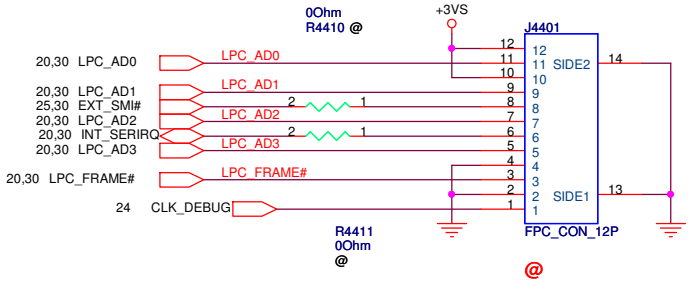
91

PEGATRON	Title : CB(3)_4in1 CardReader	
<OrgName>	Engineer: JAY TSAI	
Size C	Project Name EIH31	Rev 1.3
Date: Friday, January 07, 2011	Sheet 42 of 99	

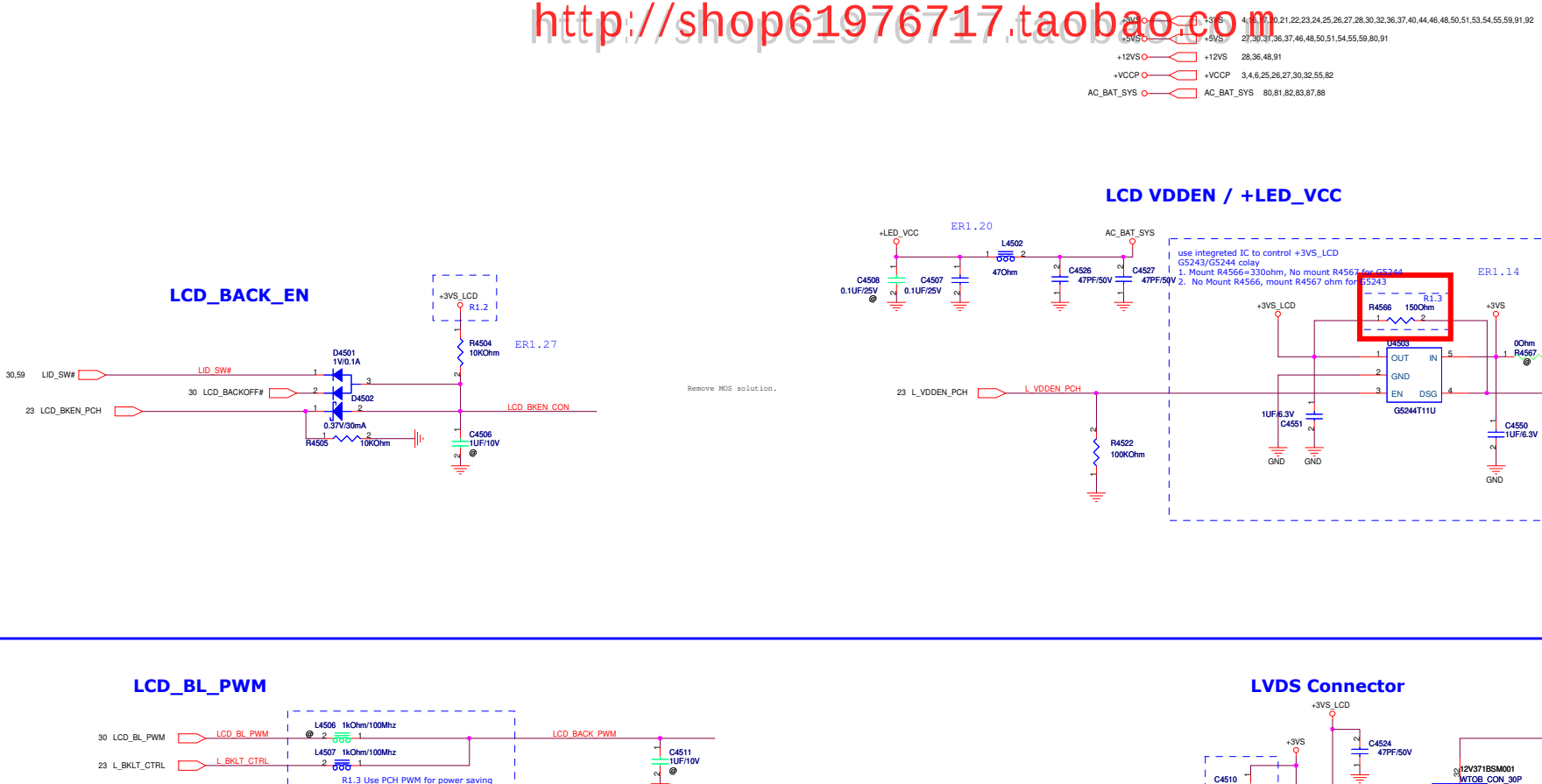
PEGATRON	Title : CB(4)_NewCard		
<OrgName>	Engineer: JAY TSAI		
Size C	Project Name EIH31		Rev 1.3
Date: Tuesday, January 04, 2011	Sheet 43 of 99		

+3VS +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,45,46,48,50,51,53,54,55,59,91,92

LPC Debug Port

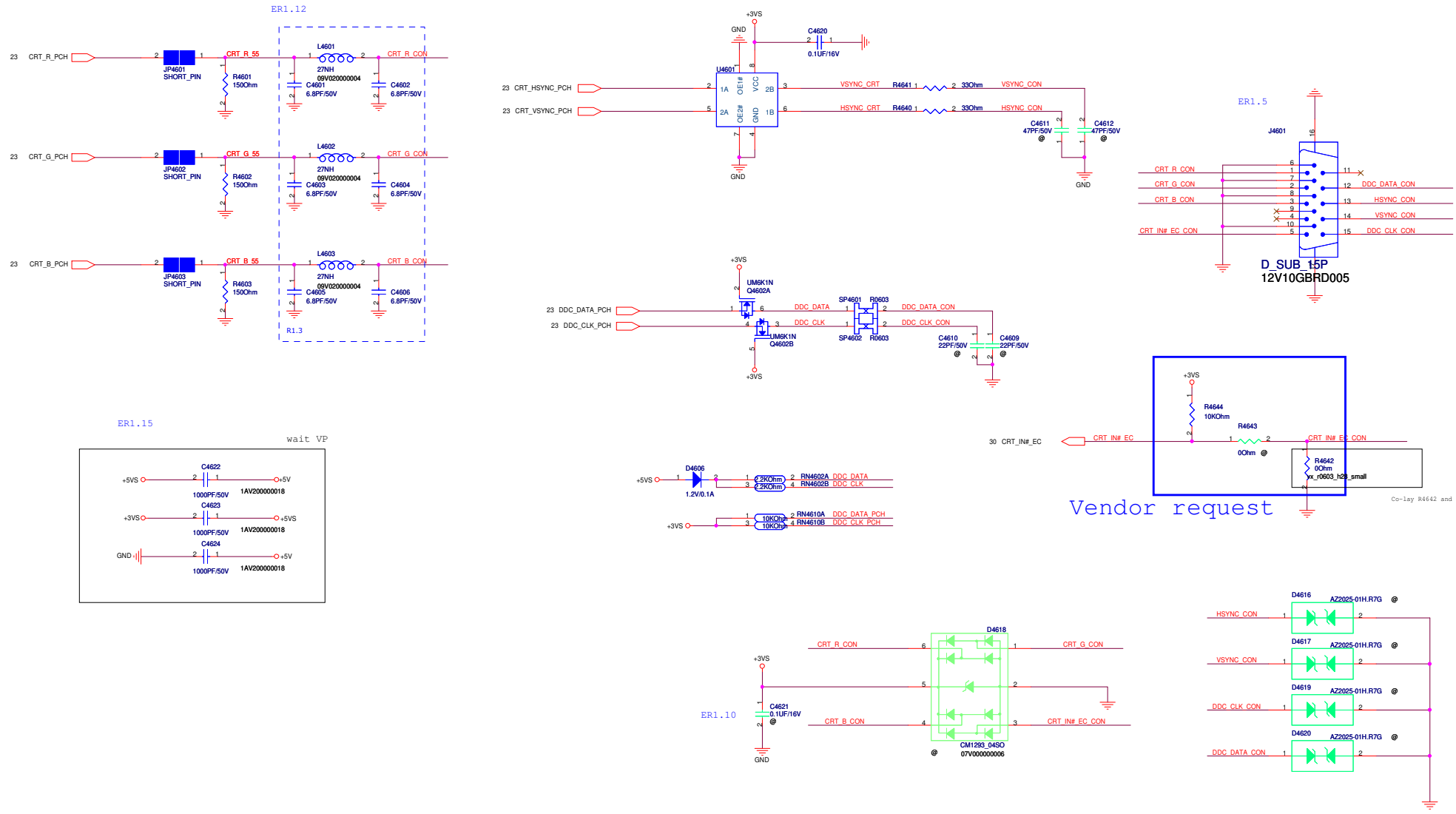


PEGATRON	Title : BUG_Debug	
<OrgName>	Engineer: JAY TSAI	
Size B	Project Name EIH31	Rev 1.3
Date: Thursday, January 13, 2011	Sheet 44 of 99	



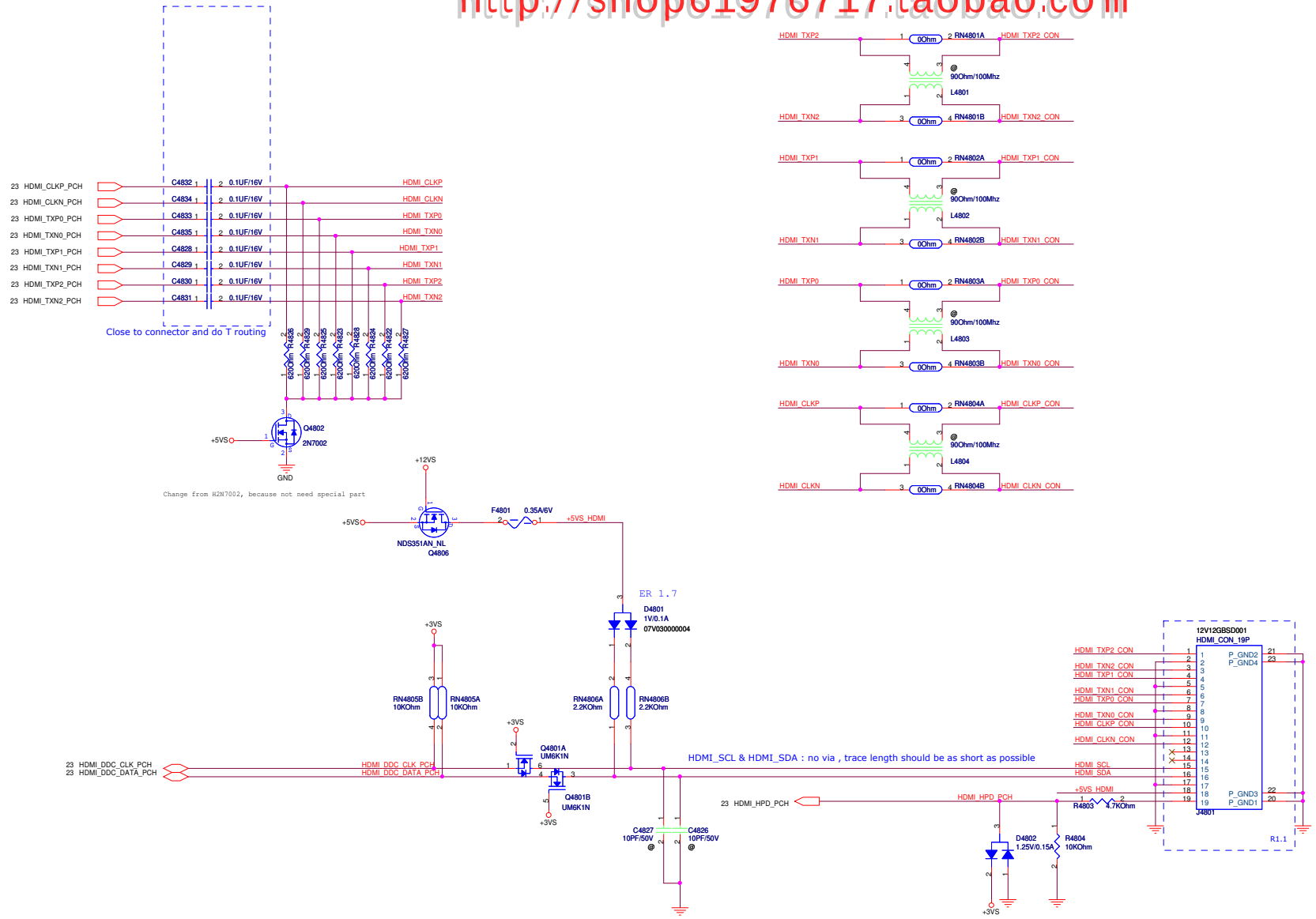
PEGATRON	Title : CRT(1)_LVDS		
<OrgName>	Engineer: JAY TSAI		
Size C	Project Name EIH31		Rev 1.3
Date: Thursday, January 13, 2011	Sheet 45 of 99		

+3VS — +3VS — 4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,48,50,51,53,54,55,59,91,92
+5V — +5V — 52,55,59,91
+5VS — +5VS — 27,30,31,36,37,48,50,51,54,55,59,80,91



PEGATRON	Title : CRT(2)_D-Sub	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Thursday, January 13, 2011	Sheet 46 of 99	

PEGATRON	Title : CRT(3)_Display Port		
<OrgName>	Engineer: JAY TSAI		
Size C	Project Name EIH31		Rev 1.3
Date: Tuesday, January 04, 2011	Sheet 47 of 99		



+12VS	+12VS	28,36,91
+3VS_VGA	+3VS_VGA	55,70,72,74,91
+3VS	+3VS	4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,50,51,53,54,55,59,91,92
+5VS	+5VS	27,30,31,36,37,46,50,51,54,55,59,80,91

PEGATRON Title : TV(1)_HDMI

<OrgName> Engineer: JAY TSAI

Size	Project Name	Rev
C	EIH31	1.3

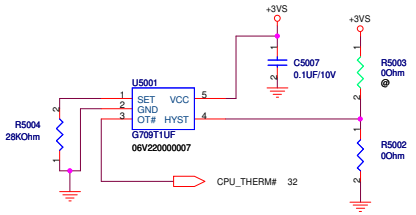
Date: Friday, January 07, 2011 Sheet 48 of 99

PEGATRON	Title : TV(2)_****		
<OrgName>	Engineer: JAY TSAI		
Size C	Project Name EIH31		Rev 1.3
Date: Tuesday, January 04, 2011	Sheet 49 of 99		

+3VS +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,51,53,54,55,59,91,92

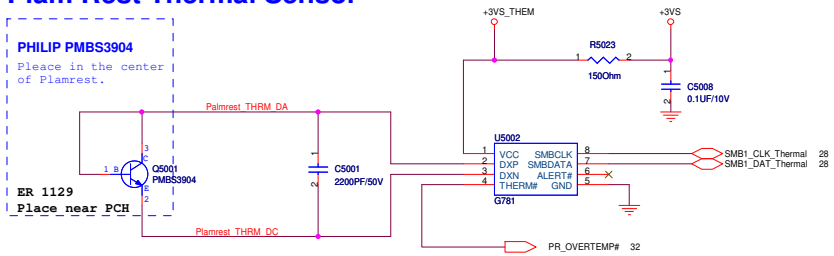
+5VS +5VS 27,30,31,36,37,46,48,51,54,55,59,80,91

CPU Thermal Sensor



(10°C for HYST =VCC)
(2°C for HYST = GND)
Hysteresis prevents the output from oscillating when the temperature is near the trip point.

Plam Rest Thermal Sensor

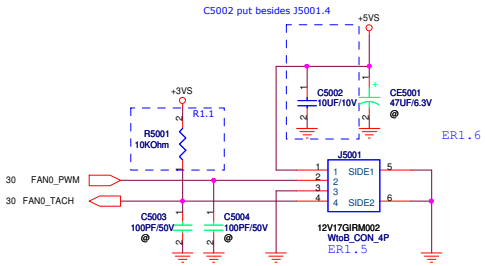


U5002 under palmrest

SMBUS addr=1001100x (98)

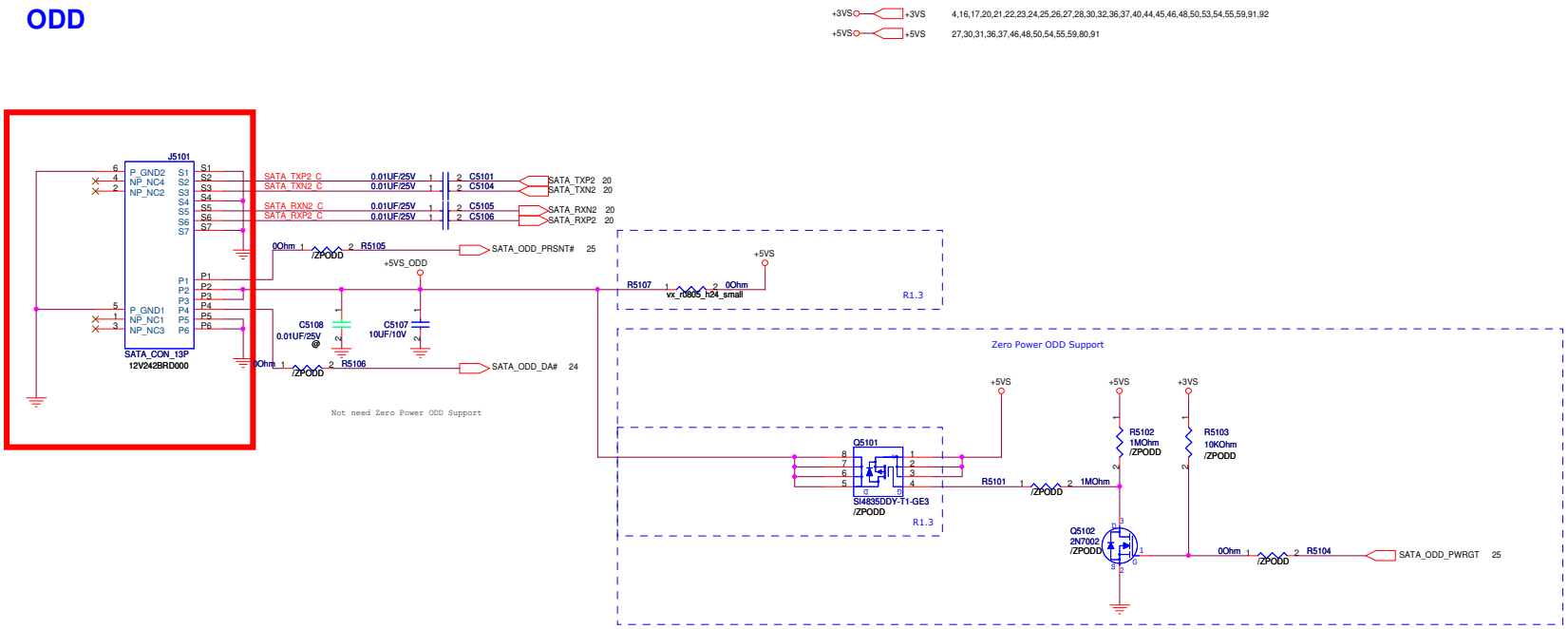
U5002: Remote(Local) thermal sensor,use remote mode.

PWM Fan

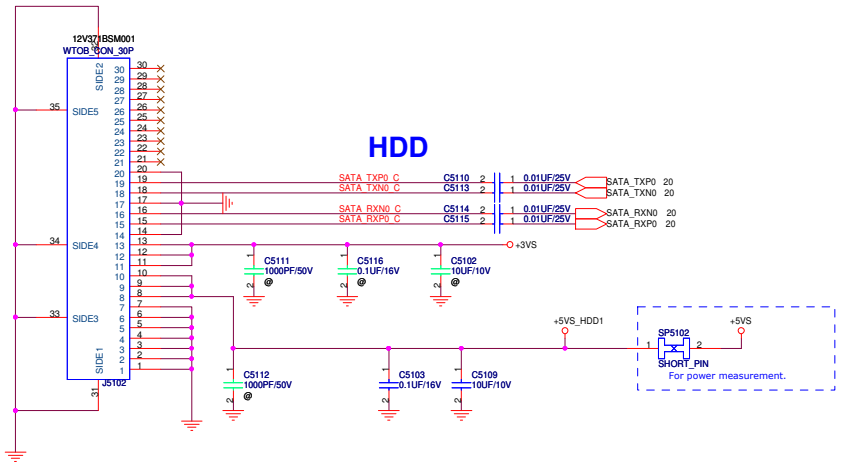


PEGATRON	Title : FAN_Fan,Sensor	
<OrgName>	Engineer: JAY TSAI	
Size C	Project Name EIH31	Rev 2.0
Date: Thursday, January 13, 2011	Sheet 50 of 99	

ODD

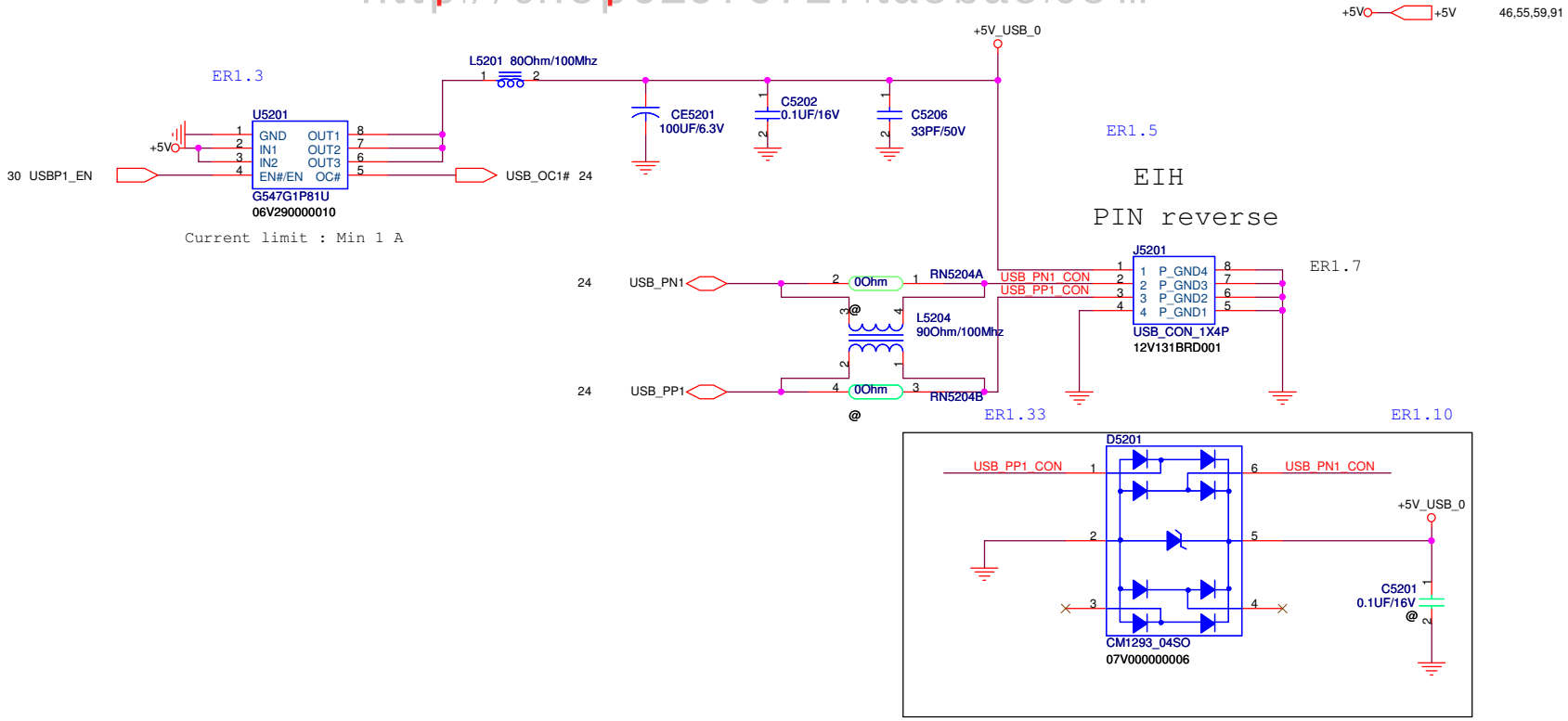


HDD

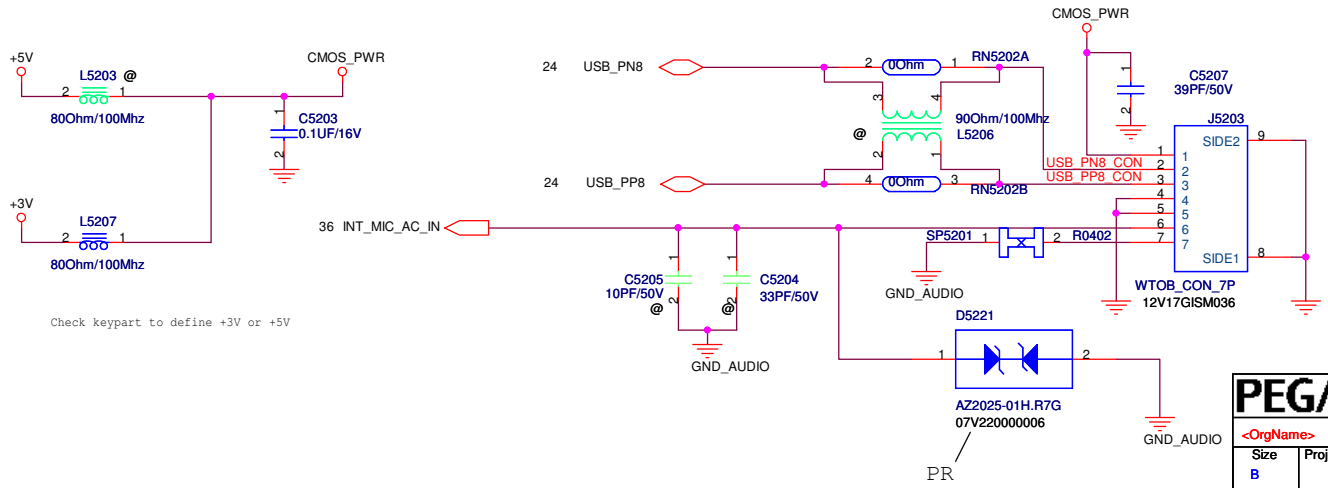


PEGATRON	Title : XDD_HDD,ODD		
<OrgName>	Engineer: JAY TSAI		
Size C	Project Name EIH31		Rev 1.3
Date: Friday, January 07, 2011	Sheet 51 of 99		

USB ports



Camera



PEGATRON	Title : USB_USB Port	
<OrgName>	Engineer: JAY TSAI	
Size B	Project Name EIH31	Rev 1.3
Date: Thursday, January 13, 2011	Sheet 52 of 99	

WLAN

Rainbow Peak

J5302 — MINI_PCI_LATCH_52P
12V44GBSD000
1244-0032000

H =9mm

Vendor request

Vendor request

Vendor request

+3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,54,55,59,91,92
+3VSUS 4,22,24,27,28,30,59,81,82,84,92
+1.5VS 26,55,91

22,59 PCIE_WAKE#
PCIE_WAKE# WLAN
2N7002
R5336 0Ohm
C5323

BT Disable Low for CHICONY
25,59 BT_ON/OFF#
BT_ON/OFF# R5315 0Ohm /CHICONYBT30

21 CLK_REQ2_WLAN#
21 CLK_PCIE_WLAN# PCH
21 CLK_PCIE_WLAN_PCH

BT Disable Low for Intel
C5348 10PF/50V @
C5347 10PF/50V @
BT_ON/OFF# R5316 0Ohm /IntelBT30

21 PCIE_RXN2_WLAN
21 PCIE_RXP2_WLAN
21 PCIE_TXN2_WLAN
21 PCIE_TXP2_WLAN

25 WLAN_ON_2
R5335 0Ohm

R5322 0Ohm vx_r0805_h24_small +3V
R5327 0Ohm vx_r0805_h24_small +3VS

C5338 33PF/50V

WLAN_ON_C
BUF_PLT_RST# 4,24,30,32,40,59,70
+3VS_Vaux_WLAN
R5332 0Ohm vx_r0603_h28_small +3V
R5331 0Ohm vx_r0603_h28_small +3VS
SMBC R5310 0Ohm
SMBD R5309 0Ohm
SMB_CLK_S 16,17,28
SMB_DAT_S 16,17,28

USB_PN9_C
USB_PP9_C
RN5302A 0Ohm
L5303 90Ohm/100Mhz
RN5303B 0Ohm
USB_PN9 24
USB_PP9 24

LED_WLAN# 54

R5314 10KOhm
R5321 0Ohm
D5302 RB751V-40
WLAN_ON 25
Check PCH WLAN_ON power plan

DVR1035_Radio control pin design guide for the acer notebook PCI-E module

WLAN +3VS bypass capactor:

Place 0.1UF near pin 2,24,52,39 41.

Place 10UF near +3VS_WLAN source side.

+3VS_WLAN
C5312 10UF/10V
C5308 0.1UF/16V
C5309 0.1UF/16V
C5310 0.1UF/16V @
C5311 0.1UF/16V @

WLAN +1.5VS bypass capactor:

Place 0.1UF near pin 6,28,48.

Place 10UF near +1.5VS source side.

+1.5VS
C5329 10UF/10V
C5318 0.1UF/16V
C5304 0.1UF/16V @
C5328 0.1UF/16V @

Remove Bead
Option :
BEAD SMD(1206)70OHM/3A
09G010070108

ER1.13

59 USIM_CLK — USIM_CLK — L5301 0Ohm — SIM_CLK_C — C5321 33PF/50V @ — C5327 33PF/50V @
59 USIM_RESET — USIM_RESET — L5302 0Ohm — SIM_RST_C — C5307 33PF/50V @ — C5322 33PF/50V @
59 USIM_PWR — USIM_PWR — SP5305 R0603 — SIM_VCC_C — C5315 33PF/50V @
USIM_PWR — R5307 10KOhm @
59 USIM_DATA — USIM_DATA — L5306 0Ohm — SIM_DIO_C — C5313 33PF/50V @ — C5305 33PF/50V NPO

ER1.5

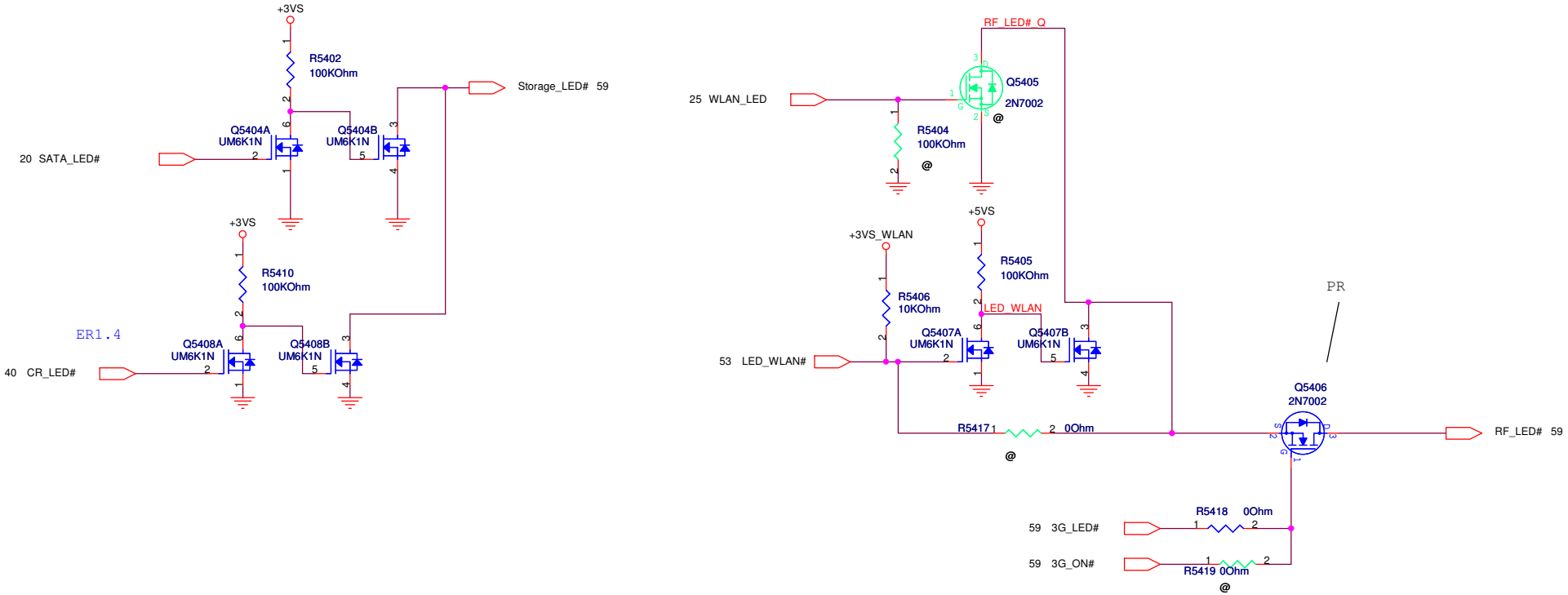
J5304 — SIM_CON_10P
12V251BSM003
SIM_VCC_C
SIM_RST_C
SIM_CLK_C
SIM_DIO_C
USB_PP10_SIM
USB_PN10_SIM
VCC, GND, RST, VPP, CLK, I/O, DAT0, MCMD, SWITCH1, SWITCH2, GND2, NP_NC2, NP_NC1, GND1

ER1.10

+3VS
C5301 0.1UF/16V @
D5301 — CM1293_04SO — 07V000000006
USB_PN10_SIM
USB_PP10_SIM
SIM_DIO_C
SIM_CLK_C
SIM_RST_C
D4612 EGA10603V05A1 @

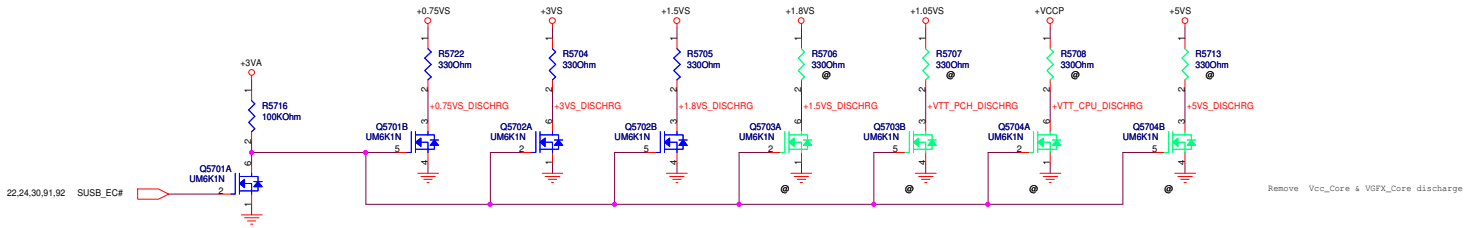
24 USB_PN10
24 USB_PP10
RN5303A 0Ohm
L5304 90Ohm/100Mhz @
RN5303B 0Ohm
USB_PN10_SIM
USB_PP10_SIM

PEGATRON	Title : WLAN/ 3G	
<OrgName>	Engineer: JAY TSAI	
Size C	Project Name EIH31	Rev 1.3
Date: Thursday, January 13, 2011	Sheet 53 of 99	

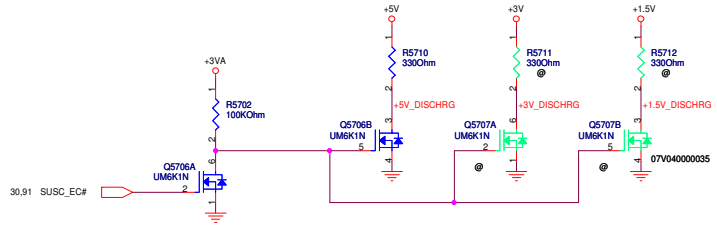


PEGATRON	Title : USB3.0	
<OrgName>	Engineer: JAY TSAI	
Size B	Project Name EIH31	Rev 1.3
Date: Thursday, January 13, 2011	Sheet 54 of 99	

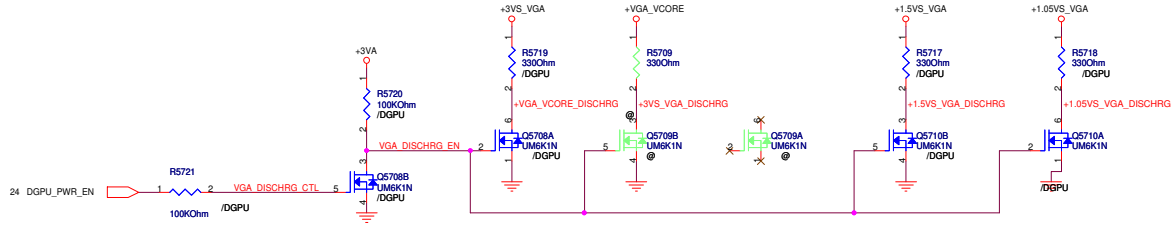
+3VA	+3VA	20,27,30,56,59,81,93
+VCC_CORE	+VCC_CORE	6,80
+VGFX_CORE	+VGFX_CORE	7,80
+VCCP	+VCCP	3,4,6,25,26,27,30,32,82
+0.75VS	+0.75VS	16,17,83
+1.05VS	+1.05VS	26,27,80,82
+1.5VS	+1.5VS	26,53,91
+1.8VS	+1.8VS	7,24,26,84
+3VS	+3VS	4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,59,91,92
+5VS	+5VS	27,30,31,36,37,46,48,50,51,54,59,80,91
+1.5V	+1.5V	5,7,16,83
+3V	+3V	4,24,52,53,59,91
+5V	+5V	46,52,59,91
+VGA_VCORE	+VGA_VCORE	75,87
+3VS_VGA	+3VS_VGA	70,72,74,91
+1.5VS_VGA	+1.5VS_VGA	71,76,91
+1.05VS_VGA	+1.05VS_VGA	70,71,72,91



Remove Vcc_Core & VGFX_Core discharge



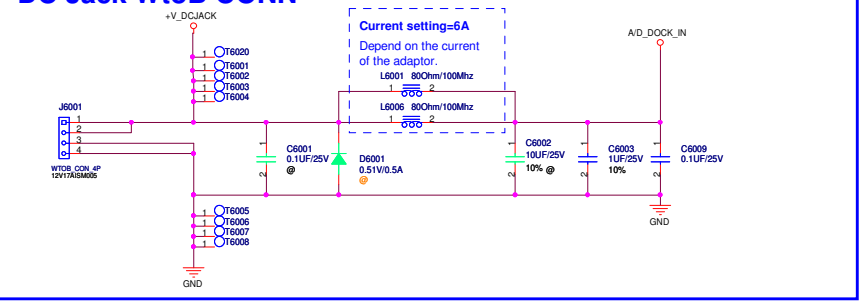
R1.1



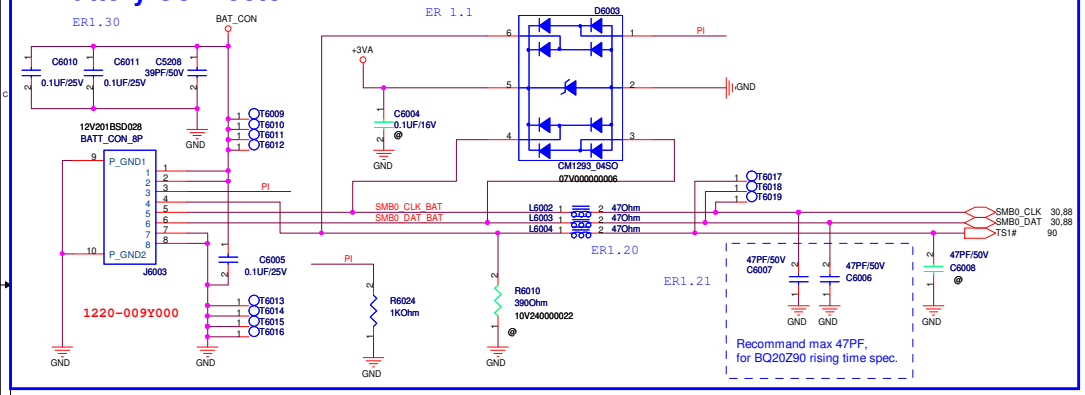
Unmount +VGA_Vcore discharg

PEGATRON	Title : DSG_Discharge		
<OrgName>	Engineer: JAY TSAI		
Size C	Project Name EIH31		Rev 1.3
Date: Thursday, January 13, 2011	Sheet 55 of 99		

DC Jack WtoB CONN

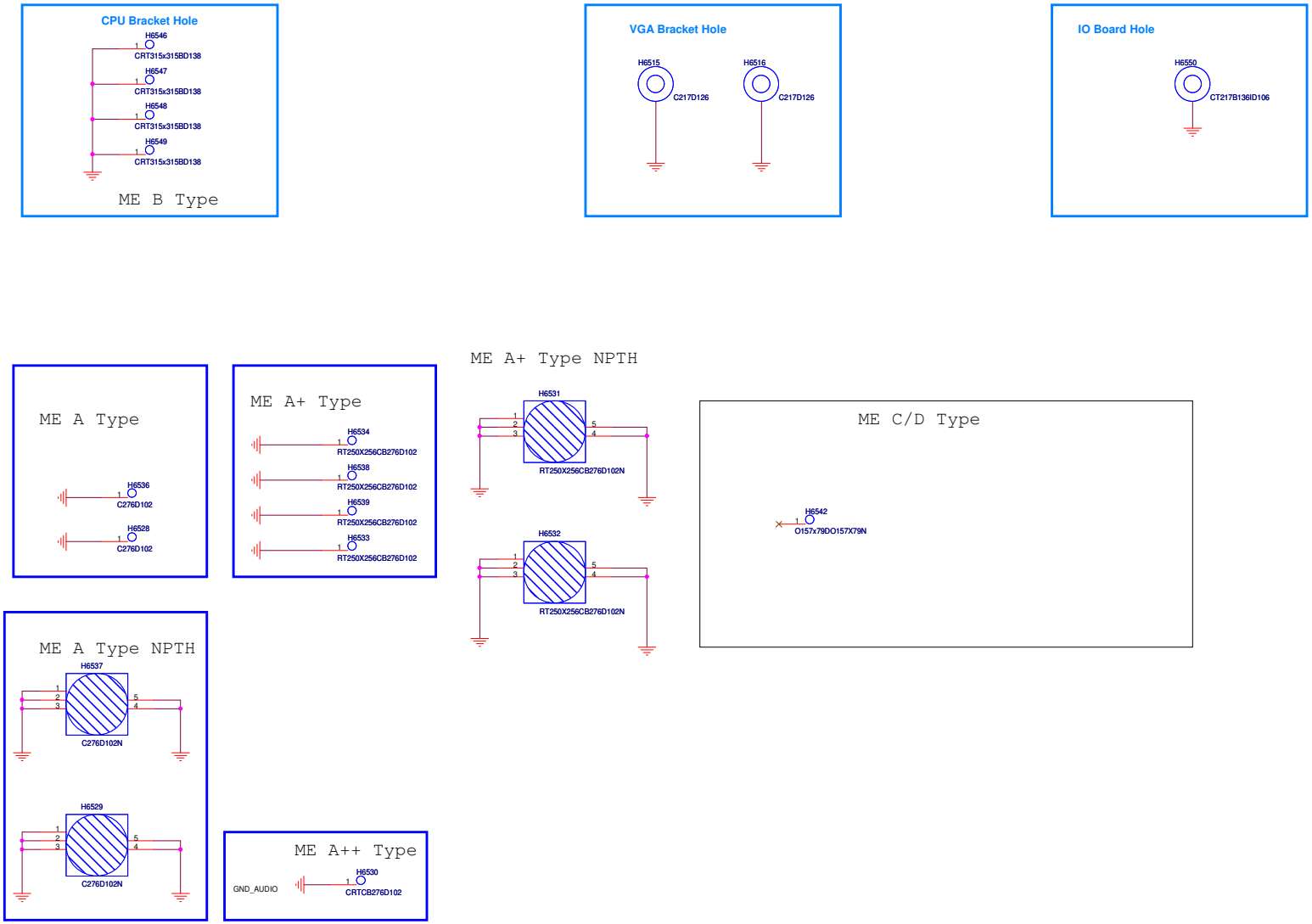


Battery Connector



+VCC_RTC	+VCC_RTC	20,22,27
+3VA_EC	+3VA_EC	28,30,32
+3VA	+3VA	20,27,30,55,59,81,93
+5VA	+5VA	59,81,88
+3VSUS	+3VSUS	4,22,24,27,28,30,59,81,82,84,92
+5VSUS	+5VSUS	22,27,81,82,83,84,87,91
+12VSUS	+12VSUS	22,28,81,91
+1.5V	+1.5V	5,7,16,55,83
+3V	+3V	4,24,52,53,55,59,91
+5V	+5V	46,52,55,59,91
+12V	+12V	91
+0.75VS	+0.75VS	16,17,55,83
+1.05VS	+1.05VS	26,27,55,80,82
+1.5VS	+1.5VS	26,53,55,91
+1.8VS	+1.8VS	7,24,26,55,84
+3VS	+3VS	4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,59,91,92
+5VS	+5VS	27,30,31,36,37,46,48,50,51,54,55,59,80,91
+12VS	+12VS	28,36,48,91
AC_BAT_SYS	AC_BAT_SYS	45,80,81,82,83,87,88
A/D_DOCK_IN	A/D_DOCK_IN	88
BAT_CON	BAT_CON	88
+1.5V_DDR3	+1.5V_DDR3	16,17,18
+VCCP	+VCCP	3,4,6,25,26,27,30,32,55,82
+VCC_CORE	+VCC_CORE	6,80
+VGFX_CORE	+VGFX_CORE	7,80
+VTT_PCH_ORG	+VTT_PCH_ORG	22,26,27
+VTT_PCH_VCCIO	+VTT_PCH_VCCIO	20,26,27
+1.05VM_ORG	+1.05VM_ORG	27
+V_VREF	+V_VREF	
+V_VREF_DDR3	+V_VREF_DDR3	7,16,17,18,83
+V_SM_VREF	+V_SM_VREF	

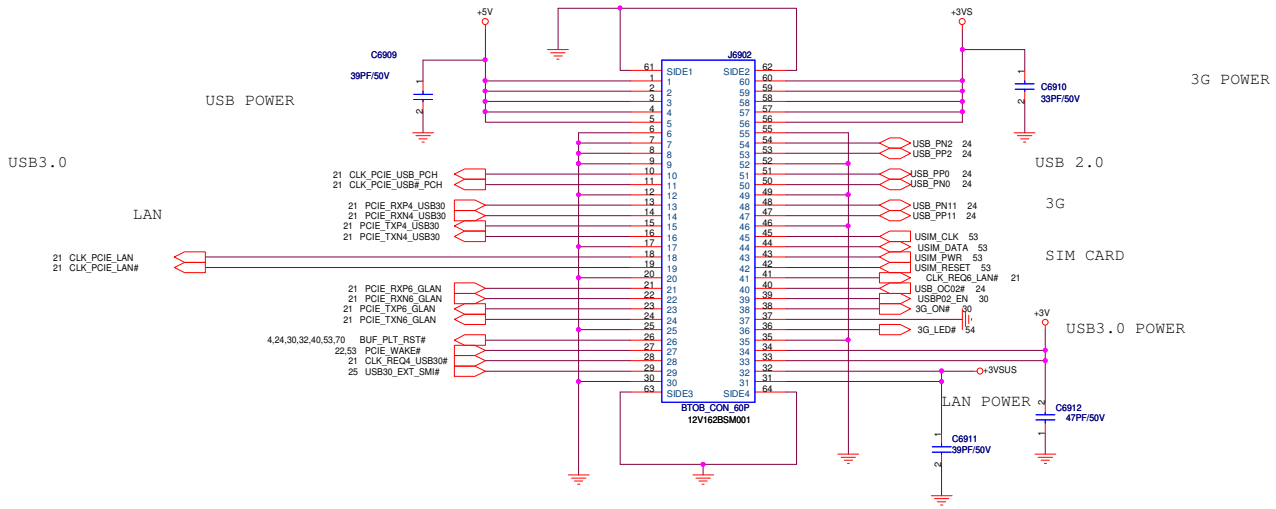
PEGATRON	Title :	DC_DC/BAT CONN
<OrgName>	Engineer:	JAY TSAI
Size: C	Project Name: EIH31	Rev: 1.3
Date: Thursday, January 13, 2011	Sheet 56 of 99	



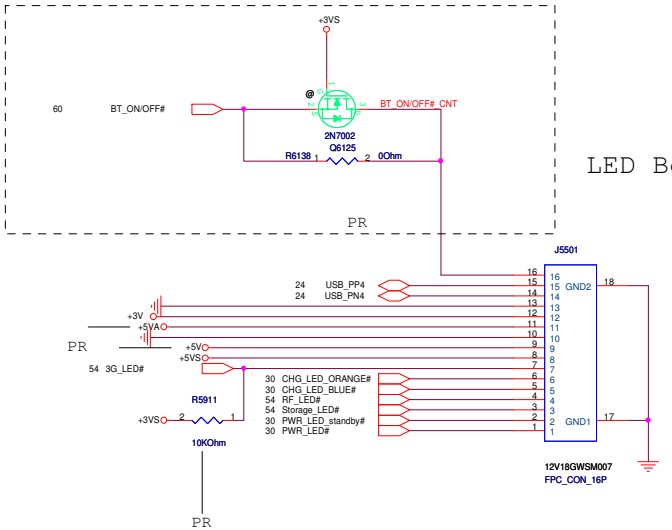
PEGATRON	Title : ME_CONN,Skew Hole	
<OrgName>	Engineer: JAY TSAI	
Size C	Project Name EIH31	Rev 1.3
Date: Thursday, January 13, 2011	Sheet 57 of 99	

PEGATRON	Title : System Setting		
<OrgName>	Engineer: JAY TSAI		
Size	Project Name		Rev
Custom	EIH31		1.3
Date: Thursday, January 06, 2011		Sheet 58 of 99	

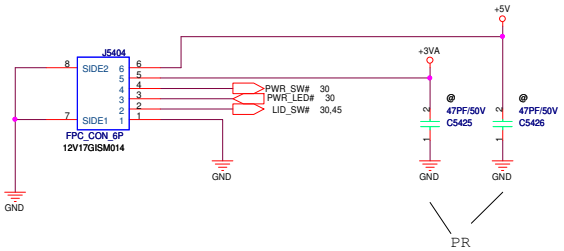
USB IO Board CNT



LED Board CNT



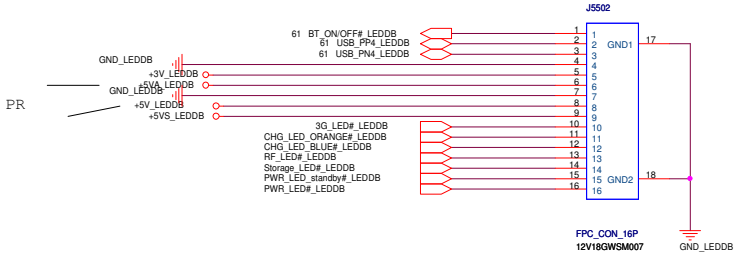
POWER Board CNT

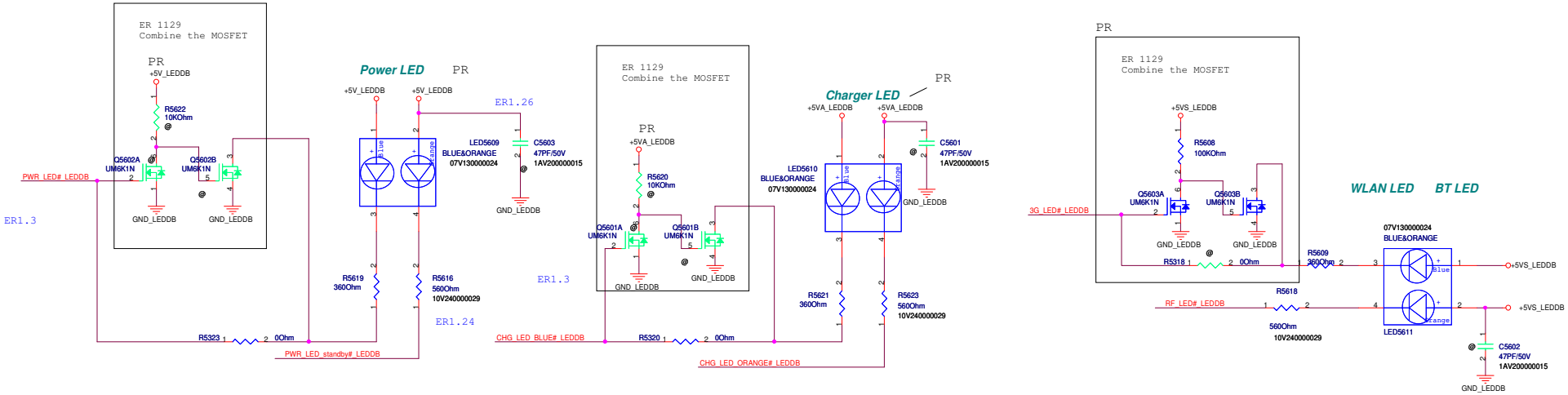


PEGATRON	Title : B to B		
<OrgName>	Engineer: JAY TSAI		
Size C	Project Name EIH31		Rev 1.3
Date: Thursday, January 13, 2011	Sheet 59 of 99		

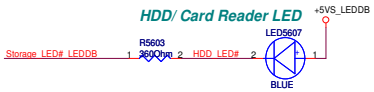
+3VA	+3VA	20,27,30,55,56,59,81,93
+3VS	+3VS	4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,59,91,92
+5VSUS	+5VSUS	22,27,81,82,83,84,87,91
+5VA	+5VA	59,81,88
+5V	+5V	46,52,55,59,91
+5VS	+5VS	27,30,31,36,37,46,48,50,51,54,55,59,80,91
AC_BAT_SYS	AC_BAT_SYS	45,80,81,82,83,87,88
+3V	+3V	4,24,52,53,55,59,91

LED DB

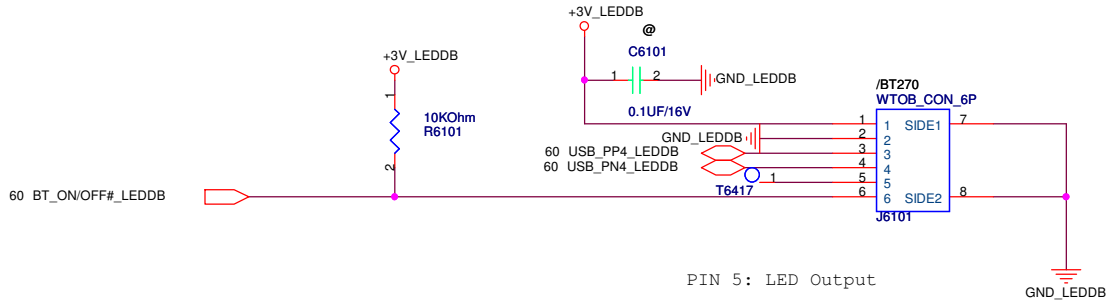




Dual Color

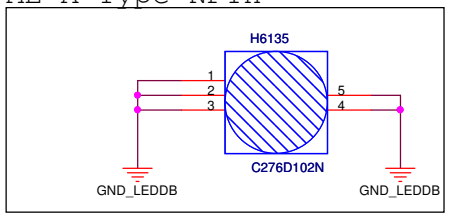


PEGATRON	Title : LED_Indicator	
<OrgName>	Engineer: JAY TSAI	
Size C	Project Name EIH31	Rev 1.3
Date: Thursday, January 13, 2011	Sheet 60 of 99	



PIN 5: LED Output

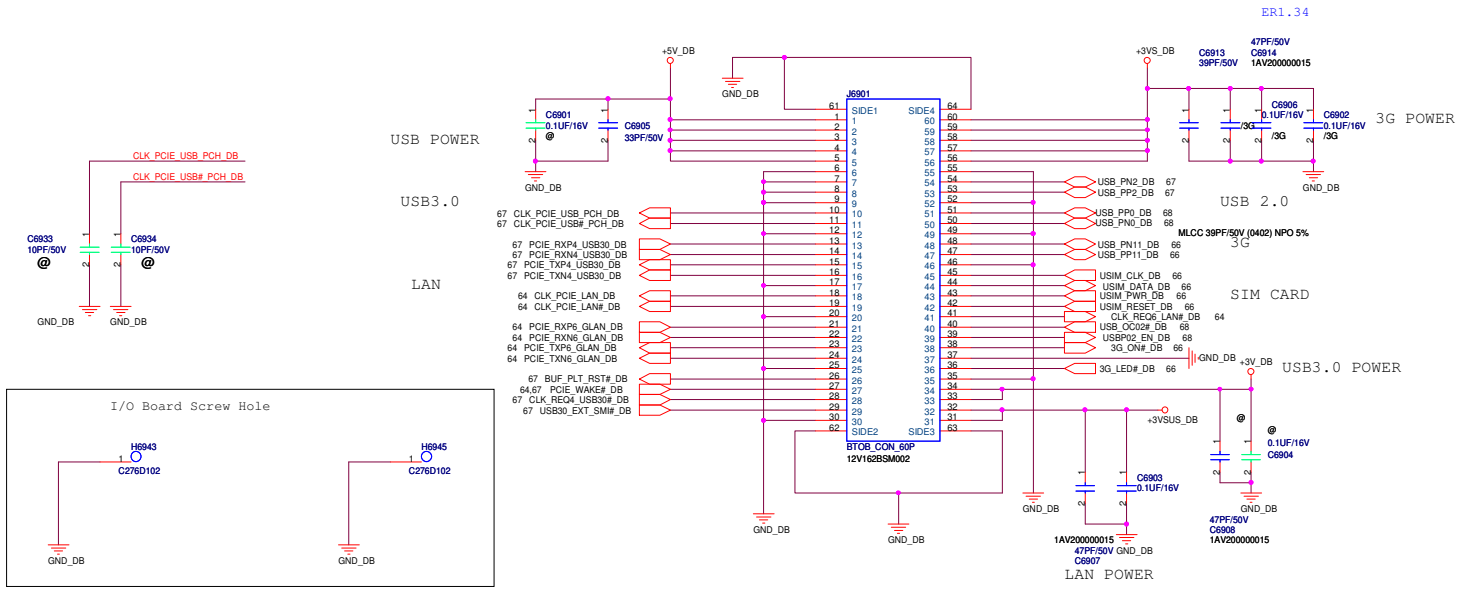
ME A Type NPTH



PEGATRON	Title : BT_Bluetooth	
<OrgName>	Engineer: JAY TSAI	
Size B	Project Name EIH31	Rev 1.3
Date: Thursday, January 13, 2011	Sheet 61 of 99	

PEGATRON	Title : System Setting		
<OrgName>	Engineer: JAY TSAI		
Size	Project Name		Rev
Custom	EIH31		1.3
Date: Thursday, January 06, 2011		Sheet 62 of 99	

DB



PEGATRON	Title : B to B	
<OrgName>	Engineer: JAY TSAI	
Size C	Project Name EIH31	Rev 1.3
Date: Thursday, January 13, 2011	Sheet 63 of 99	

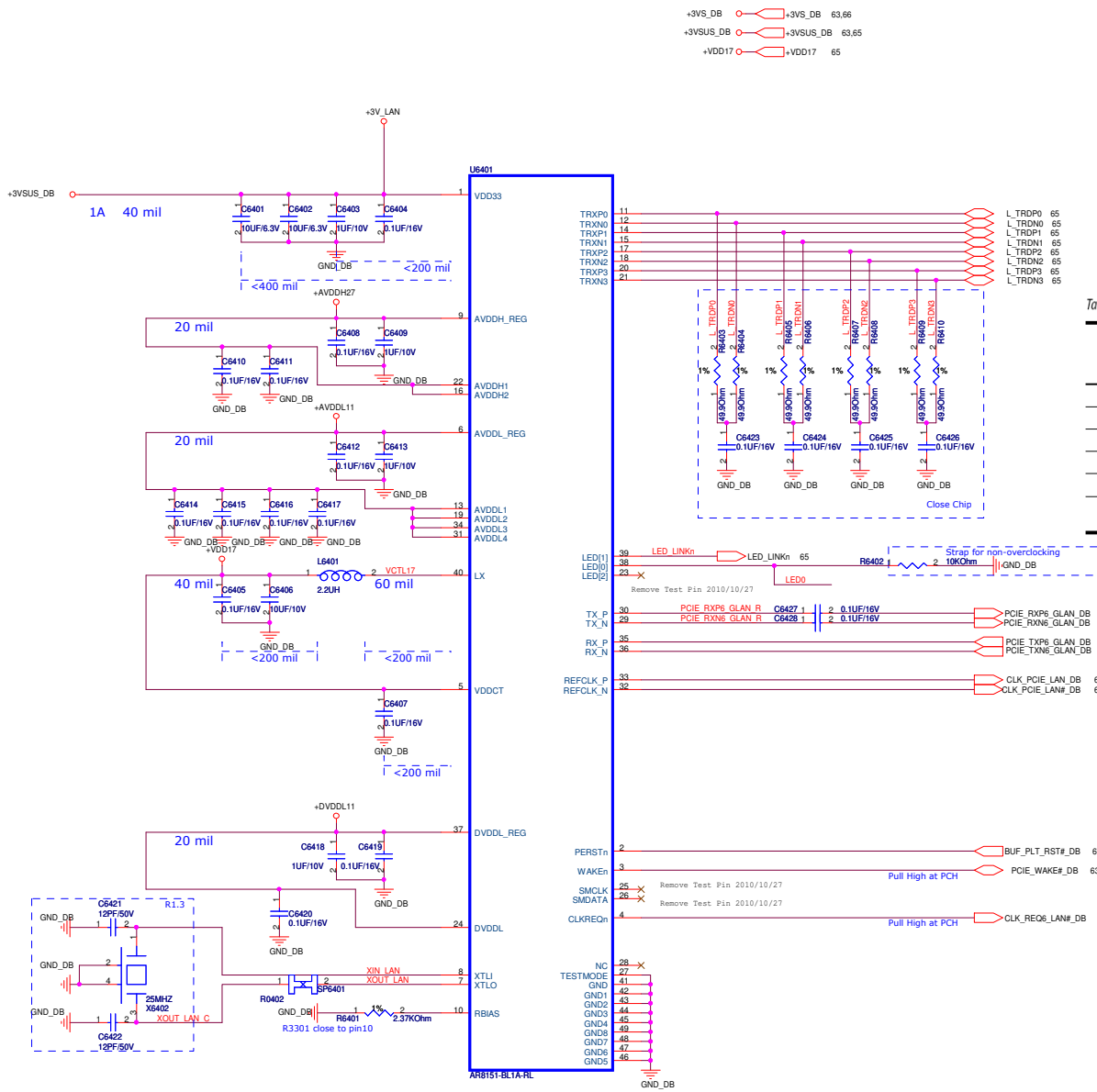
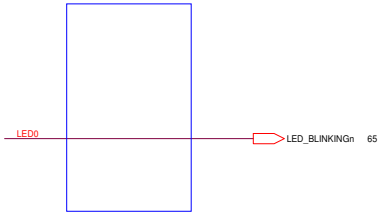


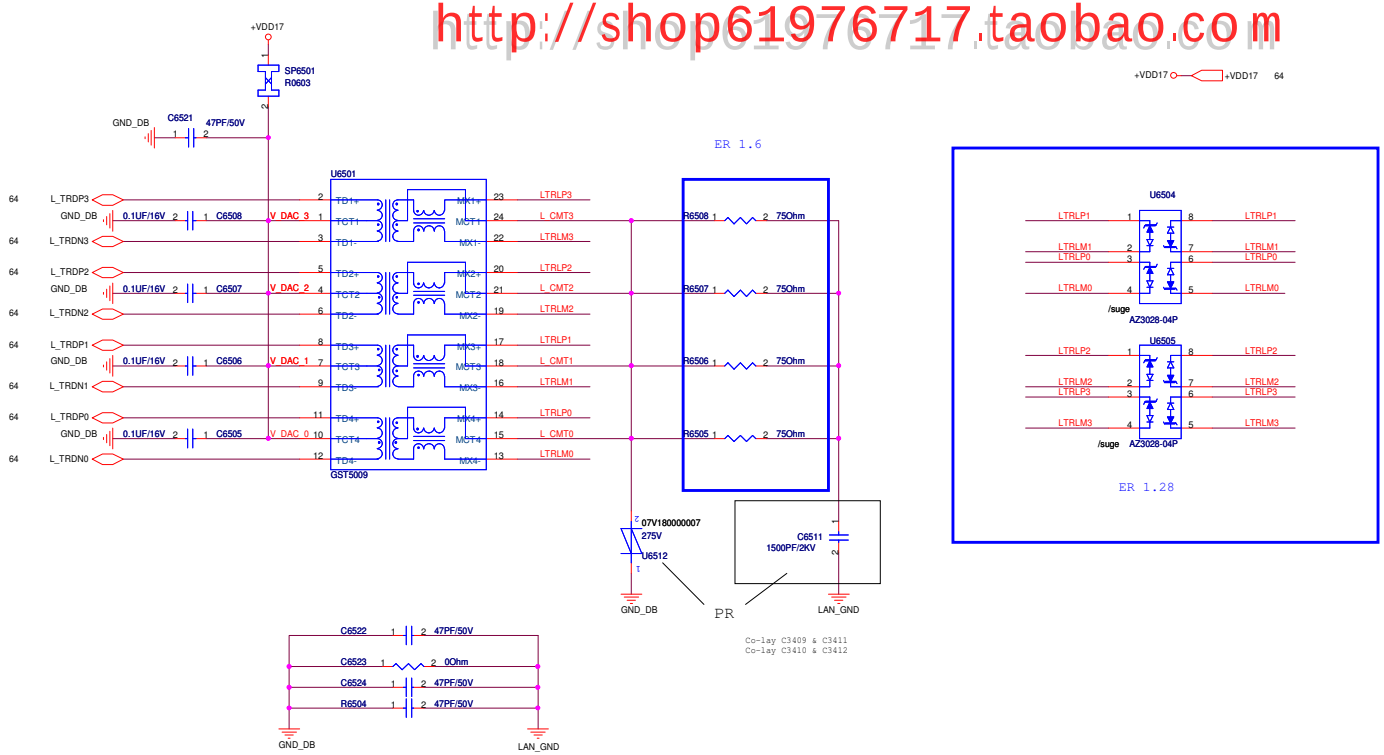
Table 2-6. **LED Link Table**

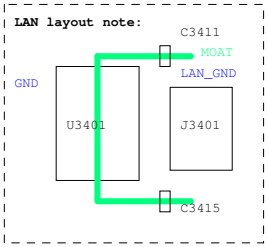
LED[0] LED_ACT	LED[1] LED_LINK	LED[2] LED_LINK_ 1000	Selected Speed	Link Status
High	High	High	Any Speed	Link Down
Blink	High	High	10 Mbps; Half-Duplex	Link Up
Blink	Low	High	10 Mbps; Full-Duplex	Link Up
Blink	Low	High	100 Mbps; Half-Duplex	Link Up
Blink	Low	High	100 Mbps; Full-Duplex	Link Up
Blink	Low	Low	Auto, 1000 Mbps, Full-Duplex	Link Up

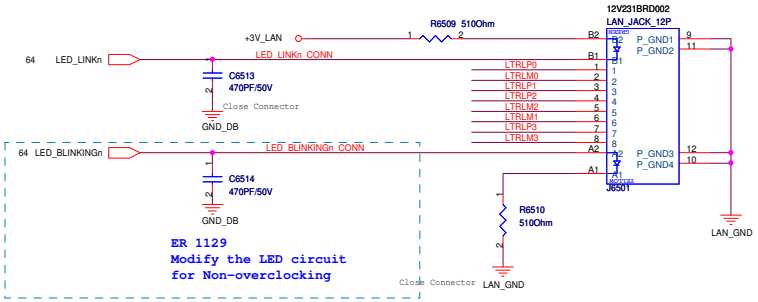


ER 1129
Remove the Q6705 and +5V_DB

PEGATRON	Title : LAN_AR8151		
<OrgName>	Engineer: JAY TSAI		
Size C	Project Name EIH31		Rev 1.3
Date: Thursday, January 13, 2011	Sheet 64 of 99		

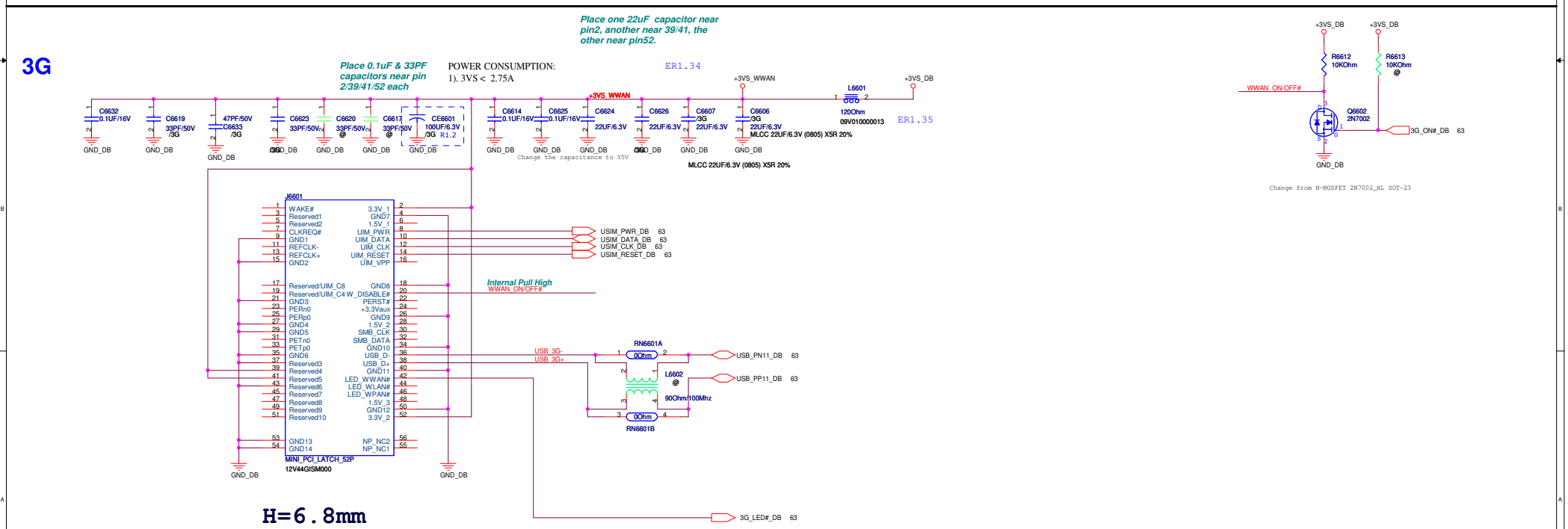




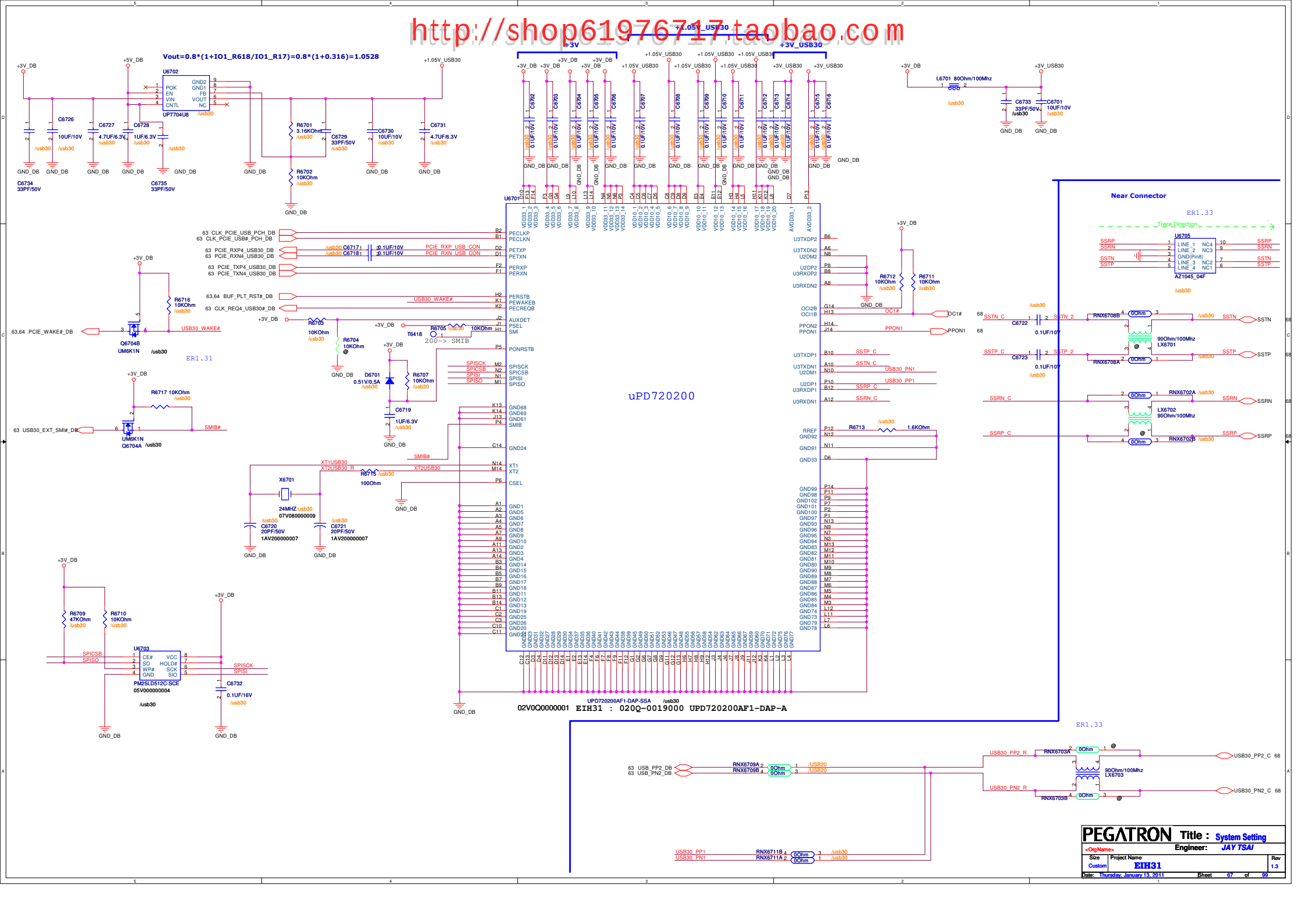


Temp follow Atheros desgin guide, check yellow is need? Check with customer.

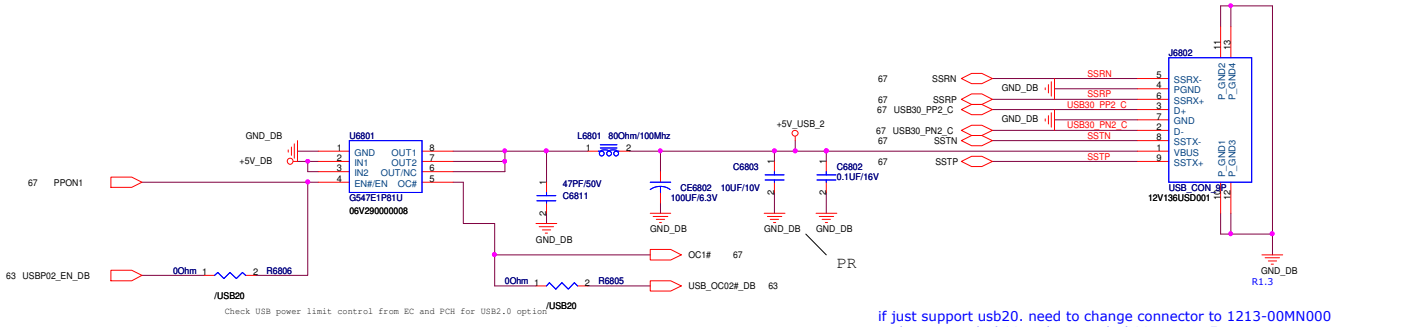
PEGATRON	Title : RJ45/ RJ11		
<OrgName>	Engineer: JAY TSAI		
Size C	Project Name EIH31		Rev 1.3
Date: Thursday, January 13, 2011	Sheet 65 of 99		



PEGATRON	Title : WLAN/ 3G		
<OrgName>	Engineer: JAY TSAI		
Size C	Project Name EIH31		Rev 1.3
Date: Thursday, January 13, 2011	Sheet 66 of 99		



USB ports



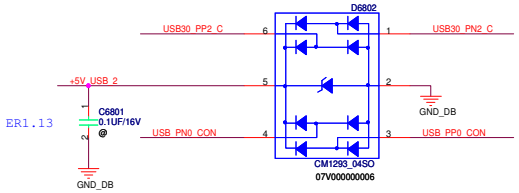
Check USB power limit control from EC and PCH for USB2.0 option

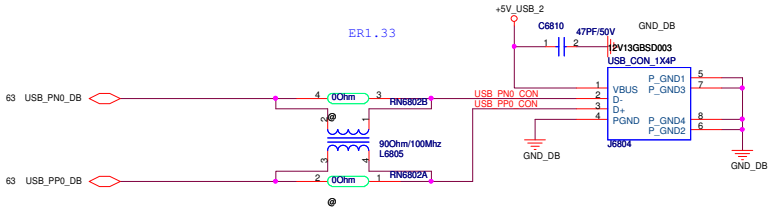
Boston:GPIO82:USBSLP_EN#,check KBID0

Boston:GPIO14:USB_OC2#_EC

BOM by USB 3.0 must change the U5201 for active HI solution.

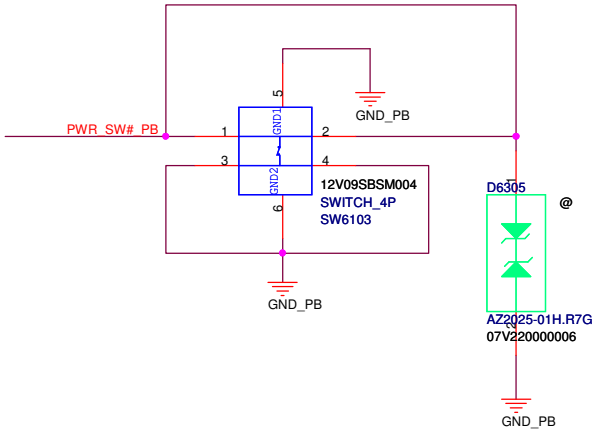
if just support usb20. need to change connector to 1213-00MN000 and unmount /usb30 and mount /usb20 in page 54



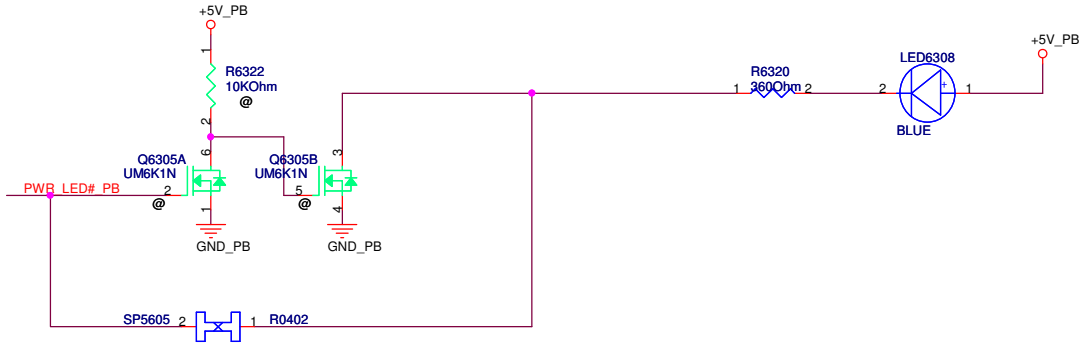


PEGATRON	Title : USB_USB Port	
<OrgName>	Engineer: JAY TSAI	
Size C	Project Name EIH31	Rev 1.3
Date: Thursday, January 13, 2011	Sheet 68 of 99	

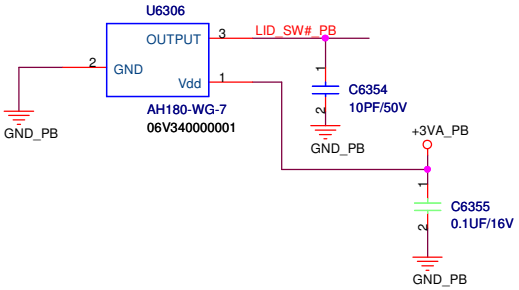
Power Button

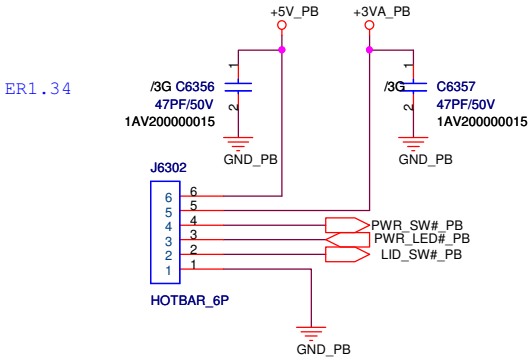


Power Button LED-Power



Hall Sensor

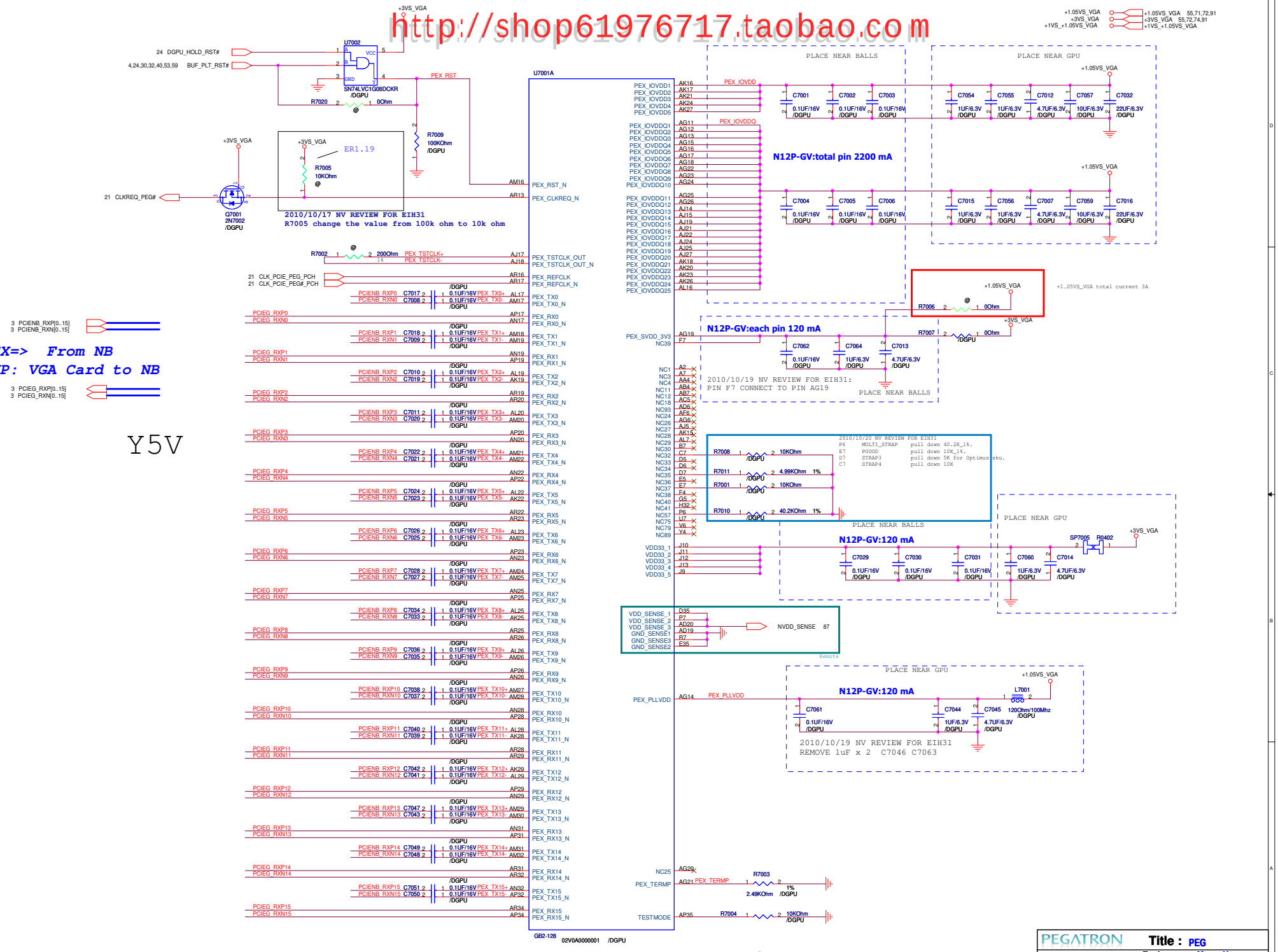


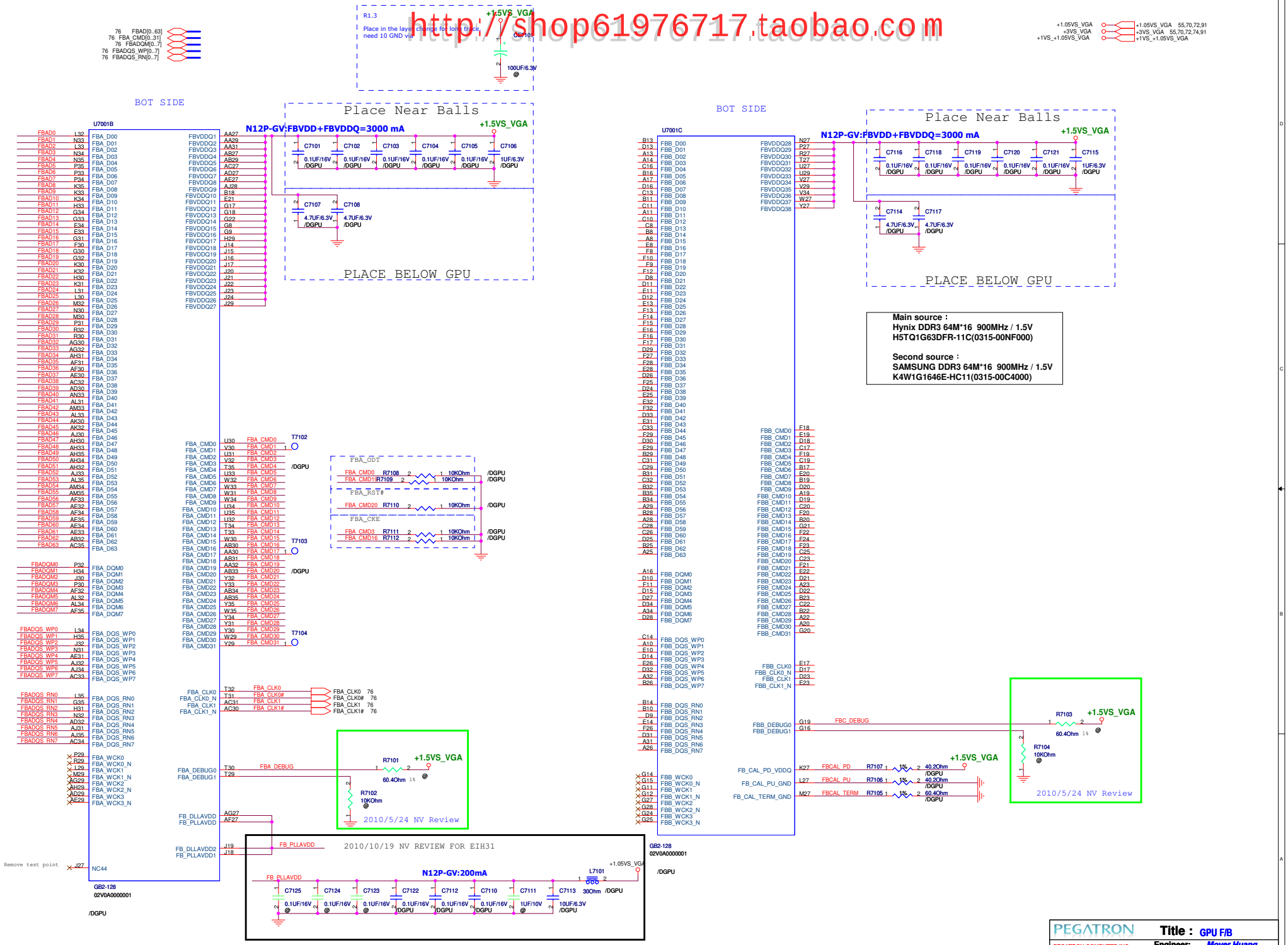


HOT bar

SKREW HOLE MAKING BY LAYOUT

PEGATRON	Title : TPM_****	
<OrgName>	Engineer: JAY TSAI	
Size B	Project Name EIH31	Rev 1.3
Date: Friday, January 07, 2011	Sheet 69 of 99	





PEGATRON

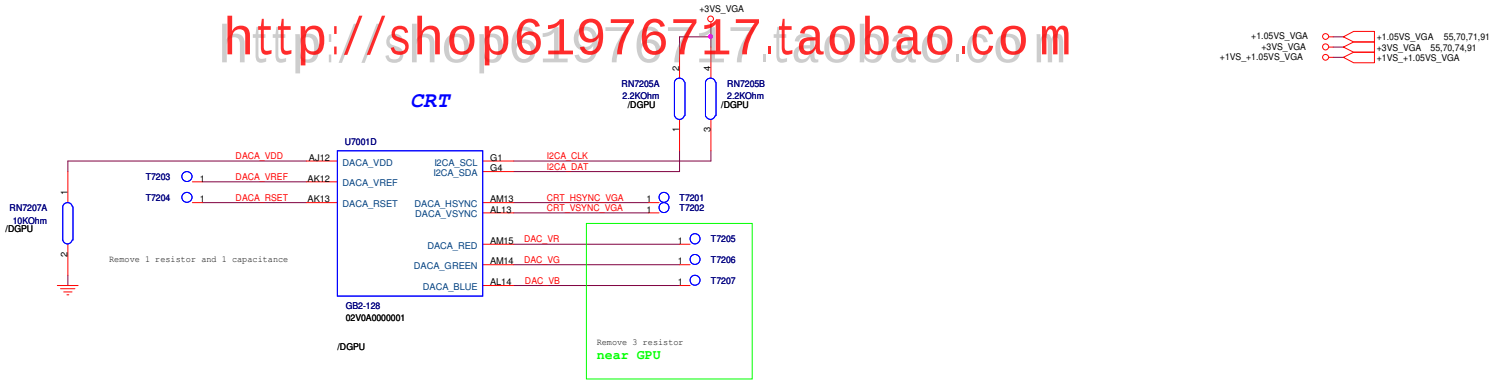
Title : GPU F/B

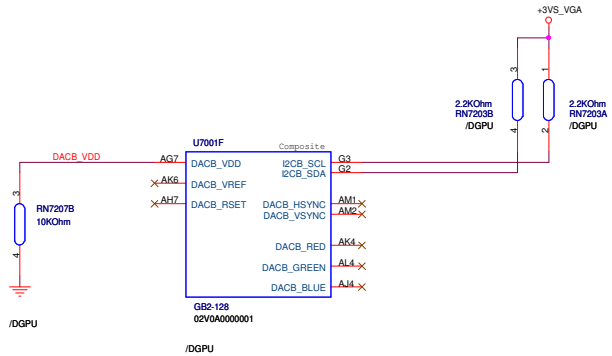
PEGATRON COMPUTER INC

Engineer: Moyer Huang

Size	Project Name	Rev
C	EIH31	1.3
	P/N <OrgAddr2>	

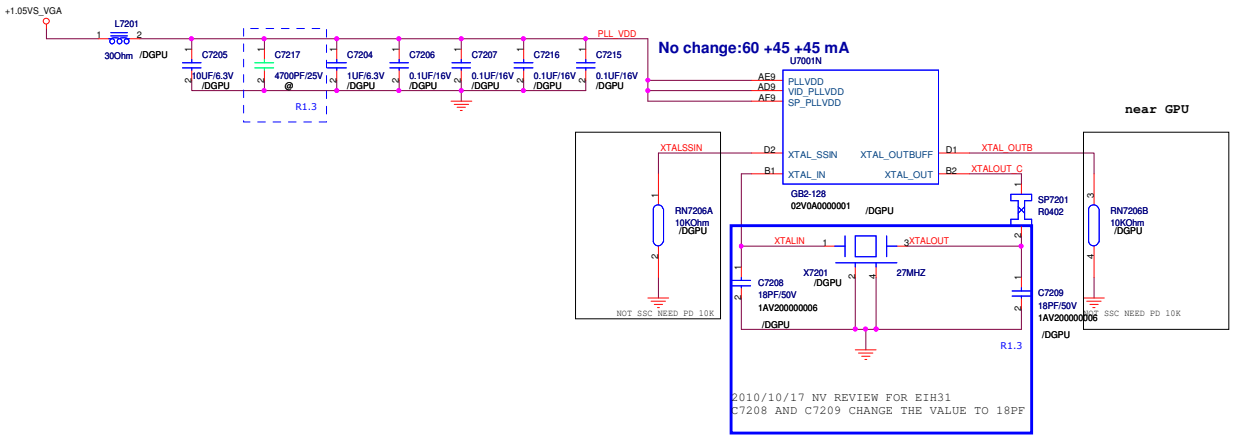
Date: Friday, January 07, 2011 Sheet 71 of 100





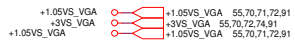
XTAL_IN , XTAL_OUT
3.3V tolerance

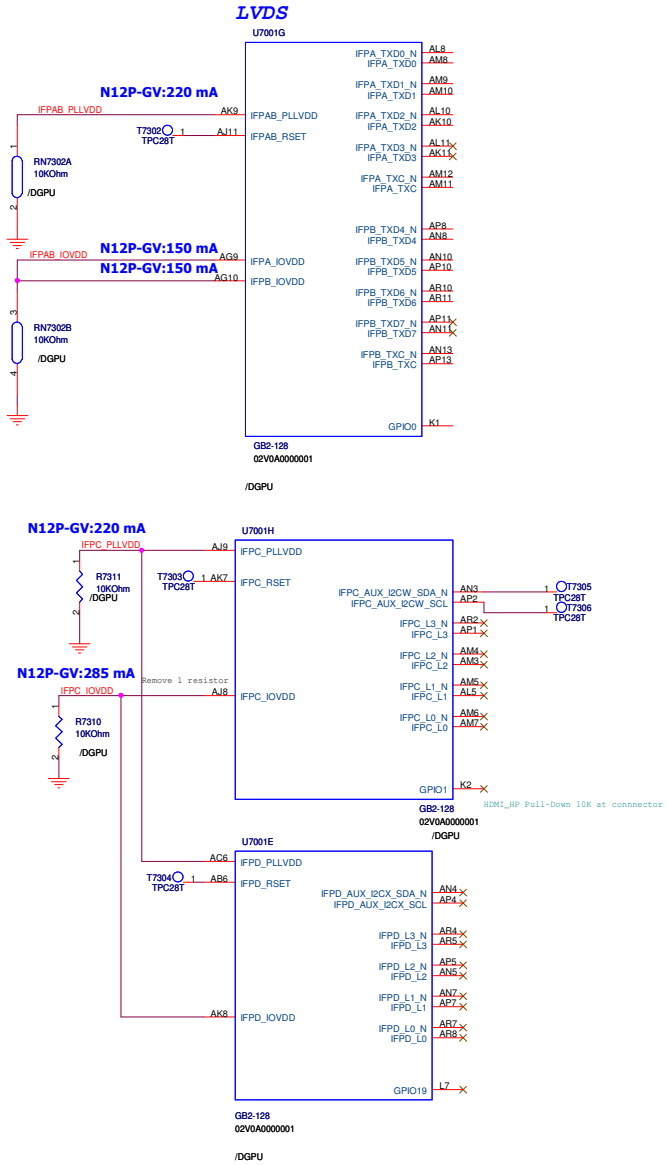
correspondent BGA balls must be
12mils and 16 mil wide
near GPU

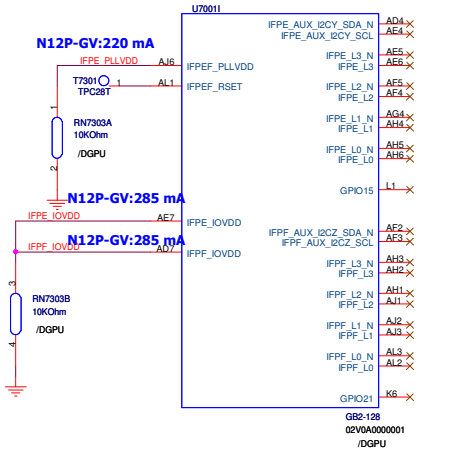


near GPU

PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Moyer Huang		
Size C	Project Name EIH31		Rev 1.3
	P/N <OrgAddr2>		
Date: Friday, January 07, 2011	Sheet 72 of 100		







Reserve Pull-down

Remove Reserved Pull-down

Table 7.1 N11x Fermi Family Display Link Summary

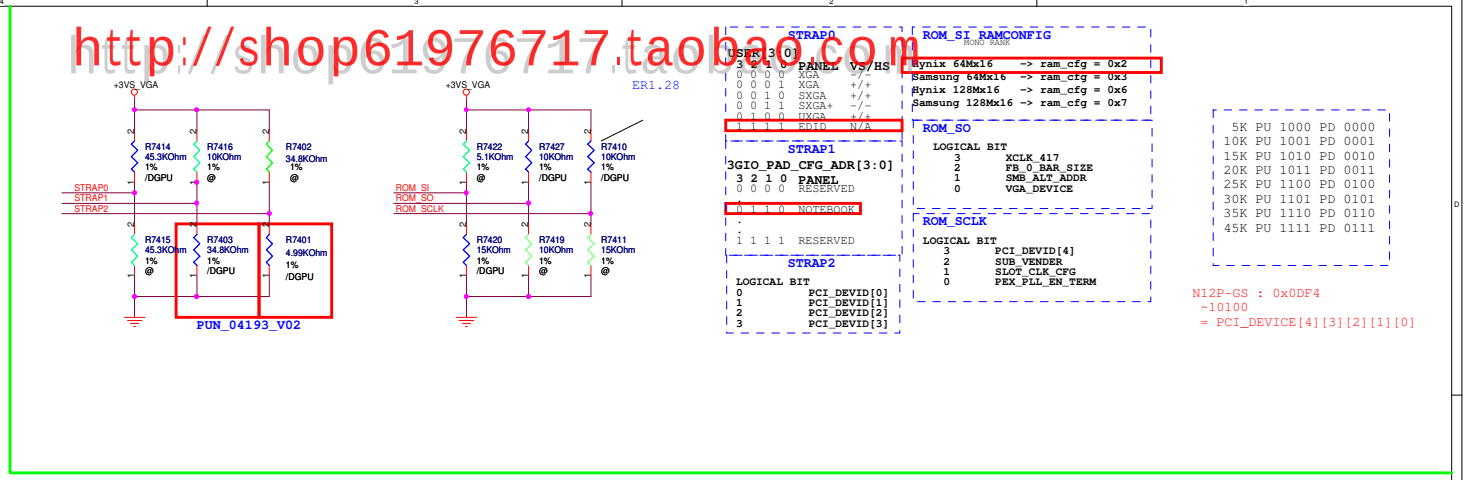
Link A	Link B	Link C	Link D	Link E	Link F
LVDS (Single Link or Dual Link with IFPB)	LVDS (Dual Link with IFPA)	DisplayPort, HDMI	DisplayPort, eDP	DisplayPort, DVI (Single Link or Dual Link with IFPF), HDMI	DisplayPort, DVI (Dual Link with IFPE)

IFPx	A	B	C	D	E	F
MASERATI						

PEGATRON
PEGATRON COMPUTER INC
Title : Connector, LED
Engineer: Moyer Huang
Size C | Project Name EIH31 | Rev 1.3
P/N <OrgAddr2>
Date: Friday, January 07, 2011 | Sheet 73 of 100

+1.05VS_VGA
+3VS_VGA
+1.05VS_VGA

+1.05VS_VGA 55,70,71,72,91
+3VS_VGA 55,70,72,91
+1.05VS_VGA 55,70,71,72,91



STRAP0

3 2 1 0	PANEL	VS/HS
0 0 0 0	XGA	-/-
0 0 0 1	XGA	+/+
0 0 1 0	SXGA	+/+
0 0 1 1	SXGA+	-/-
0 1 0 0	UXGA	+/+
1 1 1 1	EDID	N/A

STRAP1

3GIO_PAD_CFG_ADR[3:0] 3 2 1 0	PANEL
0 0 0 0	RESERVED
0 1 1 0	NOTEBOOK
1 1 1 1	RESERVED

STRAP2

LOGICAL BIT	
0	PCI_DEVID[0]
1	PCI_DEVID[1]
2	PCI_DEVID[2]
3	PCI_DEVID[3]

ROM_SI_RAMCONFIG
MONO RANK

Hynix 64Mx16 -> ram_cfg = 0x2
Samsung 64Mx16 -> ram_cfg = 0x3
Hynix 128Mx16 -> ram_cfg = 0x6
Samsung 128Mx16 -> ram_cfg = 0x7

ROM_SO

LOGICAL BIT	
3	XCLK_417
2	FB_0_BAR_SIZE
1	SMB_ALT_ADDR
0	VGA_DEVICE

ROM_SCLK

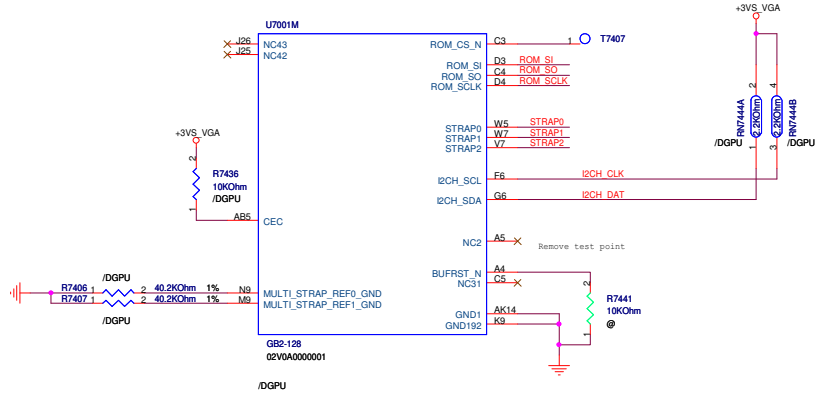
LOGICAL BIT	
3	PCI_DEVID[4]
2	SUB_VENDER
1	SLOT_CLK_CFG
0	PEX_PLL_EN_TERM

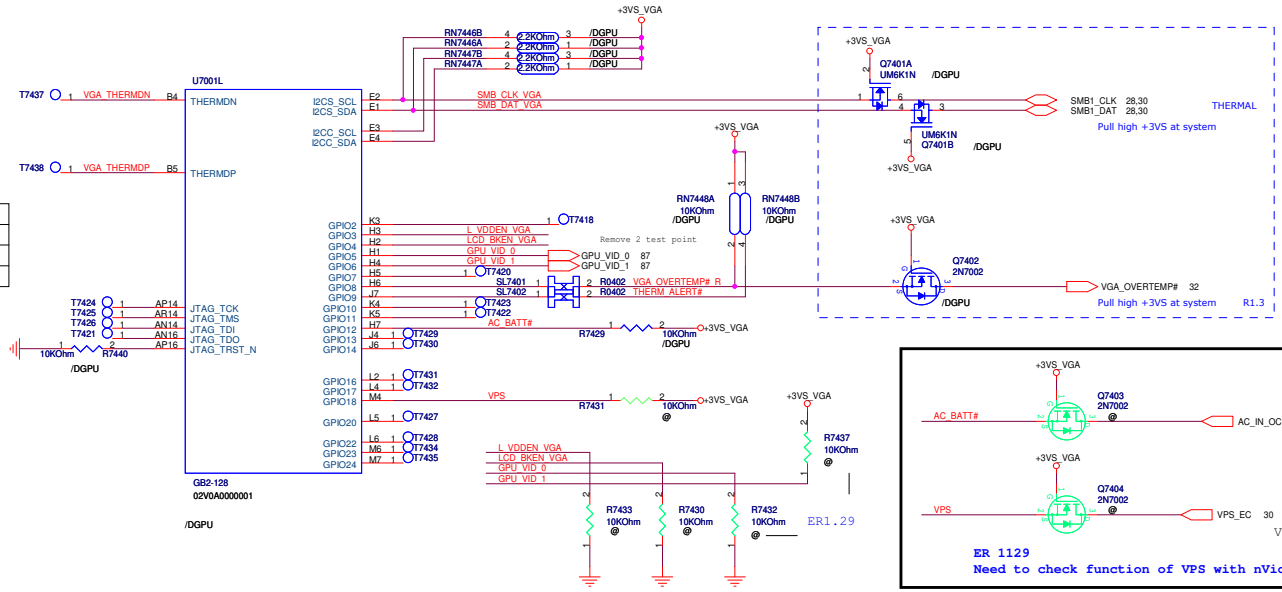
5K PU 1000 PD 0000
10K PU 1001 PD 0001
15K PU 1010 PD 0010
20K PU 1011 PD 0011
25K PU 1100 PD 0100
30K PU 1101 PD 0101
35K PU 1110 PD 0110
45K PU 1111 PD 0111

N12P-GS : 0x0DF4
~10100
= PCI_DEVICE[4][3][2][1][0]

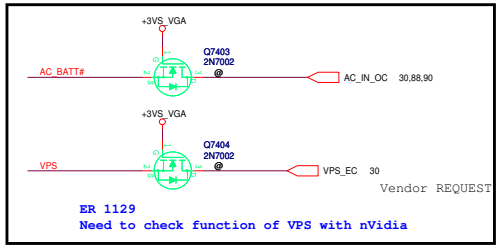
GPIO USAGE

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	IFPAB HOTPLUG DETECT
1	IN	N/A	IFPC HOTPLUG DETECT
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	HIGH	NVVDD ALTV0
6	OUT	HIGH	NVVDD ALTV1
7	OUT	HIGH	FBVDDQ ALTV
8	IN/OUT	LOW	OVERTEMP ALERT
9	OUT	LOW	THERMAL ALERT
10	OUT	HIGH	FB_VREF CONTROL
11	OUT	HIGH	RESERVED
12	IN	N/A	AC DETECT
13	OUT	LOW	LOAD STEP DOWN
14	OUT	HIGH	LOAD STEP UP
15	IN	N/A	IFPE HOTPLUG DETECT
16	IN	N/A	FAN PWM OUT
17	IN	N/A	FAN TACH IN
18	IN	N/A	RESERVED
19	IN	N/A	IFPD HOTPLUG DETECT
20	IN	N/A	RESERVED
21	IN	N/A	IFPF HOTPLUG DETECT
22	IN	N/A	RESERVED
23	IN	N/A	RESERVED
24	IN	N/A	RESERVED





GPU_VID	VID1	VID0	+VGA_VCORE
Low	0	0	0.85V
Med	0	1	1V
High	1	0	1.025V

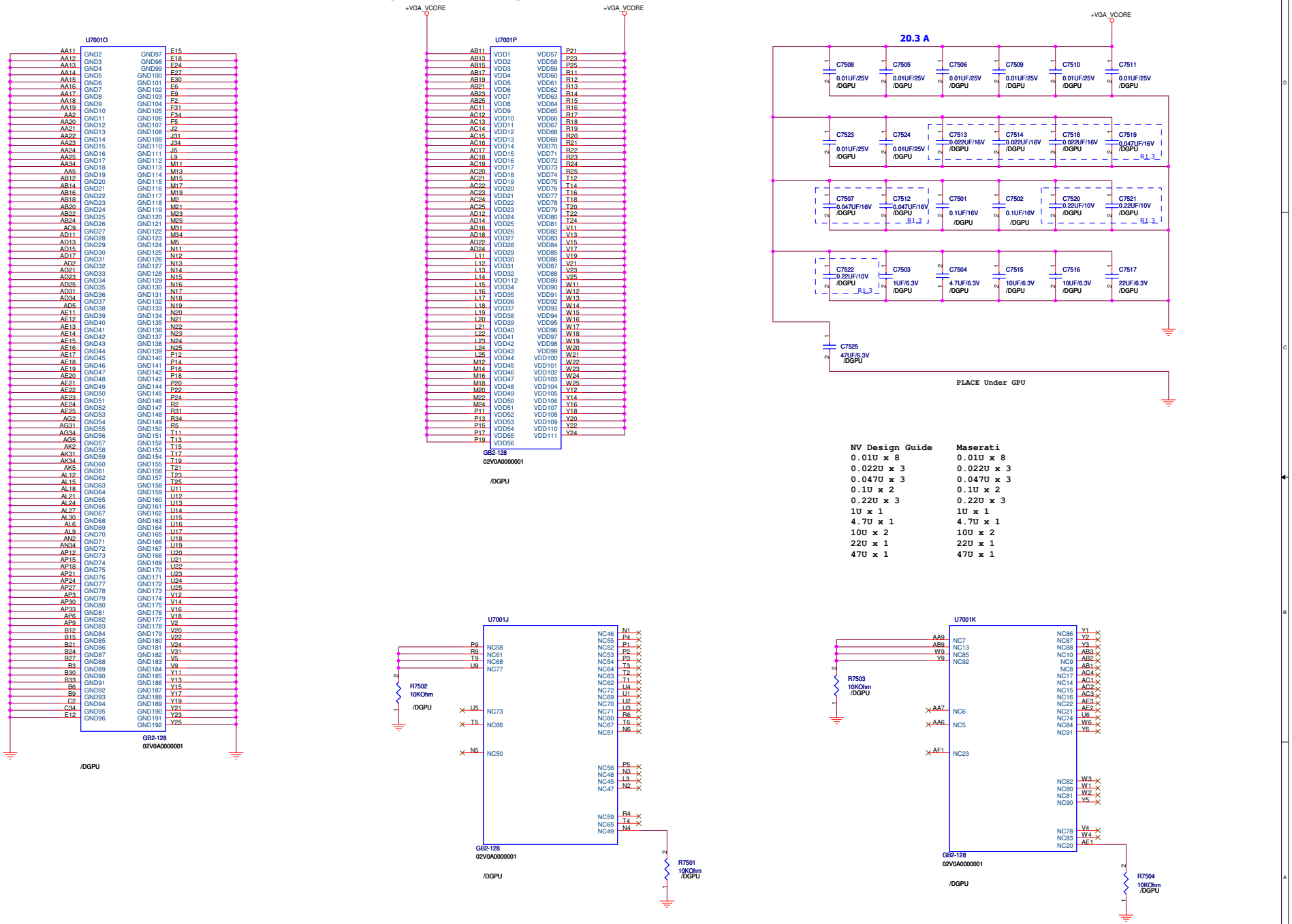


PEGATRON
PEGATRON COMPUTER INC

Title : Connector, LED
Engineer: Moyer Huang

Size	Project Name	Rev
C	EIH31	1.3
	P/N <OrgAddr2>	

Date: Thursday, January 13, 2011 Sheet 74 of 100



PEGATRON

Title : GPU PWR/GND

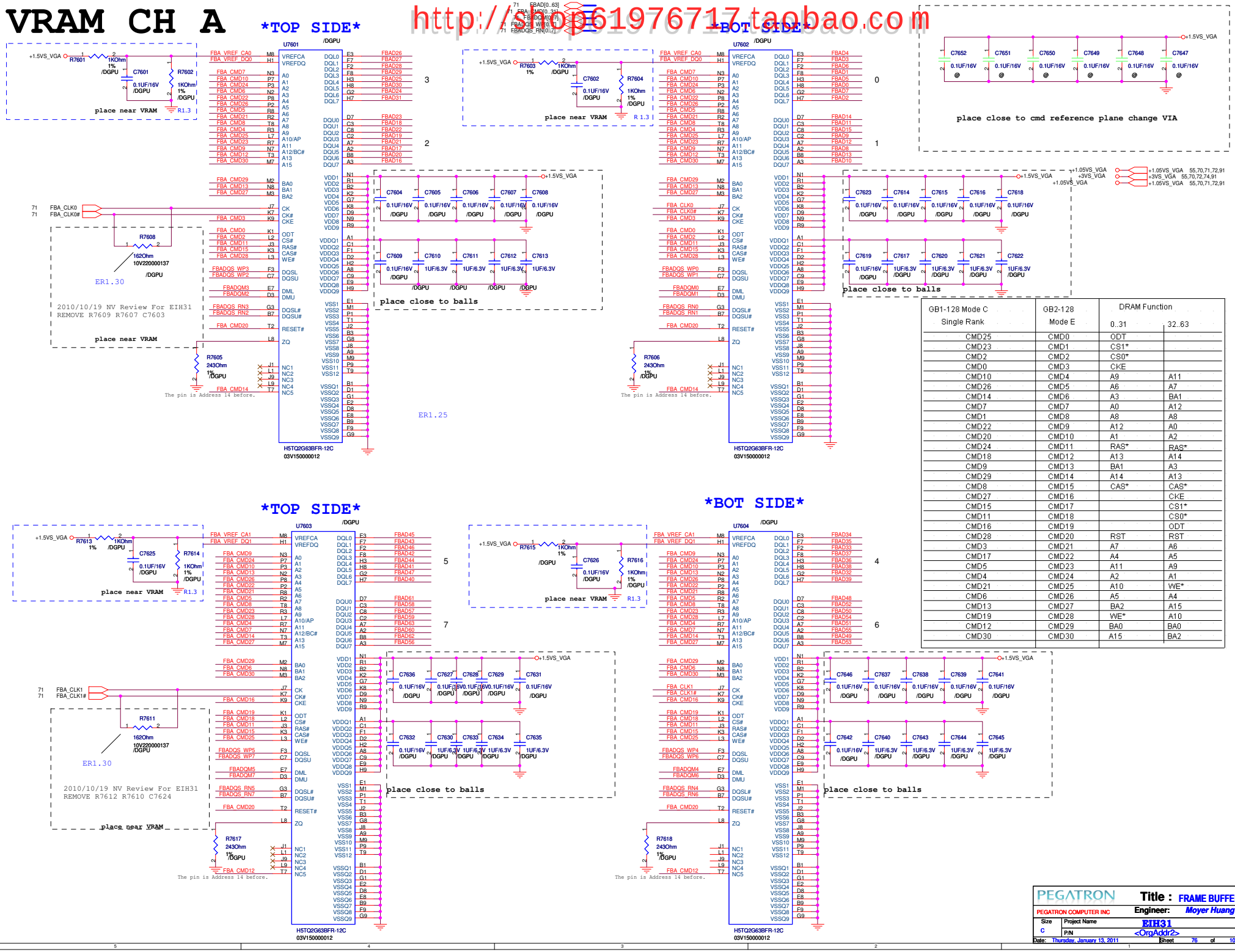
PEGATRON COMPUTER INC

Engineer: Moyer Huang

Size	Project Name	Rev
C	EIH31	1.3
	P/N <OrgAddr2>	

Date: Friday, January 07, 2011 Sheet 75 of 100

VRAM CH A



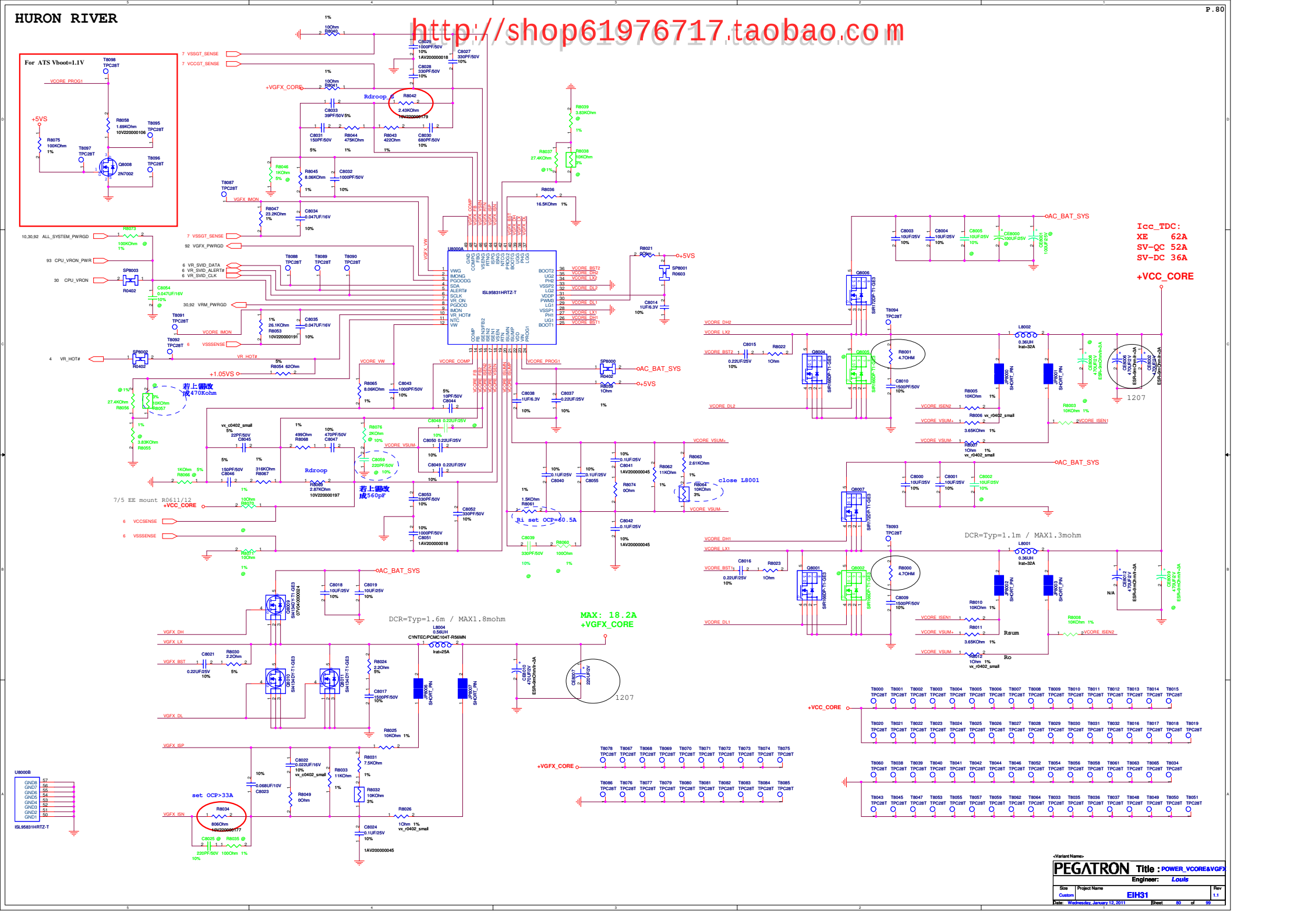
GB1-128 Mode C Single Rank	GB2-128 Mode E	DRAM Function 0..31	32..63
CMD25	CMD0	ODT	
CMD23	CMD1	CS1*	
CMD2	CMD2	CS0*	
CMD0	CMD3	CKE	
CMD10	CMD4	A9	A11
CMD26	CMD5	A6	A7
CMD14	CMD6	A3	BA1
CMD7	CMD7	A0	A12
CMD1	CMD8	A8	A8
CMD22	CMD9	A12	A0
CMD20	CMD10	A1	A2
CMD24	CMD11	RAS*	RAS*
CMD18	CMD12	A13	A14
CMD9	CMD13	BA1	A3
CMD29	CMD14	A14	A13
CMD8	CMD15	CAS*	CAS*
CMD27	CMD16		CKE
CMD15	CMD17		CS1*
CMD11	CMD18		CS0*
CMD16	CMD19		ODT
CMD28	CMD20	RST	RST
CMD3	CMD21	A7	A6
CMD17	CMD22	A4	A5
CMD5	CMD23	A11	A9
CMD4	CMD24	A2	A1
CMD21	CMD25	A10	WE*
CMD6	CMD26	A5	A4
CMD13	CMD27	BA2	A15
CMD19	CMD28	WE*	A10
CMD12	CMD29	BA0	BA0
CMD30	CMD30	A15	BA2

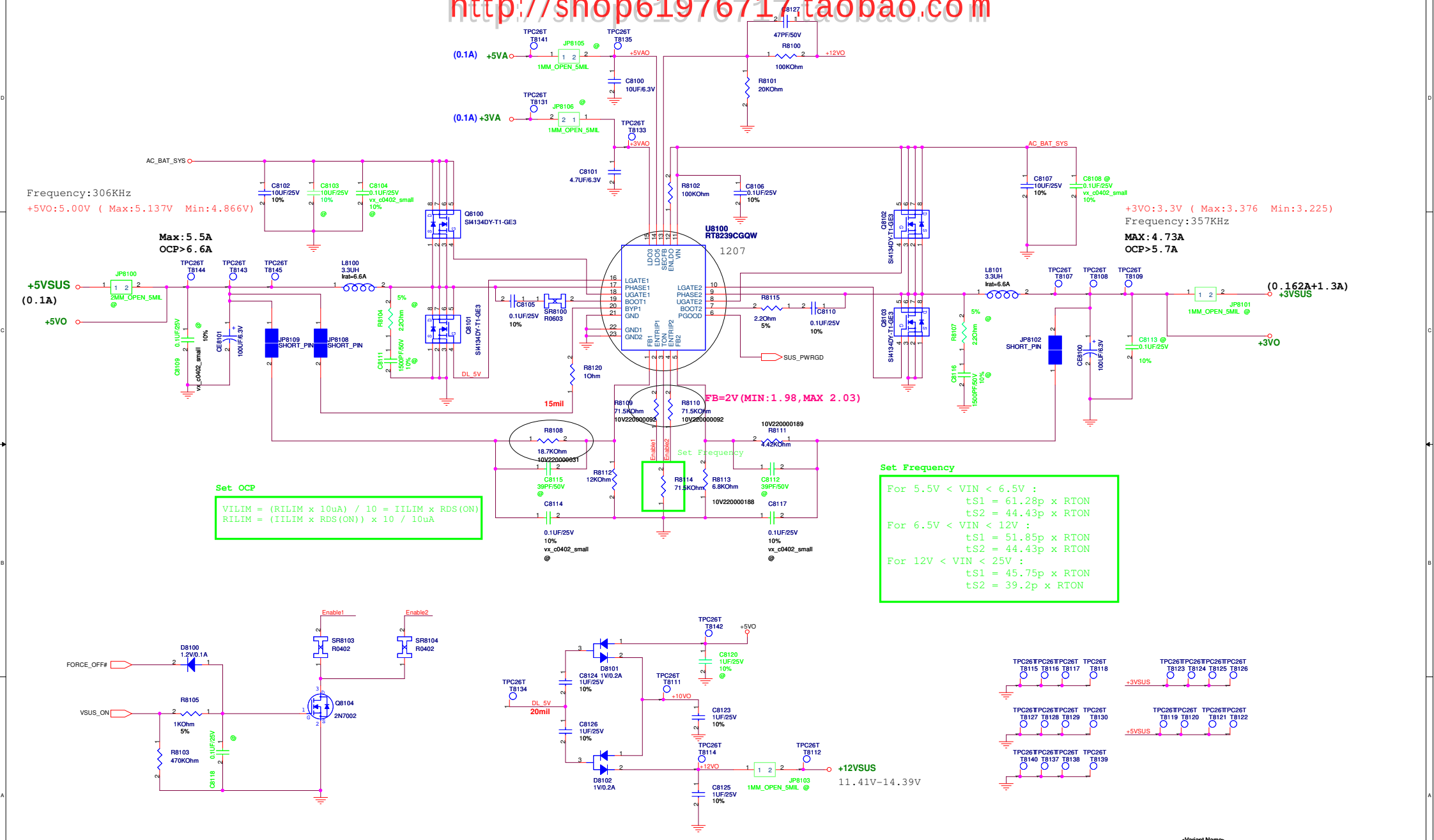
PEGATRON	Title : FRAME BUFFER A		
PEGATRON COMPUTER INC	Engineer: Moyer Huang		
Size C	Project Name EIH31		Rev 1.3
	P/N <OrgAddr2>		
Date: Thursday, January 13, 2011	Sheet 76 of 100		

PEGATRON	Title : FRAME BUFFER C		
PEGATRON COMPUTER INC	Engineer: Moyer Huang		
Size C	Project Name EIH31		Rev 1.3
	P/N <OrgAddr2>		
Date: Tuesday, January 04, 2011	Sheet 77 of 100		

PEGATRON	Title :	FRAME BUFFER C	
PEGATRON COMPUTER INC	Engineer:	Moyer Huang	
Size A	Project Name	EIH31	Rev 1.3
	P/N	<OrgAddr2>	
Date: Tuesday, January 04, 2011	Sheet 78 of 100		

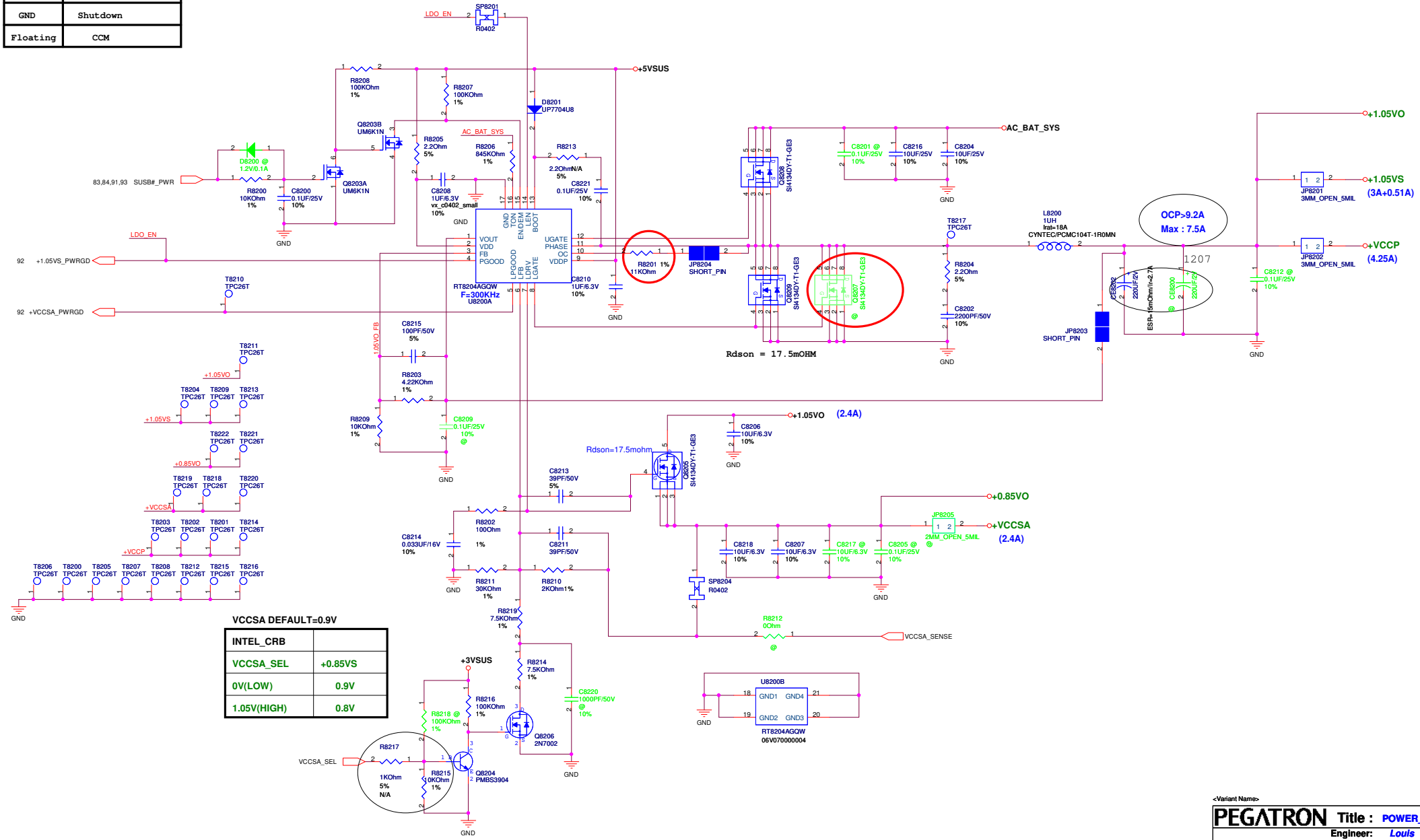
PEGATRON	Title :	FRAME BUFFER C	
PEGATRON COMPUTER INC	Engineer:	Moyer Huang	
Size A	Project Name	EIH31	Rev 1.3
	P/N	<OrgAddr2>	
Date: Tuesday, January 04, 2011	Sheet 79 of 100		





VCCP & VCCSA POWER SUPPLY

EN/DEM	Function
VDD	Diode-emulation'
GND	Shutdown
Floating	CCM



VCCSA DEFAULT=0.9V

INTEL_CRB	
VCCSA_SEL	+0.85VS
0V(LOW)	0.9V
1.05V(HIGH)	0.8V

<Variant Name>

PEGATRON Title : POWER_VCCP

Engineer: Louis

Size	Project Name	Rev
Custom	EIH31	1.1

Date: Thursday, January 13, 2011 Sheet 82 of 94

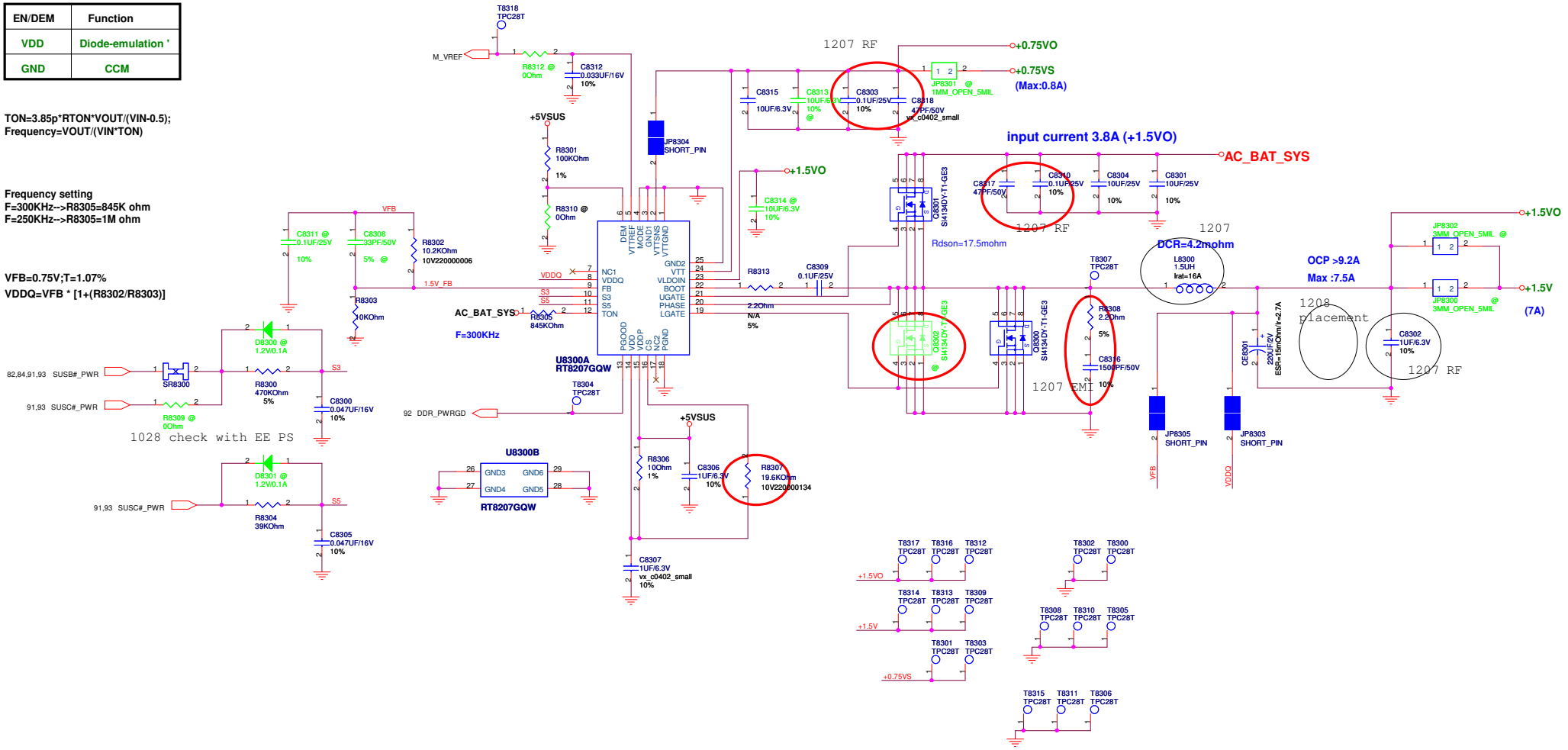
DDR & VTT POWER SUPPLY

EN/DEM	Function
VDD	Diode-emulation '
GND	CCM

TON=3.85p*RTON*VOUT/(VIN-0.5);
Frequency=VOUT/(VIN*TON)

Frequency setting
F=300KHz-->R8305=845K ohm
F=250KHz-->R8305=1M ohm

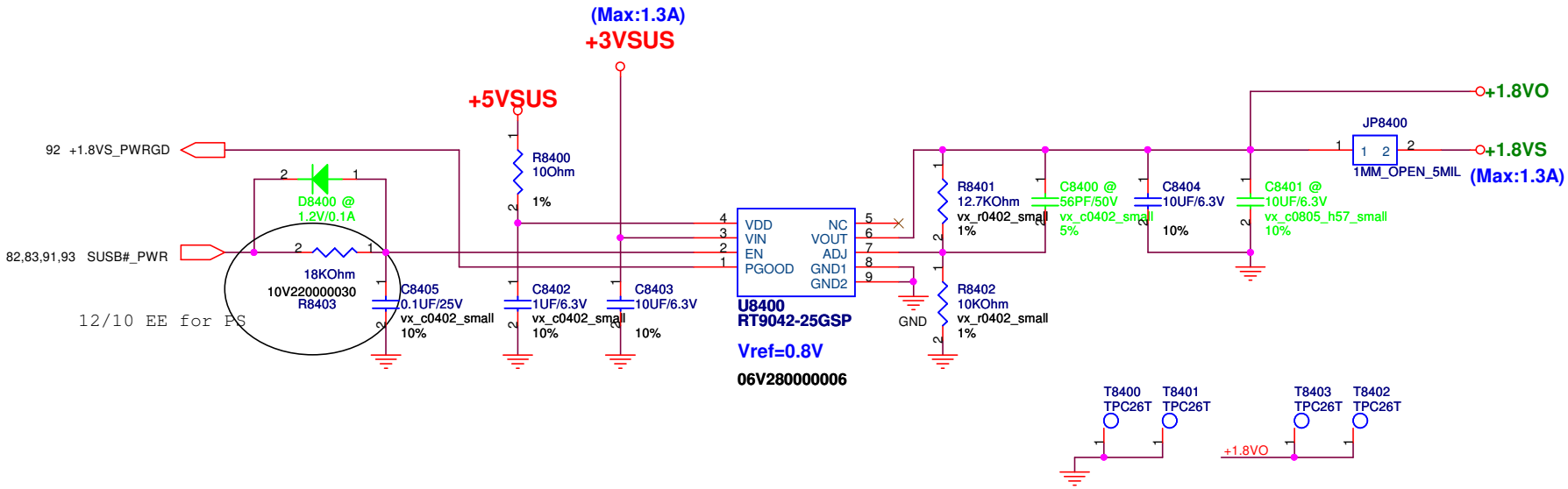
VFB=0.75V;T=1.07%
VDDQ=VFB * [1+(R8302/R8303)]



<Variant Name>

PEGATRON	Title : POWER_DDR & VTT	
	Engineer: Louis	
Size: Custom	Project Name: EIH31	Rev: 1.1
Date: Thursday, January 13, 2011	Sheet 83 of 94	

1.8VS POWER SUPPLY

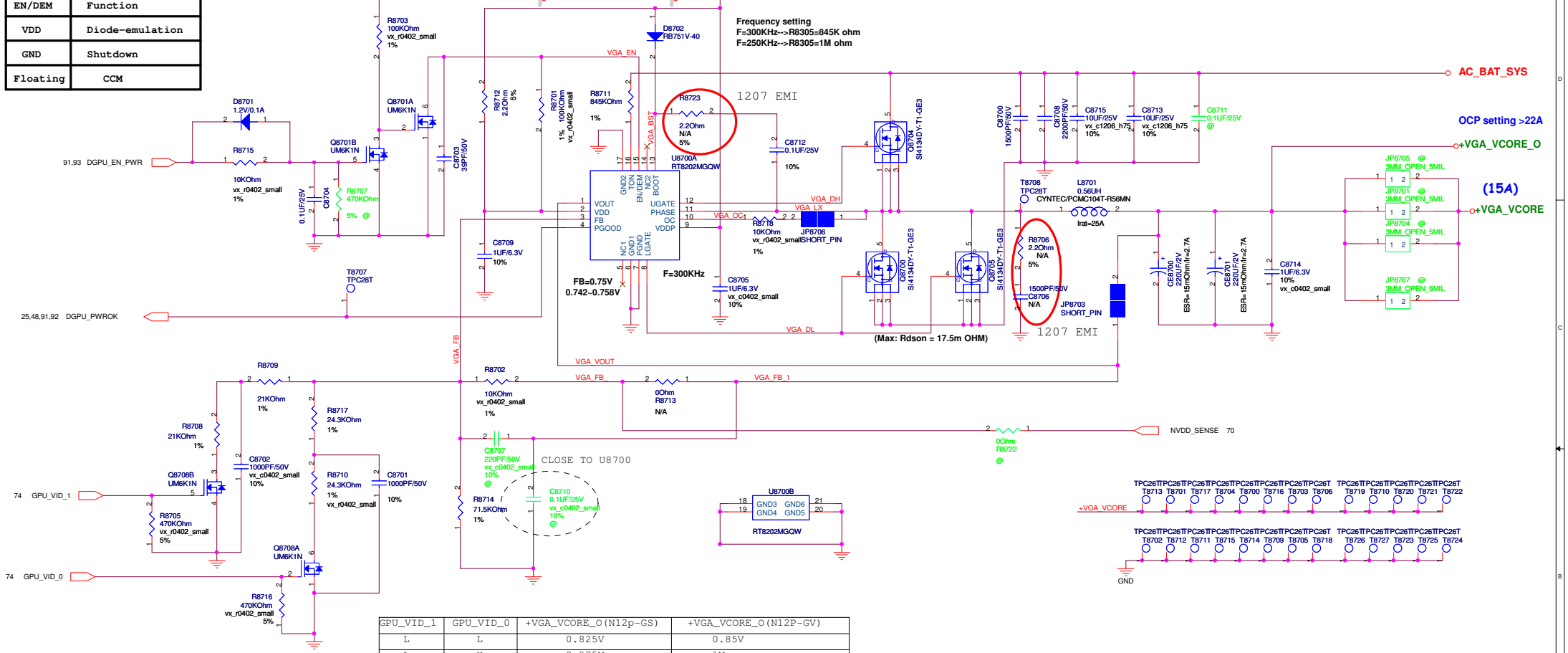


<Variant Name>

PEGATRON	Title : POWER_1.8VS	
	Engineer: *Louis*	
Size: Custom	Project Name: EIH31	Rev: 1.1
Date: Wednesday, January 12, 2011	Sheet 84 of 94	

DSC

EN/DEM	Function
VDD	Diode-emulation
GND	Shutdown
Floating	CCM



GPU_VID_1	GPU_VID_0	+VGA_VCORE_O(N12p-GS)	+VGA_VCORE_O(N12P-GV)
L	L	0.825V	0.85V
L	H	0.975V	1V
H	L	1V	1.025V
H	H	X	

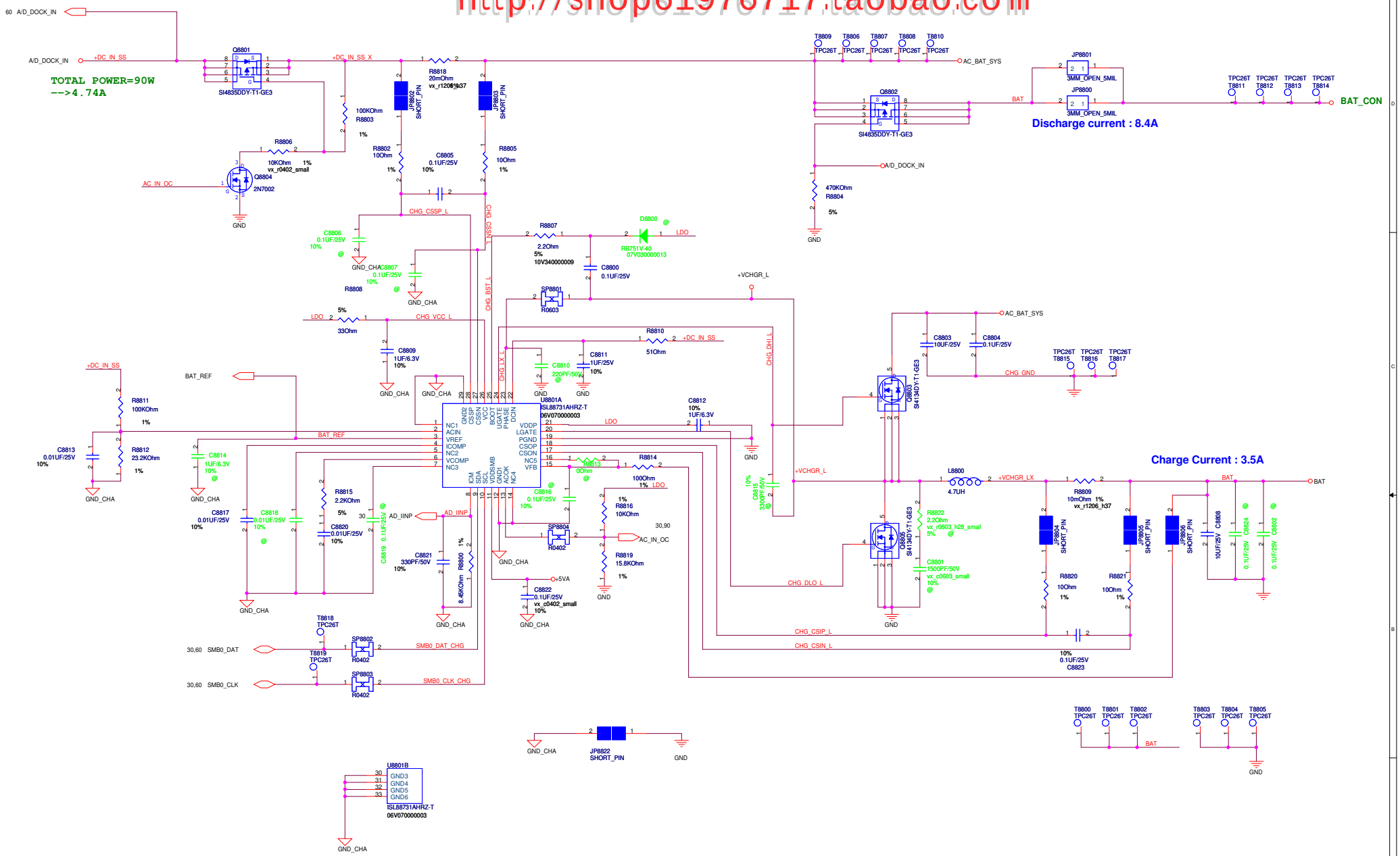
<Variant Name>

PEGATRON Title : POWER_VGA_CORE

Engineer: Louis

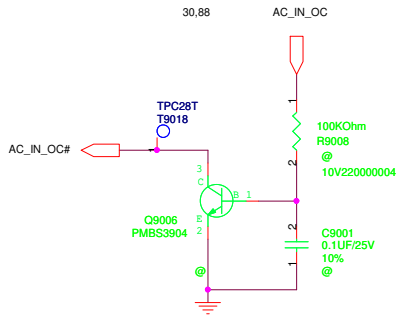
Size	Project Name	Rev
Custom	EIH31	1.1

Date: Wednesday, January 12, 2011 Sheet 87 of 95



BATTERY IN DETECT

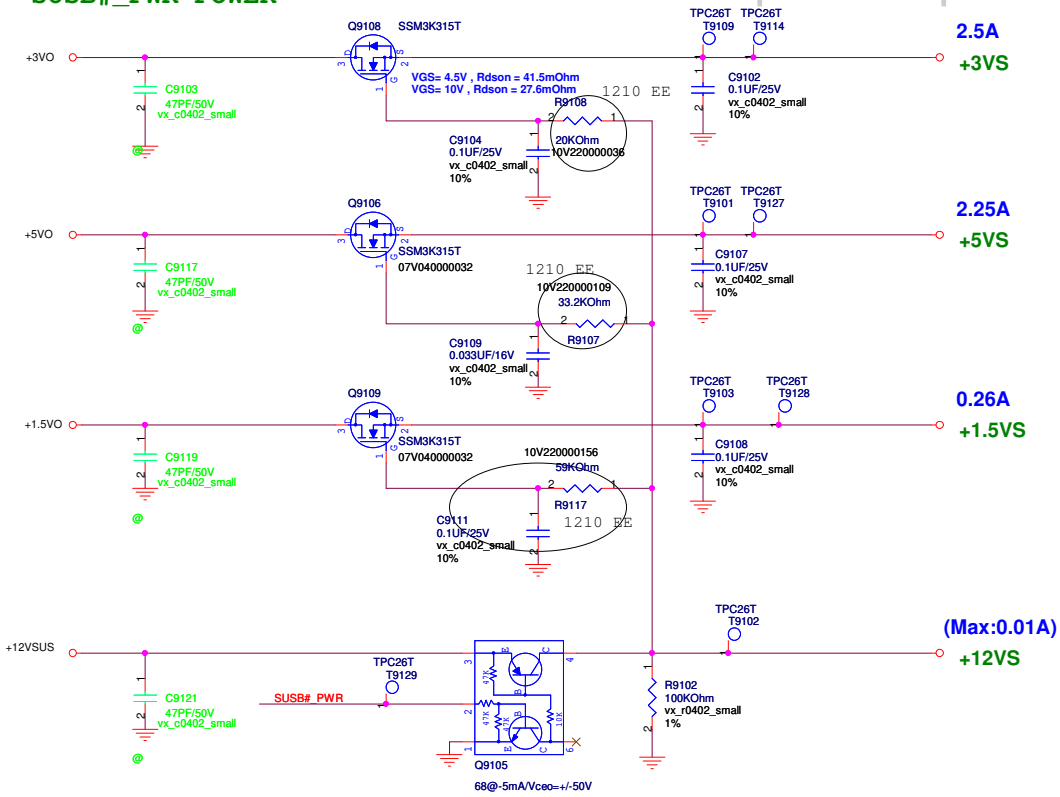
ADAPTER IN DETECT

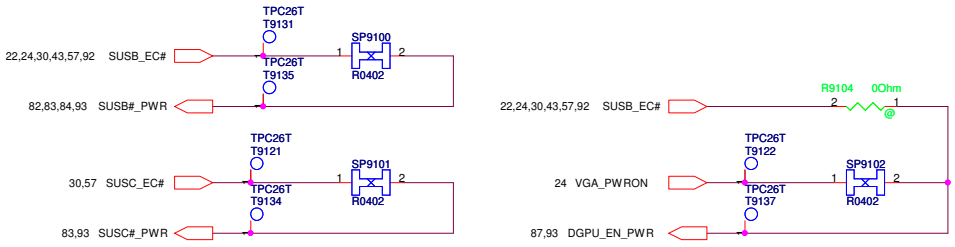


<Variant Name>

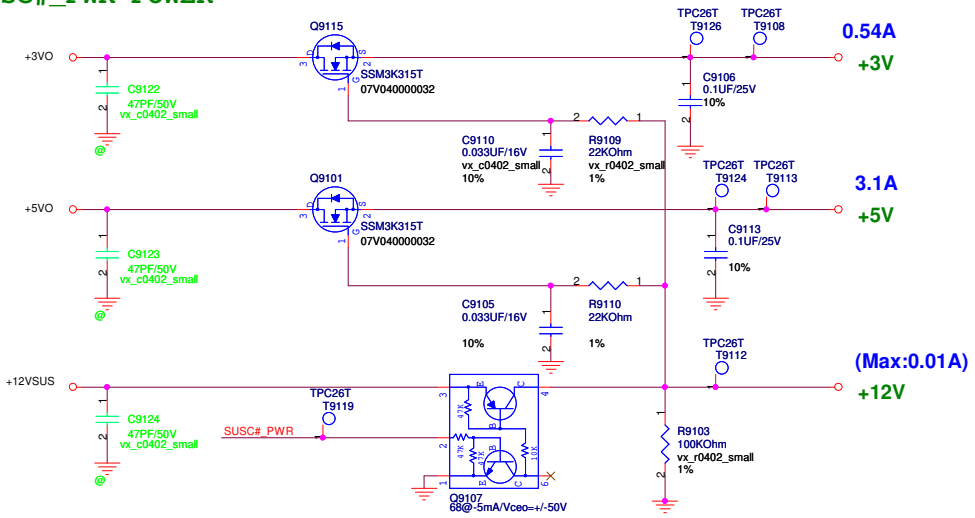
PEGATRON	Title : POWER_DETECT	
	Engineer: *Louis*	
Size: Custom	Project Name: EIH31	Rev: 1.1
Date: Thursday, January 13, 2011	Sheet 90 of 99	

SUSB#_PWR POWER



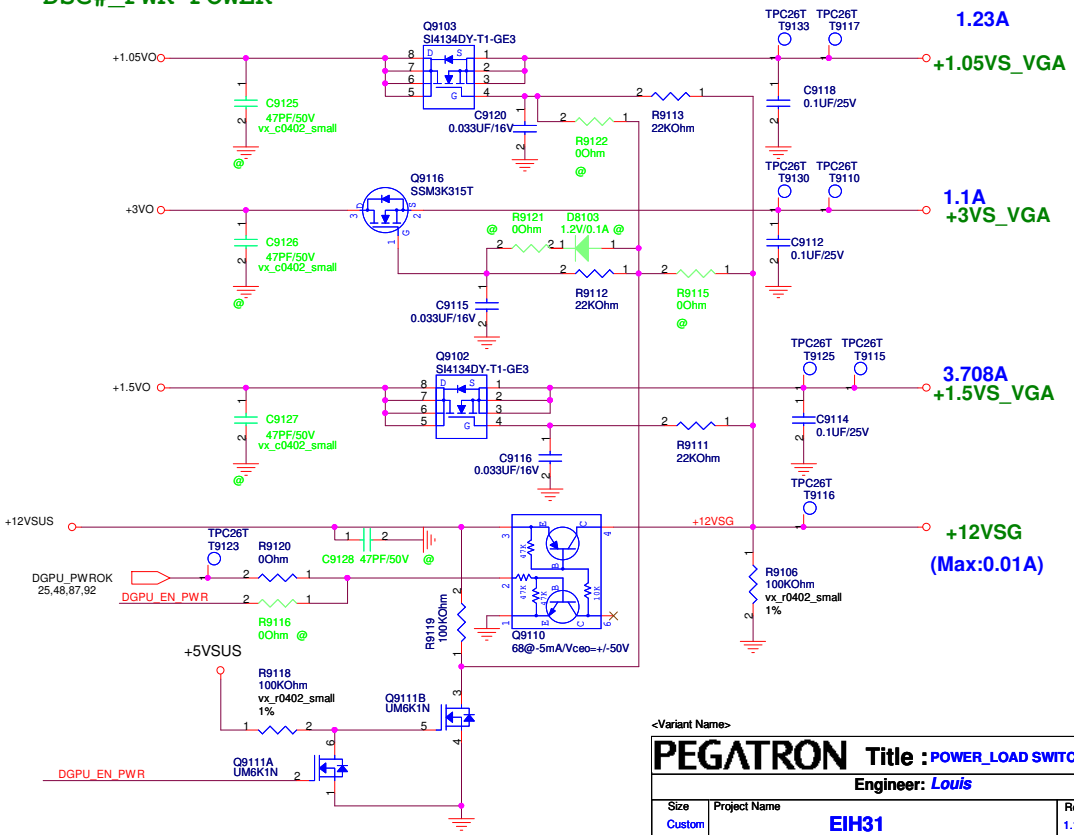


SUSC#_PWR POWER



DSC#_PWR POWER

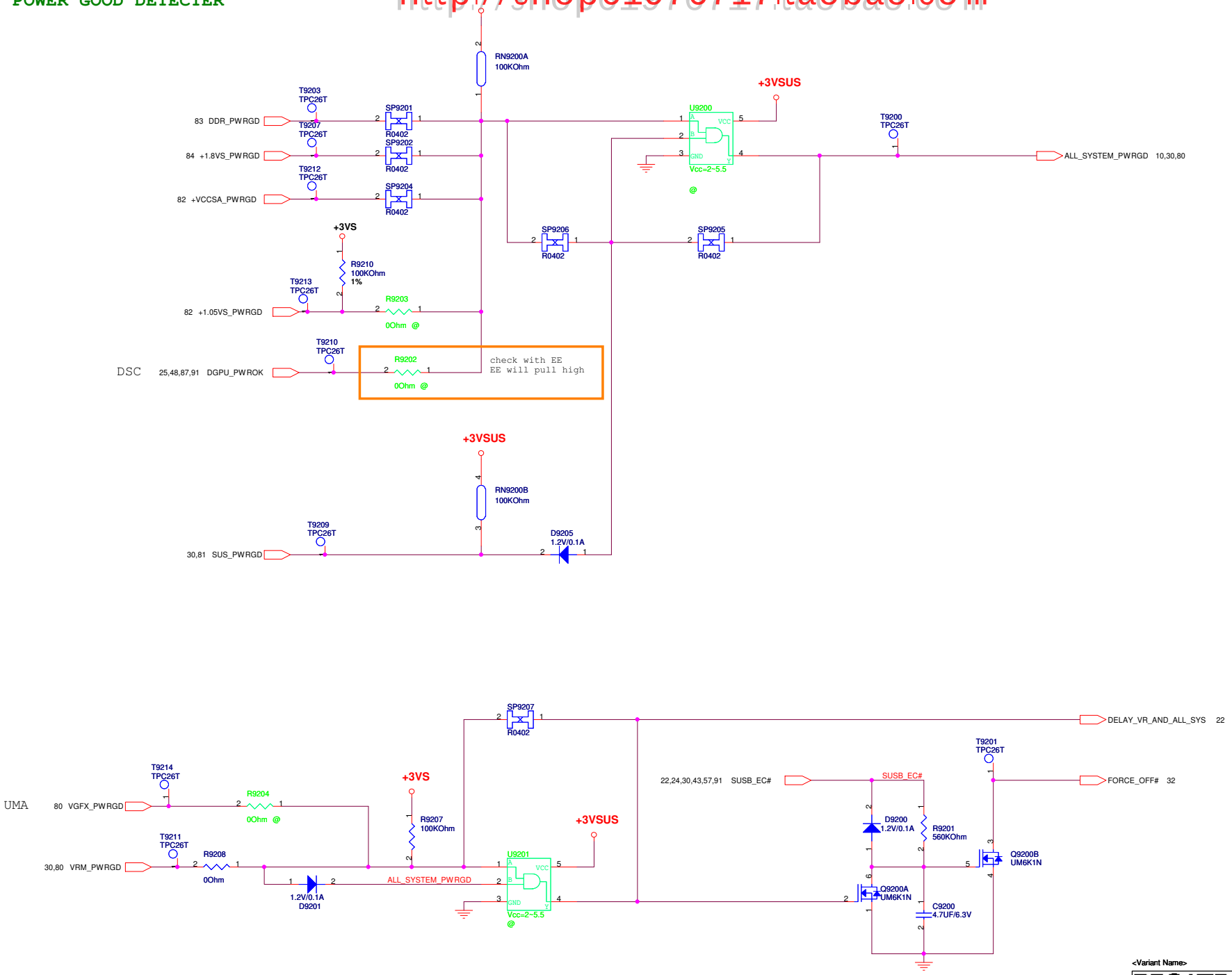
for:17W



<Variant Name>

PEGATRON	Title : POWER_LOAD SWITCH	
	Engineer: Louis	
Size: Custom	Project Name: EIH31	Rev: 1.1
Date: Thursday, January 13, 2011	Sheet 91 of 99	

POWER GOOD DETECTER

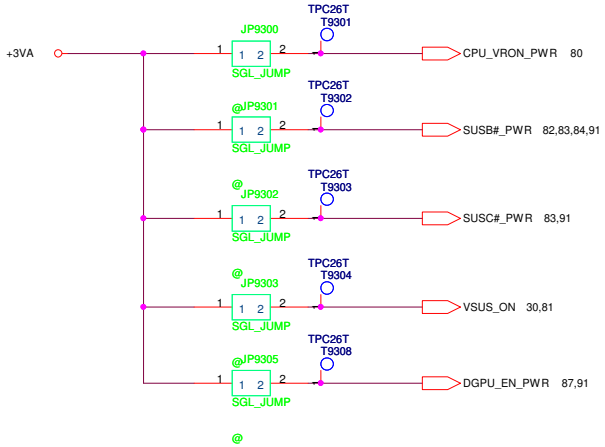


<Variant Name>

PEGATRON	Title :POWER_PROTECT	
	Engineer: *Louis*	
Size: Custom	Project Name: EIH31	Rev: 1.1
Date: Thursday, January 13, 2011	Sheet 92 of 99	

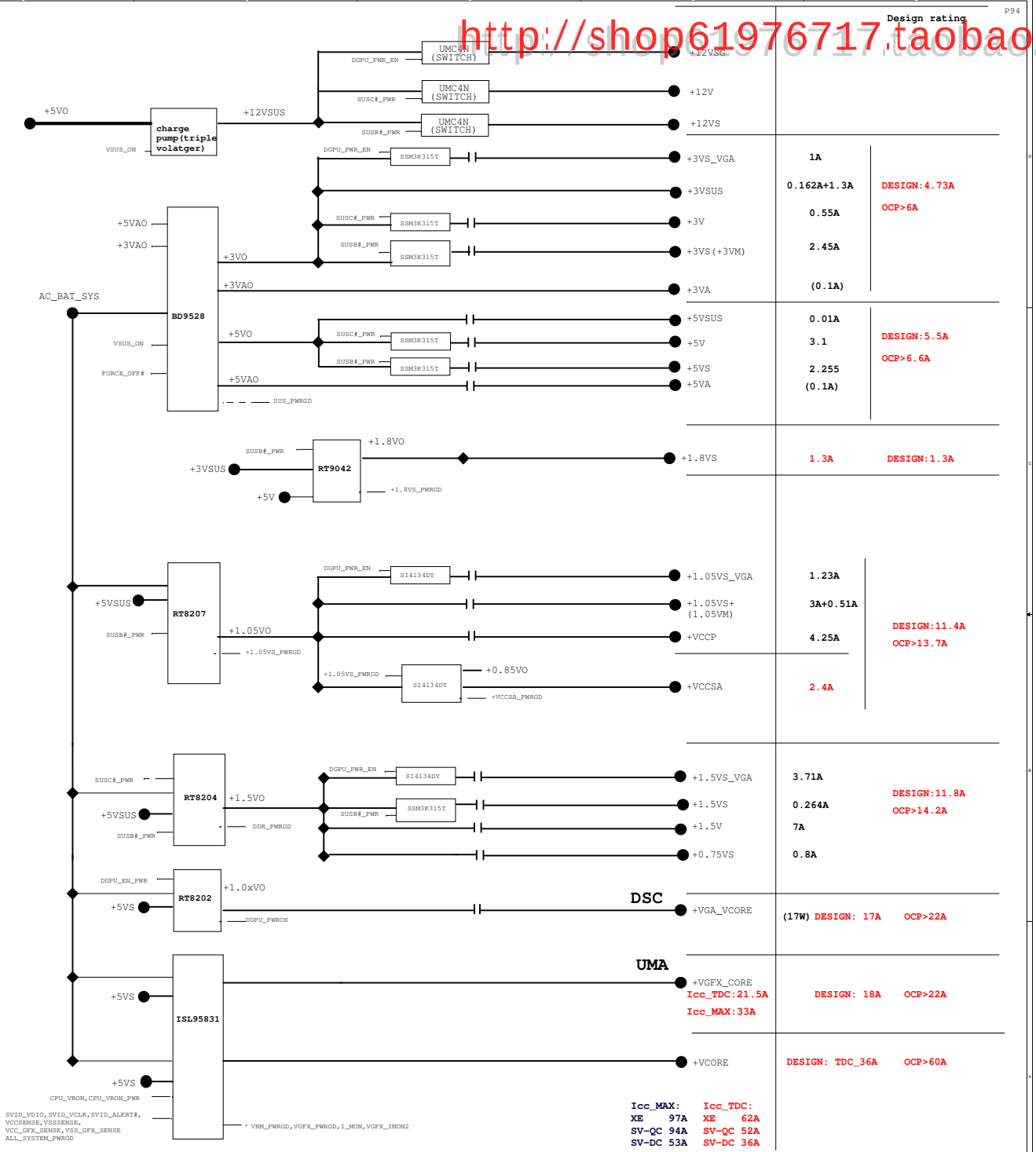
AC_BAT_SYS	AC_BAT_SYS	45,80,81,82,83,87,88
BAT	BAT	88
BAT_CON	BAT_CON	60,88
+3VA	+3VA	20,27,30,37,56,57,81
+3VAO	+3VAO	20,27,30,37,56,57,81
+5VAO	+5VAO	81
+5VA	+5VA	56,81,88
+5VO	+5VO	81,91
+3VO	+3VO	81,91
+1.05VO	+1.05VO	82,91
+0.75VO	+0.75VO	83
+1.5VO	+1.5VO	83,91
+1.8VO	+1.8VO	84
+0.85VO	+0.85VO	82
+5VSUS	+5VSUS	22,27,81,82,83,84,87,91
+3VSUS	+3VSUS	4,10,22,24,27,28,30,33,34,81,82,84,92
+12VSUS	+12VSUS	22,28,81,91
+5V	+5V	44,52,56,57,84,91
+3V	+3V	4,24,40,43,45,53,55,56,57,61,91
+12V	+12V	40,91
+1.5V	+1.5V	5,7,16,57,83
+5VS	+5VS	27,30,31,36,46,48,50,51,56,57,80,91
+3VS	+3VS	4,10,16,17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,43,44,45,46,48,50,51,53,56,57,66,80,91,92
+12VS	+12VS	28,36,45,48,91
+1.05VS	+1.05VS	26,27,57,80,82
+0.75VS	+0.75VS	16,17,57,83
+1.5VS	+1.5VS	26,43,53,57,91
+1.8VS	+1.8VS	7,24,26,57,84
+VCCSA	+VCCSA	7,82
+VCC_CORE	+VCC_CORE	6,57,80
+VGFX_CORE	+VGFX_CORE	7,57,80
+VGA_VCORE	+VGA_VCORE	57,75,87
+1.05VS_VGA	+1.05VS_VGA	57,70,71,72,73,91
+1.5VS_VGA	+1.5VS_VGA	57,71,76,77,91
+3VS_VGA	+3VS_VGA	57,70,72,73,74,91
+12VSG	+12VSG	91

FOR POWER TEST



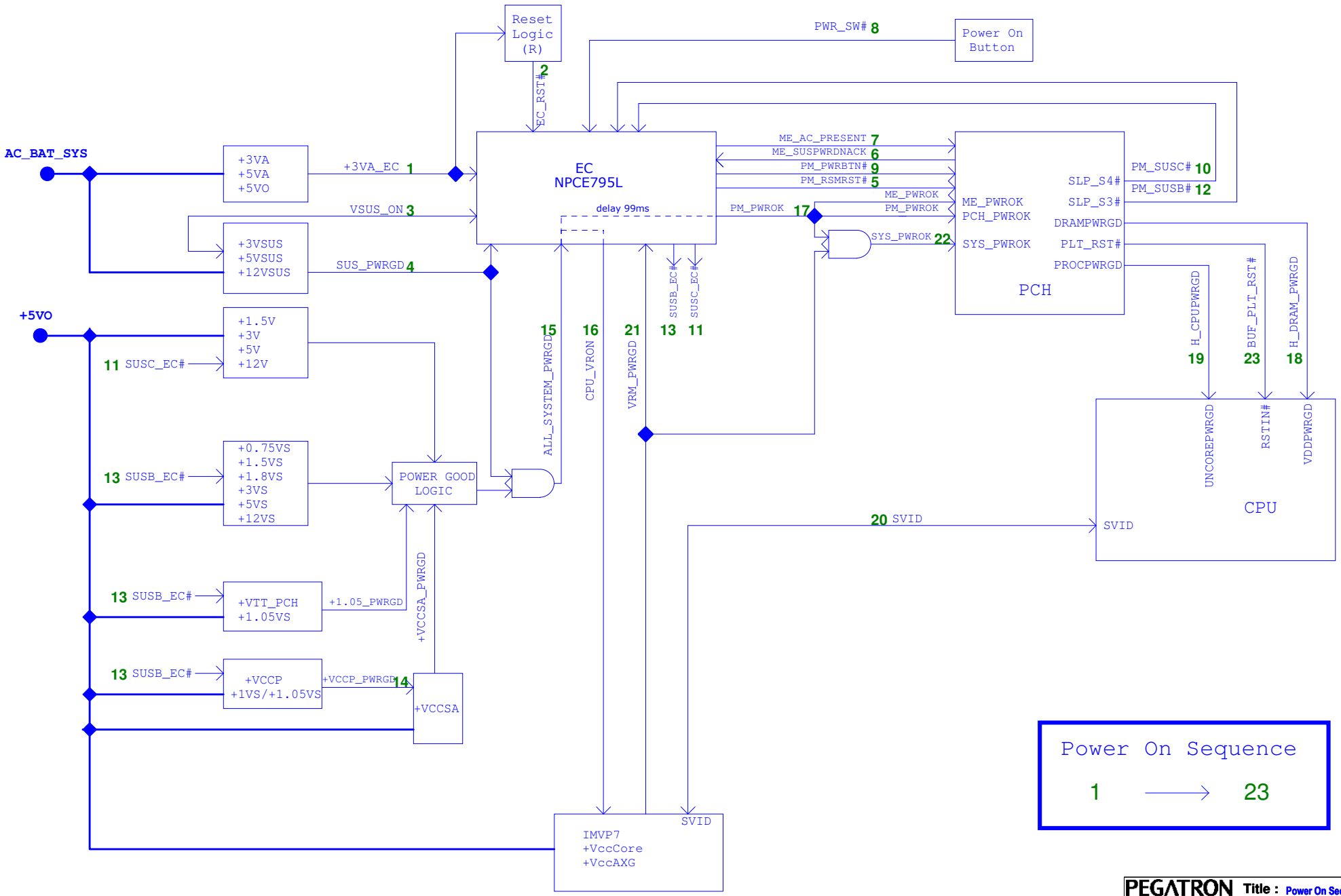
<Variant Name>

PEGATRON	Title : POWER_SIGNAL	
	Engineer: Louos	
Size: Custom	Project Name: EIH31	Rev: 1.1
Date: Thursday, January 13, 2011	Sheet 93 of 99	



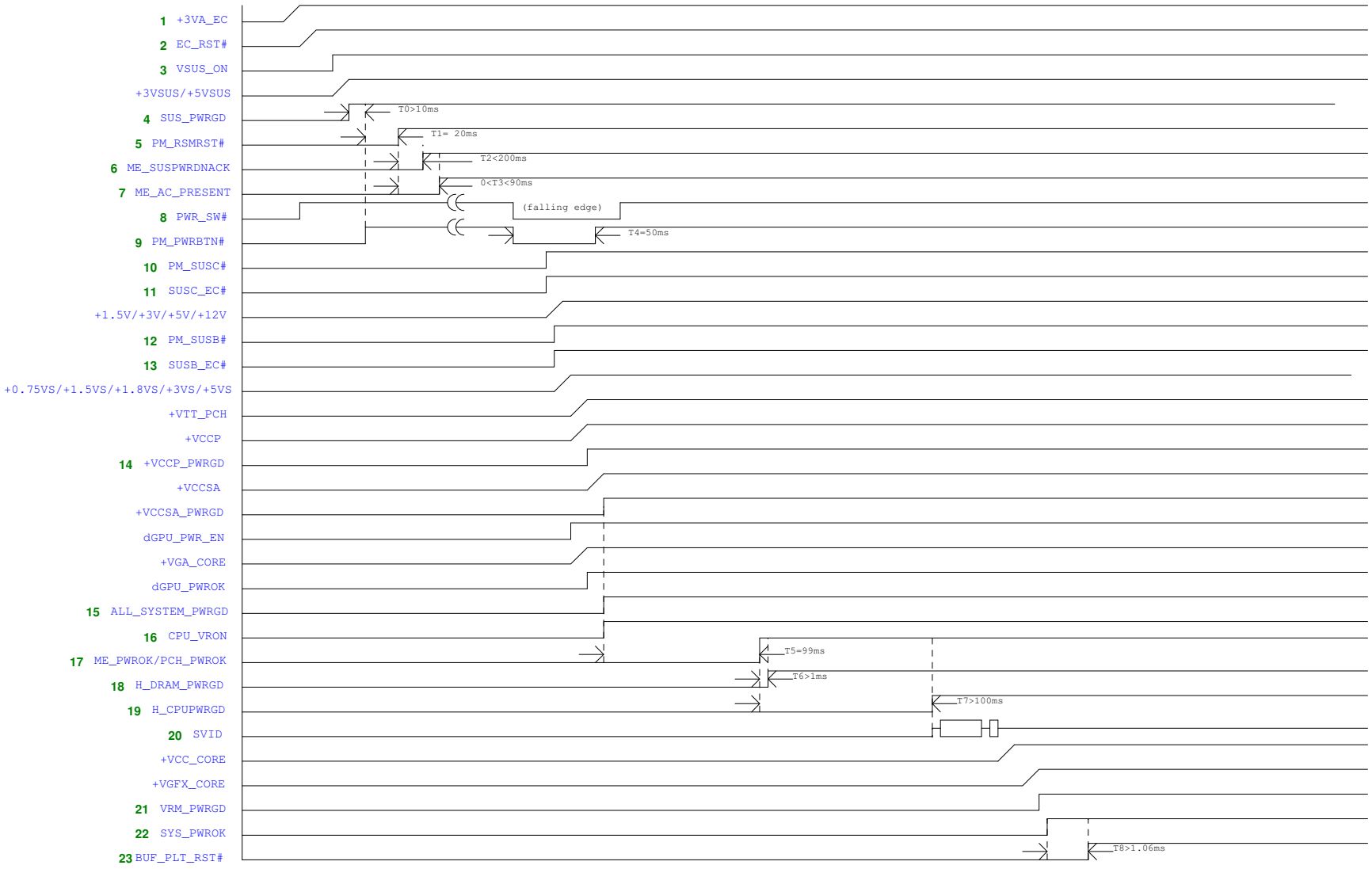
PEGATRON	Title : ****		
BG1\HW1	Engineer: *Ivan Liu*		
Size A	Project Name **H36HC**		Rev 1.3
Date: Tuesday, January 04, 2011		Sheet 96 of 99	

Power On Sequence Diagram G3-S0 R0.3 (non-IAMT,non-Deep Sx)



PEGATRON	Title : Power On Sequence		
<OrgName>	Engineer: JAY TSAI		
Size C	Project Name EIH31		Rev 1.3
Date: Thursday, January 13, 2011	Sheet 98 of 99		

Power On Sequence Diagram G3-S0 R0.3 (non-iAMT,non-Deep Sx)



PEGATRON	Title : Power On Timing	
<OrgName>	Engineer: JAY TSAI	
Size C	Project Name EIH31	Rev 1.3
Date: Tuesday, January 04, 2011	Sheet 99 of 99	