



# Compal Confidential

## Schematics Document

PAW10

Montevina

with Intel Cantiga + ICH9 core logic

REV:1.0A

2010-12-24

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**Clock Generator**  
SLG8SP556VTR

page16

**Mobile Penryn**

uPGA-478 CPU

page4, 5, 6

For 14"  
LS-7011P 4PIN PWR/B  
LS7013P Audio/B  
LS7014P Touch/B

For 15"  
LS-7012P 8PIN PWR/B  
LS7013P Audio/B  
LS7014P Touch/B

H\_A#(3..35)  
H\_D#(0..63)



FSB  
667/800MHz

CRT Connector

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LVDS  
Connector

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**Intel Cantiga GMCH**

GM45

uFCBGA 1329

page 7, 8, 9, 10, 11, 12, 13

Dual Channel  
DDR3-667/800(1.5V)

**DDR3-SO-DIMM X2**

BANK 0, 1, 2, 3

page 14,15

up to 4G

DMI \*4



C-Link

2Channel Speaker  
page26

Analog MIC\_Int  
page26

**Wire Less Mini  
card Slot 1**

page23

6\*PCL-E BUS

**Intel ICH9-M**

page 17,18,19,20

**SPI ROM  
BIOS**

LPC BUS

**EC**  
ENE KB926 E0

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**AR8151/8152**

10/100/Giga LAN

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RJ45 CONN

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AZALIA

**Audio Codec**  
CONEXTAN

CX20671

page26

14\*USB2.0

**CMOS Camera**

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**BlueTooth CONN**

page30

**USB CONN X1(Right)**

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**USB PORT X1(Left)**

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**USB PORT X1(Left)**

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**Audio Jack SB CONN**  
HP X 1+

MIC\_Ext X1

page30

Card Reader RTS5139

Int.KBD

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**SPI ROM  
BIOS**

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**Touch Pad**

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**SATA HDD CONN**

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**SATA ODD CONN**

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DDR3 Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

SMBUS Control Table

	SOURCE	BATT	KB926	SODIMM	CLK CHIP	WLAN WWAN	ICH9	Thermal
EC_SMB_CK1 EC_SMB_DA1	KB926 +3VALW	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926 +3VALW	X	X	X	X	X	X	V +3VS
ICH_SMBCLK ICH_SMBDATA	ICH +3VALW	X	X	V +3VS	V +3VS	V +3VALW	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM	A0	10100000
DDR SO-DIMM	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

@ FUNCTION

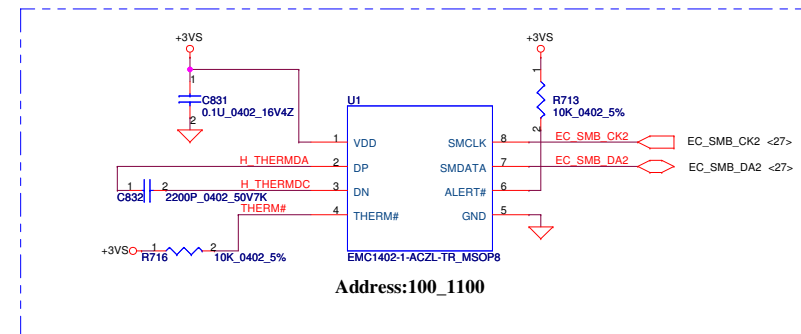
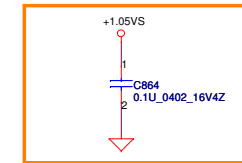
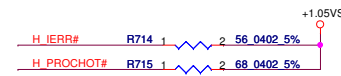
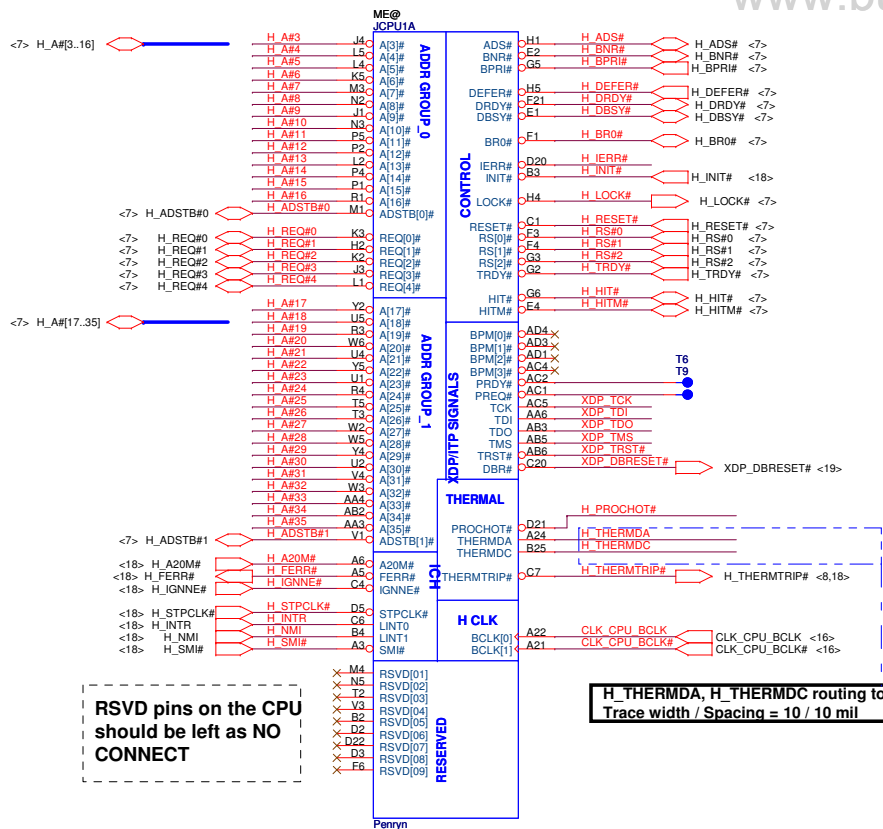
Structure	Description	NON-USE
45@	45 BOM	
BT@	Blue Tooth function	
CMOS@	CMOS CAMERA function	

PCIe PORT LIST

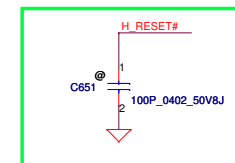
PORT	DEVICE
1	LAN
2	
3	WLAN
4	
5	
6	
7	
8	

USB PORT LIST

PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	
4	CARD READER
5	WIRELESS
6	BT
7	USB PORT (ESATA)
8	
9	
10	
11	
12	
13	

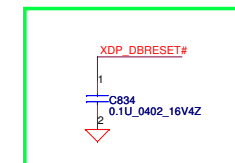


10/01 Add for reduce noise



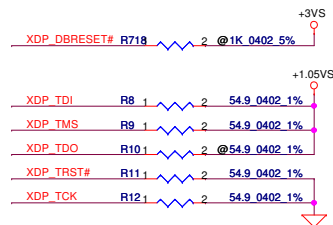
Place closely pin C1

09/16 Add C834 For ESD

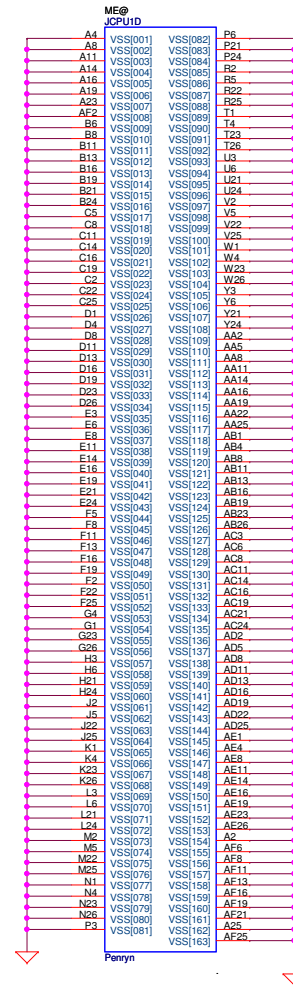


Place closely pin C20

## XDP Reserve for debug , Please close to CPU side



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FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

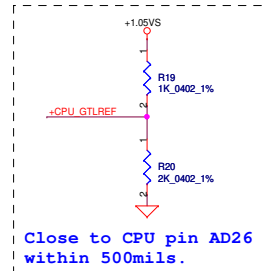
TRACE CLOSELY CPU < 0.5

COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)

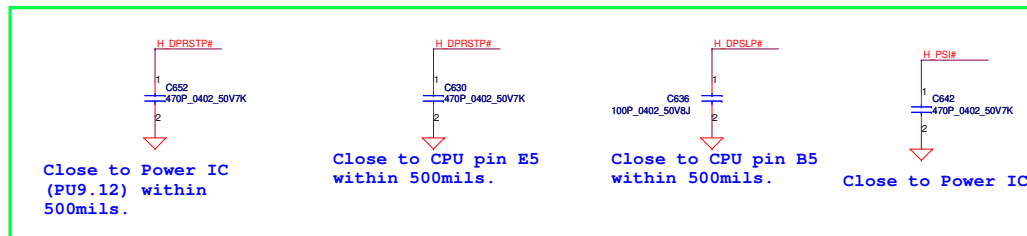
COMP1, COMP3 layout : Width 5mils and Space 25mils (55Ohms)

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

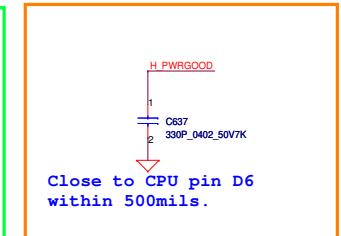
Layout note: Z0=55 ohm  
0.5" max for GTLREF.



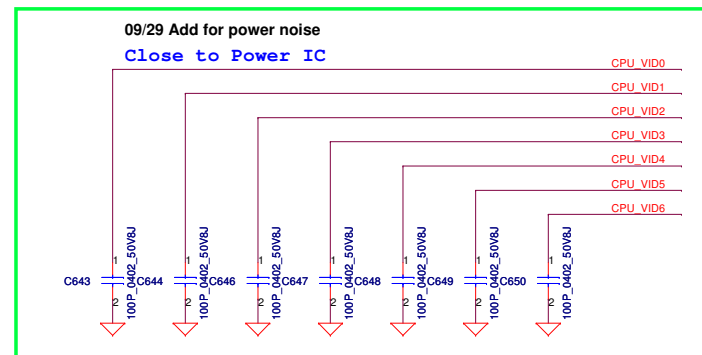
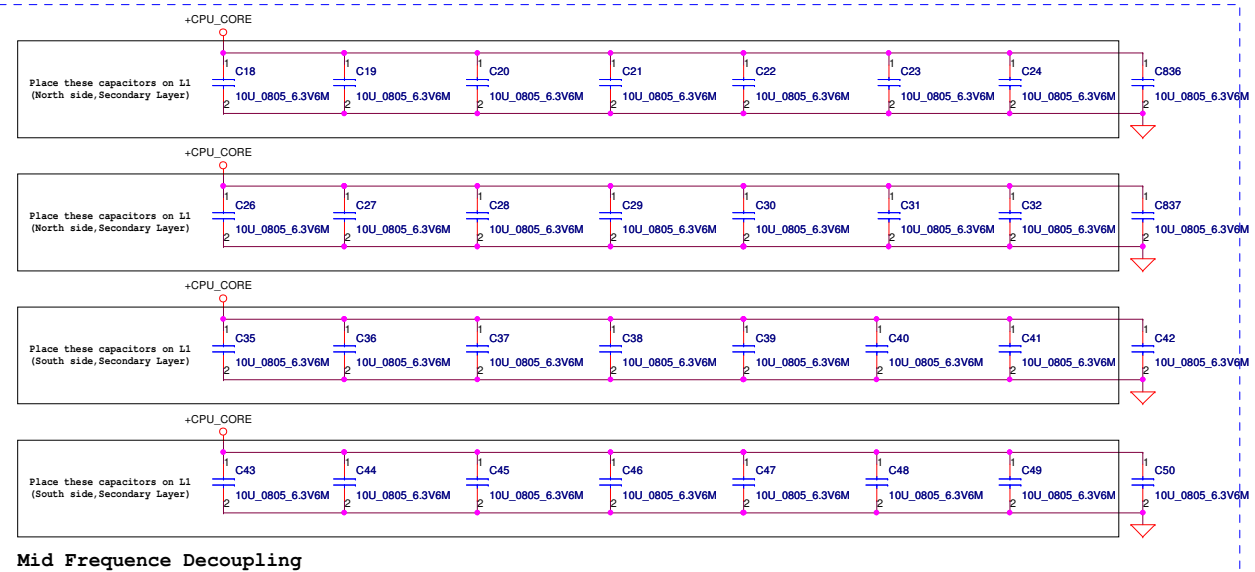
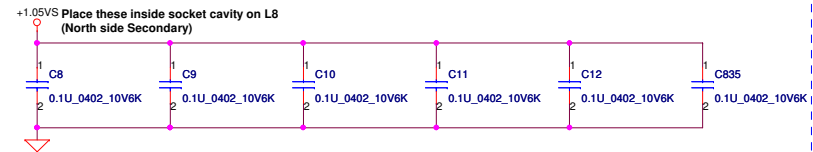
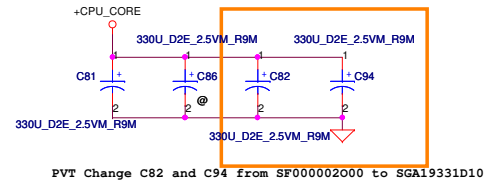
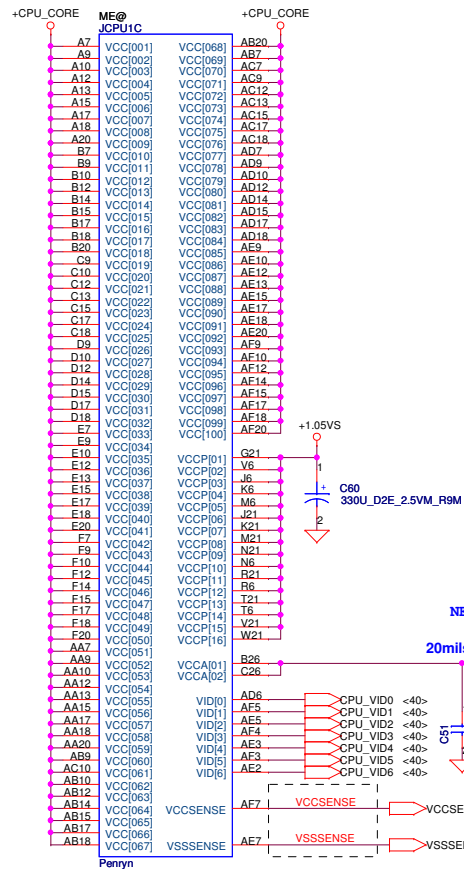
09/29 Add for power noise



### PVT for ESD solution

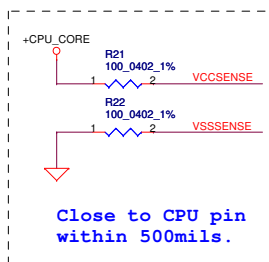


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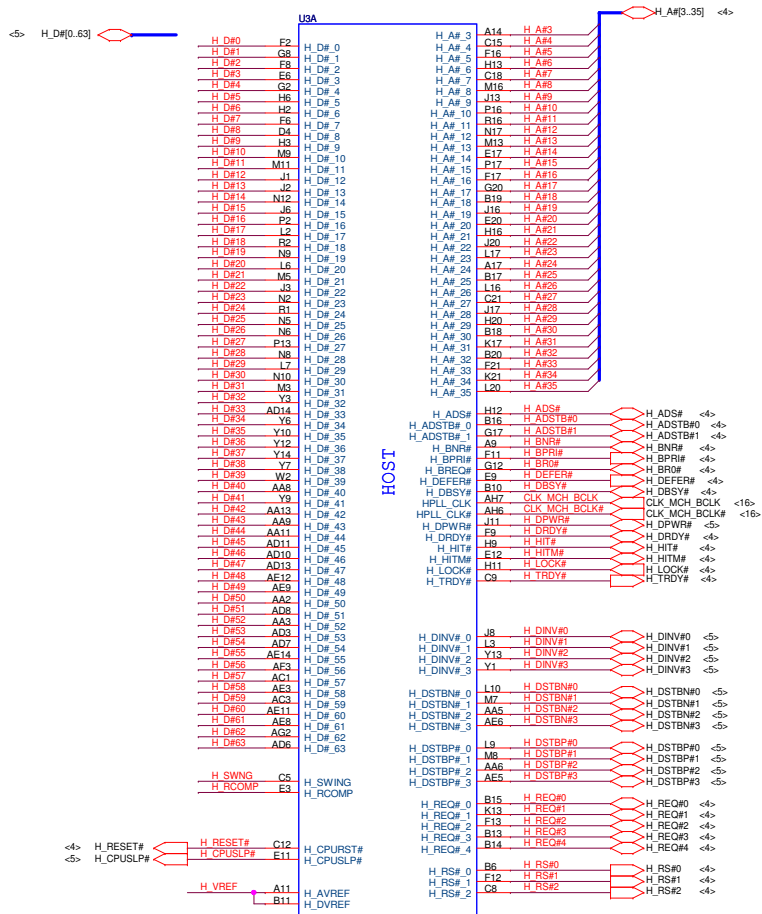


The trace width/space/other is 18/7/25.

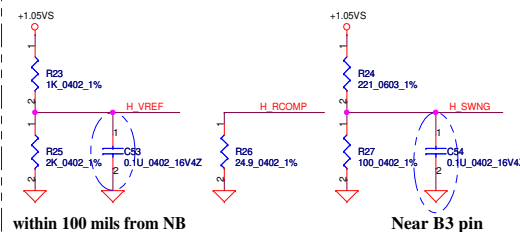
Layout Note:  
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.  
Place PU and PD within 1 inch of CPU.  
Length matched to within 25 mils.



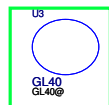
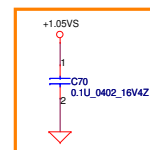
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**Layout Note:**  
H\_RCOMP / H\_VREF / H\_SWING  
trace width and spacing is 10/20



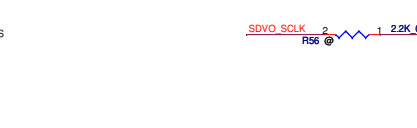
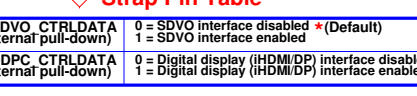
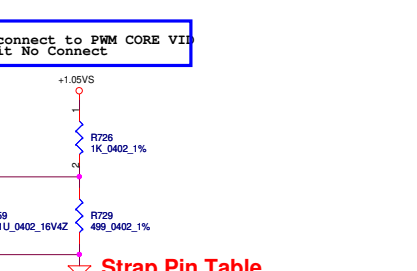
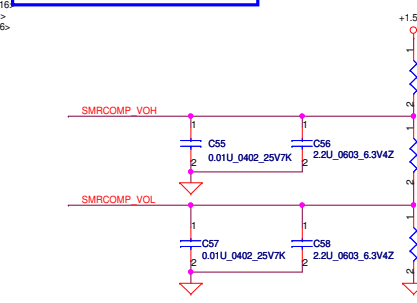
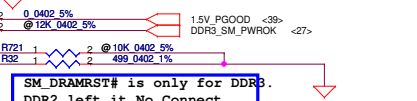
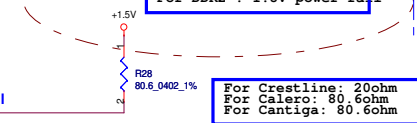
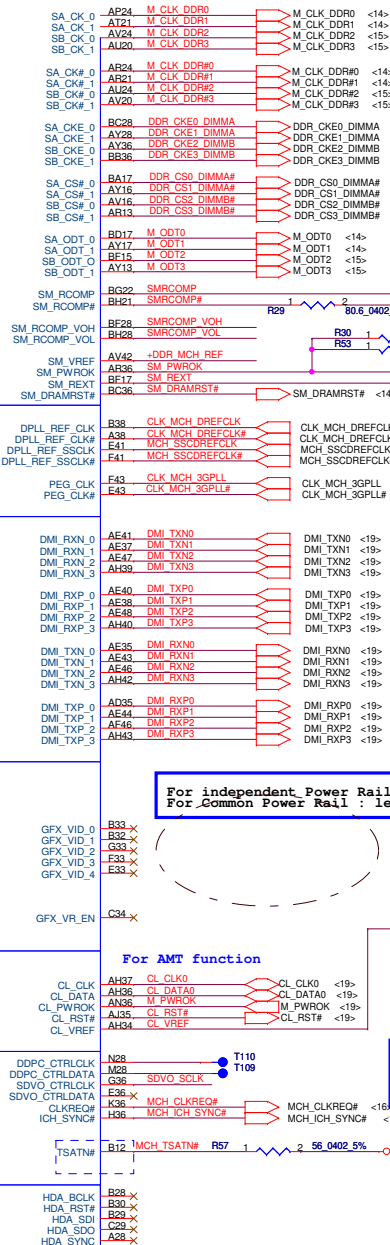
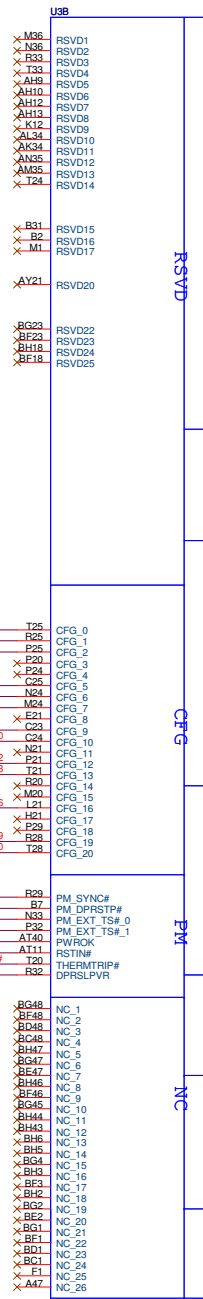
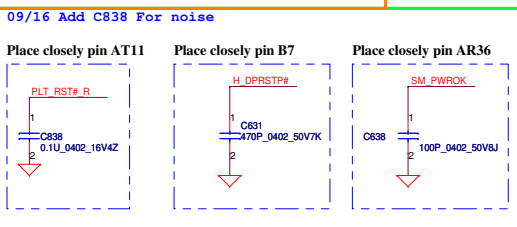
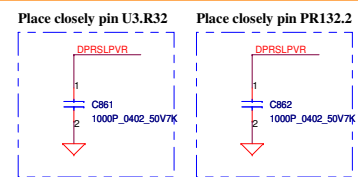
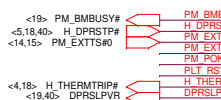
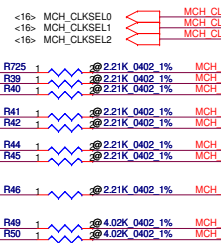
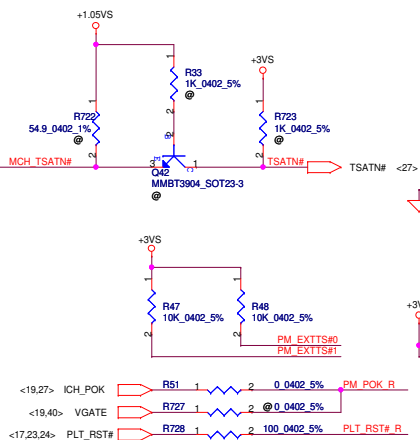
**PVT ESD solution.**  
Please close to R23



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## Strap Pin Table

CFG[2:0]		011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	Internal pull-up	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	Internal pull-up	0 = ITPM Host Interface is enabled can support disable by SW. 1 = ITPM Host Interface is Disabled * (Default)
CFG7	Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality * (Default)
CFG9	Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	Internal pull-up	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12]	Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation * (Default)
CFG16	Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	Internal pull-down	0 = Normal Operation 1 = DMI Lane Reversal Enable * (Default)
CFG20	Internal pull-down (PCIe/SDVO select)	0 = Only PCIe or (SDVO/DP/HDMI) is operational. * (Default) 1 = PCIe/(SDVO/DP/HDMI) are operating simul.



**Layout Note:**  
+DDR\_MCH\_REF trace  
width and spacing is 20/20.  
**CLOSE TO PIN.AV42**

```
DDR3 : 1.5V power rail
DDR2 : 1.8V power rail
```

For Crestline: 20ohm  
For Calero: 80.6ohm  
For Cantiga: 80.6ohm

SM\_DRAMRST# is only for DDR3  
DDR2 left it No Connect

For independent Power Rail : connect to PWM CORE VDD  
For Common Power Rail : left it No Connect

For AMT function

### Strap Pin Table

<b>SDVO_CTRLDATA</b> (Internal pull-down)	0 = SDVO interface disabled <b>*</b> (Default) 1 = SDVO interface enabled
<b>DDPC_CTRLDATA</b> (Internal pull-down)	0 = Digital display (iHDMI/DP) interface disabled <b>*</b> (Default) 1 = Digital display (iHDMI/DP) interface enabled

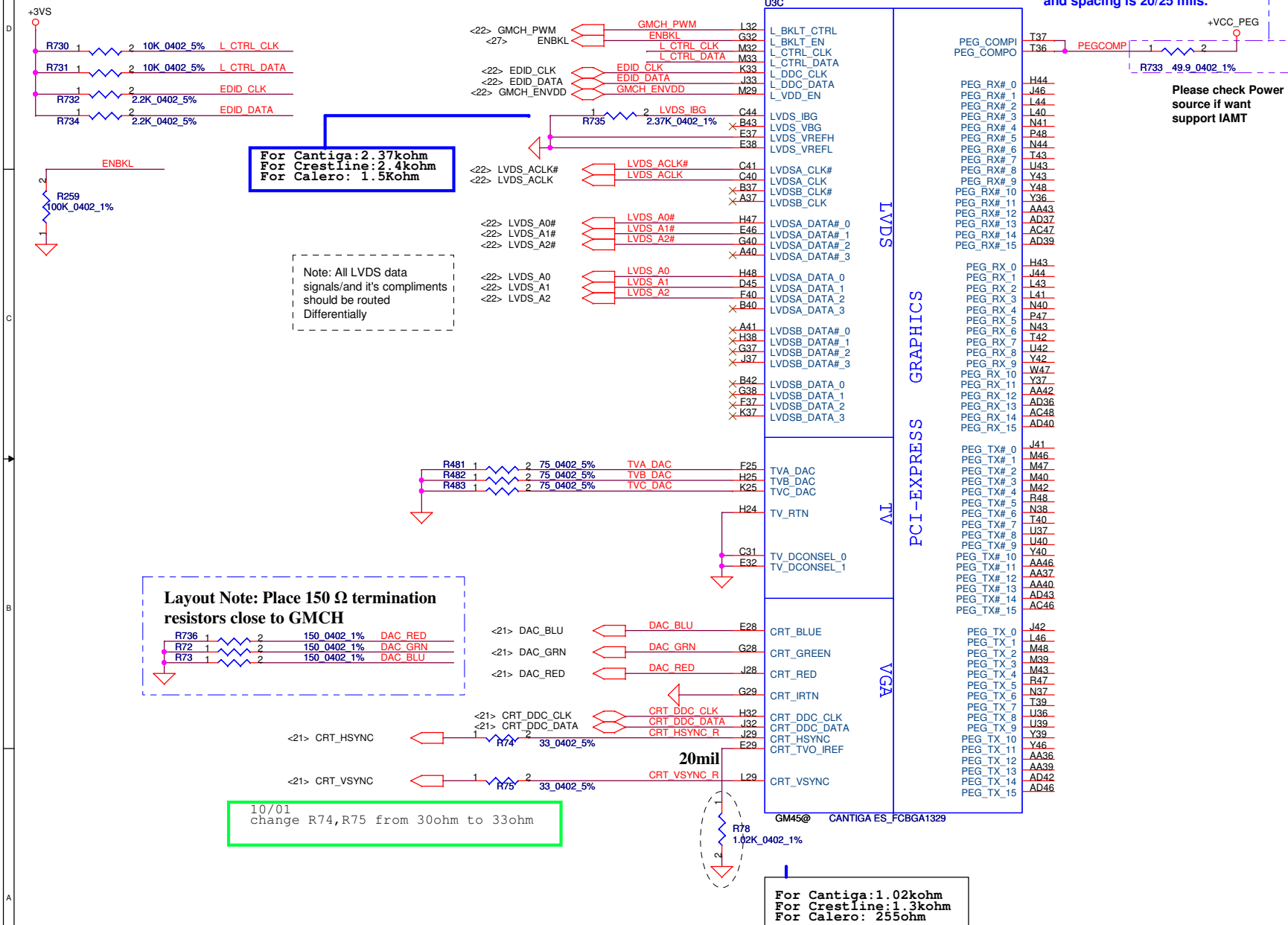
Notice: Please check HDA power rail to select HDA controller.

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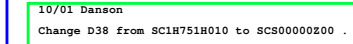
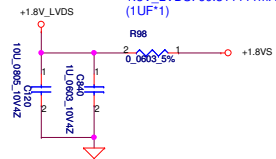




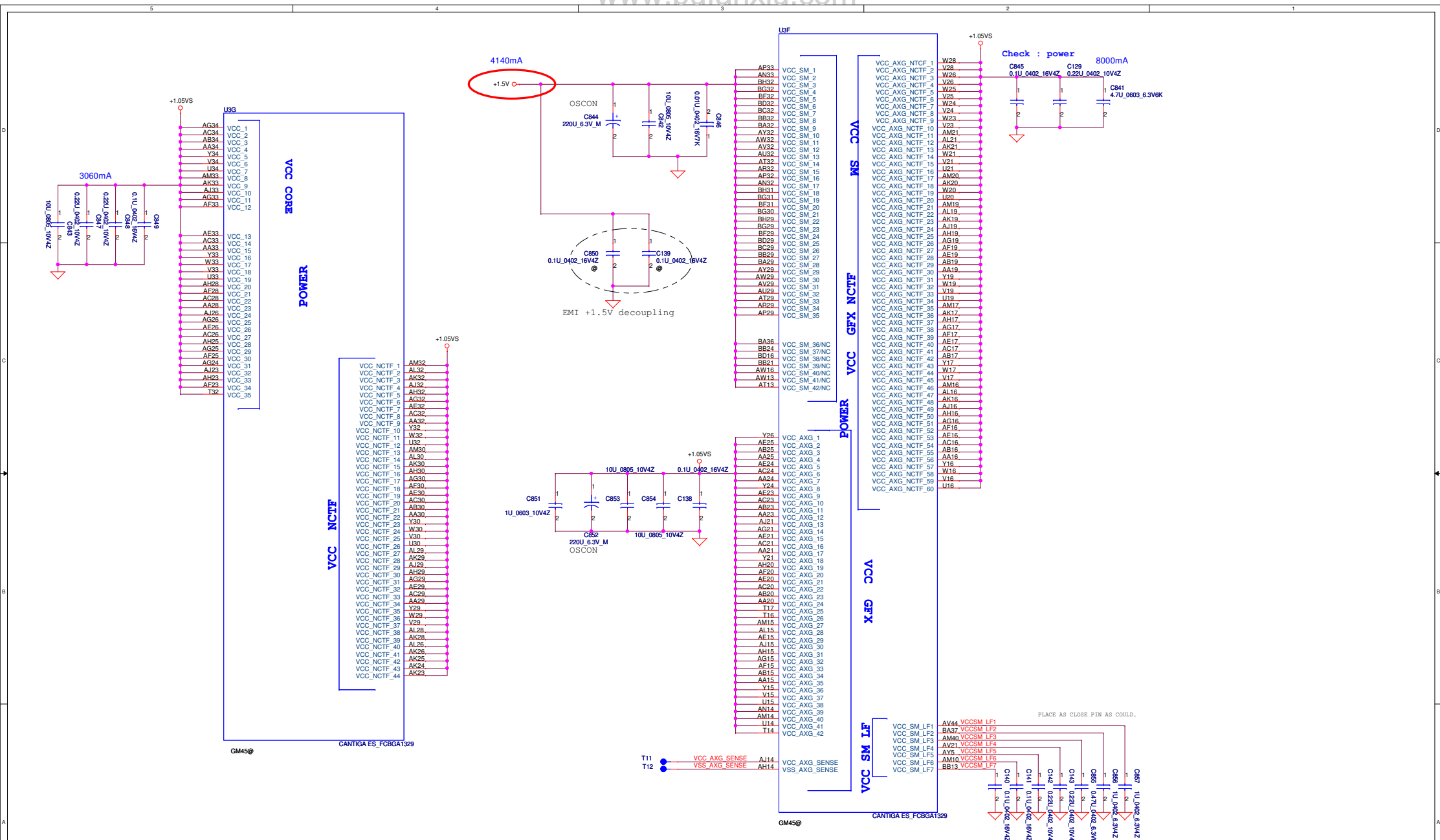
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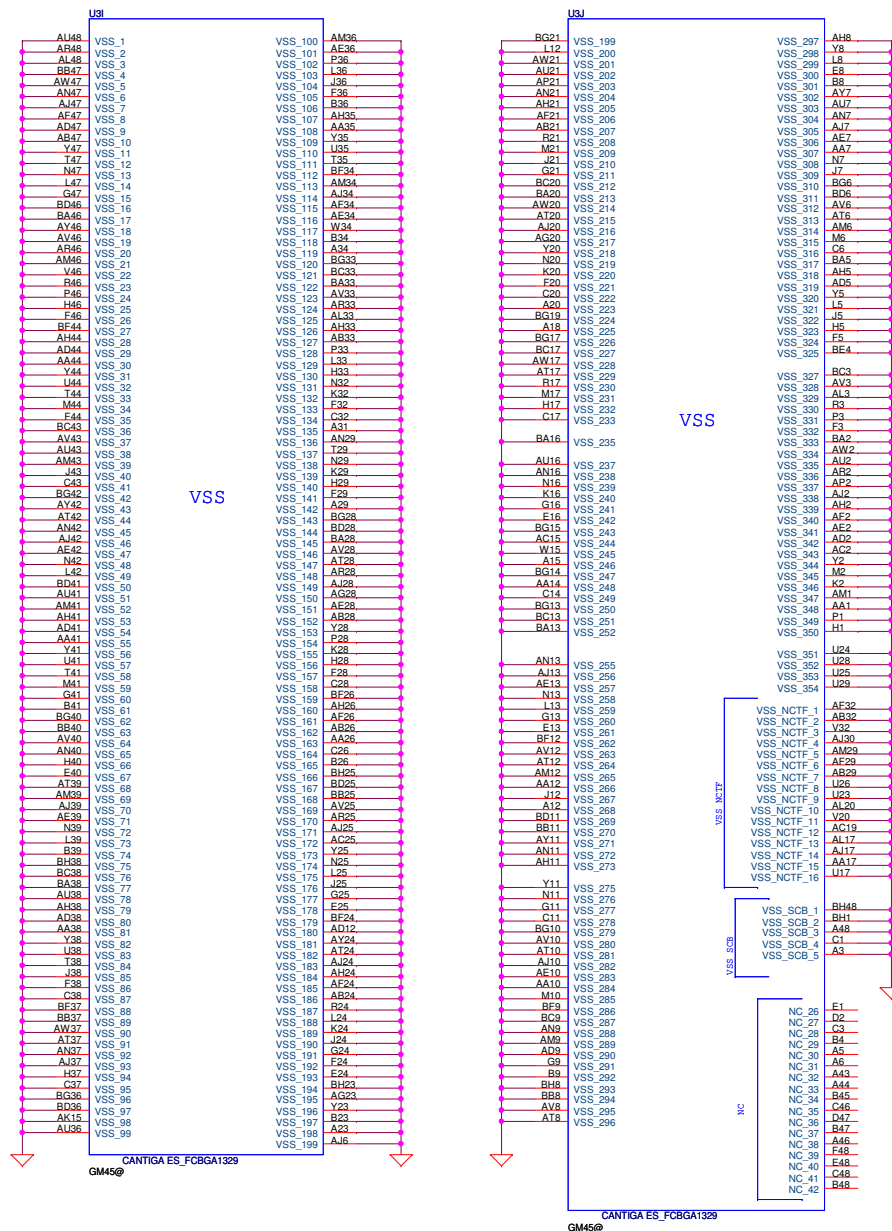


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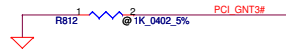
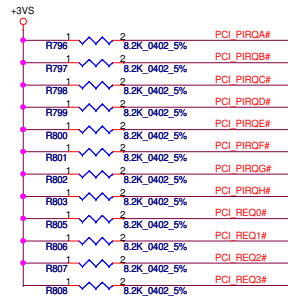
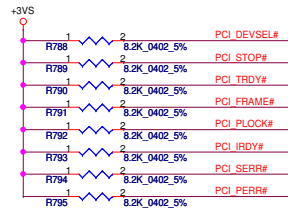




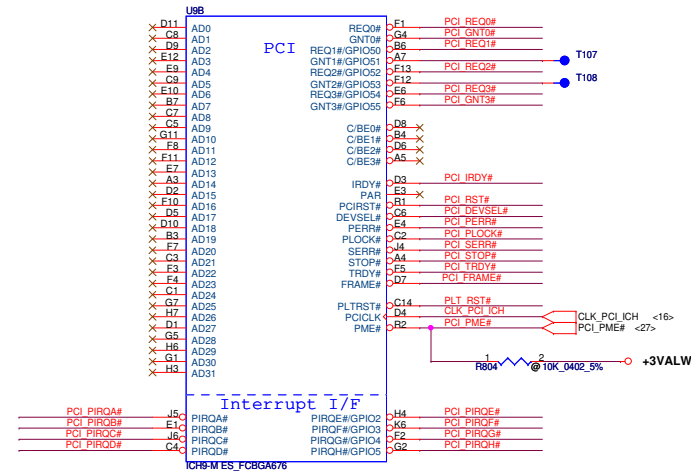






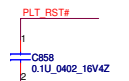


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

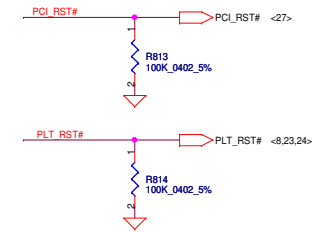
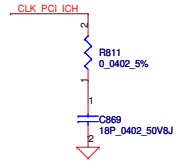


Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

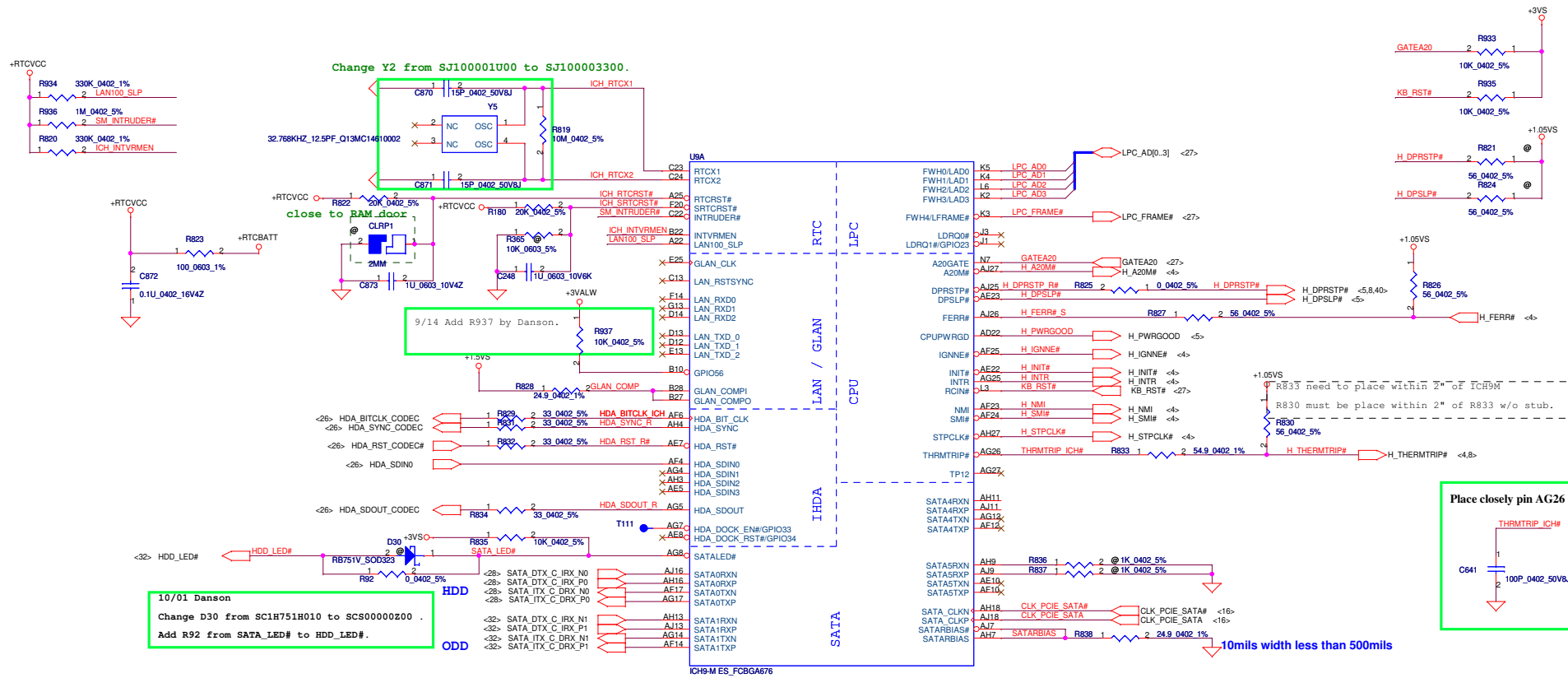
09/16 Add C858 For ESD  
Place closely pin C14



Place closely pin D4



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Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title
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Size	Custom	Document Number	LA7011P	Rev
Date	Friday, December 24, 2010	Sheet	17	of 41

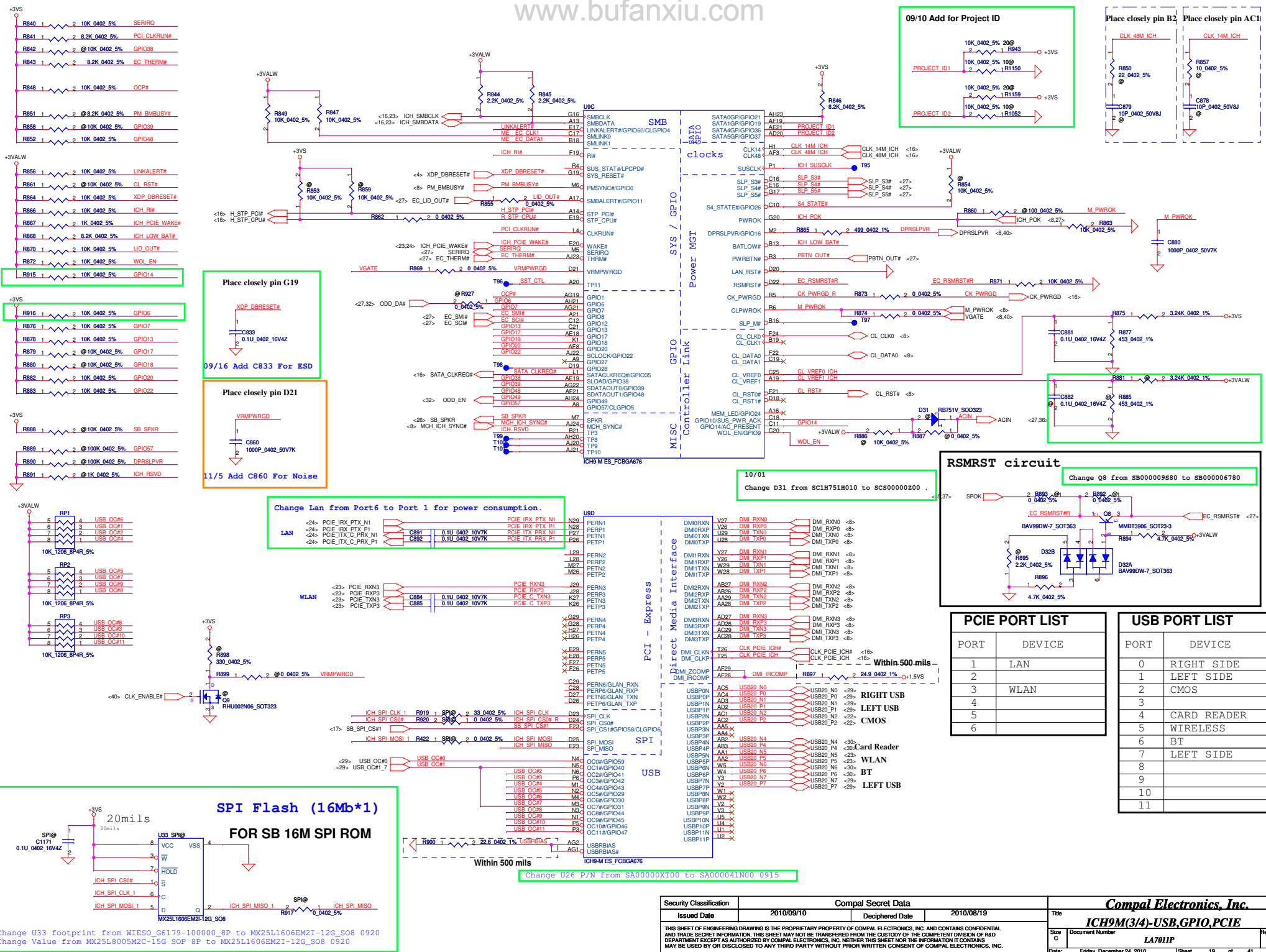


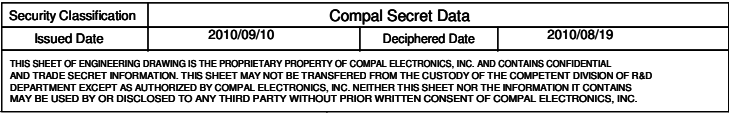
XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

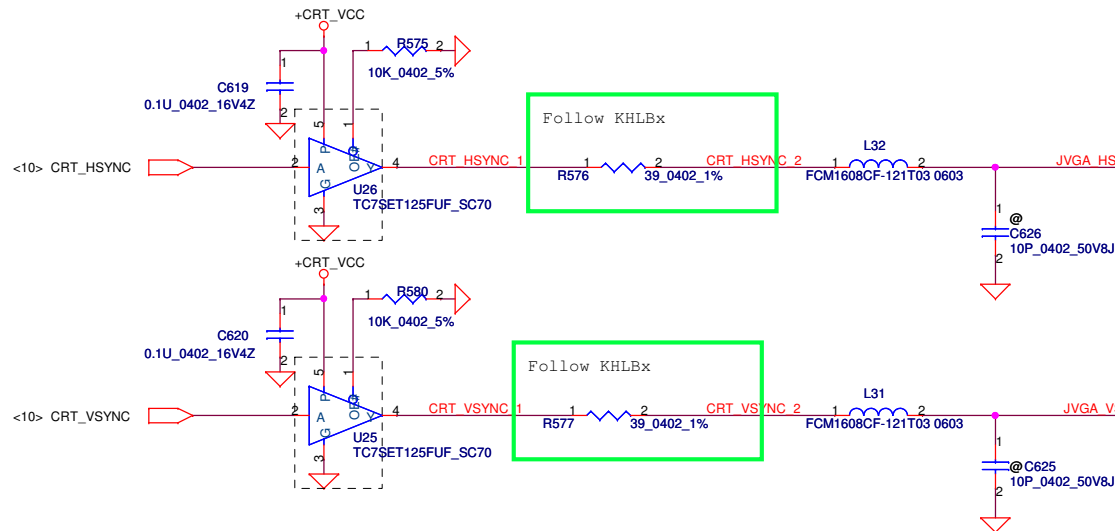
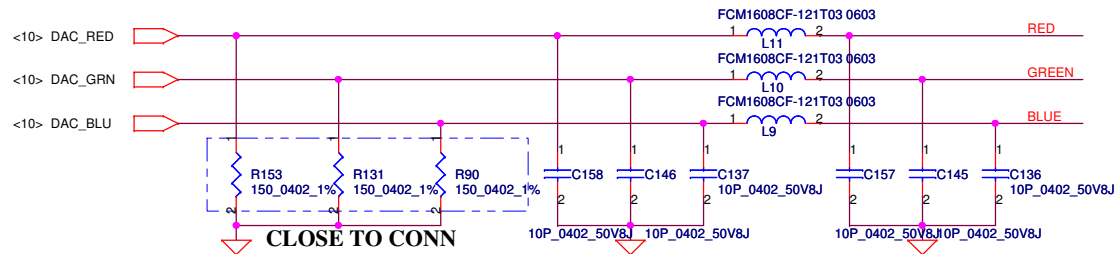
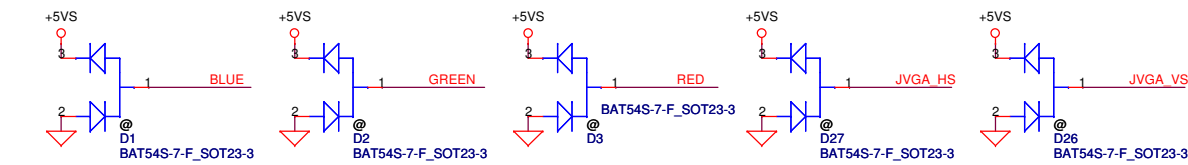
Flash Descriptor Security Override Strap	
GPIO33	Low= Descriptor Security override High= Default* (Internal pull-up)

SATA PORT LIST	
PORT	DEVICE
0	HDD
1	ODD
4	
5	

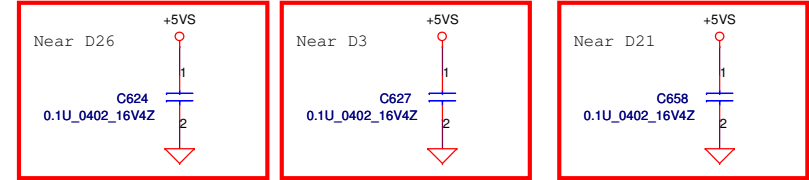
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title	ICH9M(2/4)-LAN,ATA,LPC,RTC
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				Date	Friday, December 24, 2010
				Sheet	18 of 41



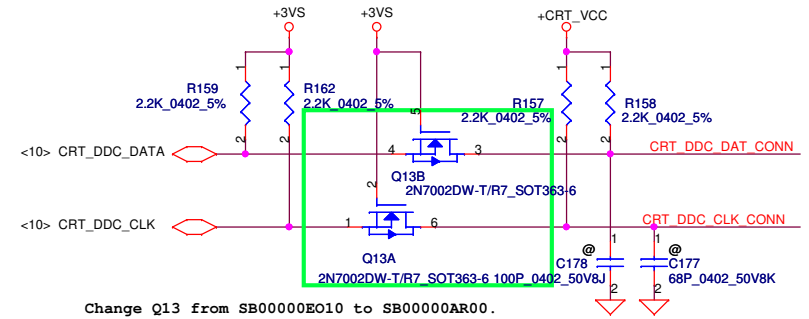
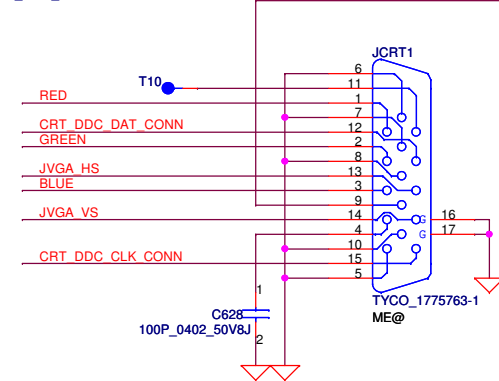
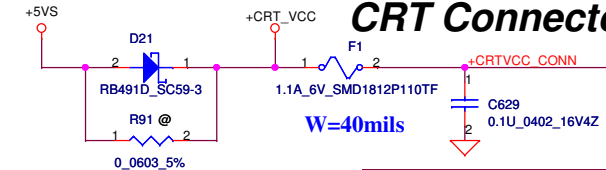




### Pre MP ADD for ESD solution

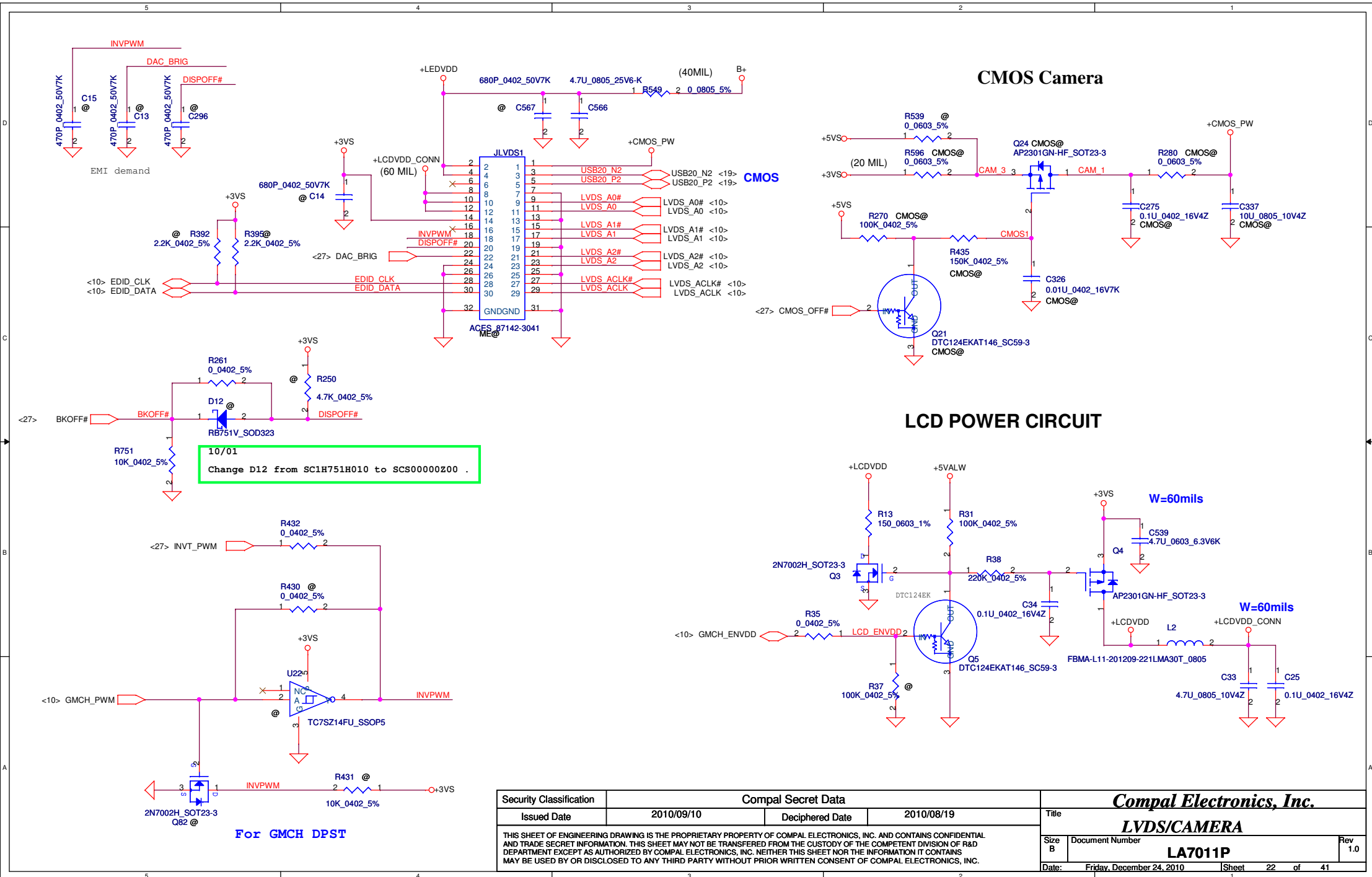


### CRT Connector

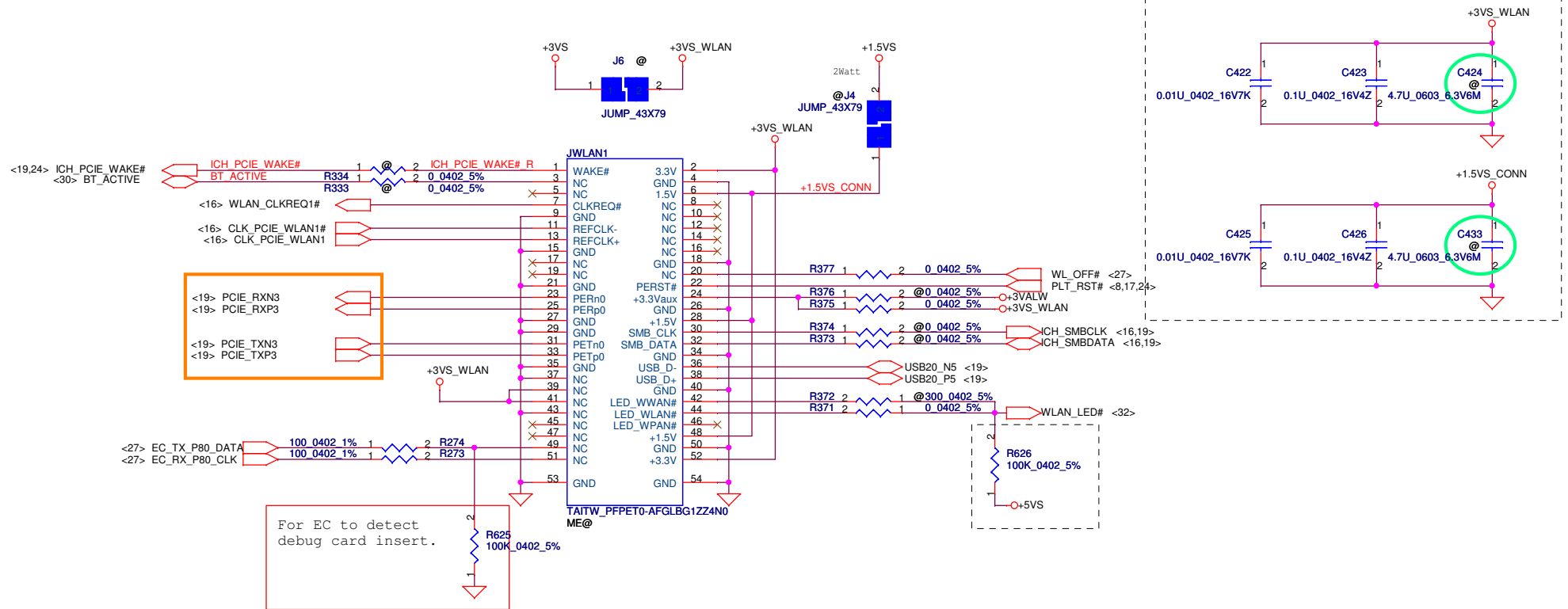


Change Q13 from SB00000EO10 to SB00000AR00.

Security Classification		Compal Secret Data		Title	
Issued Date	2010/09/10	Deciphered Date	2010/08/19	CRT Connector	
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				LA7011P	
				Date:	Friday, December 24, 2010
				Sheet	21 of 41
				Rev	1.0

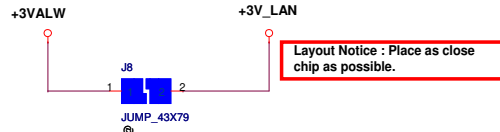


# Mini-Express Card for WLAN(Half)



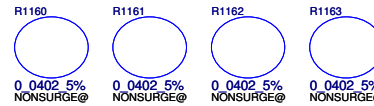
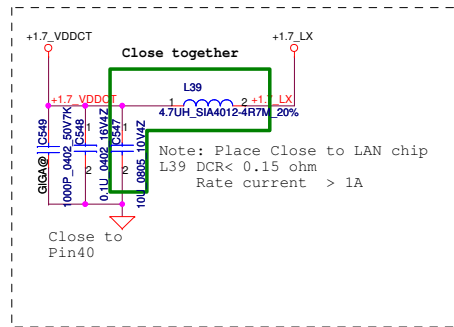
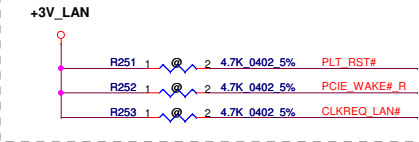
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title	
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				Size	Document Number
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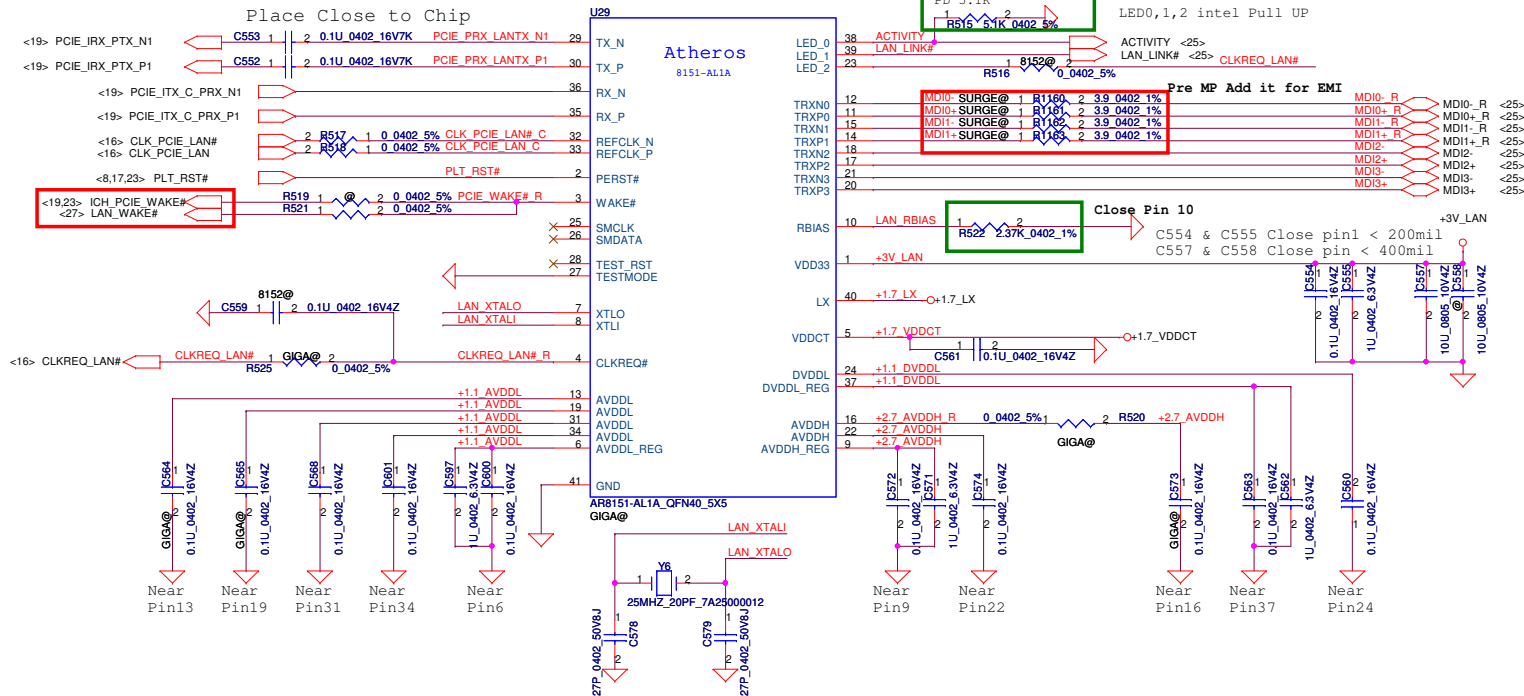


Atheros request can't disable LAN power

Atheros request reserve



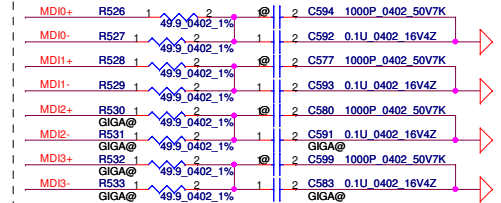
U29 8152@  
S IC AR8152-AL1E QFN 40P E-LAN CTRL



### Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
LED1	H:SWR Switch mode regulator Select AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	---

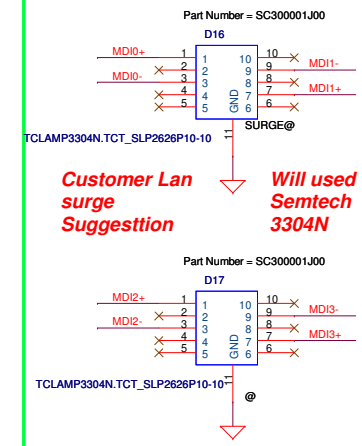
### Place Close to LAN chip



Note 1 : 8152 no mount MDI3+, MDI3-, MDI2-, MDI2+ resister and cap

Note 2 : C594, C577, C580, C599, reserved for EMI.

### 9/27 Add it for avoid to be struck by lightning



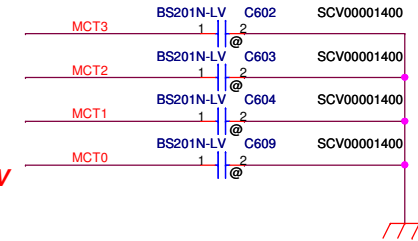
	Pin4	Configure		Pin23	Configure
AR8152	VDDCT_REG		*	CLKREQn	*
AR8151	CLKREQn	*		LED[2]	

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title
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Size	Document Number	LA7011P		Rev 1.0
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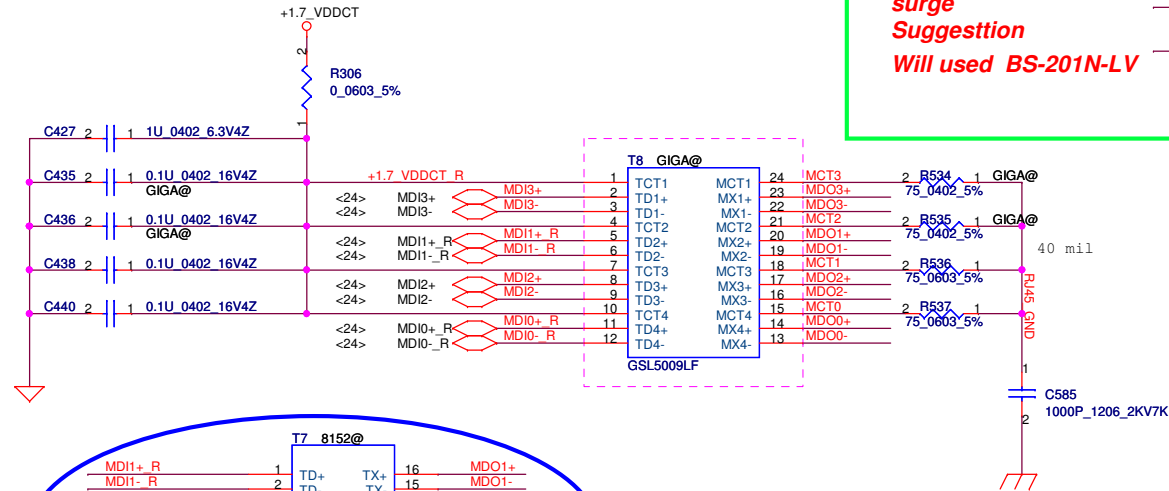
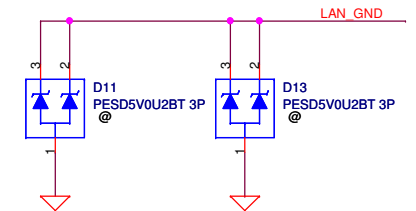


9/27 Add it for avoid to be struck by lightning

**Customer Lan surge Suggestion**  
Will used BS-201N-LV

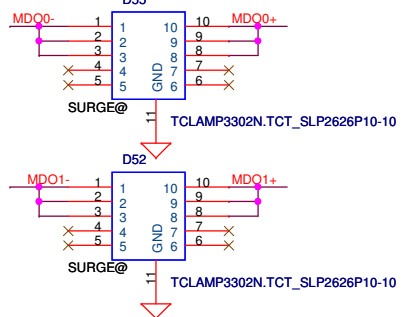


Place closely JRJ45

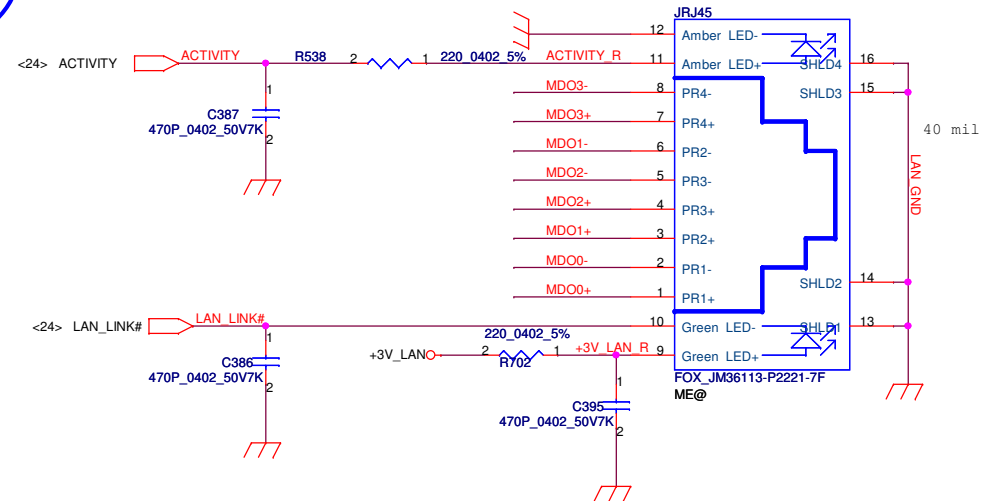
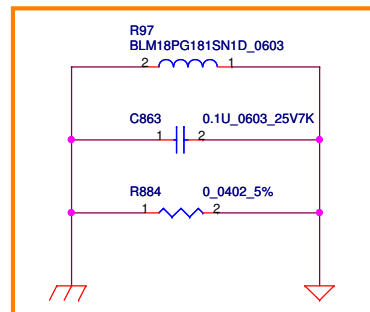


12/13 PreMP Add it for avoid to be struck by lightning

Near to near JRJ45.

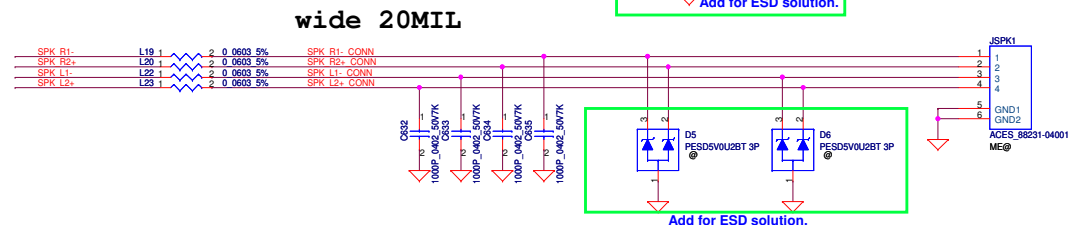
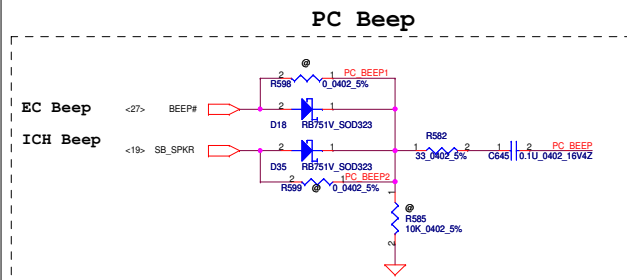
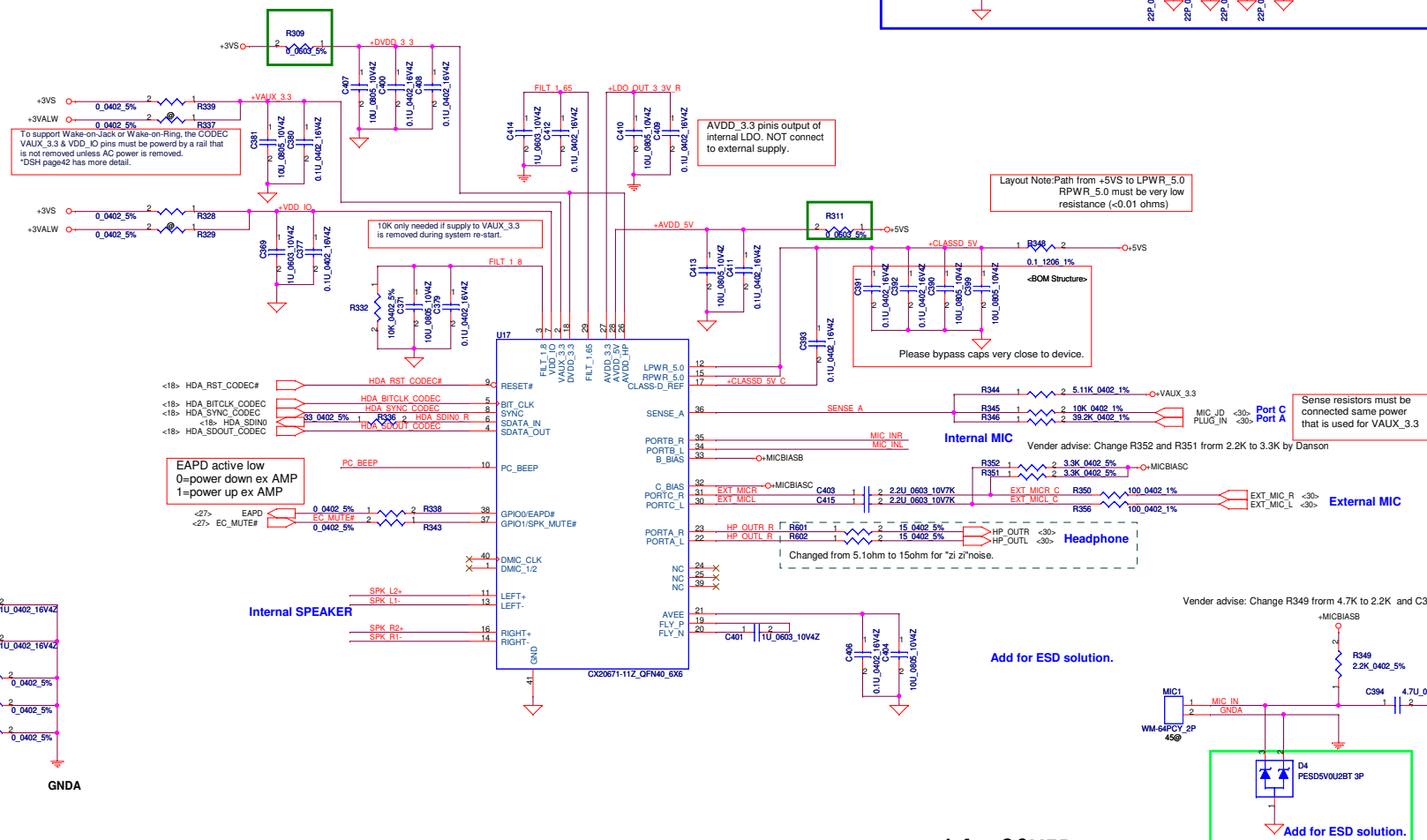


PVT Add EMI solution.

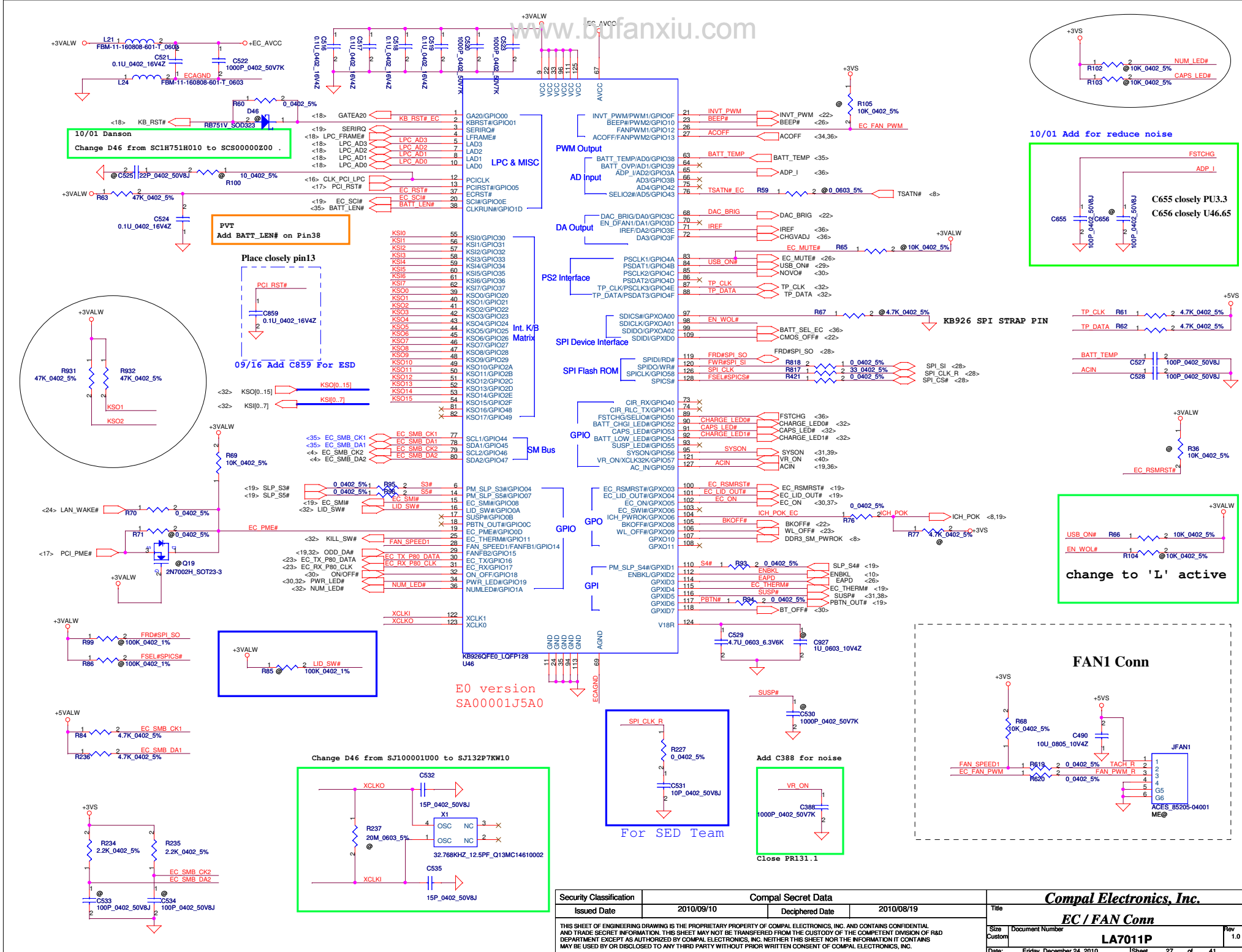


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				Size	Document Number
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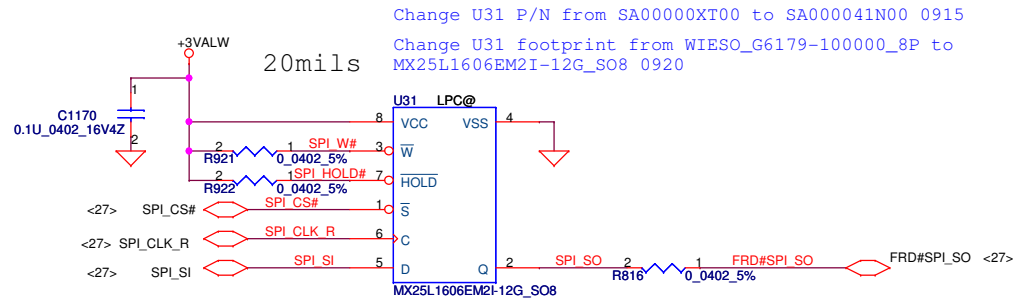


Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>	
Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title	<b>CX20671 Codec</b>
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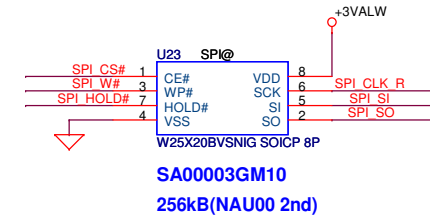
## SPI Flash (16Mb\*1)

## FOR EC 16M SPI ROM

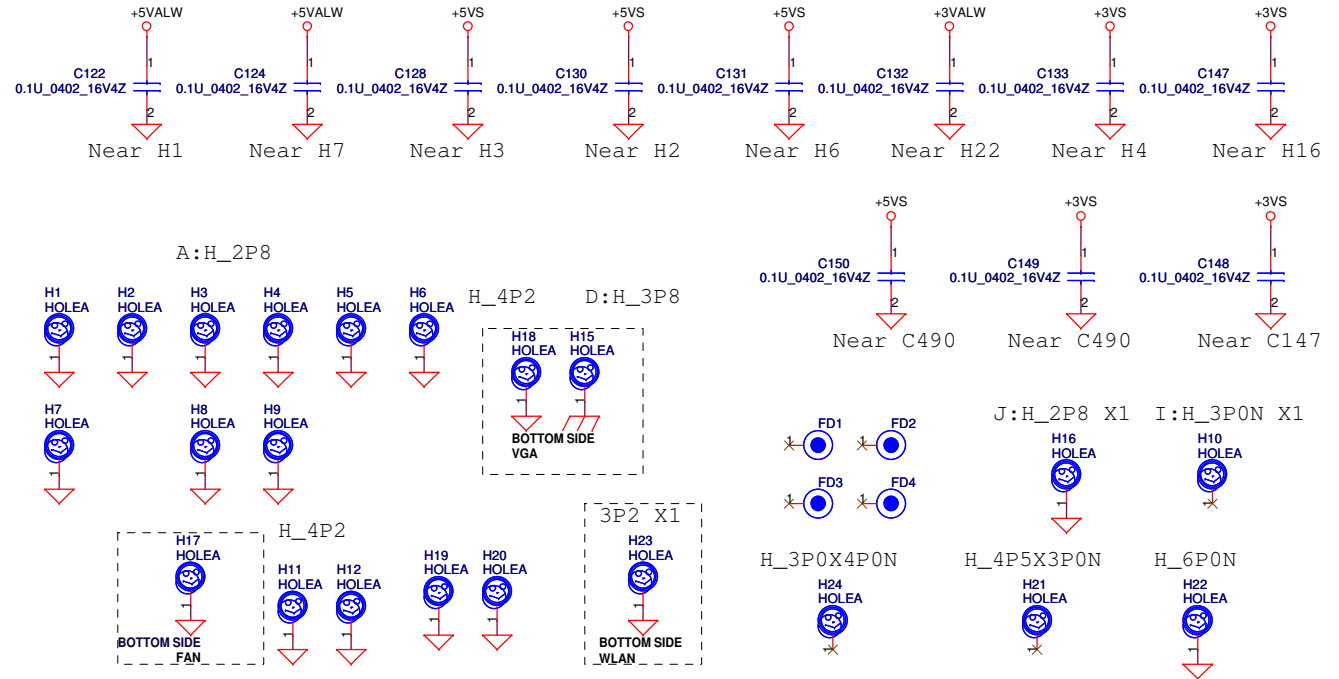
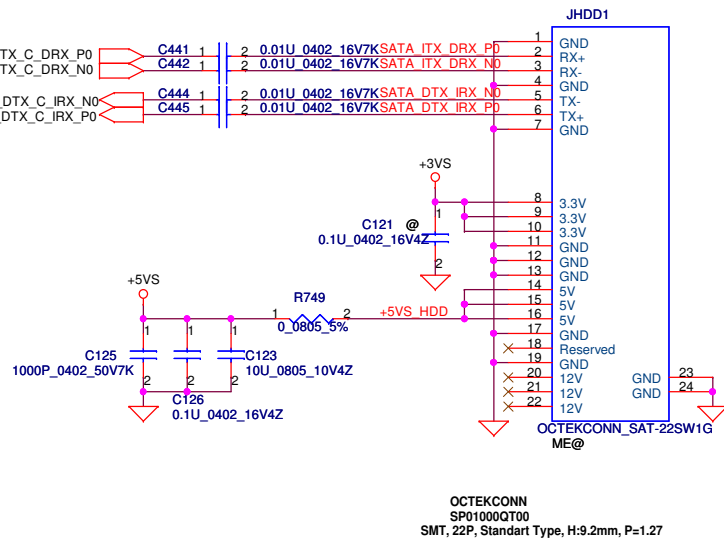


## FOR EC 256K SPI ROM (NONShare ROM)

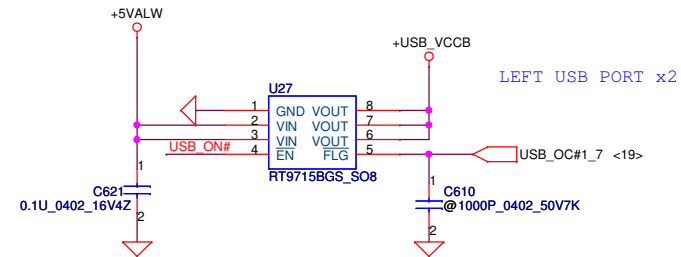
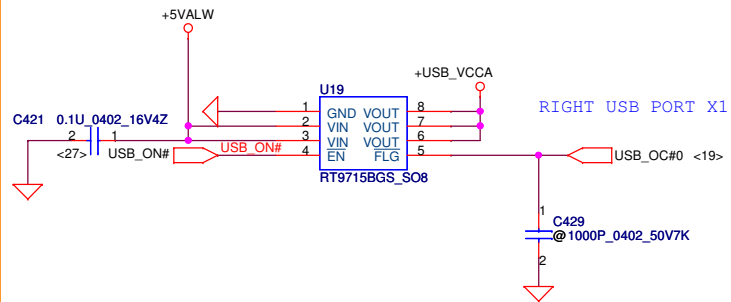
2010/09/24 Add U23 for NONShare SPI ROM.



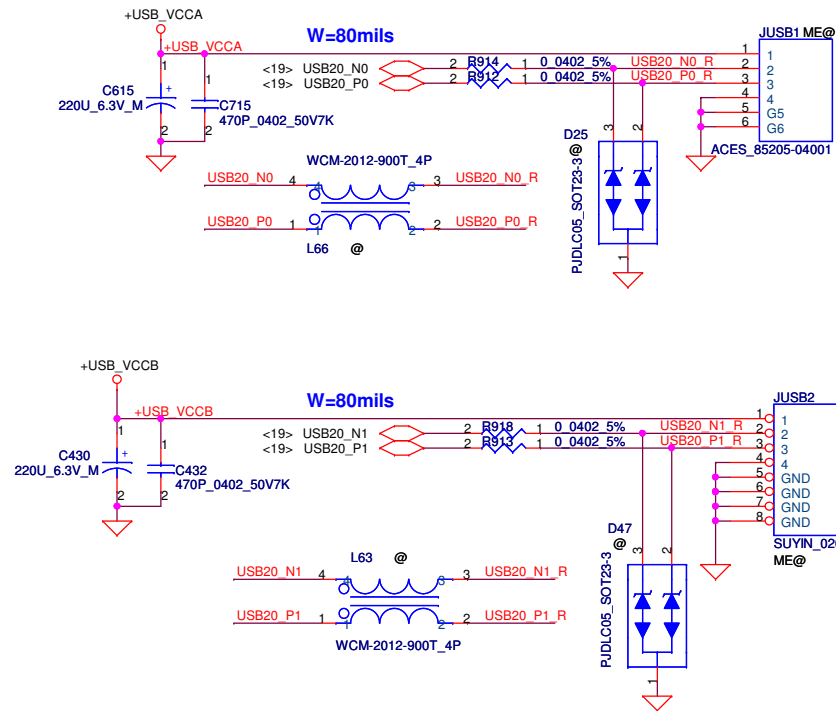
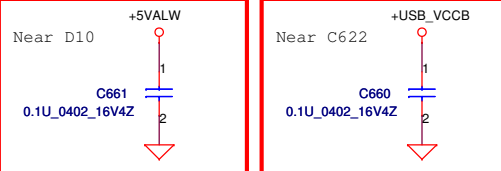
## SATA HDD Conn.



PVT Change U19 and U27 part number from SA000039E00 to SA00002XX00



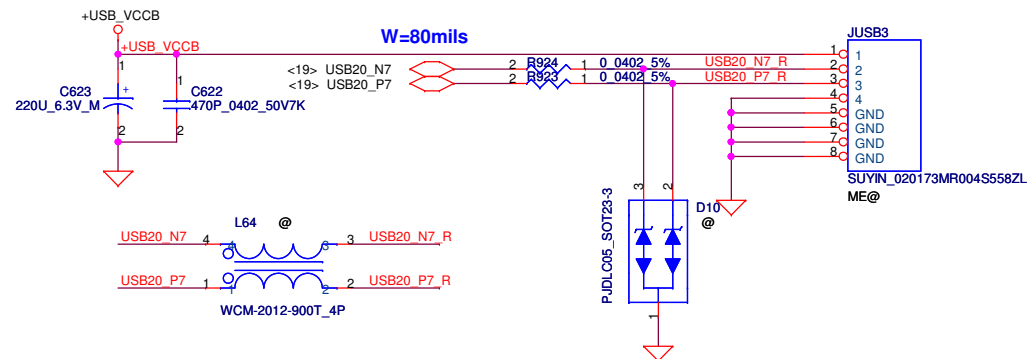
Pre MP ADD for ESD solution



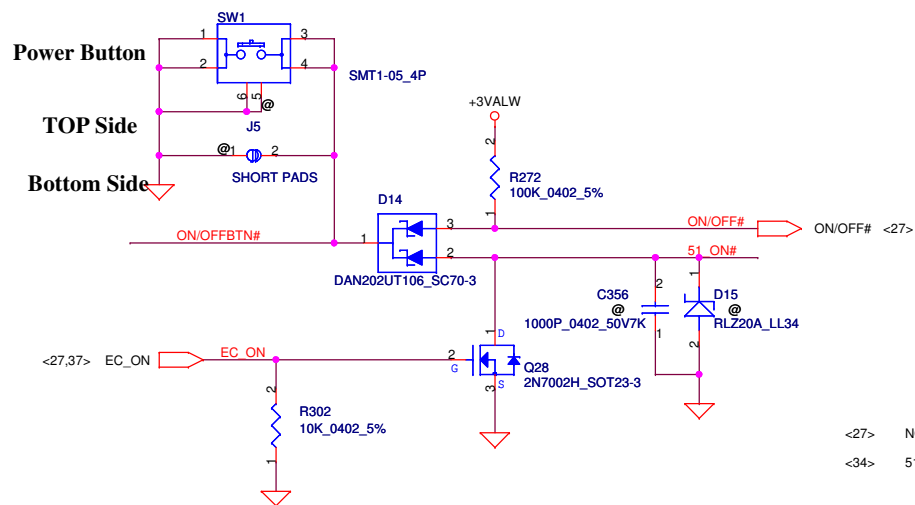
Right USB Conn.

Left USB Conn.

Change JUSB3 connector from ESATA to USB

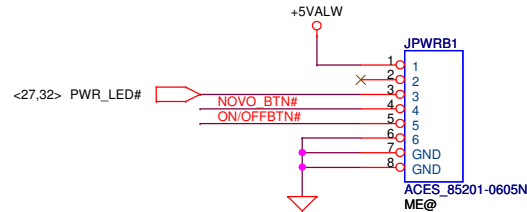


## ON/OFF switch



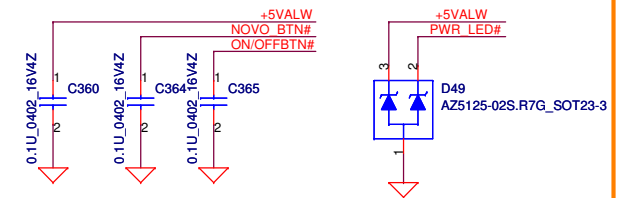
## Power Bottom Board Conn. 6pin

10/11 Change JPWRB1 P/N from SP010009010 to SP01000LB00  
Add C359 to PWR\_LED# for ESD solution.

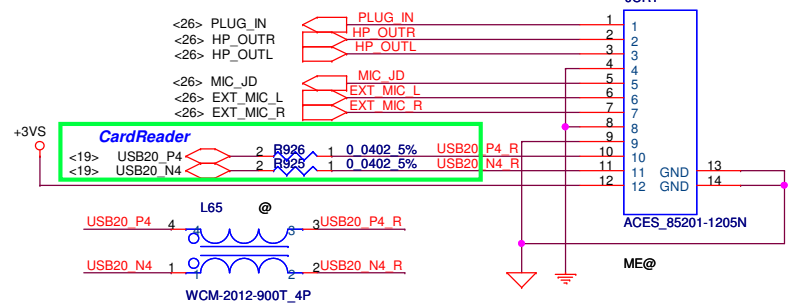


EMI REQUEST 1ST = SCA00000E00  
2ST = SCA00000R00

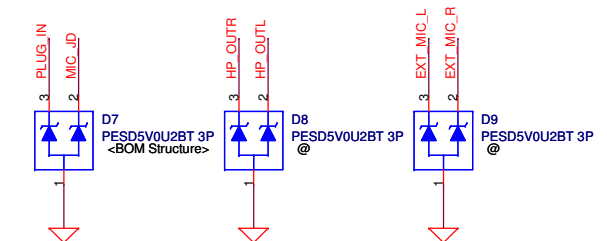
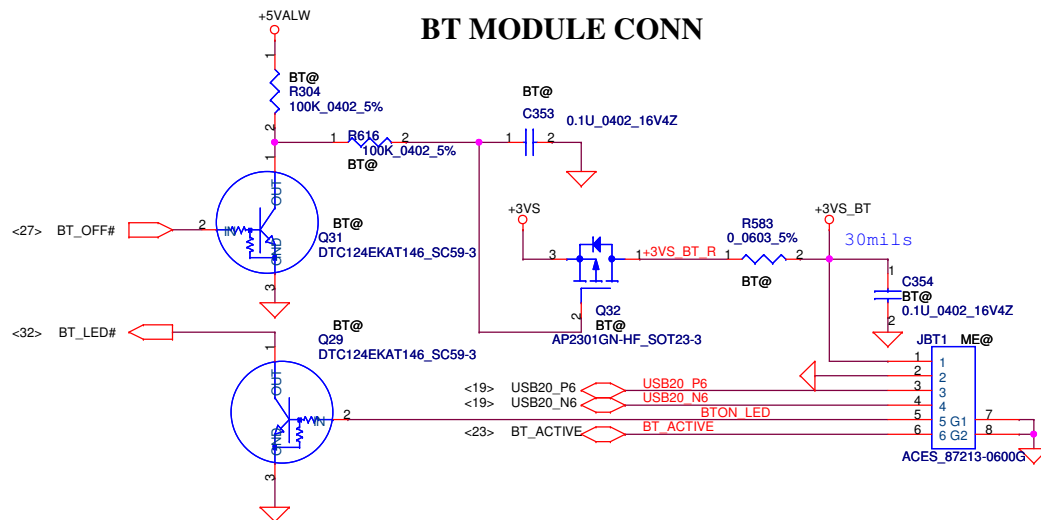
## PVT ESD solution.



## Card Reader/Audio Jack SB CONN

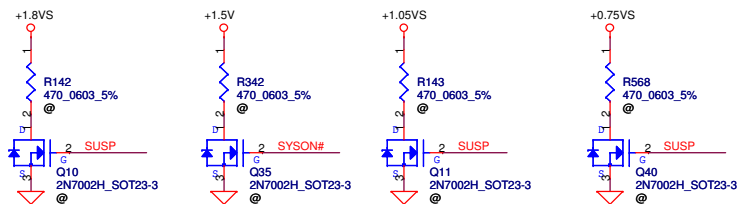
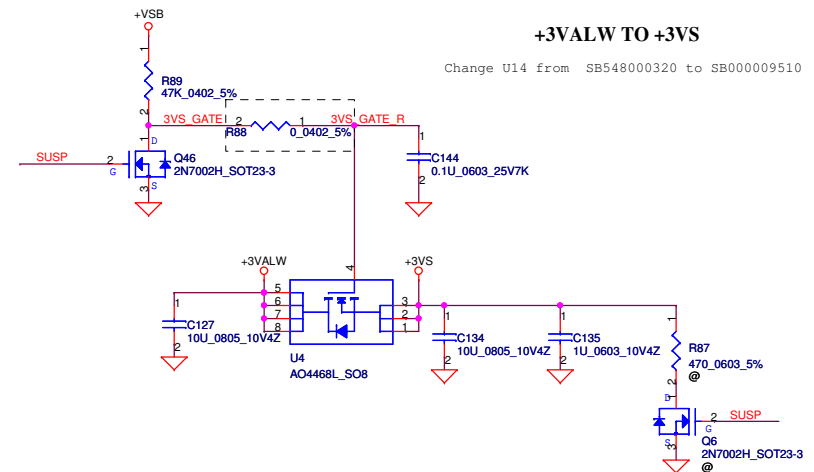
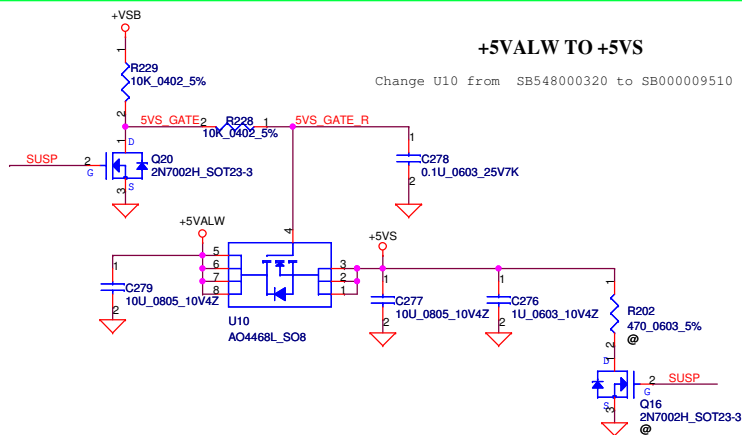


## BT MODULE CONN

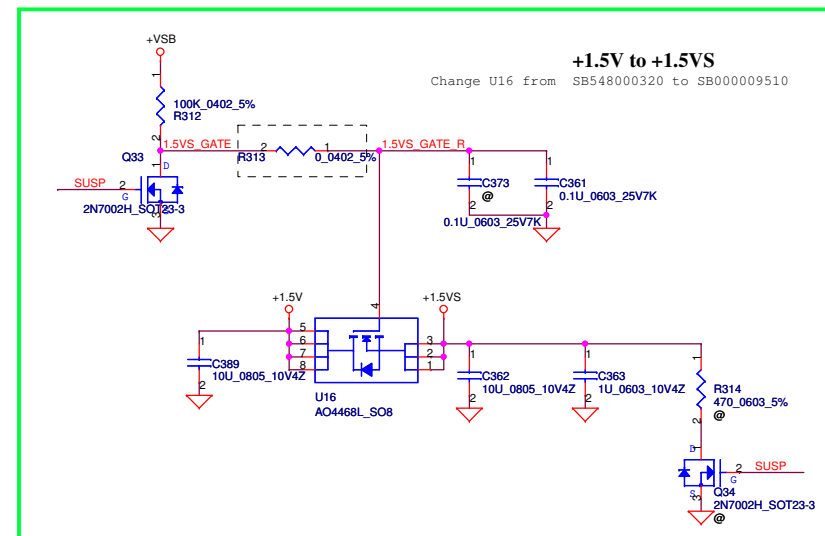
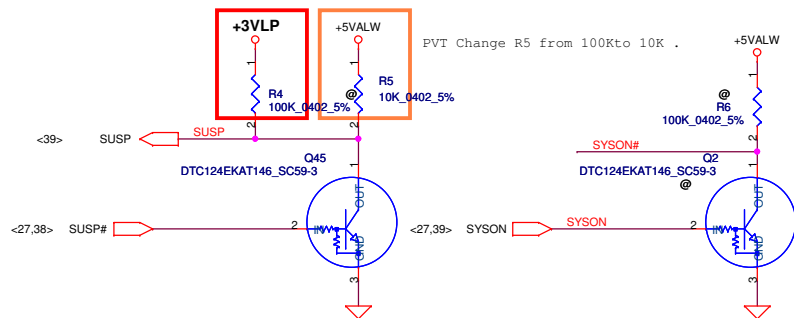


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Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title	Audio Jack & SW & BT Conn.
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A B C D E



Pre MP Change SUSP pull high from +5VALW to +3VLP



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A B C D E





## Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
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29							
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Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title HW PIR		
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1



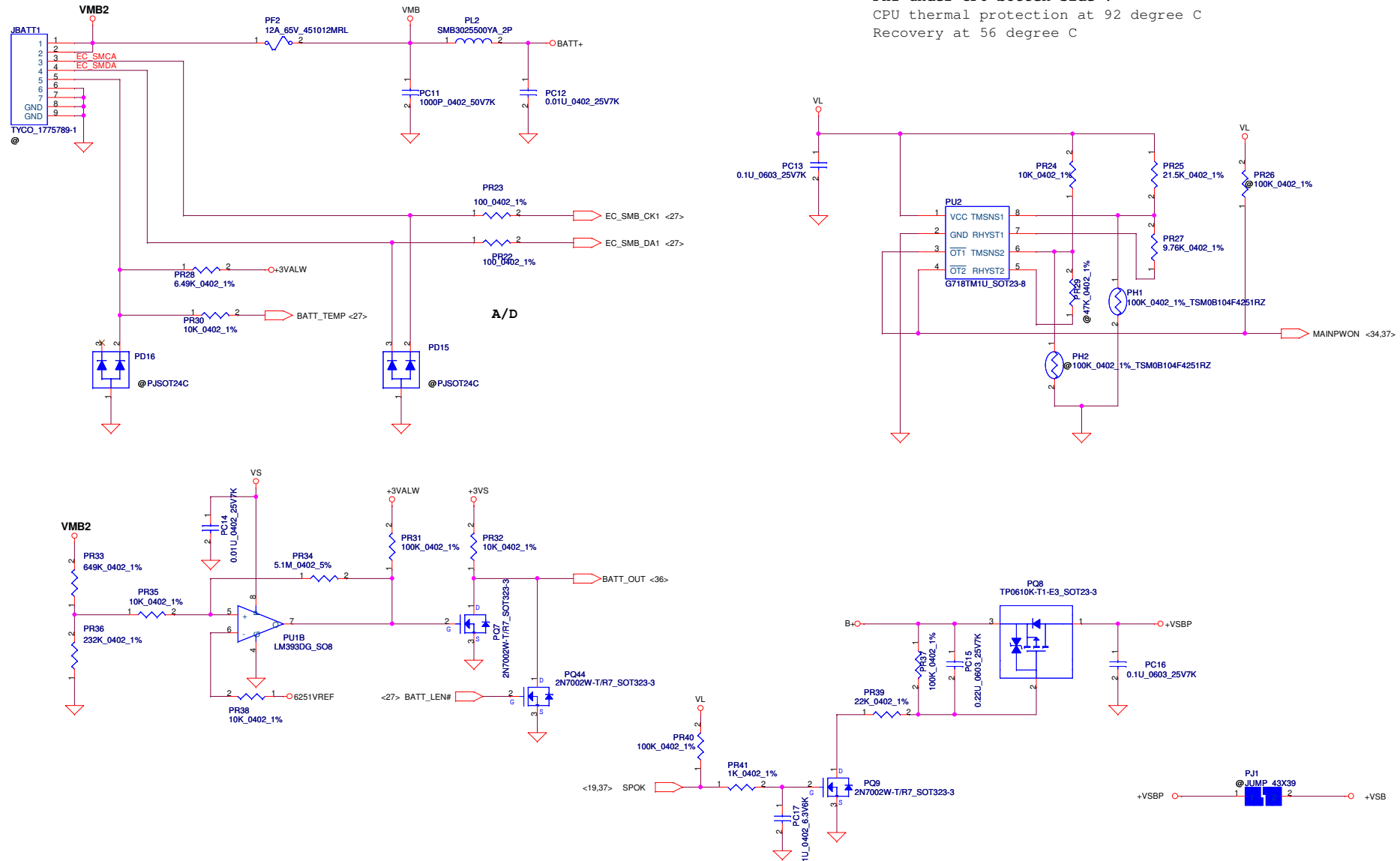
## 1

BATT ONLY			
	Precharge detector		
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

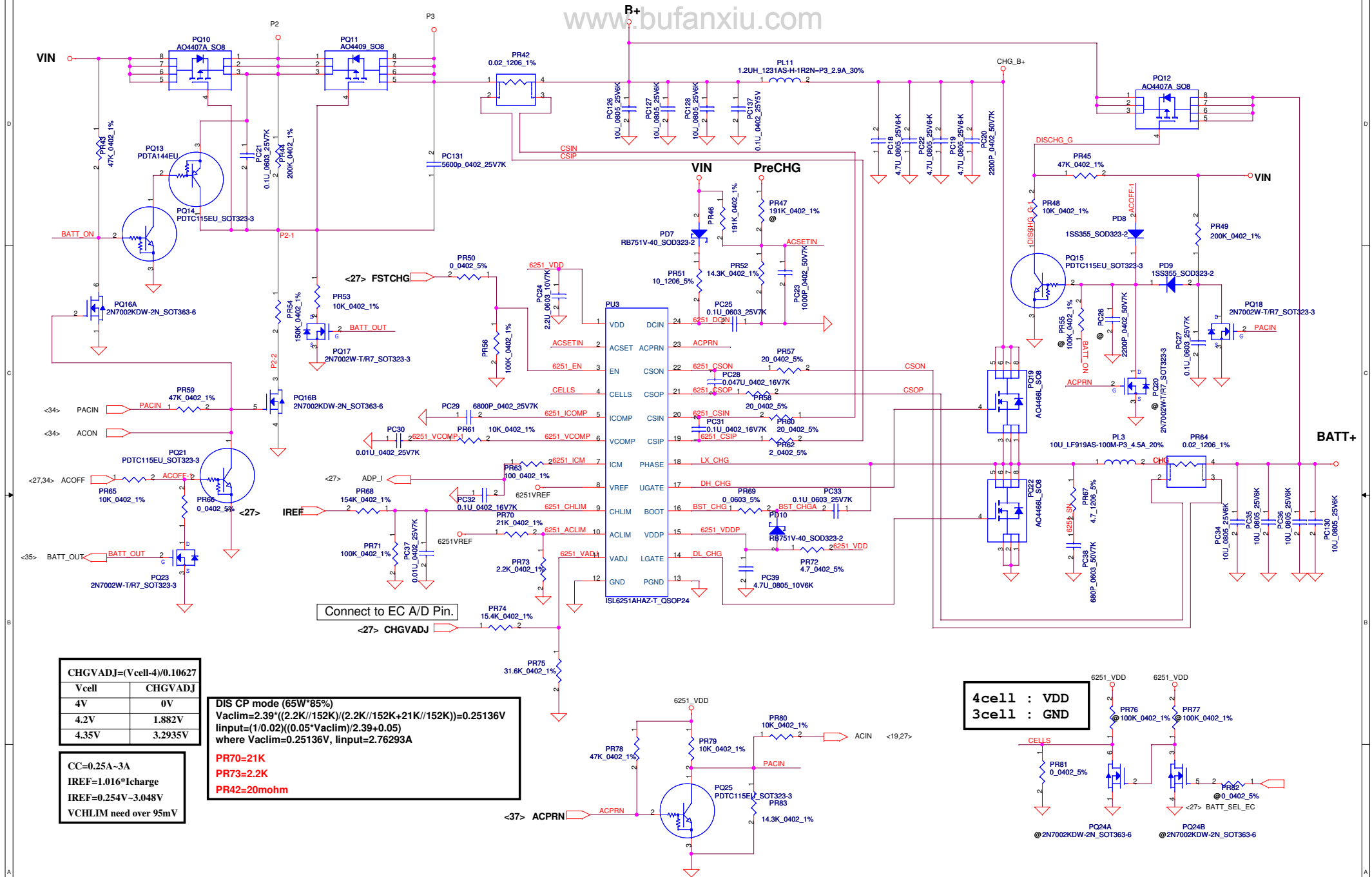
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<b><i>DCIN / Vin Detector /Pre-charge</i></b>		
<b>Size</b>	<b>Document Number</b>	<b>Rev</b>
Custom		1.0
<b>Date:</b>	<b>Editor:</b> December 24, 2010	<b>Sheet</b> 24 <b>of</b> 41

**PH1 under CPU botten side :**

CPU thermal protection at 92 degree C  
Recovery at 56 degree C

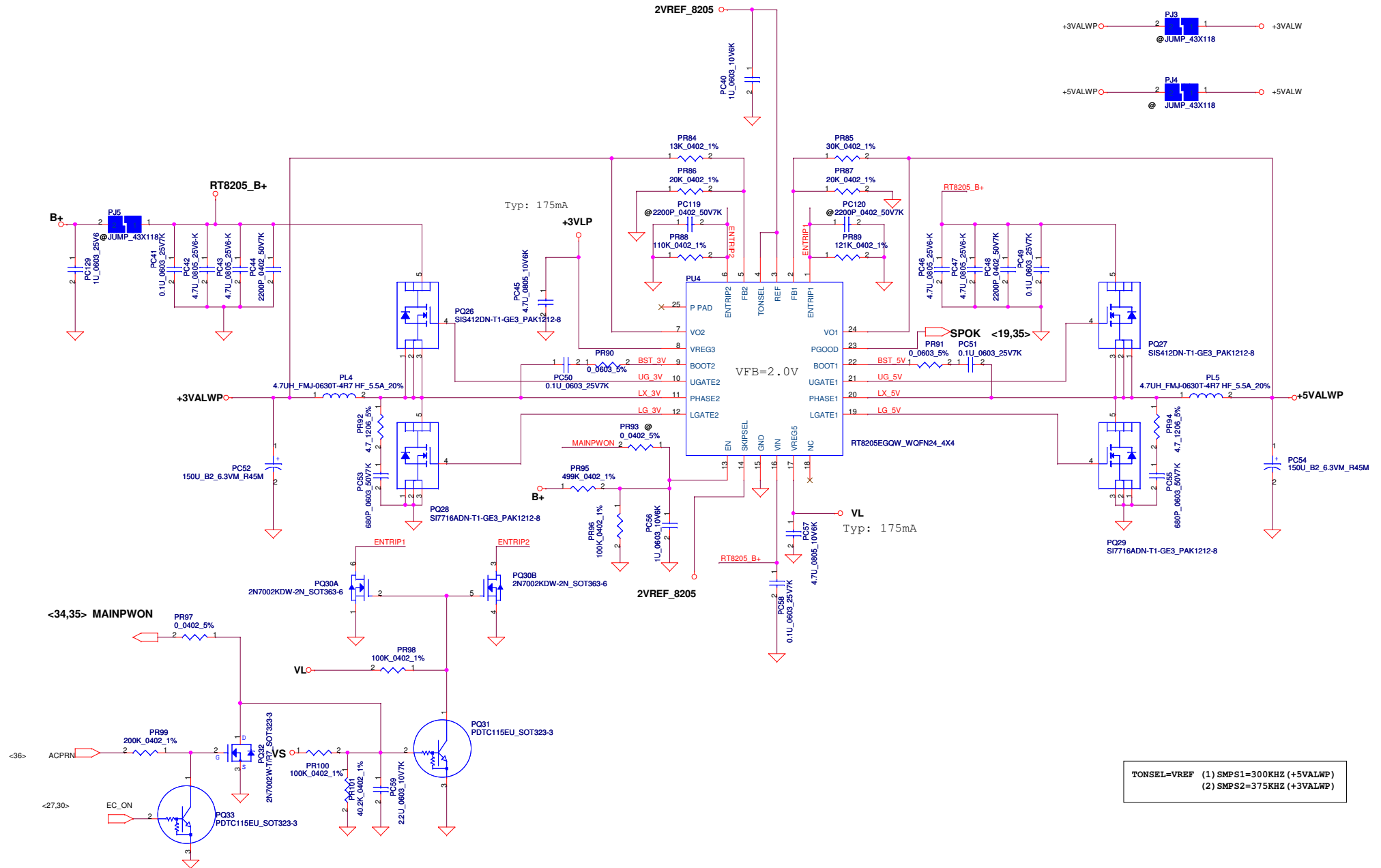


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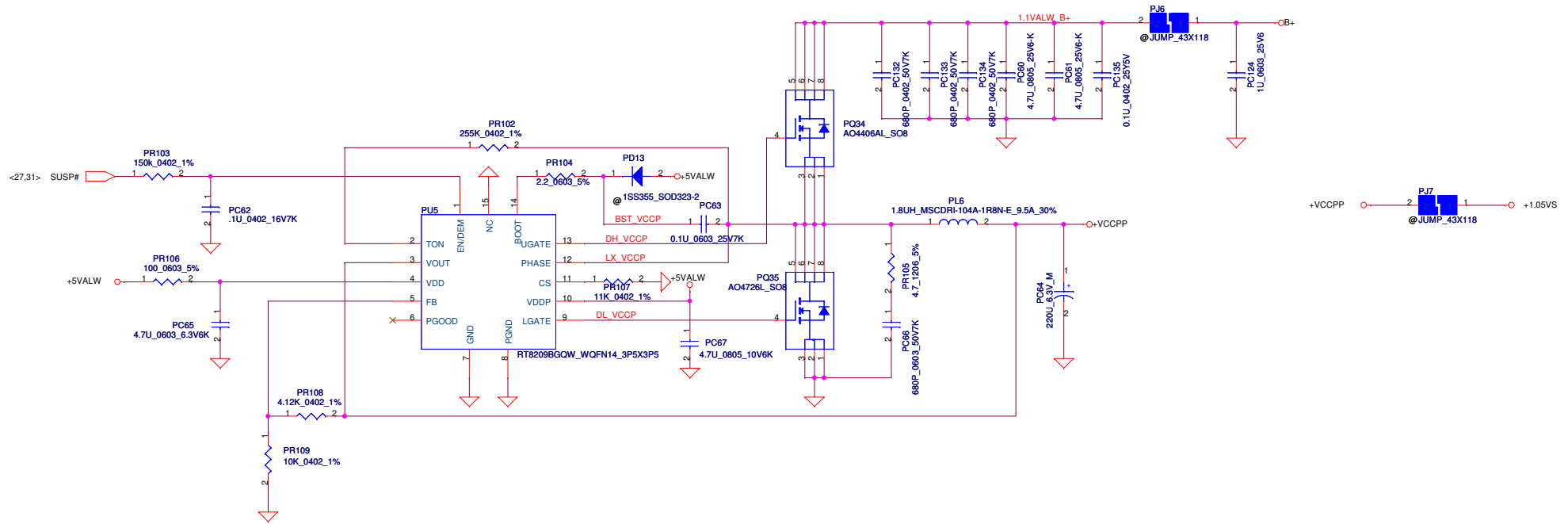


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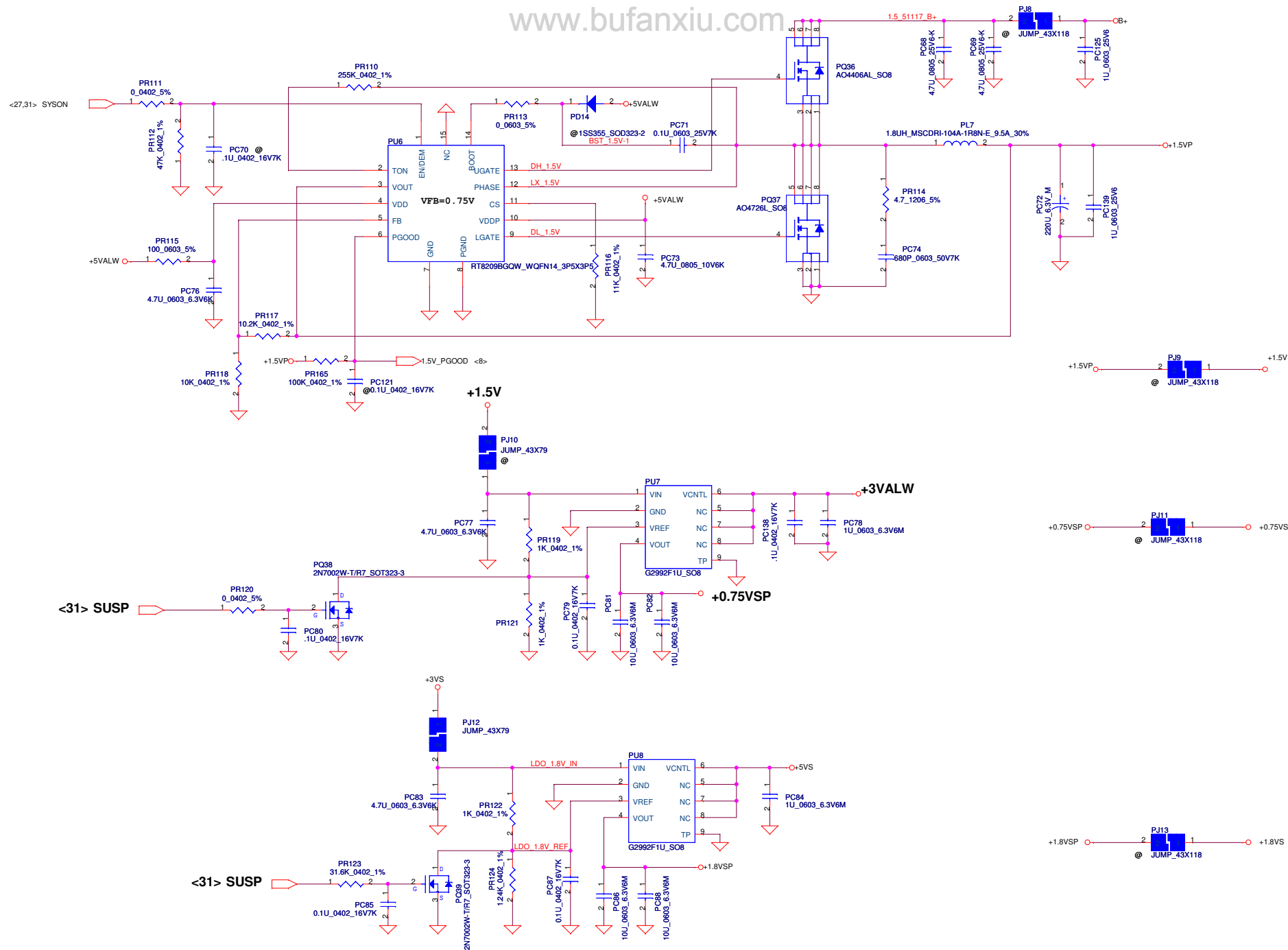
Note:  
Use TPS51125 IC can remove RTC reference LDO  
Use TPS51427 IC must keep RTC reference LDO



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# Version Change List ( P. I. R. List ) for Power Circuit

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Page#	Title	Date	Request Owner	Issue Description	Solution Description
P35,37,39	Add capacities for EMI request	2010.11.12	EMI	EMI test fail	Add PC132,PC133,PC134,PC135,PC136,PC137
P37	Change resistance for EMI request	2010.11.12	EMI	EMI test fail	Change PR104 from 0 ohm to 2.2ohm
P35	Add one capacitor for prevent inrush current too large	2010.11.12	PWR	If there isn't add capacity, the MOS of PQ11 have damaged risk.	Add PC131 which value is 5600PF
P34	Add one transistor for improve design margin	2010.11.12	PWR	If there isn't add transistor, the design margin of PQ11 is not enough.	Add PQ44
P39	Change resistance for CPU loadline fine tuning	2010.11.12	PWR	For meet the load line of intel spec	Change PR138 from 4.3k to 4.75k
P35	Add one capacitor for improve ripple current	2010.11.12	PWR	For meet the ripple current spec of Compal	Add PC130

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