LE8(K43) BLOCK DIAGRAM

01

PCB STACK UP
8L

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

CPU CORE(ISL6266A) PAGE 43

CPU Penryn
478P (uPGA)/35W
PAGE 4,5

CPU THERMAL SENSOR PAGE 5

FSB 667/800/1066

14.318MHz

CLOCK GEN
ICS9LPRS365BGLFT
PAGE 3

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

VCCP +1.5V AND GMCH 1.05V(RT8204) PAGE 41

VGACORE(OZ8118) PAGE 44

NORTH BRIDGE
Cantiga
PAGE 6~10

27MHz

NVIDIA NB9M-NS
PAGE 13~18

DDRIII-SODIMM1 PAGE 11
DDRII 800/1066 MHz

DDRIII-SODIMM2 PAGE 12
DDRII 800/1066 MHz

DDR III (TPS51116REGR)
1.5VSUS/SMDDR_VTERM
/SMDDR_VREF PAGE 39

PCI-Express 16X

CRT PAGE 23

LCD CONN PAGE 24

DMI LINK

32.768KHz

NBSRCCLK, NBSRCCLK#

SOUTH BRIDGE
ICH-9M
PAGE 19,20,21,22

USB2.0

USB2.0 Ports X2

USB+eSATA Port X1 PAGE 30

BlueTooth PAGE 33

Finger Printer CONN PAGE 33

SATA - HDD PAGE 30
SATA0 150MB

SATA - CD-ROM PAGE 30
SATA1 150MB

PCI

PCI-E

24.576Hz

Azalia

X2 Mini PCI-E Card X 2 (WLAN/ WWAN) PAGE 35

X1 LAN BROADCOM BCM 5906M/5784 (10/100/1G LAN) PAGE 31,32

X1 Express Card (NEW CARD) PAGE 33

X1 RICOH R5C847 PAGE25,26

SYSTEM POWER(ISL6237) PAGE 42

SYSTEM CHARGER(ISL6251A) PAGE 38

32.768KHz

LPC

AUDIO CODEC
CX20561-12Z
PAGE 28

MDC CONN PAGE 28

RJ11 PAGE 32

AUDIO Amplifier TPA6017A2 PAGE 29

RJ45 PAGE 32

25MHz

PCMCIA CONN PAGE 26

IEEE1394 on Daughter B PAGE 25

CardReader PAGE 26

Keyboard Touch Pad PAGE 34

TPM PAGE 34

SIO CONN PAGE 27

NS
ITE 8502E-L
PAGE 36

microphone PAGE 28

Audio Jacks (External MIC) PAGE 29

Head-Phone Jack PAGE 29

FAN PAGE 34

SPI PAGE 36

PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

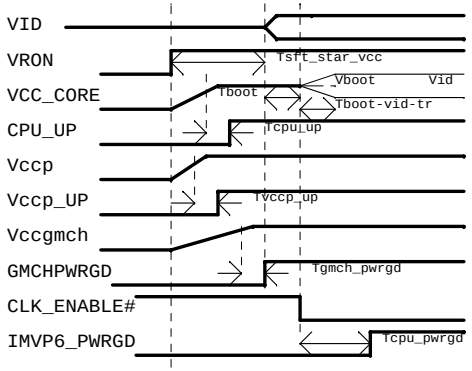
Date: Thursday, June 12, 2008 Sheet 1 of 45

Board Stack up Description

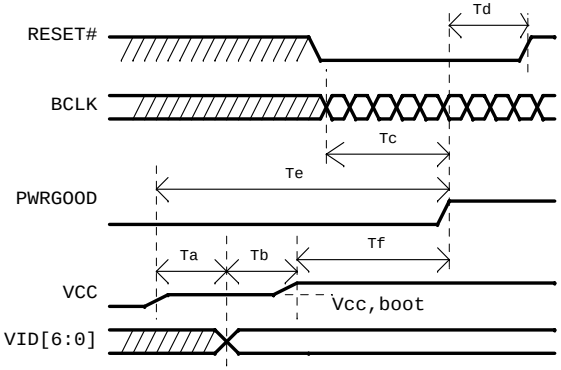
PCB Layers

Layer 1		TOP
Layer 2		GND
Layer 3		IN1
Layer 4		IN2
Layer 5		SVCC
Layer 6		IN3
Layer 7		GND
Layer 8		BOTTOM

Power On Sequencing Timing Diagram



MEROM Power-up Timing Specifications

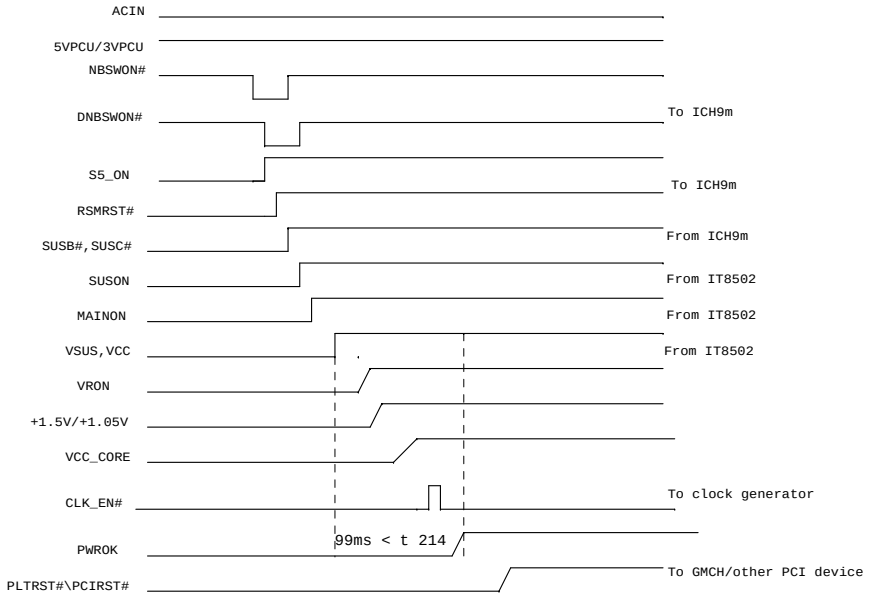


Ta=VCC and VCCP asseration to VID[6:0] vaild
Tb=VID[6:0] stable to VCC vaild
Tc=BCLK stable to PWRGOOD assertion
Td=PWRGOOD to RESET# de-assertion time
Te=Vcc,boot vaild to PWRGOOD assertion time

Voltage Rails

Voltage Rails	ON S0~S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	X				VRON
+1.5V	X				MAINON
+1.05V	X				MAINON
5V_S5/3V_S5	X	X	X	X	S5_ON
5VSUS/3VSUS/1.5VSUS	X	X			SUSON
SMDDR_VTERM/+3V/+5V/+15V/+1.8V	X				MAINON
+VGACORE/+VGA1.1V	X				MAINON
LANVCC	X	X	X	X	LAN_ON
3VPCU	X	X	X	X	VL
5VPCU	X	X	X	X	VL

ACIN POWER ON TIMING



PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SYSTEM INFORMATION	1A

Date: Thursday, June 12, 2008 Sheet 2 of 45

+3V
L23 HI0805R800R-00
+CK_VDD_MAIN
C370 10U/6.3V_8
C388 .1U/10V/04
C355 .1U/10V/04
C387 .1U/10V/04
C347 .1U/10V/04
C345 .1U/10V/04
L26 HI0805R800R-00
VDDCPU
C381 10U/6.3V_8
C385 .1U/10V/04
L20 HI0805R800R-00
+CK_VDD_MAIN2
C354 10U/6.3V_8
C384 .1U/10V/04
C386 .1U/10V/04
C383 .1U/10V/04
C343 .1U/10V/04
C344 .1U/10V/04
C346 .1U/10V/04

+3V
R193 10K/04
PCLK_MINI_LPC
R192 *4.7K/04
0=overclocking of CPU and SRC Allowed
1 = overclocking of CPU and SRC not Allowed

+3V
R178 10K/04@EV
FCTSEL1
R191 *10K/04@IV
0=UMA
1 = External VGA

Disable ITP
10K/04 R190
ITP_EN

+3V
Q12 2N7002
R207 10K
R209 10K
21,31,33 PDAT_SMB
CGDAT_SMB
+3V
Q11 2N7002
21,31,33 PCLK_SMB
CGCLK_SMB

Y3
CG_XIN
CG_XOUT
14.318MHZ+/- 10ppm
C372 27P/50V/NPO_4
C369 27P/50V/NPO_4

+3V
CLK_MCH_OE# R188 10K/04
NEW-CARD_CLK_REQ# R222 10K/04
PCIE_LANREQ# R177 10K/04

RP11 4P2R-S-33@EV
R_DREFSSCLK
R_DREFSSCLK#
27M_NONSS 15
27M_SS 15

U8
CK505
+CK_VDD_MAIN
VDDCPU
+CK_VDD_MAIN2
VDDPLL3
VDD48
VDDPCI
VDDREF
VDDSRC
VDDCPU
VDD96I/O
VDDPLL3I/O
VDDSRCI/O
VDDSRCI/O
VDDSRCI/O
VDDCPU_IO
NC
CG_XIN
CG_XOUT
X1
X2
21 CK_PWG
CLK_BSEL1
FSB
CK_PWRGD/PD#
FSLB/TEST_MODE
CGCLK_SMB
CGDAT_SMB
SCLK
SDATA
GND
GND
GND48
GNDCPU
GNDPCI
GNDREF
GNDSRC
GNDSRC
GNDSRC
ICS9LPRS365BGLFT/SLG8SP512T

CPUCLKT0 CPUCLKC0 — CLK_CPU_BCLK / CLK_CPU_BCLK# → CLK_CPU_BCLK 4 / CLK_CPU_BCLK# 4
CPUCLKT1 CPUCLKC1 — CLK_MCH_BCLK / CLK_MCH_BCLK# → CLK_MCH_BCLK 6 / CLK_MCH_BCLK# 6
CPUT2_ITP/SRCT8 CPUT2_ITP/SRCC8 — CPU_ITP / CPU_ITP# → CLK_PCIE_MINI_C 35 / CLK_PCIE_MINI_C# 35
DOTT_96/SRCT0 DOTC_96/SRCC0 — R_DOT96 / R_DOT96# — RP14 *4P2R-S-0@IV → DREFCLK 7 / DREFCLK# 7
27MHz_Nonss/SRCCLK1/SE1 27Mhz_ss/SRCCLC1/SE2 — R_DREFSSCLK / R_DREFSSCLK# — RP13 *4P2R-S-0@IV → DREFSSCLK 7 / DREFSSCLK# 7
SRCCLKT2/SATACL SRCCLKC2/SATACL — CLK_PCIE_SATA / CLK_PCIE_SATA# → CLK_PCIE_SATA 19 / CLK_PCIE_SATA# 19
SRCCLKT3/CR#_C SRCCLKC3/CR#_D — R_CLK_PCIE_VGA / R_CLK_PCIE_VGA# — RP17 4P2R-S-0@EV → CLK_PCIE_VGA 13 / CLK_PCIE_VGA# 13
SRCCLKT4 SRCCLKC4 — CLK_PCIE_LAN / CLK_PCIE_LAN# → CLK_PCIE_LAN 31 / CLK_PCIE_LAN# 31
PCI_STOP# CPU_STOP# — PM_STPPCI# / PM_STPCPU# → PM_STPPCI# 21 / PM_STPCPU# 21
SRCCLKT6 SRCCLKC6 — CLK_PCIE_ICH / CLK_PCIE_ICH# → CLK_PCIE_ICH 20 / CLK_PCIE_ICH# 20
SRCCLKT7/CR#_F SRCCLKC7/CR#_E — CLK_PCIE_MINI / CLK_PCIE_MINI# → CLK_PCIE_MINI 35 / CLK_PCIE_MINI# 35
SRCCLKT9 SRCCLKC9 — RSRC_MCH / RSRC_MCH# — RP15 4P2R-S-0 → CLK_PCIE_3GPLL 7 / CLK_PCIE_3GPLL# 7
SRCCLKT10 SRCCLKC10 — CLK_PCIE_NEW / CLK_PCIE_NEW# → CLK_PCIE_NEW_C 33 / CLK_PCIE_NEW_C# 33
SRCCLKT11/CR#_H SRCCLKC11/CR#_G — NEW-CARD_CLK_REQ#_R R223 475/F/03 NEW-CARD_CLK_REQ# / CLK_3GPLLREQ#_R R189 475/F/03 CLK_MCH_OE# → NEW-CARD_CLK_REQ# 33 / CLK_MCH_OE# 7
PCICLK0/CR#_A PCICLK1/CR#_B PCICLK2/TME PCICLK3 PCICLK4/27_SELECT — R_PCLK_8512 R186 33_4 → PCLK_LPC_8512 36; PCLK_MINI_LPC R180 475/F_4 → PCIE_LANREQ# 31; RPCI_CLK_SIO R194 33_4 → PCLK_LPC_DEBUG 35; FCTSEL1 R195 33_4 → PCLK_LPC_TPM 34; R179 33_4 → PCI_CLK_SIO 27; R184 33_4 → PCI_CLK_R5C847 25
PCI_F5/ITP_EN — ITP_EN R183 33_4 → PCLK_ICH 20
USB_48MHZ/FSLA — FSA R182 33_4; R181 4.7K_4 CLK_BSEL0 → CLK_48M_USB 21
FSLC/TST_SL/REF — FSC R217 4.7K_4 CLK_BSEL2; R216 22_4; R214 33_4 → CLK_14M_ICH 21 / CLK_SIO_14M 27

GCLK_SEL = FCTSEL1

FCTSEL1 (PIN13)	PIN13	PIN14	PIN17	PIN18
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

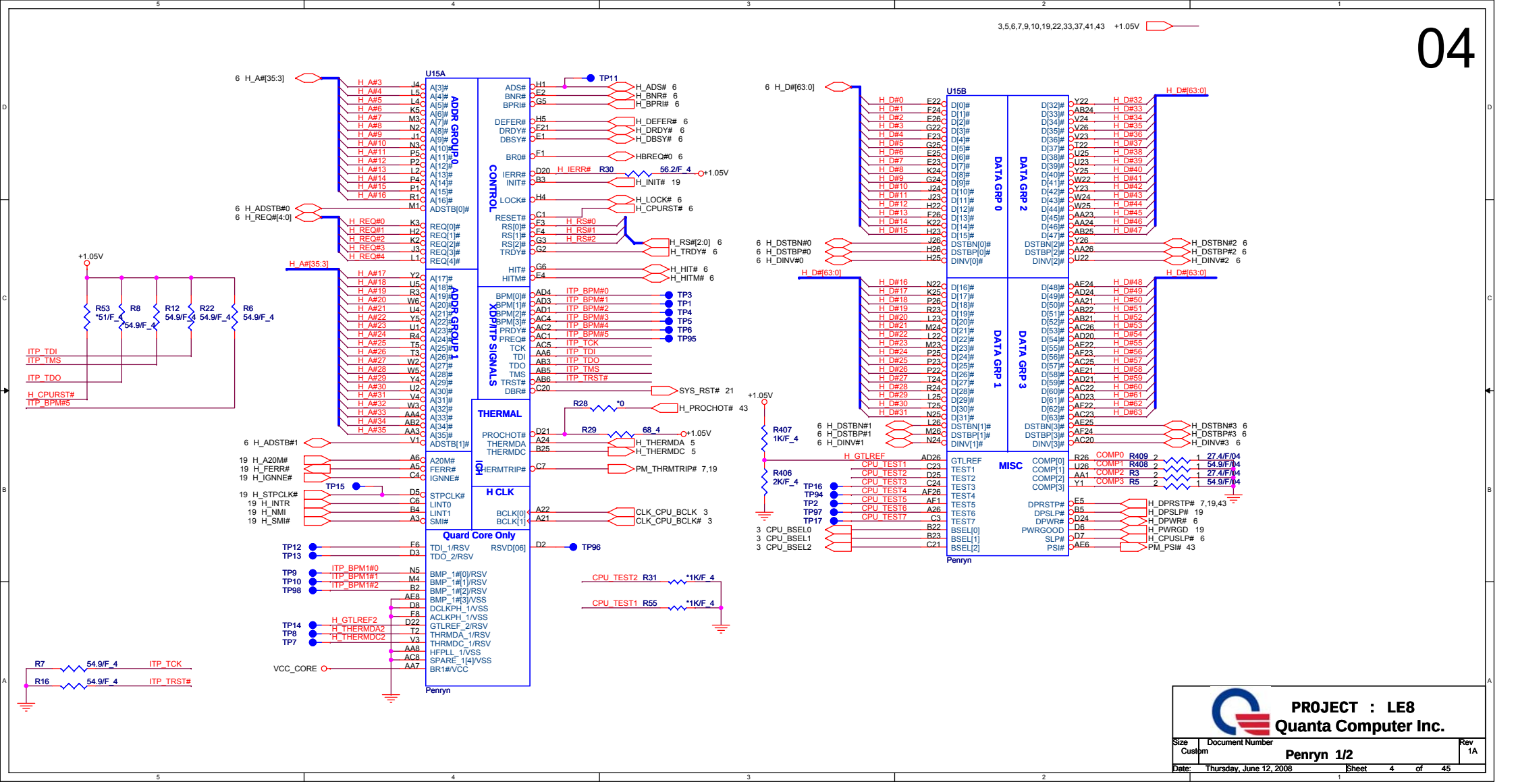
CPU Clock select

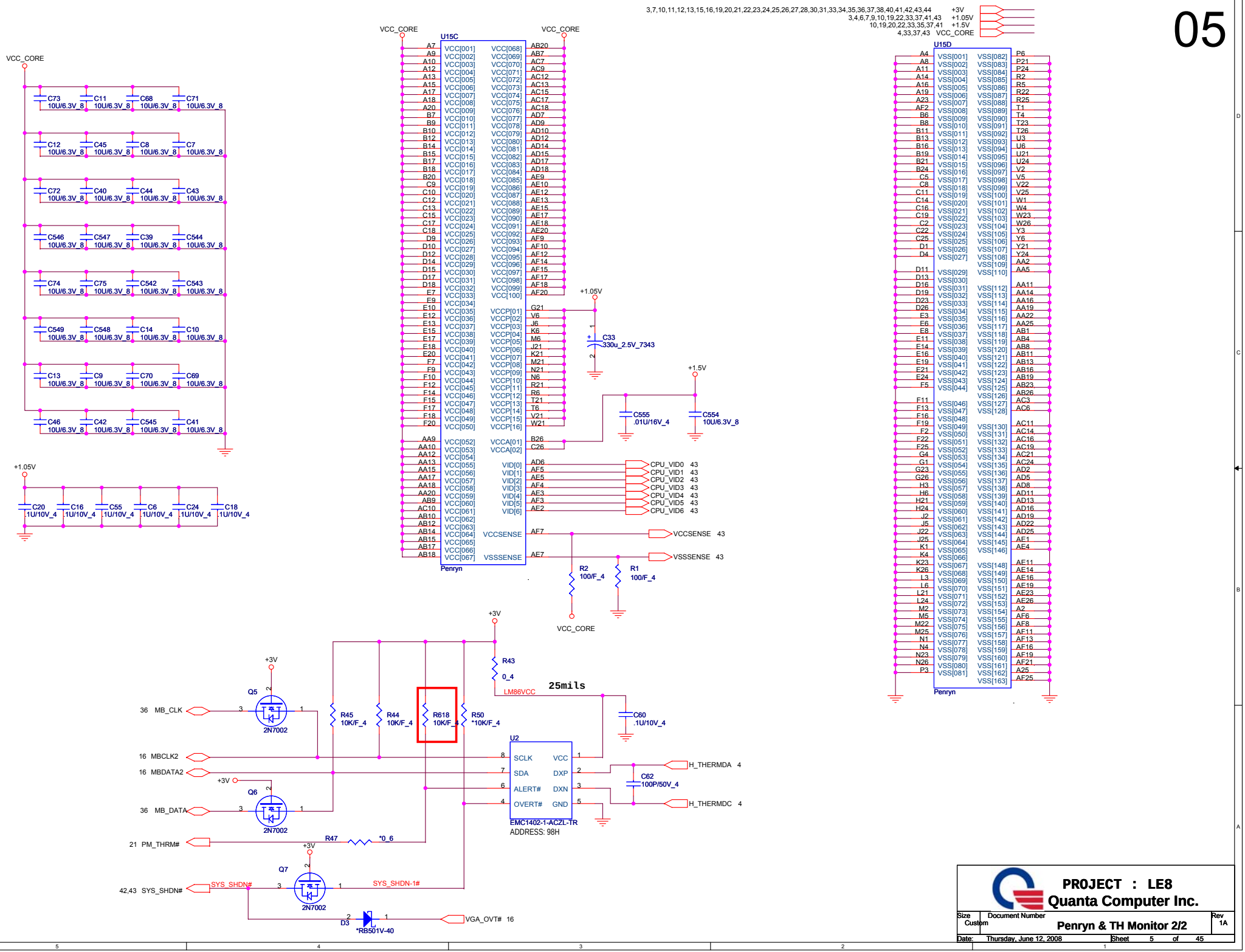
4 CPU_BSEL0 — CLK_BSEL0 — R175 0/04 — MCH_BSEL0 7
R170 *1K/04
4 CPU_BSEL1 — CLK_BSEL1 — R228 0/04 — MCH_BSEL1 7
+1.05V — R229 *1K/04
4 CPU_BSEL2 — CLK_BSEL2 — R232 0/04 — MCH_BSEL2 7
+1.05V — R231 *1K/04

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

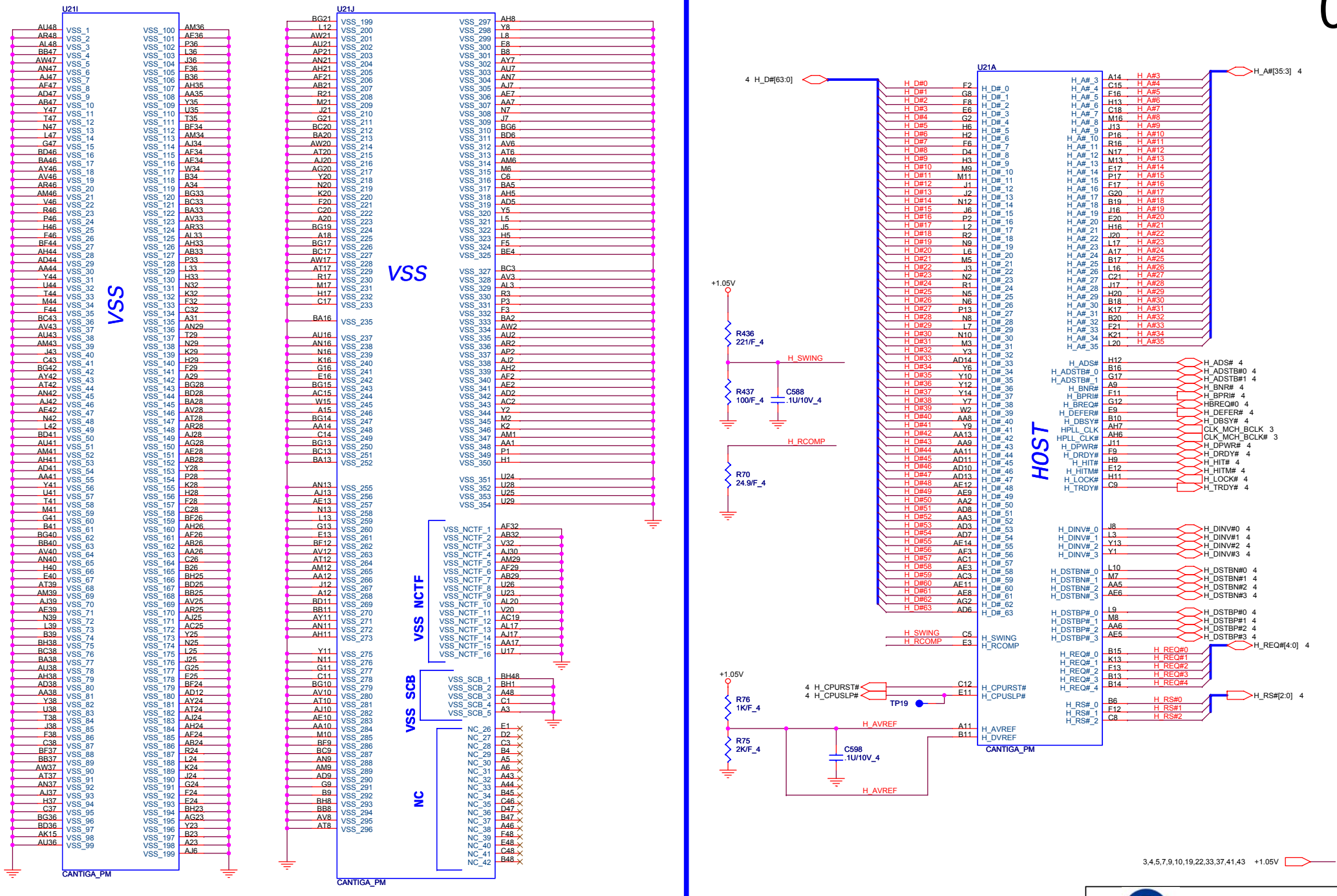
C342 *33P/50V/04 PCLK_LPC_8512
C327 *33P/50V/04 PCLK_ICH
C336 *33P/50V/04 PCLK_LPC_DEBUG
C330 27P/50V/04 CLK_48M_USB
C391 *33P/50V/04 CLK_14M_ICH
C764 *22P/50V/04 PCI_CLK_SIO
for EMI

PROJECT : LE8
Quanta Computer Inc.
Size: Custom | Document Number: CLOCK GENERATOR | Rev: 1A
Date: Thursday, June 12, 2008 | Sheet 3 of 45


04
3,5,6,7,9,10,19,22,33,37,41,43 +1.05V
U15A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
ICH
H CLK
Quard Core Only
Penryn
U15B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
Penryn
PROJECT : LE8
Quanta Computer Inc.
Penryn 1/2
Size Custom
Document Number
Rev 1A
Date: Thursday, June 12, 2008
Sheet 4 of 45



PROJECT :	LE8
Quanta Computer Inc.	
Size: Custom	Document Number: Penryn & TH Monitor 2/2
Rev: 1A	
Date: Thursday, June 12, 2008	Sheet 5 of 45



PROJECT : LE8			
Quanta Computer Inc.			
Size: Custom	Document Number: Cantiga Host & VSS 1/5		Rev: 1A
Date: Thursday, June 12, 2008	Sheet 6 of 45		

MCH_CFG_5 DMIx2 selection

Low: DMIx2
High: DMIx4 (Default)

MCH_CFG_16 FSB Dynamic ODT

Low: Dynamic ODT disabled
High: Dynamic ODT enabled (Default)

MCH_CFG_9 PCI Express Graphic Lane

Low: Reverse Lane
High: Normal operation(Default)

MCH_CFG_19 DMI Lane Reversal

Low: Normal (Default)
High: Lane Reserved

MCH_CFG_6 iTPM Host Interface

Low: iTPM Host Interface enabled
High: iTPM Host Interface disabled (Default)

MCH_CFG_7 Intel (R) Management Engine Crypto

Low: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality
High: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality (Default)

MCH_CFG_10 PCIe Lookback Enable

Low: Enabled
High: Disabled (Default)

MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13	MCH_CFG_12	Configuration
0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

U21B

RSVD
CLK/ DDR CLK/ CONTROL/COMPENSATION
CLK
ME JTAG
DMI
CFG
GRAPHICS VID
PM
ME
MISC
HDA
NC

CANTIGA_PM

U21C

LVDS
TVL
VGA
PCI-EXPRESS GRAPHICS

CANTIGA_PM

UMA & Discrete setting

LVDS Discrete / UMA
R131 NC 10K
R137 NC 10K

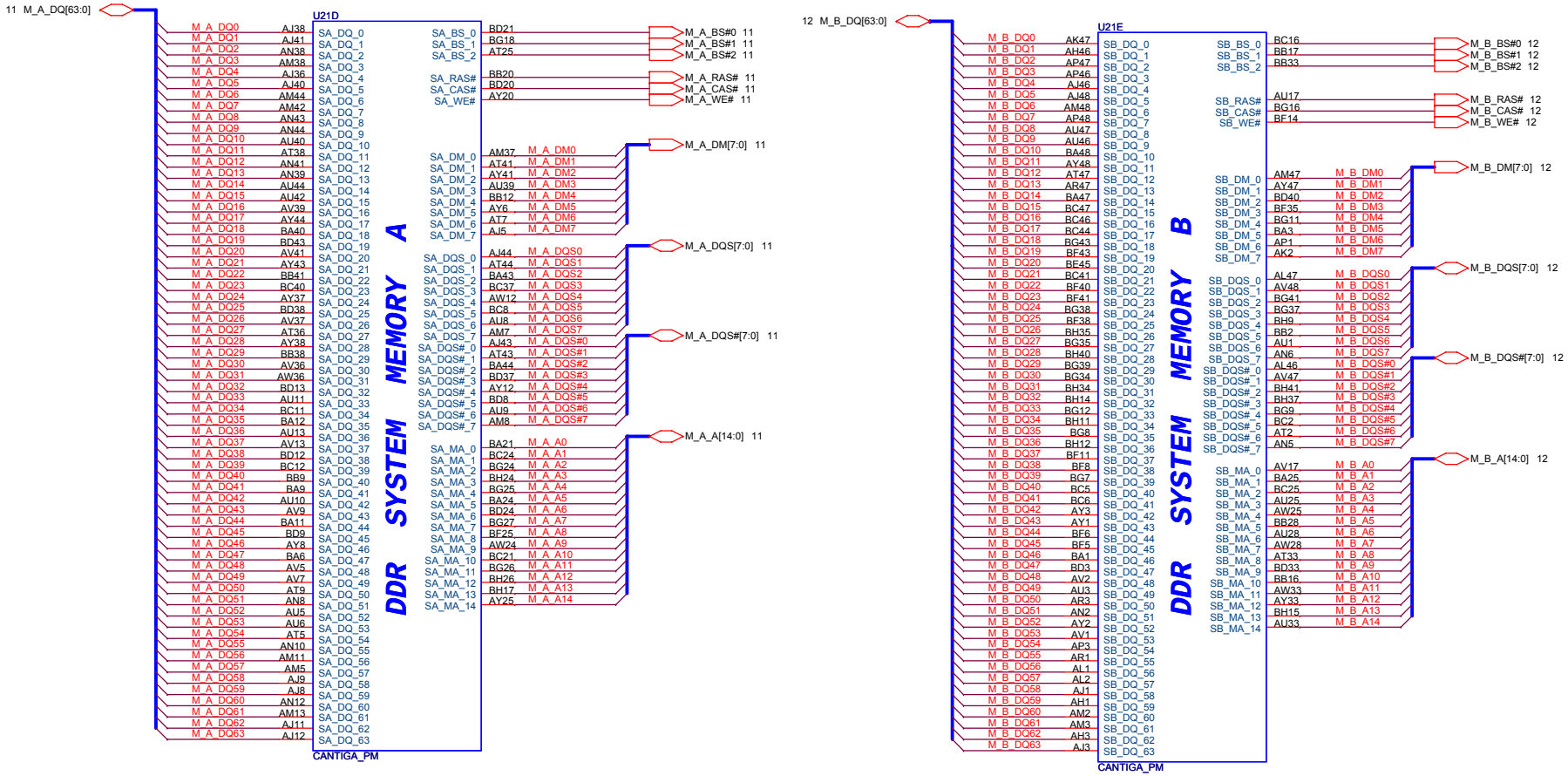
LVDS Discrete / UMA
R479 NC 2.37K

UMA & Discrete setting

UMA & Discrete setting
CRT/TV Discrete / UMA

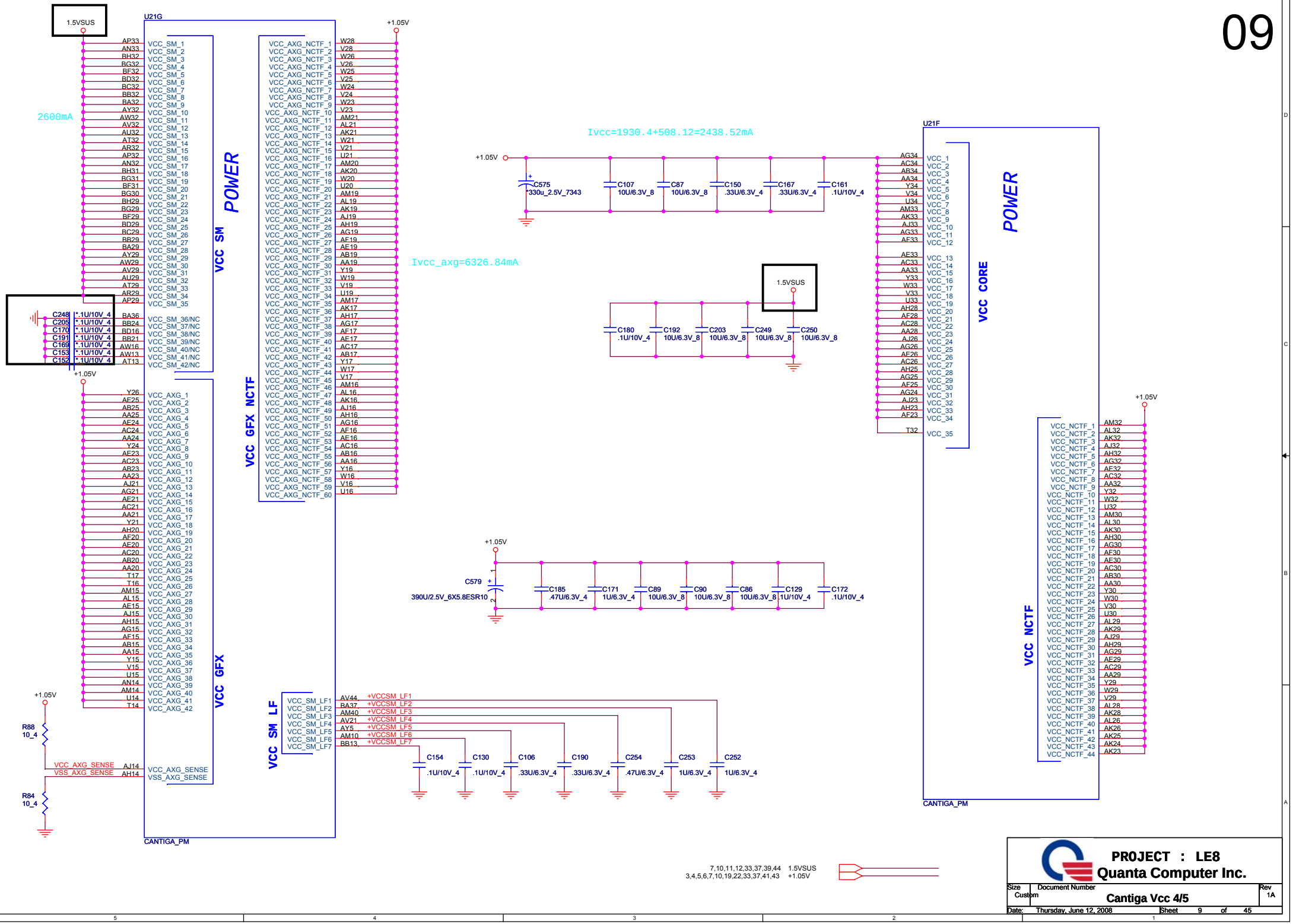
R111	0	75
R107	0	75
R112	0	75
R133	NC	0
R132	NC	0
R120	0	150
R126	0	150
R123	0	150
R121	NC	33
R127	0	1.02K
R125	NC	33

UMA & Discrete setting
Discrete DREFCLK/ DREFCLK# 0Ω
Discrete DREFSSCLK/ DREFSSCLK# 0Ω
UMA DREFCLK/ DREFCLK# NC
UMA DREFSSCLK/ DREFSSCLK# NC

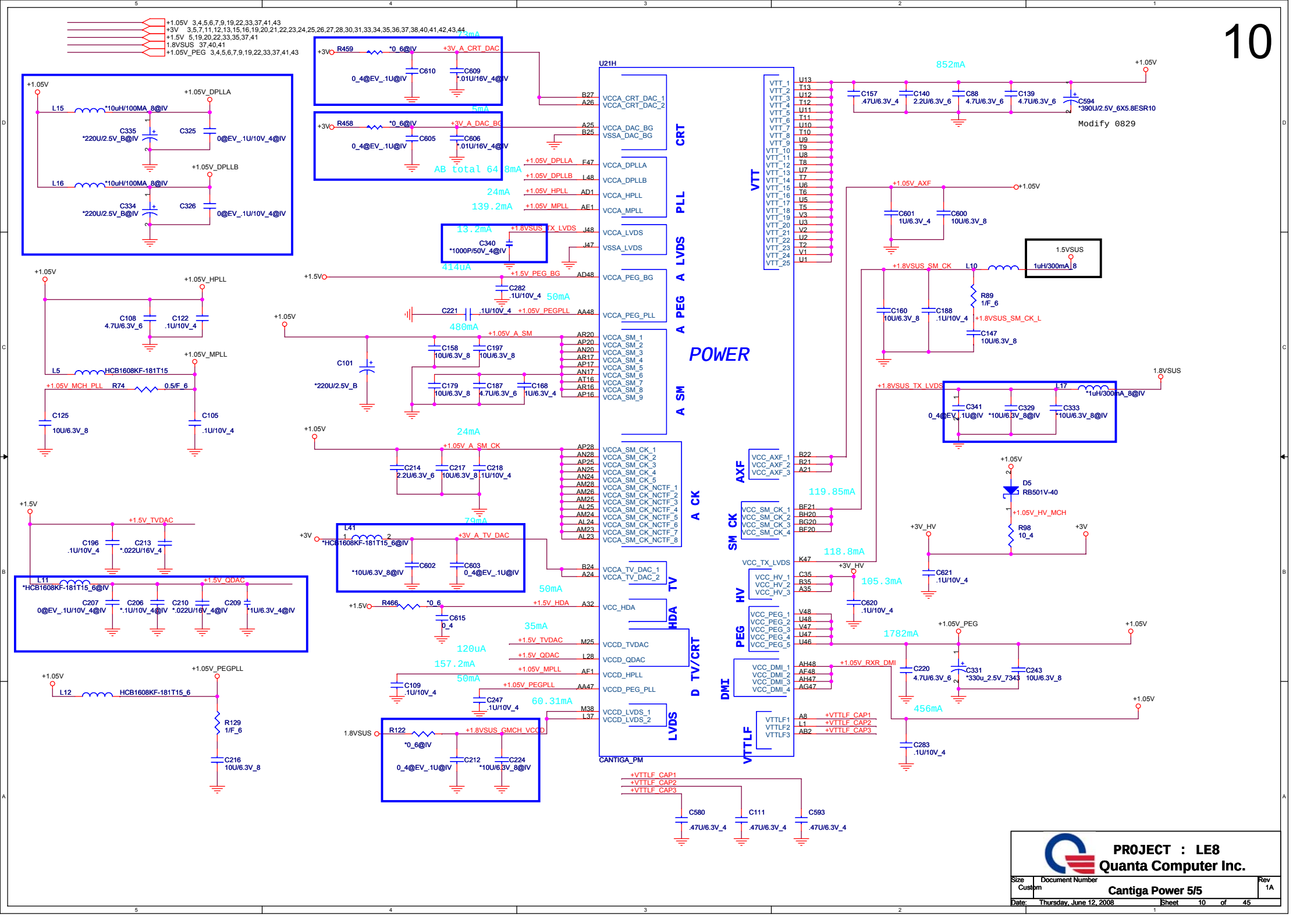


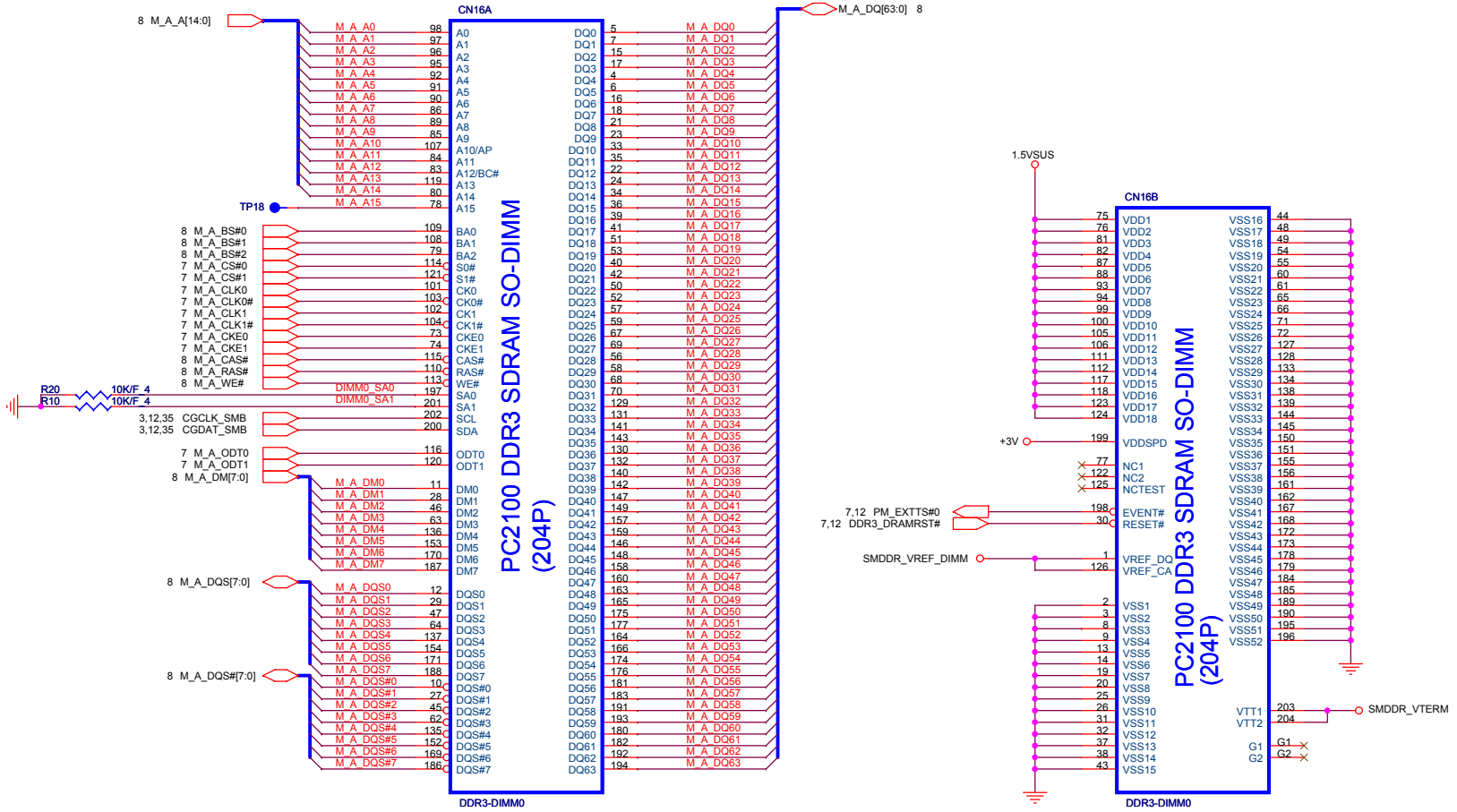
PROJECT : LE8
Quanta Computer Inc.

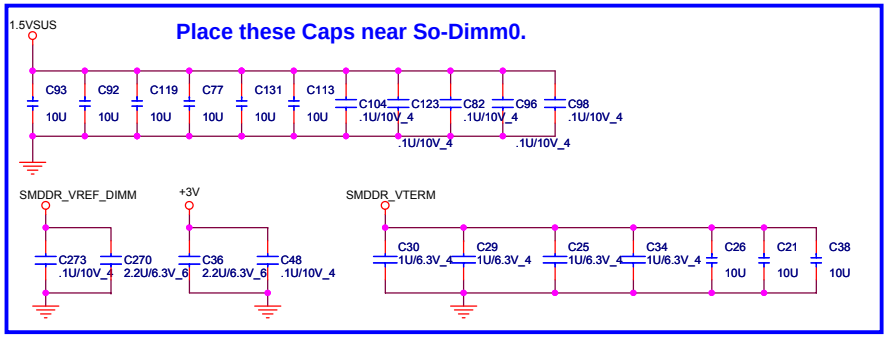
Size	Document Number	Rev
Custom	Cantiga DDR3 3/5	1A
Date: Thursday, June 12, 2008	Sheet 8 of 45	

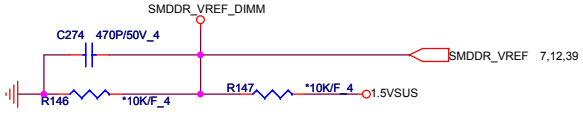


PROJECT :	LE8
Quanta Computer Inc.	
Size: Custom	Document Number: Cantiga Vcc 4/5
Rev: 1A	
Date: Thursday, June 12, 2008	Sheet 9 of 45


+1.05V 3,4,5,6,7,9,19,22,33,37,41,43
+3V 3,5,7,11,12,13,15,16,19,20,21,22,23,24,25,26,27,28,30,31,33,34,35,36,37,38,40,41,42,43,44
+1.5V 5,19,20,22,33,35,37,41
1.8VSUS 37,40,41
+1.05V_PEG 3,4,5,6,7,9,19,22,33,37,41,43
U21H
POWER
CRT
PLL
LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT
CANTIGA_PM
Modify 0829
852mA
119.85mA
118.8mA
105.3mA
1782mA
456mA
Quanta Computer Inc.
PROJECT : LE8
Cantiga Power 5/5
Size Custom
Document Number
Rev 1A
Date: Thursday, June 12, 2008
Sheet 10 of 45

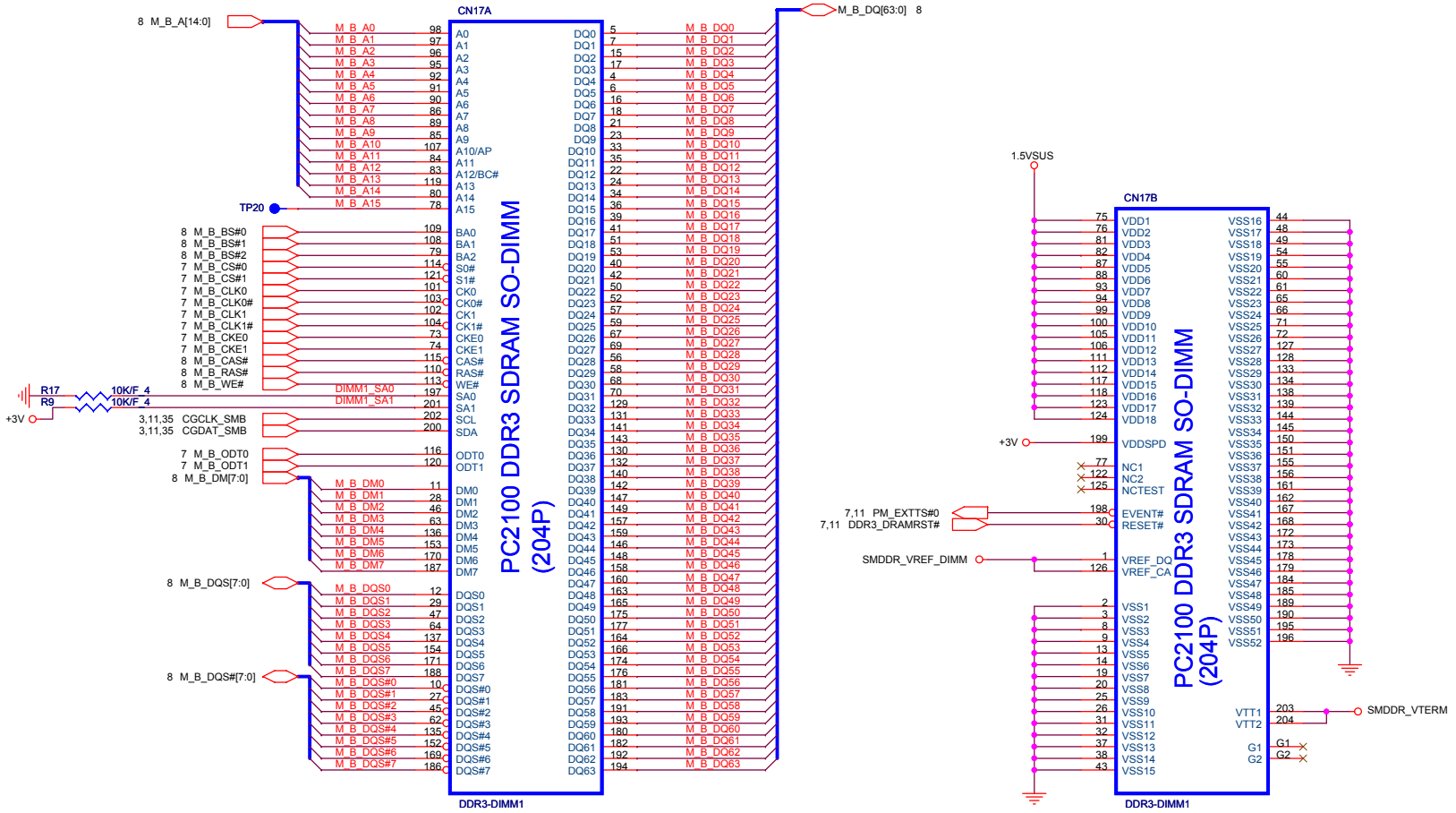


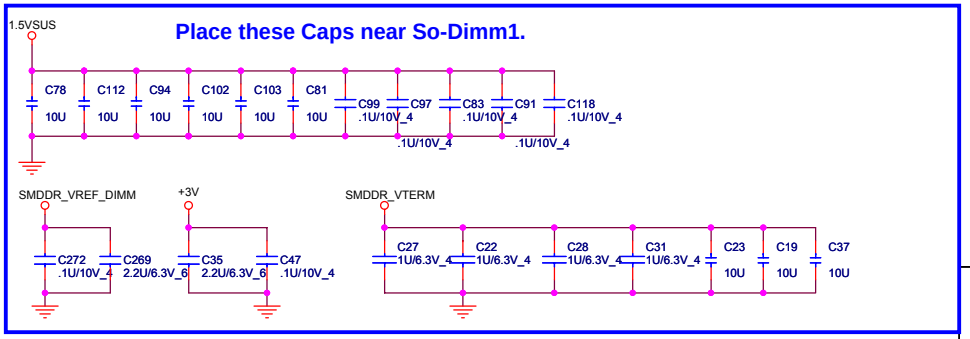




PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-0(H=5.2)	1A
Date: Thursday, June 12, 2008	Sheet 11 of 45	





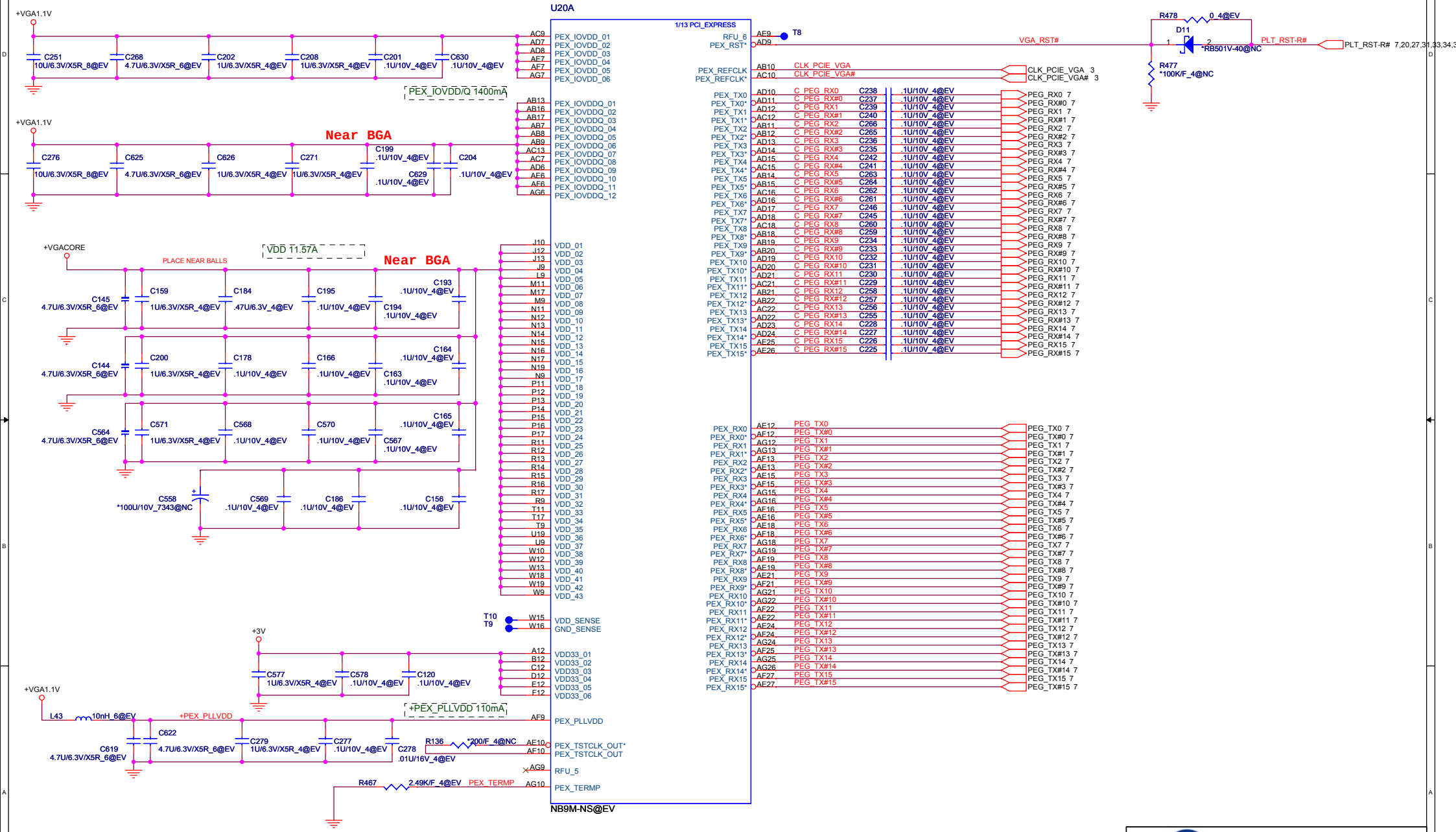
PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-1(H=9.2)	1A
Date: Thursday, June 12, 2008	Sheet 12 of 45	

NB9M-NS (G98)

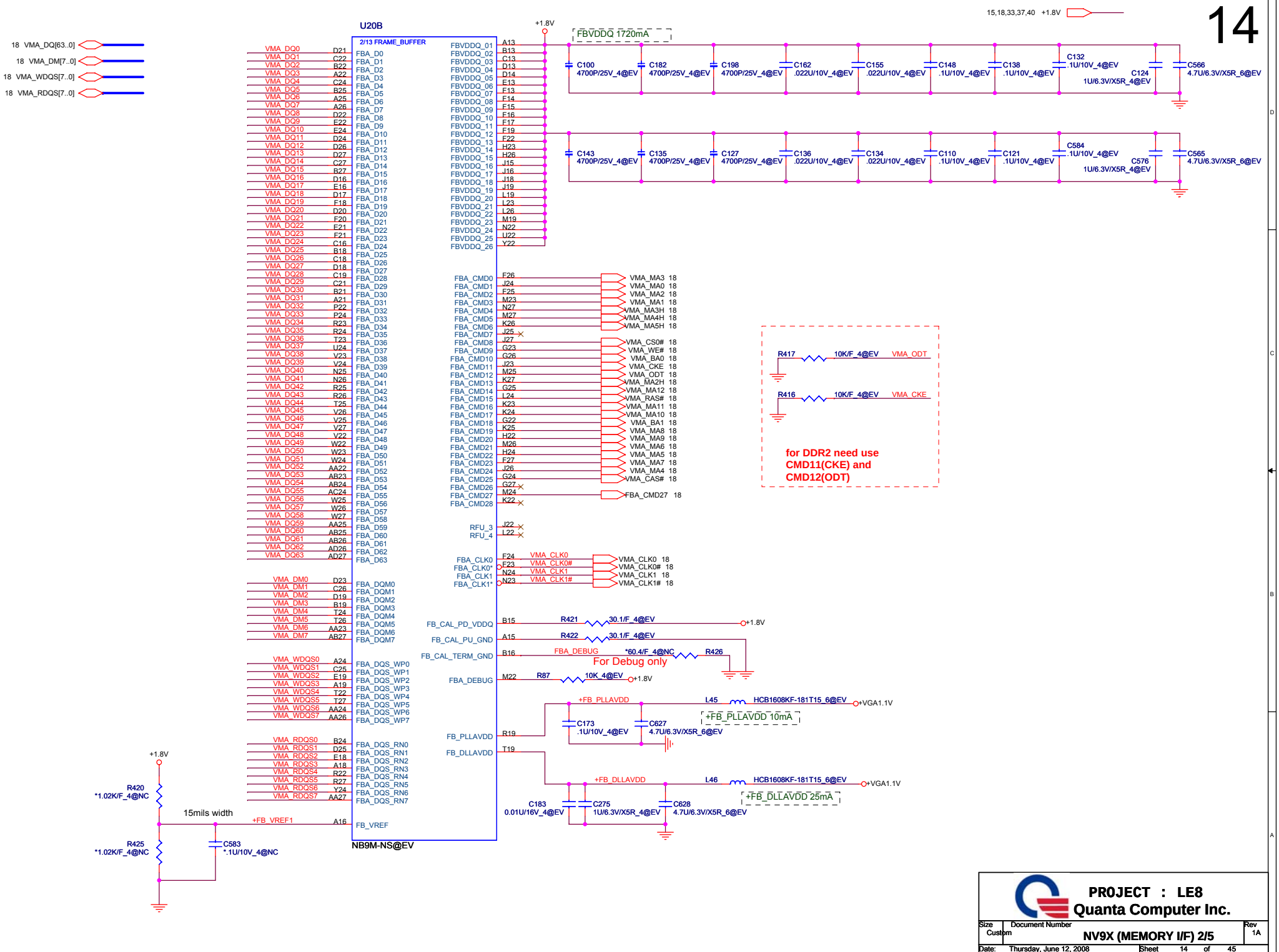
Part Value have show "@NC" is No Stuff

13



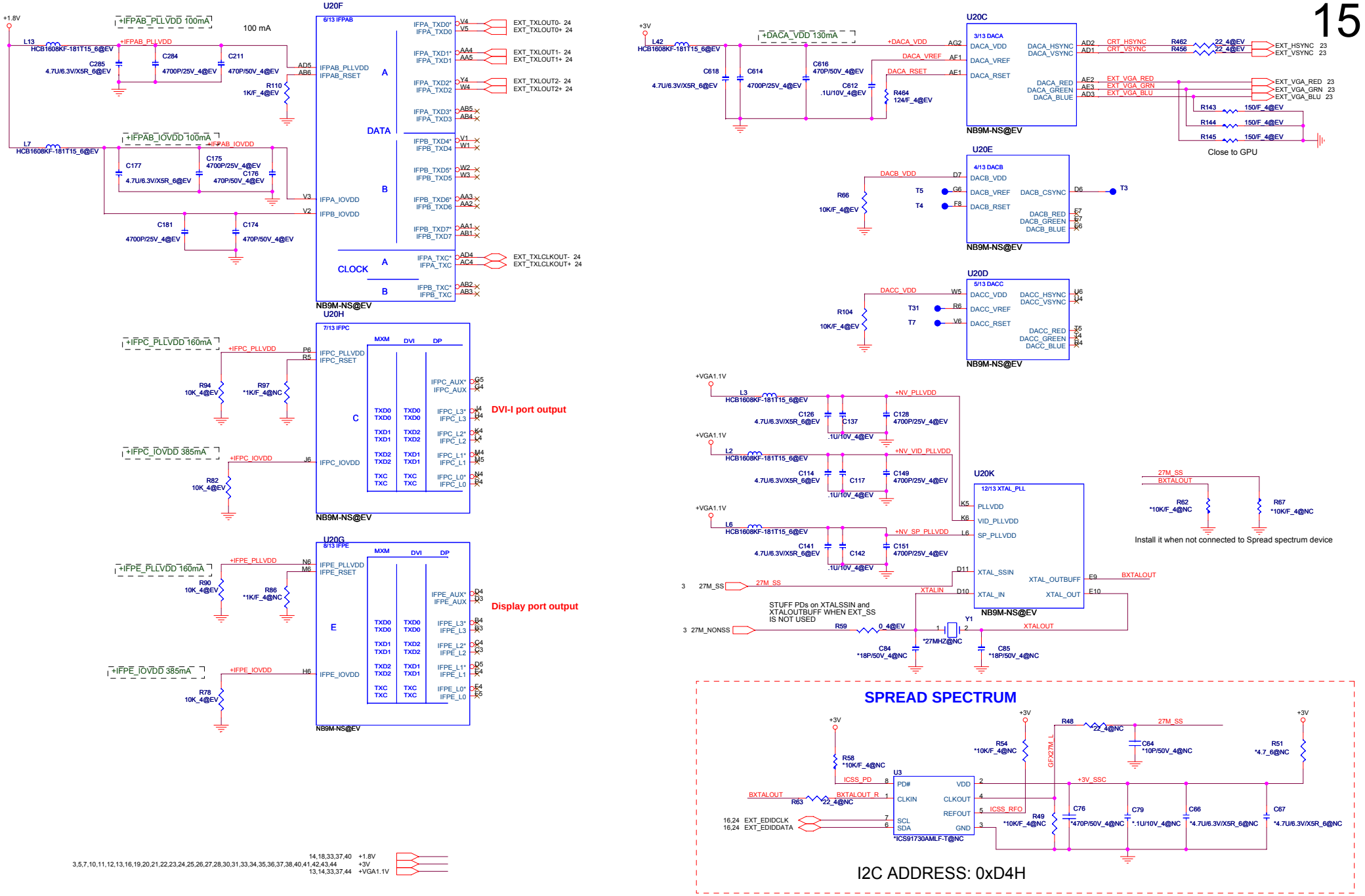
PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV9X (PCIE I/F) 1/5	1A
Date: Thursday, June 12, 2008	Sheet 13 of 45	



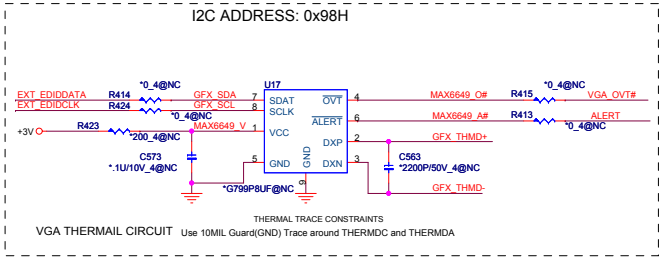
PROJECT : LE8
Quanta Computer Inc.

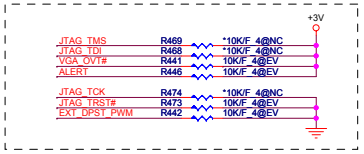
Size	Document Number	Rev
Custom	NV9X (MEMORY I/F) 2/5	1A
Date: Thursday, June 12, 2008	Sheet 14 of 45	

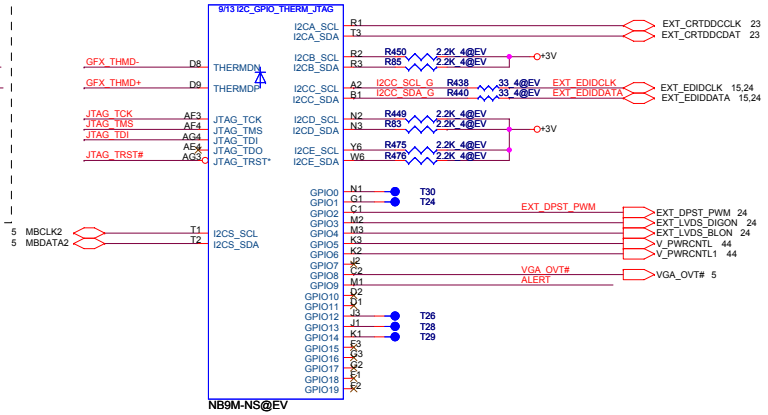


14,18,33,37,40	+1.8V
3,5,7,10,11,12,13,16,19,20,21,22,23,24,25,26,27,28,30,31,33,34,35,36,37,38,40,41,42,43,44	+3V
13,14,33,37,44	+VGA1.1V

PROJECT : LE8			
Quanta Computer Inc.			
Size: Custom	Document Number: NV9X (DISPLAY) 3/5		Rev: 1A
Date: Thursday, June 12, 2008	Sheet 15 of 45		



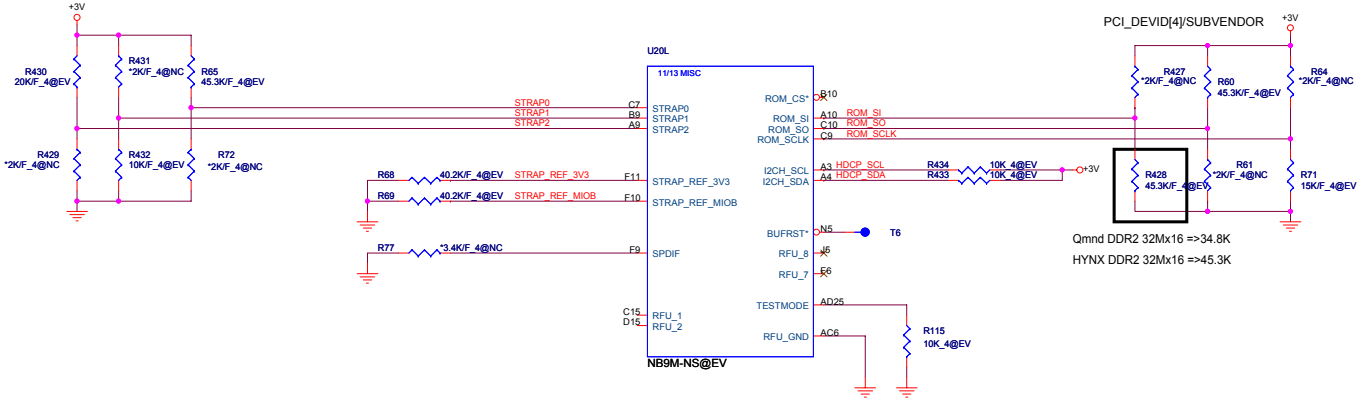




GPIO ASSIGNMENTS

SEE Datasheet for details on G9x Straps!

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	NVGEM HOTPLUG DETECT
1	IN	N/A	DVI/HDMI LINKC HOTPLUG DETECT
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	HIGH	NVVDD ALTV0
6	OUT	HIGH	NVVDD ALTV1
7	OUT	HIGH	FBVDD VID0
8	IN	LOW	OVERTEMP ALERT
9	OUT	LOW	THERMAL ALERT
10	OUT	HIGH	DYNAMIC FB VREF GDDR3(not used for DDR2)
11	OUT	HIGH	SLI SYNC0(not used for GB1-64)
12	IN	N/A	AC DETECT
13	OUT	LOW	POWER SUPPLY CONTROL0
14	OUT	HIGH	POWER SUPPLY CONTROL1
15	IN	N/A	HPD_E
16	IN	N/A	DVI_E
17	IN	N/A	HDMI_E
18	IN	N/A	DVI_F(not used)
19	IN	N/A	HDMI_F(not used)

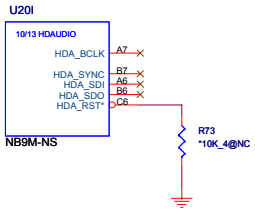


NB9M-NS Straps

NB9M-NS VRAM Configuration Table

ROM_SI VRAM CONFIG SET

STRAP	VALUE		MEMORY Vendor
0	5K	PD	NOT USED
1	10K	PD	Samsung DDR2 16Mx16
2	15K	PD	Qmnd DDR2 16Mx16
3	20K	PD	HYNX DDR2 16Mx16
4	25K	PD	NOT USED
5	30K	PD	Samsung DDR2 32Mx16
6	35K	PD	Qmnd DDR2 32Mx16
7	45K	PD	HYNX DDR2 32Mx16



3,5,7,10,11,12,13,15,19,20,21,22,23,24,25,26,27,28,30,31,33,34,35,36,37,38,40,41,42,43,44 +3V

PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
C	NV9X (GPIO & STRRAPS) 4/5	1A

Date: Thursday, June 12, 2008 Sheet 16 of 45

U20J

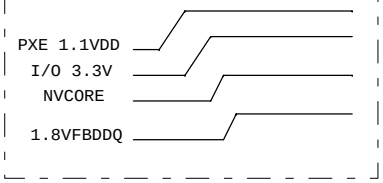
13/13 GND_NC

		NC_01	AA6
		NC_02	AC19
		NC_03	E15
		NC_04	T6
AC11	GND_01		
AC14	GND_02		
AC17	GND_03		
AC2	GND_04		
AC20	GND_05		
AC23	GND_06		
AC26	GND_07		
AC5	GND_08		
AC8	GND_09		
AE11	GND_10		
AE14	GND_11		
AE17	GND_12		
AE2	GND_13		
AE20	GND_14		
AE23	GND_15		
AE26	GND_16		
AE5	GND_17		
AE8	GND_18		
B11	GND_19		
B14	GND_20		
B17	GND_21		
B2	GND_22		
B20	GND_23		
B23	GND_24		
B26	GND_25		
B5	GND_26		
B8	GND_27		
E11	GND_28		
E14	GND_29		
E17	GND_30		
E2	GND_31		
E20	GND_32		
E23	GND_33		
E26	GND_34		
E5	GND_35		
E8	GND_36		
H2	GND_37		
H5	GND_38		
J11	GND_39		
J14	GND_40		
J17	GND_41		
K19	GND_42		
K9	GND_43		
L11	GND_44		
L12	GND_45		
L13	GND_46		
L14	GND_47		
L15	GND_48		
L16	GND_49		
L17	GND_50		
L2	GND_51		
L5	GND_52		
M12	GND_53		
M13	GND_54		
M14	GND_55		
M15	GND_56		
M16	GND_57		
P19	GND_58		
P2	GND_59		
P23	GND_60		
P26	GND_61		
P5	GND_62		
P9	GND_63		
T12	GND_64		
T13	GND_65		
T14	GND_66		
T15	GND_67		
T16	GND_68		
U11	GND_69		
U12	GND_70		
U13	GND_71		
U14	GND_72		
U15	GND_73		
U16	GND_74		
U17	GND_75		
U2	GND_76		
U23	GND_77		
U26	GND_78		
U5	GND_79		
V19	GND_80		
V9	GND_81		
W11	GND_82		
W14	GND_83		
W17	GND_84		
Y2	GND_85		
Y23	GND_86		
Y26	GND_87		
Y5	GND_88		

NB9M-NS@EV

NB9M: VGACORE +0.9V ~ +1.0V

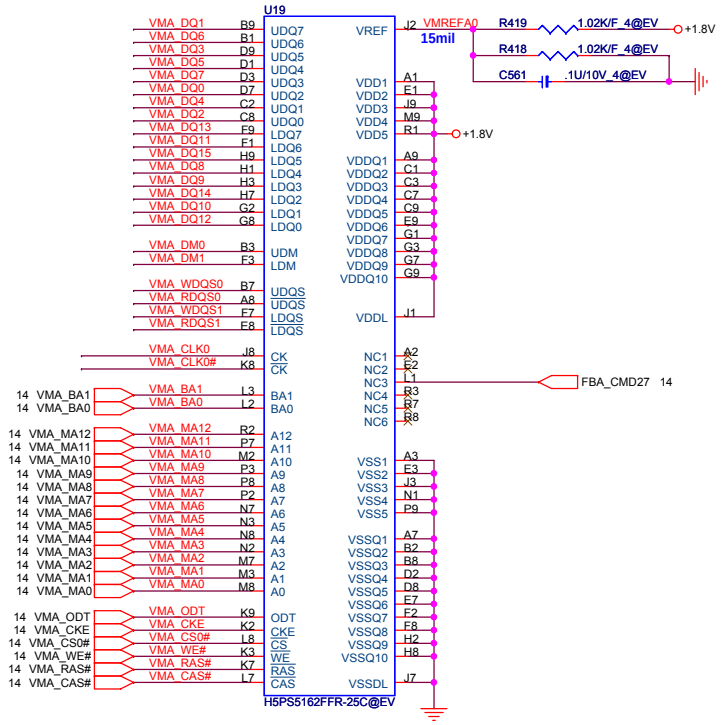
power up sequence

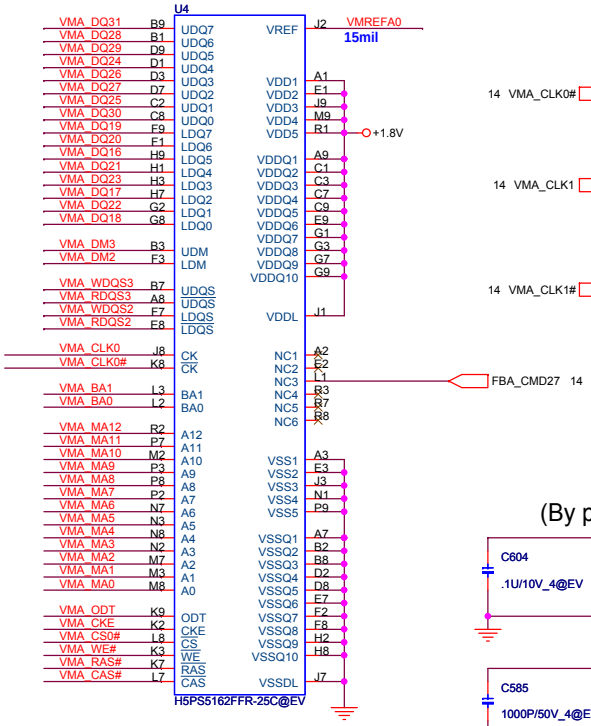


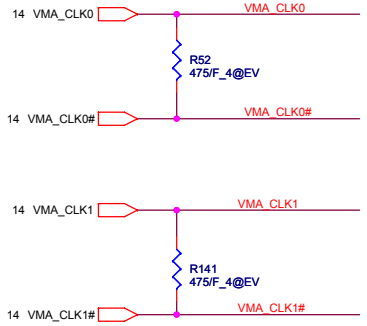
PROJECT : LE8
Quanta Computer Inc.

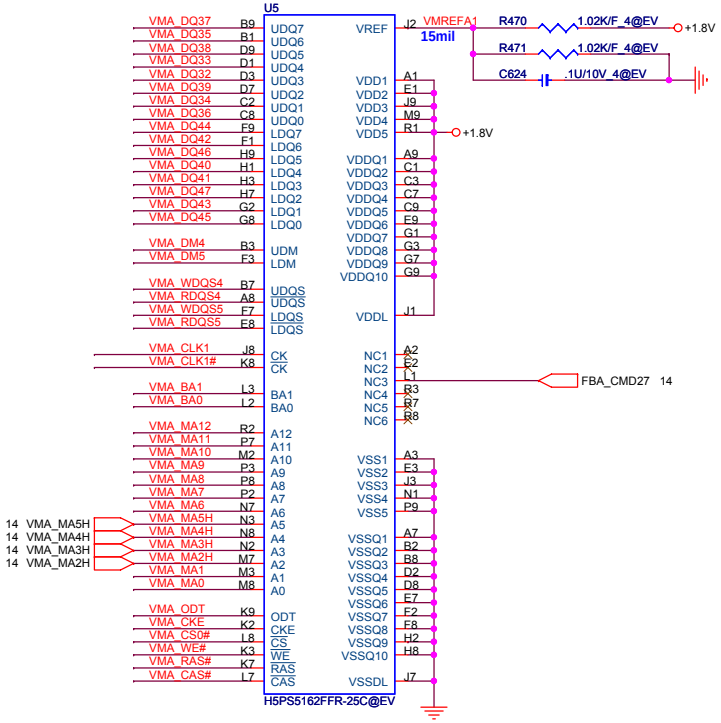
Size	Document Number	Rev
Custom	NV9X GND 5/5	1A

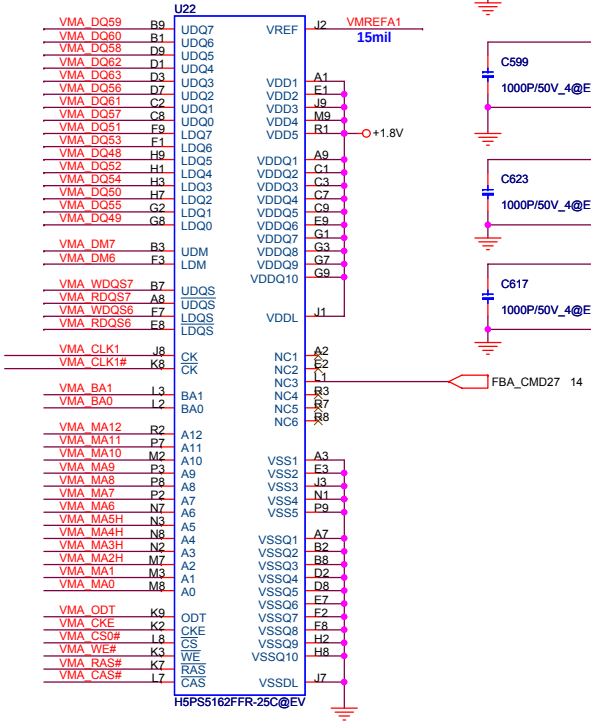
Date: Thursday, June 12, 2008 Sheet 17 of 45



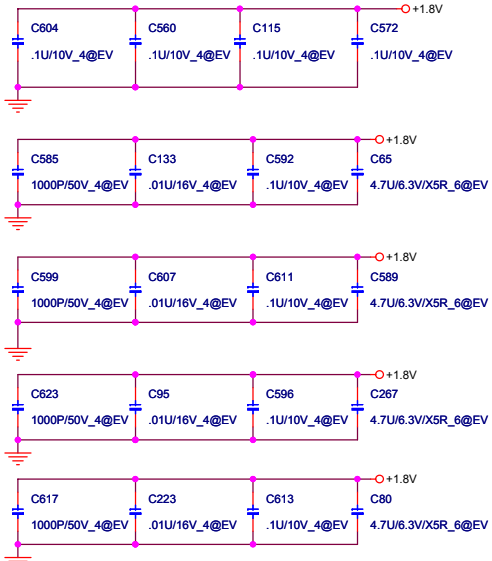








(By pass capacitor)

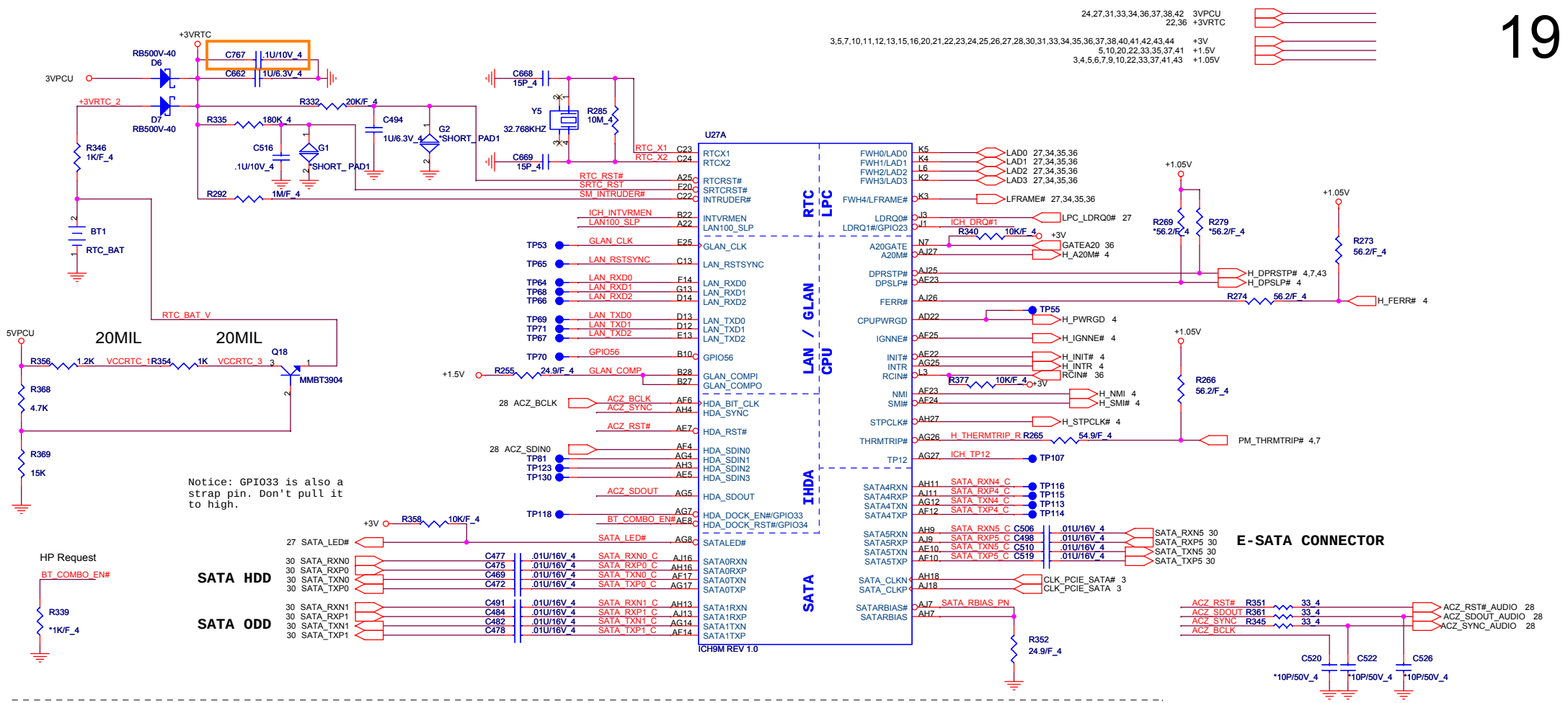


512Mb(32Mx16) : AKD5FG-TW03/Hynix(H5PS5162FFR-25C)
AKD5FG-T^03/Qimonda(HYB18T512161B2F-25)
512Mb(32Mx16) B&S : AKD5FG-TW04/Hynix(H5PS5162FFR-25C)
AKD5FG-T^10/Qimonda(HYB18T512161B2F-25)

14 VMA_DQ[63..0]
14 VMA_DM[7..0]
14 VMA_WDQS[7..0]
14 VMA_RDQS[7..0]
14,15,33,37,40 +1.8V

PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV9X VRAM-1(GDDR2 BGA84)	1A
Date: Thursday, June 12, 2008	Sheet 18 of 45	



SB Strap

ICH9-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH9-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1	
SPI	0	1	
PCI	1	0	
LPC	1	1	(default)

No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot

A16 swap override strap	
PCI_GNT#3	Low = A16 swap override enabled Hi = Default

TPM physical presence	
ICH_GPIO57	Low: Default

PROJECT : LE8
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Size	Document Number	Rev
Custom	ICH9-M Host 1/4	1A
Date: Thursday, June 12, 2008	Sheet 19 of 45	

5,10,19,22,33,35,37,41 +1.5V
3,5,7,10,11,12,13,15,16,19,21,22,23,24,25,26,27,28,30,31,33,34,35,36,37,38,40,41,42,43,44 +3V
21,25,26,28,33,34,35,36,37,39,43 3VSUS

EXPRESS CARD (NEW CARD)

MINI CARD PCI-E(WWAN)

MINI CARD PCI-E(WLAN)

PCIE-LAN

U27D

PCI-Express

Direct Media Interface

SPI

USB

ICH9M REV 1.0

USB Connector

Finger Printer

BLUETOOTH

NEW CARD

USB Connector

USB Connector

WWAN Min-Card

WLAN Min-Card

512K byte SPI ROM
For HDCP only

U14 *W25X40VSSIG

U27B

PCI

Interrupt I/F

ICH9M REV 1.0

U31 *TC7SH08FU

RP24 10P8R-8.2K

RP27 10P8R-8.2K

RP26 10P8R-8.2K

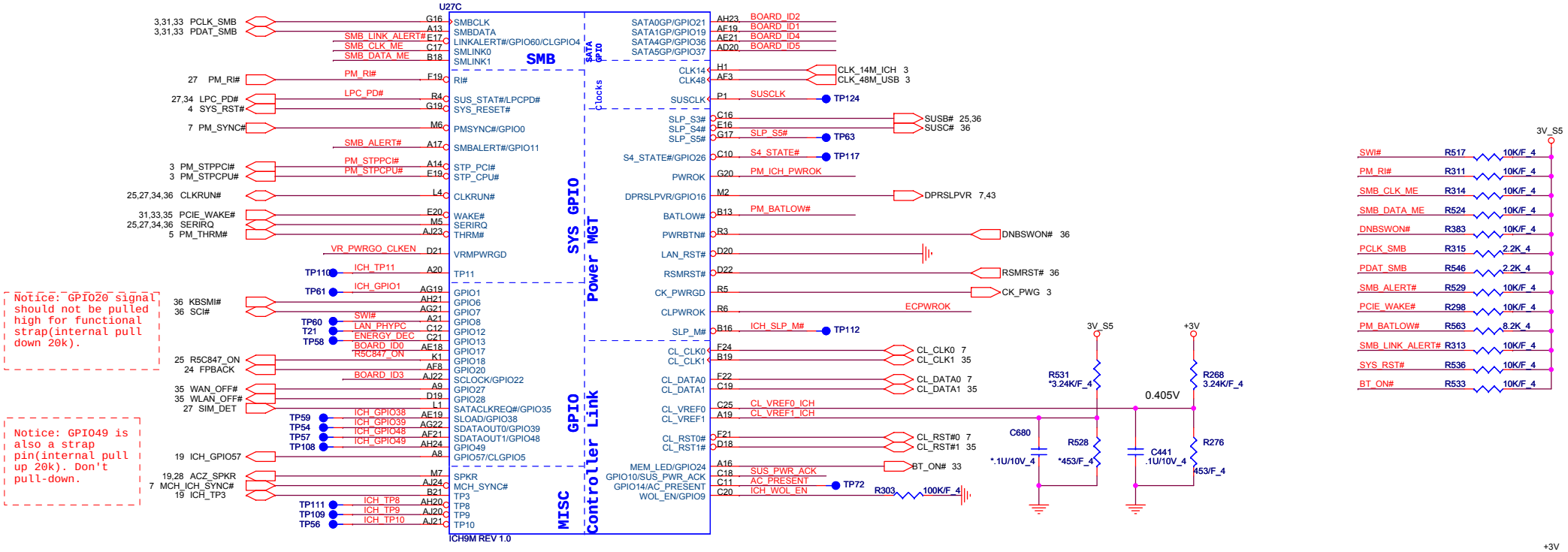
RP25 10P8R-8.2K

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTE#, F#, G#	RICOH R5C847

PROJECT : LE8
Quanta Computer Inc.

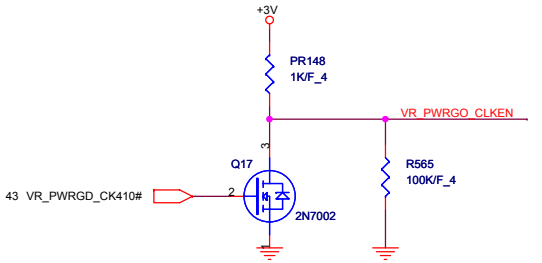
Size	Document Number	Rev
Custom	ICH9-M PCIE 2/4	1A
Date: Thursday, June 12, 2008	Sheet 20 of 45	

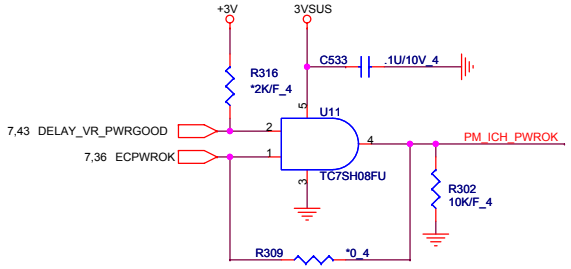
5,10,19,20,22,33,35,37,41 +1.5V
3,5,7,10,11,12,13,15,16,19,20,22,23,24,25,26,27,28,30,31,33,34,35,36,37,38,40,41,42,43,44 +3V
19,20,22,33,37 3V_S5
25,26,28,33,34,35,36,37,39,43 3VSUS



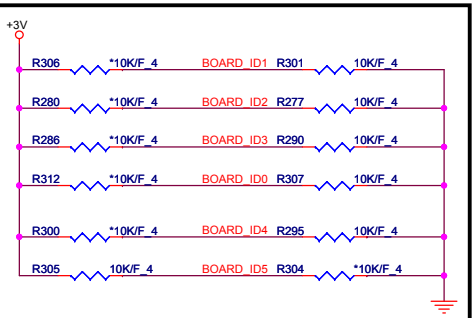
Notice: GPIO20 signal should not be pulled high for functional strap(internal pull down 20k).

Notice: GPIO49 is also a strap pin(internal pull up 20k). Don't pull-down.

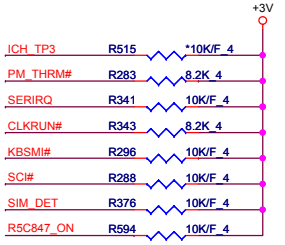


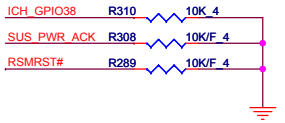


Board ID For Function	ID3 GPIO22	ID2 GPIO21	ID1 GPIO19	ID0 GPIO17
Default	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0
	0	1	0	1
	0	1	1	0
	0	1	1	1
	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	1	1
	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1



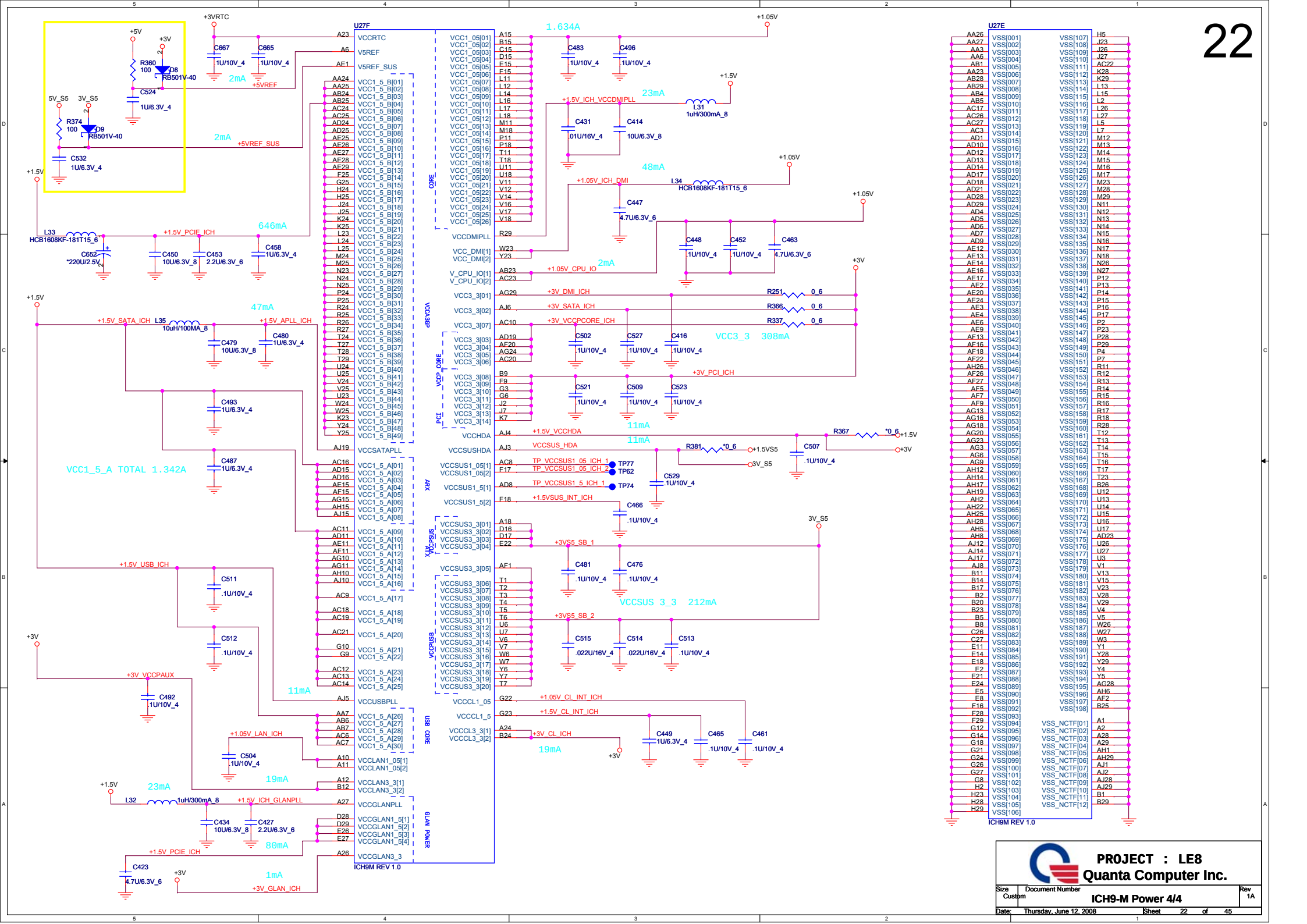
Board ID For Model	ID5 GPIO37	ID4 GPIO36
LE6	0	0
LE7	0	1
LE8	1	0
LE9	1	1





PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M GPIO 3/4	1A
Date: Thursday, June 12, 2008	Sheet 21 of 45	


U27F
U27E
+3VRTC
+5V
+3V
R360 100
D8 RB501V-40
C524 1U/6.3V_4
C667 1U/10V_4
C665 1U/10V_4
2mA
+5VREF
5V_S5
3V_S5
R374 100
D9 RB501V-40
C532 1U/6.3V_4
2mA
+5VREF_SUS
VCCRTC
V5REF
V5REF_SUS
VCC1_5_B[01]
VCC1_5_B[02]
VCC1_5_B[03]
VCC1_5_B[04]
VCC1_5_B[05]
VCC1_5_B[06]
VCC1_5_B[07]
VCC1_5_B[08]
VCC1_5_B[09]
VCC1_5_B[10]
VCC1_5_B[11]
VCC1_5_B[12]
VCC1_5_B[13]
VCC1_5_B[14]
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VCC1_5_B[16]
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VCC1_5_B[21]
VCC1_5_B[22]
VCC1_5_B[23]
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VCC1_5_B[25]
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VCCGLAN1_5[2]
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VCCGLAN1_5[4]
VCCGLAN3_3
ICH9M REV 1.0
CORE
VCCP
VCCP_CORE
PCI
RTC
VCCSUS3_3
VCCPUSB
USB CORE
GLAN POWER
VCC1_05[01]
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VCCSUS1_5[2]
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VCCSUS3_3[19]
VCCSUS3_3[20]
VCCCL1_05
VCCCL1_5
VCCCL3_3[1]
VCCCL3_3[2]
1.634A
+1.05V
C483 1U/10V_4
C496 1U/10V_4
+1.5V
23mA
+1.5V_ICH_VCCDMIPLL
L31 1uH/300mA_8
C431 .01U/16V_4
C414 10U/6.3V_8
48mA
+1.05V
+1.05V_ICH_DMI
L34 HCB1608KF-181T15_6
C447 4.7U/6.3V_6
+1.05V
C448 .1U/10V_4
C452 .1U/10V_4
C463 4.7U/6.3V_6
+1.05V_CPU_IO
2mA
+3V
+3V_DMI_ICH
R251 0_6
+3V_SATA_ICH
R366 0_6
+3V_VCCPCORE_ICH
R337 0_6
VCC3_3 308mA
C502 .1U/10V_4
C527 .1U/10V_4
C416 .1U/10V_4
+3V_PCI_ICH
C521 .1U/10V_4
C509 .1U/10V_4
C523 .1U/10V_4
11mA
+1.5V_VCCHDA
11mA
VCCSUS_HDA
R381 *0_6
+1.5VS5
3V_S5
R367 *0_6
+1.5V
+3V
C507 .1U/10V_4
TP_VCCSUS1_05_ICH_1
TP77
TP_VCCSUS1_05_ICH_2
TP62
TP_VCCSUS1_5_ICH_1
TP74
C529 .1U/10V_4
+1.5VSUS_INT_ICH
C466 .1U/10V_4
3V_S5
+3VS5_SB_1
C481 .1U/10V_4
C476 .1U/10V_4
VCCSUS 3_3 212mA
+3VS5_SB_2
C515 .022U/16V_4
C514 .022U/16V_4
C513 .1U/10V_4
+1.05V_CL_INT_ICH
+1.5V_CL_INT_ICH
+3V_CL_ICH
19mA
+3V
C449 1U/6.3V_4
C465 .1U/10V_4
C461 .1U/10V_4
VCC1_5_A TOTAL 1.342A
+1.5V
L33 HCB1608KF-181T15_6
C652 *220U/2.5V
+1.5V_PCIE_ICH
646mA
C450 10U/6.3V_8
C453 2.2U/6.3V_6
C458 1U/6.3V_4
+1.5V_SATA_ICH
L35 10uH/100MA_8
47mA
+1.5V_APLL_ICH
C479 10U/6.3V_8
C480 1U/6.3V_4
C493 1U/6.3V_4
C487 1U/6.3V_4
+1.5V_USB_ICH
C511 .1U/10V_4
C512 .1U/10V_4
+3V
+3V_VCCPAUX
C492 .1U/10V_4
11mA
+1.05V_LAN_ICH
C504 .1U/10V_4
19mA
+1.5V
23mA
L32 1uH/300mA_8
+1.5V_ICH_GLANPLL
C434 10U/6.3V_8
C427 2.2U/6.3V_6
80mA
+1.5V_PCIE_ICH
C423 4.7U/6.3V_6
+3V
1mA
+3V_GLAN_ICH
VSS[001]
VSS[002]
VSS[003]
VSS[004]
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VSS_NCTF[12]
ICH9M REV 1.0
PROJECT : LE8
Quanta Computer Inc.
Size Custom
Document Number
ICH9-M Power 4/4
Rev 1A
Date: Thursday, June 12, 2008
Sheet 22 of 45

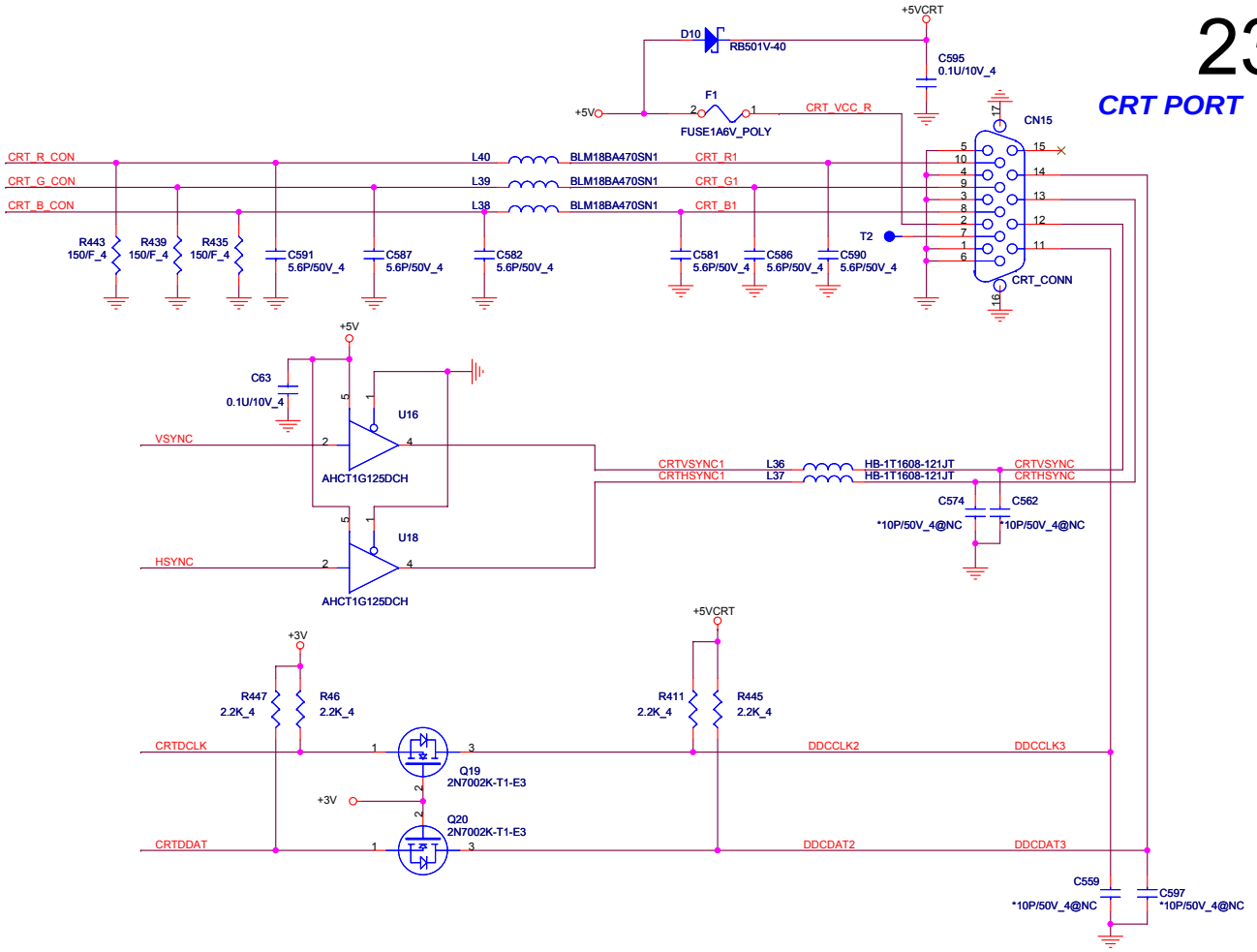
CRT PORT

CRT SWITCH

15	EXT_VGA_RED	R150 0_4@EV	CRT_R_CON
15	EXT_VGA_GRN	R149 0_4@EV	CRT_G_CON
15	EXT_VGA_BLU	R148 0_4@EV	CRT_B_CON
15	EXT_HSYNC	R463 0_4@EV	HSYNC
15	EXT_VSYNC	R457 0_4@EV	VSYNC
16	EXT_CRTDDCCLK	R451 0_4@EV	CRTDCLK
16	EXT_CRTDDCDAT	R91 0_4@EV	CRTDDAT
7	INT_CRT_RED	R155 *0_4@IV	
7	INT_CRT_GRN	R154 *0_4@IV	
7	INT_CRT_BLU	R153 *0_4@IV	
7	INT_HSYNC	R461 *0_4@IV	
7	INT_VSYNC	R460 *0_4@IV	
7	INT_CRT_DDCCLK	R452 *0_4@IV	
7	INT_CRT_DDCDAT	R92 *0_4@IV	

UMA & Discrete setting

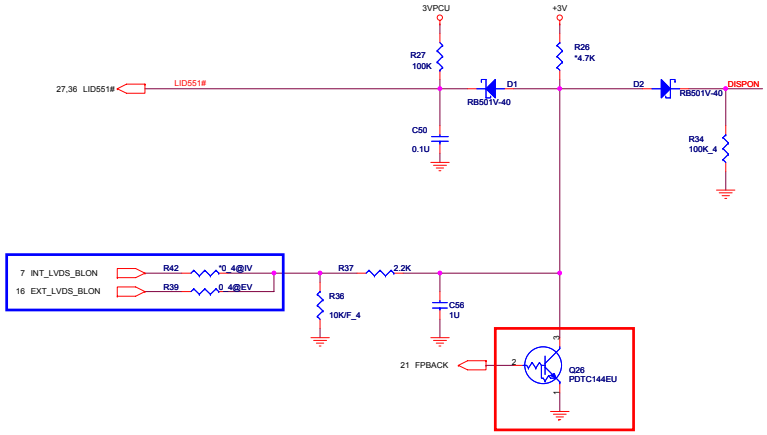
LVDS	Discrete	/ UMA
R150	0	NC
R149	0	NC
R148	0	NC
R463	0	NC
R457	0	NC
R451	0	NC
R91	0	NC
R155	NC	0
R154	NC	0
R153	NC	0
R461	NC	0
R460	NC	0
R452	NC	0
R92	NC	0

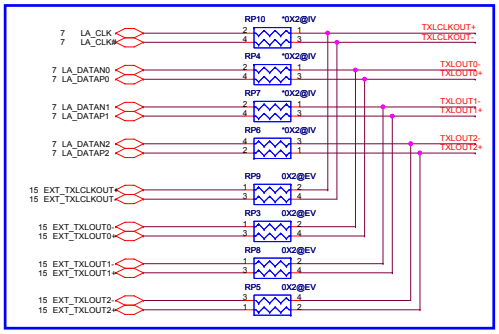


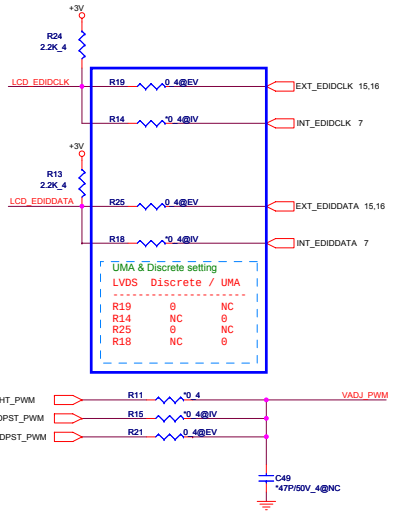
PROJECT : LE8
Quanta Computer Inc.

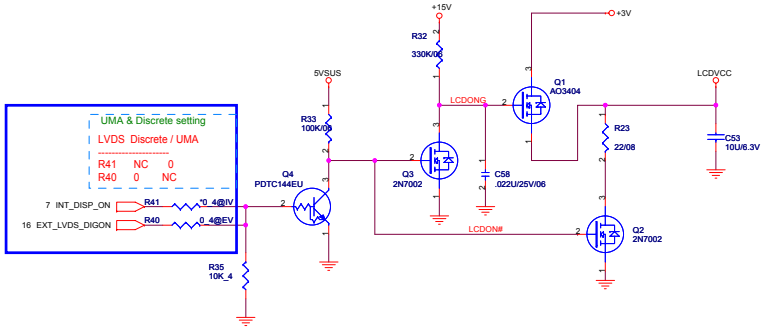
Size	Document Number	Rev
Custom	CRT CON	1A

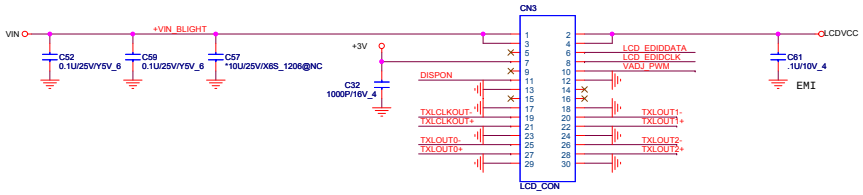
Date: Thursday, June 12, 2008 Sheet 23 of 45





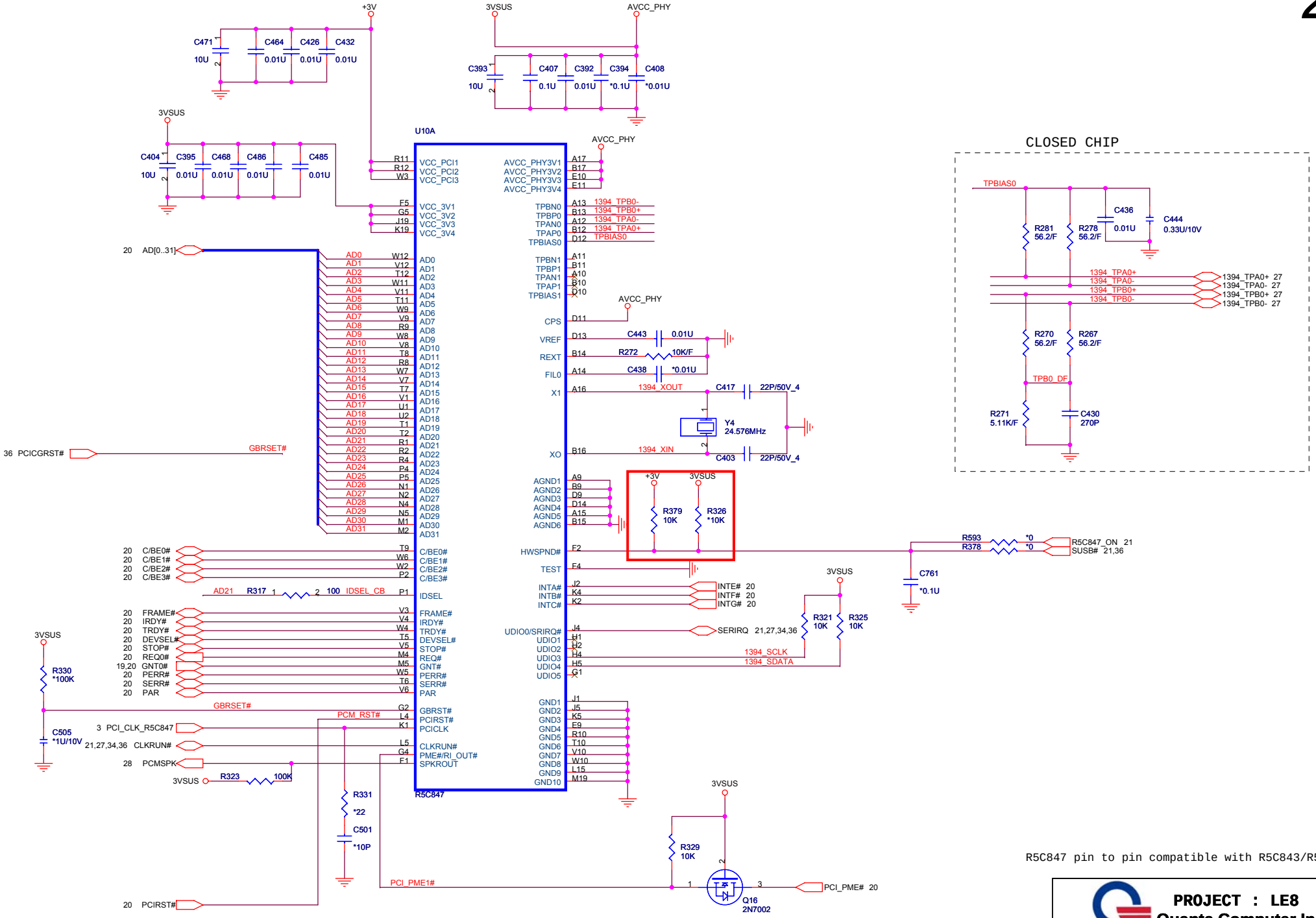






PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD & LID CON	1A
Date: Thursday, June 12, 2008	Sheet 24 of 45	


U10A
R5C847
CLOSED CHIP
R5C847 pin to pin compatible with R5C843/R5C841
PROJECT : LE8
Quanta Computer Inc.
R5C847 PCI/1394
Size Custom
Document Number
Rev 1A
Date: Thursday, June 12, 2008
Sheet 25 of 45

PCMCIA CONNECTOR

3 IN1 CARD-READER (PUSH-PUSH)

Support MMC/SD/MS Cards

26

U10B

CADR0 E16 CADR0
CADR1 F18 CADR1
CADR2 F15 CADR2
CADR3 G18 CADR3
CADR4 G15 CADR4
CADR5 H18 CADR5
CADR6 H15 CADR6
CADR7 J16 CADR7
CADR8 P15 CADR8
CADR9 R19 CADR9
CADR10 U19 CADR10
CADR11 R18 CADR11
CADR12 K18 CADR12
CADR13 N15 CADR13
CADR14 N18 CADR14
CADR15 K15 CADR15
Shield GND — R260 15 — CADR16 L19 CADR16
CADR17 P16 CADR17
CADR18 N16 CADR18
CADR19 N19 CADR19
CADR20 M16 CADR20
CADR21 L18 CADR21
CADR22 L16 CADR22
CADR23 K16 CADR23
CADR24 J15 CADR24
CADR25 J18 CADR25

CDATA0 E19 CDATA0
CDATA1 D19 CDATA1
CDATA2 C19 CDATA2
CDATA3 R14 CDATA3
CDATA4 T15 CDATA4
CDATA5 W15 CDATA5
CDATA6 W16 CDATA6
CDATA7 W17 CDATA7
CDATA8 D18 CDATA8
CDATA9 C18 CDATA9
CDATA10 B19 CDATA10
CDATA11 V15 CDATA11
CDATA12 V16 CDATA12
CDATA13 V17 CDATA13
CDATA14 W18 CDATA14
CDATA15 U18 CDATA15

OE# T19 OE#
WE# M15 WE#
CE2# T18 CE2#
CE1# V19 CE1#
REG# F16 REG#
RESET H19 RESET
WAIT# G16 WAIT#
IOIS16# A18 WP/IOIS163
IREQ# M18 RDY/IREQ#
SPKR# F19 BVD2
CHSTS# E18 BVD1
VS2 H16 VS2#
VS1 R16 VS1#
CD2# D15 CD2#
CD1# T14 CD1#
INPACK# G19 INPACK#

IORD# P18 IORD#
IOWR# P19 IOWR#

R275 10K — V14 USBDP
W14 USBDM

AVPPEN0 V13 A_VPPEN0
AVPPEN1 W13 A_VPPEN1
AVCC3EN# T13 A_VCC3EN#
AVCC5EN# R13 A_VCC5EN#

R5C847

CN9
PCMCIA_CON

CDATA3 1 GND
CDATA4 2 D3-CAD0
CDATA5 3 D4-CAD1
CDATA6 4 D5-CAD3
CDATA7 5 D6-CAD5
CE1# 6 D7-CAD7
CADR10 7 CE1#-CC/BE0#
OE# 8 A10-CAD9
CADR11 9 OE#-CAD11
CADR9 10 A11-CAD12
CADR8 11 A9-CAD14
CADR13 12 A8-CC/BE1#
CADR14 13 A13-CPAR
WE# 14 A14-CPERR#
IREQ# 15 WE/PGM-CGNT#
16 RDY/BSY-IRQ/CIN
17 VCC

A_VCC
C420 0.01U
C422 *10U

18 VPP1
CADR16 19 A16-CCLK
CADR15 20 A15-CIRDY#
CADR12 21 A12-CC/BE2#
CADR7 22 A7-CAD18
CADR6 23 A6-CAD20
CADR5 24 A5-CAD21
CADR4 25 A4-CAD22
CADR3 26 A3-CAD23
CADR2 27 A2-CAD24
CADR1 28 A1-CAD25
CADR0 29 A0-CAD26
CDATA0 30 D0-CAD27
CDATA1 31 D1-CAD29
CDATA2 32 D2-RFU
IOIS16# 33 WP/IOIS16-CCLKR
34 GND

GND 69
GND 85
GND 86
GND 87
GND 88

35 GND
CD1# 36 CD1#-CCD1#
CDATA11 37 D11-CAD2
CDATA12 38 D12-CAD4
CDATA13 39 D13-CAD6
CDATA14 40 D14-RFU
CDATA15 41 D15-CAD8
CE2# 42 CE2#-CAD10
VS1 43 VS1#/RFSH-CVS1
IORD# 44 RSVD-CAD13
IOWR# 45 RSVD-CAD15
CADR17 46 A17-CAD16
CADR18 47 A18-RFU
CADR19 48 A19-CBLOCK#
CADR20 49 A20-CSTOP#
CADR21 50 A21-CDEVSEL#
51 VCC

A_VPP
C435 0.01U

CADR22 52 VPP2/VPP2
CADR23 53 A22-CTRDY#
CADR24 54 A23-CFRAME#
CADR25 55 A24-CAD17
VS2 56 A25-CAD19
RESET 57 VS2#/RSVD-CVS2
WAIT# 58 RESET-CRST
INPACK# 59 WAIT#-CSERR#
REG# 60 RSVD-CREQ#
SPKR# 61 REG#-CC/BE3#
CHSTS# 62 BVD2/SP-CAUDIO#
CDATA8 63 BVD1-STSCHG
CDATA9 64 D8-CAD28
CDATA10 65 D9-CAD30
66 D10-CAD31
CD2# 67 CD2#-CCD2#
68 GND

C517 270pF
C389 270pF
C470 0.01U

CN12

MS_DATA2_SD_DAT2 1 SD_DAT2
2 VSS
MS_DATA3_SD_DAT3 3 SD_CD/DAT3
VCC_XD 4 VCC
SD_CLK_MS_CLK_XD-RE# 5 SCLK
MS_BS_SD_CMD_XD_WE# 6 SD_CMD
MS_DATA3_SD_DAT3 7 DATA3
MSCD# 8 INS
9 SD_VSS
MS_DATA2_SD_DAT2 10 DATA2
11 SD_VDD
MS_DATA0_SD_DAT0 12 SDIO/DATA0
MS_DATA1_SD_DAT1 13 DATA1
SD_CLK_MS_CLK_XD-RE# 14 SD_CLK
MS_BS_SD_CMD_XD_WE# 15 BS
16 VSS1
17 SD_VSS1
MS_DATA0_SD_DAT0 18 SD_DAT0
MS_DATA1_SD_DAT1 19 SD-DATA1
SDCD# 20 SD_C/D
21 SD_GND
SD_WP#_XD_R/B# 22 SD_W/P

SHIELD1-GND 23
SHIELD2-GND 24

C693 270P/25V_4
C692 270P/25V_4

R009-031-LR

+3V
VCC_XD
Q27 AO3408L
C704 0.1U
C698 10U/10V
MDIO04
XD_PWON R622 10K +5V
Q28 PDTC144EU

A_VPP
Place near the Slot A VPP pins
C437 10U
C439 *1000P_4
C445 0.1U

A_VCC
Place near the Slot A VCC pins
C421 10U
C428 *1000P_4
C429 0.1U
C433 0.1U

MDIO03 R551 33 SD_WP#_XD_R/B#
MDIO13 R549 33 MS_DATA3_SD_DAT3
MDIO12 R550 33 MS_DATA2_SD_DAT2
MDIO11 R552 33 MS_DATA1_SD_DAT1
MDIO10 R553 33 MS_DATA0_SD_DAT0
MDIO08 R548 33 MS_BS_SD_CMD_XD_WE#
MDIO19 R287 33 XD-ALE
MDIO18 R291 33 XD-CLE
MDIO09 R554 33 SD_CLK_MS_CLK_XD-RE#

C518 *22P/50V_4
EMI

A_VCC
C473 *10U/10V
C474 *0.1U
A_VPP
C508 *10U/10V
C497 *0.1U

Place near the Power IC R5531V pins

3VSUS C457 0.1U
5VSUS C454 0.1U
3VSUS C456 0.1U
5VSUS C455 0.1U
C451 10U/10V

U12

3VSUS 11 VCC3IN
5VSUS 13 VCC5IN1
15 VCC5IN2
6 NC0
AVPPEN1 4 EN1
AVPPEN0 3 EN0
AVCC3EN# 2 VCC3_EN
AVCC5EN# 1 VCC5_EN

VCCOUT1 14
VCCOUT2 12
VCCOUT3 9
A_VCC
VPPOUT 8
A_VPP
NC1 10
NC2 7
FLG 5
GND 16

Not-Support 12V

R5531V002

VCC_ROUT
3VSUS
3VSUS
C460 10U/10V
C467 0.01U

3VSUS
C446 10U/10V
C462 0.1U
C459 0.01U

R284 10K R7

U10C

R6 E13
L1 E14
A4

VCC_RIN1
VCC_RIN2
VCC_ROUT1
VCC_ROUT2
VCC_MD3V
REGEN#

SD_CD#/MDIO0 B1 MDIO00
MS_CD#/MDIO1 A2 MDIO01
MDIO2 A3 MDIO02 T20
SD_WP/MDIO3 B3 MDIO03
SD/MS_PWR0/MDIO4 B4 MDIO04
SD_PWR1/MDIO5 A5 MDIO05
SD/MS_LED#/MDIO6 B5 MDIO06 T18
SD/MS_EXTCLK_MDIO7 D5 MDIO07 T19
SD_CMD/MS_BS/MDIO8 A6 MDIO08
SD/MS_CLK/MDIO9 B6 MDIO09
SD/MS_DAT0/MDIO10 D6 MDIO10
SD/MS_DAT1/MDIO11 E6 MDIO11
SD/MS_DAT2/MDIO12 A7 MDIO12
SD/MS_DAT3/MDIO13 B7 MDIO13 T36
MDIO14 D7 MDIO14
MDIO15 E7 MDIO15 T37
MDIO16 A8 MDIO16 T17
MDIO17 B8 MDIO17 T16
MDIO18 D8 MDIO18
MDIO19 E8 MDIO19

R5C847

MDIO00 SDCD#
MDIO01 MSCD#
C499 *270pF
C500 *270pF

VCC_XD
C690 .1U/10V
C689 .1U/10V
C691 .1U/10V

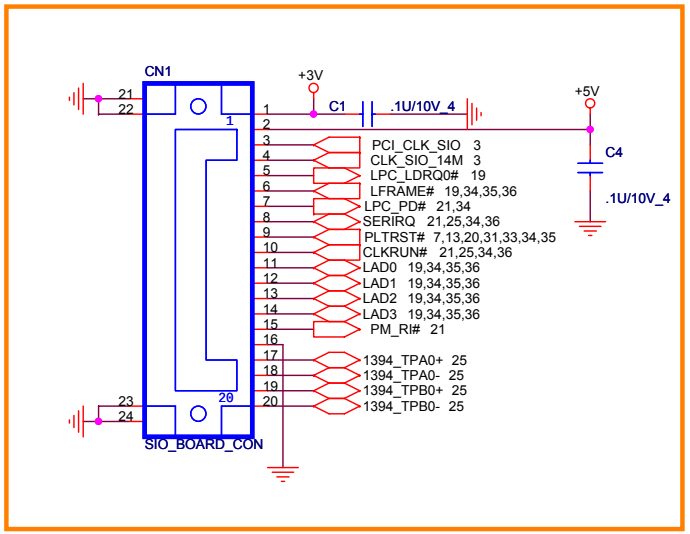
VCC_XD
C706 2.2U/6.3V
R566 150K

VCC_ROUT
C488 0.01U
C489 0.01U
C415 0.47U
C405 0.47U

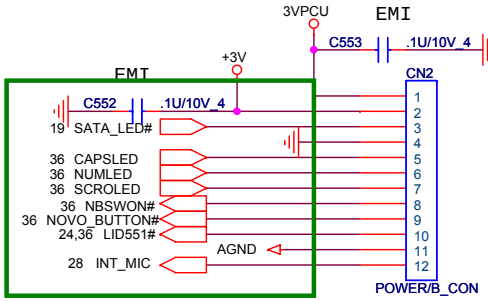
PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	R5C847 PCMCIA/ 3-IN-1 CON	1A
Date: Thursday, June 12, 2008	Sheet 26 of 45	

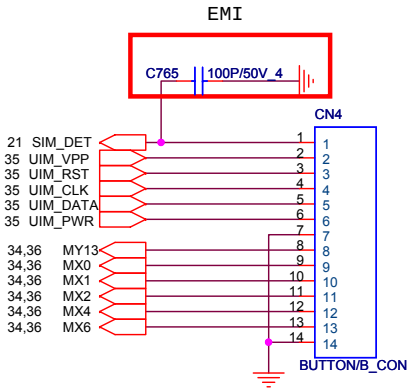
SIO BOARD



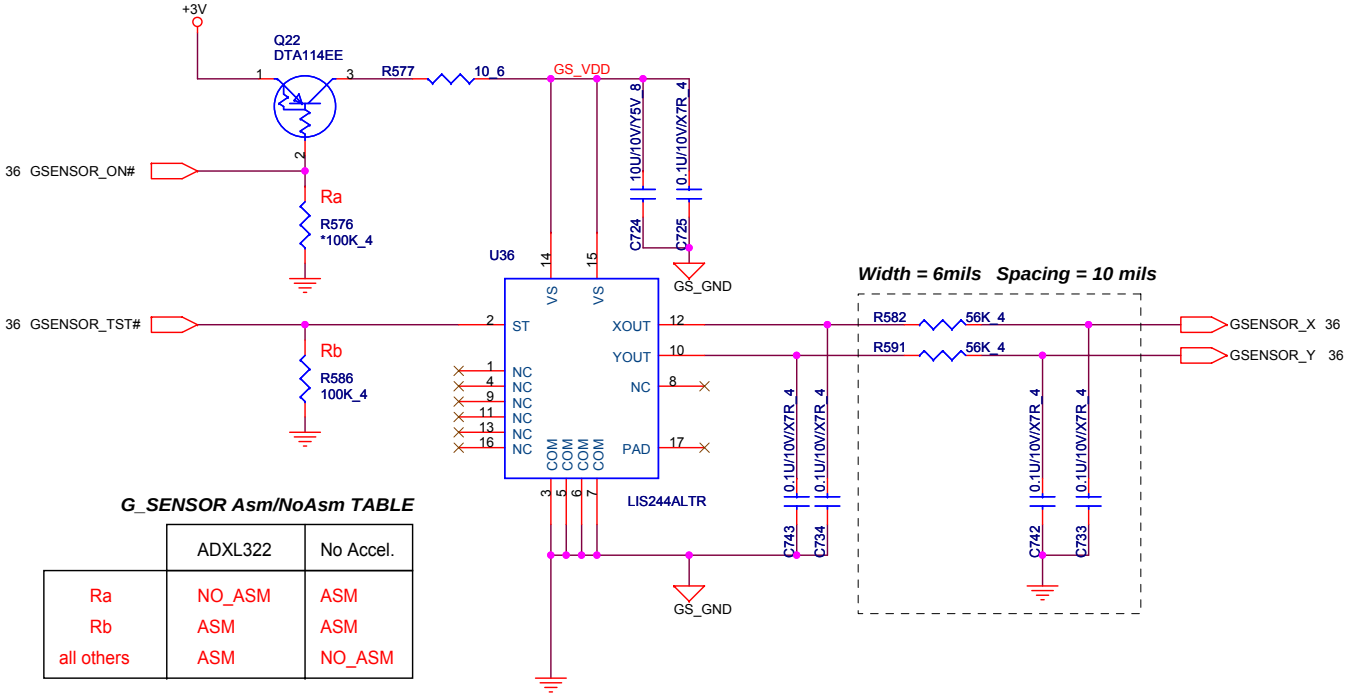
POWER BOARD



BUTTON BOARD



G-SENSOR

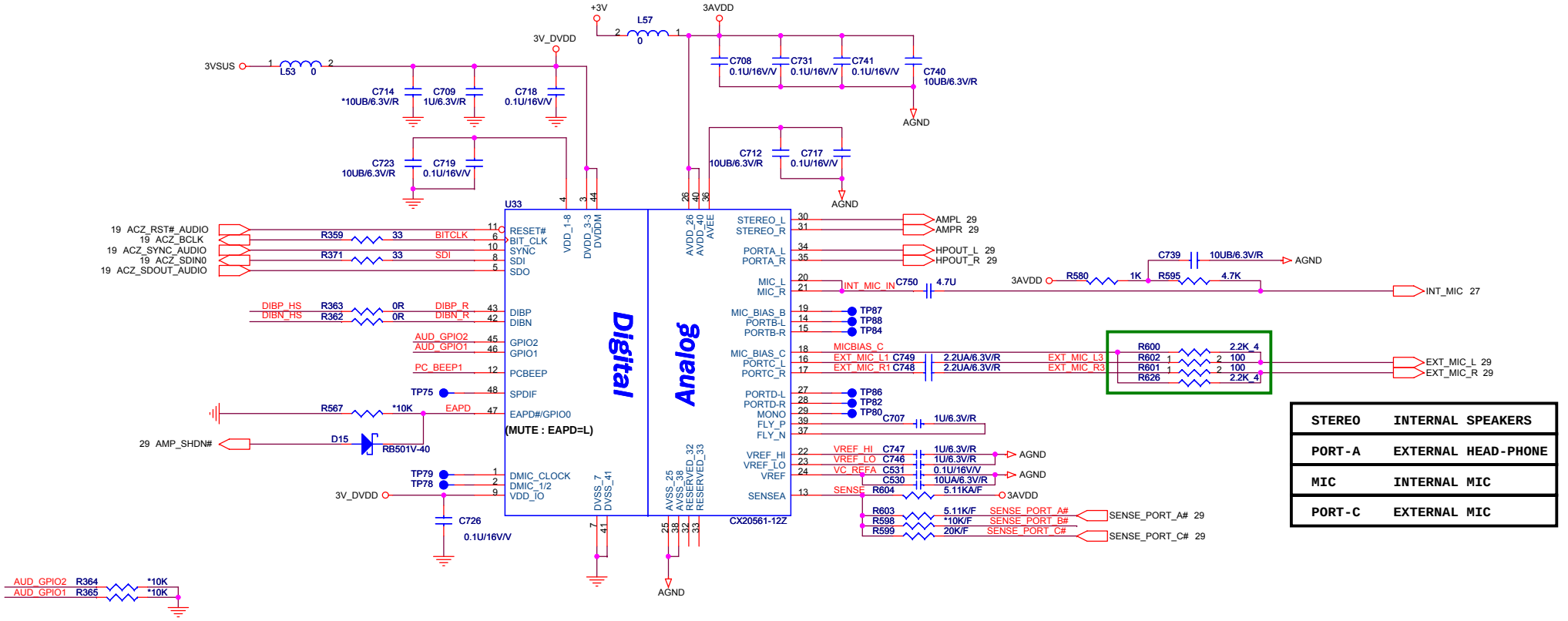


G_SENSOR Asm/NoAsm TABLE

	ADXL322	No Accel.
Ra	NO_ASM	ASM
Rb	ASM	ASM
all others	ASM	NO_ASM

PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	T/Bs & G-SENSOR	1A
Date: Thursday, June 12, 2008	Sheet 27 of 45	

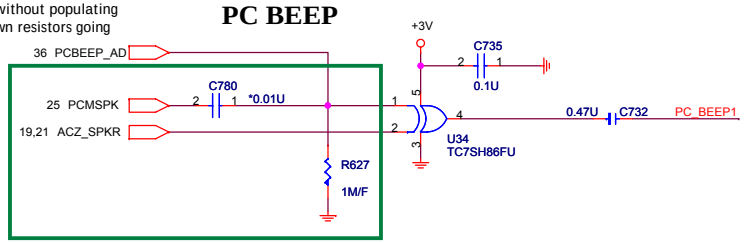


STEREO	INTERNAL SPEAKERS
PORT-A	EXTERNAL HEAD-PHONE
MIC	INTERNAL MIC
PORT-C	EXTERNAL MIC

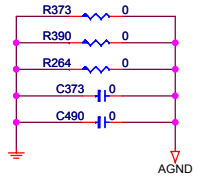
GAIN	10K GPIO RESISTORS GPIO1	GPIO2
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-16dB	Omit	Populate

Default gain is -6dB without populating the 10K ohm pull down resistors going to GPIO1 and GPIO2

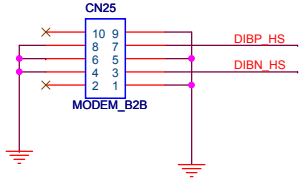
PC BEEP



FOR EMI SOLUTION



MODEM/B CONN.



PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AUDIO CODEC+MODEM	1A

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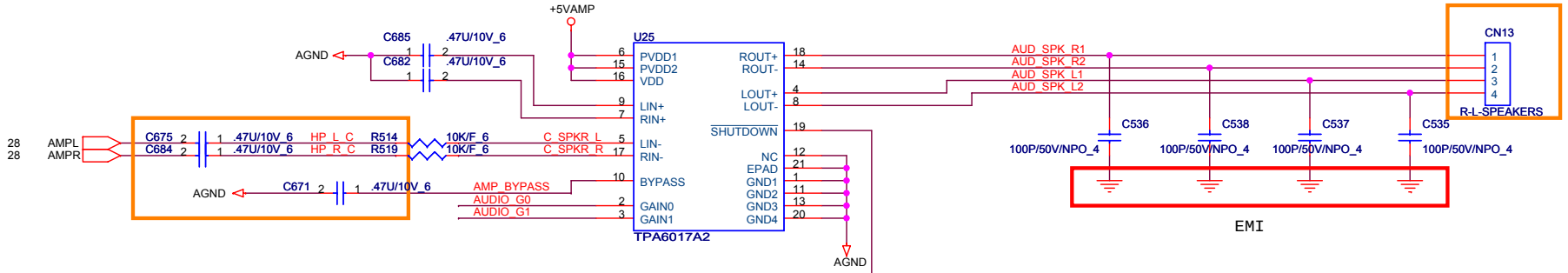
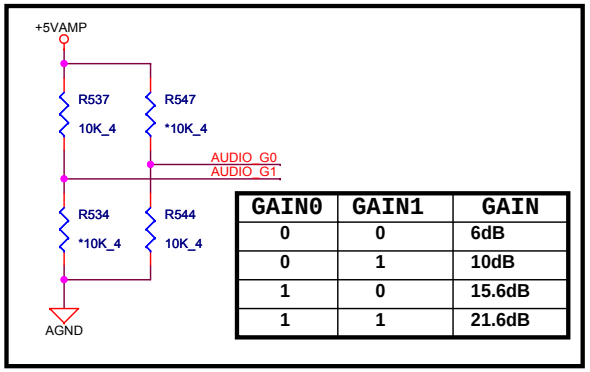
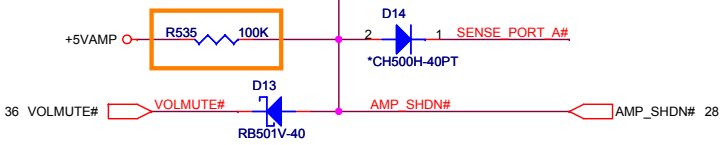
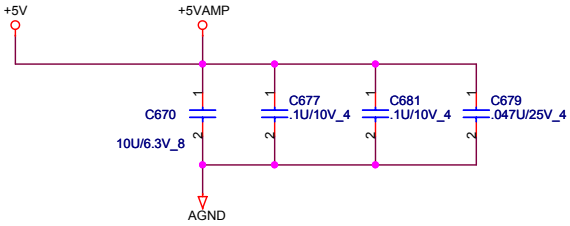
INTERNAL SPEAKER AMPLIFIER



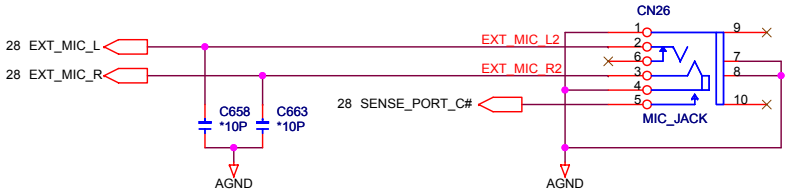


GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

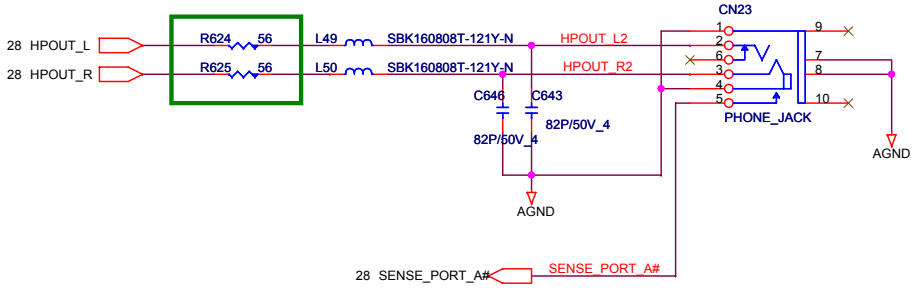




MIC-IN JACK



HEADPHONE



PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP_TPA6017 & JACKS	1A

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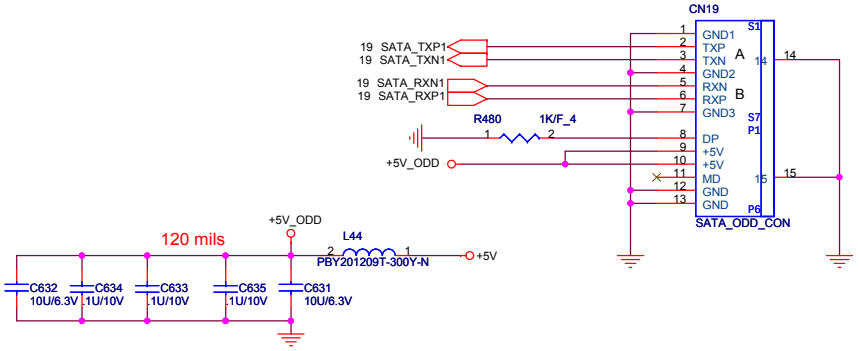
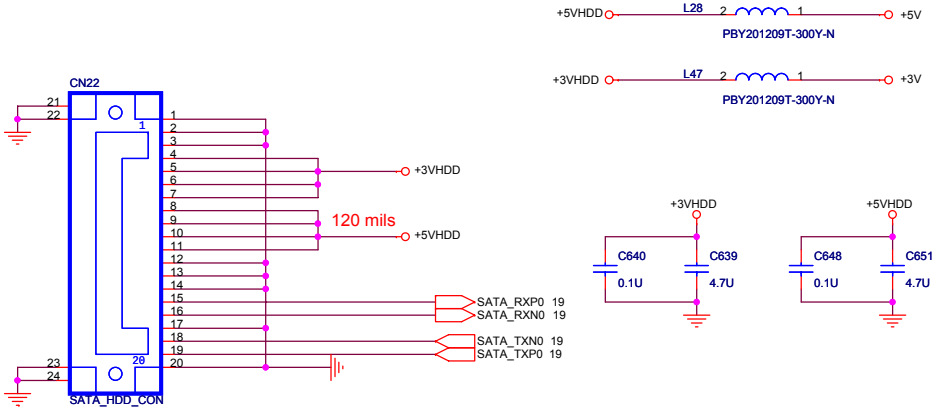
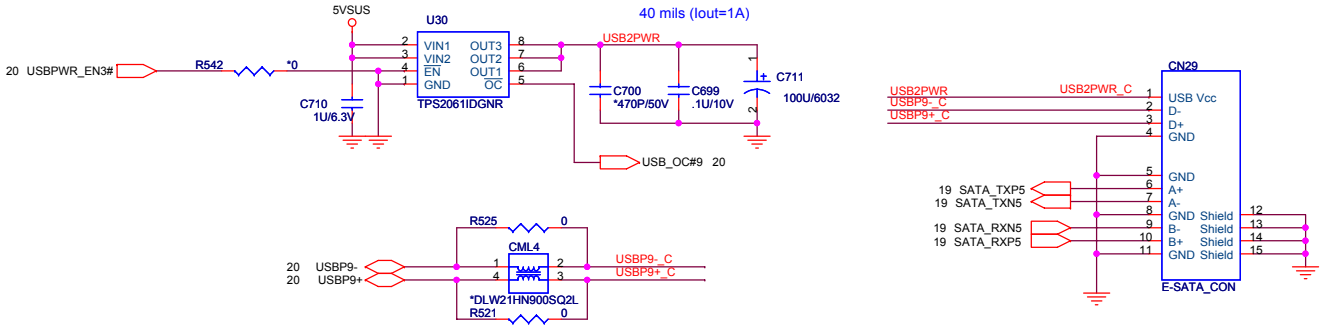
SATA CD-ROM



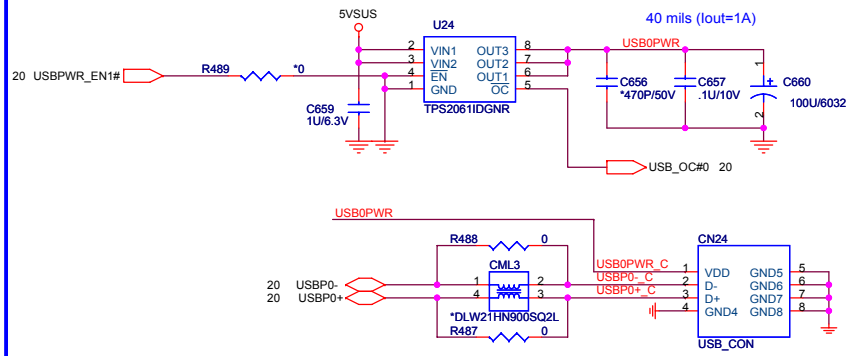
SATA-HDD CONNECTOR

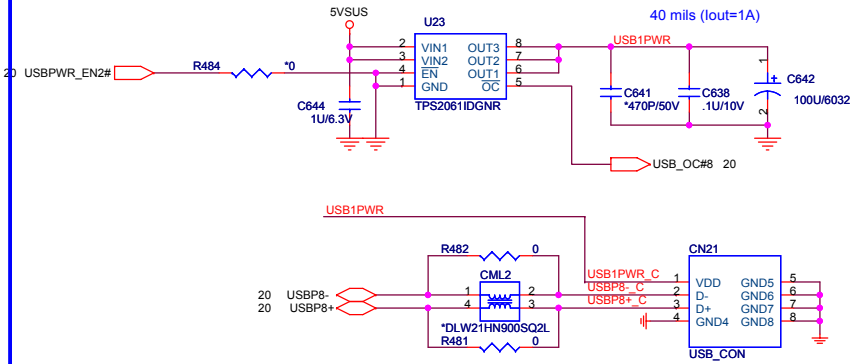


USB + eSATA CONNECTOR



USBX2





PROJECT : LE8		
Quanta Computer Inc.		
Size: Custom	Document Number: SATA HDD/CD-ROM/USB/ESATA	Rev: 1A
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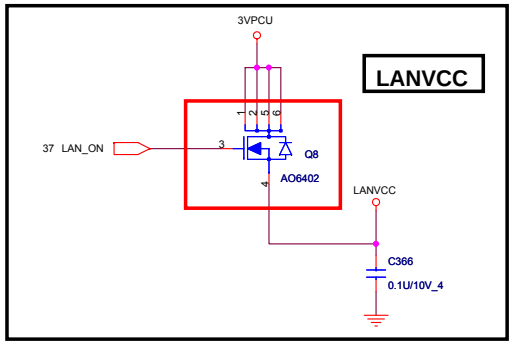

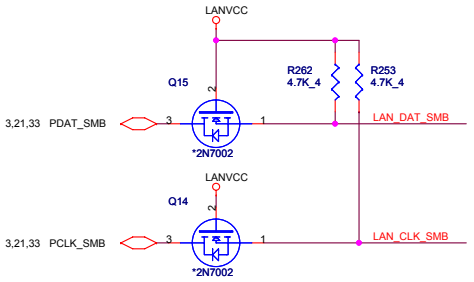

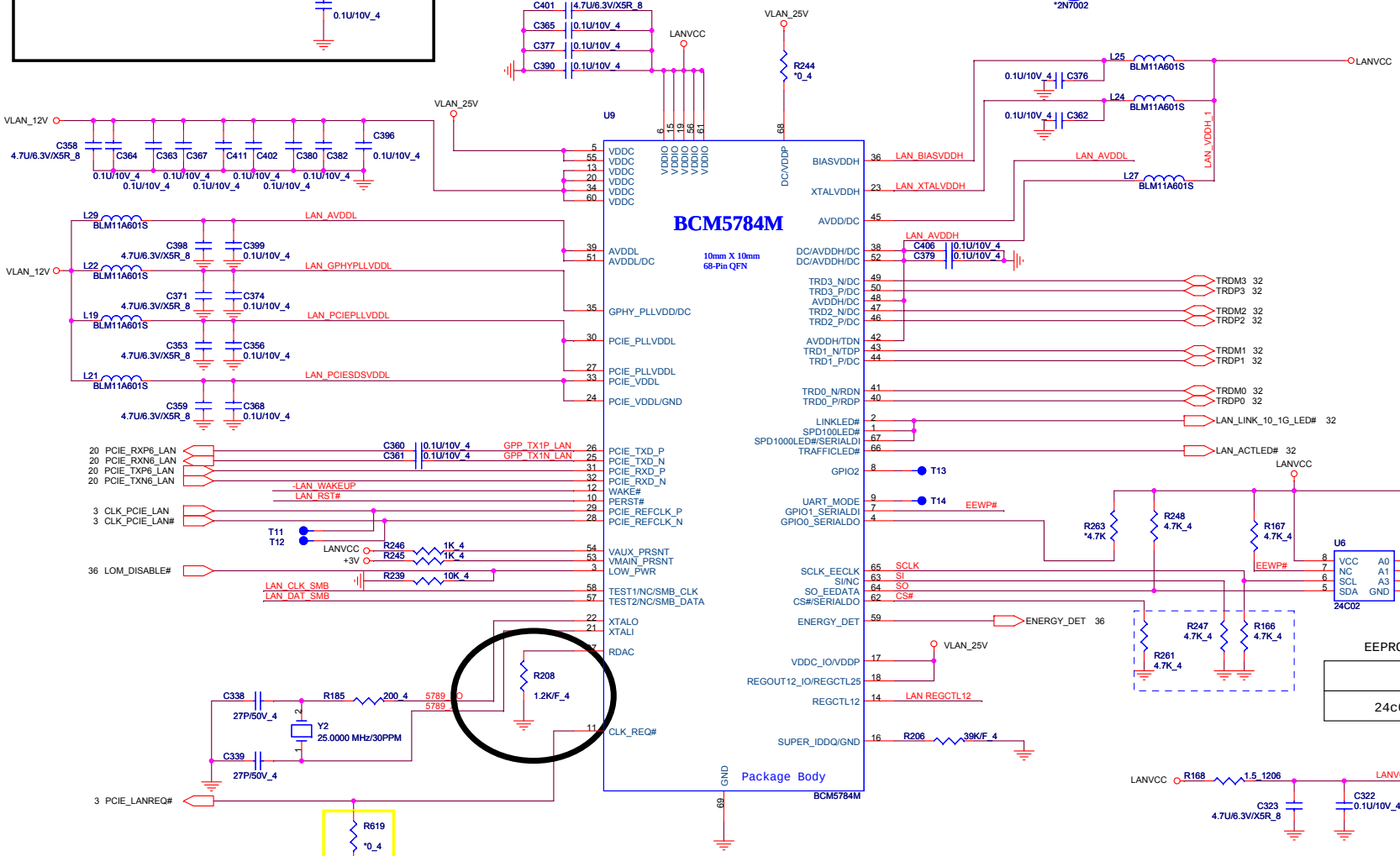

EEPROM Strapping

	SO	SI	CS#	SCLK
24c02	1	0	0	0

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN-BCM5784M	1A

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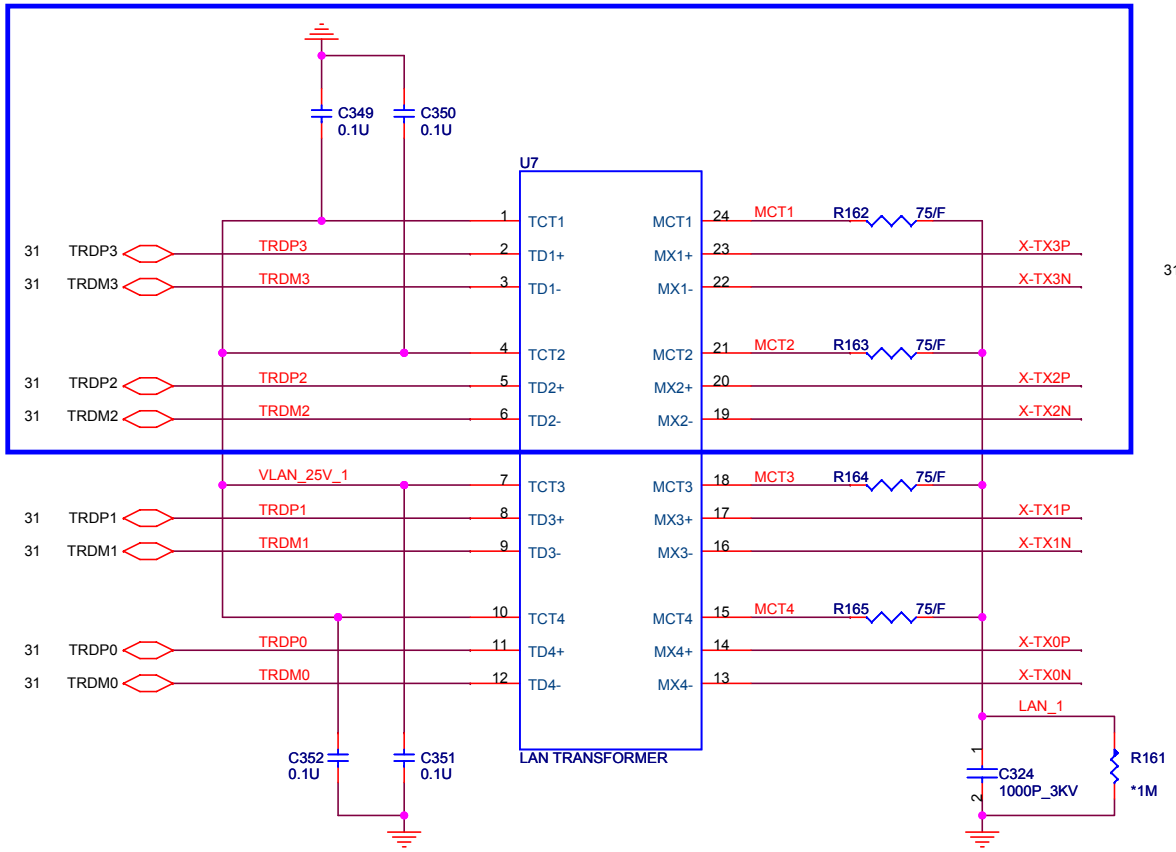

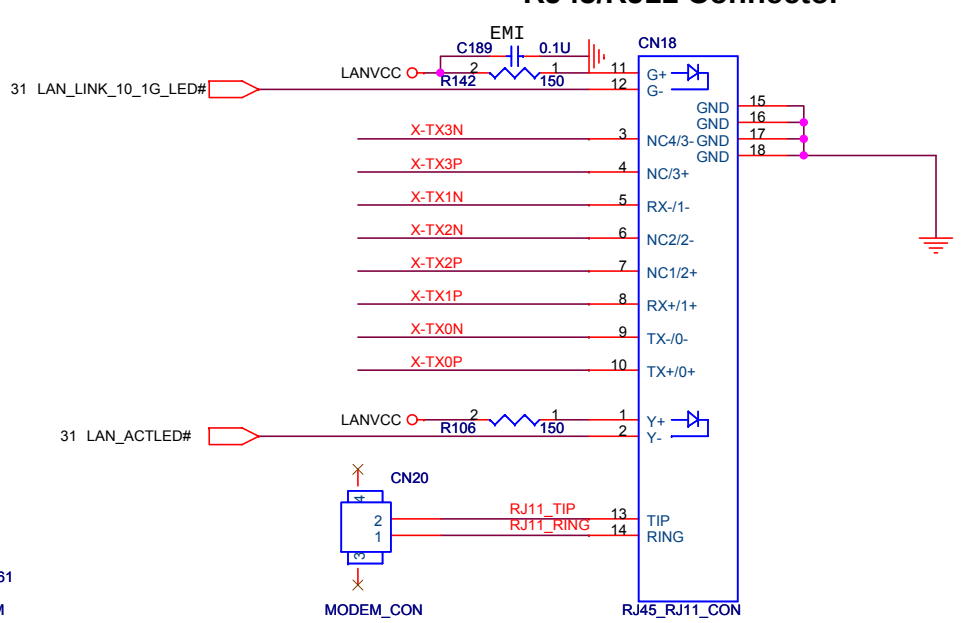

PROJECT : LE8		
Quanta Computer Inc.		
Size: Custom	Document Number: RJ11/RJ45 CONNECTOR	Rev: 1A
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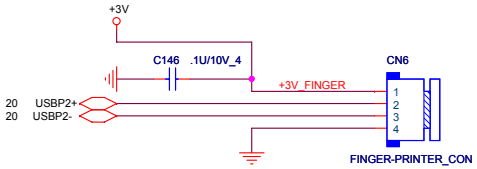
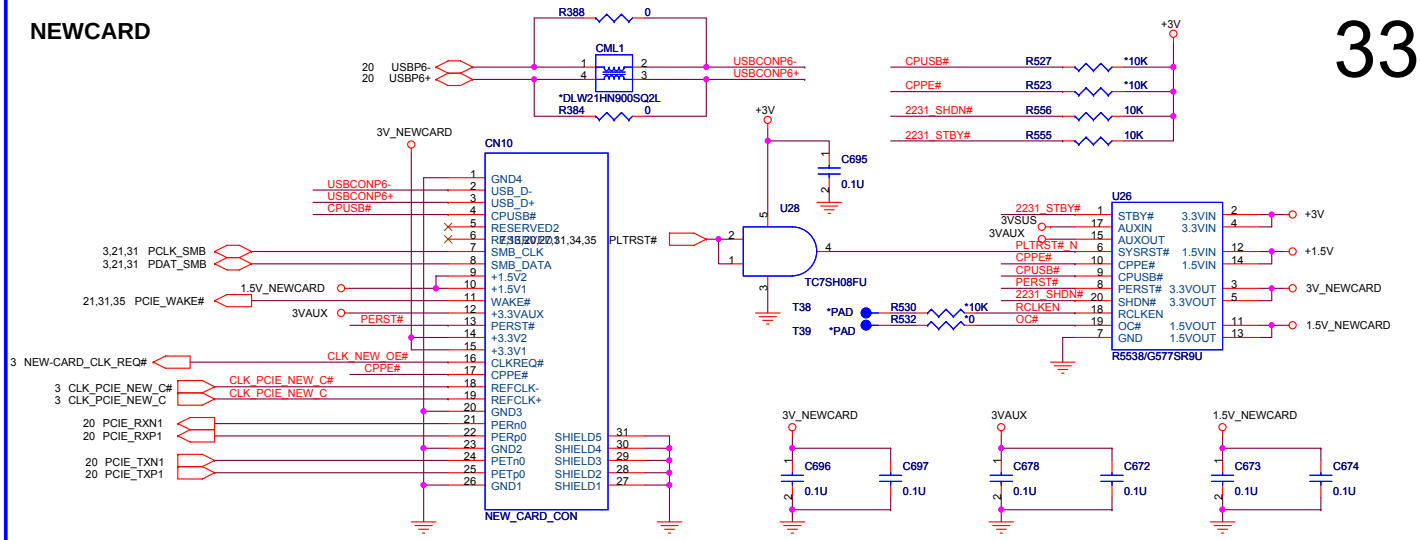
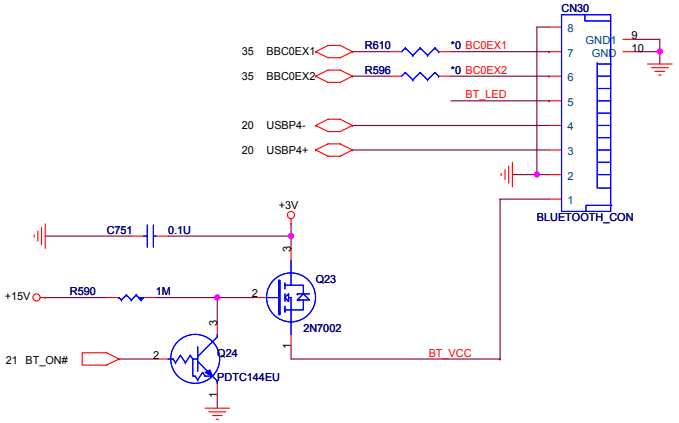
FINGER PRINTER



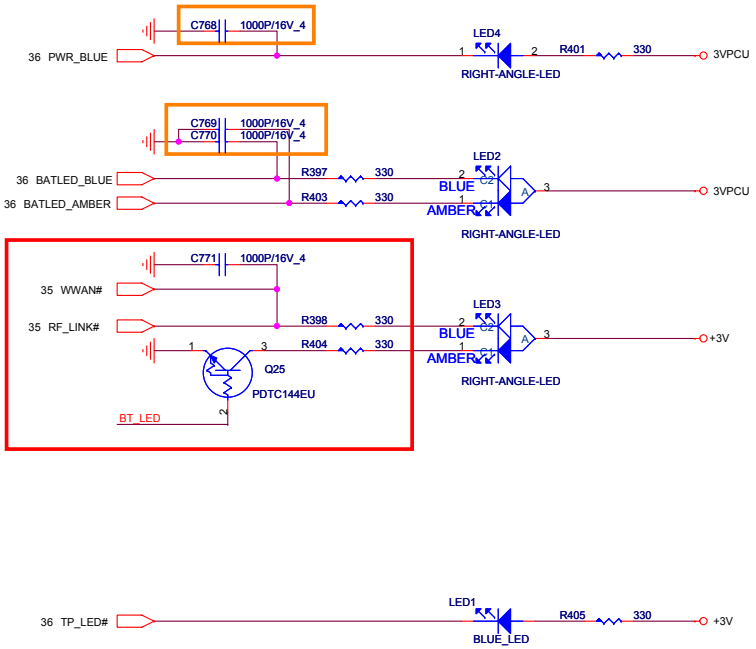
NEWCARD



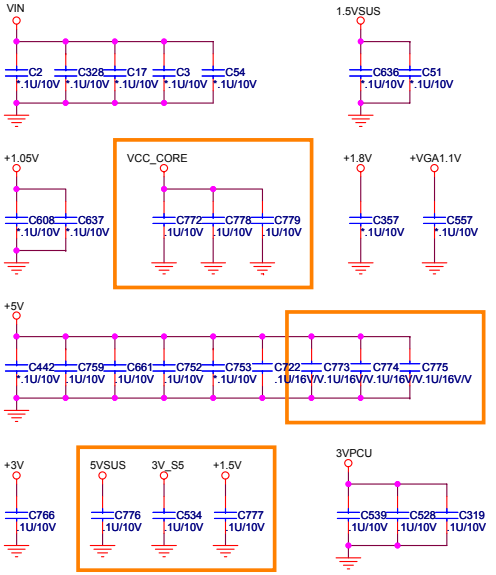
BLUETOOTH



LED



EMI CAPACITORS



PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	F/P, NEW CARD, B/T, LED	1A
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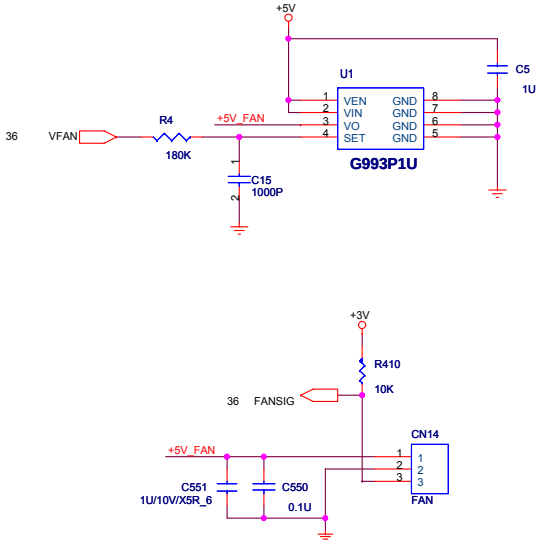
FAN CONTROL



EMI PAD

PAD14 *MDC_SPRING

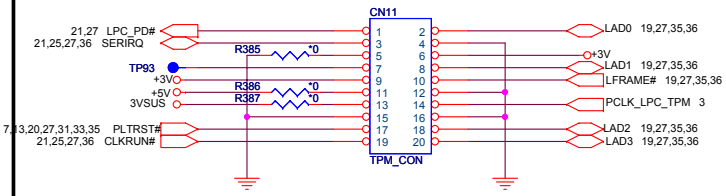
Springs

PAD3 *MDC_SPRING
PAD4 MDC_SPRING
PAD7 *MDC_SPRING
PAD8 *MDC_SPRING
PAD6 MDC_SPRING
PAD5 MDC_SPRING
PAD9 *MDC_SPRING
PAD10 *MDC_SPRING
PAD12 MDC_SPRING
PAD13 MDC_SPRING
PAD15 MDC_SPRING
PAD1 ANT_SPRING
PAD2 *ANT_SPRING
PAD11 *ANT_SPRING

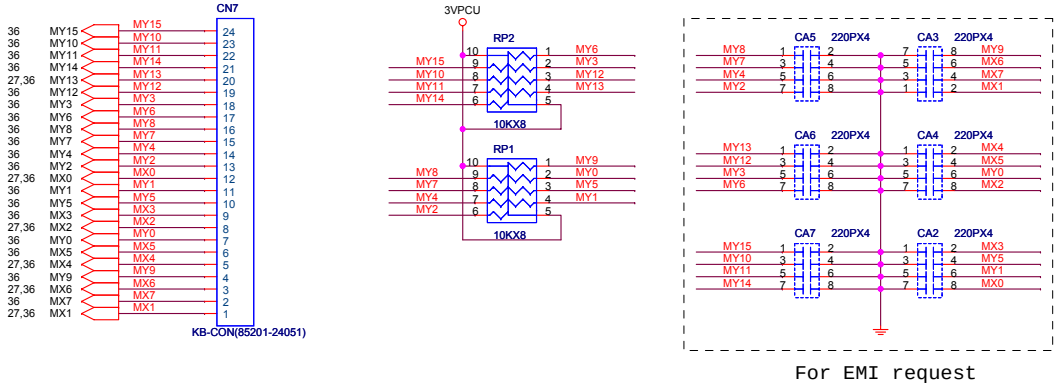
HOLES

H1 *HOLE
H13 *HOLE
H12 *HOLE
H11 *HOLE
AGND
H14 *HOLE
H4 *HOLE
H2 *HOLE
H15 HOLE
THER_GND
H5 *HOLE
H6 *HOLE
H17 *HOLE
H19 HOLE
H29 *HOLE
H22 HOLE
H23 HOLE
H20 HOLE
H16 *HOLE
H26 *HOLE
H18 HOLE
H21 HOLE
H3 *HOLE
H30 *HOLE
H31 *HOLE
H28 HOLE
H9 HOLE
H8 HOLE
H32 *HOLE
H33 *HOLE

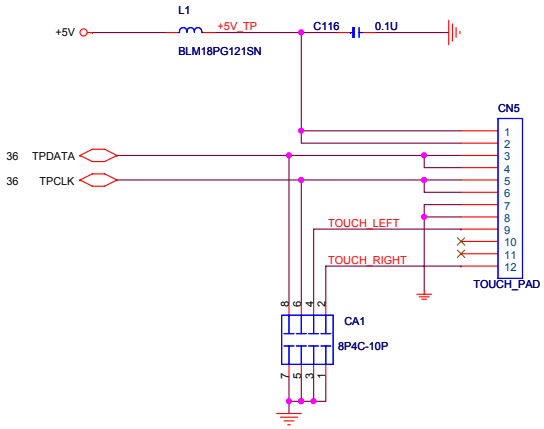
Board TO Board TPM MODULE



KEYBOARD



TOUCH PAD



PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	FAN, TPM, K/B, T/P	1A

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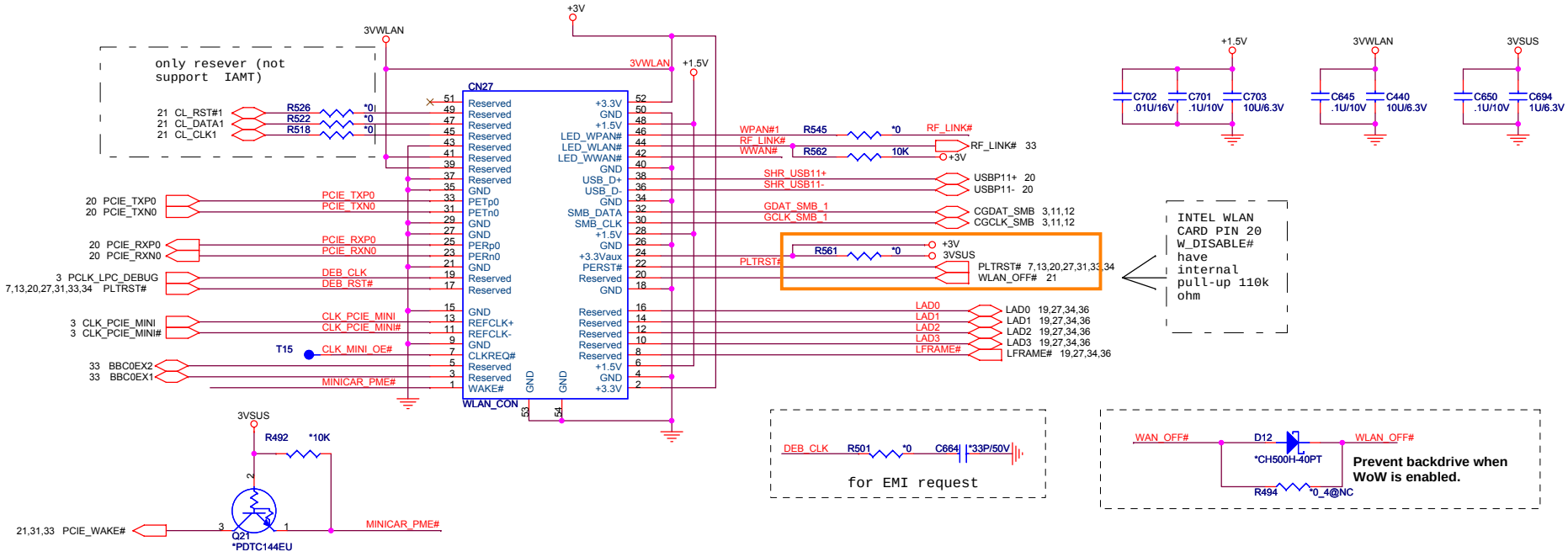
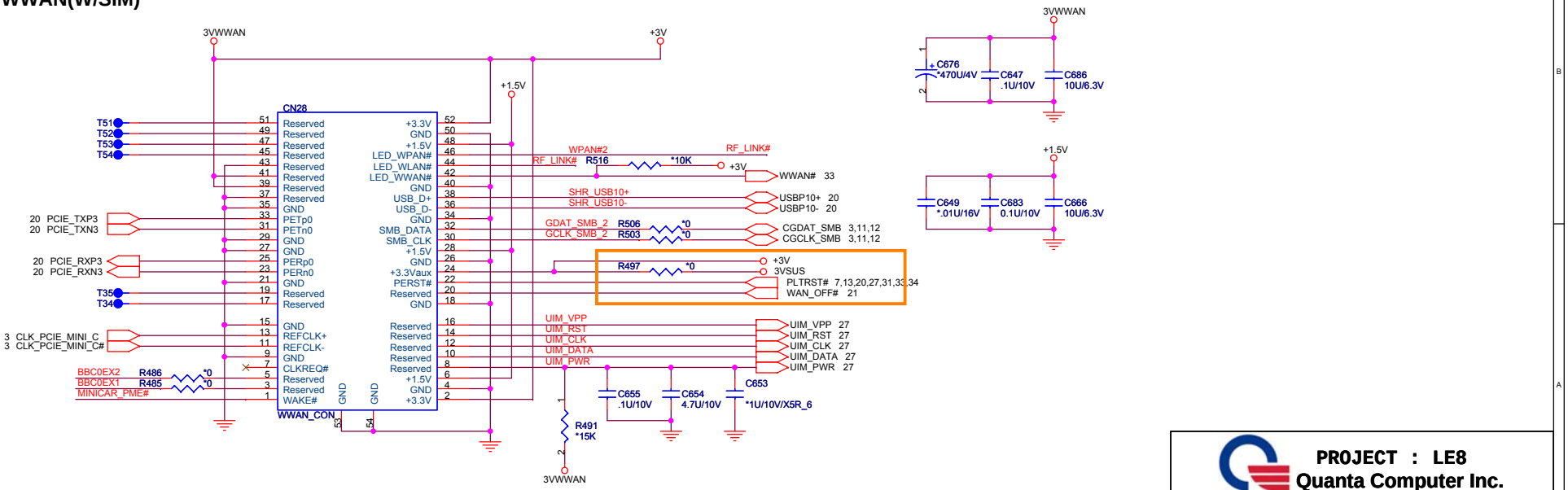
Mini PCI-E Card 1
WLAN



Mini PCI-E Card 2
WWAN(W/SIM)



PROJECT : LE8			
Quanta Computer Inc.			
Size: Custom	Document Number: WLAN & WWAN CON		Rev: 1A
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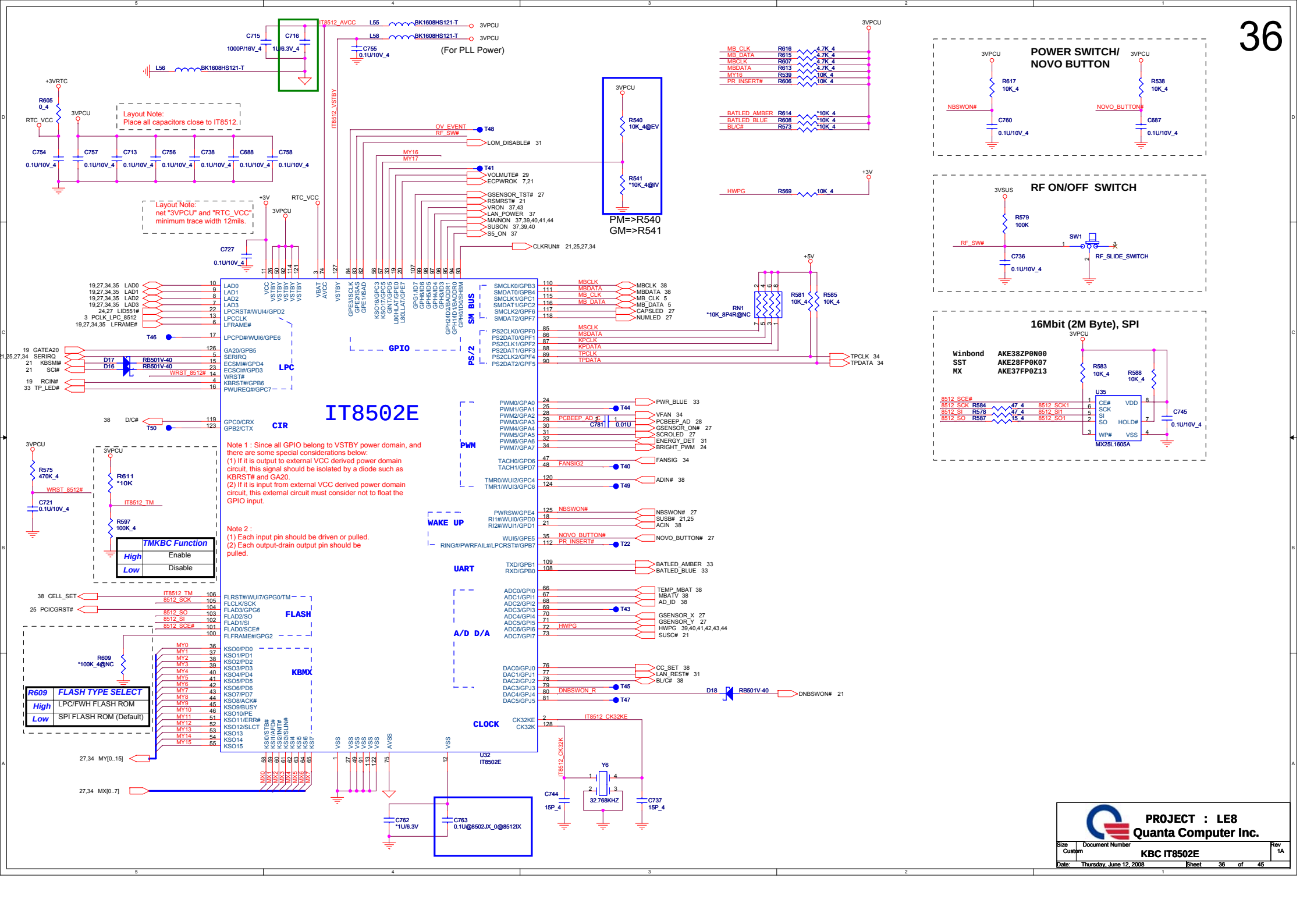
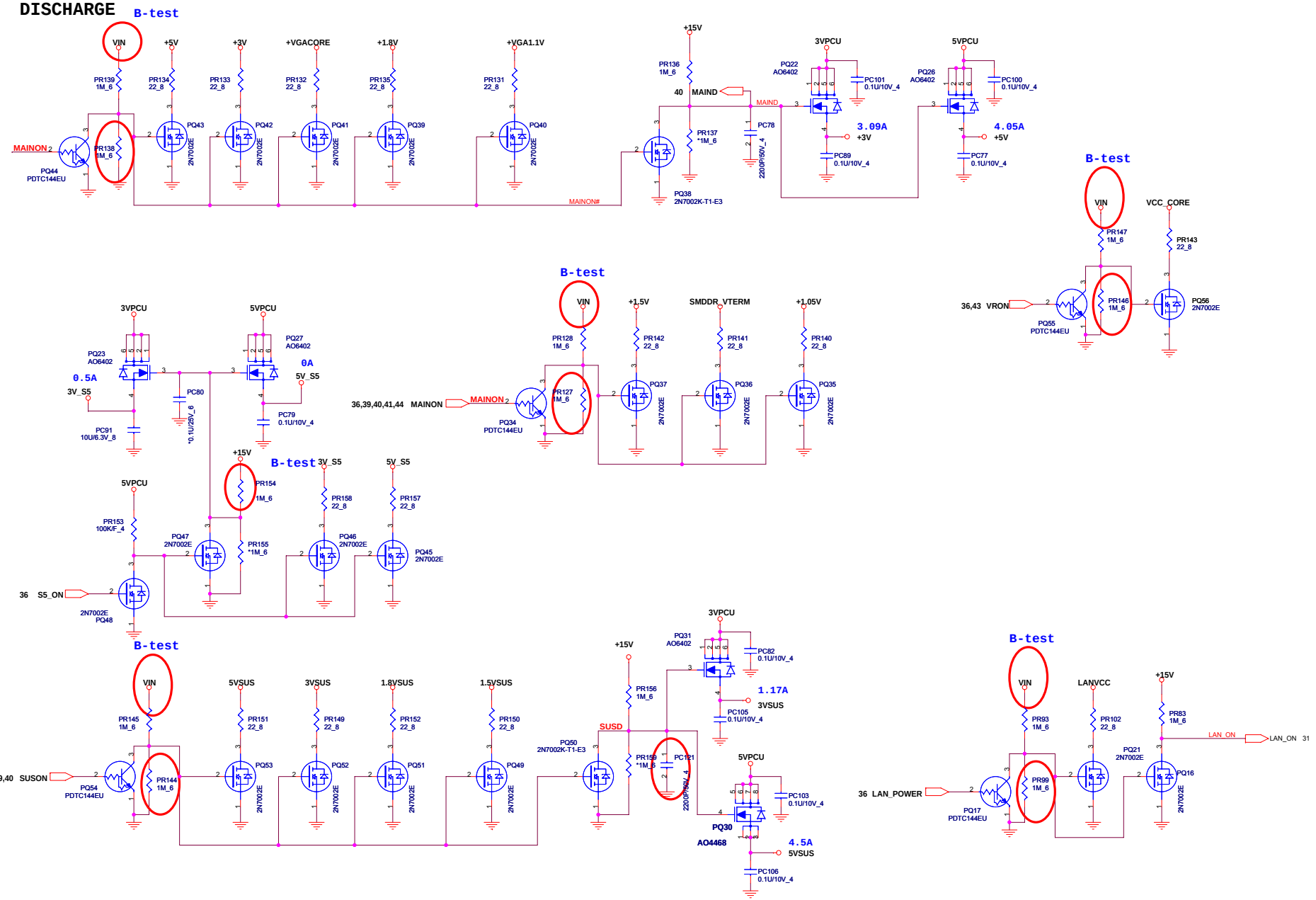

IT8502E
(For PLL Power)
Layout Note:
Place all capacitors close to IT8512.
Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.
PM=>R540
GM=>R541
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.
Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.
TMKBC Function
High Enable
Low Disable
R609 FLASH TYPE SELECT
High LPC/FWH FLASH ROM
Low SPI FLASH ROM (Default)
GPIO
LPC
CIR
SM BUS
PS/2
PWM
WAKE UP
UART
A/D D/A
FLASH
KBMX
CLOCK
POWER SWITCH/
NOVO BUTTON
RF ON/OFF SWITCH
16Mbit (2M Byte), SPI
Winbond AKE38ZP0N00
SST AKE28FP0K07
MX AKE37FP0Z13
PROJECT : LE8
Quanta Computer Inc.
KBC IT8502E
Thursday, June 12, 2008

DISCHARGE



PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discharge	1A

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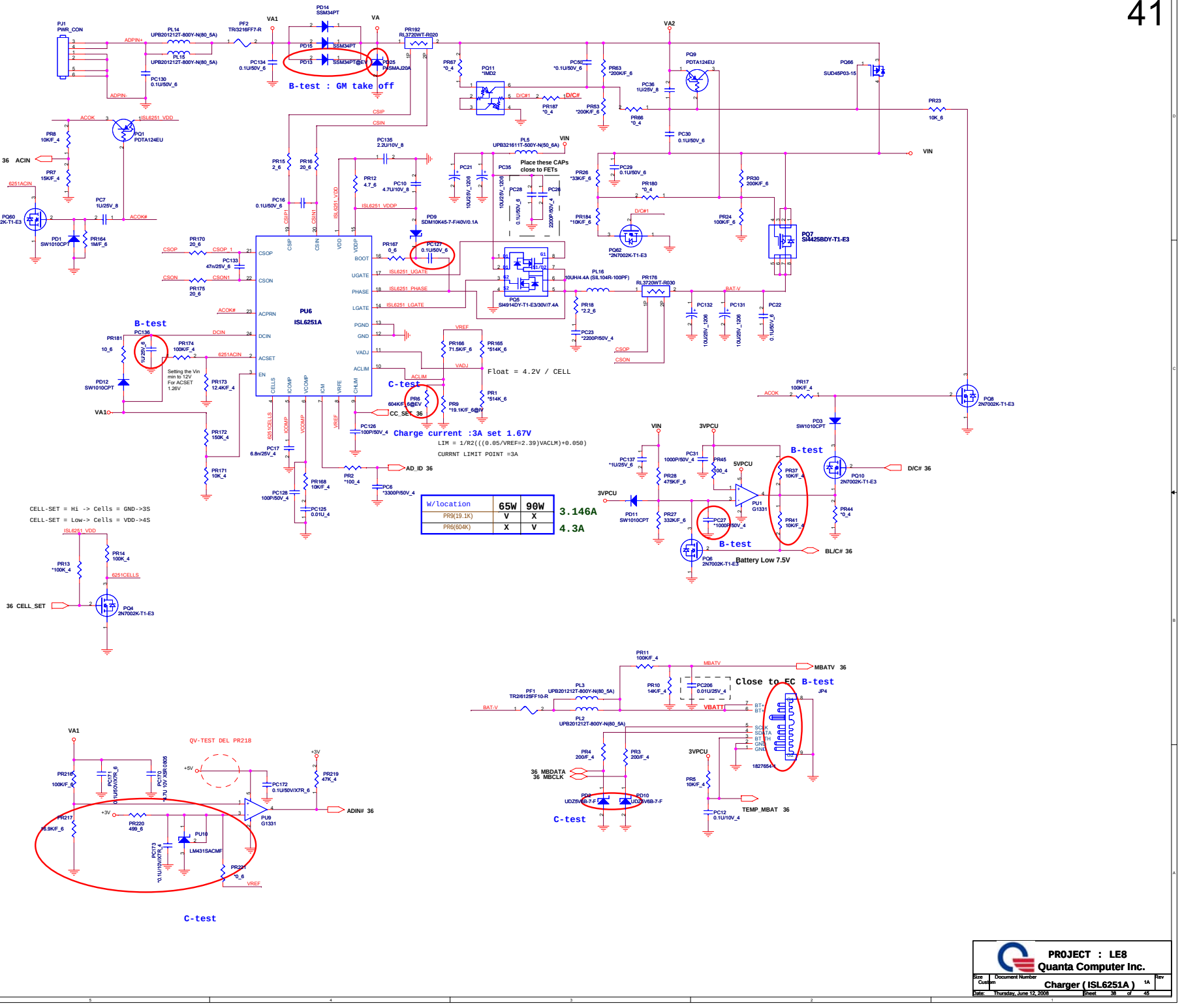
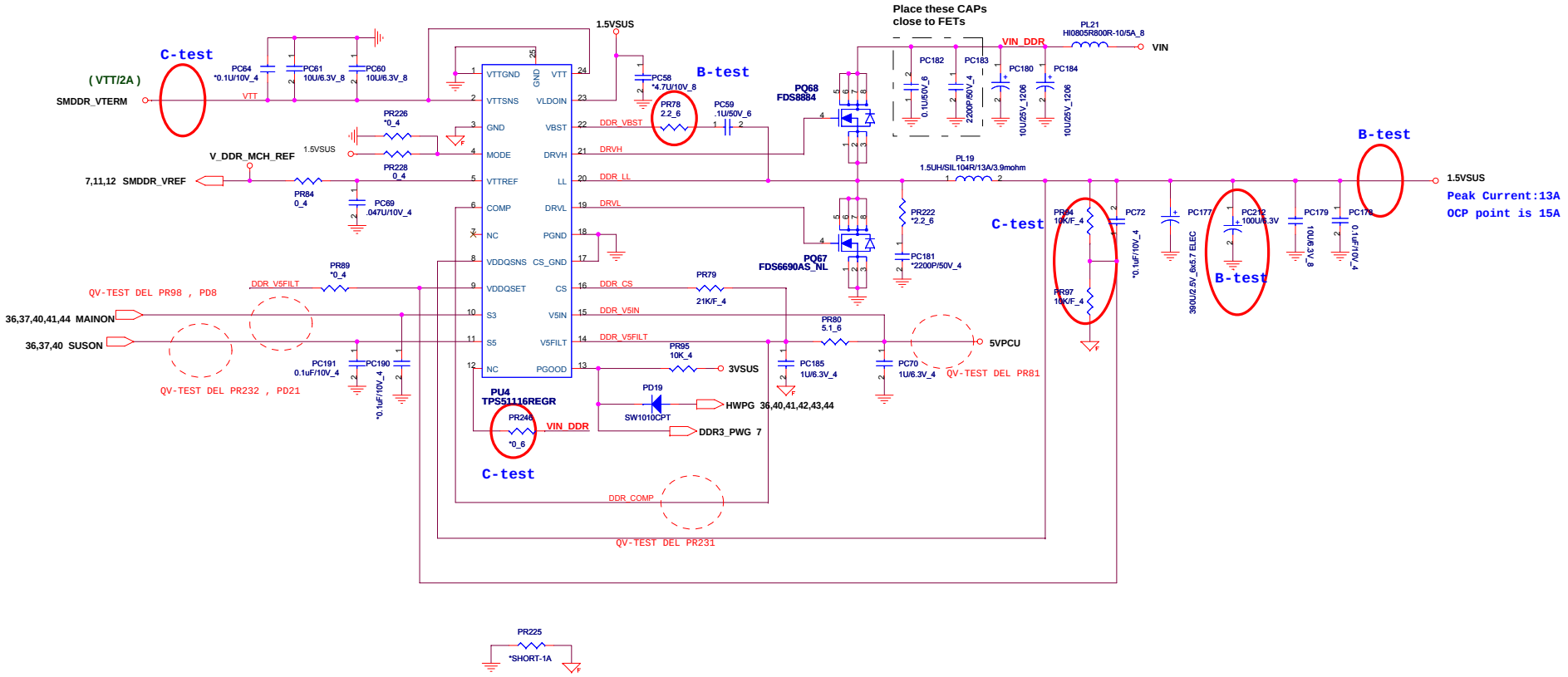

PU6
ISL6251A
B-test : GM take off
B-test
C-test
Charge current :3A set 1.67V
LIM = 1/R2(((0.05/VREF=2.39)VACLM)+0.050)
CURRNT LIMIT POINT =3A
Float = 4.2V / CELL
Place these CAPs close to FETs
Setting the Vin min to 12V For ACSET 1.26V
CELL-SET = Hi -> Cells = GND->3S
CELL-SET = Low-> Cells = VDD->4S
QV-TEST DEL PR218
Close to EC B-test
Battery Low 7.5V
W/location | 65W | 90W
PR9(19.1K) | V | X
PR6(604K) | X | V
3.146A
4.3A
PROJECT : LE8
Quanta Computer Inc.
Charger (ISL6251A)
Thursday, June 12, 2008



PROJECT : LE8			
Quanta Computer Inc.			
Size: Custom	Document Number: DDR3(TPS51116PEGR)		Rev: 1A
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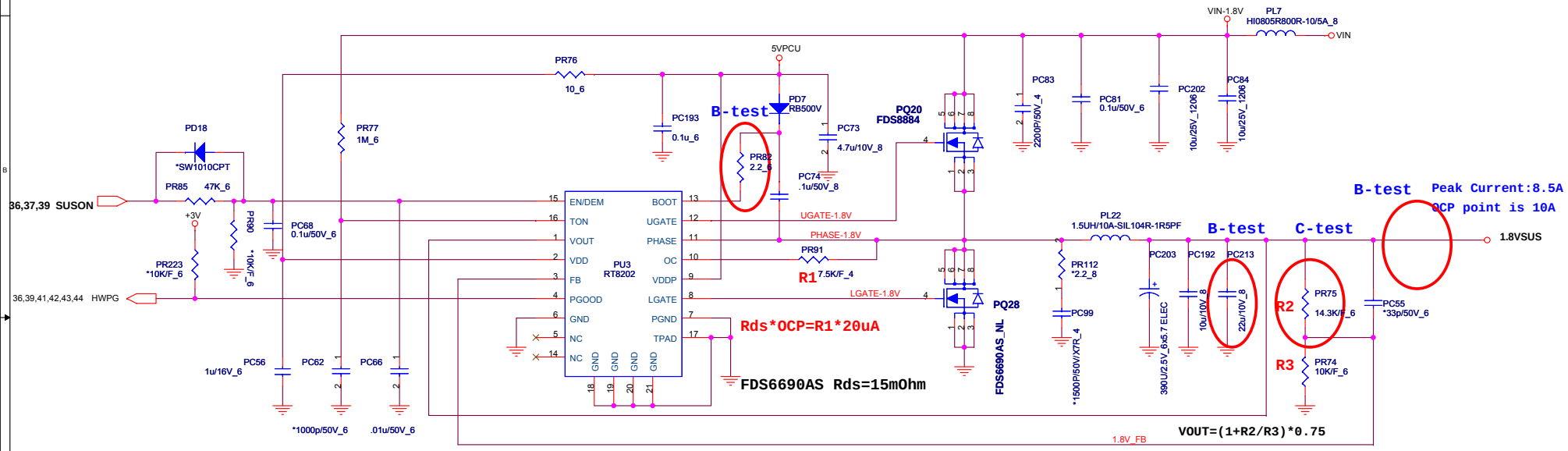
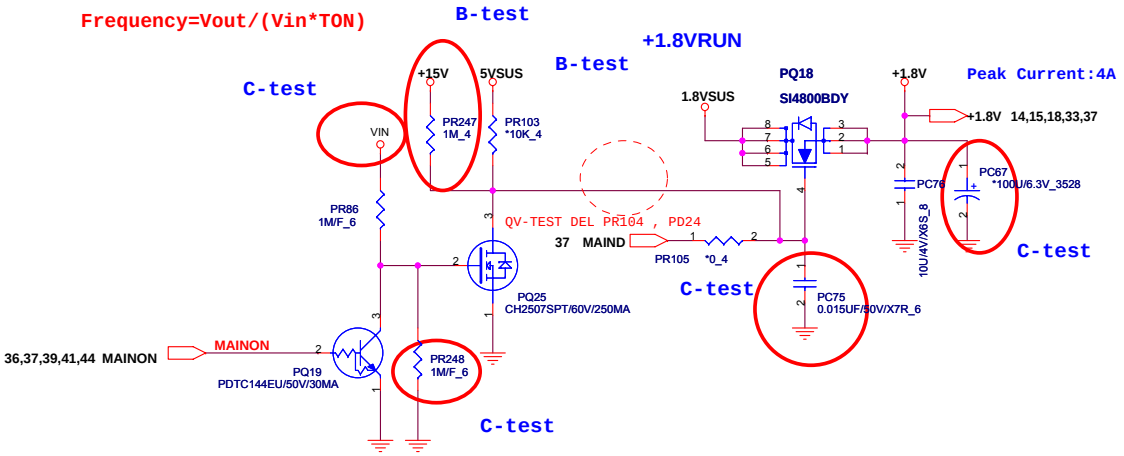


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)



PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.8VSUS(RT8202)	1A
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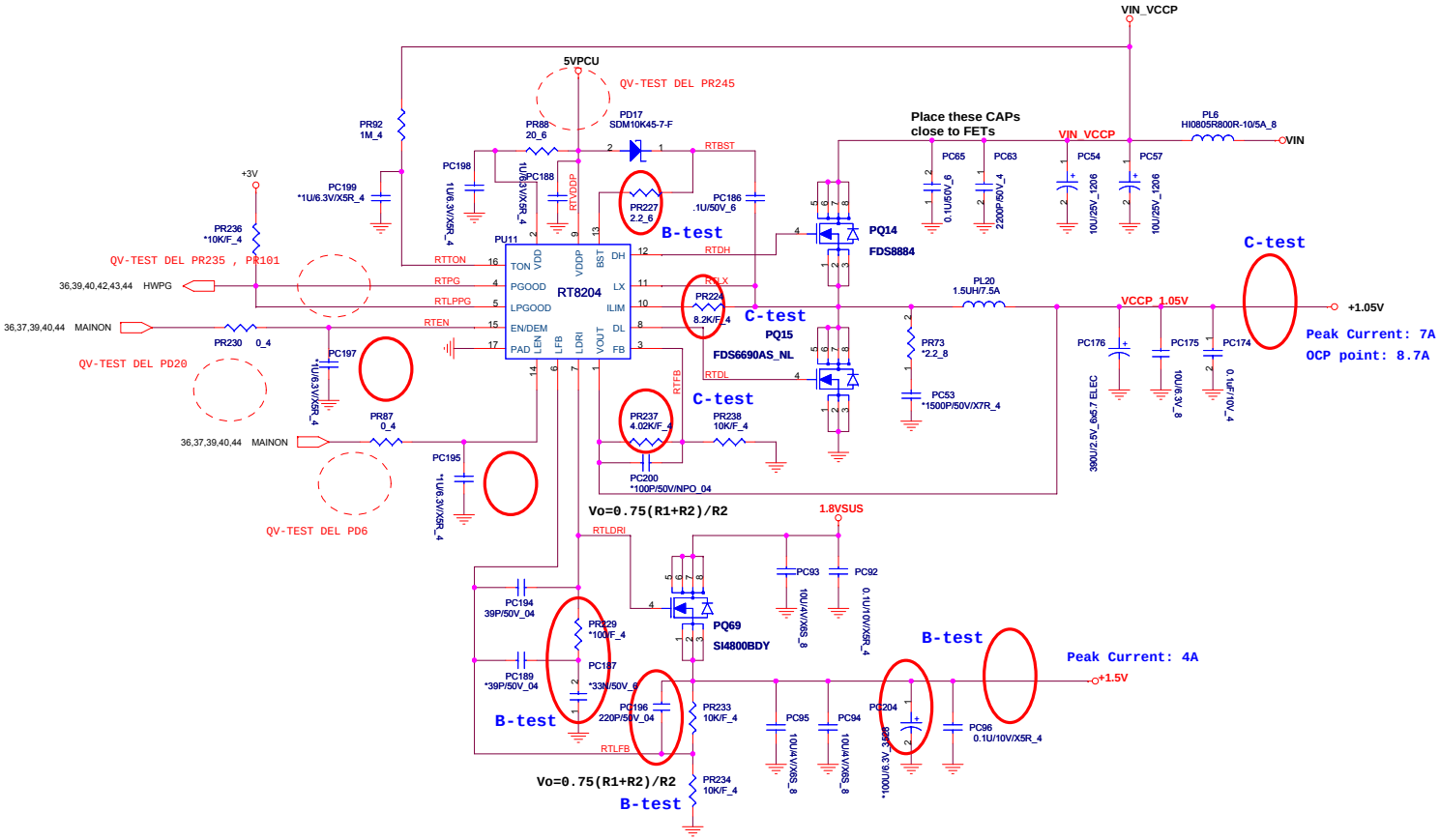

PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.05V/1.5V (RT8204)	1A

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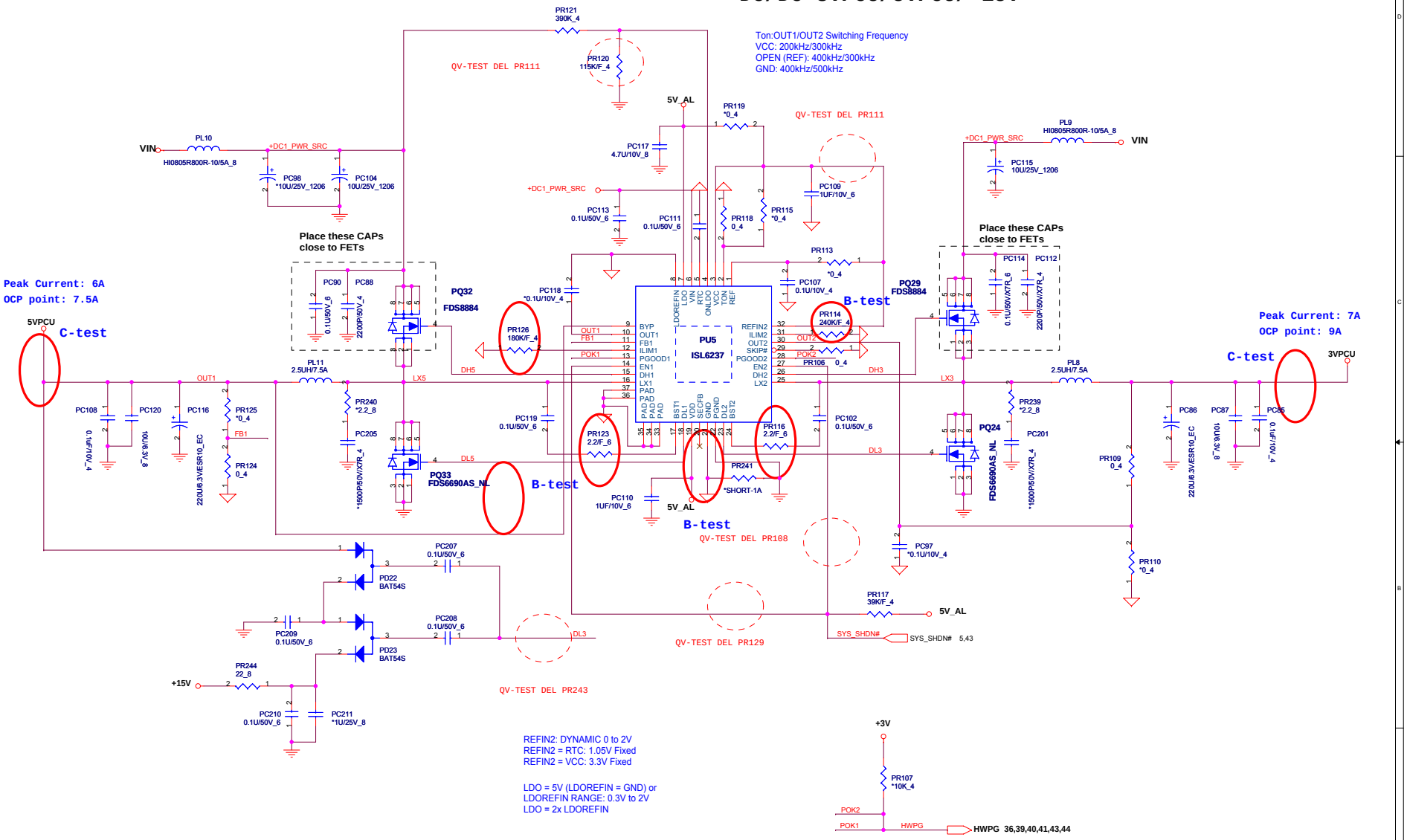
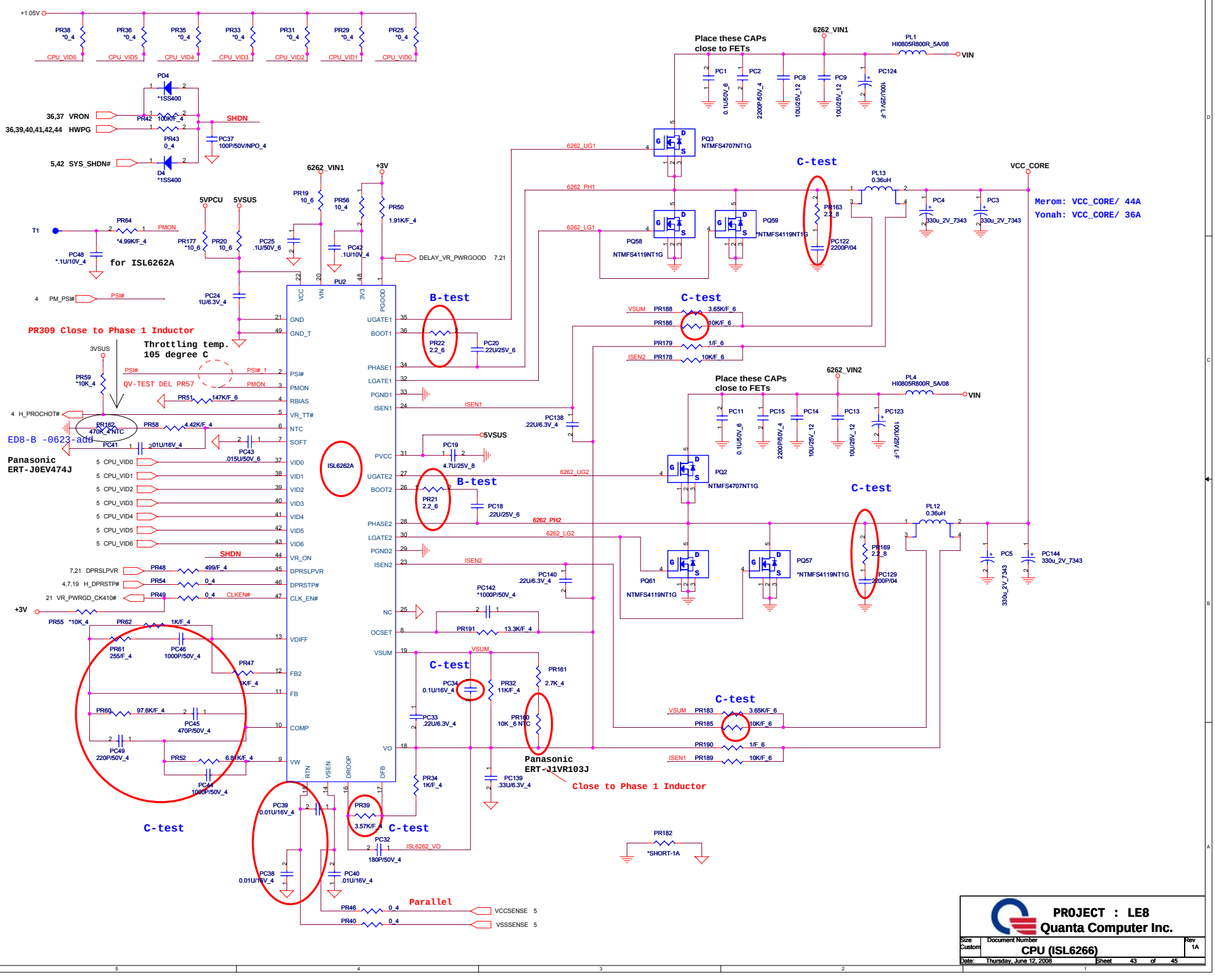
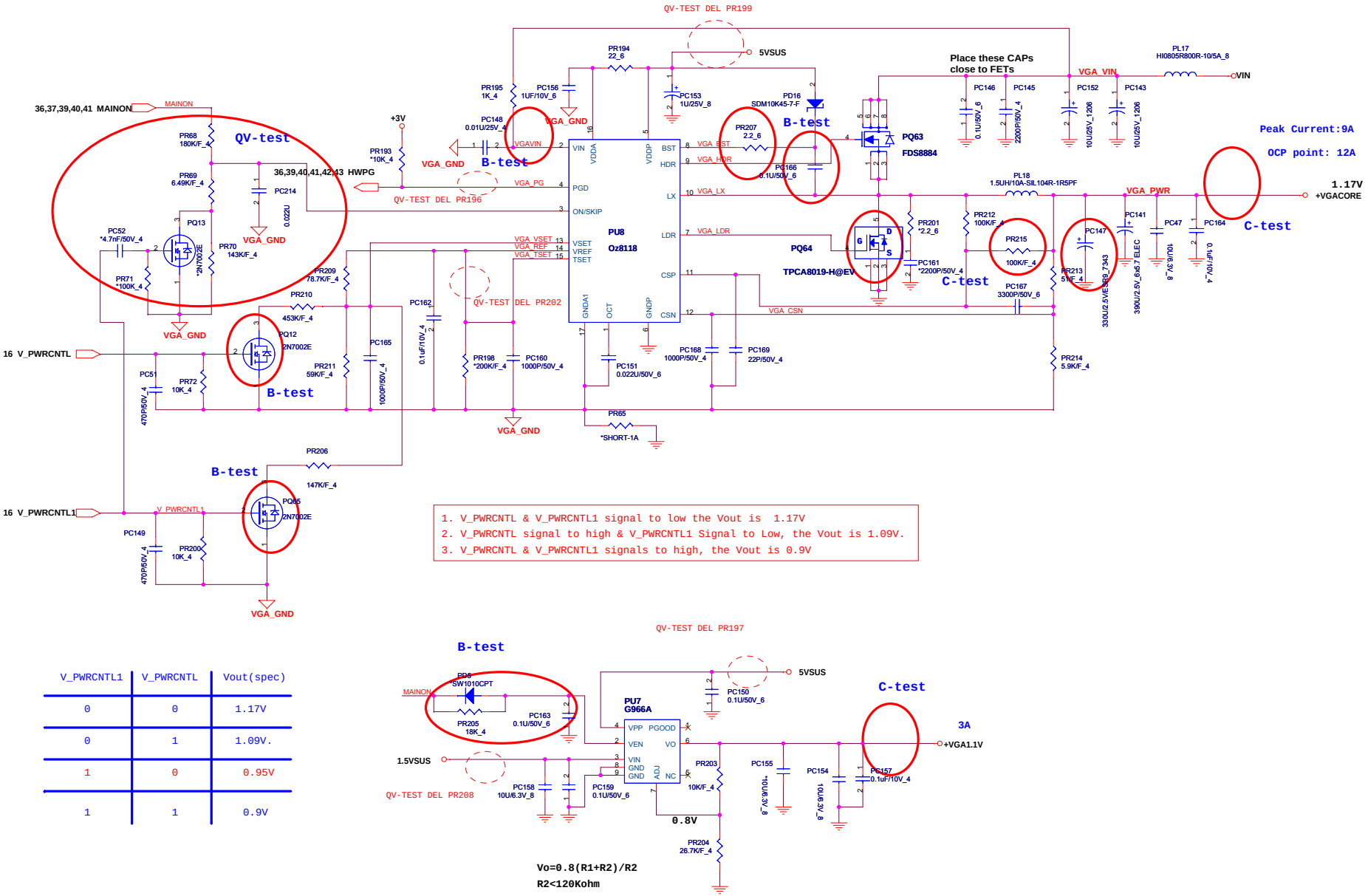
DC/DC 3VPCU/5VPCU/+15V



PROJECT : LE8			
Quanta Computer Inc.			
Size: Custom	Document Number: 3V/5V (ISL6237)		Rev: 1A
Date: Thursday, June 12, 2008	Sheet 42 of 45		



PROJECT : LE8			
Quanta Computer Inc.			
Size: Custom	Document Number: CPU (ISL6266)		Rev: 1A
Date: Thursday, June 12, 2008		Sheet 43 of 45	



V_PWRCNTL1	V_PWRCNTL	Vout(spec)
0	0	1.17V
0	1	1.09V.
1	0	0.95V
1	1	0.9V

PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGA (Oz8118)	1A

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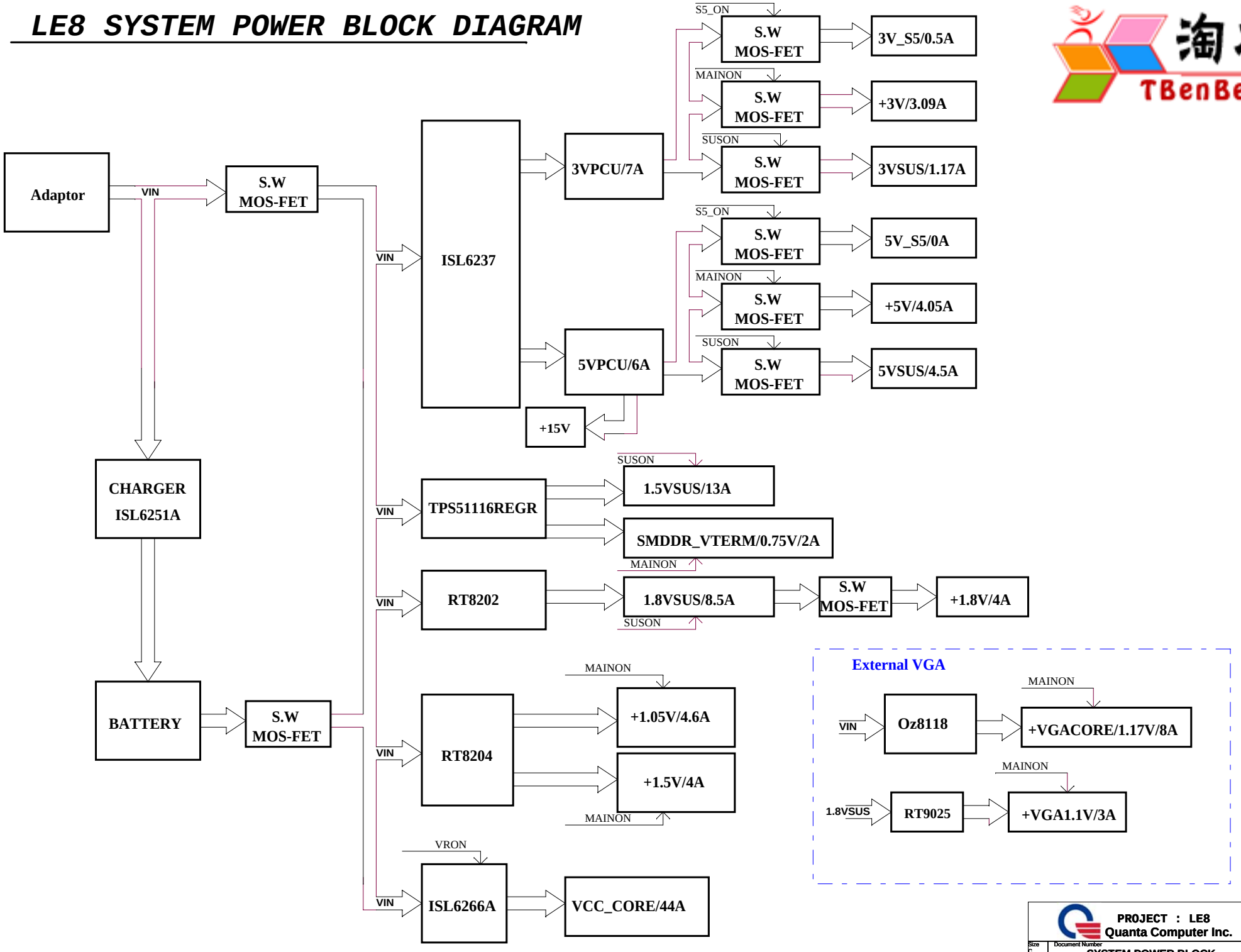
LE8 SYSTEM POWER BLOCK DIAGRAM



PROJECT : LE8
Quanta Computer Inc.
Size C | Document Number SYSTEM POWER BLOCK | Rev 1A
Date: Thursday, June 12, 2008 | Sheet 45 of 45