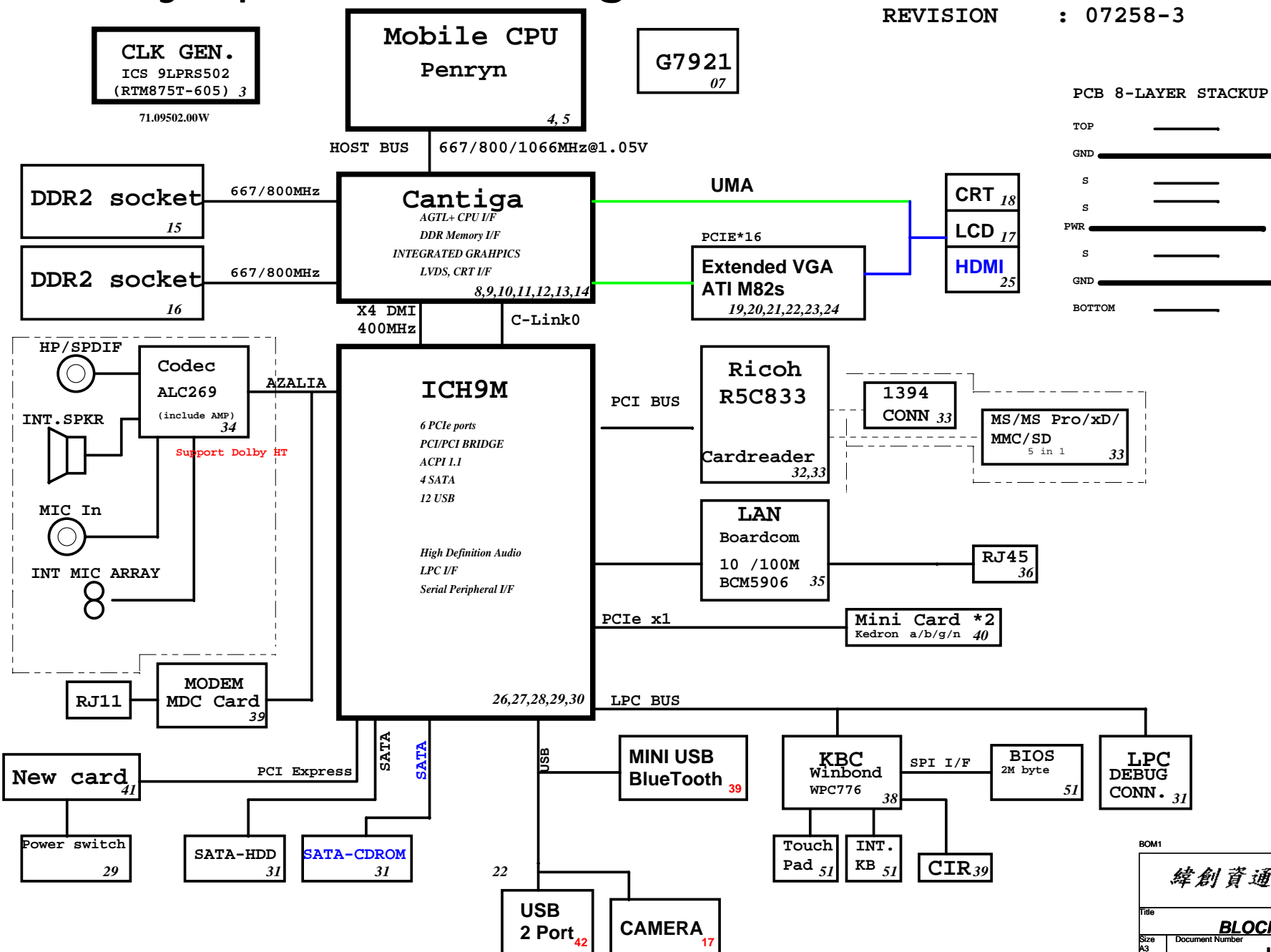


Olympus Block Diagram

Project code: 91.4Y601.001
PCB P/N : 48.4Y603.0SA
REVISION : 07258-3



SYSTEM DC/DC ISL6236 38	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(5A) 3D3V_S5(5A)
SYSTEM DC/DC TPS51124 40	
INPUTS	OUTPUTS
DCBATOUT	1D05V_M(11A) 1D5V_S3(10A)
TPS51117 39	
DCBATOUT	1D8V_S3 (2.5A)
TPS51100 39	
1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3
APL5308 39	
3D3V_S0	2D5V_S0 (300mA)
CHARGER BQ24750 42	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA
CPU DC/DC ISL6266A 37	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A
NB DC/DC ISL6263A 41	
INPUTS	OUTPUTS
DCBATOUT	GFX_CORE
SC411 48	
DCBATOUT	1D5V_S3

ICH9M Functional Strap Definitions

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Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers: Offset 224h).
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers: Offset 0224h).
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override, Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1, Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h; bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal, Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLFVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

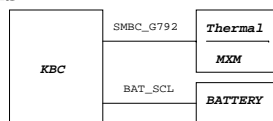
Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5
Page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host interface is enabled (Note 2) 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes, 15->0, 14->1 ect.. 1 = Normal operation (Default): Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALL mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH -> ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH -> ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default). 1 = Digital display Port and PCIE are operating simultaneously via the PG8 port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

SMBus



USB Table

Pair	Device
0	Combo (ESATA/USB)
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1

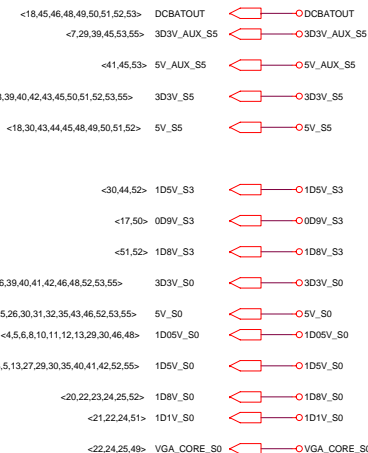
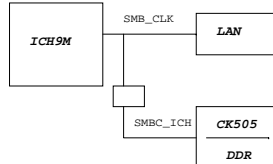
PCI Routing

page 17

IDSEL	INT	REQ	GNT
TI7412	AD22	G: CARDBUS B: 1394 F: Flash Media S: SD Host	0 0

PCIE Routing

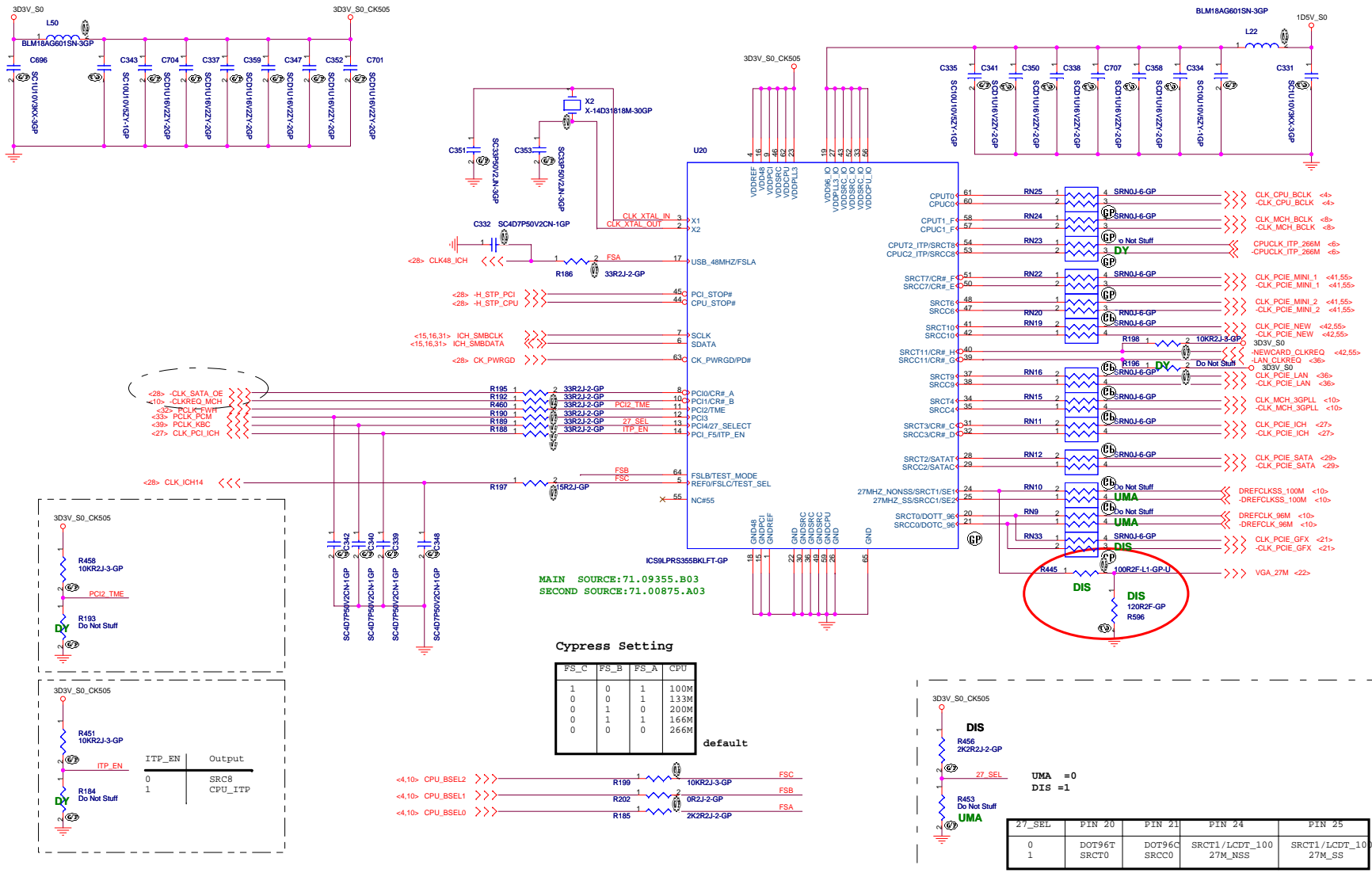
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

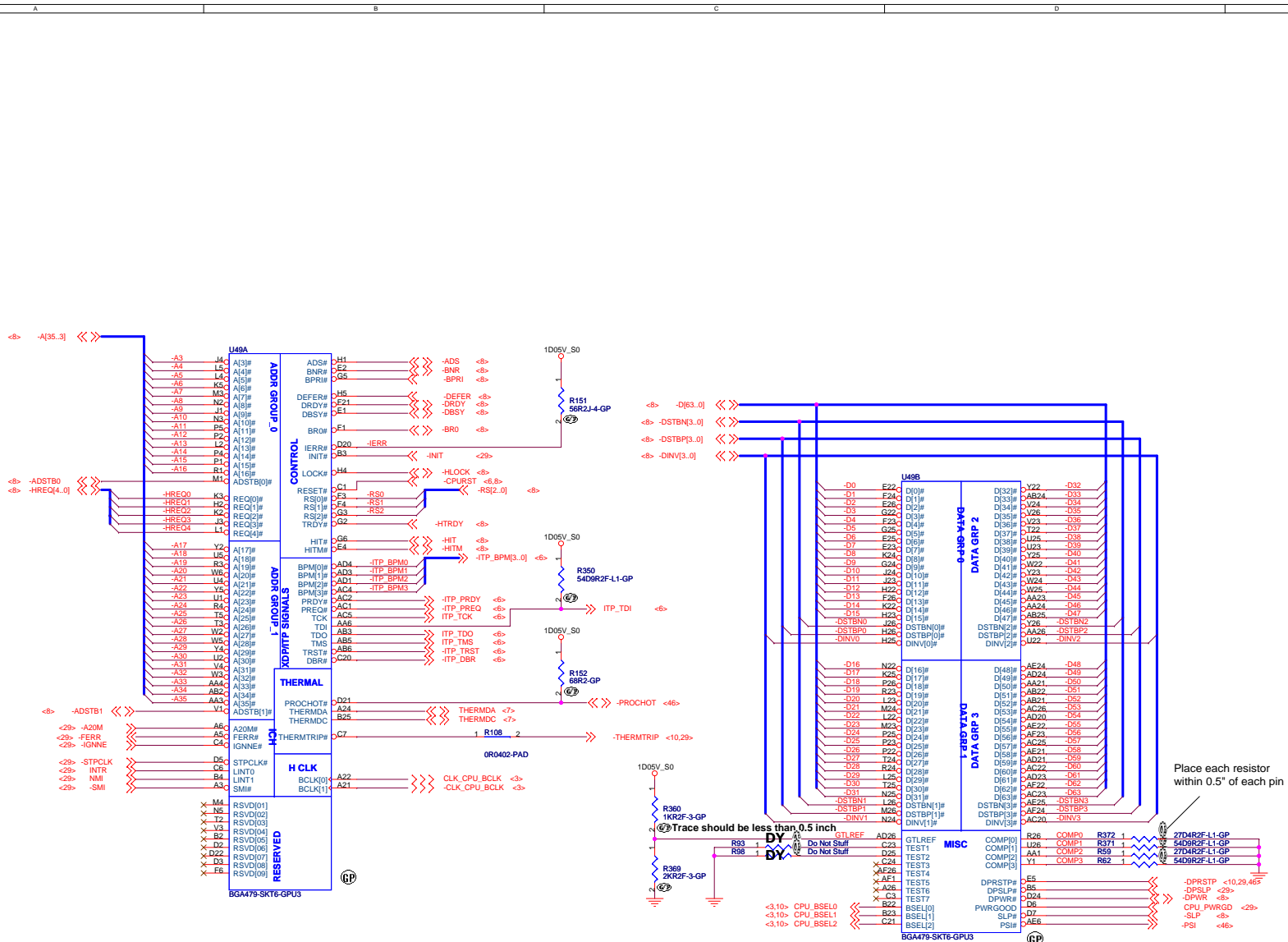


BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

Reference		
Size C	Document Number	Rev
	LT32M	-3
Date: Monday, July 07, 2008	Sheet 2	of 54





Place each resistor within 0.5" of each pin

Trace should be less than 0.5 inch

Do Not Suf

Do Not Suf

Do Not Suf

Do Not Suf

Do Not Suf

Do Not Suf

Do Not Suf

Do Not Suf

Do Not Suf

Do Not Suf

Do Not Suf

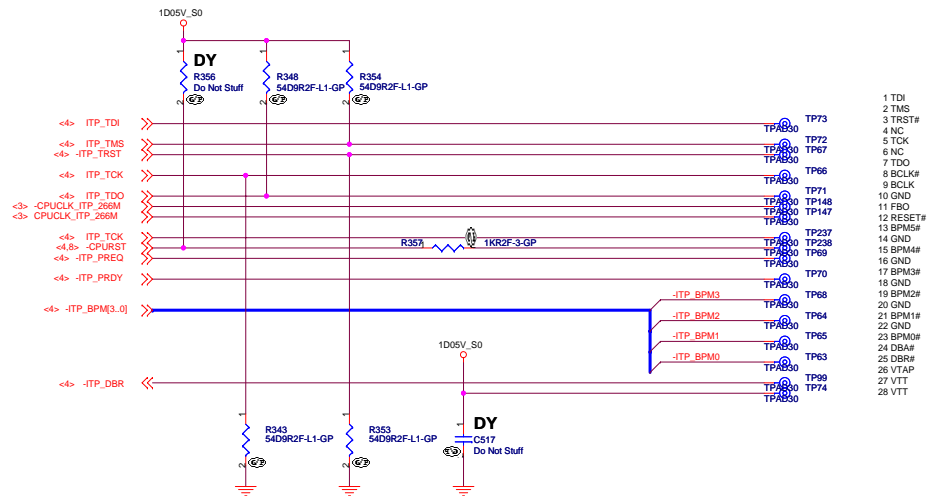
Do Not Suf

Do Not Suf

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Do Not Suf

Do Not Suf



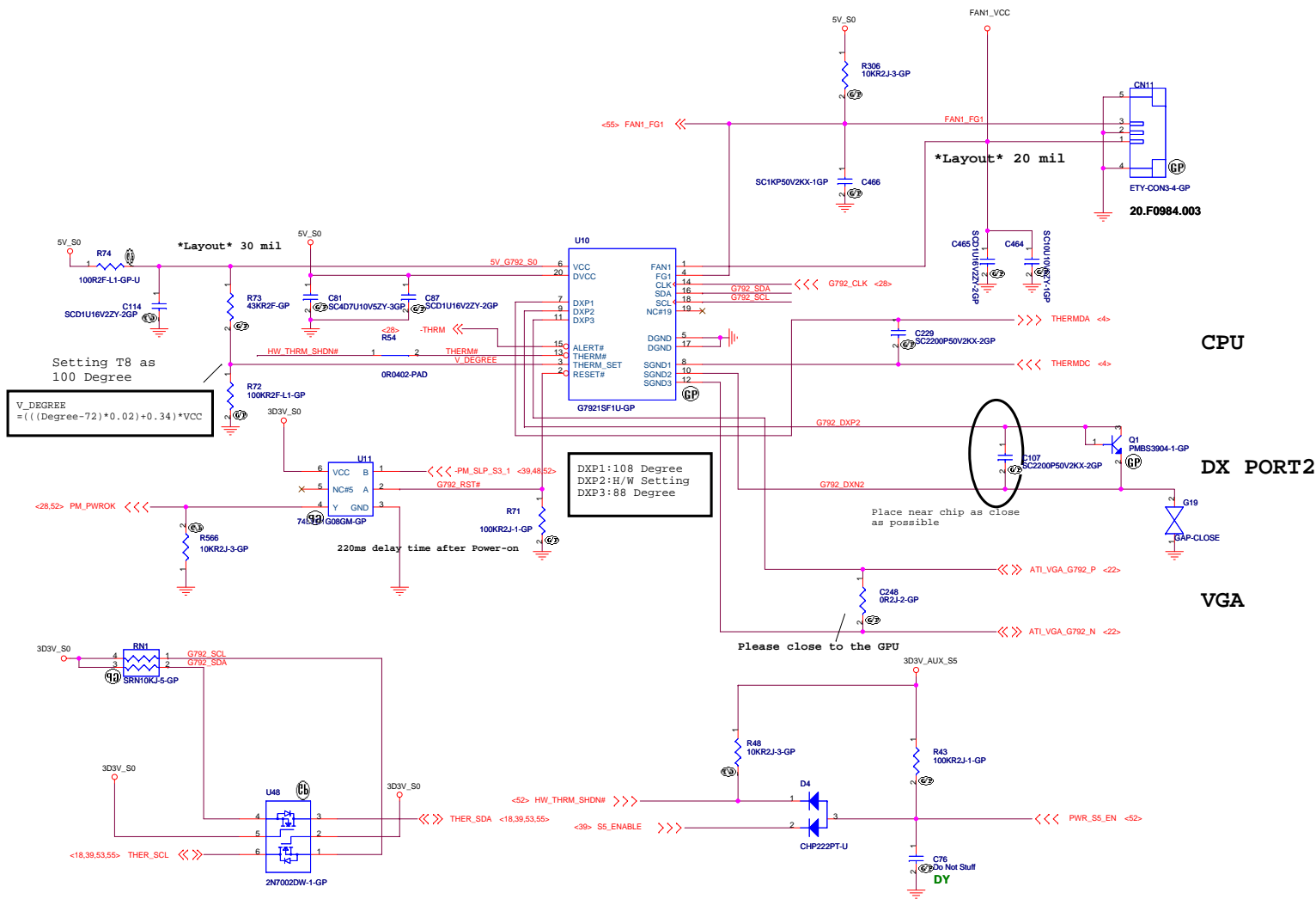
- 1 TDI
- 2 TMS
- 3 TRST#
- 4 NC
- 5 TCK
- 6 NC
- 7 TDO
- 8 BCLK#
- 9 BCLK
- 10 GND
- 11 FBO
- 12 RESET#
- 13 BPM5#
- 14 GND
- 15 BPM4#
- 16 GND
- 17 BPM3#
- 18 GND
- 19 BPM2#
- 20 GND
- 21 BPM1#
- 22 GND
- 23 BPM0#
- 24 DBR#
- 25 DBR#
- 26 VTAP
- 27 VTT
- 28 VTT

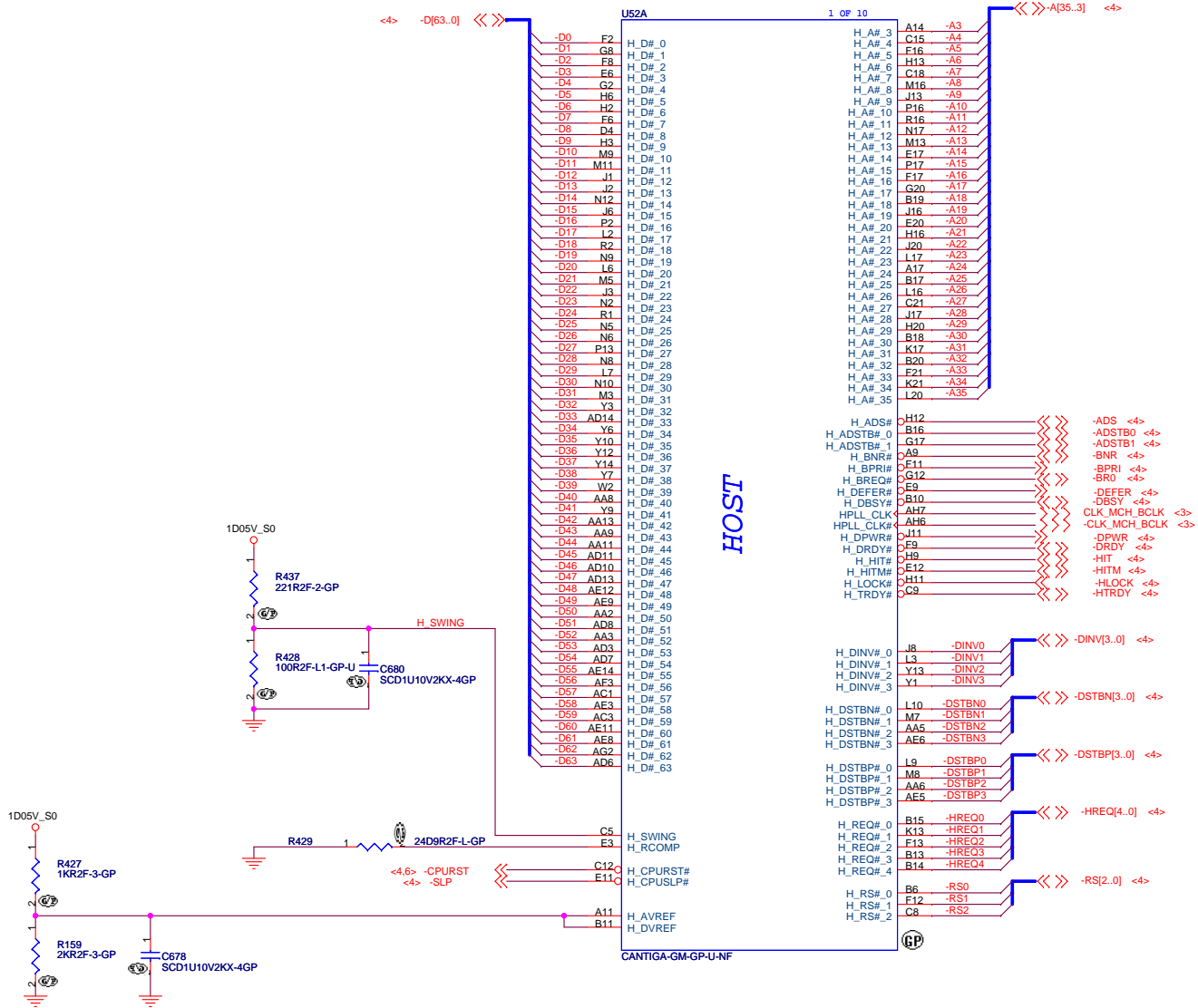
(*1) TCK SIGNAL IS BRANCHED AT CPU's PIN

(*2) CPURST# SIGNAL IS BRANCHED AT GMCH'S PIN

Ref Des	For ITP-XDP
J1	NO_ASM-->ASM
C157	NO_ASM-->ASM
R140	NO_ASM-->1K 5% ASM
R144	ASM (No Change)
R136	ASM-->NO_ASM
R145	ASM (No Change)
R141	ASM-->54.9 1% ASM
R143	ASM-->54.9 1% ASM

BOM1





Route H_XSWING & H_YSWING
10 mil wide / 20 mil spacing

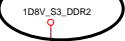
Route H_XRCOMP &
H_YRCOMP 10 mil wide /
20 mil spacing

BOM1

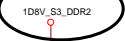
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Title Cantiga(1/7):HOST I/F	
Size A3	Document Number LT32M
Date: Monday, July 07, 2008	Sheet 8 of 54
Rev -3	

FOR DDR2

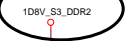
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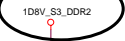
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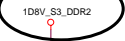
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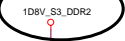
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1D0V_S0



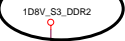
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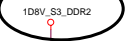
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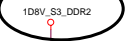
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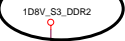
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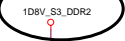
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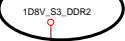
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1D0V_S0



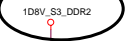
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1D0V_S0



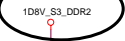
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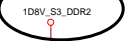
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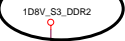
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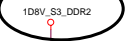
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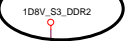
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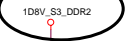
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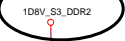
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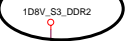
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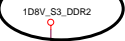
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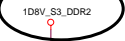
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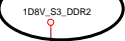
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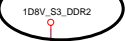
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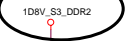
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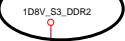
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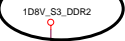
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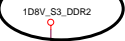
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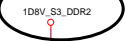
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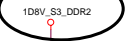
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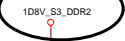
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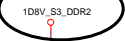
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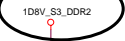
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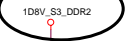
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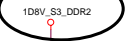
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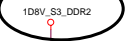
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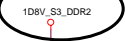
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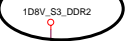
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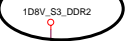
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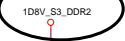
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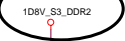
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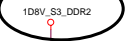
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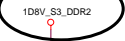
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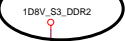
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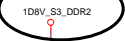
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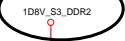
1D0V_S0



1D0V_S0



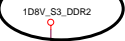
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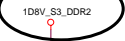
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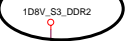
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1D0V_S0



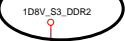
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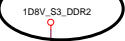
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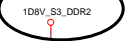
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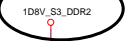
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1D0V_S0



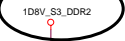
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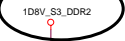
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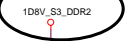
1D0V_S0



1D0V_S0



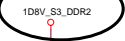
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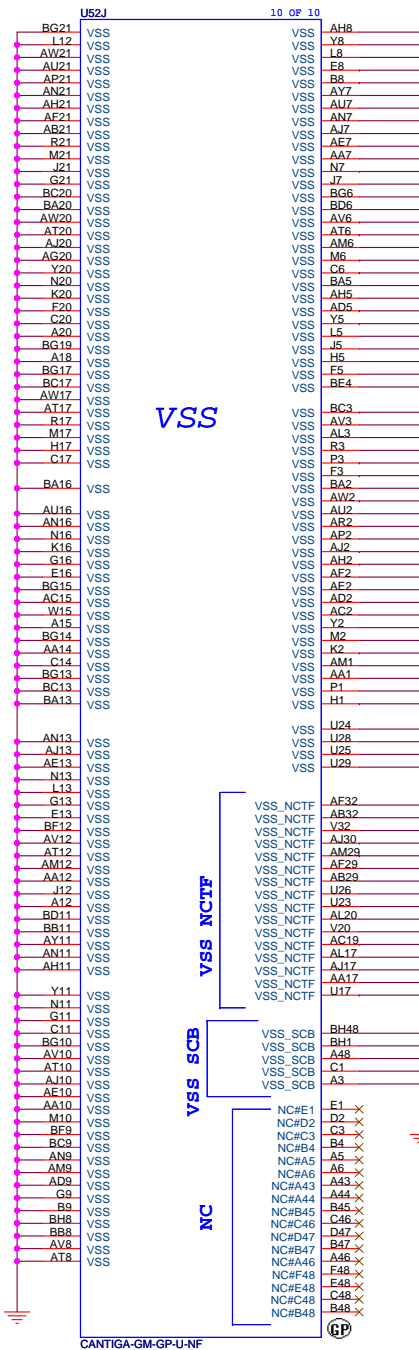
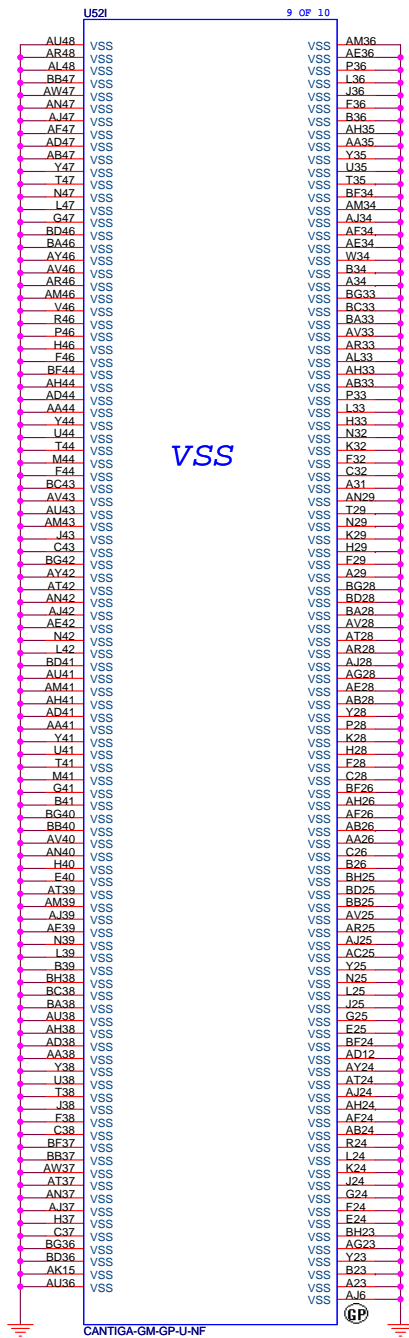


1D0V_S0



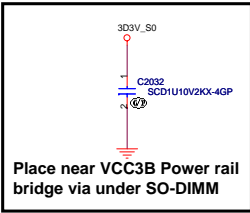
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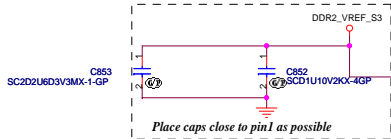
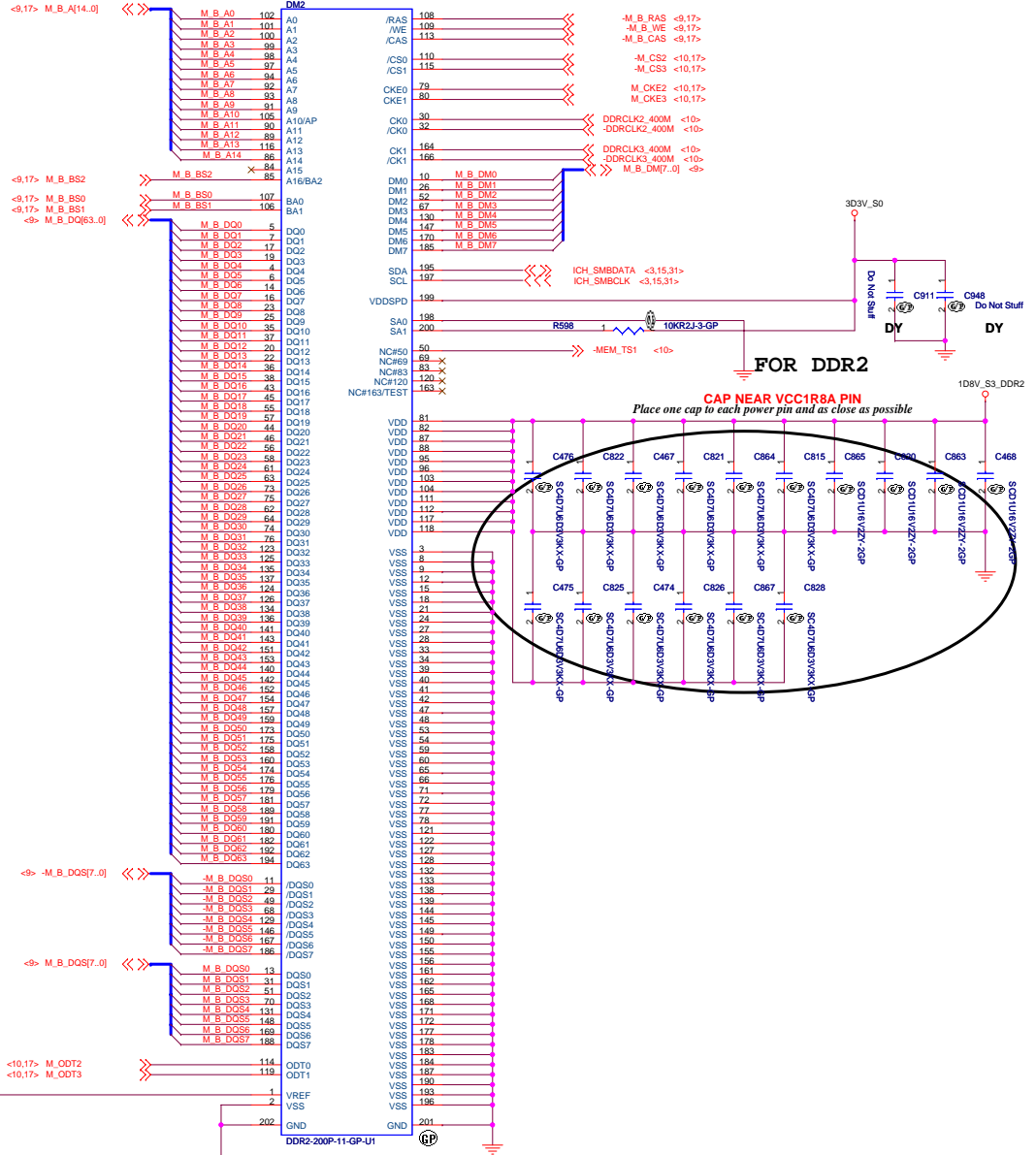
BOM1

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Cantiga(8/7):GND	
Size A3	Document Number
LT32M	
Date: Monday, July 07, 2008	Sheet 14 of 54



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Title			
DDR2 SODIMM-A			
Size	Document Number		Rev
C		LT32M	-3
Date:	Monday, July 07, 2008	Sheet 15 of	54



FOR DDR2

0D9V_S3

Legend:

- M_A_BS[2..0] <9.15>
- M_CKE[3..0] <10.15, 16>
- M_ODT[3..0] <10.15, 16>
- M_A_WE <9.15>
- M_A_CAS <9.15>
- M_CS1

Module Connections:

- RN93:** M_A_A3, M_A_A10, M_A_BS0, M_A_A12, M_A_A1, M_A_A9, M_A_A8, M_CKE1, M_A_A14, M_A_A11, M_A_A0, M_A_BS2, M_CKE0, M_A_A5
- RN94:** M_A_A12, M_A_A1, M_A_A9, M_A_A8
- RN95:** M_CKE1, M_A_A14, M_A_A11
- RN55:** M_A_A0, M_A_BS2, M_CKE0, M_A_A5
- RN96:** M_A_A7, M_A_A6, M_A_A4, M_A_A2
- RN97:** M_A_WE, M_A_BS1, M_CS1
- RN98:** M_ODT1, M_A_A13, M_CS0, M_ODT0

FOR DDR2

The diagram illustrates the DDR2 pinout for the M.B. A[14:0] and M.B. BS[2:0] signals. The central signal is 0D9V_S3, which is connected to the 0D9V_S3 pin (pin 1) of the M.B. A[14:0] and M.B. BS[2:0] signals. The M.B. A[14:0] signal is connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 162, 163, 164, 165, 166, 167, 168, 169, 170, 171, 172, 173, 174, 175, 176, 177, 178, 179, 180, 181, 182, 183, 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 237, 238, 239, 240, 241, 242, 243, 244, 245, 246, 247, 248, 249, 250, 251, 252, 253, 254, 255, 256, 257, 258, 259, 260, 261, 262, 263, 264, 265, 266, 267, 268, 269, 270, 271, 272, 273, 274, 275, 276, 277, 278, 279, 280, 281, 282, 283, 284, 285, 286, 287, 288, 289, 290, 291, 292, 293, 294, 295, 296, 297, 298, 299, 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394, 395, 396, 397, 398, 399, 400, 401, 402, 403, 404, 405, 406, 407, 408, 409, 410, 411, 412, 413, 414, 415, 416, 417, 418, 419, 420, 421, 422, 423, 424, 425, 426, 427, 428, 429, 430, 431, 432, 433, 434, 435, 436, 437, 438, 439, 440, 441, 442, 443, 444, 445, 446, 447, 448, 449, 450, 451, 452, 453, 454, 455, 456, 457, 458, 459, 460, 461, 462, 463, 464, 465, 466, 467, 468, 469, 470, 471, 472, 473, 474, 475, 476, 477, 478, 479, 480, 481, 482, 483, 484, 485, 486, 487, 488, 489, 490, 491, 492, 493, 494, 495, 496, 497, 498, 499, 500, 501, 502, 503, 504, 505, 506, 507, 508, 509, 510, 511, 512, 513, 514, 515, 516, 517, 518, 519, 520, 521, 522, 523, 524, 525, 526, 527, 528, 529, 530, 531, 532, 533, 534, 535, 536, 537, 538, 539, 540, 541, 542, 543, 544, 545, 546, 547, 548, 549, 550, 551, 552, 553, 554, 555, 556, 557, 558, 559, 560, 561, 562, 563, 564, 565, 566, 567, 568, 569, 570, 571, 572, 573, 574, 575, 576, 577, 578, 579, 580, 581, 582, 583, 584, 585, 586, 587, 588, 589, 590, 591, 592, 593, 594, 595, 596, 597, 598, 599, 600, 601, 602, 603, 604, 605, 606, 607, 608, 609, 610, 611, 612, 613, 614, 615, 616, 617, 618, 619, 620, 621, 622, 623, 624, 625, 626, 627, 628, 629, 630, 631, 632, 633, 634, 635, 636, 637, 638, 639, 640, 641, 642, 643, 644, 645, 646, 647, 648, 649, 650, 651, 652, 653, 654, 655, 656, 657, 658, 659, 660, 661, 662, 663, 664, 665, 666, 667, 668, 669, 670, 671, 672, 673, 674, 675, 676, 677, 678, 679, 680, 681, 682, 683, 684, 685, 686, 687, 688, 689, 690, 691, 692, 693, 694, 695, 696, 697, 698, 699, 700, 701, 702, 703, 704, 705, 706, 707, 708, 709, 710, 711, 712, 713, 714, 715, 716, 717, 718, 719, 720, 721, 722, 723, 724, 725, 726, 727, 728, 729, 730, 731, 732, 733, 734, 735, 736, 737, 738, 739, 740, 741, 742, 743, 744, 745, 746, 747, 748, 749, 750, 751, 752, 753, 754, 755, 756, 757, 758, 759, 760, 761, 762, 763, 764, 765, 766, 767, 768, 769, 770, 771, 772, 773, 774, 775, 776, 777, 778, 779, 780, 781, 782, 783, 784, 785, 786, 787, 788, 789, 790, 791, 792, 793, 794, 795, 796, 797, 798, 799, 800, 801, 8

0.9V_S3

PLACE 1 CAP FOR EVERY 2 BITS TERMINATION TO VCC09A.

C835 SCD U10/ZKX-6Gp

C841 SCD U10/ZKX-6Gp

C849 SCD U10/ZKX-6Gp

C831 SCD U10/ZKX-6Gp

C846 SCD U10/ZKX-6Gp

C840 SCD U10/ZKX-6Gp

C832 SCD U10/ZKX-6Gp

C838 SCD U10/ZKX-6Gp

C845 SCD U10/ZKX-6Gp

C839 SCD U10/ZKX-6Gp

C854 SCD U10/ZKX-6Gp

C855 SCD U10/ZKX-6Gp

C856 SCD U10/ZKX-6Gp

C836 SCD U10/ZKX-6Gp

C837 SCD U10/ZKX-6Gp

C843 SCD U10/ZKX-6Gp

C833 SCD U10/ZKX-6Gp

C844 SCD U10/ZKX-6Gp

C842 SCD U10/ZKX-6Gp

C847 SCD U10/ZKX-6Gp

C830 SCD U10/ZKX-6Gp

C848 SCD U10/ZKX-6Gp

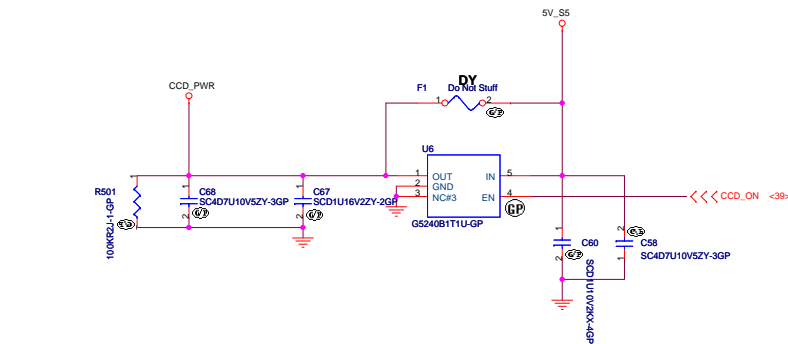
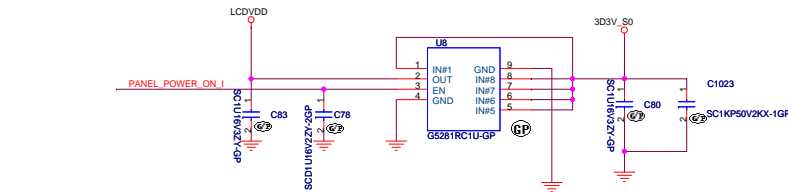
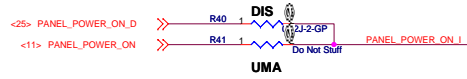
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C858 SCD U10/ZKX-6Gp

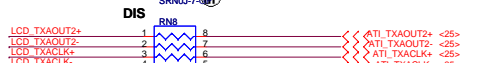
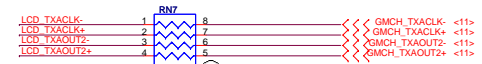
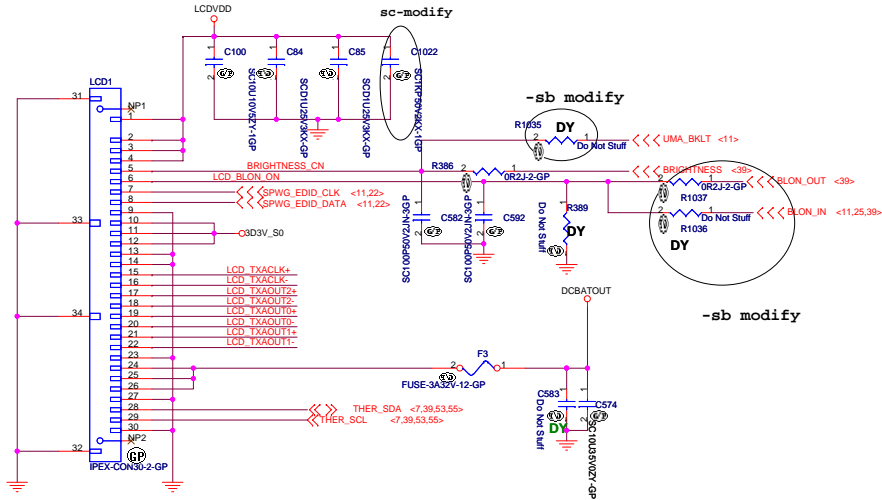
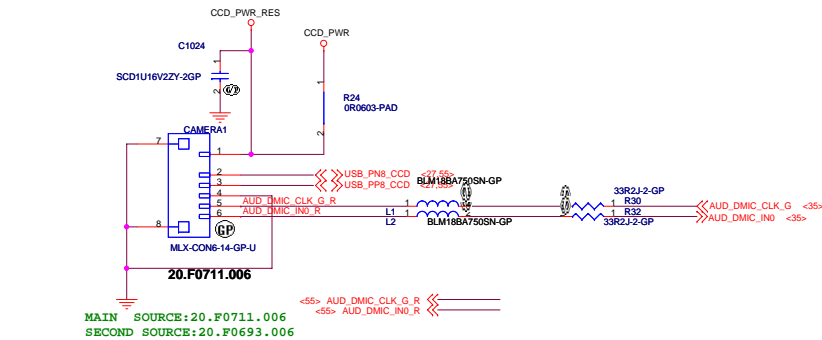
C859 SCD U10/ZKX-6Gp

C860 SCD U10/ZKX-6Gp

LCD/INVERTER CONN



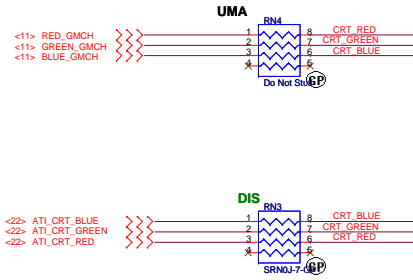
CAMERA & DIG-MIC



BOM1

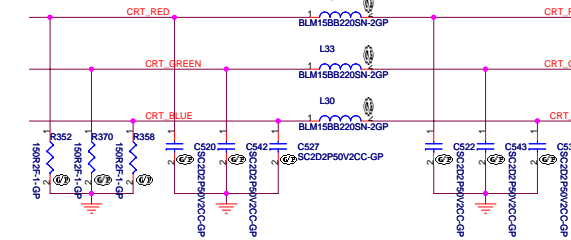
緯創資通 Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.	
LCD CONN & CAMERA & DIG-MIC	
Size	Document Number
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CRT I/F & CONNECTOR



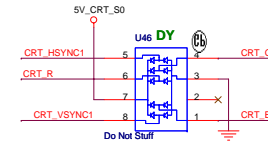
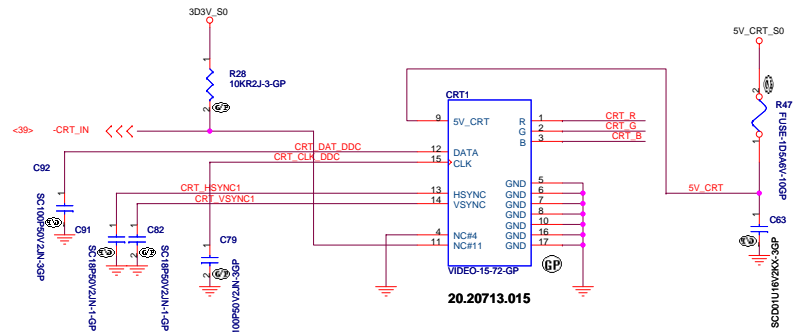
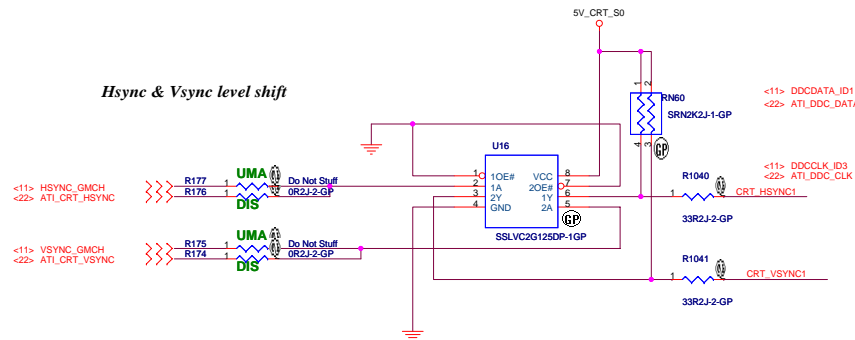
Layout Note:
Place these resistors
close to the CRT-out
connector

Ferrite bead impedance: 10 ohm@100MHz

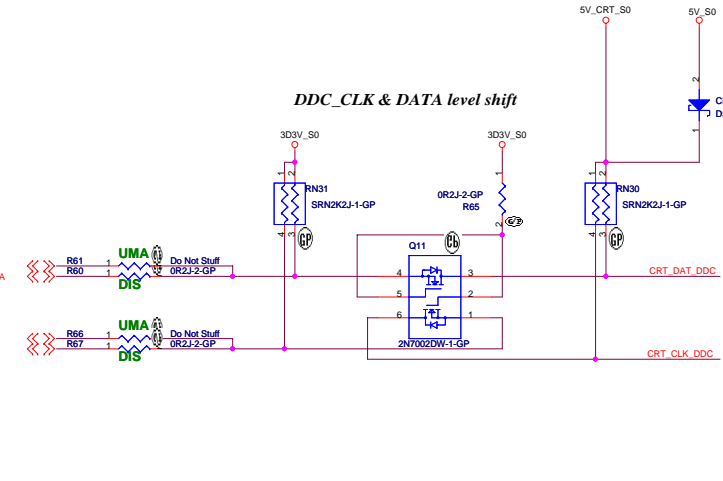


Layout Note:
* Must be a ground return path between this ground and the ground on
the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT
CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

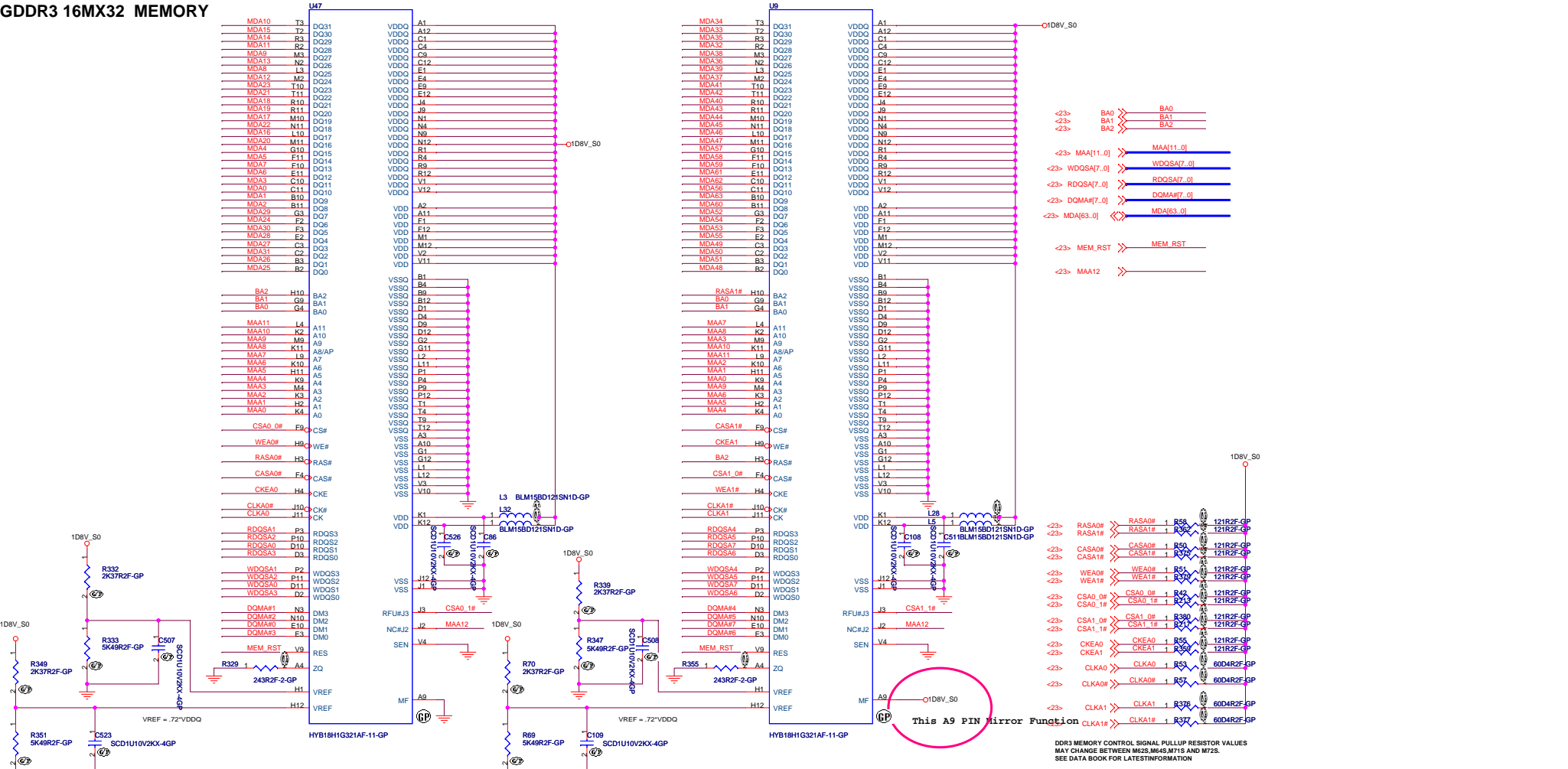


DDC_CLK & DATA level shift



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File	CRT/TV Connector		
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GDDR3 16MX32 MEMORY

DDR3 MEMORY CONTROL SIGNAL PULLUP RESISTOR VALUES
MAY CHANGE BETWEEN M62S,M64S,M71S AND M72S.
SEE DATA BOOK FOR LATEST INFORMATION

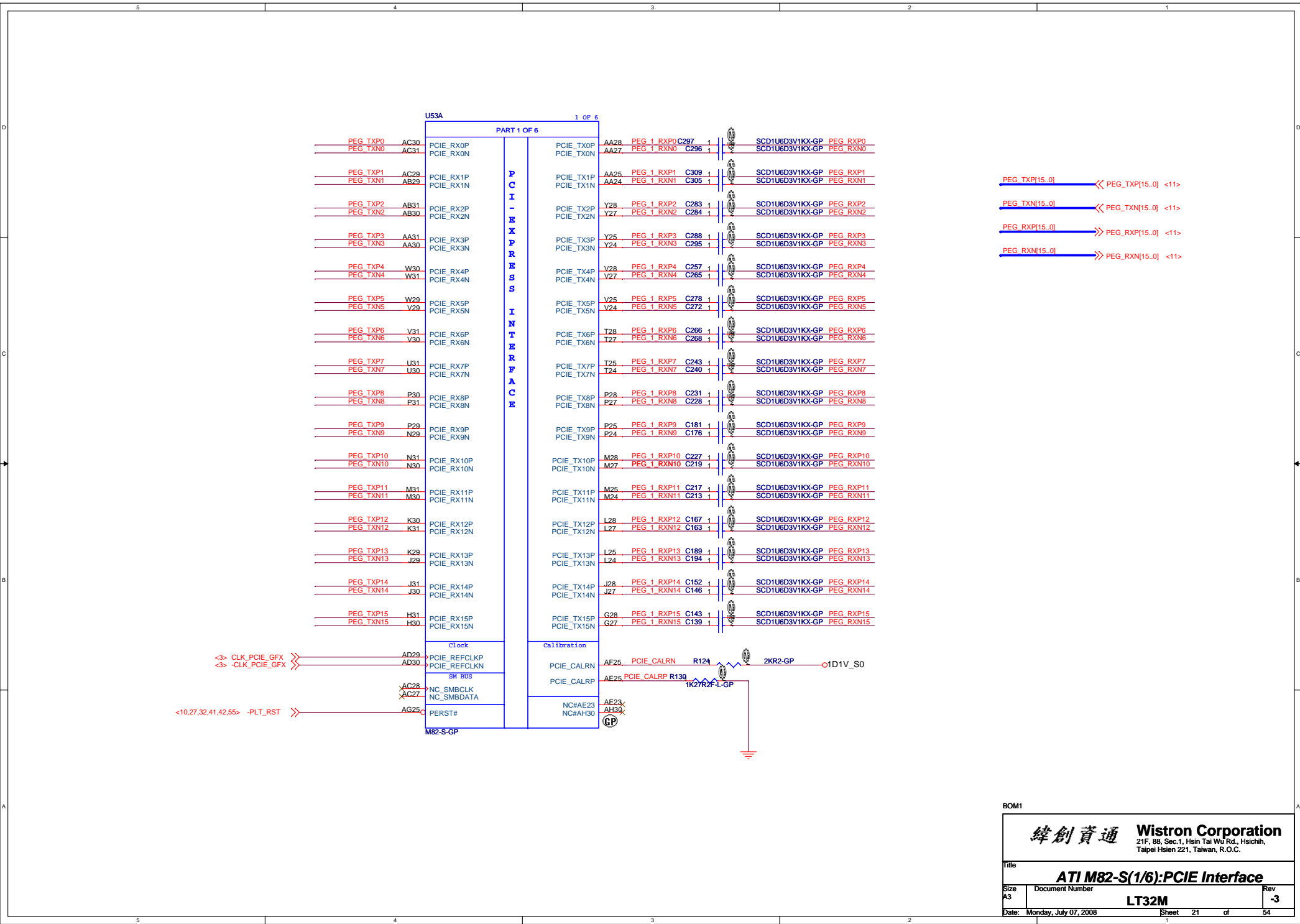
BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ATI M82-S VRAM(1,2)
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Size	Document Number
100	100

Date: Monday, July 07, 2008 Sheet 20 of



BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			ATI M82-S(1/6):PCIE Interface	
Size	Document Number	Rev		
A3	LT32M	-3		
Date:	Monday, July 07, 2008	Sheet	21	of 54

<20> RASA0# << RASA0#
 <20> RASA1# << RASA1#
 <20> CASA0# << CASA0#
 <20> CASA1# << CASA1#
 <20> WEA0# << WEA0#
 <20> WEA1# << WEA1#
 <20> CKEA0 << CKEA0
 <20> CKEA1 << CKEA1
 <20> CSA0_0# << CSA0_0#
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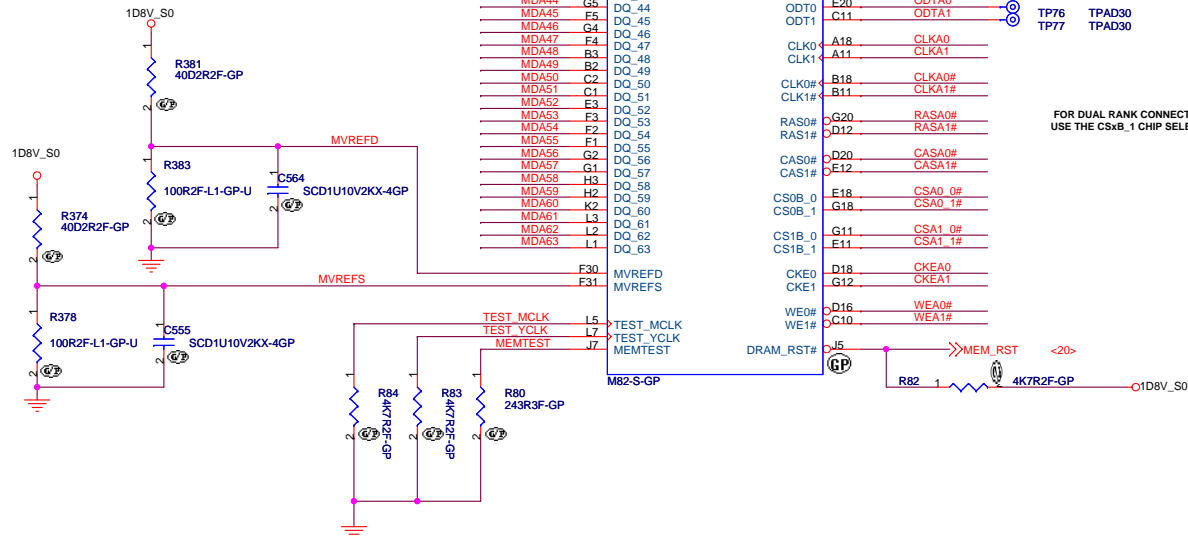
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 <20> CLKA0# << CLKA0#
 <20> CLKA1 << CLKA1
 <20> CLKA1# << CLKA1#

<20> WDQSA[7..0] << WDQSA[7..0]
 <20> RDQSA[7..0] << RDQSA[7..0]
 <20> DQMA#[7..0] << DQMA#[7..0]
 <20> MDA[63..0] << MDA[63..0]
 <20> MAA[11..0] << MAA[11..0]

<20> BA0 << BA0
 <20> BA1 << BA1
 <20> BA2 << BA2
 <20> MAA12 << MAA12

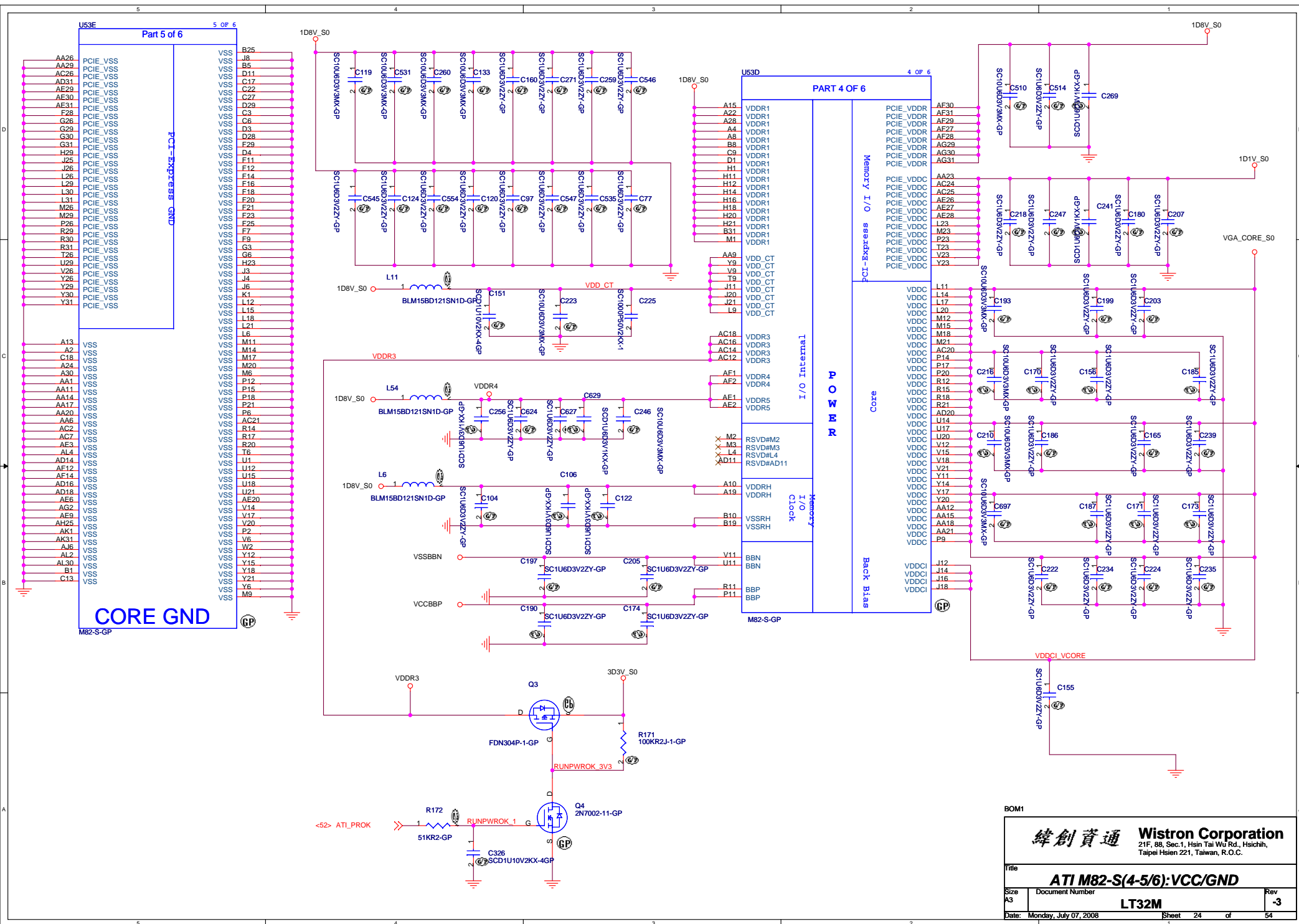
PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC

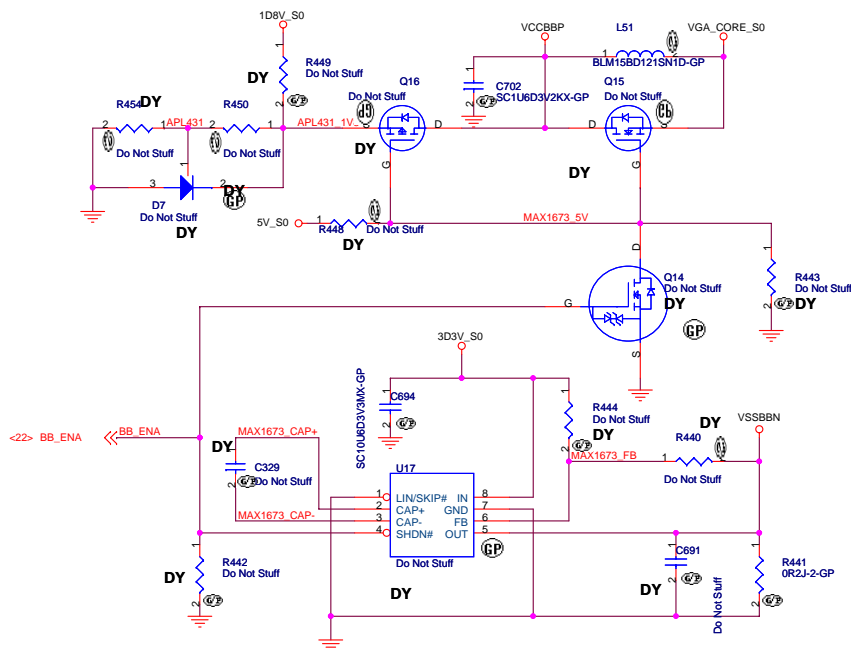
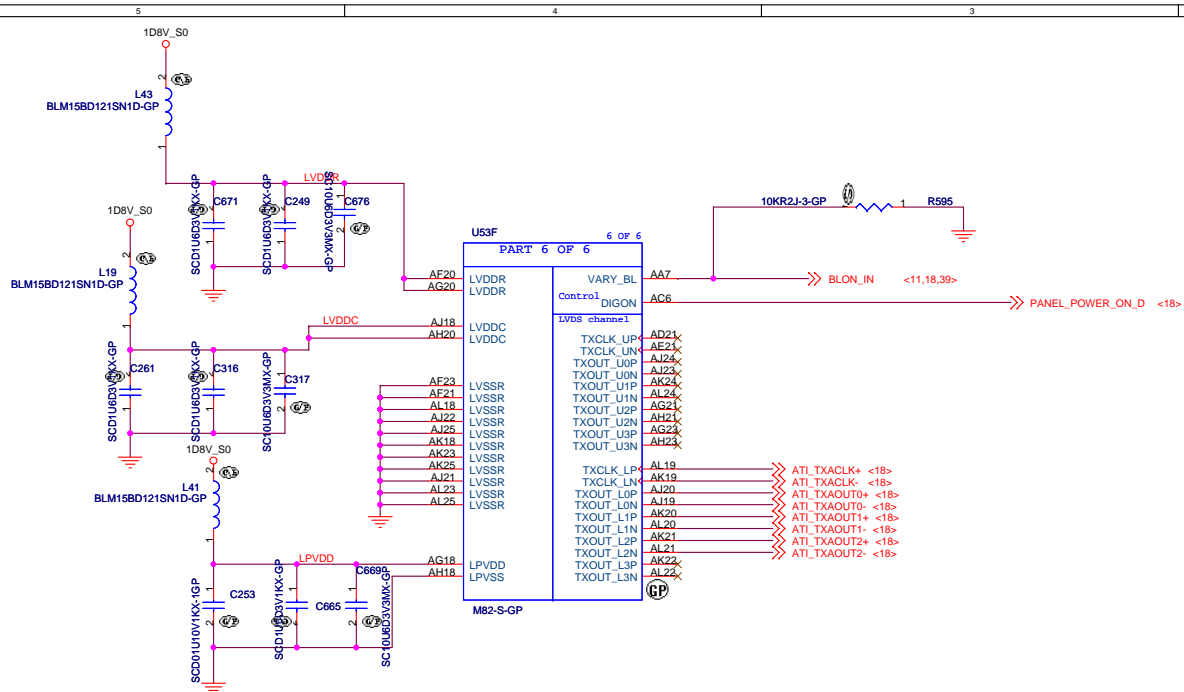
DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title AT1 M82-S(3/6):Memory Interface	
Size A3	Document Number LT32M
Date: Monday, July 07, 2008	Rev -3
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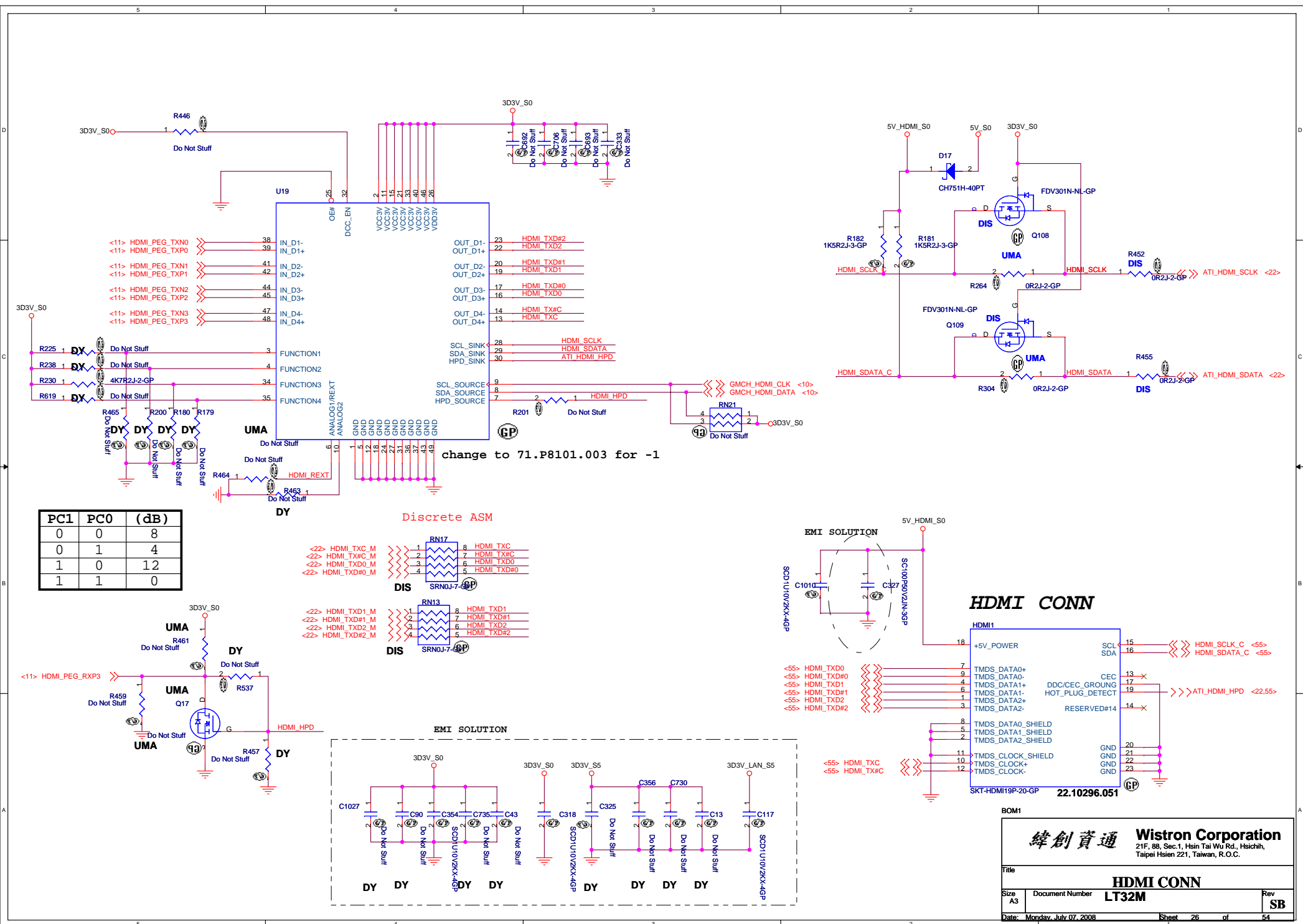


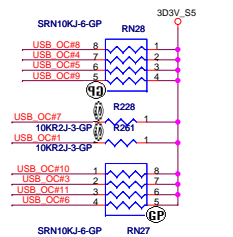
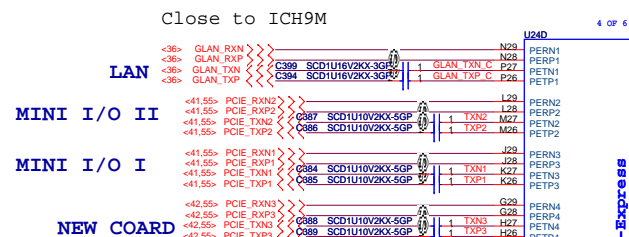
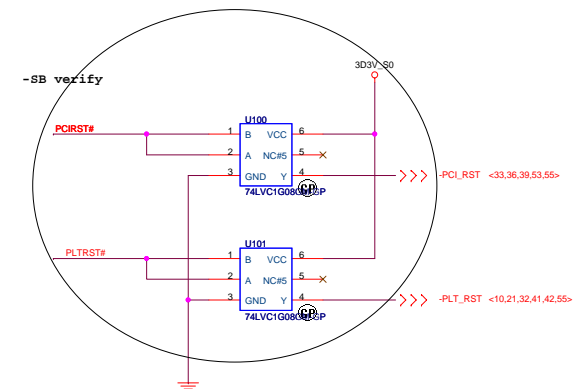


BOM1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
ATI M82-S(6/6):LVDS		
Size	Document Number	Rev
Custom	LT32M	-3
Date: Monday, July 07, 2008 Sheet 25 of 54		



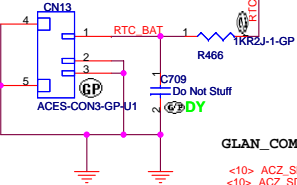


Timing diagram showing signal transitions for PCI signals. The signals are labeled as PCI_GNT#0, ICH_SPI_CS#1, and PCI_GNT#3. The diagram indicates that these signals are "Do Not Stuff" (Do Not Sample) at the transition points, as shown by the "Do Not Stuff" labels and the "DY" (Do Not Sample) markers.



MAIN SOURCE:20.F0411.003
SECOND SOURCE:20.D0246.103

20.F0714.003



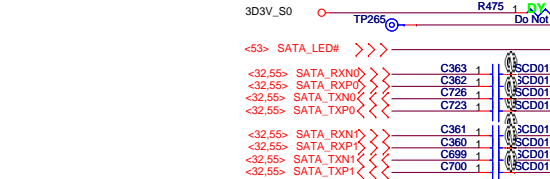
GLAN_COMP place within 500 mils of ICH9M

- <10> ACZ_SDIN
- <10> ACZ_SDOOUT
- <10> ACZ_SYNC
- <10> ACZ_RST
- <10> ACZ_BITCLK



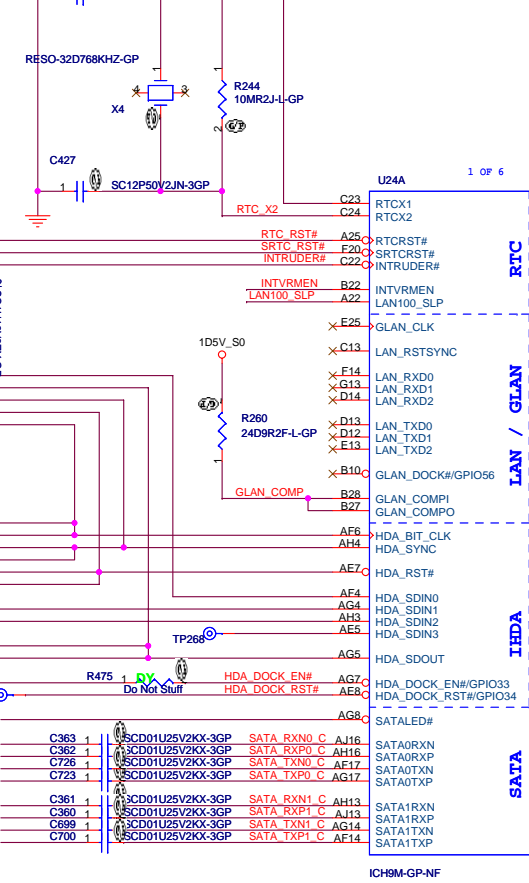
- <40,55> ACZ_BITCLK_MDC
- <35> ACZ_BITCLK_RTL
- <35> ACZ_SYNC_RTL
- <40,55> ACZ_SYNC_MDC
- <40,55> ACZ_RST_MDC
- <35> ACZ_RST_RTL

- <35> ACZ_SDATIN_RTL
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- <40,55> ACZ_SDATIN_OUT_MDC
- <35> ACZ_SDATIN_OUT_RTL

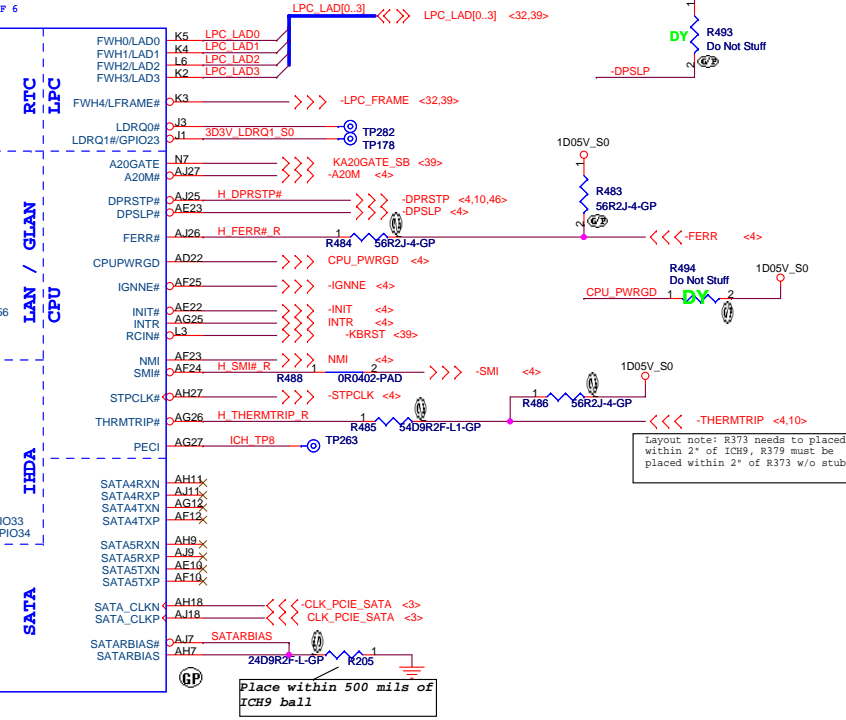
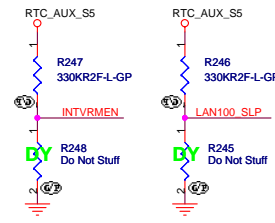


- <53> SATA_LED#
- <32,55> SATA_RXN0
- <32,55> SATA_RXP0
- <32,55> SATA_TXN0
- <32,55> SATA_TXP0
- <32,55> SATA_RXN1
- <32,55> SATA_RXP1
- <32,55> SATA_TXN1
- <32,55> SATA_TXP1

KDS: RESO 32.768KHZ / 12P



Integrated VccSus1_05,VccSus1_5,VccCl1_5	
INTVRMEN	High=Enable Low=Disable
Integrated VccLan1_05VccCl1_05	
LAN100_SLP	High=Enable Low=Disable

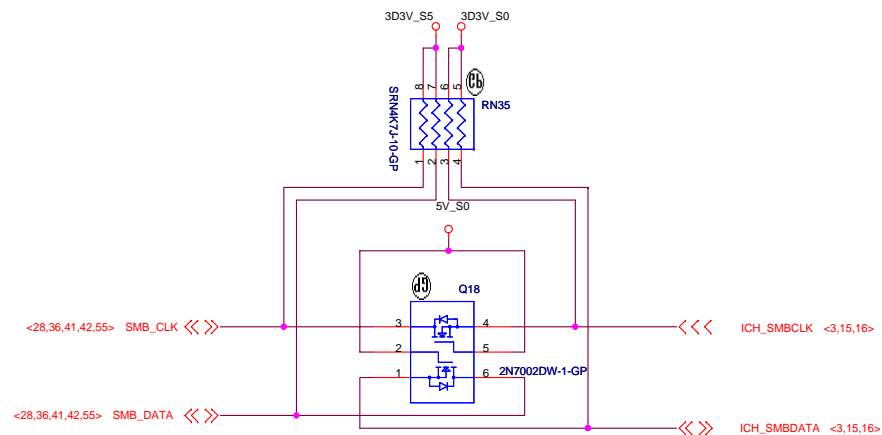
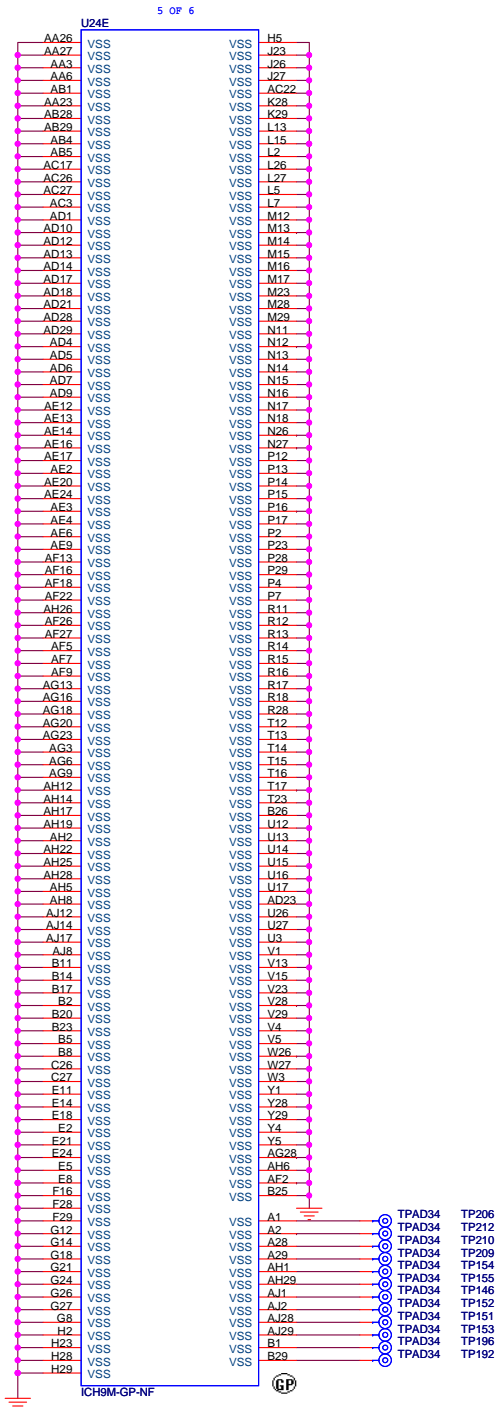


Layout note: R373 needs to be placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub

Place within 500 mils of ICH9 ball

BOM1

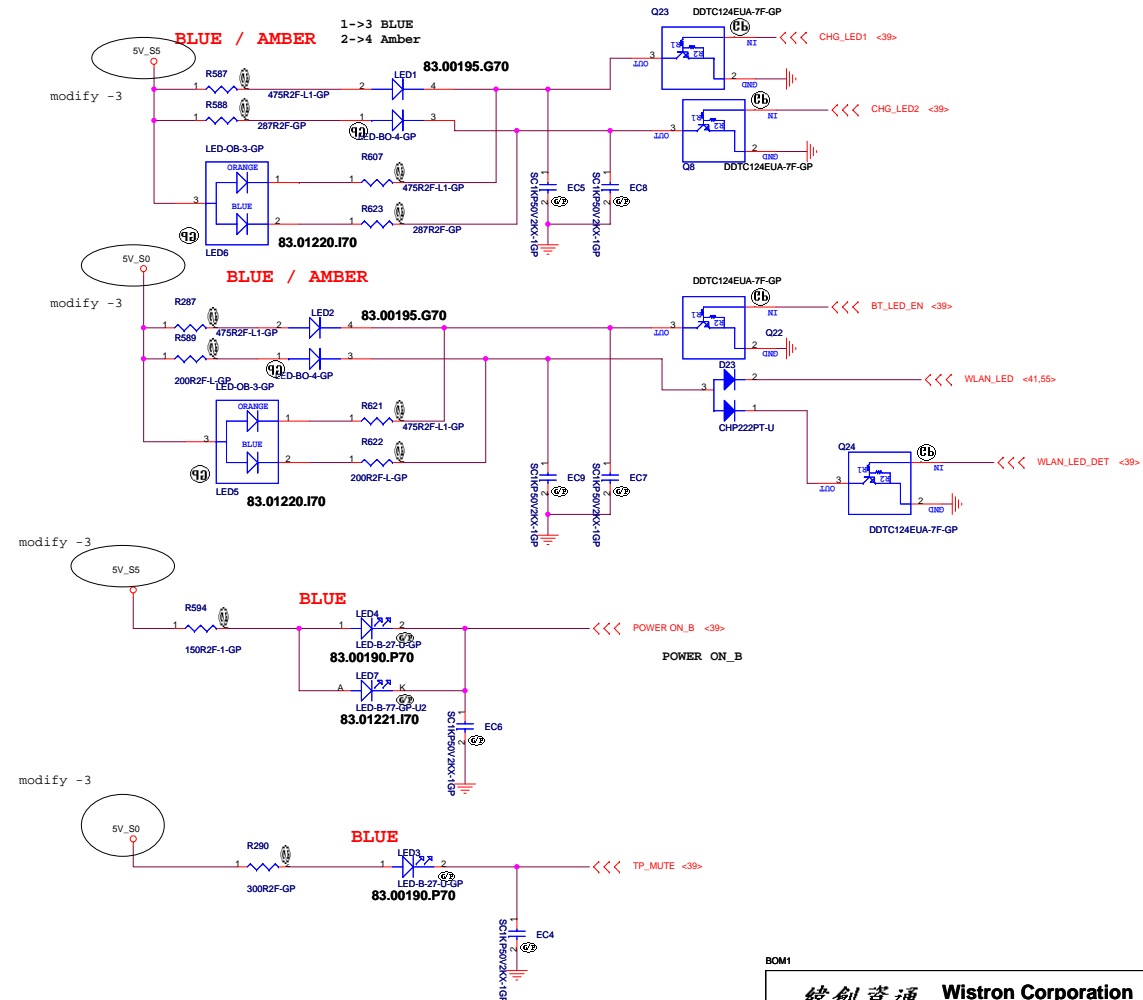
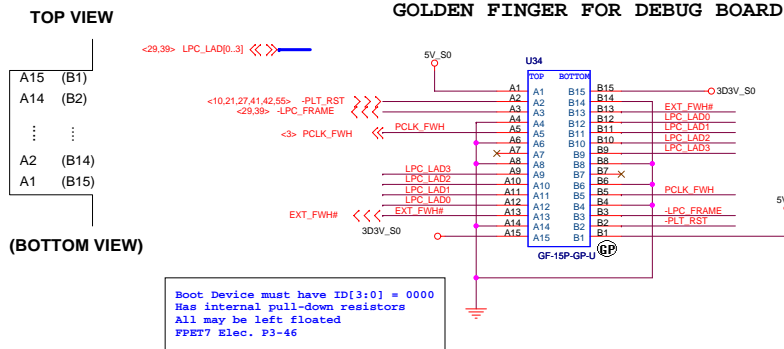
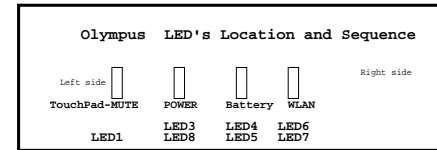
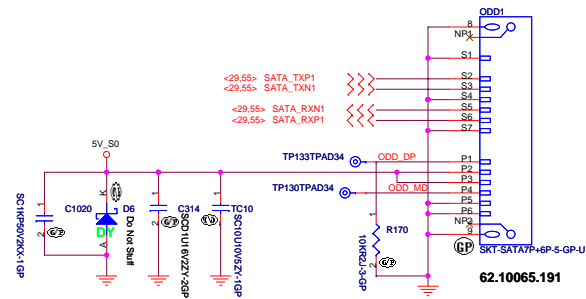
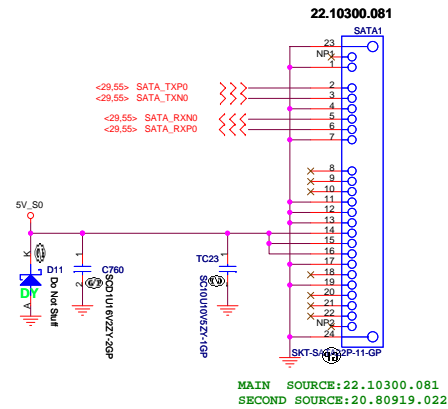
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title ICH9-M (1 of 4)	
Size	Document Number
LT32M	
Date: Monday, July 07, 2008	Sheet 29 of 54

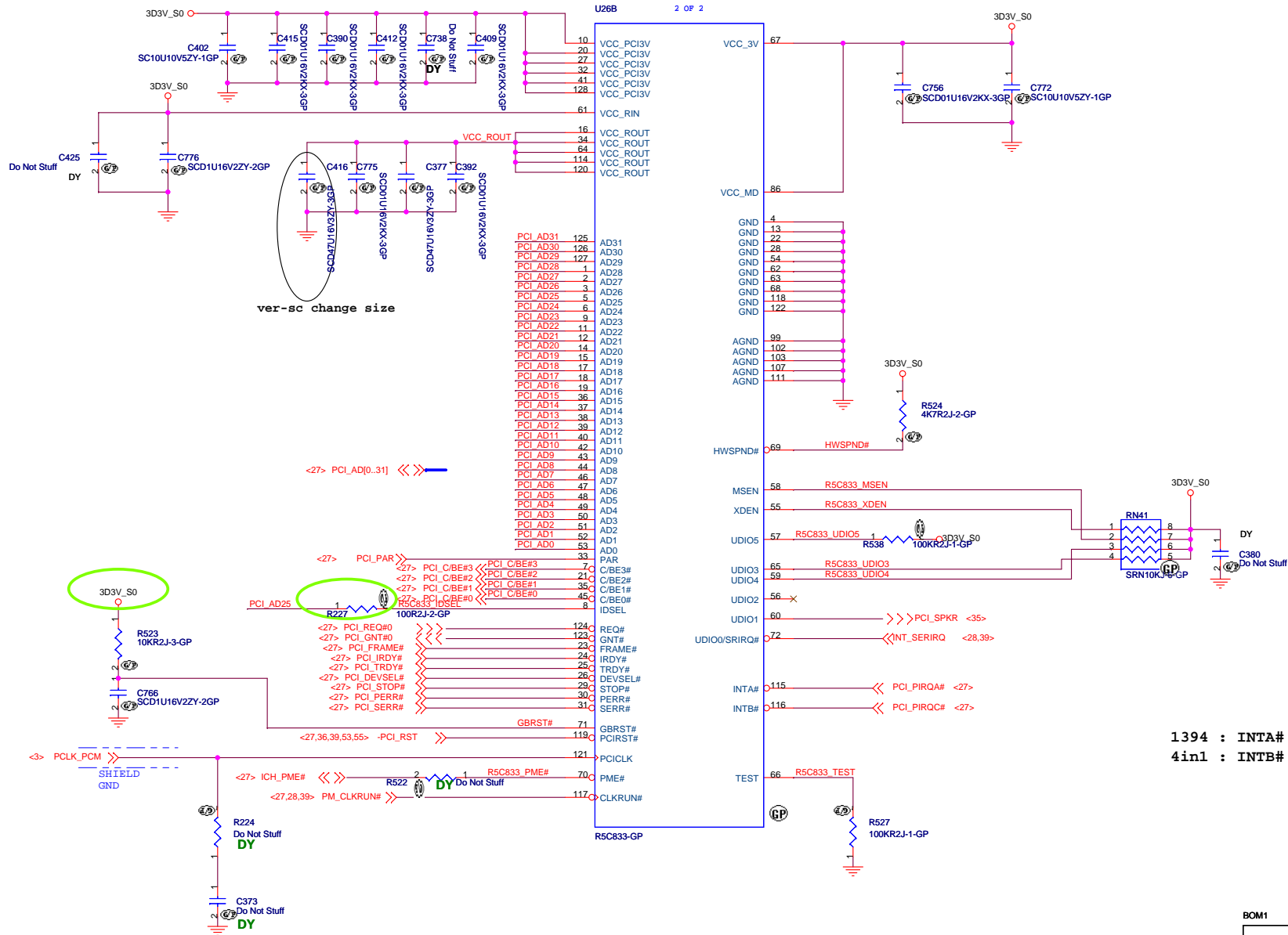


Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

SATA HD Connector

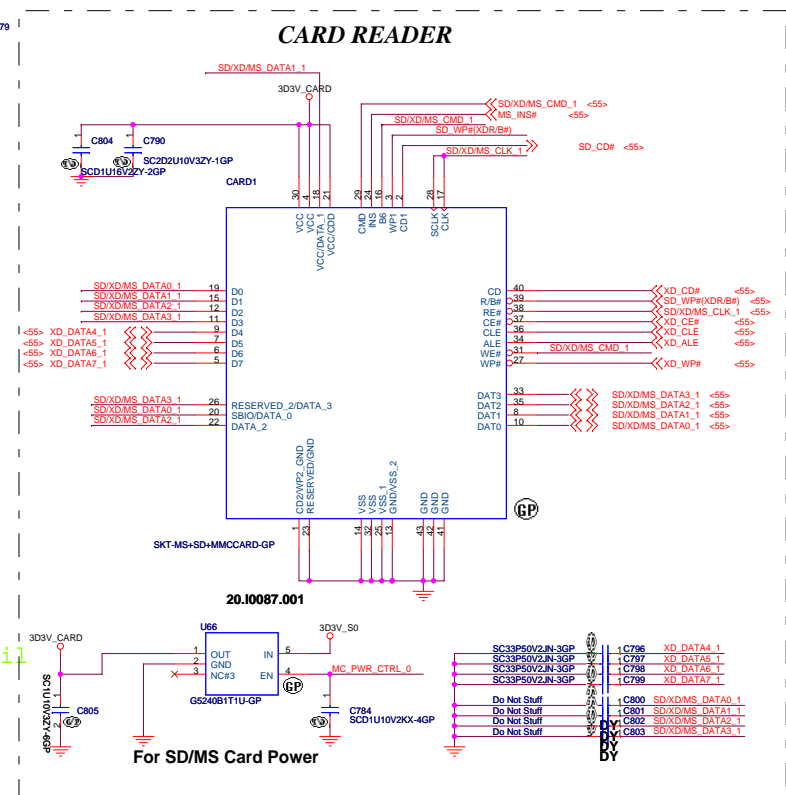


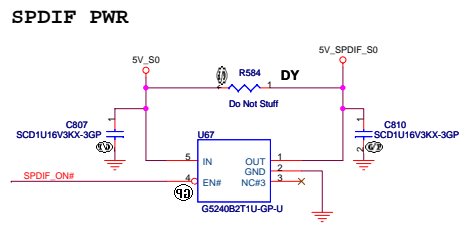
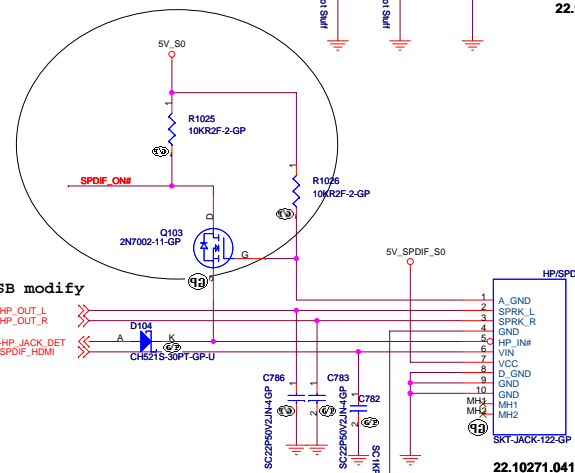
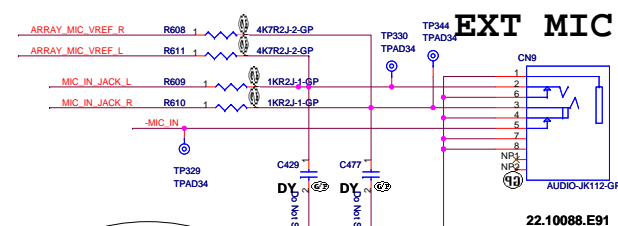
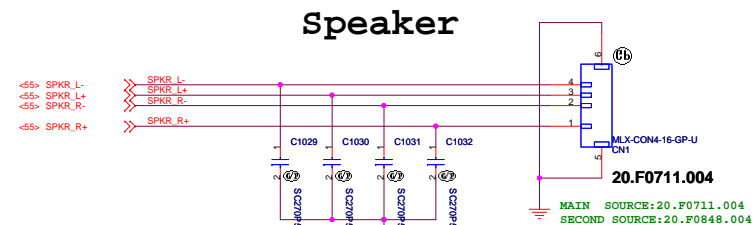


BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

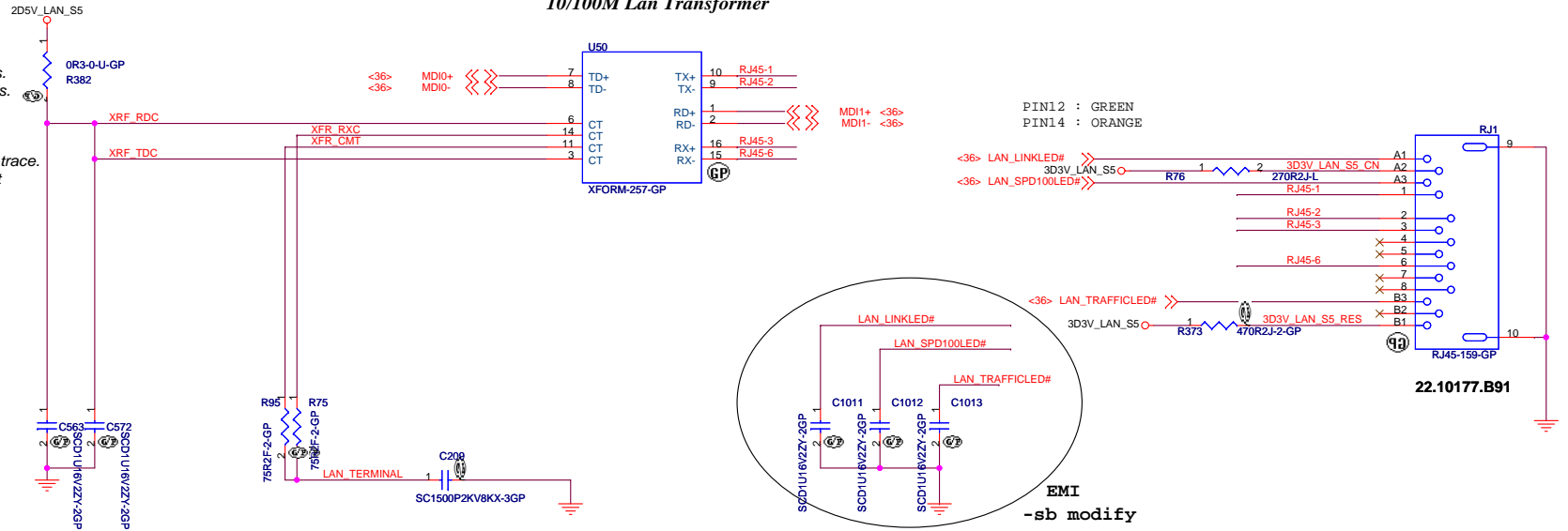
R5C832/PCI		
Size	Document Number	Rev
A3	LT32M	-3
Date:	Monday, July 07, 2008	Sheet 33 of 54





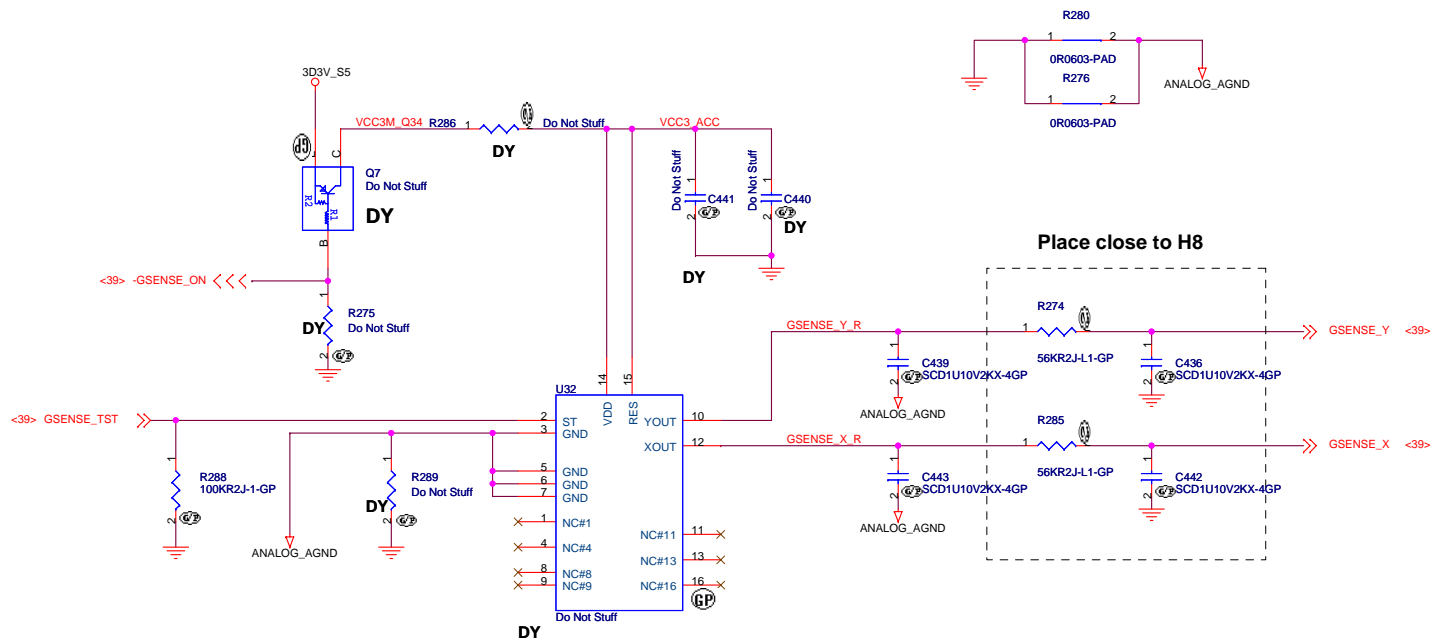
10/100M Lan Transformer

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LAN connector/NEW CARD/SIM			
Size	Document Number	Rev	
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Primary : STMicro LIS244AL
2nd: ADI ADXL322

Width = 6 mil & Spacing = 10 mil
for three Output traces

	ADXL322 LIS244AL	No Accel
R545	NO_ASM	ASM
R547	ASM	ASM
All other	ASM	NO_ASM

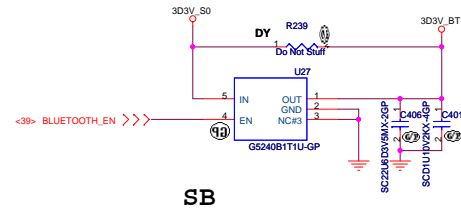
Layout Comment :

- (1) Place C439, C443, Q7, R286, R275, C441, C440, R288, R289 close to U32.
- (2) Avoid routing under DCDC switching area.

BOM1

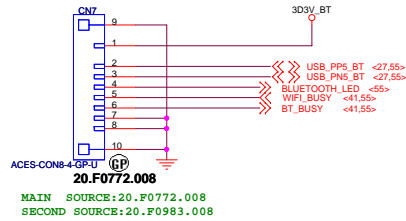
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title G-SENSOR		
Size A3	Document Number LT32M	Rev -3
Date: Monday, July 07, 2008	Sheet 38 of 54	



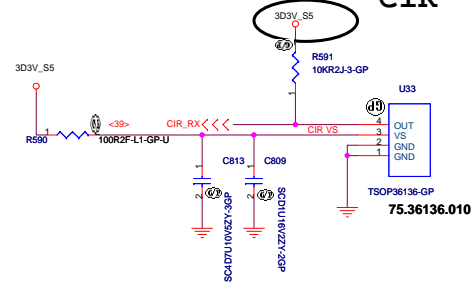


SB

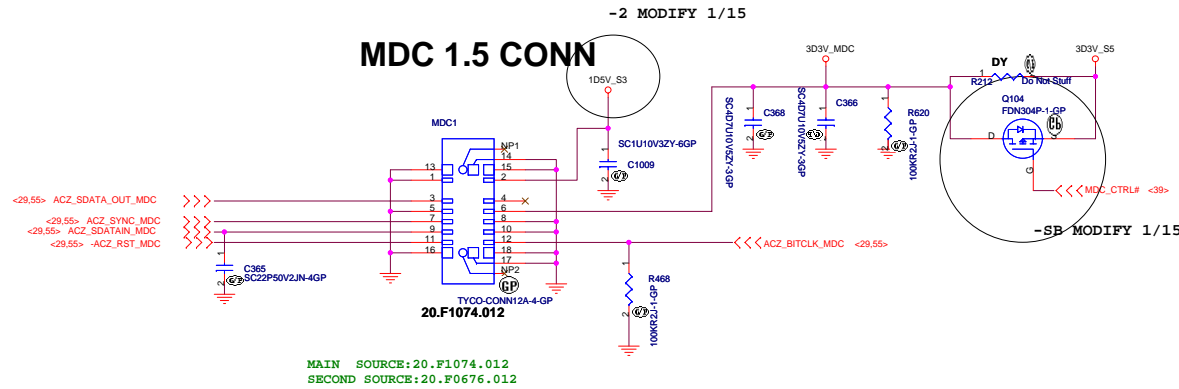
BT CONNECTOR



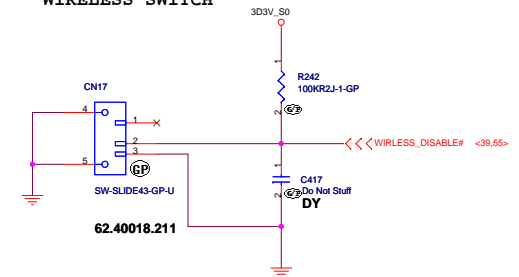
CIR



MDC 1.5 CONN



WIRELESS SWITCH



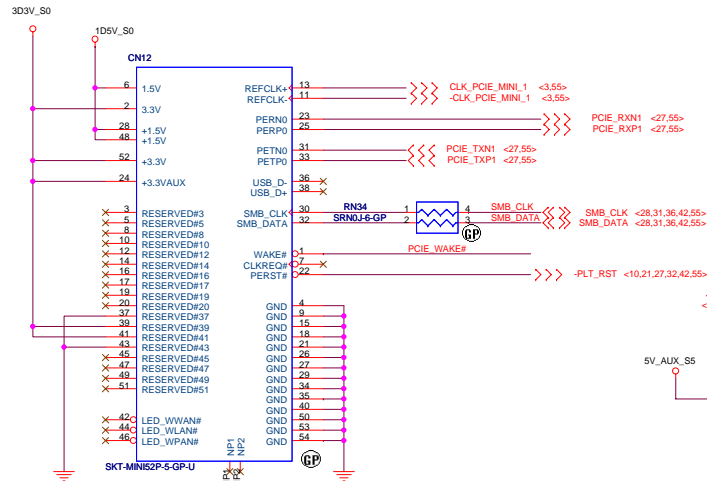
BOM#

Mini PCI-E Connector

Only port-1 support USB

For Robson

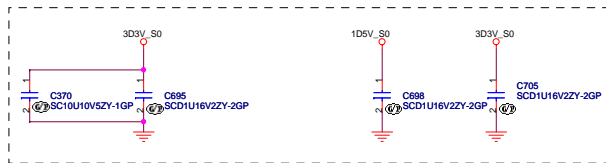
Port-1 High



20.F0832.052

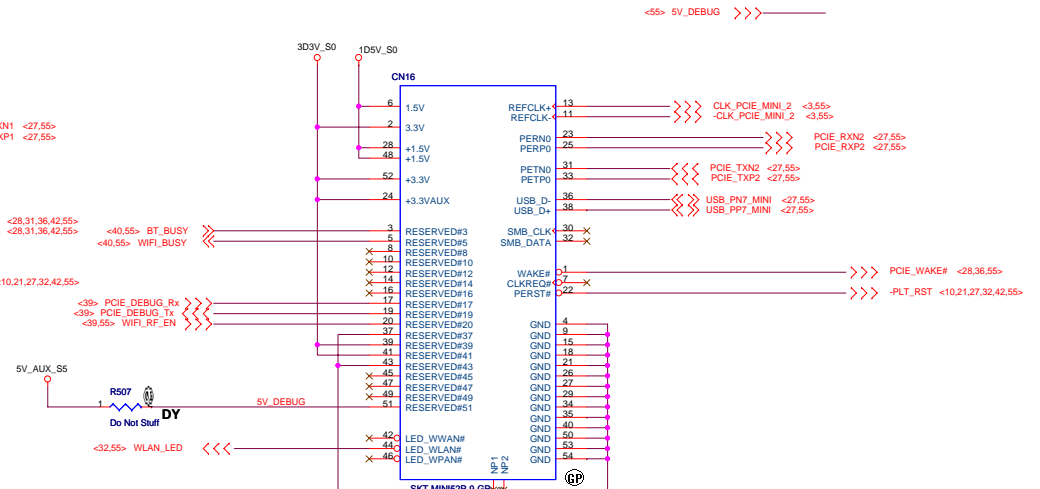
MAIN SOURCE: 20.F0832.052

SECOND SOURCE: 20.F1107.052



Mini PCI-E Connector

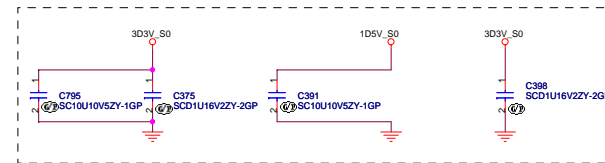
Port-2 low



62.10043.411

MAIN SOURCE: 62.10043.411

SECOND SOURCE: 20.F1084.052



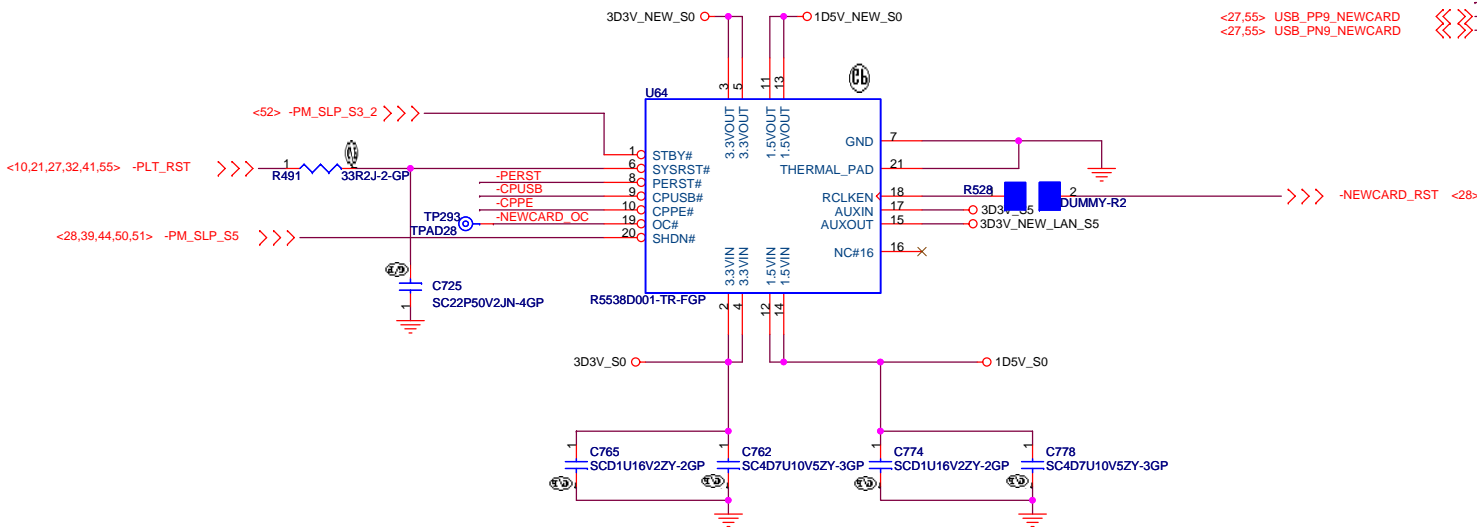
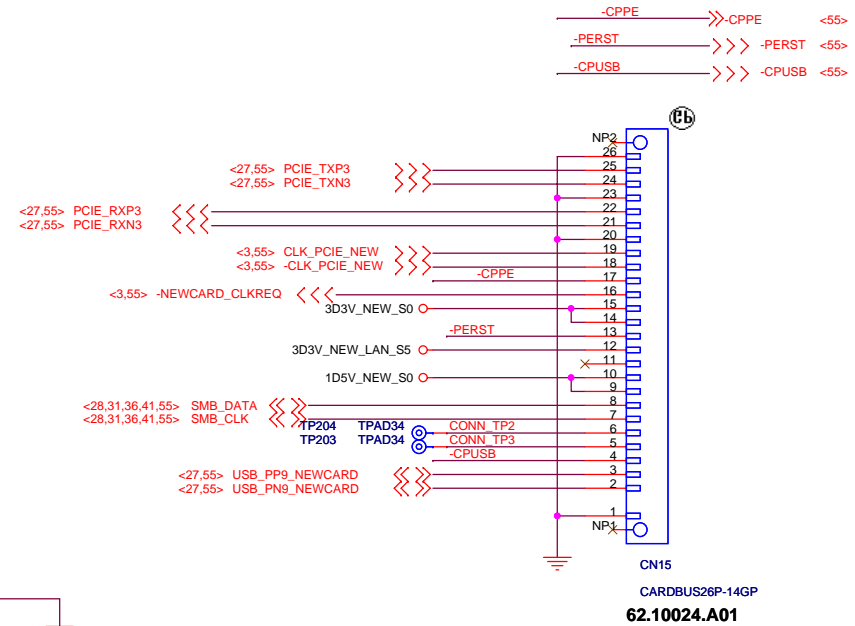
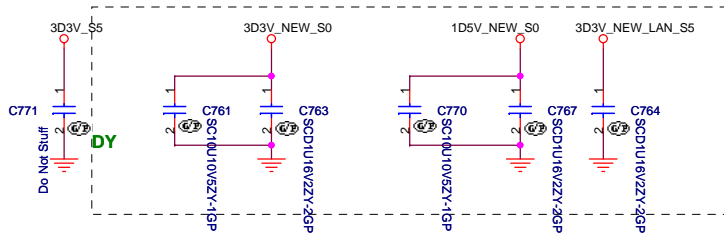
BOM1

NEWCARD Connector

For Newcard socket

Place them Near to Chip

Place them Near to Connector



BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Module NewCard	
Size Document Number LT32M	Rev -3
Date: Monday, July 07, 2008	
Sheet 42 of 54	

1394

ACES-CON5-GP

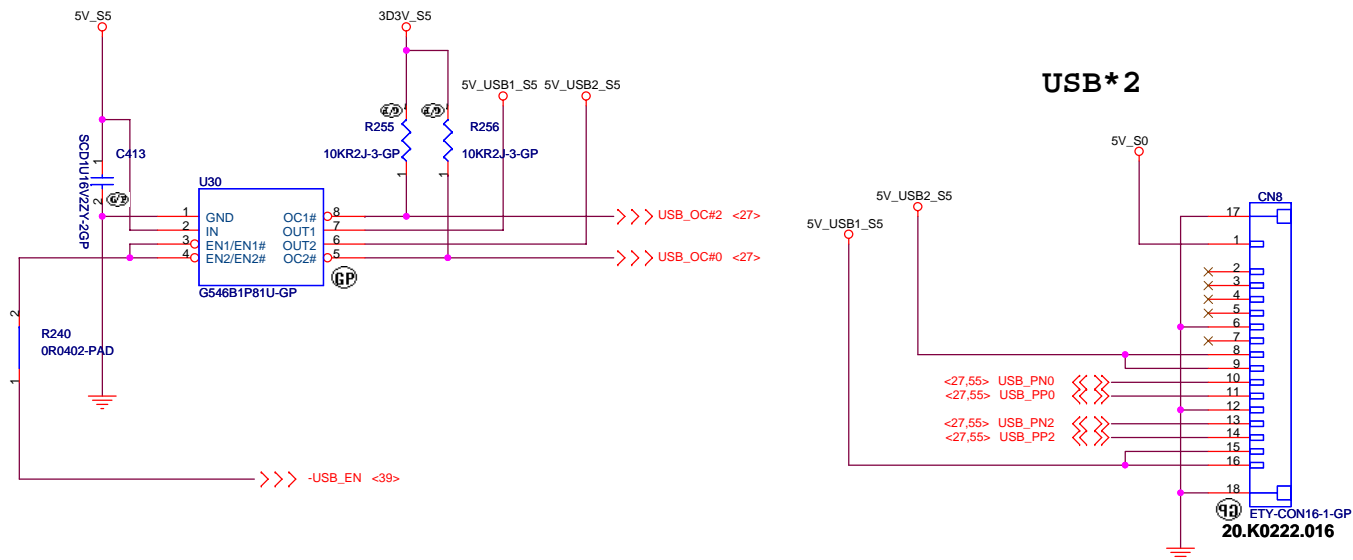
(dB)

5
4
3
2
1
6

CN5

<34,55> TPA0P <<<
<34,55> TPA0N >>>
<34,55> TPB0P >>>
<34,55> TPB0N >>>

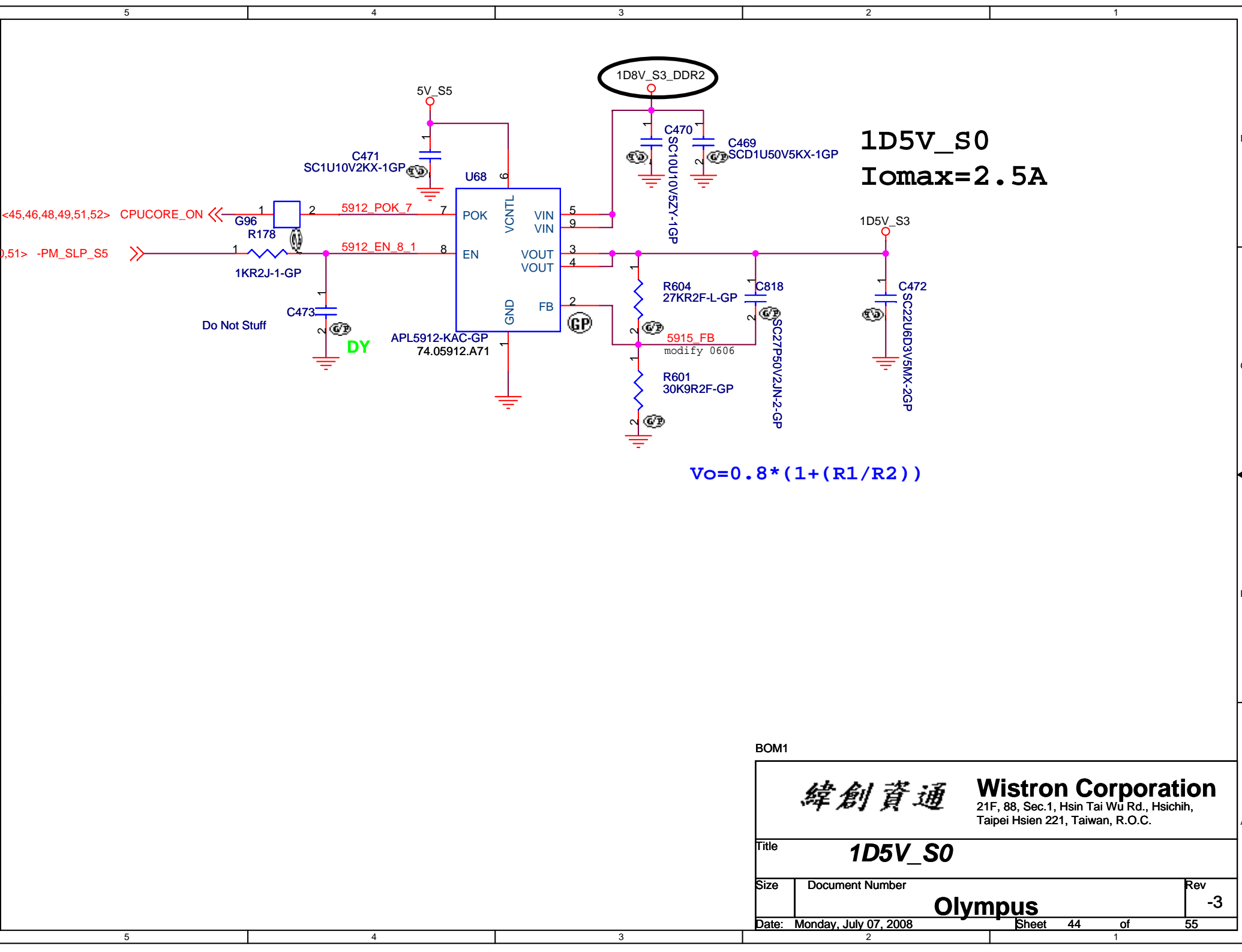
MAIN SOURCE:20.k0196.005
SECOND SOURCE:20.k0212.008



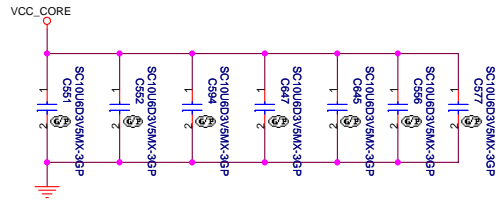
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
USB I/O & 1394 CNN			
Size B	Document Number		Rev
	LT32M		-3
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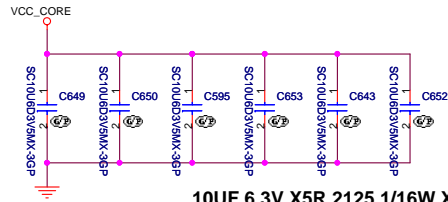
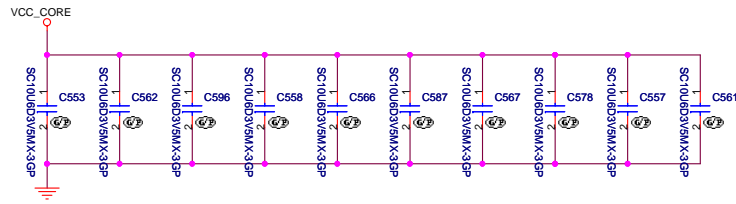
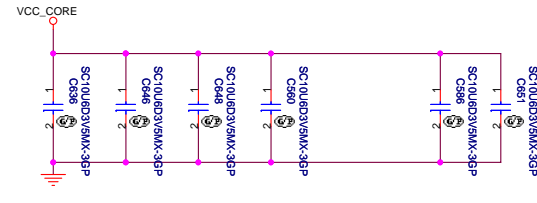
D
C
B
A



D
C
B
A



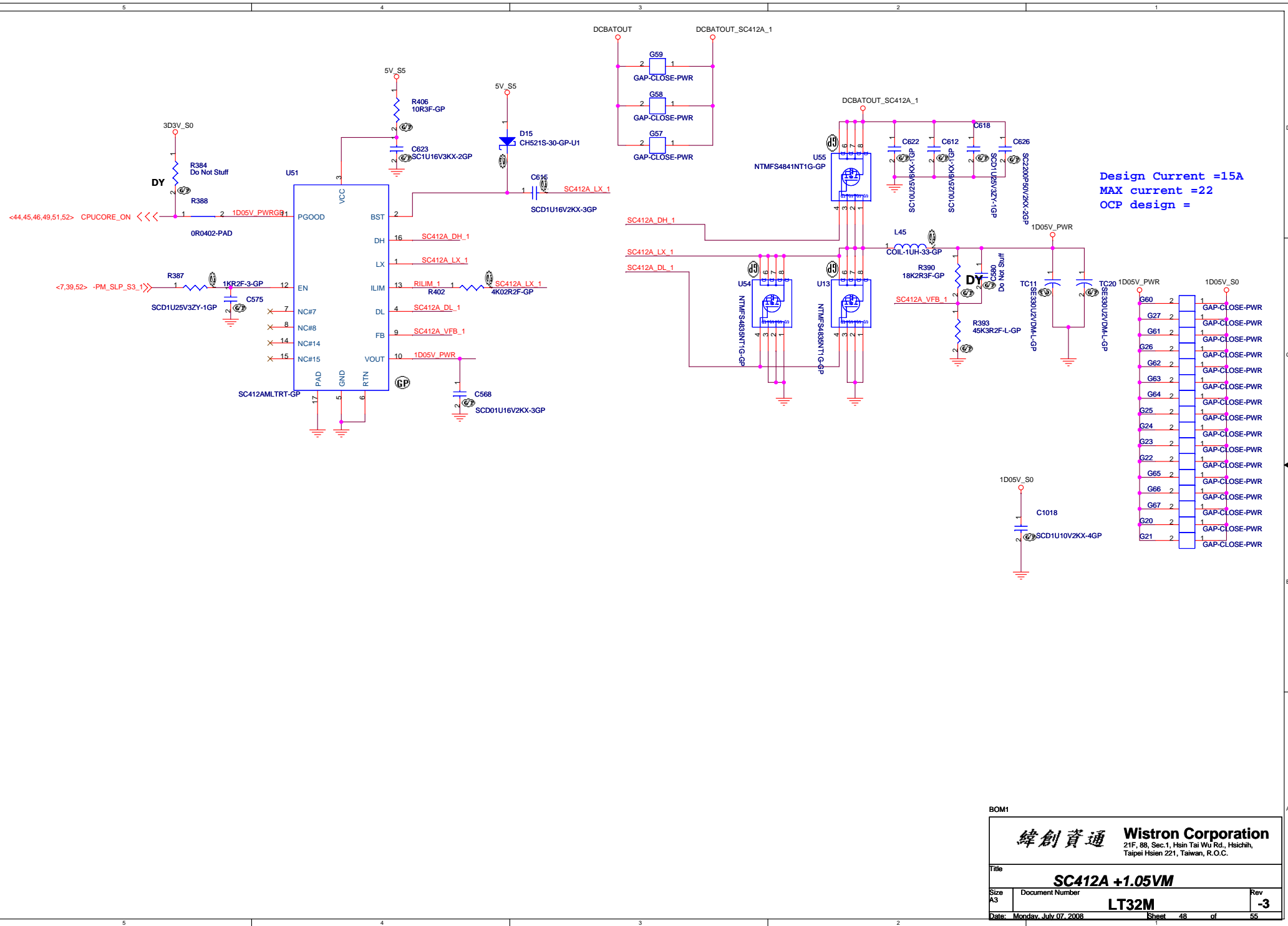
10UF 6.3V X5R 2125 1/16W X16 PCS

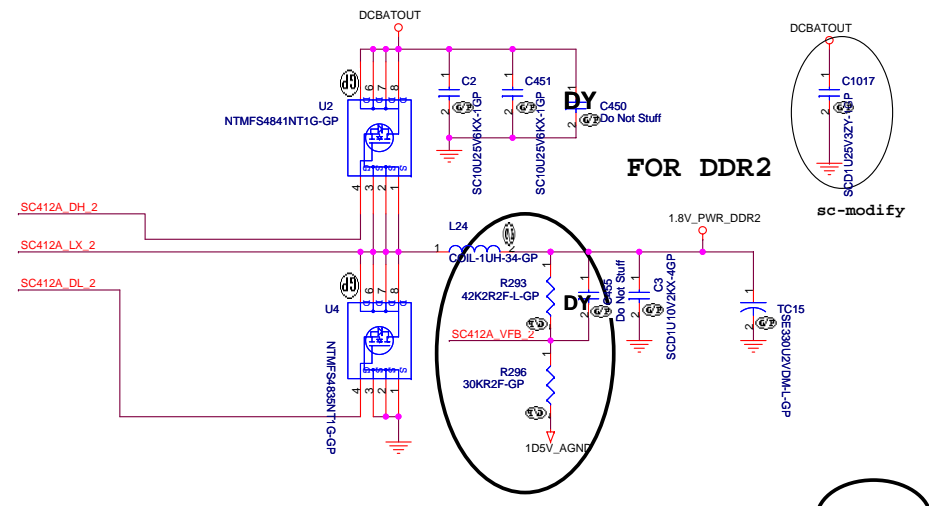


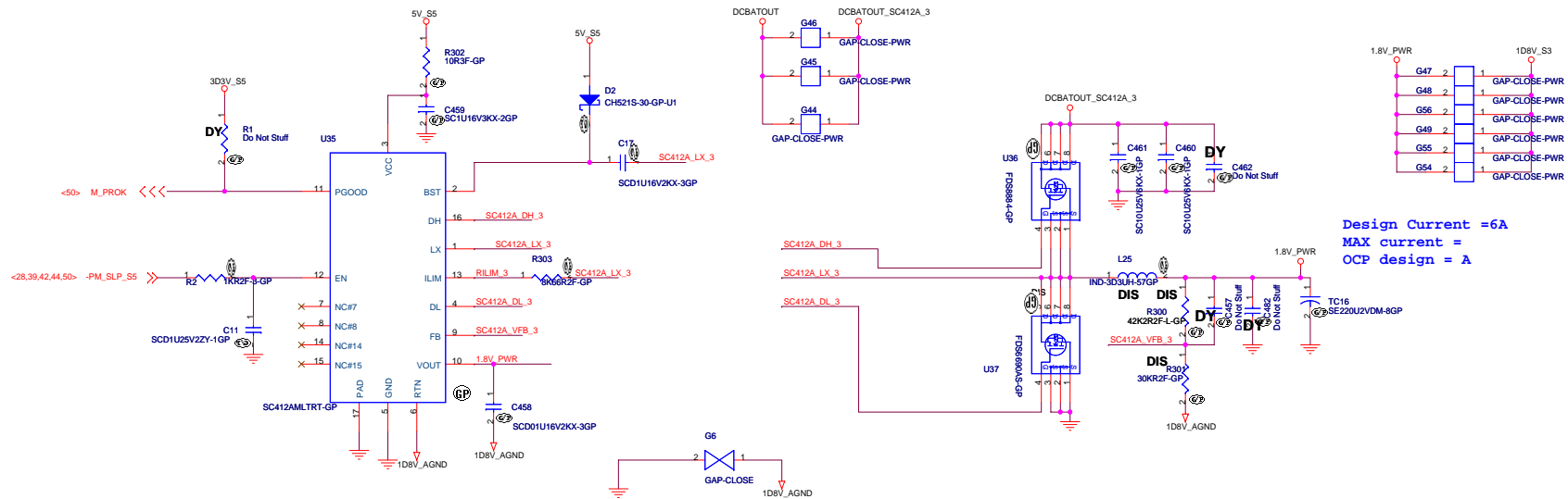
10UF 6.3V X5R 2125 1/16W X16 PCS

BOM1

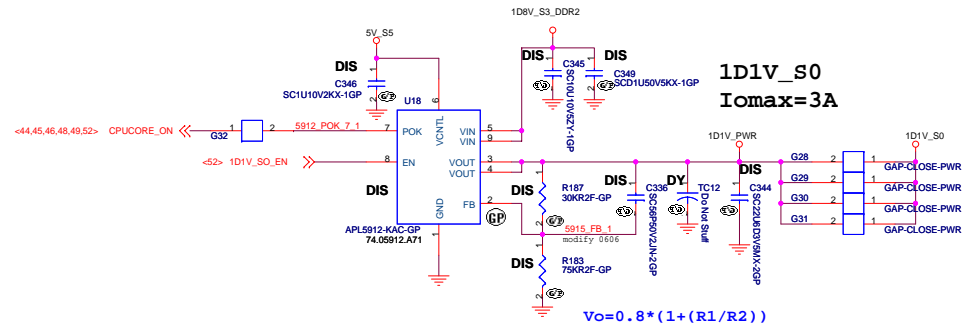
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
VCCCPUCORE DECOUPLING			
Size Custom	Document Number LT32M	Rev -3	
Date: Monday, July 07, 2008	Sheet 47	of	55



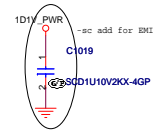




Design Current =6A
MAX current =
OCP design = A



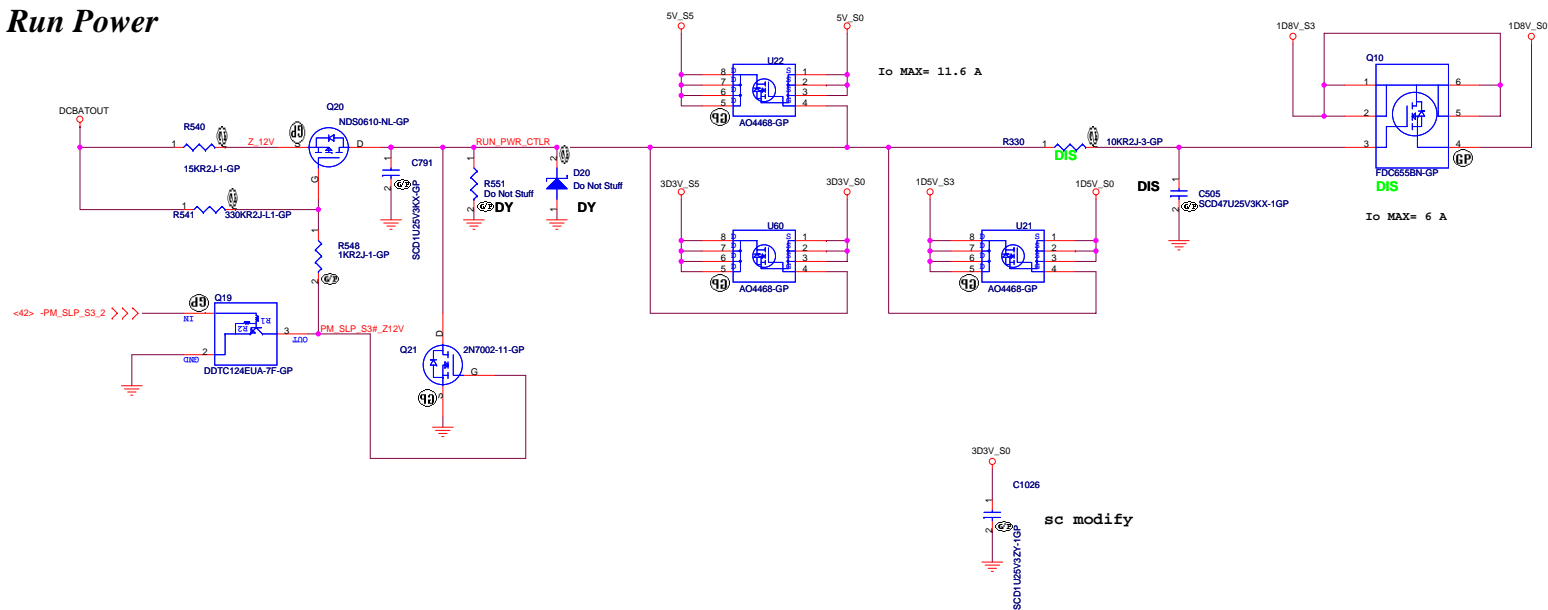
$$V_o = 0.8 * (1 + (R1/R2))$$

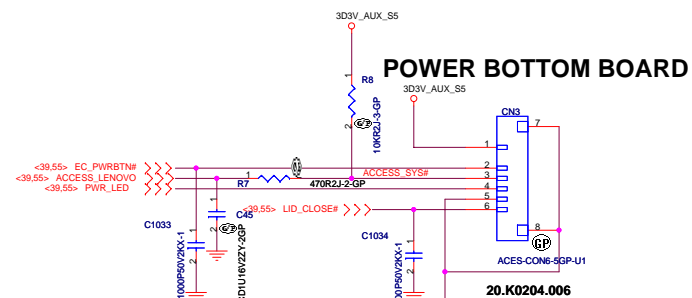


BOM1

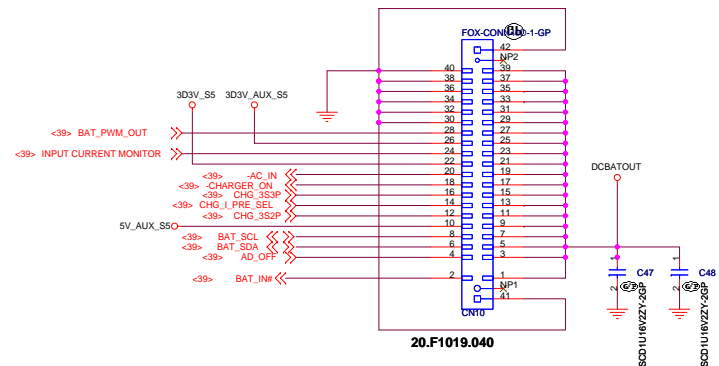
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title		SC412A 1.8V/1.1V	
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Run Power





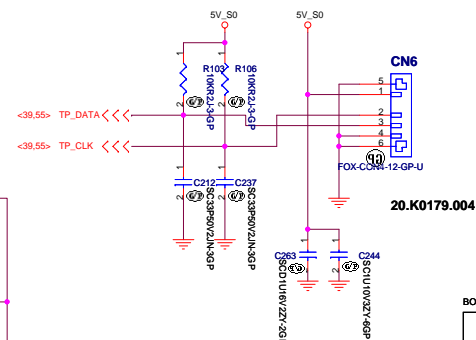
POWER BOTTOM BOARD

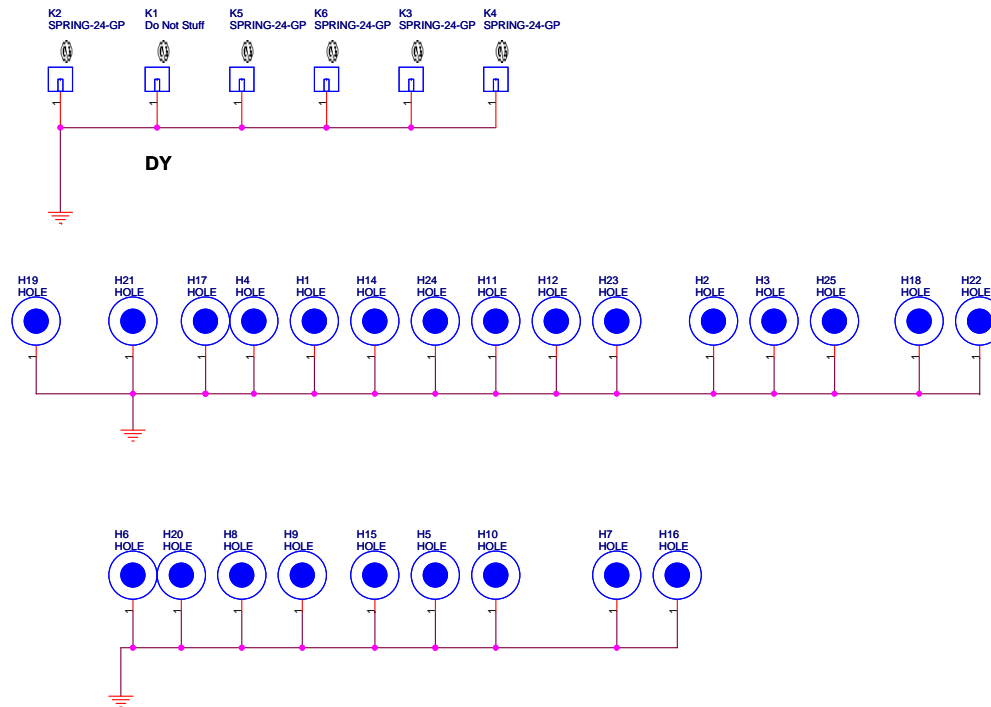


CHARGER CONNECTOR



TouchPad Connector





BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
PTH FOR SCREW HOLES			
Size	Document Number		Rev
Custom	LT32M		-3
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