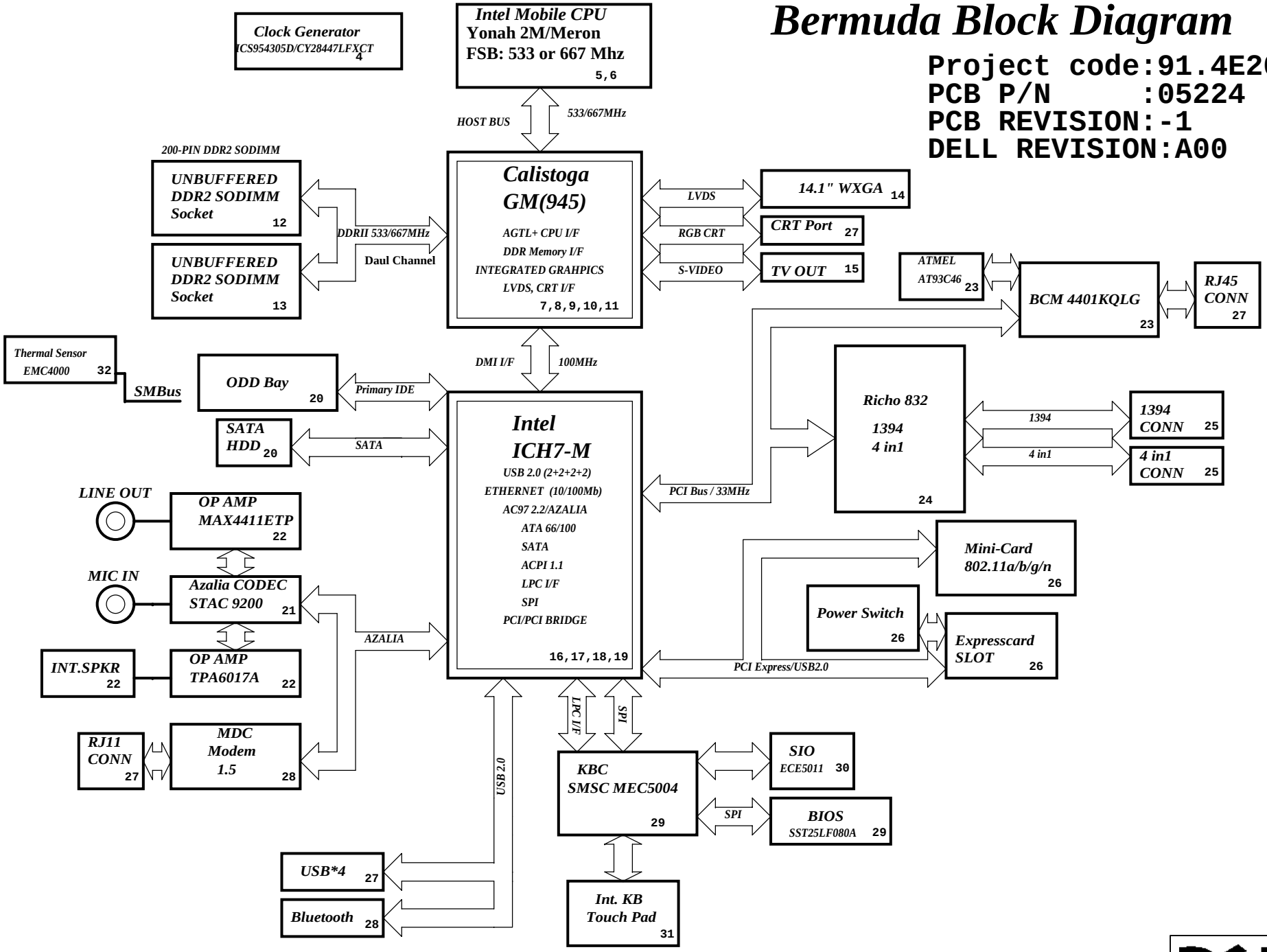
Bermuda Block Diagram

Project code:91.4E201.001
PCB P/N :05224
PCB REVISION:-1
DELL REVISION:A00



System DC/DC TPS51120 39	
INPUTS	OUTPUTS
PWR_SRC	+5VSUS +3VSUS
Battery Charger MAX8731 42	
PWR_SRC	BATT+
System DC/DC TPS51483 40	
PWR_SRC	+1.05VRUN +1.5VRUN
CPU DC/DC ADP3207 +ADP3419 38	
PWR_SRC	VCC_CORE
DDR2 DC/DC SC480 41	
PWR_SRC	+1.8VSUS +0.9VRUN +0.9VSUS_DDR2VREF

PCB LAYER
L1:TOP
L2:GND
L3:Signal
L4:Signal
L5:VCC
L6:Signal
L7:GND
L8:BOT

1208-1500

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Title: System Block Diagram
Size: A3 | Document Number: Bermuda | Rev: -1
Date: Wednesday, March 01, 2006 | Sheet 1 of 45

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ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

Calistoga Strapping Signals and Configuration

* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation *	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation *

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

954305D 27Mhz/LCDCLK Spread and Frequency Selection Table

page 3

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	0	1	-1.25 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+-0.25 Center
1	0	0	1	+-0.5 Center
1	0	1	0	+-0.75 Center
1	0	1	1	+-1.0 Center
1	1	0	0	+-0.25 Center
1	1	0	1	+-0.5 Center
1	1	1	0	+-0.75 Center
1	1	1	1	+-1.0 Center

PCI Routing

page 16

	IDSEL	IRQ	REQ/GNT
R5C832	AD17		
LAN	AD16		

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

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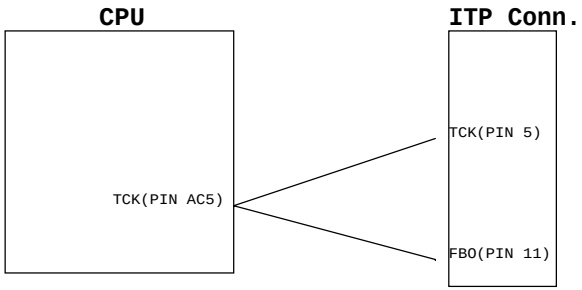
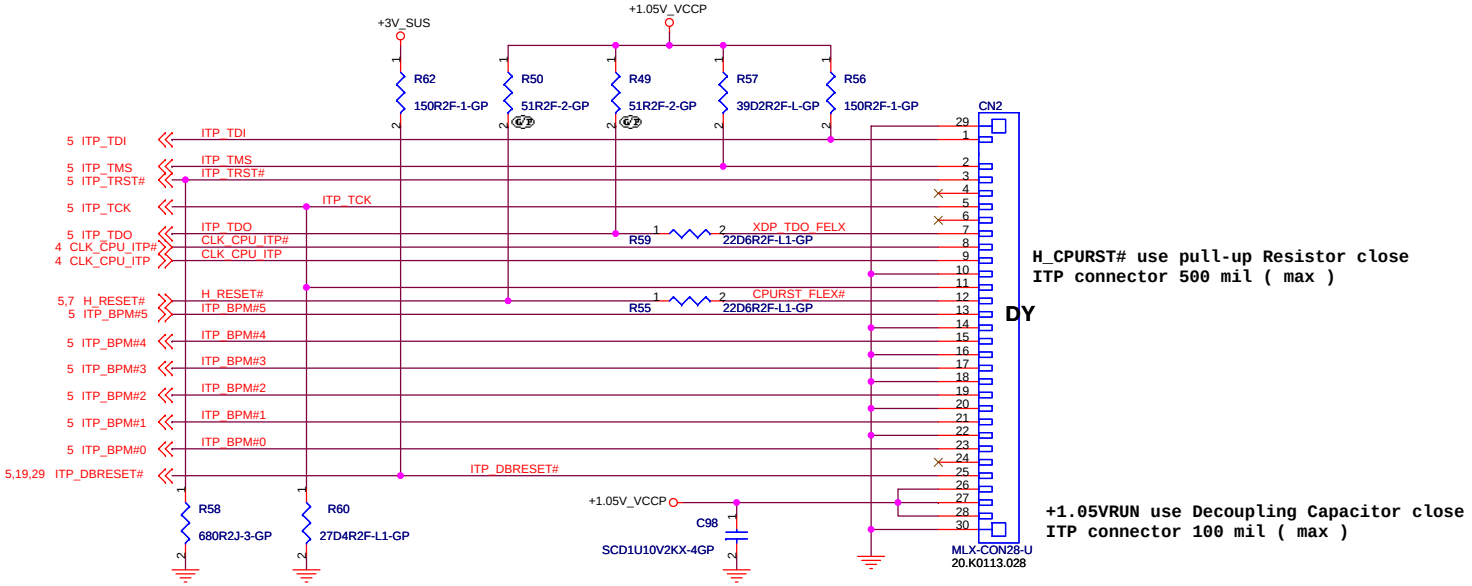
Title: Table of Content

Size: A3 | Document Number: Bermuda | Rev: -1

Date: Wednesday, March 01, 2006 | Sheet 2 of 45





H_CPURST# use pull-up Resistor close ITP connector 500 mil (max)

+1.05VRUN use Decoupling Capacitor close ITP connector 100 mil (max)

ITP Debug Conn.

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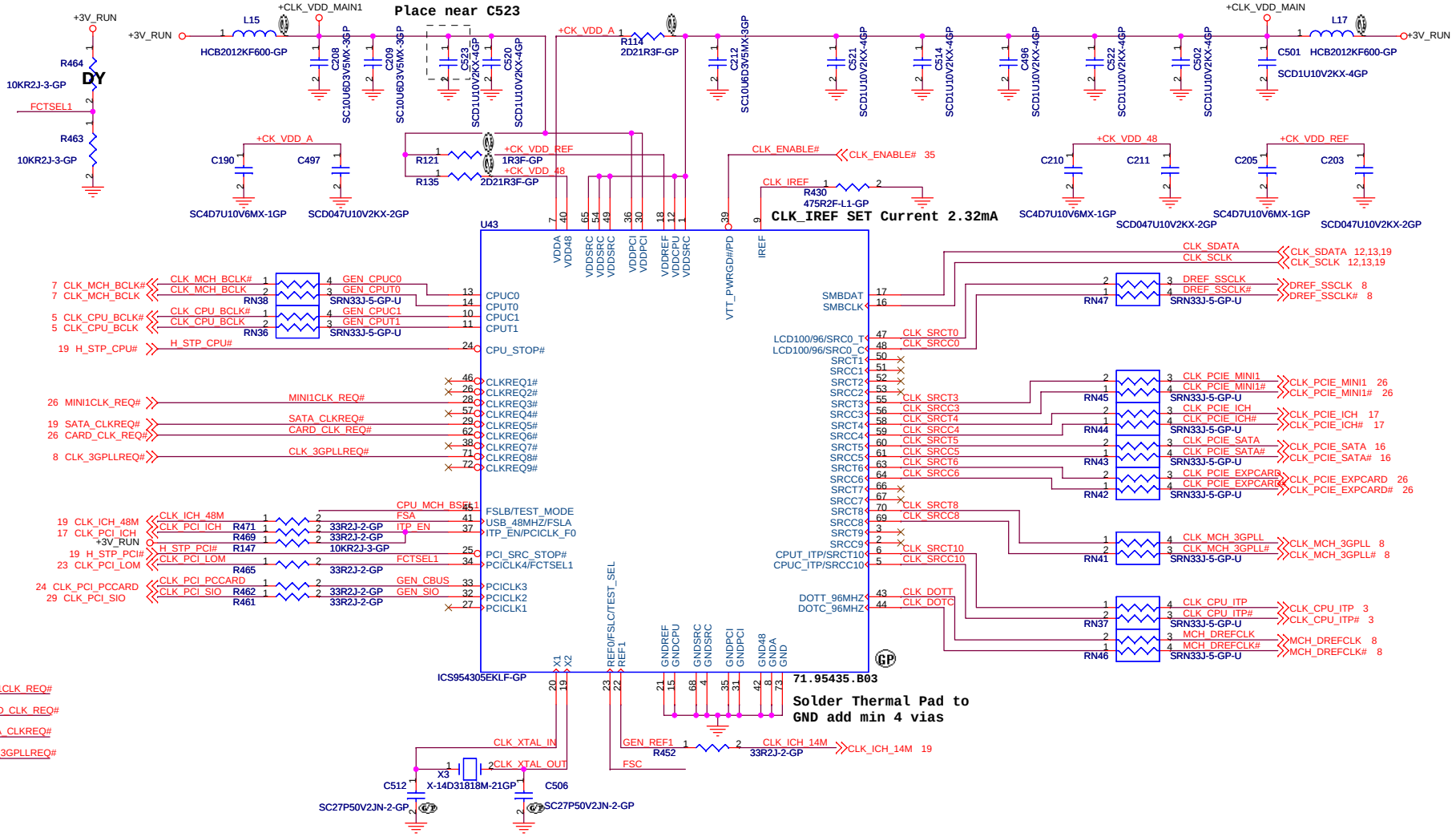
Title	ITP Debug	
Size A3	Document Number Bermuda	Rev -1
Date: Wednesday, March 01, 2006	Sheet 3 of 45	

PIN34 FCTSEL1	0	1
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRC0_T
PIN48	LCD100/96C	SRC0_C



SEL2	SEL1	SEL0	CPU	FSB
0	0	0	266M	X
0	0	1	133M	533M
0	1	0	200M	X
0	1	1	166M	667M
1	0	0	333M	X
1	0	1	100M	X
1	1	0	400M	X
1	1	1	Reserved	X

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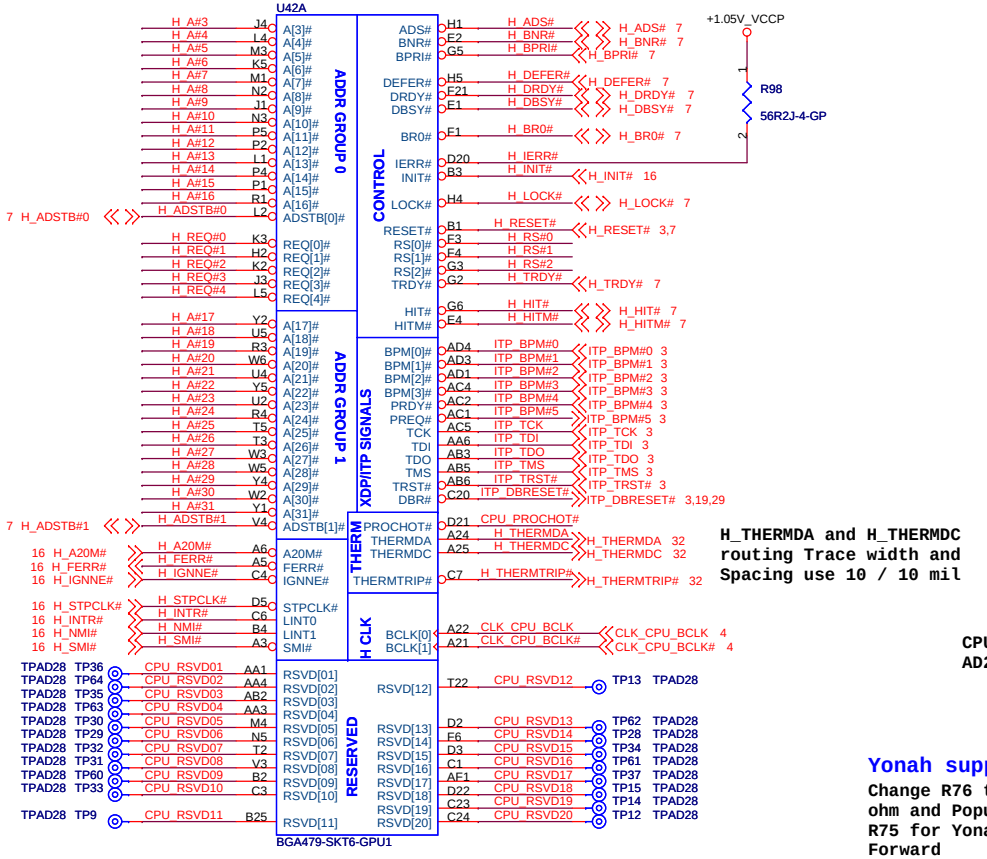
Title: Clock Generator

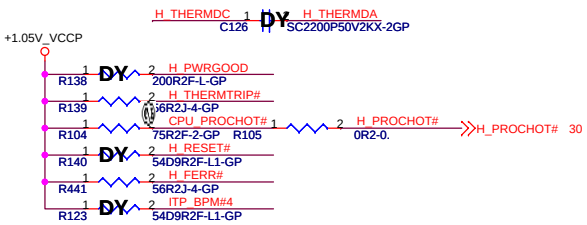
Size: A3 | Document Number: Bermuda | Rev: -1

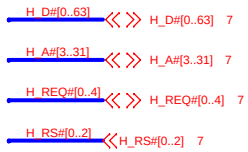
Date: Wednesday, March 01, 2006 | Sheet 4 of 45

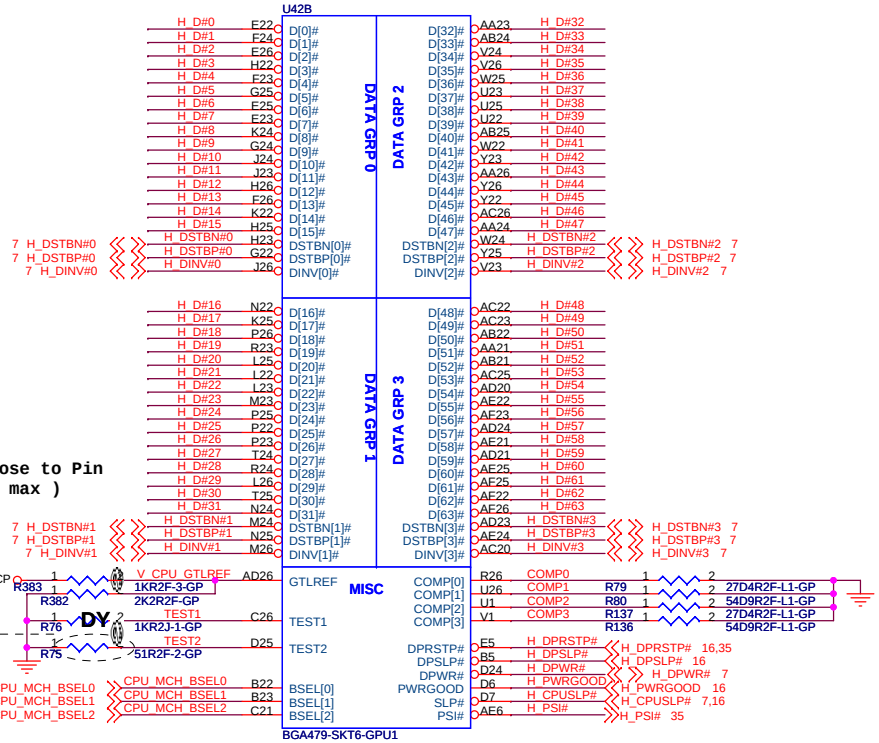


H_THERMDA and H_THERMDC routing Trace width and Spacing use 10 / 10 mil

C126 close to Pin A24 and Pin A25







CPU_GTLREF0 close to Pin AD26 500 mil (max)

Yonah support

Change R76 to 51 ohm and Populate R75 for Yonah B0 Forward

CPU_SEL	H_SEL0	H_SEL1	H_SEL2
133	0	0	1
166	0	1	1

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal.Trace should be No Longer than 500 mils

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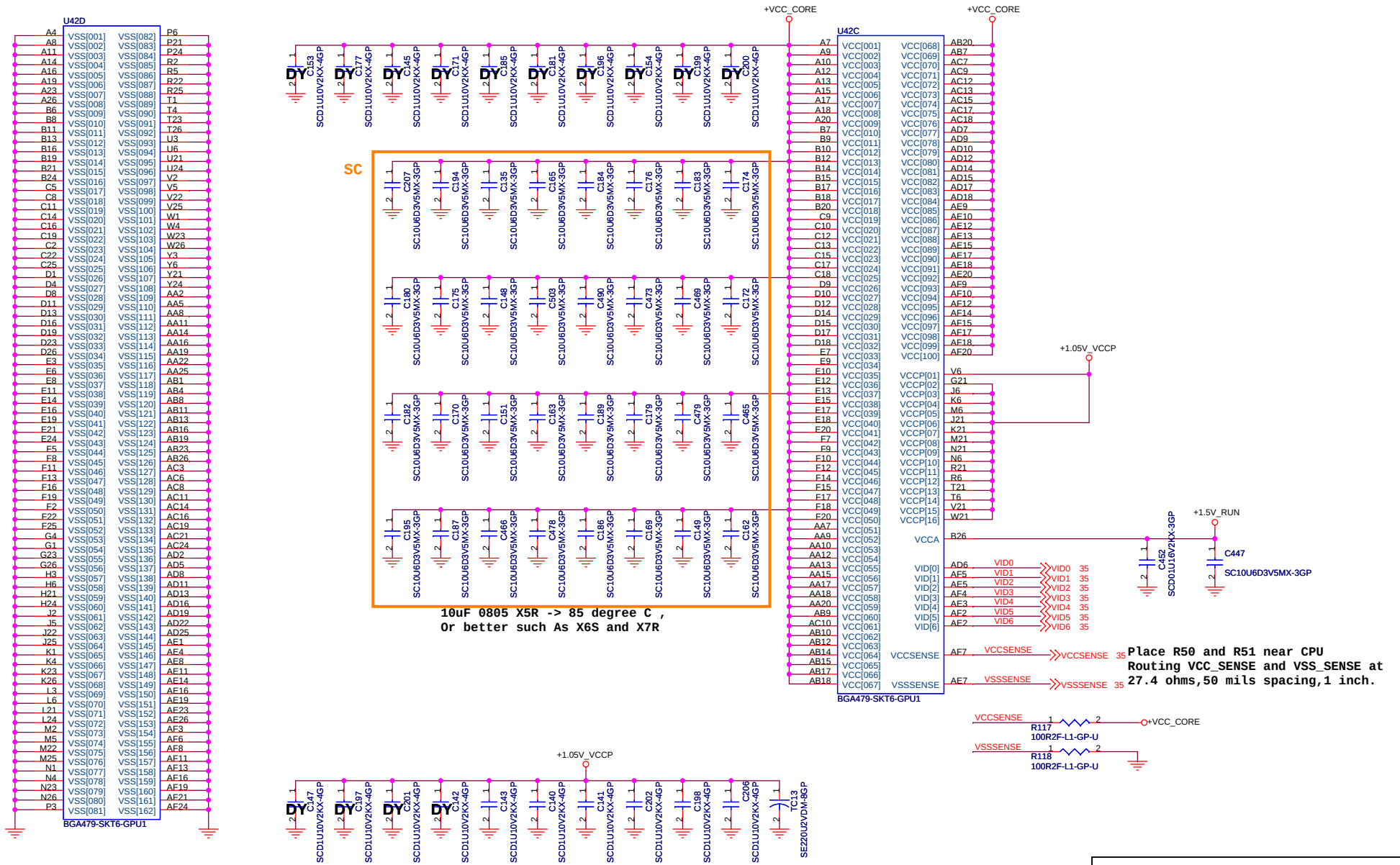
Title: CPU - 01 - Yonah - FSB

Size: A3 | Document Number: Bermuda | Rev: -1

Date: Wednesday, March 01, 2006 | Sheet 5 of 45



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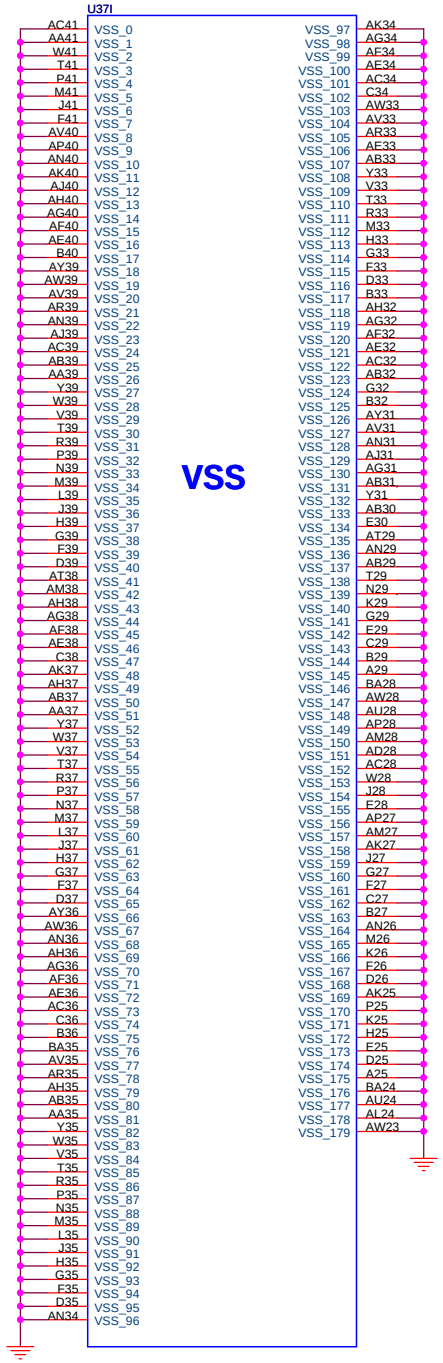
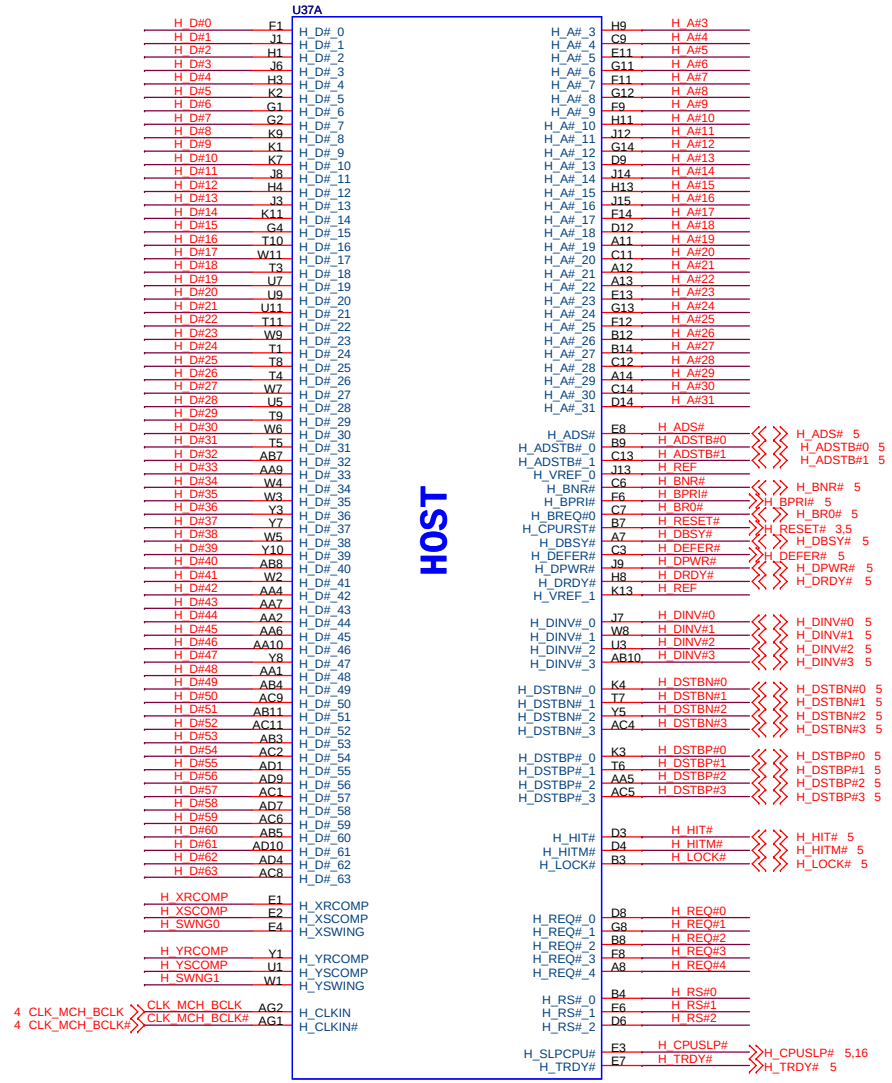
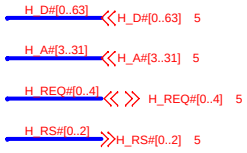
Title: CPU - 02 - Yonah - POWER

Size: A3 | Document Number: Bermuda | Rev: -1

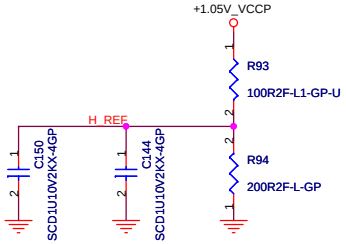
Date: Wednesday, March 01, 2006 | Sheet 6 of 45



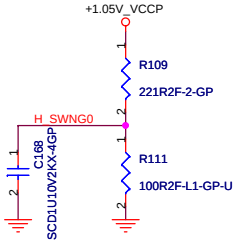




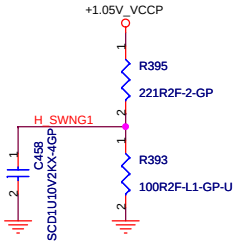
H_REF Decoupling Capacitors close Caliistoga 100 mil



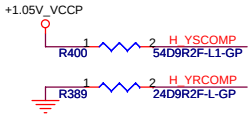
H_XSWING and H_YSWING routing Trace width and Spacing use 10 / 20 mil



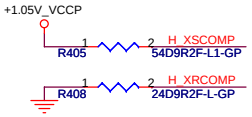
H_XSWING and H_YSWING Resistors and Capacitors close Caliistoga 500 mil (MAX)



H_XRCOMP and H_YRCOMP routing Trace width and Spacing use 10 / 20 mil



H_XSCOMP and H_YSCOMP Resistors and Capacitors close Caliistoga 500 mil (MAX)



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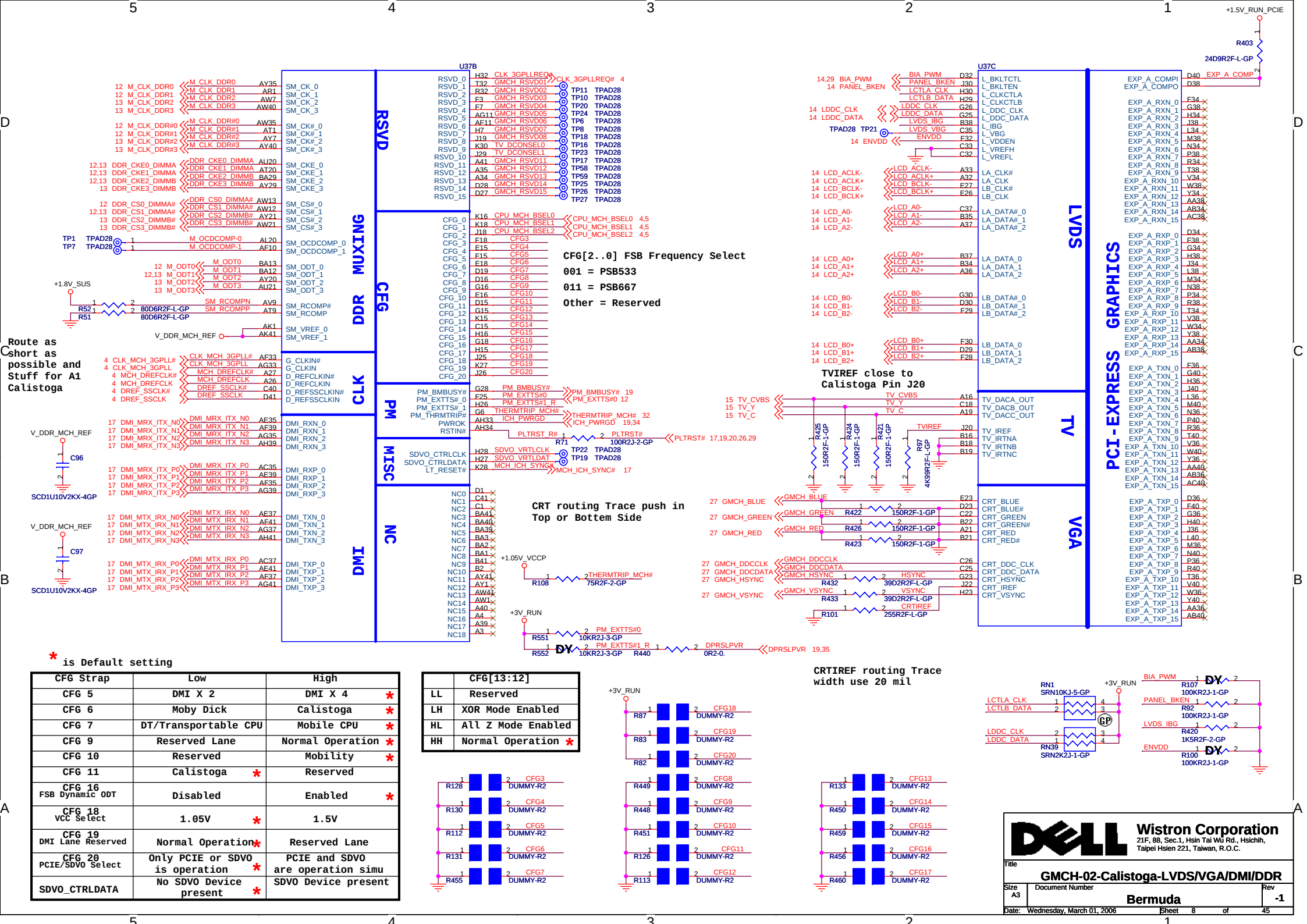
Title: **GMCH - 01 - Calistoga - FSB**

Size: A3 | Document Number: **Bermuda** | Rev: -1

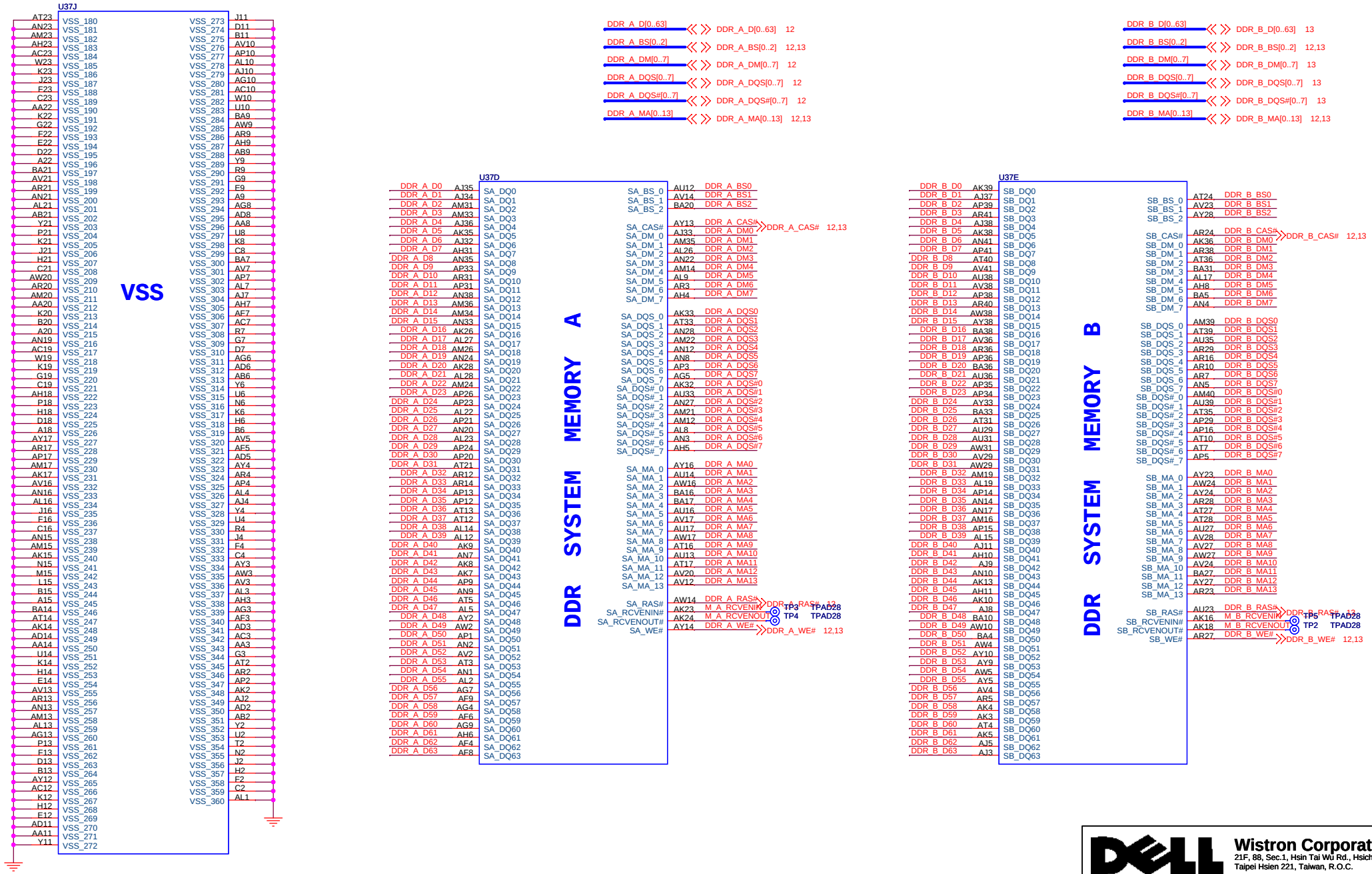
Date: Wednesday, March 01, 2006 | Sheet 7 of 45



* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation *	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation *



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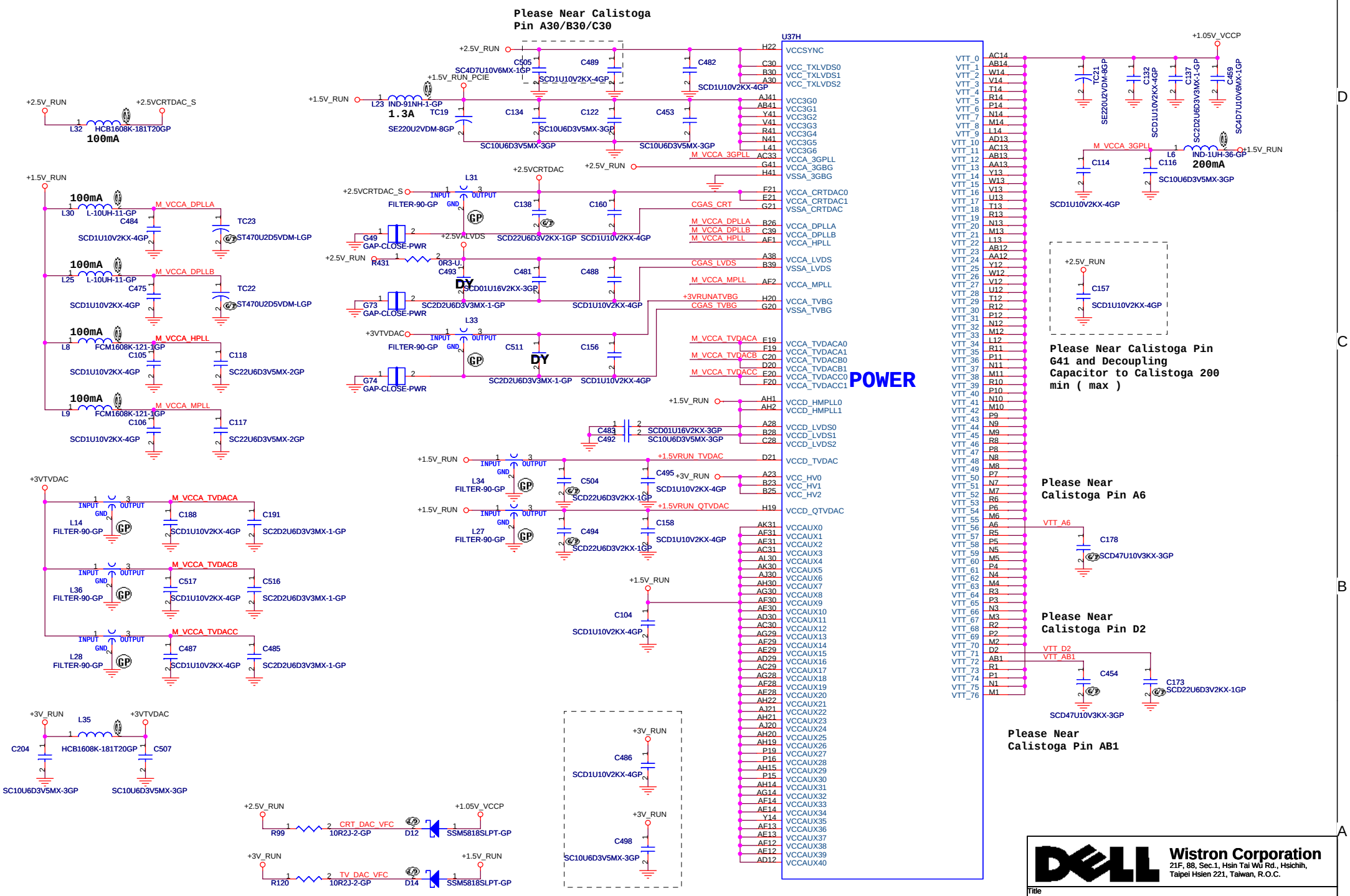
Title: **GMCH - 03 - Calistoga - DDR**

Size: A3 | Document Number: **Bermuda** | Rev: -1

Date: Wednesday, March 01, 2006 | Sheet 9 of 45



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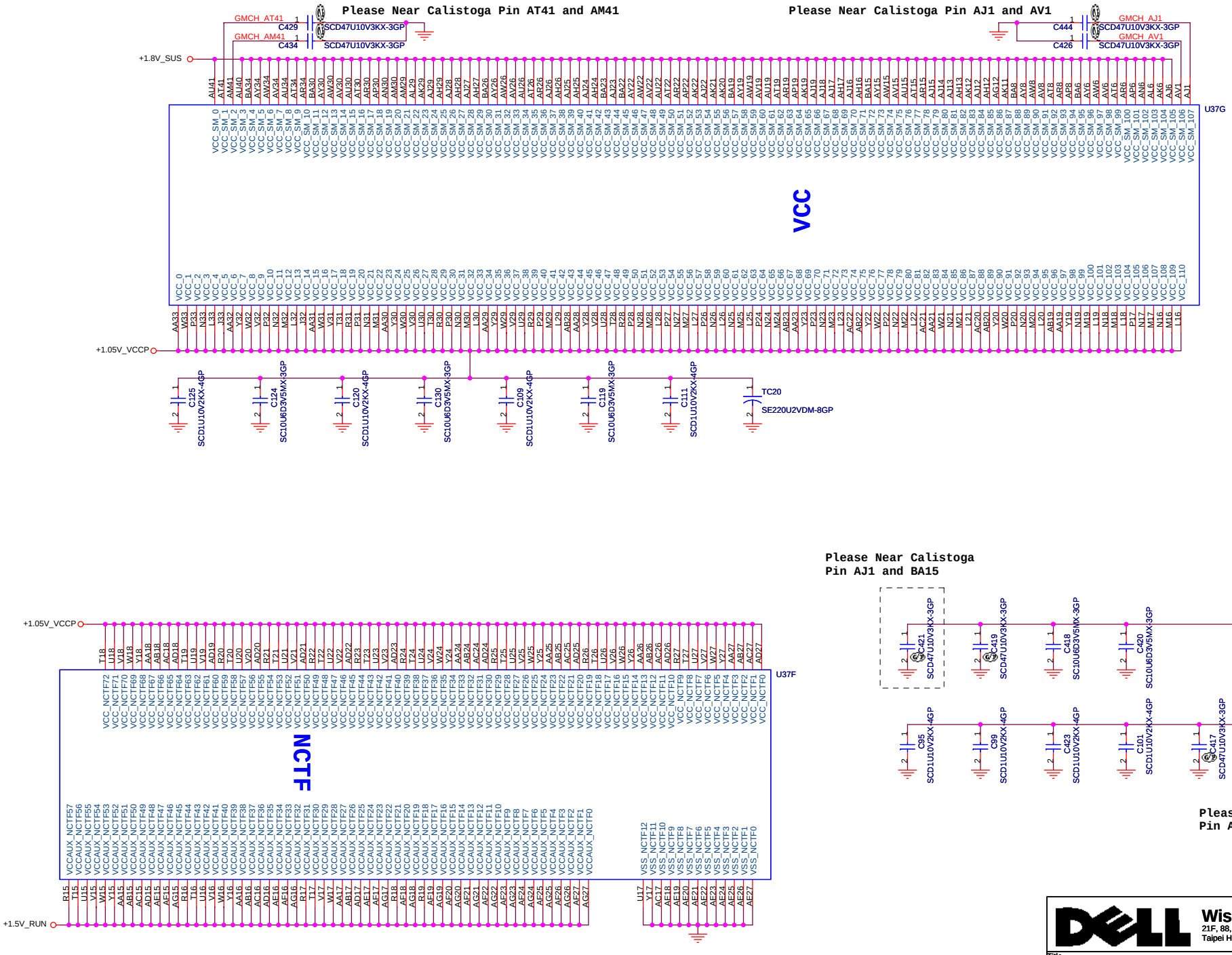
Title: GMCH - 04 - Calistoga - POWER/FILTER

Size: A3 | Document Number: Bermuda | Rev: -1

Date: Wednesday, March 01, 2006 | Sheet 10 of 45



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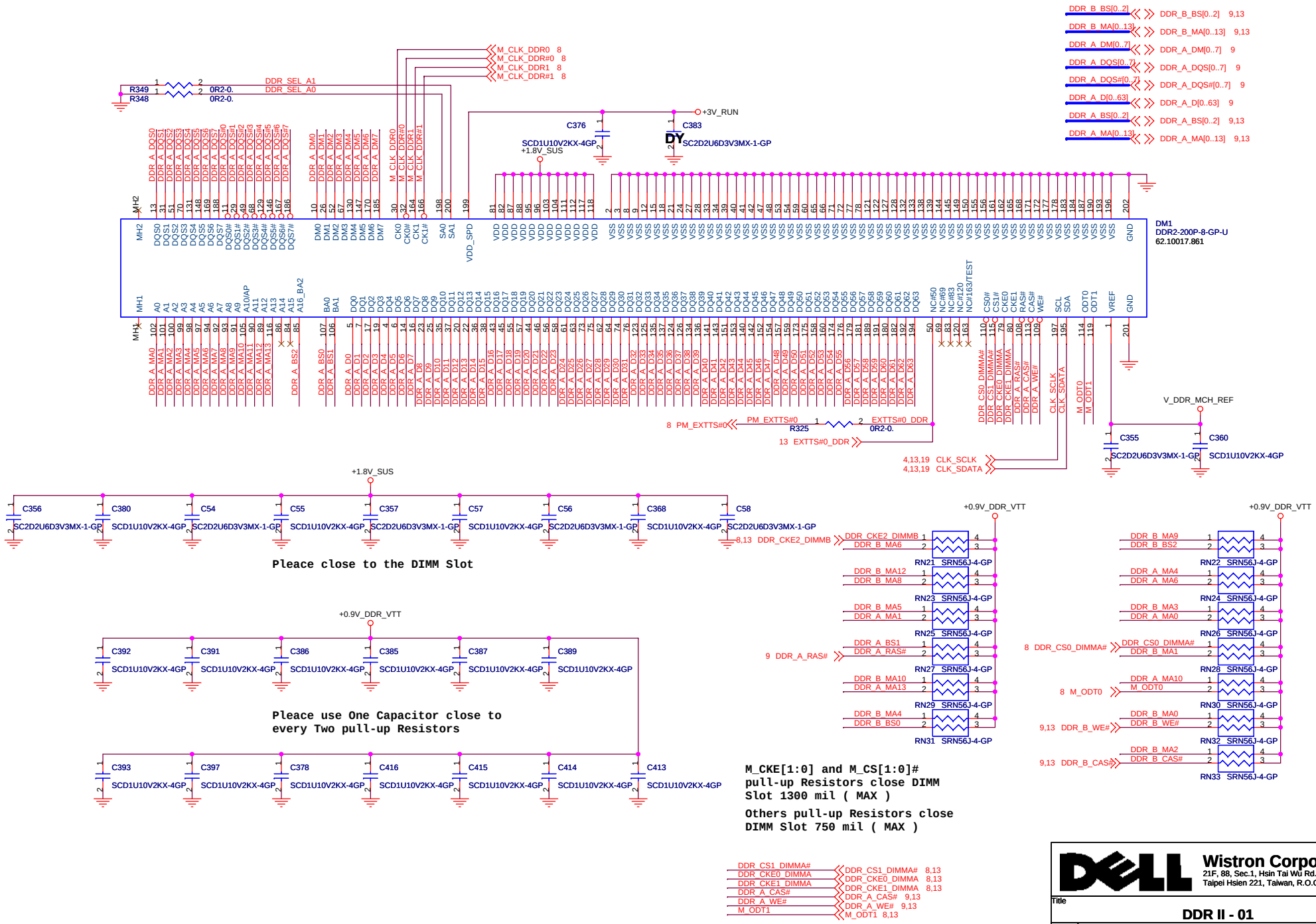
Title	GMCH - 05 - Calistoga - POWER	
Size A3	Document Number Bermuda	Rev -1
Date: Wednesday, March 01, 2006	Sheet 11 of 45	



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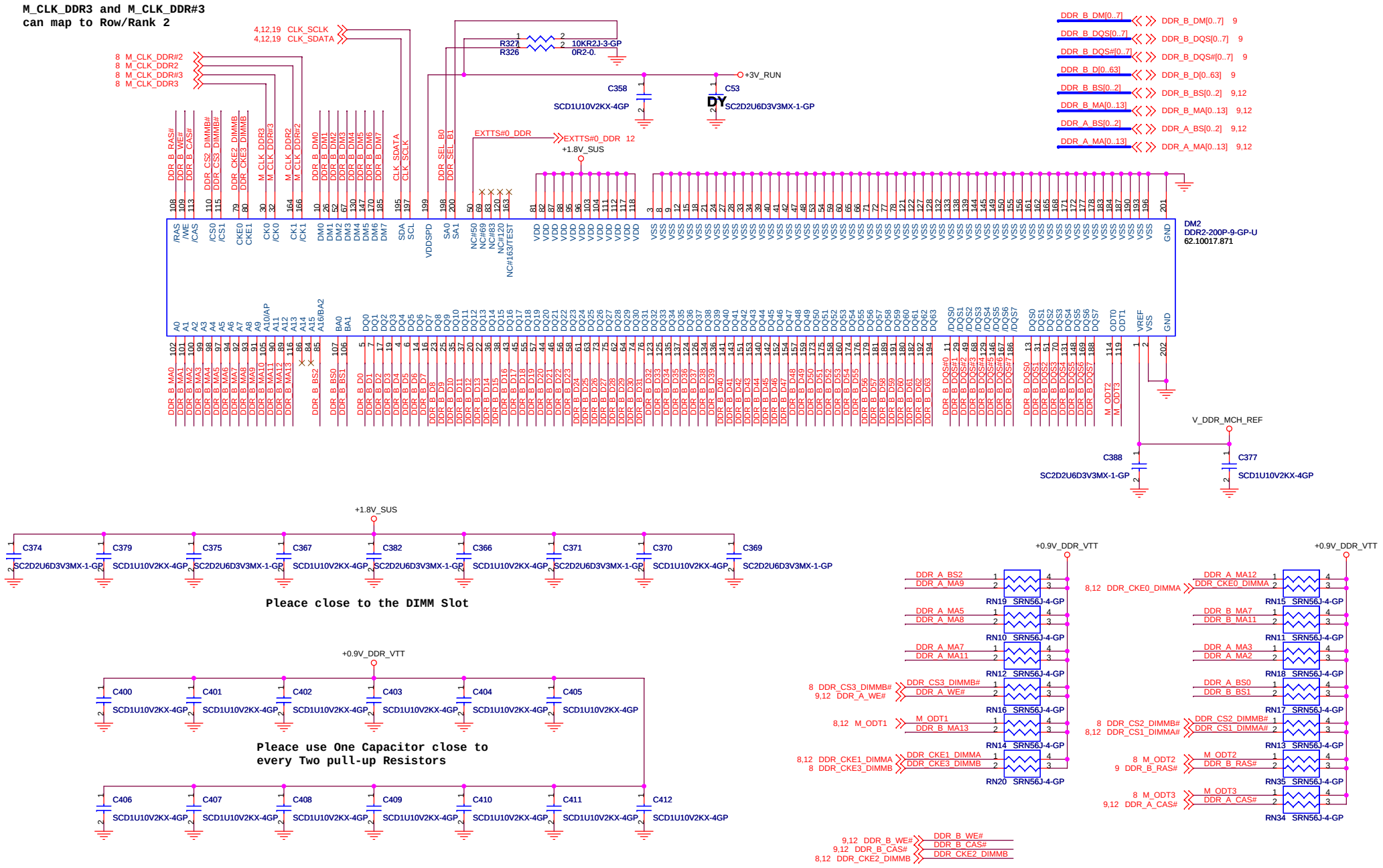
Title: DDR II - 01

Size: A3 | Document Number: Bermuda | Rev: -1

Date: Wednesday, March 01, 2006 | Sheet 12 of 45

M_CLK_DDR3 and M_CLK_DDR#3
can map to Row/Rank 2



M_CKE[3:2] and M_CS[3:2]#
pull-up Resistors close DIMM
Slot 1300 mil (MAX)

Others pull-up Resistors close
DIMM Slot 750 mil (MAX)

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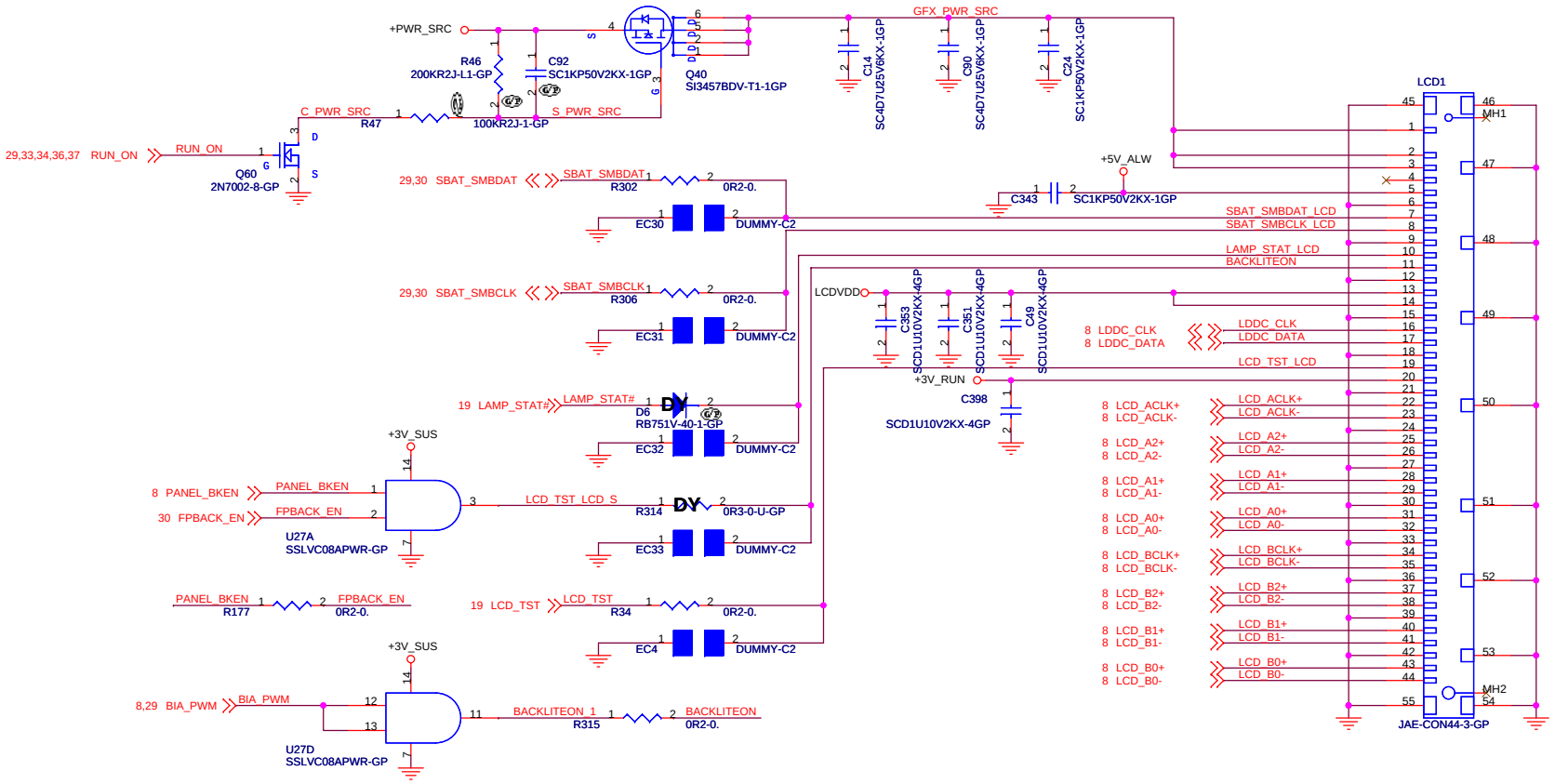
Title: DDR II - 02

Size: A3 | Document Number: Bermuda | Rev: -1

Date: Wednesday, March 01, 2006 | Sheet 13 of 45

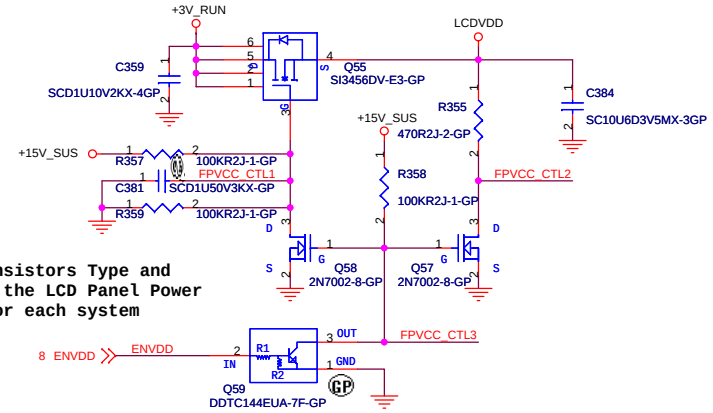
SSID = VIDEO



M00 support D05 Inverter

M'07 Inverter support : Populate this Two Resister and De-populate this SSLVC08APWR

D'05 Inverter support : De-populate this Two Resister and Populate this SSLVC08APWR



Choose the Transistors Type and Rating base on the LCD Panel Power requirements for each system

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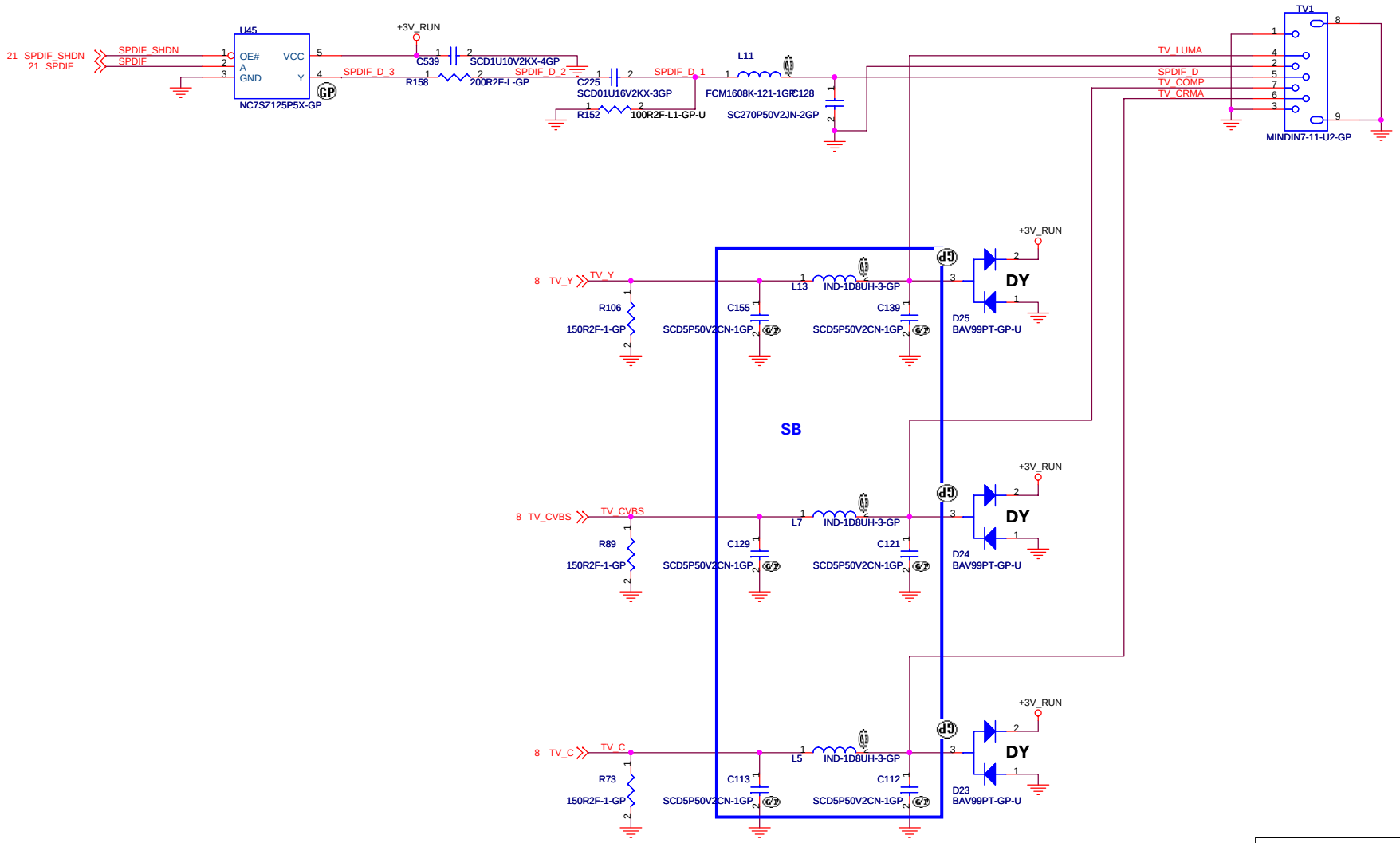
Title	LCD	
Size A3	Document Number Bermuda	Rev -1
Date: Wednesday, March 01, 2006	Sheet 14 of 45	

SSID = VIDEO



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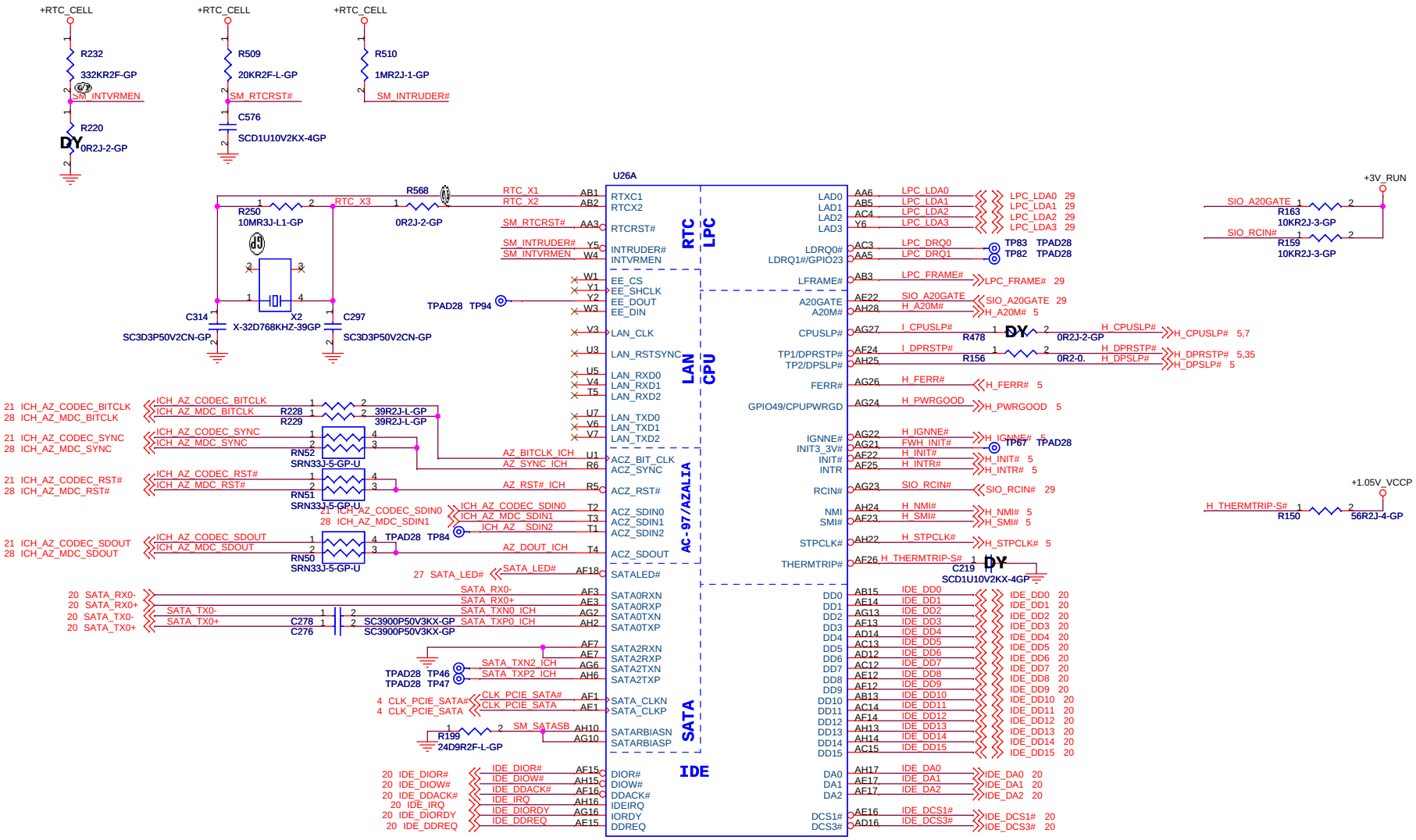
Title	TV OUT
Size A3	Document Number: Bermuda
Rev	-1
Date: Wednesday, March 01, 2006	Sheet 15 of 45



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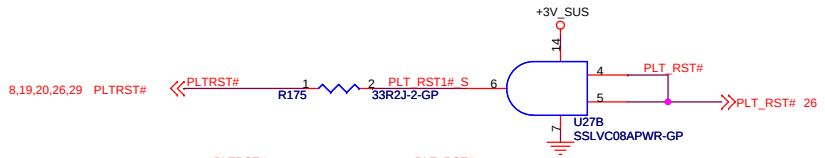
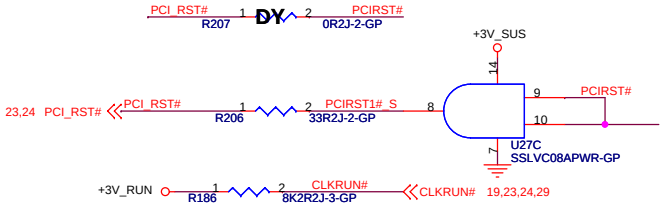
Title: **ICH7-M - 01 - PM/IDE/LPC/AC97**

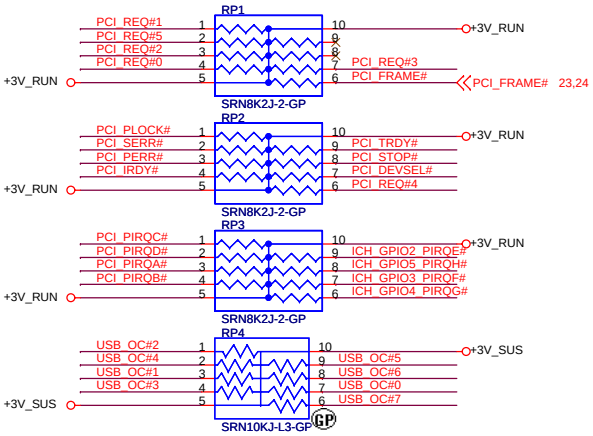
Size: A3 | Document Number: **Bermuda** | Rev: -1

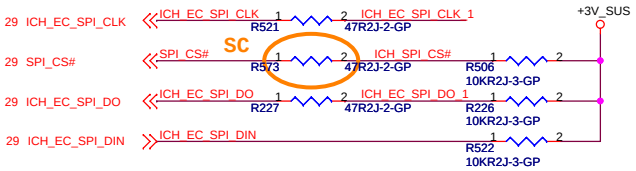
Date: Wednesday, March 01, 2006 | Sheet 16 of 45

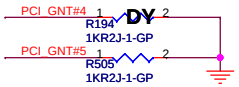


Add Buffers as need for Loading and Fanout concerns







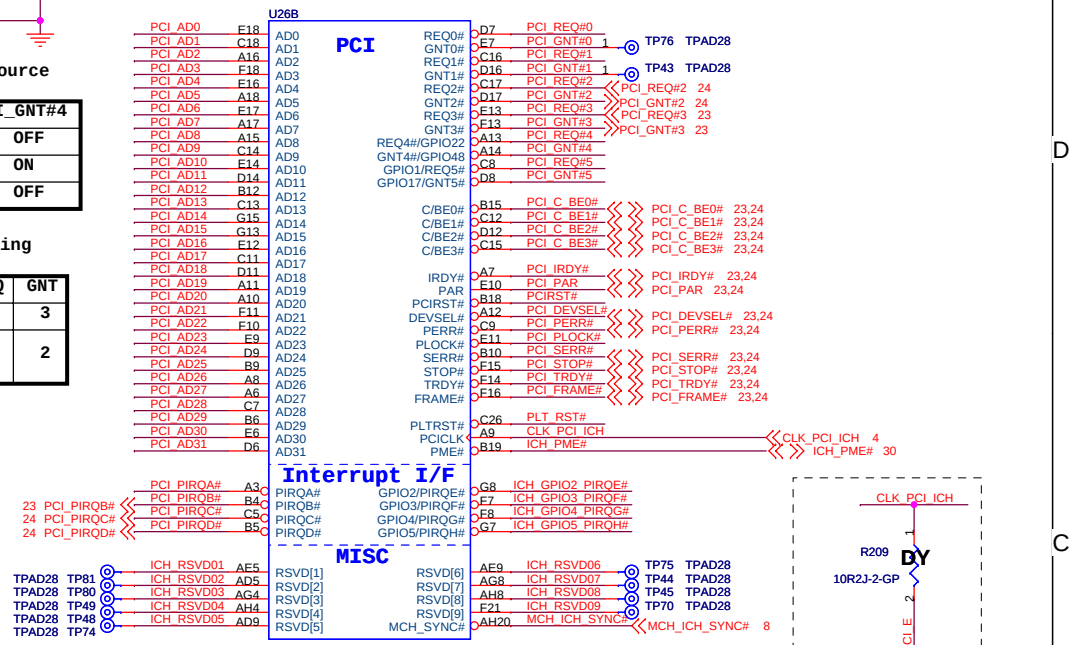


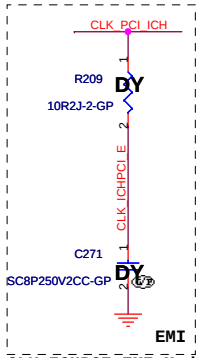
Boot from various source

		PCI_GNT#5	PCI_GNT#4
LPC	HH	OFF	OFF
PCI	HL	OFF	ON
SPI	LH	ON	OFF

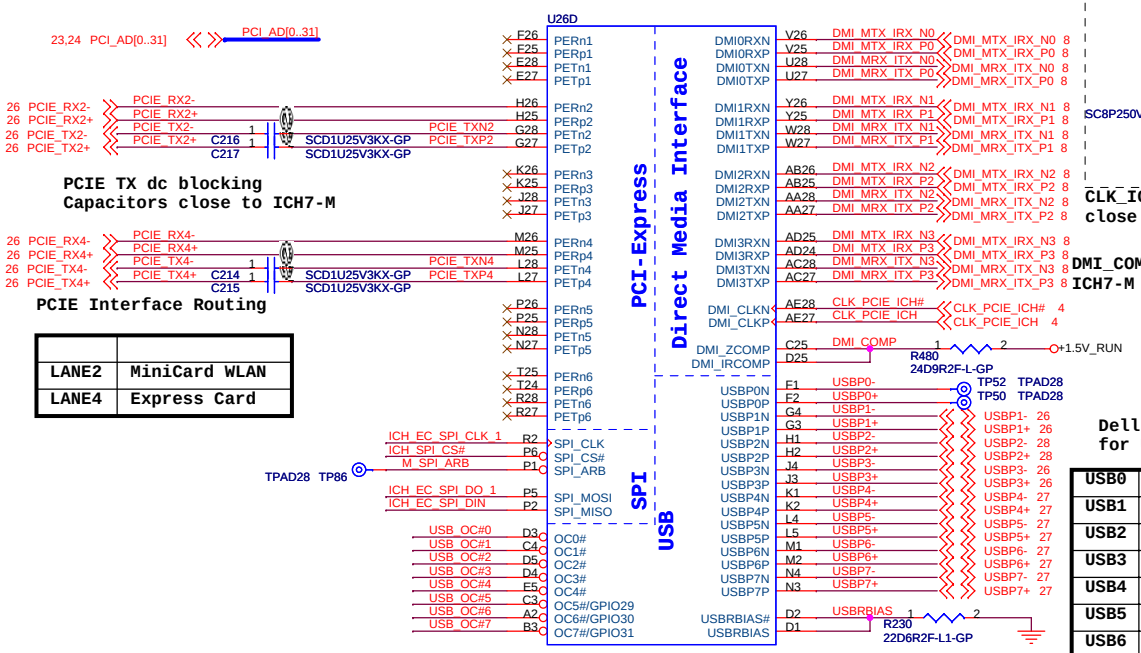
PCI Interface Routing

	IDSEL	INT	REQ	GNT
LAN	AD16	B	3	3
1394	AD17	D C	2	2





CLK_ICHPCI EMI Mode close to ICH7-M



PCIE TX dc blocking Capacitors close to ICH7-M

PCIE Interface Routing

LANE2	MiniCard WLAN
LANE4	Express Card

USBRBIAS close to ICH7-M 500 mil and Trace impedance should be 60 ohm +/- 15%

DMI_COMP close to ICH7-M 500 mil

Dell Arrangement for USB

USB0	No Use
USB1	Express Card
USB2	Bluetooth
USB3	MiniCard WLAN
USB4	Ext Side Top
USB5	Ext Back Top
USB6	Ext Side Bot
USB7	Ext Back Bot

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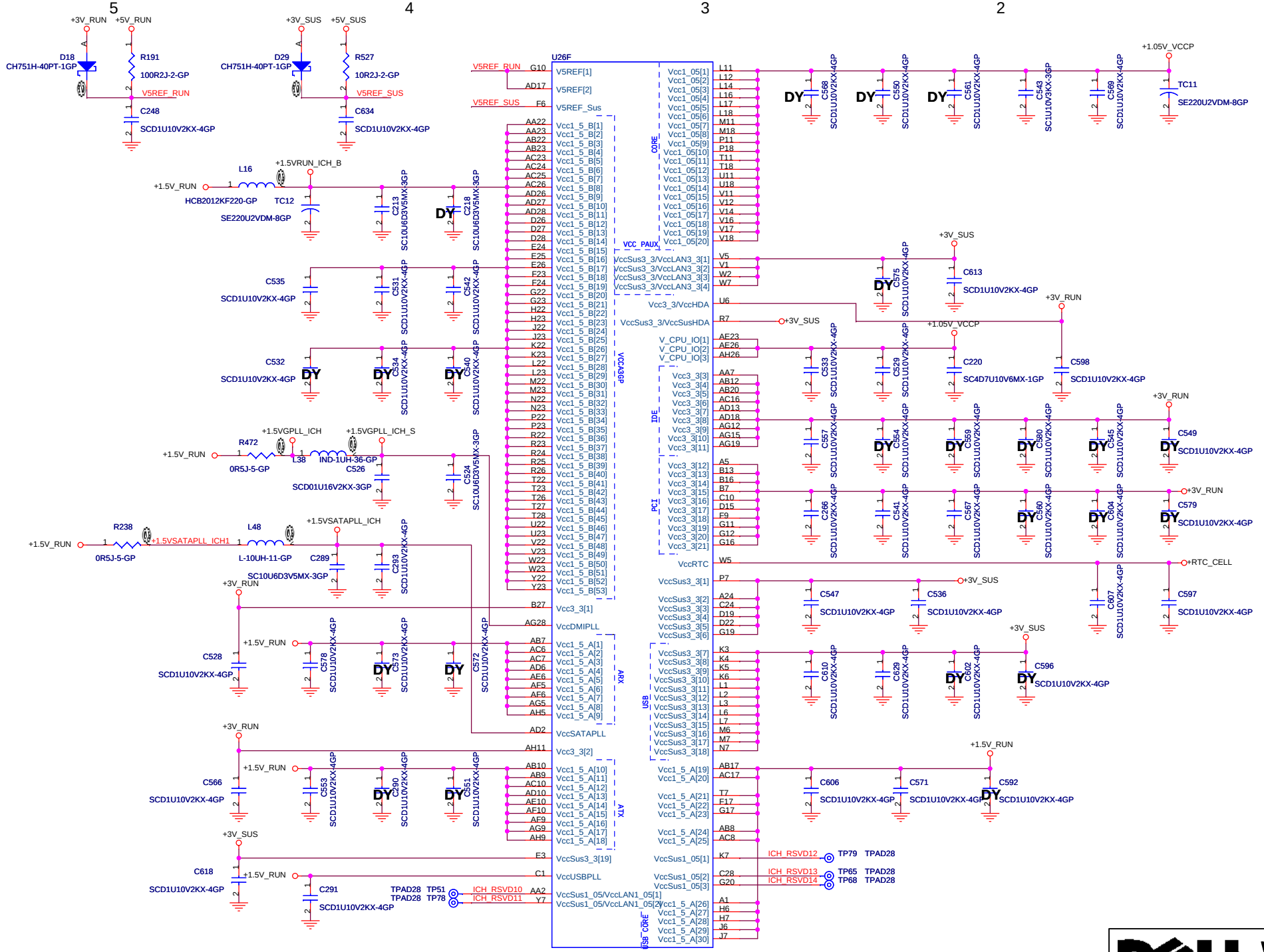
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH7-M - 02 - PCI/USB/SPI/DMI

Size: A3 | Document Number: Bermuda | Rev: -1

Date: Wednesday, March 01, 2006 | Sheet 17 of 45

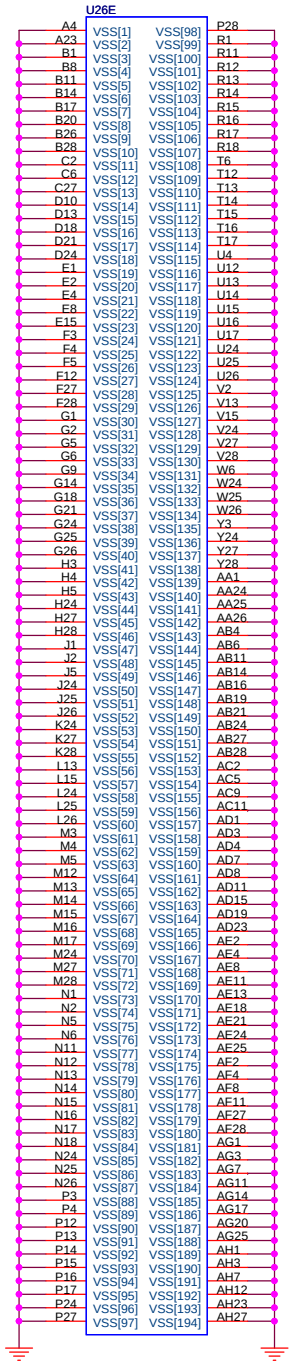


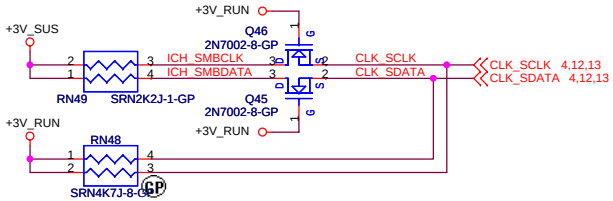
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

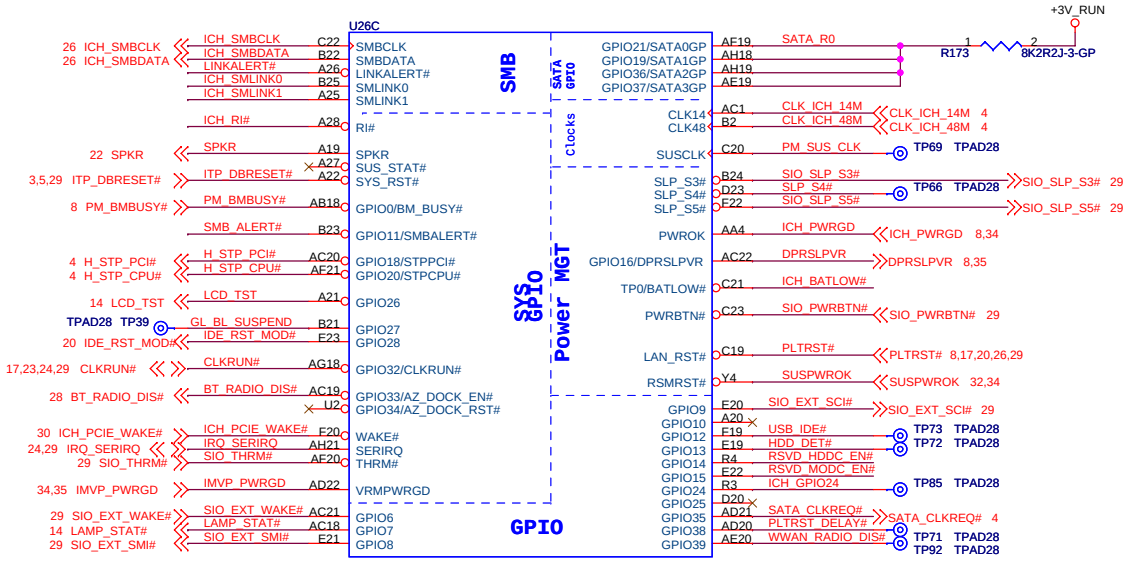
Title: ICH7-M - 03 - POWER

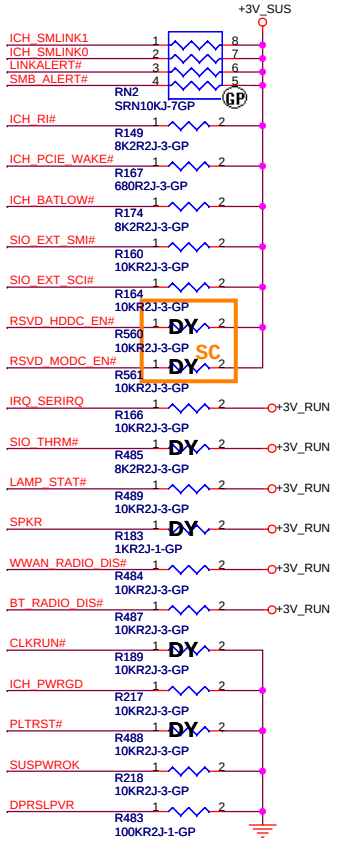
Size: A3 | Document Number: Bermuda | Rev: -1

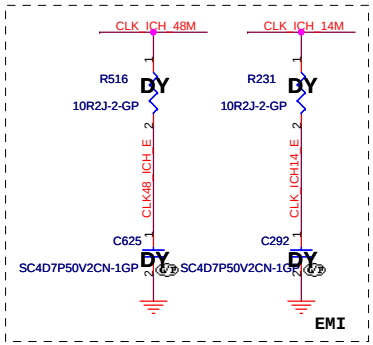
Date: Wednesday, March 01, 2006 | Sheet 18 of 45











CLK48_ICH and CLK_ICH14 EMI Mode close to ICH7-M

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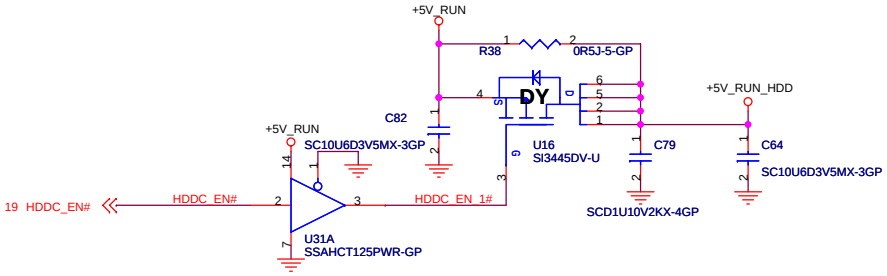
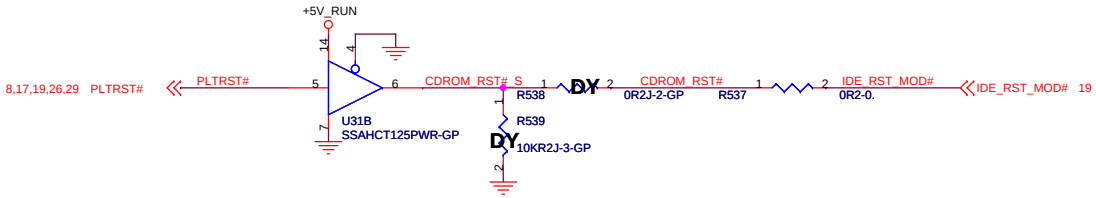
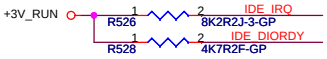
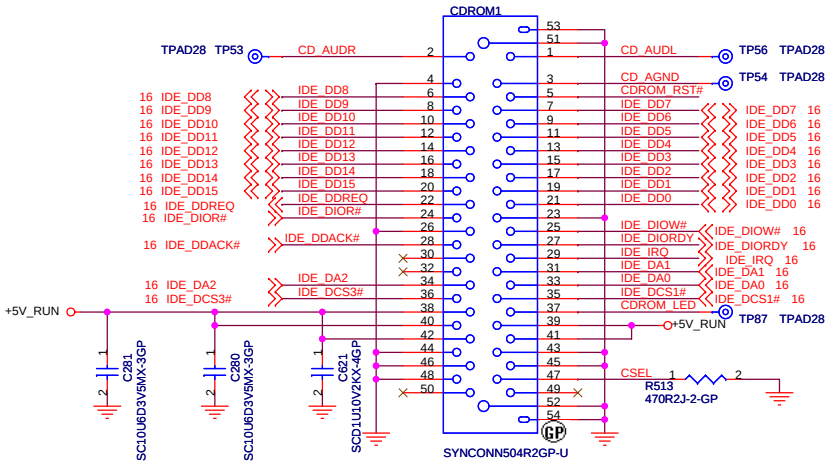
Title		
ICH7-M - 04 - PM/GPIO		
Size A3	Document Number Bermuda	Rev -1
Date: Wednesday, March 01, 2006	Sheet 19 of 45	

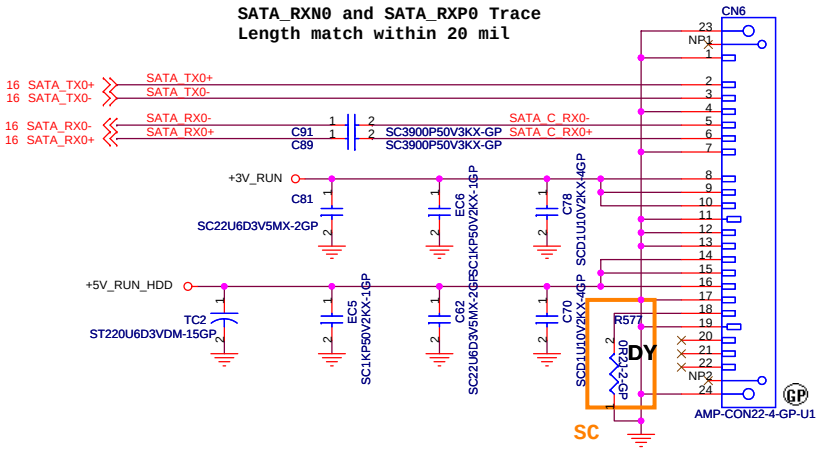
SSID = IDE & SATA











SATA HD Connector

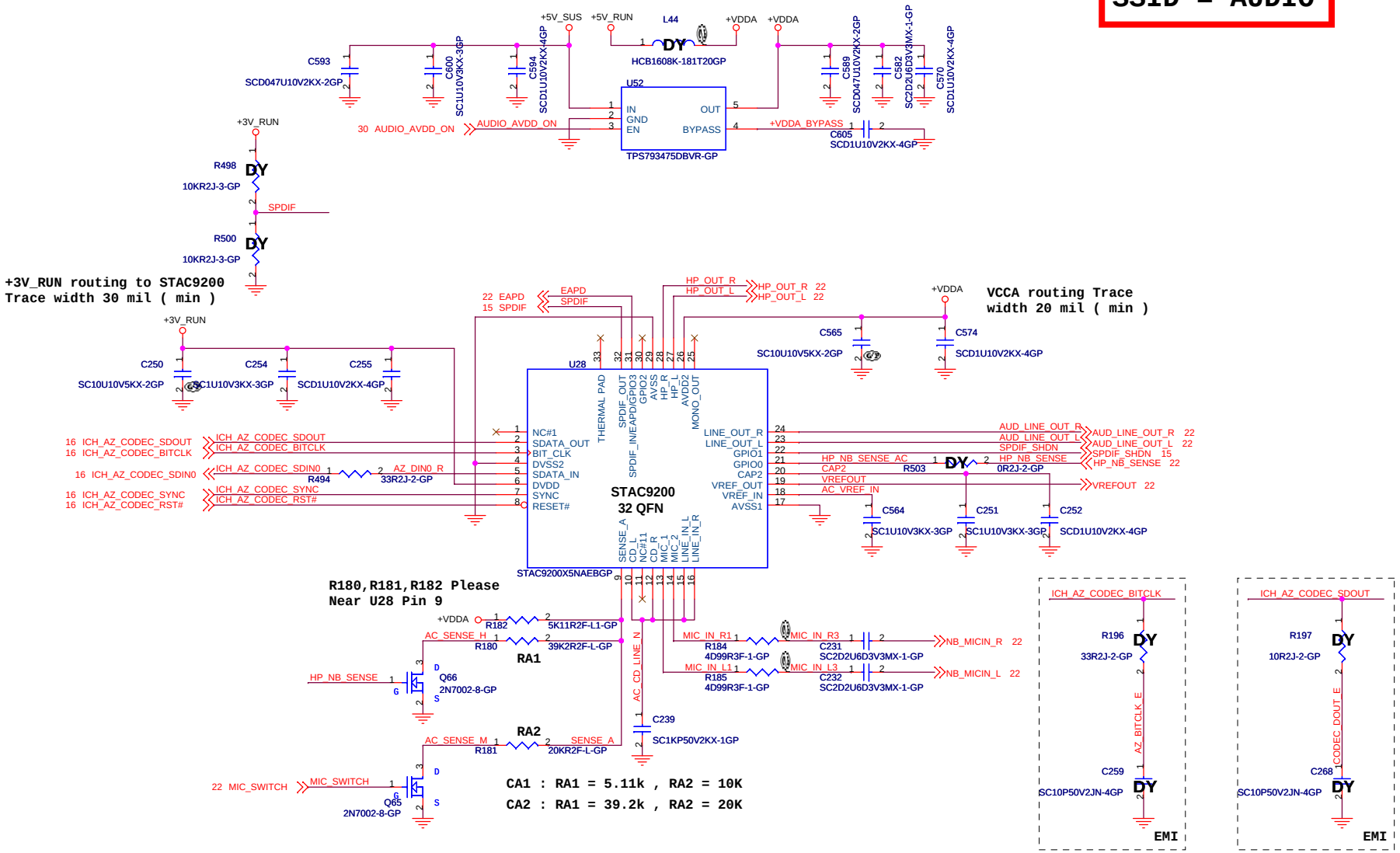
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SATA IDE & CD-ROM

Size	Document Number	Rev
A3	Bermuda	-1

Date: Wednesday, March 01, 2006 Sheet 20 of 45

SSID = AUDIO



AZ_BITCLK EMI Mode
close to ICH7-M

CODEC_DOUT EMI Mode
close to ICH7-M

HD audio port presence detect .Transistors are not required
if jacks implement isolated, normally open switches

Wistron Corporation
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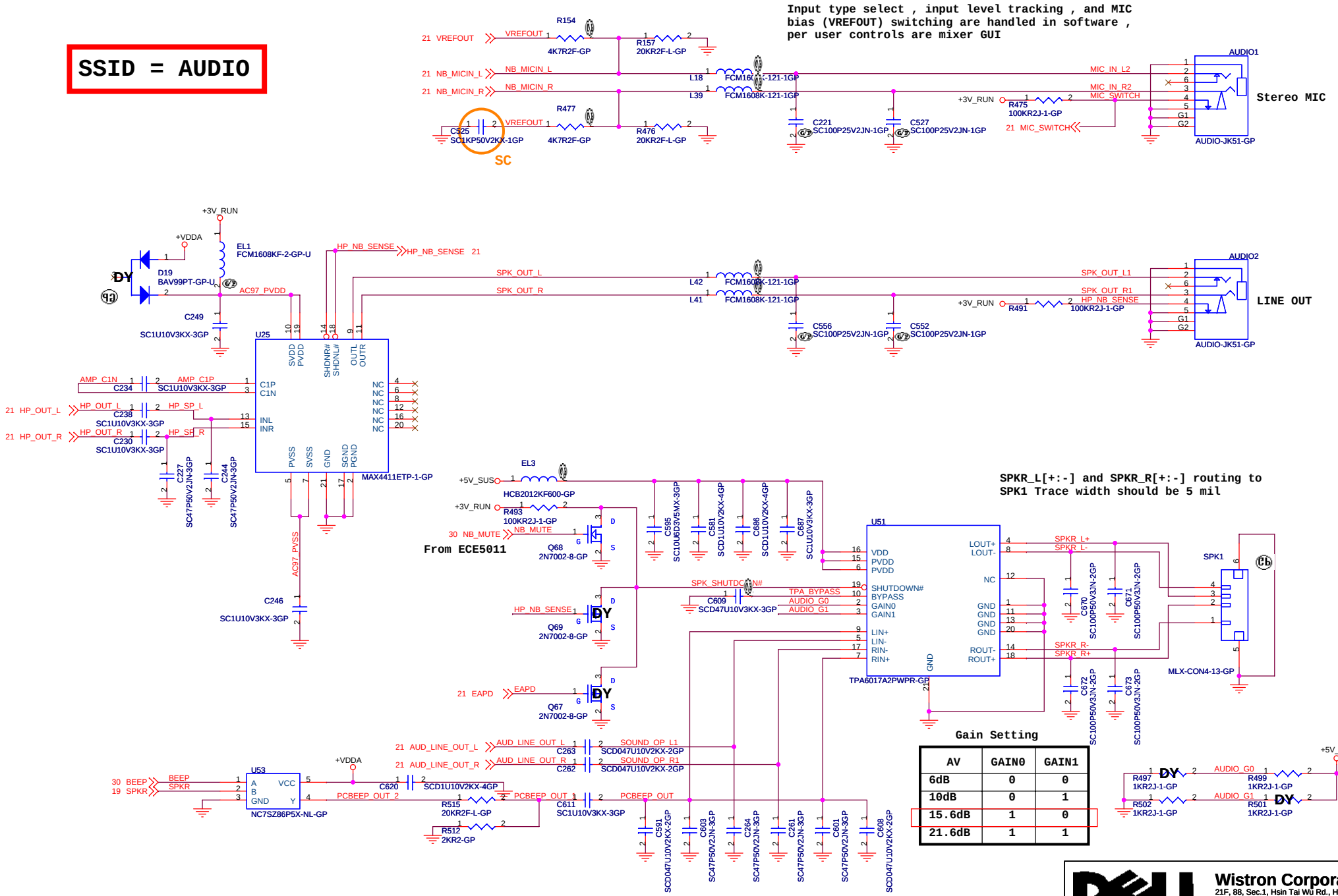
Title	AUDIO - 01 - STAC9200	
Size A3	Document Number Bermuda	Rev -1
Date: Wednesday, March 01, 2006	Sheet 21 of 45	

SSID = AUDIO

NOTE :

Input type select , input level tracking , and MIC bias (VREFOUT) switching are handled in software , per user controls are mixer GUI



Gain Setting

AV	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1

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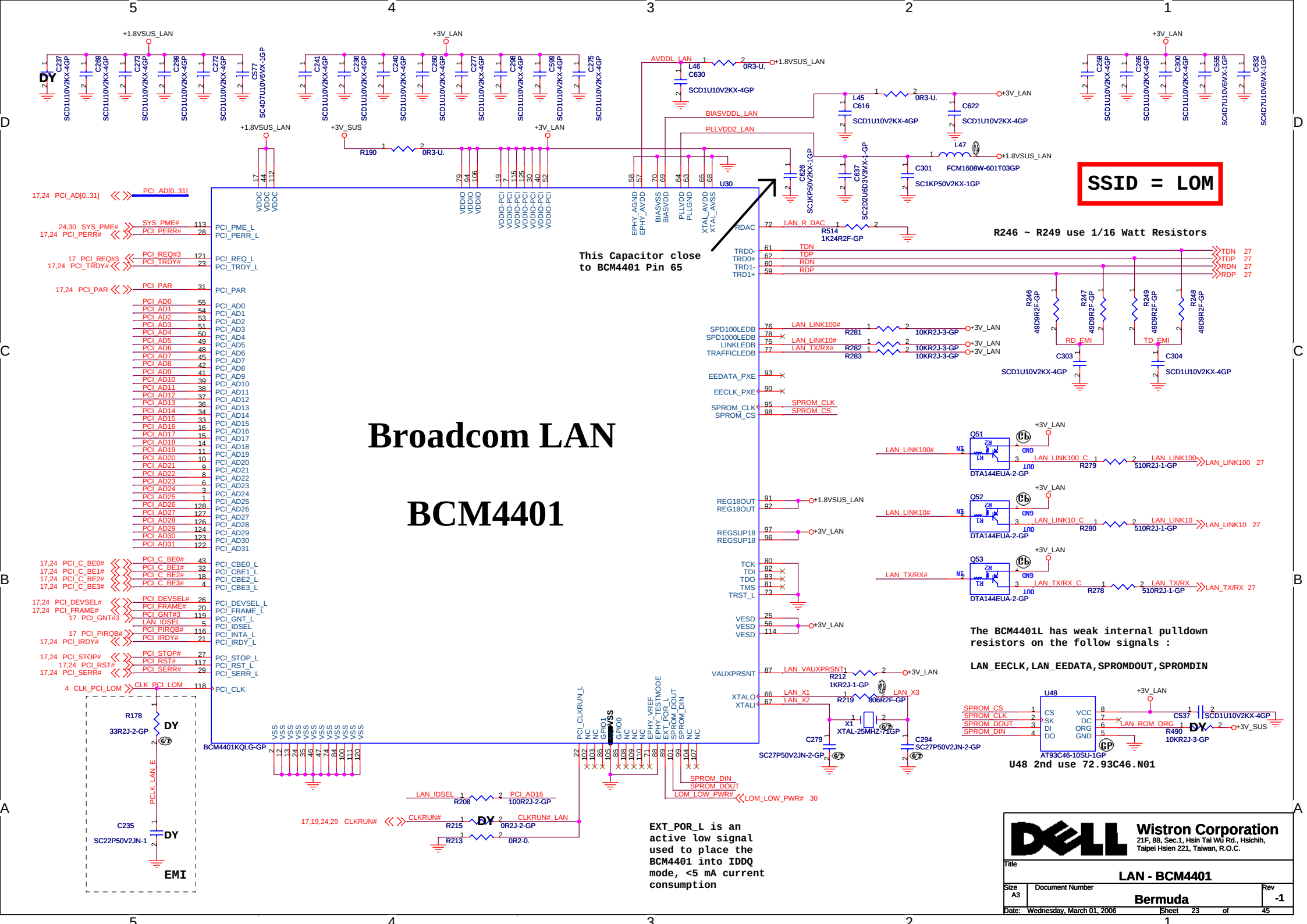
Title: ADUIO - 02 - SPK/MIC/LINE-OUT

Size: A3 | Document Number: Bermuda | Rev: -1

Date: Wednesday, March 01, 2006 | Sheet 22 of 45


Broadcom LAN
BCM4401
SSID = LOM
R246 ~ R249 use 1/16 Watt Resistors
This Capacitor close to BCM4401 Pin 65
The BCM4401L has weak internal pulldown resistors on the follow signals :
LAN_EECLK,LAN_EEDATA,SPROMDOUT,SPROMDIN
U48 2nd use 72.93C46.N01
EXT_POR_L is an active low signal used to place the BCM4401 into IDDQ mode, <5 mA current consumption
BCM4401KQLG-GP
EMI
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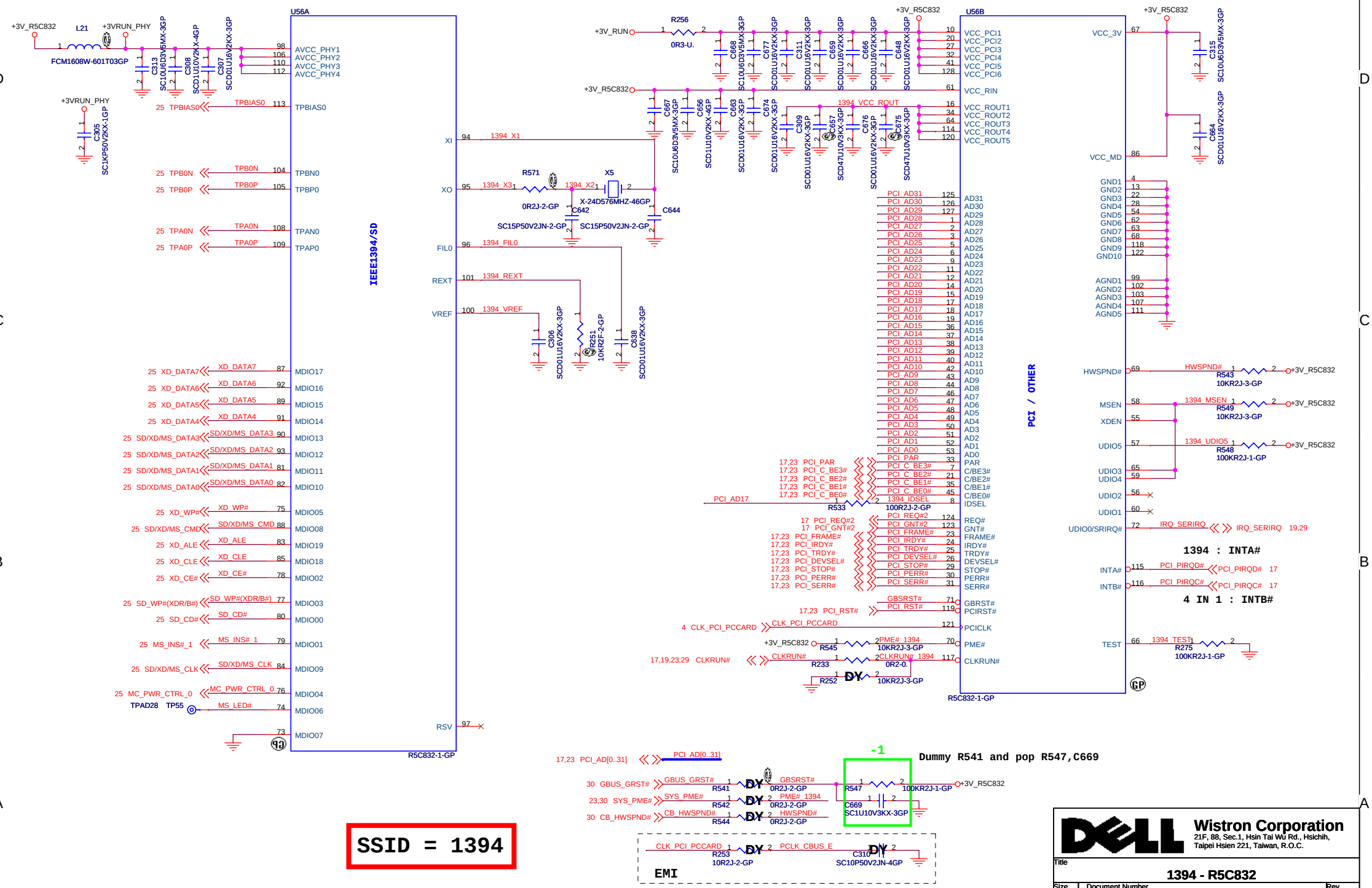
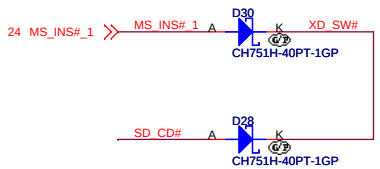
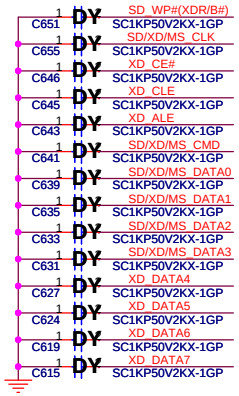
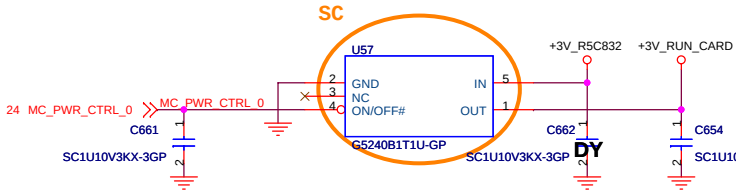
Title
LAN - BCM4401
Size A3
Document Number
Bermuda
Rev -1
Date: Wednesday, March 01, 2006
Sheet 23 of 45

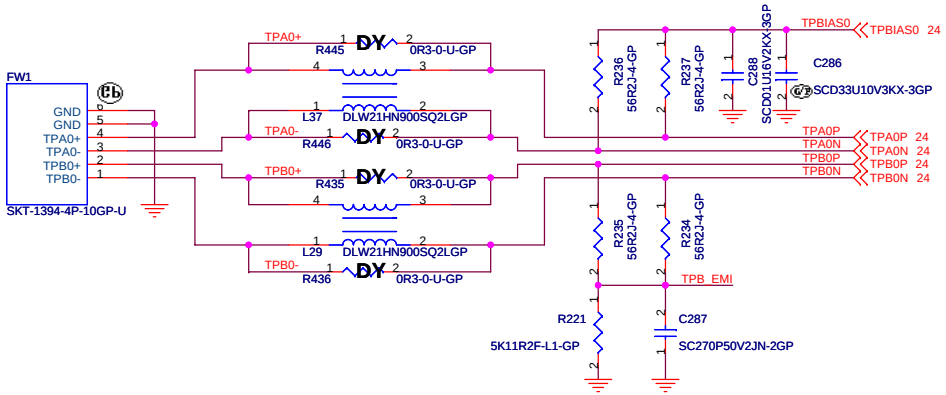

U56A
IEEE1394/SD
R5C832-1-GP
U56B
PCI / OTHER
R5C832-1-GP
1394 : INTA#
4 IN 1 : INTB#
Dummy R541 and pop R547,C669
EMI
SSID = 1394
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
1394 - R5C832
Size A3
Document Number
Bermuda
Rev -1
Date: Wednesday, March 01, 2006
Sheet 24 of 45

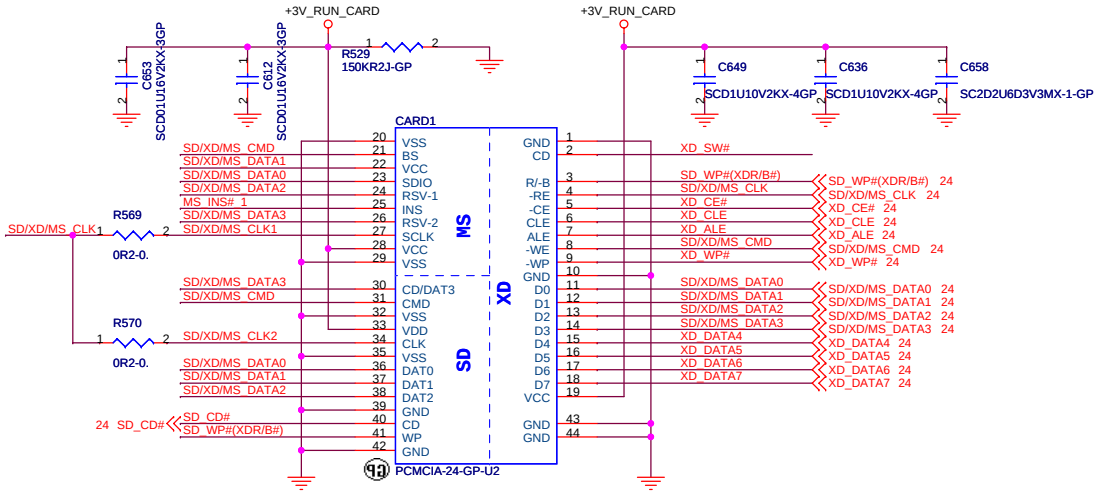
SSID = 1394











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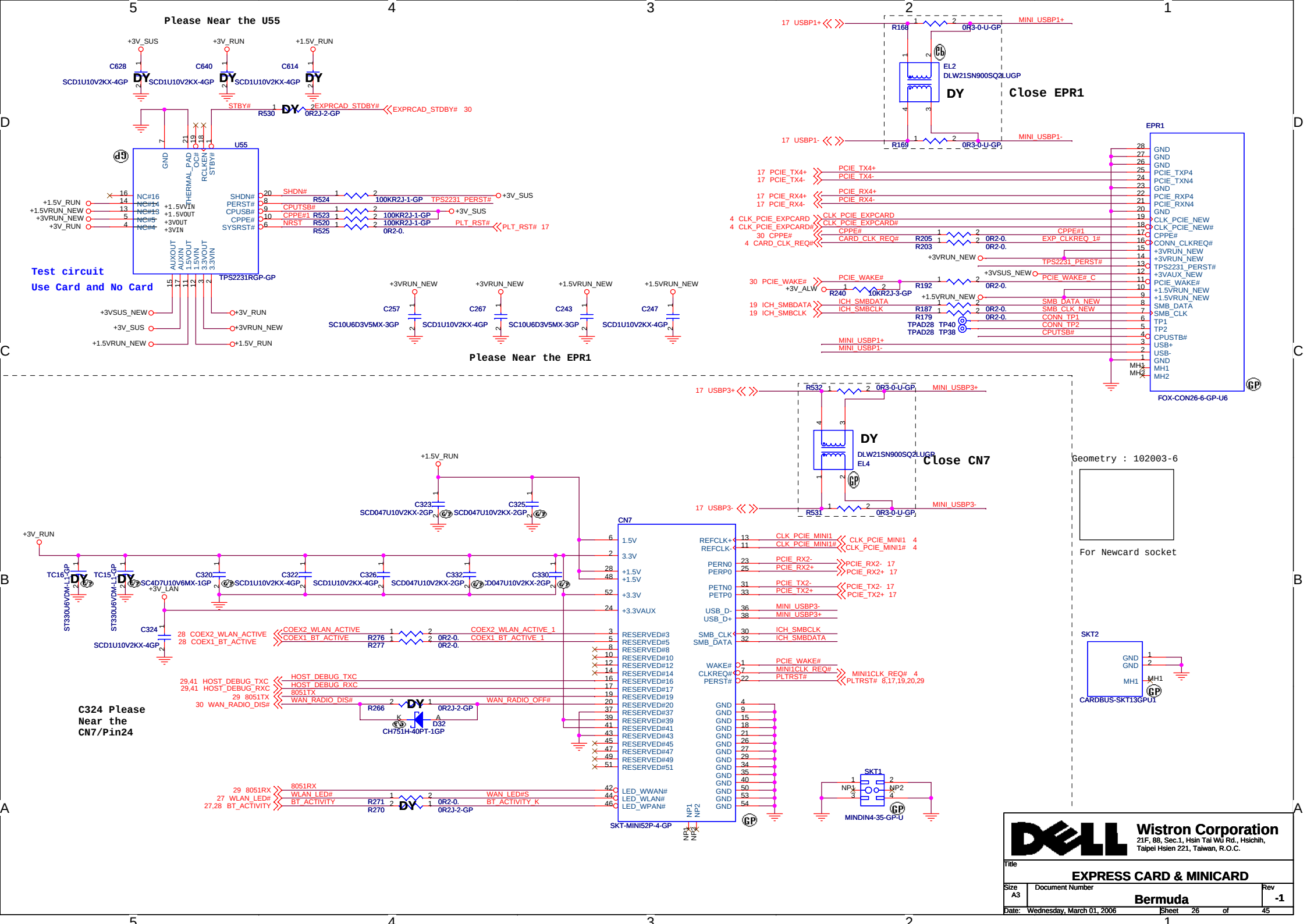
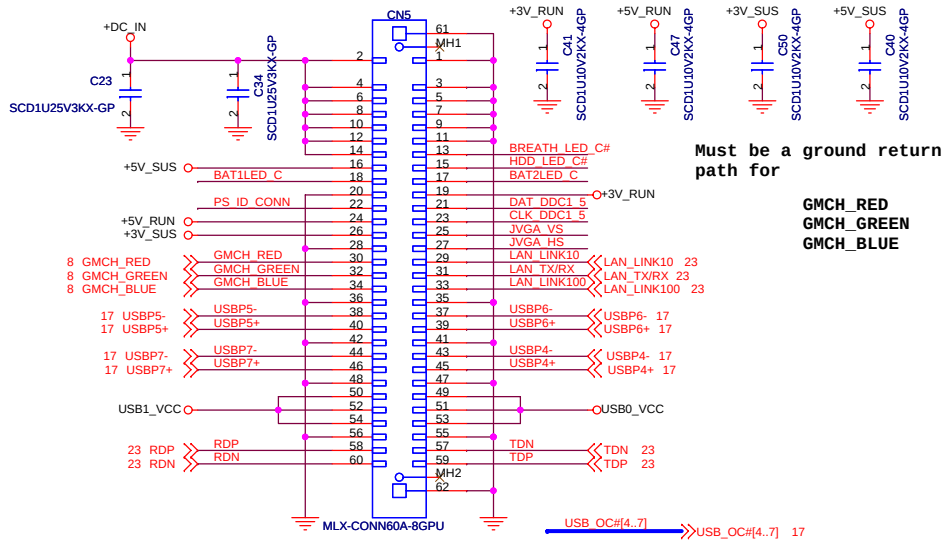
Title: **1394 - 4 IN 1 Connector**

Size	Document Number	Rev
A3	Bermuda	-1

Date: Wednesday, March 01, 2006 Sheet 25 of 45

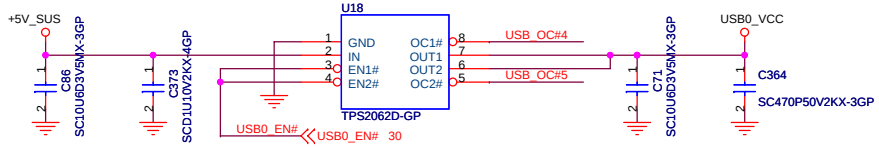

Please Near the U55
+3V_SUS
+3V_RUN
+1.5V_RUN
C628
C640
C614
SCD1U10V2KX-4GP
DY
STBY#
R530
0R2J-2-GP
EXPRCAD_STDBY#
U55
GND
THERMAL_PAD
OCR
RCLKEN
STBY#
NC#16
NC#14
NC#13
NC#5
NC#4
+1.5VIN
+1.5V0UT
+3V0UT
+3VIN
SHDN#
PERST#
CPUSB#
CPPE#
SYSRST#
AUXOUT
AUXIN
1.5VOUT
1.5VIN
3.3VOUT
3.3VIN
TPS2231RGP-GP
R524
100KR2J-1-GP
TPS2231_PERST#
R523
R520
R525
0R2-0.
PLT_RST#
Test circuit
Use Card and No Card
+3VSUS_NEW
+3V_SUS
+1.5VRUN_NEW
+3V_RUN
+3VRUN_NEW
+1.5V_RUN
+3VRUN_NEW
+1.5VRUN_NEW
C257
C267
C243
C247
SC10U6D3V5MX-3GP
SCD1U10V2KX-4GP
Please Near the EPR1
R168
R169
0R3-0-U-GP
MINI_USBP1+
MINI_USBP1-
EL2
DLW21SN900SQ2LUGP
Close EPR1
EPR1
FOX-CON26-6-GP-U6
PCIE_TX4+
PCIE_TX4-
PCIE_RX4+
PCIE_RX4-
CLK_PCIE_EXPCARD
CLK_PCIE_EXPCARD#
CPPE#
CARD_CLK_REQ#
R205
R203
CPPE#1
EXP_CLKREQ_1#
TPS2231_PERST#
PCIE_WAKE#
R192
R240
10KR2J-3-GP
ICH_SMBDATA
ICH_SMBCLK
R187
R179
TPAD28
TP40
TP38
SMB_DATA_NEW
SMB_CLK_NEW
CONN_TP1
CONN_TP2
CPUTSB#
PCIE_WAKE# C
CLK_PCIE_NEW
CLK_PCIE_NEW#
CONN_CLKREQ#
+3VRUN_NEW
+3VAUX_NEW
+1.5VRUN_NEW
SMB_DATA
SMB_CLK
TP1
TP2
CPUSTB#
USB+
USB-
MH1
MH2
R532
R531
MINI_USBP3+
MINI_USBP3-
DLW21SN900SQ2LUGP
EL4
Close CN7
Geometry : 102003-6
For Newcard socket
C323
C325
SCD047U10V2KX-2GP
TC16
TC15
ST330U6VDM-LI-GP
SC4D7U10V6MX-1GP
+3V_LAN
C320
C322
C326
C332
C330
SCD1U10V2KX-4GP
SCD047U10V2KX-2GP
D047U10V2KX-2GP
C324
SCD1U10V2KX-4GP
COEX2_WLAN_ACTIVE
COEX1_BT_ACTIVE
R276
R277
0R2-0.
COEX2_WLAN_ACTIVE_1
COEX1_BT_ACTIVE_1
HOST_DEBUG_TXC
HOST_DEBUG_RXC
8051TX
WAN_RADIO_DIS#
WAN_RADIO_OFF#
R266
0R2J-2-GP
D32
CH751H-40PT-1GP
C324 Please Near the CN7/Pin24
8051RX
WLAN_LED#
BT_ACTIVITY
WAN_LED#S
BT_ACTIVITY_K
R271
R270
0R2J-2-GP
CN7
1.5V
3.3V
+1.5V
+3.3V
+3.3VAUX
RESERVED#3
RESERVED#5
RESERVED#8
RESERVED#10
RESERVED#12
RESERVED#14
RESERVED#16
RESERVED#17
RESERVED#19
RESERVED#20
RESERVED#37
RESERVED#39
RESERVED#41
RESERVED#43
RESERVED#45
RESERVED#47
RESERVED#49
RESERVED#51
LED_WWAN#
LED_WLAN#
LED_WPAN#
REFCLK+
REFCLK-
PERN0
PERP0
PETN0
PETP0
USB_D-
USB_D+
SMB_CLK
SMB_DATA
WAKE#
CLKREQ#
PERST#
CLK_PCIE_MINI1
CLK_PCIE_MINI1#
PCIE_RX2-
PCIE_RX2+
PCIE_TX2-
PCIE_TX2+
MINI1CLK_REQ#
PLTRST#
GND
SKT-MINI52P-4-GP
SKT1
MINDIN4-35-GP-U
SKT2
CARDBUS-SKT13GPU1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EXPRESS CARD & MINICARD
Size
A3
Document Number
Bermuda
Rev
-1
Date: Wednesday, March 01, 2006
Sheet 26 of 45

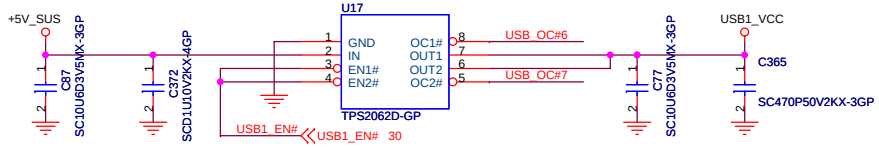
CRT BD Conn

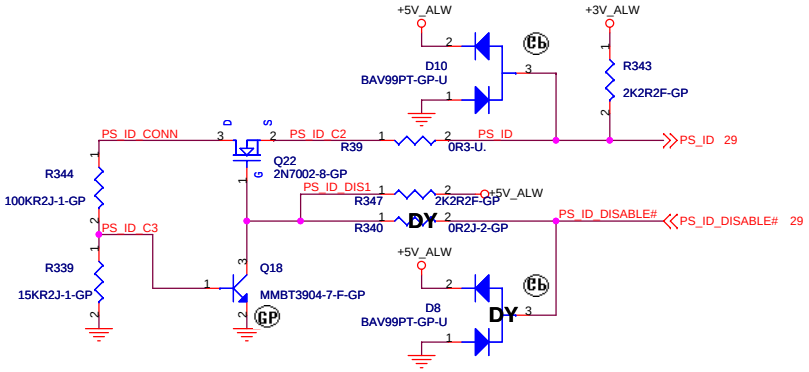


Must be a ground return path for

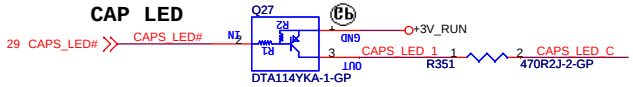
GMCH_RED
GMCH_GREEN
GMCH_BLUE



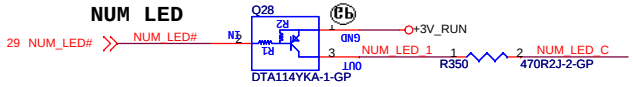




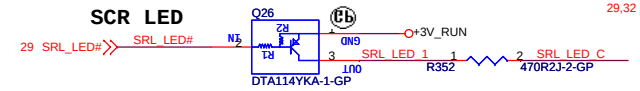
CAP LED



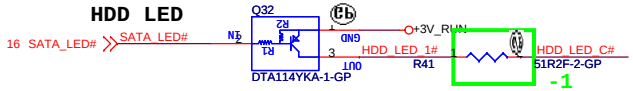
NUM LED



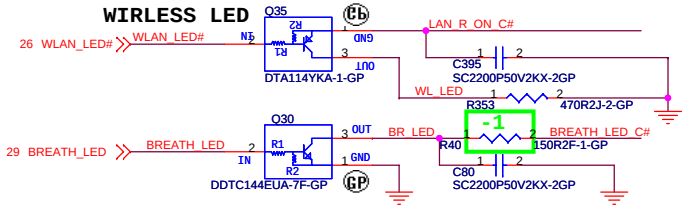
SCR LED

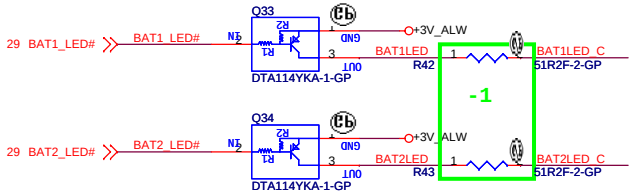


HDD LED

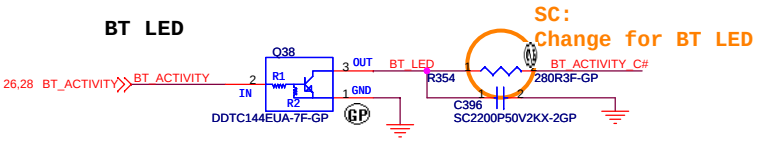


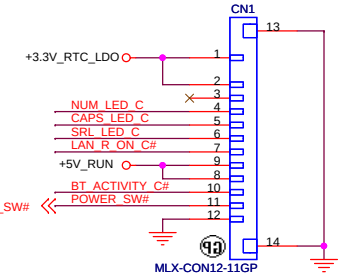
WIRLESS LED

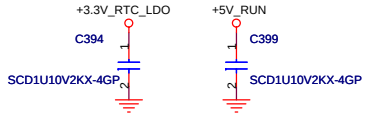


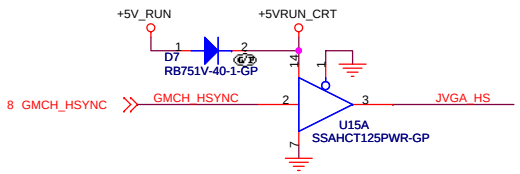


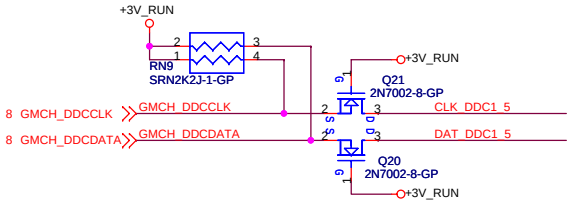
BT LED

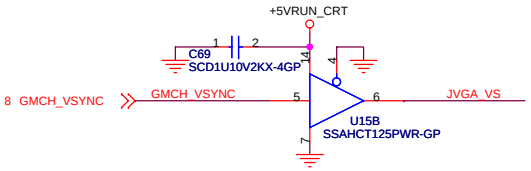






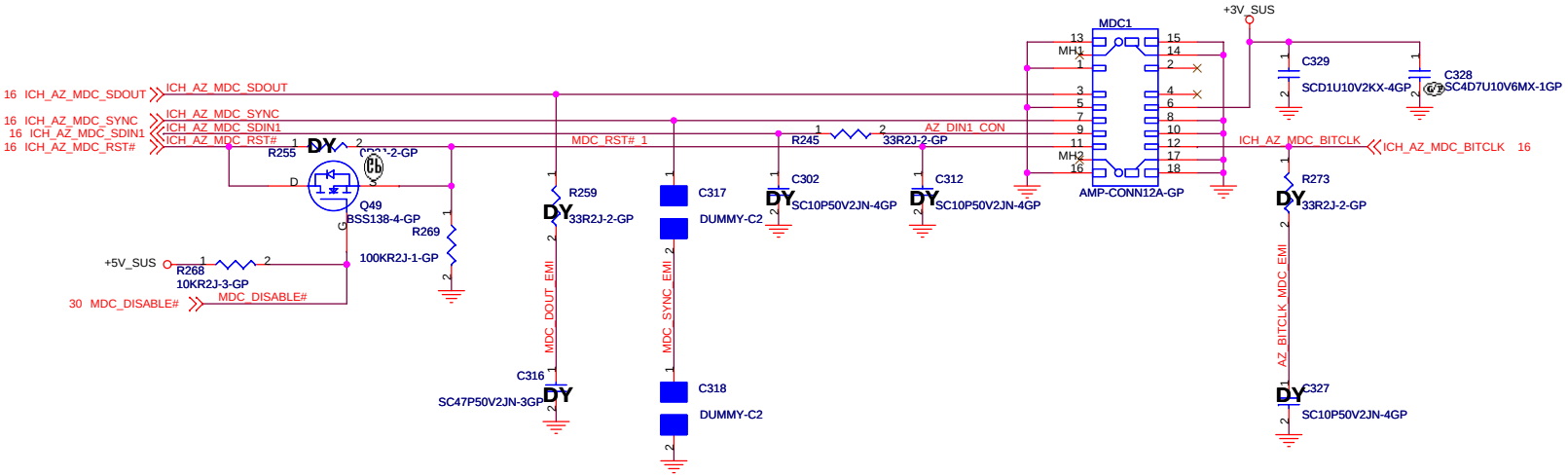




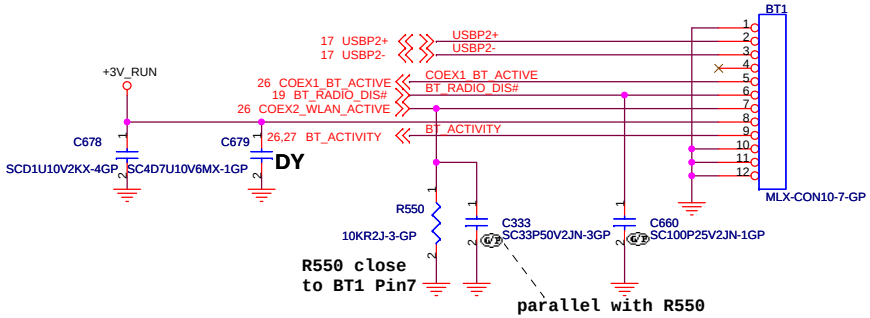


Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CRT BD CONN & LED		
Size: A3	Document Number: Bermuda	Rev: -1
Date: Wednesday, March 01, 2006	Sheet 27 of 45	

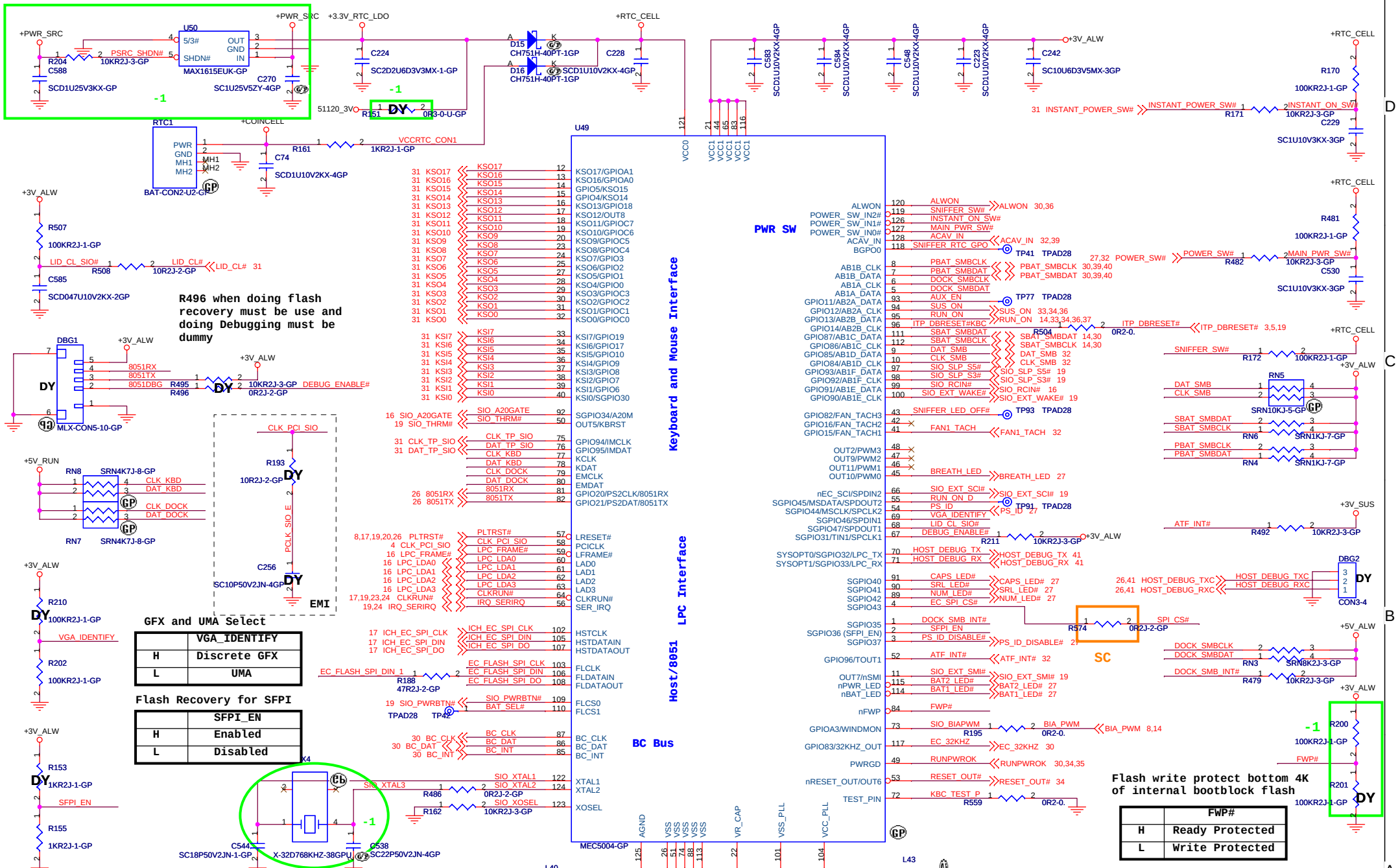
Modem Connector
(Not Standard Type)

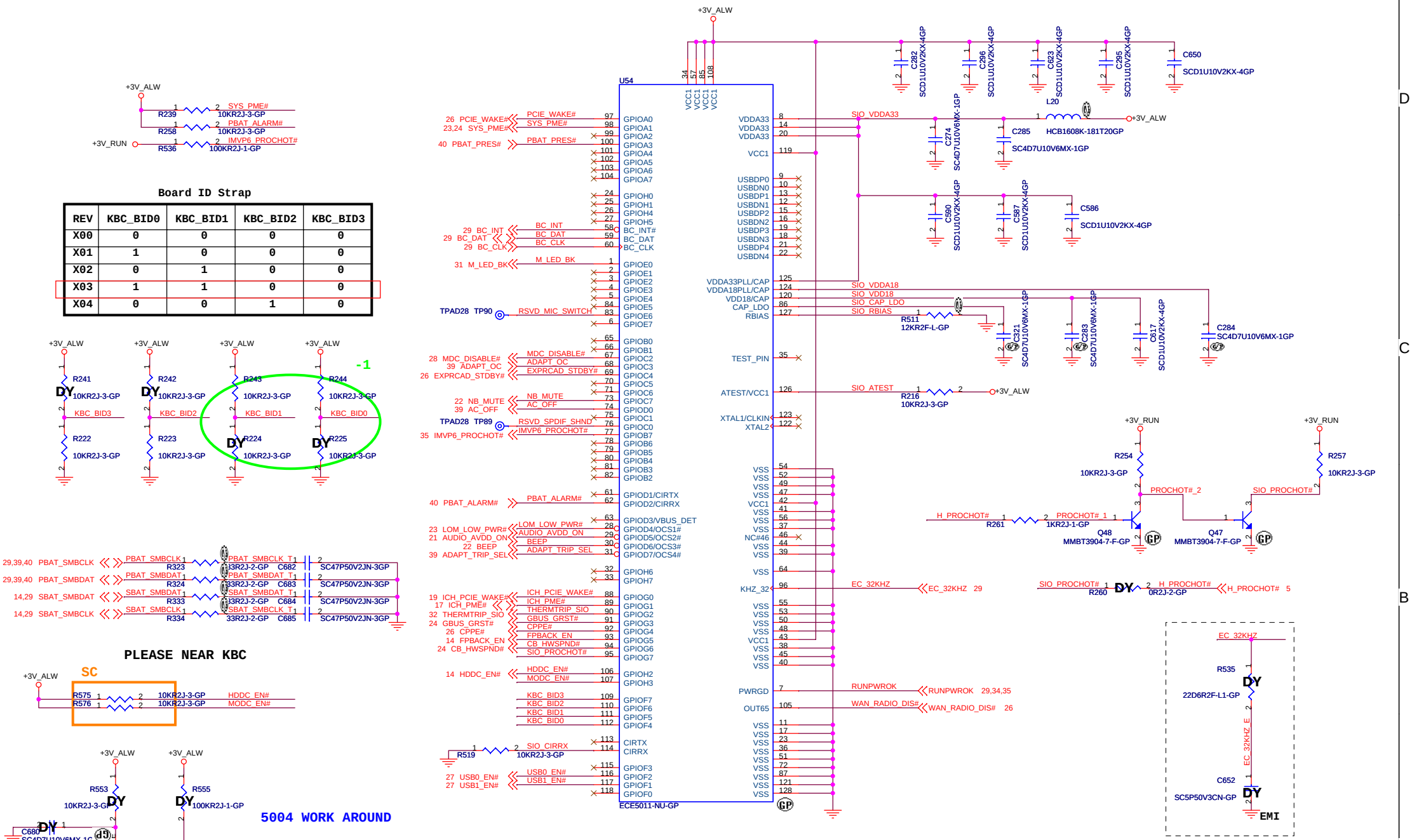


Bluetooth Module conn.

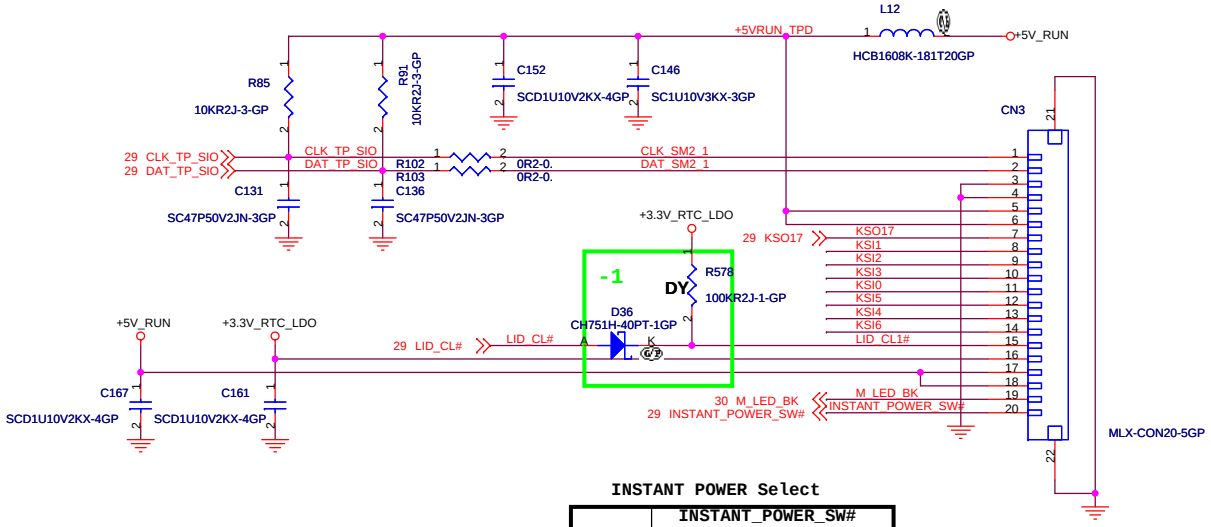


Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MDC & BT		
Size: A3	Document Number: Bermuda	Rev: -1
Date: Wednesday, March 01, 2006	Sheet 28 of 45	


U49
MEC5004-GP
Keyboard and Mouse Interface
LPC Interface
Host/8051
BC Bus
PWR SW
U50
MAX1615EUK-GP
RTC1
BAT-CON2-U2-GP
DBG1
MLX-CON5-10-GP
U29
SST25VF080B-GP
X4
X-32D768KHZ-38GPU
EMI
SC
DBG2
CON3-4
R496 when doing flash recovery must be use and doing Debugging must be dummy
GFX and UMA Select
VGA_IDENTIFY
H Discrete GFX
L UMA
Flash Recovery for SFPI
SFPI_EN
H Enabled
L Disabled
Flash write protect bottom 4K of internal bootblock flash
FWP#
H Ready Protected
L Write Protected
SPI ROM
Main source:72.25080.G01(SST)
2nd source :72.25805.001(MXIC)
The capactior C222 Impedance must < 2 ohm
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC
Size A3
Document Number
Bermuda
Rev -1
Date: Friday, March 10, 2006
Sheet 29 of 45



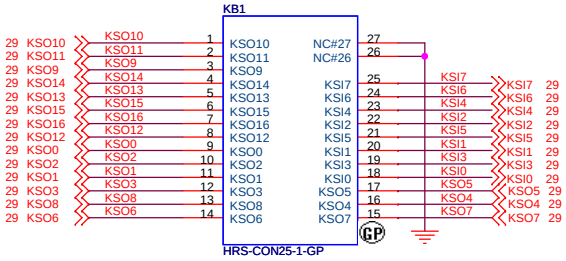
REV	KBC_BID0	KBC_BID1	KBC_BID2	KBC_BID3
X00	0	0	0	0
X01	1	0	0	0
X02	0	1	0	0
X03	1	1	0	0
X04	0	0	1	0

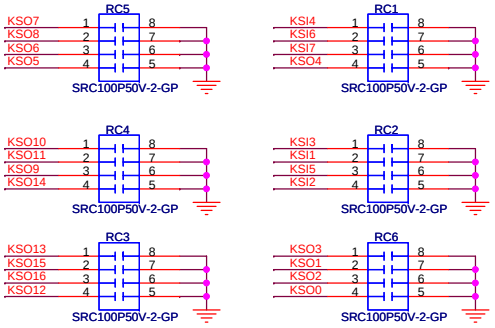


Media PlayBack / TouchPAD Connector

INSTANT POWER Select

	INSTANT_POWER_SW#
H	Power On Function
L	Regular Play Function





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Title: **KB & TPAD**

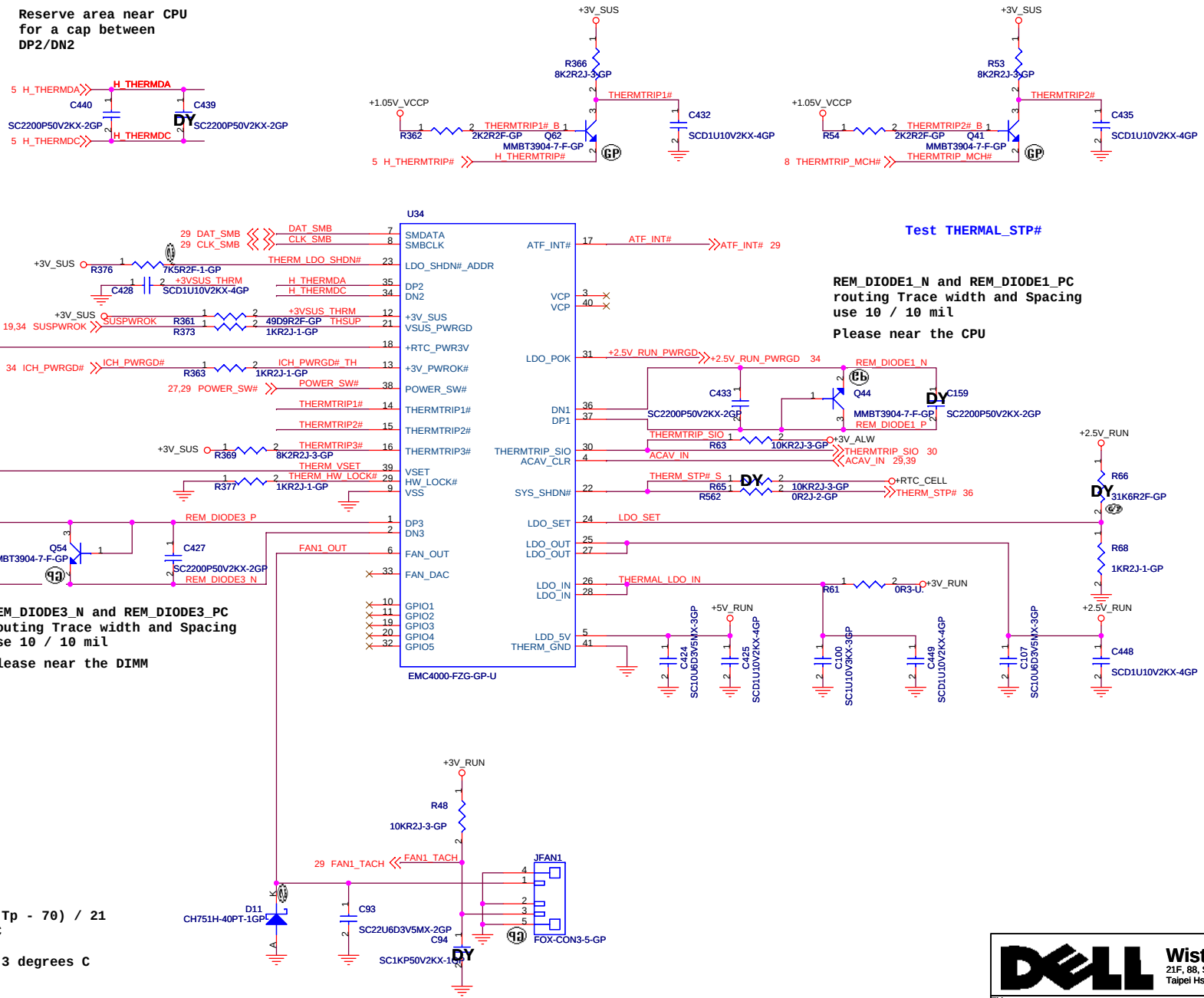
Size	Document Number	Rev
A3	Bermuda	-1

Date: Wednesday, March 01, 2006 Sheet 31 of 45

SSID = THERMAL

H_THERMDA and H_THERMDC routing Trace width and Spacing use 10 / 10 mil

Reserve area near CPU for a cap between DP2/DN2



Test THERMAL_STP#

REM_DIODE1_N and REM_DIODE1_PC routing Trace width and Spacing use 10 / 10 mil

Please near the CPU

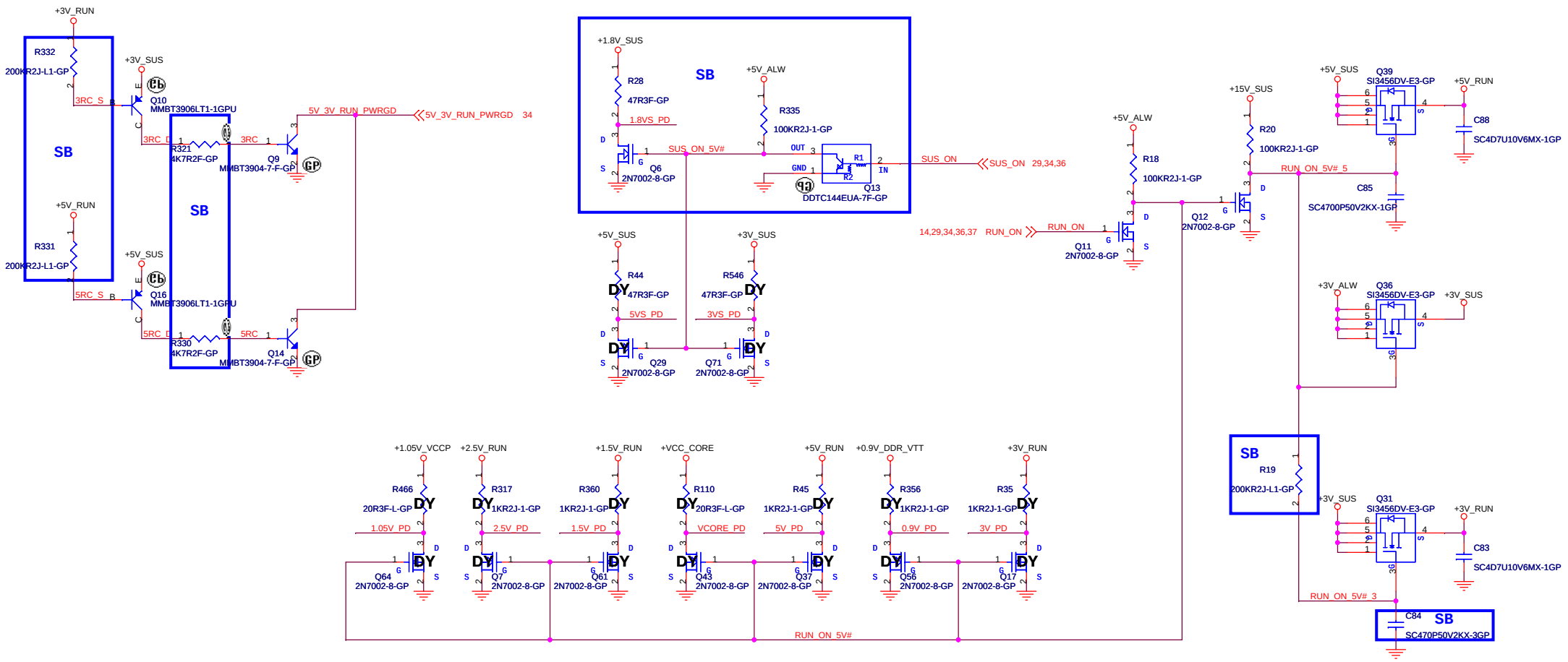
REM_DIODE3_N and REM_DIODE3_PC routing Trace width and Spacing use 10 / 10 mil

Please near the DIMM

Note :

VSET = (Tp - 70) / 21
3.3 * (R364 / R365 + R364) = (Tp - 70) / 21
Where Tp = 70 to 101 degrees C
Tp set at 85 degrees C
Guardian temp tolerance = +/- 3 degrees C

DELL	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	THERMAL Sensor & FAN	
Size A3	Document Number Bermuda	Rev -1
Date: Wednesday, March 01, 2006	Sheet 32 of 45	



Wistron Corporation
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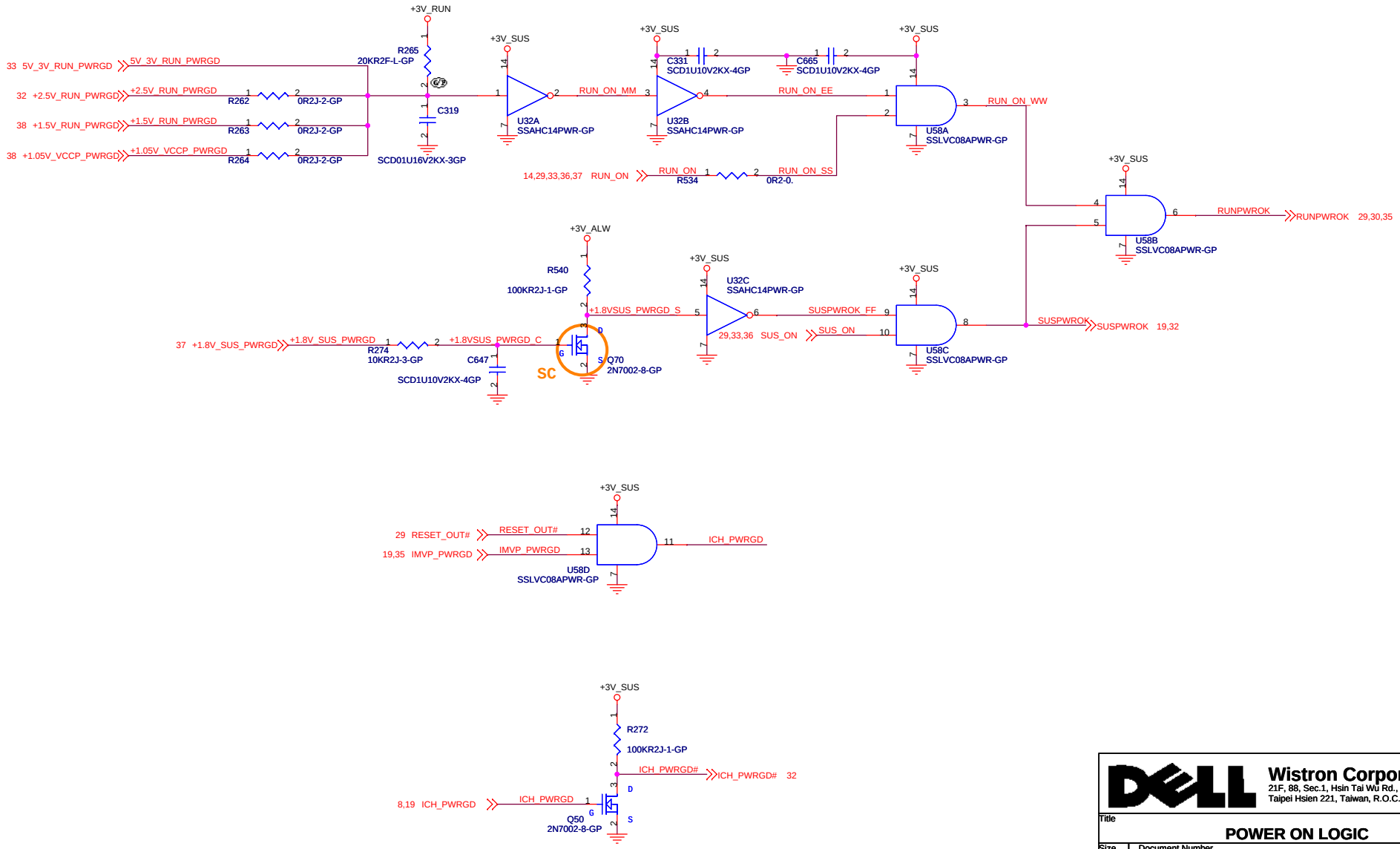
Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWER PLANE ENABLE**

Size	Document Number	Rev
A3	**Bermuda**	-1

Date: Wednesday, March 01, 2006 Sheet 33 of 45



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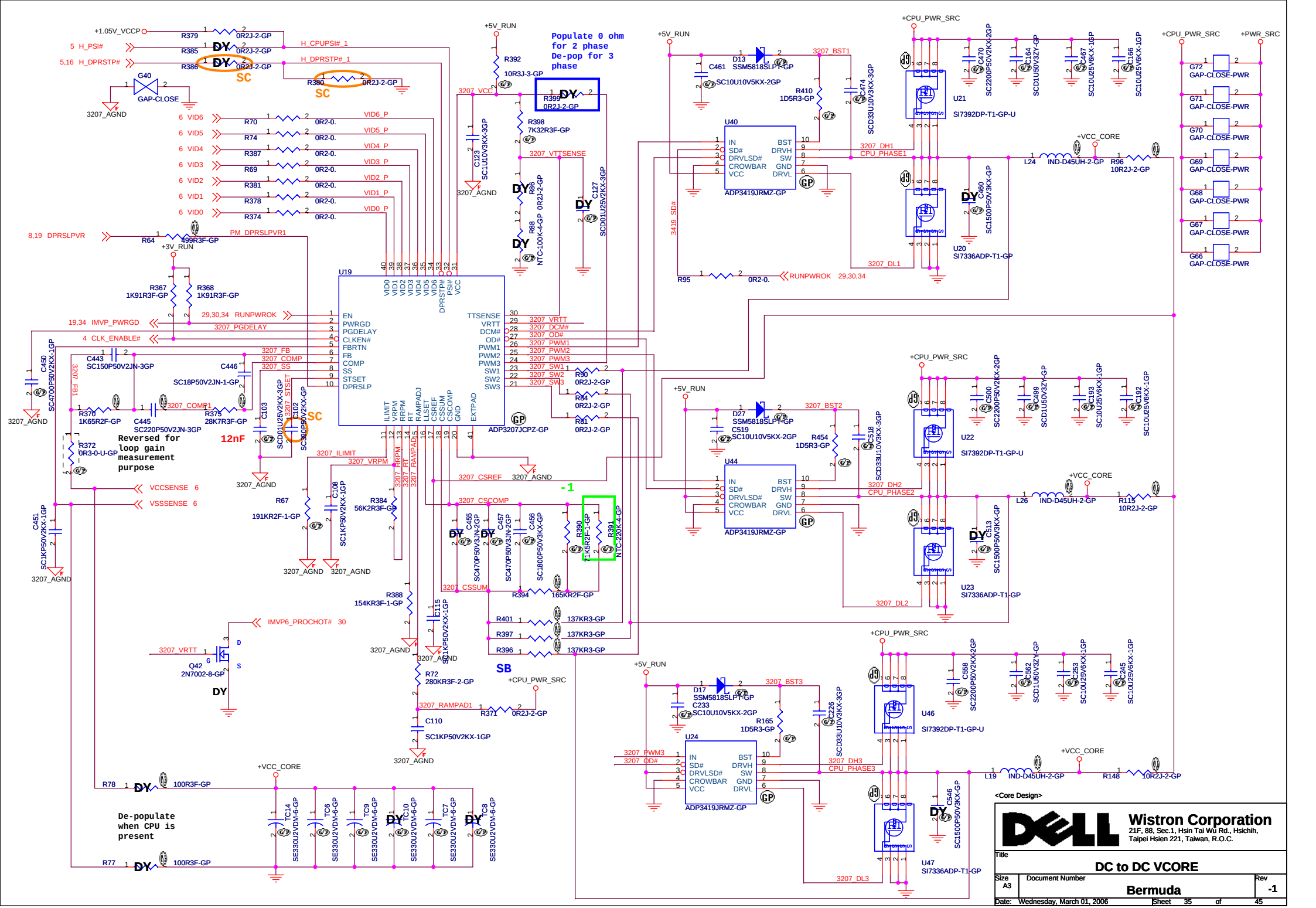
Title		
POWER ON LOGIC		
Size A3	Document Number Bermuda	Rev -1
Date: Wednesday, March 01, 2006	Sheet 34 of 45	

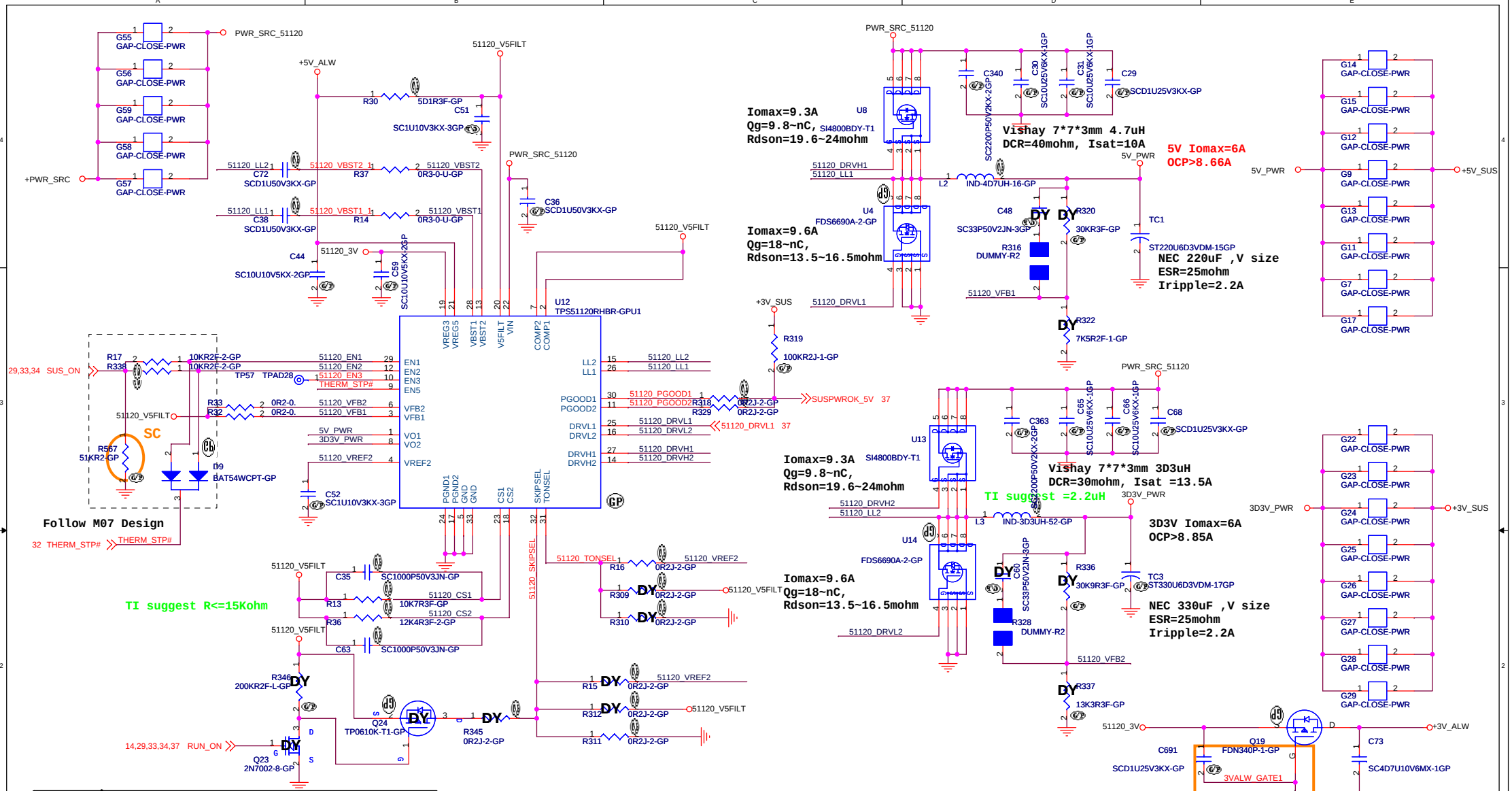


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC VCORE

Size: A3 | Document Number: Bermuda | Rev: -1

Date: Wednesday, March 01, 2006 | Sheet 35 of 45



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 580k/CH2	**280k/CH1 430k/CH2**	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	Swithchr ON	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

Vout=1V*(R1+R2)/R2

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

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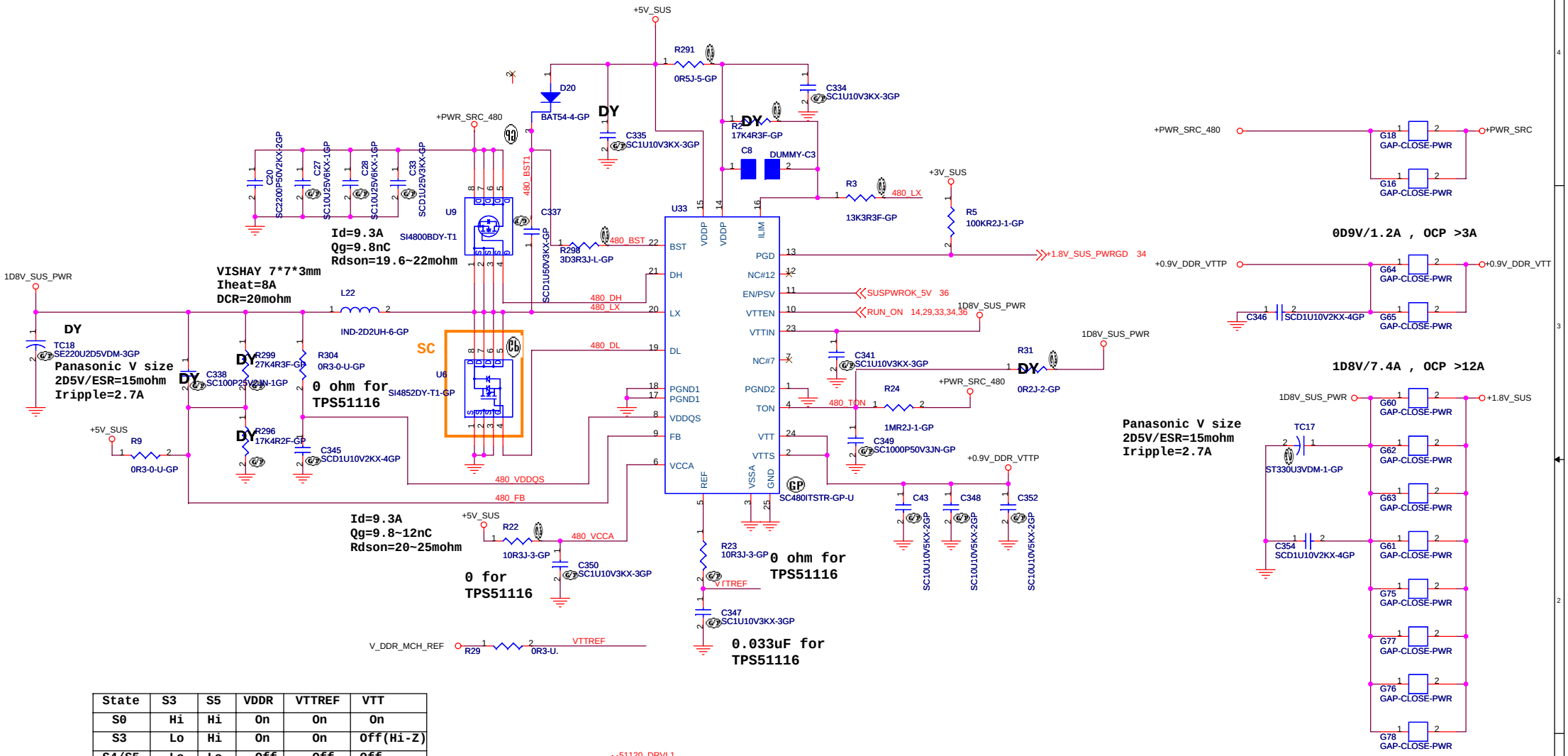
Title: **DC to DC 3.3V & 5V**

Size: A3 | Document Number: **Bermuda** | Rev: **-1**

Date: Wednesday, March 01, 2006 | Sheet 36 of 45

SC480 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

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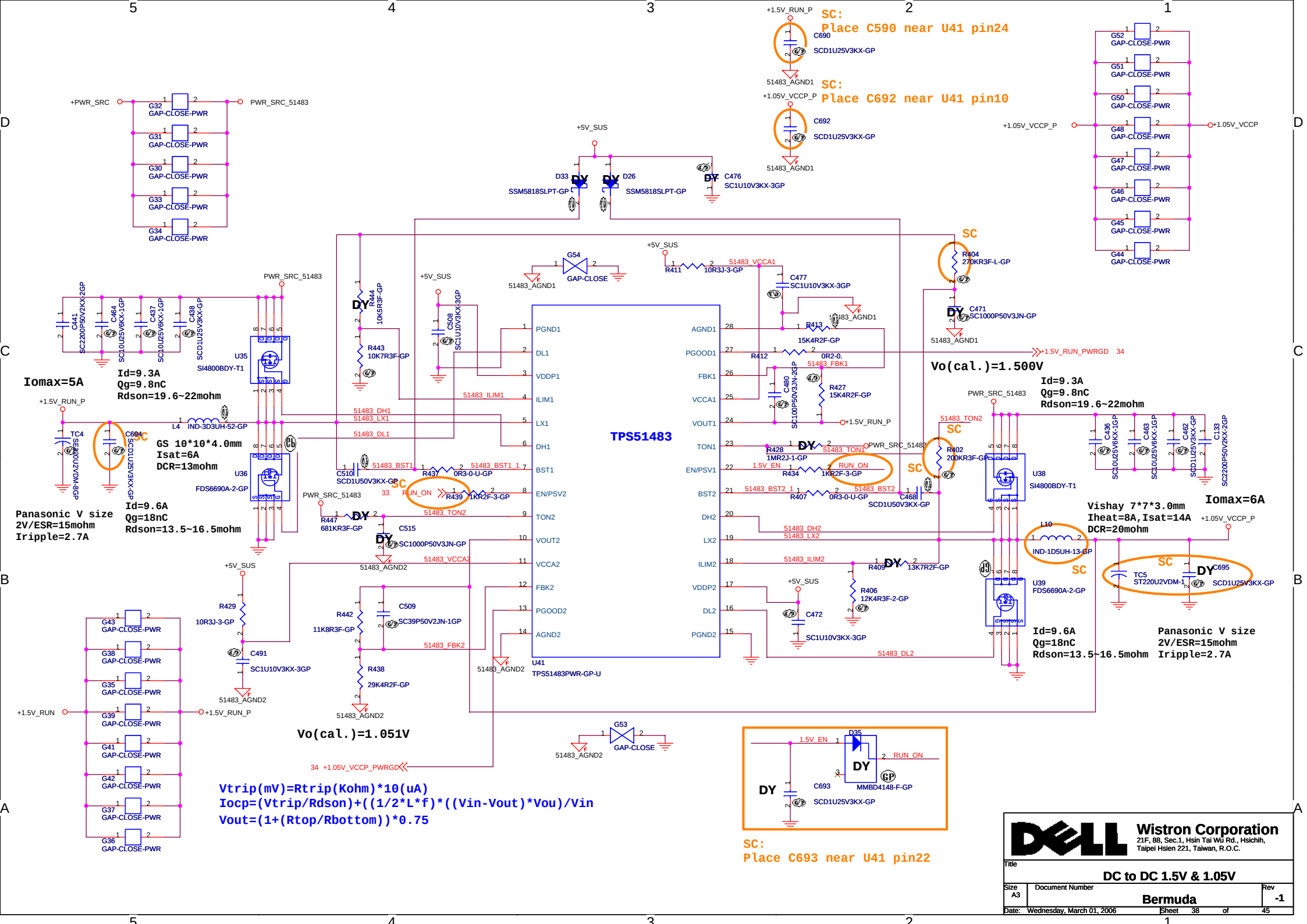
Title: DC to DC 1.8V & 0.9V & 15V

Size: A3 | Document Number: Bermuda | Rev: -1

Date: Wednesday, March 01, 2006 | Sheet 37 of 45


SC:
Place C590 near U41 pin24
SC:
Place C692 near U41 pin10
TPS51483
U41
TPS51483PWR-GP-U
Iomax=5A
Id=9.3A
Qg=9.8nC
Rdson=19.6~22mohm
GS 10*10*4.0mm
Isat=6A
DCR=13mohm
Id=9.6A
Qg=18nC
Rdson=13.5~16.5mohm
Panasonic V size
2V/ESR=15mohm
Iripple=2.7A
Vo(cal.)=1.500V
Vo(cal.)=1.051V
Iomax=6A
Vishay 7*7*3.0mm
Iheat=8A,Isat=14A
DCR=20mohm
Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/2*L*f)*((Vin-Vout)*Vou)/Vin
Vout=(1+(Rtop/Rbottom))*0.75
SC:
Place C693 near U41 pin22
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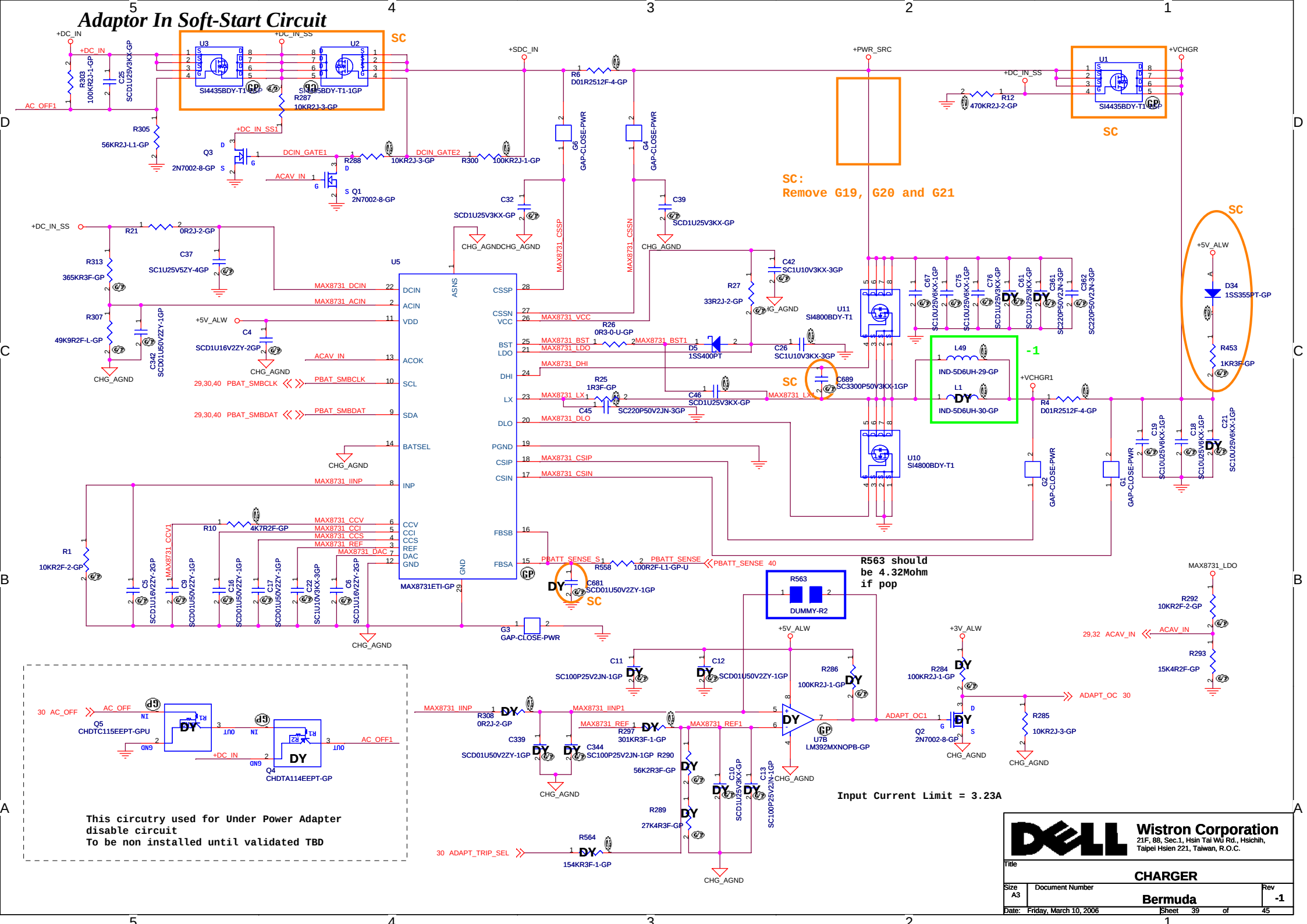
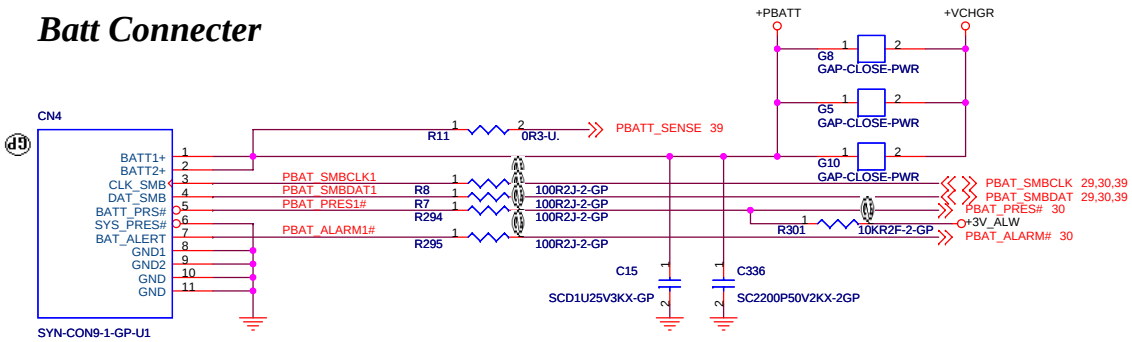
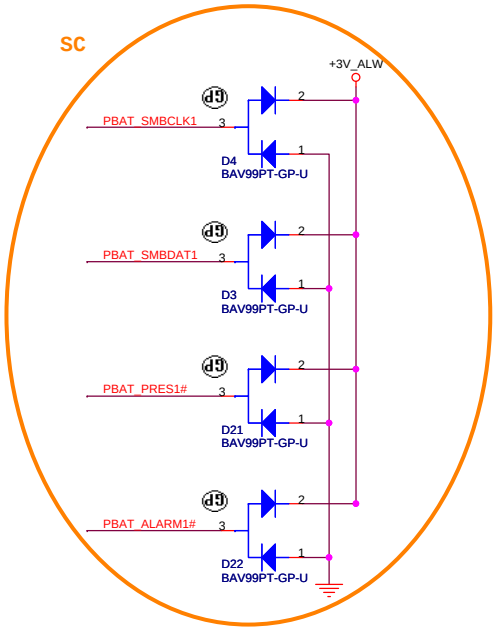
Title
DC to DC 1.5V & 1.05V
Size A3
Document Number
Bermuda
Rev -1
Date: Wednesday, March 01, 2006
Sheet 38 of 45

Adaptor In Soft-Start Circuit



Batt Connecter





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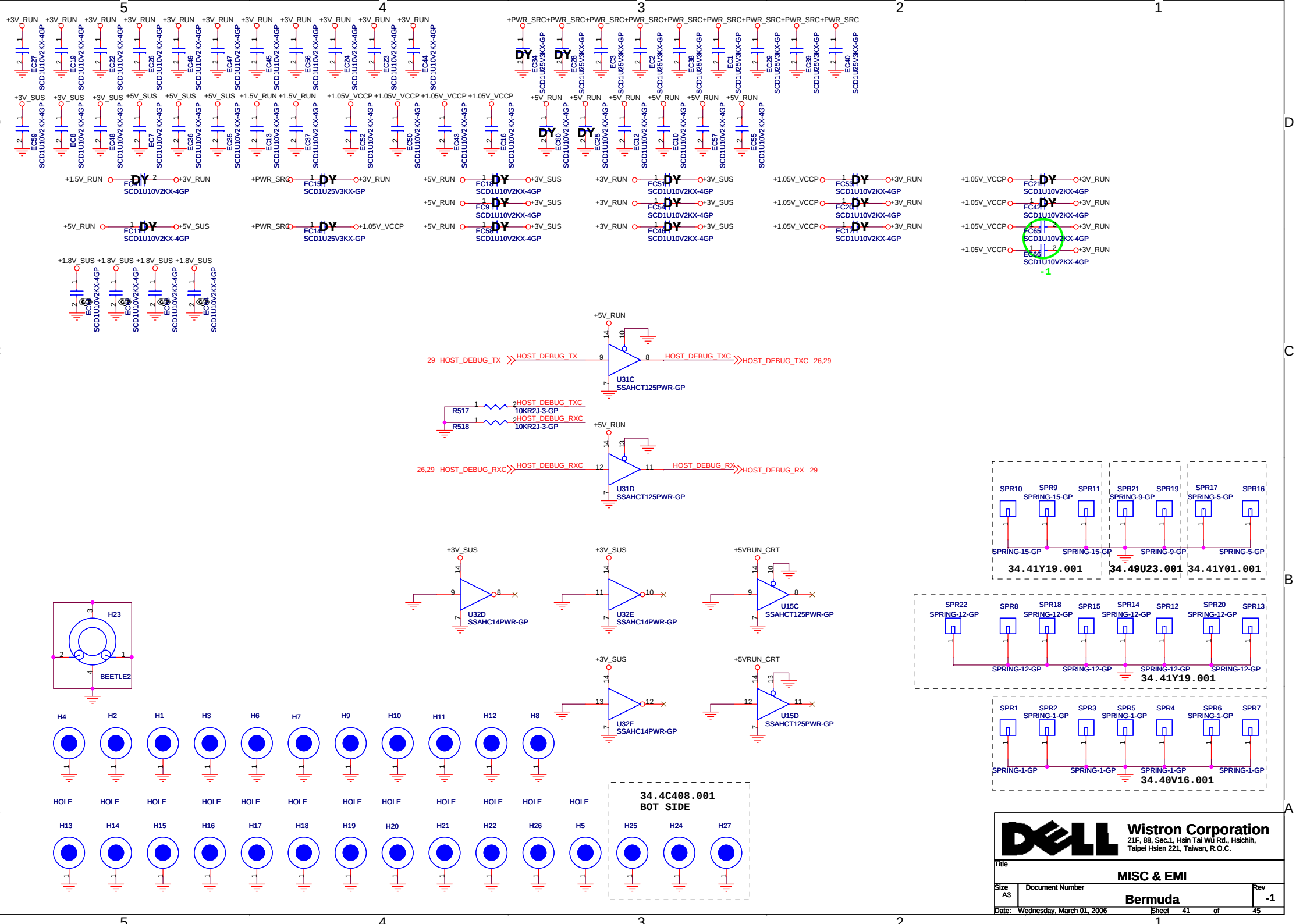
Title		
BAT Connector		
Size A3	Document Number Bermuda	Rev -1
Date: Wednesday, March 01, 2006	Sheet 40 of 45	


+3V_RUN
EC27 SCD1U10V2KX-4GP
EC19 SCD1U10V2KX-4GP
EC22 SCD1U10V2KX-4GP
EC26 SCD1U10V2KX-4GP
EC49 SCD1U10V2KX-4GP
EC47 SCD1U10V2KX-4GP
EC45 SCD1U10V2KX-4GP
EC56 SCD1U10V2KX-4GP
EC24 SCD1U10V2KX-4GP
EC23 SCD1U10V2KX-4GP
EC44 SCD1U10V2KX-4GP
+PWR_SRC
EC34 SCD1U25V3KX-GP
EC28 SCD1U25V3KX-GP
EC3 SCD1U25V3KX-GP
EC2 SCD1U25V3KX-GP
EC38 SCD1U25V3KX-GP
EC1 SCD1U25V3KX-GP
EC29 SCD1U25V3KX-GP
EC39 SCD1U25V3KX-GP
EC40 SCD1U25V3KX-GP
+3V_SUS
EC59 SCD1U10V2KX-4GP
EC8 SCD1U10V2KX-4GP
EC48 SCD1U10V2KX-4GP
EC7 SCD1U10V2KX-4GP
EC36 SCD1U10V2KX-4GP
EC35 SCD1U10V2KX-4GP
+5V_SUS
+1.5V_RUN
EC13 SCD1U10V2KX-4GP
EC37 SCD1U10V2KX-4GP
+1.05V_VCCP
EC52 SCD1U10V2KX-4GP
EC50 SCD1U10V2KX-4GP
EC43 SCD1U10V2KX-4GP
EC16 SCD1U10V2KX-4GP
+5V_RUN
EC60 SCD1U10V2KX-4GP
EC25 SCD1U10V2KX-4GP
EC12 SCD1U10V2KX-4GP
EC10 SCD1U10V2KX-4GP
EC57 SCD1U10V2KX-4GP
EC55 SCD1U10V2KX-4GP
EC41 SCD1U10V2KX-4GP
EC15 SCD1U25V3KX-GP
EC18 SCD1U10V2KX-4GP
EC51 SCD1U10V2KX-4GP
EC53 SCD1U10V2KX-4GP
EC21 SCD1U10V2KX-4GP
EC9 SCD1U10V2KX-4GP
EC54 SCD1U10V2KX-4GP
EC20 SCD1U10V2KX-4GP
EC42 SCD1U10V2KX-4GP
EC11 SCD1U10V2KX-4GP
EC14 SCD1U25V3KX-GP
EC58 SCD1U10V2KX-4GP
EC46 SCD1U10V2KX-4GP
EC17 SCD1U10V2KX-4GP
EC65 SCD1U10V2KX-4GP
EC66 SCD1U10V2KX-4GP
+1.8V_SUS
EC62 SCD1U10V2KX-4GP
EC63 SCD1U10V2KX-4GP
EC64 SCD1U10V2KX-4GP
EC61 SCD1U10V2KX-4GP
DY
-1
29 HOST_DEBUG_TX
HOST_DEBUG_TXC
HOST_DEBUG_TXC 26,29
U31C
SSAHCT125PWR-GP
R517 10KR2J-3-GP
R518 10KR2J-3-GP
HOST_DEBUG_RXC
26,29 HOST_DEBUG_RXC
HOST_DEBUG_RX
HOST_DEBUG_RX 29
U31D
SSAHCT125PWR-GP
+3V_SUS
U32D
SSAHC14PWR-GP
U32E
SSAHC14PWR-GP
+5VRUN_CRT
U15C
SSAHCT125PWR-GP
U32F
SSAHC14PWR-GP
U15D
SSAHCT125PWR-GP
H23
BEETLE2
SPR10 SPR9 SPR11 SPR21 SPR19 SPR17 SPR16
SPRING-15-GP
SPRING-9-GP
SPRING-5-GP
34.41Y19.001
34.49U23.001
34.41Y01.001
SPR22 SPR8 SPR18 SPR15 SPR14 SPR12 SPR20 SPR13
SPRING-12-GP
34.41Y19.001
SPR1 SPR2 SPR3 SPR5 SPR4 SPR6 SPR7
SPRING-1-GP
34.40V16.001
H4 H2 H1 H3 H6 H7 H9 H10 H11 H12 H8
HOLE
H13 H14 H15 H16 H17 H18 H19 H20 H21 H22 H26 H5 H25 H24 H27
34.4C408.001
BOT SIDE
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Title
MISC & EMI
Size A3
Document Number
Bermuda
Rev -1
Date: Wednesday, March 01, 2006
Sheet 41 of 45

CPU_Core
ADP3207+ADP3419

Input signal	Output Signal
EN	PWRGD
FBRTN	
FB	CLKEN#
DPRSLP	
PSI#	
DPRSTP#	
VID0~6	
Input Power	**Output Power**
VCC	

RUNPWROK, VSSSENSE, VCCSENSE, DPRSLPVR, H_PSI#, H_DPRSTP#, VID0~6

IMVP_PWRGD, CLK_ENABLE#

+5V_RUN → VCC; +VCC_CORE

5V/3D3V
TI TPS51120

Input signal	Output Signal
EN1	VREG2
EN2	VREG3
EN3	VREG5
EN5	PGOOD1
SKIPSEL	PGOOD2
TONSEL	
VO1	
VO2	
Input Power	**Output Power**
VIN	

SUS_ON / THERM_STP#, SUS_ON / THERM_STP#, SUS_ON / THERM_STP#, GND, 51120_VREF2, 5V_PWR, 3D3V_PWR

PWR_SRC_51120 → VIN

51120_VREF2, 51120_3V, +5V_ALW, SUSPWROK_5V, SUSPWROK_5V

5V_PWR, 3D3V_PWR

1D8V/0D9V
TPS51116

Input signal	Output Signal
EN/PSV (5V)	
VTTEN (5V)	PGD
TON (<5V)	
VDDP (5V)	
Input Power	**Output Power**
VTTIN	
VTTS	
VDDQS	VTT
VCCA	

SUSPWROK_5V, RUN_ON_D, 1D8V_SUS_PWR, +5V_SUS

1D8V_SUS_PWR, +0.9V_DDR_VTTP, 1D8V_SUS_PWR, +5V_SUS

+1.8V_SUS_PWRGD

1D8V_SUS_PWR, +0.9V_DDR_VTTP

1D5V/1D05V
TI TP51483

Input signal	Output Signal
EN/PSV2 (5V)	PGOOD2
TON2 (5V)	PGOOD1
EN/PSV1 (5V)	
TON1 (5V)	
Input Power	**Output Power**
VOUT2	
VCCA2	
VDDP2	
VOUT1	
VCCA1	
VDDP1	

RUN_ON_DC, 51483_TON2, RUN_ON_DC, 51483_TON1

+1.05V_VCCP_P, +5V_SUS, +5V_SUS, +1.5V_RUN_P, +5V_SUS, +5V_SUS

+1.05V_VCCP_PWRGD, +1.5V_RUN_PWRGD

+1.5V_RUN_P, +1.05V_VCCP_P

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Title: POWER DIAGRAM

Size: A3 | Document Number: Bermuda | Rev: -1

Date: Wednesday, March 01, 2006 | Sheet 42 of 45

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
2005/11/03	X00 to X01	1	37	U33 Pin10 change connect from RUN_ON_D to RUN_ON	Follow M07 design	EE
		2	26,29,41	HOST_DEBUG_TX and HOST_DEBUG_RX connect to U31 first then connect to connecter(DBG2)	TX,RX need add buffer for debug	EE,SW
		3	8	Del RN40 and add R551,R552(10k ohm) then Pop R440	Implement C4E feature on DPRSLPVR	EE
		4	14,29	Smbus which connect to LCD connecter change to SBAT_SMBDAT and SBAT_SMBCLK	This is follow M07 design	EE
		5	15	C112,C113,C121,C129,C139,C155 change from 82p to 0.5p	For TV EA measurement pass	EE
		6	16	R228,R229 change from 33 ohm to 39 ohm	For Azalia EA measurement pass	EE
		7	16	Add R568(0 ohm) for X2(Crystal for ICH7M)	This is follow COE's suggestion	EE
		8	16	C297,C314 change from 4.7P to 3.3P for X2(Crystal for ICH7M)	CRYTAL Vendor suggestion	EE
		9	18	Change R472 to 0805 size and add L48(10UH)	This is follow COE's suggestion	EE
		10	19	Add R560,R561(100k)	Follow M07 design	EE
		11	21,22	Change C250 to 10uF and add C686(0.1u),C687(1u)	This is follow COE's suggestion	EE
		12	23	X1 change from 20p to 18p type crystal	By Broadcom's suggestion,Lan crystal need use 18p type	EE
		13	24	C642,C644 change from 18P to 15P for X5(Crystal for R5C832)	CRYTAL Vendor suggestion	EE
		14	25	Swap connection for CARD1 pin22 and pin23	Card pin22 and pin23 need swap for MS card function work normally	EE
		15	25	Change L29 and L37 to 110 ohm impedance type for 1394	X00 already use 110 ohm type only forget to modify schematic	EE
		16	26	Add D32 and depop R266 to prevent leakage from WAN_RADIO_DIS#	Follow M07 design	EE
		17	27	Change R353 connection from U35 pin1 to U35 pin3	COE's suggestion to prevent the wireless LED light strength not enough	EE
		18	27	R42,R43 change to 220ohm;R40 change to 470ohm	LED light strength need change to avoid light leak	EE
		19	27	Q33 and Q34 Pin1 from +5V_ALW to +3V_ALW	Change to +3VALW for battery LED work normally	EE
		20	29	RN4 and RN6 change from 8.2K to 1K and add R323,R324,R333,R334,C682,C683,C684,C686	For SMBUS EA measurement pass	EE
		21	29	C538,C544 change from 20P to 27P for X4(Crystal for MEC5004)	CRYTAL Vendor suggestion	EE
		22	29	Reversed R553,R554,R555,R556,R557,Q72,Q73,D31,C680,R560	KBC Work Around Circuit for MEC5004 Rev "C"	EE
		23	29	Add R559(0 ohm) to GND	To Fix Rev "C" KBC bug	EE
		24	30	Pop R244 and depop R225	Change BOARD ID to X01	EE
		25	32	Add R562(0 ohm) in EMC4000 pin 22	Easily debug for THERM_STP# signal	EE
		26	33	R321,R330 from 20K ohm to 4K7 ohm R331,R332 from 10K ohm to 200K ohm	To prevent leakage from +3V_SUS to +3V_RUN when in suspend	EE
		27	33	Pop R28,R335,Q6,Q13	For 1.8V_SUS discharge more quickly	EE
		28	33	Change R19 to 200k and C84 to 470pF	For IMVP_PWRGD glitch issue,need make +5V_RUN more faster than +3V_RUN when boot up	EE
		29	33	REMOVE Q8,Q15,R323,R324,R333,R334	Follow M07 design	EE
		30	35	Change R394 to 165K and R396,R397,R401 to 137K then depop C457	This is changed for Vcore load line test fail	Power
		31	35	Change R410,R454 and R165 to 1.5 ohm	This is changed for Vcore's ring over spec	Power
		32	36	Add R565 and R566 for SUS_ON unstable when plug adapter	This is recommended by TDC Lawrence	Power
		33	36	Change TC3 to another source	This is recommended by power team	Power
		34	37	Depop TC18 and change TC17 to 330uF;change D20 to BAT54;change R3 to 13K3 ohm;change R298 to 3D3 ohm	This is recommended by power team	Power
		35	37	New add 4 gaps G75,G76,G77,G78 for 1.8V	This is requested by EMI	EMI
		36	38	Change R427 to 15K4 ohm	This is recommended by power team	Power
		37	39	Add R558,C682 in U5 pin15 pin16 for PBATT_SENSE	To prevent Charger damage when plug battery	Power
		38	39	ADD ADAPT_TRIP_SEL circuit	Follow M07 schematic	Power
		39	41	Add EC61,EC62,EC63.EC64,SPR22 and depop EC41,EC11,EC15,EC14,EC9,EC18,EC58,EC46 ,EC51,EC54,EC17,EC20,EC53,EC21,EC42	This is for EMI	EMI

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Title: HISTORY from X00 to X01

Size: A3 | Document Number: Bermuda | Rev: -1

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
2006/01/03	X01 to X02	1	6	Change CPU 22uF to 10uF for power noise,total 32 pieces	Power team suggestion	Power
		2	17,29	Add R573(47 ohm) and R574 (0 ohm) during ICH7M and KBC for SPI_CS# to verify signal quality	Suggestion by COE	EE
		3	19	Change R560 and R561 to no pop	Suggestion by COE	EE
		4	20	Reversed Pad for R577(0 ohm),because Seagate SATA HDD driver will make S3 resume issue on spin-up mode	Suggestion by COE	EE
		5	22	Pop C525 for VREFOUT	Suggestion by COE	EE
		6	25	Change U57 to G5240 for OCP Issue	Suggestion by COE	EE
		7	29	Pop R200 and de-pop R201	Enable internal bootblock flash function	EE
		8	30	Pop R243 and R225, de-pop R244 and R224	Change Board ID to X02	EE
		9	30	New add R575 and R576 for HDDC_EN# and MODC_EN#	Suggestion by COE	EE
		10	34	Change Q70 from 3904 to 2N7002	Suggestion by COE	EE
		11	35	De-pop R386 and pop R380	Power team suggestion	Power
		12	35	Change C102 from 680PF to 390PF	Power team suggestion	Power
		13	36	Add R567(51k ohm) from SUS_ON to GND to avoid SUS_ON glitch issue	Power team suggestion	Power
		14	36	Add C691 and R572 for +3V_ALW soft-start	Power team suggestion	Power
		15	37	Change U6 to SI4852DY	Power team suggestion	Power
		16	38	Change the enable pin of TPS51483 connection from RUN_ON_D to RUN_ON	Power team suggestion	Power
		17	38	Change R402 to 200k and R404 to 270K and L10 to 1D5UH	Power team suggestion	Power
		18	38	Add C690,C692,C694 and reversed C695 for 1.5V noise issue	Power team suggestion	Power
		19	38	Reversed C693 and D35 for 1.5V enable signal	Power team suggestion	Power
		20	39	Change U1,U2 and U3 to SI4435BDY	Power team suggestion: AOS is not in Dell QVL	Power
		21	39	Remove G19, G20 and G21	Power team suggestion	Power
		22	39	New add C689 (3300 PF)	Suggestion by MAXIM	Power
		23	39	New add D34 and R453 to solve MAX8731 can't charge battery when battery voltage lower than 2.5V	Suggestion by MAXIM	Power
		24	39	De-pop C681	Power team suggestion	Power
		25	40	Change D3,D4,D21,D22 connection way,before is after resistors but now change to connect battery connecter first then to resistors	This is ESD issue,the ESD diode need to be placed near to battery connecter	EMI
		26	29	Change X4 to XTAL 32.768K 6PF10PPM	This is because Barbados lesson learn,old crystal sometimes will make system can not boot.	EE

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Title: HISTORY from X01 to X02

Size: A3 | Document Number: Bermuda | Rev: -1

Date: Wednesday, March 01, 2006 | Sheet 44 of 45

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
2006/02/22	X02 to A00	1	24	De-pop R541 and pop R547 and C669 for GBSRST#	Suggestion by COE	EE
		2	29	Change X4 to XTAL 32.768K 12.5P10PPM DMX26S and sloe change C544 to 18P and C538 to 22P	Suggestion by KDS and Epson	EE
		3	30	Depop R225 and pop R244 for Board ID change	Change Board ID to X03	EE
		4	31	Add D36 and reversed R578 for leakage issue	To prevent leakage issue	EE
		5	35	Change R391 vendor from MURATA to MITSUBISHI	Suggestion by Power Team	Power
		6	36	Change R341 from 10K ohm to 1K ohm	Suggestion by Power Team	Power
		7	39	Depop L1 and pop L49 for DFX issue	Suggestion by Power Team	Power
		8	41	Add EC65 and EC66 for EMI's request	EMI's request	EMI
		9	27	For BREATH LED==>R40 change to 150 ohm For HDD LED==>R41 change to 51 ohm For battery LED==>R42 and R43 change to 51 ohm	Change brightness of LED	EE

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Title: HISTORY from X02 to X03

Size: A3 | Document Number: Bermuda | Rev: -1

Date: Wednesday, March 01, 2006 | Sheet 45 of 45