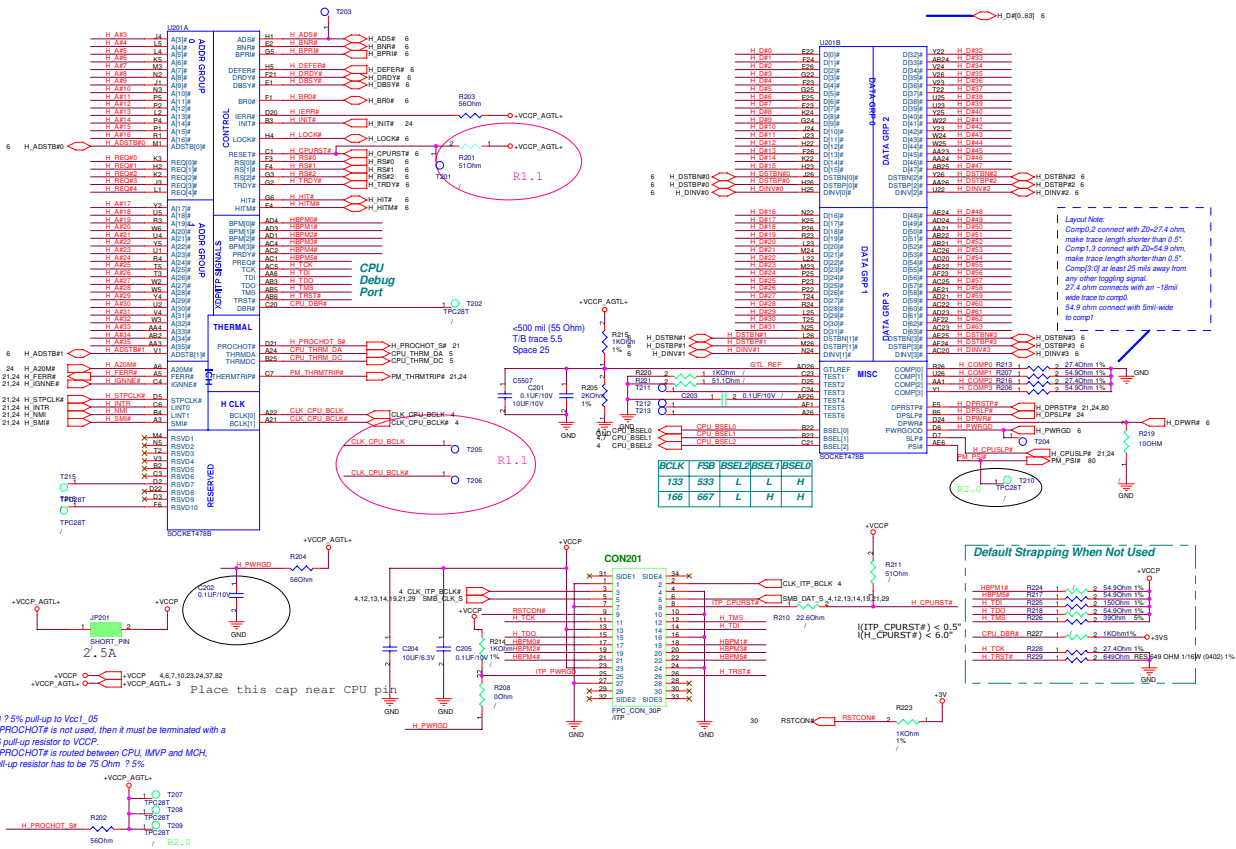


<< Kennedy_Zhang >>

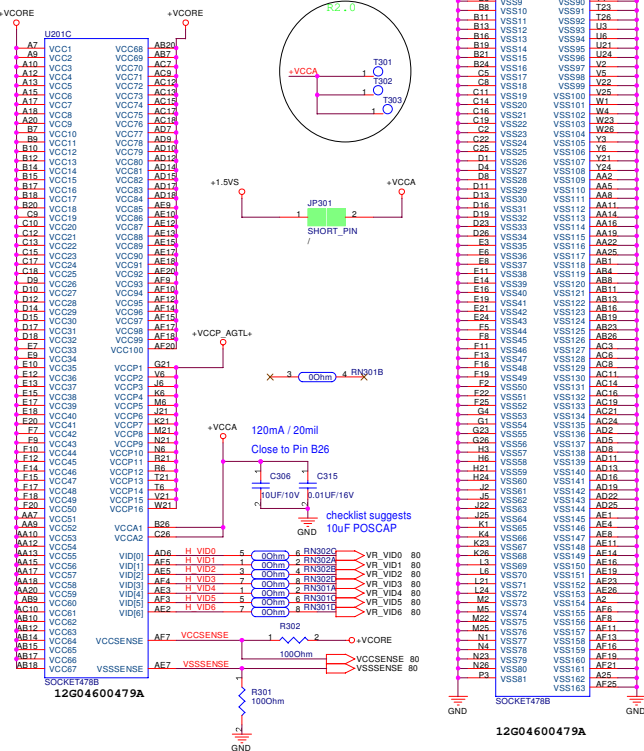
6 H_A016.3
6 H_A016.4
6 H_A016.5



<< Kennedy_Zhang >>

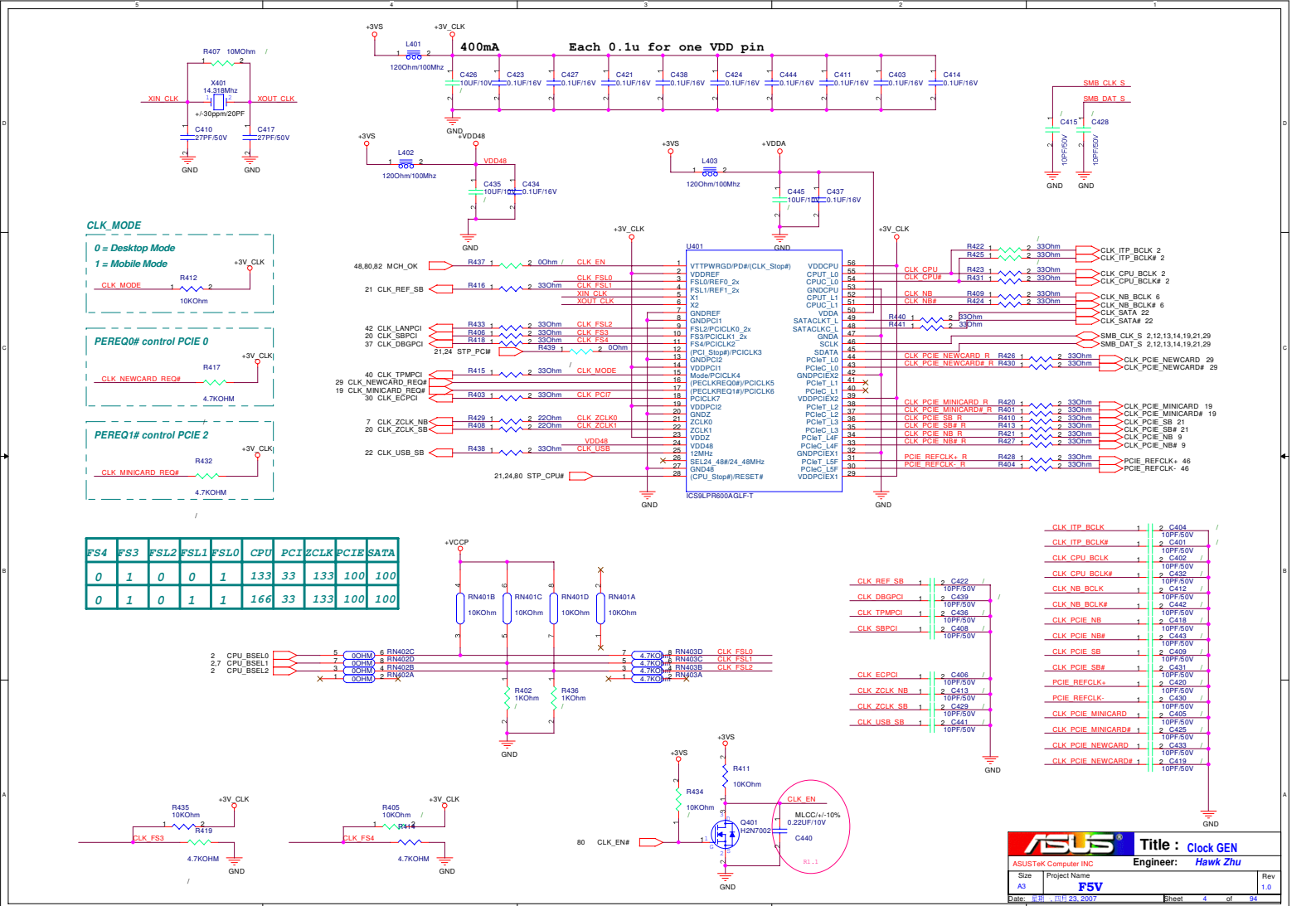
YUNAH FSB667
LFM TYP HFM
VCC 1.14V 1.2V 1.356V
C4 C3 C0
ICC 0.9A 7.59A 27A

YUNAH FSB667
Min Typ Max
VCCP 0.997V 1.05V 1.102V
Min Typ Max
ICCP 2.5A



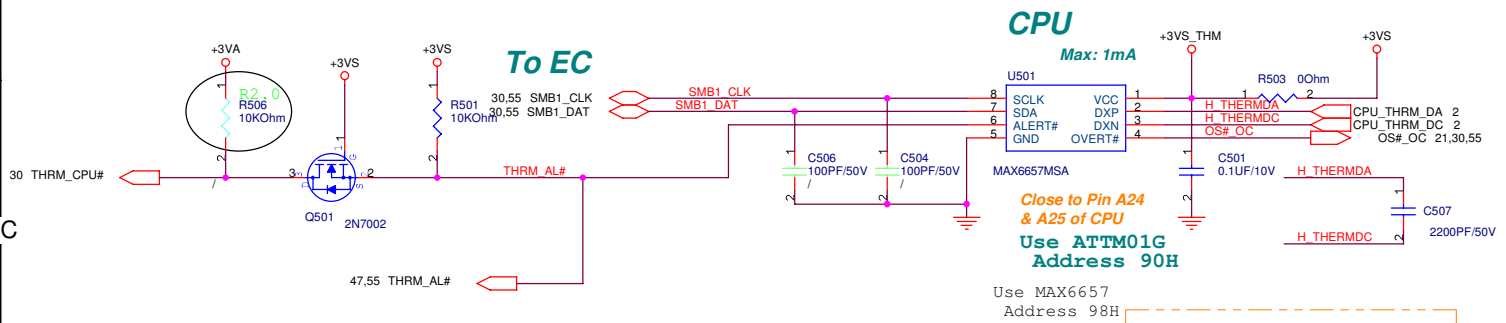
Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of 20-27.4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.

<< Kennedy_Zhang >>

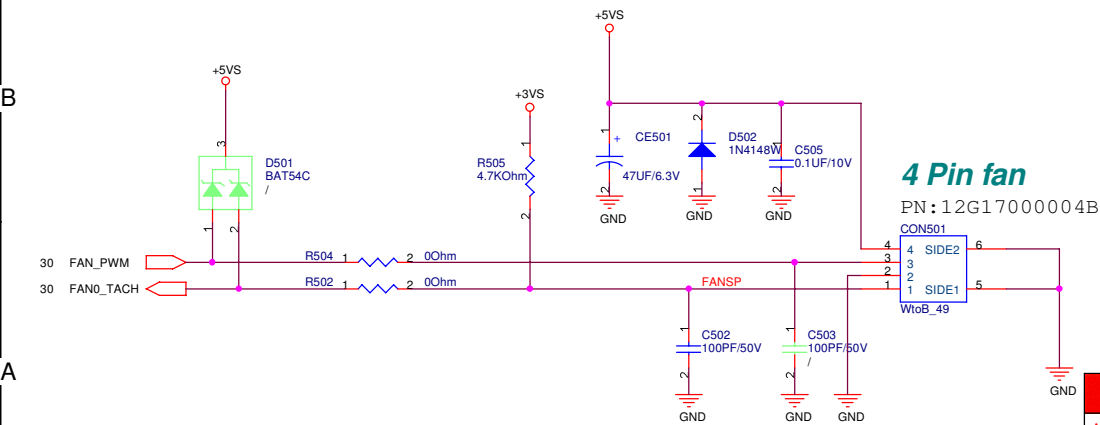


<< Kennedy_Zhang >>

Thermal Sensor



DC FAN Control



Route H_THERMDA and H_THERMDC
on the same layer

-----OTHER SIGNALS

20 mls
-----GND

10 mils

=====H_THERMDA(10 mils)
10 mils


```
=====H_THERMDO
```

10 mils

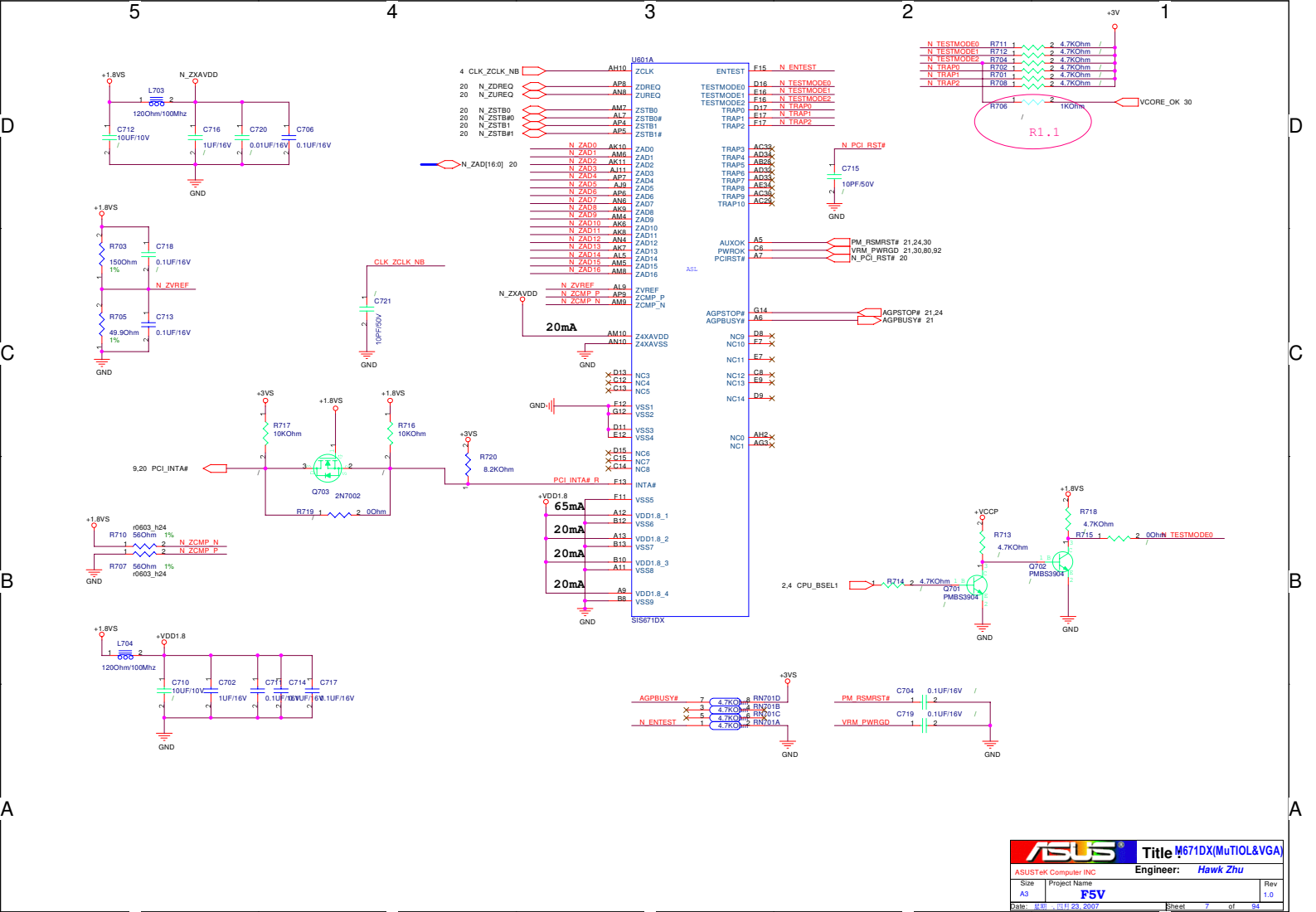
-----GND
20 mils

-----OTHER SIGNALS

Avoid FSB,Power

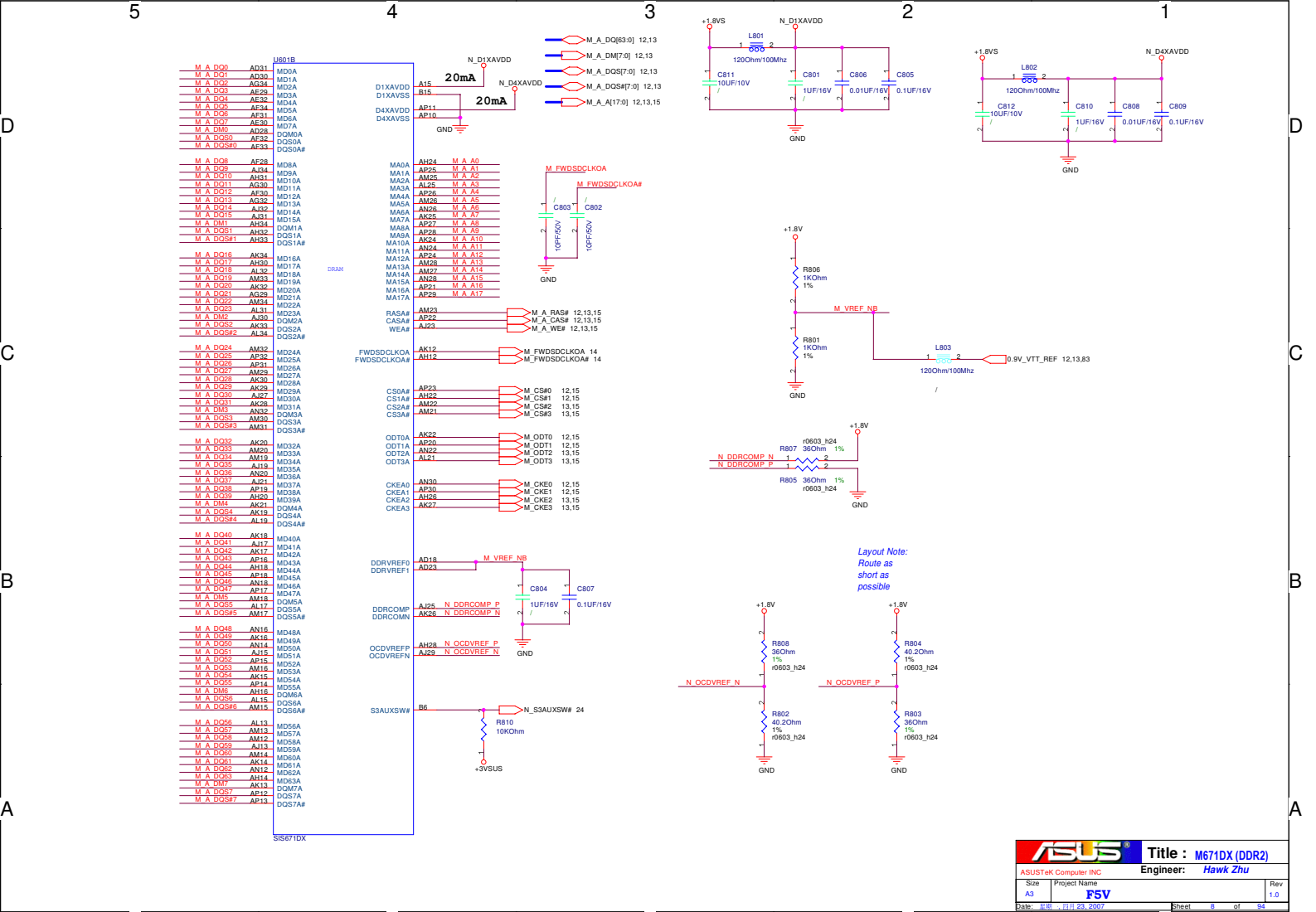
		Title : Thermal Sensor	
ASUSTeK Computer INC		Engineer: Hawk Zhu	
Size A4	Project Name F5V		Rev 1.0
Date: 星期四, 西曆 23, 2007		Sheet 5	of 94

<< Kennedy_Zhang >>



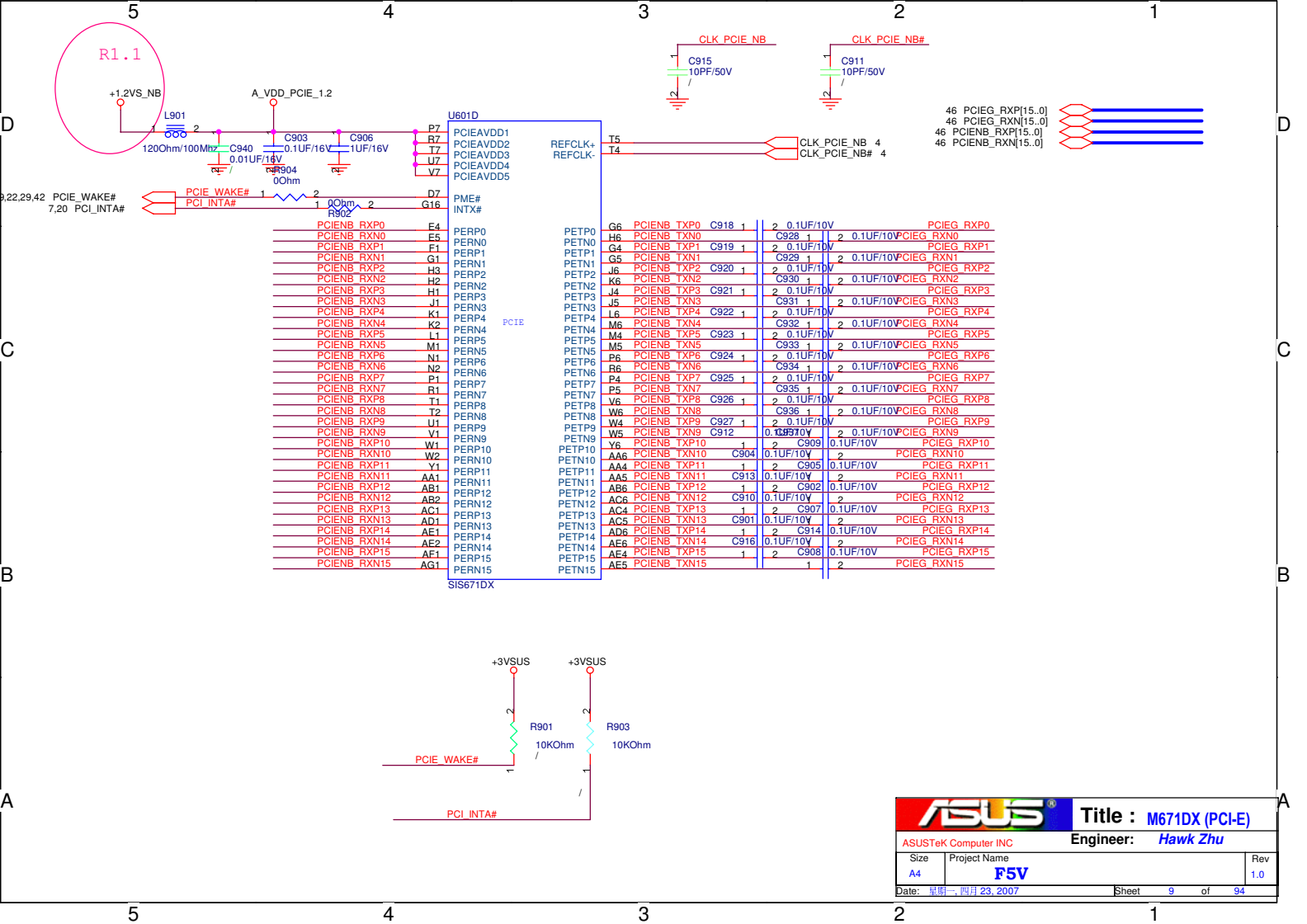
<< Kennedy_Zhang >>

ASUS		Title: M671DX(MuTIO&VGA)	
ASUSTek Computer INC		Engineer: Hawk Zhu	
Size: A3	Project Name: FSV	Rev: 1.0	
Date: 2007-11-23		Sheet: 7 of 94	



<< Kennedy_Zhang >>

ASUS®		Title : M671DX (DDR2)	
ASUSTek Computer INC		Engineer: Hawk Zhu	
Size	Project Name		Rev
A3	F5V		1.0
Date: 11/11/23/2007		Sheet 8 of 94	



<< Kennedy_Zhang >>



<< Kennedy_Zhang >>

TOP

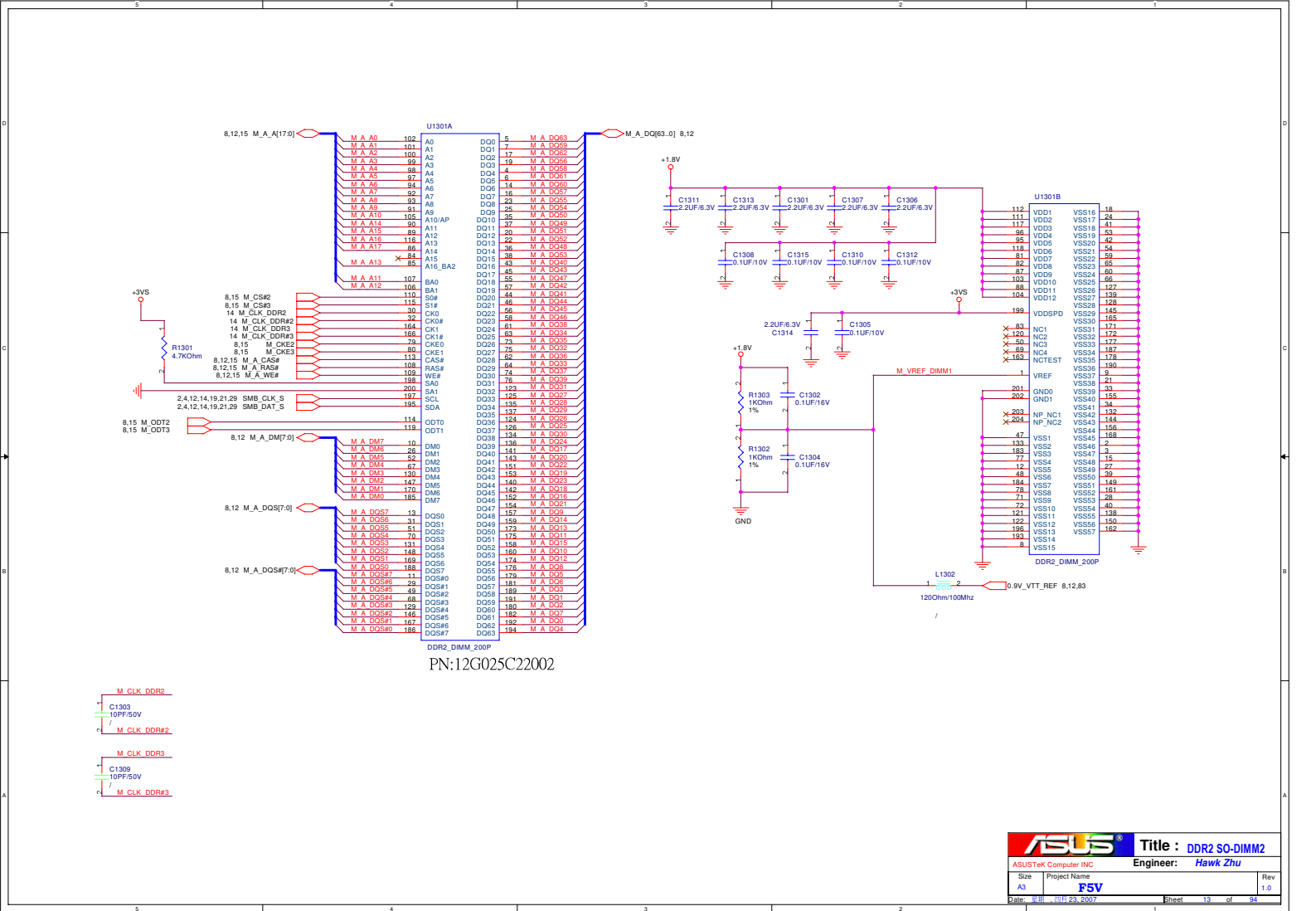
DDR2 SO-DIMM1

PN: 12C025122006

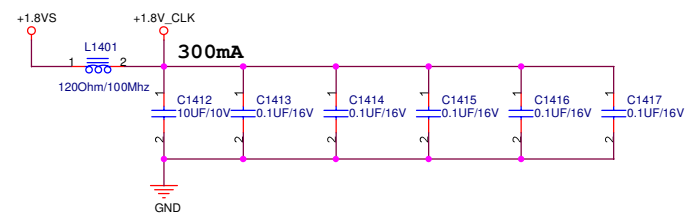
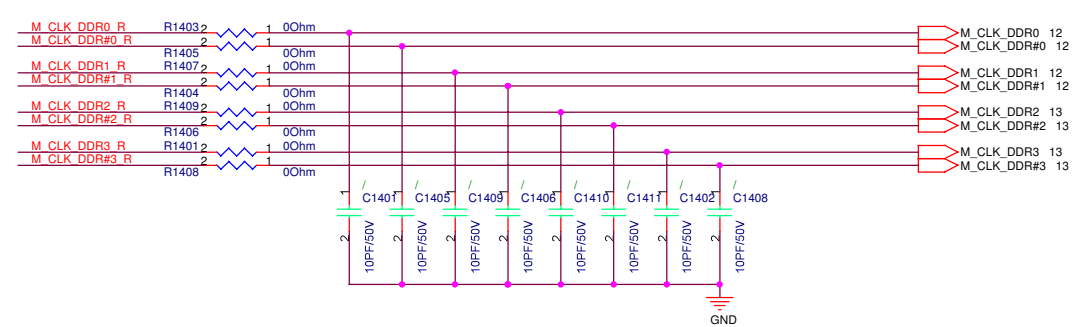
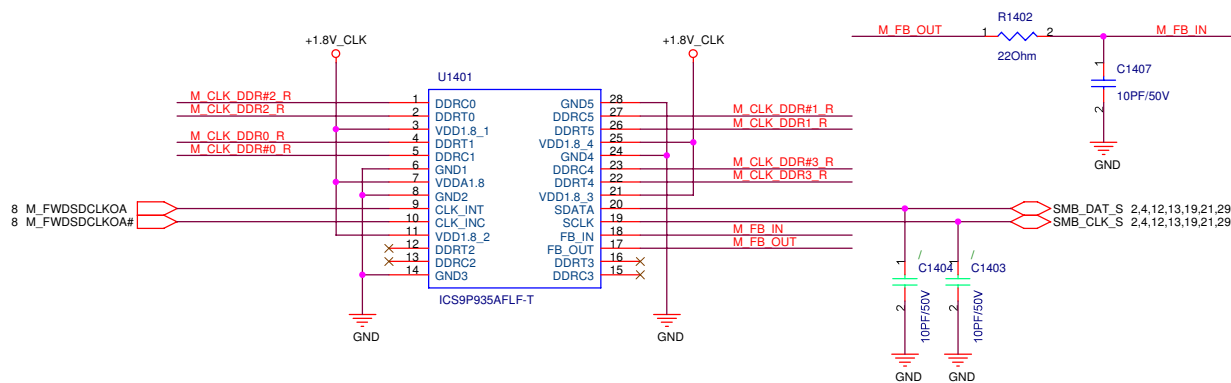
ASUS
ASUSTek Computer INC
Date: 11/23/2007
Sheet: 12 of 94

Title: DDR2 SO-DIMM1
Engineer: Hawk Zhu

Size: Project Name: F5V
Rev: 1.0

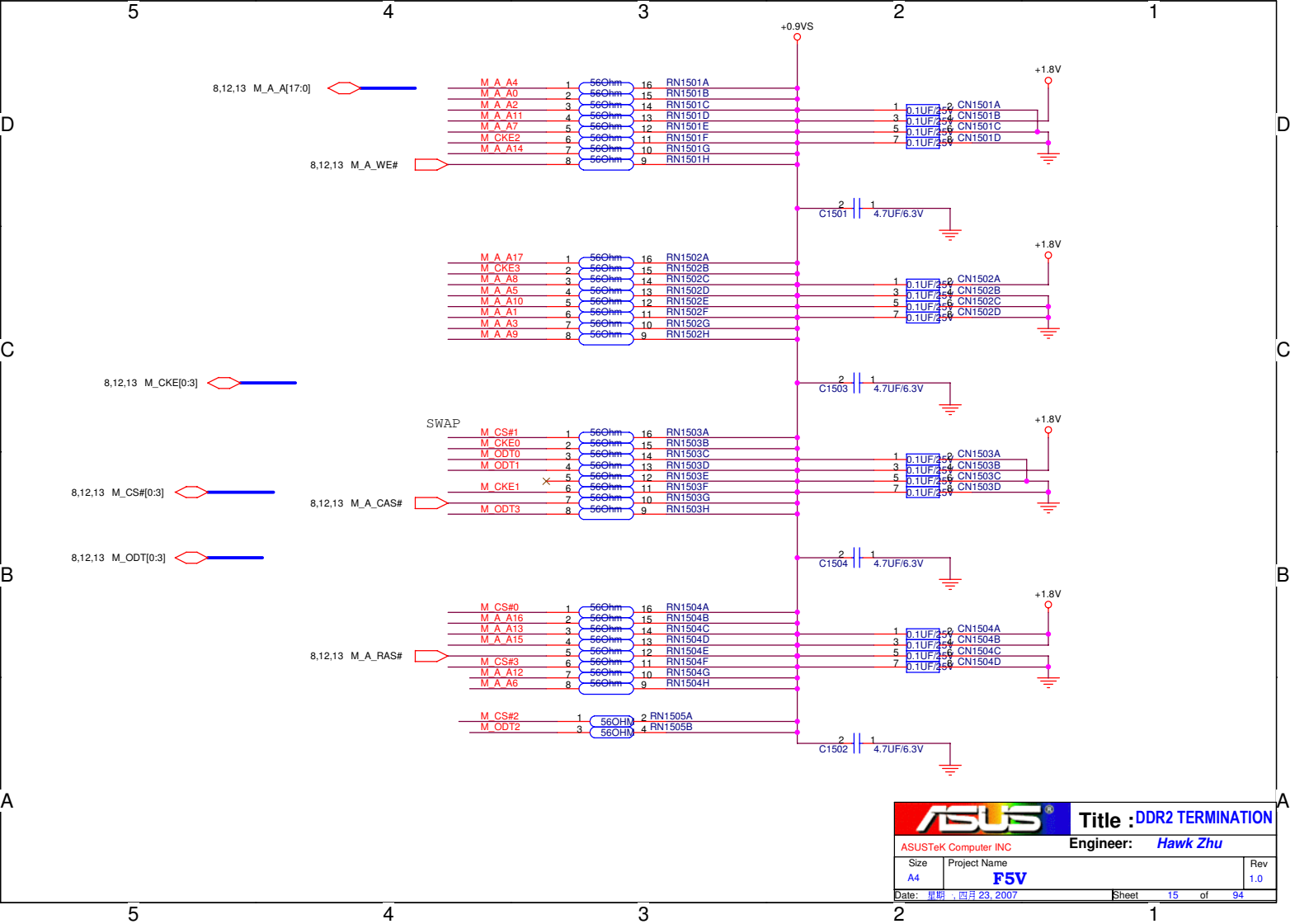


<< Kennedy_Zhang >>




ASUS		Title : DDR2 BUFFER	
ASUSTek Computer INC		Engineer: Hawk Zhu	
Size A4	Project Name F5V	Rev 1.0	
Date: 星期四, 四月 23, 2007		Sheet 14 of 94	

<< Kennedy_Zhang >>

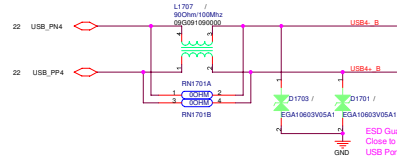
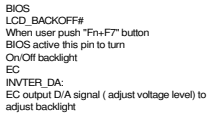


<< Kennedy_Zhang >>

<< Kennedy_Zhang >>

		Title : SIS	
ASUSTek Computer INC.		Engineer: Hawk Zhu	
Size	Project Name	Rev	
C	FSV	1.0	
Date: 2012-05-25 10:01	Sheet: 15	of	25

3~3.6V
S0-S1 M: 410
mA(Max. 500 mA)



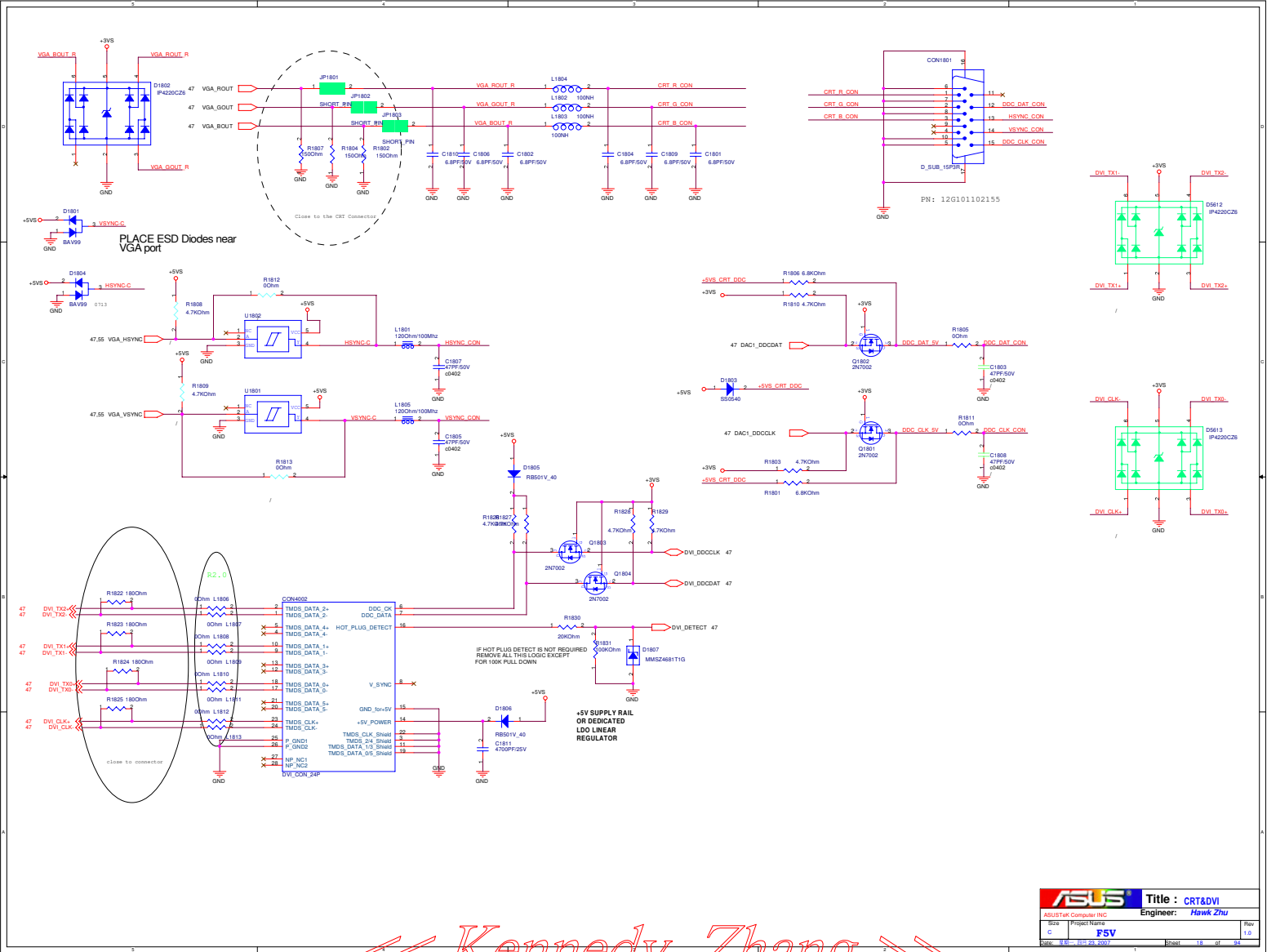
R1706 /
00hm r0402

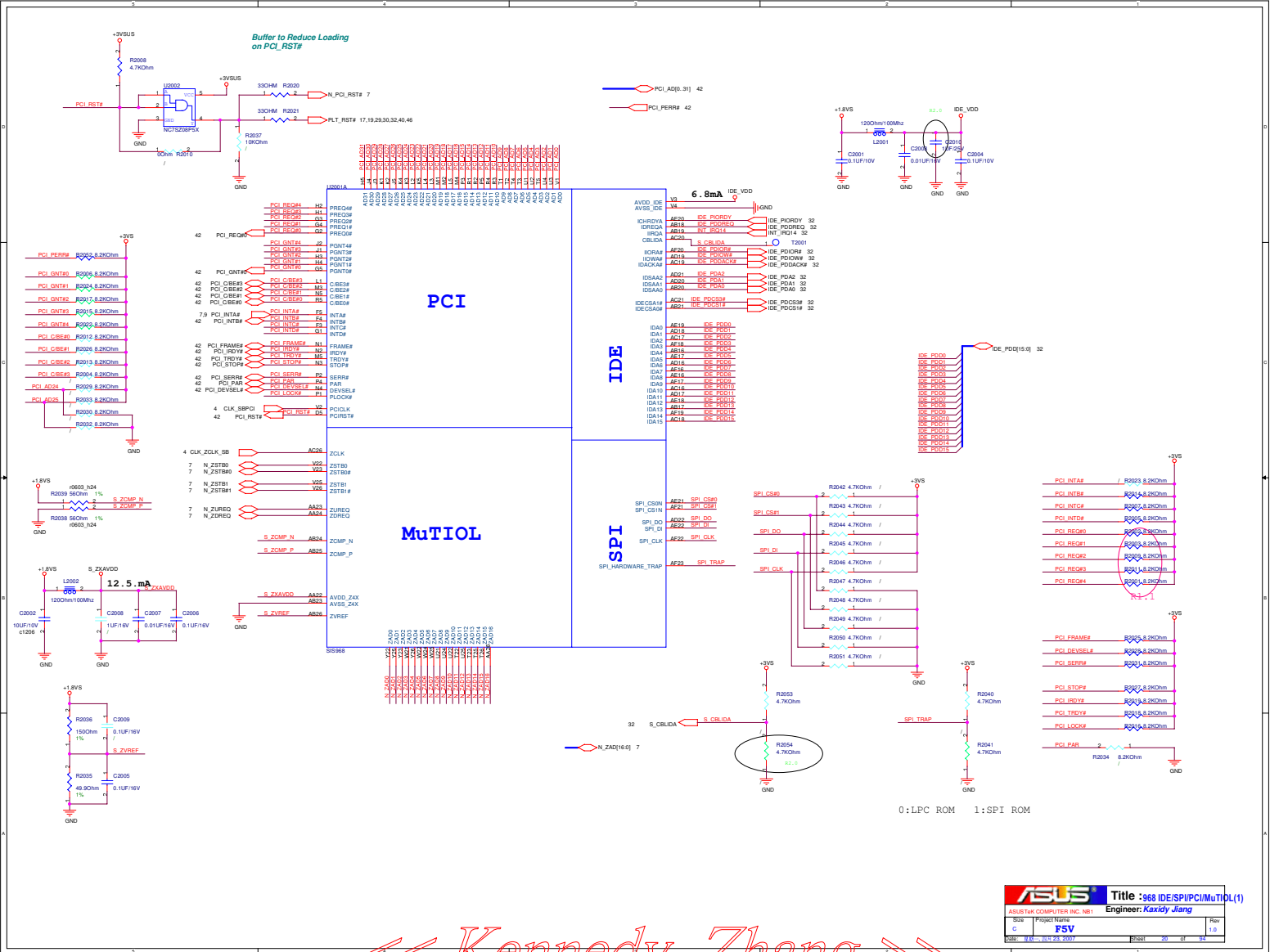
C1717
c0402 /
1000PF/50V

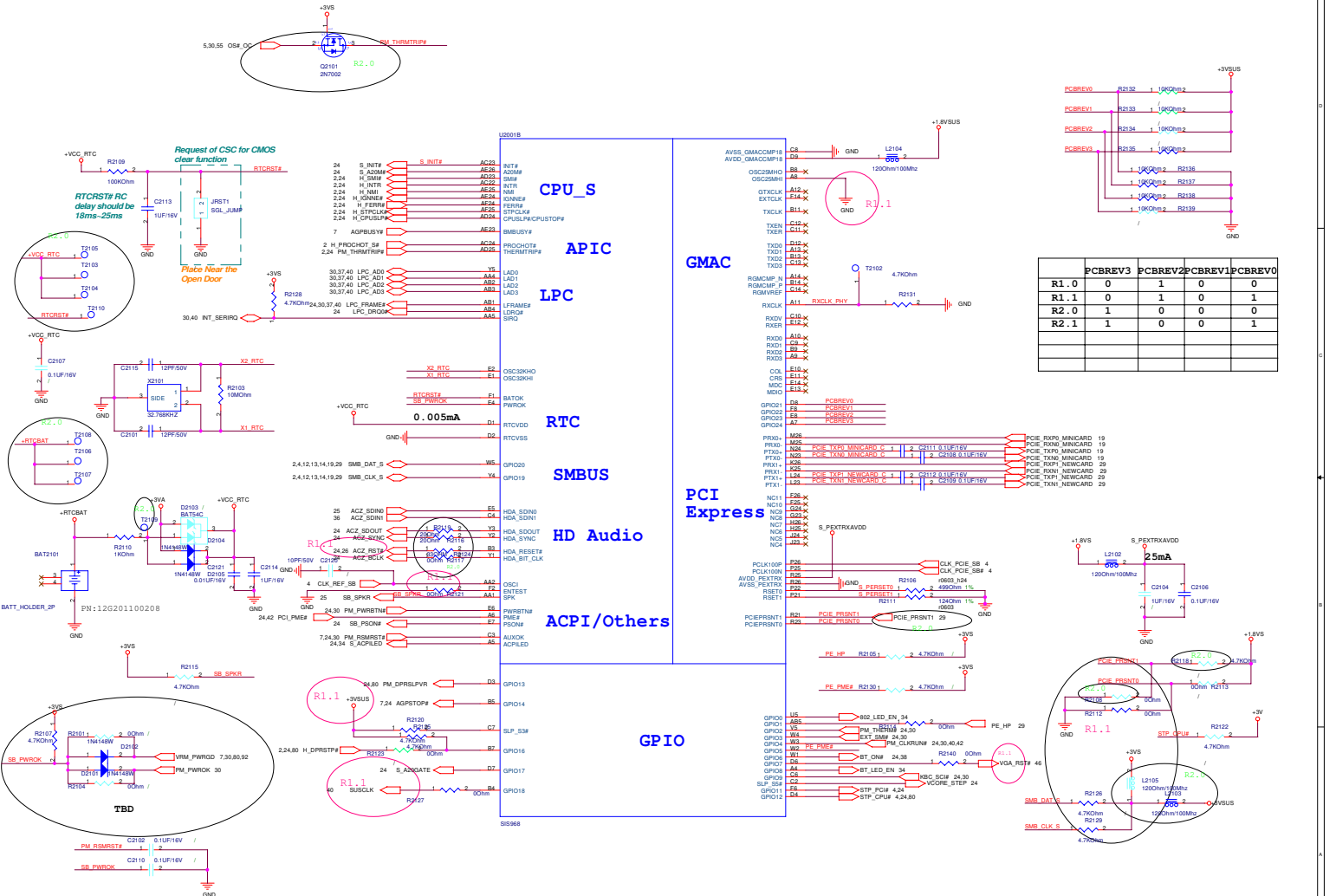
WLAN_ON# 19,24,3

		Title : LVDS	
ASUSTeK Computer INC		Engineer: Hawk Zhu	
Size C	Project Name F5V	Rev 1.0	
Date: 2007.03.23	Sheet	17	of 94

<< Kennedy_Zhang >>



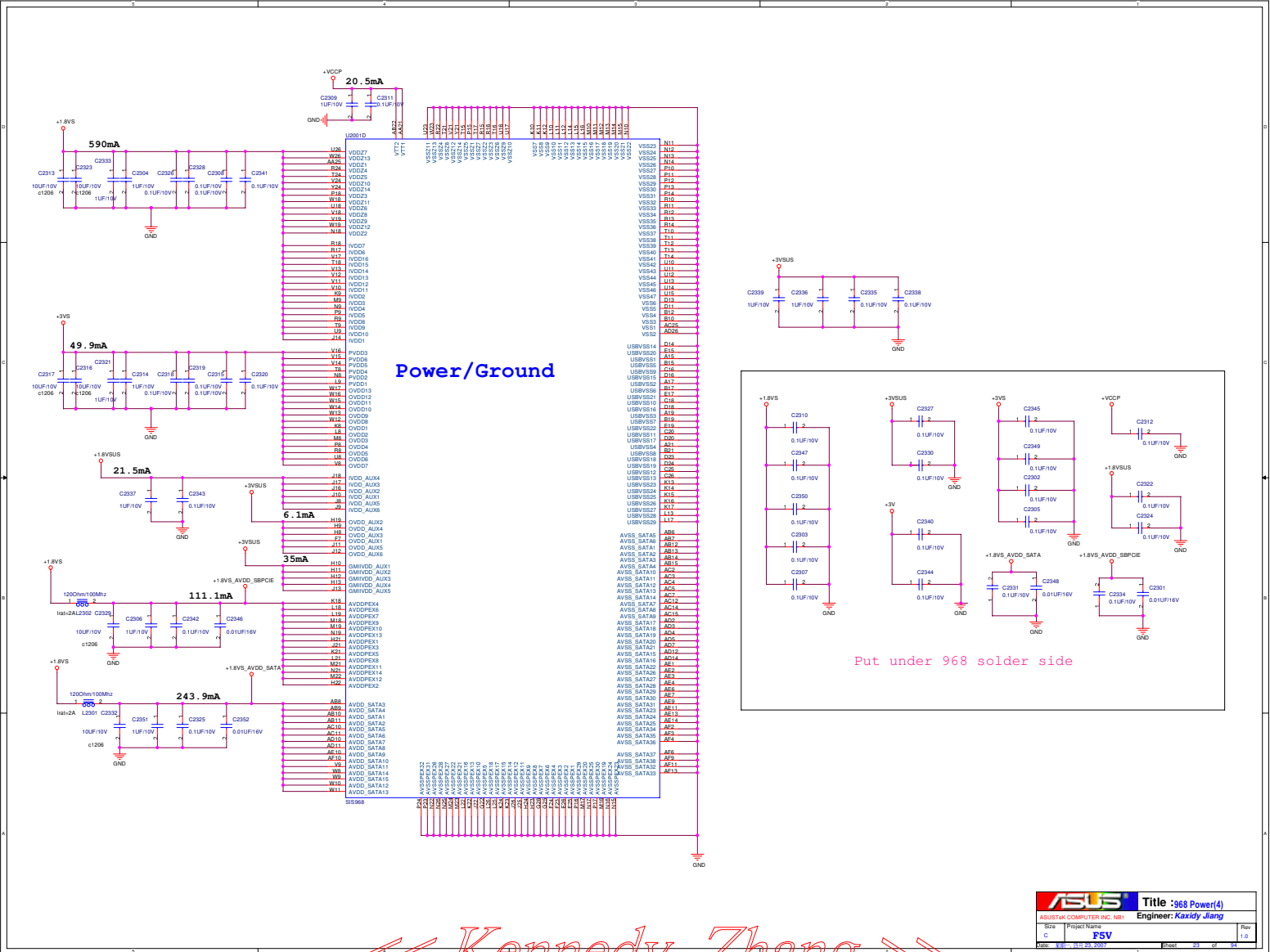




<< Kennedy_Zhang >>

PCBREV3		PCBREV2		PCBREV1		PCBREV0	
R1	0	1	0	1	0	1	0
R1.0	0	1	0	0	0	0	0
R2.0	1	0	0	0	0	0	0
R2.1	1	0	0	0	1	1	1

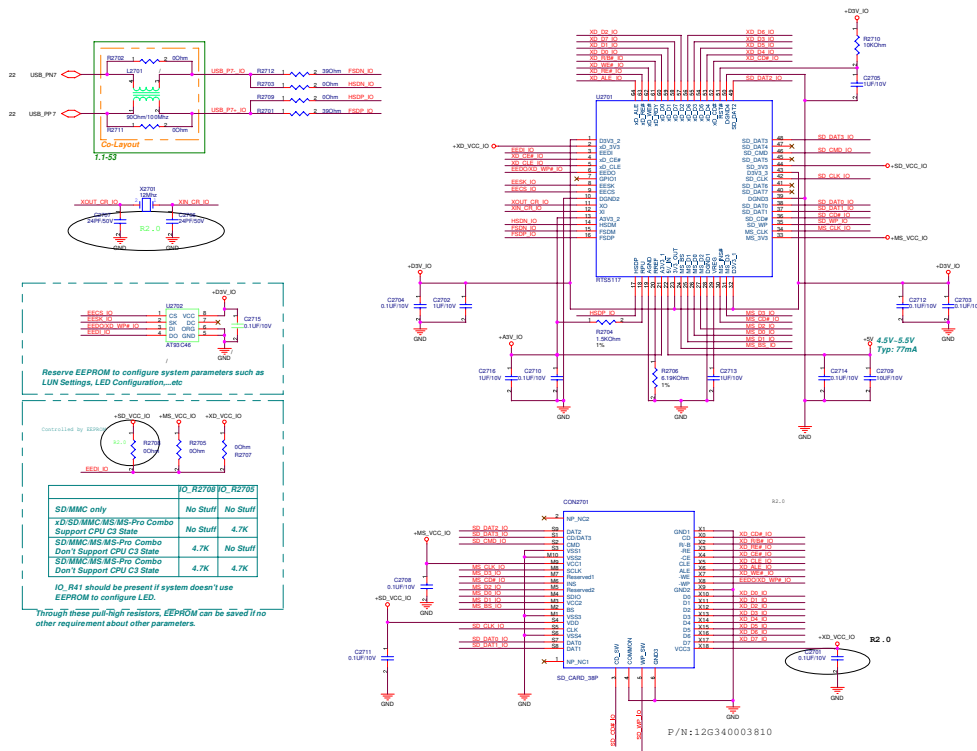
ASUS
Project Name: F5V
Engineer: Kazidy Jiang
Date: 2013.05.09
Page: 21 of 34



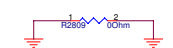
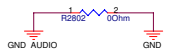
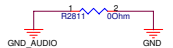
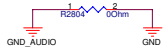
<< Kennedy_Zhang >>



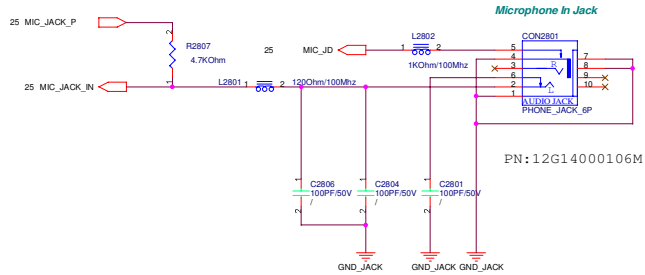
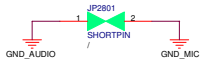




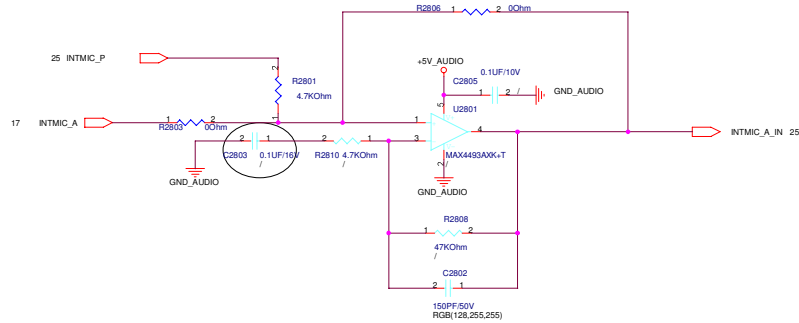
<< Kennedy_Zhang >>



INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils



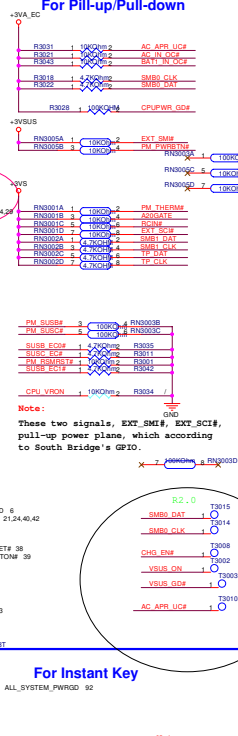
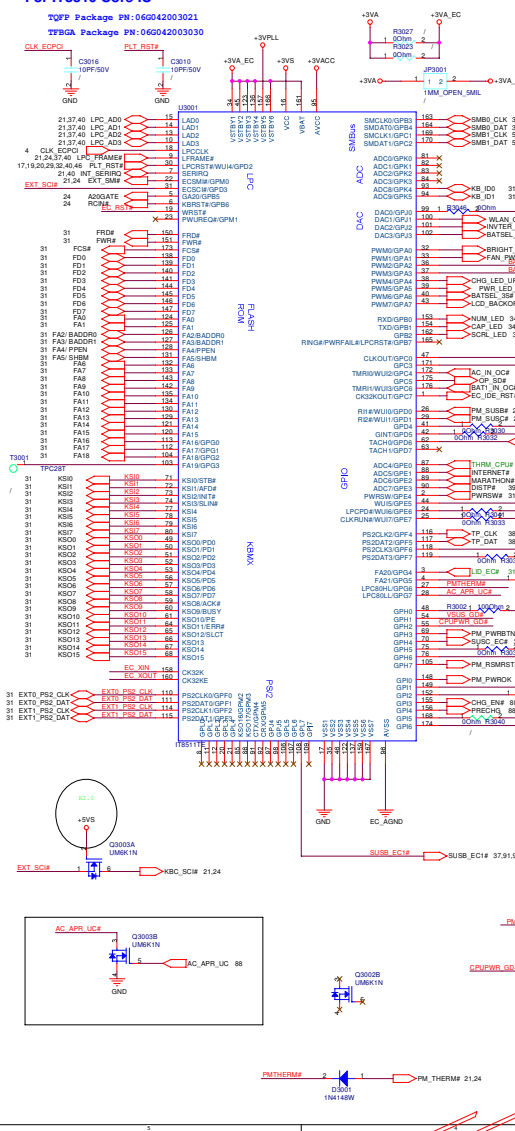
Pre-AMP For Test Function



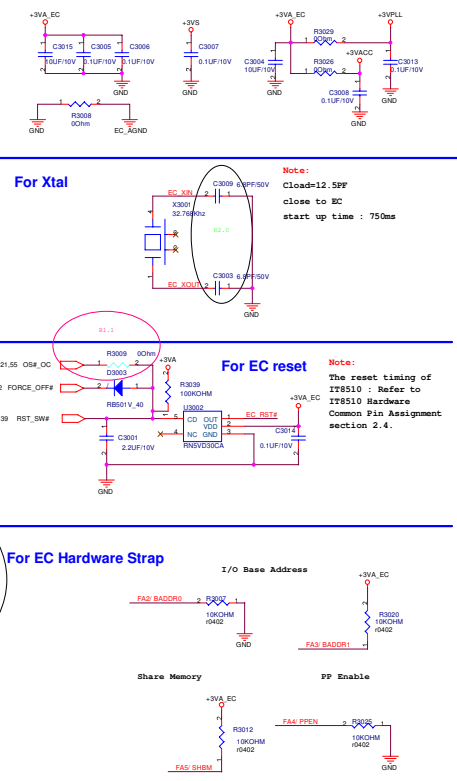
ASUS		Title : MIC.LINE-IN JACK	
Engineer: Kaxidy Jiang			
Size	Project Name	Rev	
Custom	F5V	1.0	
Date: 11/13/2007	Sheet 28 of 94		

<< Kennedy_Zhang >>

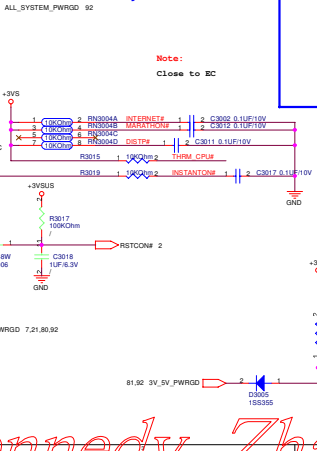
TQFP Package PN:06G042003021
TFBGA Package PN:06G042003030



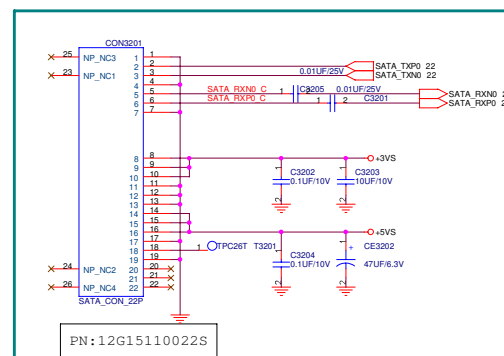
+3VA_EC



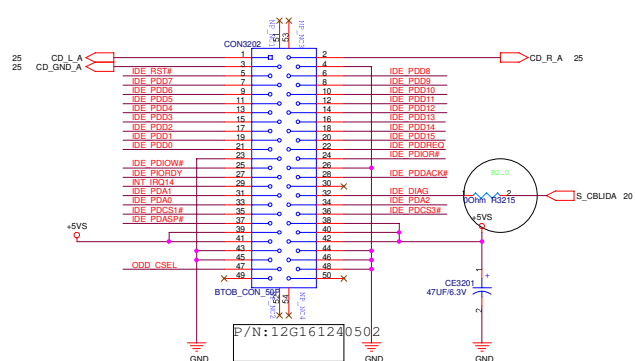
STEM_PWRGD 92



<< Kennedy_Zhang >>



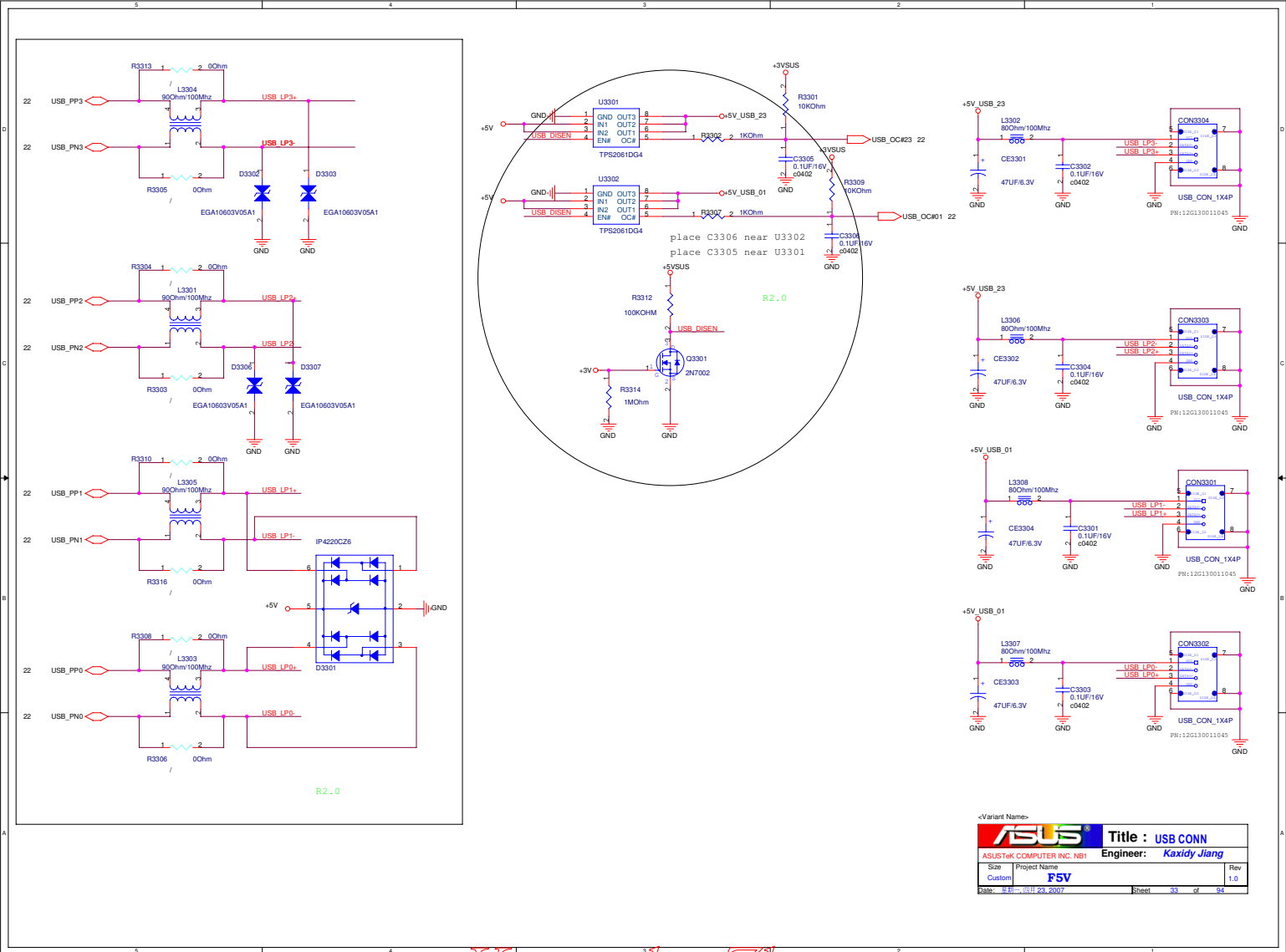
SATA



<Variant Name>

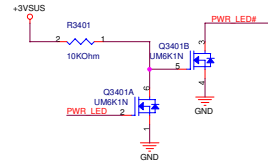
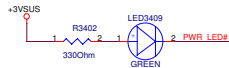
		Title : HDD & CD-ROM	
ASUSTEK COMPUTER INC		Engineer: <i>Kaxidy Jiang</i>	
Size Custom	Project Name F5V	Rev 1.0	
Date: 星期五, 四月 23, 2007		Sheet 32	of 94

<< Kennedy_Zhang >>

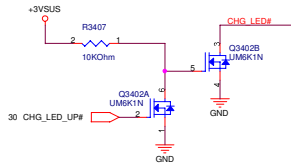
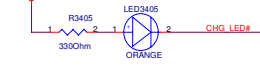


<< Kennedy_Zhang >>

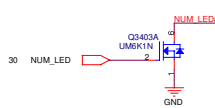
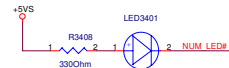
For POWER LED



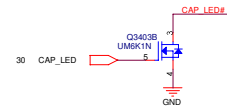
BATTERY LED



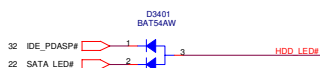
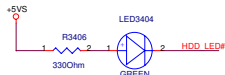
Num Lock



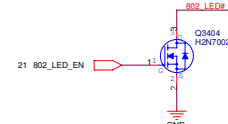
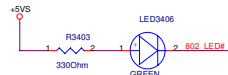
Cap Lock



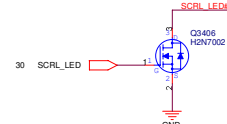
SATA/IDE LED



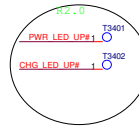
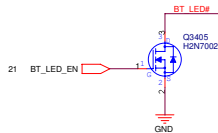
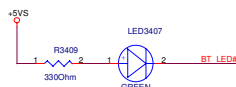
WireLess LED



Scroll Lock



BT LED



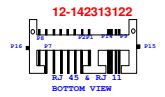
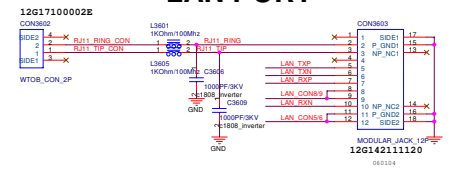
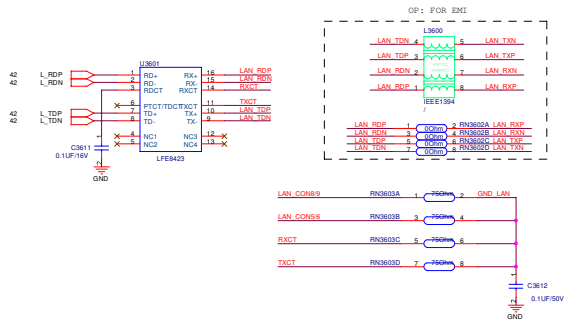
<Variant Name>		Title : LED	
ASUSTeK COMPUTER INC		Engineer: Kazidy Jiang	
Size	Project Name	Rev	
Custom	FSV	1.0	
Date: 2007-10-23	Sheet: 34	of 34	

<< Kennedy_Zhang >>

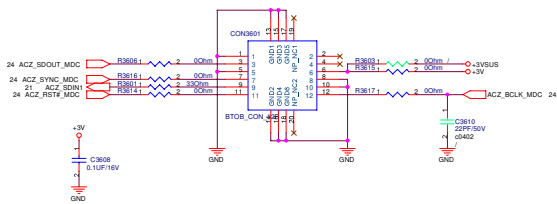
5		4		3		2		1	
D									
C									
B									
A									
									
					Title : BLANK				
					Engineer: Hawk Zhu				
Size		Project Name						Rev	
B		F5V						1.0	
Date: 11/11/2007					Sheet 35 of 94				

<< Kennedy_Zhang >>

LAN PORT

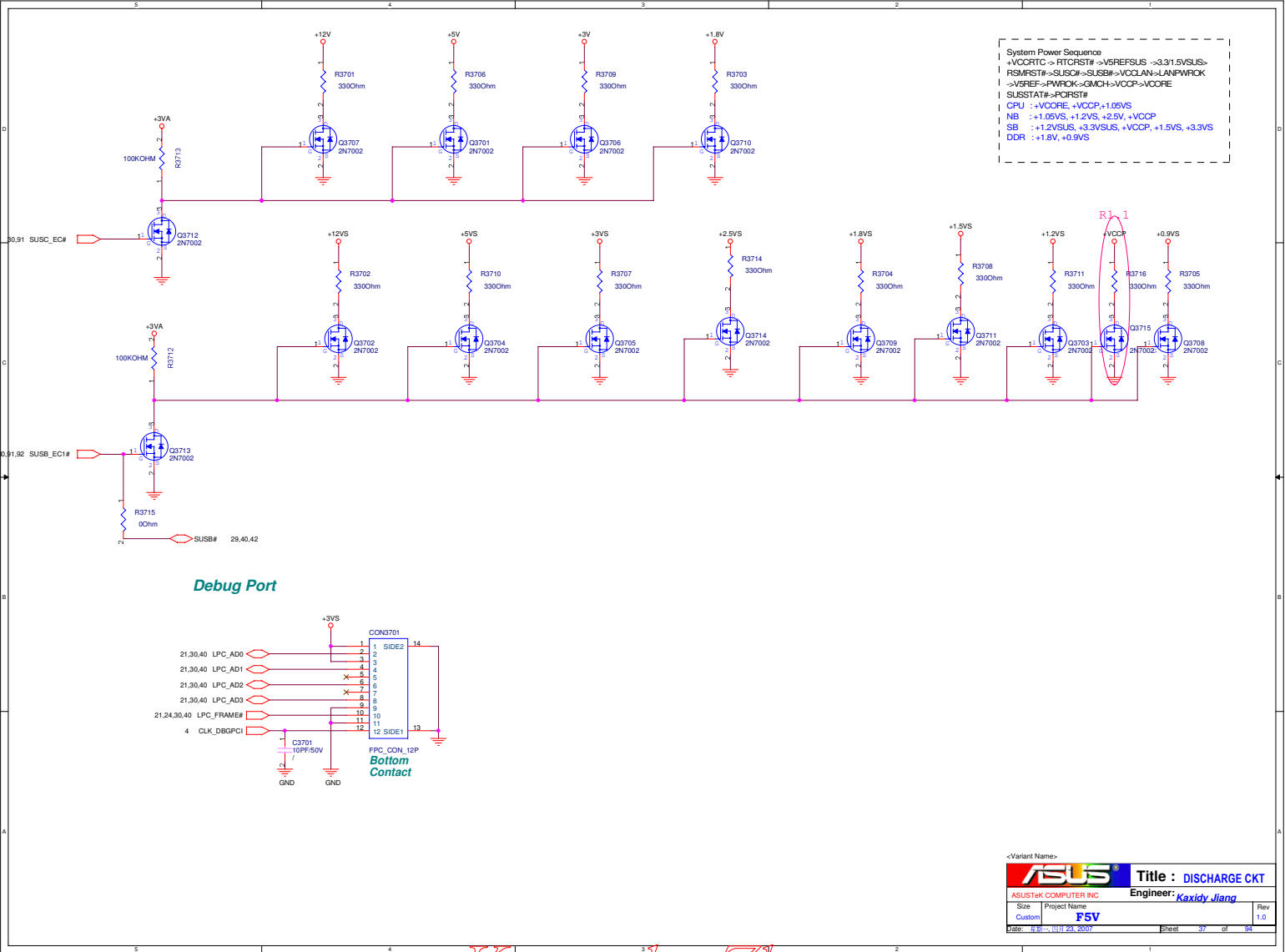


MDC



		Title : RJ11+45 & MDC	
ASUSTeK COMPUTER INC		Engineer: <i>Kaxidy Jiang</i>	
Size	Project Name		Rev
C	F5V		1.0
Date: 8/21/2007		Sheet	36 of 34

<< Kennedy_Zhang >>

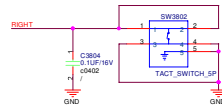
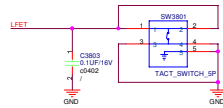
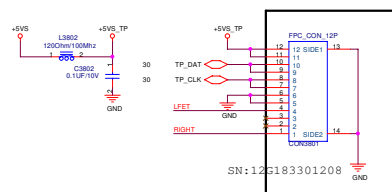


<< Kennedy_Zhang >>

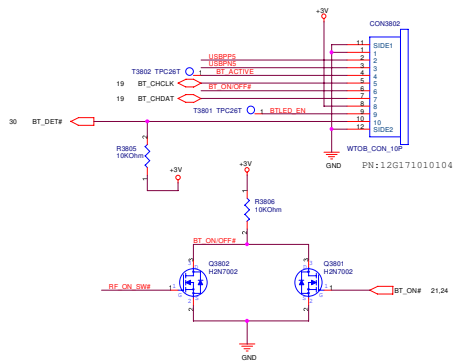
<Variant Name>		Title : DISCHARGE CKT	
ASUSTeK COMPUTER INC.		Engineer: Kaxidy Jiang	
Size	Project Name		Rev
Custom	F5V		1.0
Date: 2007-10-23	Sheet: 87	of 94	

Touch-Pad

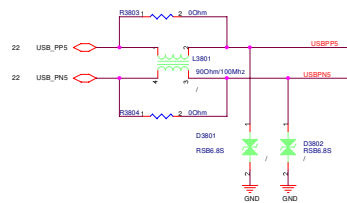
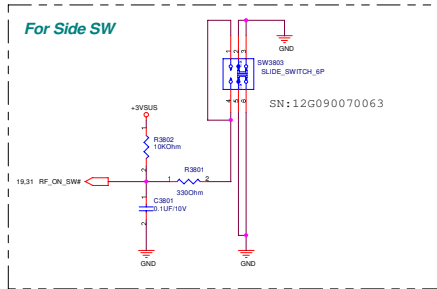
R1.1



For Bluetooth

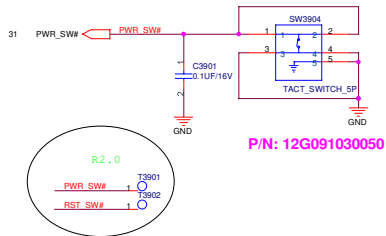


For Side SW

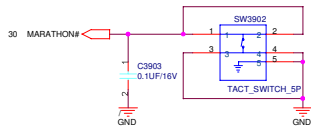


<< Kennedy_Zhang >>

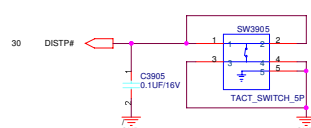
Power SW.



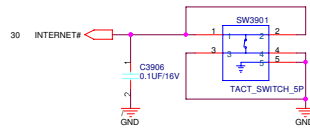
Marathon SW.



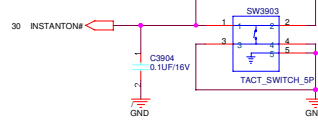
Disable Touch Pad SW.



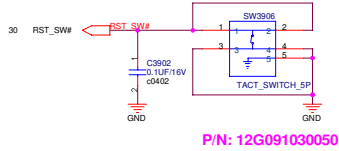
Internet SW.



InstantON SW.



RESET SW.

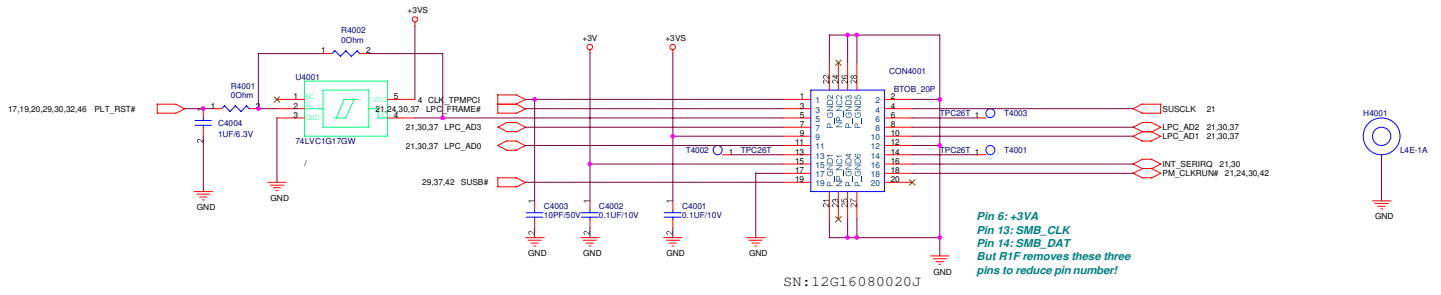



<Variant Name>

ASUS		Title : SWITCH	
ASUSTeK COMPUTER INC.		Engineer: Kaxidy Jiang	
Size	Project Name		Rev
Custom	F5V		1.0
Date: 2007-10-23		Sheet	of
		89	94

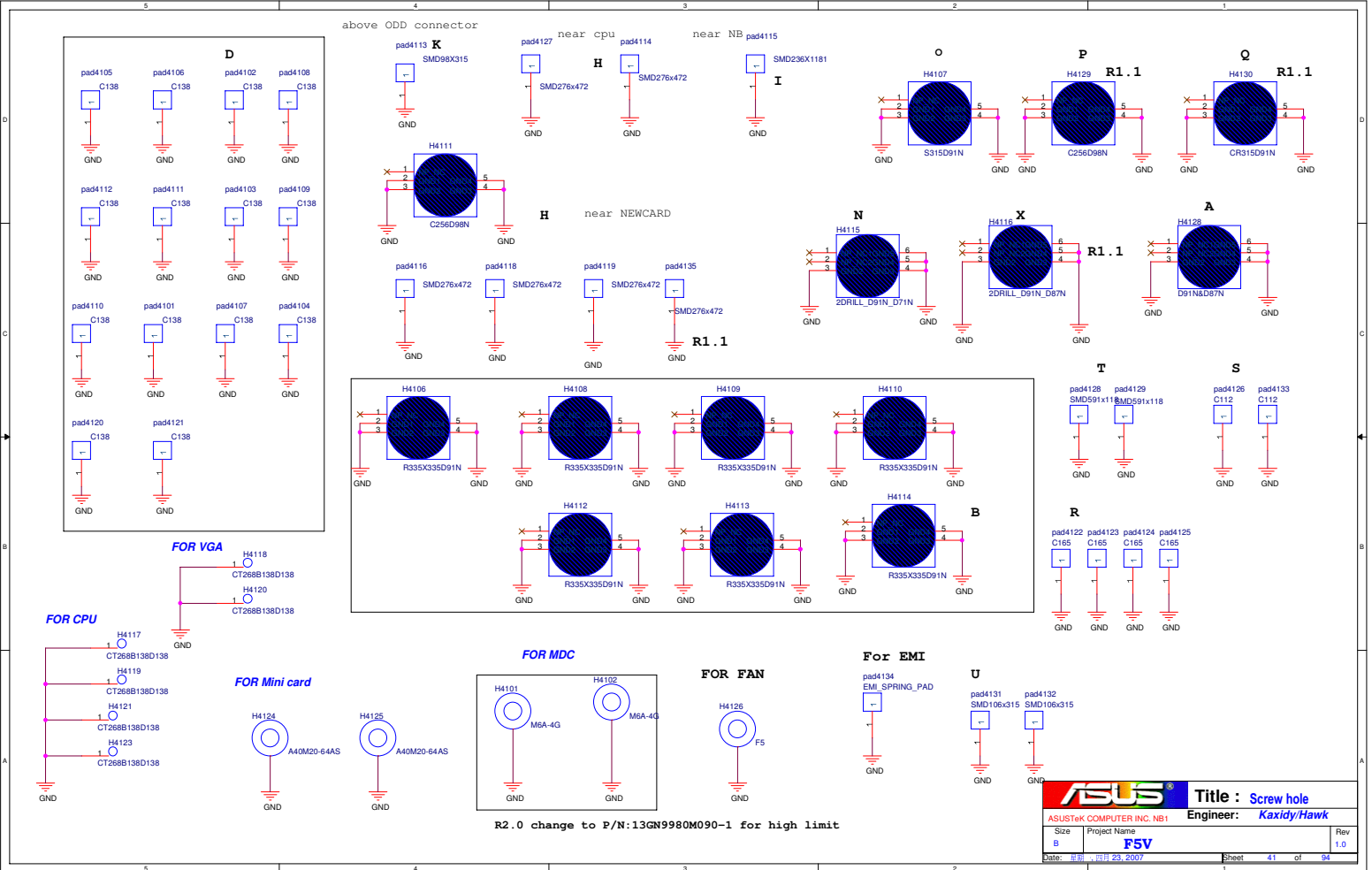
<< Kennedy_Zhang >>

For TPM Module

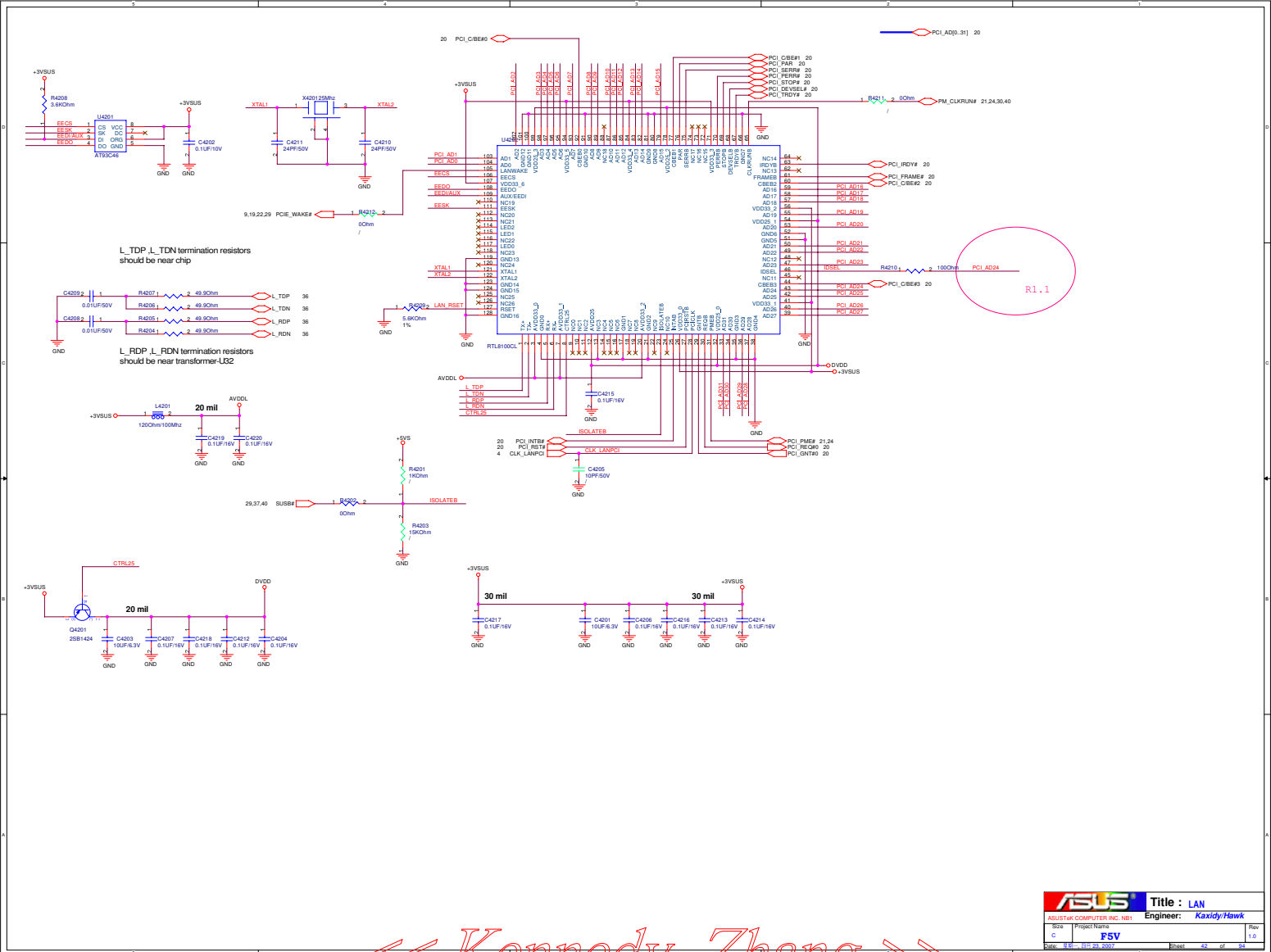


<Variant Name>			
		Title : TPM	
ASUSTeK COMPUTER INC. NB1		Engineer: Kaxidy Jiang	
Size	Project Name		Rev
Custom	F5V		1.0
Date: 4月23, 2007	Sheet 40 of 94		

<< Kennedy_Zhang >>




<< Kennedy_Zhang >>



<< Kennedy_Zhang >>

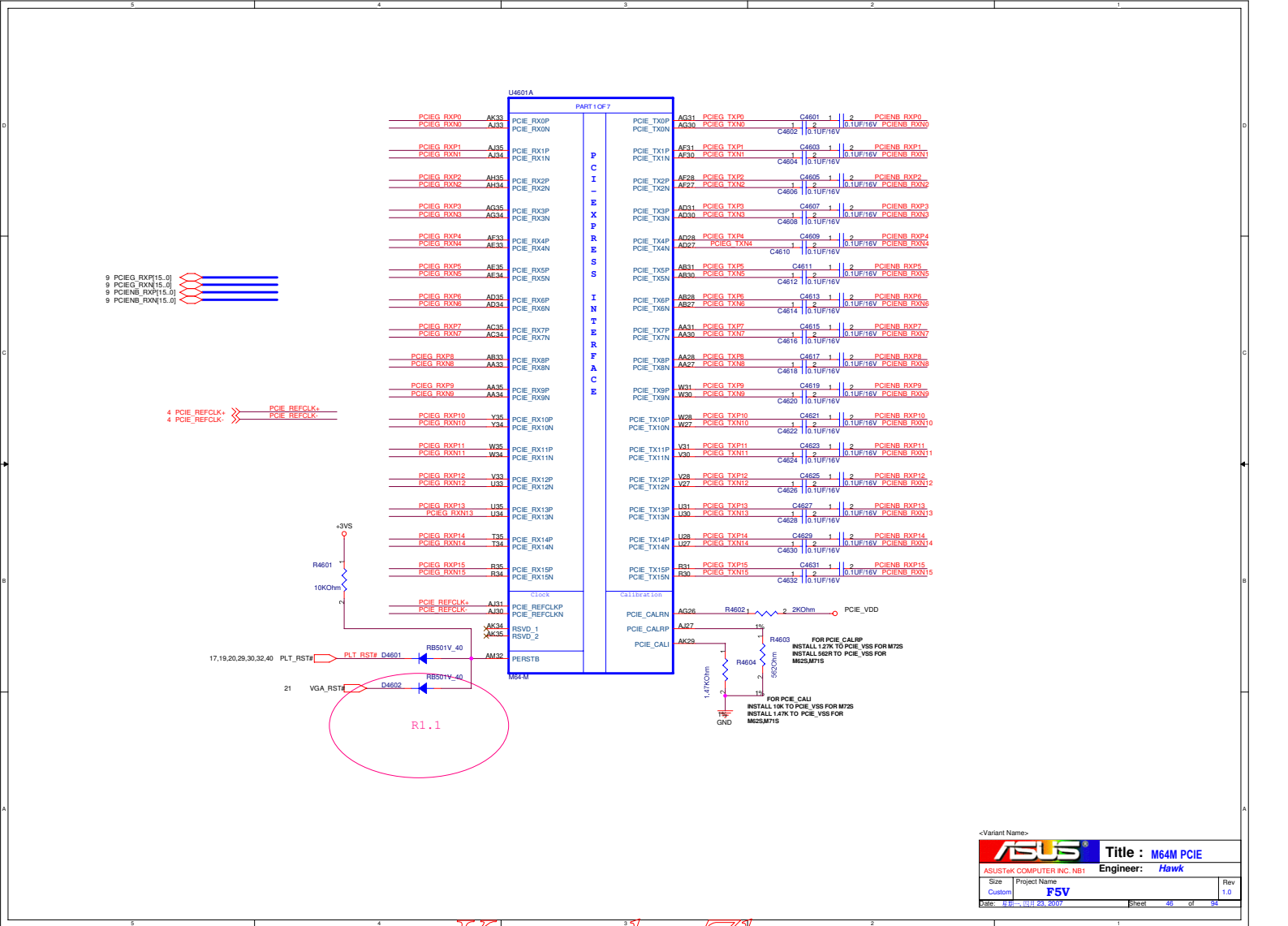
5		4		3		2		1	
D									
C									
B									
A									

5		4		3		2		1	
D									
C									
B									
A									
5		4		3		2		1	

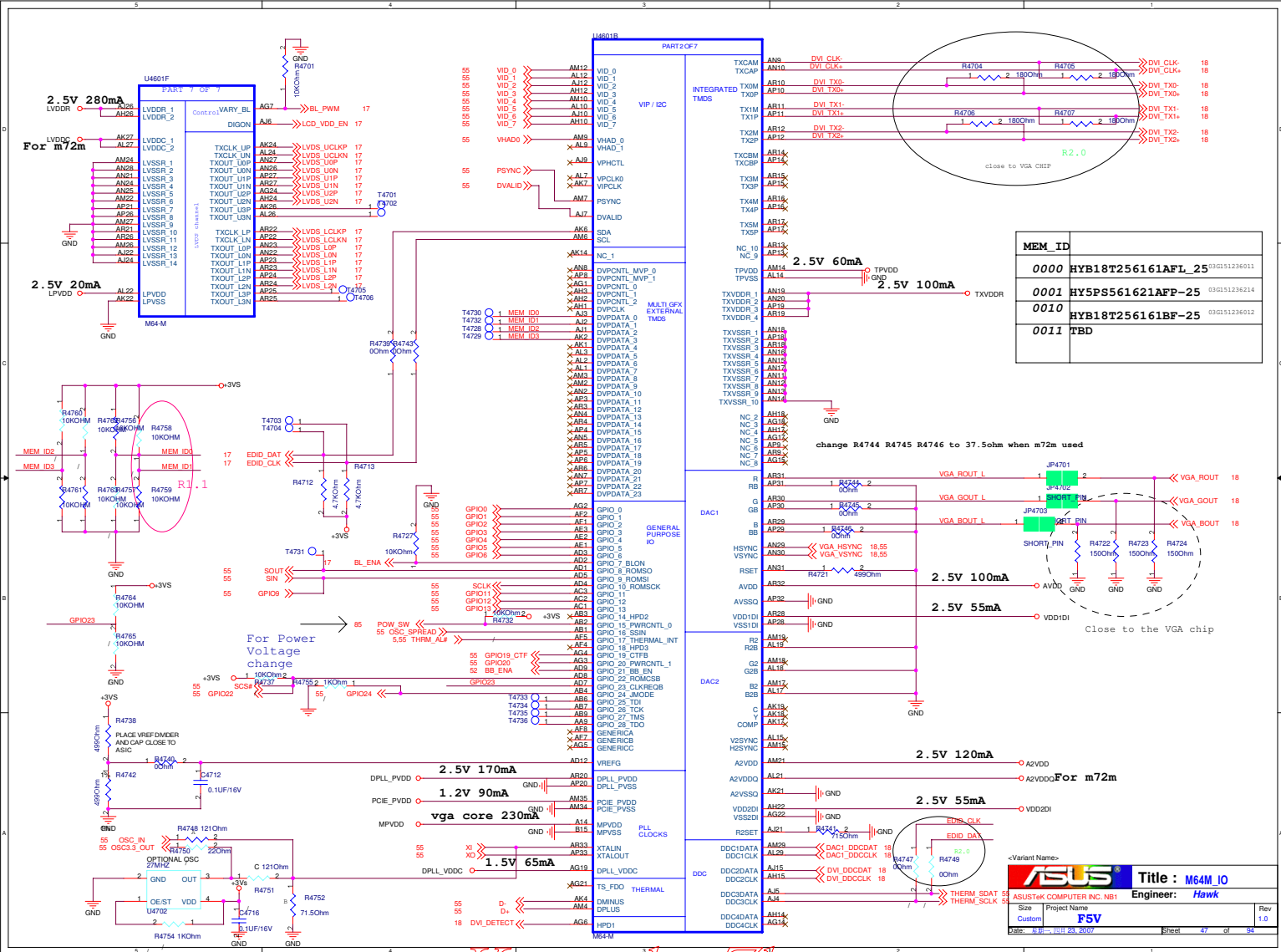
		Title : BLANK	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>	
Size A	Project Name F5V		Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 44 of 94	

<< Kennedy_Zhang >>

5		4		3		2		1	
D									
C									
B									
A									



<< Kennedy_Zhang >>



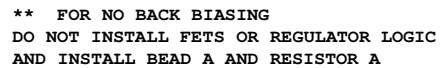
<< Kennedy_Zhang >>

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>	
Size	Project Name		Rev
A	F5V		1.0
Date: 星期一, 四月 23, 2007		Sheet	50 of 94

<< Kennedy_Zhang >>

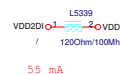
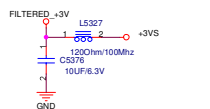
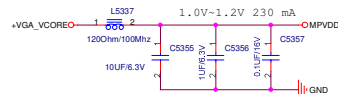
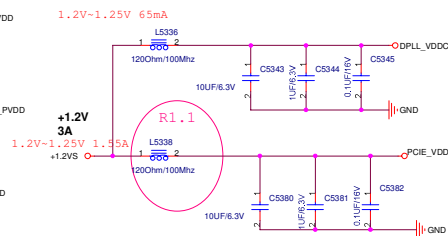
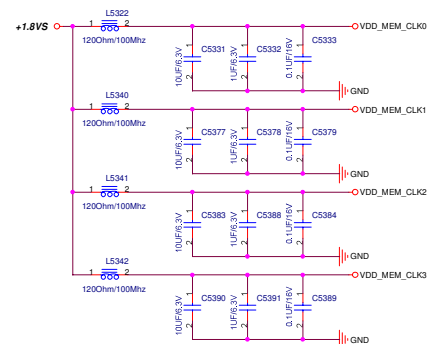
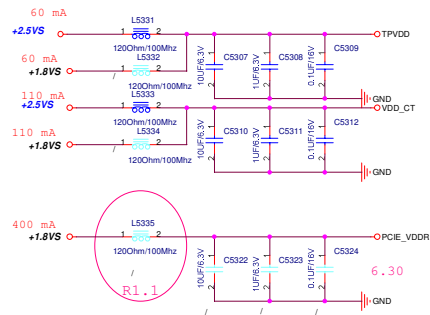
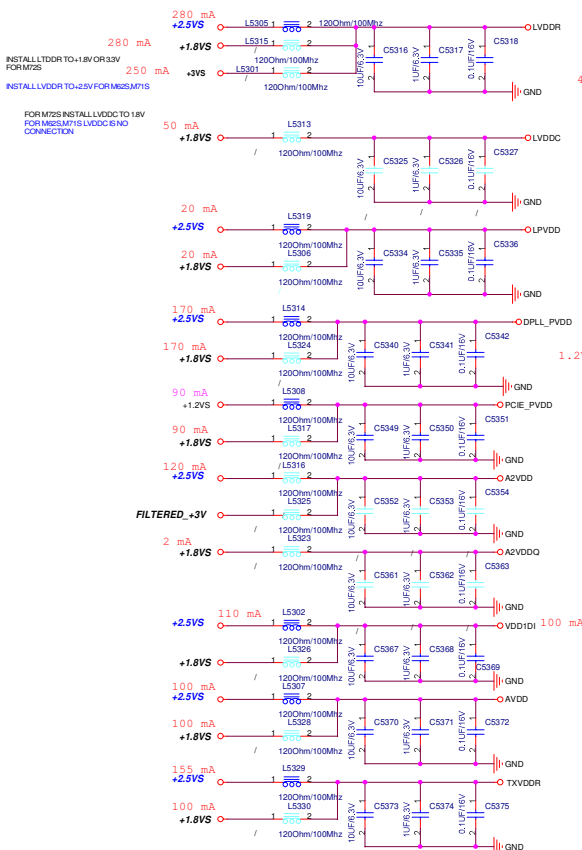

```
-BBN = -.5V
N FET A = ON, P FET B = ON, N FET C = OFF
+BBP = +1.5V
```



COMPONENTS SHOWN ARE EXAMPLES ONLY AND NOT NECESSARILY QUALIFIED

LTPVSS18 DVSSDI TPVSS MPVSS
* PCIE_PVSS PVSS A2VSSQ AVSSQ

PLACE CAPS FOR THESE GROUNDS CLOSE TO ASIC AND RUN DEDICATED TRACES FROM PINS TO JOIN THE GROUND PLANE WITH ONE VIA AT CAP

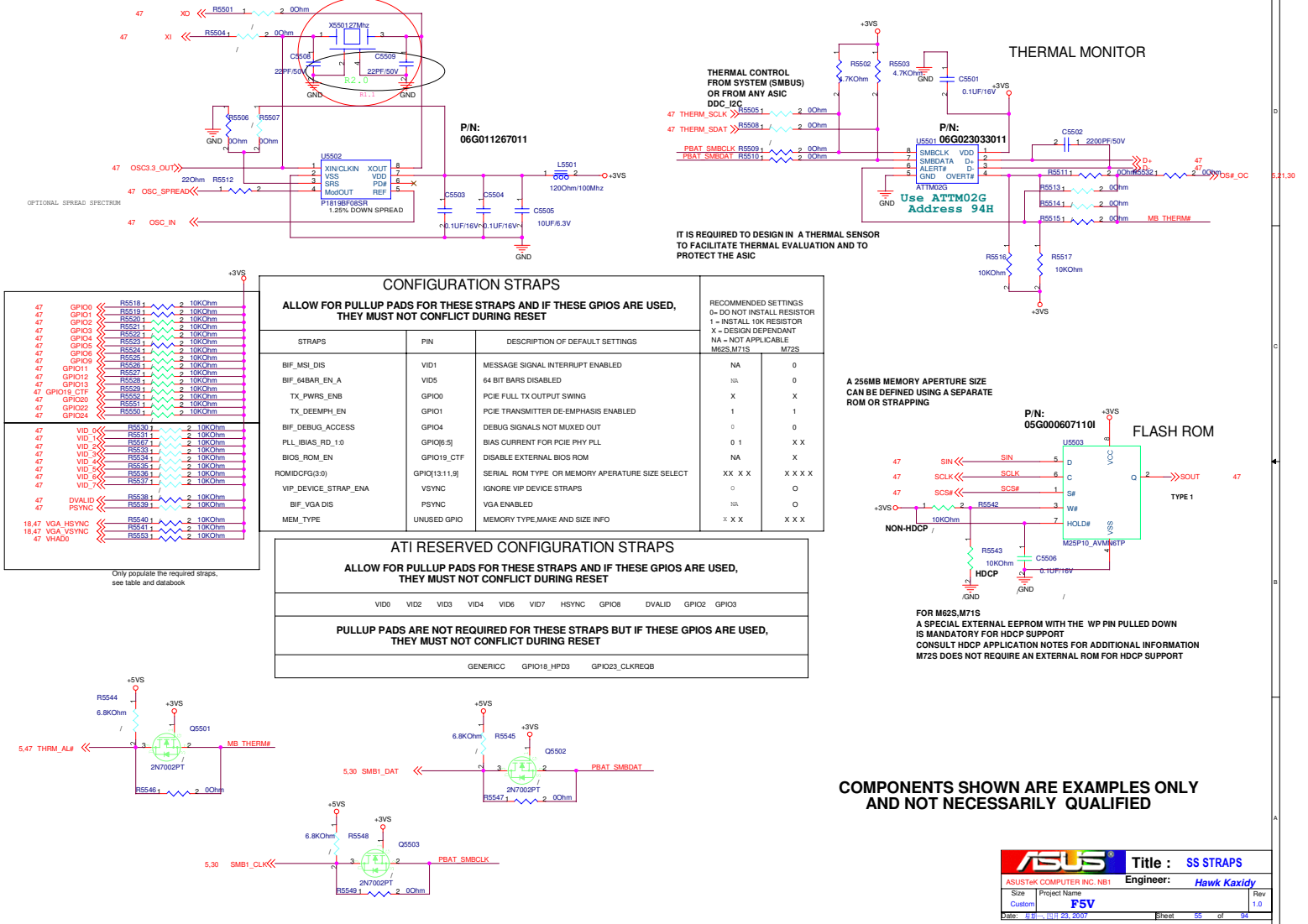


ASUS		Title : IO capacitor	
ASUSTek COMPUTER INC. NB1		Engineer: Hawk	
Size	Project Name	Rev	
Custom	FSV	1.0	
Date: 11/23/2007	Sheet 53 of 94		

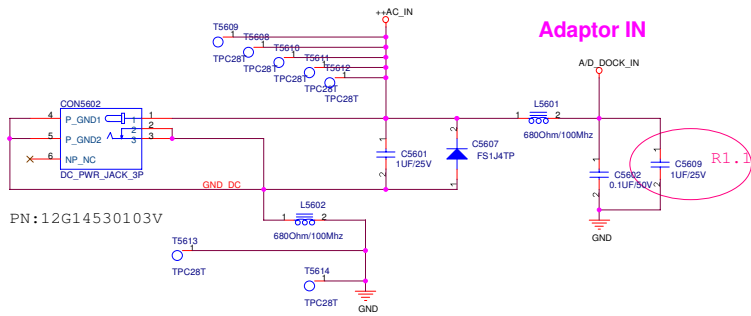
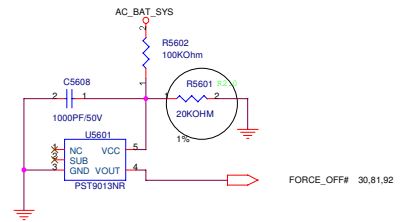
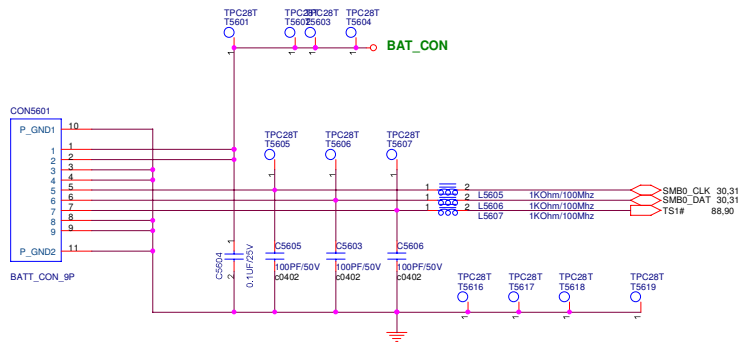
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<Variant Name>			
		Title : VRAM2	
ASUSTeK COMPUTER INC. NB1		Engineer: Hawk	
Size	Project Name		Rev
C	F5V		1.0
Date: 10/26/2007		Sheet 54	of 94

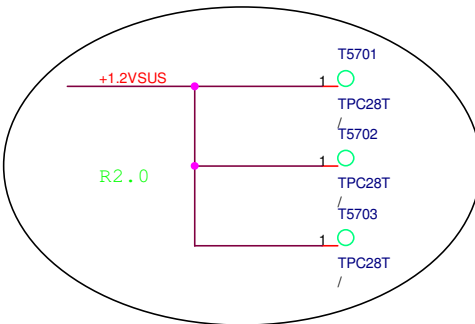


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ASUS		Title : AC/BAT JACK	
ASUSTek COMPUTER INC. NB1		Engineer: Hawk	
Size	Project Name	Rev	
B	F5V	1.0	
Date: 11/11/23/2007	Sheet 56 of 94		

<< Kennedy_Zhang >>



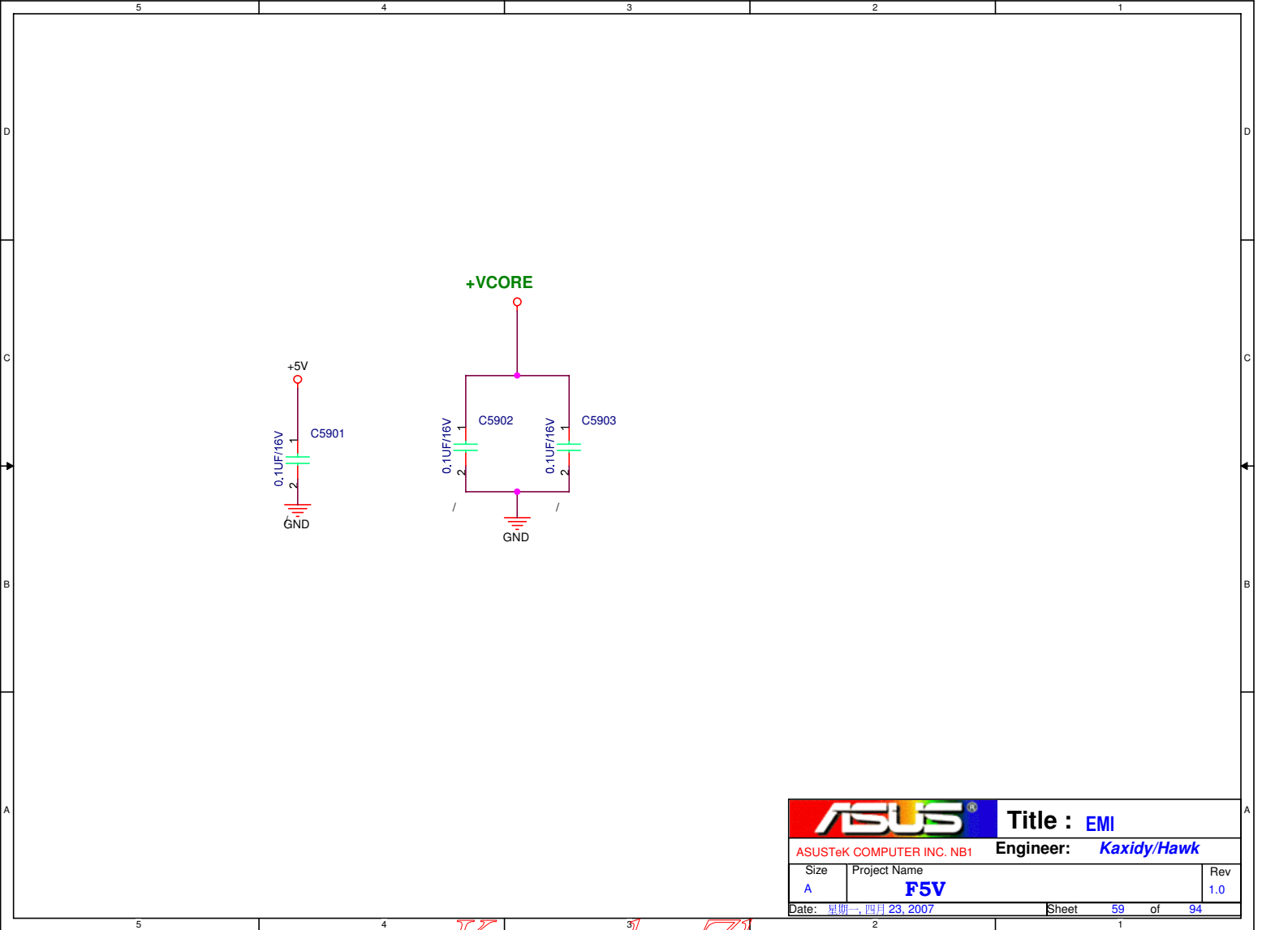
Engineer: *Kaxidy/Hawk*

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		Title : BLANK	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>	
Size A	Project Name F5V		Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 58 of 94	

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<< Kennedy_Zhang >>

1. P2 unmount R201 for H_CPURST#, add T205/T206 for CLK_CPU_BCLK#/CLK_CPU_BCLK test.
2. P6 mount R605 for H_PWRGD timing, add T603/T604/T605/T606 to HA[32:35]#.
3. P7 unmount R706
4. P20 mount R2001/R2002/R2003/R2009/R2011 for PCI_REQ#[0:4]
5. P21 change R2121 to 00hm
add R2124(330hm) for AC2_RST# according to 968 ACT.
add R2108/R2112(00hm) for PCIEPRSNTO/1 according to sis ACT.
ADD GMAC OSC25MHZ to GND according to sis ACT.
unmount L2103,mount L2105 according to spec.
unmount R2122 for repeat with R2453, change R2120/R2125 PU to +3VSUS according to spec.
change GPIO17 from VIN4 to S_A20GATE, add R2127(00hm) for reserve SUSCLK
- 6.P17 add R1708 and R1709 to change BL_PWM to BL_ENA to fix garbage
7. P22 change R2217 to 12KOhm, add C2237(22pF) for SATA REXT according to 968 ACT.
8. P24 add R2434 for A20GATE to H_A20M#,add R2457 for A20GATE to S_A20GATE,add R2456 to PU S_A20GATE
9. P29 add R2909/R2910(00hm), unmount L2901 for EMI.
10. P30 change D3002 to R3009 for OS#_OC to avoid no EC reset, .
delete D3004 for DDR power are not SUS power,
add R3045 for VSUS_GD# PU, change GPJ0 to VIN4 to control NEW card shutdown, add R3046 for VIN4,
Add R3019 for INSTANTON#
11. P33/P5/P32 change the P/N of CE3202/CE501/CE3301/CE3302/CE3303/CE3304 for low cost
12. P37 mount R3716/Q3715 for +VCCP discharge
13. P42 change IDSEL to PCI_AD24
- 14.P46 add D4602 for VGA_RST#
15. P48 unmount L4803/R4809, delete L4801
unmount R4806,mountQ4801/R4807/Q4802/R4808
16. P53 change L5335/L5338 to match the current.
- 17.P55 change X5501 to +-10ppm to follow spec,add C5508/C5509 to match X5501
18. P56 add C5609 for over current damaging charge IC.
19. P4 Change C440 from 0.1UF to 0.22UF
20. P10 change L1001 to 2A to match the current,, Add +1.2VS delay circuit.
- 21.P21 Add VGA_RST# to GPIO7, add R2140 for VGA_RST#.
- 22.P47 Unmount R4759,mount R4758 for Vram changed from 03G151236011 to 03G151236012.

- R2.0
- 1.R29 mount R2907, connect PCIE_PRSNT1 to CPPE#
- R21 unmount R2109, mount R2119, change R2118 from 00hm to 4.7KOhm but unmount R2118
- 2.P27 change R2708 to 00hm and mount it to not support C3 mode
- 3.P33&22 add two TFS2061 (U3301/U3302) to avoid not start up caused by USB device with external power supply
- 4.P21 add R2141 to connect OS#_OC to PM_THERMTRIP#, change R2141 to Q2101
- 5.P30 change C3009/C3003 to 6.8pF
- 6.P27 change C2706/C2707 to 24pF
- 7.P55 change C5508/C5509 to 22pF
- 8.P33 unmount R3313/R3305/R3304/R3303/R3310/R3316/R3308/R3306, mount L3304/L3301/L3305/L3303, mount D3302/D3303/D3306/D3307/D3301
- 9.P47 add R4747/R4749 to reserve EDID_DAT/EDID_CLK to DDC3
- 10.P30 change Q3003 PU from +5V to +5VS
- 11.P5 unmount R506
- 12.P56 change R5601 to 20KOhm
- 13.P20 unmount R2054,add and mount C2010
- P32 add R3215 to connect S_CBLIDA to IDE_DIAG, unmount C3206
- P22 add and unmount C2215/C2238/C2239/C2236, add and mount C2206
- 14.P27 change 4in1 cardreader
- 15.P47 mount R4704/R4705/R4706/R4707
- P18 change DVI bead to R1832/R1833/R1834/R1835/R1836/R1837/R1838/R1839,change R1832/R1833/R1834/R1835/R1836/R1837/R1838/R1839 reference to L1806/L1807/L1808/L1809/L1810/L1811/L1812/L1813
- 16.P21 Unmount L2105, mount L2103
- 17.P21 change R2116 from 330hm to 200hm, change R2117 from 330hm to 00hm, change R2119 from 330hm to 200hm
- P24 change R2418 from 330hm to 00hm, change R2420 from 330hm to 00hm, change R2419 from 330hm to 00hm, change R2422 from 330hm to 00hm, change R2423 from 330hm to 00hm, change R2425 from 330hm to 00hm
- P25 change R2514 from 330hm to 470hm

- F5VL
1. P2/3 change CPU socket to P
2. P32 delete R3205/R3212
3. P59 add C5902/C5903 for EMI

			Title : BLANK	
ASUSTek COMPUTER INC. NBI			Engineer: KazidyHawk	
Size	Project Name		Rev	
C	FSV		1.0	
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		Title : BLANK	
ASUSTeK COMPUTER INC. NB1		Engineer: Kaxidy/Hawk	
Size	Project Name		Rev
A	F5V		1.0
Date: 星期一, 四月 23, 2007		Sheet	63 of 94

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ASUSTeK COMPUTER INC. NB1		Engineer: Kaxidy/Hawk	
Size	Project Name		Rev
A	F5V		1.0
Date: 星期一, 四月 23, 2007		Sheet	65 of 94

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		Title : BLANK	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>	
Size A	Project Name F5V		Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 66 of 94	

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		Title : BLANK	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>	
Size A	Project Name F5V		Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 67 of 94	

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	5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC. NB1		Engineer: Kaxidy/Hawk	
Size	Project Name		Rev
A	F5V		1.0
Date: 星期一, 四月 23, 2007		Sheet	69 of 94

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5		4		3		2		1	
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5		4		3		2		1	

		Title : BLANK	
ASUSTeK COMPUTER INC. NB1		Engineer: Kaxidy/Hawk	
Size	Project Name		Rev
A	F5V		1.0
Date: 星期一, 四月 23, 2007		Sheet	70 of 94

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		Title : BLANK	
ASUSTeK COMPUTER INC. NB1		Engineer: Kaxidy/Hawk	
Size	Project Name		Rev
A	F5V		1.0
Date: 星期一, 四月 23, 2007		Sheet	72 of 94

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	5	4	3	2	1
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	5	4	3	2	1


		Title : BLANK	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>	
Size	Project Name		Rev
A	F5V		1.0
Date: 星期一, 四月 23, 2007		Sheet	73 of 94

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5		4		3		2		1	
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5		4		3		2		1	
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	5	4	3	2	1
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	5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC. NB1		Engineer: Kaxidy/Hawk	
Size	Project Name		Rev
A	F5V		1.0
Date: 星期一, 四月 23, 2007		Sheet	76 of 94

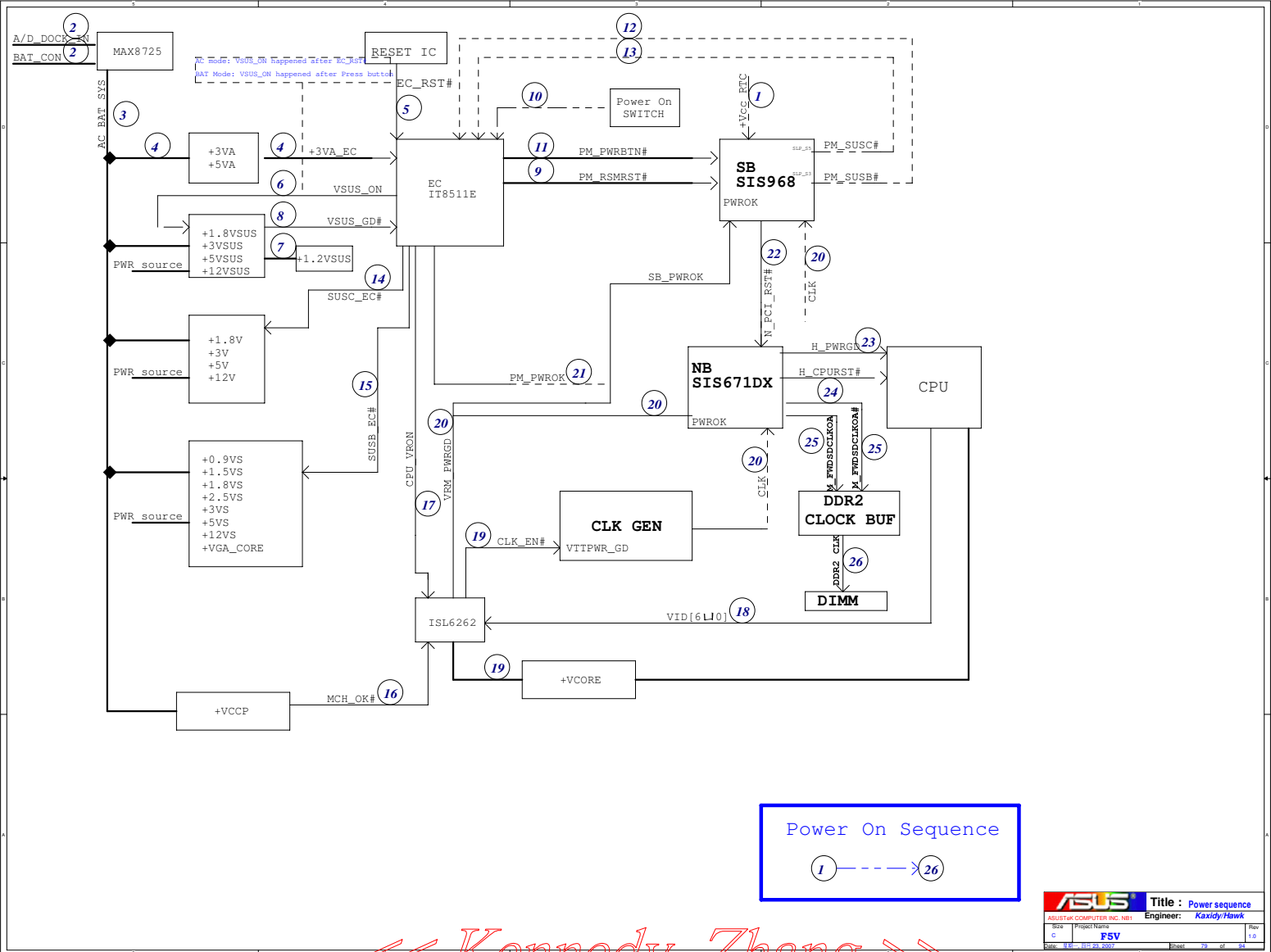
<< Kennedy_Zhang >>

5		4		3		2		1	
D									
C									
B									
A									

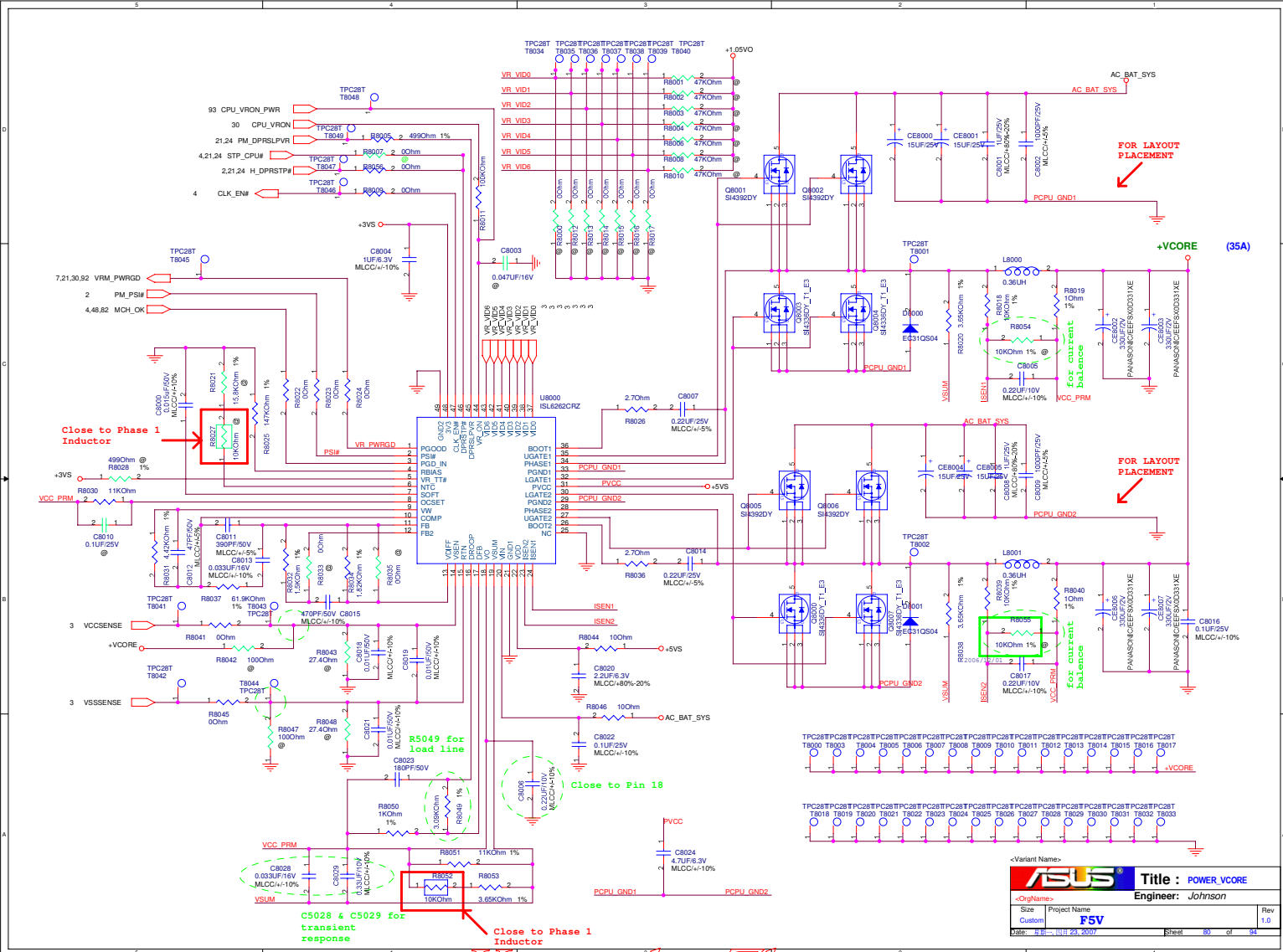
5		4		3		2		1	
D									
C									
B									
A									
5		4		3		2		1	

		Title : BLANK	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>	
Size	Project Name		Rev
A	F5V		1.0
Date: 星期一, 四月 23, 2007		Sheet 78 of 94	

<< Kennedy_Zhang >>

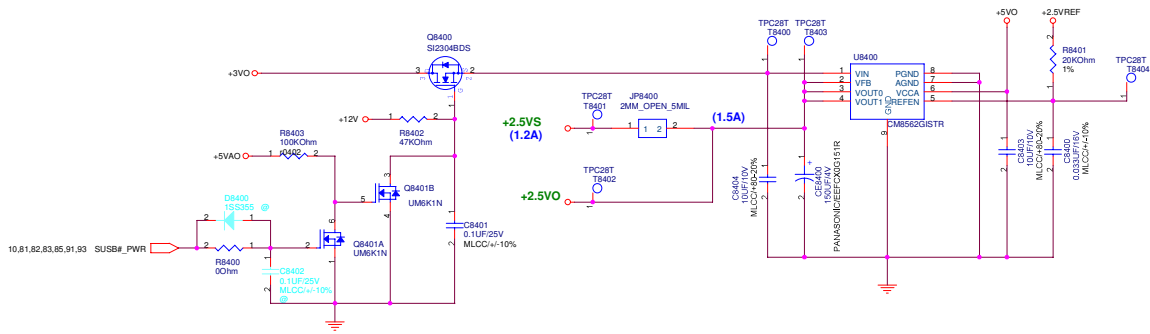


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+2.5V



<Variant Name>




Title :POWER_I/O_+3VA & +2.5V

Engineer: *Johnson*

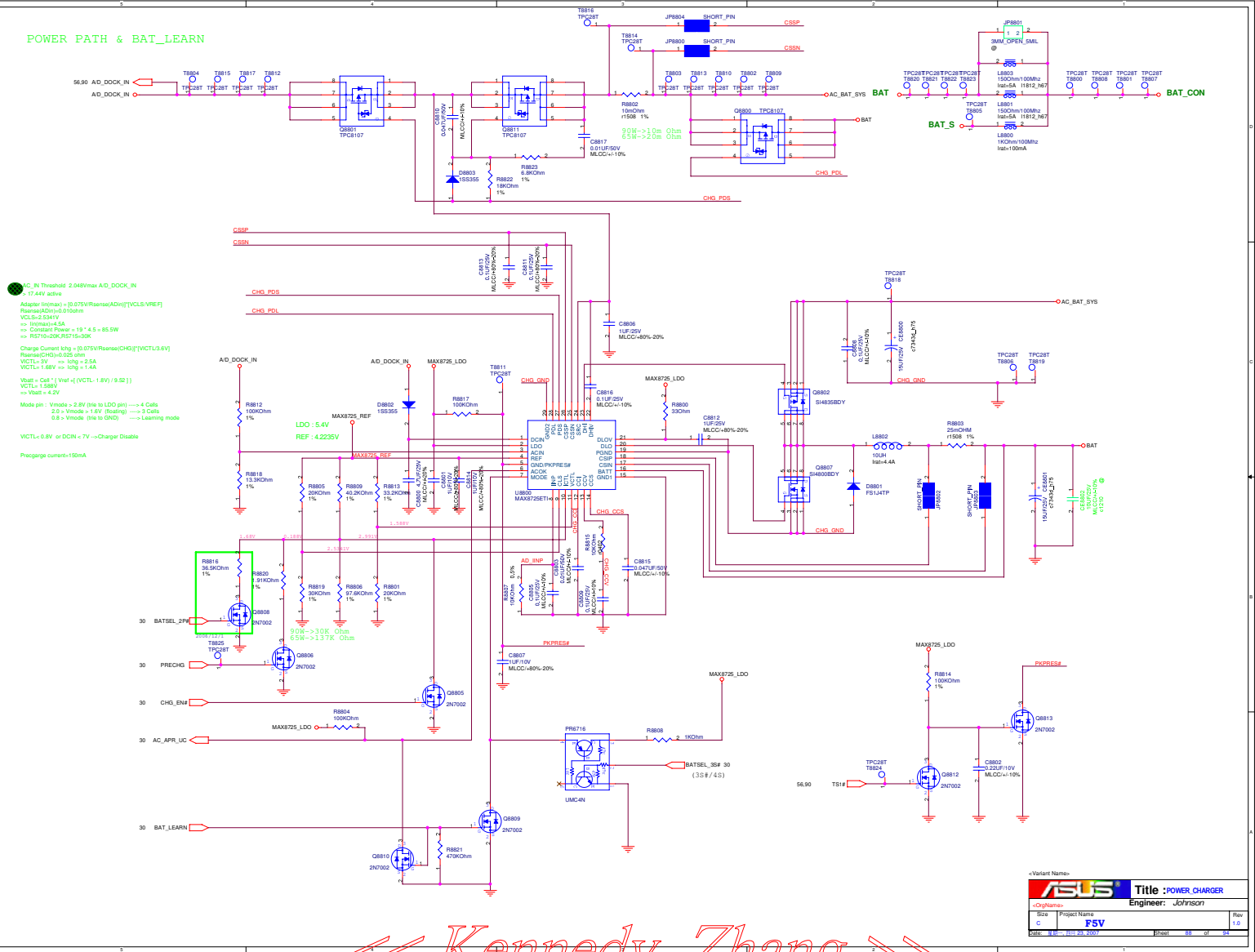
Size Custom	Project Name F5V	Rev 1.0
Date: 5月11日 23, 2007	Sheet 84 of 94	

<< Kennedy_Zhang >>

<Variant Name>		A	
		Title : N/A	
<OrgName>		Engineer: <i>Johnson</i>	
Size B	Project Name F5V	Rev 1.0	
Date: 星期四, 四月 23, 2007		Sheet 86 of 94	

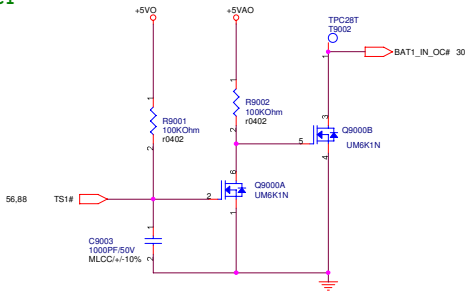
<< Kennedy_Zhang >>

POWER PATH & BAT_LEARN

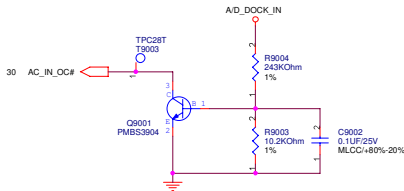


<< Kennedy_Zhang >>

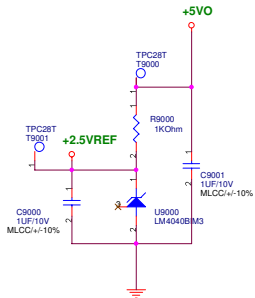
BATTERY IN DETECT



ADAPTER IN DETECT



+2.5VREF



<Variant Name>			
ASUS		Title :POWER_DETECT	
<OrgName>		Engineer: Johnson	
Size	Project Name	Rev	
Custom	F5V	1.0	
Date: 2007-10-23		Sheet	90 of 94

<< Kennedy_Zhang >>

SUSC#_STAGE POWER

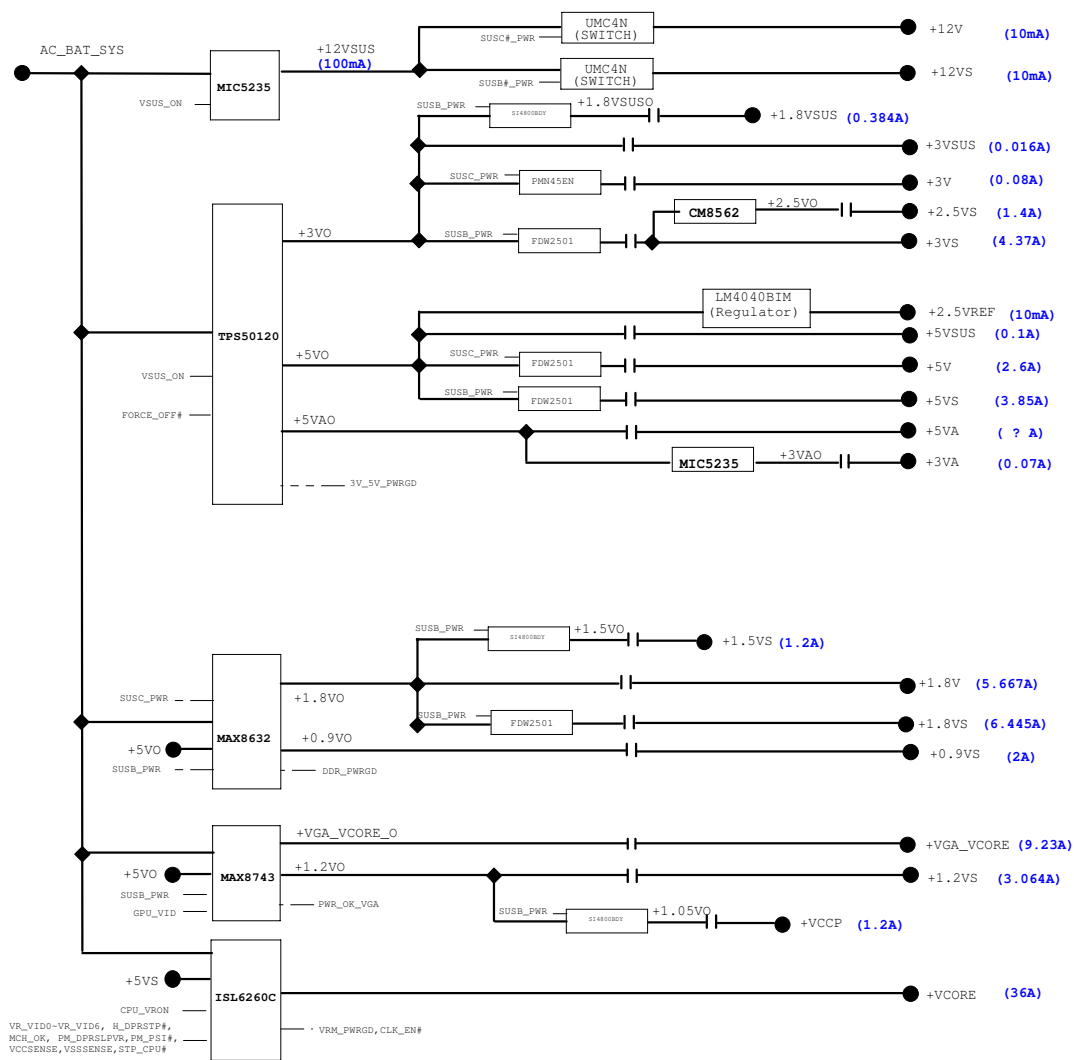
SUSB#_PWR POWER

ASUS Title : POWER_LOAD_SWITCH
Engineer: Johnson
Size Project Name
Custom FSV
Date: 2007.03.23 Sheet 91 of 94

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ASUS		Title :POWER_FLOWCHART	
Engineer: Johnson			
Rev	Project Name	Rev	
Custom	FSV	1.0	
Date: 2007-10-25	Sheet	15	of 15