

Compal Confidential

VAWGA/B Schematics Document

AMD "Kabini" Platform

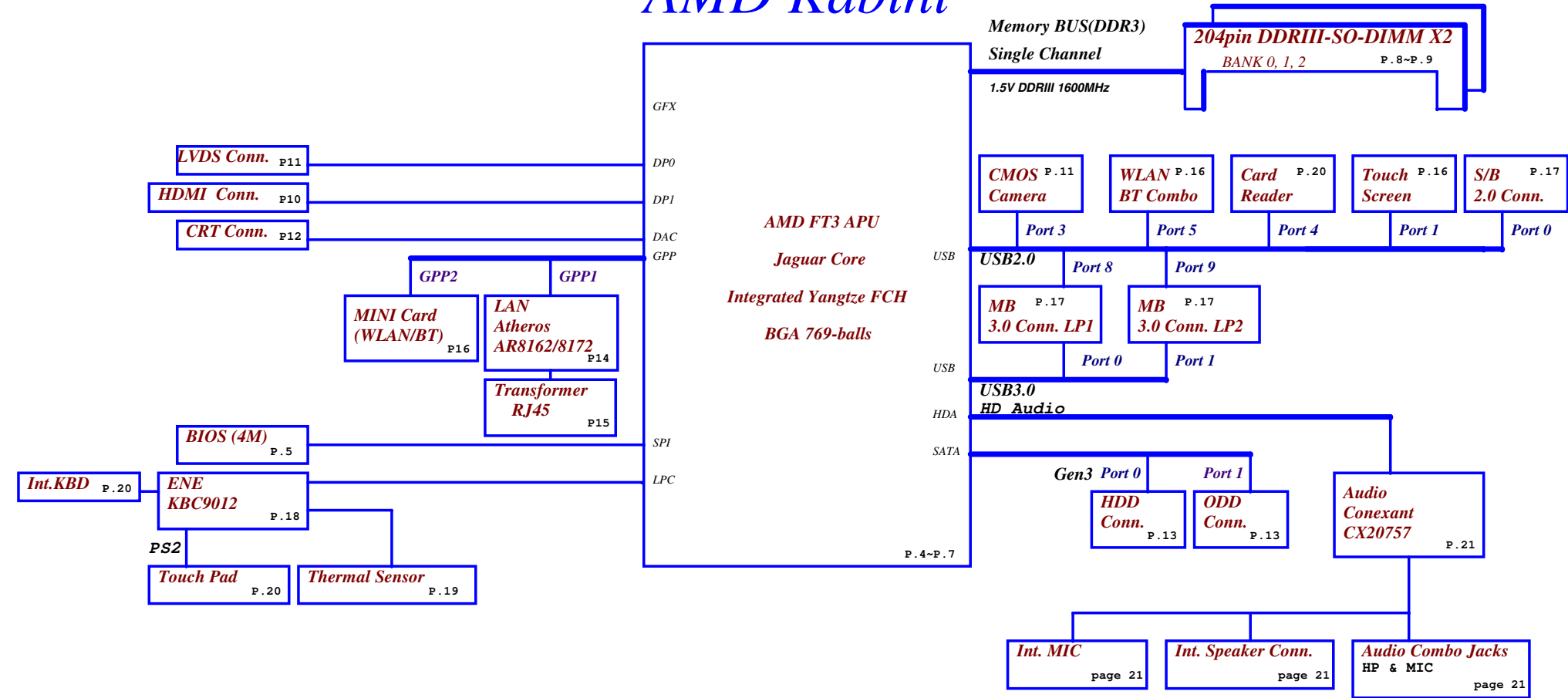
AMD 25W APU With Jaguar Core and Integrated Yangtze FCH + ATI Sun

LA-9912P REV: 1.0

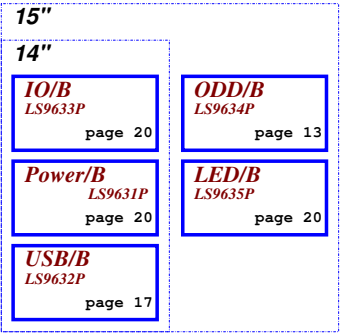
2013-04-01

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AMD Kabini



Sub-board



Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+0.95VALW	0.95V always on power rail	ON	OFF	OFF
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for APU and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+3VGS	3.3V switched power rail for VGA	ON	OFF	OFF
+1.8VGS	1.8V switched power rail for VGA	ON	OFF	OFF
+1.5VGS	1.5V switched power rail for VGA	ON	OFF	OFF
+0.95VGS	0.95V switched power rail for VGA	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON
+RTC_APU	RTC power	ON	ON	ON
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	MP
1	PVT
2	DVT
3	EVT
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
R1562	100K +/- 5%			
Board ID	R1564	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

USB OC MAPPING

OC#	USB Port
0	USB20 port0
1	USB20 port1,2,8,9
2	
3	

BOM Structure Table

BOM Structure	BTO Item
A6@	A6 R3 BGA APU
A4@	A4 R3 BGA APU
E2@	E2 R3 BGA APU
E1@	E1 R3 BGA APU
E1PC@	E1 PC BGA APU
X4@	X4 ES2 BGA APU
X5@	X5 ES2 BGA APU
X2@	X2 ES2 BGA APU
EMICU@	CardReader EMI Un pop
EMICP@	CardReadear EMI pop
EMIUSB2RU@	Right USB2.0 port EMI un pop
EMIUSB2RP@	Right USB2.0 port EMI pop
USB2R@	Right USB2.0 port component
SUN@	SUN PRO GPU (R3 compal part)
MARS@	MARS XT GPU (R1 compal part)
14@	for 14" componect
15@	for 15" componect
PX@	Common VGA circuit
CMOS@	CMOS Camera part
HDMI@	HDMI part
EMIGASP@	Gastube
8162@	Ateros AR8162 LAN Chip
8172@	Ateros AR8172 LAN Chip
SWR@	LAN Switching mode
LDO@	LAN LDO mode
THERMAL@	Lenovo Thermal Sensor
ME@	ME part
UMA@	UMA part
@	Unpop
ZODD@	Zero Power ODD part
TS@	Touch Screen
EMIP@	EMI pop component
EMIU@	EMI Un pop component
ESDP@	ESD pop component
ESDU@	ESD Un pop component

SMRUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	FCH	APU	RTD2132
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X	X	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V +3VS	V +3VS	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VS	V +3VS	X	X	X	X	V +3VS	X	V +3VS	X

APU PCIE PORT LIST

Port	Device
0	
1	LAN
2	WLAN
3	

USB Port Table

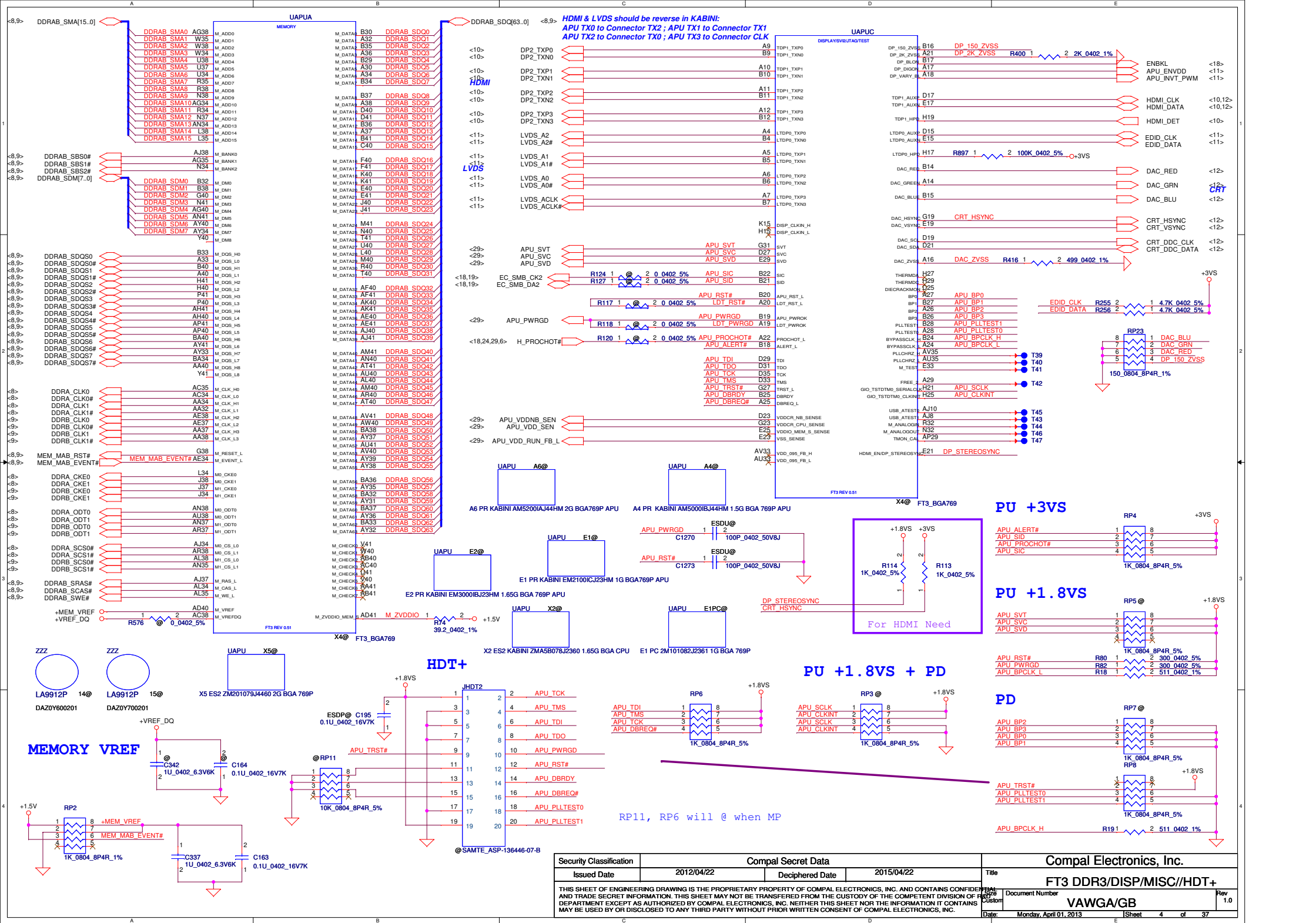
USB 2.0	USB 3.0	Port	3 External USB Port
		0	RIGHT USB
		1	Touch Screen
		2	
		3	Camera
		4	CardReader
		5	WLAN/BT Combo
		6	LEFT USB (for colay)
		7	LEFT USB (for colay)
	XHCI	0	LEFT USB3.0
		1	LEFT USB3.0

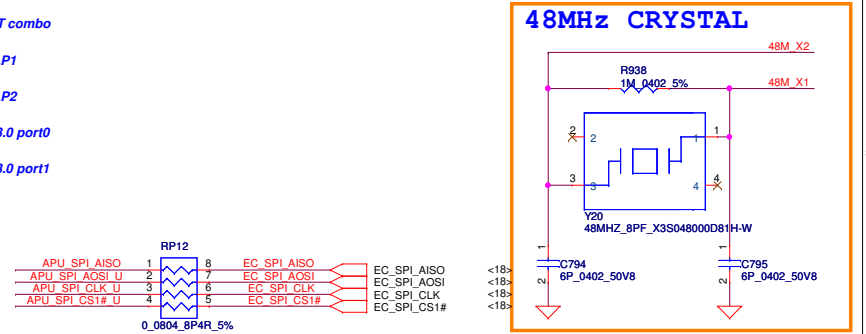
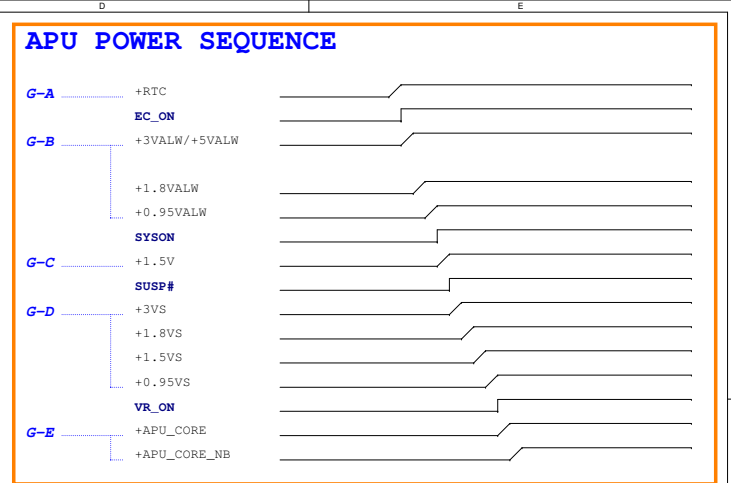
EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	Thermal Sensor	1001 101X b	9AH
			SB-TSI (APU)	1001 100X b	98H
			VGA Internal Thermal	1000 001X b	82H

APU SM Bus address

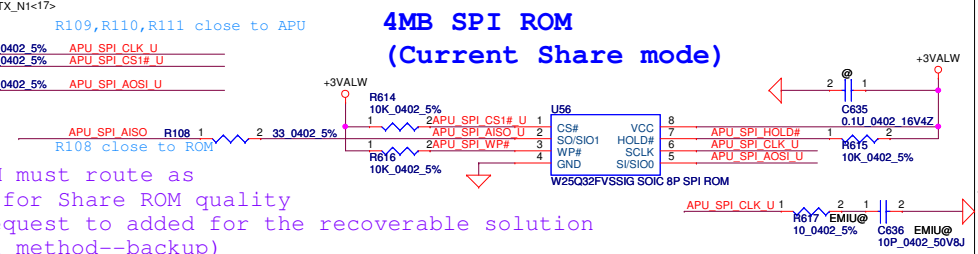
Device	Address	HEX
DDR DIMM1	1010 000Xb	A0H
DDR DIMM2	1010 001Xb	A2H

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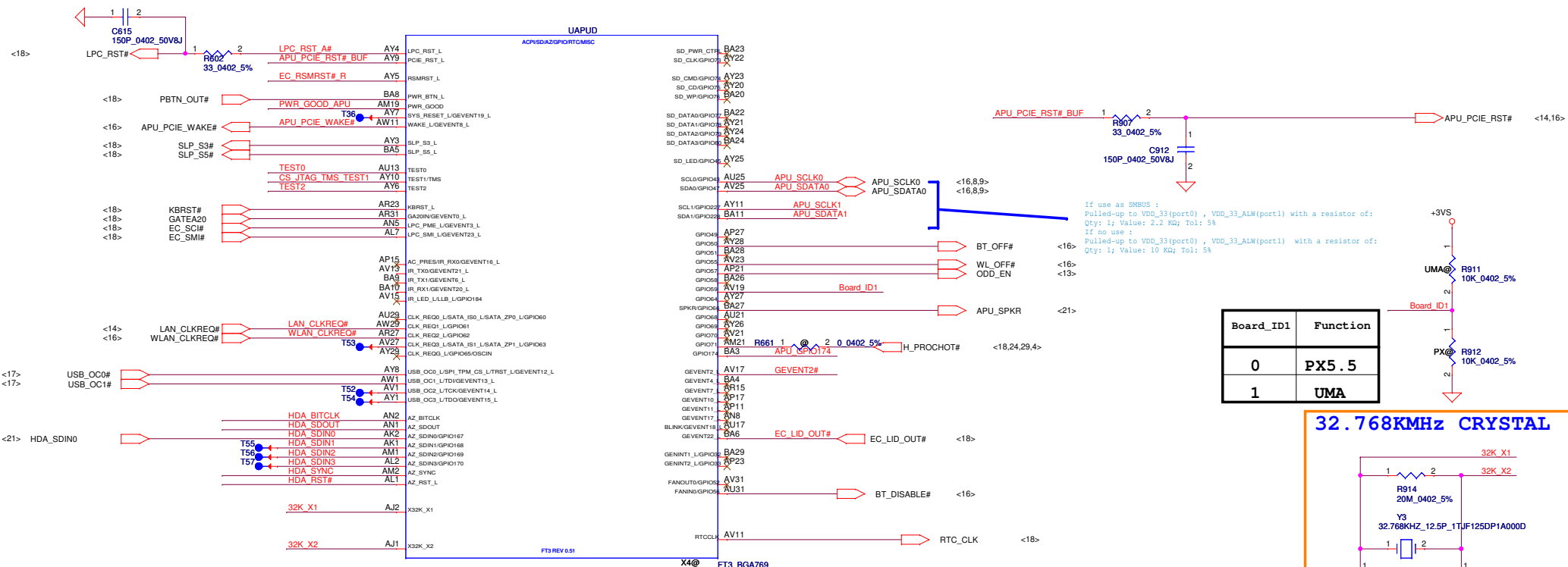




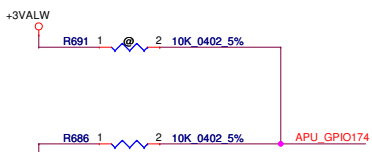
APU->EC->ROM must route as
Daisy Chain for Share ROM quality
(RP12 was request to added for the recoverable solution
as original method--backup)



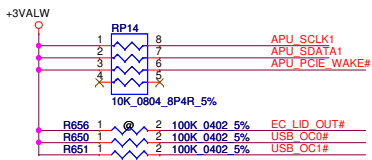
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						Date:		Thursday, March 28, 2013	



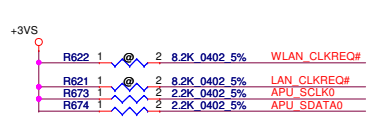
PU +3VALW + PD



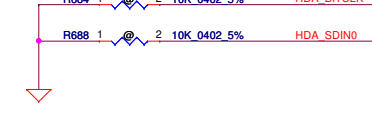
PU +3VALW



PU +3VS

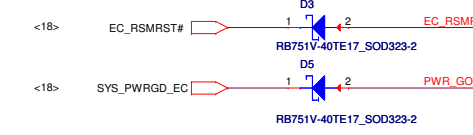


PD

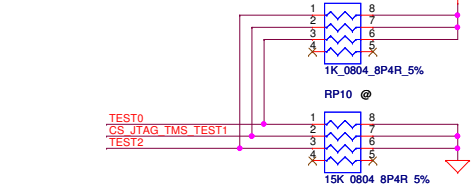


EC_RSMRST# , POWER_GOOD follow CRB (APU side 1.8V power rail)

Must connected to 10 ms RC delay circuit on +1.8-V S5 power rail.

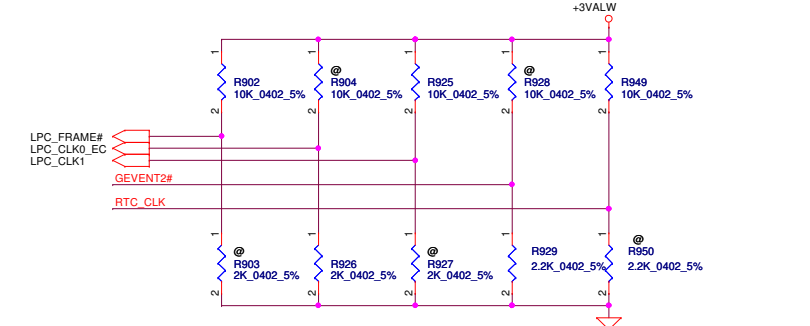


PU +3VALW + PD

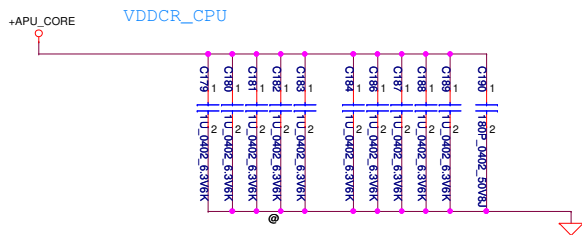


STRAPS OF APU

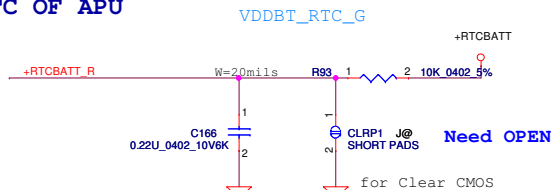
	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWER UP/RESET TIMING (DEFAULT)
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	FAST POWER UP/RESET TIMING FOR SIMULATION



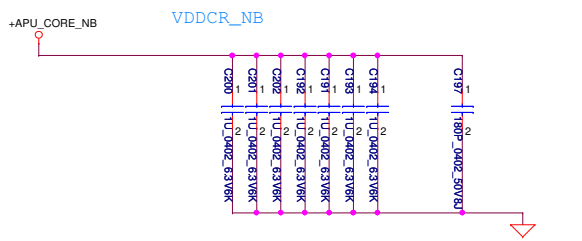
CORE POWER OF APU



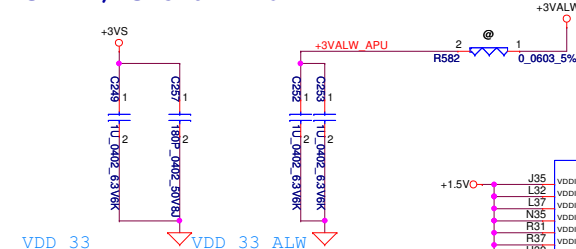
RTC OF APU



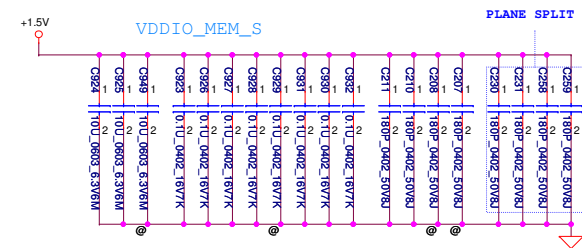
INTEGRATED GPU POWER OF APU



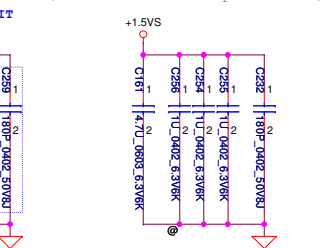
+3VALW/+3VS OF APU



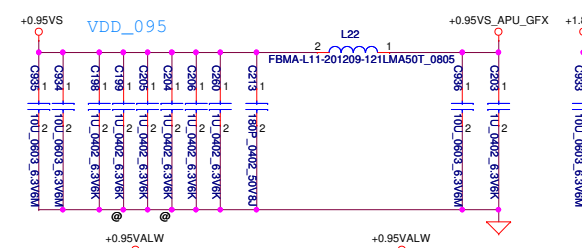
+1.5V/+1.5VS OF APU



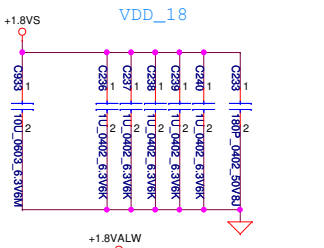
VDDIO_AZ_ALW (Could be S0 or S5 power rail)



+0.95VALW/+0.95VS OF APU



+1.8VALW/+1.8VS OF APU



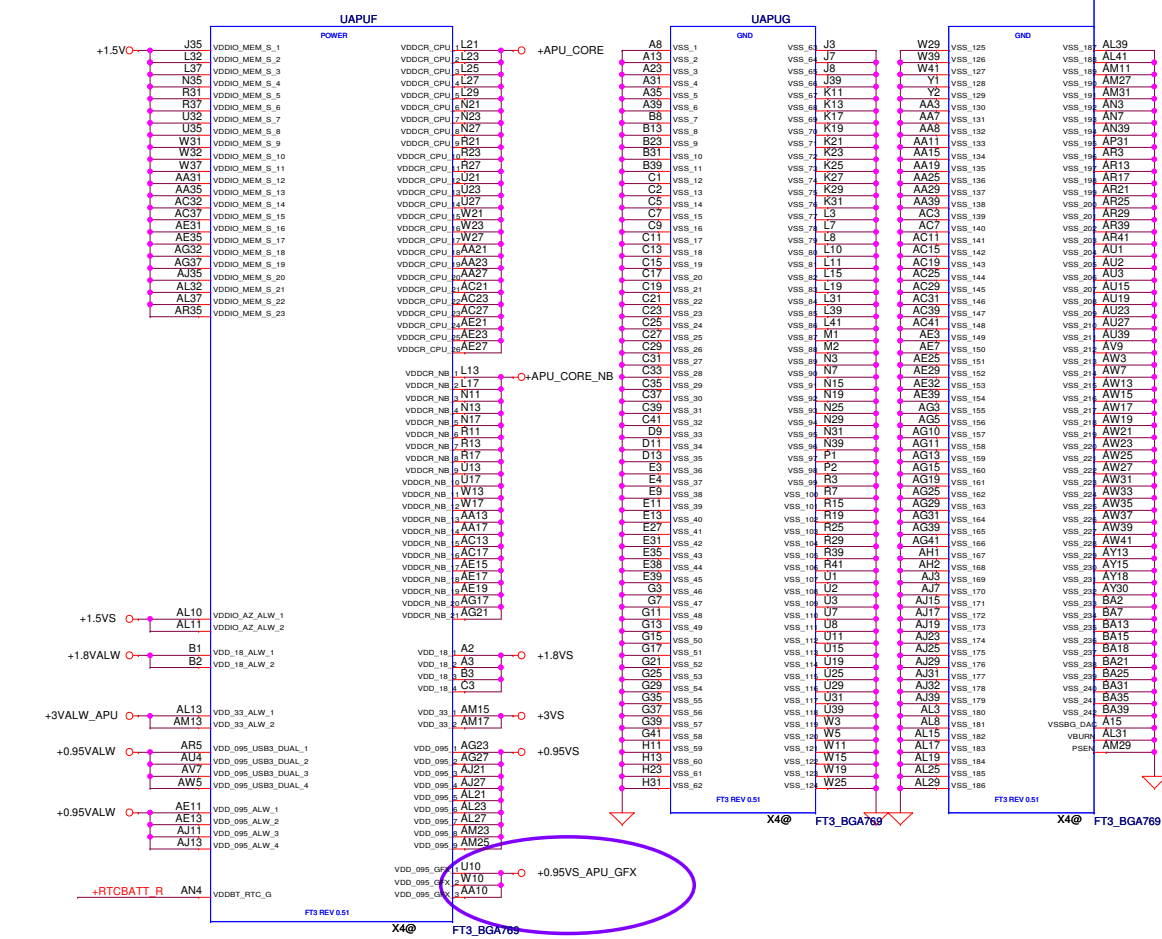
VDD_095_USB3_DUAL



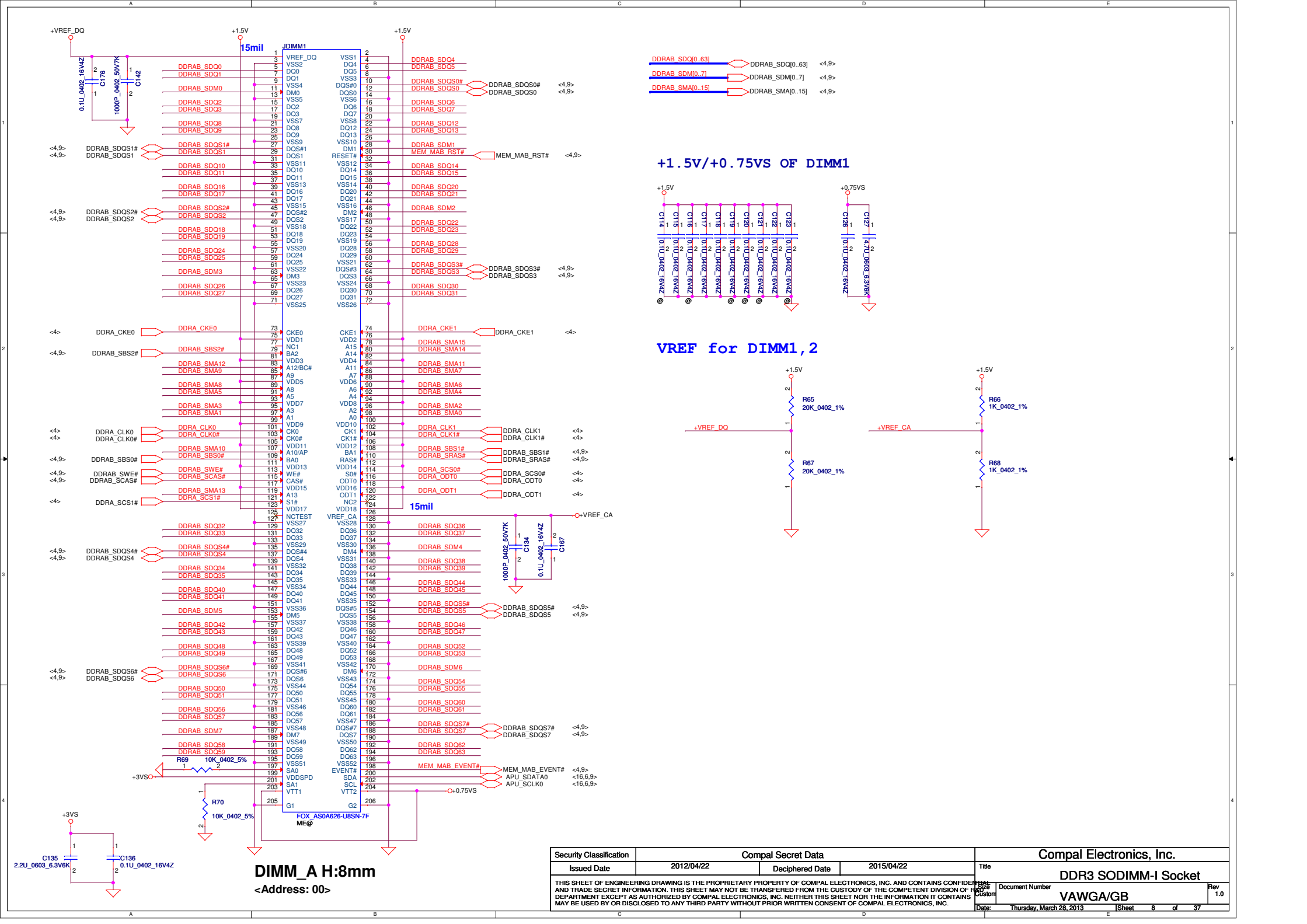
VDD_095_ALW

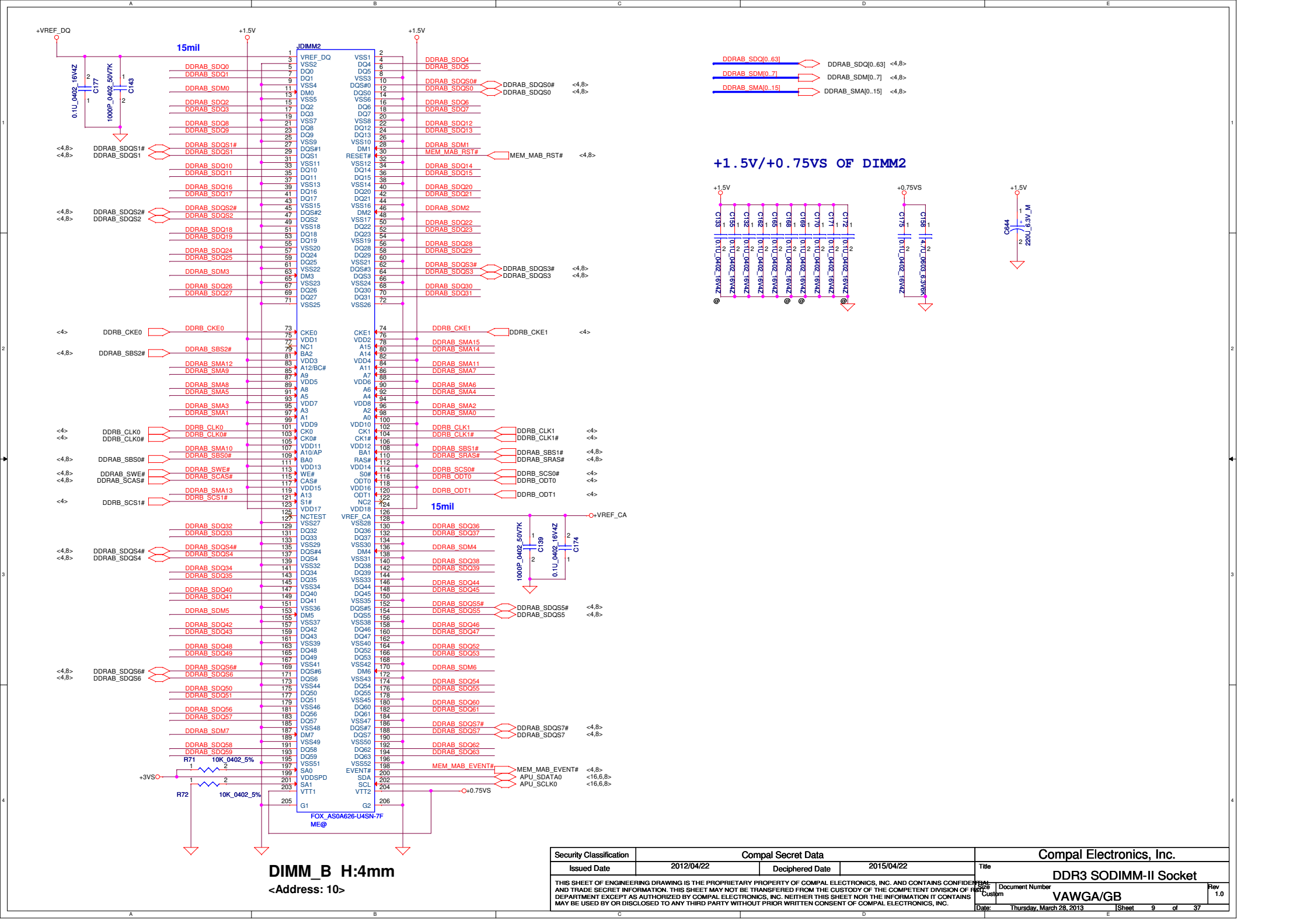


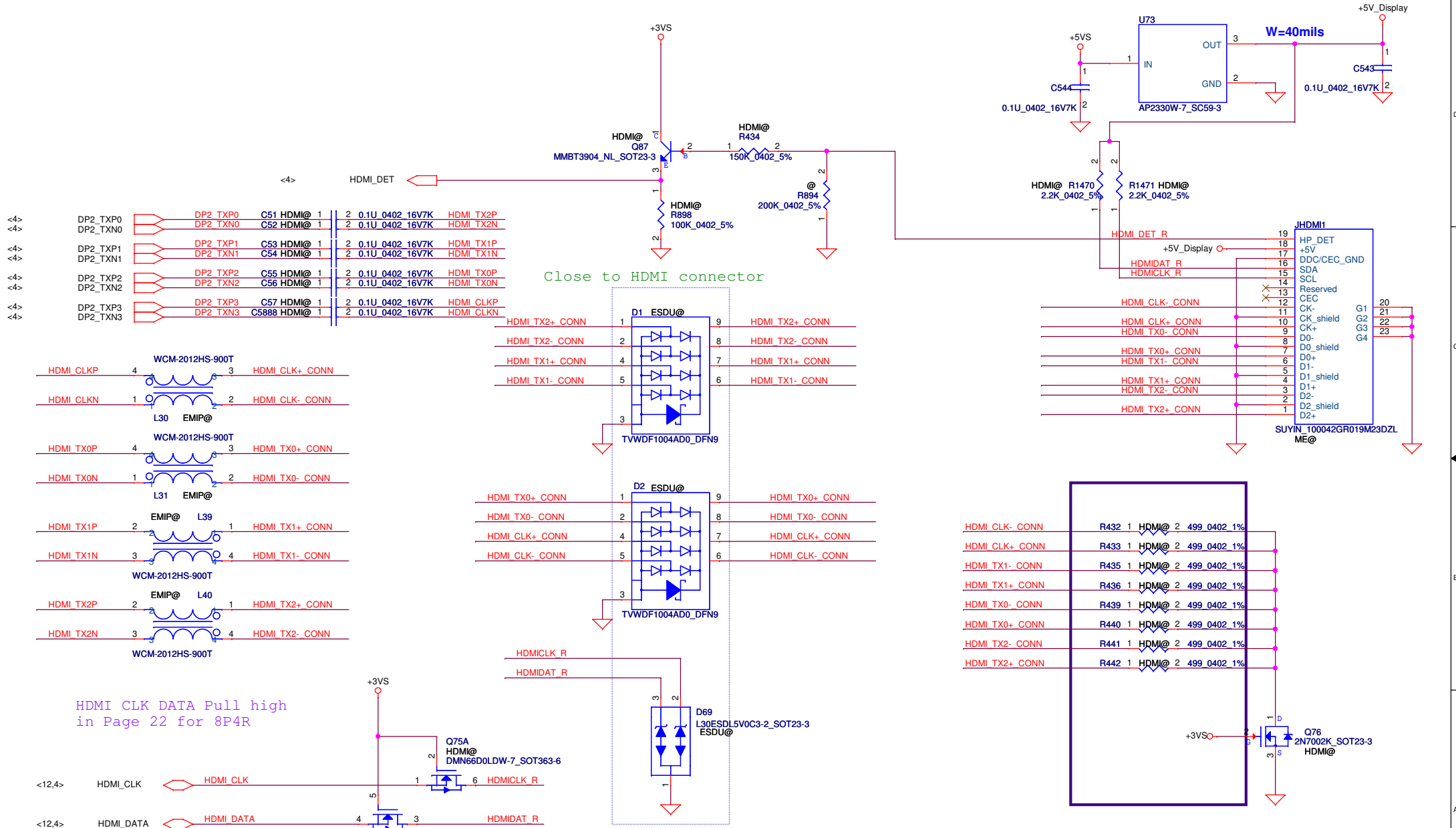
VDD_18_ALW



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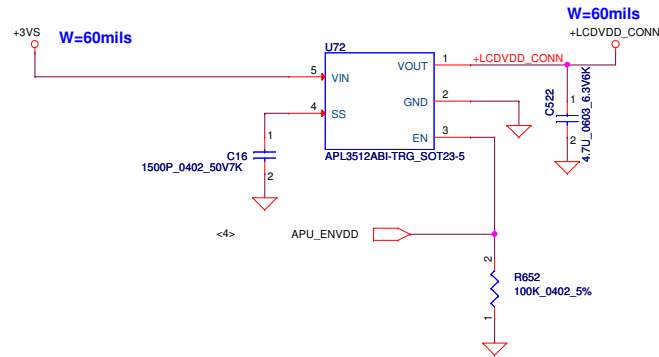




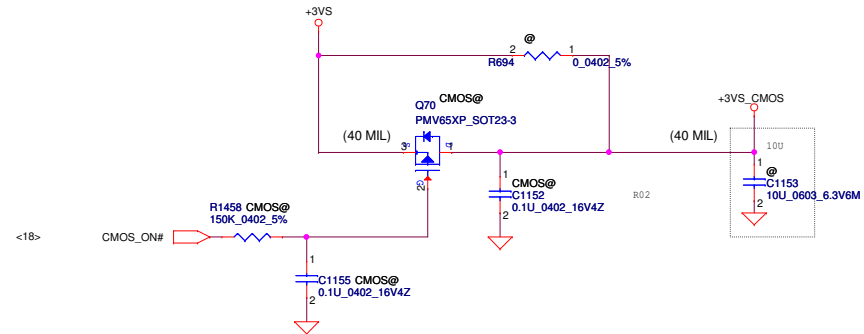
HDMI CLK DATA Pull high
in Page 22 for 8P4R

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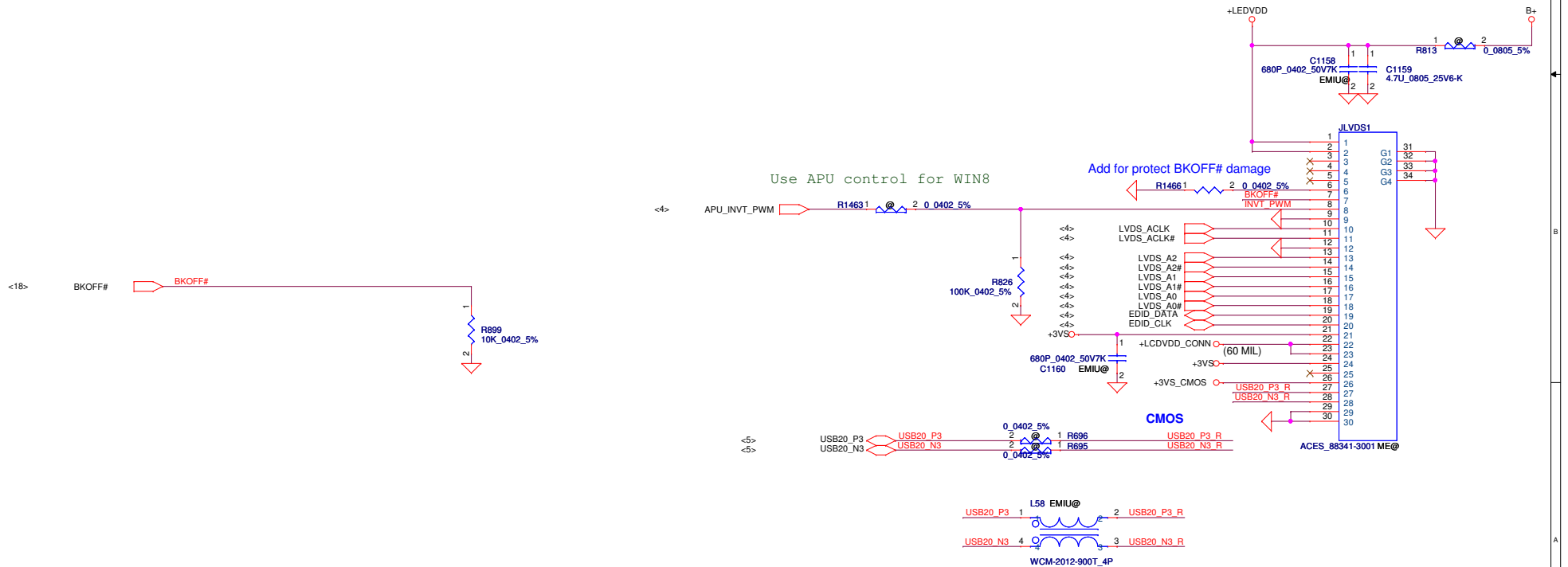
LCD POWER CIRCUIT



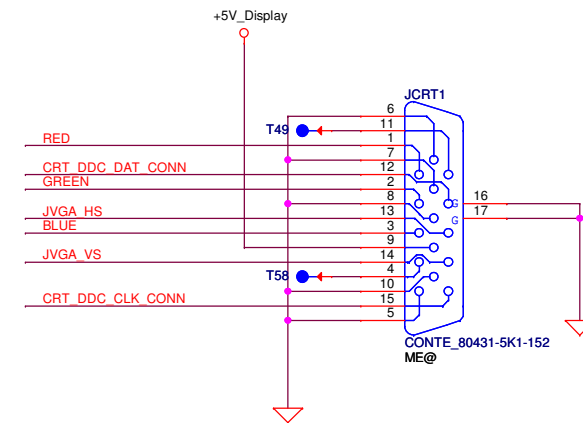
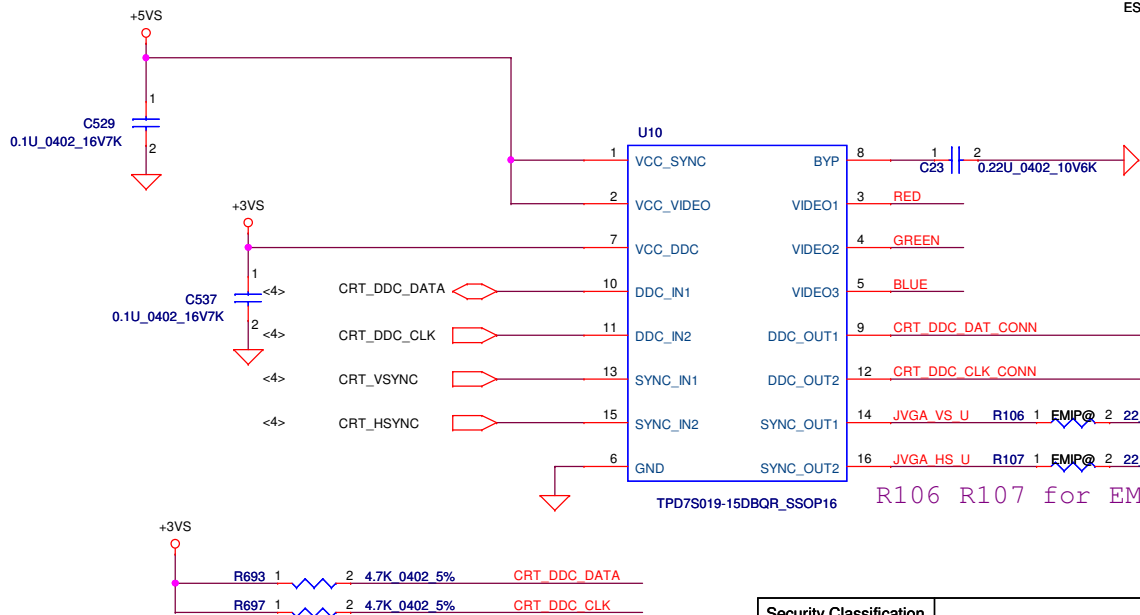
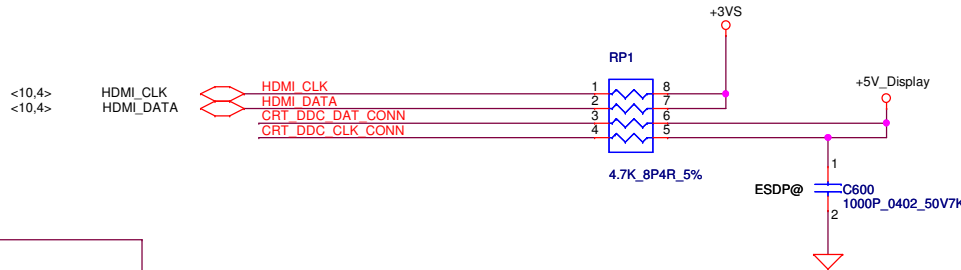
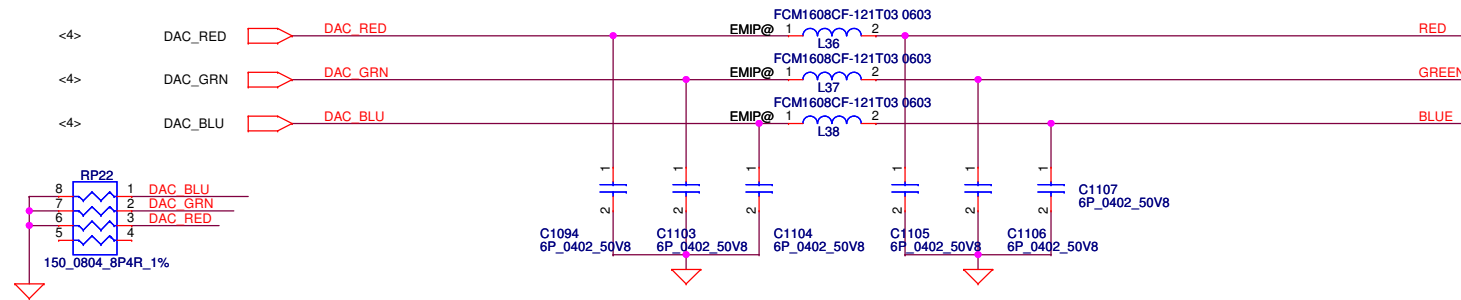
CMOS Camera



VGA LCD/PANEL BD. Conn.

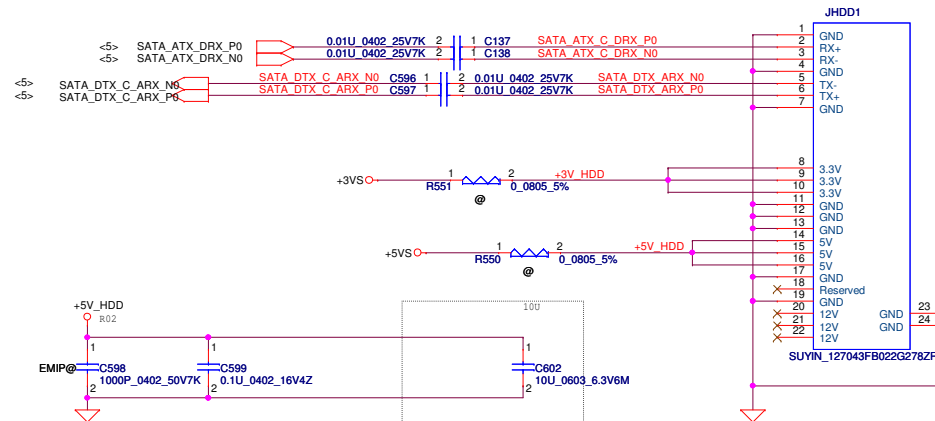


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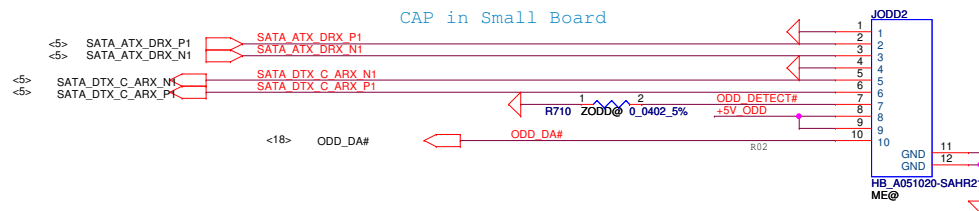


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SATA HDD Conn.

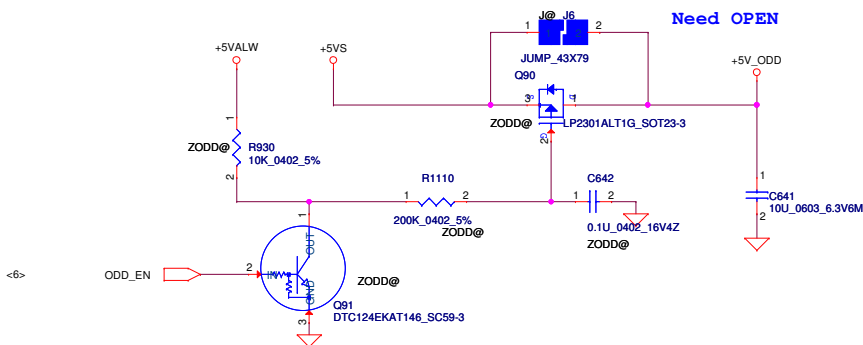


FOR 15" SATA ODD FFC Conn.

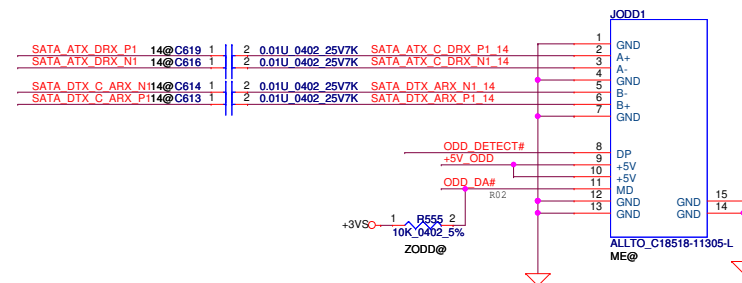


Co-lay

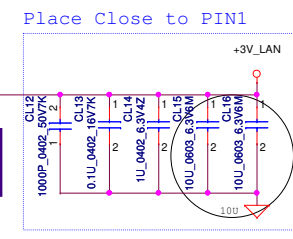
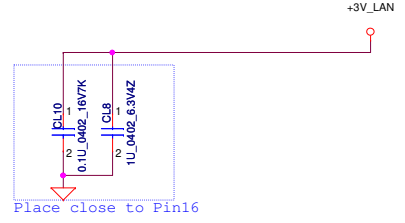
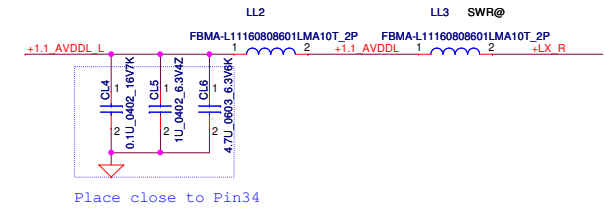
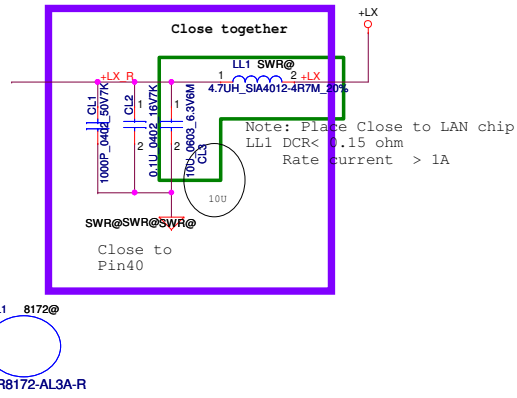
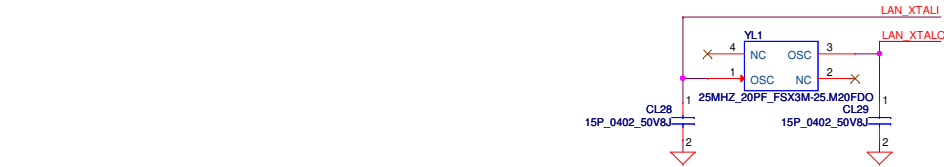
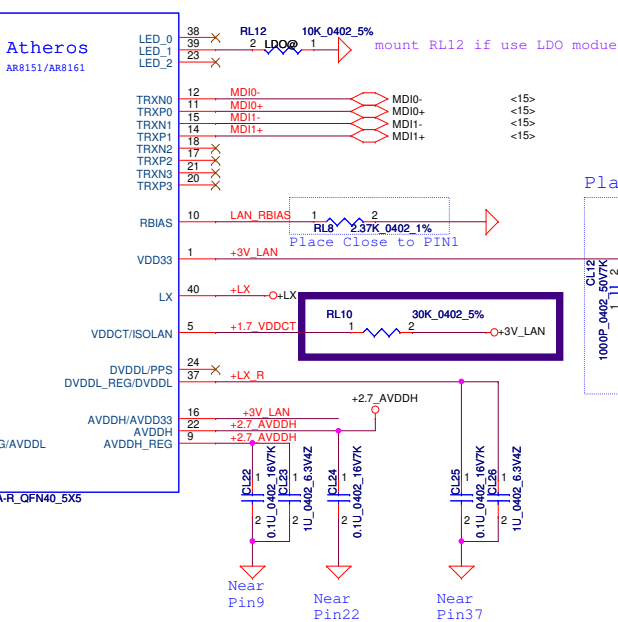
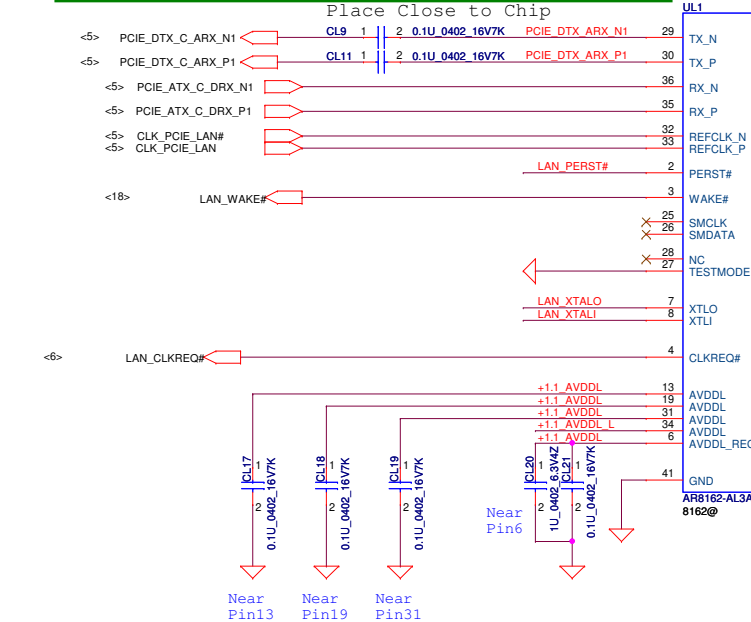
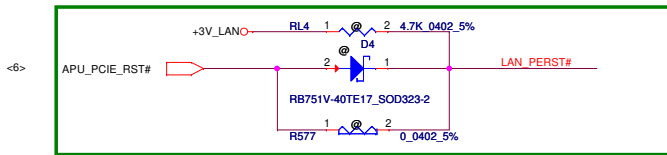
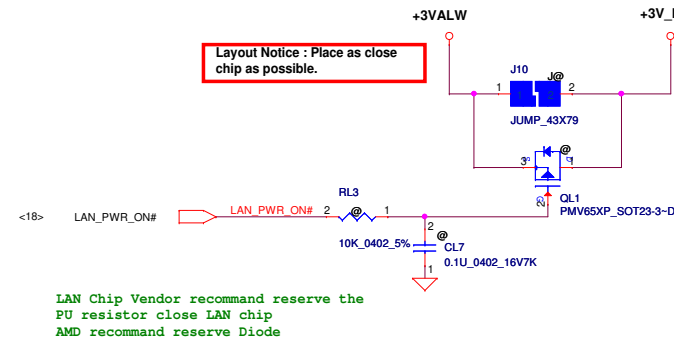
ODD Power Control



FOR 14" SATA ODD Conn.



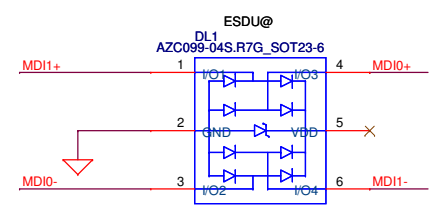
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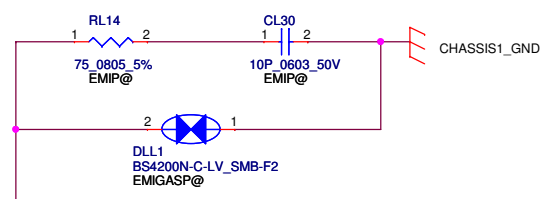
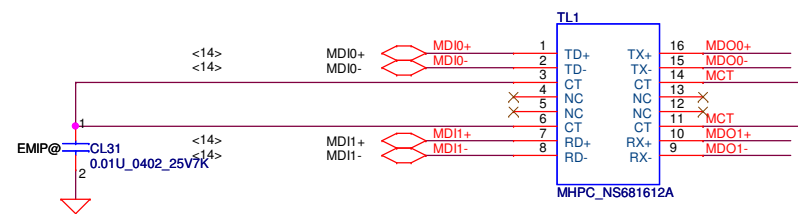
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				Date: Thursday, March 28, 2013	Rev 1.0
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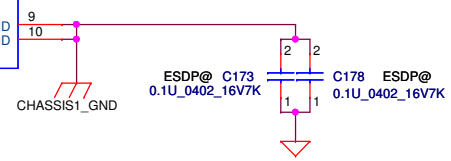
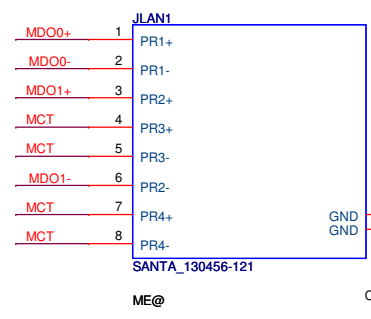
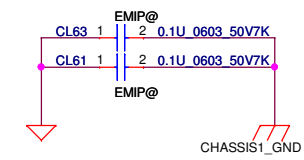
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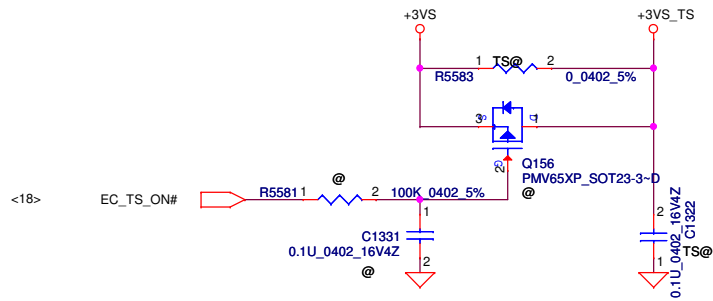
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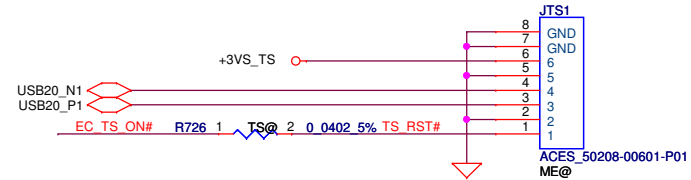
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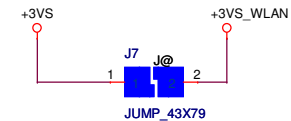
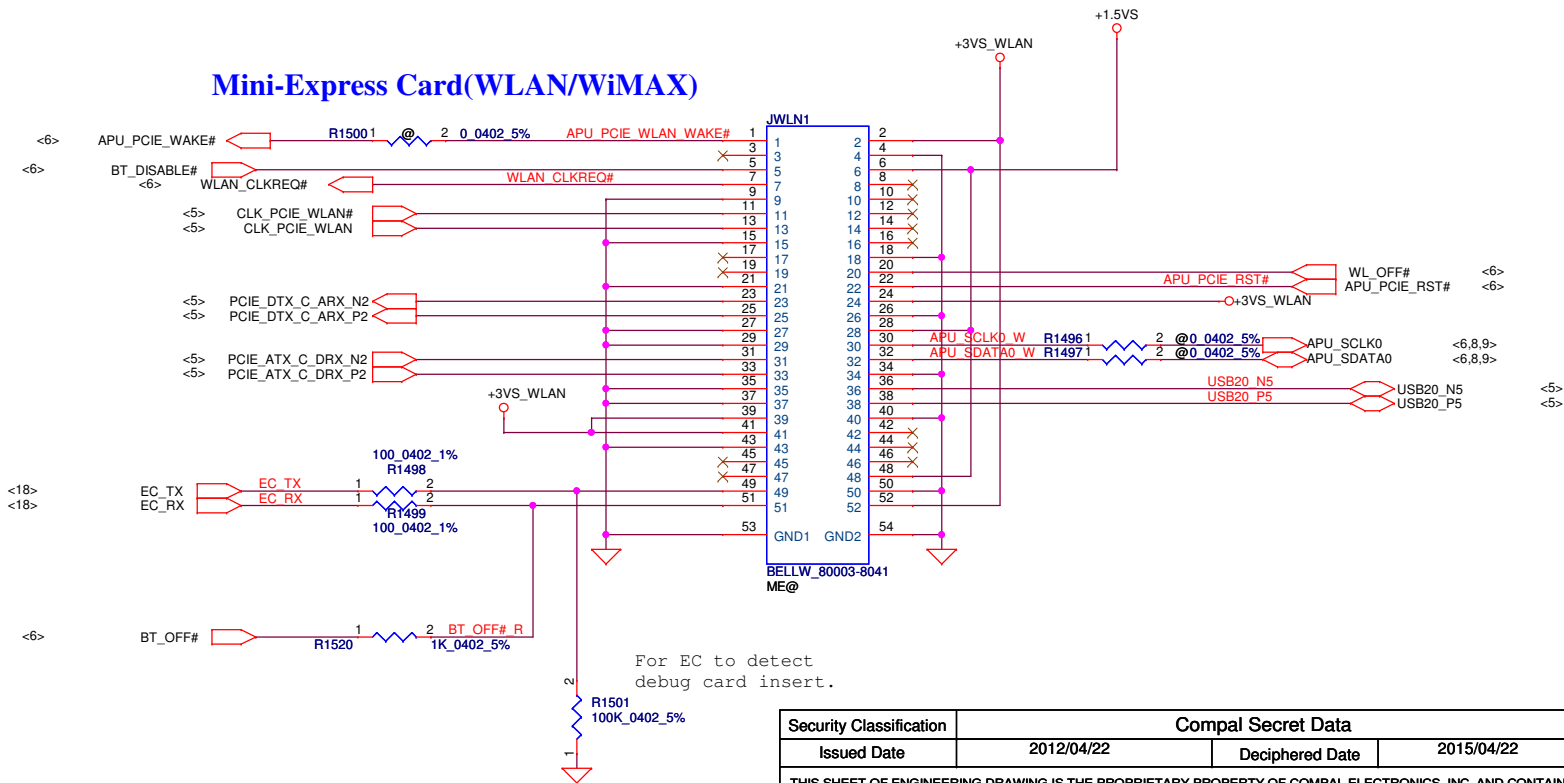
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				Rev	1.0
				Date:	Thursday, March 28, 2013
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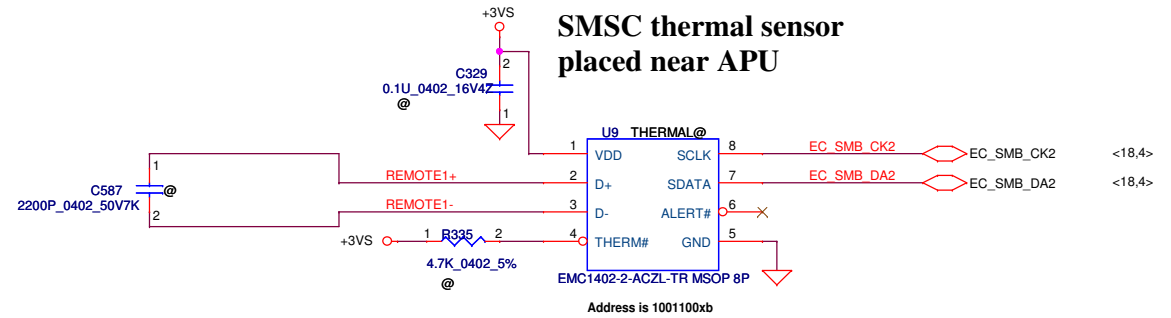
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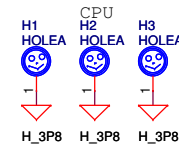
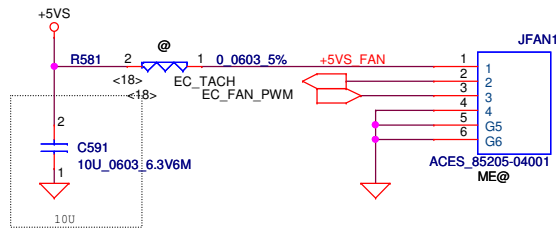
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										Document Number	
										VAWGA/GB	
										Date: Thursday, March 28, 2013	
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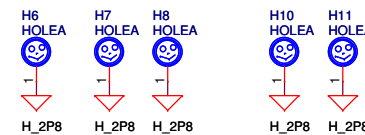
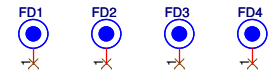
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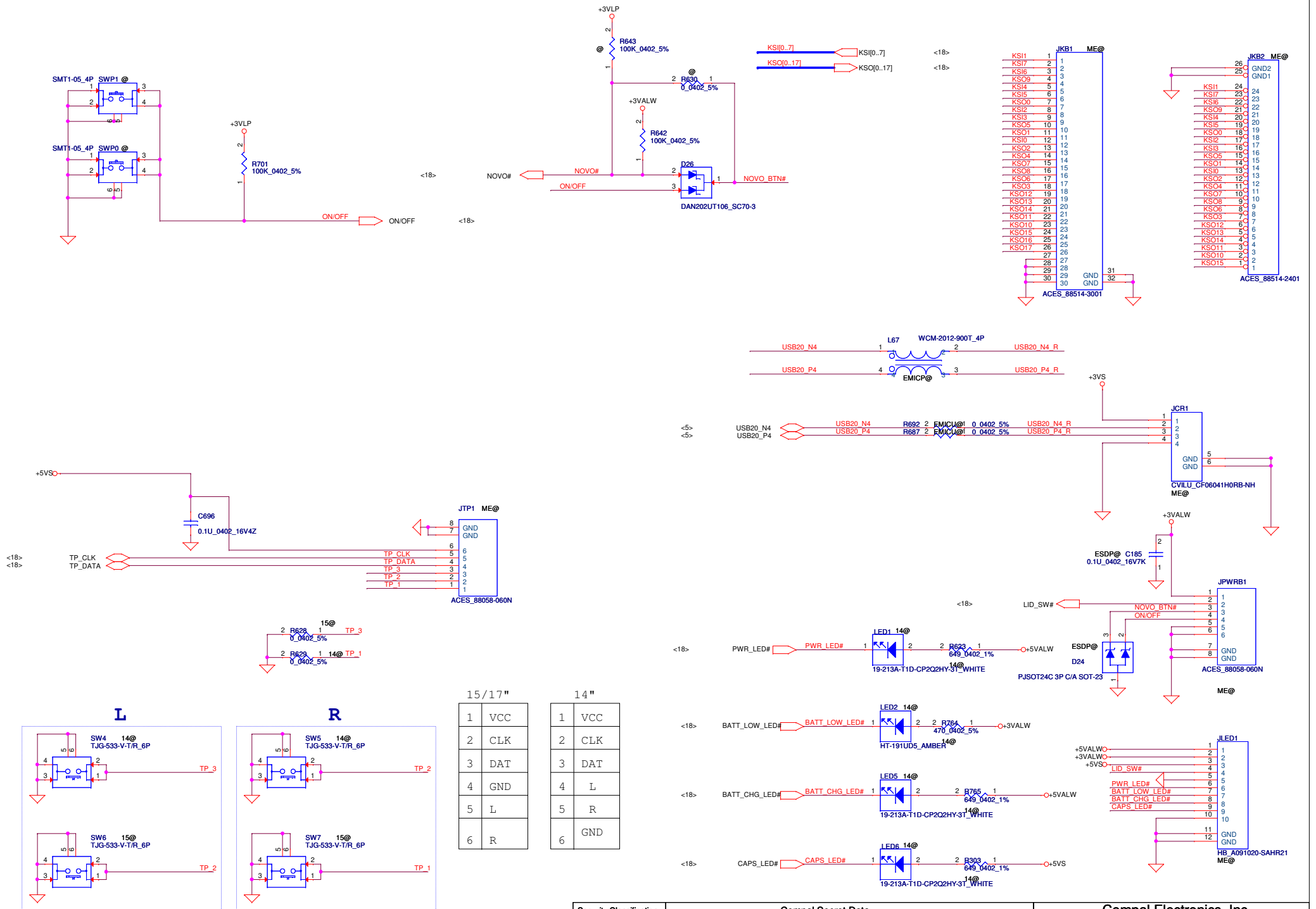


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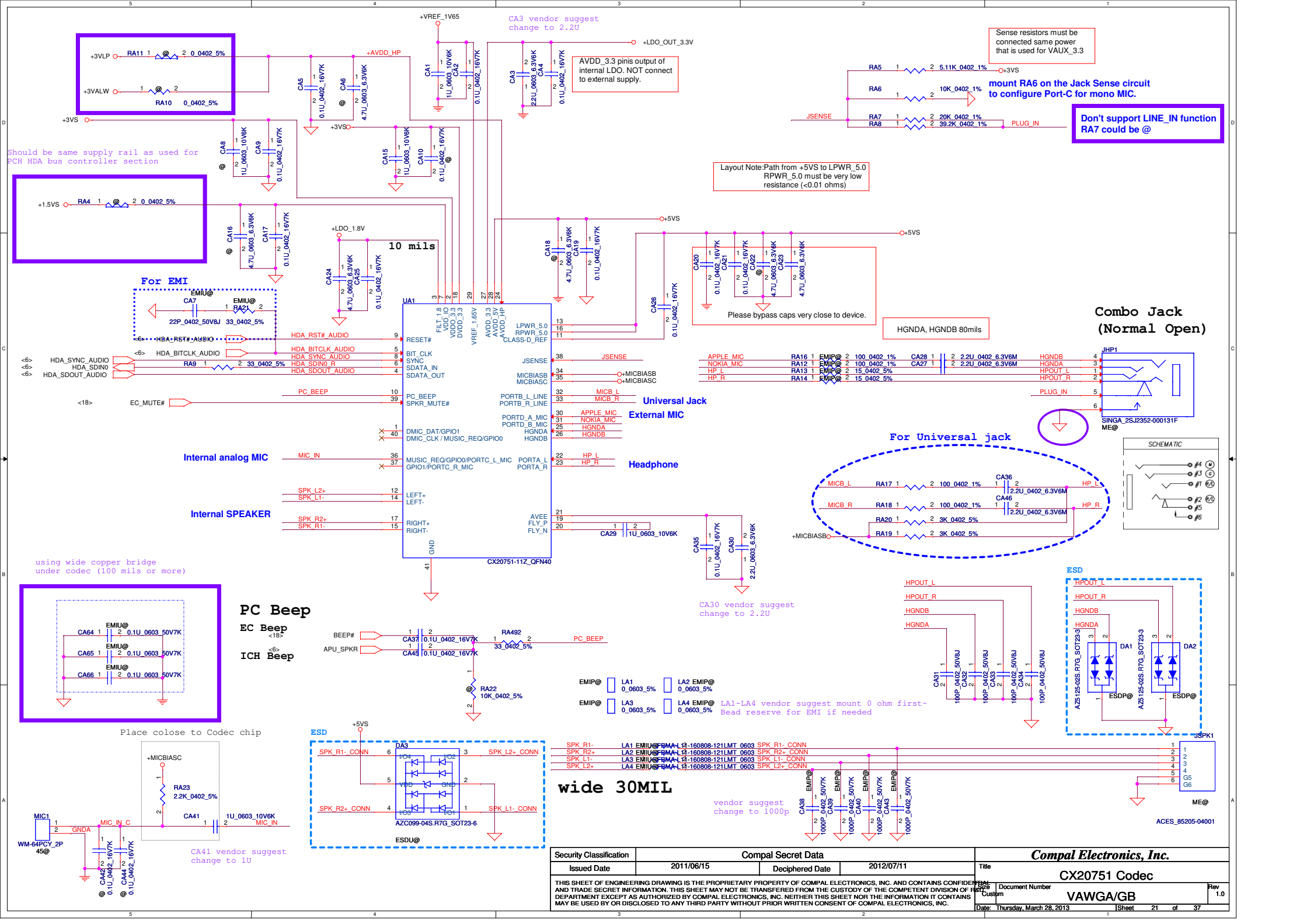
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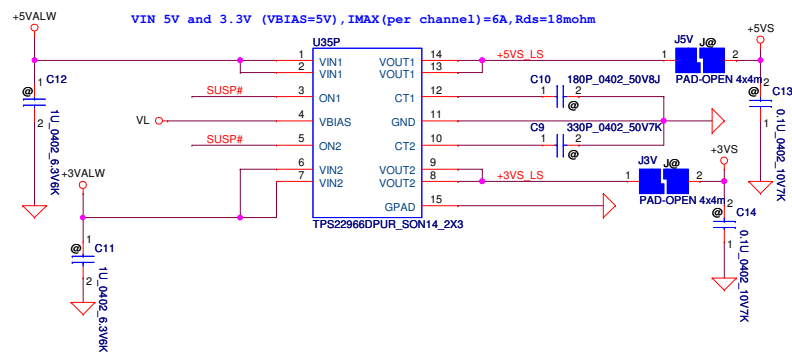
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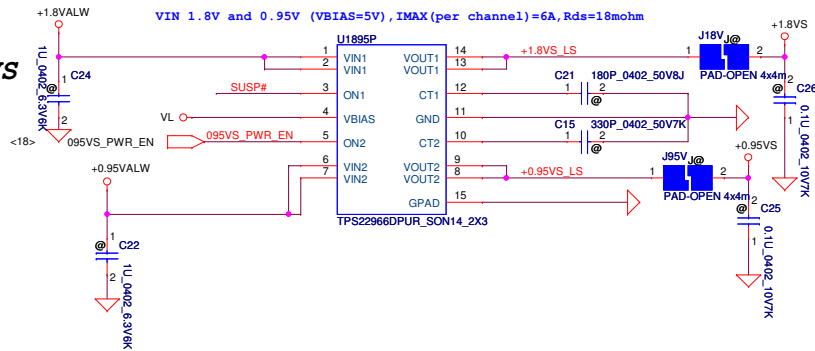
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Issued Date		2012/04/22		Deciphered Date		2015/04/22		Title					
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								Document Number		Rev			
								VAWGA/GB				1.0	
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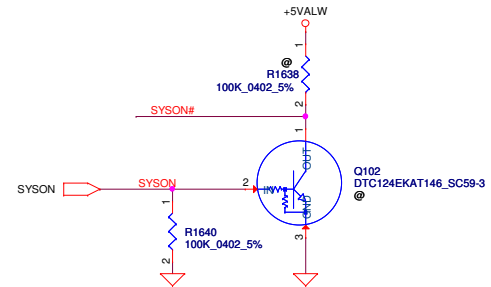
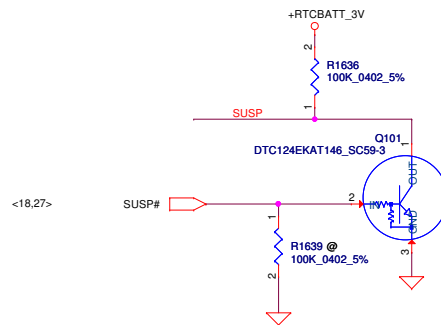
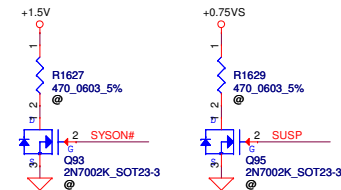
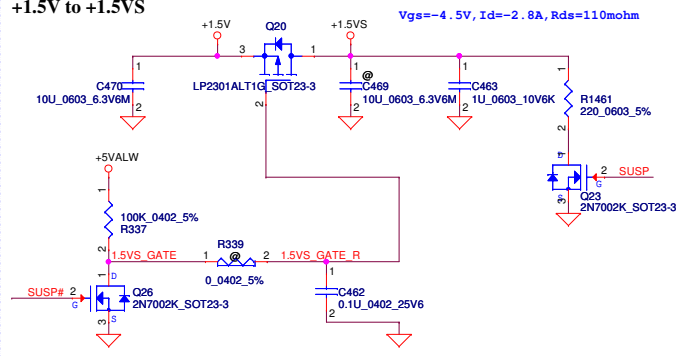
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+3VALW TO +3VS
Load switch



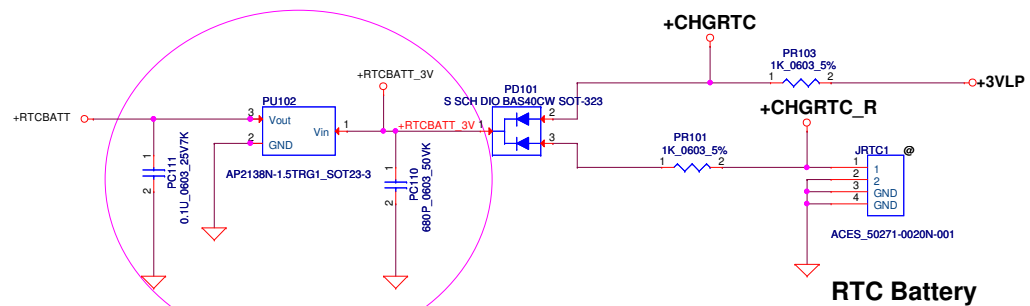
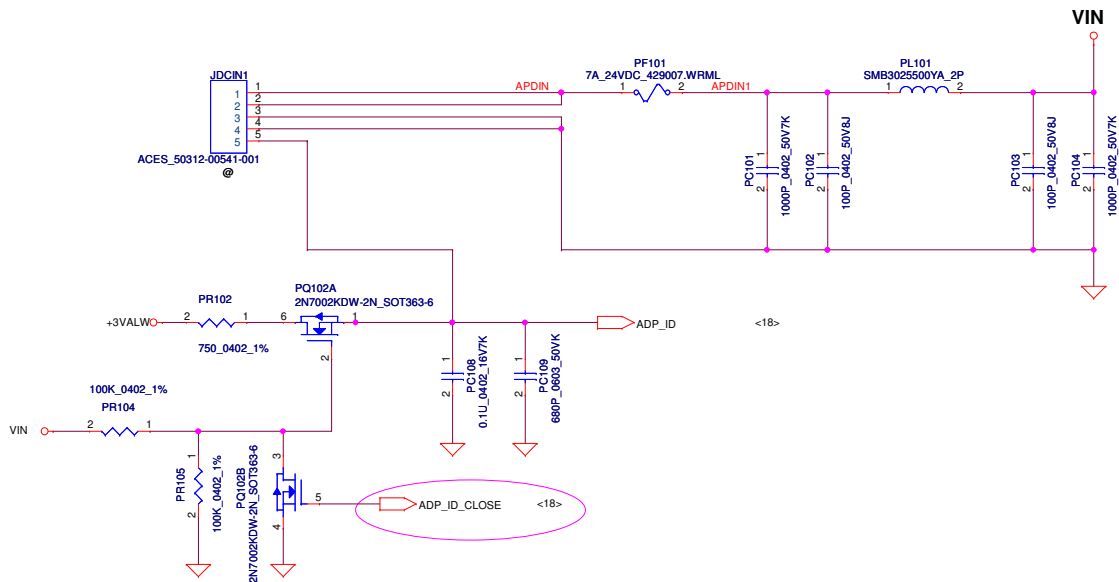
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+0.95VALW TO +0.95VS
Load switch



+1.5V to +1.5VS

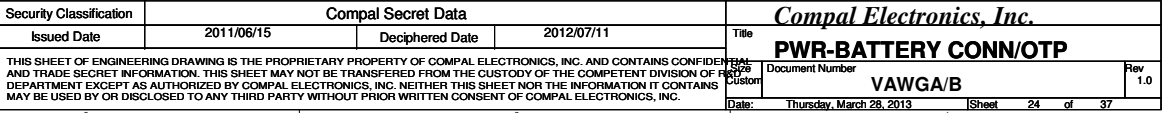


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Issued Date	2012/04/22	Deciphered Date	2015/04/22	Title	
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Need use +3.3V transfer to +1.5V LDO to APU side for Kaibini

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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	PWR-DCIN / RTC Battery
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				Date:	Thursday, March 28, 2013
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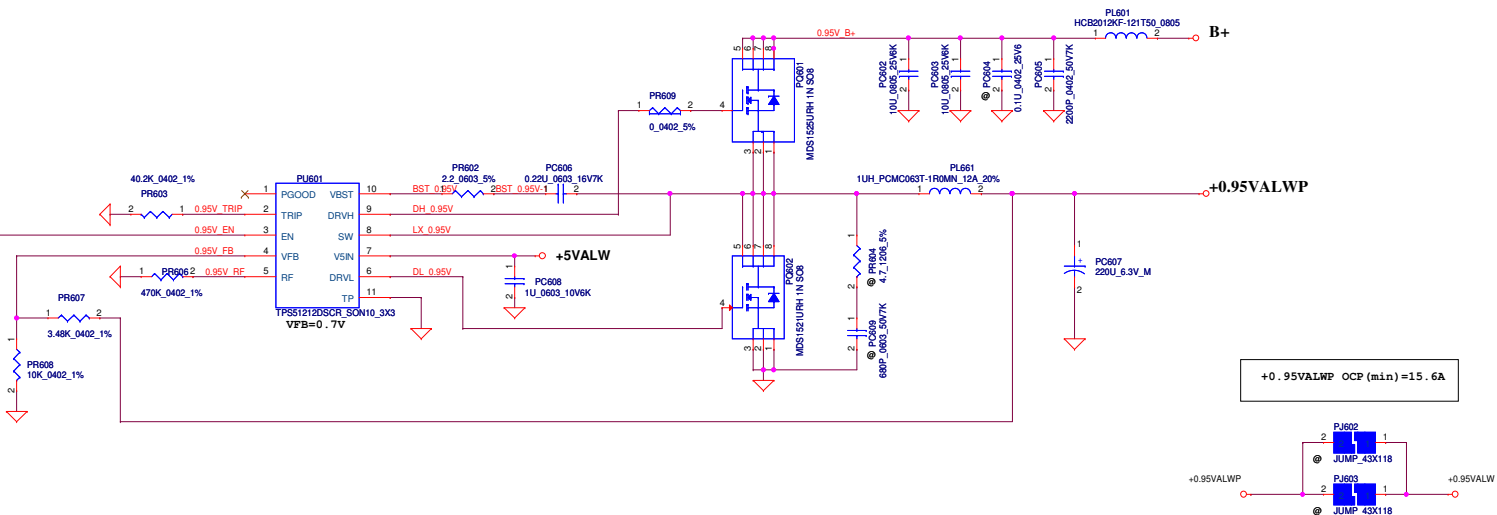
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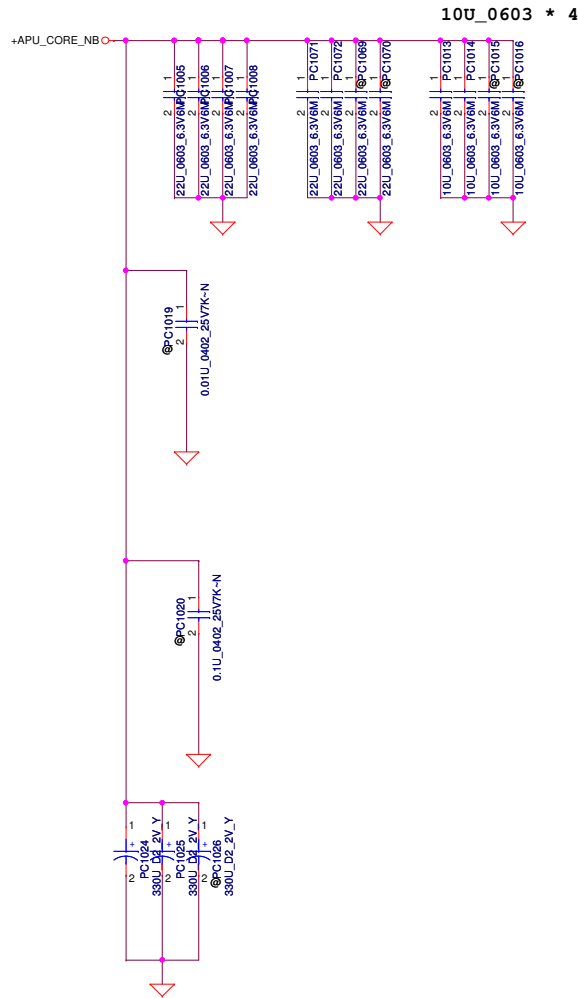
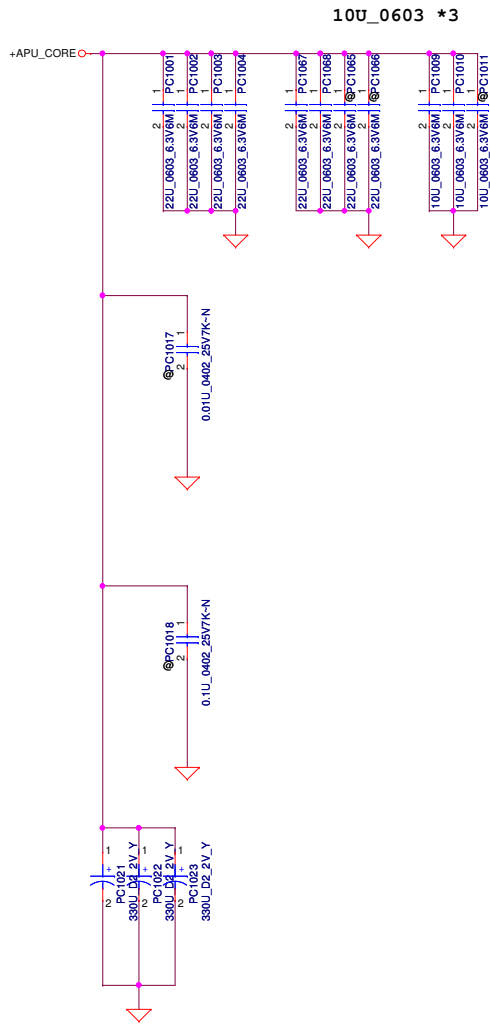
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SPOK

PR605 reserve



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Security Classification	Compal Secret Data			Compal Electronics, Inc.		
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Item	Reason for change	PG#	Modify List	Date	Phase
1					
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Item	Reason for change	PG#	Modify List	Date	Phase
1					
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11					
12					
13					
14					
15					
16					
17					

Version change list (P.I.R. List)

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for HW

Item	Reason for change	PG#	Modify List	Date	Phase
1	For share rom	18	Change SYS_PWRGD_EC from pin 86 to pin 32	12/17	DVT
2	For 095VS_PWR_EN pull down	18	Add R207	12/17	DVT
3	For VBIAS first raise up	22	Change U1895V, U35P, U1895P VBIAS from +5VALW to VL	12/17	DVT
4	For follow VIWGP design	17	Change JUSB3 pin define	12/18	DVT
5	For Audio Precision	21	Change CA36, CA46 from 1U to 2.2U	12/21	DVT
6	For SYS_PWRGD_EC pull down	18	Add R208	12/24	DVT
7	For share rom	18	Change R1575, R1576 to 100K	12/24	DVT
8	For reserve EC +3VL	18 05	Add J11, J12 and modify +3VALW to +3V_EC	12/24	DVT
9	For share ROM	05	modify ROM net-name & resistor value	12/24	DVT
10	For common VIWGP design	12	modify R106, R107 to 22ohm	12/24	DVT
11	For power S3 reduction	18	Change EC_INVT_PWM to ADP_ID_CLOSE	12/25	DVT
12	For common VIWGP design	13	Change JODD1 symbol	12/27	DVT
13	For reserve wake on wlan function	16	Add R1500	12/27	DVT
14	For 1.5VS discharge	22	Change R339 to 0ohm, mount Q23 & R1461	12/29	DVT
15	For AMD suggest	4	Change R576 to 0ohm	12/29	DVT
16	For +3VALW APU Power Consumption	7	Add R582	01/03	DVT
17	For ESD request	12 18 29	Add C600, C601, PC6601, PC6602	01/03	DVT
18	For no support DC wake & LID function	18	Pull high only SMB & RST use +3V_EC, other use +3VALW	01/04	DVT
19	For reserve cost down experiment	20	Add R630, R643	01/04	DVT
20	For Common VIWGP	20	Change SW4,SW5,SW6,SW7 footprint	01/04	DVT
21	For instant plug/unplug AC has beep sound	21	@RA22	01/04	DVT
22	For Crystal Capactance fine tune	5 6	Modify C794,C795,C682,C686 value	01/09	DVT

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				C38-G series Chief River Schematic ^{1.0}	
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Version change list (P.I.R. List)

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for HW

Item	Reason for change	PG#	Modify List	Date	Phase
1	For EMI request	20	Change L67 to EMICP@, Change R692,R687 to EMICU@	02/02	PVT
2	For Share ROM recoverable solution as original method	05	Add RP12	02/02	PVT
3	For ZiZi noise	21	Change AVDD_HP from +3VS to +3VLP	02/02	PVT
4	For follow KABINI latest CRB	04	@ R576,C164,C342	02/02	PVT
5	For APU control PWM only	11	Delete R1465	02/02	PVT
6	For Corret Net-name to prevet confuse	04 11	Change TL_INVT_PWM, TL_ENVDD to APU_INVT_PWM, APU_ENVDD	02/02	PVT
7	For Reserve DDC CLK DATA pull high	12	Add R693, R697	02/02	PVT
8	For Common Intel project	20	Change R623,R765,R303 to 620ohm	02/02	PVT
9	For Common Intel project	13	Reserve R551	02/02	PVT
10	For reduce BOM	21	Delete RA3, and Change RA4 to short-pad	02/05	PVT
11	For reduce BOM	16	Change R1498,R1499 from 0 ohm to 100 ohm	02/05	PVT
12	For reduce BOM	11	Change R1463 from 0 ohm to short-pad	02/06	PVT
13	For better audio precision performance	21	Change CA27,CA28 from 1U to 2.2U	02/08	PVT
14	For reduce BOM & layout concern	07	Delete C195	02/16	PVT
15	For test point request	12	Add T49, T58 on JCRT1	02/18	PVT
16	For ESD request	15	Add C173, C178	02/18	PVT
17	For reduce BOM	05	Change R116, R119, R125, R126 to short-pad	02/18	PVT
18	For Crystal timing	06	Change C682 from 18P to 22P	02/20	PVT
19	For ESD request	20	Change D24 from ESDU@ to ESDP@, Part number from SCA00000E00 to SCA00001G00	02/23	PVT
20	For EMI request	11 17 20	Change L58,L51,L55,L66,L67 from SM070000K00 to SM070000Z00	02/23	PVT
21					
22					
23					

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				C38-G series Chief River Schematic ^{1.0}	
Date: Thursday, March 28, 2013				Sheet	34 of 37

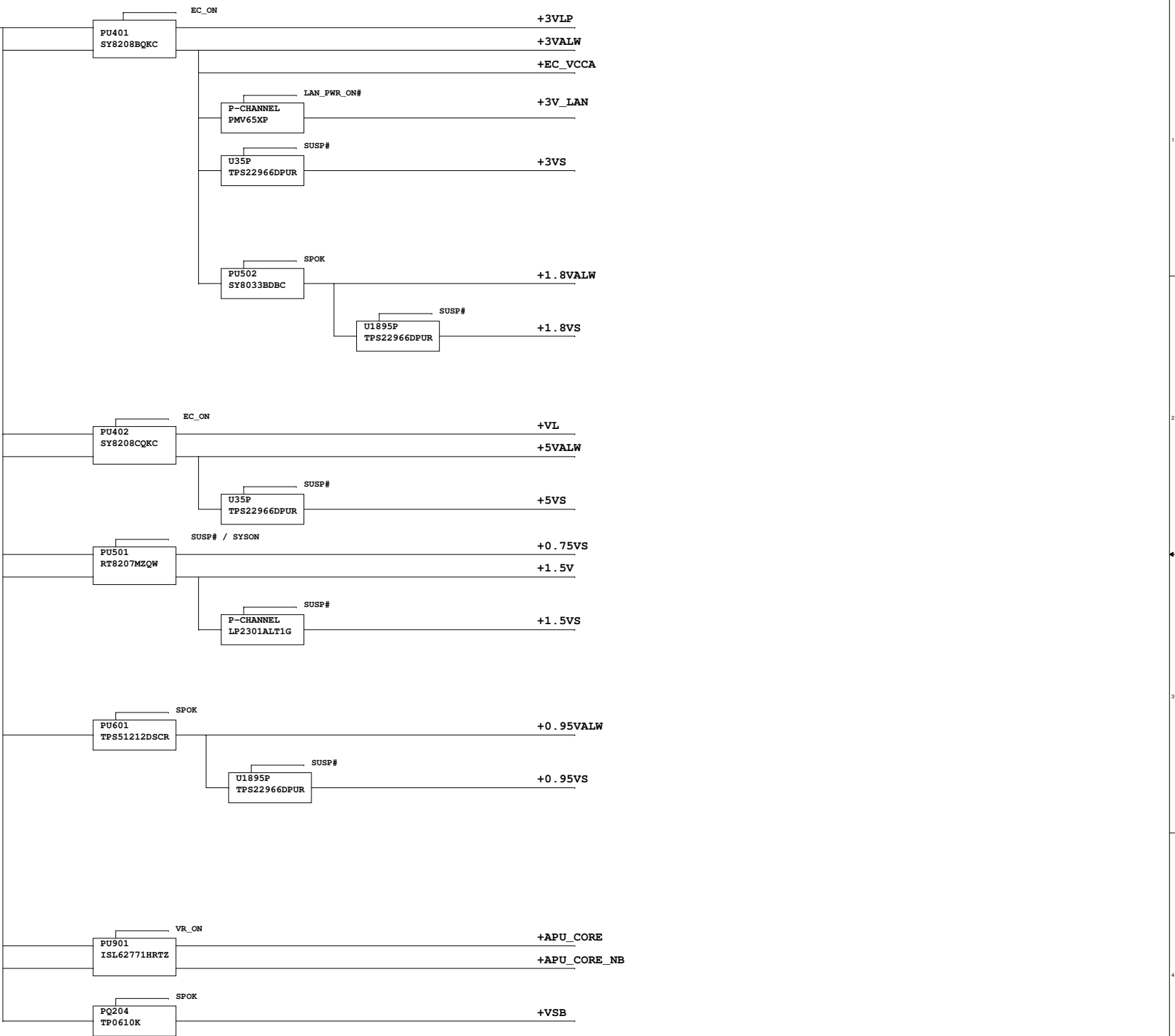
Version change list (P.I.R. List)

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for PWR

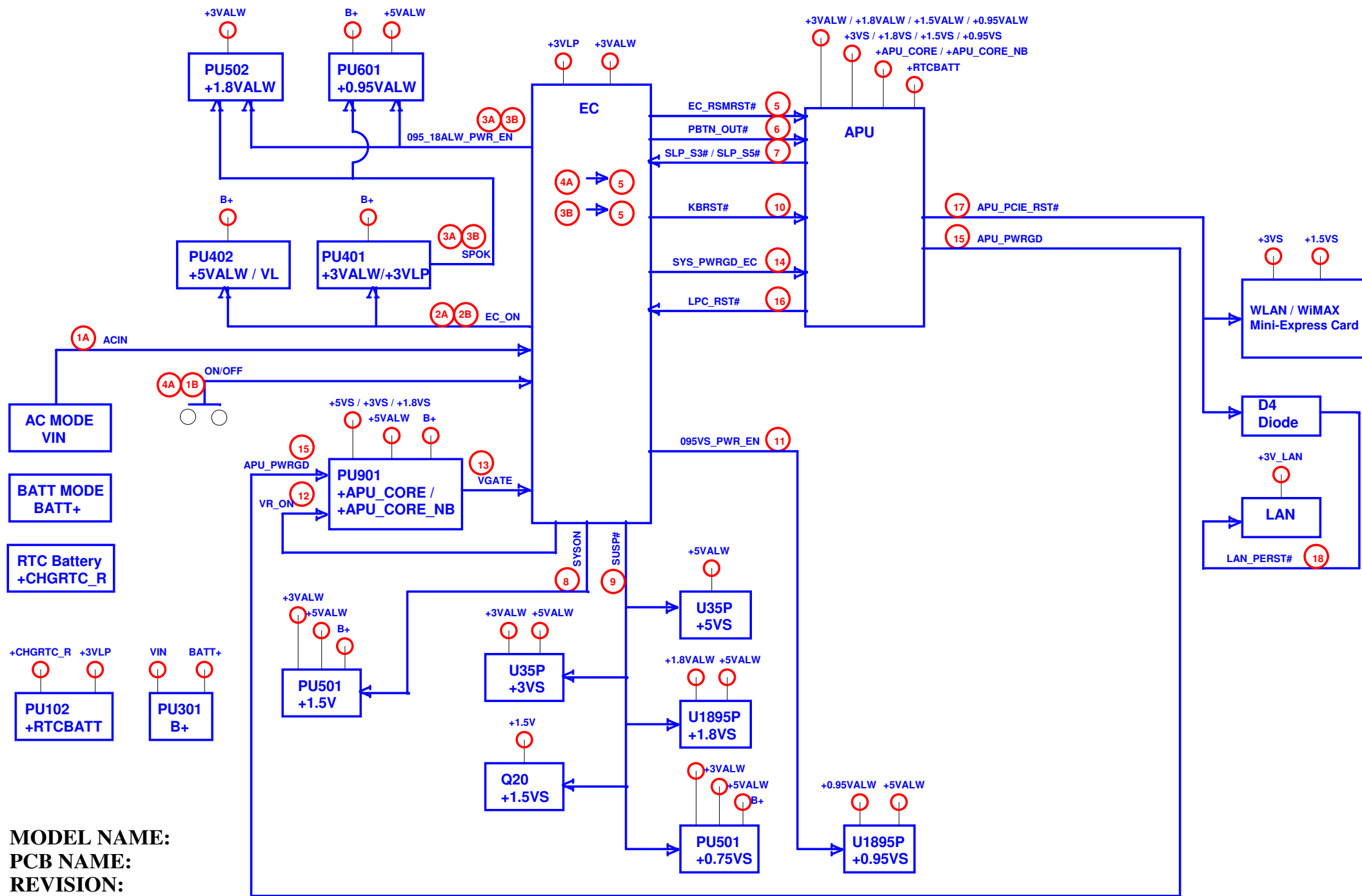
Item	Reason for change	PG#	Modify List	Date	Phase
1	For Common Intel project	20	Change R623,R765,R303 to 649ohm	03/05	PreMP
2	For Reduce BOM	05	Change R103, R104 to short-pad	03/11	PreMP
3	For Reduce BOM	11	Change R696, R695, R813 to short-pad	03/11	PreMP
4	For Reduce BOM	13	Change R550 to short-pad	03/11	PreMP
5	For Reduce BOM	18	Change R1564 to short-pad	03/11	PreMP
6	For Reduce BOM	19	Change R581 to short-pad	03/11	PreMP
7	For Reduce BOM	21	Change RA11 to short-pad	03/11	PreMP
8	For Reduce BOM	22	Change R339 to short-pad	03/11	PreMP
9	For Reduce BOM	07	Change R582 to short-pad	03/11	PreMP
10	For ESD require	20	Add C185	03/25	PreMP
11	For Module Design	12	Change R693, R697 from 10k to 4.7k	03/25	PreMP
12	For ESD require	04	Add C195	03/26	PreMP
13	For Reduce BOM	04	@ RP11	03/26	PreMP
14	For Board ID	18	@ R1562 and change R1564 to 0ohm	03/28	PreMP
15					
16					
17					

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				Custom	C38-G series Chief River Schematic ^{1.0}
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MODEL NAME:
PCB NAME:
REVISION:
DATE: 2011/11/23

COMPAL CONFIDENTIAL

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