

MODEL : 8060+Revision R03

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DRAW	DESIGN	CHECK	ISSUED

IDSEL

IDSEL	CHIP
AD11	
AD18	LAN
AD19	PCMCIA
AD17	MINIPCI
AD21	USB2.0

BUS MASTER

REQ/GNT	CHIP
-REQ0/-GNT0	
-REQ1/-GNT1	PCMCIA
-REQ2/-GNT2	LAN
-REQ3/-GNT3	USB2.0
-REQ4/-GNT4	MINIPCI

PCIINT

PCIINT	CHIP
INTA	PCMCIA/MAP17/USB2.0
INTB	MINIPCI/USB2.0
INTC	PCMCIA/1394/USB2.0
INTD	LAN
INTE	MINIPCI/OZ165

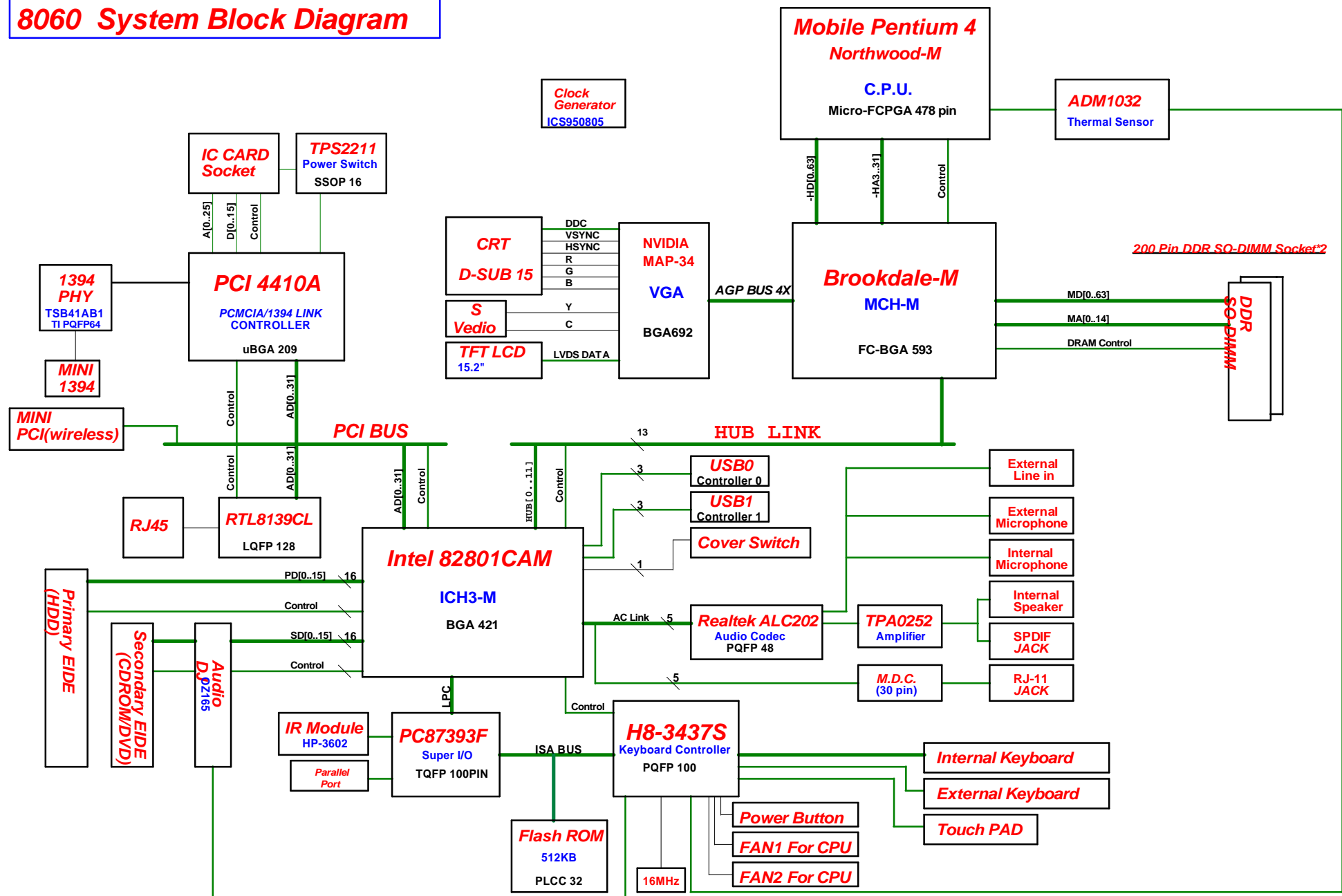
1		COMP
2		GBD
3		IN-1
4		IN-2
5		POWER
6		IN-2
7		GBD
8		SOLDER

POWER STATES

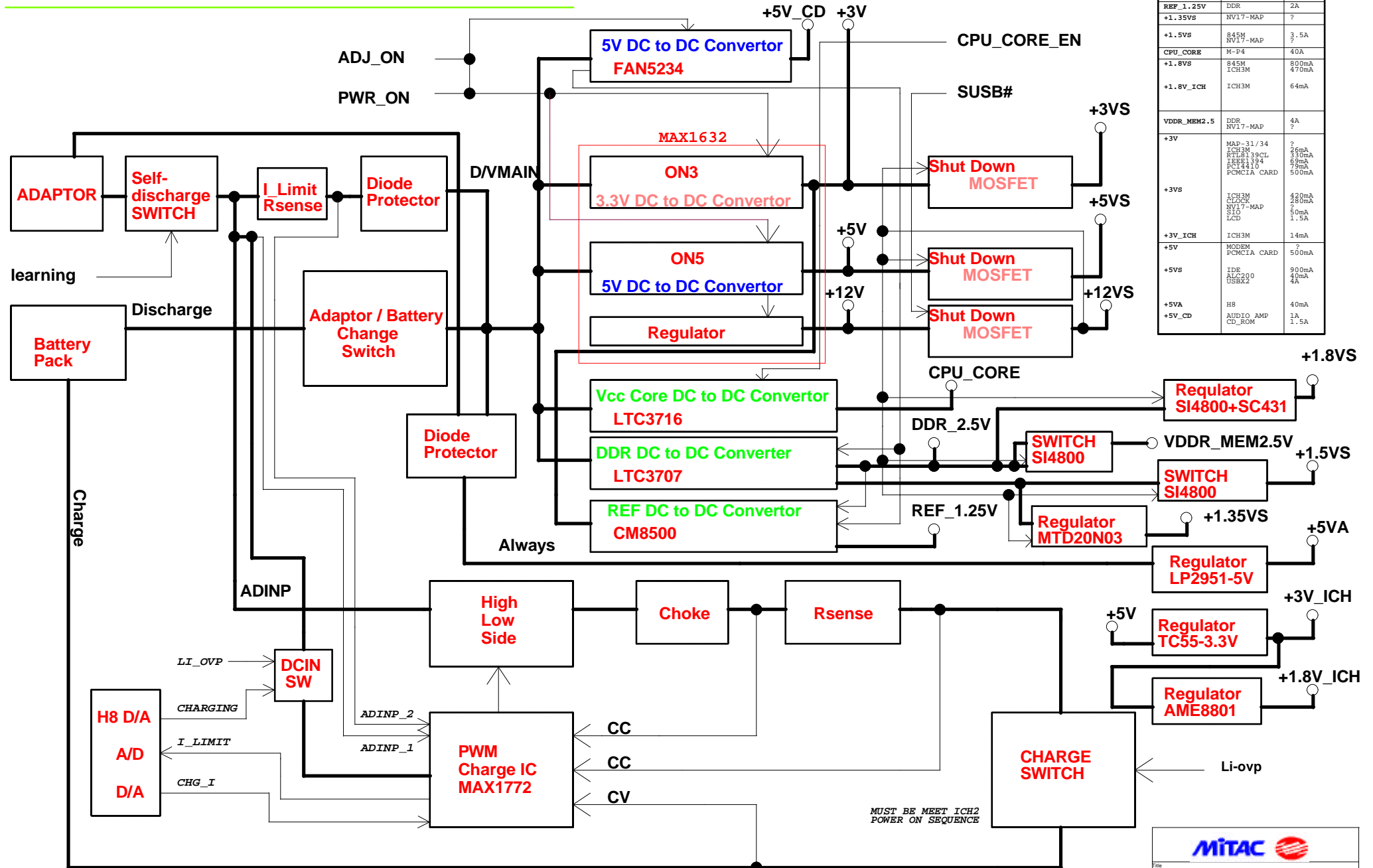
STATE SIGNAL	VOTAGE	S0	S1	S3	S4	S5
-SUSA	-	HIGH	LOW	LOW	LOW	LOW
-SUBS	-	HIGH	HIGH	LOW	LOW	LOW
-SUSC	-	HIGH	HIGH	HIGH	LOW	LOW
ADP	+19V	O	O	O	O	O
BATTERY	+12V	O	O	O	O	O
RTC_VCC	+3.3V	O	O	O	O	O
CPU_CORE	+1.75V	O	O	O	X	X
+1.35VS	+1.35V	O	O	X	X	X
+1.8VS	+1.8V	O	O	X	X	X
+1.8V_ICH	+1.8V	O	O	O	O	O
VDDR_MEM2.5	+2.5V	O	O	O	X	X
+3VS	+3.3V	O	O	X	X	X
+3V	+3.3V	O	O	O	X	X
+3V_ICH	+3.3V	O	O	O	O	O
+5VS	+5V	O	O	X	X	X
+5V	+5V	O	O	O	X	X
+5VA	+5V	O	O	O	O	O
+12VS	+12V	O	O	X	X	X
+12V	+12V	O	O	O	X	X
+5V_CD	+5V	O	O	O	O	O/X byADJ_BTN



8060 System Block Diagram



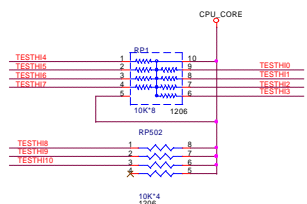
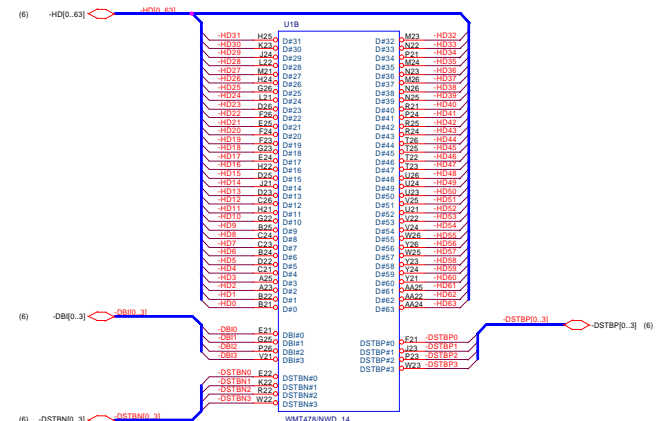
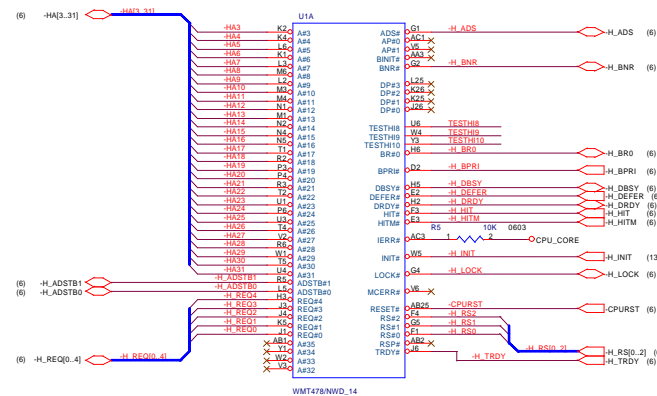
BLOCK DIAGRAM OF THE 8060+



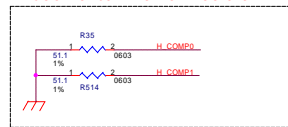
* OPTION(NO LINK)

RTC	ICH3M	4uA
REF_1.25V	DDR	2A
+1.35VS	NV17-MAP	?
+1.5VS	845M NV17-MAP	?
CPU_CORE	M-P4	40A
+1.8VS	845M ICH3M	800mA
+1.8V_ICH	ICH3M	470mA
VDDR_MEM2.5	DDR NV17-MAP	4A
+3V	MAP-31/34 ICH3M RT18139CL 188P1394 PCT4410 PCMCIA CARD	?
+3VS	ICH3M GFPCF NV17-MAP S10 LCD	?
+3V_ICH	ICH3M	14mA
+5V	MODEM PCMCIA CARD	500mA
+5VS	IDE AL200 USBX2	900mA
+5VA	H8	40mA
+5V_CD	AUDIO AMP CD_ROM	1A
		1.5A

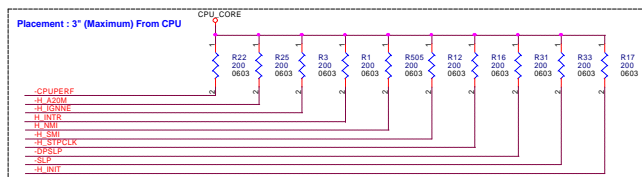
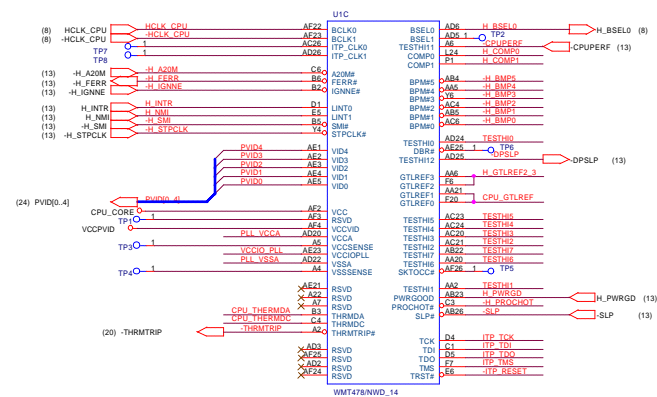
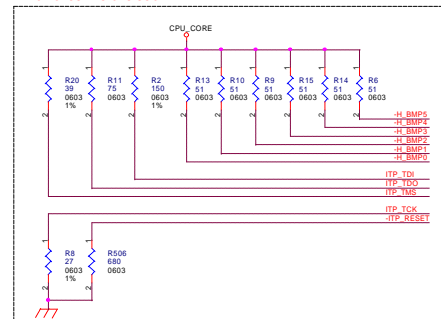
MOBILE P4



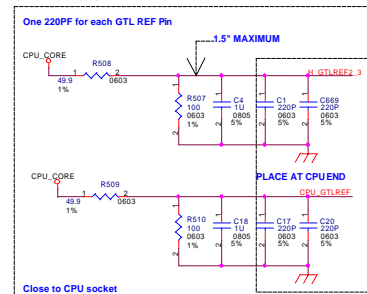
PRECISION FSB COMPENSATION RESISTORS



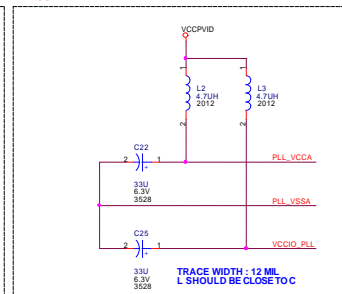
PLACE CLOSE TO CPU SOCKET



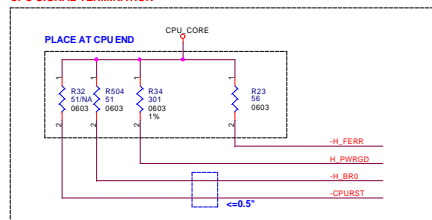
GTL Reference CKT



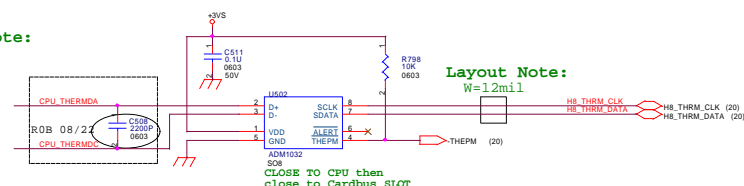
PLL SUPPLY FILTER



CPU SIGNAL TERMINATION

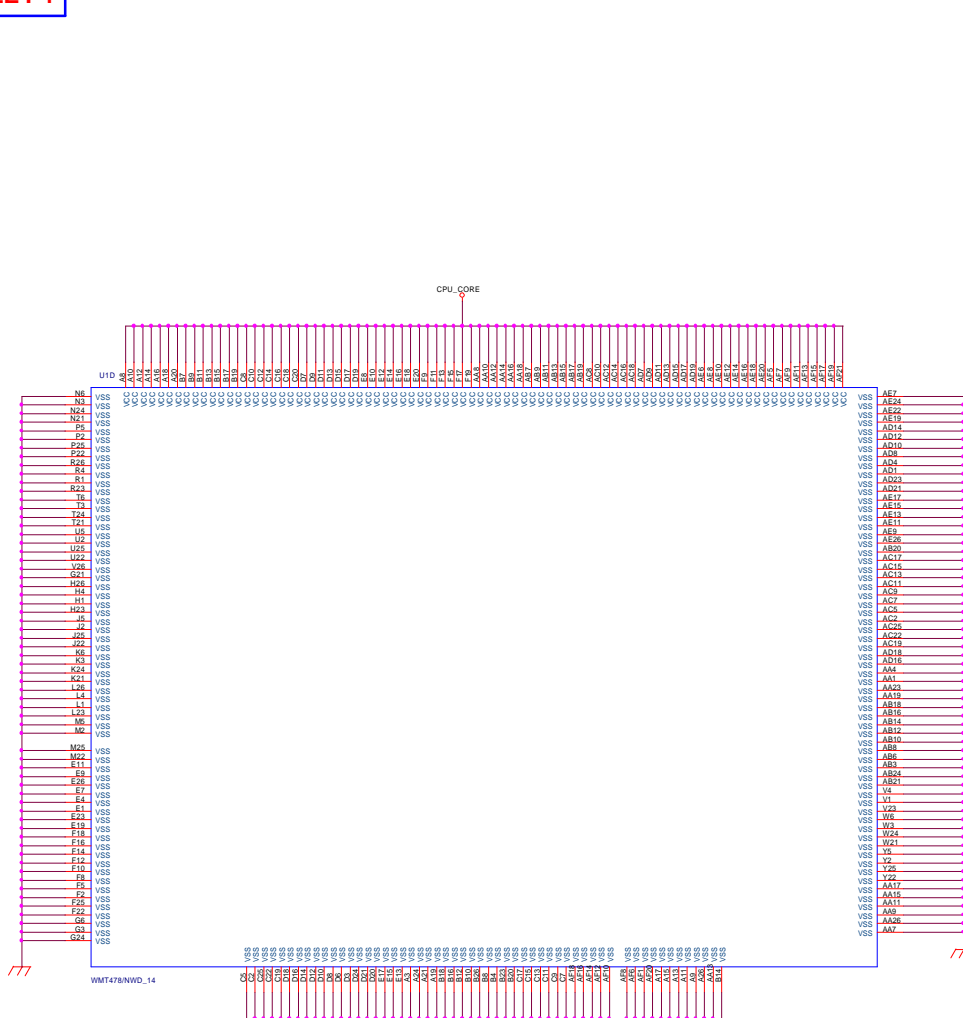


Layout Note:
(平行且等長)
as short as possible

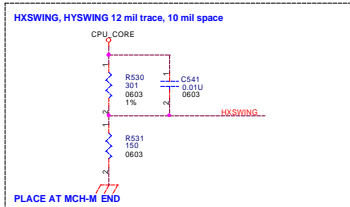
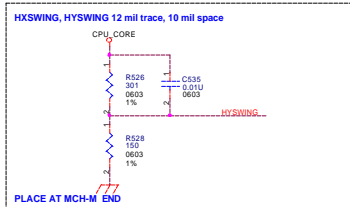


Layout Note:
W=12mil

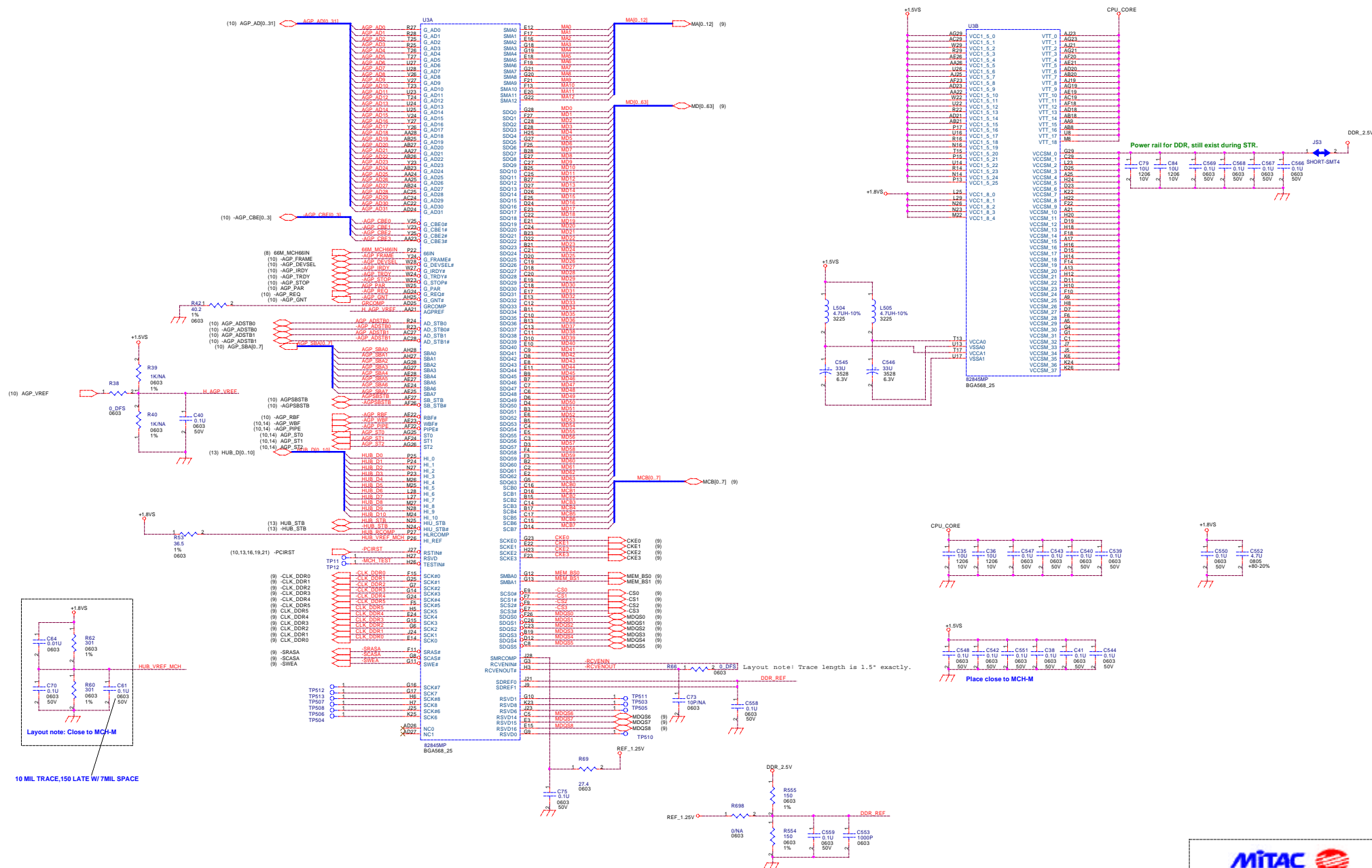
MOBILE P4



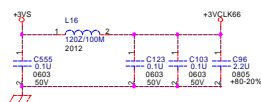
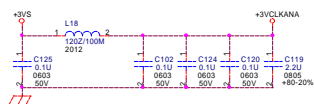
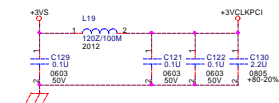
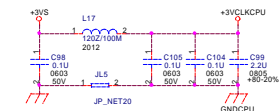
MEMORY CONTROL HUB



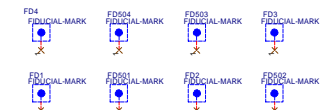
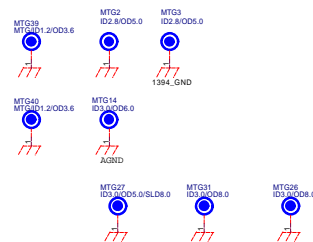
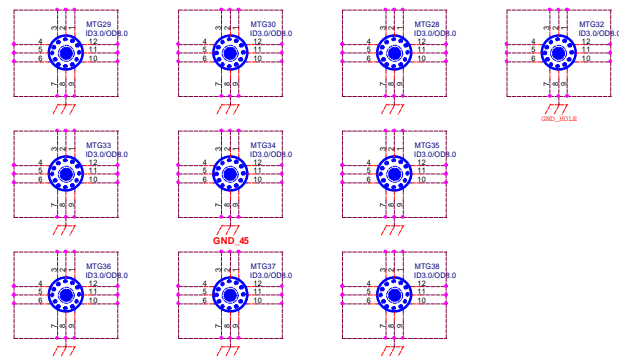
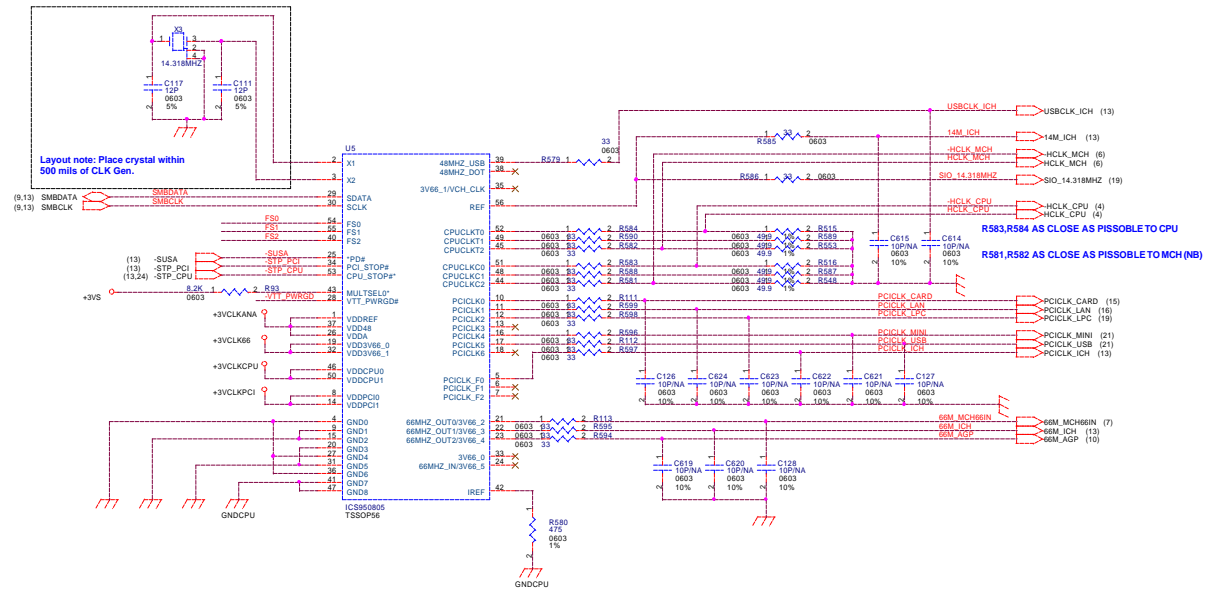
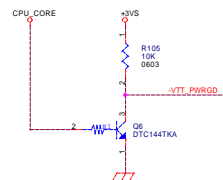
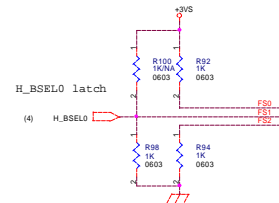
MEMORY CONTROL HUB



CLOCK GENERATOR

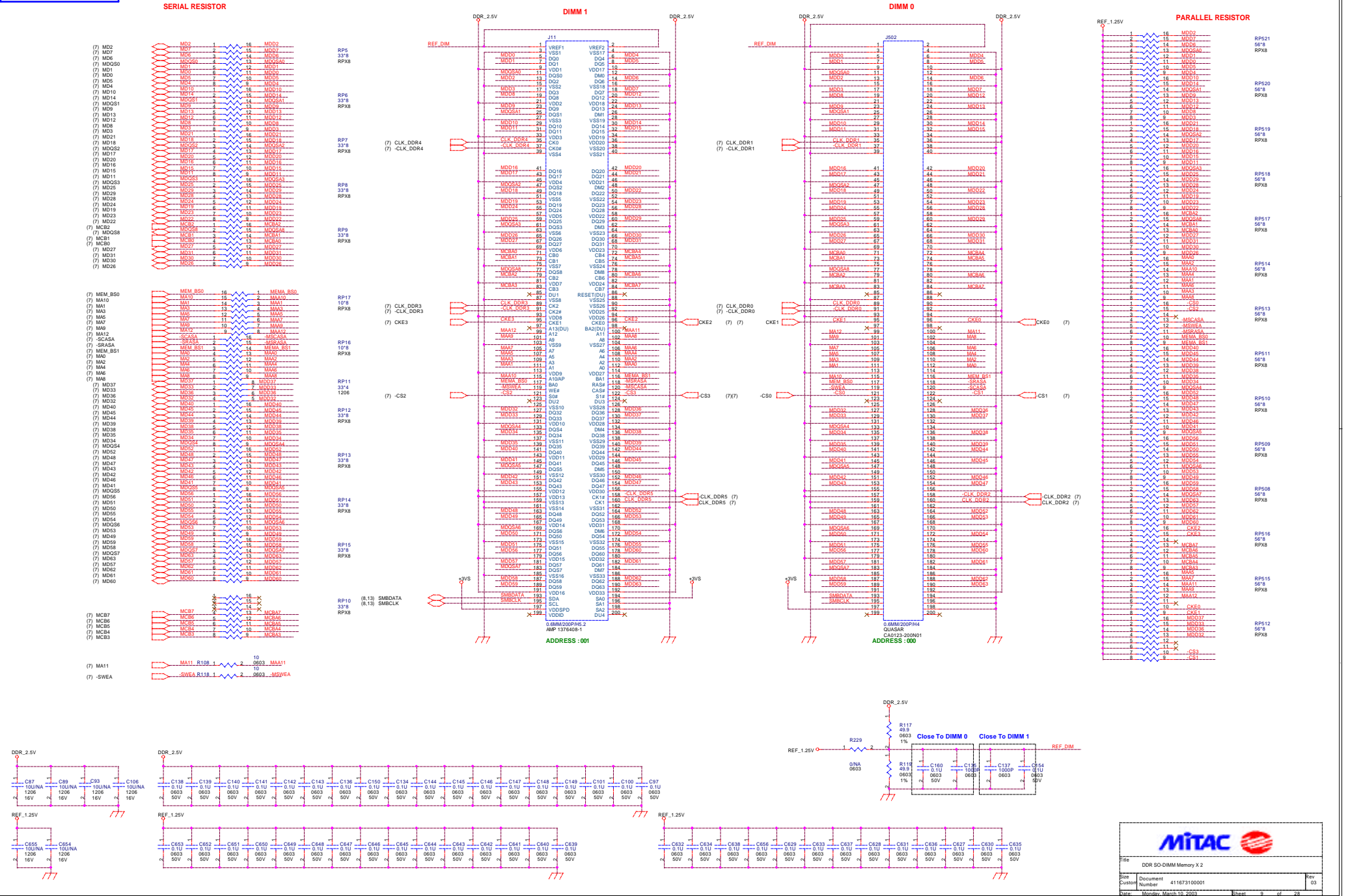


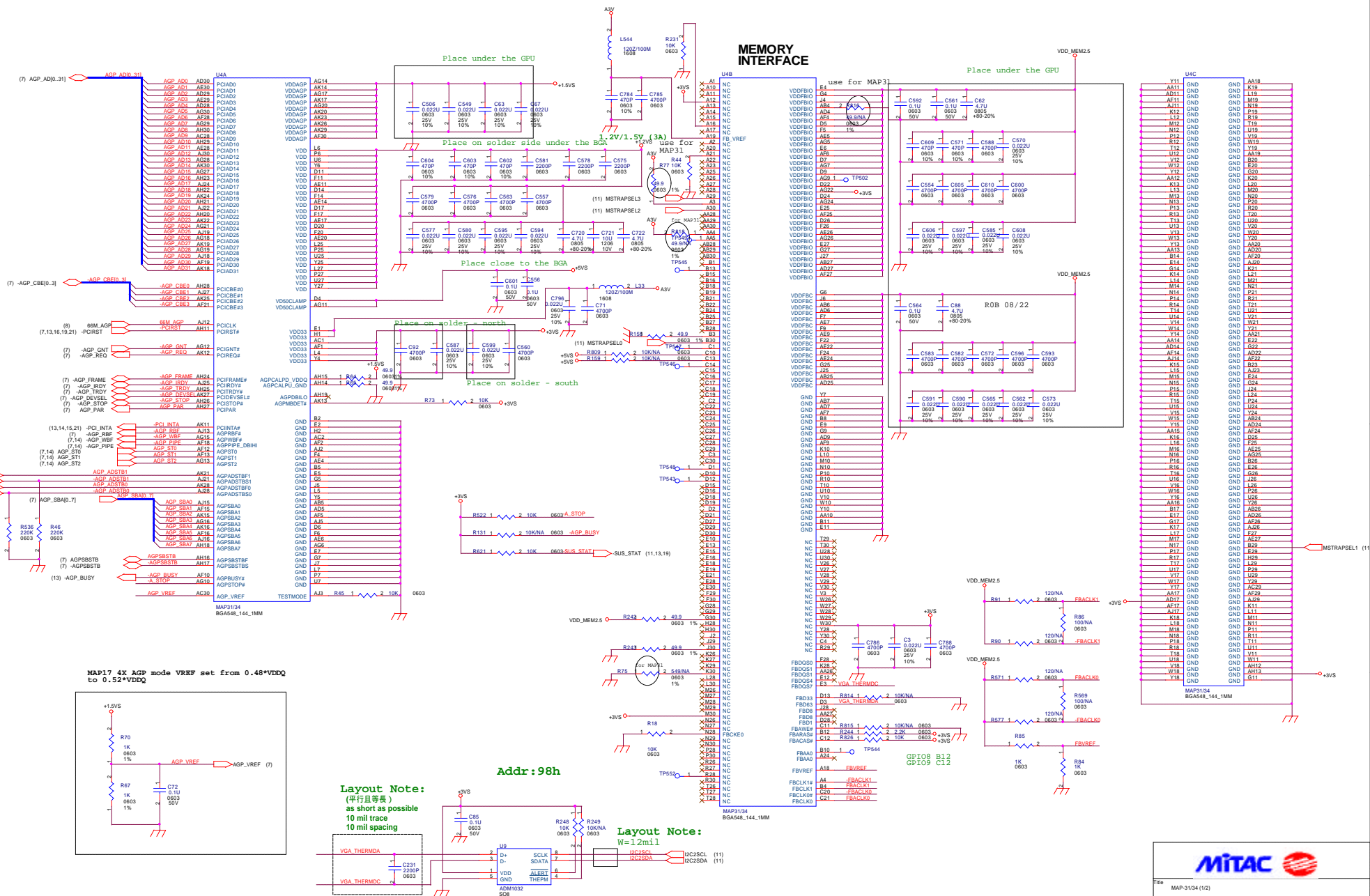
FS2	FS1	FS0	CPUCLK
0	0	1	100MHZ
0	1	1	133MHZ



DDR SO-DIMM

DDR SO-DIMM Module

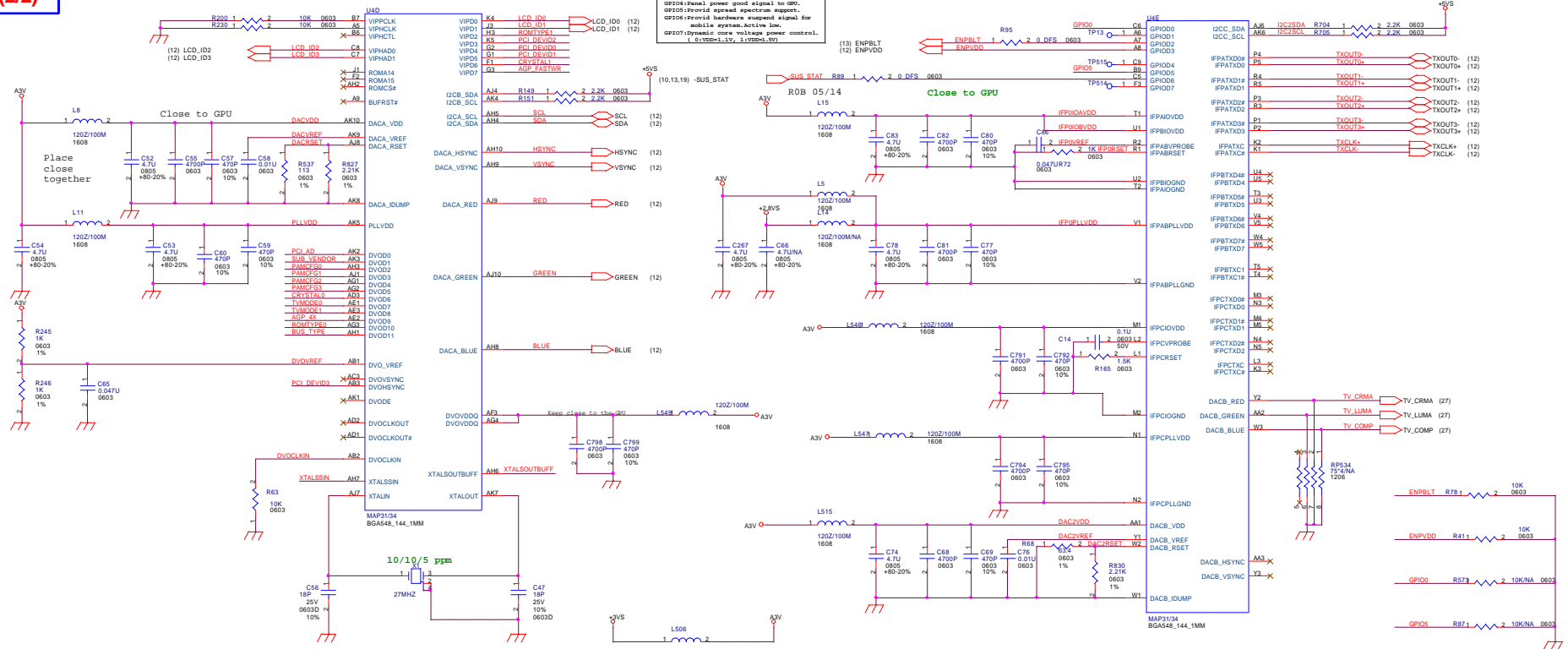




MAP-31/34(2/2)

Check!

GP100: General purpose I/O
 GP101: General purpose I/O
 GP102: Provide backlight enable.
 GP103: Provide panel power enable.
 GP104: Panel power good signal to GPU.
 GP105: Provide spread spectrum support.
 GP106: Provide hardware suspend signal for mobile system. Active low.
 GP107: Dynamic core voltage power control. (0: VDD=1.2V, 1: VDD=1.0V)



T12C2SDA/STOP Fout

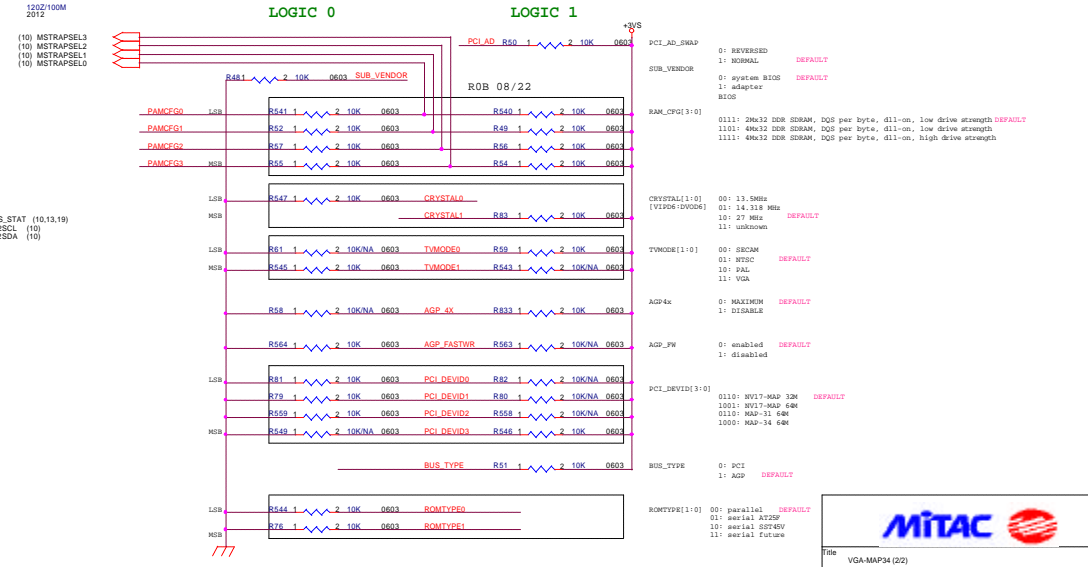
0	Enable
1	Disable

R0 R1 S0 S1 Fout

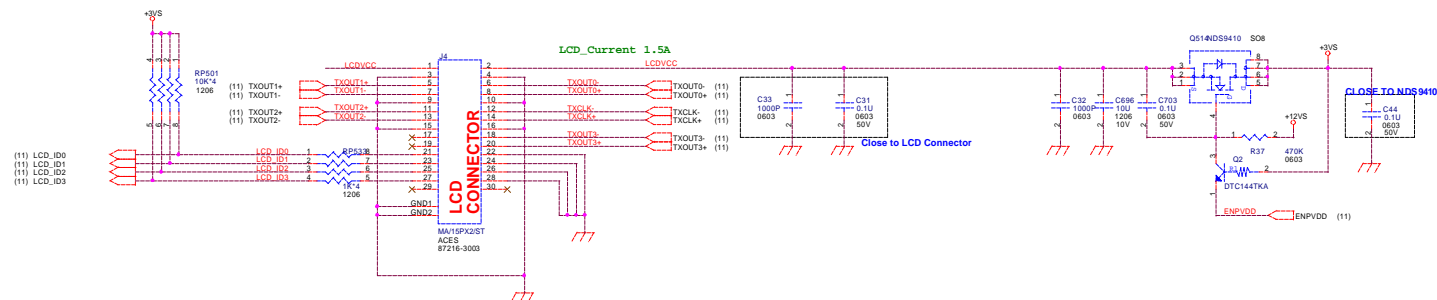
X	X	0	0	Power down mode
0	1	0	1	1x Fin

Power down mode :

SO	S1	S2	S3	Fout
0	0	0	1	Factory Test
0	0	1	1	Hi-z
0	0	0	0	0
0	0	1	0	1



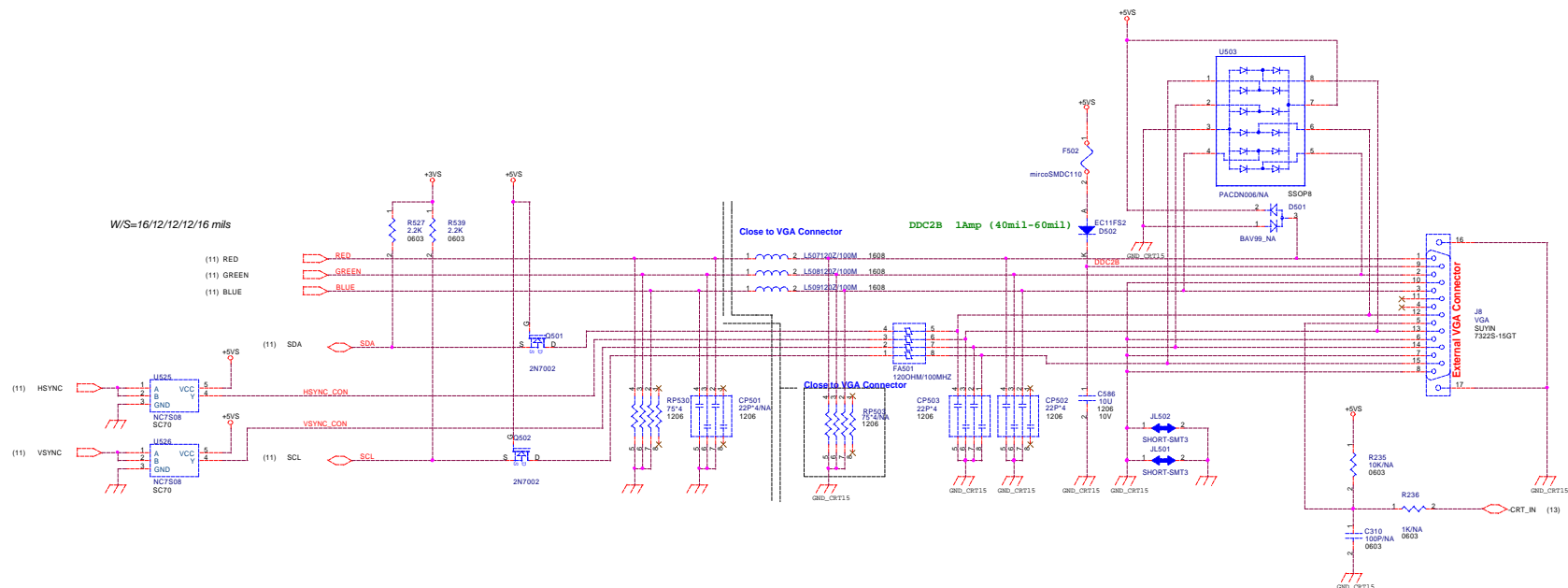
LCD & CRT INTERFACE



Layout Note: S/W/W/S=12/6/6/12 mls
as short as possible
四組各自平行走線等長

LCD ID Select Table

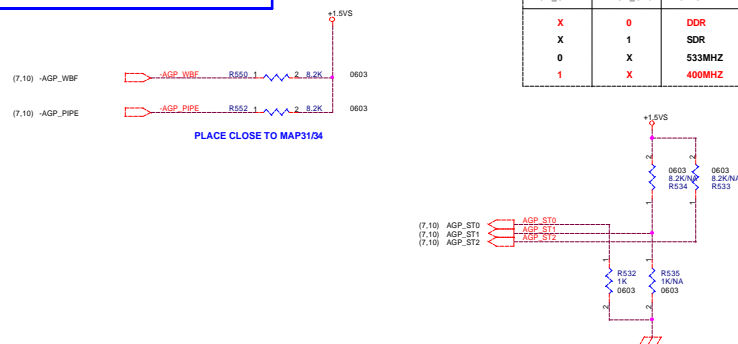
Display	LCD_ID3	LCD_ID2	LCD_ID1	LCD_ID0
LTN152W3 & B152EW01	0	0	0	1



(15 16 31) AD(0 31)

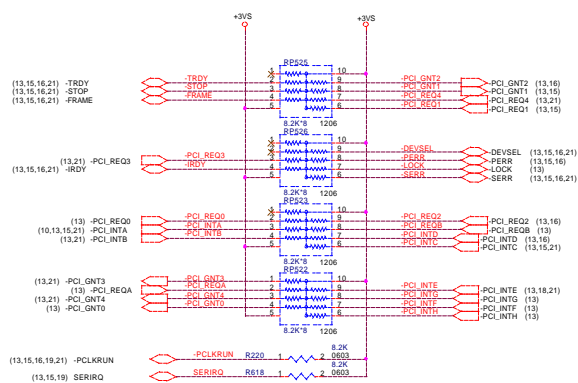


AGP BUS PULL UP/DOWN

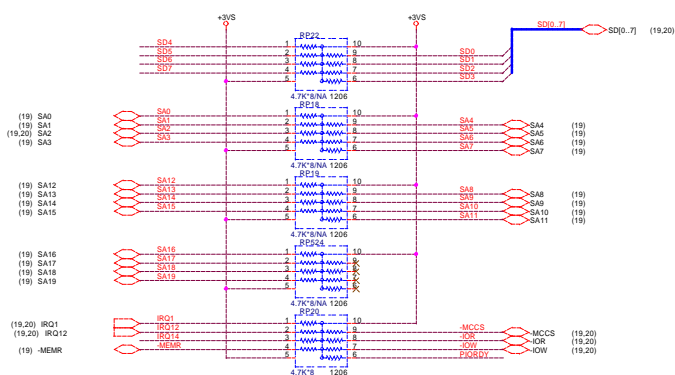


AGP_ST1	AGP_ST0	MCH STRAP
X	0	DDR
X	1	SDR
0	X	533MHZ
1	X	400MHZ

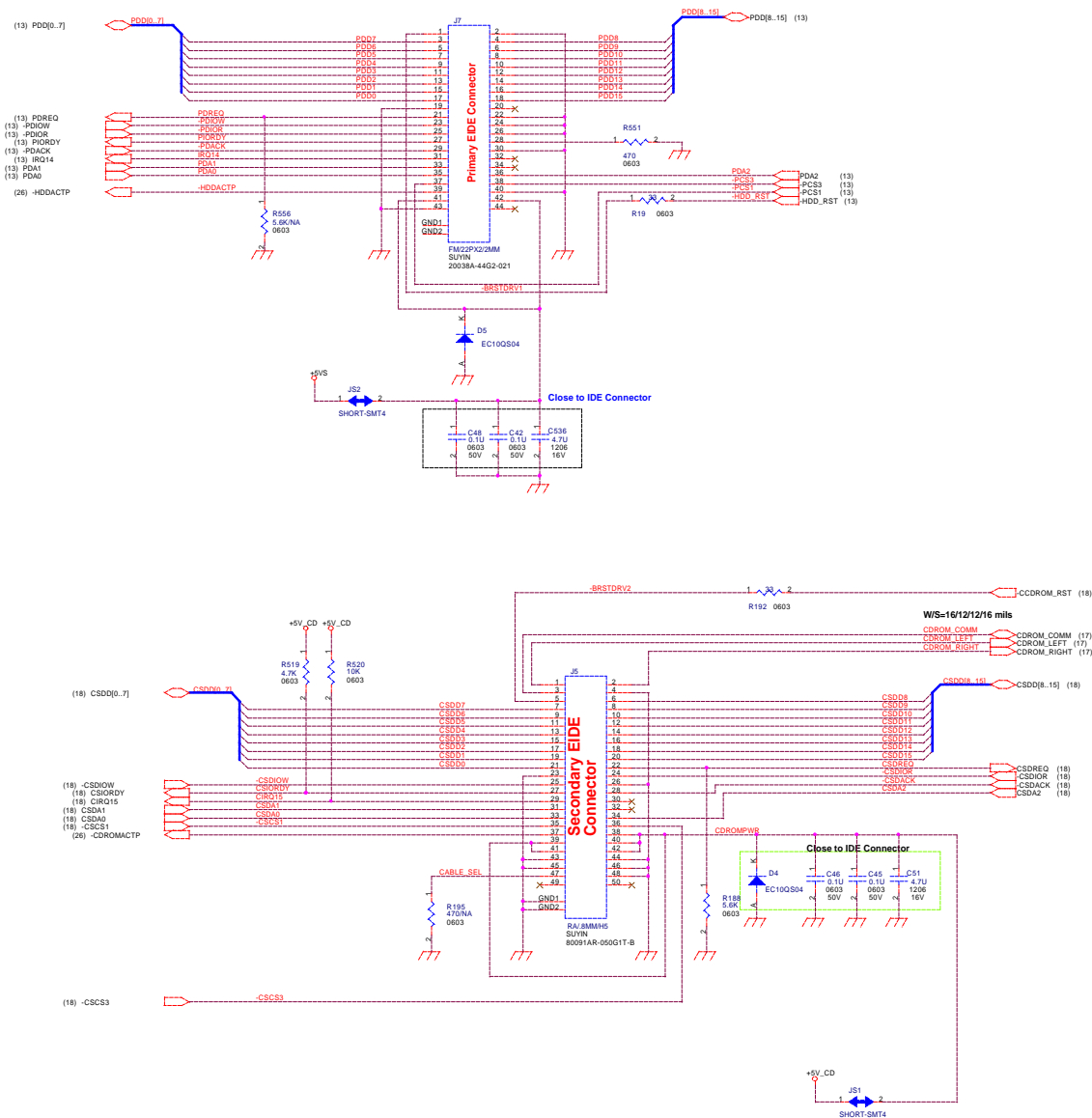
PCI BUS PULL UP/DOWN



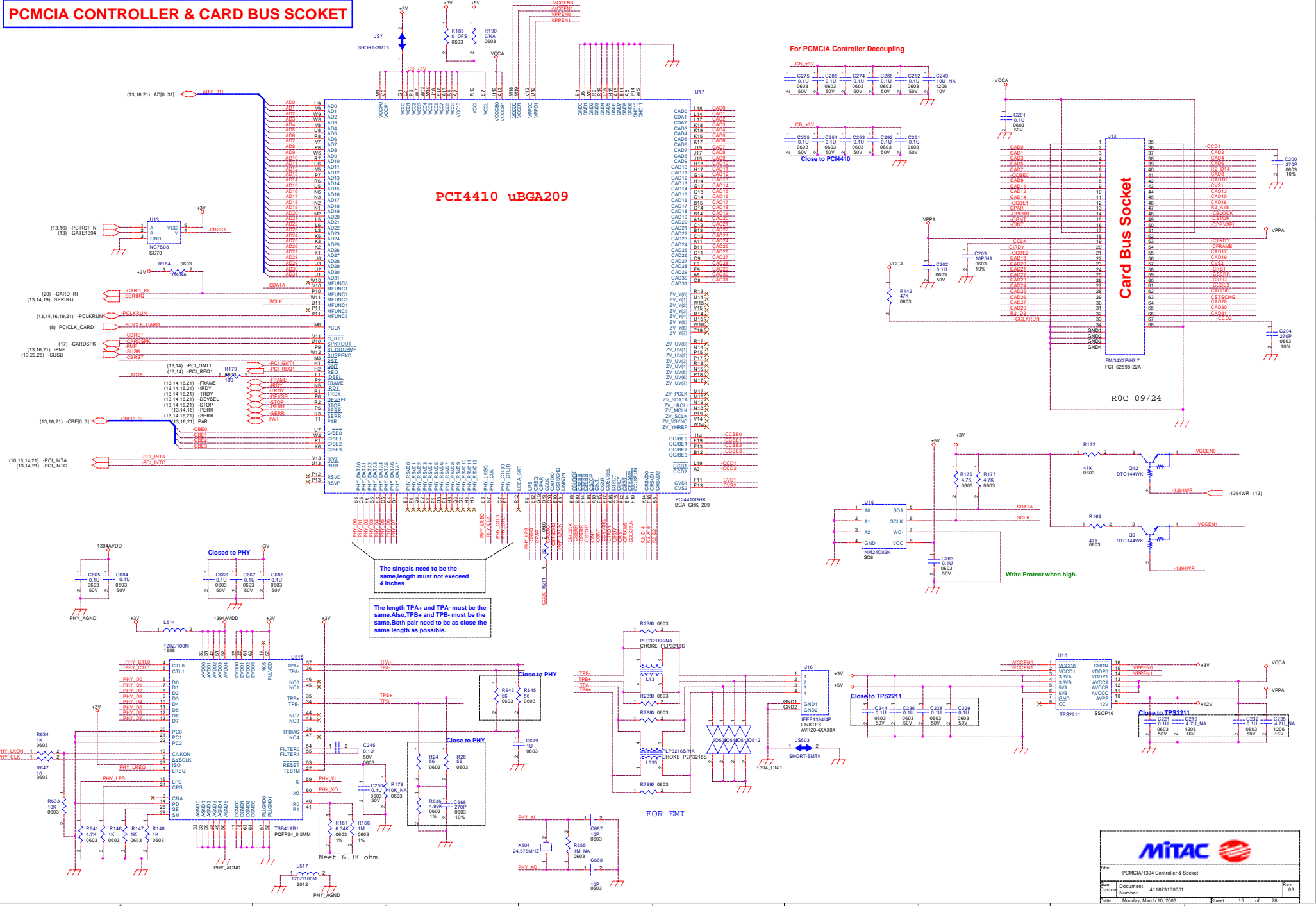
ISA BUS PULL UP/DOWN



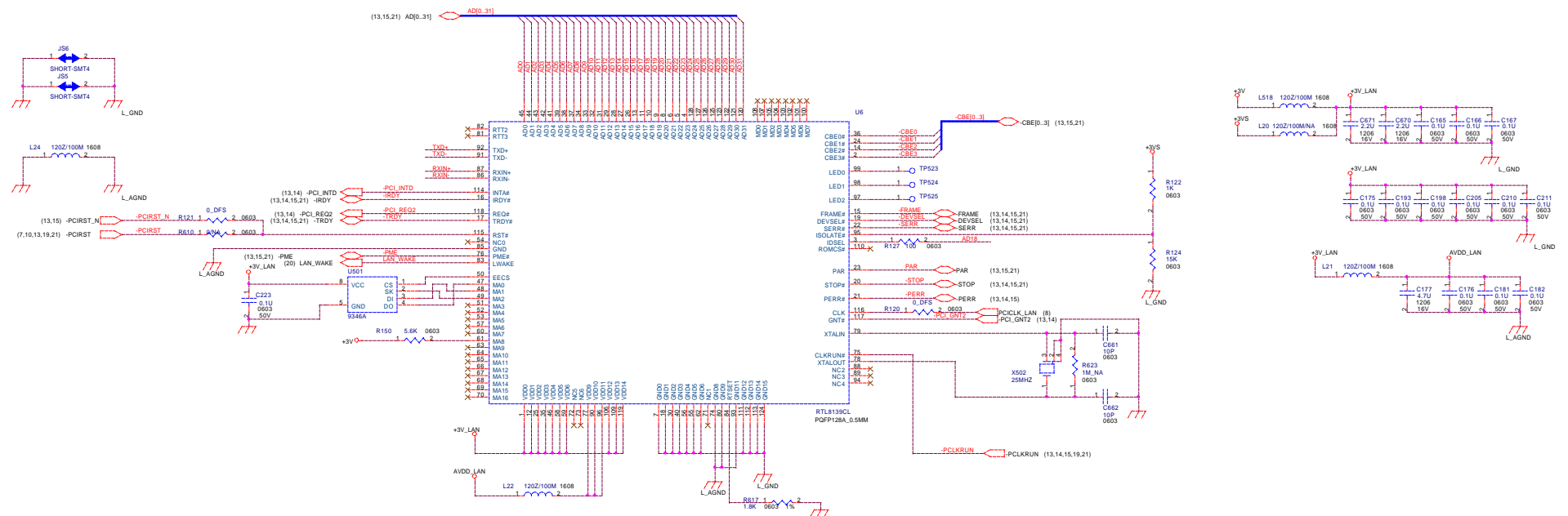
ENHANCED IDE



PCMCIA CONTROLLER & CARD BUS SOCKET

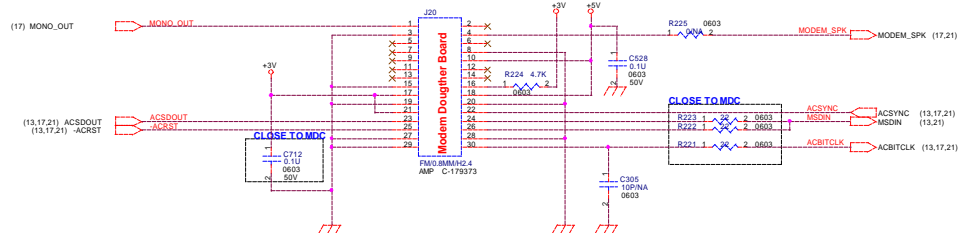
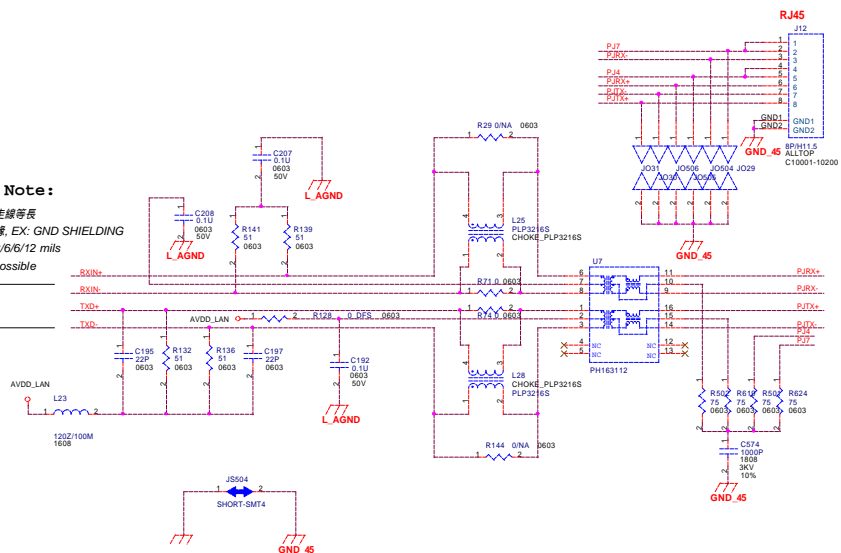


LAN CONTROLLER



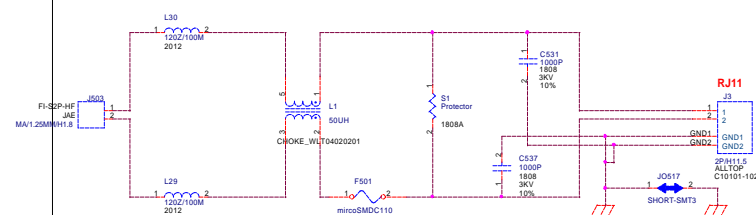
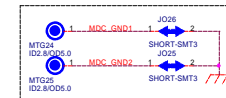
Layout Note:

二組各自平行走線等長
二組中間須絕緣, EX: GND SHIELDING
S/W/W/S=12/6/6/12 mils
as short as possible

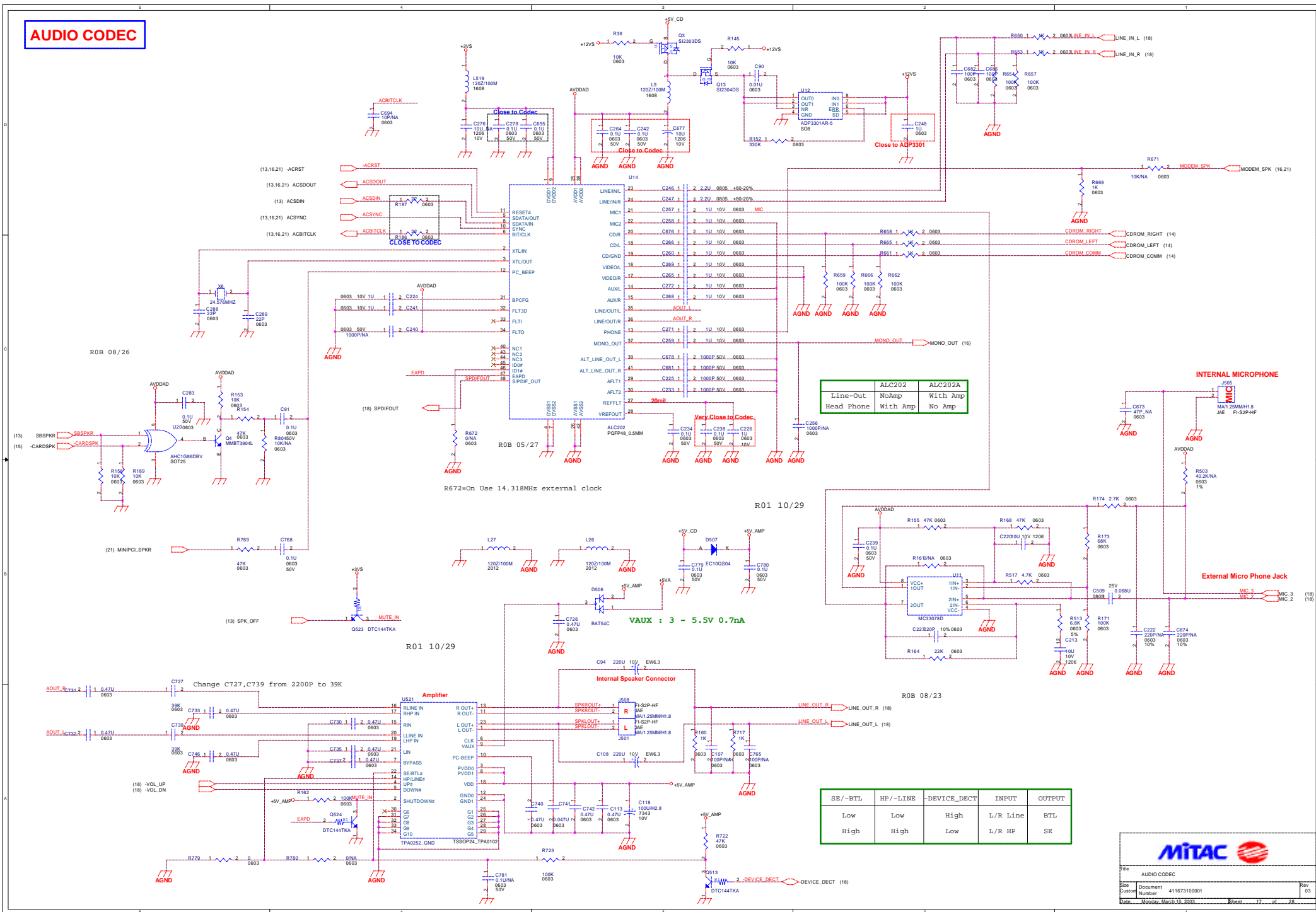


	HIGH	LOW
PIN 16	AUDIO CODEC ON MOTHER BD	AUDIO CODEC ON DAUGHTER BOARD

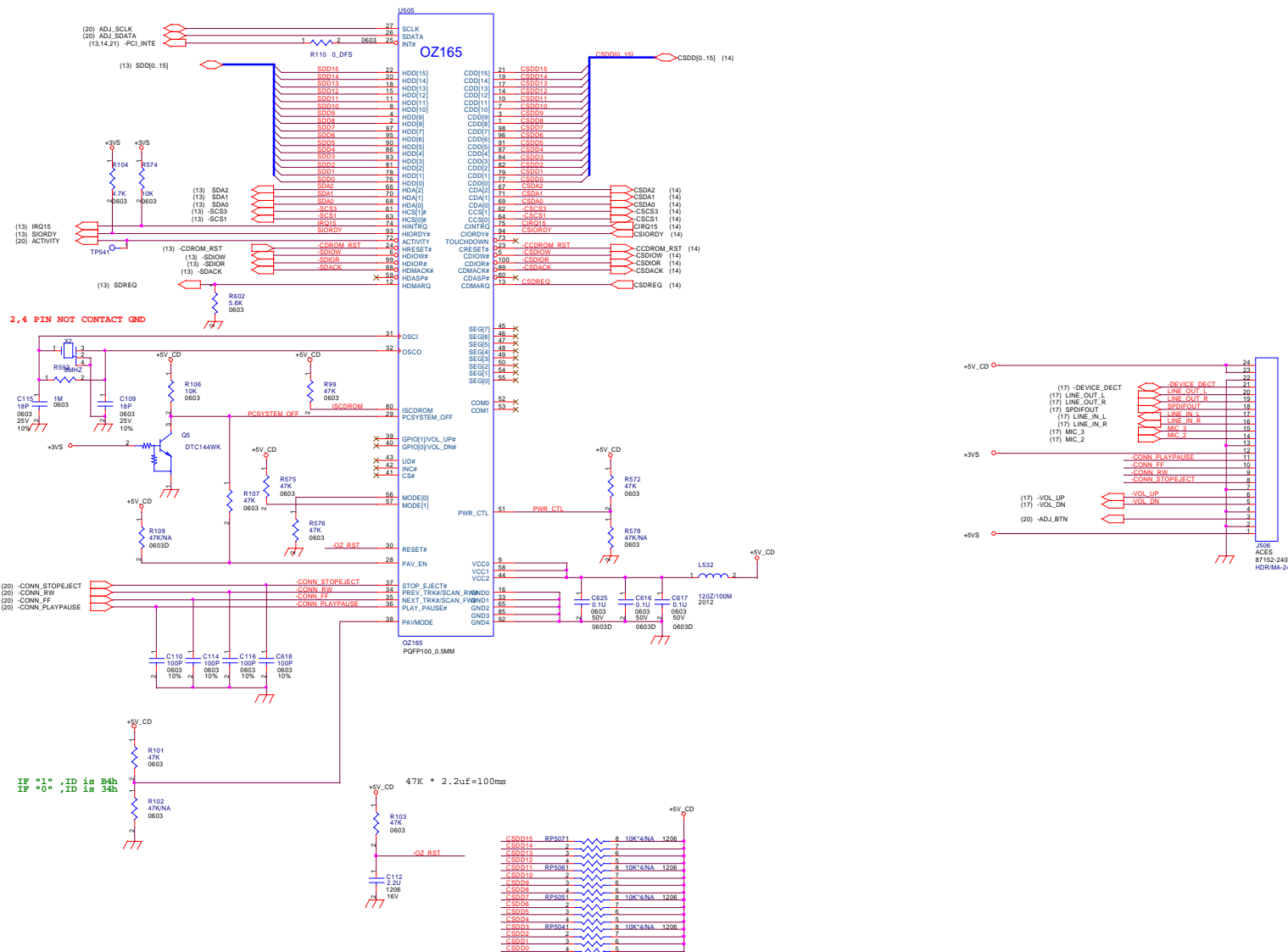
MDC SCREW HOLE



AUDIO CODEC



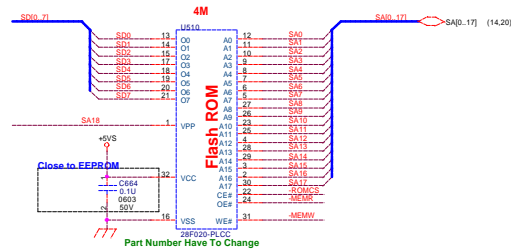
AUDIO DJ



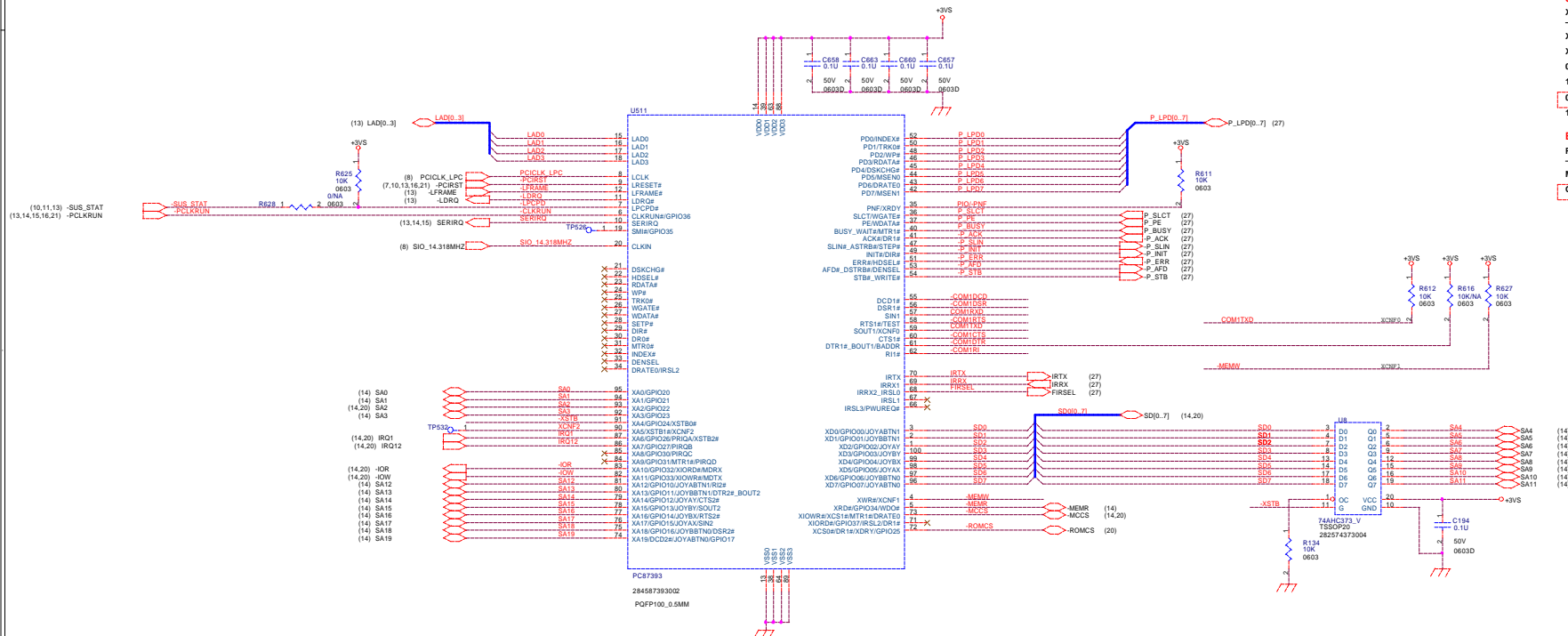
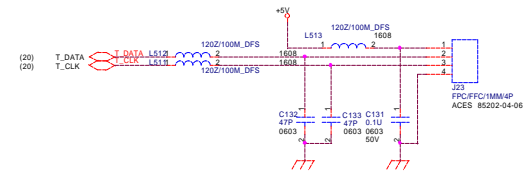
Mode	PAV_EN	ISCDROM	PCSYSTEM_OFF
CDPlayer(system off)	1	1	1
Direct(system on)	X	X	0
pass through(system on)	X	X	0
no CD-ROM	1	0	1
Power_off	0	X	1

BIOS & T/P & SUPER I/O CHIP

BIOS ROM

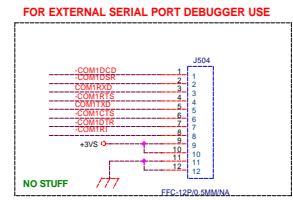


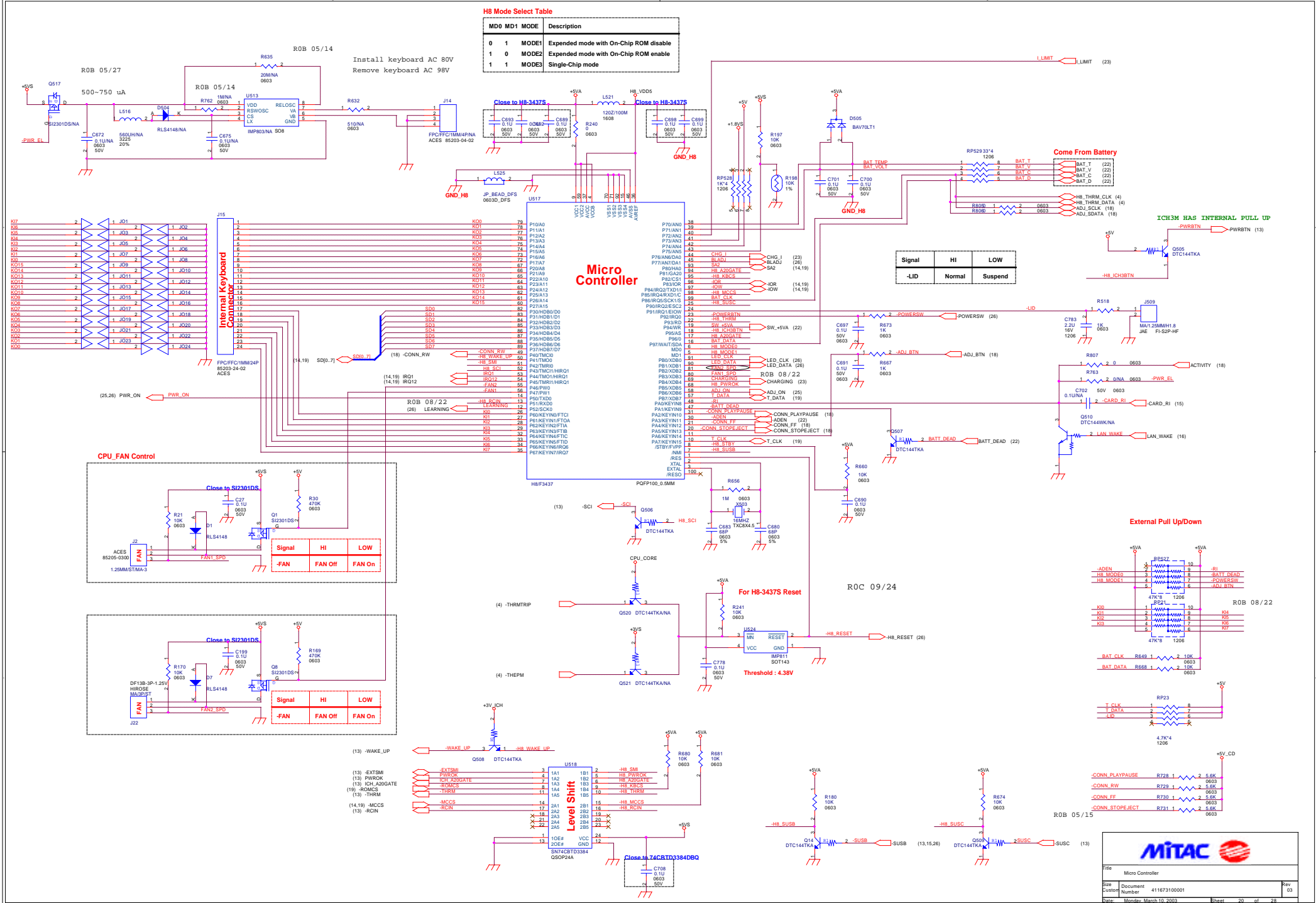
TOUCH_PAD

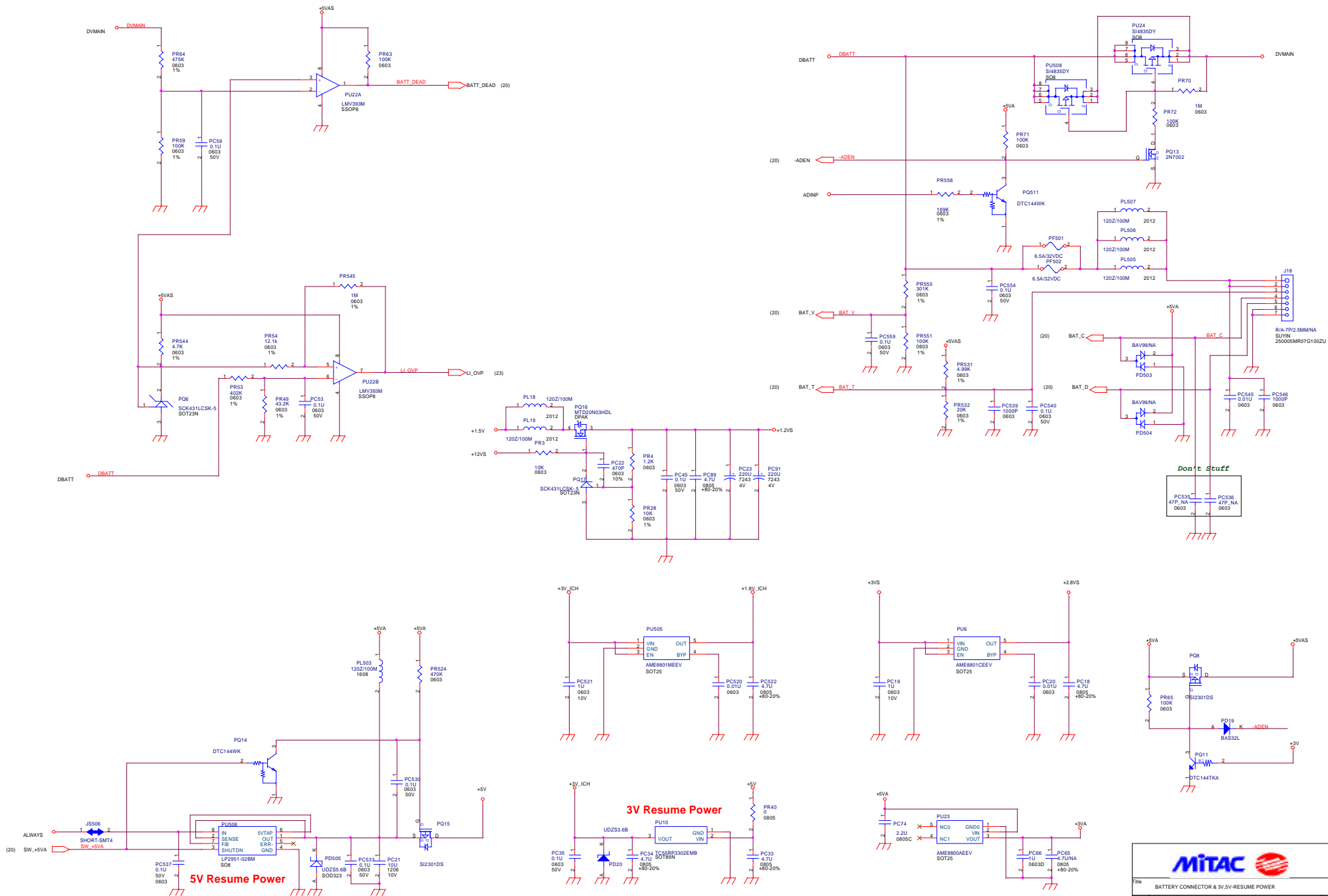


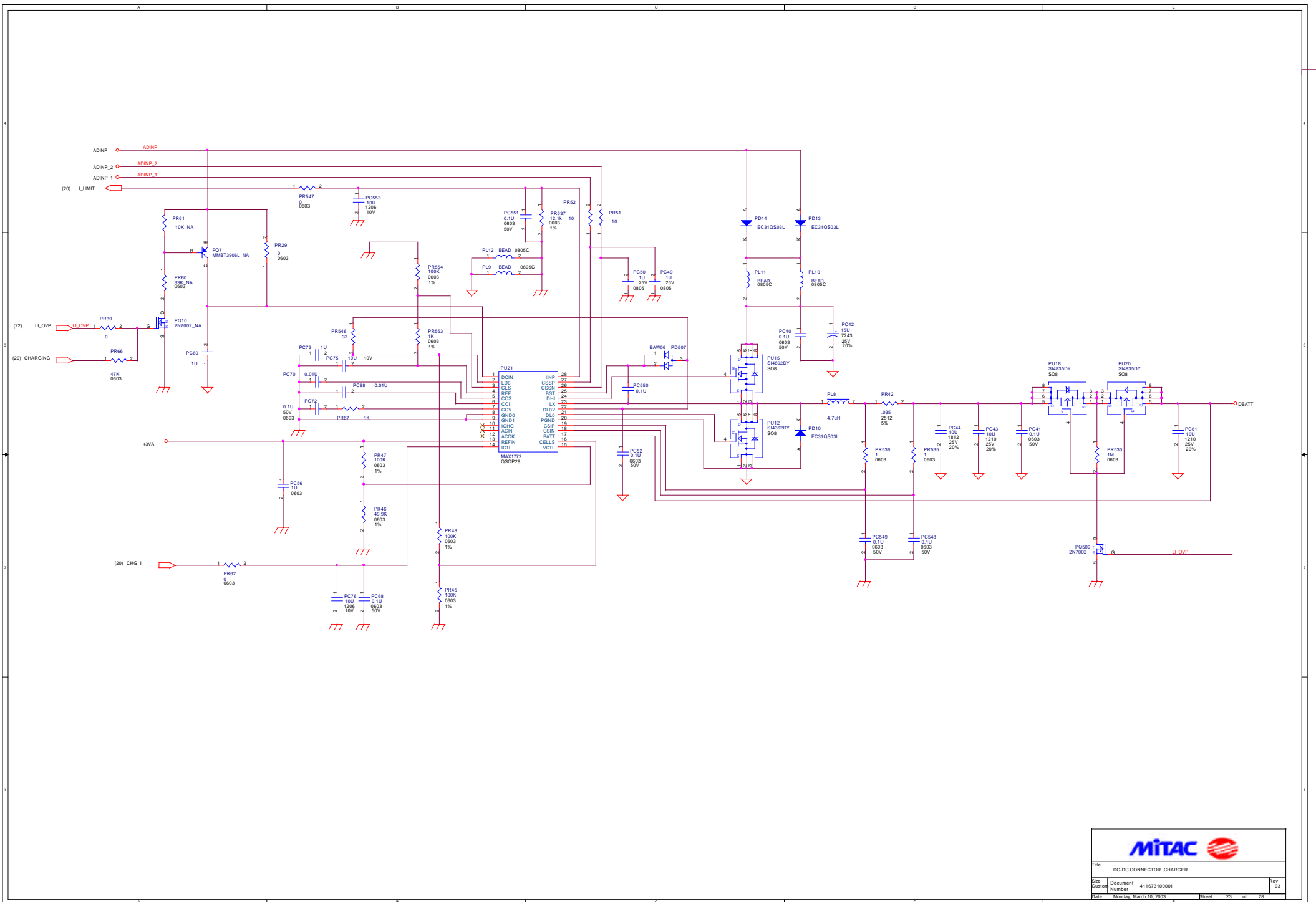
STRAP OPTION				FUNCTIONALITY
XCNF2	XCNF1	XCNF0		
X	0	0		NO BIOS
X	0	1		NORMAL MODE , XRDY DISABLE
0	1	0		LATCH MODE , XA12-19, XRDY ENABLE
1	1	0		LATCH MODE , GPIO 10-17, XRDY ENABLE
0	1	1		LATCH MODE , XA12-19, XRDY DISABLE
1	1	1		LATCH MODE , GPIO 10-17, XRDY DISABLE

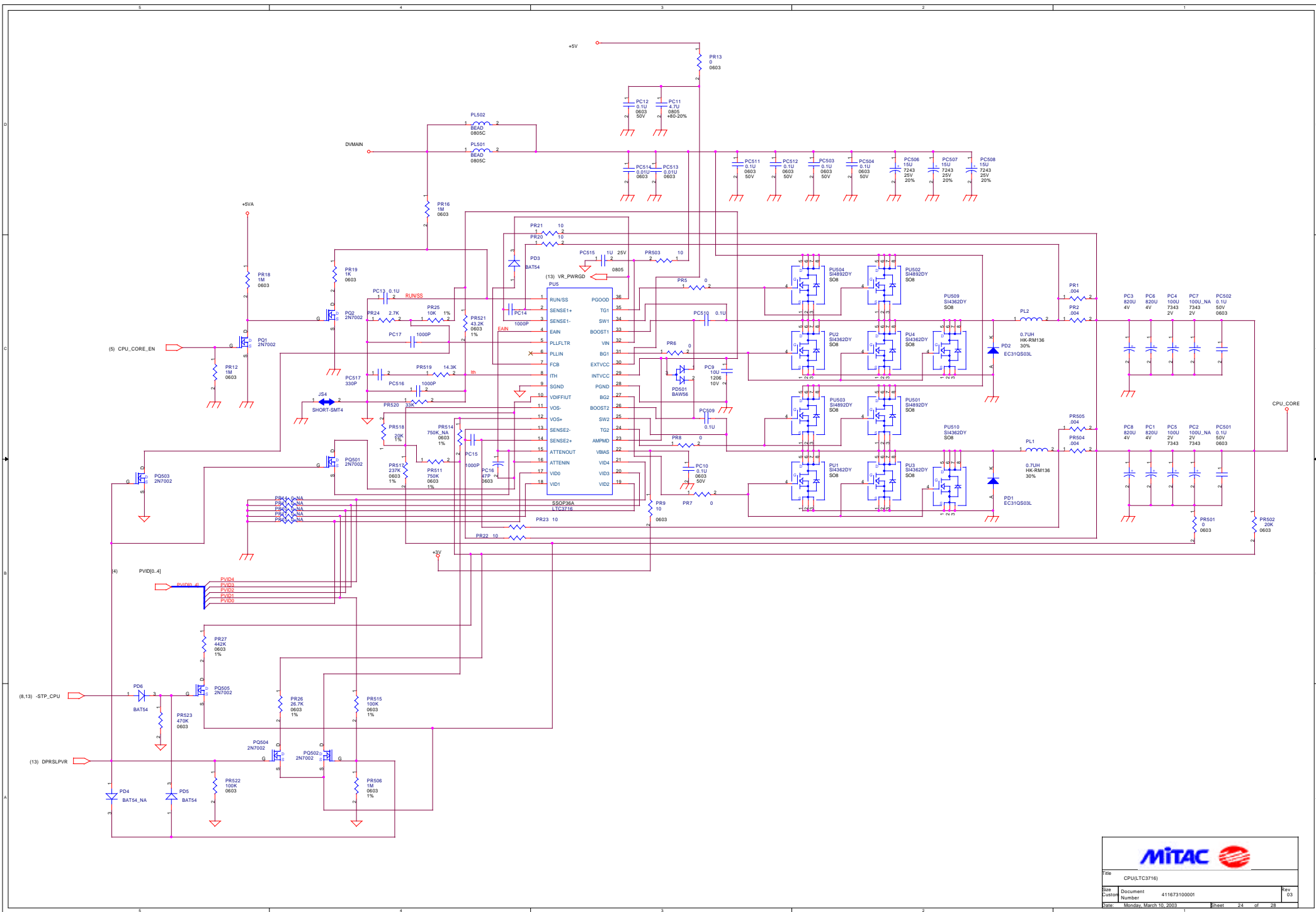
BASE ADDRESS SELECT			
R643	INDEX REGISTER	DATA REGISTER	
MOUNTED	4EH	4FH	
OPEN	2EH	2FH	



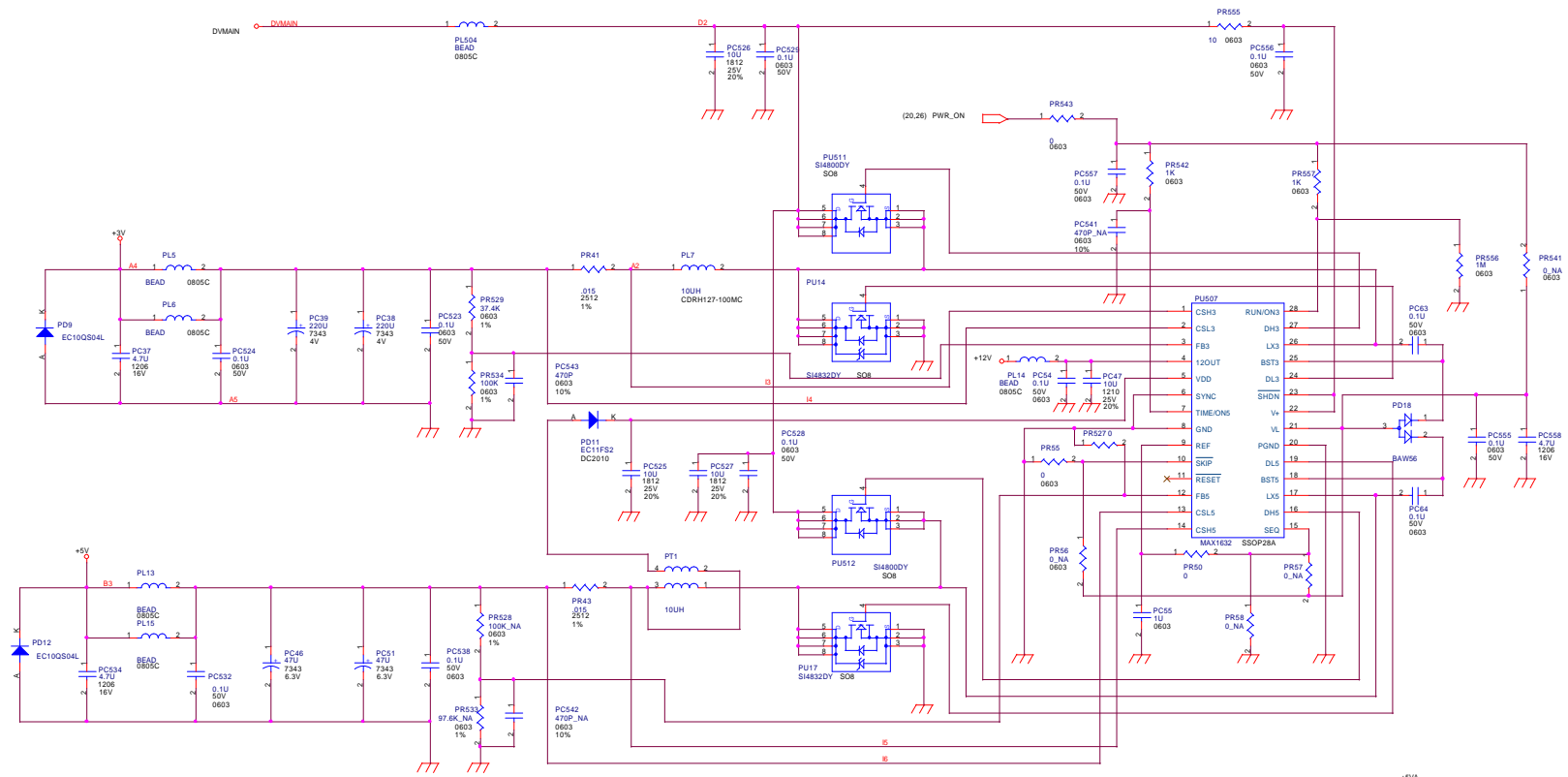




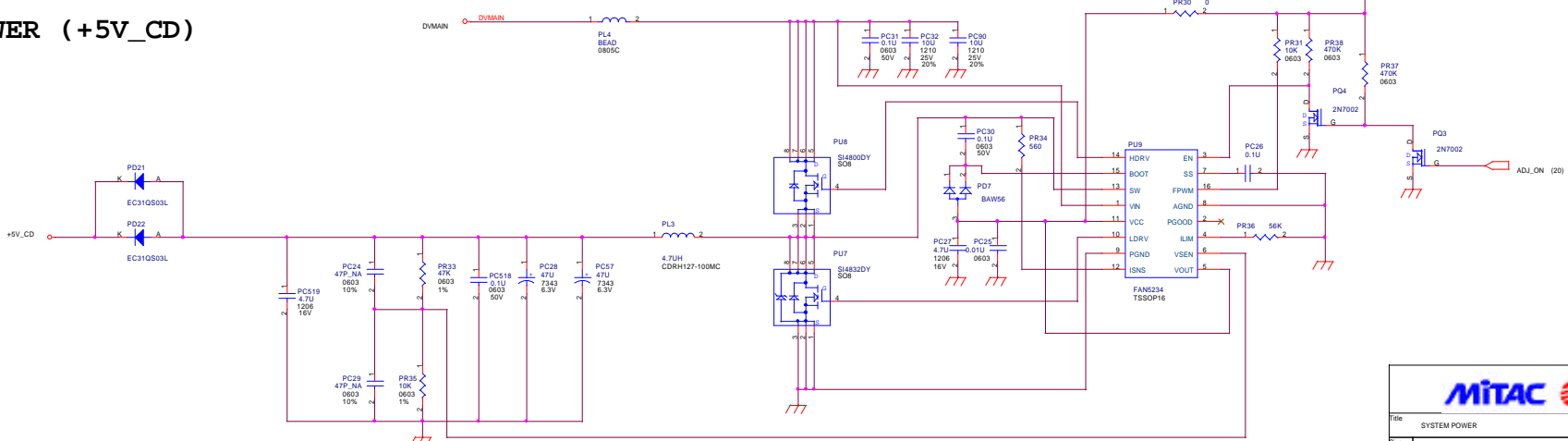


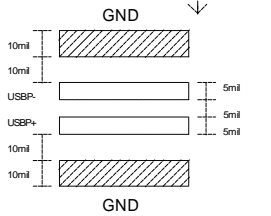
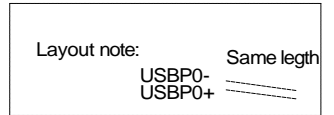
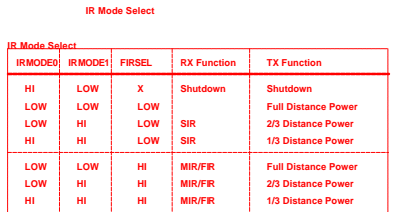
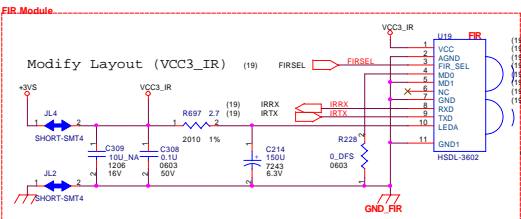


SYSTEM POWER (5V 3V 12V)



AUDIO DJ POWER (+5V_CD)





HISTORY

ROA->ROB

- Page 4, Change C508 from 1000P to 2200P.
- Page 5, Change C5-C13,C16,C19,C21,C23,C24,C26,C28,C501,C503-C507,C509,C510,C512-C534 from Y5V to X7R
- Page 5, Add U519 for CPU_CORE_EN.
- Page 7, Add R38 and Delete R39,R40 for H_AGP_VREF.
- Page 7, Add R698 and Delete R554,R555 for DDR_REF.
- Page 9, Add R229 and Delete R117,R119 for REF_1.25V.
- Page 10, Add MSTRAPSEL[0:3] for Nvidia MAP17 64MB.
- Page 10, Add C720-C722 for +1.35VS (MAP17_VDD).
- Page 10, Add C723 for VDD_MMR2.5.
- Page 10, Change signal name from -AGP_STOP to -A_STOP for the sme as AGP BUS's -AGP_STOP.
- Page 11, Change PCI_DEVID3 from AC3 to AB3.
- Page 11, Add X1 ,C47,C56 and Delete R44 for MAP17 CLK.
- Page 11, Delete X501,C584,C589 for CLK_GEN OSCIN.
- Page 11, Add L528,C74,C78,C83and Delete L14 for A3V (MAP17_ PLLVDD).
- Page 11, Change R95 to DFS.
- Page 11, Add MSTRAPSEL0-3 for Nvidia MAP17 64MB.
- Page 11, Add R82,R79,R559,R546 and Delete R81,R80,R558,R549 for PCI_DEVID[3:0] Set up Nvidia MAP17 64MB.
- Page 12, Change RP3 from 10K to 1K for LCD_ID[3:0].
- Page 12, Change R529,R539 value from 4.7K to 2.2K for pull-up SDA and SCL.
- Page 12, Add RP530 for EMI.
- Page 12, Add C586 for DDC2B
- Page 13, Add -USB_SMI,MINI_Pd,-CRT_IN function for usb in dos boot,minipci powerdown,crt detect.
- Page 14, Change J7,J5 from SMD Part to DIP Part.
- Page 15, Add L534,L535 for EMI.
- Page 15, Change R185 valur from 0 ohm to DFS for costdown.
- Page 16, Add L536,L537 for EMI.
- Page 16, Change U6.95pin pull high from +3V to +3VS.
- Page 17, Add U12,R708,C724,C248,Q511,R36,L530 for ALC202_AVDDAD.
- Page 17, Change Amplifer from LM4840 to TPA0552.
- Page 18, Change J506 pitch from 1.0mm to 0.5 mm.
- Page 18, Change R103 form 100K to 47K and C112 from 1U to 2.2U for -OZ RST.
- Page 18, Modify X3 pin2 ,pin4 contact to GND.
- Page 20, Add Q515,R732,R733,C748,D506,J509 for System 2nd FAN.
- Page 20, Add Q518-Q521,R770-R774 for H8 hang reset H8.
- Page 20, Add R763 for -PWR_EL.
- Page 20, Add -CONN_PLAYPAUSE,-CONN_RW,-CONN_FF,-CONN_STOP&JECT signal's R728-R731 pull-up for Audio DJ BTN.
- Page 20, Modify U518 pin1,pin13 connect to GND and pin24 connect to +5VS.
- Page 20, Add R765,R764 for system Thermal Resistor Sensor.
- Page 21, Add U523,C770-C773,R778 and Delete R775 for MiniPCI VOC5VA.
- Page 21, Add Q516,Q522,C749,C774 for VT6202 Leakage.
- Page 21, Change to 25V_USB for support USB wake up.
- Page 21, Change X5 from 24.768 MHZ to 24MHZ for VT6202 CLK.
- Page 25, Change to ADJ_ON for AudioDJ +5V_CD.
- Page 27, Add RP531,RP532 for EMI.

ROB->ROC

- Page 4, Add R798 for -THEPM pull +3VS
- Page 5, Delete U1,R74,R144,and R145 for usually don't boot
- Page 7, Mount R555,R54,Delete R698 for DDR_REF voltage stable
- Page 7, R38 0 ohm change DFS.
- Page 9, Mount R117,R119 ,remove R229 for REF_DIM voltage stable
- Page 9, R229 0 ohm change DFS
- Page 9, R231,R565 0 ohm change DFS
- Page 13, Add R799,Q518,U523 for backlight enable
- Page 17, Add Q519,R800 for +5V_CD leakage.
- Page 17 change C727,C739 value from 0.47uf to 2200pf
- Page 17 change C733,C746 value from 0.47uf to 0.22uf
- Page 17 change C94,C108 value from 330uf to 220uf
- Page 17, R780 0 ohm change DFS
- Page 18, R110 0 ohm change DFS
- Page 20, modify -THMTRIP and -THEMP circuit for can't boot
- Page 20, Add R801 for debug
- Page 21, change R217,R690,R175 value from 0 ohm to DFS
- Page 21, Add Q522,R803 for -WIRE_LED
- Page 27, modify TV-out pin define for can't output TV
- Page 21, Change GND_USB to GND
- Page 27, Change GND_USB to GND
- Page 27, Add RP535,RP536 for EMI.
- Page 12, Add RP534 for EMI.

ROC->R01

- Page 17, Change R661 value from 0 to 1K.
- Page 17, R662 value from 0 to 100K
- Page 17, Add DTC144TKA for audio Amplifer Mute
- Page 17, Add 0.1u for HP/-LINE by pass
- Page 17, change L531 from Read to RC10Q804 for CD-ROM noise
- Page 17, change C531 and C532 shape from 0805 to 0603
- Page 16, change J1 shape
- Page 17, delete C231,C237,C243 for layout space not enough
- Page 8, change C117,C111 from 5P to 22P for WinXP time
- Page 20,18 add ADJ_SCLK and ADJ_SDATA signal for memory button push.

R01->R02

- Page 18,20, U517.48 pin contact to U505.72 for audioDJ in idle powe down
- Page 27, Modify common chock from 120ohm(MURATA) to 90ohm(TDK) for SI measure

			
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