LCFC Confidential

E455

NM-A231 Schematics

AMD Kaveri 2.0 Processor with DDR3L + Bolton FCH

GPU AMD JET XT

2014-7-7

REV:1.0

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Title: Cover Page

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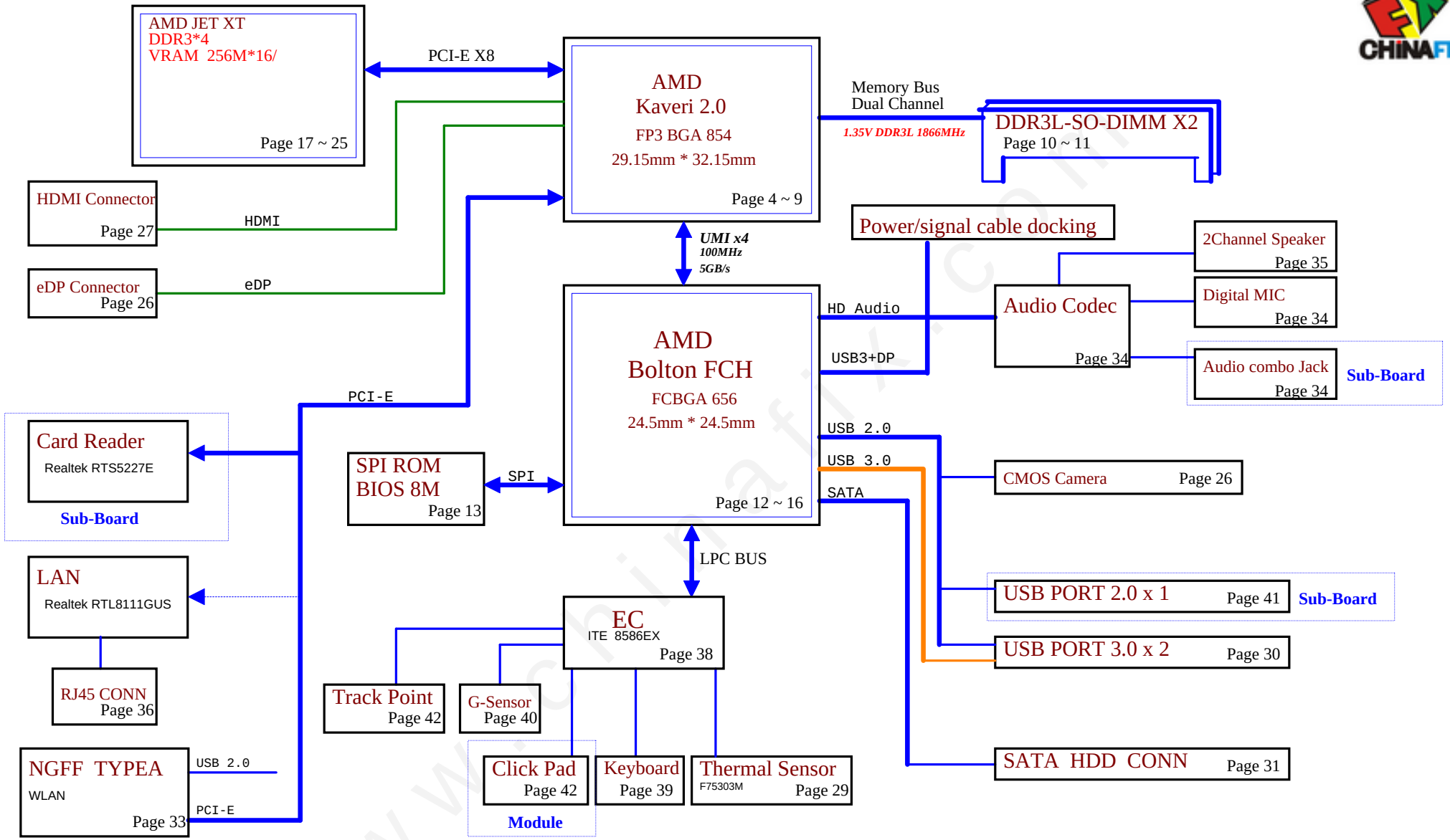
Date: Tuesday, August 19, 2014 | Sheet 1 of 60

Model Name : AAVE1



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Title: Block Diagram

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+1.35V	+5VS +3VS +0.675VS +0.95VS_VDDP +0.95VS_VDDR +1.8VS_VDDA +1.1VS +VDD_CORE +VDDNB_CORE +VGA_CORE +3VS_VGA +1.8VS_VGA +1.5VS_VGA +0.95VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 3.0	Port	Port	3 External USB Port
EHCI			0	USB 2.0 Port
			1	
			2	
			3	
			4	
EHCI			5	Camera
			6	WLAN/BT
			7	FPR
			8	
			9	
	xHCI	0	10	USB 3.0 Port
		1	11	
	xHCI	2	12	USB 3.0 Port
		3	13	Docking port

BOM Structure Table

BTO Item	BOM Structure
Un-mount	@
Connector	ME@
GPU	DIS@
UMA	UMA@
VRAM Option	X76@
RF Part Option	RF@
EMI Part Option	EMI@
ESD Part Option	ESD@
JET GPU	JET@
TOPAZ GPU	TOPAZ@
Quad Core APU	QC@
14 MB	14@

PCIE PORT LIST

Port	Device
0	LAN
1	Card Reader
2	WLAN
3	
4	
5	
6	
7	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus3 address

Device	Address
Thermal Sensor	

FCH SM Bus address

Device	Address
DDR DIMM1	
DDR DIMM2	

ZZZ1

DAZ0TV00100

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Title: Notes List

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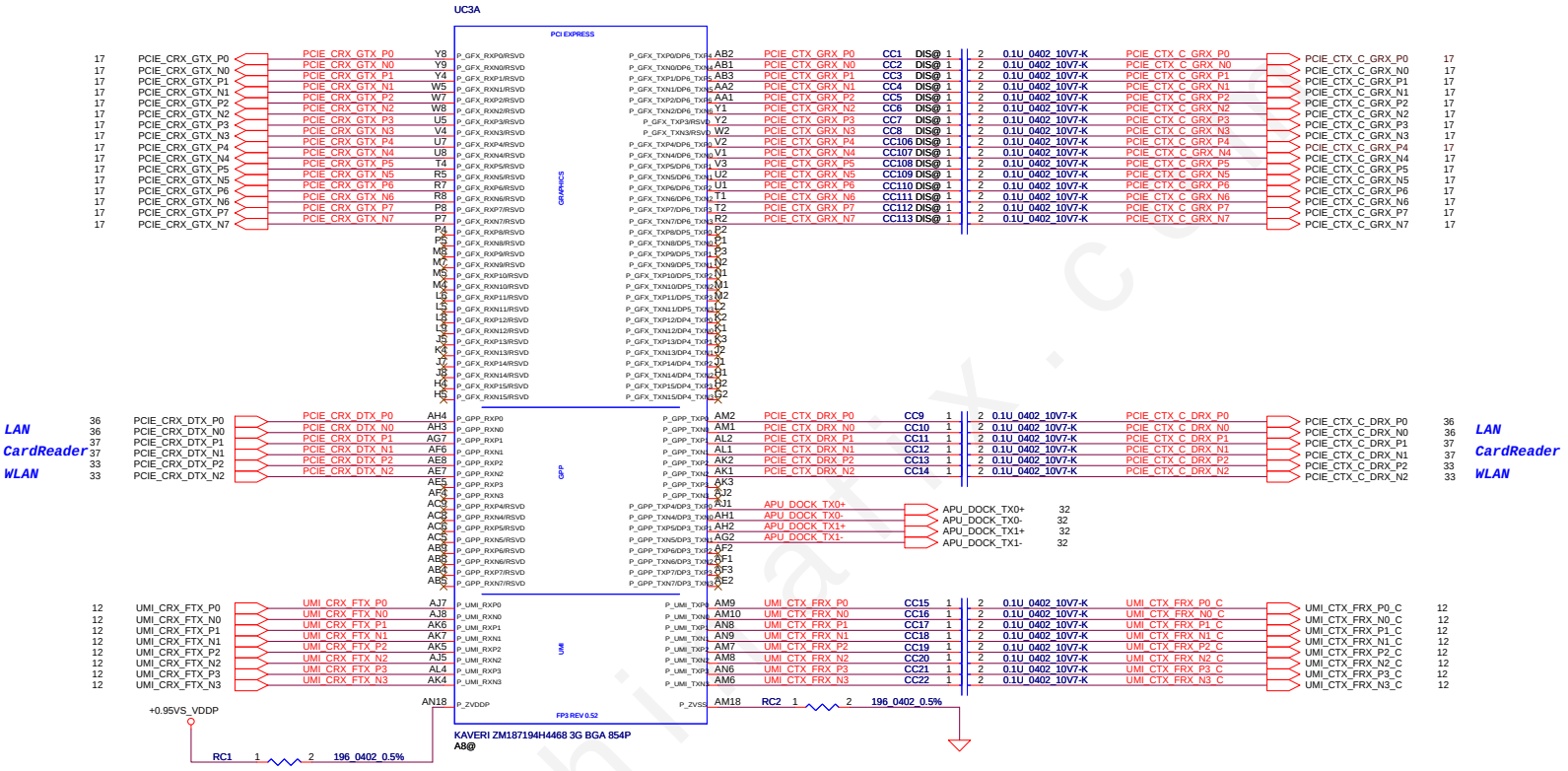

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Title: APU PEG/PCIe/UMI

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Title: APU DDRB/2

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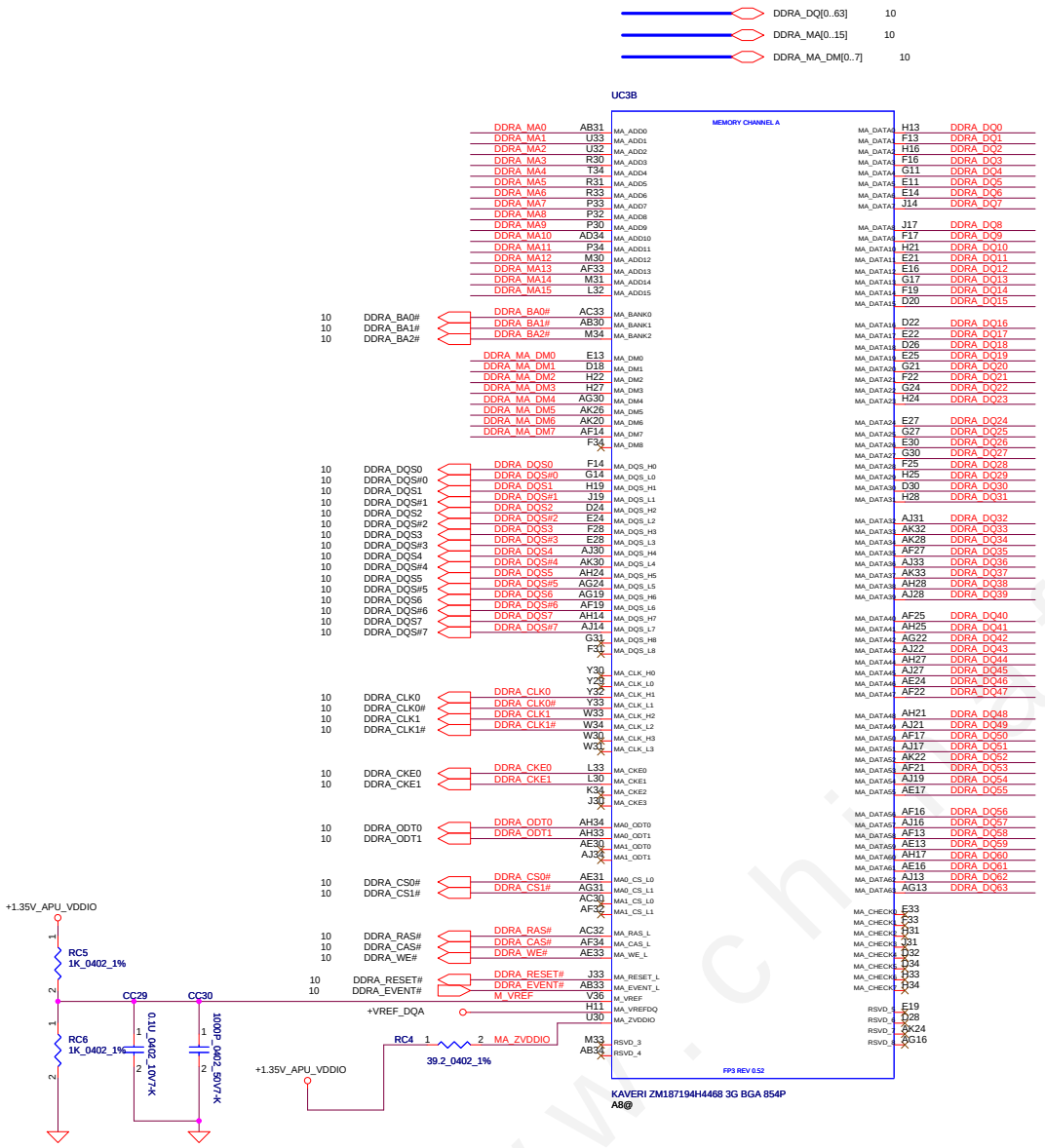

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Title: APU DDRA/1

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H_PROCHOT# :
Normal high
Active low
Keep low after susp# sustp#

Check connect to FCH or EC

UC3D

KAVERI ZM187194H4468 3G BGA 854P
A8@

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Title: APU Misc

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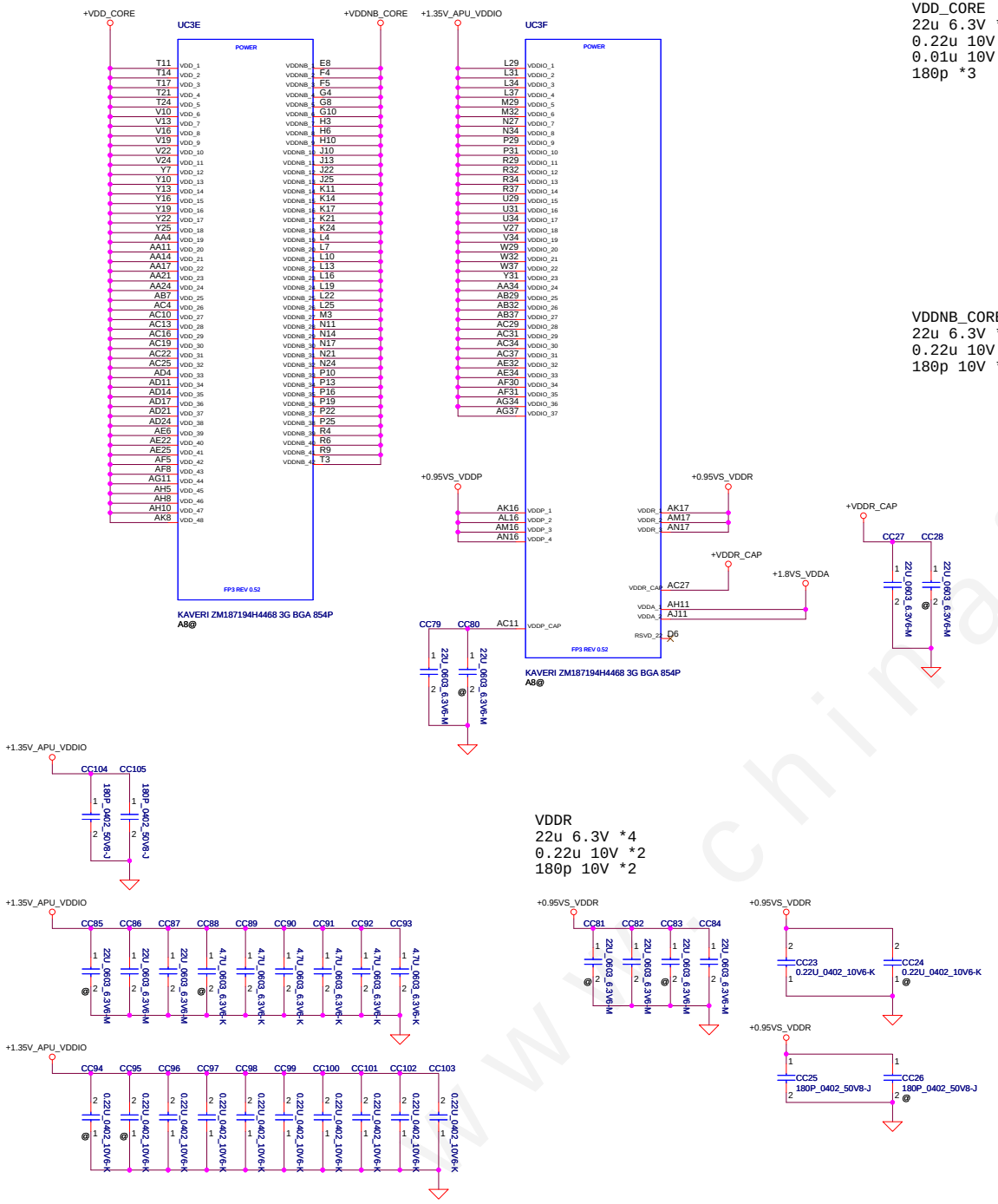
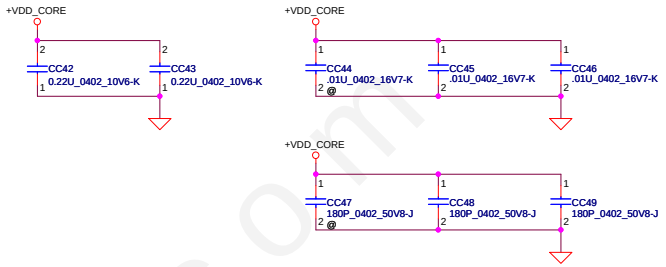
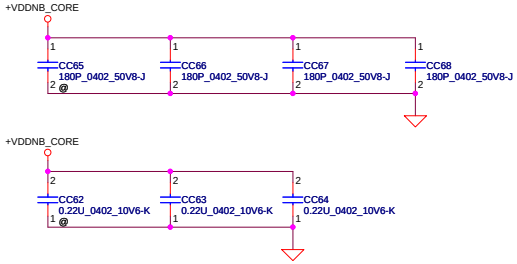


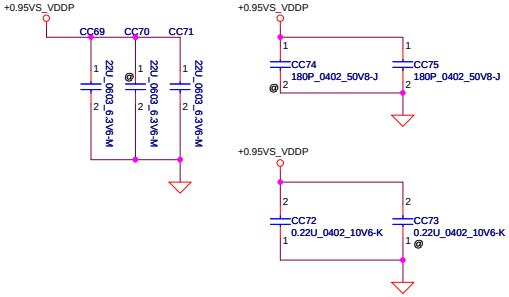
VDD_CORE
22u 6.3V *11 @*2 Design Guide
0.22u 10V *2
0.01u 10V *3
180p *3



VDDNB_CORE
22u 6.3V *10 @*2 Design Guide
0.22u 10V *3
180p 10V *4

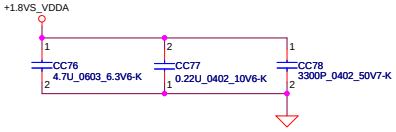


VDDP
22u 6.3V *3
0.22u 10V *2
180p 10V *2



VDDR
22u 6.3V *4
0.22u 10V *2
180p 10V *2

VDDA
4.7u 6.3V *1
0.22u 10V *1
3.3n 10V *1



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Title: APU Power

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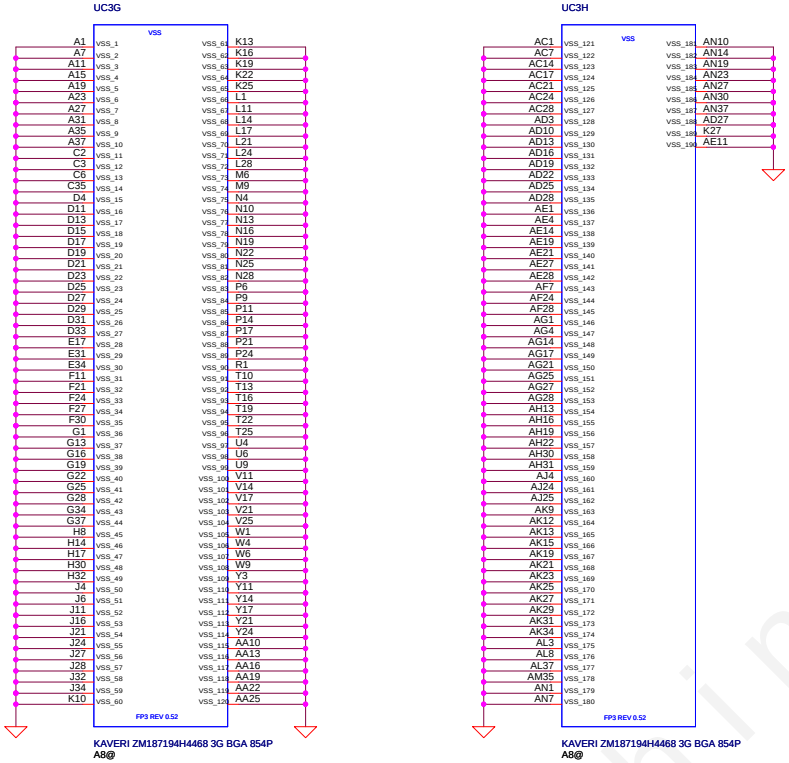

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Title: APU GND

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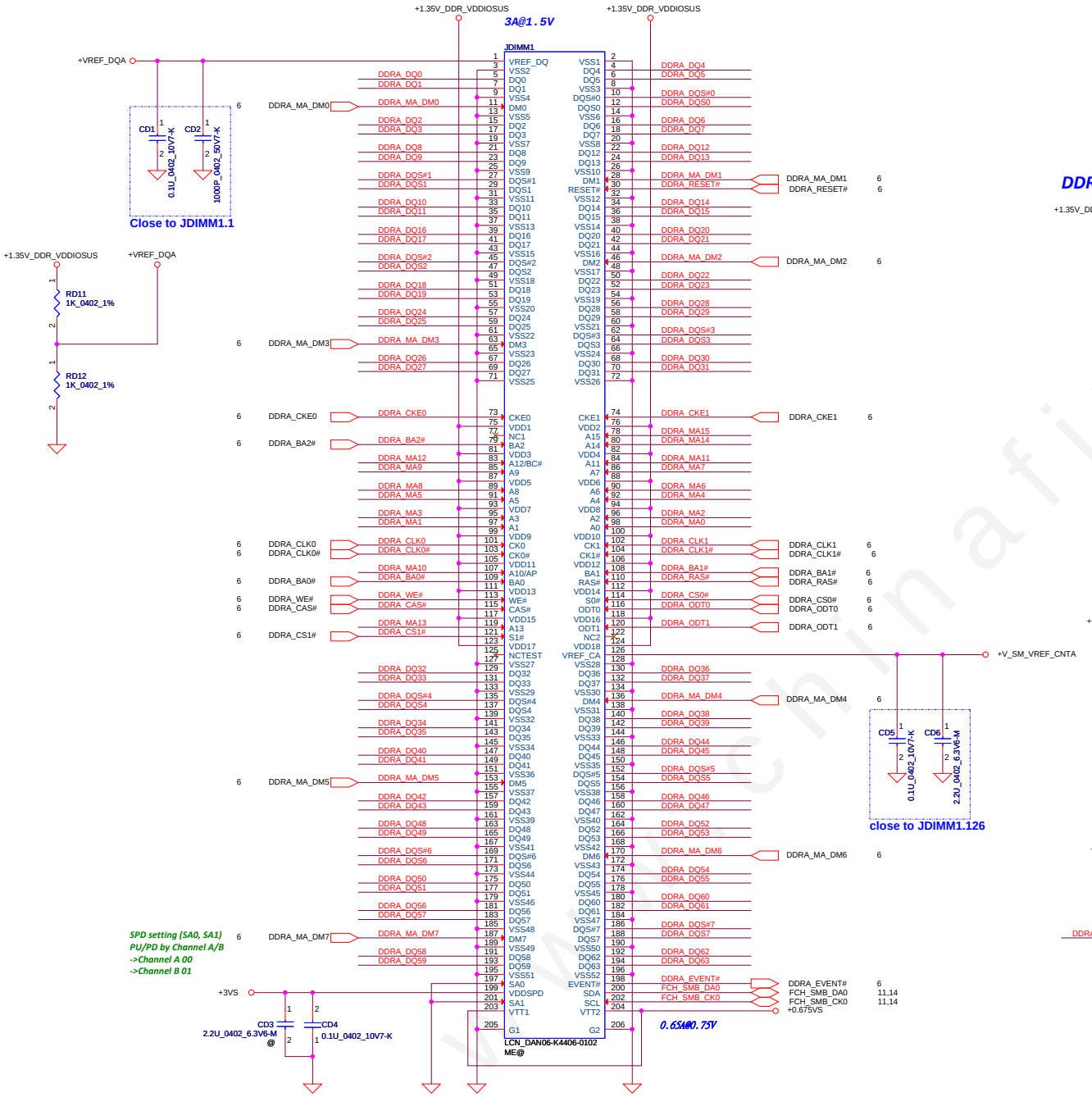
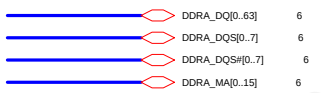
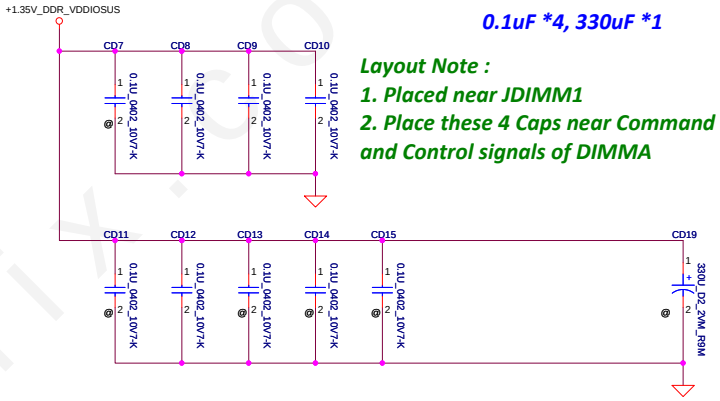
DDR3L SO-DIMM A



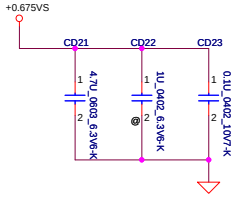


DDR Decoupling



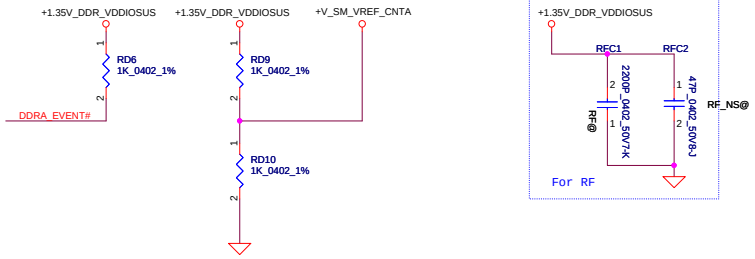
0.1uF *4, 330uF *1

Layout Note :
1. Placed near JDIMM1
2. Place these 4 Caps near Command and Control signals of DIMMA



Layout Note : Placed near JDIMM1.Pin203, 204

All VREF traces should have 20 mil trace width



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Title: DDR3L SO-DIMMA/1

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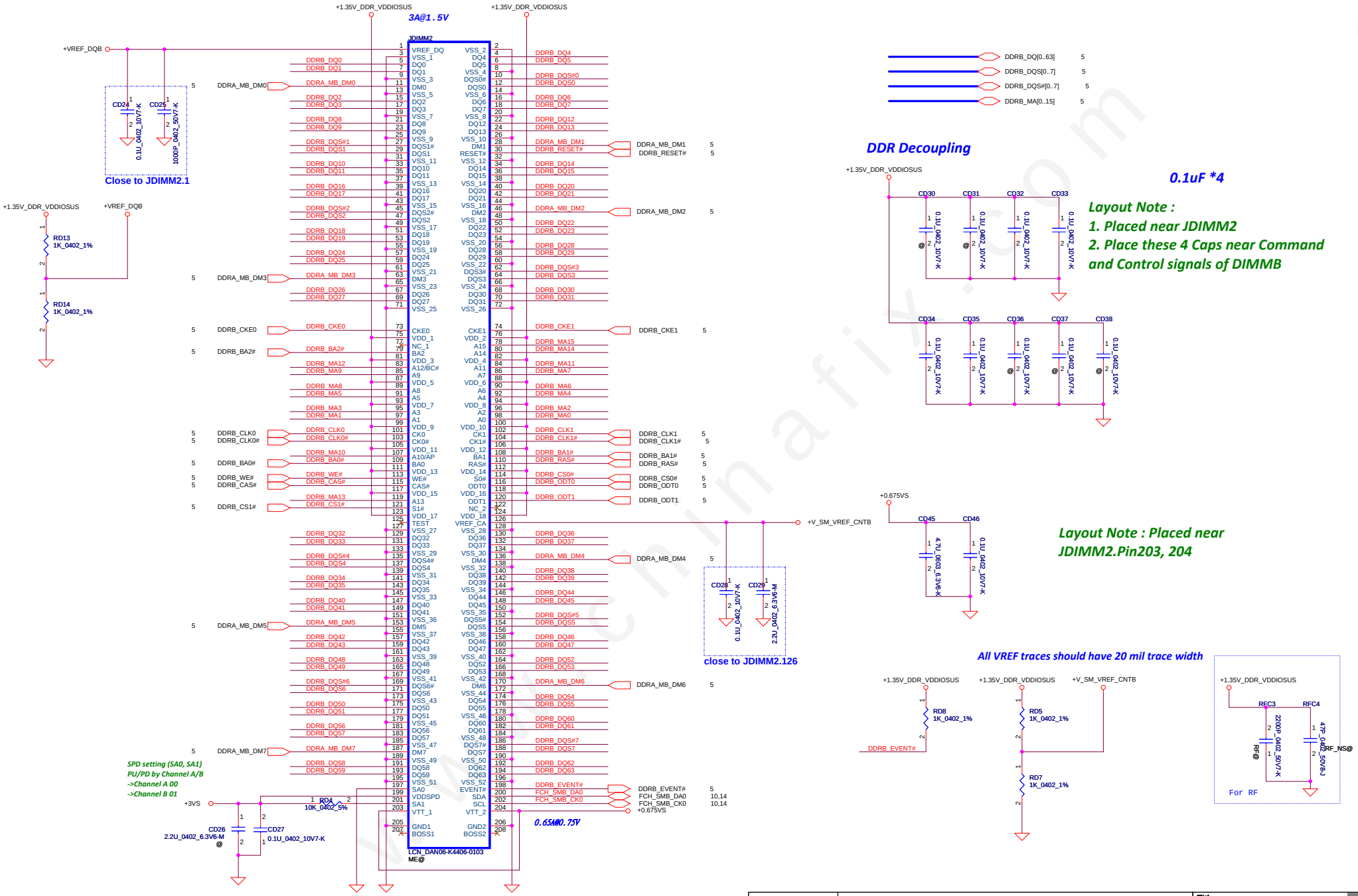
DDR3L SO-DIMM B



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Title: DDR3L SO-DIMMB/2

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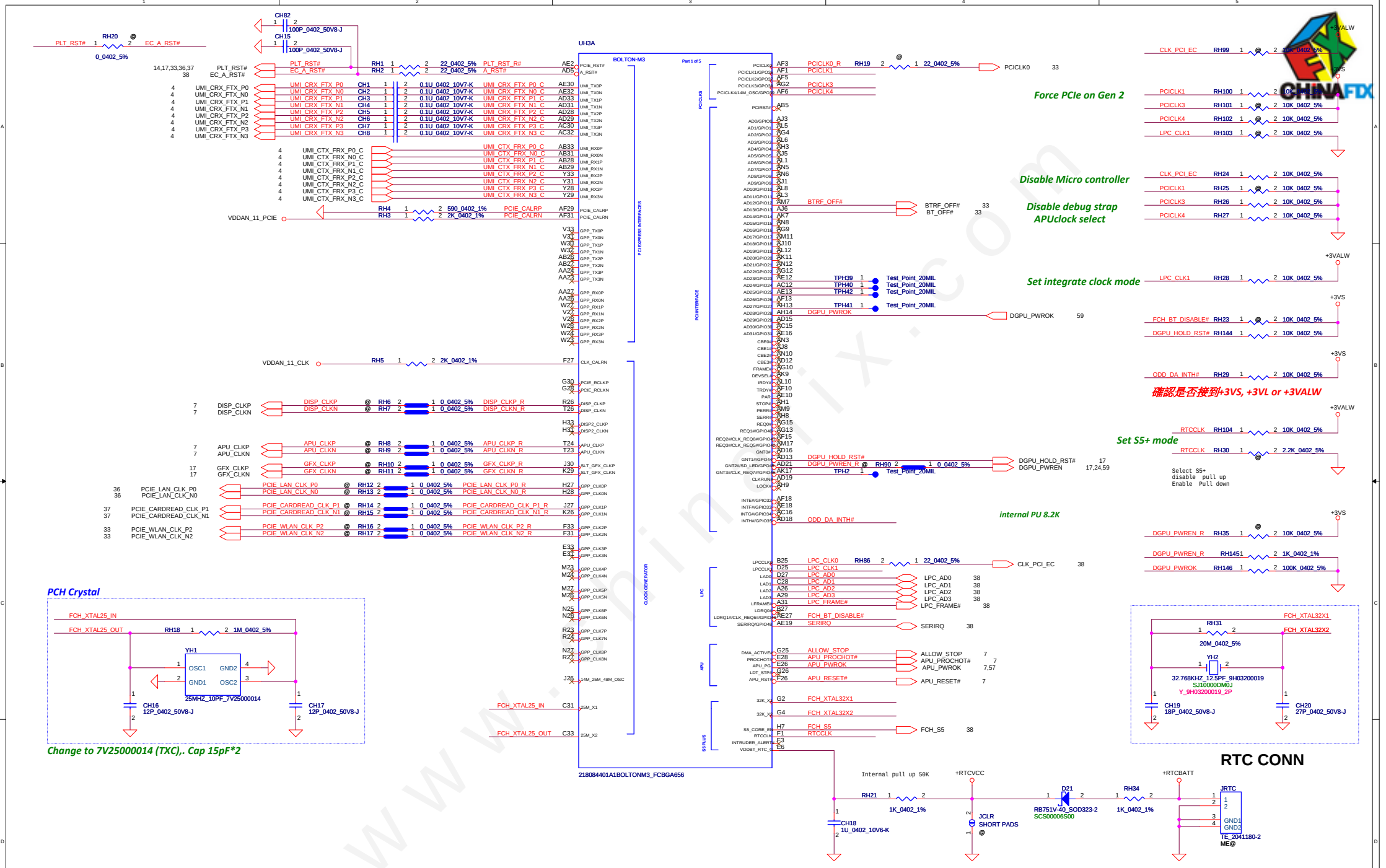

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Title: FCH PCIe/PCI/LPC/APU/S5+

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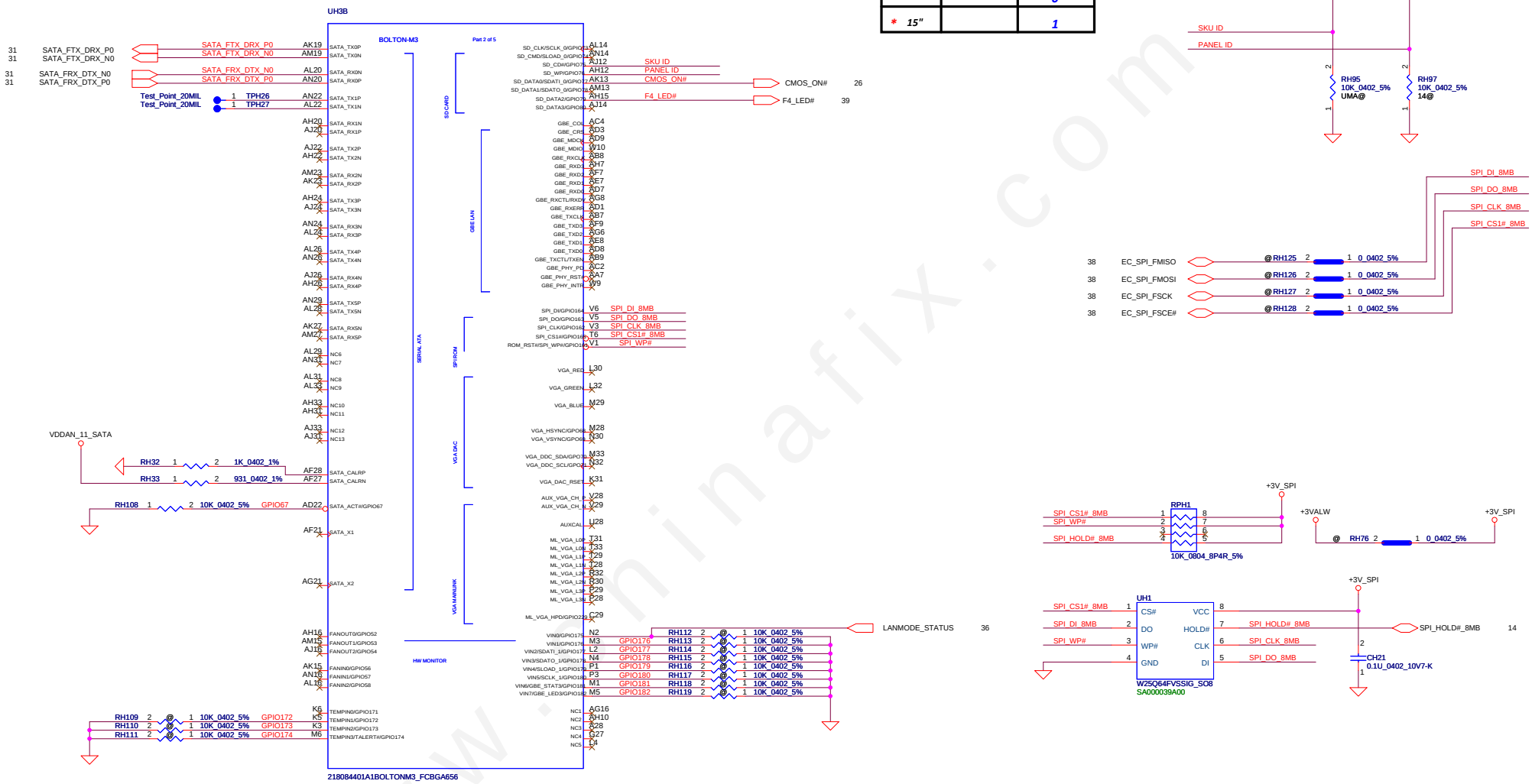
Table

Function	SKU_ID	PANEL_ID
* UMA	0	
* DIS	1	
* 14"		0
* 15"		1



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Title: **FCH SATA/GBE/SPI**

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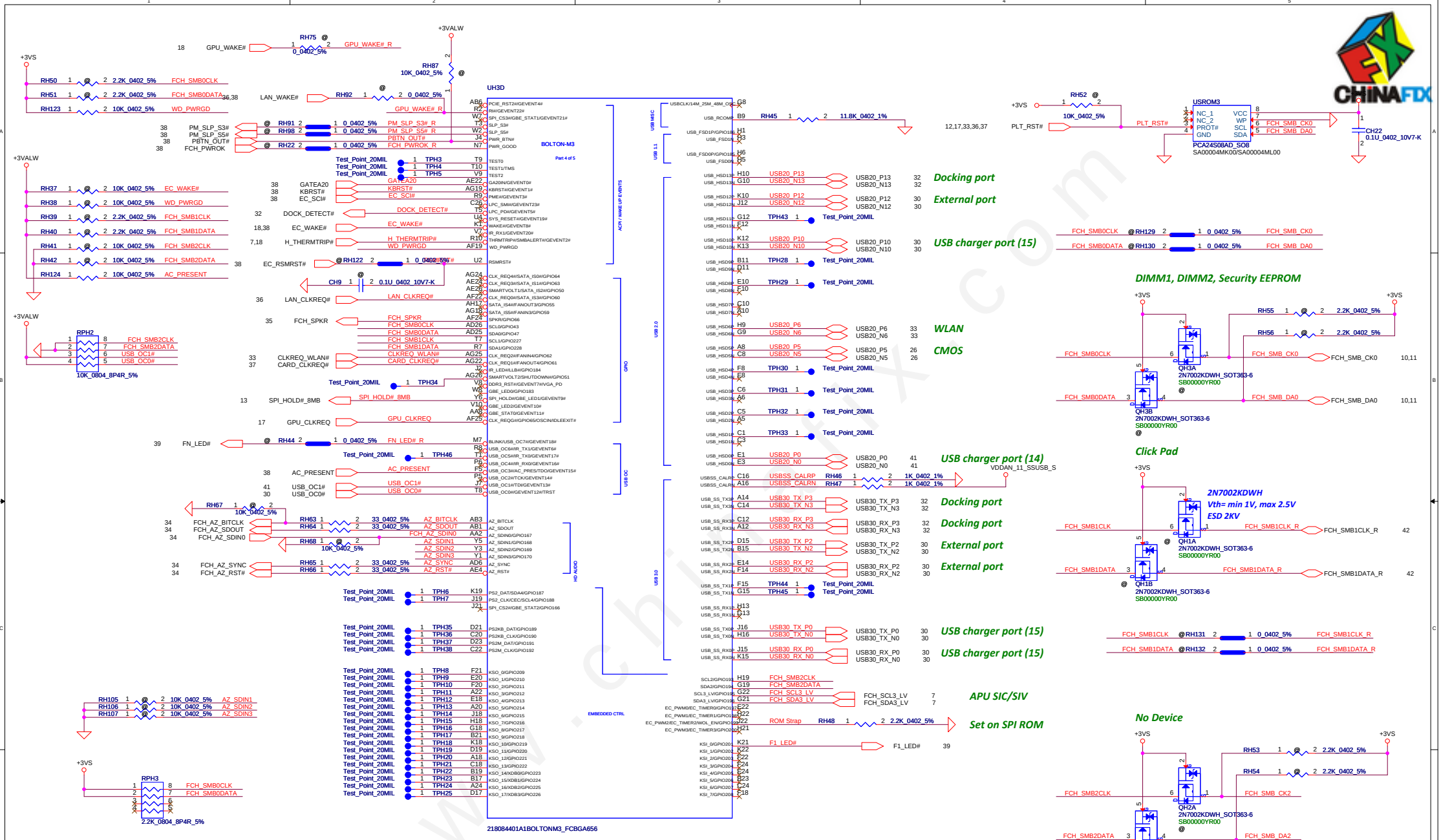

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Title: FCH ACPI/USB/GPIO

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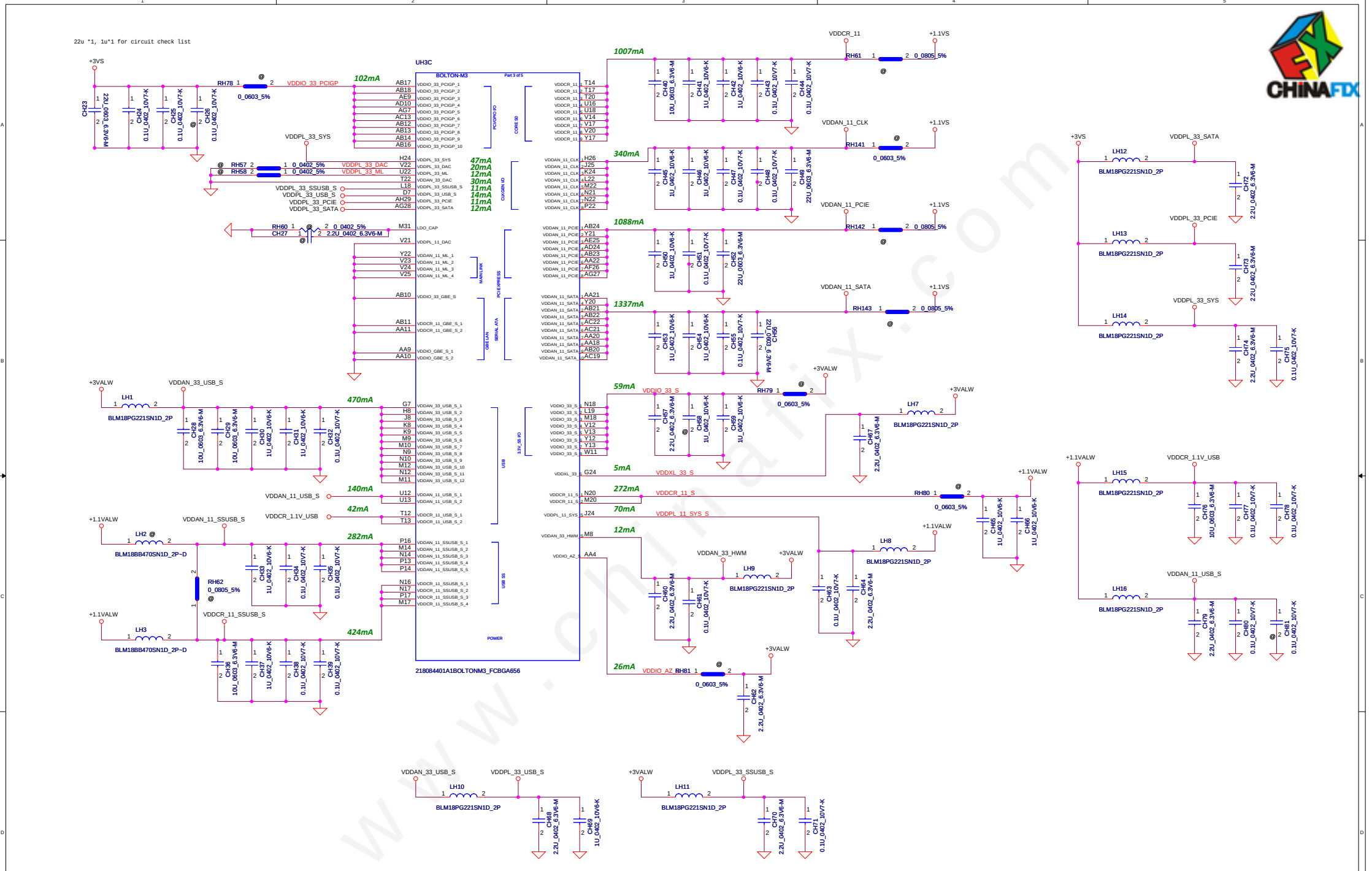

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Title: **FCH POWER/GND**

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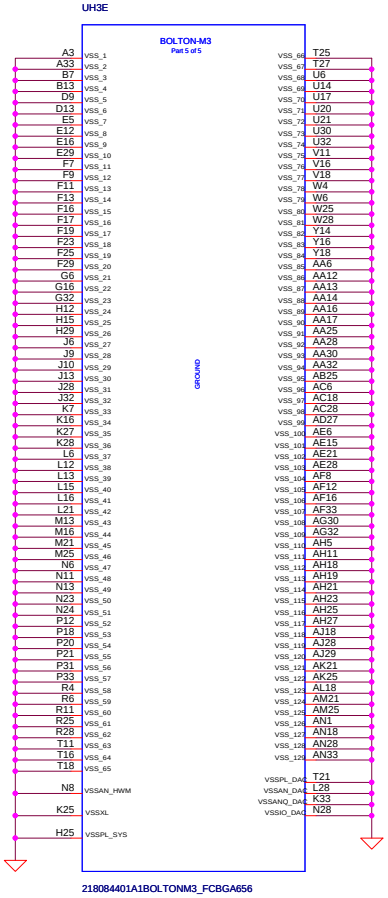

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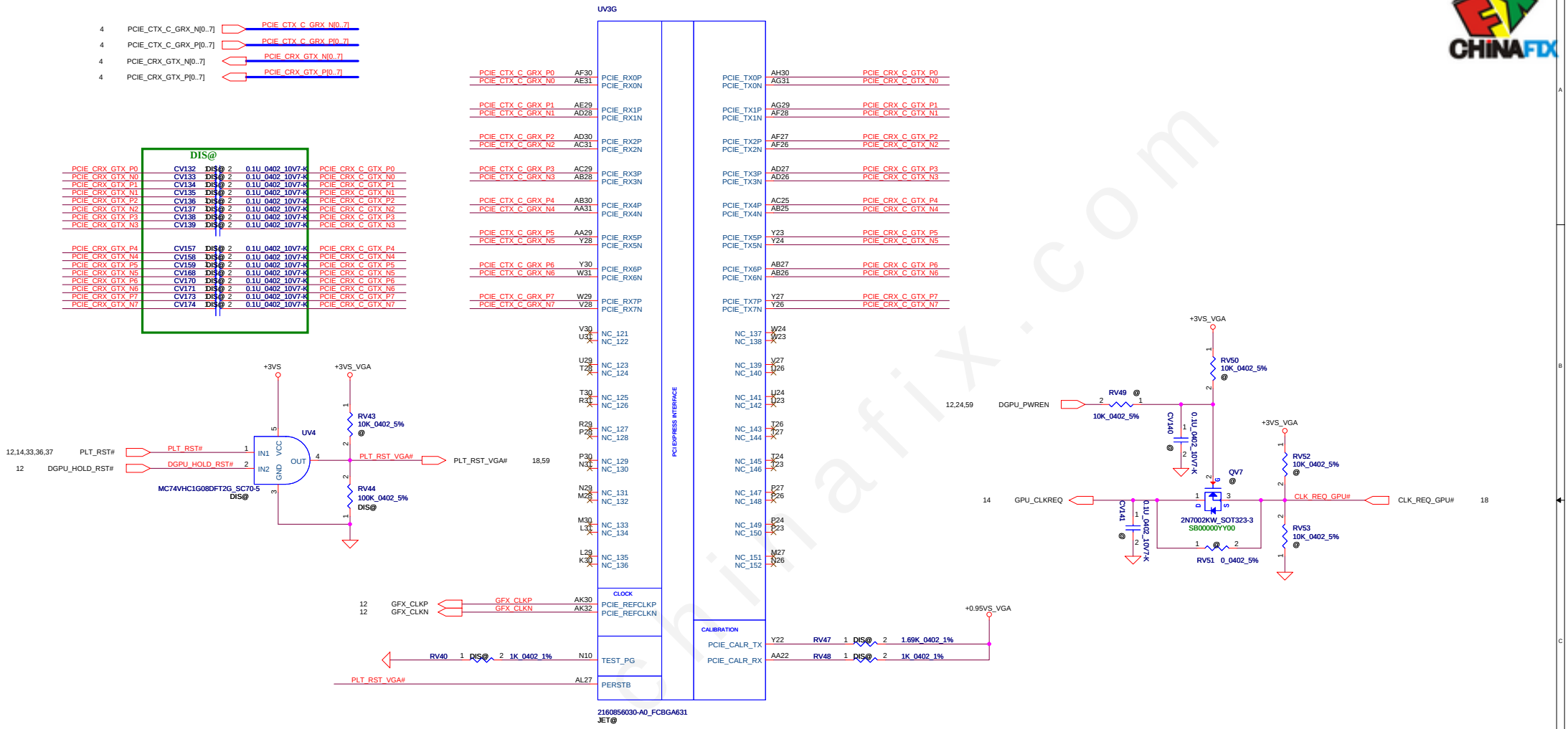

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Title: Topaz & Jet PCIE

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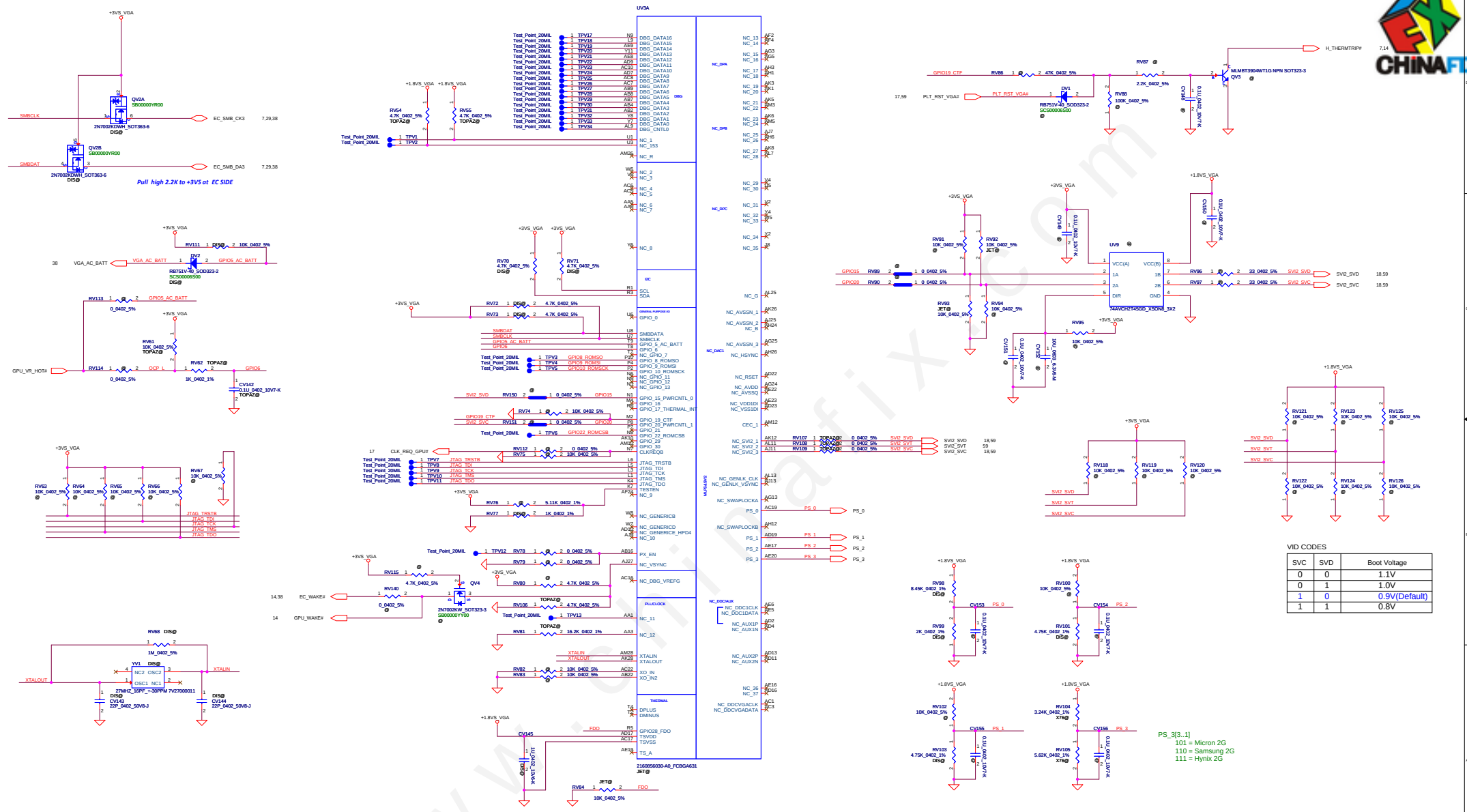

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V(Default)
1	1	0.8V

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Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title: Topaz & Jet GPIO

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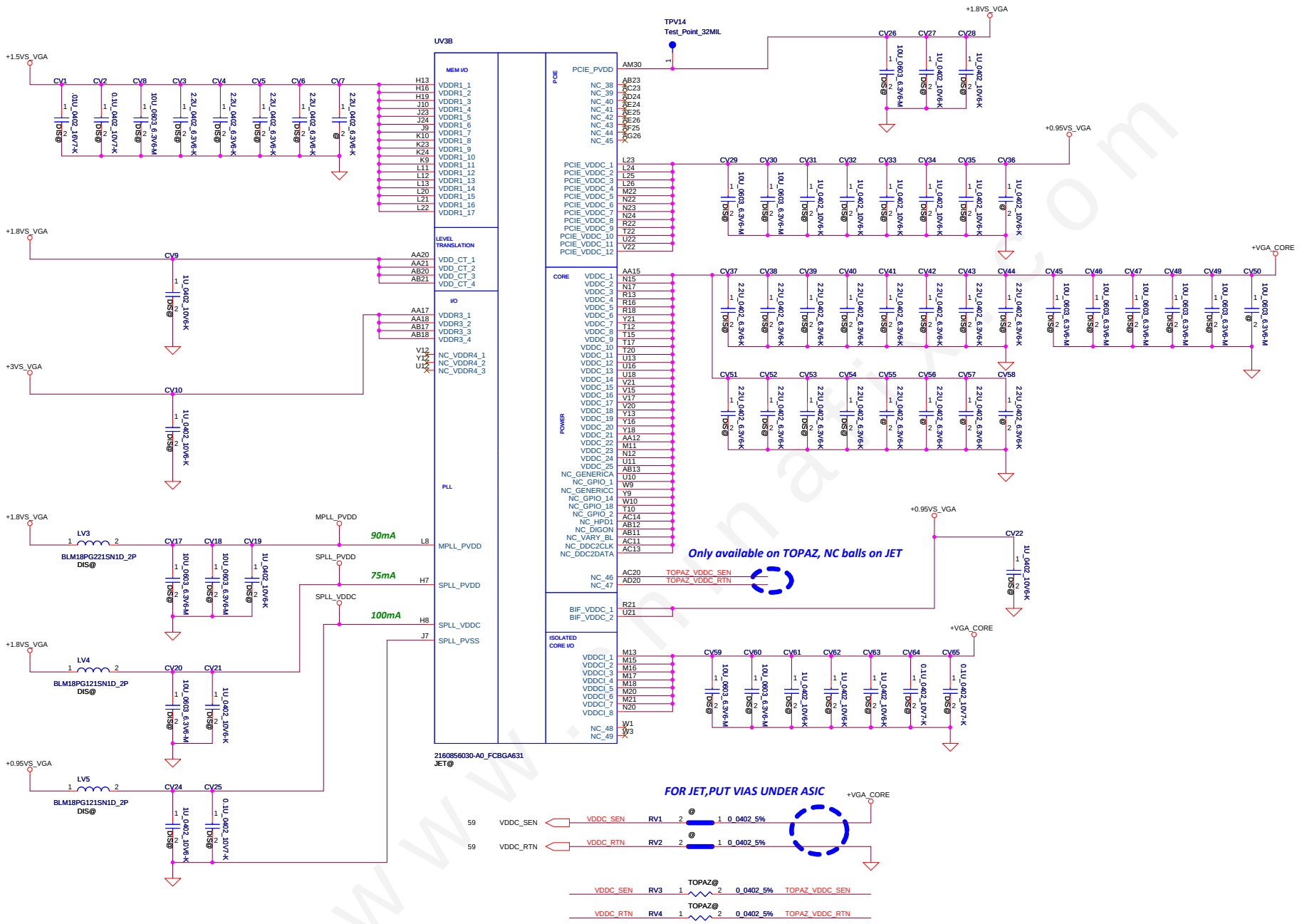

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title: *Topaz & Jet Core Power*

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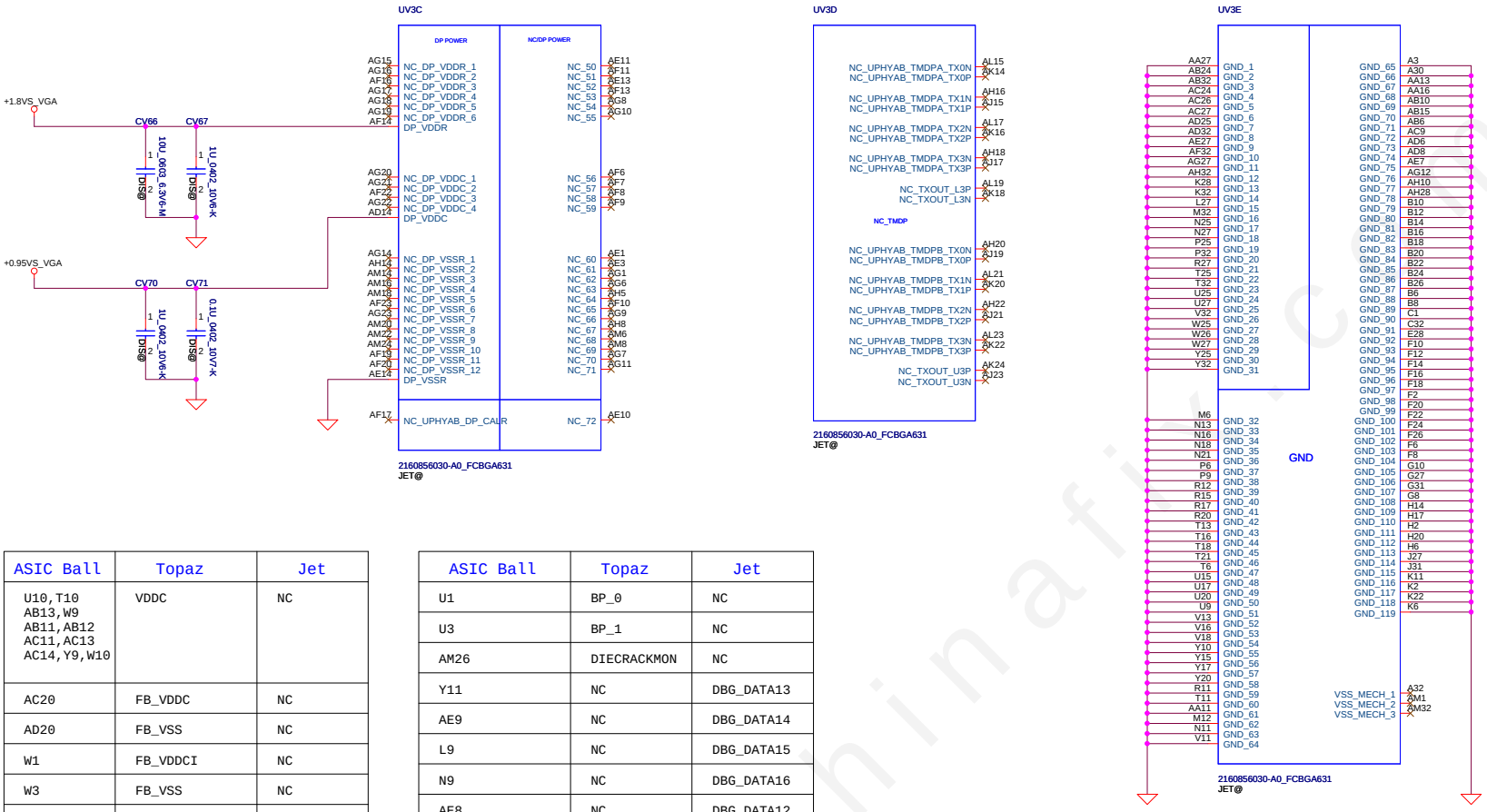
Date: Monday, July 07, 2014 | Sheet 19 of 60



ASIC Ball	Topaz	Jet
U10,T10 AB13,W9 AB11,AB12 AC11,AC13 AC14,Y9,W10	VDDC	NC
AC20	FB_VDDC	NC
AD20	FB_VSS	NC
W1	FB_VDDCI	NC
W3	FB_VSS	NC
AJ11	GPIO_SVC	NC_SVI2
AK12	GPIO_SVD	NC_SVI2
AL11	GPIO_SVT	NC_SVI2
N6	GPIO_11	NC_GPIO11
N5	GPIO_12	NC_GPIO12
N3	GPIO_13	NC_GPIO13
AJ27	WAKEB	NC_VSYNC
T8	PCC/GPIO_6	GPIO_6
AA3	PLL_ANALOG_OUT	NC
AA1	PLL_ANALOG_IN	NC

ASIC Ball	Topaz	Jet
U1	BP_0	NC
U3	BP_1	NC
AM26	DIECRACKMON	NC
Y11	NC	DBG_DATA13
AE9	NC	DBG_DATA14
L9	NC	DBG_DATA15
N9	NC	DBG_DATA16
AE8	NC	DBG_DATA12
AL9	NC	DBG_CNTL0
H13,H16,H19,J10 J23,J24,J9,K10 K23,K24,K9,L11 L12,L13,L20,L21 L22	VMEMIO	VDDR1
AA17,AA18 AB17,AB18	VDD_GPIO33	VDDR3
AA20,AA21 AB20,AB21	VDD_GPIO18	VDD_CT

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Title: Topaz & Jet DP Power/GND

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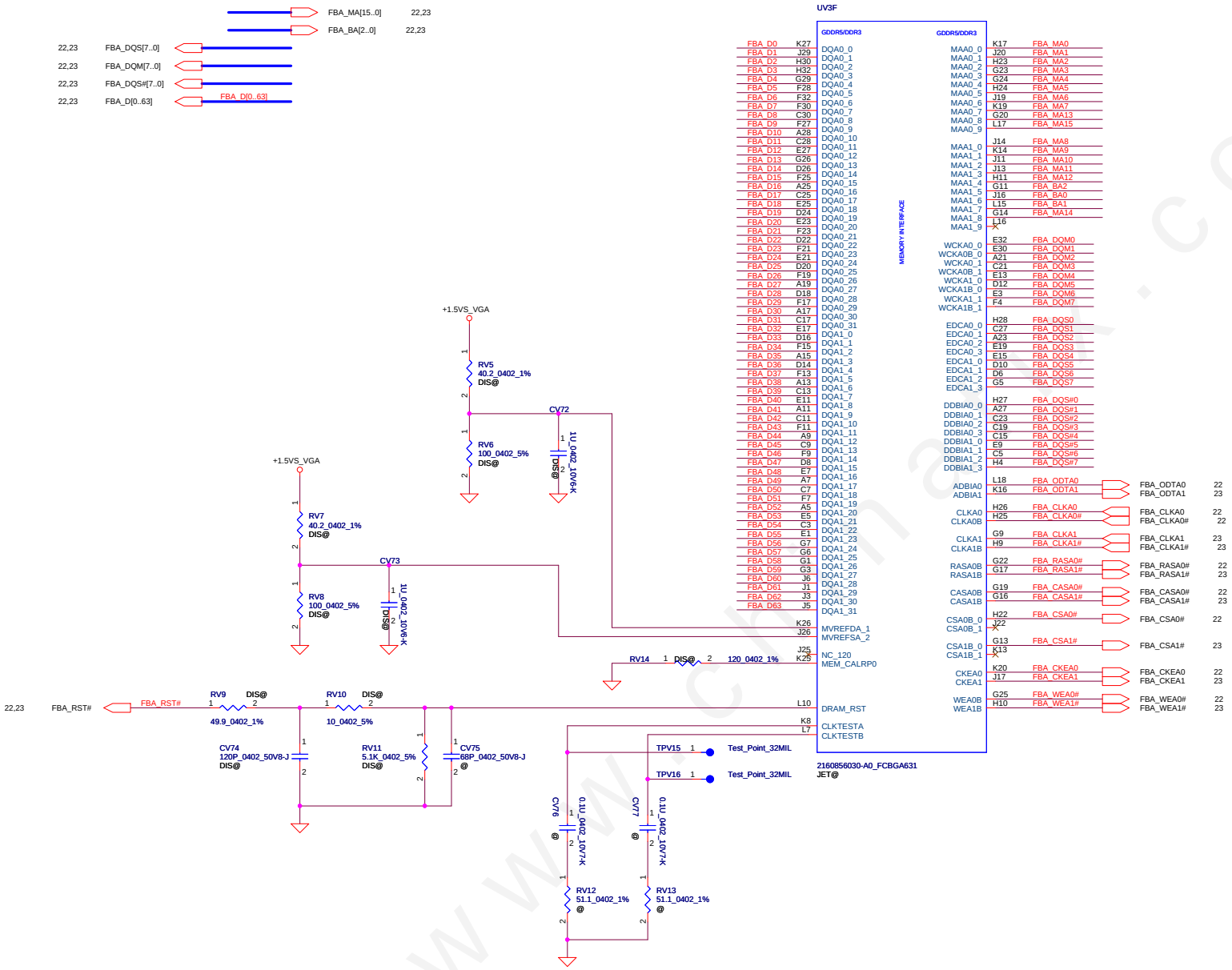

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Title: *Topaz & Jet MEM Interface*

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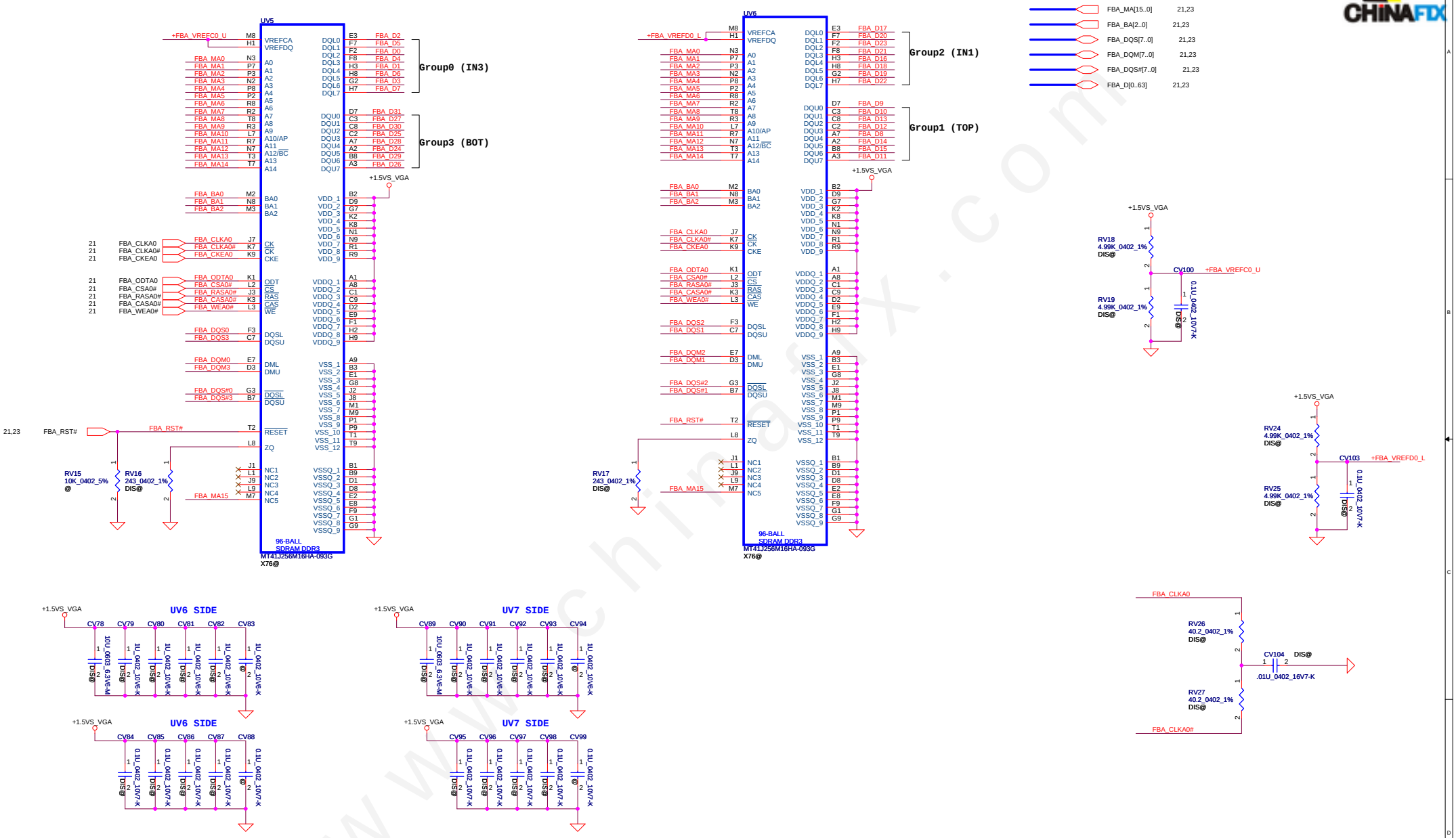
Memory Partition A - Lower 32 bits



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Title: *Topaz & Jet DDR3 VRAM 0*

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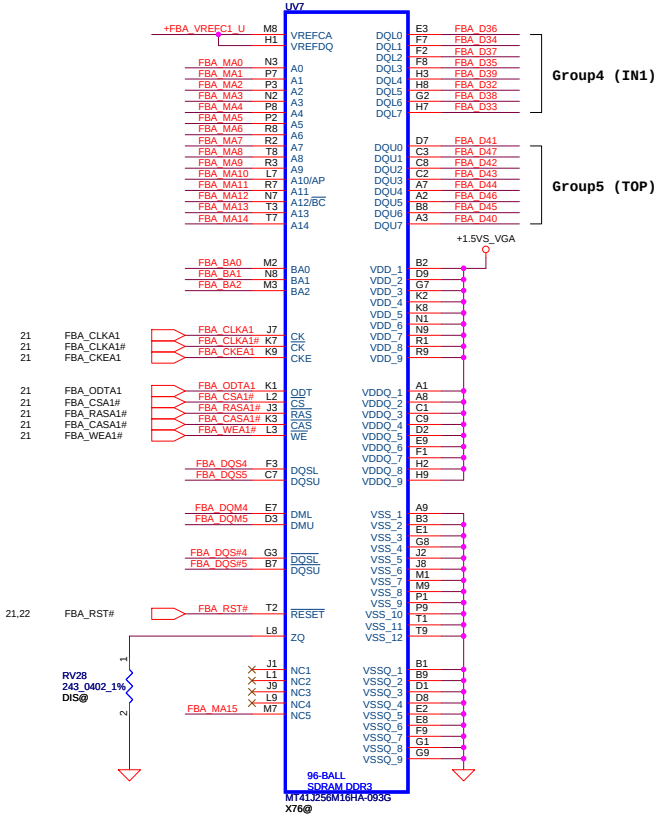
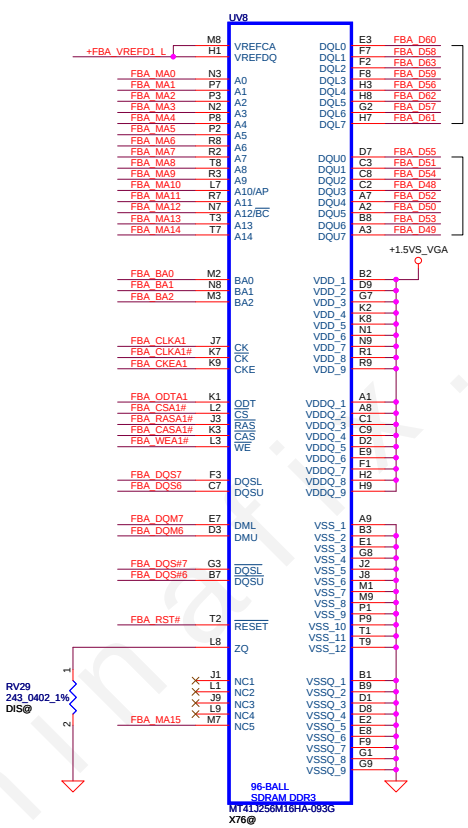
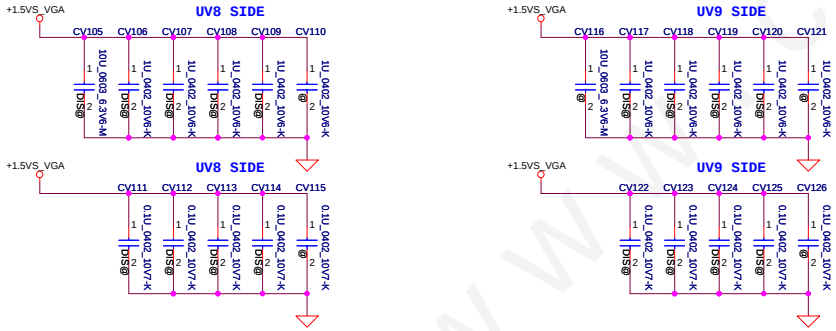
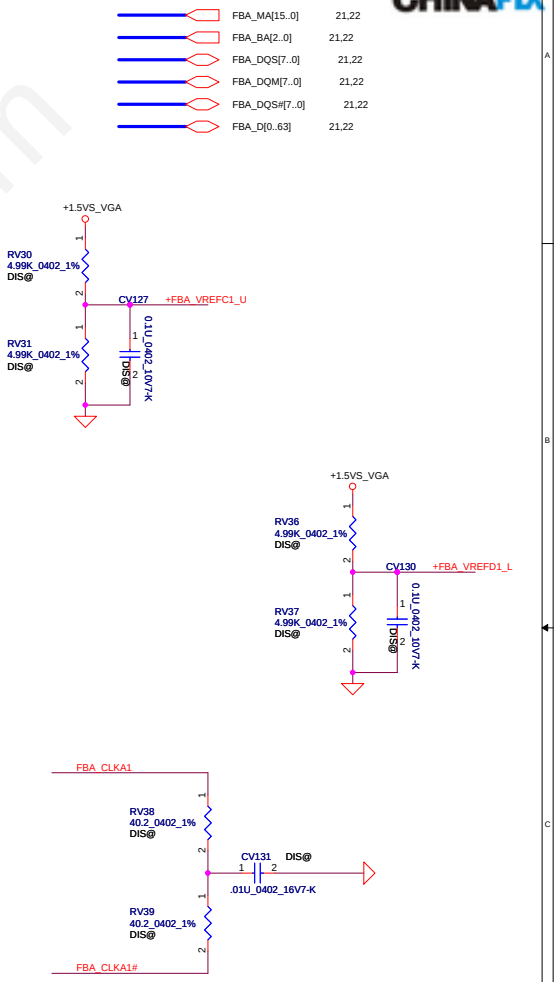
Memory Partition A - Upper 32 bits









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Title: *Topaz & Jet DDR3 VRAM 1*

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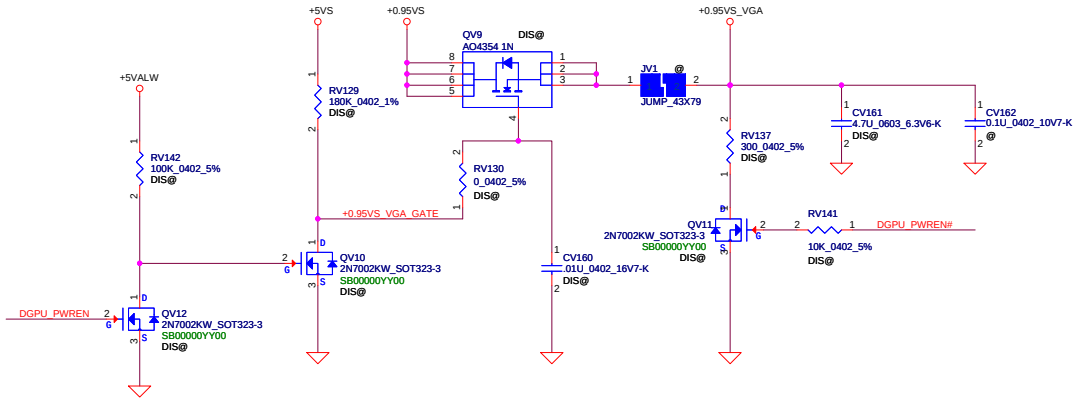
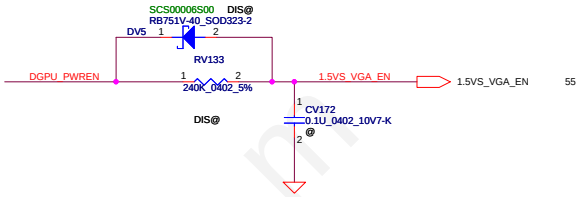
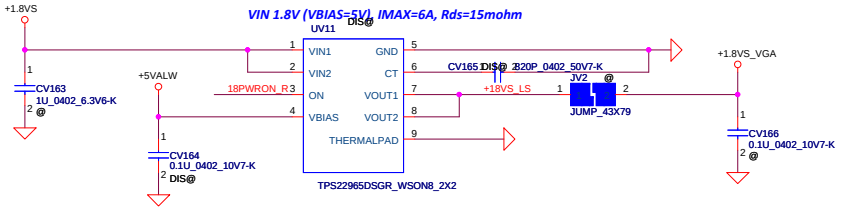
+0.95VS to +0.95VS_VGA

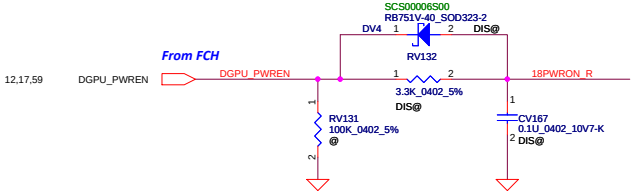


+1.5VS to +1.5VS_VGA

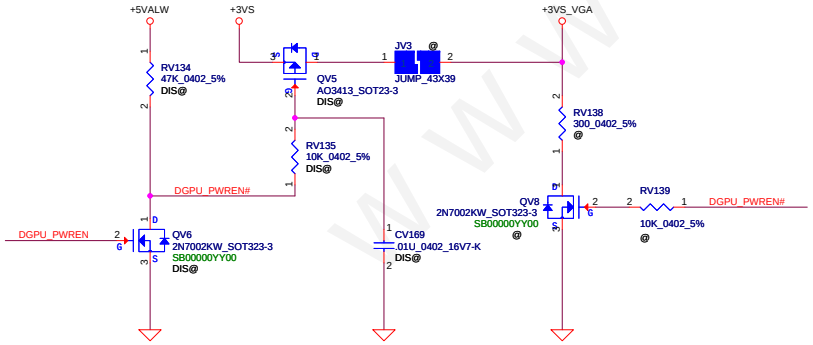


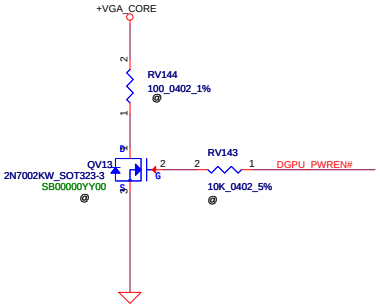
+1.8VS to +1.8VS_VGA





+3VS to +3VS_VGA





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Title: Topaz & Jet SWITCH POWER

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PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	STRAP_BIOS_ROM_EN = 1 ROM_CONFIG[2:0] = [001] 256MB
PS_0[4]	N/A	1 (Default)
PS_0[5]	N/A	1 (Default)
PS_1[1]	STRAP_BIF_GEN3_EN_A	0 = PCIe GEN3 is not supported
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled
PS_1[3]	N/A	0 (Default)
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	1 = The transmitter full-swing is enabled
PS_1[5]	STRAP_TX_DEEMPH_EN	1 = Tx deemphasis enabled
PS_2[1]	N/A	0 (Default)
PS_2[2]	N/A	0 (Default)
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device
PS_2[4]	N/A	1 (Default)
PS_2[5]	N/A	1 (Default)
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	PS_3[3..1] 101 = Micron 2G 110 = Samsung 2G 111 = Hynix 2G
PS_3[4]	N/A	1 (Default)
PS_3[5]	N/A	1 (Default)

MLPS	Bit				
	5	4	3	2	1
PS_0[5:1]	1	1	0	0	1
PS_1[5:1]	1	1	0	0	0
PS_2[5:1]	1	1	0	0	0
PS_3[5:1]	1	1	X	X	X

	PS_0		PS_1		PS_2		PS_3	
	RV98	RV99	RV102	RV103	RV100	RV101	RV104	RV105
Micron 2G	PU 8.45K	PD 2K	NC	PD 4.75K	NC	PD 4.75K	**PU 3.24K**	**PD 5.62K**
Samsung 2G	PU 8.45K	PD 2K	NC	PD 4.75K	NC	PD 4.75K	**PU 3.4K**	**PD 10K**
Hynix 2G	PU 8.45K	PD 2K	NC	PD 4.75K	NC	PD 4.75K	**PU 4.75K**	**NC**

3.24K SD03432418T
5.62K SD03456210T
3.4K SD03434010T

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Title: Topaz & Jet BLANK

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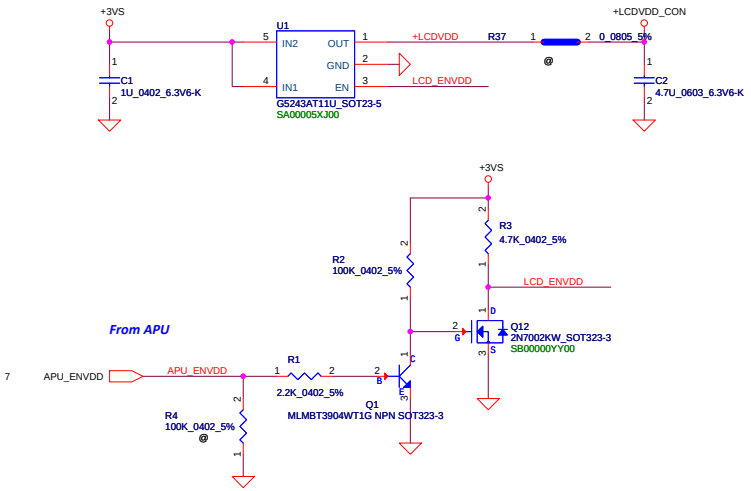
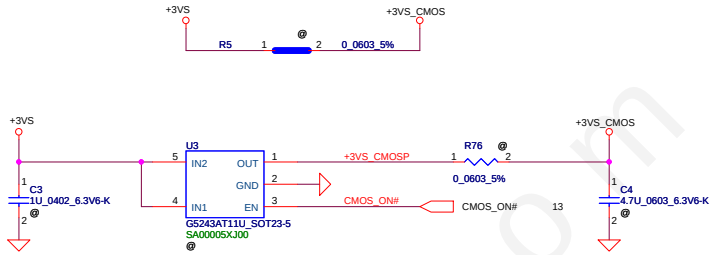
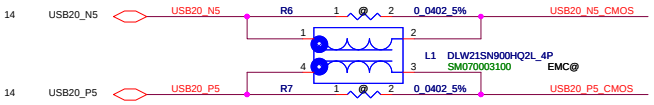
LCDVDD Circuit

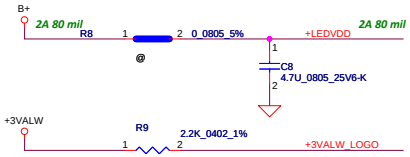


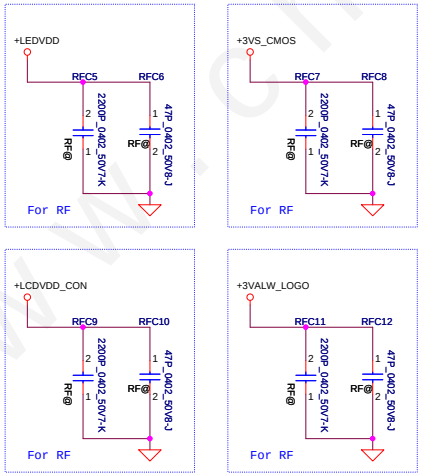
CMOS Camera

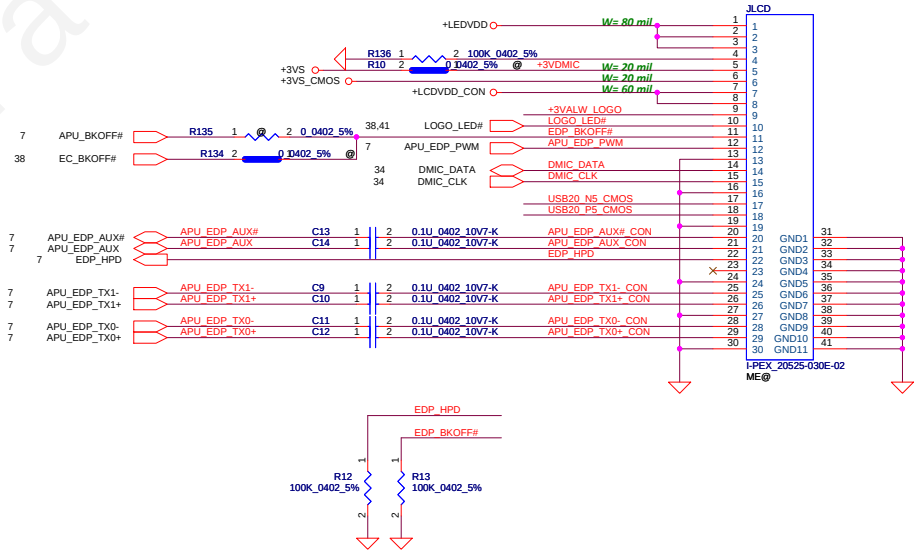


CMOS USB Port5

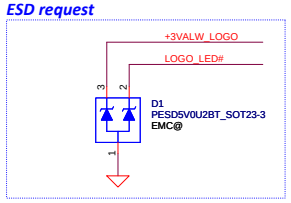








ESD request



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Title: LCD/CMOS CONN

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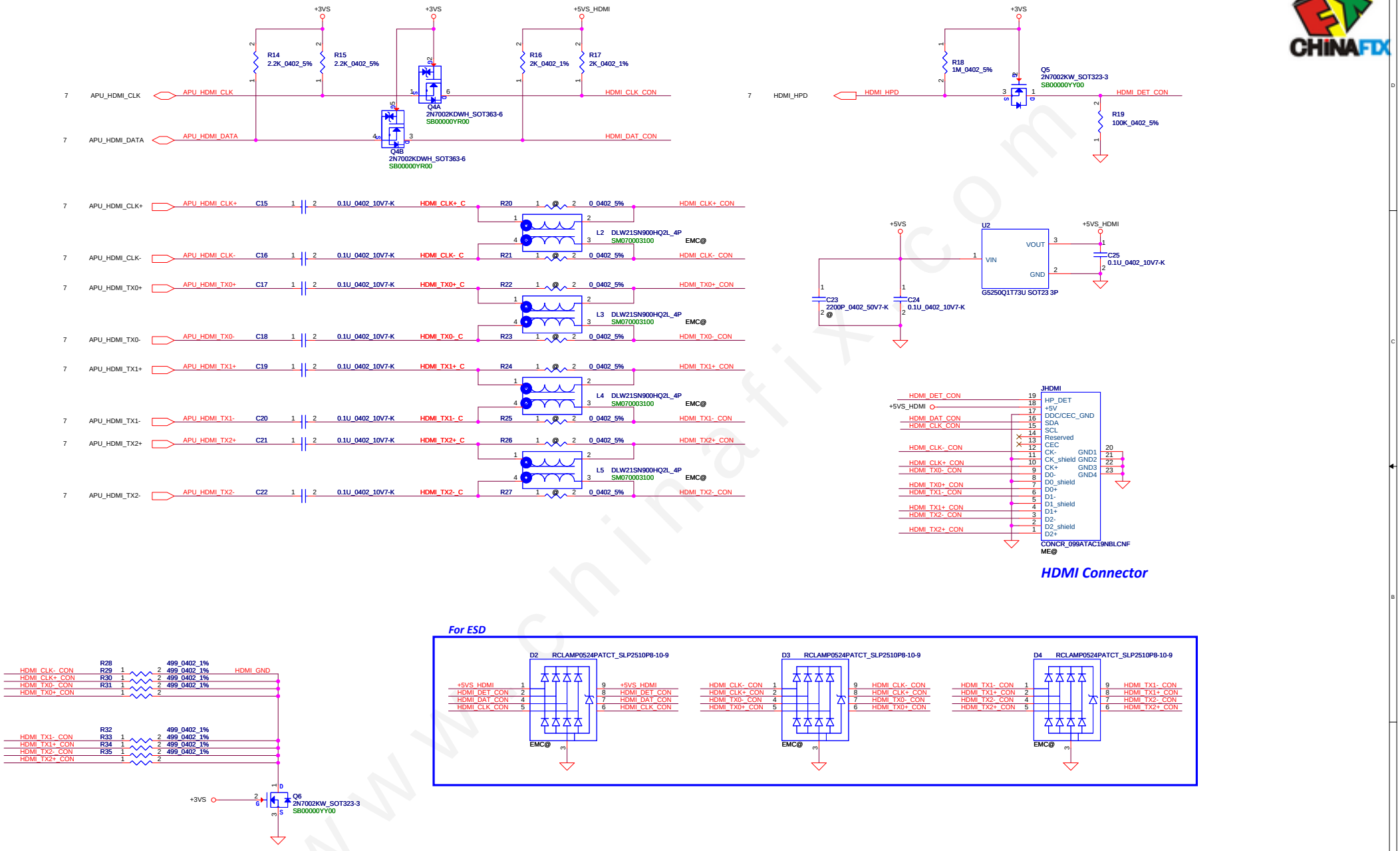

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Title: HDMI CONN

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Title

CRT CONN

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Custom	NM-A231	0.2

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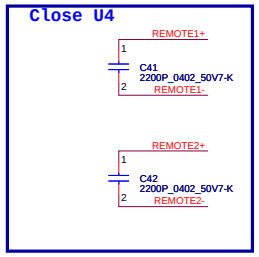
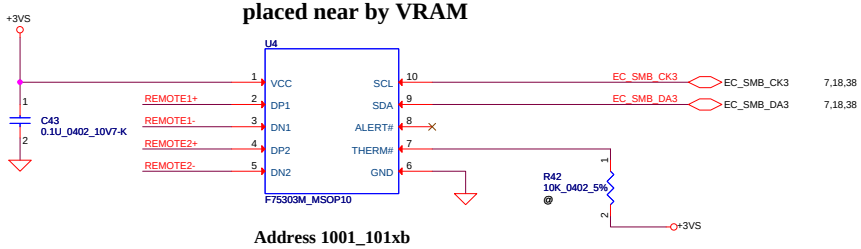
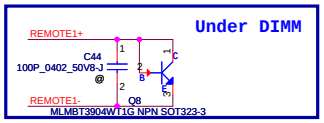


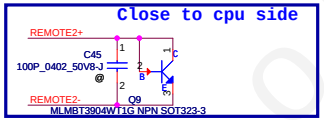
thermal sensor
placed near by VRAM



Address 1001_101xb

internal pull up 1.2K to 1.5V
R for initial thermal
shutdown temp





REMOTE2+/-:
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Trace length:<8"

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Title: *Thermal sensor*

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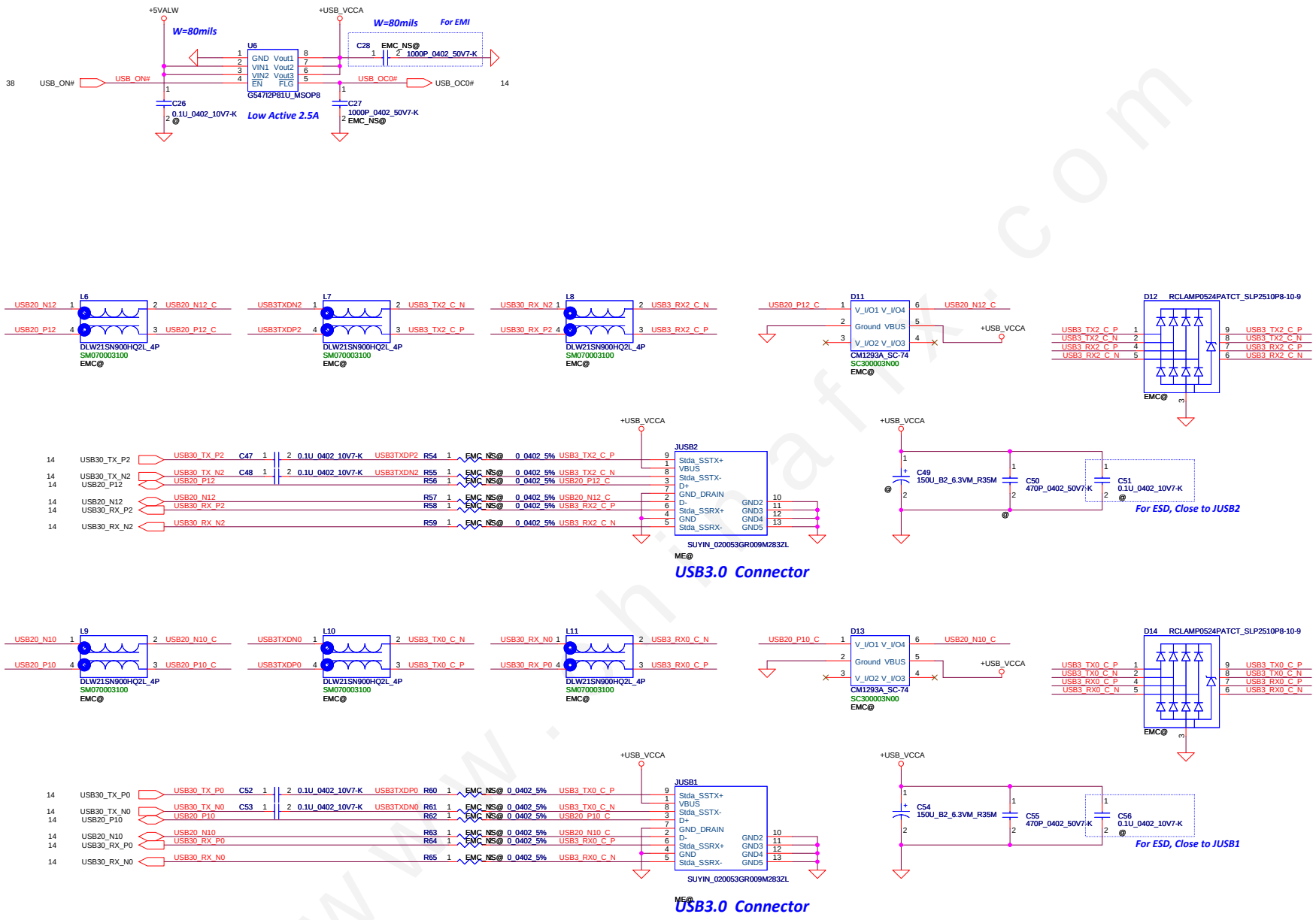

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Title: USB CONN

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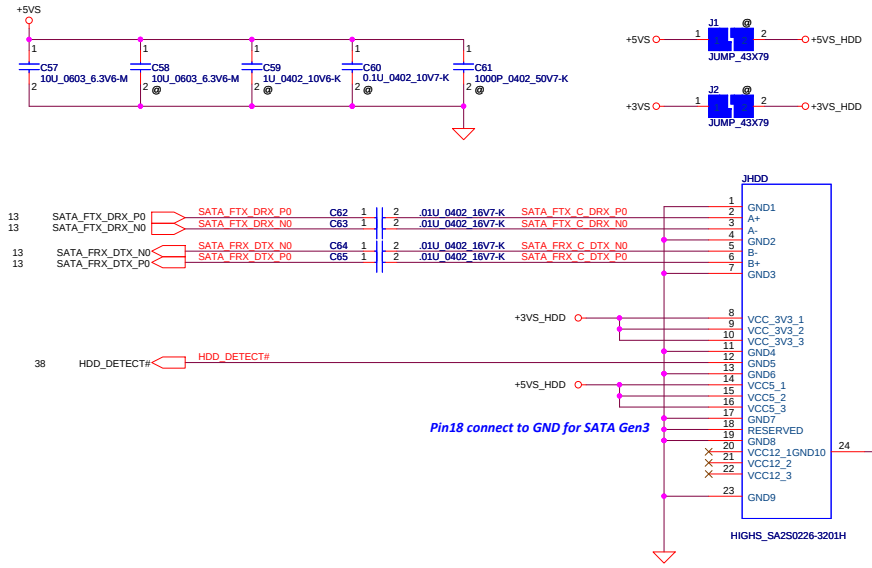
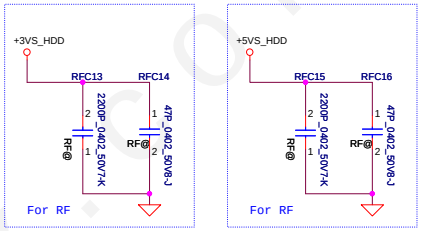
SATA HDD





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Title: HDD/ODD CONN

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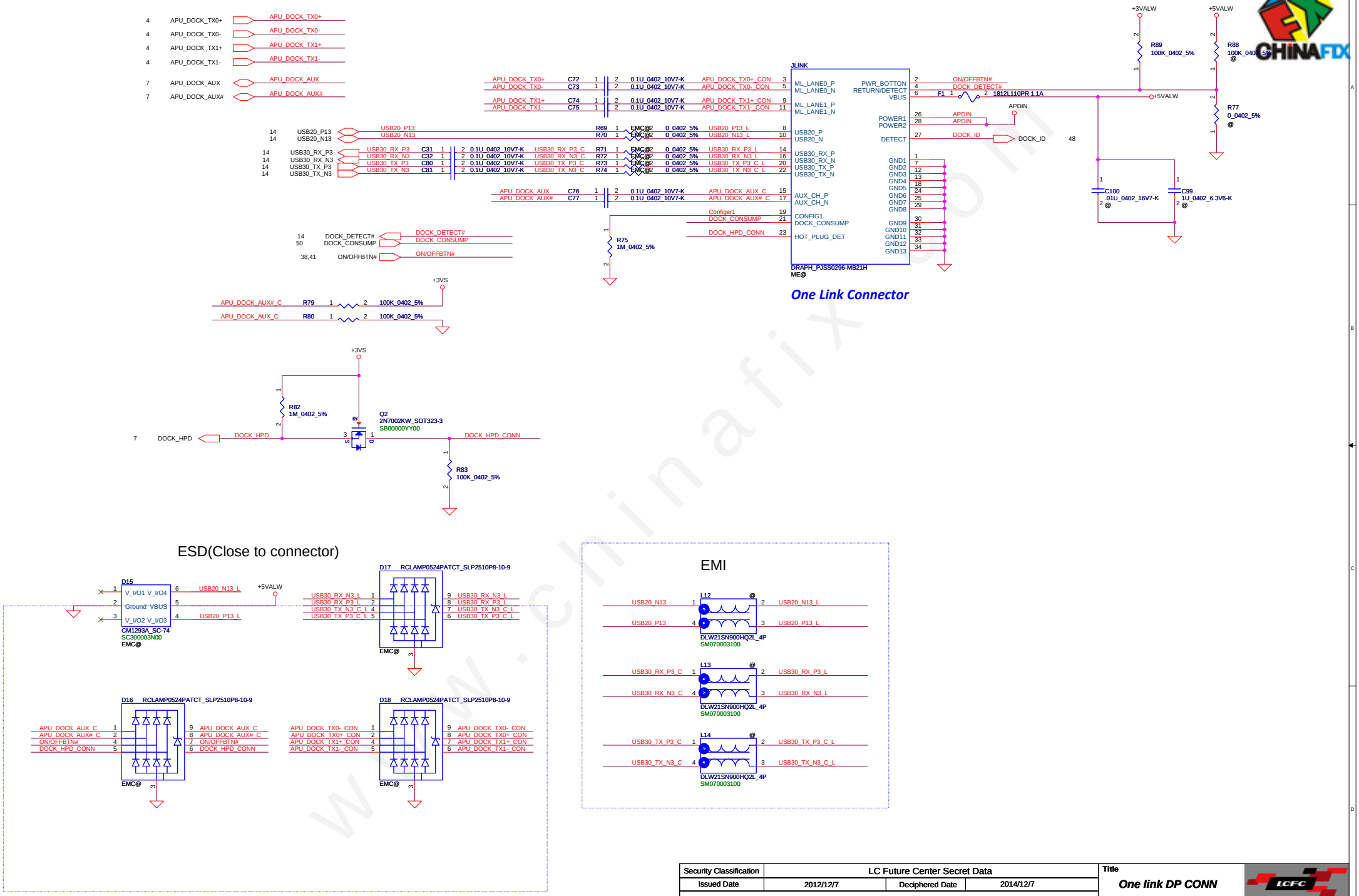

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Title: **One link DP CONN**

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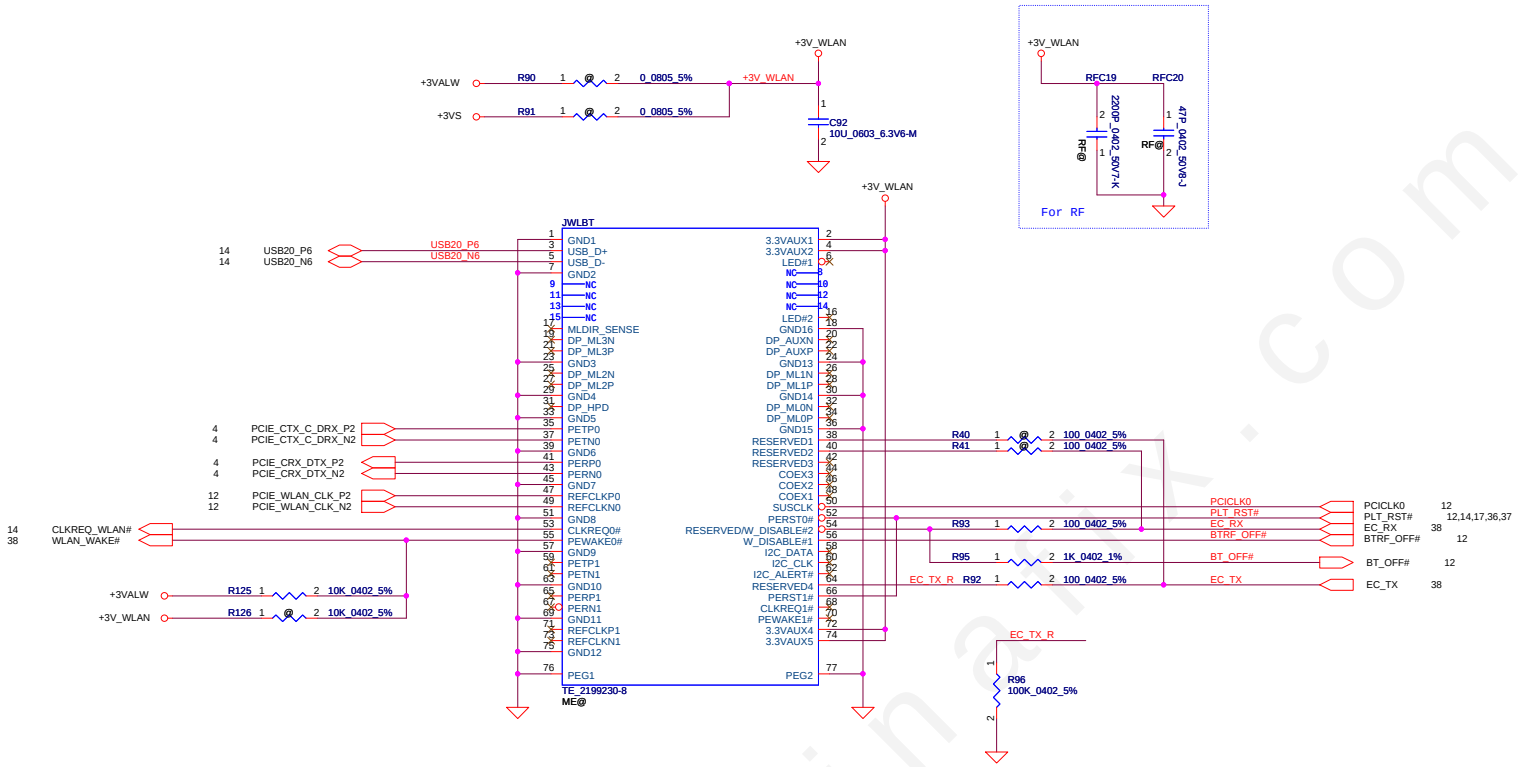
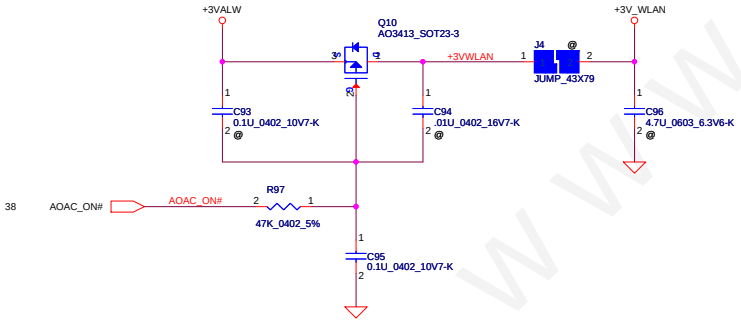
NGFF typeA Card(WLAN)



1. softstart (RC) will check on EVT PCB
2. if AOAC enable +3V_WLAN always ON
if AOAC disable +3V_WLAN is same as +3VS

+3VALW to +3V_WLAN



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Title: NGFF TYPEA WLAN CARD

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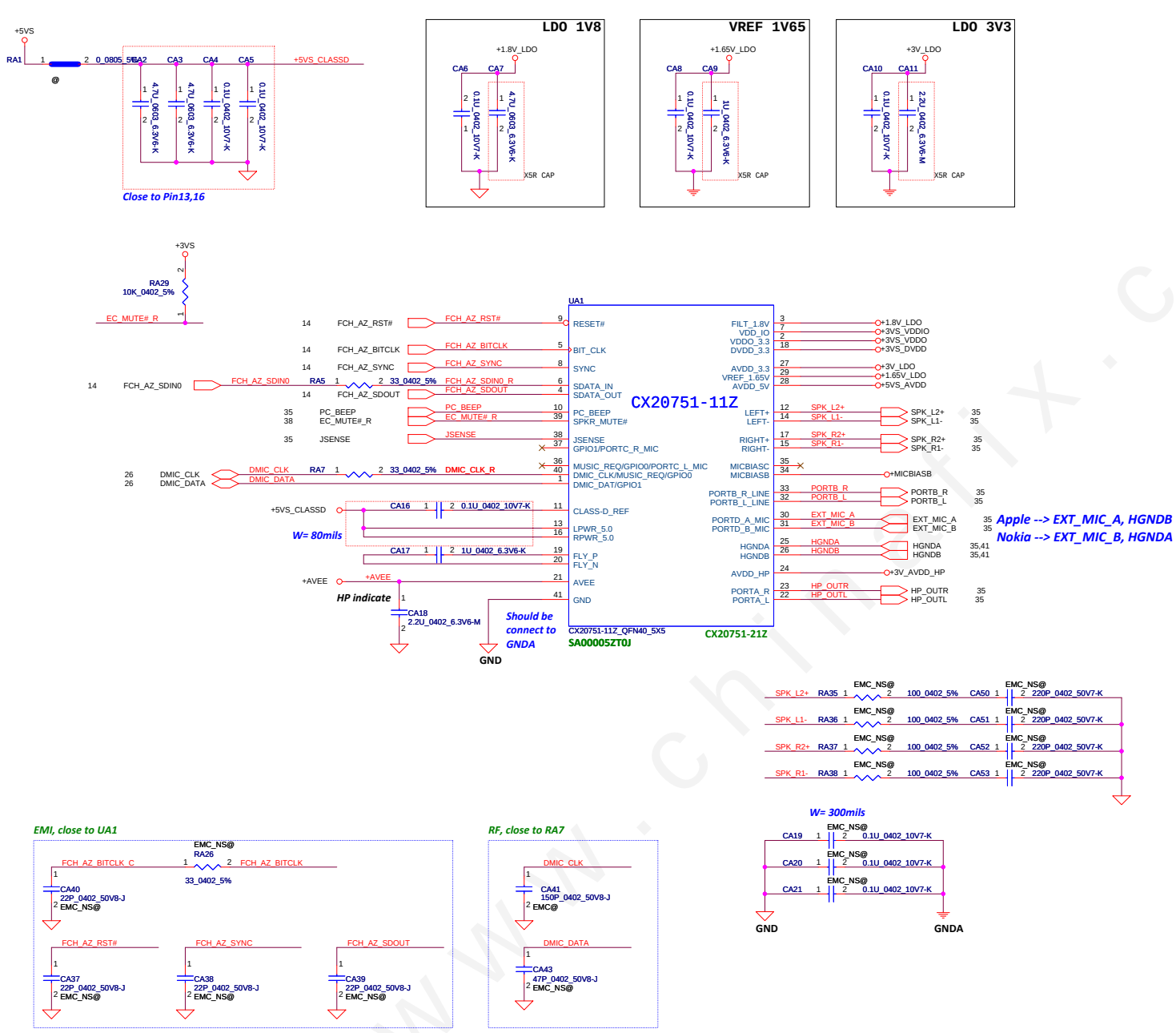

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Issued Date	2012/12/05	Deciphered Date	2014/12/05

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Title: HDA-CX20751

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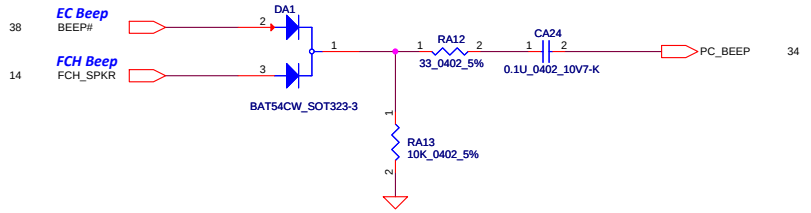
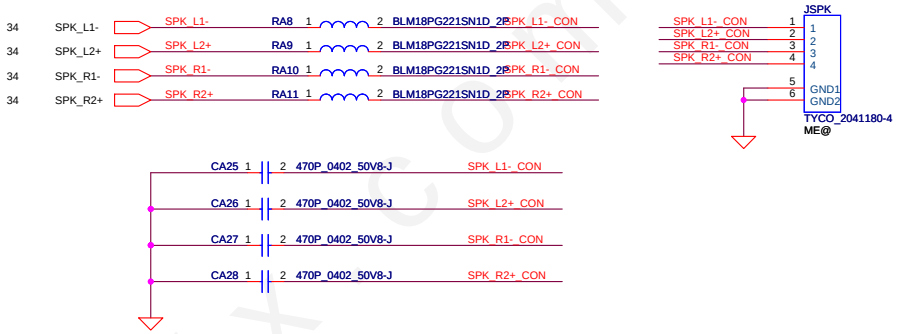
PC Beep



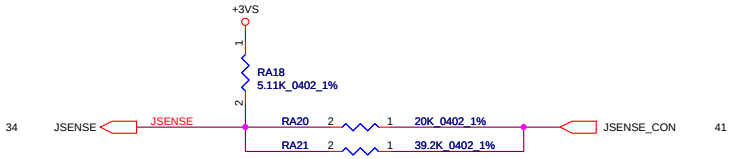
Speaker



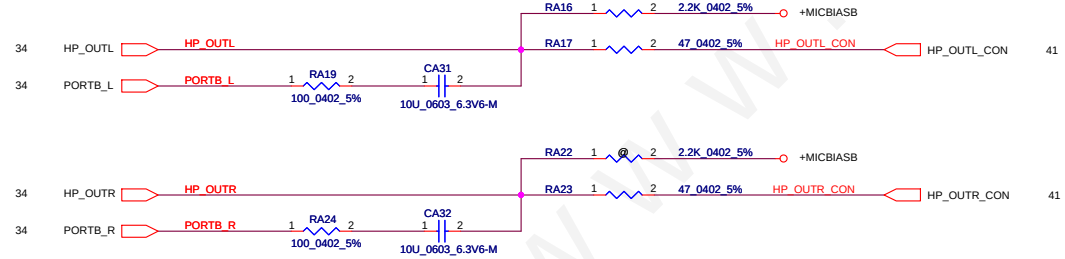
EXT. MIC/LINE IN

Apple --> EXT_MIC_A, HGNDB
Nokia --> EXT_MIC_B, HGNDA

Changed CA29 & CA30 from 1uF to 2.2uF/X5R to meet Port-D(headset-Mic) THD+N <= -65 dB



HeadPhone/LINE OUT



CA31, CA32 change to 4.7U for Quality requirement

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Title: HDA-HP/EXT MIC/SPK CONN

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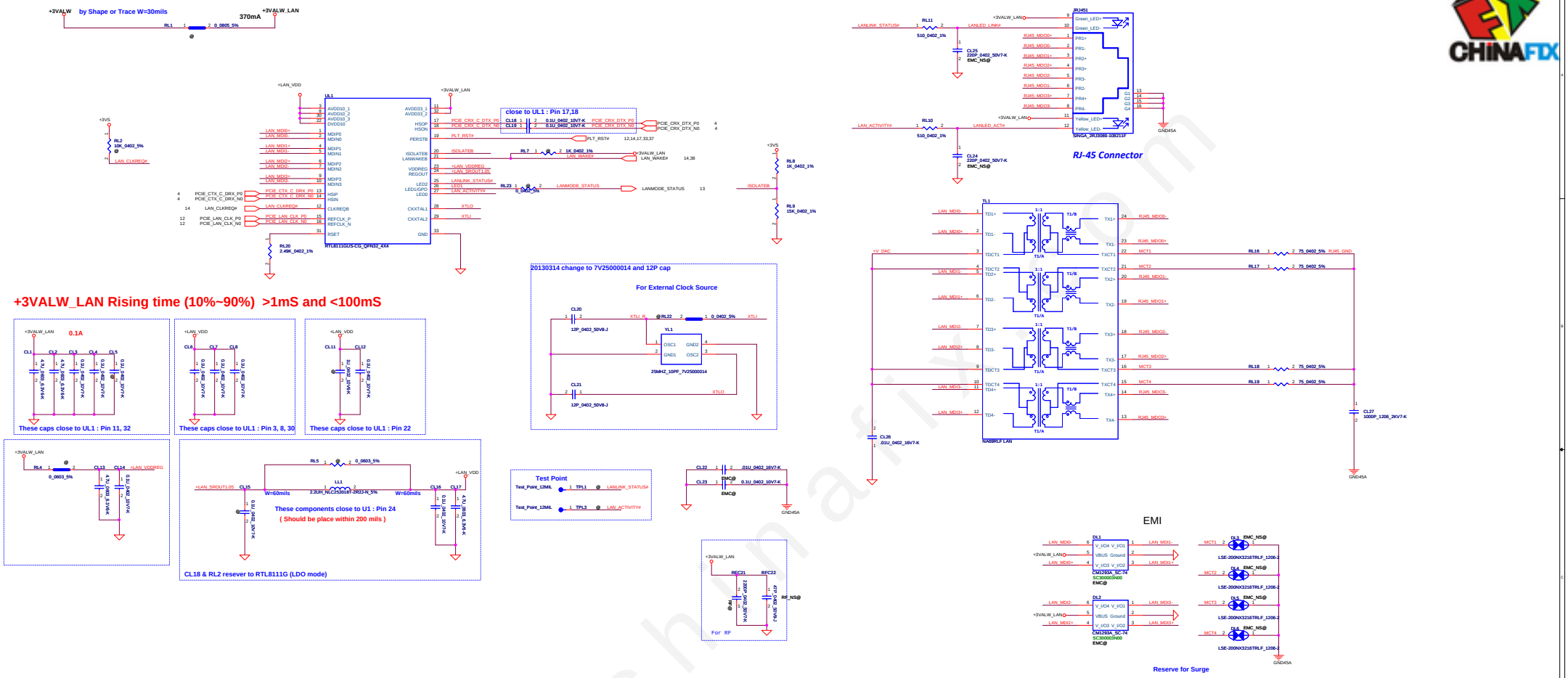

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Title: LAN/RJ45 CONN

Size: D | Document Number: NM-A231 | Rev: 0.2

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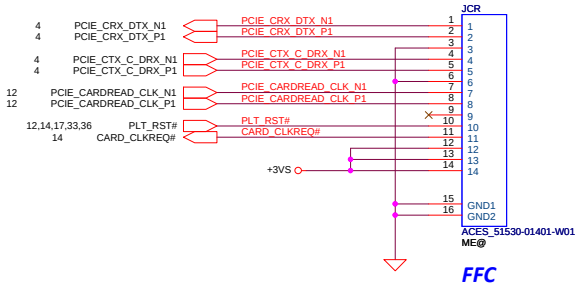
Only for Edge 14"



FFC

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Title: **Card Reader**

Size: Custom | Document Number: NM-A231 | Rev: 0.2

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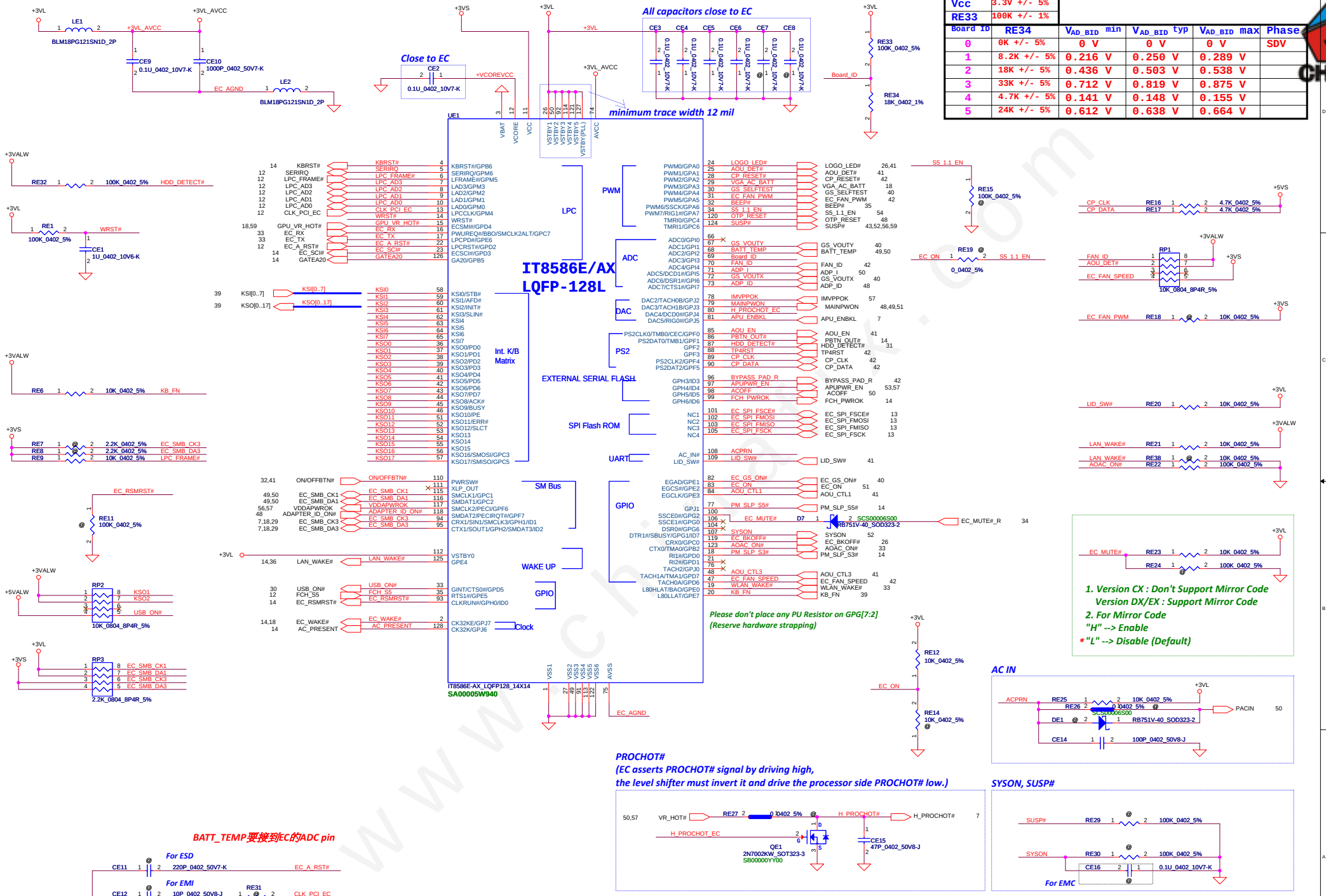
Vcc	3.3V +/- 5%				
RE33	100K +/- 1%				
Board ID	RE34	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	



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Title: EC_IT8586E/FX

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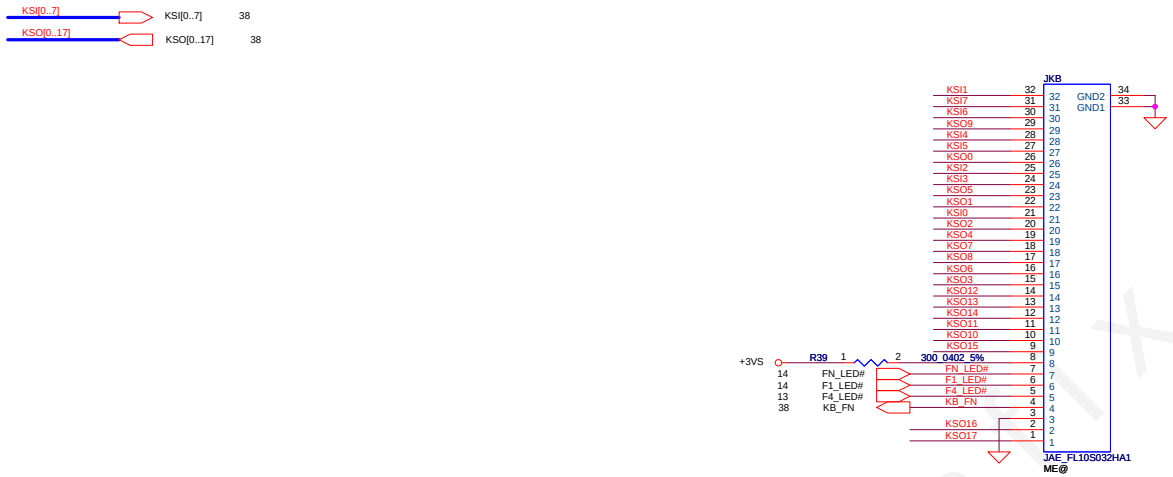
KeyBoard CONN.(14")



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Title: KB

Size: Custom | Document Number: NM-A231 | Rev: 0.2

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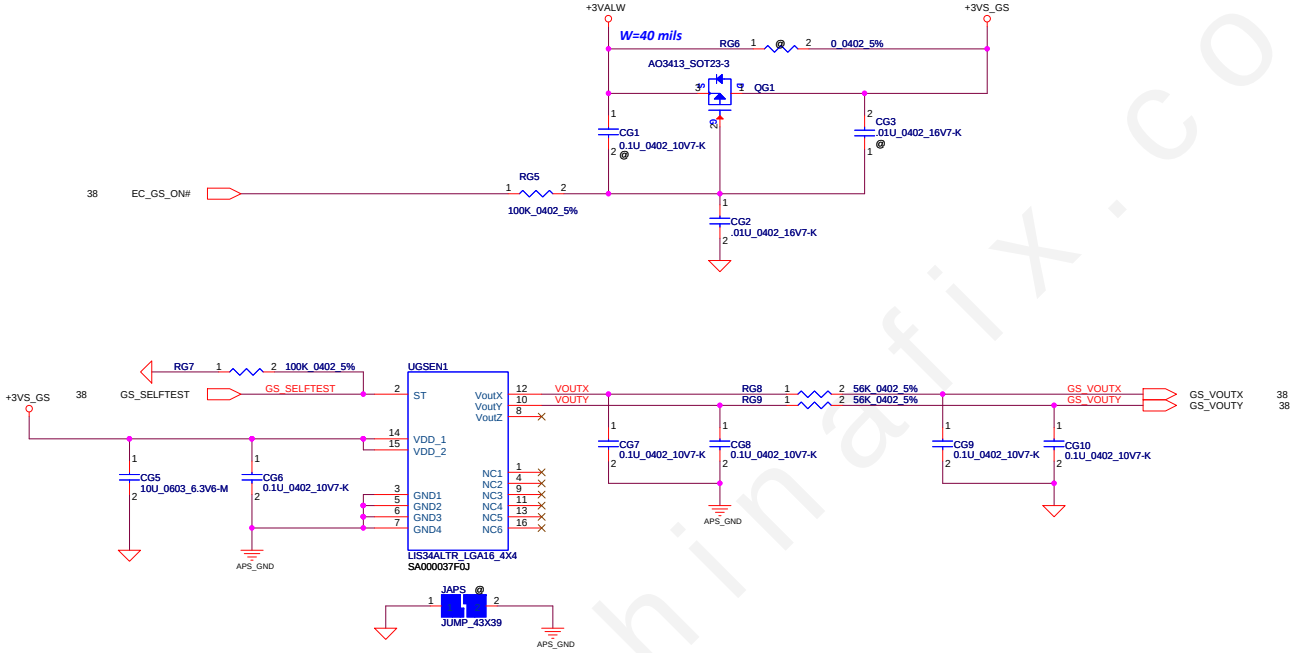
APS G-Sensor



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Title: APS G-SENSOR

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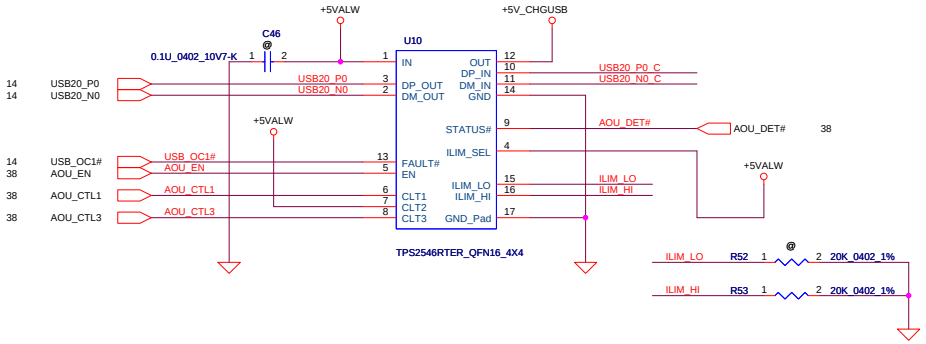
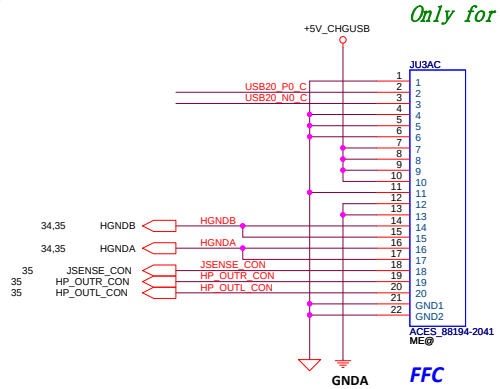
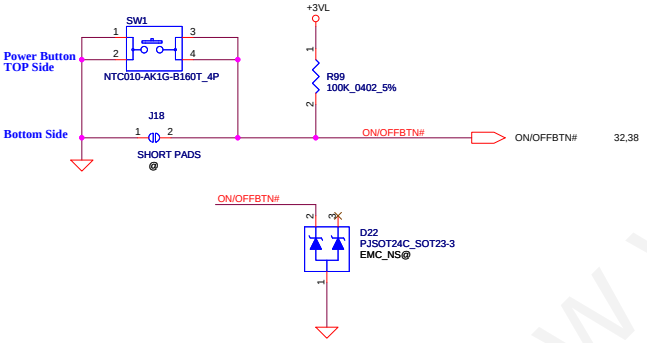




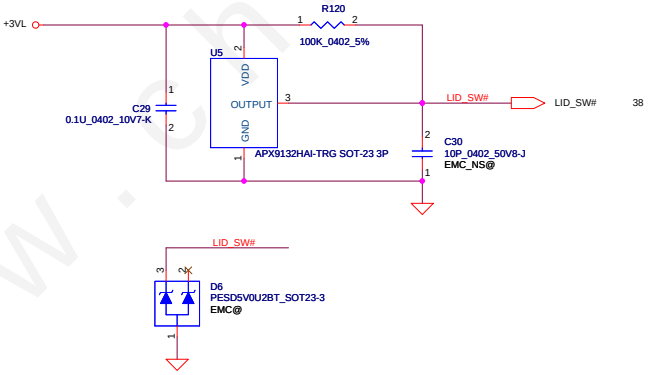
Power Button

ON/OFF switch

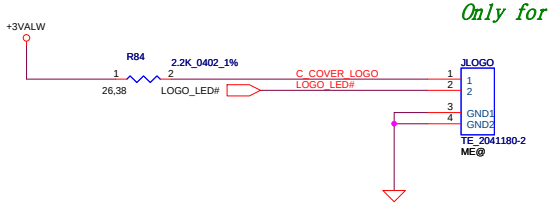


Only for Edge 14"

Lid Switch



Only for Edge 14"



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Title: Sub-board/Power Button

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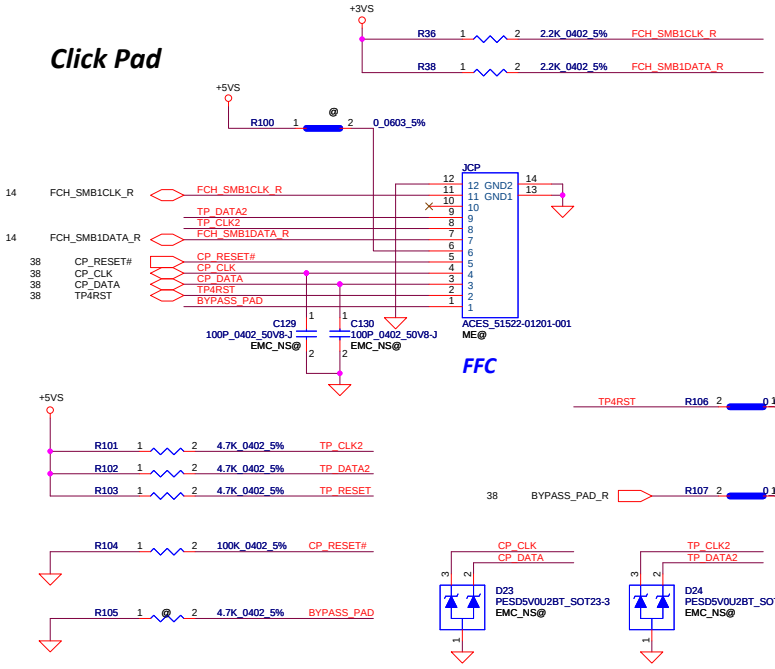
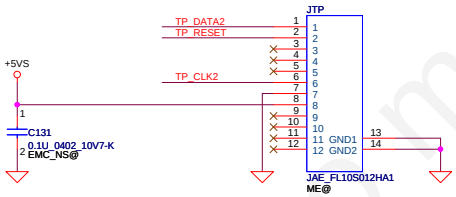
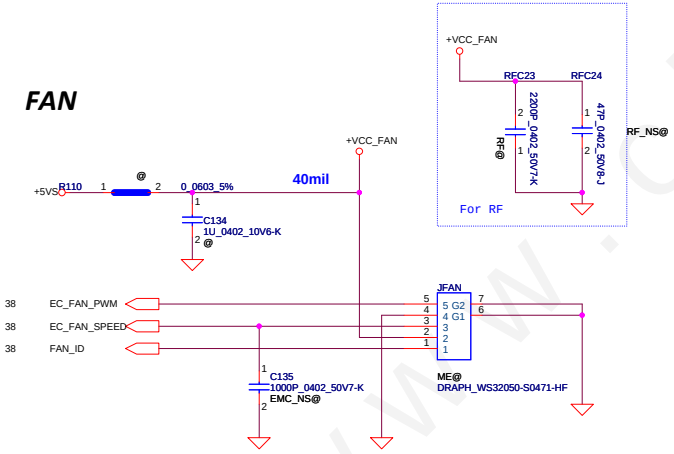
Click Pad



Track point



FAN



FingerPrint

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Title: CP/TP/FAN/FP CONN

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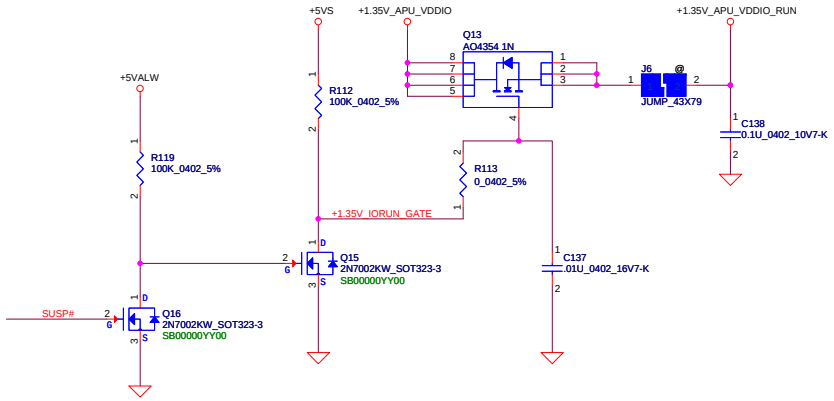
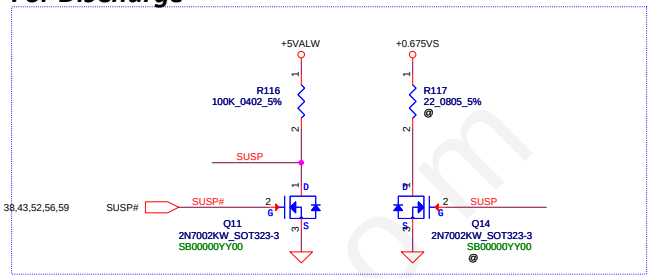
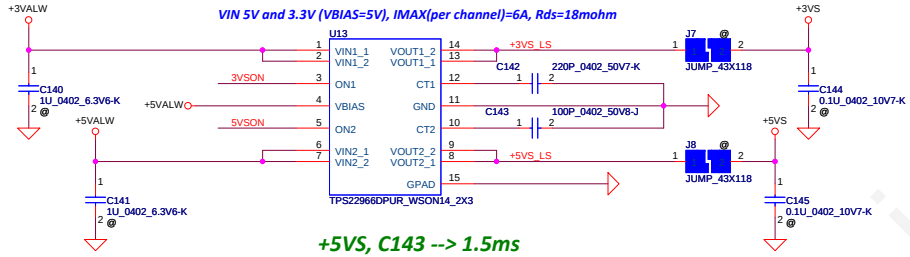
+VDDIO to +VDDIO_RUN



For DisCharge

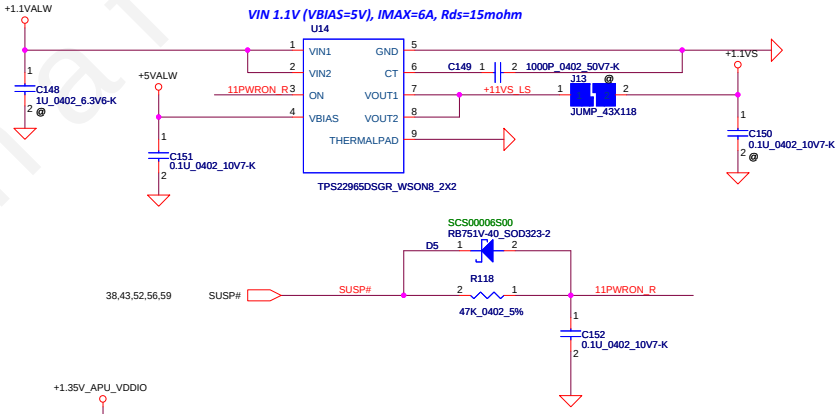


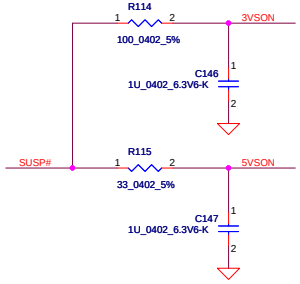
+5VALW To +5VS
+3VALW To +3VS

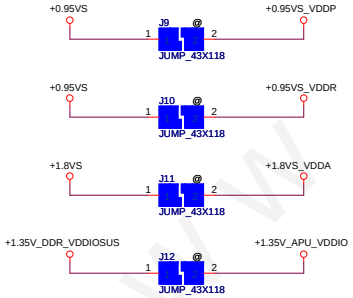


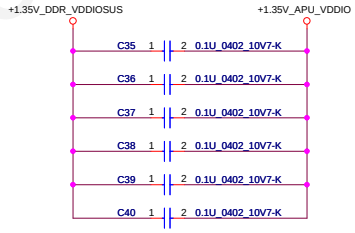
+5VS, C143 --> 1.5ms
+3VS, C142 --> 2.5ms

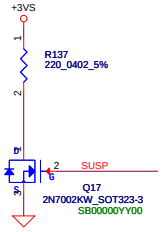
+1.1VALW to +1.1VS











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Title: 3VS/5VS/1.1VS/VDDIO_RUN

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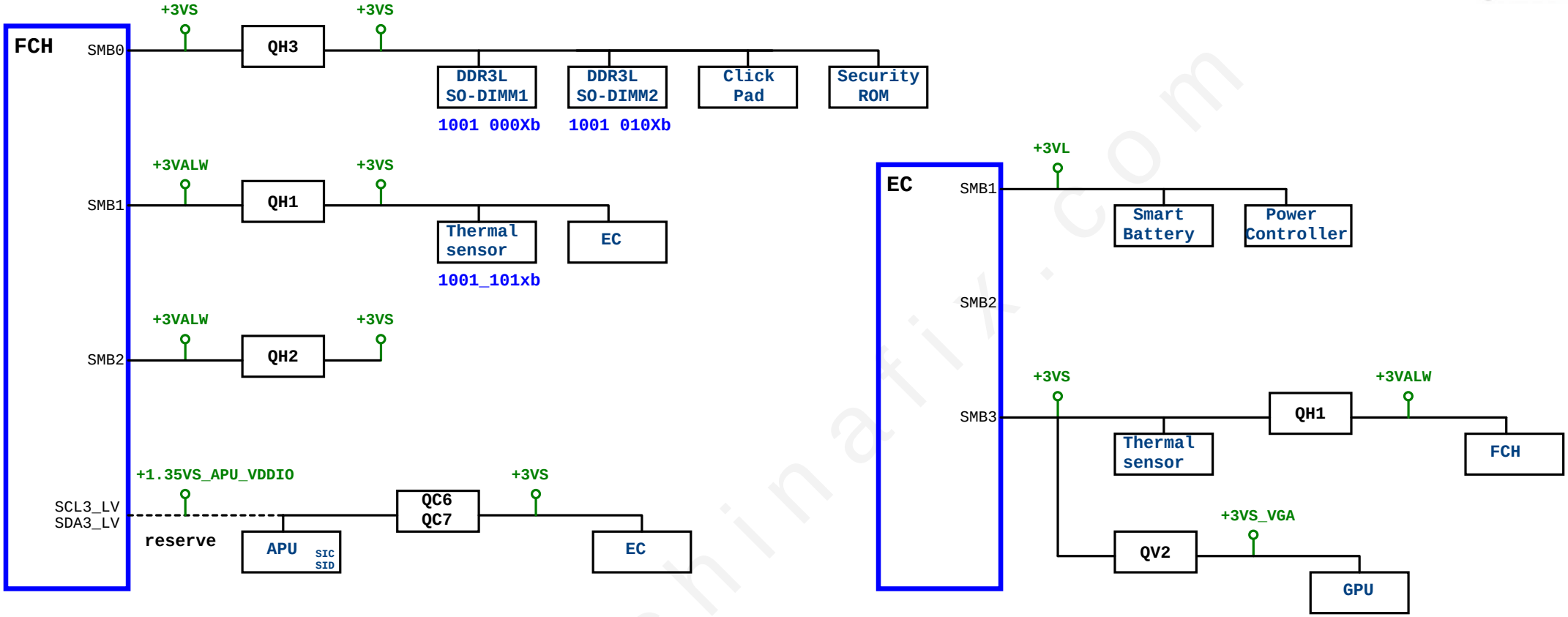
SMBus block diagram



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Title: SMBUS Block Diagram

Size: Custom | Document Number: NM-A231 | Rev: 0.2

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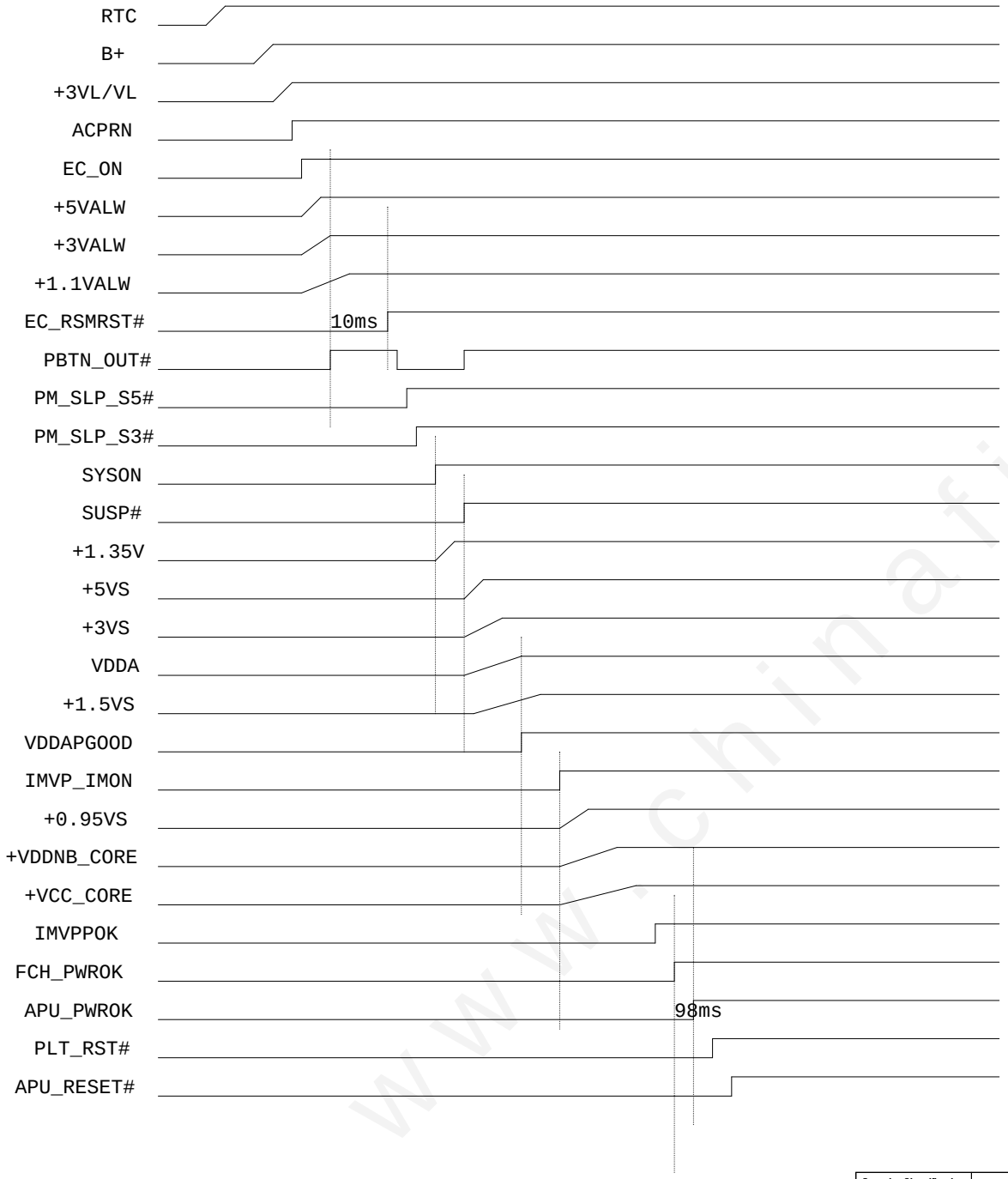

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Title: **Power Sequence**

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Only for Edge 14" SCREW LOCATION

H17
PAD_C8P0D2P5

H16
PAD_C8P0D2P5

H15
PAD_CT6P0SHAPEB8P0X6P65D2P5

H6
PAD_CT8P0B6P0D3P3

H5
PAD_CT8P0B6P0D3P3

H7
PAD_CT8P0B6P0D3P3

H18
PAD_shapeT8P0X10P5CB8P0D2P5

H20
PAD_C6P0D3P3

H19
PAD_CT8P0B6P0D3P3

H1
PAD_CT8P0B6P0D3P3

H2
PAD_CT8P0B6P0D3P3

H14
PAD_shapeT8P0X10P5CB8P0D2P5

H22
PAD_C2P3D2P3N

H8
PAD_C8P0D2P5

H21
PAD_CT8P0B6P0D3P3

H3
PAD_CT8P0B6P0D3P3

H4
PAD_CT8P0B6P0D3P3

H23
PAD_O2P3X3P5D2P3X3P5N

H9
PAD_C5P0D2P5

H12
PAD_C8P0D2P5

H13
PAD_C6P0D2P3

H24
PAD_O2P3X3P5D2P3X3P5N

H10
PAD_CT8P0B6P0D2P5

H11
PAD_C6P0D2P3

H26
PAD_O2P7X3P9D2P7X3P9N

PCB Fedical Mark PAD

FD1 FD2 FD3 FD4 FD5 FD6

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Title: SCREW

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POWER MAP

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Title: Power Map

Size	Document Number	Rev
Custom	NM-A231	0.2

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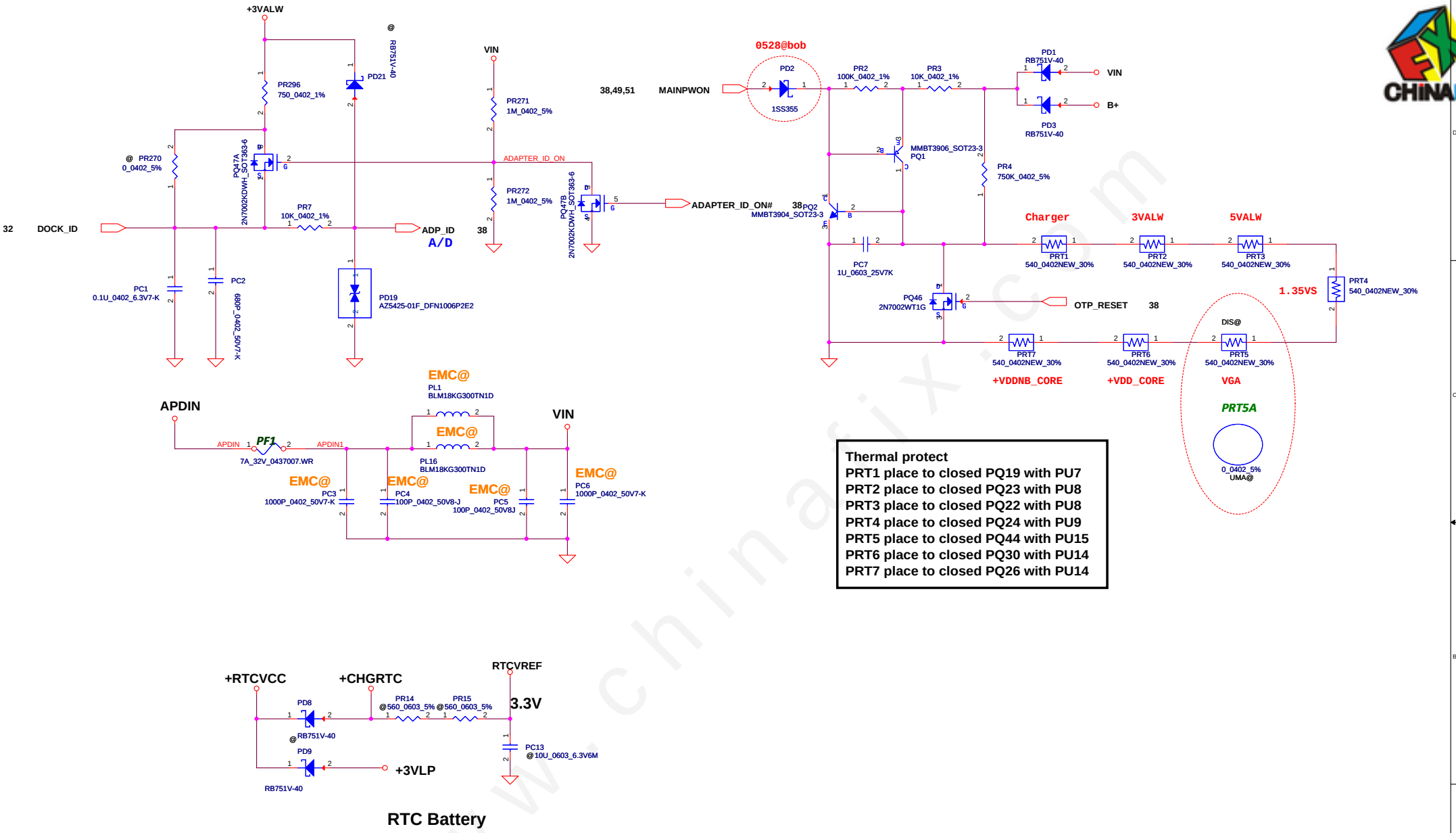

Thermal protect
PRT1 place to closed PQ19 with PU7
PRT2 place to closed PQ23 with PU8
PRT3 place to closed PQ22 with PU8
PRT4 place to closed PQ24 with PU9
PRT5 place to closed PQ44 with PU15
PRT6 place to closed PQ30 with PU14
PRT7 place to closed PQ26 with PU14

RTC Battery

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Title: *DCIN / Vin Detector*

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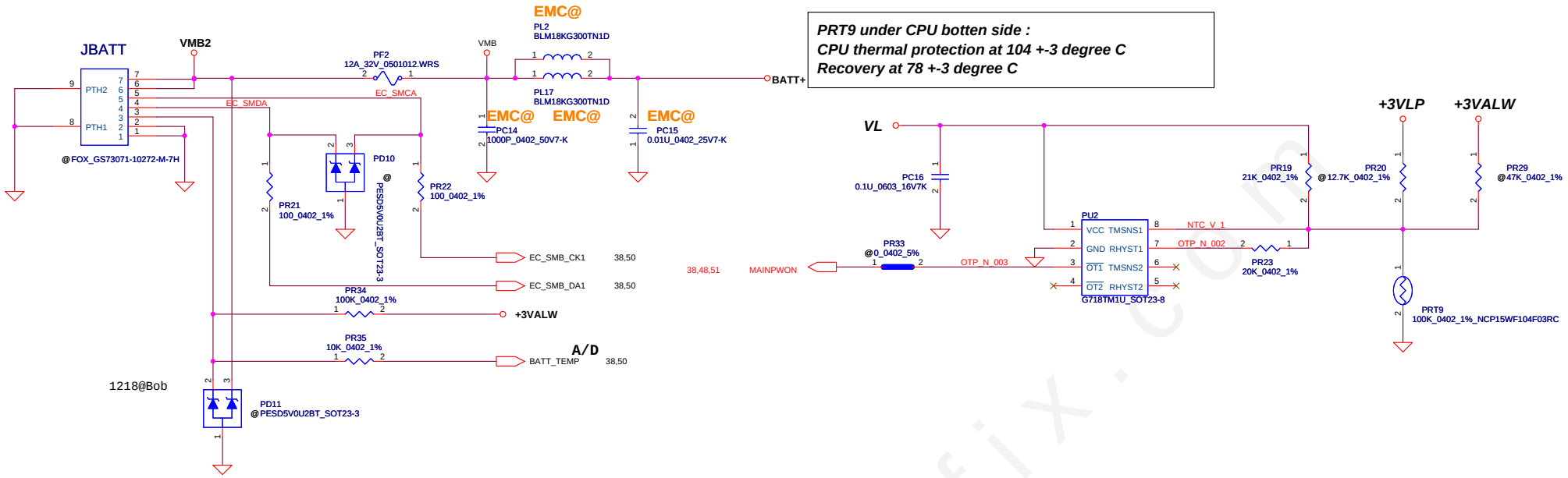

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Title: BATTERY CONN/OTP

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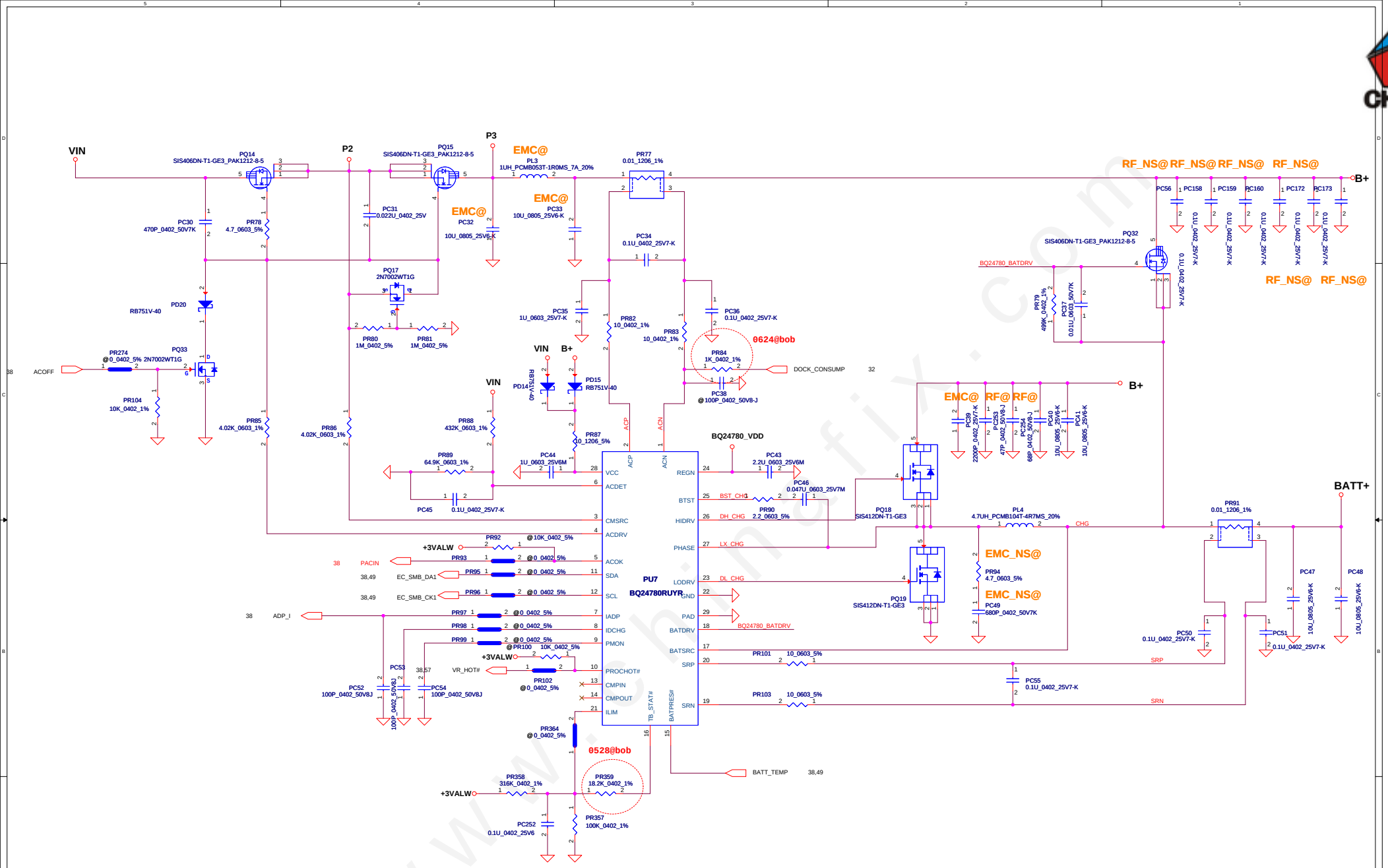

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Title: CHARGER

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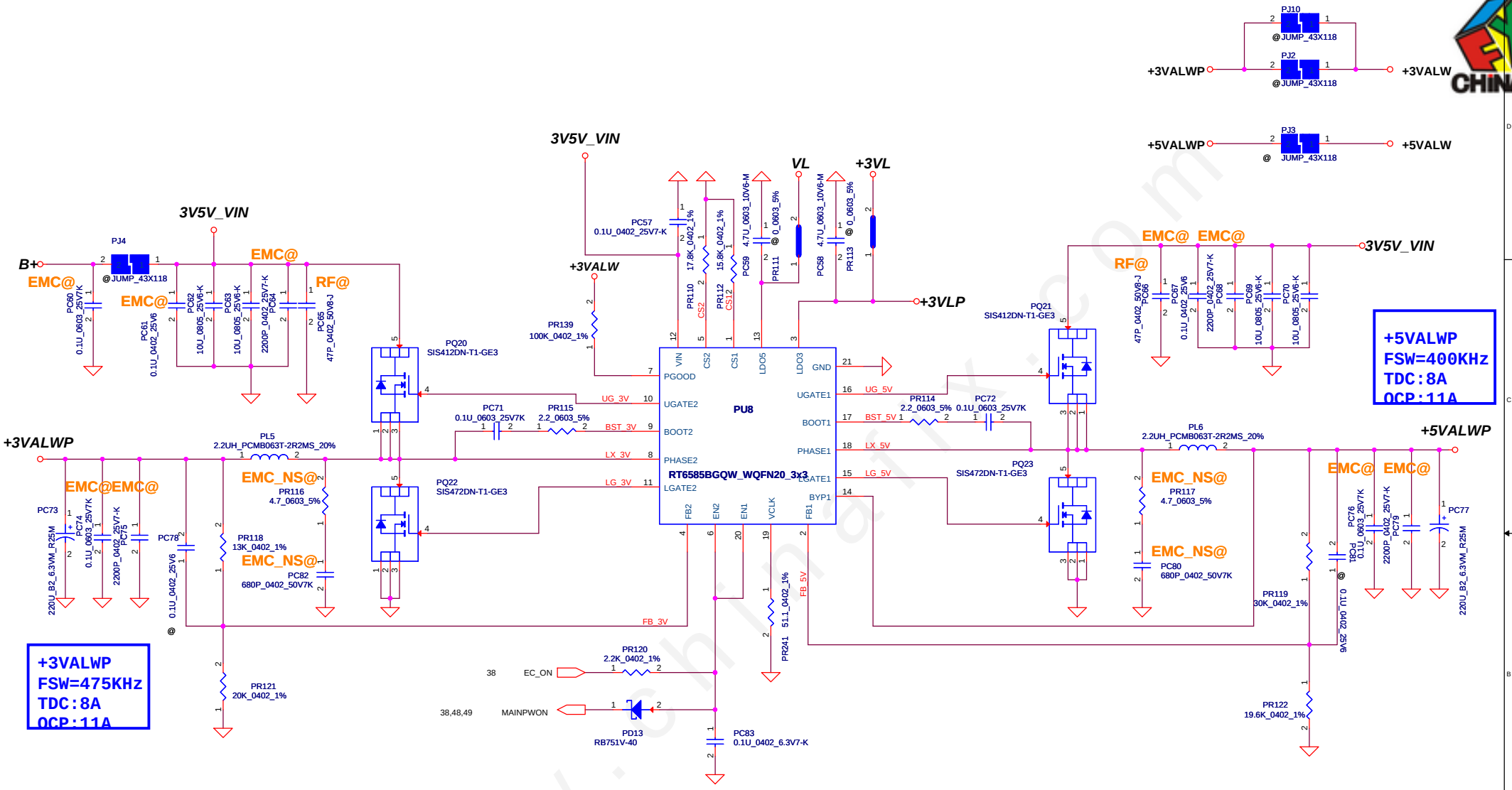

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Title: 3VALWP/5VALWP

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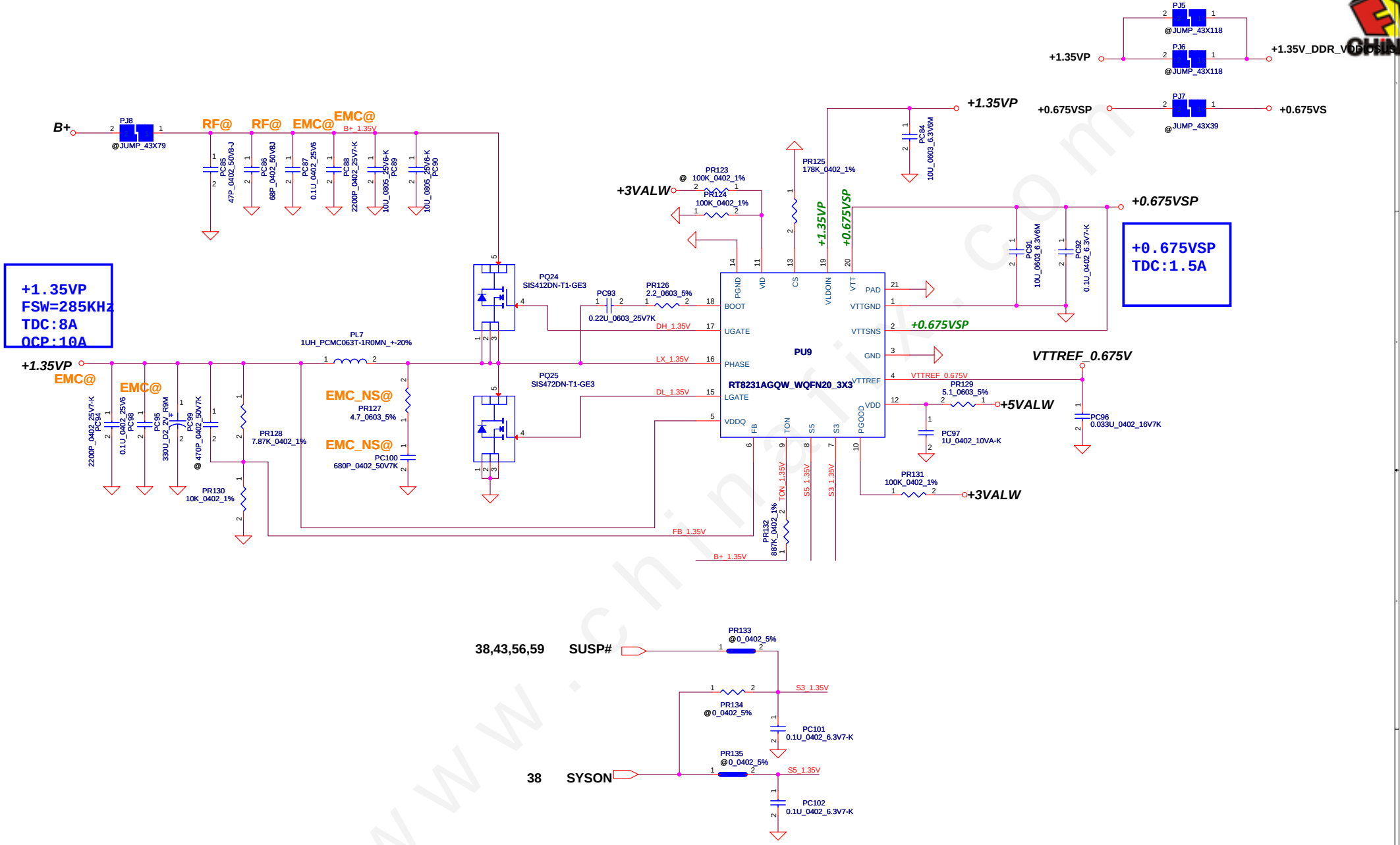

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Title: +1.35VP/+0.675VSP

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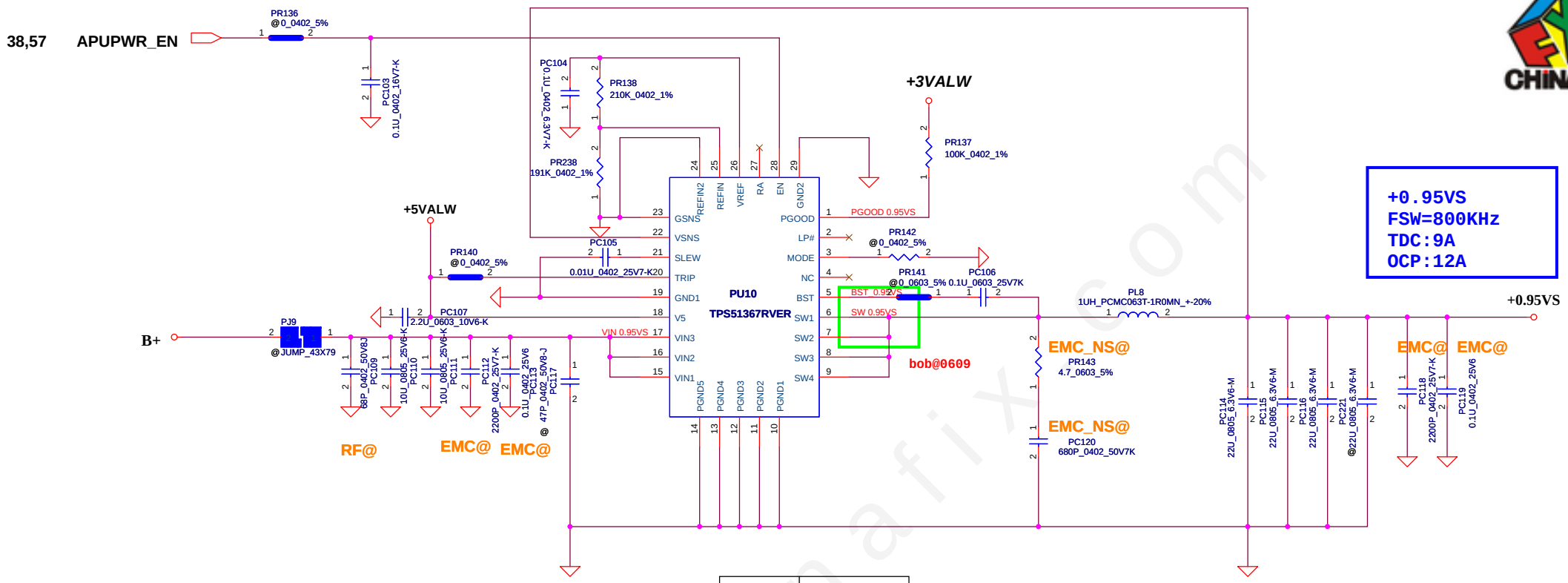

Mode	Frequency
GND	400KHz
Float	800KHz

J9,J10 at EE side

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Issued Date	2013/08/01	Deciphered Date	2014/08/01

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Title: +0.95VS

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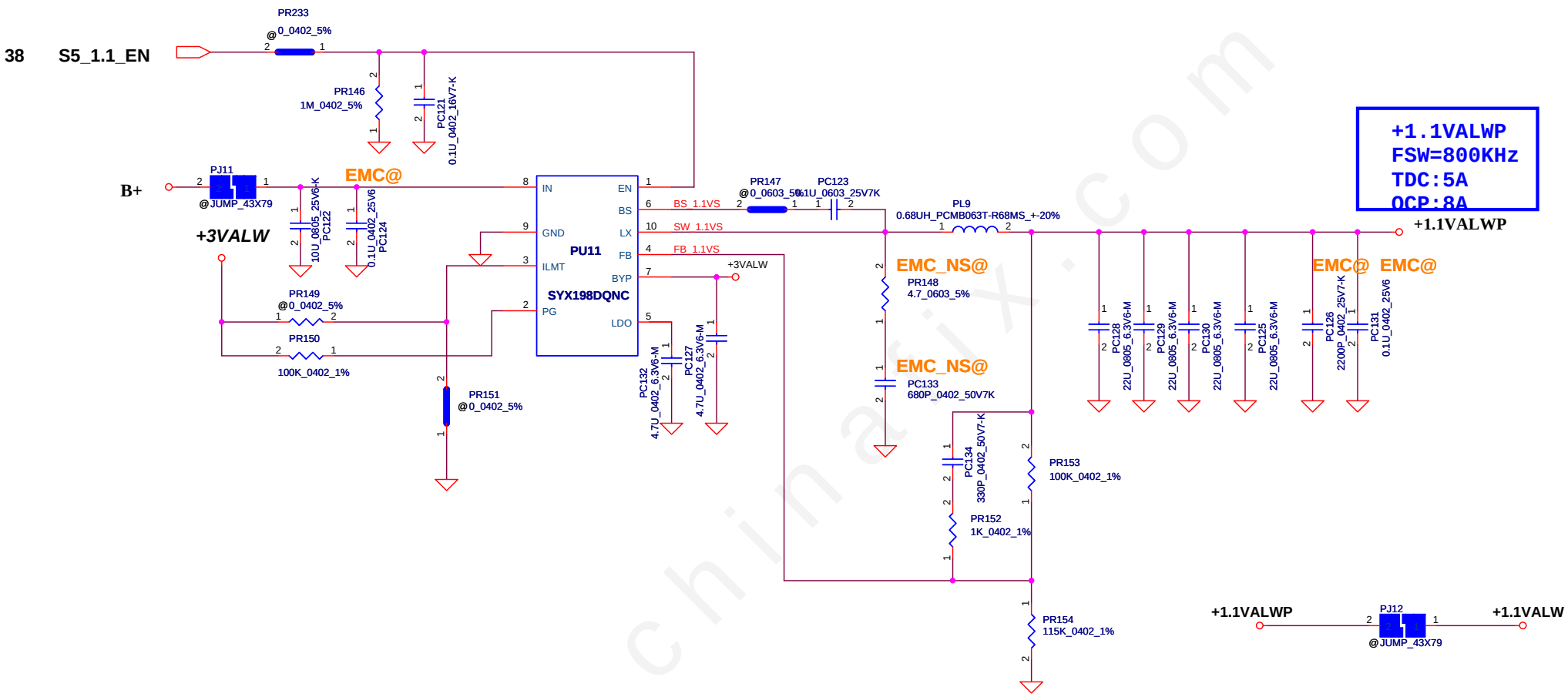

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Title: +1.1VALWP

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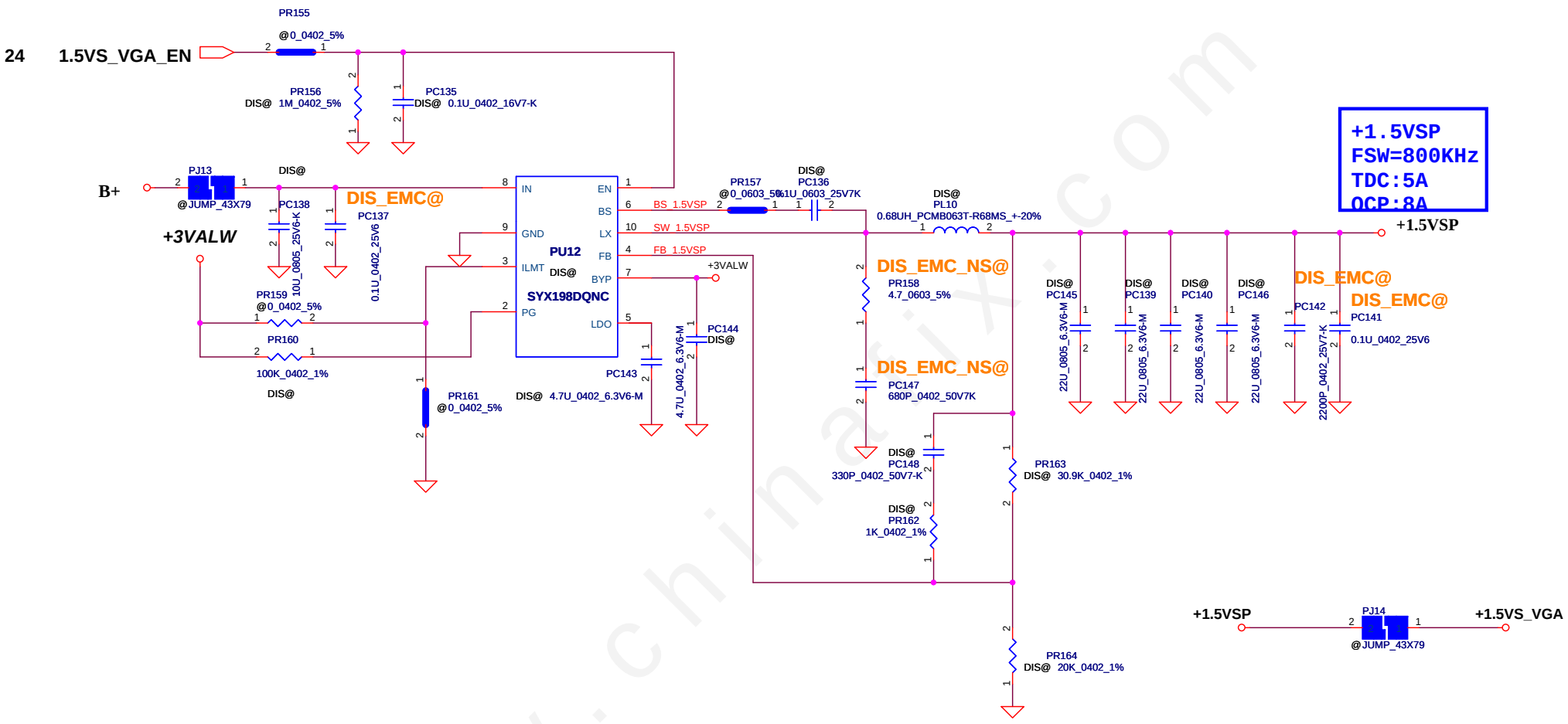

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Title: +1.5VSP

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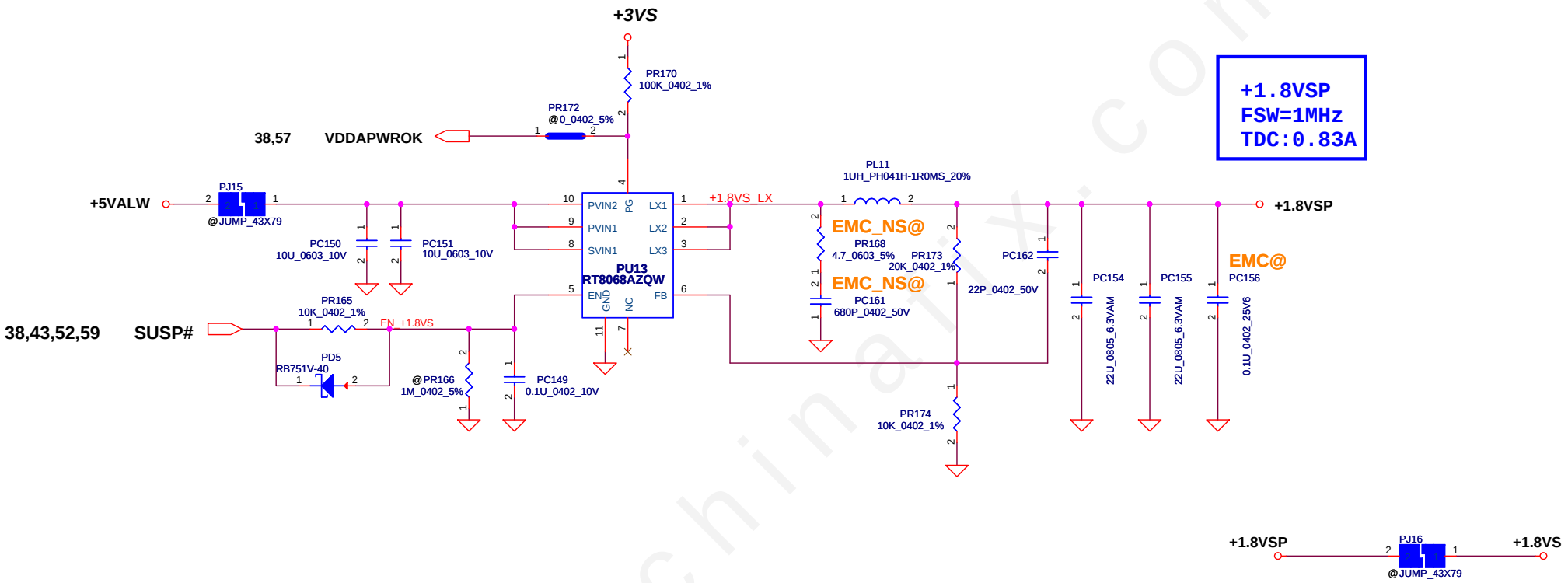

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Title: +1.8VSP

Size: B | Document Number: NM-A231 | Rev: 0.2

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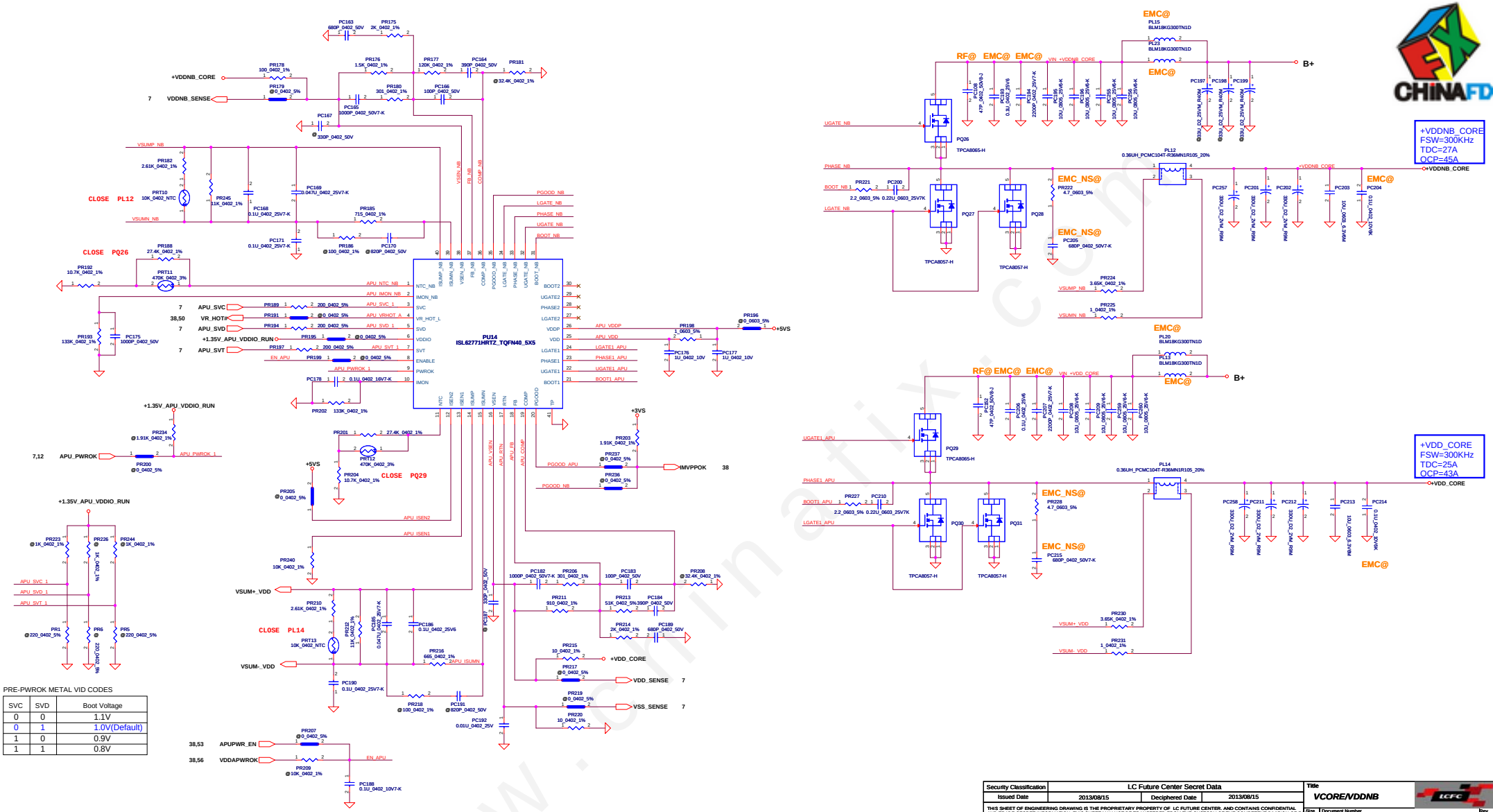

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V(Default)
1	0	0.9V
1	1	0.8V

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Title: VCORE/VDDNB

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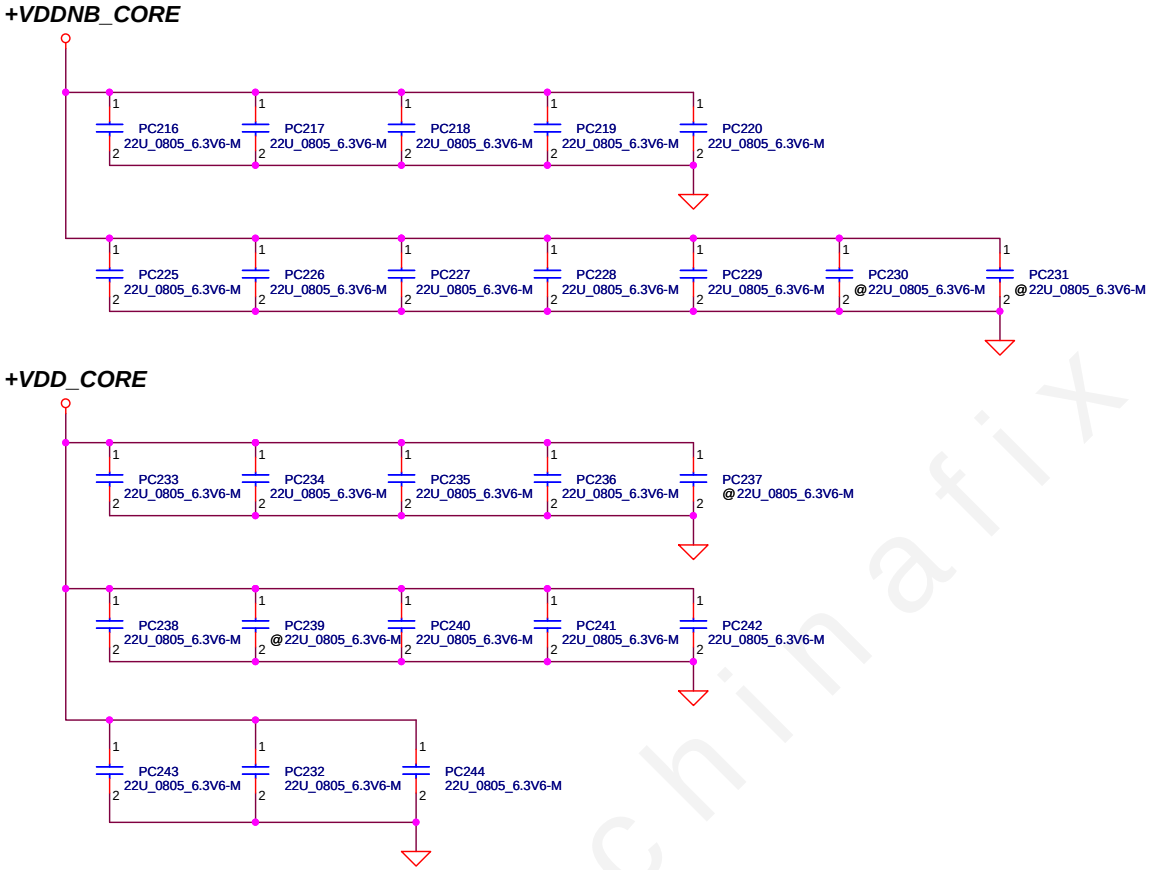

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Title: VCCCPUCORE DECOUPLING

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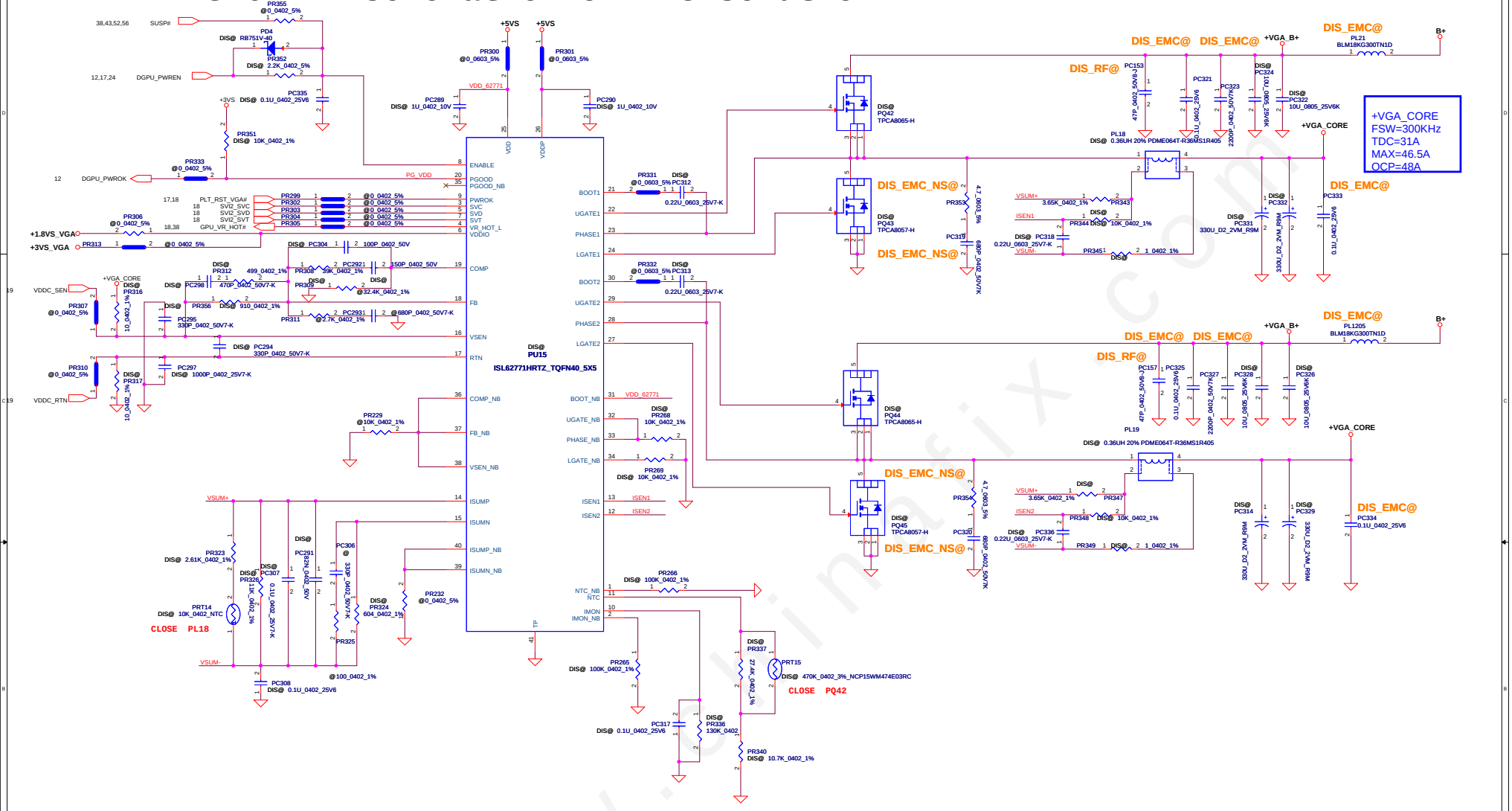
ISL62771 Schematic for FT3 solution



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Title: +VGA_CORE

Size: A3 | Document Number: NM-A231 | Rev: 0.2

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Item	Reason for change	PG#	Modify List	Date	Phase
1	GPU power sequence tuning	24 12	1.RV132 from 20K ohm change to 3.3K ohm 2.CV165 from 1000PF change to 820PF 3.RV129 from 51K ohm change to 180K ohm 4.RV133 from 47K ohm change to 240K ohm 5.Add DV5 6.RH145 pull down to 1K ohm 7.change RH35 to @ 8.reserver GPU core discharge circiut(RV144, RV143,QV13)	2013.12.26	FVT
2	del double component	38	1.Del RE2, RE3	2013.12.26	FVT
3	EMI request	36	1.CL27 change to 2000V	2013.12.26	FVT
4	Common design	14	1.add RH92 to separate	2013.12.26	FVT
5	System power sequence	43	1.add +3VS discharge circuit Q17,R137 2.change D5 to mount form @	2013.12.26	FVT
6	Common design	43	1.RA2 change to @ , Add RA3 connect to 3VL	2013.12.26	FVT
7	ECSL request	40 24	1.SB000007H1J change to AOS AO3413 SB93413000J(QG1, QV5) 2.SB000002R0J change to LRC LMBT3904WT1G SB00000ZJ00 (Q1,Q8,Q9,QC1,QC2,QV3,,QC4,QC5) 3.SE000000KMT change to SE00000X30T(C1,C3,C99,C140,C141,C146,C147,C148, CA9,CA13,CA14,CA15,CA17,CD22,CV163)	2013.12.26	FVT
8	modify SMBus issue	7	1.QC7, QC6 gate G connect to 1.35V run del RC71,RC72	2013.12.26	FVT
9	Cost down component count	38	1.RE30, RE29, RE11 change to @	2013.12.30	FVT
10	Cost down component count	14	1.RH87 change to @	2013.12.30	FVT
11	Cost down	15	1.RH62 change to mount, LH2 change to @	2013.12.30	FVT
12	Cost down component count	18	1.RV75 change to @	2013.12.30	FVT
13	Cost down component count	18	1.RV82, RV83 change to @	2013.12.30	FVT
14	Cost down component count	18	1.RV150, RV151 change to JET@ from @ 2.RV125, RV122 change to @ form DIS@ 3.CV149,CV150,RV96, RV97,RV95,CV152,CV151,UV9 change to @ form JET@	2013.12.30	FVT
15	Cost down component count	26 7	1.R4, RC73,RC74 change to @	2013.12.30	FVT
16	SMBus issue	7	1.add RC21	2013.12.30	FVT
17	ECSL request	7	1.SA00005QN0Jchange to ANPEC APX3132H SA00005Z200	2013.12.30	FVT
18	Cost down component count	7	1.RC17,18,13, 19 del add RP4	2013.12.30	FVT
19	Cost down component count	7	1.RC47,48,49 del add RP5	2013.12.30	FVT
20	Cost down component count	7	1.RC37,38,39,40 del add RP6	2013.12.30	FVT
21	EC_MUTE# leakage issue	38	1.add D6	2013.1.3	FVT

Title	<Title>		
Size C	Document Number <Doc>		Rev <RevCode>
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Item	Reason for change	PG#	Modify List	Date	Phase
23	for EC mirro function	38	add D6,RA29 and RE12 change to mount	2013.01.06	FVT
24	BIOS request	14	change GPIO ipin to G-event 5	2013.01.06	FVT
25	PEG signal EA request	7/17	change PEG capacitor to 0.22u, change to 0.1 u	2013.01.06	FVT
26	reduce component count	7/17	DEL RC45,R66, RH70,RH71,RH72,RH73,RH77,RV136,RW4,RW5,RW7,RW8,RW9,RW10	2013.01.06	FVT
27	FAN Pin define reserve	42		2014.02.24	SIV
28	remove GPU CTF function	18	DEL QV3,CV148,RV87,DV1,RV86,RV88,RV74	2014.02.24	SIV
29	remove Fingerprint	42	DEL R111,D25,C136, JFPB	2014.02.24	SIV
30	DFB issue for L9 issue	30	change C54 form @ to mount	2014.02.24	SIV
31	reduce component count		del 0402 R10 R106 R107 R134 RA28 RC43 RE26 RH6 RH7 RH8 RH9 RH10 RH11 RH12 RH13 RH14 RH15 RH16 RH17 RH44 RH22 RH57 RH58 RH76 RH91 RH98 RH90 RH122 RH125 RH126 RH127 RH128 RH129 RH130 RL22 RV150 RV151 0603 R5 R100 R110 RH78 RH79 RH80 RH81 RL4 0805 R8 R37 RA1 RA3 RA4 RA6 RH62 RH61 RH142 RH143 RL1	2014.02.24	SIV
32	CP SMB issue	14/42	add R36,R38 for SMB pull up	2014.02.24	SIV
33	component reduce	4	CC1~8,CC106~CC113 change to DIS@	2014.05.14	SVT
34	Audio test request	35	CA 31, CA 32 change to 10u form 4.7u	2014.05.28	SVT
35	Power sequence modify	43	C142 change to 220p form 2200p C143 change to 100p form 1000p	2014.05.28	SVT
36	LAN LED function change	36	LANLED_LINK# connect to pin 10 LANLED_ACT# connect to pin 12	2014.05.28	SVT

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Title <Title>		
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