MODEL NAME : VBW01
PROJECT CODE : ANRVBW0100
PCB NO : DA8000WL000 LA-9982P M/B
DA40001FO00 LS-9101P POWER BUTTON/B
DA40001FP00 LS-9102P USB/B
DA40001FQ00 LS-9103P TP BUTTON/B

Dell / Compal Confidential

Schematic Document

Intel Shark Bay ULT
OAK Mainstream2
UMA/DIS AMD Venus Pro

2013-05-29 Rev: 3.0

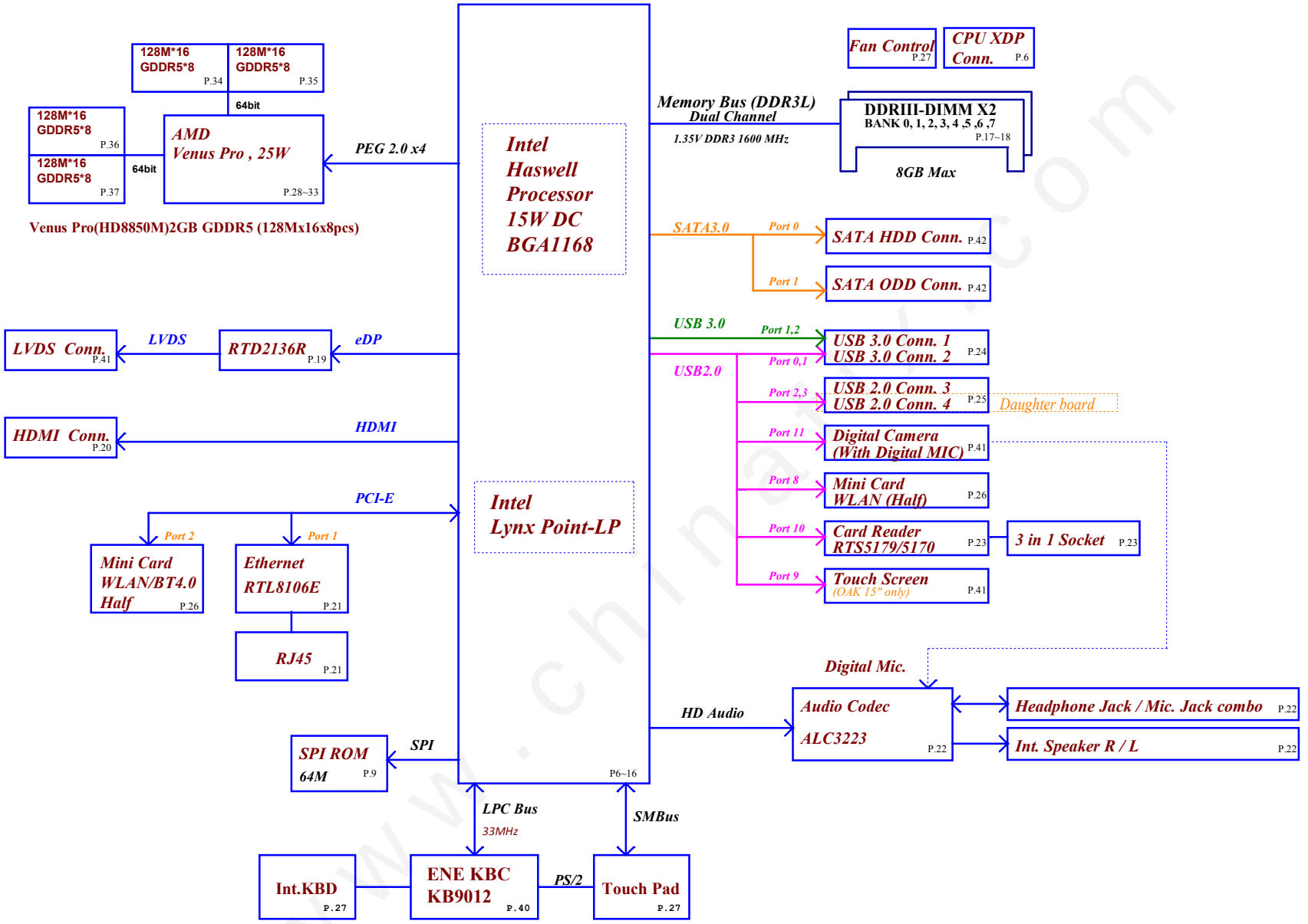
X76@ : 76 level
46@ : 46 level
@ : Nopop component
CONN@ : Connector component
XDP@ : XDP function
UMA@ : Only for UMA
DIS@ : Only for Discrete
VENUS@ : VENUS Pro,VENUS XT
VENUSXT@ : VENUS XT
VENUSPRO@ : VENUS Pro
@VENUS@ : VENUS nopop component
EMI@ : EMI parts
@EMI@ : Reserve EMI parts
ESD@ : ESD parts
RF@ : RF parts

BOM config
UMA : UMA@,EMI@,ESD@,RF@
DIS VENUS : VENUS@,VENUSPRO@,DIS@,EMI@,ESD@,RF

ZZZ R1@
PCB VBW01 LA9982P/LS9101P/LS9102P/LS9103P
DAZ0ZG00120

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

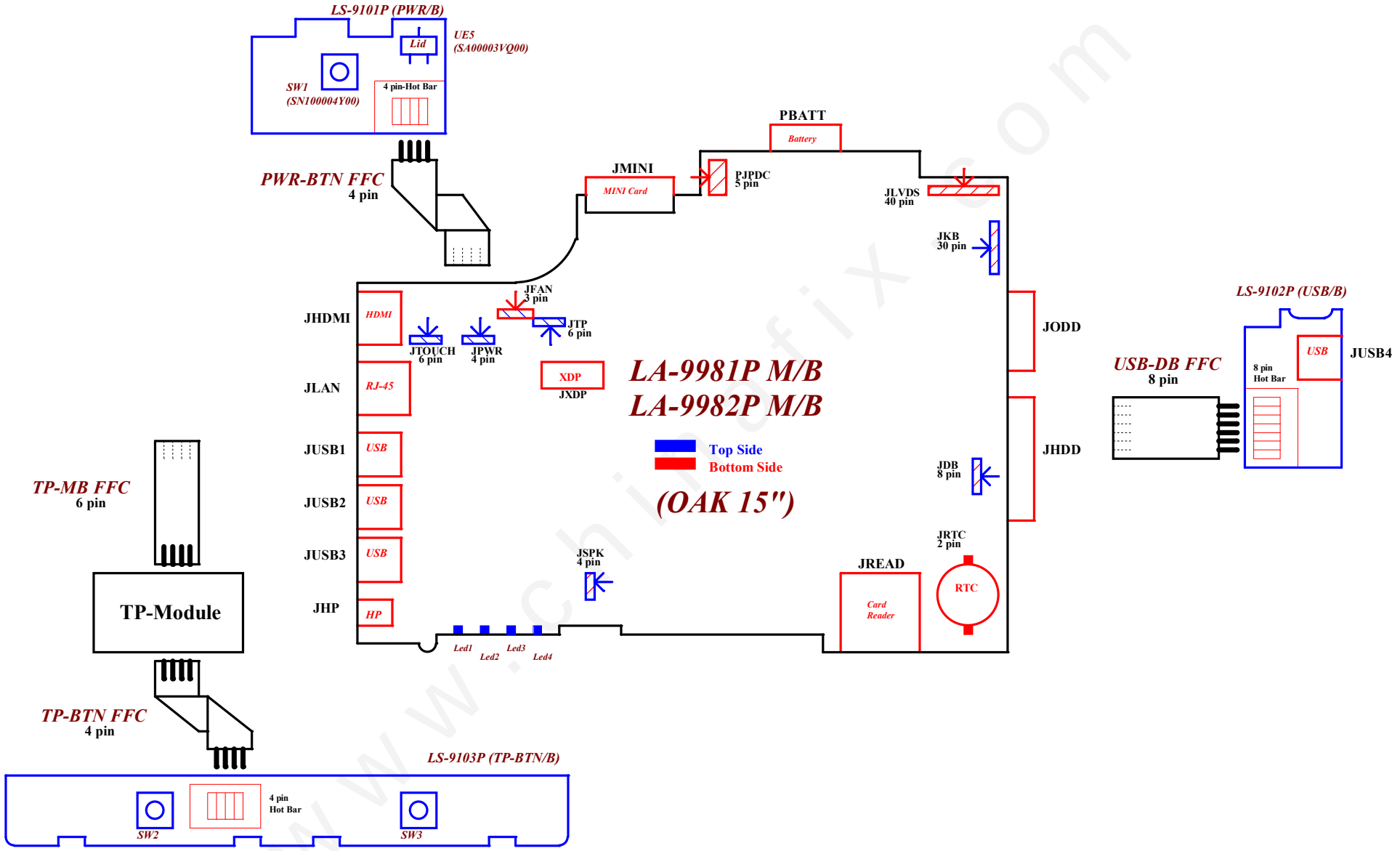
Compal Electronics, Inc.		
Title: Cover Page		
Size: Custom	Document Number: LA-9982P	Rev: 3.0
Date: Wednesday, May 29, 2013	Sheet 1 of 57	



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title: Block diagram			
Size	Document Number: LA-9982P		Rev: 3.0
Date: Wednesday, May 29, 2013	Sheet 2 of 57		

Compal Confidential
Project Code : VAW00 / VAW01
File Name : LA-9981P / LA-9982P



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: DB block diagram

Size | Document Number: LA-9982P | Rev: 3.0

Date: Wednesday, May 29, 2013 | Sheet 3 of 57

Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

	SOURCE	BATT	Charger	RTD2136S	VGA	DDR3L	XDP	WLAN mini card	Touch pad
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9012			V	V				
SMBCLK SMBDATA	ULT					V	V	V	V
SML0CLK SML0DATA	ULT								
SML1CLK SML1DATA	ULT								

Link

Board ID TABLE

ID	PCB Revision			
	UMA	Sun XT	VenusPro	VenusXT
0	SSI&A02			
1		SSI&A02		
2			SSI&A02	
3				SSI&A02
4	PT			
5		PT		
6			PT	
7				PT
8	ST			
9		ST		
10			ST	
11				ST
12	XB			
13		XB		
14			XB	
15				XB
16	A01			
17		A01		
18			A01	
19				A01

Symbol Note :

: means Digital Ground

: means Analog Ground

CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

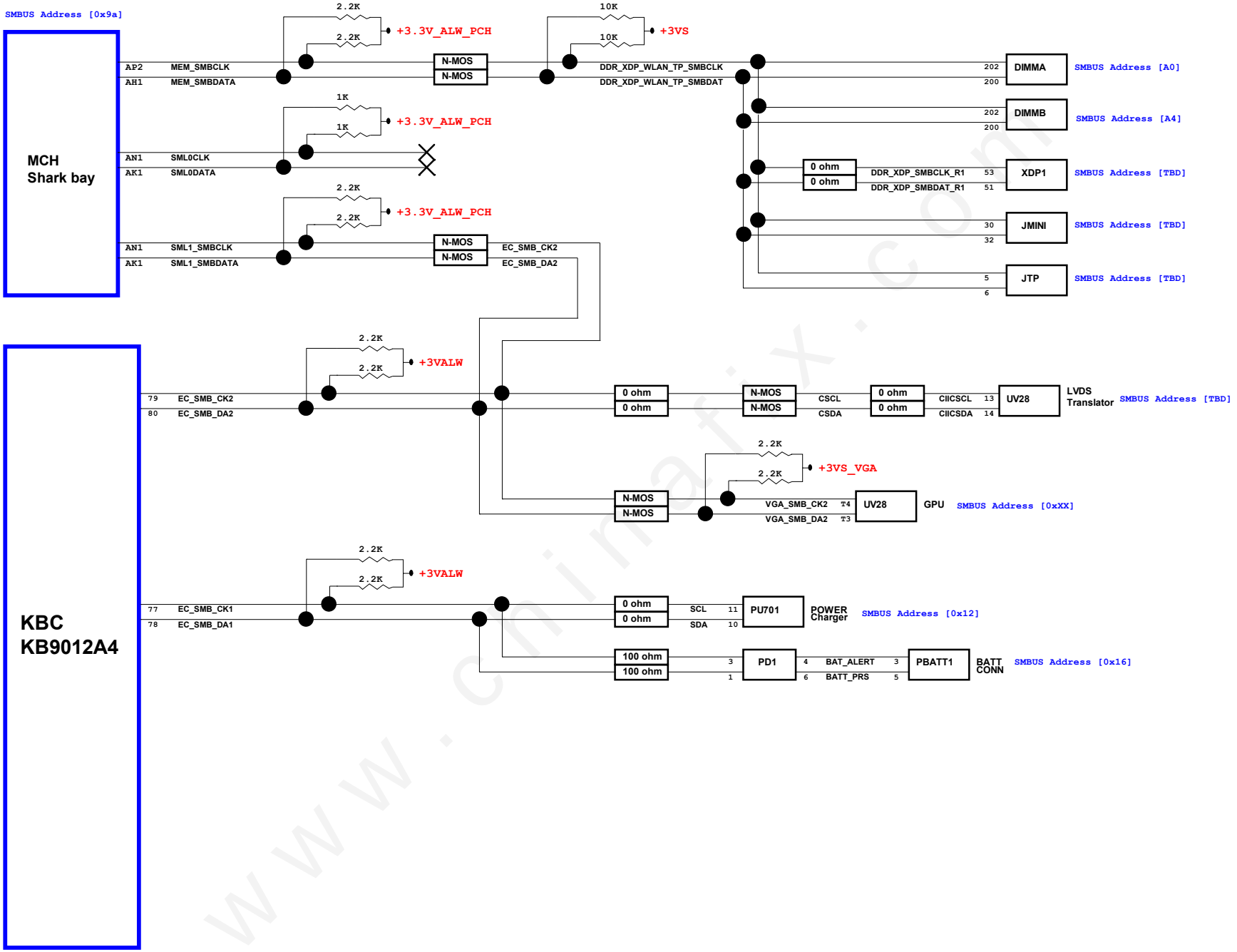
ULT		
	USB3.0	
	Port1	USB connector 2
	Port2	USB connector 1
	Port3	
	Port4	
	USB2.0	
	Port0	USB connector 2
	Port1	USB connector 1
	Port2	USB connector 3
	Port3	USB connector 4 (DB)
	Port4	MINI Card (WLAN)
	Port5	Touch Screen Panel
	Port6	Card Reader
	Port7	Camera
	PCI EXPRESS	
	Lane 1	
	Lane 2	
	Lane 3	10/100 LAN
	Lane 4	MINI Card (WLAN)
	Lane 5	PEG (N14P)
	Lane 6	PEG (N14P)
	SATA	
	SATA0	HDD
	SATA1	ODD
	SATA2	
	SATA3	

Compal Electronics, Inc.

Title: Notes List

Size: | Document Number: LA-9982P | Rev: 3.0

Date: Wednesday, May 29, 2013 | Sheet 4 of 57



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: SMBus block diagram

Size: | Document Number: LA-9982P | Rev: 3.0

Date: Wednesday, May 29, 2013 | Sheet 5 of 57

i3-4010U-15W-GT2-MP

UC1 4010Ui3G2R1@

CL8064701478202 SR16Q C1 1.7G BGA

SA00006SX1L

UC1 4010Ui3G2R3@

CL8064701478202 SR16Q C1 1.7G A31!

SA00006SX2L

i5-4200U-15W-GT2-MP

UC1 4200Ui5G2R1@

CL8064701477702 SR170 C1 1.6G BGA

SA00006SM2L

UC1 4200Ui5G2R3@

CL8064701477702 SR170 C1 1.6G A31!

SA00006SM3L

i7-4500U-15W-GT2-MP

UC1 4500Ui7G2R1@

CL8064701477202 SR16Z C1 1.8G BGA

SA00006SL1L

UC1 4500Ui7G2R3@

CL8064701477202 SR16Z C1 1.8G A31!

SA00006SL2L

UC1A HASWELL_MCP_F

DDI1_LANE_N0 DDI1_LANE_P0 DDI1_LANE_N1 DDI1_LANE_P1 DDI1_LANE_N2 DDI1_LANE_P2 DDI1_LANE_N3 DDI1_LANE_P3

DDI1_TXN0 DDI1_TXP0 DDI1_TXN1 DDI1_TXP1 DDI1_TXN2 DDI1_TXP2 DDI1_TXN3 DDI1_TXP3

DDI2_TXN0 DDI2_TXP0 DDI2_TXN1 DDI2_TXP1 DDI2_TXN2 DDI2_TXP2 DDI2_TXN3 DDI2_TXP3

EDP_TXN0 EDP_TXP0 EDP_TXN1 EDP_TXP1 EDP_TXN2 EDP_TXP2 EDP_TXN3 EDP_TXP3

EDP_CPU_LANE_N0 EDP_CPU_LANE_P0 EDP_CPU_LANE_N1 EDP_CPU_LANE_P1

EDP_AUXN EDP_AUXP

EDP_CPU_AUX# EDP_CPU_AUX

EDP_RCOMP EDP_DISP_UTIL

EDP_COMP EDP_DISP_UTIL

RC72 0_0402_5%

1 OF 19

Rev1p2

COMPENSATION PU FOR eDP

+VCCIOA_OUT

24.9_0402_1%~D RC71

CAD Note: Trace width=20 mils ,Spacing=25mil, Max length=100 mils.

UC4 74CBTLV3126BQ_DHVQFN14_2P5X3

CC13 0.1U_0402_10V7K

PCH_JTAG_TDO TDO_XDP RC43 0_0402_1%

PCH_JTAG_TDI TDI_XDP RC44 0_0402_1% TDI_XDP_R RC45 0_0402_1%

PCH_JTAG_TMS TMS_XDP RC46 0_0402_1%

TRST#_XDP RC47 0_0402_1%

RUNPWROK

XDP_TDO XDP_TDI XDP_TMS XDP_TRST#

CC29 ESD@ 0.1U_0402_10V7K

Place CC29 close to UC4

reference Shark Bay ULT Validation Customer Debug Port Implementation Requirement Rev 1.0

Place near JXDP1

JXDP1 SAMTE_BSH-030-01-L-D-A CONN@

XDP_PREQ# XDP_PRDY#

CFG0 CFG1 CFG2 CFG3 CFG4 CFG5 CFG6 CFG7 CFG8 CFG9 CFG10 CFG11 CFG12 CFG13 CFG14 CFG15 CFG16 CFG17 CFG18 CFG19

XDP_OBS0_R XDP_OBS1_R

H_CPUPWRGD RC48 1K_0402_5%

PBTN_OUT#

SYS_PWROK RC52 0_0402_5%

CPU_PWR_DEBUG# RC50 0_0402_5%

SYS_PWROK_XDP

H_VCCST_PWRGD_XDP

CPU_PWR_DEBUG# R

DDR_XDP_SMBDAT_R1 DDR_XDP_SMBCLK_R1

PCH_JTAG_TCK

RP46 0_8P4R_5%

XDP@

CLK_CPU_ITP CLK_CPU_ITP#

PLT_RST# RC362 1K_0402_1%

RC51 1K_0402_5%

TDO_XDP TRST#_XDP TDI_XDP TMS_XDP CFG3_R RC56 1K_0402_5%

PLT_RST# CC30 ESD@ 0.047U_0402_16V4Z

Place CC30 close to RC51.1

CC17 0.1U_0402_10V7K

H_CATERR# RC58 49.9_0402_1%

H_PROCHOT# RC60 62_0402_5%

PCH_JTAG_RST# RC57 0_0402_1%

PCH_JTAG_TCK XDP_TCLK RC59 0_0402_1%

PCH_JTAG_TDO TDO_XDP RC62 0_0402_5%

PCH_JTAG_TDI XDP_TDI_R RC63 0_0402_5%

PCH_JTAG_TCK XDP_TCLK RC65 0_0402_5%

RC64 1K_0402_5%

SYS_PWROK_XDP

ESD@ CC16 0.1U_0402_10V7K

Place near JXDP1.47

XDP_DBRESET# RC26 0_0402_1% SYS_RESET# SYS_RESET# <10>

H_CPUPWRGD RC66 10K_0402_5%

CC27 100P_0402_50V8J ESD@

ESD solution

CAD Note: Avoid stub in the PWRGD path while placing resistors RC115

DDR3 COMPENSATION SIGNALS

200_0402_1% RC68 SM_RCOMP0

120_0402_1% RC69 SM_RCOMP1

100_0402_1% RC70 SM_RCOMP2

CAD Note: Trace width=12~15 mil, Spcing=20 mils Max trace length= 500 mil

UC1B HASWELL_MCP_F

CPU_DETECT# H_CATERR# PECI_EC

H_PROCHOT# RC67 56_0402_5%

H_CPUPWRGD

DDR3_DRAMRST#_CPU DDR_PG_CTRL

SM_RCOMP0 SM_RCOMP1 SM_RCOMP2 SM_DRAMRST SM_PG_CNTL1

PRDY PREQ PROC_TCK PROC_TMS PROC_TRST PROC_TDI PROC_TDO

XDP_PRDY# XDP_PREQ# XDP_TCK XDP_TMS XDP_TRST# XDP_TDI XDP_TDO

PCH_JTAG_RST# R2341 0_0402_5%

BPM#0 BPM#1 BPM#2 BPM#3 BPM#4 BPM#5 BPM#6 BPM#7

XDP_OBS0_R XDP_OBS1_R RC141 0_0402_1%

T111 T112 T113 T114 T115 T116

2 OF 19

Rev1p2

PU/PD for JTAG signals

XDP_TMS XDP_TDI XDP_PREQ# TDO_XDP RP44 51_8P4R_5%

XDP_TDO XDP_TCK XDP_TRST# RP45 51_8P4R_5%

DDR3_DRAMRST#_CPU CC35 ESD@ 0.047U_0402_16V4Z

Place CC35 on BOT

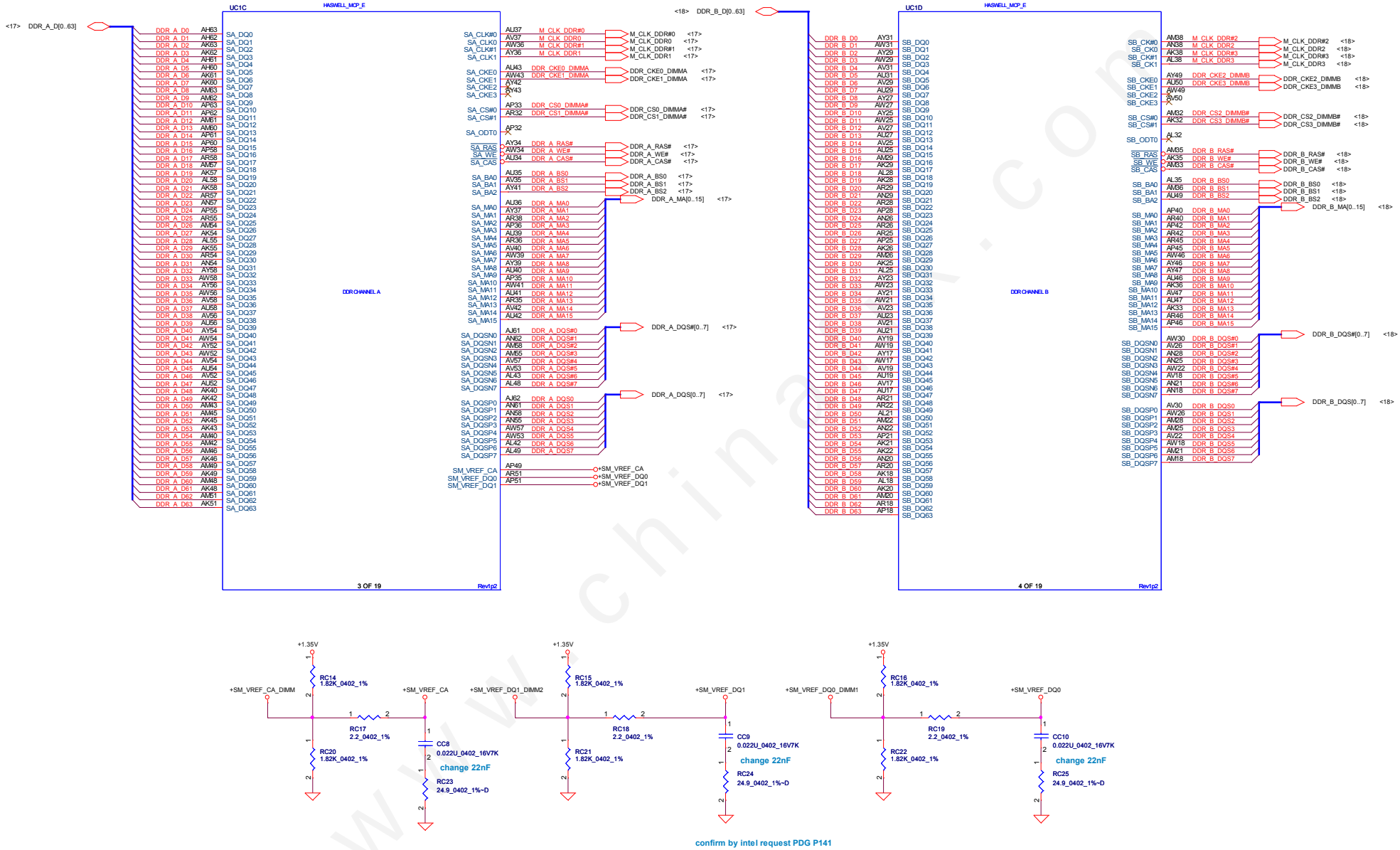
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: MCP(1,2/19) eDP,XDP,MISC

Size: Document Number: LA-9982P Rev: 3.0

Date: Wednesday, May 29, 2013 Sheet 6 of 57



confirm by intel request PDG P141

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: MCP(3.4/19) DDR3

Size: | Document Number: LA-9982P | Rev: 3.0

Date: Wednesday, May 29, 2013 | Sheet 7 of 57

RTC Battery

+RTCBATT
+CHGRTC
RC10 1K_0402_5%
W=20mils
W=20mils
W=20mils
DC1 BAT54CW_SOT323-3
+RTCVCC
CC26 1U_0603_10V6K

+CHGRTC — JP12 JUMP_43X39 — +3VLP

For GCLK

<29> PCH_RTCX1 — PCH_RTCX1

+RTCVCC
RC1 330K_0402_1%
PCH_INTVRMEN
RC2 330K_0402_1%

INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs

+3VS
@ RC3 PCH_AZ_SDOUT 1K_0402_5%

FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DESABLED (DEFAULT)
HIGH = ENABLED

CC1 15P_0402_50V8J XTAL@
XTAL@ YC1 32.768KHZ_12.5PF_Q13FC1350000
XTAL@ RC4 10M_0402_5%
CC2 XTAL@ 15P_0402_50V8J
PCH_RTCX1
PCH_RTCX2
INTRUDER#
PCH_INTVRMEN
SRTCRST#
PCH_RTCRST#
+RTCVCC
RC7 1M_0402_5%
RC5 20K_0402_5%
RC6 20K_0402_5%

UC1E — HASWELL_MCP_E

RTCX1
RTCX2
INTRUDER
INTVRMEN
SRTCRST
RTCRST
RTC

HDA_BCLK/I2S0_SCLK
HDA_SYNC/I2S0_SFRM
HDA_RST/I2S_MCLK
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD
HDA_SDO/I2S0_TXD
HDA_DOCK_EN/I2S1_TXD
HDA_DOCK_RST/I2S1_SFRM
I2S1_SCLK
AUDIO

PCH_AZ_BITCLK
PCH_AZ_SYNC
PCH_AZ_RST#
PCH_AZ_CODEC_SDIN0
<22> PCH_AZ_CODEC_SDIN0
<30> ME_EN — RC8 1K_0402_5% — PCH_AZ_SDOUT

SATA_RN0/PERN6_L3
SATA_RP0/PERP6_L3
SATA_TN0/PETN6_L3
SATA_TP0/PETP6_L3
SATA_RN1/PERN6_L2
SATA_RP1/PERP6_L2
SATA_TN1/PETN6_L2
SATA_TP1/PETP6_L2
SATA_RN2/PERN6_L1
SATA_RP2/PERP6_L1
SATA_TN2/PETN6_L1
SATA_TP2/PETP6_L1
SATA_RN3/PERN6_L0
SATA_RP3/PERP6_L0
SATA_TN3/PETN6_L0
SATA_TP3/PETP6_L0
SATA

SATA_PRX_DTX_N0_C <32>
SATA_PRX_DTX_P0_C <32>
SATA_PTX_DRX_N0_C <32>
SATA_PTX_DRX_P0_C <32>
SATA HDD
SATA_PRX_DTX_N1_C <32>
SATA_PRX_DTX_P1_C <32>
SATA_PTX_DRX_N1_C <32>
SATA_PTX_DRX_P1_C <32>
SATA ODD

PCH Rx side need use strap pin to update PCIE +/-

+3VS
RC107 10K_0402_5%
EC_SMI# <30>
SATA0GP/GPIO34
SATA1GP/GPIO35
SATA2GP/GPIO36
SATA3GP/GPIO37
PCH_GPIO35
ODD_DETECT#
PCH_GPIO37
ODD_DETECT# <32>
+1.05VS_ASATA3PLL
SATA_IREF
RSVD
RSVD
SATA_RCOMP
SATALED
SATA_IREF
SATA_RCOMP
SATA_ACT#
RC126 @ 0_0603_1%
RC131 3.01K_0402_1%
SATA_ACT# <26>
within 500 mils

SATA Impedance Compensation

CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.
reference FFRD sch 0.5

@ ME1 SHORT PADS~D — CC3 1U_0402_6.3V6K
@ CMOS1 SHORT PADS~D — CC4 1U_0402_6.3V6K

CMOS place near DIMM

<6> PCH_JTAG_RST# — PCH_JTAG_RST# — PCH_TRST
<6> PCH_JTAG_TCK — PCH_JTAG_TCK — PCH_TCK
<6> PCH_JTAG_TDI — PCH_JTAG_TDI — PCH_TDI
<6> PCH_JTAG_TDO — PCH_JTAG_TDO — PCH_TDO
<6> PCH_JTAG_TMS — PCH_JTAG_TMS — PCH_TMS
RSVD
RSVD
<6> PCH_JTAG_JTAGX — PCH_JTAG_JTAGX — JTAGX
RSVD
JTAG

5 OF 19
Rev1p2

+1.05VS
@ RC130 PCH_JTAG_JTAGX 1K_0402_1%
@ RC135 PCH_JTAG_TCK 51_0402_1%

+1.05VS
RP48 51_8P4R_5%
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_TMS

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

HDA for Codec

<22> PCH_AZ_CODEC_SDOUT — EMI@ R2356 33_0402_5% — PCH_AZ_SDOUT
<22> PCH_AZ_CODEC_SYNC — EMI@ R2357 33_0402_5% — PCH_AZ_SYNC
<22> PCH_AZ_CODEC_RST# — EMI@ R2358 33_0402_5% — PCH_AZ_RST#
<22> PCH_AZ_CODEC_BITCLK — EMI@ R2359 33_0402_5% — PCH_AZ_BITCLK
@EMI@ CC5 27P_0402_50V8J

EMI depop location

+3VS
ODD_DETECT#
PCH_GPIO35
PCH_GPIO37
RP37 10K_8P4R_5%

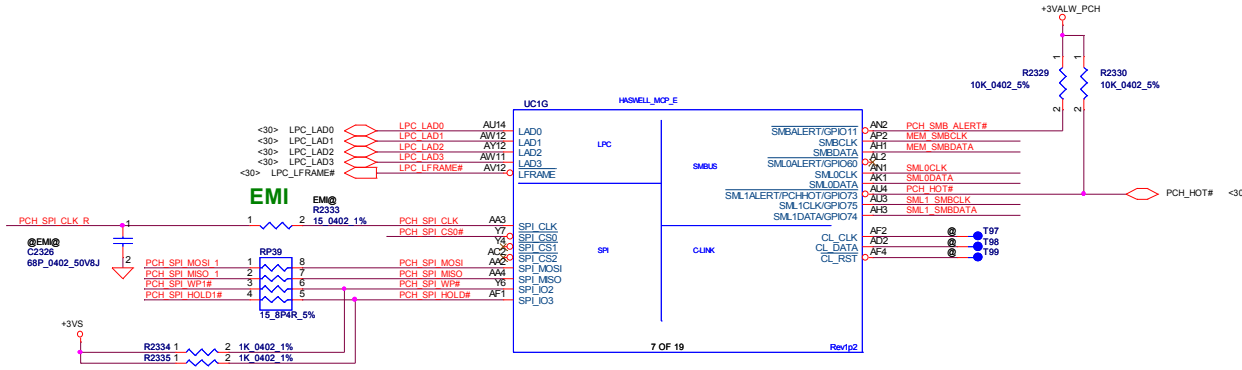
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

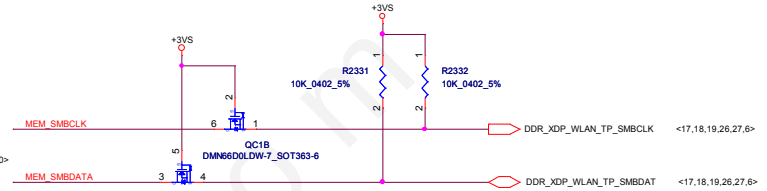
Title: MCP(5/19) RTC,SATA,HDA,JTAG

Size | Document Number: LA-9982P | Rev: 3.0

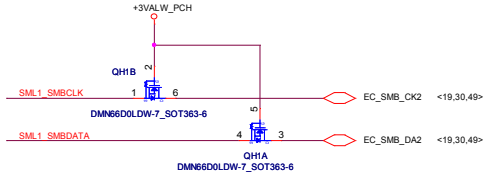
Date: Wednesday, May 29, 2013 | Sheet 8 of 57



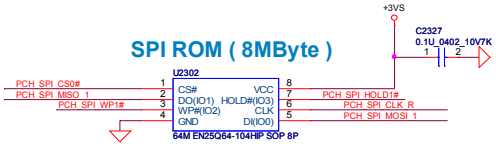
MEM Bus : DDR/XDP/WLAN/TP

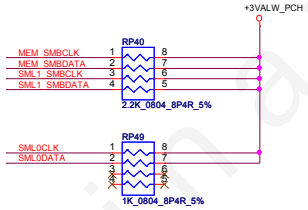


SML1 Bus : EC/Sensors



SPI ROM (8MByte)

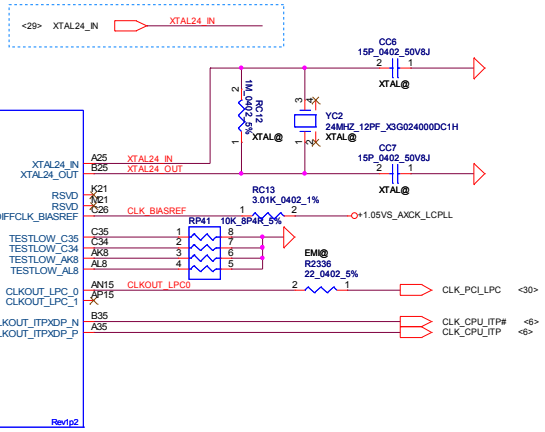


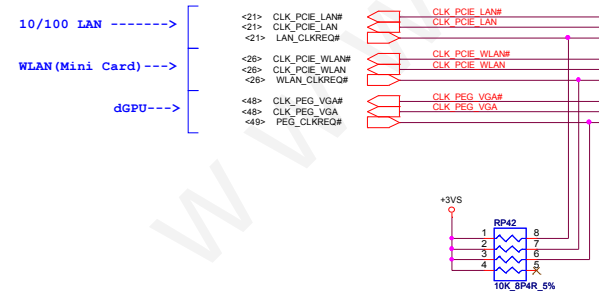


PN : SA000046400 ,64M,EN25Q64-104HIP

Place T183, T184, T185, T186 close to
PCH_SPI_MOSI_1
PCH_SPI_MISO_1
PCH_SPI_CLK_R
PCH_SPI_CS0#
near U2302

For GCLK





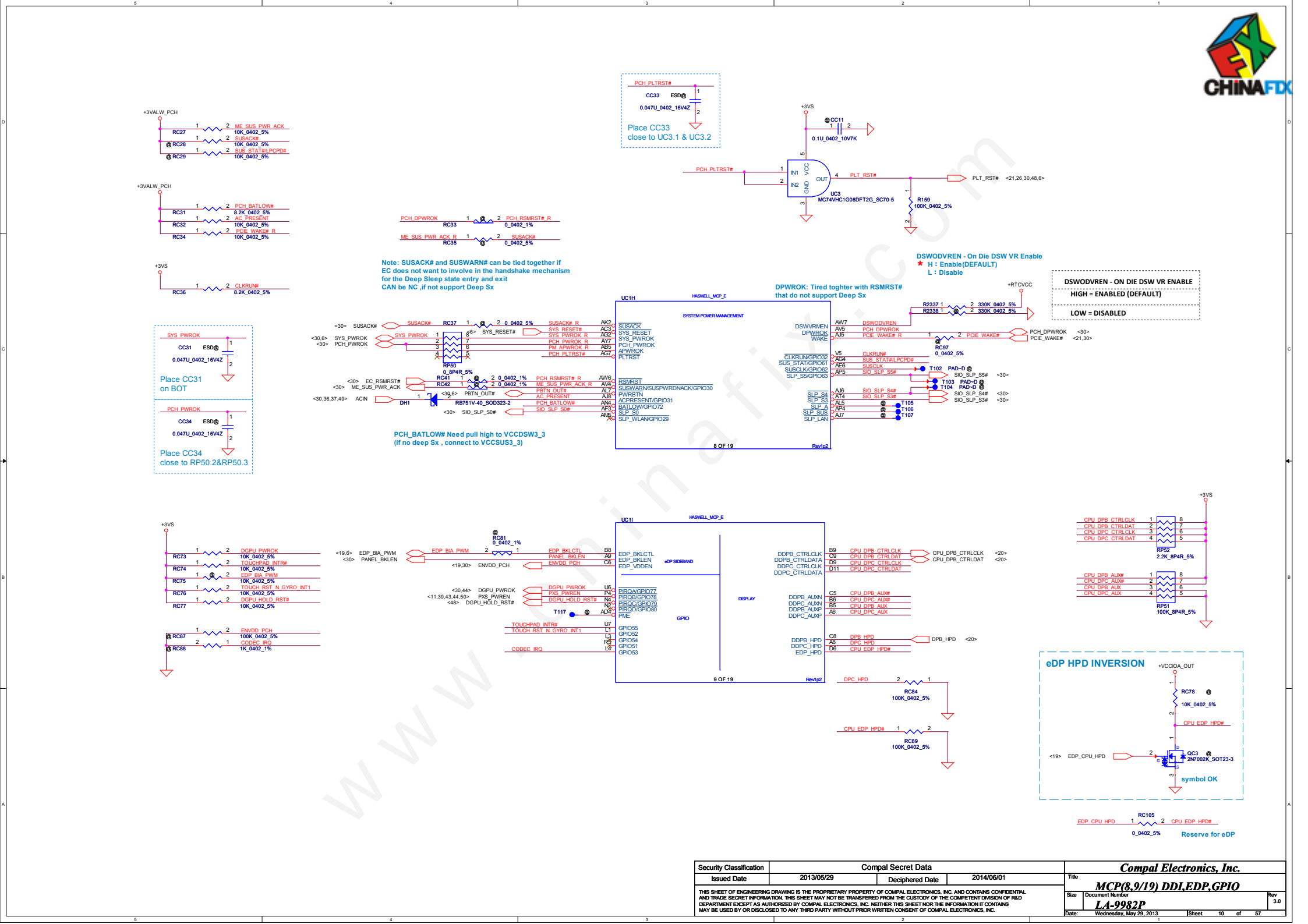
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: MCP(6,7/19) CLK,SMB,SPI,LPC

Size	Document Number	Rev
	LA-9982P	3.0

Date: Wednesday, May 29, 2013 Sheet 9 of 57



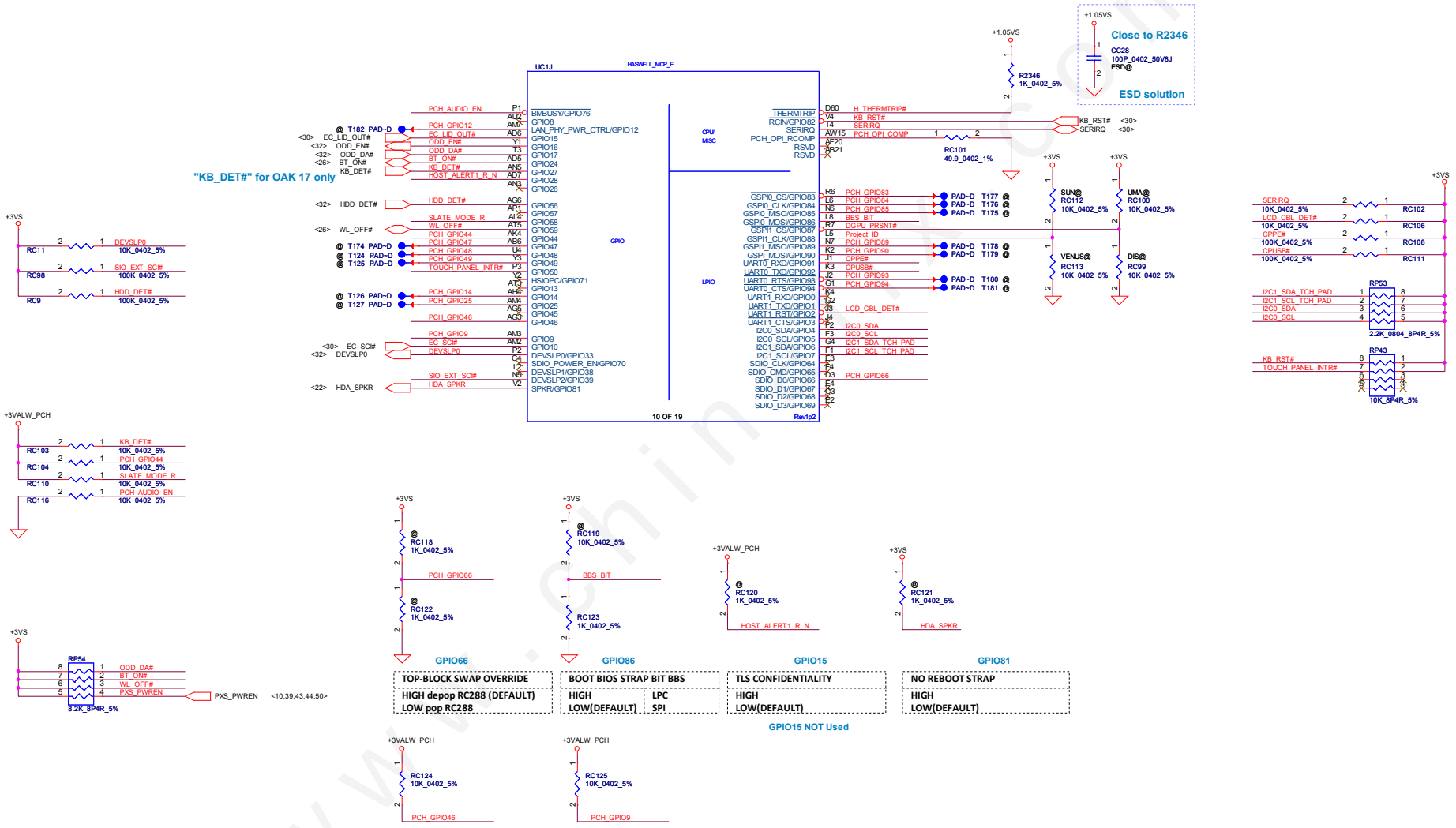
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: MCP(8,9/19) DDI,EDP,GPIO

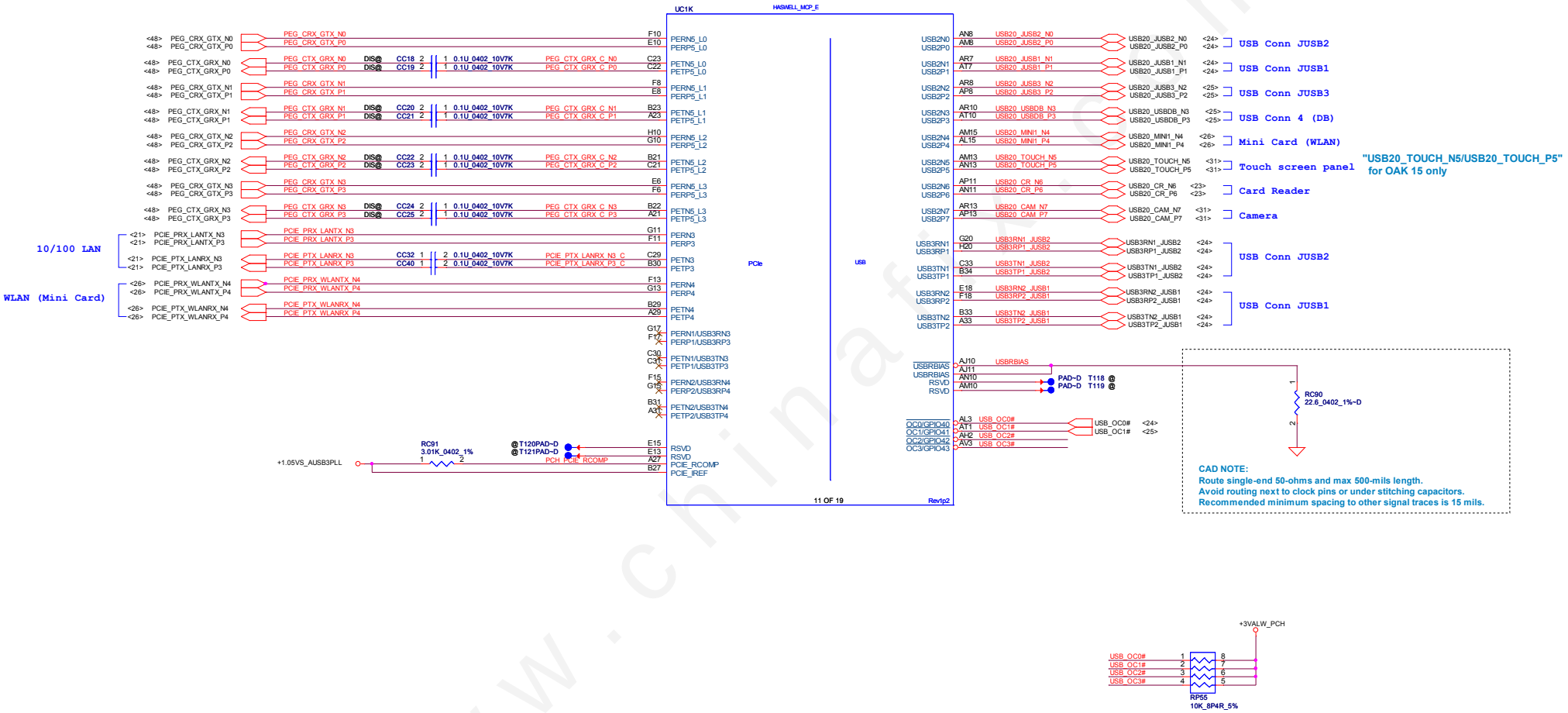
Size	Document Number	Rev
	LA-9982P	3.0

Date: Wednesday, May 29, 2013 Sheet 10 of 57



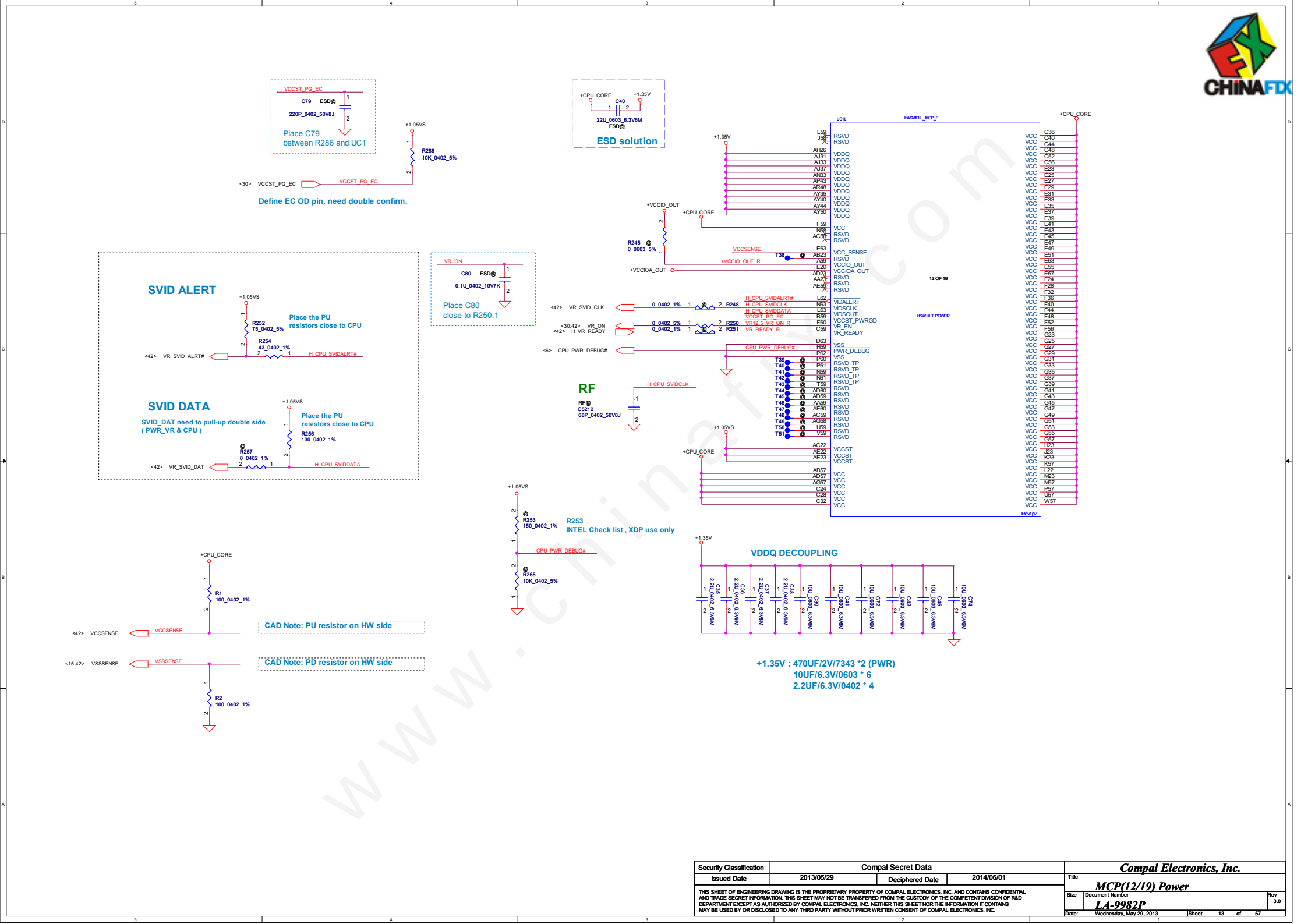
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title	MCP(10/19) GPIO,LPIO,MISC		
Size	Document Number		Rev
	LA-9982P		3.0
Date:	Wednesday, May 29, 2013	Sheet	11 of 57



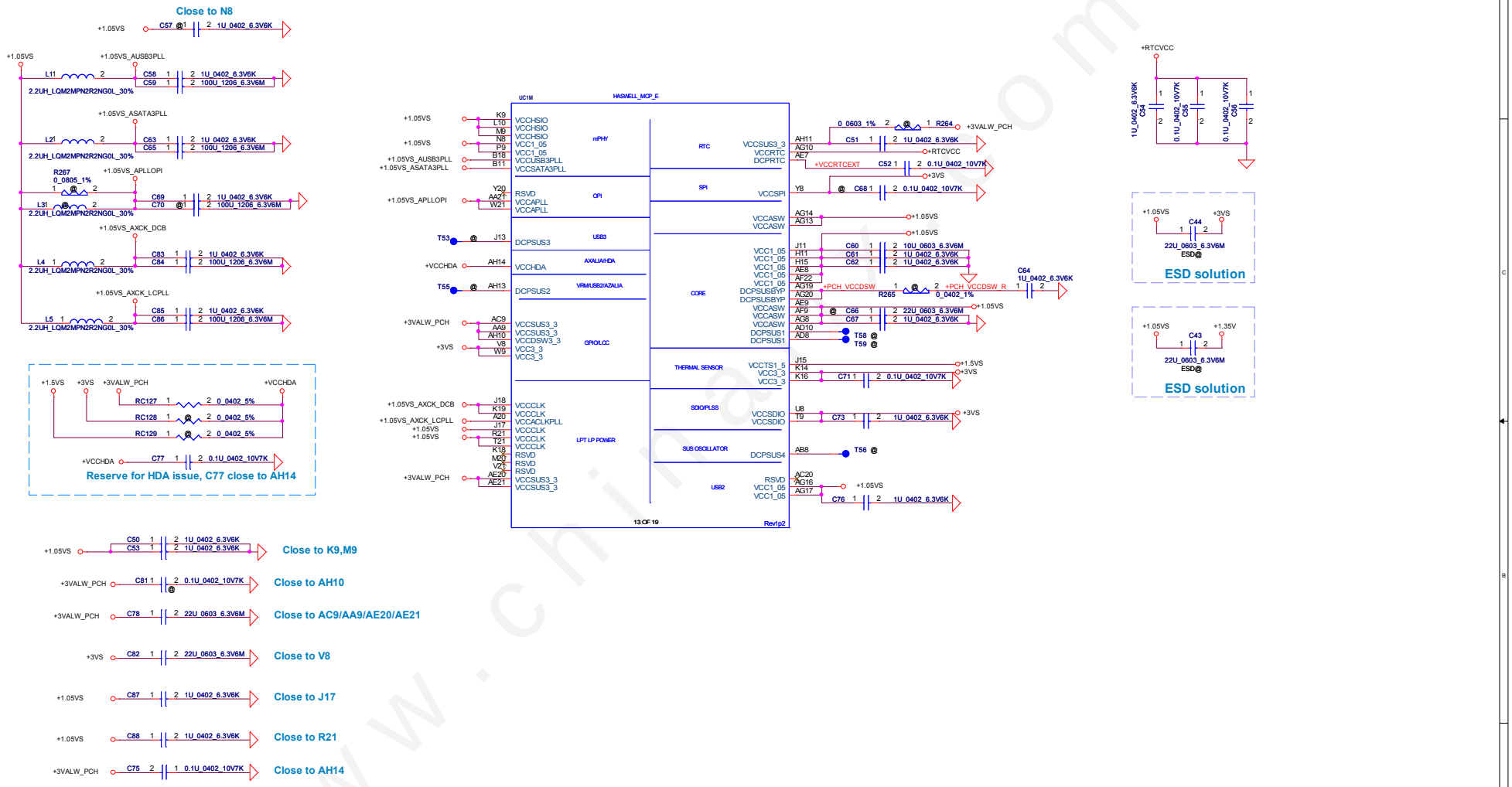
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.		
Title: MCP(11/19) PCIE,USB		
Size	Document Number: LA-9982P	Rev: 3.0
Date: Wednesday, May 29, 2013	Sheet 12 of 57	



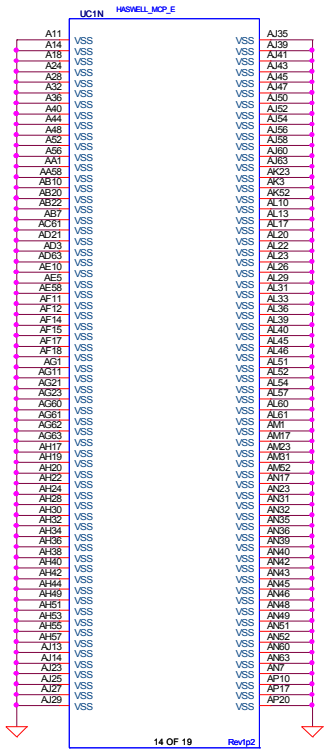
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

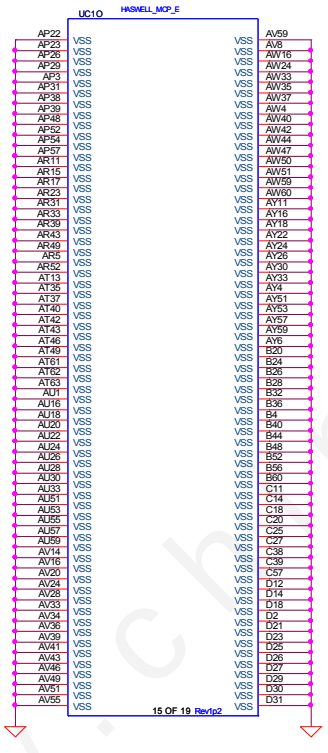
Compal Electronics, Inc.			
Title	MCP(12/19) Power		
Size	Document Number		Rev
	LA-9982P		3.0
Date:	Wednesday, May 29, 2013	Sheet	13 of 57

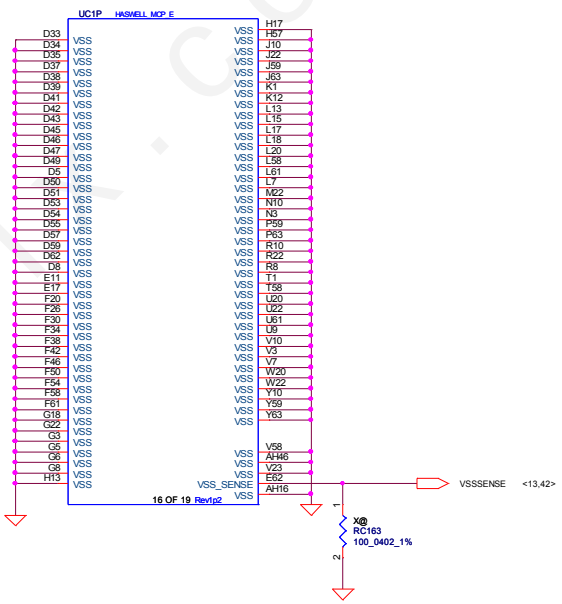


Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title	MCP(13/19) Power		
Size	Document Number		Rev
	LA-9982P		3.0
Date:	Wednesday, May 29, 2013	Sheet 14 of 57	



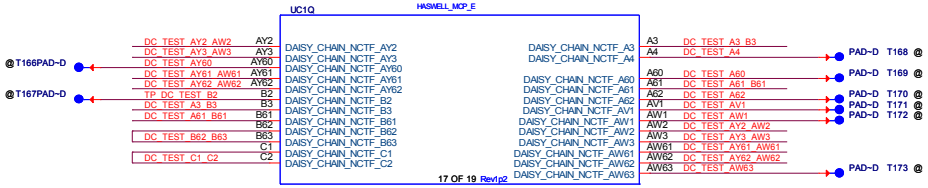


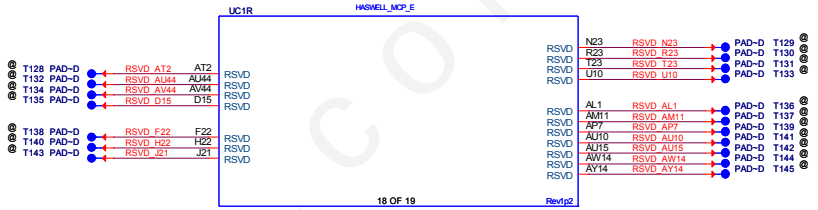


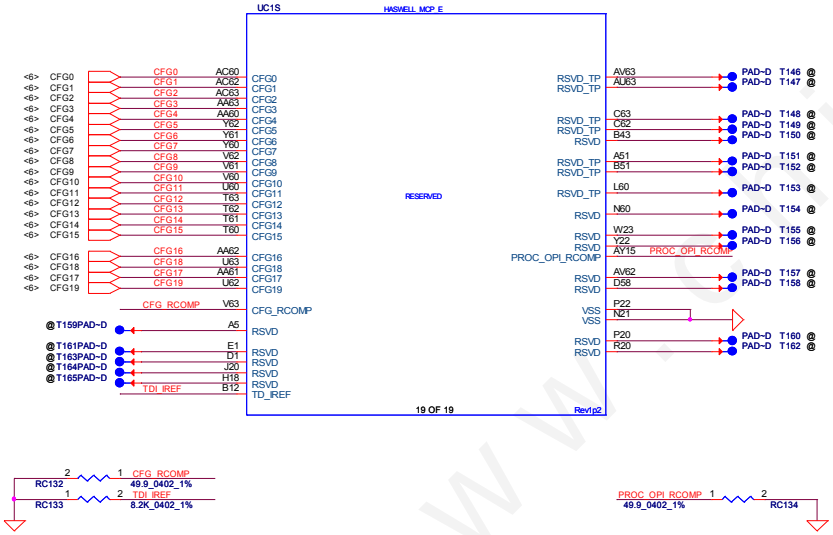
CAD Note: RC163 SHOULD BE PLACED CLOSE TO CPU

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

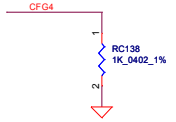
Compal Electronics, Inc.			
Title	MCP(14,15,16/19) VSS		
Size	Document Number		Rev
	LA-9982P		3.0
Date:	Wednesday, May 29, 2013	Sheet 15 of 57	







CFG STRAPS for CPU



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title	MCP(17,18,19/19) CFG,RSVD		
Size	Document Number LA-9982P		Rev 3.0
Date: Wednesday, May 29, 2013	Sheet 16 of 57		

H=4mm

2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMM1

Note: Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note: Place near JDIMM1.203,204

CAD NOTE PLACE THE CAP NEAR TO DIMM RESET PIN

DDR3L SODIMM ODT GENERATION

Place CC31 between QD2 and R2349

ESD solution

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: DDRIII DIMMA

Size: | Document Number: LA-9982P | Rev: 3.0

Date: Wednesday, May 29, 2013 | Sheet 17 of 57

H=4mm

2-3A to 1 DIMMs/channel

Populate RD4, De-Populate RD8 for Intel DDR3 VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3 VREFDQ multiple methods M3

<7> DDR_B_DQS#[0..7]
<7> DDR_B_D[0..63]
<7> DDR_B_DQS[0..7]
<7> DDR_B_MA[0..15]

All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM2

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note:
Place near JDIMM2.203,204

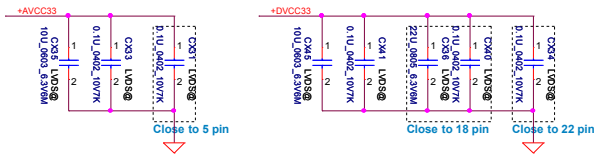
For ME concern, CD51 uesd H1.4

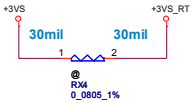
CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

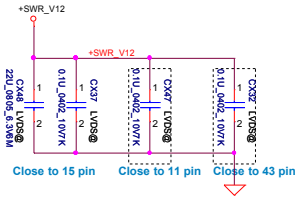
JDIMM2
CONN@
LCN_DAN06-K4406-0102

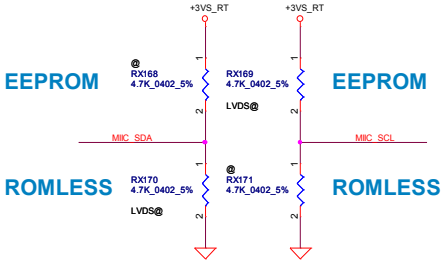
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

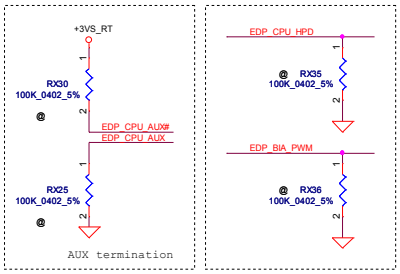
Compal Electronics, Inc.	
Title	DDRIII DIMMB
Size	Document Number: LA-9982P
Rev	3.0
Date:	Wednesday, May 29, 2013
Sheet	18 of 57

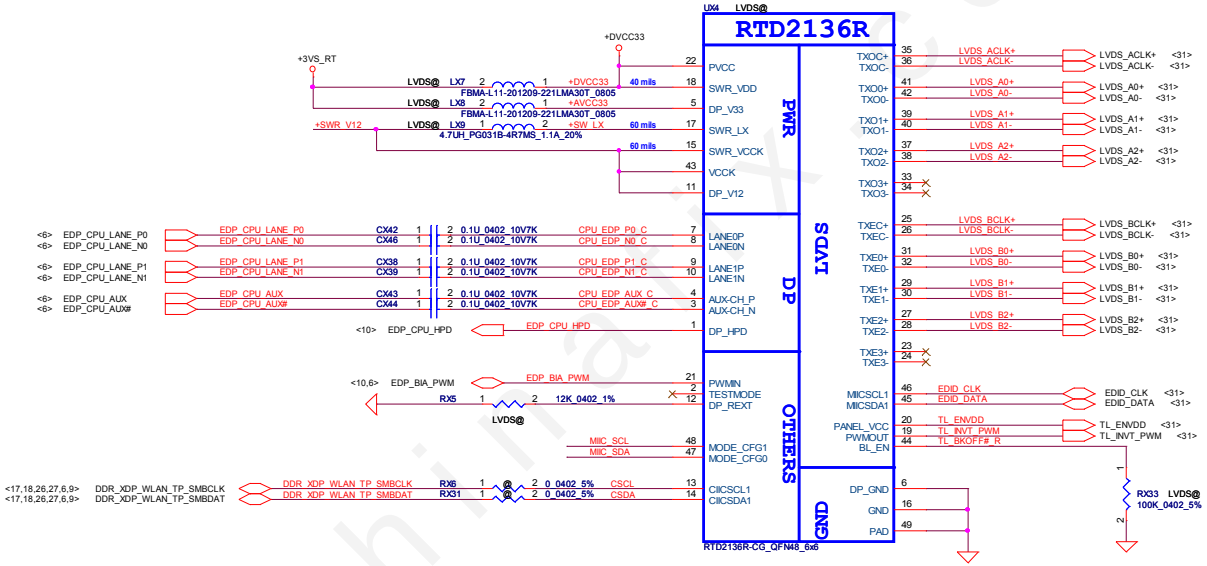




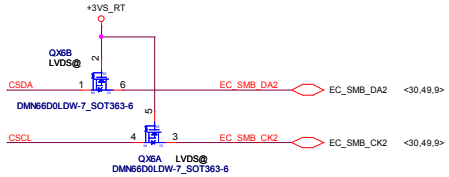


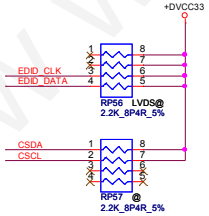




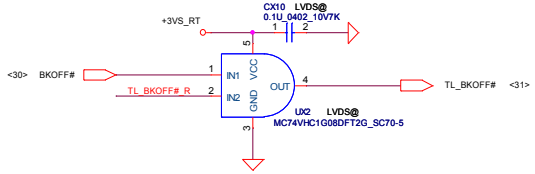


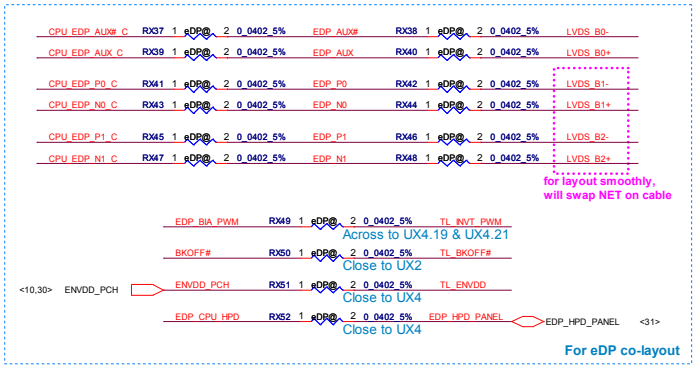
RTD2136S : SA00004NW10
RTD2136R : SA000067100





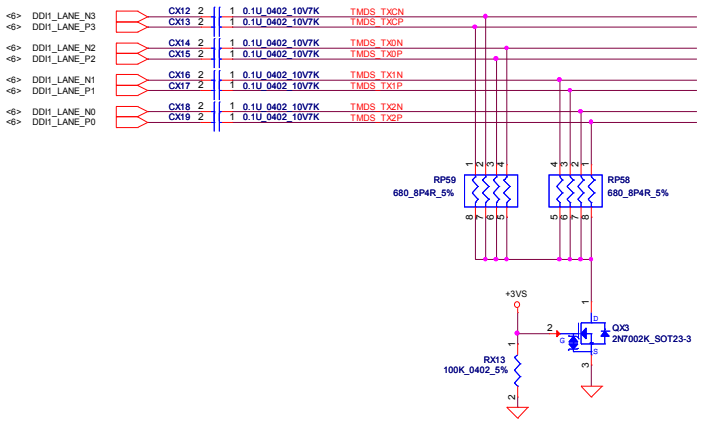
Vendor advise reserve it



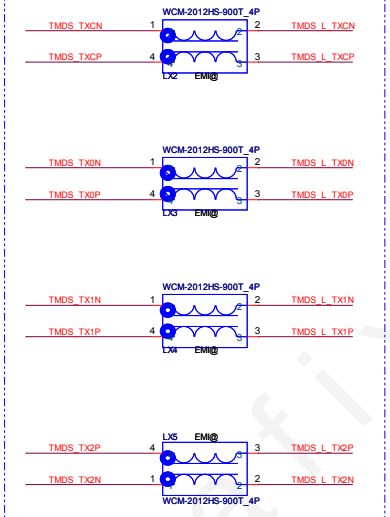


Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

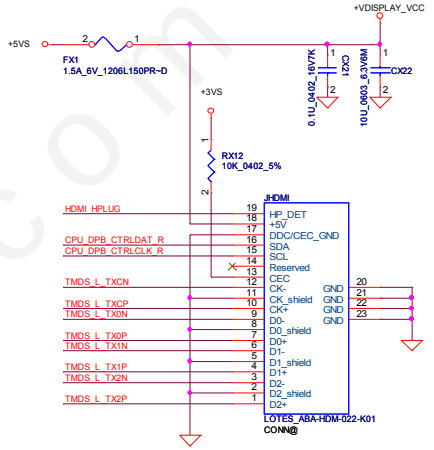
Compal Electronics, Inc.			
Title	eDP to LVDS converter		
Size	Document Number		Rev
	LA-9982P		3.0
Date:	Wednesday, May 29, 2013	Sheet	19 of 57

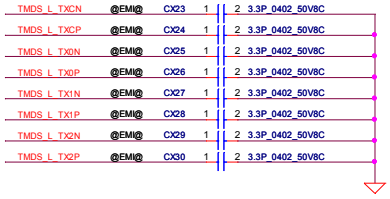


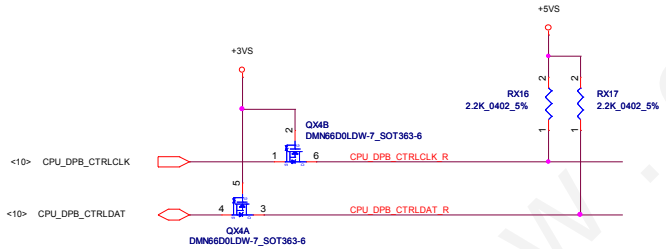
Place close to JHDMI1

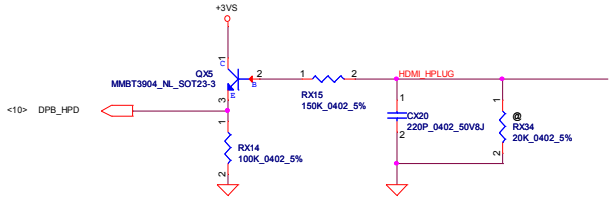


W=40mils



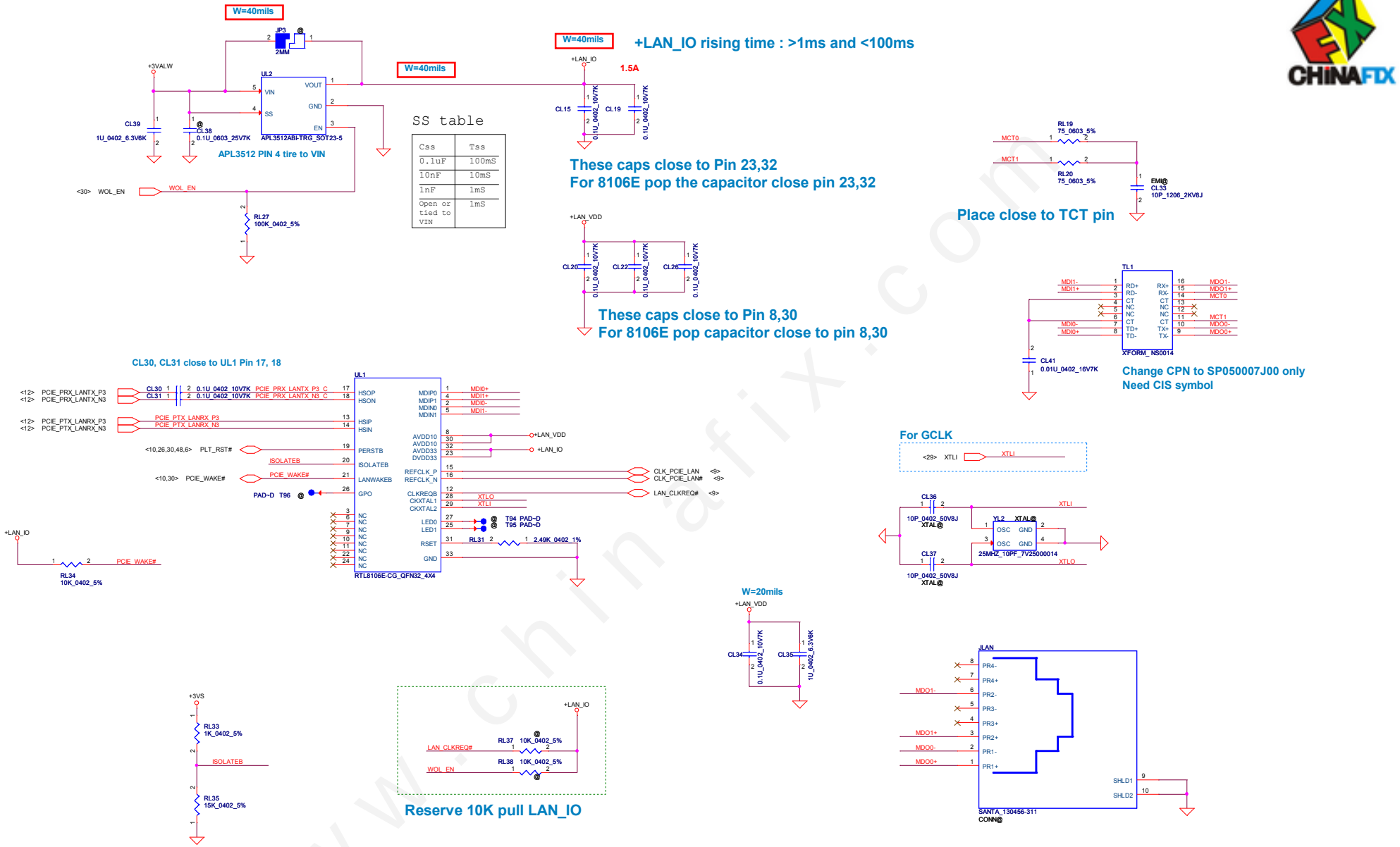






Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title: HDMI			
Size	Document Number: LA-9982P		Rev: 3.0
Date: Wednesday, May 29, 2013	Sheet 20 of 57		



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title: LAN RTL8106E			
Size	Document Number: LA-9982P		Rev: 3.0
Date: Wednesday, May 29, 2013	Sheet 21 of 57		

Reserve for HDA issue

CA71, CA51 place close to Pin 26

CA53, CA55 change Value from 10U_0603_6.3V6M~D to 4.7U_0603_6.3V6K

CA57,CA58 close to UA1 pin1

RA51, RA33 place close to UA1

JACK_PLUG Delay circutis

Reserve for cancel Delay circutis

Place on the moat between GND & GNDA.

SM01000BV00 need CIS symbol

EC Beep

MCU Beep

PC Beep

Close to UA1 Pin11,13,14,16

close to Codec

Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

iPhone and Nokia type Combo Jack

40mil

40mil

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

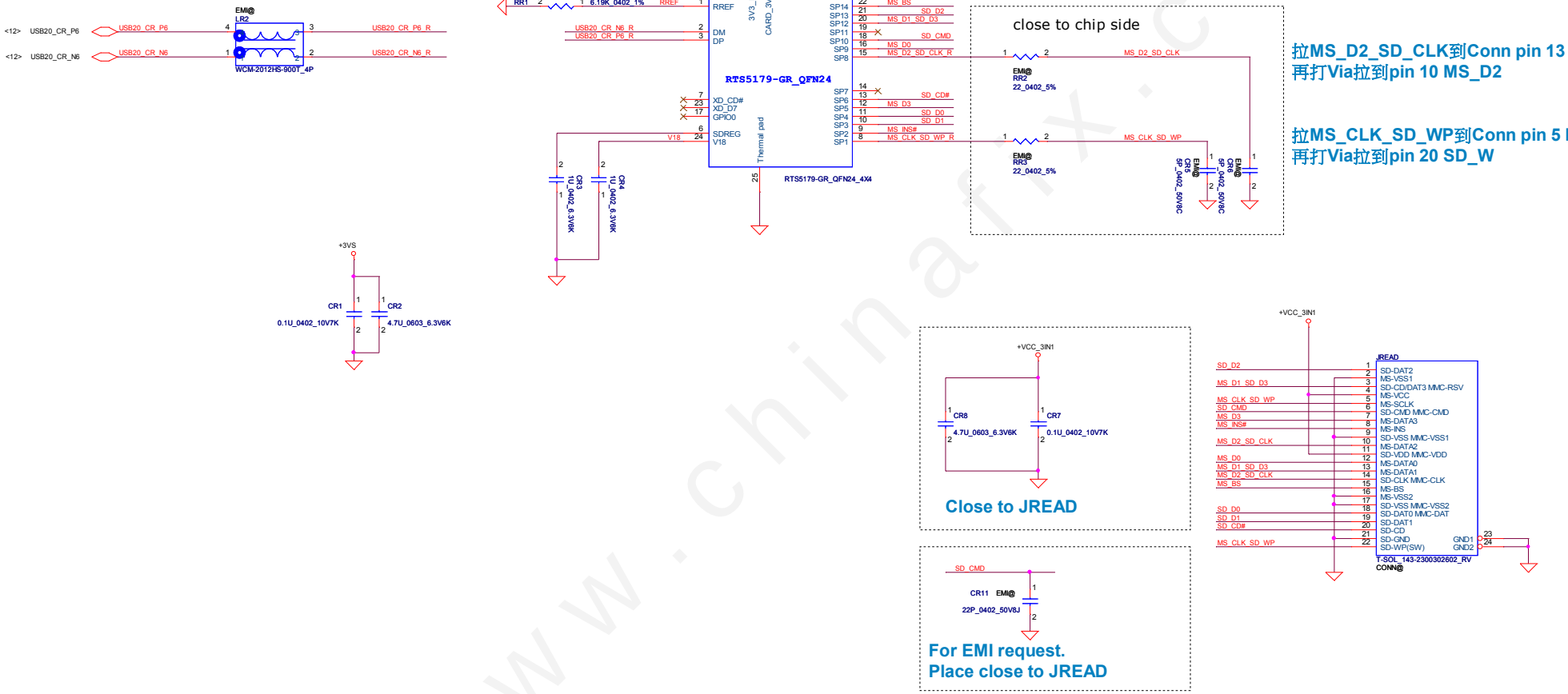
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: Audio Codec ALC3223

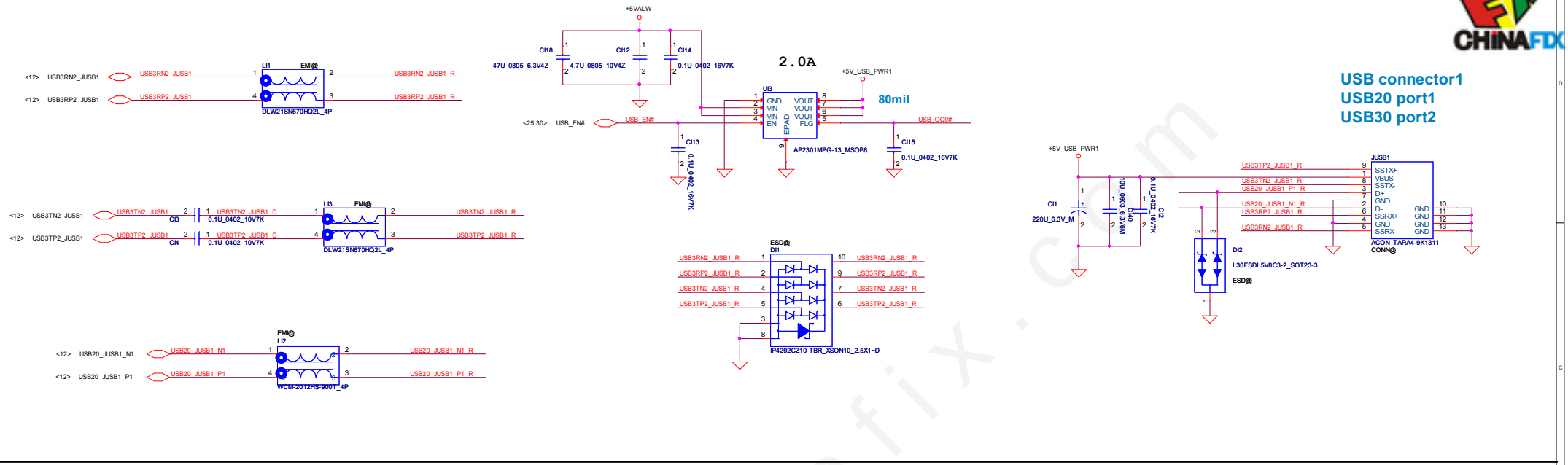
Size: | Document Number: LA-9982P | Rev: 3.0

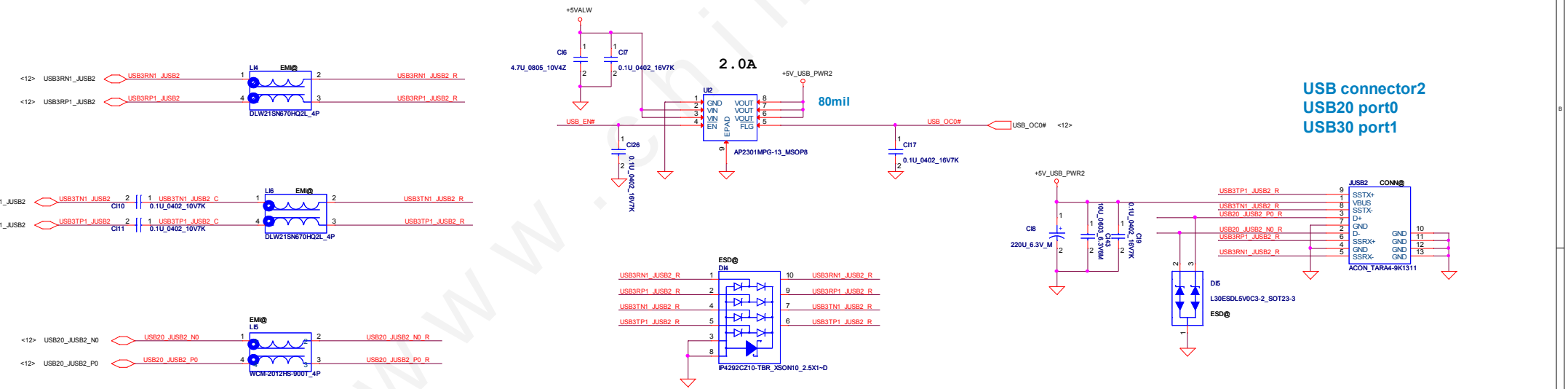
Date: Wednesday, May 29, 2013 | Sheet 22 of 57



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title	Card Reader RTS5179		
Size	Document Number		Rev
	LA-9982P		3.0
Date:	Wednesday, May 29, 2013	Sheet 23 of 57	

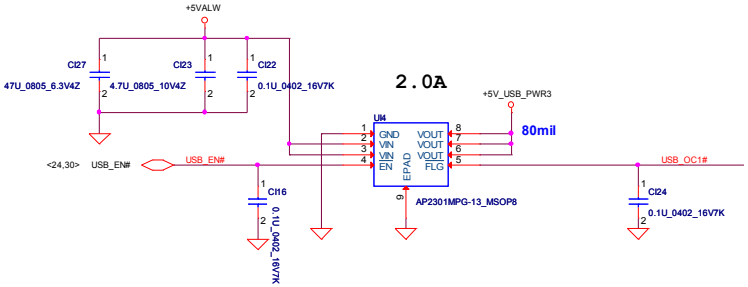


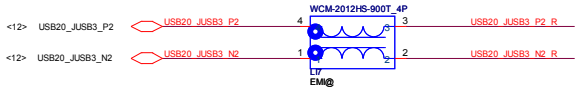


Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

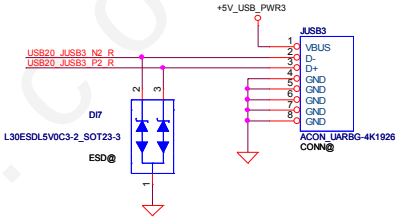
Compal Electronics, Inc.

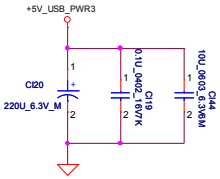
Title	USB3.0	
Size	Document Number	Rev
	LA-9982P	3.0
Date: Wednesday, May 29, 2013	Sheet 24 of 57	



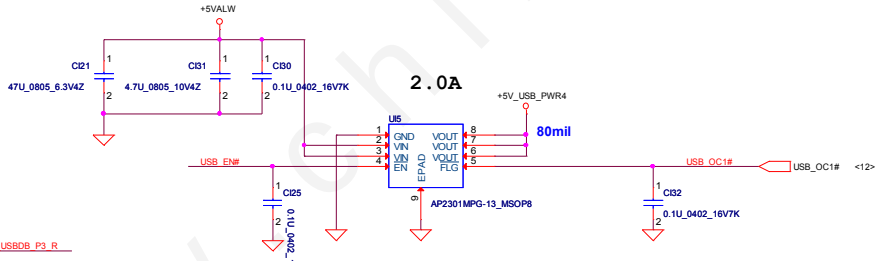


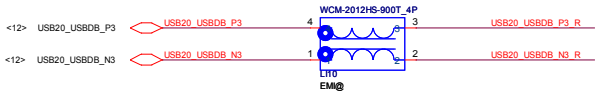
USB connector3
USB20 port2



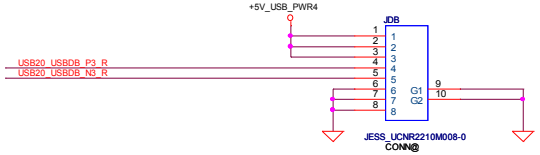


Place close to JUSB3





USB connector4
USB20 port3



2nd: SP01001EX00
Main: SP01001AA00
Change CONN symbol for DFB

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

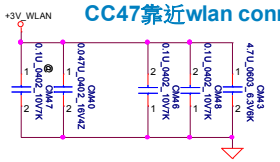
Compal Electronics, Inc.

Title: MB to USB2.0 DB

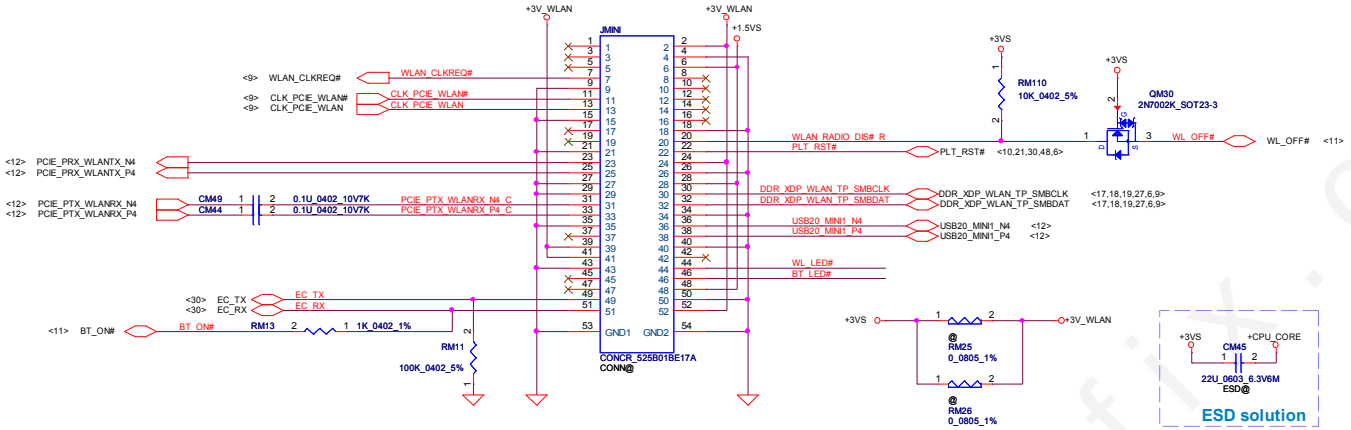
Size | Document Number: LA-9982P | Rev: 3.0

Date: Wednesday, May 29, 2013 | Sheet 25 of 57

CC47靠近wlan connector



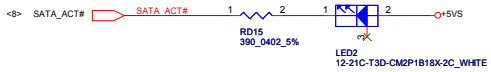
Mini WLAN/WIMAX H=6.7



ESD solution

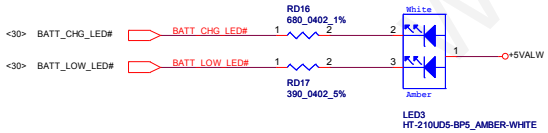
HDD LED

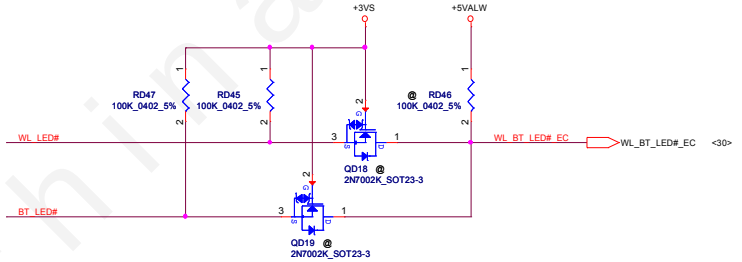
10mils, All pins

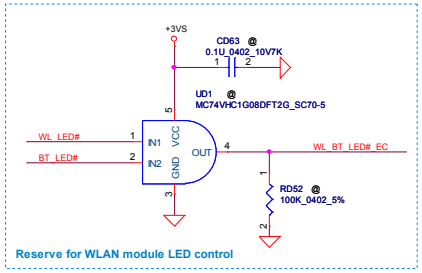


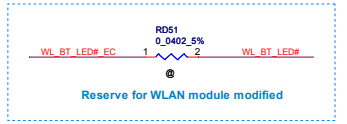
Power LED

Battery LED

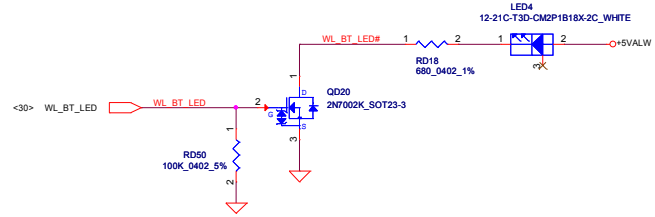








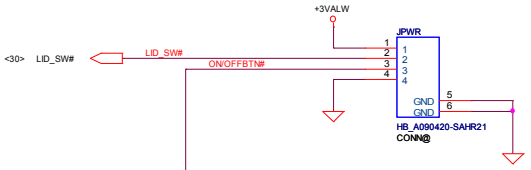
Wireless LED



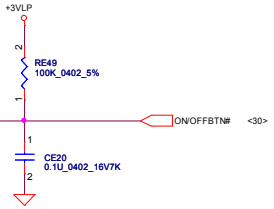
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title: Mini Card/LED			
Size	Document Number: LA-9982P		Rev: 3.0
Date: Wednesday, May 29, 2013	Sheet 26 of 57		

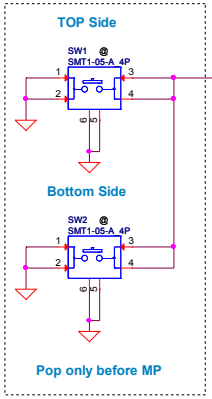
POWER/B



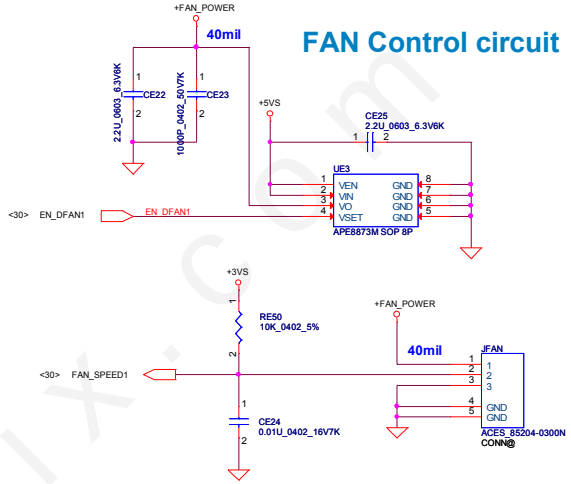
Power ON Circuit



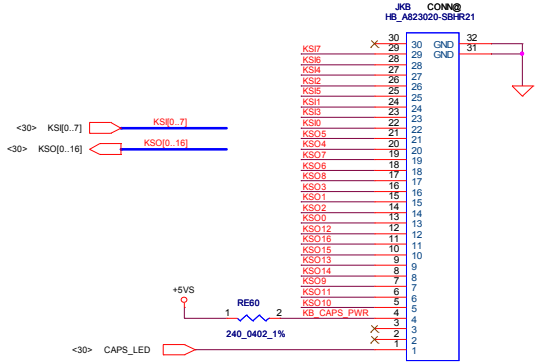
ON/OFF switch



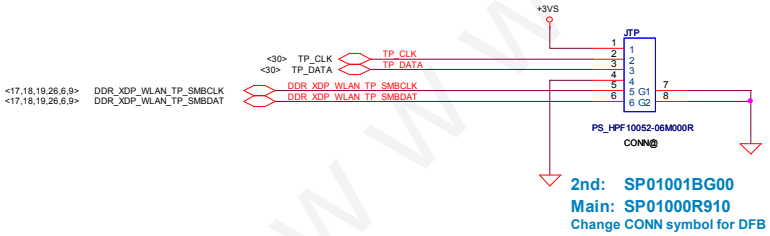
FAN Control circuit



INT_KBD Connector



Touch pad

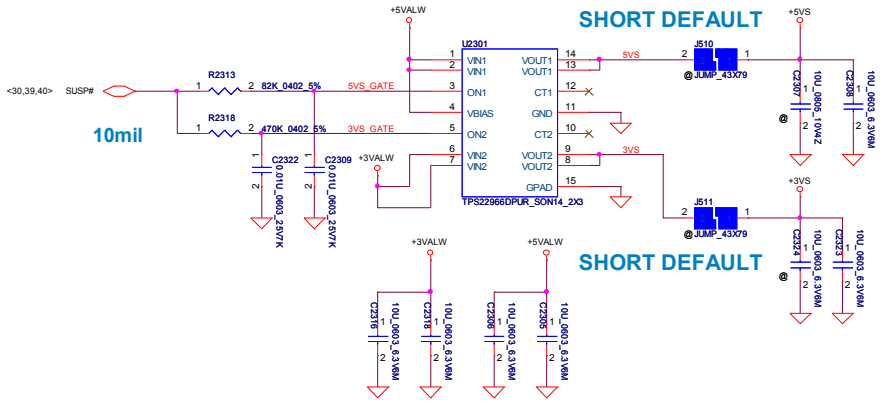


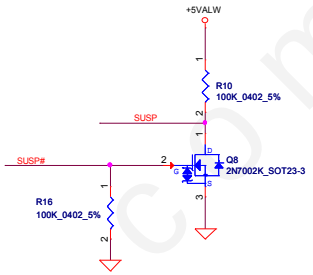
2nd: SP01001BG00
Main: SP01000R910
Change CONN symbol for DFB

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

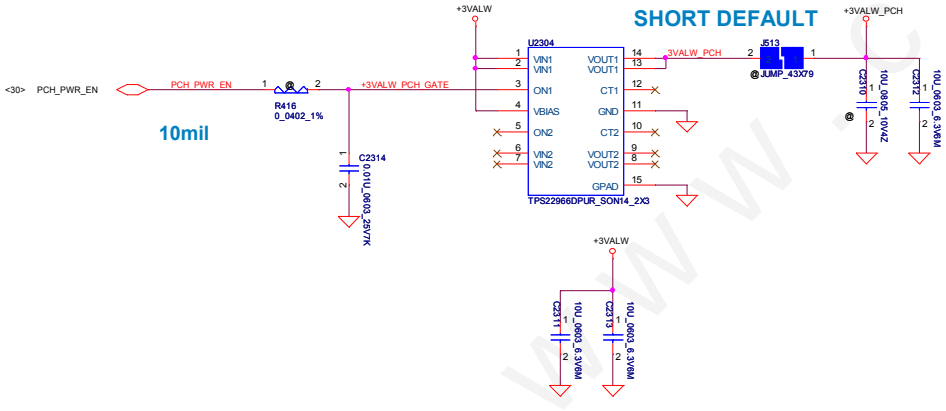
Compal Electronics, Inc.			
Title	FAN/TP/PWR SW		
Size	Document Number		Rev
	LA-9982P		3.0
Date:	Wednesday, May 29, 2013	Sheet	27 of 57

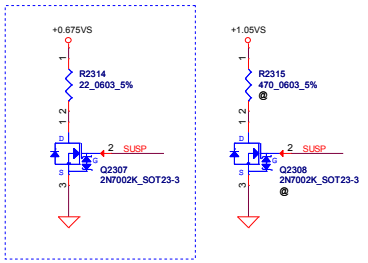
+5VS and +3VS switch





+3VALW_PCH switch

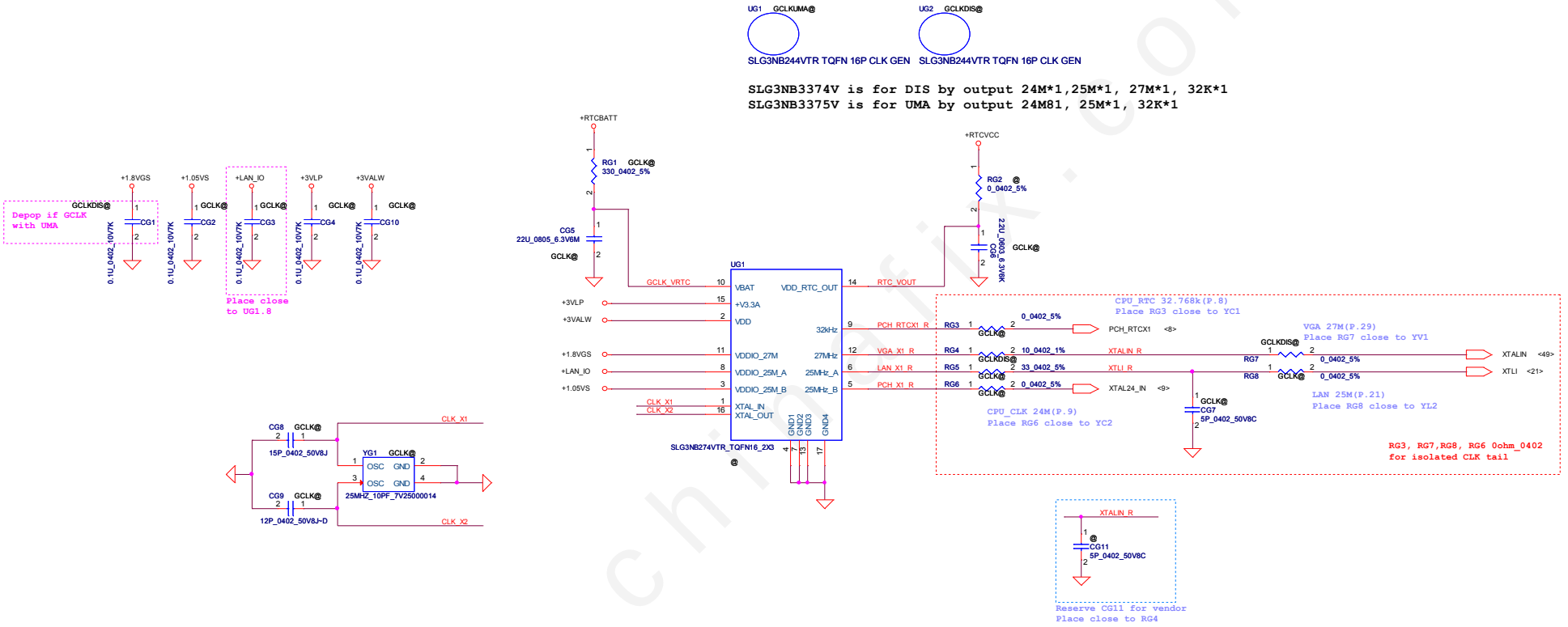




For Intel S3 Power Reduction

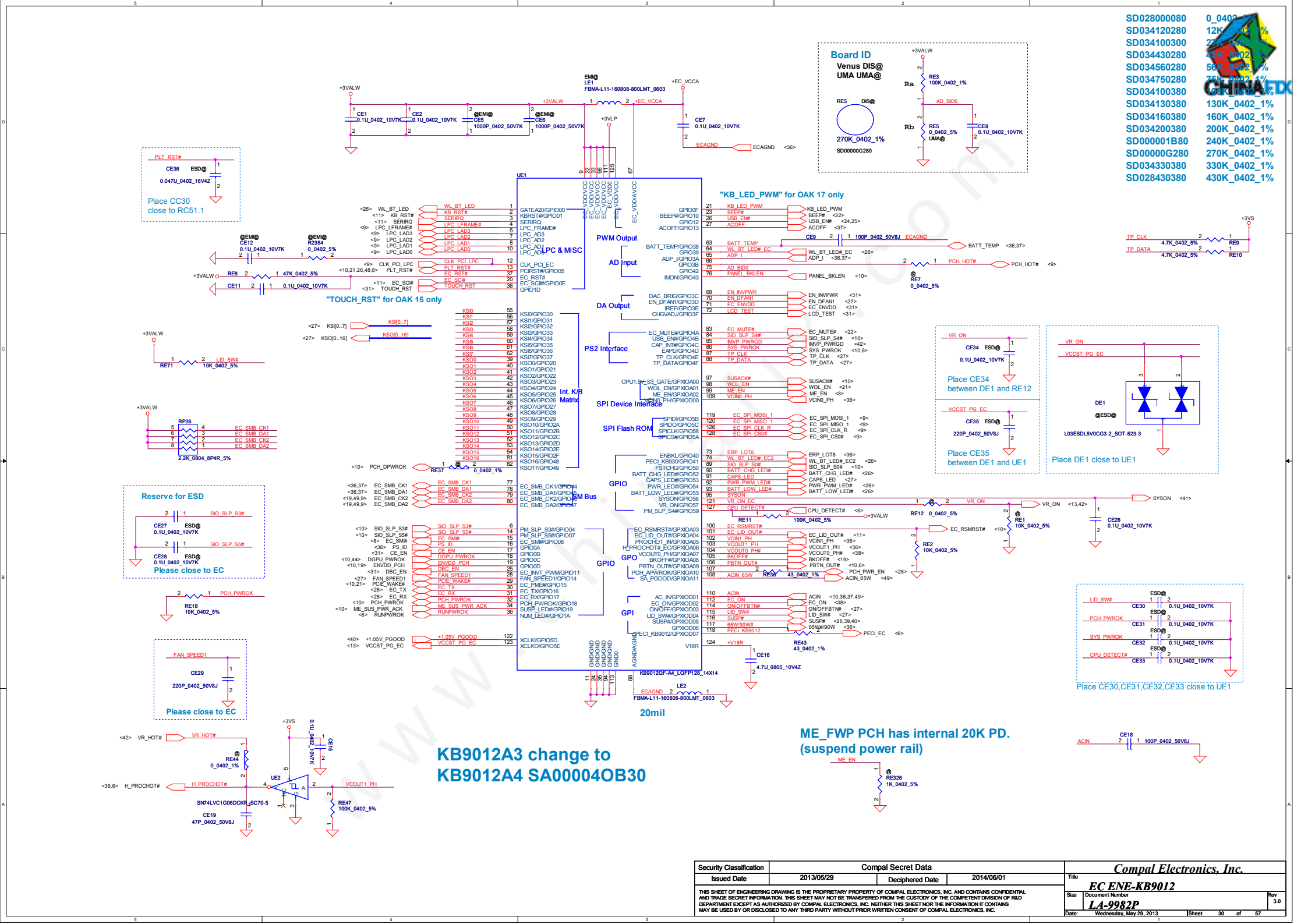
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title	DC/DC Interface		
Size	Document Number	LA-9982P	Rev 3.0
Date:	Wednesday, May 29, 2013	Sheet 28 of 57	



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title: GCLK			
Size	Document Number: LA-9982P		Rev: 3.0
Date: Wednesday, May 29, 2013	Sheet 23 of 57		



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

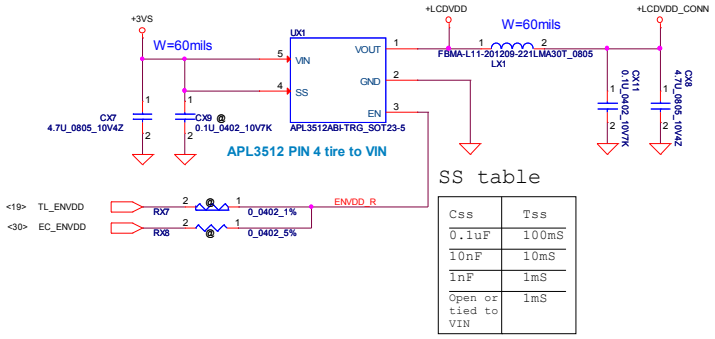
Compal Electronics, Inc.

Title: EC ENE-KB9012

Size: | Document Number: LA-9982P | Rev: 3.0

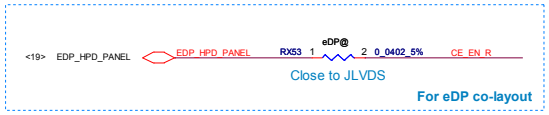
Date: Wednesday, May 29, 2013 | Sheet 30 of 57

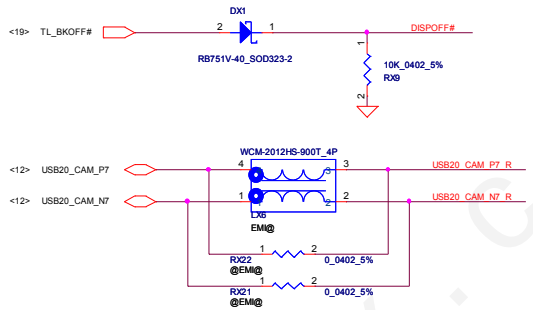
LCD PWR CTRL



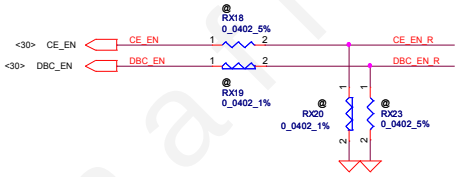
SS table

Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

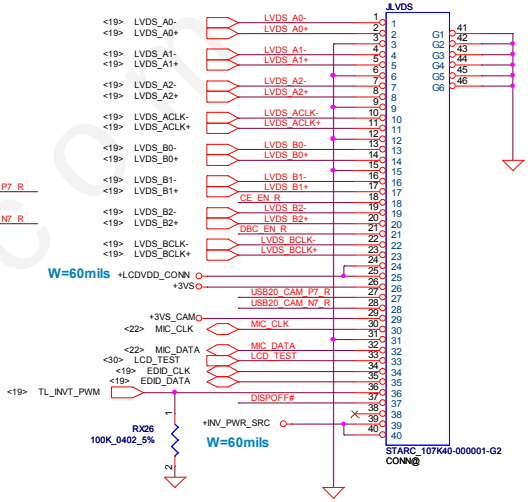


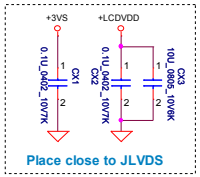


CE_EN_R only for reserve.

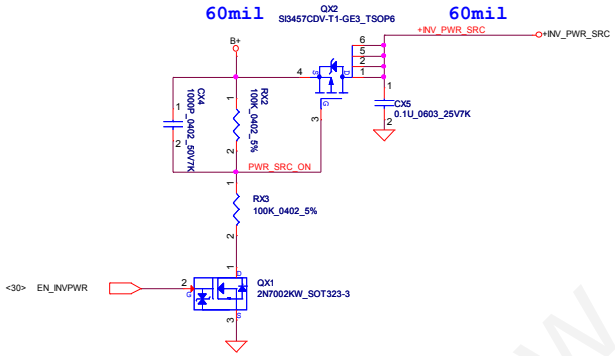


LVDS Connector

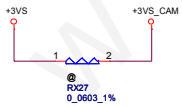




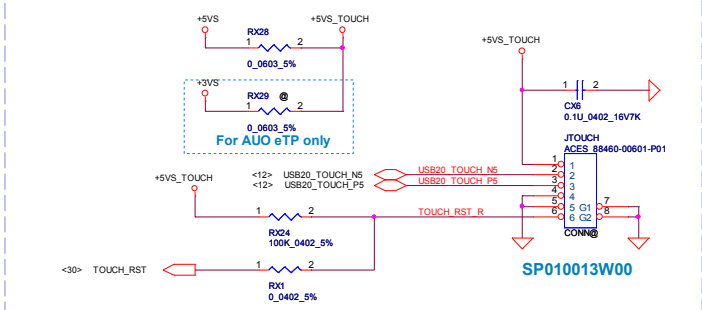
LCD backlight PWR CTRL



Webcam PWR CTRL



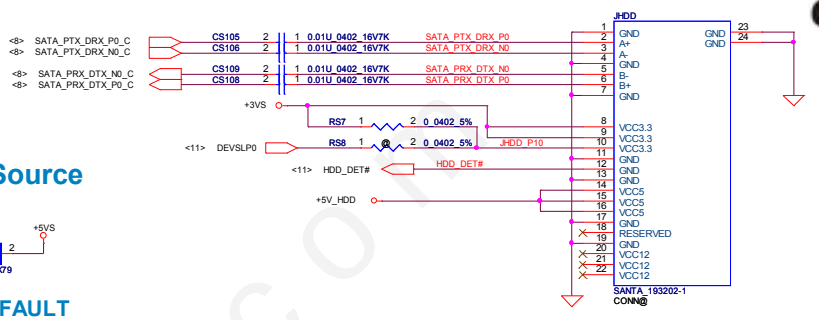
* Touch Screen Panel



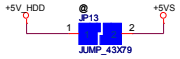
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title	LVDS/webcam/touch		
Size	Document Number	LA-9982P	Rev 3.0
Date: Wednesday, May 29, 2013	Sheet 31 of 57		

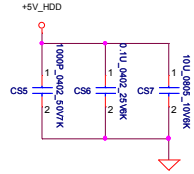
SATA HDD Connector



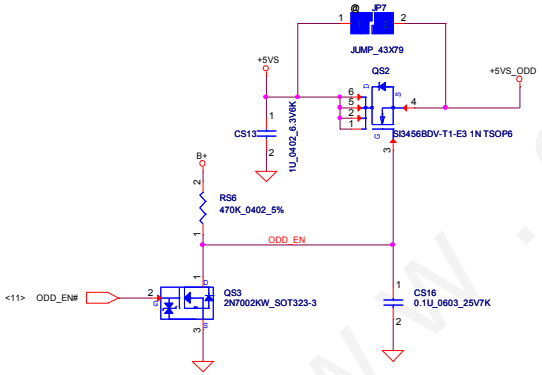
+5V_HDD Source



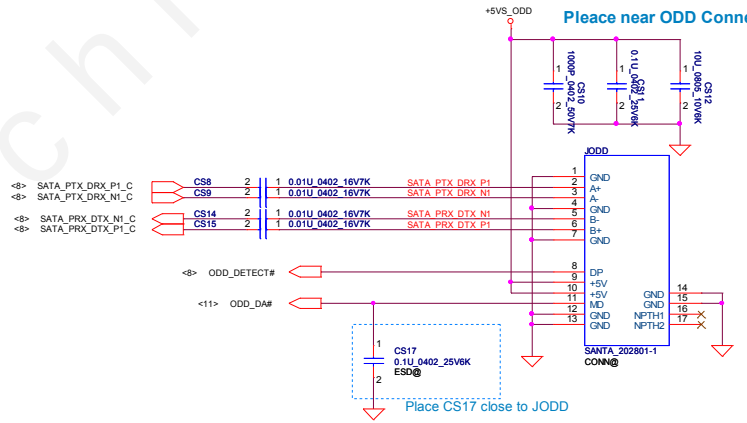
SHORT DEFAULT



ODD Power Control



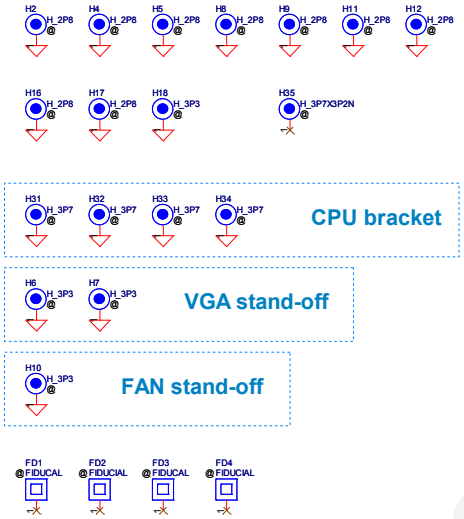
SATA ODD Connector

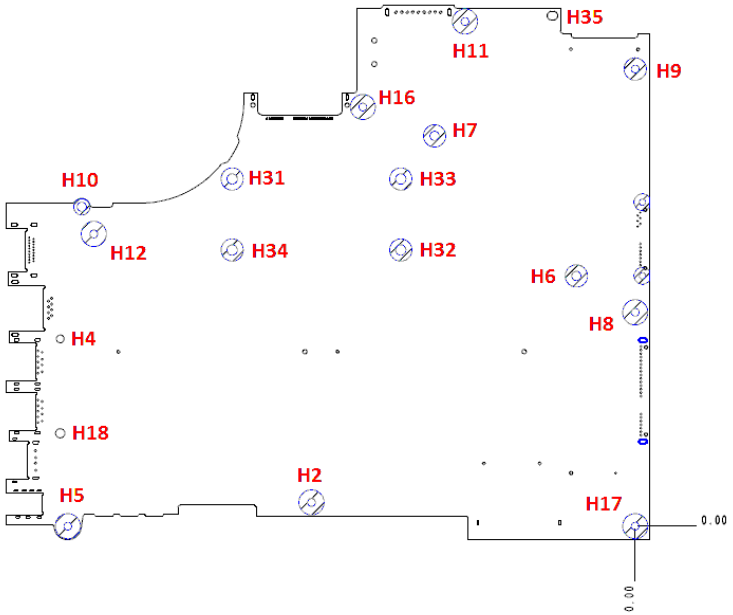


Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.	
Title	HDD/ODD
Size	Document Number: LA-9982P
Rev	3.0
Date:	Wednesday, May 29, 2013
Sheet	32 of 57

Screw Hole





Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: Screw Hole

Size | Document Number: LA-9982P | Rev: 3.0

Date: Wednesday, May 29, 2013 | Sheet 33 of 57

Version Change List (P. I. R. List)

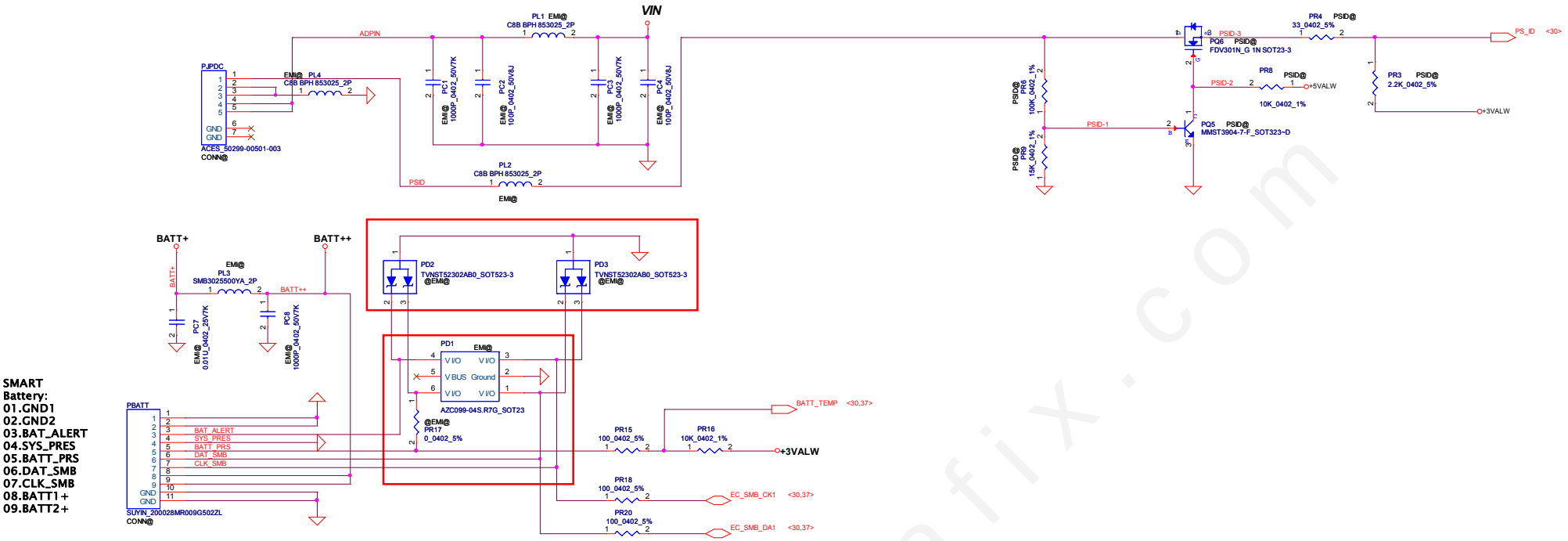
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							
20							
21							
22							
23							
24							
25							
26							
27							
28							
29							
30							
31							
32							
33							
34							
35							
36							
37							
38							
39							
40							
41							

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.
Title: HW-PIR Page.1
Size: Document Number: LA-9982P
Rev: 3.0
Date: Wednesday, May 29, 2013 Sheet 34 of 57

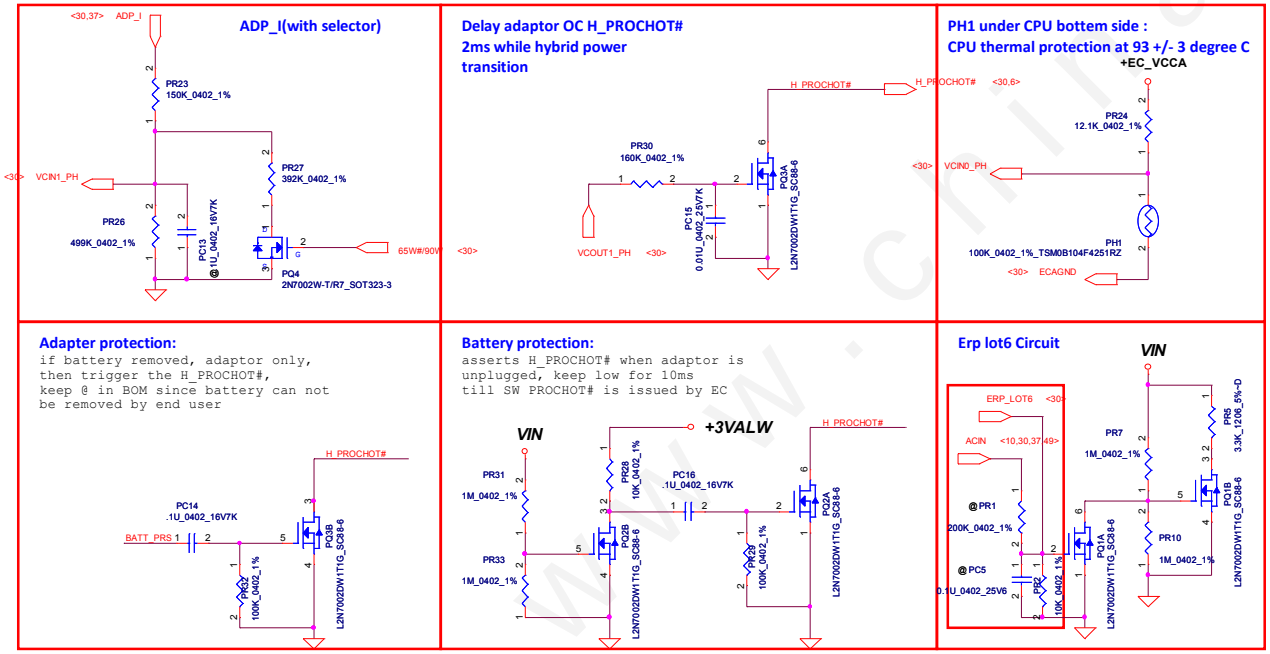
Version Change List (P. I. R. List) Page 2

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40							
41							
42							
43							
44							
45							
46							
47							
48							
49							
50							
51							
52							
53							
54							



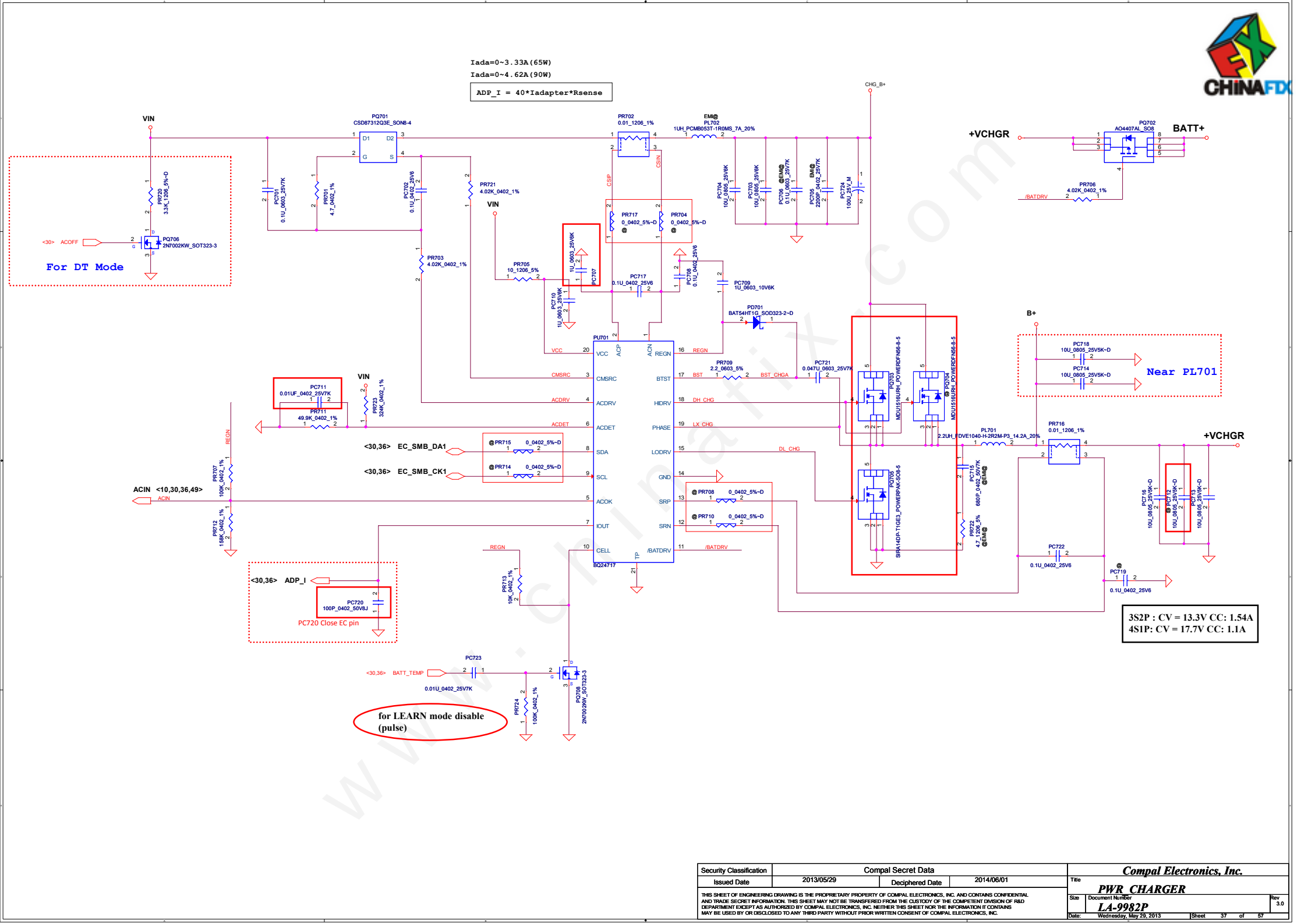
SMART Battery:
01.GND1
02.GND2
03.BAT_ALERT
04.SYS_PRES
05.BATT_PRS
06.DAT_SMB
07.CLK_SMB
08.BATT1+
09.BATT2+

Other component (37.1)



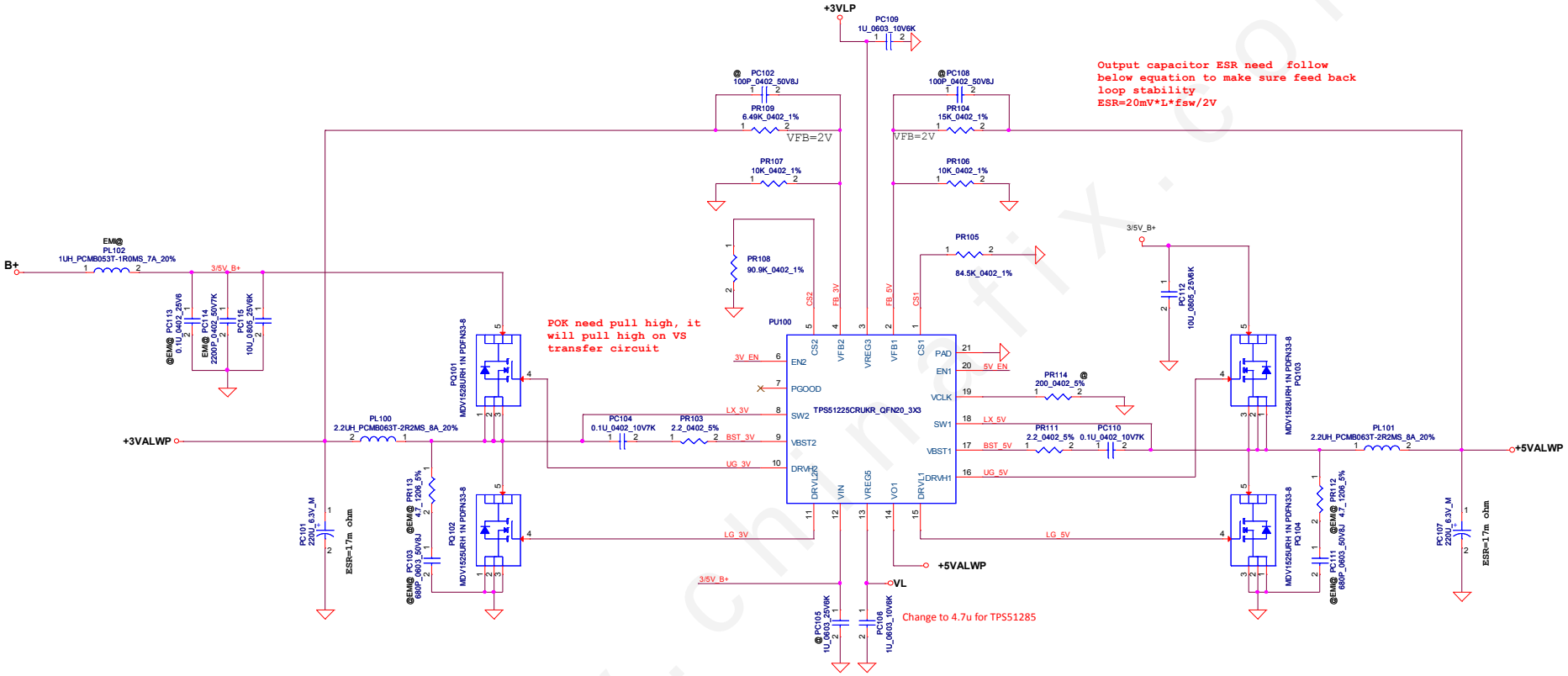
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.	
Title	PWR_DCIN/BATT CONN/OTP
Size	Document Number: LA-9982P
Rev	3.0
Date:	Wednesday, May 29, 2013
Sheet	36 of 57



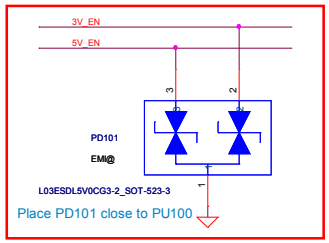
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

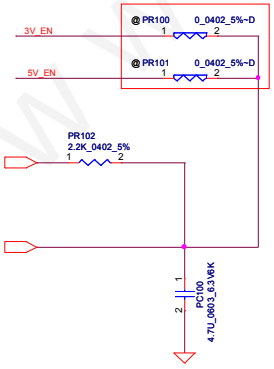
Compal Electronics, Inc.		
Title: PWR_CHARGER		
Size	Document Number: LA-9982P	Rev: 3.0
Date: Wednesday, May 29, 2013	Sheet 37 of 57	



3VALWP
TDC 5.95A
Peak Current 8.5A
OCP current 10.2A

	TYP	MAX
H/S Rds(on):	22mohm ,	30mohm
L/S Rds(on):	10.8mohm ,	13.6mohm





5VALWP
TDC 5.96A
Peak Current 8.51A
OCP current 10.2A

	TYP	MAX
H/S Rds(on):	22mohm ,	30mohm
L/S Rds(on):	10.8mohm ,	13.6mohm

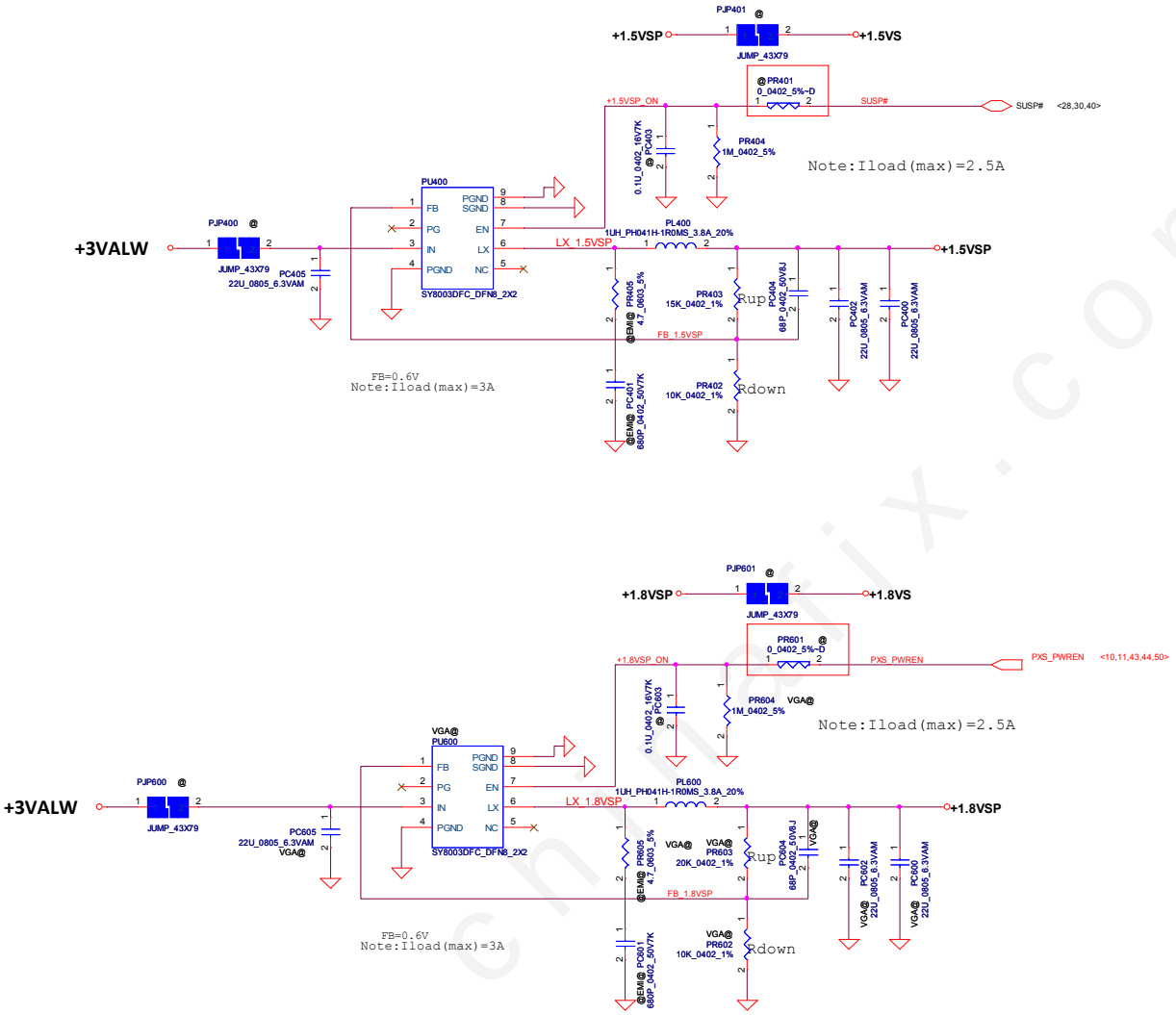
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: PWR_3.3VALWP/5VALWP

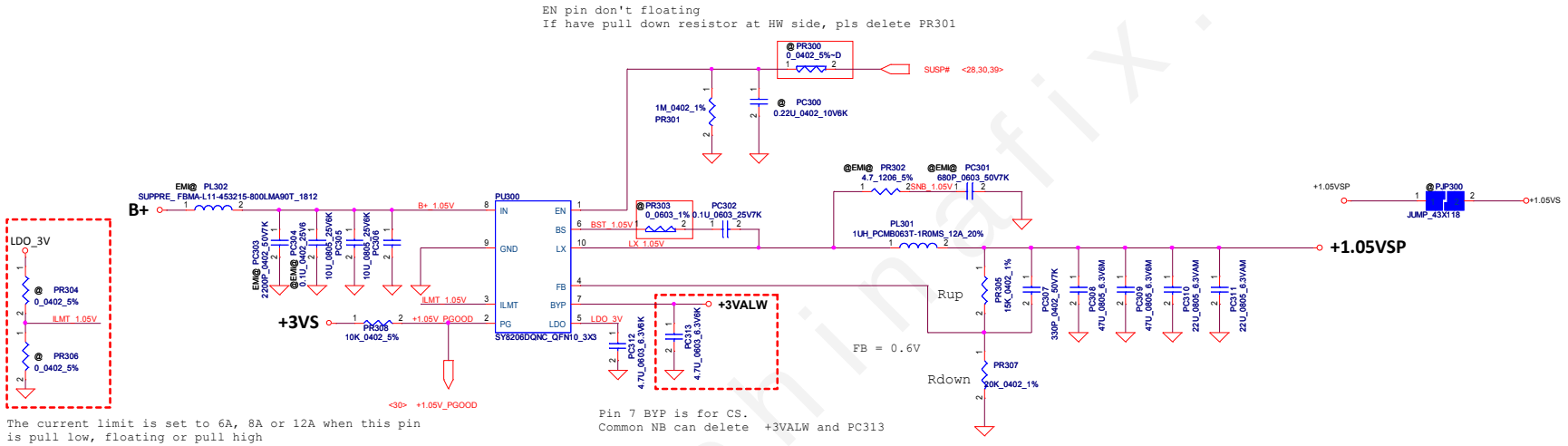
Size | Document Number: LA-9982P | Rev: 3.0

Date: Wednesday, May 29, 2013 | Sheet 38 of 57



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title	PWR_1.5VSP/1.8VSP		
Size	Document Number	LA-9982P	Rev 3.0
Date:	Wednesday, May 29, 2013	Sheet 39 of 57	



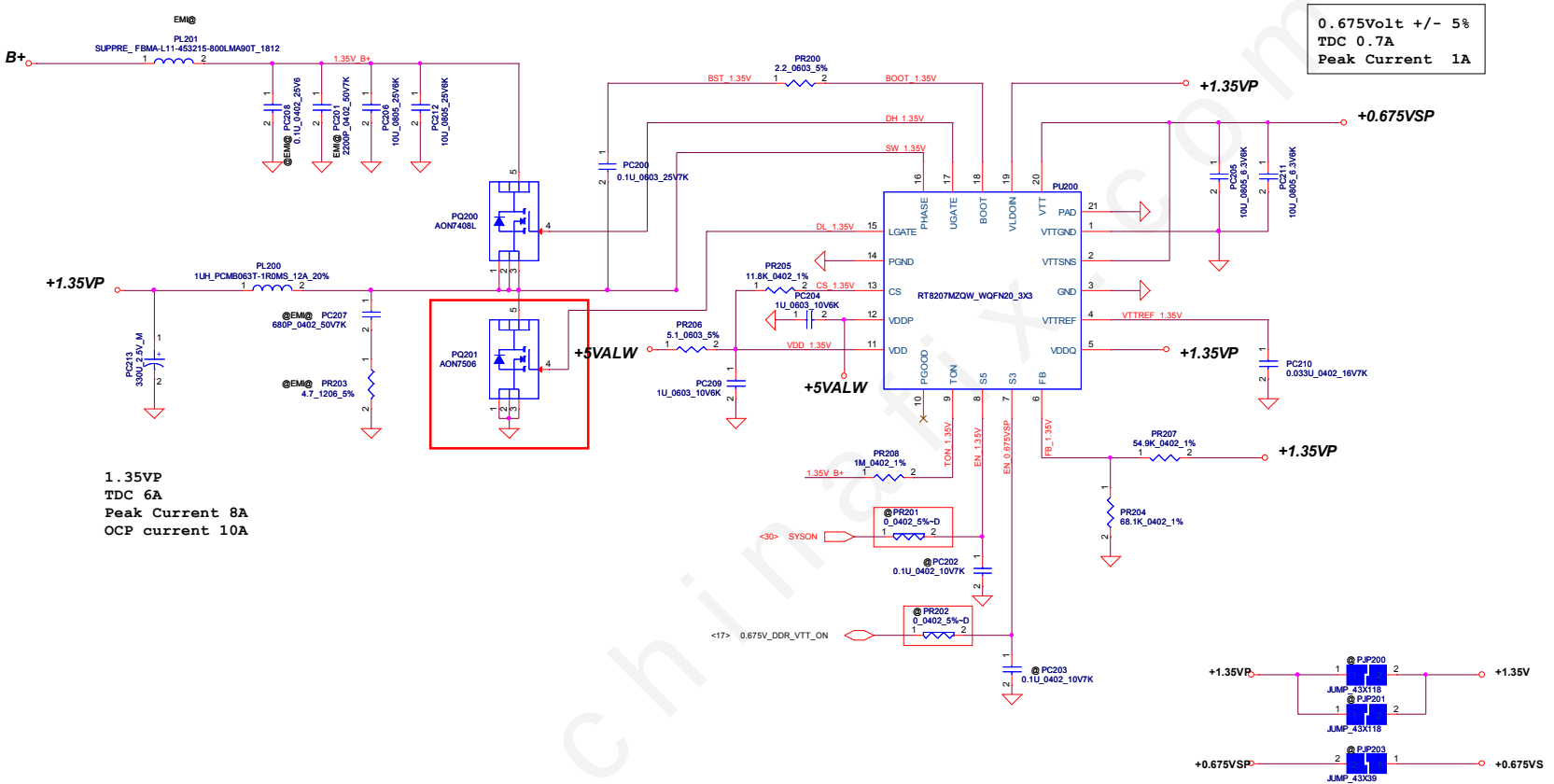
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: PWR_+VCCIO

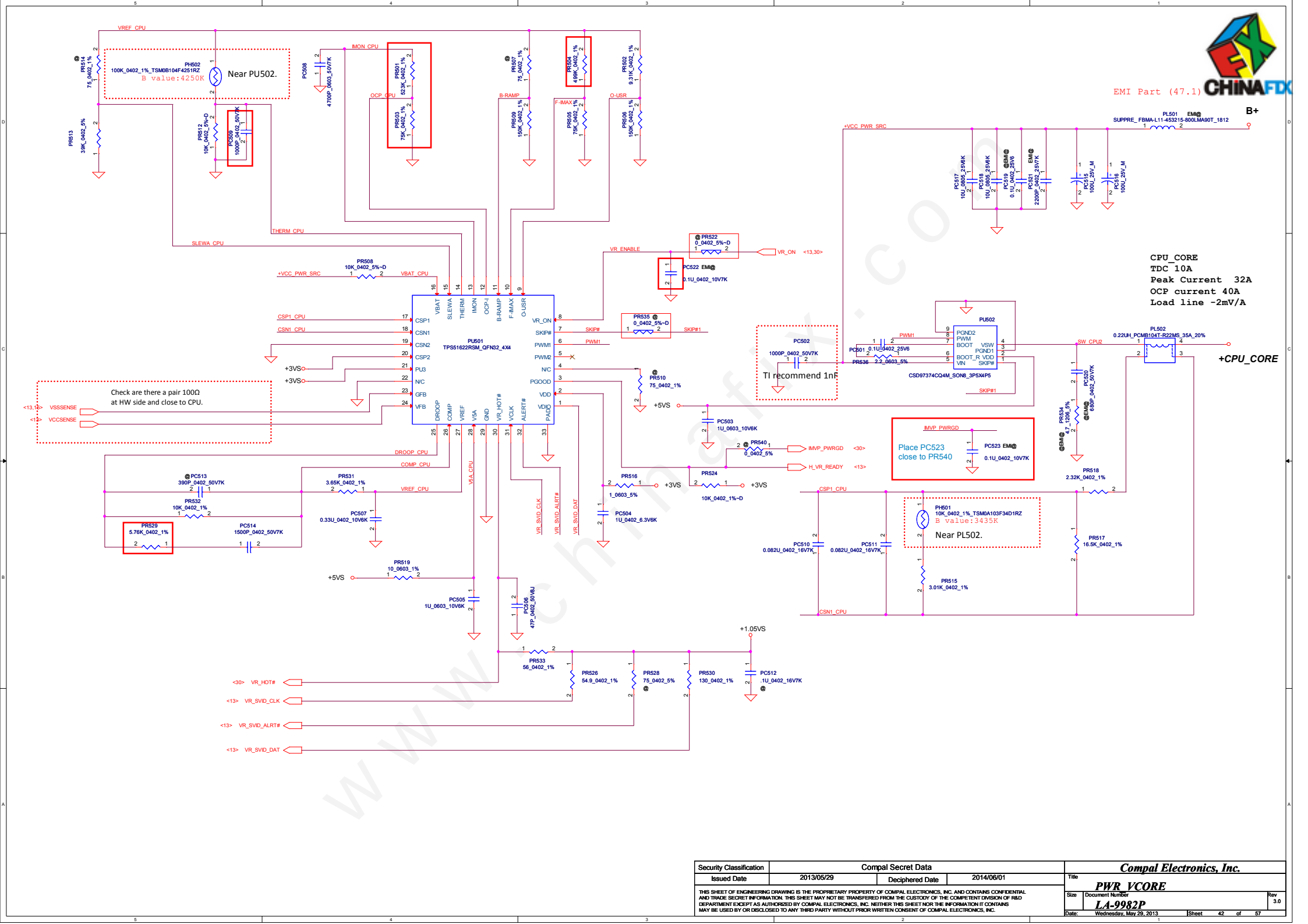
Size	Document Number	Rev
C		3.0

Date: Wednesday, May 29, 2013 Sheet 40 of 57



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.		
Title: PWR_+1.35VP/0.675VSP		
Size	Document Number: LA-9982P	Rev: 3.0
Date: Wednesday, May 29, 2013	Sheet 41 of 57	



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title: PWR_VCORE			
Size	Document Number: LA-9982P		Rev: 3.0
Date: Wednesday, May 29, 2013	Sheet 42 of 57		

TDC=9A
Peak Current=13A
OCP=16A

	VDDCI_VID (GPIO_6)
High	0.95V
Low	0.9V

+VDDCIP
TDC 7A
Peak Current 13A
OCP current 16A

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC1205

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=0.9V

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

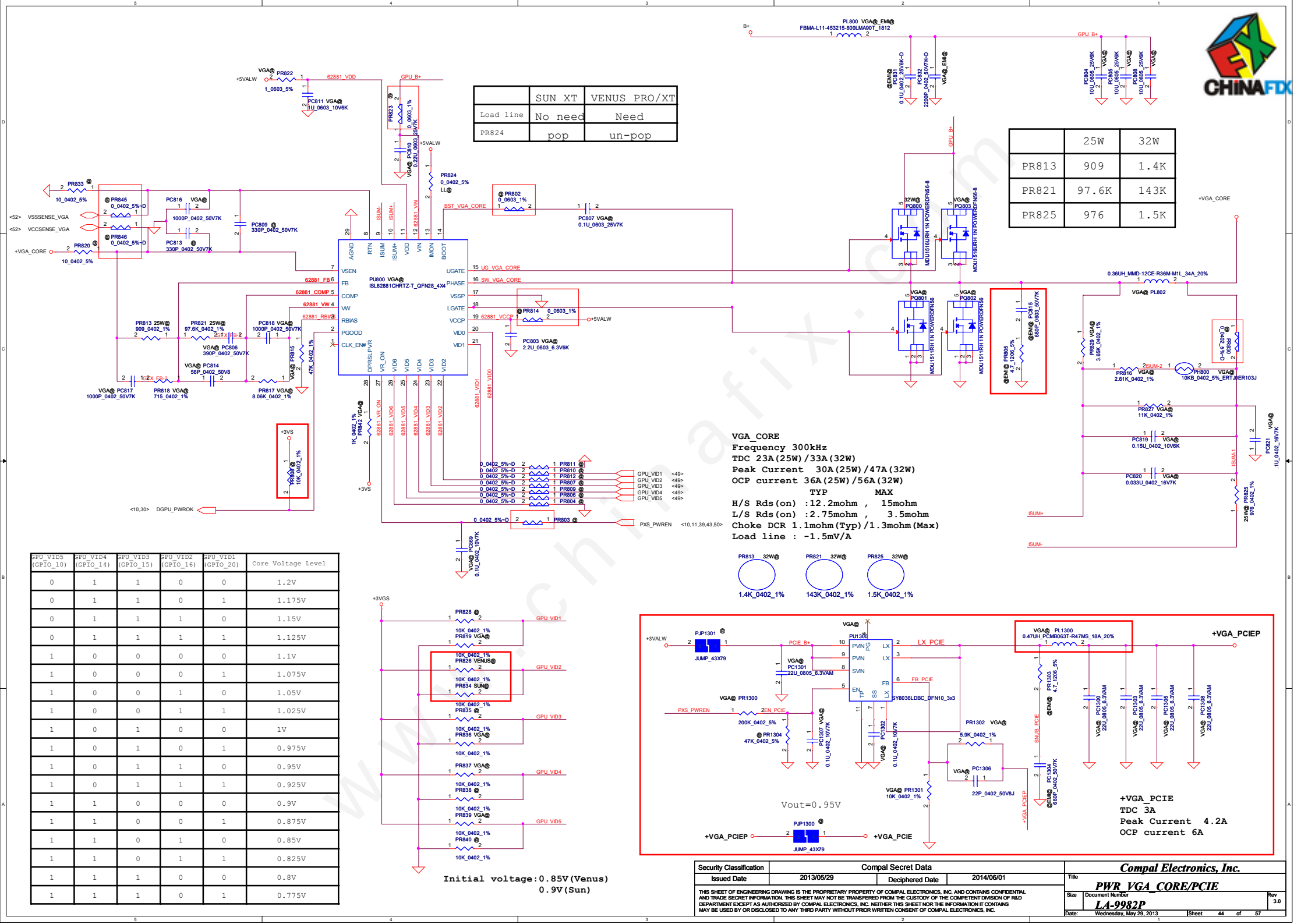
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: PWR +1.35VGPU/VDDCIP

Size | Document Number: LA-9982P | Rev: 3.0

Date: Wednesday, May 29, 2013 | Sheet 43 of 57



	SUN XT	VENUS PRO/XT
Load line	No need	Need
PR824	pop	un-pop

	25W	32W
PR813	909	1.4K
PR821	97.6K	143K
PR825	976	1.5K

VGA_CORE
Frequency 300kHz
TDC 23A(25W)/33A(32W)
Peak Current 30A(25W)/47A(32W)
OCP current 36A(25W)/56A(32W)

	TYP	MAX
H/S Rds(on)	:12.2mohm ,	15mohm
L/S Rds(on)	:2.75mohm ,	3.5mohm

Choke DCR 1.1mohm(Typ)/1.3mohm(Max)
Load line : -1.5mV/A

PR813 32W@ 1.4K_0402_1%
PR821 32W@ 143K_0402_1%
PR825 32W@ 1.5K_0402_1%

GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	0	0	1.2V
0	1	1	0	1	1.175V
0	1	1	1	0	1.15V
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V
1	1	1	0	1	0.775V

Initial voltage:0.85V(Venus)
0.9V(Sun)

+VGA_PCIE
TDC 3A
Peak Current 4.2A
OCP current 6A

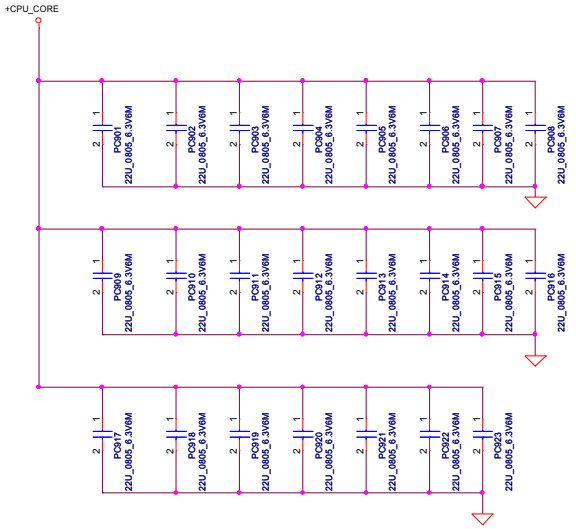
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

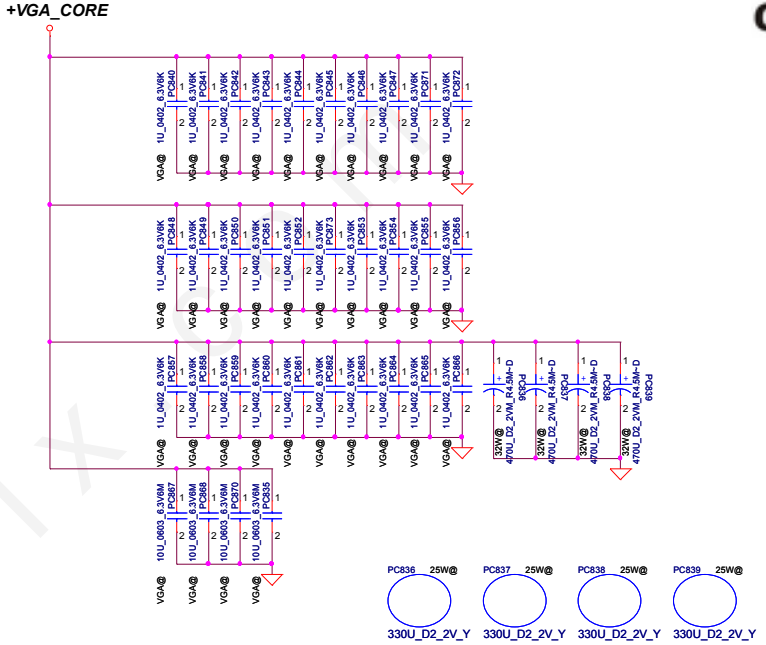
Compal Electronics, Inc.

Title: PWR_VGA_CORE/PCIE

Size: | Document Number: LA-9982P | Rev: 3.0

Date: Wednesday, May 29, 2013 | Sheet 44 of 57





Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

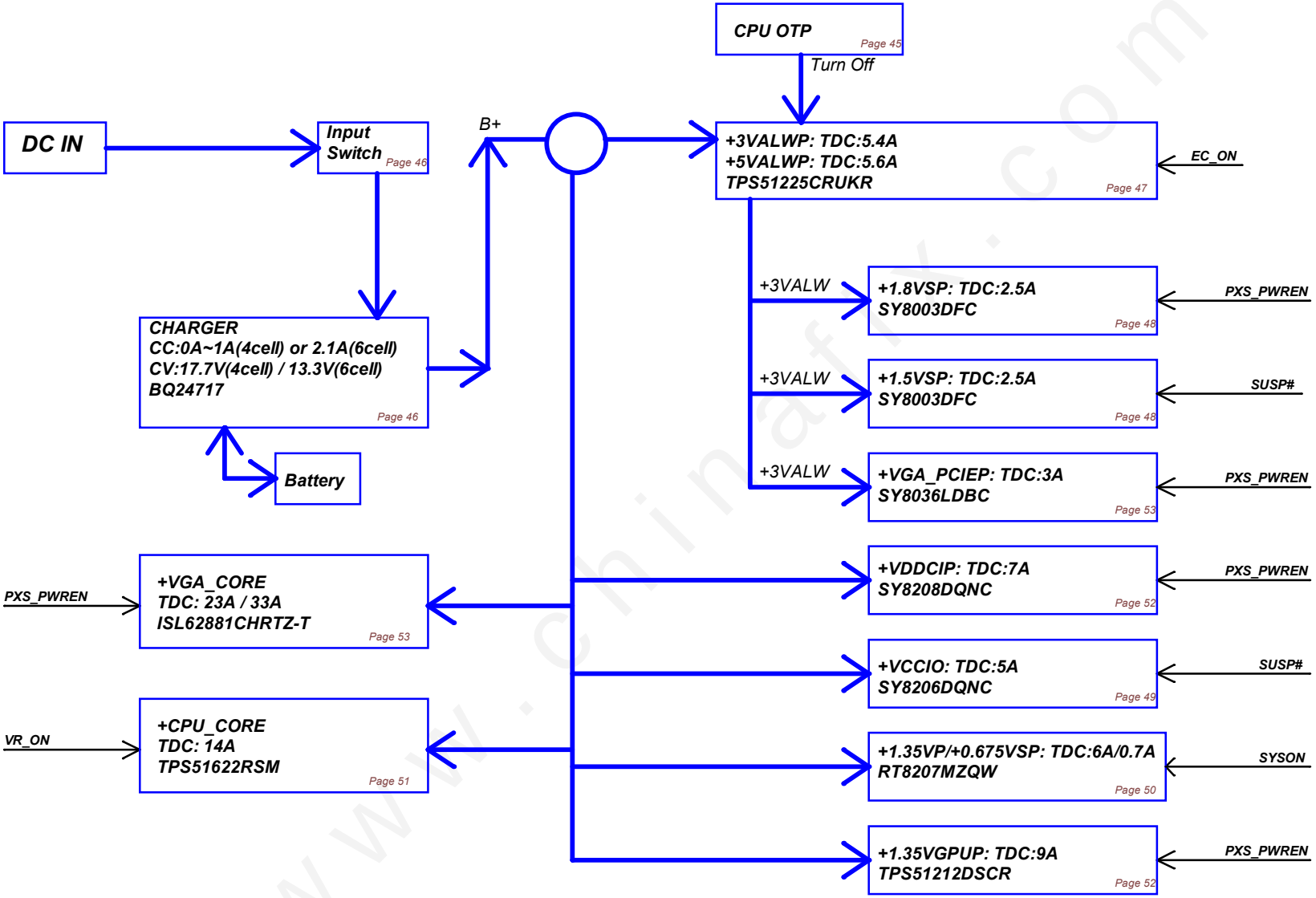
Compal Electronics, Inc.

Title: **PWR_PROCESSOR DECOUPLING**

Size	Document Number	Rev
	LA-9982P	3.0

Date: Wednesday, May 29, 2013 Sheet 45 of 57

Power block



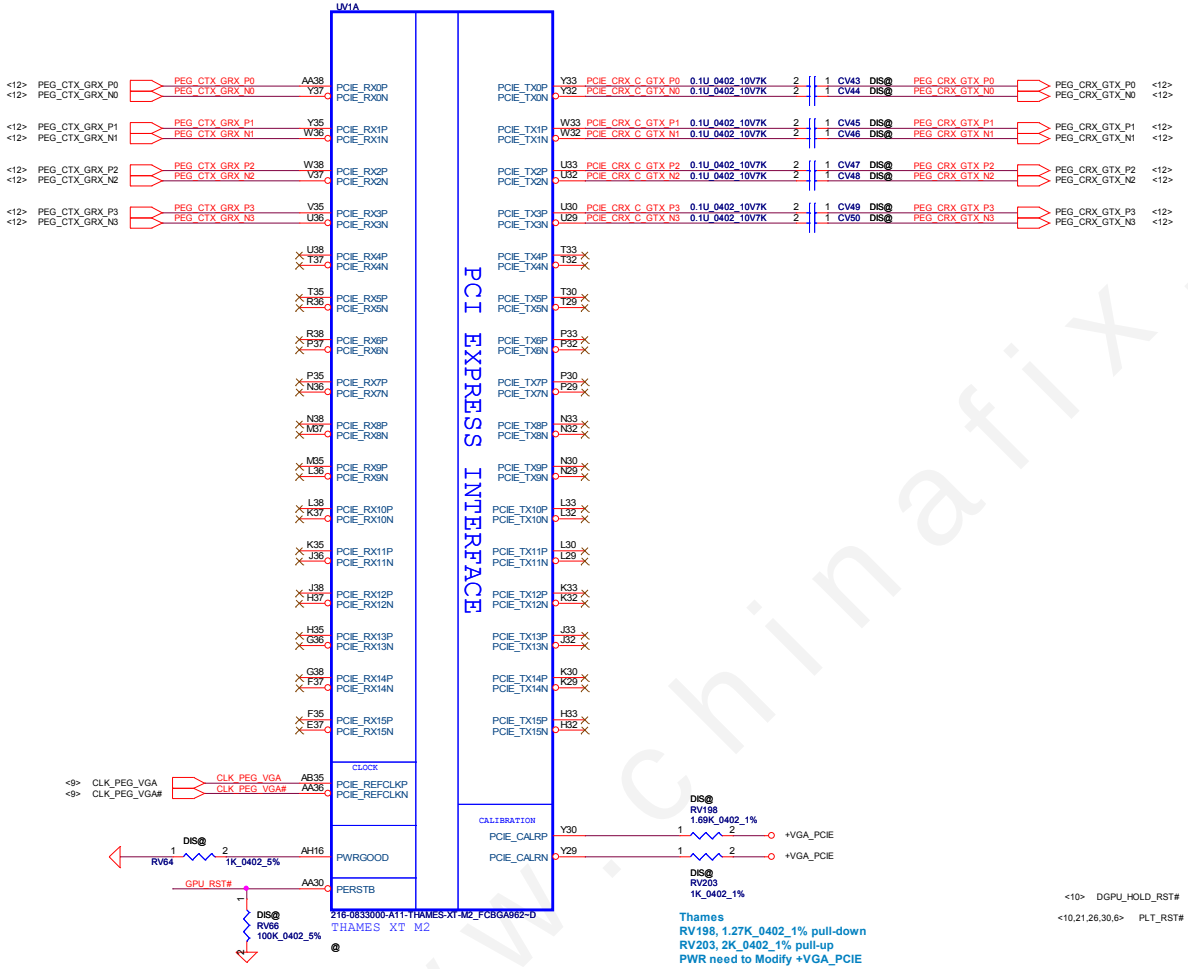
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.	
Title	PWR_POWER BLOCK DIAGRAM
Size	Document Number: LA-9982P
Rev	3.0
Date:	Wednesday, May 29, 2013
Sheet	46 of 57

Version Change List (P. I. R. List)

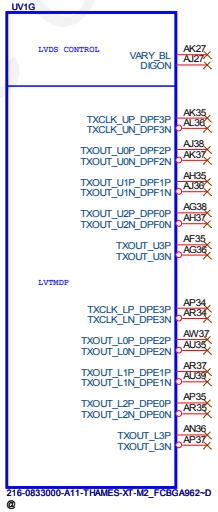
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	CHARGER	13/01/30	Morris	adjust design parameter from vendor recommend	delete PD702 change PC712 to unpop change PQ704 to unpop change PC707 from 0.1uF_0402 to 1uF_0603 change PC720 from 0.1uF to 100pF change PC711 from 1000pF to 0.01uF change PQ705 from SB00000SD00 to SB00000WY00	0.3
2	42	VCORE	13/01/30	Morris	adjust design parameter from vendor recommend	change PC509 from 0.1uF to 1000pF change PR529 from 3.83K to 5.76K change PR504 from 523K to 499K	0.3
3	36	DCIN/BATT CONN/OTP	13/01/30	Morris	change from ESD request	change PD1 from SC300002E00 to SC300001G00	0.3
4	38	3.3VALWP/5VALWP	13/02/01	Morris	add ESD diode from ESD request	add PD101(SCA00002A00)	0.3
5	42	VCORE	13/02/21	Morris	adjust design parameter from fine tune result	change PR501 from 422K to 523K change PR503 from 56K to 75K	0.3
6	44	VGA_CORE/PCIE	13/02/21	Morris	unpop from EE request	unpop PR808	0.3
7	44	VGA_CORE/PCIE	13/03/05	Morris	adjust output voltage from vender request	unpop PR826 and pop PR834 (only for Sun XT)	0.4
8	37 38 39 40 41 42	CHARGER 3.3VALWP/5VALWP 1.5VSP/1.8VSP +VCCIO +1.35VP/0.675VSP VCORE	13/03/28	Morris	verify function ok, so delete 0 ohm to short	unpop PR100,PR101,PR201,PR202,PR300,PR303,PR401,PR522,PR535, PR704,PR708,PR710,PR714,PR715,PR717	1.0
9	36	DCIN/BATT CONN/OTP	13/04/09	Morris	design change for solve issue	unpop PR1 and PC5	2.0
10	41 43	+1.35VP/0.675VSP +1.35VGPU/VDDCI	13/04/09	Morris	part shortage issue	change PQ201 and PQ1101 from SB00000T600 to SB000010A00	2.0
11	39 43 44	1.5VSP/1.8VSP +1.35VGPU/VDDCI VGA_CORE/PCIE	13/04/09	Morris	verify function ok, so delete 0 ohm to short	unpop PR601,PR802,PR803,PR814,PR823,PR830,PR845,PR846, PR1103,PR1200,PR1206,PR1210	2.0
12	43	+1.35VGPU/VDDCI	13/04/09	Morris	unpop VDDCI parts from vendor recommend and EEverify ok only for Sun XT	unpop PL1200,PL1201,PU1200,PQ1201,PR1201,PR1203,PR1204,PR1208,PR1209, PR1211,PR1212,PR1213,PC1201,PC1202,PC1204,PC1205,PC1206,PC1207, PC1209,PC1210,PC1211,PC1213 (only for Sun XT)	2.0
13	44	VGA_CORE/PCIE	13/04/12	Morris	part shortage issue	change PL1300 from SH00000GQ00 to SH00000PK00	2.0
14	36	DCIN/BATT CONN/OTP	13/04/12	Morris	customer request	add PR2 10Kohm	2.0
15	42	VCORE	13/04/15	Morris	EMI request	pop PC522 and add PC523 0.1uF	2.0
16	36	DCIN/BATT CONN/OTP	13/05/22	Morris	reserve parts from ESD request	reserve PD2,PD3,PR17 and unpop PR17	3.0

GFX PCIE LANE REVERSAL

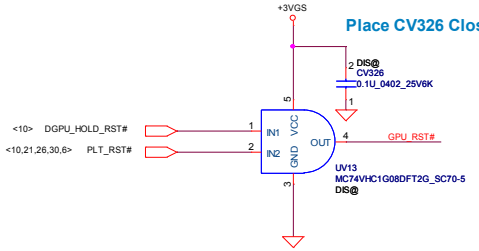


Thames
RV198, 1.27K_0402_1% pull-down
RV203, 2K_0402_1% pull-up
PWR need to Modify +VGA_PCIE

LVDS Interface



Place CV326 Close to UV13



UV1 VENUSXT@

216-0846000 A1 VENUS XT M2 FCBGA 962P 0FD

SA00006KW0L

UV1 VENUSPRO@

216-0846009 A1 VENUS PRO M2 FCBGA 962P 0FD

SA00006MW0L

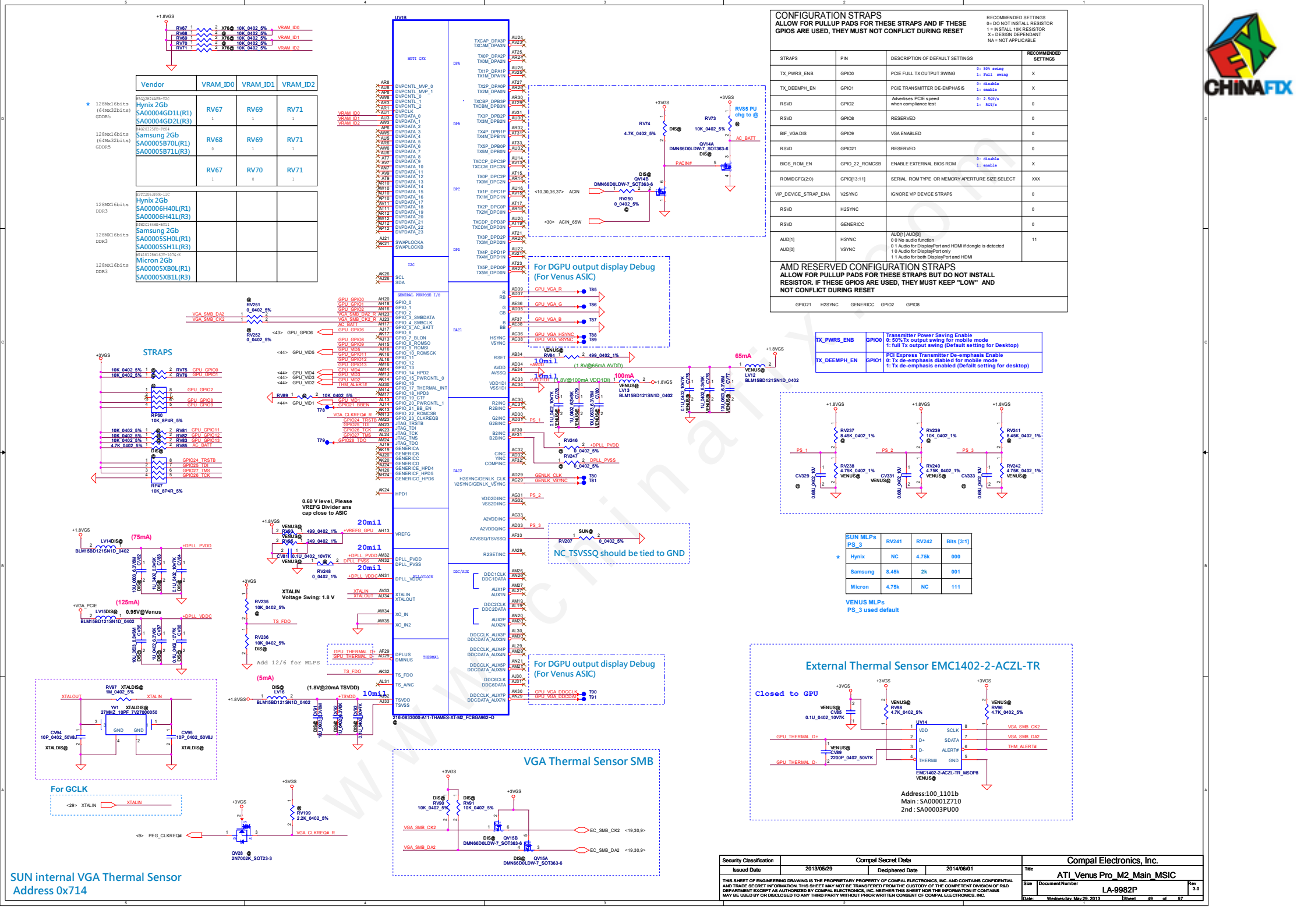
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: ATI_Venus Pro_M2_PCIE/LVDS

Size | Document Number: LA-9982P | Rev: 3.0

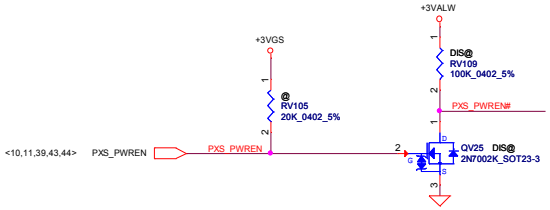
Date: Wednesday, May 29, 2013 | Sheet 48 of 57


CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE
STRAPS | PIN | DESCRIPTION OF DEFAULT SETTINGS | RECOMMENDED SETTINGS
TX_PWRS_ENB | GPIO0 | PCIE FULL TX OUTPUT SWING | 0: 50% swing 1: Full swing | X
TX_DEEMPH_EN | GPIO1 | PCIE TRANSMITTER DE-EMPHASIS | 0: disable 1: enable | X
RSVD | GPIO2 | Advertises PCIE speed when compliance test | 0: 2.5GT/s 1: 5GT/s | 0
RSVD | GPIO8 | RESERVED | | 0
BIF_VGA_DIS | GPIO9 | VGA ENABLED | | 0
RSVD | GPIO21 | RESERVED | | 0
BIOS_ROM_EN | GPIO_22_ROMCSB | ENABLE EXTERNAL BIOS ROM | 0: disable 1: enable | X
ROMIDCFG[2:0] | GPIO[13:11] | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT | | XXX
VIP_DEVICE_STRAP_ENA | V2SYNC | IGNORE VIP DEVICE STRAPS | | 0
RSVD | H2SYNC | | | 0
RSVD | GENERICC | | | 0
AUD[1] AUD[0] | HSYNC VSYNC | AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI | | 11
AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET
GPIO21 H2SYNC GENERICC GPIO2 GPIO8
TX_PWRS_ENB GPIO0 Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN GPIO1 PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)
Vendor | VRAM_ID0 | VRAM_ID1 | VRAM_ID2
128Mx16bits (64Mx32bits) GDDR5
Hynix 2Gb SA00004GD1L(R1) SA00004GD2L(R3) | RV67 1 | RV69 1 | RV71 1
Samsung 2Gb SA00005B70L(R1) SA00005B71L(R3) | RV68 0 | RV69 1 | RV71 1
RV67 1 | RV70 0 | RV71 1
128MX16bits DDR3
Hynix 2Gb SA00006H40L(R1) SA00006H41L(R3)
Samsung 2Gb SA00005SH0L(R1) SA00005SH1L(R3)
Micron 2Gb SA00005XB0L(R1) SA00005XB1L(R3)
UV1B
MUTI GFX
DPA
DPB
DPC
DPD
I2C
GENERAL PURPOSE I/O
DAC1
DAC2
DDC/AUX
THERMAL
For DGPU output display Debug (For Venus ASIC)
For DGPU output display Debug (For Venus ASIC)
NC_TSVSSQ should be tied to GND
SUN MLPs PS_3 | RV241 | RV242 | Bits [3:1]
Hynix | NC | 4.75k | 000
Samsung | 8.45k | 2k | 001
Micron | 4.75k | NC | 111
VENUS MLPs PS_3 used default
STRAPS
XTALIN Voltage Swing: 1.8 V
0.60 V level, Please VREFG Divider ans cap close to ASIC
Add 12/6 for MLPS
For GCLK
External Thermal Sensor EMC1402-2-ACZL-TR
Closed to GPU
Address:100_1101b
Main : SA00001Z710
2nd : SA00003PU00
VGA Thermal Sensor SMB
SUN internal VGA Thermal Sensor
Address 0x714
Security Classification Compal Secret Data
Issued Date 2013/05/29 Deciphered Date 2014/06/01
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title ATI_Venus Pro_M2_Main_MSIC
Size Document Number LA-9982P Rev 3.0
Date: Wednesday, May 29, 2013 Sheet 49 of 57

PX_MODE=1 for Normal Operation
PX_MODE=0 for BACO mode to shut down power rails expcept VDDR3,PCIE_VDDC and 1.8V rail

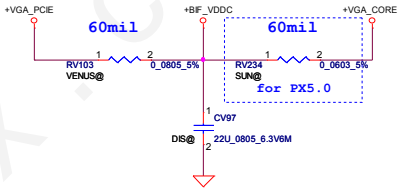
Note:

PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON
PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF
PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

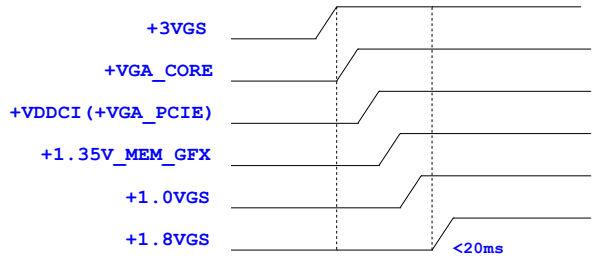


for PX4.0 and PX5.0

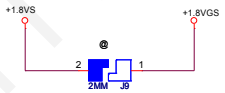
Switch circuits in BACO desingns for Thames/Seymour only 55mA@1.0V, in BACO mode



Power seguence of Sun XT,Venus Pro,Venus XT

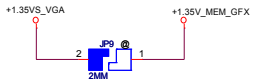


+1.8VS TO +1.8VGS



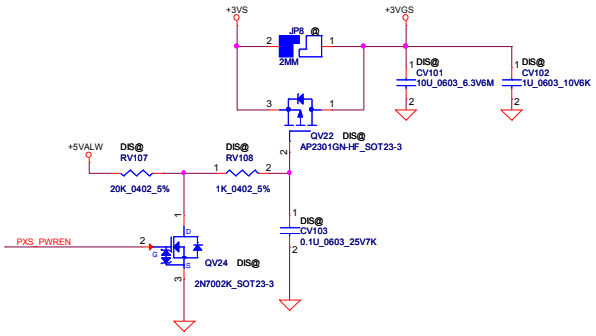
SHORT DEFAULT

+1.35VS_VGA TO +1.35V_MEM_GFX



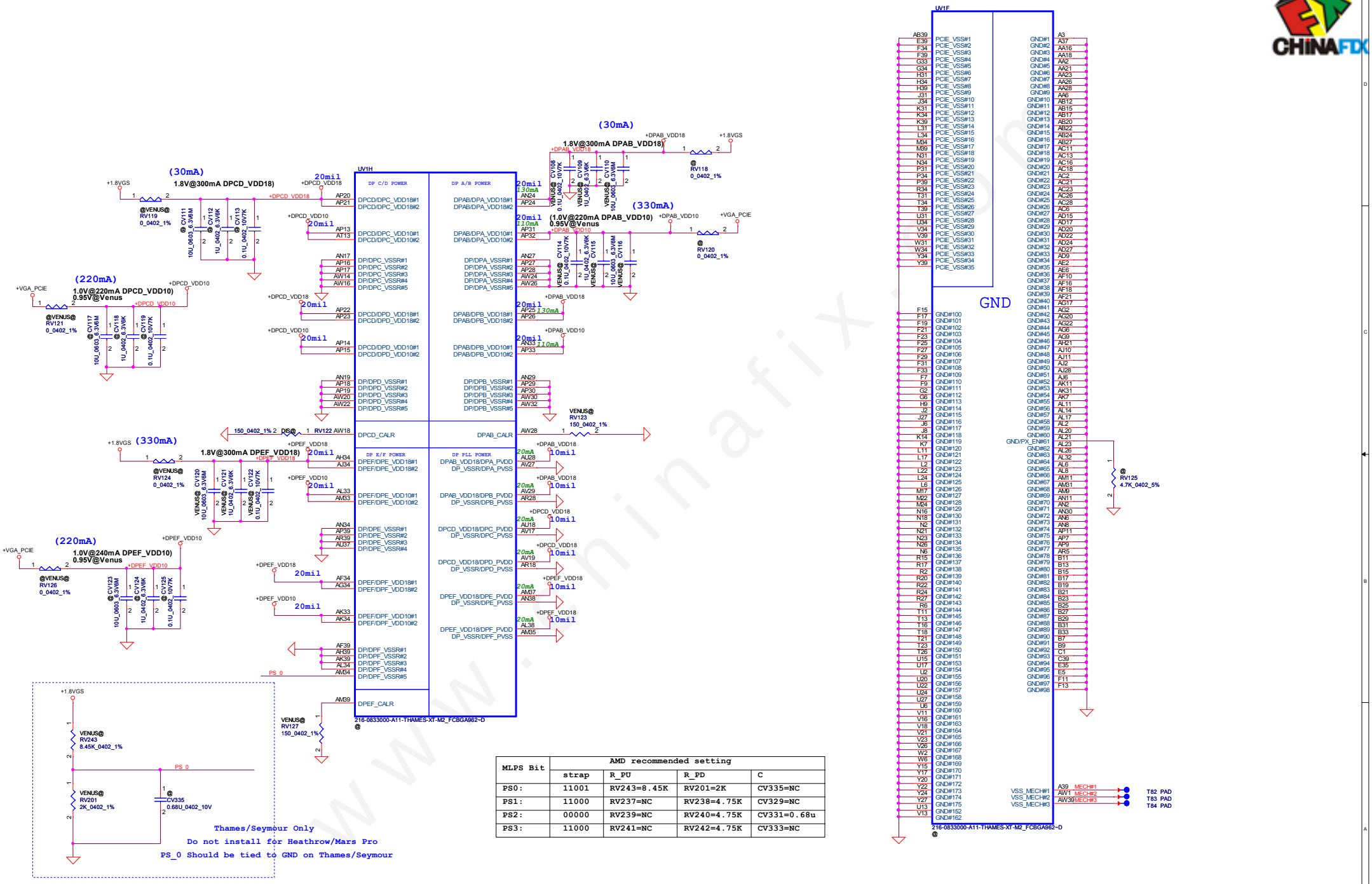
SHORT DEFAULT

+3VS TO +3VGS



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title	ATI_Venus Pro_M2_BACO POWER		
Size	Document Number		Rev
	LA-9982P		3.0
Date:	Wednesday, May 29, 2013	Sheet	50 of 57



MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

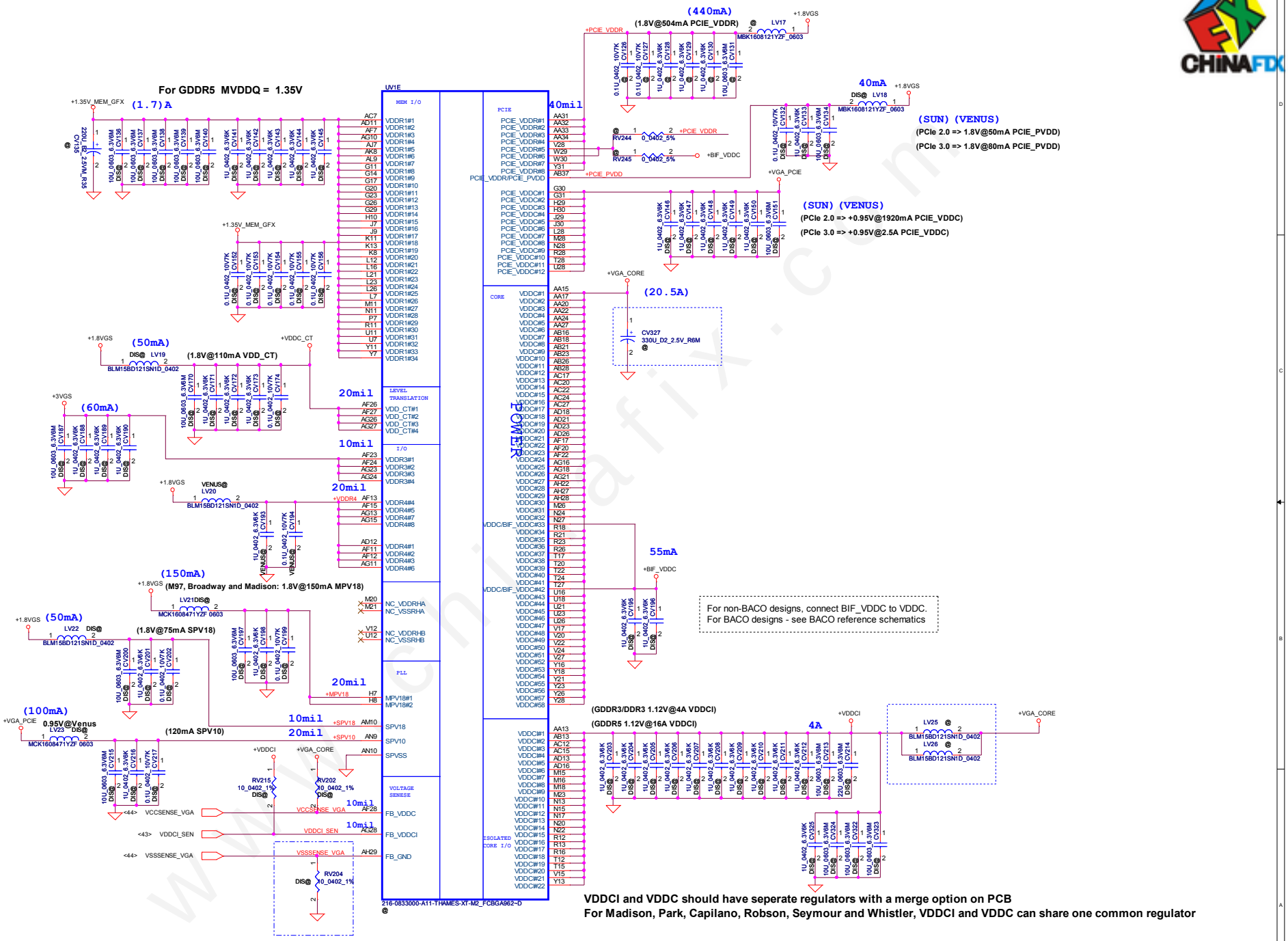
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: ATI_Venus Pro_M2_PWR_GND

Size: | Document Number: LA-9982P | Rev: 3.0

Date: Wednesday, May 29, 2013 | Sheet 51 of 57



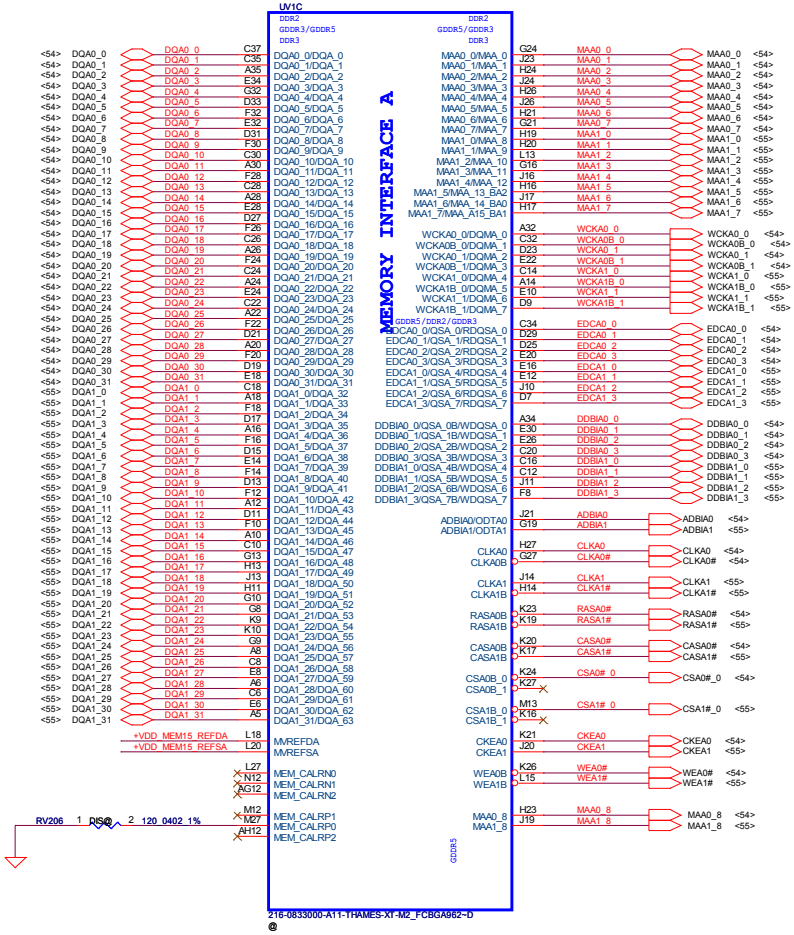
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: ATI_Venus Pro_M2_Power

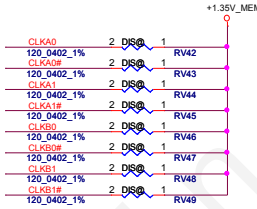
Size	Document Number	Rev
	LA-9982P	3.0

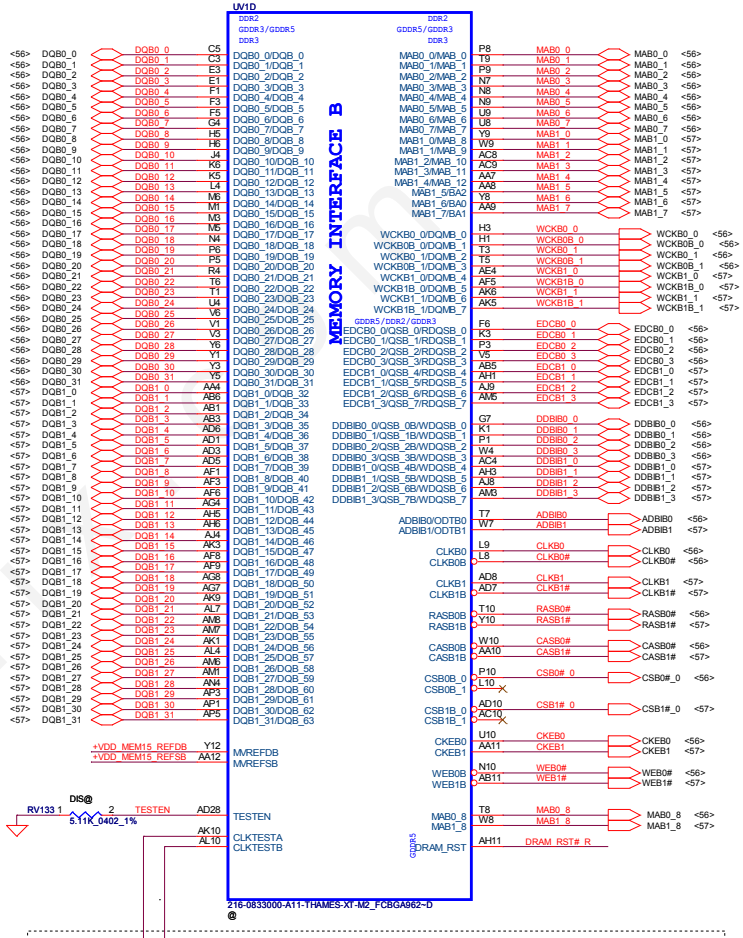
Date: Wednesday, May 29, 2013 Sheet 52 of 57



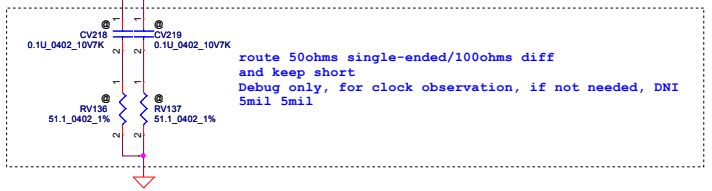
GDDR5 CMD Mapping Table

<0..31>	<32..63>	Memory
CMD12	CMD28	RAS#
CMD15	CMD31	CAS#
CMD5	CMD21	WE#
CMD0	CMD16	CS#
CMD8	CMD24	ABI#
CMD10	CMD26	A0_A10
CMD11	CMD27	A1~A9
CMD2	CMD18	A2~BA0
CMD1	CMD17	A3~BA3
CMD3	CMD19	A4~BA2
CMD4	CMD20	A5~BA1
CMD7	CMD23	A6~A11
CMD6	CMD22	A7~A8
CMD9	CMD25	A1Z_FRU
CMD14	CMD30	CKE#
CMD13	CMD29	RESET#

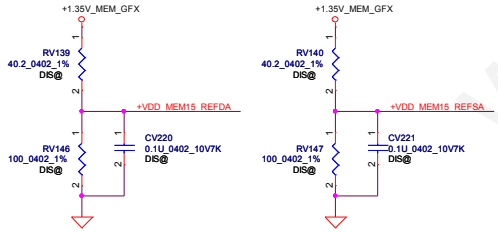


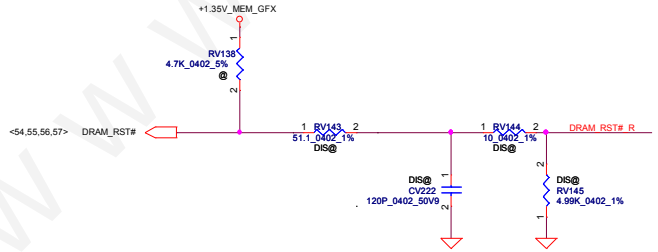


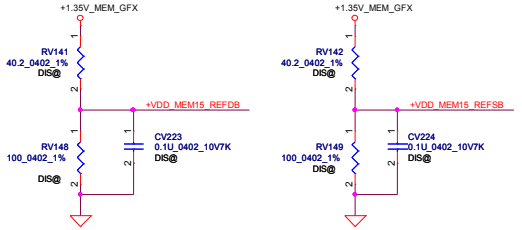
This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2



route 50ohms single-ended/100ohms diff and keep short
Debug only, for clock observation, if not needed, DNI 5mil 5mil







Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

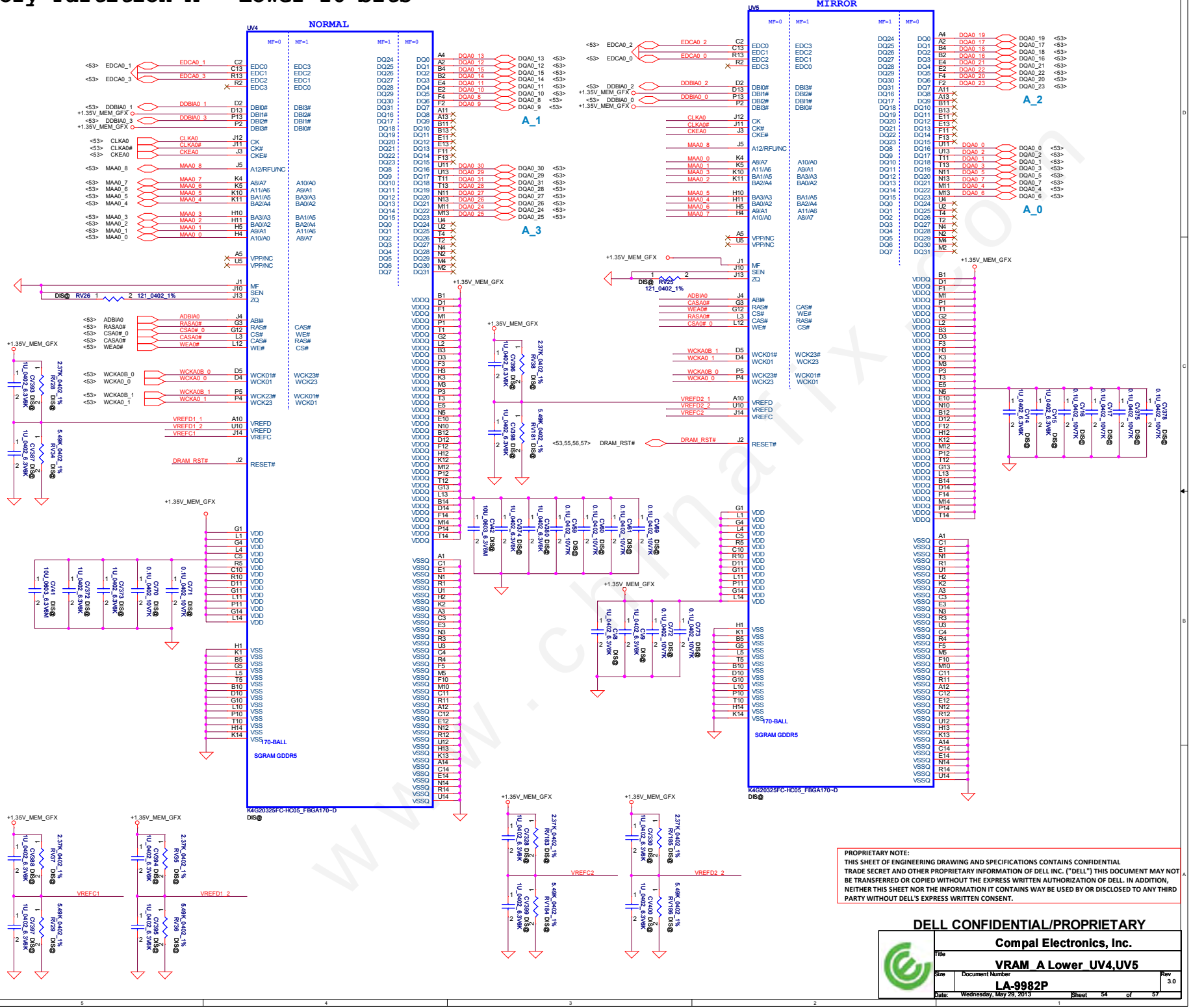
Title: ATI_Venus Pro_M2_MEM IF

Size	Document Number	Rev
	LA-9982P	3.0

Date: Wednesday, May 29, 2013 Sheet 53 of 57

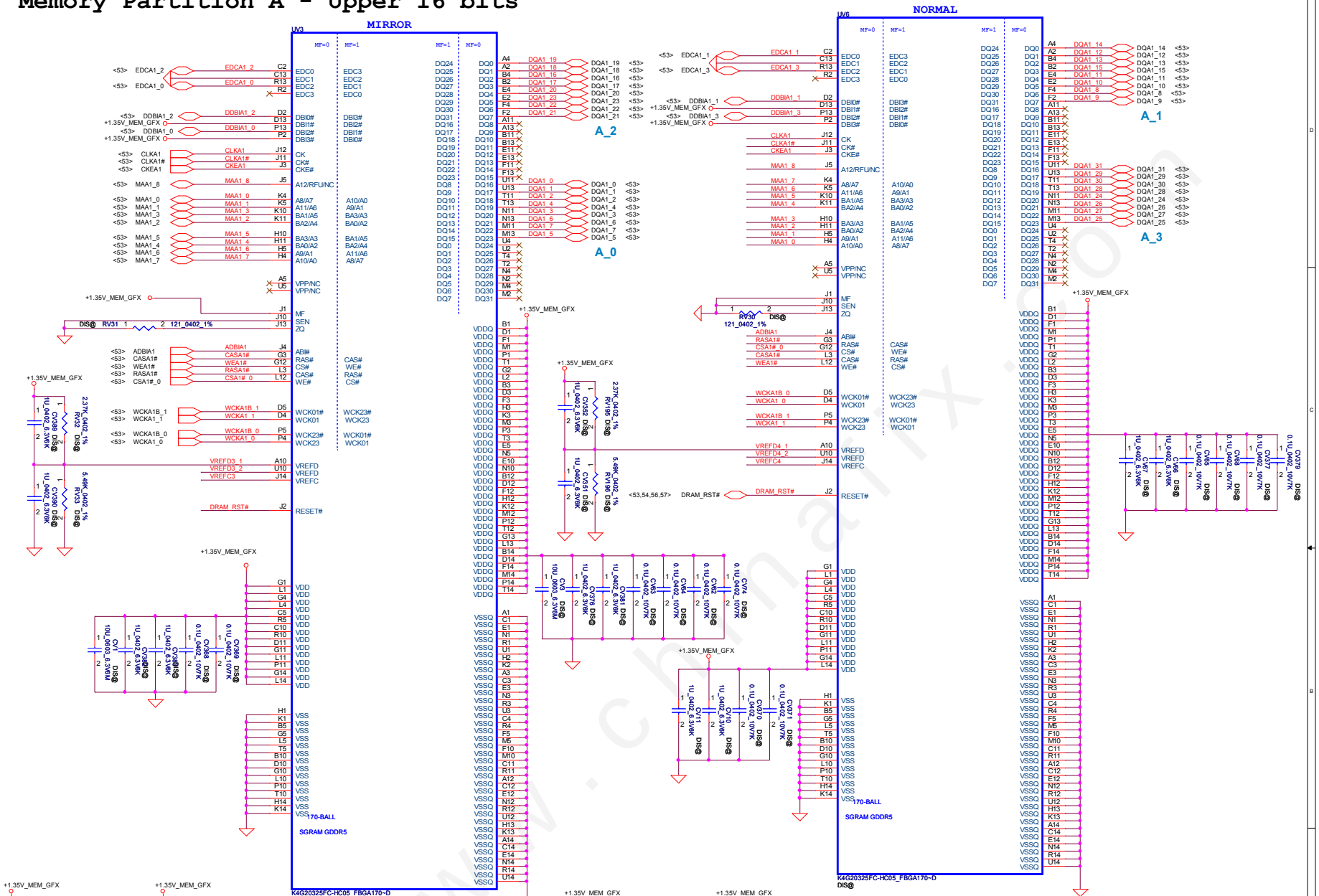
Memory Partition A - Lower 16 bits

64X32 GDDR5



Compal Electronics, Inc.		
Title: VRAM_A Lower_UV4,UV5		
Size	Document Number: LA-9982P	Rev: 3.0
Date: Wednesday, May 29, 2013	Sheet 54 of 57	

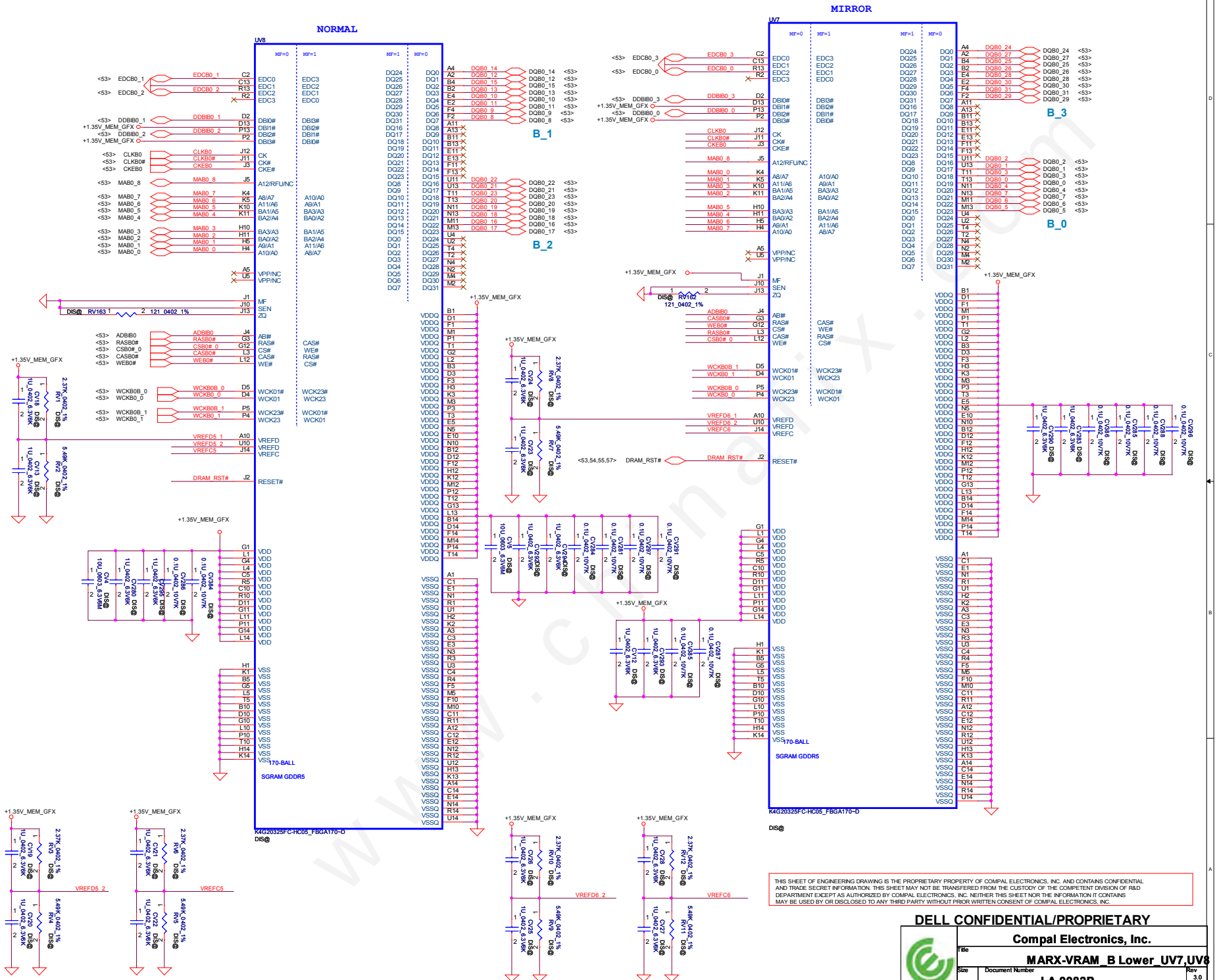
Memory Partition A - Upper 16 bits



Compal Electronics, Inc.

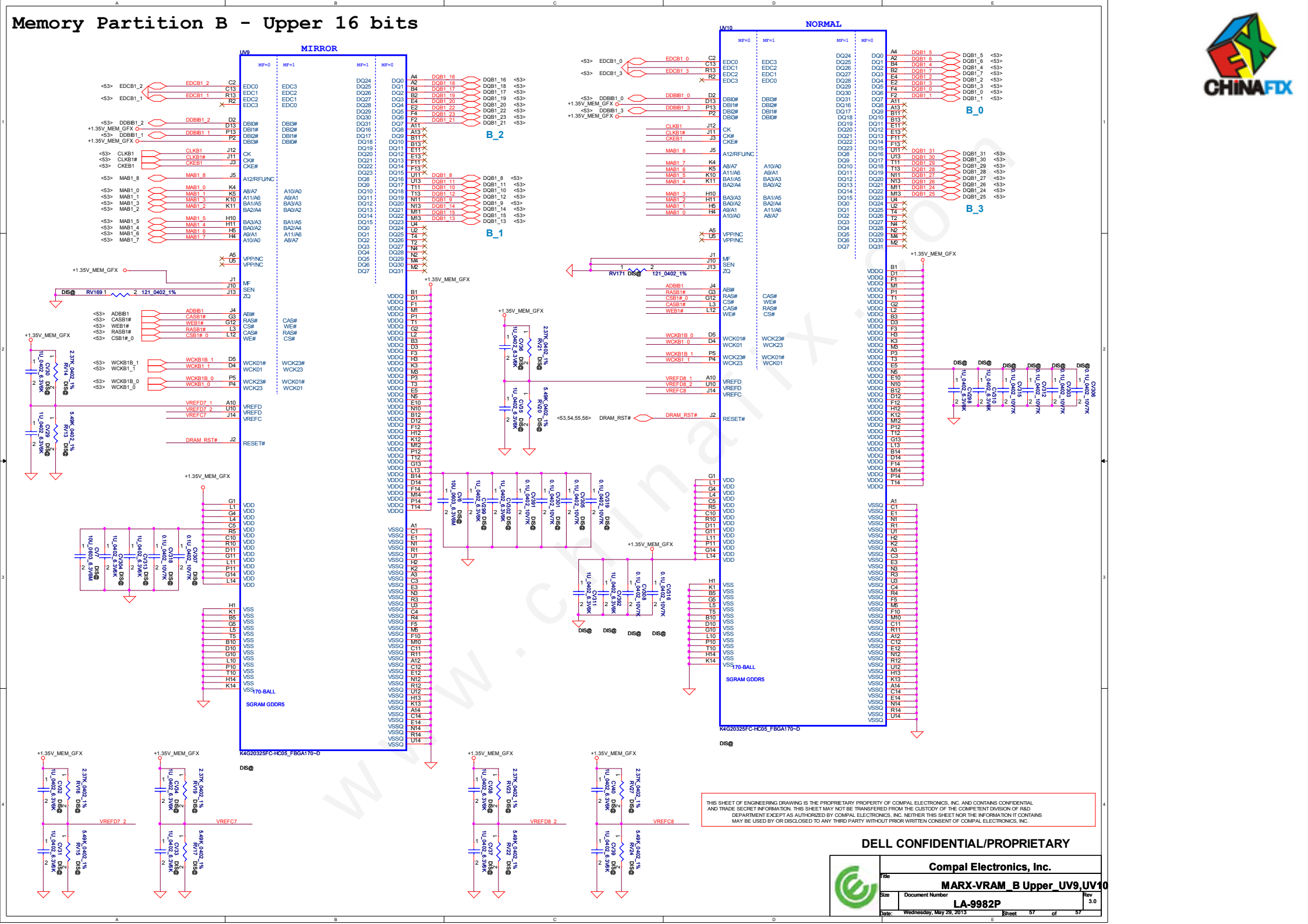
Title	MARX-VRAM_A Upper_UV3,UV6	
Size	Document Number: LA-9982P	Rev: 3.0
Date: Wednesday, May 29, 2013	Sheet 55 of 57	

Memory Partition B - Lower 16 bits



Compal Electronics, Inc.	
Title	MARX-VRAM_B Lower_UV7,UV8
Size	Document Number: LA-9982P
Rev	3.0
Date:	Wednesday, May 29, 2013
Sheet	56 of 57

Memory Partition B - Upper 16 bits



Compal Electronics, Inc.

Title	MARX-VRAM_B Upper_UV9,UV10	
Size	Document Number: LA-9982P	Rev: 3.0
Date: Wednesday, May 29, 2013	Sheet 57 of 57	